Course ID: ECE 522 Hardware/Software Codesign with FPGAs

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Course Description

This course provides an introduction to the design of electronic systems that incorporate both hardware (HW) and software (SW) components. Students are exposed to hardware-software codesign concepts using a commercial computer-aided design (CAD) tool called Xilinx Vivado and an FPGA system-on-chip (SoC) hardware architecture. Dataflow models are discussed as a state-of-the-art methodology to solve codesign problems and to optimize the balance between software, e.g., written in C, and hardware, e.g., described in a hardware description language (HDL) such as VHDL or verilog. Students gain experience in translating between software and hardware descriptions through laboratory and project assignments. A broad range of system architectures are described, as well as the trade-offs associated with choosing one architecture over another. Students develop a fundamental understanding of state-of-the-art practices in developing codesign solutions to problems that prepare them well for industrial and academic careers in this field.

Course Goals

The goal of this course is to enable you to analyze a C code implementation of an algorithm, translate it into a concurrent specification and then map in onto an SoC architecture such that some components execute on a microprocessor while others execute directly in the hardware. In order to be effective, you will need to be able to translate between C code and a HDL, be aware of the options and trade-offs among various system architectures, have knowledge of state-of-the-art codesign methodologies and have hands-on experience working with commercial CAD tools.

NOTE This is a laboratory/project based course. Most of your learning will take place as you complete the laboratory and project assignments. The lecture material is supplemental to your learning, i.e., you should become familiar with the tools and techniques described in the lecture material, assimilate and apply those techniques as needed to complete the laboratory and project assignments. This is a graduate course and therefore, I will expect you to evaluate the problems,

decide on which tools/techniques are relevant and useful for the task, and then adapt and apply them to derive a solution.

Course Objectives/Learning Outcomes

- **C1 (Concurrent Specification):** Define a concurrent specification from an algorithm, analyze its behavior and partition the specification into software (C code) and hardware (HDL) components.
- **C2 (Codesign Architectures):** Describe the broad range of system architectures that currently exist and define their fundamental attributes including speed, energy, area, design complexity, design cost, etc.
- **C3 (CAD Tools):** Demonstrate the ability to translate between C code and VHDL by solving meaningful, real-world problems and then implementing and testing your solution on a FPGA SoC architecture.

Technical Goals

- An important component of Computer Engineering is becoming fluent with Computer-Aided Design tools, such as Xilinx Vivado and Cadence Virtuoso. This course will introduce you to Vivado, which will be used in combination with other software programming tools such as C and high-level synthesis (HLS).
- Hardware-software codesign is focused on the design and implementation of systems which have components that run in both software and hardware. A key skill to designing such systems is being able to partition and translate between C programs and VHDL or HLS. This course will provide guidance and hands-on exercises to give students experience in carrying out software-hardware codesign activities using a FPGA as a base platform.
- Proficiency in hardware-software codesign requires a broad knowledge of the variety of system architectures available commercially for system implementations, and an in-depth awareness of the trade-offs among system attributes including performance, speed, energy, area, design complexity and design cost trade-offs. This course will provide instruction on commercially available system platforms and their applicability to modern microelectronic systems including automotive, industrial control and emerging Internet-of-Things (IoT) applications.

Technical Skills

In order to participate and succeed in this class, you will need to be able to perform the following basic technical tasks:

- Use UNM Learn.
- Use email, including attaching files, opening files, downloading attachments and open a hyperlink.
- Use a word processor to create homework, laboratory and project reports. NOTE: YOU MUST ONLY SUBMIT TXT and/or PDF files. WORD, EXCEL or other types of word processing formats will NOT be accepted.
- Create and upload PDF files.
- Work within a Linux operating system environment, e.g., have knowledge of basic commands including file and directory operations, of software for editing files, of networking concepts, e.g., setting static IPs, configuring routers, etc.
- Have experience with writing, compiling and debugging C programs.
- Have experience with the VHDL hardware description language and hardware system design concepts, e.g., logic gates, state machines with data paths, etc.

- Install and use computer-aided design (CAD) tools and be familiar with the concepts of logic synthesis, place and route, simulation and timing closure.
- Connect, configure and carry out hardware demonstrations on FPGAs, e.g., powering up an FPGA board, connecting ethernet and USB cables to computers and routers, running serial and network communication and file transfer programs.

Supplemental documentation is provided for computer management tasks

Course Requirements

Students are expected to view the video lectures covering the technical topics, take the quizzes and complete the reading, laboratory and project assignments. This course includes one mid-term exam. There is no final exam, instead students are expected to complete a final project and perform a hardware demonstration.

Technical Requirements

Computer

- A high speed Internet connection is highly recommended.
- Supported browsers include: Internet Explorer, Firefox, and Safari. Detailed Supported Browsers and Operating Systems: http://online.unm.edu/help/learn/students/
- Any computer capable of running a recently updated web browser should be sufficient to access your online course. However, bear in mind that processor speed, amount of RAM and Internet connection speed can greatly affect performance. Many locations offer free high-speed Internet access including UNM's Computer Pods.
- For using the Kaltura Media Tools inside Learn, be sure you have downloaded and installed the latest version of Java, Flash, and Mozilla Firefox. They may not come preloaded.
- Microsoft Office products are available free for all UNM students (more information on the UNM IT Software Distribution and Downloads page: http://it.unm.edu/software/index.html)

For UNM Learn Technical Support: (505) 277-0857 (24/7) or use the "Create a Support Ticket" link in your course.

Textbook and Supplemental Materials

- "A Practical Introduction to Hardware/Software Codesign", Patrick Schaumont, Springer, 2010, ISBN 978-1-4614-3736-9 and ISBN 978-1-4614-3737-6 (eBook)

Required Supplementary Materials

- Students will be required to setup an account with Xilinx (www.xilinx.com) as a mechanism to download the Vivado software tool. A free license will be provided by Xilinx.
- Students will be required to buy an FPGA board (at an academic discount price) as covered in the laboratory introductory video(s).

Coursework and Deadlines

Weekly Schedule

- Each module will be covered in 1 week, e.g., Module 1 in week 1, etc.
- All screen casts will be followed by a quiz. Quizzes corresponding to a module MUST be completed in order, and by Sunday at 11pm.

- Laboratory reports and the project report must be submitted by Sunday, by 11pm the week they are assigned.
- The midterm will be a 2-hour timed exam.

Every effort will be made to answer student questions within 2 days, and to report grading to students within 1 week of the submission deadline.

Class Effort and Expectations

Please plan on devoting approx. 15 hour per week to cover the lecture material, participate in discussions and to do the homework, laboratories and project. Your previous coursework using VHDL necessarily exposed you to CAD tools such as Vivado. However, if your experience is limited, please plan on spending additional time beyond the 15 hours per week. This course is 8 weeks long and therefore, runs at twice the pace of a regular course. Therefore, 15 hours may sound like a lot but we'll need to cover 16 weeks of material in 8 short weeks. Other requirements to consider:

- Students are expected to learn how to navigate in UNM Learn.
- Students are expected to communicate with one another on laboratory and project assignments.
- Students are expected to keep abreast of course announcements.
- Students are expected to use the Learn course email as opposed to a personal email address.
- Students are expected to keep instructor informed of class related problems, or problems that may prevent the student from full participation.
- Students are expected to address technical problems immediately.
- Students are expected to observe course netiquette at all times.

Grading Procedures

All homeworks, laboratories and the project are designed to be tied directly to the core material in this course. Becoming efficient at codesign requires hands-on experience, i.e., lecture material is important but most of your learning will occur while designing solutions, testing them through simulation and hardware experiments, and examining how the tools synthesize designs to implementations. Therefore, a large portion of the grade is allocated to labs and projects, as shown below. All exams will be take-home.

Grading Policy

I will accept late work but please submit your initial attempt by the indicated times. Late work will be automatically be assigned half-credit if submitted after the deadline, so turn in whatever you can before the deadline. Also, all the work in this class is cumulative so if you fall behind, it will be very hard for you to catch up.

If you anticipate difficulty in meeting a deadline, you need to notify me at least 1 day in advance of the deadline and be prepared to provide evidence explaining why you will be late.

All written work needs to be submitted online. If you have difficulty using a tool to complete work, use the "Create a Support Ticket" link in the Course Menu and immediately notify me of your difficulties.

Grading Distribution and Description

The distribution of weights for the exams, laboratories and projects is as follows:

Midterm	30%
Laboratories	30%
Project	30%
Participation (5%) and Quizzes (5%)	10%

Midterm Exam: The mid-term exam consists entirely of short answer types of questions. A sample exam is provided to enable students to be prepared for the type of questions they will be expected to answer. Your written answers will be assessed according to the level of understanding that you have of the subject matter, i.e., primarily on the correctness of your answer, but also on the conciseness of your answer. Focus on answering the question and avoid writing 'everything you know' about the topic. The exam is designed to give you enough time to write concise answers to the questions.

Laboratories: Students purchase an FPGA board at the beginning of the course and work through a series of laboratories to become familiar with the process of creating programming bitstreams for the FPGA using computer-aided design tools, e.g., Xilinx Vivado. There are 3 laboratories, but the first lab, called Lab #0, consists of 10 parts. Lab #0 is designed 1) to train you on the use of the Vivado, 2) to give you exposure to FPGAs and embedded system development, and 3) to introduce you to important codesign concepts as they manifest in commerical CAD tool environments. The two remaining laboratories (and project) are designed to give you experience solving actual problems. The laboratory reports are graded according to the rubrics defined below.

Project: Students will work in groups of two to implement and hardware-software codesign version of an algorithm. The algorithm is drawn from state-of-the-art practice in another discipline, e.g., machine learning algorithms such as K-means or one of several recent post-quantum cryptographic algorithms. The C code for the algorithm is provided. Students are required to obtain some domain knowledge of the problem being solved through research papers provided by the instructor, and then need to develop a solution that partitions the algorithm in the software and hardware components. The software components will continue to execute as a C program while the hardware components of the algorithm are to be mapped into VHDL and synthesized onto an FPGA. A project hardware demonstration and a project report are used to assess the student's mastery of the codesign process. The project report is graded according to the rubrics defined below.

Discussions: Every module will include a 'Questions' discussion forum. Students are expected to participate actively in discussions by asking and answering questions that other students or the instructor posts. Participation in question and answer discussion forums represent the main component of the 'Participation' component of your grade. At least one post which asks a question, provides a comment or an answer to another student's question is required from each student in each of the 8 modules in order to receive 3% of the 5% allocated for participation. Student engagement will be monitored by the instructor and exceptional interaction will be rewarded with full credit of %5.

Participation: Tracking Course Activity UNM Learn automatically records all students' activities including: your first and last access to the course, the pages you have accessed, the number of discussion messages you have read and sent, discussion text and posted discussion topics. This

data can be accessed by the instructor to evaluate class participation and to identify students having difficulty.
Summary of Course Work: There are a total of 12 laboratories, with the individual parts of lab #0 counting as 10 of them. Each laboratory is considered an 'Assignment' and requires a laboratory report. You are also expected to participate in all 8 discussion forums, one within each of the 8 modules. The mid-term and final project are also components of the required work in this course.

No incompletes will be given, except as required by university policy for truly exceptional circumstances.

Cheating at any time in this course will cause you to fail the course.
For a complete description of academic dishonesty, refer to the UNM Student Handbook.

Laboratory and Project Rubrics

- 20% Description
  Does the report minimally include the following components: title, introduction to the lab that describes the problem to be solved, a body section that shows how the problem was solved (with schematic and supporting waveforms, if needed), and concluding remarks on the results and the student's experience?
- 20% Correctness
  Is the problem solved correctly?
- 20% Completeness
  Are all the steps needed to solve the problem explicitly shown. For example, are the schematic diagram and the boolean equations given? Is the code given? Are the waveforms given? Are there comments in the Verilog code? Depending on the requirements given in the lab description, some of these components are not needed.
- 20% Clarity/Conciseness
  Are the description and results clearly and concisely presented or is there unnecessary clutter or redundancy?
- 20% Quality of write-up
  Is the lab report easy to read? Are the figures, plots, etc. neatly and professionally presented, i.e., in electronic form with arrows and text explaining the important features? Is the information on the title page complete, with a meaningful title and the student's name.

Grading Scale

A+	(97-100)
A	(93-96)
A-	(90-92)
B+	(87-89)
B	(83-86)
B-	(80-82)
C+	(77-79)
C	(73-76)
C-	(70-72)
D+	(67-69)
D	(63-66)
D-	(60-62)
F	(0-59)

Schedule of Activities

Week(1): Introduction
Week(2): Introduction and DataFlow
Week(3): DataFlow Models
Week(4): DataFlow Implementations
Week(5): FSMD
Week(6): Control and DataFlow Analysis I
Week(7): Control and DataFlow Analysis II
Week(8): Project

Netiquette

- In following with the UNM Student Handbook, all students will show respect to their fellow students and instructor when interacting in this course. Take Netiquette suggestions seriously. Flaming is considered a serious violation and will be dealt with promptly. Postings that do not reflect respect will be taken down immediately.
- This course encourages different perspectives related to such factors as gender, race, nationality, ethnicity, sexual orientation, religion, and other relevant cultural identities. The course seeks to foster understanding and inclusiveness related to such diverse perspectives and ways of communicating.
- Link to Netiquette document: http://online.unm.edu/help/learn/students/pdf/discussion-netiquette.pdf

UNM Policies

Title IX: Gender Discrimination

In an effort to meet obligations under Title IX, UNM faculty, Teaching Assistants, and Graduate Assistants are considered "responsible employees" by the Department of Education (see page 15 - http://www2.ed.gov/about/offices/list/ocr/docs/qa-201404-title-ix.pdf). This designation requires that any report of gender discrimination which includes sexual harassment, sexual misconduct and sexual violence made to a faculty member, TA, or GA must be reported to the Title IX Coor-

dinator at the Office of Equal Opportunity (oeo.unm.edu). For more information on the campus policy regarding sexual misconduct, see: https://policy.unm.edu/university-policies/2000/2740.html

Copyright Issues

All materials in this course fall under copyright laws and should not be downloaded, distributed, or used by students for any purpose outside this course.

Accessibility

The American with Disabilities Act (ADA) is a federal anti-discrimination statute that provides comprehensive civil rights protection for persons with disabilities. Among other things, this legislation requires that all students with disabilities be guaranteed a learning environment that provides for reasonable accommodations of their disabilities. If you have a disability requiring accommodation, please contact the UNM Accessibility Resource Center in 2021 Mesa Vista Hall at 277-3506 or http://as2.unm.edu/index.html. Information about your disability is confidential.

- Blackboard's Accessibility statement: http://www.blackboard.com/accessibility.aspx

Academic Misconduct

You should be familiar with UNM's Policy on Academic Dishonesty and the Student Code of Conduct (http://pathfinder.unm.edu/code-of-conduct.html) which outline academic misconduct defined as plagiarism, cheating, fabrication, or facilitating any such act.

Drop Policy

UNM Policies: This course falls under all UNM policies for last day to drop courses, etc. Please see http://www.unm.edu/studentinfo.html or the UNM Course Catalog for information on UNM services and policies. Please see the UNM academic calendar for course dates, the last day to drop courses without penalty, and for financial disenrollment dates.

UNM Resources

CAPS Tutoring Services http://caps.unm.edu/programs/online-tutoring/
CAPS is a free-of-charge educational assistance program available to UNM students enrolled in classes. Online services include the Online Writing Lab, Chatting with or asking a question of a Tutor.

Embedded Tutor - if this course has a tutor assigned, substitute the following:
This course has tutoring services incorporated into the course. Please see the "CAPS Tutor" link in the course menu on the left for more details.

UNM Libraries http://library.unm.edu

Student Health & Counseling (SHAC) Online Services
http://online.unm.edu/help/learn/support/shac