Course Objectives/Learning Outcomes

- **C1 (Concurrent Specification):** Define a concurrent specification from an algorithm, analyze its behavior and partition the specification into software (C code) and hardware (HDL) components.
- **C2 (Codesign Architectures):** Describe the broad range of system architectures that currently exist and define their fundamental attributes including speed, energy, area, design complexity, design cost, etc.
- **C3 (CAD Tools):** Demonstrate the ability to translate between C code and VHDL by solving meaningful, real-world problems and then implementing and testing your solution on a FPGA SoC architecture.

Module 1: Start Here and Introduction

Learning Objectives	Activities	Materials	Course Objective Alignment
Describe the nature of this course	Watch Intro to 'Hardware-Software Codesign with FPGAs' video	Video	
Demonstrate proficiency with UNM Learn Describe the course learning objectives	Review syllabus and course schedule	UNM Learn, Documentation	
	Email Dr. Plusquellic	UNM Learn, Email	
	Setup Digilent and Xilinx accounts	Web	
	Post an introduction on Discussion board	UNM Learn, Discussion board	
	Complete practice assignment	UNM Learn, Assignment submission	
	Complete Welcome Survey	UNM Learn, Survey	
	Review Learn Tools and Tips	UNM Learn, Documentation	
Describe important differences between hardware (HW) and software (SW)	This is a laboratory/project based course. You will be assessed on these learning objectives on the mid-term exam and Project. The quizzes will evaluate only your familiarity with these concepts.	Screencasts and lecture slides	C1
Name and summarize the five elements which characterize the Codesign space			C2
Describe the steps of the Codesign process			C1
	Lab 0: Part 1, Install Vivado on your laptop	Screen casts, laptop and Xilinx CAD tools	C1
Demonstrate skills in creating a project with the Xilinx Vivado CAD tool	Lab 0: Part 2: Use Xilinx Vivado CAD GUI to create a project		C3
Demonstrate knowledge of carrying out behavioral synthesis within Vivado	Lab 0: Part 3: Construct a simple VHDL design in Vivado and synthesize it		C3
	Discussion: Questions about module	UNM Learn, Discussion board	

Module 2: Introduction and Data Flow

Learning Objectives	Activities	Materials	Course Objective Alignment
Describe the dualistic relationship between hardware (HW) and software (SW)	This is a laboratory/project based course. You will be assessed on these learning objectives on the mid-term exam and Project. The quizzes will evaluate only your familiarity with these concepts.	Screencasts and lecture slides	C1
Distinguish between concurrency and parallelism			C1
Describe the role of the block diagram in DataFlow processes			C1
Name the benefits of a concurrent specification			C1
Distinguish between DataFlow models and C programs			C1
Demonstrate the ability to draw DataFlow diagrams with actors, queues, markings and firing rules			C1
Demonstrate knowledge of using Vivado to program the FPGA and perform a hardware demonstration	Lab 0: Part 4: Program the board and create a snapshot of your hardware demo of Even Detector	Screen casts, laptop and Xilinx CAD tools	C3
Describe important SoC concepts as they relate to Vivado	FPGA board exploration		C2
Create block diagrams with Vivado	Lab 0: Part 5: Create a Screen Snapshot of Vivado after you have create the GPIO BRAM block diagram		C3
	Discussion: Questions about module	UNM Learn, Discussion board	

Module 3: DataFlow Models

Learning Objectives	Activities	Materials	Course Objective Alignment
Derive a Synchronous DataFlow (SDF) graph and periodic admissible schedule (PASS) that implements a concurrent specification of an algorithm	This is a laboratory/project based course. You will be assessed on these learning objectives on the mid-term exam and Project. The quizzes will evaluate only your familiarity with these concepts.	Screencasts and lecture slides	C1
Name and discuss SDF limitations and extensions to overcome them			C1
Evaluate the performance of DataFlow graphs (DFGs) and describe four performance enhancing transformations			C1
Design register transfer level (RTL) and finite state machine (FSM) solutions for a concurrent specification of an algorithm			C1
Implement a SoC design using an illustrative example	VHDL instruction	Screencasts and lecture slides	C2
Construct an FSM in VHDL			C2
Create the hardware component of a codesign project within Vivado	Lab 0: Part 6: Create the design_1_wrapper.vhd file and a Screen Snapshot of Vivado after you have successfully synthesized the GPIO BRAM project	Screen casts, laptop and Xilinx CAD tools	C3
	Discussion: Questions about module	UNM Learn, Discussion board	

Module 4: Data Flow Implementations

Learning Objectives	Activities	Materials	Course Objective Alignment
Translate a DFG to software implemented using a static or dynamic schedule	This is a laboratory/project based course. You will be assessed on these learning objectives on the mid-term exam and Project. The quizzes will evaluate only your familiarity with these concepts.	Screencasts and lecture slides	C1
Write a C code implementation of a DFG with actors and queues			C1
Describe the performance trade-offs between static and dynamic schedules			C1
Translate a DFG into a hardware implementation with pipelining			C2
Implement a C application using SDK	Lab 0: Part 7: Create a Screen Snapshot of SDK after you have created the application	Screen casts, laptop and Xilinx CAD tools	C3
Perform a hardware demonstration of the GPIO BRAM project	Lab 0: Part 8: Create a Screen Snapshot of the output after you have run the GPIO BRAM application on the Zybo board		C3
	Discussion: Questions about module	UNM Learn, Discussion board	

Module 5: FSMD

Learning Objectives	Activities	Materials	Course Objective Alignment
Describe the process of creating a finite state machine with datapath (FSMD) from a C program	This is a laboratory/project based course. You will be assessed on these learning objectives on the mid-term exam and Project.	Screencasts and lecture slides	C3
Write the VHDL that implements an FSMD			C3
Create an algorithmic state machine with datapath (ASMD) from C code or an FSMD	Lab #0: Part 9: Finish the ASMD Diagram for HISTO	Screen casts, laptop and Xilinx CAD tools	C3
Analyze performance of a HW/SW implementation on an FPGA	Lab #0: Part 10: Create a Screen Snapshot of the output after you have run the HISTO application on the Zybo board		C2
	Midterm exam	UNM Learn	
	Discussion: Questions about module	UNM Learn, Discussion board	

Module 6: Control and Data Flow Analysis I

Learning Objectives	Activities	Materials	Course Objective Alignment
Perform a control and data flow analysis on a C program	You will be assessed on these learning objectives in Lab #1 and in the Project. The quizzes will evaluate only your familiarity with these concepts.	Screencasts and lecture slides	C1
Analyze the behavior of control flow graphs (CFGs) and data flow graphs (DFGs)			C1
Map C programming constructs into CFGs and DFGs			C1
Compose and modify a VHDL description	Lab #1: Add a module to the HISTO project that computes pairwise differences from the data values stored in the BRAM	Screen casts, laptop and Xilinx CAD tools	C1 and C3
	Discussion: Questions about module	UNM Learn, Discussion board	

Module 7: Control and Data Flow Analysis II

Learning Objectives	Activities	Materials	Course Objective Alignment
Translate a C program into a FSMD using a standard methodology	This is a laboratory/project based course. You will be assessed on these learning objectives in Lab #2 and in the Project. The quizzes will evaluate only your familiarity with these concepts. You should leverage the tools and techniques covered in the lectures and laboratories to complete the Project assignment.	Screencasts and lecture slides	C3
Construct a hardware datapath from a C program			C2
Create the finite state machine that correctly implements the CFG for the C program			C3
Appy an optimization technique to improve hardware performance			C1
Use Xilinx's High Level Synthesis (HLS) tool to implement a codesign system	Lab #2: Run Vivado High Level Synthesis (HLS) on the LFSR_11Bit design, and add the automatically generated FSMD to your lab#1 project	Screencasts, laptop and Xilinx CAD tools	C3
Putting it all together: Design a solution to a HW/SW codesign problem working together on a team	Project: Create a Hardware-Software Codesign version of the k-mean clustering algorithm	Laptop and Xilinx CAD tools	C1, C2 and C3
	Discussion: Questions about module	UNM Learn, Discussion board	

Module 8: Project

Learning Objectives	Activities	Materials	Course Objective Alignment
Putting it all together: Design a solution to a HW/SW codesign problem working together on a team	This is a laboratory/project based course. You should leverage the tools and techniques covered in the lectures and laboratories to complete the Project assignment. Project: Create a Hardware-Software Codesign version of the k-mean clustering algorithm	Laptop and Xilinx CAD tools	C1, C2 and C3
	Discussion: Group discussions about project	UNM Learn, Discussion board	