Course Outline:

Module	Date	Lecture
"START HERE" Module 1	Oct. 14 - Oct. 20	Introduction I and II Vivado Installation, Create Project, Vivado Synthesis (Lab #0, Parts 1, 2 and 3), All assignments due on the last day of the week by 11pm.
Module 2	Oct. 21 - Oct. 27	Introduction III, Data Flow I Hardware Demo, Vivado SoC Programming Concepts and Block Diagram, (Lab #0, Parts 4 and 5)
Module 3	Oct. 28 - Nov. 3	Data Flow II and III Adding Custom VHDL to the Block Diagram, FSM I and II (Lab #0, Part 6)
Module 4	Nov. 4 - Nov. 10	DataFlow Software Implementation I and II DataFlow Hardware Implementation I Vivado SDK I and II (Lab #0, Parts 7 and 8)
Module 5	Nov. 11- Nov. 17	Midterm FSMD I (Lab #0, Parts 9 and 10)
Module 6	Nov. 18 - Nov 24	Control Flow and Data Flow Analysis I Lab #1
Module 7	Nov. 25 - Dec. 1	Control Flow and Data Flow Analysis II Lab #2, Due. Oct. 7, and Project
Module 8	Dec. 2 - Dec. 14	Project

Changes/Additions to this schedule will be posted as needed throughout the term