SSD1298
Application Note

240 RGB x 320 TFT LCD Controller Driver

Integrated Power Circuit, Gate and Source Driver

with built-in RAM

Prepared by : CY Ng

Ver 1: New release – 5 Dec 2007
Ver 2: Added PVI 2.6" and AUO 2.4" and VCI connection – 14 Dec 2007

Table of content

Capacitor Function

CYP/CYN capacitor is VCIX2 booster capacitor

CXP/CXN capacitor is VCIM booster

C1P/C1N and C2P/C2N capacitors are VGH booster. C1P/C1N is the primary booster.

C3P/C3N capacitor is VGL booster.

The voltage rating of C2P/C2N and C3P/C3N need to set up to 16V as VGH and VGL are over +/-10V.

C1P/C1N can be 10V rating since it is primary booster capacitor.

Recommend capacitor value and rating.

1. VCIX2 = 2.2uF/10V

2. C2P/C2N and C3P/C3N = 0.1uF / 16V.

3. CDUM0 (Pin 5-7) is a charge sharing pin. A 1uF capacitor connect to Vss can enable the charge sharing function.

   The current consumption can be reduced by 1mA at 2.8V operation

4. All other capacitors 1.0uF ~ 2.2uF
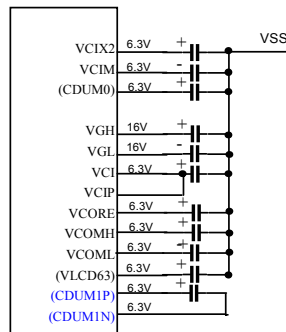
Recommend connection in VCI pin

All VCI pins (P210-226) are suggested to connect together and provide power.

- all those VCI are power source for VCIX2, VGH and analog voltage.

- recommended connection can help to improve VCIX2 strength.
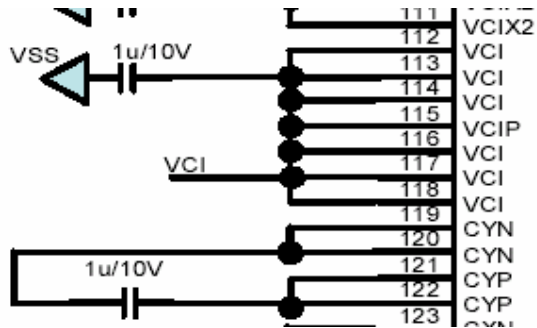
Application FPC Circuit

1.1 AUO 2.8' Panel

PS3 PS2 PS1 PS0	MODE
0 0 1 0	16 Bit 8080 Parallel
0 0 1 1	8 Bit 8080 Parallel
1 0 1 0	18 Bit 8080 Parallel

1.1.1 AUO 2.8' initial code

```
void SSD1298_AUO28_Init(void)
{
// VCI=2.8V
//************* Reset LCD Driver ***************//
LCD_RESET_signal = 1;
delayms(1); // Delay 1ms
LCD_RESET_signal = 0;
delayms(10); // Delay 10ms    // Reset duration
LCD_RESET_signal = 1;
delayms(50); // Delay 50 ms
//************* Start Initial Sequence *********//
LCD_Send_SSD1298(0x0000, 0x0001); // Start internal OSC.
LCD_Send_SSD1298(0x0001, 0x333F); // Driver output control, RL=0;REV=1;GD=1;BGR=0;SM=0;TB=1
LCD_Send_SSD1298(0x0002, 0x0600); // set 1 line inversion
//************* Power control setup ***********//
LCD_Send_SSD1298(0x000C, 0x0007); // Adjust VCIX2 output voltage
LCD_Send_SSD1298(0x000D, 0x0006); // Set amplitude magnification of VLCD63
LCD_Send_SSD1298(0x000E, 0x3000); // Set alternating amplitude of VCOM
LCD_Send_SSD1298(0x001E, 0x00B8); // Set VcomH voltage
LCD_Send_SSD1298(0x0003, 0x6A64); // Step-up factor/cycle setting
//************* Turn On display ****************//
LCD_Send_SSD1298(0x0010, 0x0000); // Sleep mode off.
delayms(30); // Wait 30mS
LCD_Send_SSD1298(0x0011, 0x4870); // Entry mode setup. 262K type B, take care on the data bus with 16it only
LCD_Send_SSD1298(0x0007, 0x0033); // Display ON
//************* LCD driver AC setting ***************//
LCD_Send_SSD1298(0x0025, 0x8000); // Frame freq control, 65Hz
LCD_Send_SSD1298(0x000B, 0x5308); // Frame cycle control, POR setting
//************* RAM position control **********//
LCD_Send_SSD1298(0x000F, 0x0000); // Gate scan position start at G0.
LCD_Send_SSD1298(0x0044, 0xEF00); // Horizontal RAM address position
LCD_Send_SSD1298(0x0045, 0x0000); // Vertical RAM address start position
LCD_Send_SSD1298(0x0046, 0x013F); // Vertical RAM address end position
// ----------- Adjust the Gamma Curve ----------//
```
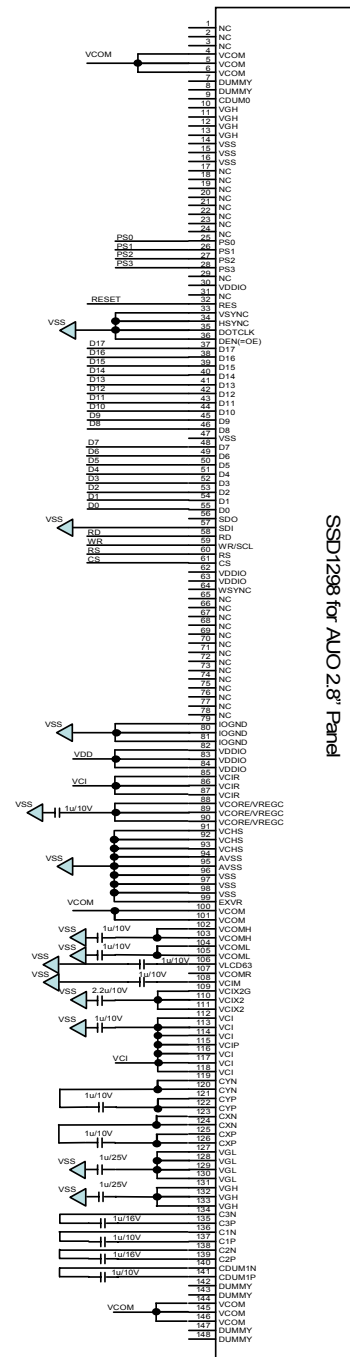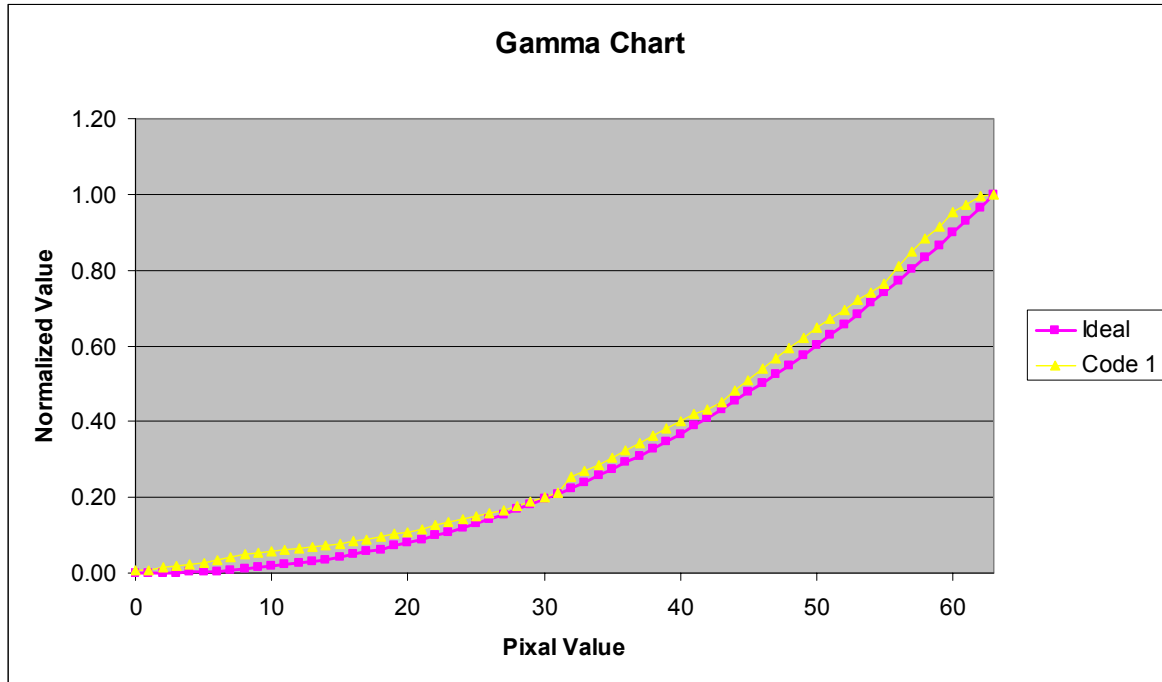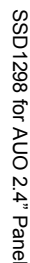
```
LCD_Send_SSD1298(0x0030, 0x0000);

LCD_Send_SSD1298(0x0031, 0x0400);

LCD_Send_SSD1298(0x0032, 0x0205);

LCD_Send_SSD1298(0x0033, 0x0500);

LCD_Send_SSD1298(0x0034, 0x0103);

LCD_Send_SSD1298(0x0035, 0x0702);

LCD_Send_SSD1298(0x0036, 0x0707);

LCD_Send_SSD1298(0x0037, 0x0102);

LCD_Send_SSD1298(0x003A, 0x0F00);

LCD_Send_SSD1298(0x003B, 0x1100);

//************* Special command **************//

LCD_Send_SSD1298(0x0028, 0x0006); // Enable test command

LCD_Send_SSD1298(0x002F, 0x12EB); // RAM speed tuning

LCD_Send_SSD1298(0x0026, 0x7000); // Internal Bandgap strength

LCD_Send_SSD1298(0x0020, 0xB0E3); // Internal Vcom strength

LCD_Send_SSD1298(0x0027, 0x0044); // Internal Vcomh/VcomL timing

LCD_Send_SSD1298(0x002E, 0x7E45); // VCOM charge sharing time

LCD_Send_SSD1298(0x0022); // Write RAM data

}
```

1.1.2 AUO 2.8" panel gamma curve

1.2 AUO 2.4' Panel

PS3 PS2 PS1 PS0	MODE
0 0 1 0	16 Bit 8080 Parallel
0 0 1 1	8 Bit 8080 Parallel
1 0 1 0	18 Bit 8080 Parallel

SSD1298 for AUO 2.4" Panel

1.2.1 AUO 2.4' initial code

```
void SSD1298_AUO24_Init(void)
{
// VCI=2.8V
//************* Reset LCD Driver ***************//
LCD_RESET_signal = 1;
delayms(1); // Delay 1ms
LCD_RESET_signal = 0;
delayms(10); // Delay 10ms     // Reset duration
LCD_RESET_signal = 1;
delayms(50); // Delay 50 ms
//************* Start Initial Sequence **********//
LCD_Send_SSD1298(0x0000, 0x0001); // Start internal OSC.
LCD_Send_SSD1298(0x0001, 0x333F); // Driver output control, RL=0;REV=1;GD=1;BGR=0;SM=0;TB=1
LCD_Send_SSD1298(0x0002, 0x0600); // set 1 line inversion
//************* Power control setup ************//
LCD_Send_SSD1298(0x000C, 0x0007); // Adjust VCIX2 output voltage
LCD_Send_SSD1298(0x000D, 0x0006); // Set amplitude magnification of VLCD63
LCD_Send_SSD1298(0x000E, 0x3000); // Set alternating amplitude of VCOM
LCD_Send_SSD1298(0x001E, 0x00B8); // Set VcomH voltage
LCD_Send_SSD1298(0x0003, 0x6A64); // Step-up factor/cycle setting
//************* Turn On display ****************//
LCD_Send_SSD1298(0x0010, 0x0000); // Sleep mode off.
delayms(30); // Wait 30mS
LCD_Send_SSD1298(0x0011, 0x4870); // Entry mode setup. 262K type B, take care on the data bus with 16it only
LCD_Send_SSD1298(0x0007, 0x0033); // Display ON
//************* LCD driver AC setting ***************//
LCD_Send_SSD1298(0x0025, 0x8000); // Frame freq control, 65Hz
LCD_Send_SSD1298(0x000B, 0x5308); // Frame cycle control, POR setting
//************* RAM position control **********//
LCD_Send_SSD1298(0x000F, 0x0000); // Gate scan position start at G0.
LCD_Send_SSD1298(0x0044, 0xEF00); // Horizontal RAM address position
LCD_Send_SSD1298(0x0045, 0x0000); // Vertical RAM address start position
LCD_Send_SSD1298(0x0046, 0x013F); // Vertical RAM address end position
// ----------- Adjust the Gamma Curve ----------//
```

```
LCD_Send_SSD1298(0x0030, 0x0000);

LCD_Send_SSD1298(0x0031, 0x0300);

LCD_Send_SSD1298(0x0032, 0x0206);

LCD_Send_SSD1298(0x0033, 0x0400);

LCD_Send_SSD1298(0x0034, 0x0202);

LCD_Send_SSD1298(0x0035, 0x0703);

LCD_Send_SSD1298(0x0036, 0x0707);

LCD_Send_SSD1298(0x0037, 0x0101);

LCD_Send_SSD1298(0x003A, 0x0F00);

LCD_Send_SSD1298(0x003B, 0x1200);

//************* Special command **************//

LCD_Send_SSD1298(0x0028, 0x0006); // Enable test command

LCD_Send_SSD1298(0x002F, 0x12EB); // RAM speed tuning

LCD_Send_SSD1298(0x0026, 0x7000); // Internal Bandgap strength

LCD_Send_SSD1298(0x0020, 0xB0E3); // Internal Vcom strength

LCD_Send_SSD1298(0x0027, 0x0044); // Internal Vcomh/VcomL timing

LCD_Send_SSD1298(0x002E, 0x7E45); // VCOM charge sharing time

LCD_Send_SSD1298(0x0022); // Write RAM data

}
```

1.2.2 AUO 2.4" panel gamma curve
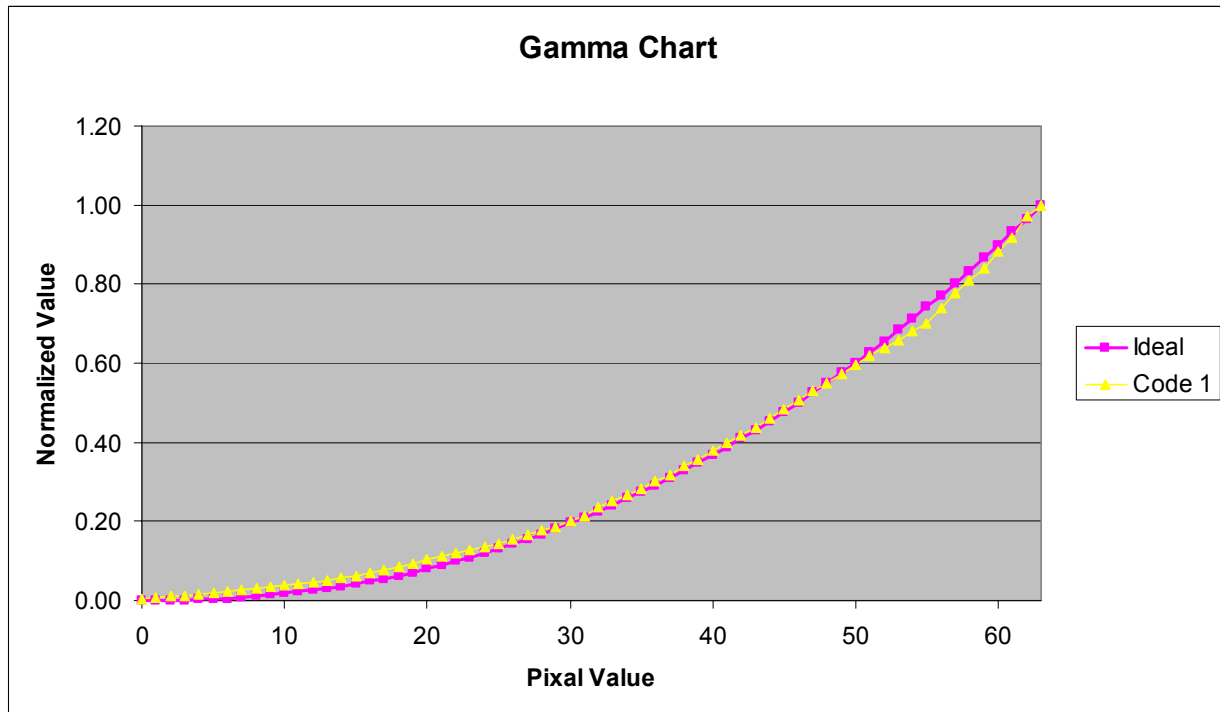
1.3 CPT 2.4" Panel

PS3 PS2 PS1 PS0	MODE
0 0 1 0	16 Bit 8080 Parallel
0 0 1 1	8 Bit 8080 Parallel
1 0 1 0	18 Bit 8080 Parallel

SSD1298 for CPT 2.4" Panel
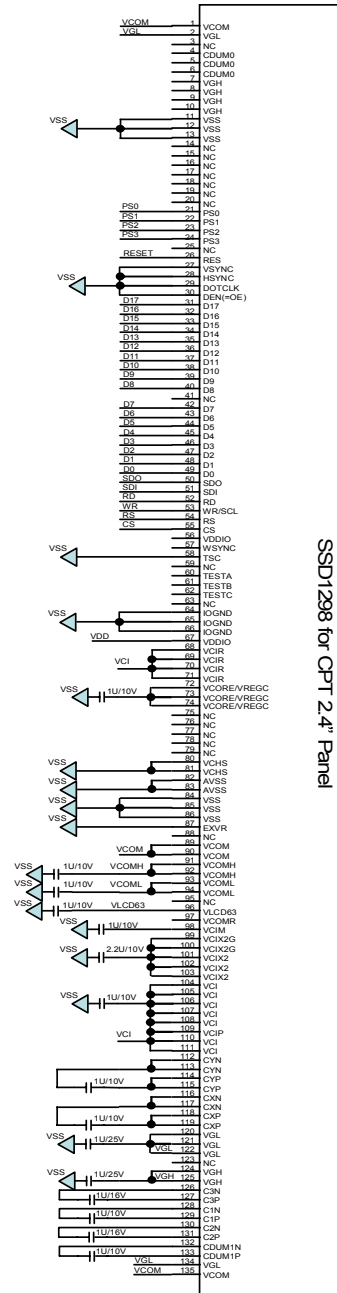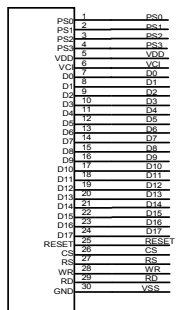
1.2.1 CPT 2.4" initial code

```c
void SSD1298_CPT24_Init(void)
{
// VCI=2.8V
//************* Reset LCD Driver ***************//
LCD_RESET_signal = 1;
delayms(1); // Delay 1ms
LCD_RESET_signal = 0;
delayms(10); // Delay 10ms     // Reset duration
LCD_RESET_signal = 1;
delayms(50); // Delay 50 ms
//************* Start Initial Sequence *********//
LCD_Send_SSD1298(0x0000, 0x0001); // Start internal OSC.
LCD_Send_SSD1298(0x0001, 0x333F); // Driver output control, RL=0;REV=1;GD=1;BGR=0;SM=0;TB=1
LCD_Send_SSD1298(0x0002, 0x0600); // set 1 line inversion
//************* Power control setup ***********//
LCD_Send_SSD1298(0x000C, 0x0007); // Adjust VCIX2 output voltage
LCD_Send_SSD1298(0x000D, 0x0006); // Set amplitude magnification of VLCD63
LCD_Send_SSD1298(0x000E, 0x3000); // Set alternating amplitude of VCOM
LCD_Send_SSD1298(0x001E, 0x00B8); // Set VcomH voltage
LCD_Send_SSD1298(0x0003, 0x6A64); // Step-up factor/cycle setting
//************* Turn On display *****************//
LCD_Send_SSD1298(0x0010, 0x0000); // Sleep mode off.
delayms(30); // Wait 30mS
LCD_Send_SSD1298(0x0011, 0x4870); // Entry mode setup. 262K type B, take care on the data bus with 16it only
LCD_Send_SSD1298(0x0007, 0x0033); // Display ON
//************* LCD driver AC setting ****************//
LCD_Send_SSD1298(0x0025, 0x8000); // Frame freq control, 65Hz
LCD_Send_SSD1298(0x000B, 0x5308); // Frame cycle control, POR setting
//************* RAM position control **********//
LCD_Send_SSD1298(0x000F, 0x0000); // Gate scan position start at G0.
LCD_Send_SSD1298(0x0044, 0xEF00); // Horizontal RAM address position
LCD_Send_SSD1298(0x0045, 0x0000); // Vertical RAM address start position
LCD_Send_SSD1298(0x0046, 0x013F); // Vertical RAM address end position
// ----------- Adjust the Gamma Curve ----------//
```

```
LCD_Send_SSD1298(0x0030, 0x0000);

LCD_Send_SSD1298(0x0031, 0x0400);

LCD_Send_SSD1298(0x0032, 0x0205);

LCD_Send_SSD1298(0x0033, 0x0500);

LCD_Send_SSD1298(0x0034, 0x0103);

LCD_Send_SSD1298(0x0035, 0x0702);

LCD_Send_SSD1298(0x0036, 0x0707);

LCD_Send_SSD1298(0x0037, 0x0102);

LCD_Send_SSD1298(0x003A, 0x0F00);

LCD_Send_SSD1298(0x003B, 0x1100);

//************* Special command *************//

LCD_Send_SSD1298(0x0028, 0x0006); // Enable test command

LCD_Send_SSD1298(0x002F, 0x12EB); // RAM speed tuning

LCD_Send_SSD1298(0x0026, 0x7000); // Internal Bandgap strength

LCD_Send_SSD1298(0x0020, 0xB0E3); // Internal Vcom strength

LCD_Send_SSD1298(0x0027, 0x0044); // Internal Vcomh/VcomL timing

LCD_Send_SSD1298(0x002E, 0x7E45); // VCOM charge sharing time

LCD_Send_SSD1298(0x0022); // Write RAM data

}
```

1.2.1 CPT 2.4" panel gamma curve
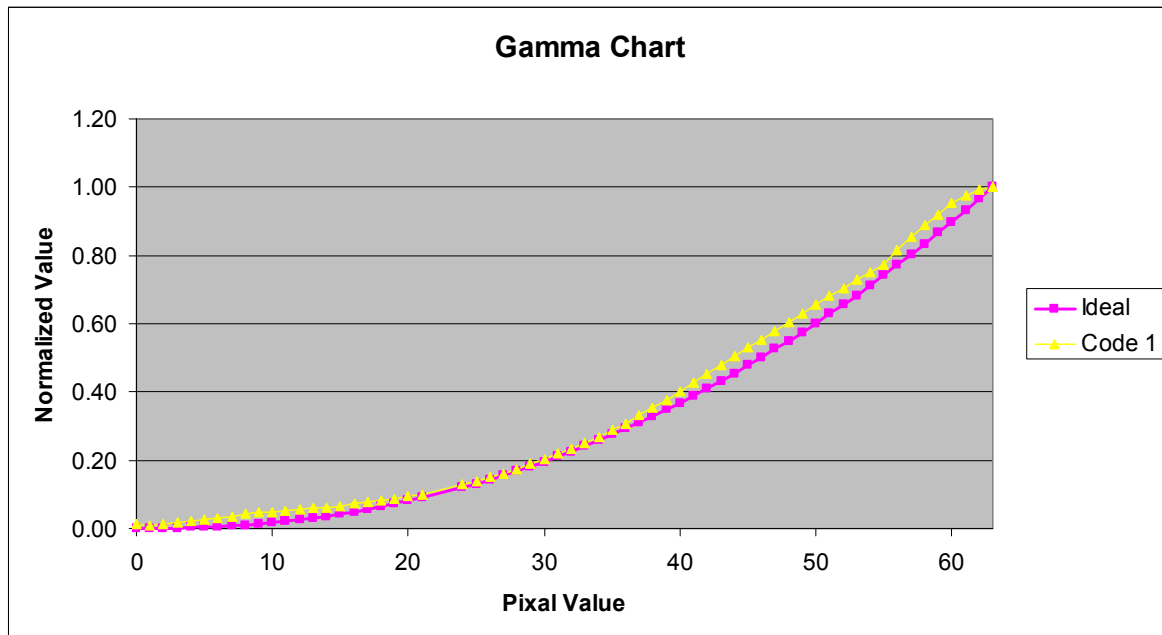
1.3 CPT 3.2" Panel

PS3 PS2 PS1 PS0	MODE
0 0 1 0	16 Bit 8080 Parallel
0 0 1 1	8 Bit 8080 Parallel
1 0 1 0	18 Bit 8080 Parallel
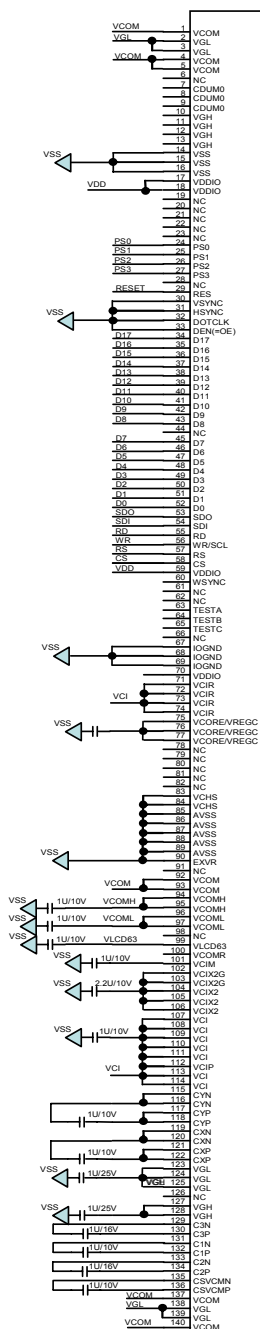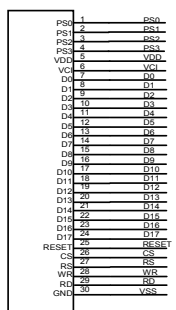
SSD1298 for CPT 2.8" Panel

1.3.1 CPT 3.2" initial code

void SSD1298_CPT32_Init(void)

```
{
// VCI=2.8V
//************** Reset LCD Driver ***************//
LCD_RESET_signal = 1;
delayms(1); // Delay 1ms
LCD_RESET_signal = 0;
delayms(10); // Delay 10ms     // Reset duration
LCD_RESET_signal = 1;
delayms(50); // Delay 50 ms
//************** Start Initial Sequence *********//
LCD_Send_SSD1298(0x0000, 0x0001); // Start internal OSC.
LCD_Send_SSD1298(0x0001, 0x333F); // Driver output control, RL=0;REV=1;GD=1;BGR=0;SM=0;TB=1
LCD_Send_SSD1298(0x0002, 0x0600); // set 1 line inversion
//************** Power control setup ************//
LCD_Send_SSD1298(0x000C, 0x0007); // Adjust VCIX2 output voltage
LCD_Send_SSD1298(0x000D, 0x0006); // Set amplitude magnification of VLCD63
LCD_Send_SSD1298(0x000E, 0x3200); // Set alternating amplitude of VCOM
LCD_Send_SSD1298(0x001E, 0x00BB); // Set VcomH voltage
LCD_Send_SSD1298(0x0003, 0x6A64); // Step-up factor/cycle setting
//************** Turn On display *****************//
LCD_Send_SSD1298(0x0010, 0x0000); // Sleep mode off.
delayms(30); // Wait 30mS
LCD_Send_SSD1298(0x0011, 0x4870); // Entry mode setup. 262K type B, take care on the data bus with 16it only
LCD_Send_SSD1298(0x0007, 0x0033); // Display ON
//************** LCD driver AC setting ****************//
LCD_Send_SSD1298(0x0025, 0xE000); // Frame freq control, 65Hz
LCD_Send_SSD1298(0x000B, 0x5308); // Frame cycle control, POR setting
//************** RAM position control **********//
LCD_Send_SSD1298(0x000F, 0x0000); // Gate scan position start at G0.
LCD_Send_SSD1298(0x0044, 0xEF00); // Horizontal RAM address position
LCD_Send_SSD1298(0x0045, 0x0000); // Vertical RAM address start position
LCD_Send_SSD1298(0x0046, 0x013F); // Vertical RAM address end position
// ----------- Adjust the Gamma Curve ----------//
LCD_Send_SSD1298(0x0030, 0x0000);
```

```
LCD_Send_SSD1298(0x0031, 0x0706);

LCD_Send_SSD1298(0x0032, 0x0206);

LCD_Send_SSD1298(0x0033, 0x0300);

LCD_Send_SSD1298(0x0034, 0x0002);

LCD_Send_SSD1298(0x0035, 0x0000);

LCD_Send_SSD1298(0x0036, 0x0707);

LCD_Send_SSD1298(0x0037, 0x0200);

LCD_Send_SSD1298(0x003A, 0x0908);

LCD_Send_SSD1298(0x003B, 0x0F0D);

//************* Special command **************//

LCD_Send_SSD1298(0x0028, 0x0006); // Enable test command

LCD_Send_SSD1298(0x002F, 0x12EB); // RAM speed tuning

LCD_Send_SSD1298(0x0026, 0x7000); // Internal Bandgap strength

LCD_Send_SSD1298(0x0020, 0xB0E3); // Internal Vcom strength

LCD_Send_SSD1298(0x0027, 0x0044); // Internal Vcomh/VcomL timing

LCD_Send_SSD1298(0x002E, 0x7E45); // VCOM charge sharing time

LCD_Send_SSD1298(0x0022); // Write RAM data

}
```

1.3.2　CPT 3.2" panel gamma curve

1.4 LPL 2.4" Panel

PS3	PS2	PS1	PS0	MODE
0	0	1	0	16 Bit 8080 Parallel
0	0	1	1	8 Bit 8080 Parallel
1	0	1	0	18 Bit 8080 Parallel

SSD1298 for LPL 2.4" Panel

Left connector (J, 30-pin):

Pin	Signal		Pin	Signal
1	PS0		16	D9
2	PS1		17	D10
3	PS2		18	D11
4	PS3		19	D12
5	VDD		20	D13
6	VCI		21	D14
7	D0		22	D15
8	D1		23	D16
9	D2		24	D17
10	D3		25	RESET
11	D4		26	CS
12	D5		27	RS
13	D6		28	WR
14	D7		29	RD
15	D8		30	VSS

Right connector (SSD1298, 160-pin):

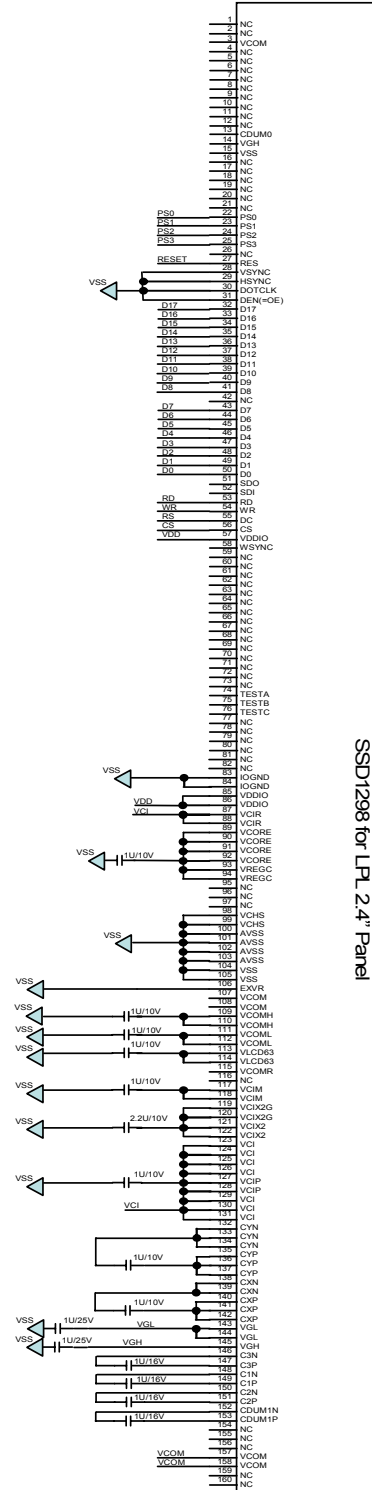| Pin	Signal		Pin	Signal
1	NC		81	NC
2	NC		82	NC
3	VCOM		83	IOGND
4	NC		84	IOGND
5	NC		85	VDDIO
6	NC		86	VDDIO
7	NC		87	VCIR
8	NC		88	VCIR
9	NC		89	VCORE
10	NC		90	VCORE
11	NC		91	VCORE
12	NC		92	VCORE
13	CDUM0		93	VREGC
14	VGH		94	VREGC
15	VSS		95	NC
16	NC		96	NC
17	NC		97	NC
18	NC		98	VCHS
19	NC		99	VCHS
20	NC		100	AVSS
21	NC		101	AVSS
22	PS0		102	AVSS
23	PS1		103	AVSS
24	PS2		104	VSS
25	PS3		105	VSS
26	NC		106	EXVR
27	RES		107	VCOM
28	VSYNC		108	VCOM
29	HSYNC		109	VCOMH
30	DOTCLK		110	VCOMH
31	DEN(=OE)		111	VCOML
32	D17		112	VCOML
33	D16		113	VLCD63
34	D15		114	VLCD63
35	D14		115	VCOMR
36	D13		116	NC
37	D12		117	VCIM
38	D11		118	VCIM
39	D10		119	VCIX2G
40	D9		120	VCIX2G
41	D8		121	VCIX2
42	NC		122	VCIX2
43	D7		123	VCI
44	D6		124	VCI
45	D5		125	VCI
46	D4		126	VCI
47	D3		127	VCIP
48	D2		128	VCIP
49	D1		129	VCI
50	D0		130	VCI
51	SDO		131	VCI
52	SDI		132	CVN
53	RD		133	CVN
54	WR		134	CYN
55	DC		135	CYP
56	CS		136	CYP
57	VDDIO		137	CYP
58	WSYNC		138	CXN
59	NC		139	CXN
60	NC		140	CXP
61	NC		141	CXP
62	NC		142	CXP
63	NC		143	VGL
64	NC		144	VGL
65	NC		145	VGH
66	NC		146	C3N
67	NC		147	C3P
68	NC		148	C1N
69	NC		149	C1P
70	NC		150	C2N
71	NC		151	C2P
72	NC		152	CDUM1N
73	NC		153	CDUM1P
74	TESTA		154	NC
75	TESTB		155	NC
76	TESTC		156	NC
77	NC		157	VCOM
78	NC		158	VCOM
79	NC		159	NC
80	NC		160	NC

Capacitor values: 1U/10V, 2.2U/10V, 1U/25V, 1U/16V

1.4.1 LPL 2.4" initial code

void SSD1298_LPL24_Init(void)

```
{
// VCI=2.8V
//************* Reset LCD Driver ***************//
LCD_RESET_signal = 1;
delayms(1); // Delay 1ms
LCD_RESET_signal = 0;
delayms(10); // Delay 10ms     // Reset duration
LCD_RESET_signal = 1;
delayms(50); // Delay 50 ms
//************* Start Initial Sequence **********//
LCD_Send_SSD1298(0x0000, 0x0001); // Start internal OSC.
LCD_Send_SSD1298(0x0001, 0x033F); // Driver output control, RL=0;REV=1;GD=1;BGR=0;SM=0;TB=1
LCD_Send_SSD1298(0x0002, 0x0600); // set 1 line inversion
//************* Power control setup ************//
LCD_Send_SSD1298(0x000C, 0x0007); // Adjust VCIX2 output voltage
LCD_Send_SSD1298(0x000D, 0x0006); // Set amplitude magnification of VLCD63
LCD_Send_SSD1298(0x000E, 0x3000); // Set alternating amplitude of VCOM
LCD_Send_SSD1298(0x001E, 0x00B8); // Set VcomH voltage
LCD_Send_SSD1298(0x0003, 0x6A64); // Step-up factor/cycle setting
//************* Turn On display *****************//
LCD_Send_SSD1298(0x0010, 0x0000); // Sleep mode off.
delayms(30); // Wait 30mS
LCD_Send_SSD1298(0x0011, 0x4870); // Entry mode setup. 262K type B, take care on the data bus with 16it only
LCD_Send_SSD1298(0x0007, 0x0033); // Display ON
//************ LCD driver AC setting ******************//
LCD_Send_SSD1298(0x0025, 0x8000); // Frame freq control, 65Hz
LCD_Send_SSD1298(0x000B, 0x5308); // Frame cycle control, POR setting
//************ RAM position control **********//
LCD_Send_SSD1298(0x000F, 0x0000); // Gate scan position start at G0.
LCD_Send_SSD1298(0x0044, 0xEF00); // Horizontal RAM address position
LCD_Send_SSD1298(0x0045, 0x0000); // Vertical RAM address start position
LCD_Send_SSD1298(0x0046, 0x013F); // Vertical RAM address end position
// ----------- Adjust the Gamma Curve ----------//
LCD_Send_SSD1298(0x0030, 0x0000);
```
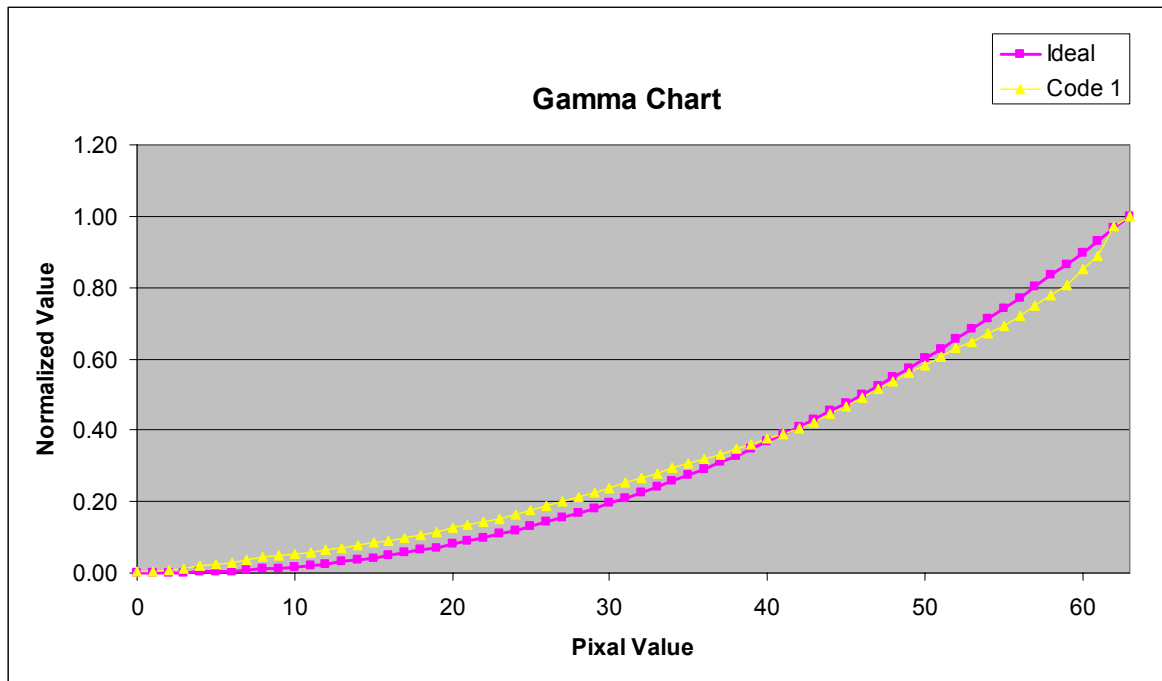
```
LCD_Send_SSD1298(0x0031, 0x0707);

LCD_Send_SSD1298(0x0032, 0x0707);

LCD_Send_SSD1298(0x0033, 0x0000);

LCD_Send_SSD1298(0x0034, 0x0000);

LCD_Send_SSD1298(0x0035, 0x0000);

LCD_Send_SSD1298(0x0036, 0x0707);

LCD_Send_SSD1298(0x0037, 0x0000);

LCD_Send_SSD1298(0x003A, 0x1A0F);

LCD_Send_SSD1298(0x003B, 0x1F00);

}
```
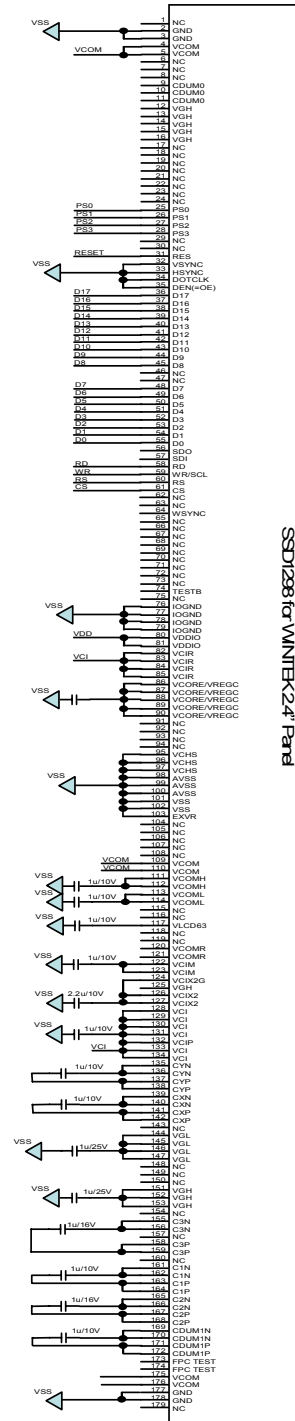
1.4.2 LPL 2.4" panel gamma curve

1.5 Wintek 2.4" Panel

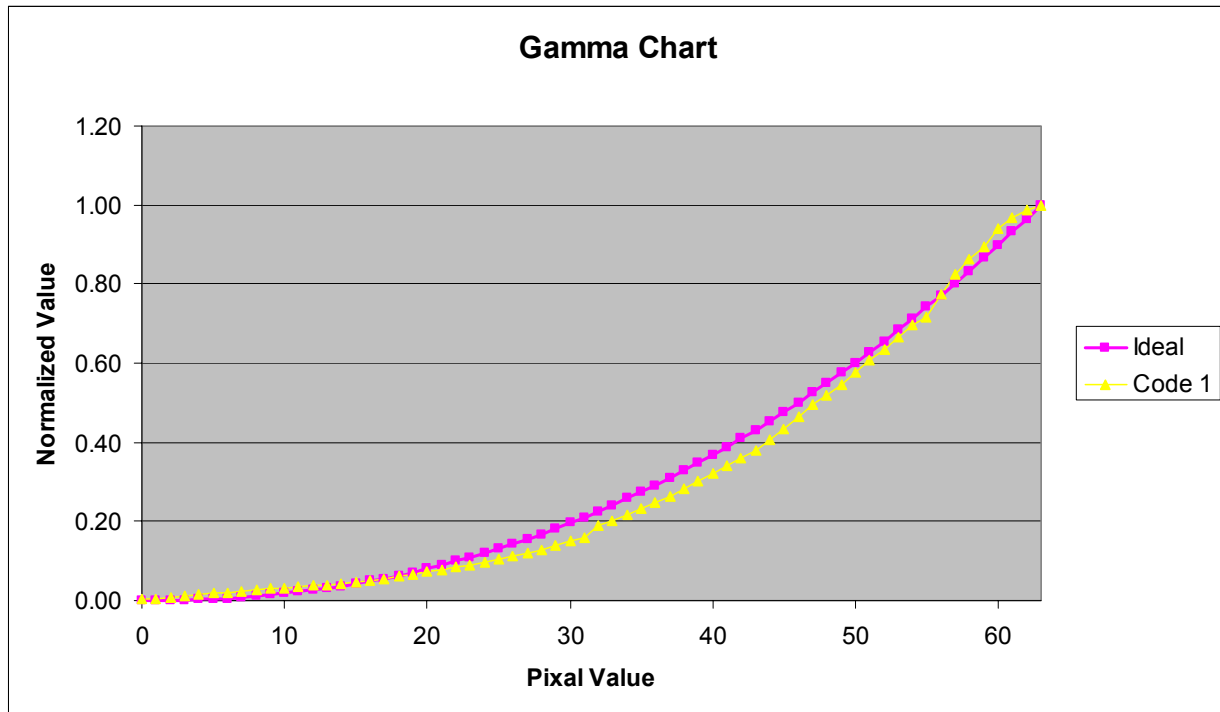| PS3	PS2	PS1	PS0	MODE
0	0	1	0	16 Bit 8080 Parallel
0	0	1	1	8 Bit 8080 Parallel
1	0	1	0	18 Bit 8080 Parallel

1.5.1 Wintek 2.4" initial code

void SSD1298_Wintek24_Init(void)

```
{
// VCI=2.8V
//************* Reset LCD Driver ***************//
LCD_RESET_signal = 1;
delayms(1); // Delay 1ms
LCD_RESET_signal = 0;
delayms(10); // Delay 10ms     // Reset duration
LCD_RESET_signal = 1;
delayms(50); // Delay 50 ms
//************* Start Initial Sequence *********//
LCD_Send_SSD1298(0x0000, 0x0001); // Start internal OSC.
LCD_Send_SSD1298(0x0001, 0x3B3F); // Driver output control, RL=0;REV=1;GD=1;BGR=1;SM=0;TB=1
LCD_Send_SSD1298(0x0002, 0x0600); // set 1 line inversion
//************* Power control setup ***********//
LCD_Send_SSD1298(0x000C, 0x0004); // Adjust VCIX2 output voltage
LCD_Send_SSD1298(0x000D, 0x080C); // Set amplitude magnification of VLCD63
LCD_Send_SSD1298(0x000E, 0x2B00); // Set alternating amplitude of VCOM
LCD_Send_SSD1298(0x001E, 0x00B3); // Set VcomH voltage
LCD_Send_SSD1298(0x0003, 0xA8A8); // Step-up factor/cycle setting
//************* Turn On display *****************//
LCD_Send_SSD1298(0x0010, 0x0000); // Sleep mode off.
delayms(30); // Wait 30mS
LCD_Send_SSD1298(0x0011, 0x4870); // Entry mode setup. 262K type B, take care on the data bus with 16it only
LCD_Send_SSD1298(0x0007, 0x0033); // Display ON
//************* LCD driver AC setting ****************//
LCD_Send_SSD1298(0x0025, 0x8000); // Frame freq control, 65Hz
LCD_Send_SSD1298(0x000B, 0x5308); // Frame cycle control, POR setting
//************* RAM position control **********//
LCD_Send_SSD1298(0x000F, 0x0000); // Gate scan position start at G0.
LCD_Send_SSD1298(0x0044, 0xEF00); // Horizontal RAM address position
LCD_Send_SSD1298(0x0045, 0x0000); // Vertical RAM address start position
LCD_Send_SSD1298(0x0046, 0x013F); // Vertical RAM address end position
// ----------- Adjust the Gamma Curve ----------//
```

LCD_Send_SSD1298(0x0030, 0x0000);

LCD_Send_SSD1298(0x0031, 0x0400);

LCD_Send_SSD1298(0x0032, 0x0205);

LCD_Send_SSD1298(0x0033, 0x0500);

LCD_Send_SSD1298(0x0034, 0x0103);

LCD_Send_SSD1298(0x0035, 0x0702);

LCD_Send_SSD1298(0x0036, 0x0707);

LCD_Send_SSD1298(0x0037, 0x0102);

LCD_Send_SSD1298(0x003A, 0x0F00);

LCD_Send_SSD1298(0x003B, 0x1100);

//************* Special command *************//

LCD_Send_SSD1298(0x0028, 0x0006); // Enable test command

LCD_Send_SSD1298(0x002F, 0x12EB); // RAM speed tuning

LCD_Send_SSD1298(0x0026, 0x7000); // Internal Bandgap strength

LCD_Send_SSD1298(0x0020, 0xB0E3); // Internal Vcom strength

LCD_Send_SSD1298(0x0027, 0x0044); // Internal Vcomh/VcomL timing

LCD_Send_SSD1298(0x002E, 0x7E45); // VCOM charge sharing time

LCD_Send_SSD1298(0x0022); // Write RAM data

}

1.5.2 Wintek 2.4" panel gamma curve

1.6 Wintek 2.8" Panel

PS3 PS2 PS1 PS0	MODE
0 0 1 0	16 Bit 8080 Parallel
0 0 1 1	8 Bit 8080 Parallel
1 0 1 0	18 Bit 8080 Parallel
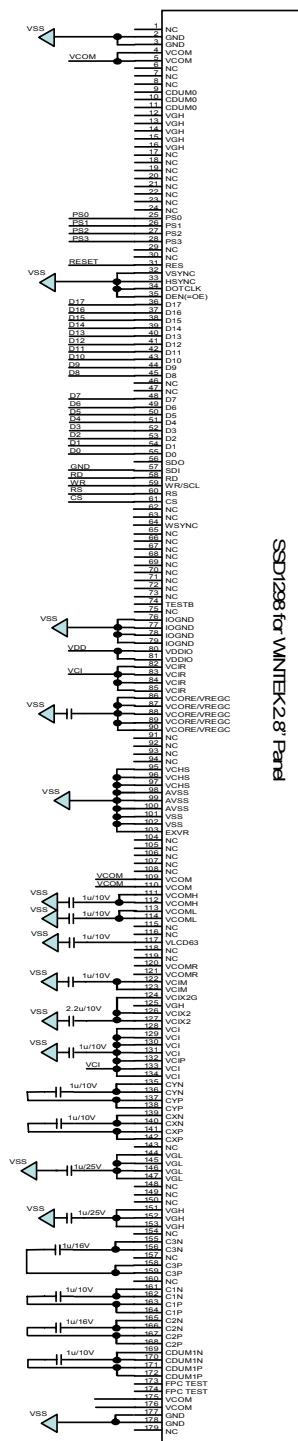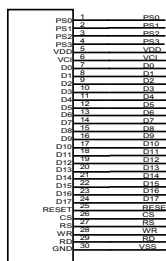
1.6.1 Wintek 2.8" Initial code

void SSD1298_Wintek28_Init(void)

```
{
// VCI=2.8V
//************* Reset LCD Driver ***************//
LCD_RESET_signal = 1;
delayms(1); // Delay 1ms
LCD_RESET_signal = 0;
delayms(10); // Delay 10ms      // Reset duration
LCD_RESET_signal = 1;
delayms(50); // Delay 50 ms
//************* Start Initial Sequence *********//
LCD_Send_SSD1298(0x0000, 0x0001); // Start internal OSC.
LCD_Send_SSD1298(0x0001, 0x3B3F); // Driver output control, RL=0;REV=1;GD=1;BGR=0;SM=0;TB=1
LCD_Send_SSD1298(0x0002, 0x0600); // set 1 line inversion
//************* Power control setup ************//
LCD_Send_SSD1298(0x000C, 0x0000); // Adjust VCIX2 output voltage
LCD_Send_SSD1298(0x000D, 0x080C); // Set amplitude magnification of VLCD63
LCD_Send_SSD1298(0x000E, 0x2B00); // Set alternating amplitude of VCOM
LCD_Send_SSD1298(0x001E, 0x00B3); // Set VcomH voltage
LCD_Send_SSD1298(0x0003, 0xA8A4); // Step-up factor/cycle setting
//************* Turn On display ******************//
LCD_Send_SSD1298(0x0010, 0x0000); // Sleep mode off.
delayms(30); // Wait 30mS
LCD_Send_SSD1298(0x0011, 0x4870); // Entry mode setup. 262K type B, take care on the data bus with 16it only
LCD_Send_SSD1298(0x0007, 0x0033); // Display ON
//************* LCD driver AC setting ********************//
LCD_Send_SSD1298(0x0025, 0x8000); // Frame freq control, 65Hz
LCD_Send_SSD1298(0x000B, 0x5308); // Frame cycle control, POR setting
//************* RAM position control **********//
LCD_Send_SSD1298(0x000F, 0x0000); // Gate scan position start at G0.
LCD_Send_SSD1298(0x0044, 0xEF00); // Horizontal RAM address position
LCD_Send_SSD1298(0x0045, 0x0000); // Vertical RAM address start position
LCD_Send_SSD1298(0x0046, 0x013F); // Vertical RAM address end position
// ----------- Adjust the Gamma Curve ----------//
LCD_Send_SSD1298(0x0030, 0x0707);
LCD_Send_SSD1298(0x0031, 0x0204);
```

```
LCD_Send_SSD1298(0x0032, 0x0204);

LCD_Send_SSD1298(0x0033, 0x0502);

LCD_Send_SSD1298(0x0034, 0x0507);

LCD_Send_SSD1298(0x0035, 0x0204);

LCD_Send_SSD1298(0x0036, 0x0204);

LCD_Send_SSD1298(0x0037, 0x0502);

LCD_Send_SSD1298(0x003A, 0x0302);

LCD_Send_SSD1298(0x003B, 0x0302);

//************* Special command **************//

LCD_Send_SSD1298(0x0028, 0x0006); // Enable test command

LCD_Send_SSD1298(0x002F, 0x12EB); // RAM speed tuning

LCD_Send_SSD1298(0x0026, 0x7000); // Internal Bandgap strength

LCD_Send_SSD1298(0x0020, 0xB0E3); // Internal Vcom strength

LCD_Send_SSD1298(0x0027, 0x0044); // Internal Vcomh/VcomL timing

LCD_Send_SSD1298(0x002E, 0x7E45); // VCOM charge sharing time

LCD_Send_SSD1298(0x0022); // Write RAM data

}
```

1.6.2 Wintek 2.8" panel gamma curve

Gamma Chart - Wintek 2.8" - 2.8V
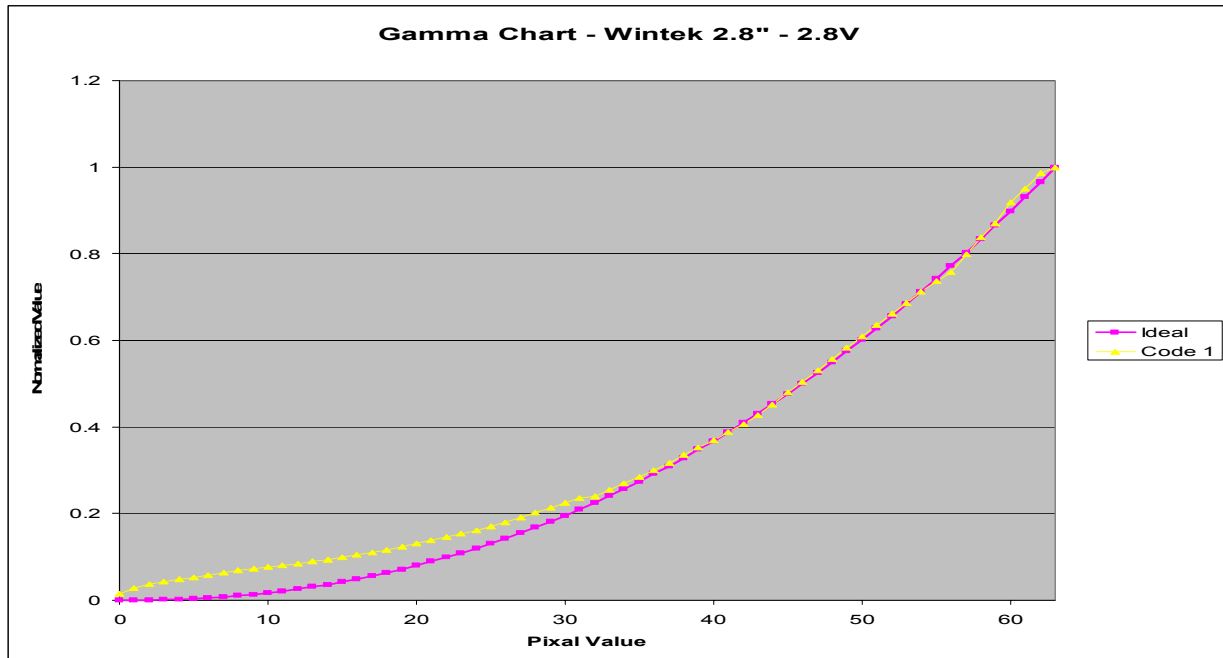
1.7 Wintek 3.2" Panel
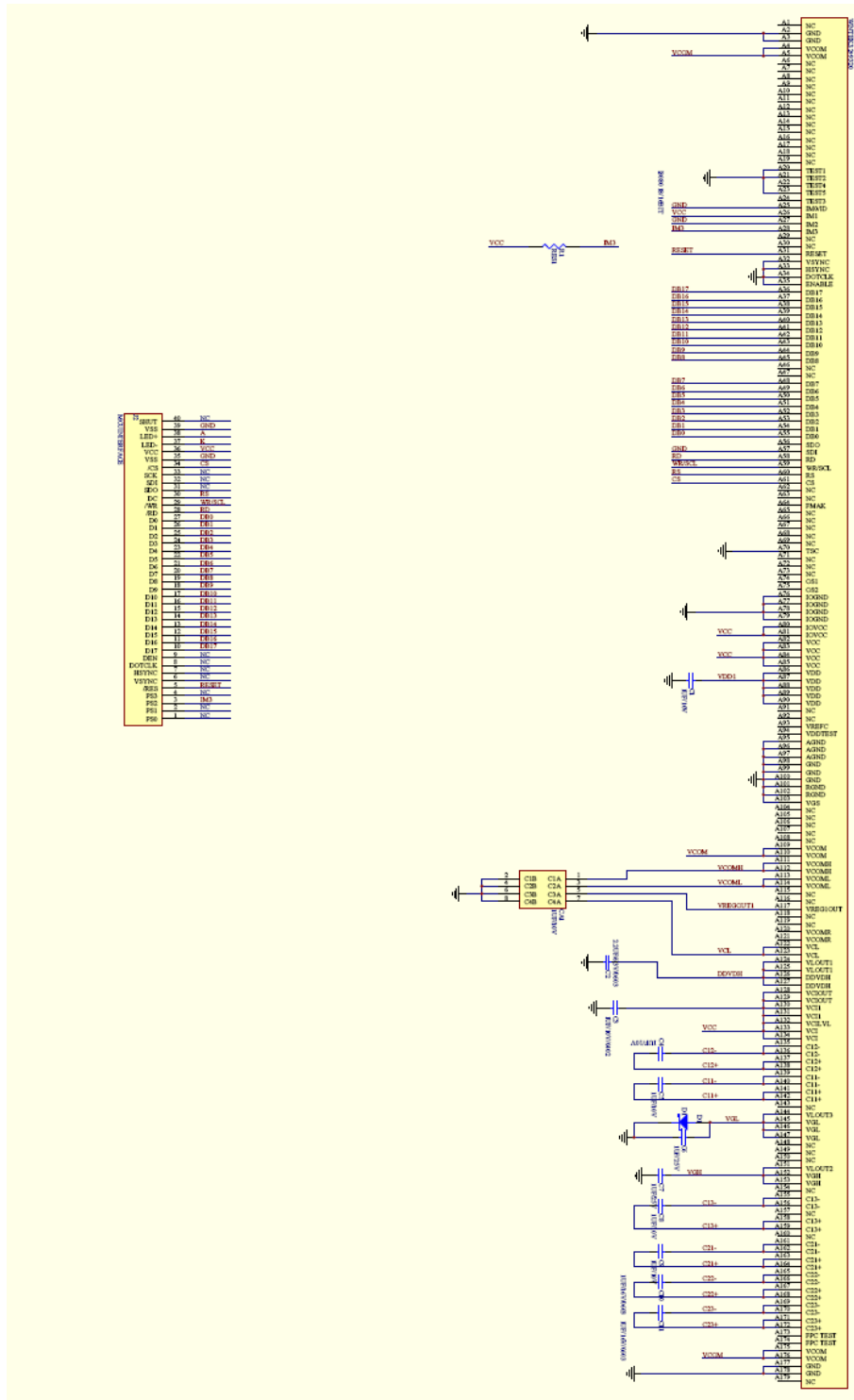
1.7.1 Wintek 3.2" Initial code

void SSD1298_Wintek28_Init(void)

```
{
// VCI=2.8V
//************* Reset LCD Driver ***************//
LCD_RESET_signal = 1;
delayms(1); // Delay 1ms
LCD_RESET_signal = 0;
delayms(10); // Delay 10ms    // Reset duration
LCD_RESET_signal = 1;
delayms(50); // Delay 50 ms
//************* Start Initial Sequence *********//
LCD_Send_SSD1298(0x0000, 0x0001); // Start internal OSC.
LCD_Send_SSD1298(0x0001, 0x3B3F); // Driver output control, RL=0;REV=1;GD=1;BGR=0;SM=0;TB=1
LCD_Send_SSD1298(0x0002, 0x0600); // set 1 line inversion
//************* Power control setup ***********//
LCD_Send_SSD1298(0x000C, 0x0004); // Adjust VCIX2 output voltage
LCD_Send_SSD1298(0x000D, 0x0000F); // Set amplitude magnification of VLCD63
LCD_Send_SSD1298(0x000E, 0x2B00); // Set alternating amplitude of VCOM
LCD_Send_SSD1298(0x001E, 0x00B5); // Set VcomH voltage
LCD_Send_SSD1298(0x0003, 0xA8A4); // Step-up factor/cycle setting
//************* Turn On display *****************//
LCD_Send_SSD1298(0x0010, 0x0000); // Sleep mode off.
delayms(30); // Wait 30mS
LCD_Send_SSD1298(0x0011, 0x6870); // Entry mode setup. 65K type B, take care on the data bus with 16it only
LCD_Send_SSD1298(0x0007, 0x0033); // Display ON
//************* LCD driver AC setting ******************//
LCD_Send_SSD1298(0x0025, 0x8000); // Frame freq control, 65Hz
LCD_Send_SSD1298(0x000B, 0x5308); // Frame cycle control, POR setting
//************* RAM position control **********//
LCD_Send_SSD1298(0x000F, 0x0000); // Gate scan position start at G0.
LCD_Send_SSD1298(0x0044, 0xEF00); // Horizontal RAM address position
LCD_Send_SSD1298(0x0045, 0x0000); // Vertical RAM address start position
LCD_Send_SSD1298(0x0046, 0x013F); // Vertical RAM address end position
// ----------- Adjust the Gamma Curve ----------//
LCD_Send_SSD1298(0x0030, 0x0707);
LCD_Send_SSD1298(0x0031, 0x0204);
```
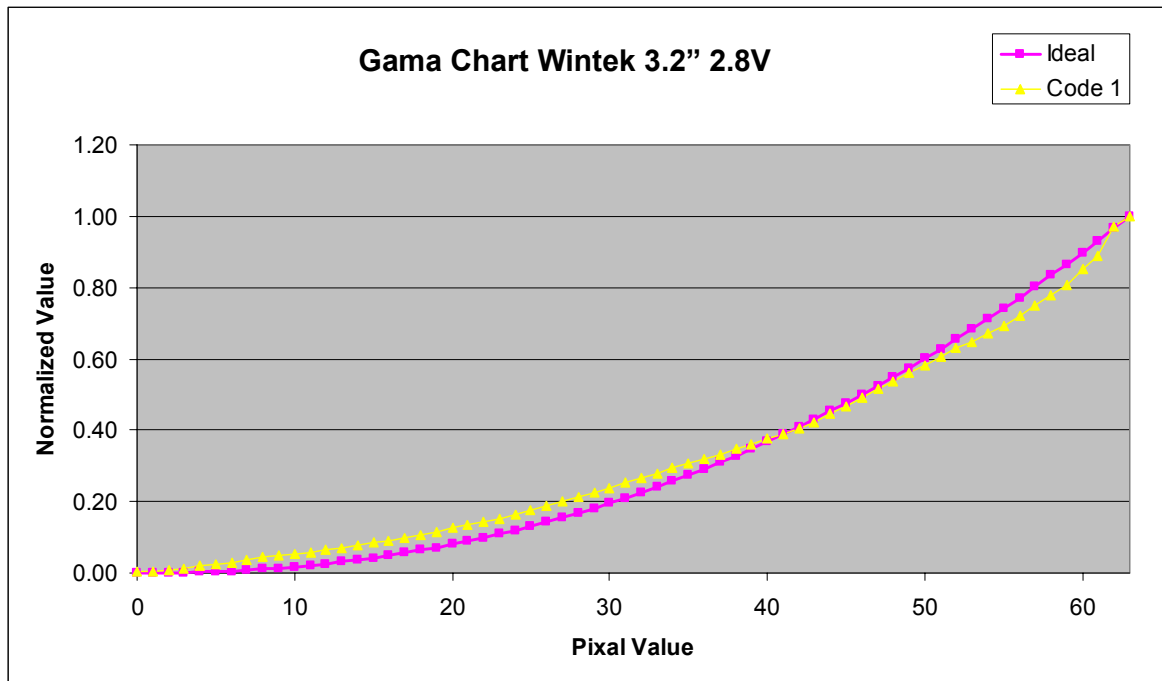
```
LCD_Send_SSD1298(0x0032, 0x0204);

LCD_Send_SSD1298(0x0033, 0x0105);

LCD_Send_SSD1298(0x0034, 0x0507);

LCD_Send_SSD1298(0x0035, 0x0204);

LCD_Send_SSD1298(0x0036, 0x0204);

LCD_Send_SSD1298(0x0037, 0x0500);

LCD_Send_SSD1298(0x003A, 0x0308);

LCD_Send_SSD1298(0x003B, 0x1002);

//************* Special command *************//

LCD_Send_SSD1298(0x0028, 0x0006); // Enable test command

LCD_Send_SSD1298(0x002F, 0x12EB); // RAM speed tuning

LCD_Send_SSD1298(0x0026, 0x7000); // Internal Bandgap strength

LCD_Send_SSD1298(0x0020, 0xB0E3); // Internal Vcom strength

LCD_Send_SSD1298(0x0027, 0x0044); // Internal Vcomh/VcomL timing

LCD_Send_SSD1298(0x002E, 0x7E45); // VCOM charge sharing time

LCD_Send_SSD1298(0x0022); // Write RAM data

}
```
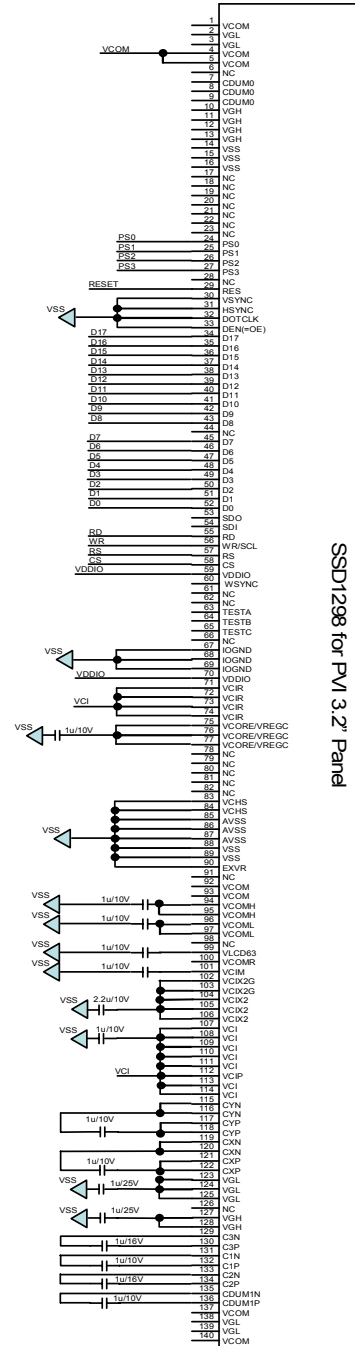
1.7.2 Wintek 3.2" panel gamma curve

Gama Chart Wintek 3.2" 2.8V

Legend: Ideal, Code 1

Y-axis: Normalized Value (0.00, 0.20, 0.40, 0.60, 0.80, 1.00, 1.20)
X-axis: Pixal Value (0, 10, 20, 30, 40, 50, 60)

1.8 PVI 2.6" Panel

PS3 PS2 PS1 PS0	MODE
0 0 1 0	16 Bit 8080 Parallel
0 0 1 1	8 Bit 8080 Parallel
1 0 1 0	18 Bit 8080 Parallel

SSD1298 for PVI 3.2" Panel

1.8.1 PVI 2.6" Initial code

void SSD1298_PVI26_Init(void)

{

// VCI=2.8V

//************* Reset LCD Driver ***************//

LCD_RESET_signal = 1;

delayms(1); // Delay 1ms

LCD_RESET_signal = 0;

delayms(10); // Delay 10ms   **// Reset duration**

LCD_RESET_signal = 1;

delayms(50); // Delay 50 ms

//************* Start Initial Sequence *********//

LCD_Send_SSD1298(0x0000, 0x0001); // Start internal OSC.

LCD_Send_SSD1298(0x0001, 0x333F); // Driver output control, RL=0;REV=1;GD=1;BGR=0;SM=0;TB=1

LCD_Send_SSD1298(0x0002, 0x0600); // set 1 line inversion

//************* Power control setup ************//

LCD_Send_SSD1298(0x000C, 0x0007); // Adjust VCIX2 output voltage

LCD_Send_SSD1298(0x000D, 0x0006); // Set amplitude magnification of VLCD63

LCD_Send_SSD1298(0x000E, 0x3000); // Set alternating amplitude of VCOM

LCD_Send_SSD1298(0x001E, 0x00B8); // Set VcomH voltage

LCD_Send_SSD1298(0x0003, 0x6A64); // Step-up factor/cycle setting

//************* Turn On display ******************//

LCD_Send_SSD1298(0x0010, 0x0000); // Sleep mode off.

delayms(30); // Wait 30mS

LCD_Send_SSD1298(0x0011, 0x4870); // Entry mode setup. 262K type B, take care on the data bus with 16it only

LCD_Send_SSD1298(0x0007, 0x0033); // Display ON

//************* LCD driver AC setting *****************//

LCD_Send_SSD1298(0x0025, 0x8000); // Frame freq control, 65Hz

LCD_Send_SSD1298(0x000B, 0x5308); // Frame cycle control, POR setting

//************* RAM position control **********//

LCD_Send_SSD1298(0x000F, 0x0000); // Gate scan position start at G0.

LCD_Send_SSD1298(0x0044, 0xEF00); // Horizontal RAM address position

LCD_Send_SSD1298(0x0045, 0x0000); // Vertical RAM address start position

LCD_Send_SSD1298(0x0046, 0x013F); // Vertical RAM address end position

// ----------- Adjust the Gamma Curve ----------//

LCD_Send_SSD1298(0x0030, 0x0000);

LCD_Send_SSD1298(0x0031, 0x0077);

```
LCD_Send_SSD1298(0x0032, 0x0007);

LCD_Send_SSD1298(0x0033, 0x0500);

LCD_Send_SSD1298(0x0034, 0x0005);

LCD_Send_SSD1298(0x0035, 0x0000);

LCD_Send_SSD1298(0x0036, 0x0707);

LCD_Send_SSD1298(0x0037, 0x0003);

LCD_Send_SSD1298(0x003A, 0x1400);

LCD_Send_SSD1298(0x003B, 0x1900);

//************* Special command **************//

LCD_Send_SSD1298(0x0028, 0x0006); // Enable test command

LCD_Send_SSD1298(0x002F, 0x12BE); // RAM speed tuning

LCD_Send_SSD1298(0x0026, 0x7000); // Internal Bandgap strength

LCD_Send_SSD1298(0x0020, 0xB0E3); // Internal Vcom strength

LCD_Send_SSD1298(0x0027, 0x0044); // Internal Vcomh/VcomL timing

LCD_Send_SSD1298(0x002E, 0x7E45); // VCOM charge sharing time

LCD_Send_SSD1298(0x0022); // Write RAM data

}
```

1.8.2 PVI 2.6" panel gamma curve