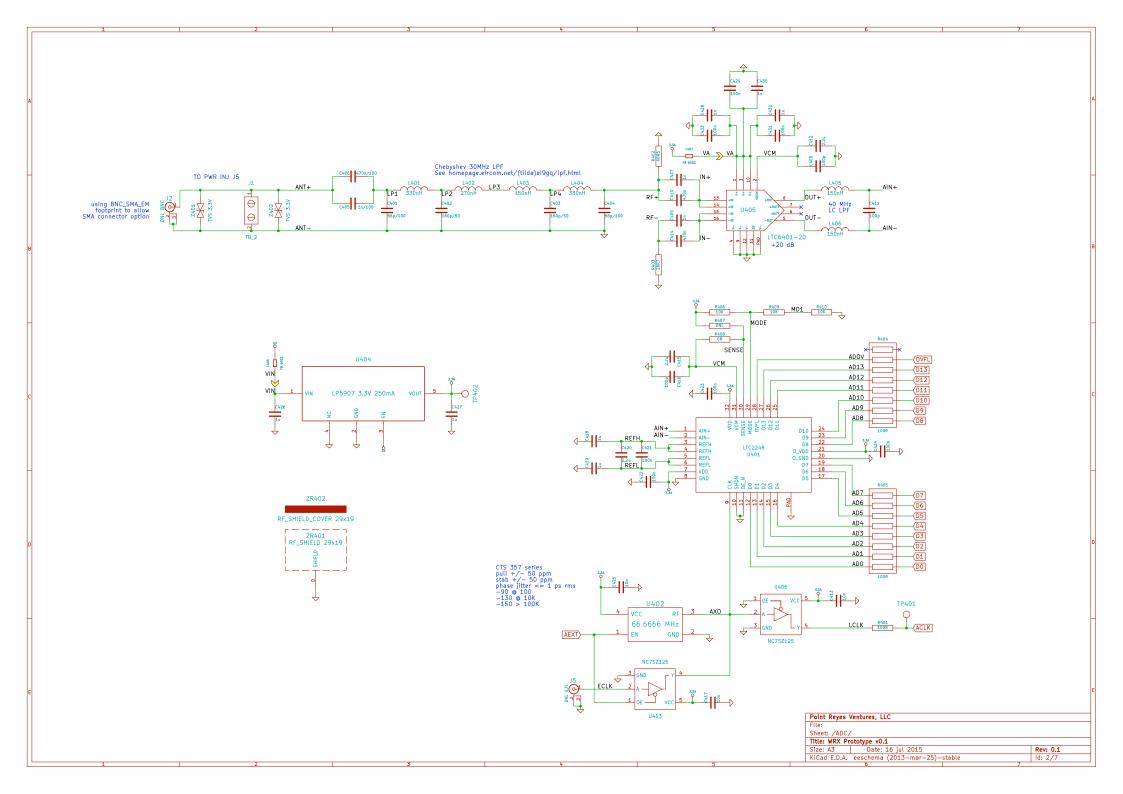
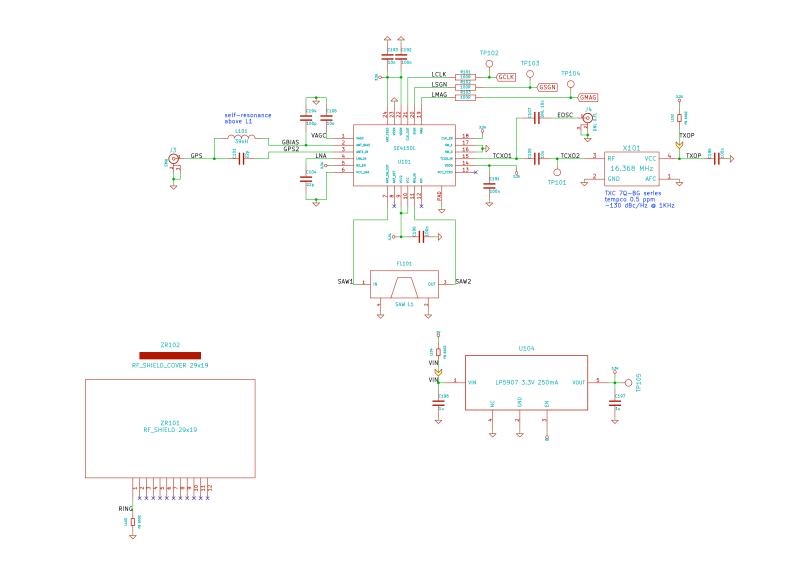
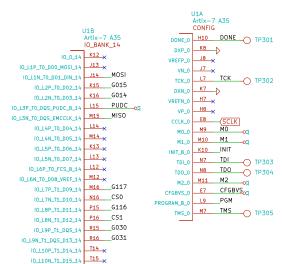
1	2	3	4	5
	Sheet: ADC	Sheet: FPGA_Power		
	File: wrx.ADC.sch	File: wrx.FPGA_power.sch		<u> </u>
	Sheet: GPS	Sheet: Power_Supplies		
	SHEEC. OF S	Sheet. Fower_Supplies		
	File: wrx.GPS.sch	File: wrx.power_supplies.sch		
	Sheet: BeagleBone			
	Sheet: beagtebolle			
	File: wrx.BeagleBone.sch			
	, and the second se			B
	CL L EDGA IO			
	Sheet: FPGA_IO			
	File: wrx.FPGA_IO.sch			
				c
			Point Reyes Ventures, LLC	
			File:	
			Sheet: / Title: WRX Prototype v0.1	
			Size: A/L Date: 16 iul 2015	Rev: 0.1
			Size: A4 Date: 16 jul 2015 KiCad E.D.A. eeschema (2013-mar-25)-stabl	e Id: 1/7
			Turena Finiti ecacionia (Zota-mai-Za)-stant	. 10, 1//



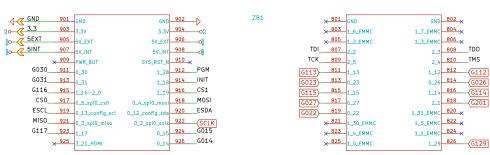


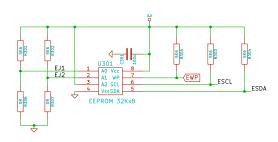




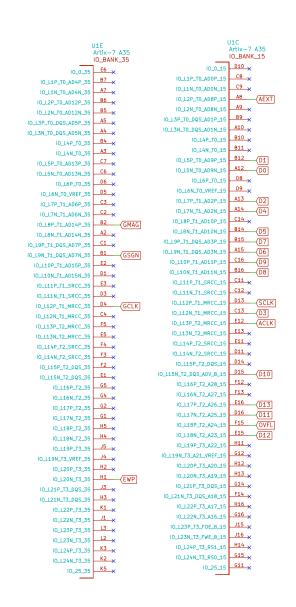
IO_L17N_T2_A13_D29_14 R11 ×

IO_L18P_T2_A12_D28_14 N9 ×





Point Reyes Ventures, LLC					
File:					
Sheet: /BeagleBone/					
Title: WRX Prototype v0.1					
Size: A3	Date: 16 jul 2015	Rev: 0.1			
KiCad E.D.A.	eeschema (2013-mar-25)-stable	ld: 4/7			
	6	7			



Artix-7 A35 IO_BANK_34

10_0_34 L5 (G129)

IO_L1P_T0_34 L4 G022

IO_L2P_T0_34 M2 G027

IO_L2N_T0_34 M1 G201

IO_L4P_T0_34 N1 (G114)

IO_L4N_T0_34 P1 G026

IO_L7P_T1_34 R2 G112

IO_L7N_T1_34 R1 G113

IO_L3P_T0_DQS_34 N3 G023

IO_L3N_TO_DQS_34 N2 G115

I0_L5P_T0_34 P4 ×

IO_L5N_T0_34 P3 ×

IO_L6P_T0_34 M5 ×

IO_L8P_T1_34 R3 ×

IO_L8N_T1_34 T2 ×

10_L10P_T1_34 P5 ×

IO_L9N_T1_DQS_34 T3 ×

FID2

FPGA FIDUCIAL

FID4

GLOBAL FIDUCIAL

FID6

GLOBAL FIDUCIAL GLOBAL FIDUCIAL

FID1

FPGA FIDUCIAL

FID3

GLOBAL FIDUCIAL

FID5

IO_L6N_TO_VREF_34 N4 ×

IO_L1N_T0_34 ×

Point Reyes Ventures, LLC				
File:				
Sheet: /FPGA_IO/				
Title: WRX Prototype v0.1				
Size: A3	Date: 16 jul 2015	Rev: 0.1		
KiCad E.D.A.	eeschema (2013-mar-25)-stable	ld: 5/7		

