Data Sheet

CN700
North Bridge
with Integrated
UniChrome Pro 3D/2D
Graphics Controller

Revision 1.32
September 9, 2009

VIA TECHNOLOGIES, INC.

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REVISION HISTORY

Document Release	Date	Revision	Initials
1.0	7/28/05	Initial release	JW
1.01	8/1/05	Updated strapping table	JW
1.02	8/24/05	Updated pin lists and ball diagram Updated system block diagram Updated ATX layout diagram Updated strap table Updated product name Updated South Bridge name Added AGP 3.5 support	JW
1.03	8/31/05	Updated FSB information	JW
1.04	9/22/05	Updated MEMDET pin description	JW
1.05	9/29/05	Updated processor support information Updated system block diagram	JW
1.06	10/12/05	Updated ball diagram, lists and descriptions with GDVP1 information	JW
1.07	9/28/06	Removed VT8235M and VT8237R information Removed FSB 800/533 from product descriptions Removed 1024 MB from DDR and DDR2 descriptions	JW
1.08	9/29/06	Updated CRT max supported resolution	JW
1.09	10/2/06	Removed 800 MHz from Electrical Specifications Changed VT1631 to VT1636 and VT1632 to VT1632A. Removed VT1623 description.	JW
1.10	10/9/06	Updated display section descriptions according to the system block diagram. Removed 1623M and 1622AM description Revised “VT8251” to “VT8251 Version CD / CE” Revised strap pin table South Bridge names Updated mechanical drawings Removed pin list ordered by pin number	JW
1.11	4/26/07	Added 800 MHz for CPU FSB speed Updated System Block Diagram ***Updated the following registers:*** D0F2: Rx7A register descriptions D0F3: RxA1-A0[14:12] bit descriptions D0F7: RxB4[0] attribute	AT
1.2	10/22/07	Added Package Thermal Simulation subsection under Electrical Specification section	SY
1.21	1/22/08	Updated Package Thermal Simulation section under Electrical Specification	AT
1.22	2/5/08	Updated signals GPOUT and GPO0 in Pin Descriptions table	AT
1.23	7/11/08	Removed old OS support for Windows 9X/ME, Windows 2000 and NT4.0	AT
1.3	12/4/08	Updated the legal page Added supported CPU, FSB and related descriptions Added VT8237S support under Product Features section Changed Lead-Free Package to RoHS Package under Mechanical Specifications Added Total Green package under Mechanical Specifications	LW
1.31	6/2/09	Updated the legal page Updated the default value of D0F3 Rx3-2 Modified the delay format for D0F3 Rx73-70 and Rx77 Updated the package under Mechanical Specifications	LW
1.32	9/9/09	Updated the package under Mechanical Specifications	EY

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CN700 NORTH BRIDGE

800 / 533 / 400 MHz FSB VIA C7 / C7-D / C7-M / Eden / Nano Processor
Integrated UniChrome Pro 3D / 2D Graphics & Video Controller
Advanced 64-bit DDR2 and DDR400 SDRAM Controller
533 MB/Sec V-Link Interface
External 8x / 4x AGP Bus

PRODUCT FEATURES

- **Defines Highly Integrated Solutions for Value Embedded PC Designs**
  - High Performance UMA North Bridge: Integrated VIA C7 North Bridge with 800 / 533 / 400 MHz FSB support and UniChrome Pro 3D / 2D Graphics & Video Controllers in a single chip
  - Advanced 64-bit SDRAM controller supporting DDR2 and DDR400 / 333 / 266 SDRAM
  - Combines with VIA VT8237R Plus / VT8251 Version CD/CE / VT8237S V-Link South Bridge for integrated PCI-Express (VT8251 Version CD/CE), 10 / 100 LAN, HD Audio (VT8251 Version CD/CE / VT8237S), ATA133 IDE, LPC, USB 2.0 and Serial ATA (VT8237R Plus / VT8251 Version CD/CE / VT8237S)
  - 37.5 x 37.5mm HSBGA package (Ball Grid Array with Heat Spreader) with 567 balls and 1.27 mm ball pitch
- **High Performance CPU Interface**
  - Supports 800 / 400 MHz FSB VIA C7 / C7-D / C7-M / Eden processor
  - Supports 800 / 533 MHz FSB VIA Nano processor
  - Supports DBI (Dynamic Bus Inversion)
  - Deep In-Order command Queue (IOQ)
  - Integrated CPU-to-DRAM write buffers and CPU-to-DRAM read prefetch buffers
  - Built-in Phase Lock Loop circuitry for optimal skew control within and between clocking regions
- **Full Featured Accelerated Graphics Port (AGP) Controller**
  - AGP v3.5 compliant 8x / 4x transfer modes with Fast Write support
  - 1.5V AGP I/O interface
  - Pipelined split-transaction long-burst transfers up to 2.1GB/sec
  - Supports Side Band Addressing (SBA) mode
  - Supports Flush / Fence commands
  - Supports DBI (Dynamic Bus Inversion)
  - Pseudo-synchronous AGP and CPU interfaces with optimal skew control
  - Eight level read request queue
  - Four level posted-write request queue
  - Thirty-two level (quad word per level) read and write FIFO, separately
  - Graphics Address Relocation Table (GART)
    - One level TLB structure
    - Eight page direct map page table
    - LRU replacement scheme

- **Advanced High-Performance DDR2 SDRAM Controller**
  - DDR2 Mode
    - Supports DDR2 533 / 400 memory
    - Supports mixed 64 / 128 / 256 / 512 Mb SDRAM in x8 or x16 configurations
    - Supports CL 2 / 3 / 4 / 5 for DDR2 533 / 400
    - Supports 2 unbuffered double-sided DIMMs (4 banks) and up to 2 GB of physical memory
  - DDR Mode
    - Supports DDR400 / 333 / 266 memory types with 2.5V SSTL-2 DRAM interface
    - Supports mixed 64 / 128 / 256 / 512 Mb SDRAM in x8 or x16 configurations
    - Supports CL 2 / 2.5 for DDR266 / 333 and CL 2.5 / 3 for DDR400
    - Supports 2 unbuffered double-sided DIMMs (4 banks) and up to 2 GB of physical memory
  - Programmable I/O drive capability for memory address, data and control signals
  - DRAM interface pseudo-synchronous with host CPU for optimal memory performance
  - Concurrent CPU, AGP, internal graphics controller and V-Link access for minimum memory access latency
  - Rank interleave and up to16-bank page interleave (i.e., 16 pages open simultaneously) based on LRU to effectively reduce memory access latency
  - Seamless DRAM command scheduling for maximum DRAM bus utilization (e.g., precharge other banks while accessing the current bank)
  - CPU Read-Around-Write capability for non-stalled operation
  - Speculative DRAM read before snoop result to reduce PCI master memory read latency
  - Supports Burst Read and Write operations with burst length of 4 or 8
  - Optional dynamic Clock Enable (CKE) control for DRAM power reduction during normal system state (S0)
  - Supports self-refresh and CAS-before-RAS DRAM refresh with staggered RAS timing
- **High Bandwidth 533 MB/Sec 8-bit V-Link Host Controller**
  - Supports 66 MHz, 4x and 8x transfer modes, V-Link interface with 533 MB/sec total bandwidth
  - Half duplex transfers with separate command / strobe for 4x 8-bit mode and full duplex for 8x 4-bit mode
  - Request / Data split-transaction
  - Transaction assurance for V-Link Host-to-Client access eliminates V-Link Host-Client Retry cycles
  - Intelligent V-Link transaction protocol to minimize data wait-state and throttle transfer latency to avoid data overflow
  - Highly efficient V-Link arbitration with minimum overhead
- **Advanced System Power Management Support**
  - ACPI 2.0 and PCI Bus Power Management 1.1 compliant
  - Supports Suspend-to-DRAM (STR) and DRAM self refresh
  - Supports dynamic Clock Enable (CKE) control for DRAM power reduction during normal system state (S0)
  - Supports SMI, SMM and STPCLK mechanisms
  - Low-leakage I/O pads

- **Integrated Graphics with 2D / 3D / Video Controllers**
  - Optimized Unified Memory Architecture (UMA)
  - Supports 16 / 32 / 64 MB Frame Buffers size
  - Graphics engine clocks up to 200 MHz decoupled from memory clock
  - Internal AGP 8x performance
  - Two 128-bit internal data paths between North Bridge and graphics core for frame buffer and texture /command access
  - PCI v2.2 Host Bus compliant
  - AGP v3.5 compliant

2D Acceleration Features

- 128-bit 2D graphics engine
- Supports ROP3, 256 operations
- Supports 8bpp, 15/16bpp and 32bpp color depth modes
- BitBLT (Bit Block Transfer) functions including alpha BLTs
- Color expansion, source Color Key and destination Color Key
- Bresenham line drawing / style line function
- Transparency mode
- Window clipping
- Text function

3D Acceleration Features

3D Graphics Processor

- 128-bit 3D graphics engine
- Dual pixel rendering pipes
- Dual texture units
- Floating-point setup engine
- Internal full 32-bit ARGB format for high rendering quality
- 8K Texture Cache

Capability

- Supports ROP2
- Supports various texture formats, including: 16/32 bbp ARGB, 8 bbp Palletized (ARGB), YUV 422/420 and compressed texture (DXTC)
- Texture sizes up to 2048x2048
- High quality texture filter for Nearest, Linear, Bi-linear, Tri-linear and Anisotropic modes
- Flat and Gouraud shading
- Vertex Fog and Fog Table
- Z-Bias, LOD-Bias, Polygon offset, Edge Anti-aliasing and Alpha Blending
- Bump mapping and cubic mapping
- Hardware Back-Face culling
- Specular Lighting

Performance

- Two textures per pass
- Triangle rate up to 4.5 million polygons per second
- Pixel rate up to 400 million pixels per second for 2 textures each
- Texel bilinear fill rate up to 266 million texels per second
- High quality dithering

Video Acceleration Features

High Quality Video Processor

- RGB555, RGB565, RGB8888 and YUV422 video playback formats
- High quality 5-tap horizontal and 5-tap vertical scaler (up or down) for both horizontal and vertical scaling (linear interpolation for horizontal and vertical p-scaling and filtering for horizontal and vertical down-scaling)
- Independent graphics and video gamma tables
- 2 sets of Color and Chroma key support
- Color enhancement for contrast, hue, saturation and brightness
- YUV-to-RGB color space conversion
- Bob, Weave, Median-filter and Adaptive de-interlacing modes
- 3:2 / 2:2 pull-down detection
- De-blocking mode support
- Combining of many special effects such as filter, scaling up or down, sub-picture blending, de-interlacing and de-blocking to one pass process
- Tear-free double / triple buffer flipping
- Input video vertical blanking or line interrupt
- Video gamma correction

Video Overlay

- Simultaneous graphics and TV video playback overlay
- Supports video window overlays
- Supports both YUV and RGB format Chroma key
- Supports 16 operations for Color and Chroma key
- Hardware sub-picture blending

MPEG Video Playback

- MPEG-2 hardware VLD (Various Length Decode), iDCT and motion compensation for full speed DVD and MPEG-2 playback at full D1 resolution
- High quality DVD and streaming video playback
- DVD playback auto-flipping
- DVD sub-picture playback overlay

DuoView+™ Capability

- Supports multi-monitor and extended desktop for Windows XP
- Provides two independent display engines, each of which can display completely different information at different resolutions, pixel depths and refresh rates
- Improved display flexibility with simultaneous CRT / DVI, CRT / TV, DVI / TV and other combined operations

Full Software Support

- Microsoft DirectX 7.0, 8.0 and 9.0 compatible
- Supports OpenGL™
- Drivers for major operating systems and APIs: Windows XP, Direct3D™, DirectDraw™ and DirectShow™, and OpenGL™ ICD for Windows XP

- **Extensive Display Support for External Video Output**
  - A dedicated CRT interface
  - A dedicated Digital Video Port supports TV-Out interface
  - An AGP-multiplexed 12-bit interface to external DVI transmitter for driving a DVI monitor
  - An AGP-multiplexed 12-bit TV-Out interface to TV encoder

  ### CRT Display
  - CRT display interface with 24-bit true-color RAMDAC up to 300 MHz pixel rate with gamma correction capability
  - Supports CRT resolutions up to 1920x1440

  ### 12-bit DVI Transmitter Interface
  - 12-bit, 1.5V low-swing, DVO interface for connecting DVI Monitor through DVI transmitter
  - 12-bit DDR and clock rate up to 165 MHz
  - Built-in digital phase adjuster to fine tune signal timing between clock and data bus

  ### 24-bit Flat Panel Display Interface
  - Multiplexed with external AGP port pins
  - Supports 18/24-bit FPD interface with external LVDS transmitter chip using single or double-data rate transfer
  - Supports panel resolutions up to 1600x1200

  ### Dual 12-bit Flat Panel Display Interface
  - Alternate operating mode of FPD interface with external LVDS transmitters
  - Single or separate sets of clock and sync signals
  - Supports panel resolutions up to 1600x1200

  ### TV-Out Interface
  - 12-bit Interface to an external TV encoder for SDTV and HDTV display

- **Advanced Graphics Power Management Support**
  - Built-in reference voltage generator and monitor sense circuits
  - Automatic panel power sequencing and VESA DPMS (Display Power Management Signaling) CRT power-down
  - External I/O signal controlling enabling graphics accelerator into standby / suspend-off state
  - Auto clock gating for each engine to achieve power saving
  - I^2C Serial Bus and DDC Monitor Communications for CRT Plug-and-Play configuration

CN700 SYSTEM OVERVIEW

The CN700 is a high performance, cost-effective and energy efficient UMA North Bridge with integrated UniChrome Pro graphics / video controller used for the implementation of embedded systems based on 800 / 533 / 400 MHz FSB VIA C7 / C7-D / C7-M / Eden / Nano super-scalar processor.

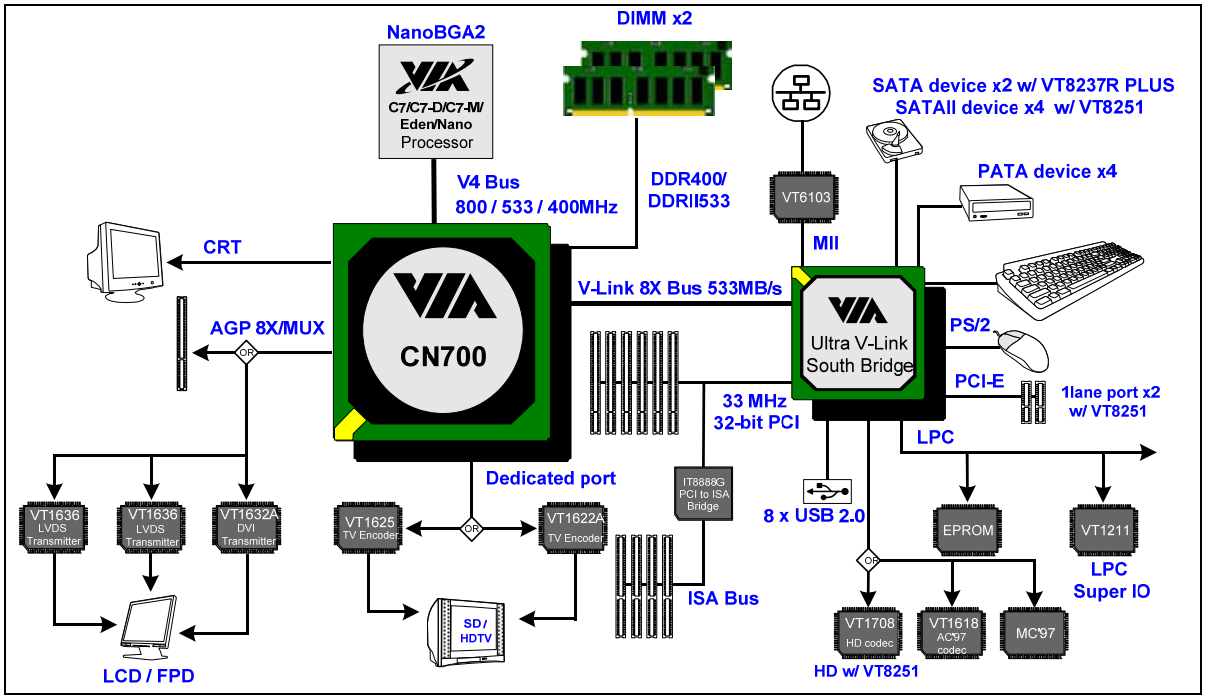


Figure 1. System Block Diagram

The complete embedded system chipset consists of the CN700 North Bridge and the VT8237R Plus V-Link South Bridge. The CN700 integrates VIA's most advanced system controller with high-performance UniChrome Pro 3D / 2D graphics and video controller, DVI monitor and TV-Out interfaces. The CN700 provides superior performance between the CPU, DRAM, V-Link and internal or external AGP 8x graphics controller with pipelined, burst and concurrent operation. The VT8237R Plus is a highly integrated peripheral controller which includes V-Link-to-PCI / V-Link-to-LPC controllers. It also integrates Serial ATA, Ultra DMA IDE, USB 2.0, 10/100 MB networking MAC, AC'97 and system power management controllers. For applications that require PCI-Express support, VT8251 Version CD/CE could be paired with CN700 for additional supports of two 1-Lane PCI-E ports, High Definition Audio and four Serial ATA 2.0 ports.

CN700 Overview

The CN700 supports 800 / 533 / 400 MHz FSB VIA C7 / C7-D / C7-M / Eden / Nano processor. The CN700 implements a deep In-Order Queue to improve system performance for multi-threaded software applications. DBI and V4 bus protocol are supported which effectively reduce overall system power consumption.

The AGP controller is AGP v3.5 compliant with up to 2.1GB/second data transfer rate. It supports pseudo-synchronous AGP and CPU interface to maximize system performance. Deep read and write (256 bytes each) FIFO are integrated for optimal bus utilization and minimum data transfer latency.

The CN700 supports 64-bit memory data bus access and up to 2 double-sided DDR2 533 / 400 or DDR 400 / 333 / 266 SDRAM DIMMs for 2 GB maximum physical memory. The DDR DRAM interface allows zero wait-state data transfer bursting between the DRAM and memory controller's data buffers. The different banks of DRAM can be composed of an arbitrary mixture of 64 / 128 / 256 / 512 Mb SDRAM in x 8 or x16 configurations. The DRAM controller can run either synchronous or pseudo-synchronous with the host CPU bus.

The CN700 North Bridge interfaces to the South Bridge through a high speed (up to 533 MB/sec) 8x 66 MHz Data Transfer interconnect bus called V-Link interface. Deep pre-fetch and post-write buffers are included to allow for concurrent CPU and V-Link operation. The combined CN700 North Bridge and VT8237R Plus South Bridge system supports enhanced PCI bus commands such as "Memory-Read-Line", "Memory-Read-Multiple" and "Memory-Write-Invalid" commands to minimize snoop overhead. In addition, advanced features are supported such as CPU write-back forward to PCI master and CPU write-back merged with PCI post-write buffers to minimize PCI master read latency and DRAM utilization. Delay transaction mechanism is also implemented for further improvement of overall system performance.

System Power Management

For sophisticated power management, the CN700 supports dynamic CKE control to minimize DDR SDRAM power consumption during normal system state (S0). A separate suspend power plane is implemented for the memory control logic for Suspend-to-DRAM state. The CN700 graphics controller implements dynamic clock gating for inactive functions to achieve maximum power saving. The system can be switched to standby or suspend states to further reduce power consumption when idle. VESA DPMS (Display Power Management Signaling) CRT power-down is supported. Coupled with the VT8237R Plus South Bridge chip, a complete power conscious PC main board can be implemented with no external glue logic.

3D Graphics Engine

Featuring an integrated 128-bit 3D graphics engine, the CN700 North Bridge utilizes a single cycle architecture that provides high performance along with superior image quality. Several new features enhance the 3D architecture, including single-pass multitexturing, anisotropic filtering, and an 8-bit stencil buffer. The chip also offers the industry's only simultaneous usage of single-pass multitexturing and single-cycle trilinear filtering – enabling stunning image quality without performance loss. Image quality is further enhanced with true 32-bit color rendering throughout the 3D pipeline to produce more vivid and realistic images. The advanced triangle setup engine provides realistic user experiences in games and other interactive 3D applications. The 3D engine is optimized for AGP texturing from system memory.

2D Graphics Engine

The CN700 North Bridge's advanced 128-bit 2D graphics engine delivers high-speed 2D acceleration for productivity applications. The enhanced 2D architecture with direct access frame buffer capability optimizes UMA performance and provides acceleration of all color depths.

MPEG Video Playback

The CN700 North Bridge provides the ideal architecture for high quality MPEG-2 based video applications. For MPEG playback, the integrated video accelerator offloads the CPU by performing the motion compensation tasks, while its enhanced scaling algorithm delivers incredible full-screen video playback.

LCD, DVI Monitor and TV Output Display Support

The CN700 provides three "Digital Video Port" interfaces: FPDP, GDVP1, and DVP0. The Flat Panel Display Port (FPDP) implements a 24-bit / dual 12-bit interface which is designed to drive a Flat Panel Display via an external LVDS transmitter chip (such as the VIA VT1636). The CN700 can be connected to the external LVDS transmitter chip in either 24-bit or dual-12-bit modes. A wide variety of LCD panels are supported including VGA, SVGA, XGA, SXGA+ and up to UXGA-resolution TFT color panels, in either SDR (1 pixel / clock) or DDR (2 pixels / clock) modes. UXGA and higher resolutions require dual-edge data transfer (DDR) mode, which is supported by the VIA VT1636 LVDS transmitter chip.

One 12-bit "Display Port" interface (GDVP1) is provided (through multiplexing with AGP interface) plus a dedicated 12-bit display port interface. Multiplexing display functions with the AGP bus allows embedded systems to support an external AGP connector for future performance upgrade through the external graphics controller. It also allows add-in cards to be designed with an AGP-compatible connector for implementing the display interface logic to reduce cost in the base (CRT-only) configuration. In the value system configurations, the external AGP upgrade capability is not normally required by the system, allowing all the AGP pins to be used for implementing very flexible display functions.

The multiplexed "Display Port" implements a 12-bit DVI transmitter interface and is normally connected to an external DVI transmitter (such as VIA VT1632A) to drive external DVI monitor. The dedicated 12-bit interface may be configured for support of an external TV encoder (such as VIA VT1622A).

The flexible display configurations of the CN700 allows the support of a Flat Panel Display (FPD) using the LVDS interface, DVI monitor using the DVI Panel interface or TV and CRT display simultaneously. Internally the CN700 North Bridge provides two separate display engines, so if two display devices are connected, each can display completely different information at different resolutions, pixel depths and refresh rates. If more than two display devices are connected, the additional displays must have the same resolution, pixel depth and refresh rate as one of the first two. The maximum display resolutions supported for one display device are listed in the table below. If more than one display is implemented (i.e., if both display engines are functioning at the same time), then available memory bandwidth may limit the display resolutions supported on one or both displays. This will be dependent on many factors including primarily clock rates and memory speeds (contact VIA for additional information).

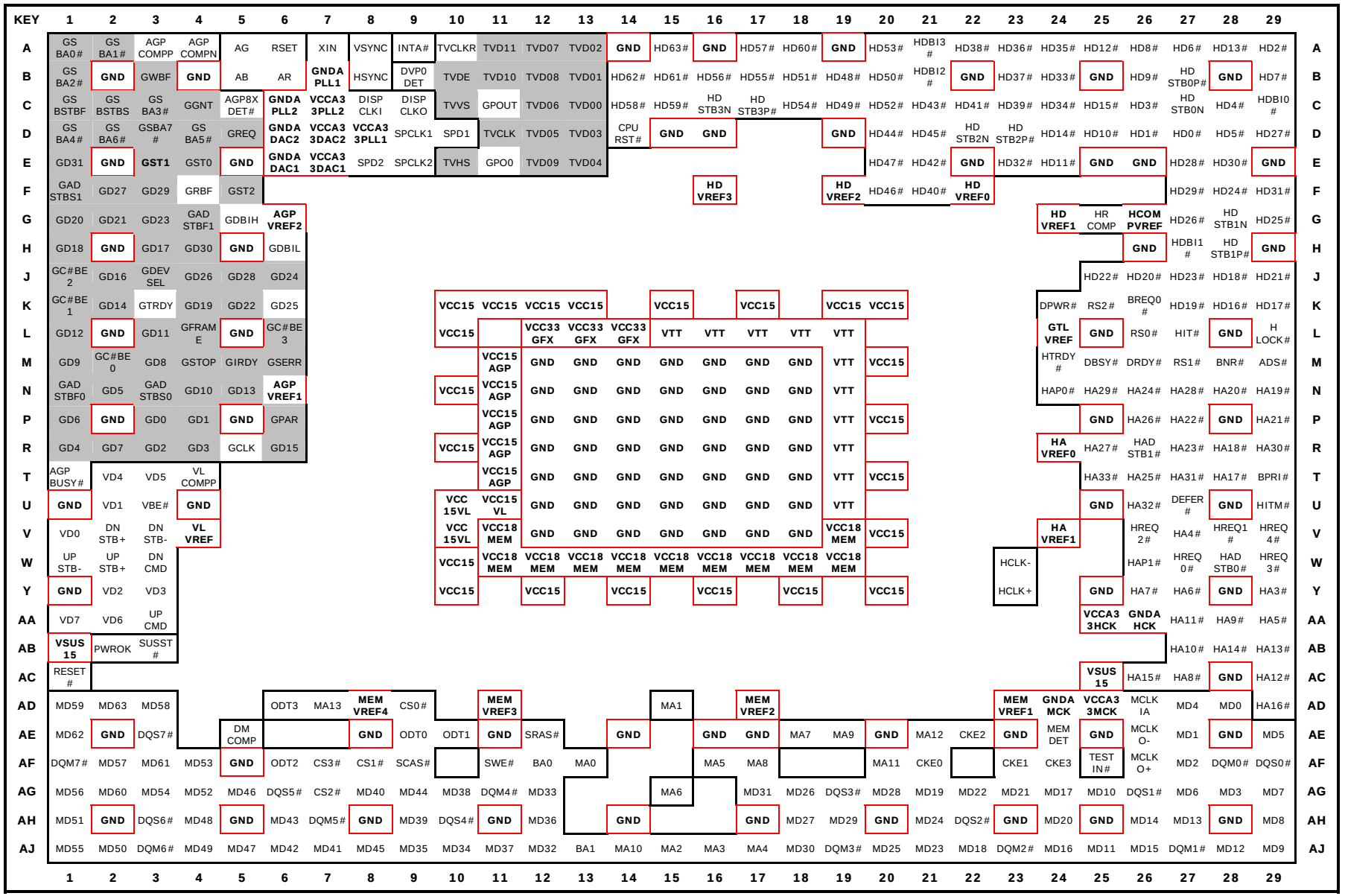
High Screen Resolution Display Support

Resolutions Supported	Resolution Name	Pixel Depths Supported	System Memory Frame Buffer Size		
			16 MB	32 MB	64 MB
640x480 (4:3)	VGA	8 / 16 / 32	✔	✔	✔
800x600 (4:3)	SVGA	8 / 16 / 32	✔	✔	✔
1024x768 (4:3)	XGA	8 / 16 / 32	✔	✔	✔
1280x1024 (5:4)	SXGA	8 / 16 / 32	✔	✔	✔
1400x1050 (4:3)	SXGA+	8 / 16 / 32	✔	✔	✔
1600x1200 (4:3)	UXGA, UXGA+	8 / 16 / 32	✔	✔	✔
1920x1440 (4:3)	—	8 / 16 / 32	✔	✔	✔

Table 1. Supported CRT Resolutions

PINOUT AND PINLIST

Figure 2. CN700 Ball Diagram (Top View)



KEY	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	
A	GS BA0#	GS BA1#	AGP COMPP	AGP COMPN	AG	RSET	XIN	VSYNC	INTA#	TVCLKR	TVD11	TVD07	TVD02	GND	HD63#	GND	HD57#	HD60#	GND	HD53#	HDBI3 #	HD38#	HD36#	HD35#	HD12#	HD8#	HD6#	HD13#	HD2#	A
B	GS BA2#	GND	GWBF	GND	AB	AR	GNDA PLL1	HSYNC	DVP0 DET	TVDE	TVD10	TVD08	TVD01	HD62#	HD61#	HD56#	HD55#	HD51#	HD48#	HD50#	HDBI2 #	GND	HD37#	HD33#	GND	HD9#	HD STB0P#	GND	HD7#	B
C	GS BSTBF	GS BSTBS	GS BA3#	GGNT	AGP8X DET#	GNDA PLL2	VCCA3 3PLL2	DISP CLKI	DISP CLKO	TVVS	GPOUT	TVD06	TVD00	HD58#	HD59#	HD STB3N	HD STB3P#	HD54#	HD49#	HD52#	HD43#	HD41#	HD39#	HD34#	HD15#	HD3#	HD STB0N	HD4#	HDBI0 #	C
D	GS BA4#	GS BA6#	GSBA7 #	GS BA5#	GREQ	GNDA DAC2	VCCA3 3DAC2	VCCA3 3PLL1	SPCLK1	SPD1	TVCLK	TVD05	TVD03	CPU RST#	GND	GND			GND	HD44#	HD45#	HD STB2N	HD STB2P#	HD14#	HD10#	HD1#	HD0#	HD5#	HD27#	D
E	GD31	GND	GST1	GST0	GND	GNDA DAC1	VCCA3 3DAC1	SPD2	SPCLK2	TVHS	GPO0	TVD09	TVD04							HD47#	HD42#	GND	HD32#	HD11#	GND	GND	HD28#	HD30#	GND	E
F	GAD STBS1	GD27	GD29	GRBF	GST2											HD VREF3			HD VREF2	HD46#	HD40#	HD VREF0					HD29#	HD24#	HD31#	F
G	GD20	GD21	GD23	GAD STBF1	GDBIH	AGP VREF2																		HD VREF1	HR COMP	HCOM PVREF	HD26#	HD STB1N	HD25#	G
H	GD18	GND	GD17	GD30	GND	GDBIL																				GND	HDBI1 #	HD STB1P#	GND	H
J	GC#BE 2	GD16	GDEV SEL	GD26	GD28	GD24																			HD22#	HD20#	HD23#	HD18#	HD21#	J
K	GC#BE 1	GD14	GTRDY	GD19	GD22	GD25				VCC15	VCC15	VCC15	VCC15		VCC15		VCC15		VCC15	VCC15				DPWR#	RS2#	BREQ0 #	HD19#	HD16#	HD17#	K
L	GD12	GND	GD11	GFRAM E	GND	GC#BE 3				VCC15		VCC33 GFX	VCC33 GFX	VCC33 GFX	VTT	VTT	VTT	VTT	VTT						GTL VREF	GND	RS0#	HIT#	GND	H LOCK#	L
M	GD9	GC#BE 0	GD8	GSTOP	GIRDY	GSERR					VCC15 AGP	GND	GND	GND	GND	GND	GND	GND	VTT	VCC15					HTRDY #	DBSY#	DRDY#	RS1#	BNR#	ADS#	M
N	GAD STBF0	GD5	GAD STBS0	GD10	GD13	AGP VREF1				VCC15	VCC15 AGP	GND	GND	GND	GND	GND	GND	GND	VTT						HAP0#	HA29#	HA24#	HA28#	HA20#	HA19#	N
P	GD6	GND	GD0	GD1	GND	GPAR					VCC15 AGP	GND	GND	GND	GND	GND	GND	GND	VTT	VCC15					GND	HA26#	HA22#	GND	HA21#	P
R	GD4	GD7	GD2	GD3	GCLK	GD15				VCC15	VCC15 AGP	GND	GND	GND	GND	GND	GND	GND	VTT					HA VREF0	HA27#	HAD STB1#	HA23#	HA18#	HA30#	R
T	AGP BUSY#	VD4	VD5	VL COMPP							VCC15 AGP	GND	GND	GND	GND	GND	GND	GND	VTT	VCC15					HA33#	HA25#	HA31#	HA17#	BPRI#	T
U	GND	VD1	VBE#	GND						VCC 15VL	VCC15 VL	GND	GND	GND	GND	GND	GND	GND	VTT						GND	HA32#	DEFER #	GND	HITM#	U
V	VD0	DN STB+	DN STB-	VL VREF						VCC 15VL	VCC18 MEM	GND	GND	GND	GND	GND	GND	GND	VCC18 MEM	VCC15				HA VREF1		HREQ 2#	HA4#	HREQ1 #	HREQ 4#	V
W	UP STB-	UP STB+	DN CMD							VCC15	VCC18 MEM	VCC18 MEM	VCC18 MEM	VCC18 MEM	VCC18 MEM	VCC18 MEM	VCC18 MEM	VCC18 MEM	VCC18 MEM				HCLK-			HAP1#	HREQ 0#	HAD STB0#	HREQ 3#	W
Y	GND	VD2	VD3							VCC15		VCC15		VCC15		VCC15		VCC15		VCC15			HCLK+		GND	HA7#	HA6#	GND	HA3#	Y
AA	VD7	VD6	UP CMD																						VCCA3 3HCK	GNDA HCK	HA11#	HA9#	HA5#	AA
AB	VSUS 15	PWROK	SUSST #																								HA10#	HA14#	HA13#	AB
AC	RESET #																								VSUS 15	HA15#	HA8#	GND	HA12#	AC
AD	MD59	MD63	MD58			ODT3	MA13	MEM VREF4	CS0#		MEM VREF3				MA1		MEM VREF2						MEM VREF1	GNDA MCK	VCCA3 3MCK	MCLK IA	MD4	MD0	HA16#	AD
AE	MD62	GND	DQS7#		DM COMP			GND	ODT0	ODT1	GND	SRAS#		GND		GND	GND	MA7	MA9	GND	MA12	CKE2	GND	MEM DET	GND	MCLK O-	MD1	GND	MD5	AE
AF	DQM7#	MD57	MD61	MD53	GND	ODT2	CS3#	CS1#	SCAS#		SWE#	BA0	MA0			MA5	MA8			MA11	CKE0		CKE1	CKE3	TEST IN#	MCLK O+	MD2	DQM0#	DQS0#	AF
AG	MD56	MD60	MD54	MD52	MD46	DQS5#	CS2#	MD40	MD44	MD38	DQM4#	MD33			MA6		MD31	MD26	DQS3#	MD28	MD19	MD22	MD21	MD17	MD10	DQS1#	MD6	MD3	MD7	AG
AH	MD51	GND	DQS6#	MD48	GND	MD43	DQM5#	GND	MD39	DQS4#	GND	MD36		GND			GND	MD27	MD29	GND	MD24	DQS2#	GND	MD20	GND	MD14	MD13	GND	MD8	AH
AJ	MD55	MD50	DQM6#	MD49	MD47	MD42	MD41	MD45	MD35	MD34	MD37	MD32	BA1	MA10	MA2	MA3	MA4	MD30	DQM3#	MD25	MD23	MD18	DQM2#	MD16	MD11	MD15	DQM1#	MD12	MD9	AJ
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	

Note: Multiplexed signals are marked in gray. See pin lists and pin descriptions for more information.

Table 2. Pin List – Listed by Pin Name

Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name
B05	AB	A11	DVP0D11	R06	GD15	D02	GSBA6#	A29	HD2#	D22	HDSTB2N#
M29	ADS#	B10	DVP0DE	J02	GD16	D03	GSBA7#	J26	HD20#	D23	HDSTB2P#
A05	AG	B09	DVP0DET	H03	GD17	C01	GSBSTBF	J29	HD21#	C16	HDSTB3N#
C05	AGP8XDET#	E10	DVP0HS	H01	GD18	C02	GSBSTBS	J25	HD22#	C17	HDSTB3P#
T01	AGPBUSY#	C10	DVP0VS	K04	GD19	M06	GSERR	J27	HD23#	L27	HIT#
A04	AGPCOMPN	F05	ENABLT	R03	GD2	E04	GST0	F28	HD24#	U29	HITM#
A03	AGPCOMPP	E03	ENAVDD	G01	GD20	E03	GST1	G29	HD25#	L29	HLOCK#
B06	AR	E04	ENAVEE	G02	GD21	F05	GST2	G27	HD26#	G25	HRCOMP
AF12	BA0	R03	FP1CLK	K05	GD22	M04	GSTOP	D29	HD27#	W27	HREQ0#
AJ13	BA1	M04	FP1CLK#	G03	GD23	K03	GTRDY	E27	HD28#	V28	HREQ1#
M28	BNR#	M06	FP1DE	J06	GD24	B03	GWBF	F27	HD29#	V26	HREQ2#
T29	BPRI#	M03	FP1DET	K06	GD25	AB27	HA10#	C26	HD3#	W29	HREQ3#
K26	BREQ0#	M01	FP1HS	J04	GD26	AA27	HA11#	E28	HD30#	V29	HREQ4#
AF21	CKE0	P06	FP1VS	F02	GD27	AC29	HA12#	F29	HD31#	B08	HSYNC
AF23	CKE1	G02	FPCLK	J05	GD28	AB29	HA13#	E23	HD32#	M24	HTRDY#
AE22	CKE2	B03	FPCLK#	F03	GD29	AB28	HA14#	B24	HD33#	A09	INTA#
AF24	CKE3	L01	FPD00	R04	GD3	AC26	HA15#	C24	HD34#	AF13	MA0
D14	CPURST#	N04	FPD01	H04	GD30	AD29	HA16#	A24	HD35#	AD15	MA1
AD09	CS0#	N03	FPD02	E01	GD31	T28	HA17#	A23	HD36#	AJ14	MA10
AF08	CS1#	M02	FPD03	R01	GD4	R28	HA18#	B23	HD37#	AF20	MA11
AG07	CS2#	N01	FPD04	N02	GD5	N29	HA19#	A22	HD38#	AE21	MA12
AF07	CS3#	R02	FPD05	P01	GD6	N28	HA20#	C23	HD39#	AD07	MA13
M25	DBSY#	P01	FPD06	R02	GD7	P29	HA21#	C28	HD4#	AJ15	MA2
U27	DEFER#	N02	FPD07	M03	GD8	P27	HA22#	F21	HD40#	AJ16	MA3
C08	DISPCLKI	R01	FPD08	M01	GD9	R27	HA23#	C22	HD41#	AJ17	MA4
C09	DISPCLKO	R04	FPD09	G05	GDBIH	N26	HA24#	E21	HD42#	AF16	MA5
AE05	DMCOMP	P03	FPD10	H06	GDBIL	T26	HA25#	C21	HD43#	AG15	MA6
W03	DNCMD	P04	FPD11	J03	GDEVSEL	P26	HA26#	D20	HD44#	AE18	MA7
V03	DNSTB-	G04	FPD12	D02	GDVP1CLK	R25	HA27#	D21	HD45#	AF17	MA8
V02	DNSTB+	K05	FPD13	D03	GDVP1CLK#	N27	HA28#	F20	HD46#	AE19	MA9
K24	DPWR#	G01	FPD14	B01	GDVP1D00	N25	HA29#	E20	HD47#	AD26	MCLKIA
AF28	DQM0#	G03	FPD15	C01	GDVP1D01	Y29	HA3#	B19	HD48#	AE26	MCLKO-
AJ27	DQM1#	H01	FPD16	C02	GDVP1D02	R29	HA30#	C19	HD49#	AF26	MCLKO+
AJ23	DQM2#	H03	FPD17	D04	GDVP1D03	T27	HA31#	D28	HD5#	AD28	MD0
AJ19	DQM3#	J02	FPD18	F02	GDVP1D04	U26	HA32#	B20	HD50#	AE27	MD1
AG11	DQM4#	J01	FPD19	D01	GDVP1D05	T25	HA33#	B18	HD51#	AG25	MD10
AH07	DQM5#	R06	FPD20	F03	GDVP1D06	V27	HA4#	C20	HD52#	AJ25	MD11
AJ03	DQM6#	K02	FPD21	J05	GDVP1D07	AA29	HA5#	A20	HD53#	AJ28	MD12
AF01	DQM7#	N05	FPD22	H04	GDVP1D08	Y27	HA6#	C18	HD54#	AH27	MD13
AF29	DQS0#	L03	FPD23	J06	GDVP1D09	Y26	HA7#	B17	HD55#	AH26	MD14
AG26	DQS1#	K04	FPDE	J04	GDVP1D10	AC27	HA8#	B16	HD56#	AJ26	MD15
AH22	DQS2#	F01	FPDET	L06	GDVP1D11	AA28	HA9#	A17	HD57#	AJ24	MD16
AG19	DQS3#	L04	FPHS	A02	GDVP1DE	W28	HADSTB0#	C14	HD58#	AG24	MD17
AH10	DQS4#	J03	FPVS	E01	GDVP1DET	R26	HADSTB1#	C15	HD59#	AJ22	MD18
AG06	DQS5#	N01	GADSTBF0	C03	GDVP1HS	N24	HAP0#	A27	HD6#	AG21	MD19
AH03	DQS6#	G04	GADSTBF1	A01	GDVP1VS	W26	HAP1#	A18	HD60#	AF27	MD2
AE03	DQS7#	N03	GADSTBS0	L04	GFRAME	W23	HCLK-	B15	HD61#	AH24	MD20
M26	DRDY#	F01	GADSTBS1	C04	GGNT	Y23	HCLK+	B14	HD62#	AG23	MD21
D11	DVP0CLK	M02	GC#BE0	M05	GIRDY	D27	HD0#	A15	HD63#	AG22	MD22
C13	DVP0D00	K01	GC#BE1	P06	GPAR	D26	HD1#	B29	HD7#	AJ21	MD23
B13	DVP0D01	J01	GC#BE2	E11	GPO0	D25	HD10#	A26	HD8#	AH21	MD24
A13	DVP0D02	L06	GC#BE3	C11	GPOUT	E24	HD11#	B26	HD9#	AJ20	MD25
D13	DVP0D03	R05	GCLK	F04	GRBF	A25	HD12#	C29	HDBI0#	AG18	MD26
E13	DVP0D04	P03	GD0	D05	GREQ	A28	HD13#	H27	HDBI1#	AH18	MD27
D12	DVP0D05	P04	GD1	A01	GSBA0#	D24	HD14#	B21	HDBI2#	AG20	MD28
C12	DVP0D06	N04	GD10	A02	GSBA1#	C25	HD15#	A21	HDBI3#	AH19	MD29
A12	DVP0D07	L03	GD11	B01	GSBA2#	K28	HD16#	C27	HDSTB0N#	AG28	MD3
B12	DVP0D08	L01	GD12	C03	GSBA3#	K29	HD17#	B27	HDSTB0P#	AJ18	MD30
E12	DVP0D09	N05	GD13	D01	GSBA4#	J28	HD18#	G28	HDSTB1N#	AG17	MD31
B11	DVP0D10	K02	GD14	D04	GSBA5#	K27	HD19#	H28	HDSTB1P#	AJ12	MD32

Note: Multiplexed signals are marked in gray.

Table 3. Pin List – Listed by Pin Name (continued)

Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name
AG12	MD33	AH04	MD48	AE01	MD62	D05	SBDDCCLK	B13	TVD01	W02	UPSTB+
AJ10	MD34	AJ04	MD49	AD02	MD63	C04	SBDDCDAT	A13	TVD02	U03	VBE#
AJ09	MD35	AE29	MD5	AG29	MD7	M05	SBPLCLK	D13	TVD03	V01	VD0
AH12	MD36	AJ02	MD50	AH29	MD8	K01	SBPLDAT	E13	TVD04	U02	VD1
AJ11	MD37	AH01	MD51	AJ29	MD9	AF09	SCAS#	D12	TVD05	Y02	VD2
AG10	MD38	AG04	MD52	AE24	MEMDET	D09	SPCLK1	C12	TVD06	Y03	VD3
AH09	MD39	AF04	MD53	AE09	ODT0	E09	SPCLK2	A12	TVD07	T02	VD4
AD27	MD4	AG03	MD54	AE10	ODT1	D10	SPD1	B12	TVD08	T03	VD5
AG08	MD40	AJ01	MD55	AF06	ODT2	E08	SPD2	E12	TVD09	AA02	VD6
AJ07	MD41	AG01	MD56	AD06	ODT3	AE12	SRAS#	B11	TVD10	AA01	VD7
AJ06	MD42	AF02	MD57	AB02	PWROK	AB03	SUSST#	A11	TVD11	T04	VLCOMPP
AH06	MD43	AD03	MD58	AC01	RESET#	AF11	SWE#	B10	TVDE	A08	VSYNC
AG09	MD44	AD01	MD59	L26	RS0#	AF25	TESTIN#	E10	TVHS	A07	XIN
AJ08	MD45	AG27	MD6	M27	RS1#	D11	TVCLK	C10	TVVS		
AG05	MD46	AG02	MD60	K25	RS2#	A10	TVCLKR	AA03	UPCMD		
AJ05	MD47	AF03	MD61	A06	RSET	C13	TVD00	W01	UPSTB-		

Note: Multiplexed signals are marked in gray.

Table 4. Pin List – Power-Related Pins

Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name
N06	AGPVREF1	M17	GND	T17	GND	AE25	GND	K11	VCC15	W12	VCC18MEM
G06	AGPVREF2	M18	GND	T18	GND	AE28	GND	K12	VCC15	W13	VCC18MEM
A14	GND	N12	GND	U01	GND	AF05	GND	K13	VCC15	W14	VCC18MEM
A16	GND	N13	GND	U04	GND	AH02	GND	K15	VCC15	W15	VCC18MEM
A19	GND	N14	GND	U12	GND	AH05	GND	K17	VCC15	W16	VCC18MEM
B02	GND	N15	GND	U13	GND	AH08	GND	K19	VCC15	W17	VCC18MEM
B04	GND	N16	GND	U14	GND	AH11	GND	K20	VCC15	W18	VCC18MEM
B22	GND	N17	GND	U15	GND	AH14	GND	L10	VCC15	W19	VCC18MEM
B25	GND	N18	GND	U16	GND	AH17	GND	M20	VCC15	L12	VCC33GFX
B28	GND	P02	GND	U17	GND	AH20	GND	N10	VCC15	L13	VCC33GFX
D15	GND	P05	GND	U18	GND	AH23	GND	P20	VCC15	L14	VCC33GFX
D16	GND	P12	GND	U25	GND	AH25	GND	R10	VCC15	E07	VCCA33DAC1
D19	GND	P13	GND	U28	GND	AH28	GND	T20	VCC15	D07	VCCA33DAC2
E02	GND	P14	GND	V12	GND	E06	GNDADAC1	V20	VCC15	AA25	VCCA33HCK
E05	GND	P15	GND	V13	GND	D06	GNDADAC2	W10	VCC15	AD25	VCCA33MCK
E22	GND	P16	GND	V14	GND	AA26	GNDAHCK	Y10	VCC15	D08	VCCA33PLL1
E25	GND	P17	GND	V15	GND	AD24	GNDAMCK	Y12	VCC15	C07	VCCA33PLL2
E26	GND	P18	GND	V16	GND	B07	GNDAPLL1	Y14	VCC15	V04	VLVREF
E29	GND	P25	GND	V17	GND	C06	GNDAPLL2	Y16	VCC15	AB01	VSUS15
H02	GND	P28	GND	V18	GND	L24	GTLVREF	Y18	VCC15	AC25	VSUS15
H05	GND	R12	GND	Y01	GND	R24	HAVREF0	Y20	VCC15	L15	VTT
H26	GND	R13	GND	Y25	GND	V24	HAVREF1	M11	VCC15AGP	L16	VTT
H29	GND	R14	GND	Y28	GND	G26	HCOMPVREF	N11	VCC15AGP	L17	VTT
L02	GND	R15	GND	AC28	GND	F22	HDVREF0	P11	VCC15AGP	L18	VTT
L05	GND	R16	GND	AE02	GND	G24	HDVREF1	R11	VCC15AGP	L19	VTT
L25	GND	R17	GND	AE08	GND	F19	HDVREF2	T11	VCC15AGP	M19	VTT
L28	GND	R18	GND	AE11	GND	F16	HDVREF3	U10	VCC15VL	N19	VTT
M12	GND	T12	GND	AE14	GND	AD23	MEMVREF1	U11	VCC15VL	P19	VTT
M13	GND	T13	GND	AE16	GND	AD17	MEMVREF2	V10	VCC15VL	R19	VTT
M14	GND	T14	GND	AE17	GND	AD11	MEMVREF3	V11	VCC18MEM	T19	VTT
M15	GND	T15	GND	AE20	GND	AD08	MEMVREF4	V19	VCC18MEM	U19	VTT
M16	GND	T16	GND	AE23	GND	K10	VCC15	W11	VCC18MEM		

PIN DESCRIPTIONS

CPU Interface Pin Descriptions

CPU Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
HA[33:3]#	(see pin lists)	IO	**Host Data Address.** **(V4 Host Protocol)** Host data addresses are transferred in 4X rate. On beat 0 and 2, address bits HA[30, 16:3]# are transferred on signal balls HA[30, 16:3]#. On beat 1 and 3, address bits HA[31, HAP, 29:17]# are transferred on signal balls HA[30, 16:3]#.
HADSTB0P# (muxed with HADSTB0#) **HADSTB0N#** (muxed with HAP1#) **HADSTB1#**	W28 W26 R26	IO	**Host Address Strobe.** **(V4 Host Protocol)** HADSTB0P# / HADSTB0N# (ball locations: W28, W26) are differential synchronous strobes used to transfer HA[31:3]# and HREQ[4:0]# at a 4x transfer rate.
HAP[1:0]#	W26, N24	IO	**Host Address Parity.**
HD[63:0]#	(see pin lists)	IO	**Host CPU Data.** These signals are connected to the CPU data bus.
HDBI[3:0]#	A21, B21, H27, C29	IO	**Host CPU Dynamic Bus Inversion.** Driven along with HD[63:0]# to indicate if the associated signals are inverted or not. Used to limit the number of simultaneously switching signals to 8 for the associated 16-bit data pin group (HDBI3# for HD[63:48]#, HDBI2# for HD[47:32]#, HDBI1# for HD[31:16]#, and HDBI0# for HD[15:0]#). HDBIn# is asserted such that the number of data bits driven low for the corresponding group does not exceed 8.
HDSTB[3:0]P# **HDSTB[3:0]N#**	C17, D23, H28, B27 C16, D22, G28, C27	IO	**Host CPU Differential Data Strobes.** Source synchronous strobes used to transfer HD[63:0]# and HDBI[3:0]# at a 4x transfer rate. HDSTB3P# / HDSTB3N# are the strobes for HD[63:48]# & HDBI3#; HDSTB2P# / HDSTB2N# are the strobes for HD[47:32]# & HDBI2#; HDSTB1P# / HDSTB1N# are the strobes for HD[31:16]# & HDBI1#; and HDSTB0P# / HDSTB0N# are the strobes for HD[15:0]# & HDBI0#.

CPU Interface (continued)			
ADS#	M29	IO	**Address Strobe**. The CPU asserts ADS# in T1 of the CPU bus cycle.
DBSY#	M25	IO	**Data Bus Busy**. Used by the data bus owner to hold the data bus for transfers requiring more than one cycle.
DRDY#	M26	IO	**Data Ready**. Asserted for each cycle that data is transferred.
HIT#	L27	IO	**Hit**. Indicates that a caching agent holds an unmodified version of the requested line. Also driven in conjunction with HITM# by the target to extend the snoop window.
HITM#	U29	I	**Hit Modified**. Asserted by the CPU to indicate that the address is modified in the L1 cache and needs to be written back.
HLOCK#	L29	I	**Host Lock**. All CPU cycles sampled with the assertion of HLOCK# and ADS# until the negation of HLOCK# must be atomic.
HREQ[4:0]#	V29, W29, V26, V28, W27	IO	**Host Request Command**. **(V4 Host Protocol)** Host request commands are transferred in 4X rate. On beat 0 and 2, host request bits HREQ[2:0]# on transferred on signal balls HREQ[2:0]#. On beat 1 and 3, host request bits HREQ[4:3]# are transferred on signal balls HREQ[1:0]#.
HTRDY#	M24	IO	**Host Target Ready**. Indicates that the target of the processor transaction is able to enter the data transfer phase.

Note: Clocking of the CPU interface is performed with HCLK+ and HCLK– (see clock pin description group).

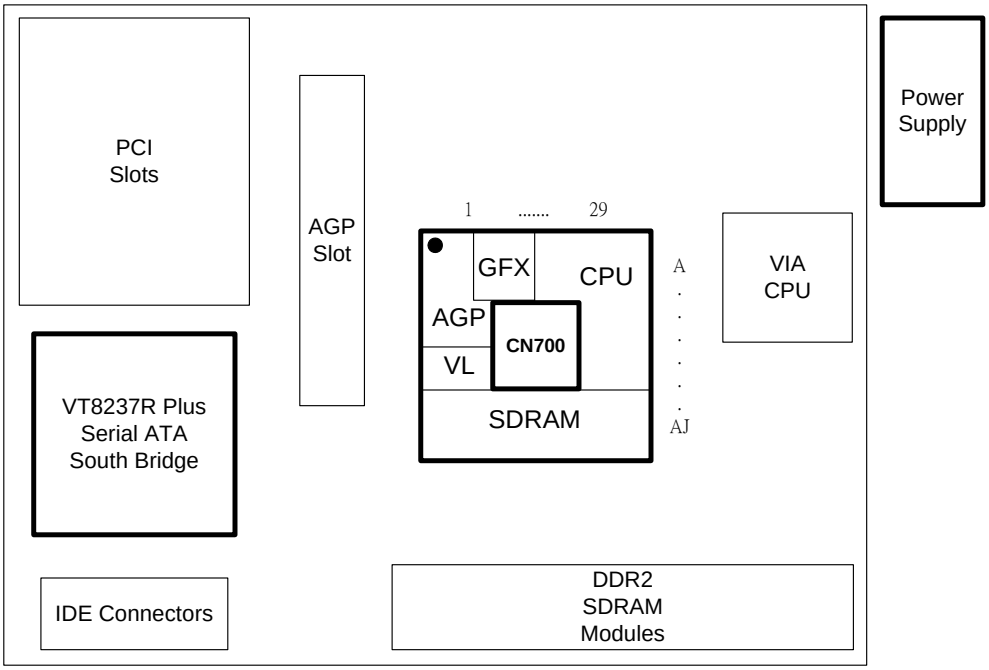
Note: Internal pullup resistors are provided on all AGTL+ interface pins. If the CPU does not have internal pullups, these North Bridge internal pullups may be enabled to allow the interface to meet AGTL+ bus interface specs (see VD3 strap).

Note: I/O pads for the above pins are powered by VTT. Input voltage levels are referenced to HAVREF, HDVREF & GTLVREF.

CPU Interface (continued)			
Signal Name	**Pin #**	**I/O**	**Signal Description**
RS[2:0]#	K25, M27, L26	IO	**Response Signals**. Indicates the type of response per the table below: **RS[2:0]# Response type** / **RS[2:0]# Response type** 000 Idle State / 100 Hard Failure 001 Retry Response / 101 Normal Without Data 010 Defer Response / 110 Implicit Writeback 011 Reserved / 111 Normal With Data
DPWR#	K24	O	**Data Bus Power Reduction.** Request to reduce power on the mobile CPU data bus input buffer. Connect to mobile CPU if used.
BREQ0#	K26	O	**Bus Request 0.** Bus request output to CPU.
BPRI#	T29	IO	**Priority Agent Bus Request**. The owner of this signal will always be the next bus owner. This signal has priority over symmetric bus requests and causes the current symmetric owner to stop issuing new transactions unless the HLOCK# signal is asserted. The CN700 drives this signal to gain control of the processor bus.
BNR#	M28	IO	**Block Next Request**. Used to block the current request bus owner from issuing new requests. This signal is used to dynamically control the processor bus pipeline depth.
DEFER#	U27	IO	**Defer**. The CN700 uses a dynamic deferring policy to optimize system performance. The CN700 also uses the DEFER# signal to indicate a processor retry response.
CPURST#	D14	O	**CPU Reset.** Reset output to CPU. External pullup and filter capacitor to ground should be provided per CPU manufacturer's recommendations.

Note: I/O pads for the above pins are powered by VTT. Input voltage levels are referenced to HAVREF, HDVREF, & GTLVREF.

The pinouts were defined assuming the ATX PCB layout model shown below (and general pin layout shown) as a guide for PCB component placement. Other PCB layouts (AT, LPX, and NLX) were also considered and can typically follow the same general component placement.



DDR SDRAM Memory Controller Pin Descriptions

DRAM Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
MD[63:0]	(see pin lists)	IO	**Memory Data.** These signals are connected to the DRAM data bus.
MA[13:0]	(see pin lists)	O	**Memory Address.** DRAM address lines.
SRAS#, **SCAS#, SWE#**	AE12, AF9, AF11	O	**Row Address, Column Address and Write Enable Command Indicator Set.**
CS[3:0]#	AF7, AG7, AF8, AD9	O	**Chip Select.** Chip select of each bank.
DQM[7:0]#	AF1, AJ3, AH7, AG11, AJ19, AJ23, AJ27, AF28	O	**DDR Data Mask.** Data mask of each byte lane.
DQS[7:0]#	AE3, AH3, AG06, AH10, AG19, AH22, AG26, AF29	IO	**DDR Data Strobe.** Data strobe of each byte.
CKE[3:0]	AF24, AE22, AF23, AF21	O	**Clock Enables.** Clock enables for each DRAM bank for powering down the SDRAM or clock control for reducing power usage and for reducing heat / temperature in high-speed memory systems.
ODT[3:0]	AD6, AF6, AE10, AE9	O	**On Die Termination.** Enables termination resistance internal to the DDR2 SDRAM
MEMDET	AE24	I	**Memory Detect:** Strap low for DDR and high for DDR2.
BA[1:0]	AF12, AJ13	O	**DRAM Bank Address.** Defines which bank will receive an ACTIVE, READ, WRITE or PRECHARGE command.

Note: I/O pads for all SDRAM pins are powered by VCC18MEM. MD / DQS input voltage levels are referenced to MEMVREF.

Accelerated Graphics Port Pin Descriptions

AGP 3.5 Bus Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
GD[31:0]	(see pin list)	IO	**Address / Data Bus.** Address is driven with GADSTB assertion for AGP-style transfers and with GFRAME assertion for PCI-style transfers.
GC#BE[3:0]	L6 J1 K1 M2	IO	**Command / Byte Enable.** For AGP cycles these pins provide command information (different commands than for PCI) driven by the master (graphics controller). These pins provide valid byte information during AGP write transactions and are driven by the master. The target (this chip) drives these lines to "0000" during the return of AGP read data. For PCI cycles, commands are driven with GFRAME assertion. Byte enables corresponding to supplied or requested data are driven on following clocks.
GPAR	P6	IO	**AGP Parity.** A single parity bit is provided over GD[31:0] and GC#BE[3:0].
GDBIH / GDBIL	G5 H6	IO	**Dynamic Bus Inversion High / Low.** AGP 8x transfer mode only. Driven by the source to indicate whether the corresponding data bit group (GDBIH for GD[31:16] and GDBIL for GD[15:0]) needs to be inverted on the receiving end (1 on GDBIx indicates that the corresponding data bit group should be inverted). Used to limit the number of simultaneously switching outputs to 8 for each 16-pin group.
GADSTBF0 **GADSTBS0**	N1 N3	IO	**Bus Strobe 0.** Source synchronous strobes for GD[15:0] (the agent that is providing the data drives these signals). For 8x transfer mode, GADSTB0 is interpreted as GADSTBF0 ("First" strobe) and GADSTB0# as GADSTBS0 ("Second" strobe).
GADSTBF1 **GADSTBS1**	G4 F1	IO	**Bus Strobe 1.** Source synchronous strobes for GD[31:16] (i.e., the agent that is providing the data drives these signals). For 8x transfer mode, GADSTB1 is interpreted as GADSTBF1 ("First" strobe) and GADSTB1# as GADSTBS1 ("Second" strobe).
GFRAME	L4	IO	**Frame.** Assertion indicates the address phase of a PCI transfer. Negation indicates that one more data transfer is desired by the cycle initiator.
GDEVSEL	J3	IO	**Device Select (PCI transactions only).** Driven by the North Bridge when a PCI initiator is attempting to access main memory. Input when the chip is acting as PCI initiator. Not used for AGP cycles.
GIRDY	M5	IO	**Initiator Ready.** For AGP write cycles, the assertion of this pin indicates that the master is ready to provide all write data for the current transaction. Once this pin is asserted, the master is not allowed to insert wait states. For AGP read cycles, the assertion of this pin indicates that the master is ready to transfer a subsequent block of read data. The master is *never* allowed to insert a wait state during the initial block of a read transaction. However, it may insert wait states after each block transfers. For PCI cycles, asserted when initiator is ready for data transfer.
GTRDY	K3	IO	**Target Ready.** For AGP cycles, indicates that the target is ready to provide read data for the entire transaction (when the transaction can complete within four clocks) or is ready to transfer a (initial or subsequent) block of data when the transfer requires more than four clocks to complete. The target is allowed to insert wait states after each block transfer for both read and write transactions. For PCI cycles, asserted when target is ready for data transfer.

Note: I/O pads for all pins on this page are powered by VCC15AGP. Input voltage levels are referenced to AGPVREF.

Note: The AGP interface pins can be optionally configured as additional interfaces for connecting to external display devices. For simplification of the AGP pin description tables above and on the next page, that multiplexing is not shown.

AGP 3.5 Bus Interface (continued)			
Signal Name	**Pin #**	**I/O**	**Signal Description**
AGP8XDET#	C5	I	**AGP 8x Transfer Mode Detect.** Low indicates that the external graphics card can support 8x transfer mode.
GRBF	F4	I	**Read Buffer Full.** Indicates if the master (graphics controller) is ready to accept previously requested low priority read data. When GRBF is asserted, the North Bridge will not return low priority read data to the graphics controller.
GWBF	B3	I	**Write Buffer Full.**
GSBA[7:0]#	D3, D2, D4, D1, C3, B1, A2, A1	I	**Side Band Address.** Provides an additional bus to pass address and command information from the master (graphics controller) to the target (North Bridge). These pins are ignored until enabled.
GSBSTBF **GSBSTBS**	C1 C2	I	**Side Band Strobe.** Driven by the master to provide timing for GSBA[7:0]. 8x mode uses GSBSTBF ("First" strobe) and GSBSTBS ("Second" strobe).
GST[2:0]	F5, E3, E4	O	**Status (AGP only).** Provides information from the arbiter to a master to indicate what it may do. Only valid while GGNT is asserted. 000 Indicates that previously requested low priority read or flush data is being returned to the master (graphics controller). 001 Indicates that previously requested high priority read data is being returned to the master. 010 Indicates that the master is to provide low priority write data for a previously enqueued write command. 011 Indicates that the master is to provide high priority write data for a previously enqueued write command. 100 Reserved. (arbiter must not issue, may be defined in the future). 101 Reserved. (arbiter must not issue, may be defined in the future). 110 Reserved. (arbiter must not issue, may be defined in the future). 111 Indicates that the master (graphics controller) has been given permission to start a bus transaction. GST[2:0] are always outputs from the target (North Bridge) & inputs to the master (graphics controller).
GREQ	D5	I	**Request.** Master (graphics controller) request for use of the AGP bus.
GGNT	C4	O	**Grant.** Permission is given to the master (graphics controller) to use the AGP bus.
GSERR	M6	IO	**System Error.**
GSTOP	M4	IO	**Stop.** Asserted by the target to request the master to stop the current transaction.

Note: I/O pads for all pins on this page are powered by VCC15AGP. Input voltage levels are referenced to AGPVREF.

Note: The AGP interface pins can be optionally configured as additional interfaces for connecting to external display devices. For simplification of the AGP pin description tables above and on the next page, that multiplexing is not shown here.

Note: Separate system interrupts are not provided for AGP. The AGP connector provides interrupts via PCI bus INTA#.

Note: A separate reset is not required for the AGP bus (RESET# resets both PCI and AGP buses)

Note: The AGP bus to uses the GSBA port to enqueue master requests (send addresses unmultiplexed). AGP masters implements it at the time of initialization. GRBF has an internal pullup to maintain it in the de-asserted state in case it is not implemented on the master device.

Note: AGP 8x signal levels are 0V and 0.8V. AGP 8x mode maintains most signals at a low level when inactive resulting in no current flow.

V-Link Pin Descriptions

V-Link Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
VD7, **VD6,** **VD5**, **VD4**, **VD3**, **VD2**, **VD1**, **VD0**	AA1 AA2 T3 T2 Y3 Y2 U2 V1	IO IO IO IO IO IO IO IO	**V-Link Data Bus.** During system initialization, VD[7:0] are used to transmit strap information from the South Bridge (the straps are not on the VD pins but are on the indicated pins of the South Bridge chip). Check the strap pin table for details.
VBE#	U3	IO	**V-Link Byte Enable.**
UPCMD	AA3	I	**V-Link Command from Client (South Bridge) to Host (North Bridge).**
UPSTB+	W2	I	**V-Link Strobe from Client to Host.**
UPSTB–	W1	I	**V-Link Complement Strobe from Client to Host.**
DNCMD	W3	O	**V-Link Command from Host (North Bridge) to Client (South Bridge).**
DNSTB+	V2	O	**V-Link Strobe from Host to Client.**
DNSTB–	V3	O	**V-Link Complement Strobe from Host to Client.**

Note: I/O pads for the pins in the above table are powered by VCC15VL. Input voltage levels are referenced to VLVREF.

CRT and Serial Bus Pin Descriptions

CRT Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
AR	B6	AO	**Analog Red.** Analog red output to the CRT monitor.
AB	B5	AO	**Analog Blue.** Analog blue output to the CRT monitor.
AG	A5	AO	**Analog Green.** Analog green output to the CRT monitor.
HSYNC	B8	O	**Horizontal Sync.** Output to CRT.
VSYNC	A8	O	**Vertical Sync.** Output to CRT.
RSET	A6	AI	**Reference Resistor.** Tie to GND through an external 80.6Ω 1% resistor to control the RAMDAC full-scale current value.

I/O pads for the pins in the above table are powered by VCC33GFX (i.e., 3.3V I/O).

SMB / I^2C Interface				
Signal Name	**AGP Name**	**Pin #**	**I/O**	**Signal Description**
SBPLCLK	GIRDY	M5	IO	**I^2C Serial Bus Clock for Panel (Muxed on AGP Bus Pins).**
SBPLDAT	GC#BE1	K1	IO	**I^2C Serial Bus Data for Panel (Muxed on AGP Bus Pins).**
SBDDCCLK	GREQ	D5	IO	**I^2C Serial Bus Clock for CRT DDC (Muxed on AGP Bus Pins).**
SBDDCDAT	GGNT	C4	IO	**I^2C Serial Bus Data for CRT DDC (Muxed on AGP Bus Pins).**
SPCLK2 **SPCLK1** **SPD2,** **SPD1**	n/a n/a n/a n/a	E9 D9 E8 D10	IO	**Serial Port (SMB/I^2C) Clock and Data.** The SPCLKn pins are the clocks for serial data transfer. The SPDn pins are the data signals used for serial data transfer. SPxxx1 is typically used for DVI monitor communications and SPxxx2 is typically used for DDC for CRT monitor communications.

I/O pads for SPCLK[2:1] / SPDAT[2:1] above are powered by VCC33GFX (i.e., 3.3V I/O).
All other pins in the above table are powered by VCC15AGP (i.e., 1.5V I/O).

Dedicated Digital Video Port 0 (DVP0) Pin Descriptions

The DVP0 dedicated Digital Video Port can be configured as a TV Encoder interface port, selectable via strap pins DVP0D[6:4] (see the TV Encoder Interface pin descriptions for details)..

Dedicated Digital Video Port 0 (DVP0)			
Signal Name	**Pin #**	**I/O**	**Signal Description**
DVP0D11 / TVD11, **DVP0D10** / TVD10, **DVP0D9** / TVD9, **DVP0D8** / TVD8, **DVP0D7** / TVD7, **DVP0D6** / TVD6, **DVP0D5** / TVD5, **DVP0D4** / TVD4, **DVP0D3** / TVD3, **DVP0D2** / TVD2, **DVP0D1** / TVD1, **DVP0D0** / TVD0	A11 B11 E12 B12 A12 C12 D12 E13 D13 A13 B13 C13	O	**Digital Video Port 0 Data.** Default output drive is 8 mA. NOTE: DVP0D[6:0] are also used for power-up reset straps for the embedded graphics controller. Check the Strap Pin table for details.
DVP0HS / TVHS	E10	O	**Digital Video Port 0 Horizontal Sync.** Internally pulled down.
DVP0VS / TVVS	C10	O	**Digital Video Port 0 Vertical Sync.** Internally pulled down.
DVP0DE / TVDE	B10	O	**Digital Video Port 0 Data Enable.** Internally pulled down.
DVP0DET	B9	I	**Digital Video Port 0 Display Detect.**
DVP0CLK / TVCLK	D11	O	**Digital Video Port 0 Clock.** Internally pulled down.

The terminology “3C5.nn” above refers to the VGA “Sequencer” registers at I/O port 3C5 index “nn”

Dedicated Digital Video Port 0 (DVP0) - TV Encoder Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
TVD11 / DVP0D11 **TVD10** / DVP0D10, **TVD9** / DVP0D9, **TVD8** / DVP0D8, **TVD7** / DVP0D7, **TVD6** / DVP0D6, **TVD5** / DVP0D5, **TVD4** / DVP0D4, **TVD3** / DVP0D3, **TVD2** / DVP0D2, **TVD1** / DVP0D1, **TVD0** / DVP0D0	A11 B11 E12 B12 A12 C12 D12 E13 D13 A13 B13 C13	O	**TV Encoder 0 Data.** To configure DVP0 as a TV Out interface port, pins DVP0D[6:5] must be strapped high. Note: The CN700 North Bridge supports one TV Encoder interface through DVP0.
TVHS / DVP0HS	E10	O	**TV Encoder 0 Horizontal Sync.** Internally pulled down.
TVVS / DVP0VS	C10	O	**TV Encoder 0 Vertical Sync.** Internally pulled down.
TVDE / DVP0DE	B10	O	**TV Encoder 0 Display Enable.** Internally pulled down.
TVCLKR	A10	I	**TV Encoder 0 Clock In.** Input from TV encoder. Internally pulled down.
TVCLK / DVP0CLK	D11	O	**TV Encoder 0 Clock Out.** Output to TV encoder. Internally pulled down.

The above pins may be connected to an external TV Encoder chip such as a VIA VT1622A for driving a TV set.
I/O pads for the pins on this page are powered by VCC33GFX (3.3V I/O).

AGP-Multiplexed Digital Video Port 0 (GDVP0) Pin Descriptions

The GDVP0 Digital Video Port is supported through multiplexing its interface signal pins with AGP pins. It is used as a TV Encoder interface port.

AGP-Multiplexed Digital Video Port 0 (GDVP0) - TV Encoder Interface				
Signal Name	**AGP Name**	**Pin #**	**I/O**	**Signal Description**
GTVD11, **GTVD10,** **GTVD9,** **GTVD8,** **GTVD7,** **GTVD6,** **GTVD5,** **GTVD4,** **GTVD3,** **GTVD2,** **GTVD1,** **GTVD0**	GD11 GD13 GD14 GD15 GC#BE2 GD16 GD17 GD18 GD23 GD20 GD22 GADSTB1F	L3 N5 K2 R6 J1 J2 H3 H1 G3 G1 K5 G4	O	**TV Encoder Data.** The CN700 North Bridge supports one TV Encoder interface through either GDVP0 or DVP0.
GTVHS	GFRAME	L4	O	**TV Encoder Horizontal Sync.**
GTVVS	GDEVSEL	J3	O	**TV Encoder Vertical Sync.**
GTVDE	GD19	K4	O	**TV Encoder Data Enable.**
GTVCLKIN	GADSTBS1	F1	I	**TV Encoder Clock In.** Input from TV encoder. Internal pull down.
GTVCLK	GD21	G2	O	**TV Encoder Clock Out.** Output to TV encoder. Internally pulled down.
GTVCLK#	GWBF	B3	O	**TV Encoder Clock Out Complement.** Output to TV encoder. Internally pulled down.

AGP-Multiplexed Digital Video Port 1 (GDVP1) Signal Descriptions

The GDVP1 Digital Video Port is supported through multiplexing its interface signals with AGP signals. It is used as a DVI Transmitter interface port.

AGP-Multiplexed Digital Video Port 1 (GDVP1) – DVI Interface				
Signal Name	**AGP Name**	**Ball #**	**I/O**	**Signal Description**
GDVP1D11, **GDVP1D10**, **GDVP1D9**, **GDVP1D8**, **GDVP1D7**, **GDVP1D6**, **GDVP1D5**, **GDVP1D4**, **GDVP1D3**, **GDVP1D2**, **GDVP1D1**, **GDVP1D0**,	GC#BE3 GD26 GD24 GD30 GD28 GD29 GSBA4# GD27 GSBA5# GSBSTBS GSBSTBF GSBA2#	L06 J04 J06 H04 J05 F03 D01 F02 D04 C02 C01 B01	O	**Data.**
GDVP1HS	GSBA3#	C03	O	**Horizontal Sync.**
GDVP1VS	GSBA0#	A01	O	**Vertical Sync.**
GDVP1DE	GSBA1#	A02	O	**Data Enable.**
GDVP1DET	GD31	E01	I	**Display Detect.**
GDVP1CLK	GSBA6#	D02	O	**Clock.**
GDVP1CLK#	GSBA7#	D03	O	**Clock Complement.**

I/O pads for all signals on this page are powered by VCC15AGP (1.5V I/O).

AGP-Multiplexed Flat Panel Display Port (FPDP) Pin Descriptions

The FPDP Flat Penel Display Port is supported through multiplexing flat panel display interface signal pins with AGP pins.

24-Bit / Dual 12-Bit Flat Panel Display Interface

Signal Name	AGP Name	Pin #	I/O	Signal Description
FPD23 / GTVD11, **FPD22 / GTVD10,** **FPD21 / GTVD09,** **FPD20 / GTVD08,** **FPD19 / GTVD07,** **FPD18 / GTVD06,** **FPD17 / GTVD05,** **FPD16 / GTVD04,** **FPD15 / GTVD03,** **FPD14 / GTVD02,** **FPD13 / GTVD01,** **FPD12 / GTVD00,** **FPD11 / NC**, **FPD10 / NC**, **FPD09 / NC**, **FPD08 / NC**, **FPD07 / NC**, **FPD06 / NC**, **FPD05 / NC**, **FPD04 / NC**, **FPD03 / NC**, **FPD02 / NC**, **FPD01 / NC**, **FPD00 / NC**	GD11 GD13 GD14 GD15 GC#BE2 GD16 GD17 GD18 GD23 GD20 GD22 GADSTB1F GD1 GD0 GD3 GD4 GD5 GD6 GD7 GADSTB0F GC#BE0 GADSTB0S GD10 GD12	L3 N5 K2 R6 J1 J2 H3 H1 G3 G1 K5 G4 P4 P3 R4 R1 N2 P1 R2 N1 M2 N3 N4 L1	O	**Flat Panel Data.** For 24-bit or dual 12-bit flat panel display modes. Two FPD interface modes, 24-bit and dual 12-bit, are supported. Strapping pin DVP0D4 is used to select the interface mode to the LVDS transmitter chip: Strap High (3C5.12[4]=1): 24-bit Strap Low (3C5.12[4]=0): Dual 12-bit In "24-bit" mode, only one set of control pins is required. However, in dual 12-bit mode, the cCN700 provides two sets of control signals that are required for certain LVDS transmitter chips. In 24-bit mode, two operating modes are supported: 3C5.12[4]=1 & 3x5.88[2]=0 & 3x5.88[4]=0 Double data rate: each rising & falling clock edge transmits a complete 24-bit pixel 3C5.12[4]=1 & 3x5.88[2]=0 & 3x5.88[4]=1 Single data rate: each clock rising edge transmits a complete 24-bit pixel In dual 12-bit mode, 3C5.12[4]=0 & 3x5.88[2] = 1 Double data rate: each rising and falling clock edge transmits half (12 bits) of two 24-bit pixels
FPHS / GTVHS	GFRAME	L4	O	**Flat Panel Horizontal Sync.** 24-bit mode or port 0 in dual 12-bit mode.
FPVS / GTVVS	GDEVSEL	J3	O	**Flat Panel Vertical Sync.** 24-bit mode or port 0 in dual 12-bit mode.
FPDE / GTVDE	GD19	K4	O	**Flat Panel Data Enable.** 24-bit mode or port 0 in dual 12-bit mode
FPDET / GTVDET	GADSTB1S	F1	I	**Flat Panel Detect.** 24-bit mode or port 0 in dual 12-bit mode
FPCLK / GTVCLK	GD21	G2	O	**Flat Panel Clock.** 24-bit mode or port 0 in dual 12-bit mode
FPCLK# / NC	GWBF	B3	O	**Flat Panel Clock Complement.** 24-bit mode or port 0 in dual 12-bit mode. For double-data-rate data transfers.
FP1HS / NC	GD9	M1	O	**Flat Panel Horizontal Sync.** For port 1 in dual 12-bit mode.
FP1VS / NC	GPAR	P6	O	**Flat Panel Vertical Sync.** For port 1 in dual 12-bit mode.
FP1DE / NC	GSERR	M6	O	**Flat Panel Data Enable.** For port 1 in dual 12-bit mode.
FP1DET / NC	GD8	M3	I	**Flat Panel Detect.** For port 1 in dual 12-bit mode.
FP1CLK / NC	GD2	R3	O	**Flat Panel Clock.** For port 1 in dual 12-bit mode.
FP1CLK# / NC	GSTOP	M4	O	**Flat Panel Clock Complement.** For port 1 in dual 12-bit mode. For double-data-rate data transfers.

Flat Panel Power Control (Muxed with AGP)

Signal Name	AGP Name	Pin #	I/O	Signal Description
ENAVDD / NC	ST1	E3	IO	**Enable Panel VDD Power.**
ENAVEE / NC	ST0	E4	IO	**Enable Panel VEE Power.**
ENABLT / NC	ST2	F5	IO	**Enable Panel Back Light.**

Note: I/O pads for all pins on this page are powered by VCC15AGP (i.e., 1.5V I/O).

Clock, Reset, Power Control, GPIO, Interrupt and Test Pin Descriptions

Clocks, Resets, Power Control, General Purpose I/O, Interrupts and Test				
Signal Name	**Pin #**	**I/O**	**Signal Description**	**Power Plane**
HCLK+	Y23	I	**Host Clock.** This pin receives the host CPU clock (100 / 133 / 200 MHz). This clock is used by all CN700 logic that is in the host CPU domain.	**VTT**
HCLK–	W23	I	**Host Clock Complement.** Used for Quad Data Transfer on host CPU bus.	**VTT**
MCLKO+	AF26	O	**Memory (SDRAM) Clock.** Output from internal clock generator to external memory interface clock buffer (if required for fanout)	**VCC18MEM**
MCLKO-	AE26	O	**Memory (SDRAM) Clock Complement.**	**VCC18MEM**
MCLKIA	AD26	I	**Memory (SDRAM) Clock Feedback.** Input from MCLKO.	**VCC18MEM**
DISPCLKI	C8	I	**Dot Clock (Pixel Clock) In.** Used for external EMI reduction circuit if used. Connect to **GND** if external EMI reduction circuit not implemented.	**VCC33GFX**
DISPCLKO	C9	O	**Dot Clock (Pixel Clock) Out.** Used for external EMI reduction circuit if used. NC if external EMI reduction circuit not implemented.	**VCC33GFX**
GCLK	R5	I	**AGP Clock.** Clock for AGP logic.	**VCC15AGP**
XIN	A7	I	**Reference Frequency Input.** External 14.31818 MHz clock source. All internal graphics controller clocks are synthesized on chip using this frequency as a reference.	**VCC33GFX**
RESET#	AC1	I	**Reset.** Input from the South Bridge chip. When asserted, this signal resets the CN700 and sets all register bits to the default value. The rising edge of this signal is used to sample all power-up strap options	**VCC18MEM**
PWROK	AB2	I	**Power OK.** Connect to South Bridge and Power Good circuitry.	**VCC18MEM**
SUSST#	AB3	I	**Suspend Status.** For implementation of the Suspend-to-DRAM feature. Connect to an external pull-up to disable.	**VCC18MEM**
AGPBUSY#	T1	O	**AGP Interface Busy.** Connect to a South Bridge GPIO pin for monitoring the status of the internal AGP bus. See Design Guide for details.	**VCC15AGP**
GPOUT	C11	O	**Reserved for display.**	**VCC33GFX**
GPO0	E11	O	**Reserved for display.**	**VCC33GFX**
INTA#	A9	O	**Interrupt.** PCI interrupt output (handled by the interrupt controller in the South Bridge)	**VCC33GFX**
TESTIN#	AF25	I	**Test In.** This pin is used for testing and must be connected to VTT through a 1K-4.7K ohm resistor for all board designs.	**VCC18MEM**

Compensation and Reference Voltage Pin Descriptions

Compensation				
Signal Name	**Pin #**	**I/O**	**Signal Description**	**Power Plane**
HRCOMP	G25	AI	**Host CPU Compensation.** Connect a 20.5 Ω 1% resistor to ground. Used for Host CPU interface I/O buffer calibration.	**VTT**
VLCOMPP	T4	AI	**V-Link Compensation.** Connect a 402 Ω 1% resistor to ground.	**VCC15VL**
DMCOMP	AE5	AI	**DRAM Compensation.** Memory interface IO buffer calibration.	**VCC18MEM**
AGPCOMPP **AGPCOMPN**	A3, A4	AI	**AGP Compensation.**	**VCC15AGP**

Reference Voltages				
Signal Name	**Pin #**	**I/O**	**Signal Description**	**Power Plane**
GTLVREF	L24	P	**Host CPU Interface AGTL+ Voltage Reference.** 2/3 VTT ±2% typically derived using a resistive voltage divider. See Design Guide.	**VTT**
HDVREF[3:0]	F16, F19, G24, F22	P	**Host CPU Data Voltage Reference.** 2/3 VTT ±2% typically derived using a resistive voltage divider. See Design Guide.	**VTT**
HAVREF[1:0]	V24, R24	P	**Host CPU Address Voltage Reference.** 2/3 VTT ±2% typically derived using a resistive voltage divider. See Design Guide.	**VTT**
HCOMPVREF	G26	P	**Host CPU Compensation Voltage Reference.** 1/3 VTT ±2% typically derived using a resistive voltage divider. See Design Guide.	**VTT**
MEMVREF [4:1]	AD8, AD11, AD17, AD23	P	**Memory Voltage Reference.** ½ VCC18MEM ±2% typically derived using a resistive voltage divider. See Design Guide.	**VCC18MEM**
VLVREF	V4	P	**V-Link Voltage Reference.** 0.625V ±2% derived using a resistive voltage divider. See Design Guide.	**VCC15VL**
AGPVREF[2:1]	G6, N6	P	**AGP Voltage Reference.** ½ VCC15AGP (0.75V) for AGP 2.0 (4x transfer mode) and 0.23 VCC15AGP (0.35V) for AGP 3.5 (8x transfer mode). See the Design Guide for additional information and circuit implementation details.	**VCC15AGP**

Power Pin Descriptions

Analog Power / Ground			
Signal Name	**Pin #**	**I/O**	**Signal Description**
VCCA33HCK	AA25	P	**Power for Host CPU Clock PLL** (3.3V ±5%).
GNDAHCK	AA26	P	**Ground for Host CPU Clock PLL.** Connect to main ground plane through a ferrite bead.
VCCA33MCK	AD25	P	**Power for Memory Clock PLL** (3.3V ±5%)
GNDAMCK	AD24	P	**Ground for Memory Clock PLL.** Connect to main ground plane through a ferrite bead.
VCCA33PLL1	D8	P	**Power for Graphics Controller PLL1** (3.3V ±5%).
GNDAPLL1	B7	P	**Ground for Graphics Controller PLL1.** Connect to main ground plane through a ferrite bead.
VCCA33PLL2	C7	P	**Power for Graphics Controller PLL2** (3.3V ±5%).
GNDAPLL2	C6	P	**Ground for Graphics Controller PLL2.** Connect to main ground plane through a ferrite bead.
VCCA33DAC[2:1]	D7, E7	P	**Power for DAC.** (3.3V ±5%)
GNDADAC[2:1]	D6, E6	P	**Ground for DAC.** Connect to main ground plane through a ferrite bead.

Digital Power / Ground			
Signal Name	**Pin #**	**I/O**	**Signal Description**
VTT	(see pin lists)	P	**Power** for **CPU I/O Interface Logic.** Voltage is CPU dependent. See Design Guide for details.
VCC18MEM	(see pin lists)	P	**DDR2: Power** for **Memory I/O Interface Logic.** 1.8V ±5%. **DDR: Power** for **Memory I/O Interface Logic.** 2.5V ±5%.
VCC15VL	U10-11, V10	P	**Power** for **V-Link I/O Interface Logic.** 1.5V ±5%
VCC15AGP	(see pin lists)	P	**Power** for **AGP Bus I/O Interface Logic.** 1.5V ±5%
VCC33GFX	(see pin lists)	P	**Power for Graphics Display I/O Logic.** 3.3V ±5%
VCC15	(see pin lists)	P	**Power** for **Internal Logic.** 1.5V ±5%
VSUS15	AB1, AC25	P	**Suspend Power.** 1.5V ±5%
GND	(see pin lists)	P	**Digital Ground.** Connect to main ground plane.

Strap Pin Descriptions

Strap Pins (External pullup / pulldown straps are required to select "H" / "L")				
Signal	**Actual Strap Pin**	**Function**	**Description**	**Status Bit**
DVP0D[10,9,7]		-reserved-	Always pulled down	
DVP0D8	**AGP:** TYPEDET#	VIA AGP Riser	L: VIA AGP Riser not installed H: VIA AGP Riser installed	3C5.13[3]
DVP0D6	DVP0D6	Dedicated DVI Port Selection	L: Disable H: Enable	3C5.12[6]
DVP0D5	DVP0D5	Dedicated DVI Port Configuration	L: DVI Transmitter H: TV Encoder	3C5.12[5]
DVP0D4	DVP0D4	AGP Port Muxing	L: Two 12-bit DVI interface H: One 24-bit Panel interface	3C5.12[4]
DVP0D[3:0]	DVP0D[3:0]	OEM Panel Type	Reserved for customer definition	3C5.12[3:0]
VD7	**VT8237R Plus, VT8251 CD/CE:** PDCS3#	Reference Voltage	L: 0.75 V H: 0.90 V Reference voltage for VKCOMP at VLINK 4X mode	–
VD6	**VT8237R Plus, VT8251 CD/CE:** PDA2	V4 Capability	L: Disable H V4 Capability	–
VD5	**VT8237R Plus, VT8251 CD/CE:** PDA1	V4-lite Capability	L: Disable H V4-lite Capability	–
VD3	**VT8237R Plus, VT8251 CD/CE:** GPIOD	AGTL+ Pullups	L: Enable internal AGTL+ Pullups H: Disable internal AGTL+ Pullups	–
VD2	**VT8237R Plus, VT8251 CD/CE:** GPIOB	IOQ Depth	L: 8-Level deep H: 1-Level deep	–
VD1	**VT8237R Plus, VT8251 CD/CE:** GPIOA	V-Link Compensation	L: Auto Compensation H: Manual Compensation	–
VD0	**VT8237R Plus, VT8251 CD/CE:** GPIOC	FSB Frequency	Must pull high for Auto Mode	–

Note: VD[7:0] signals are sampled during system initialization. The actual strapping pins are located on the South Bridge chip.

REGISTERS OVERVIEW

In the register descriptions, column "Default" indicates the default value of register bit(s). While column "Attribute" indicates access type of register bit(s).

Abbreviation

Attribute definitions are

RW: Read / Write.
RO: Read Only.
RZ: Read as Zero.
R1: Read as 1.
W1: Write Once then Read Only after that.
W1C: Write of "1" clears bit to zero.
ROS: Sticky-Read Only. Registers will not be set or altered by hot reset.
RWS: Sticky-Read/Write. Registers will not be set or altered by hot reset.
RW1CS: Sticky-Write-1-to-Clear. Registers will not be set or altered by hot reset.
IW: Ignore Write.
MW: Must Write back what is read.
XW: Backdoor Write.
"—": Reserved (essentially the same as RO).

Bit default value indicated as "dip" means the default value is set by dip switch or strapping.

Note: The graphics registers are described in a separate document.

There are two PCI devices, device 0 and device 1, and up to 7 PCI functions are implemented in this chip. To specifically identify a PCI function, the following abbreviations will be applied in subsequent sections.

D0F0: Device 0, Function0 – Host and AGP Control

D0F1: Device 0, Function1 – Error Reporting

D0F2: Device 0, Function2 – Host Bus Control

D0F3: Device 0, Function3 – DRAM Control

D0F4: Device 0, Function4 – Power Management Control

D0F7: Device 0, Function7 – V-Link Control

D1F0: Device 1, Function0 – PCI-to-PCI Bridge

REGISTER DESCRIPTIONS

I/O Ports

IO Port Address: 022h

PCI Arbiter Control **Default Value: 00**

Bit	Attribute	Default	Description
1	RW	0	**AGP / PCI2 Arbiter Control** 0: Enable AGP / PCI2 Bus Arbiter 1: Disable AGP / PCI2 Bus Arbiter
0	RW	0	**PCI Arbiter Control** 0: Enable PCI Bus Arbiter (arbiter will respond to REQ# assertion) 1: Disable PCI Bus Arbiter (arbiter will not respond to PCI-1 REQ# and PREQ# assertion)

PCI Configuration Space I/O

The chip's PCI space registers are addressed via configuration mechanism #1.

Mechanism #1

The I/O ports respond only to double-word accesses. Byte or word accesses will be passed on unchanged.

I/O Port Address: 0CFB-0CF8h

PCI Configuration Address **Default Value: —**

Bit	Attribute	Default	Description
31	RW	0	**Configuration Space Enable** 0: Disabled 1: Convert configuration data port writes to configuration cycles on the PCI bus
30:24	RO	0	**Reserved** (always reads 0)
23:16	RW	0	**PCI Bus Number** Used to choose a specific PCI bus in the system
15:11	RW	0	**Device Number** Used to choose a specific device in the system
10:8	RW	0	**Function Number** Used to choose a specific function if the selected device supports multiple functions
7:2	RW	0	**Register Number (also called the "Offset")** Used to select a specific DWORD in the configuration space
1:0	RW	0	**Fixed** (always reads 0)

I/O Port Address: 0CFF-0CFCh

PCI Configuration Data **Default Value: —**

Bit	Attribute	Default	Description
31:0	RW	0	**PCI Configuration Data**

Note. Refer to PCI Bus Specification Version 2.3 for further details on operation of the above configuration registers.

Device 0 Function 0 (D0F0): AGP Control

Header Registers (0-3Fh)

Offset Address: 1-0h (D0F0)

Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**VIA Technologies ID Code**

Offset Address: 3-2h (D0F0)

Device ID **Default Value: 0314h**

Bit	Attribute	Default	Description
15:0	RO	0314h	**Device ID Code**

Offset Address: 5-4h (D0F0)

PCI Command **Default Value: 0006h**

Bit	Attribute	Default	Description
15:10	—	0	**Reserved**
9	RO	0	**Fast Back-to-Back Cycle Enable** Hardwired to 0. (Disable)
8	RO	0	**SERR# Enable** Hardwired to 0 (Disable)
7	RO	0	**Address / Data Stepping** Hardwired to 0 (Not supported).
6	RW	0	**Parity Checking** 0: Ignore parity errors 1: Perform parity check and take normal action on detected parity errors
5	RO	0	**VGA Palette Snooping** Hardwired to 0 (Not implemented)
4	RO	0	**Memory Write and Invalidate** Hardwired to 0 (Not supported)
3	RO	0	**Respond To Special Cycle** Hardwired to 0 (Does not monitor special cycles)
2	RO	1	**PCI Master Function** Hardwired to 1 (May behave as a bus master)
1	RO	1	**Memory Space Access** Hardwired to 1 (Responds to memory space access)
0	RO	0	**I/O Space Access** Hardwired to 0 (Does not respond to I/O space)

Offset Address: 7-6h (D0F0)
PCI Status **Default Value: 0210h**

Bit	Attribute	Default	Description
15	RW1C	0	**Detect Parity Error** 0: No parity error detected 1: Error detected in either address or data phase
14	RO	0	**Signaled System Error (SERR#)** Hardwired to 0
13	RW1C	0	**Set when terminated with Master-Abort, except special cycle** 0: No abort received 1: Transaction aborted by the master
12	RW1C	0	**Set when received a Target-Abort** 0: No abort received 1: Transaction aborted by the target
11	RO	0	**Set when signaled a Target-Abort** NB never signals Target Abort
10-9	RO	01	**DEVSEL# Timing** 00: Fast 01: Medium (default) 10: Slow 11: Reserved
8	RW1C	0	**Set when set or observed SERR# and Parity Error (Rx04[6])** 0: Disable 1: Enable
7	RO	0	**Capable of Accepting fast back-to-back as a target** Hardwired to 0 (Not implemented)
6	RO	0	**User Definable Features** Hardwired to 0
5	RO	0	**66 MHz Capable** Hardwired to 0 (Not implemented)
4	RO	1	**Support New Capability List**
3:0	—	0	**Reserved**

Offset Address: 8h (D0F0)
Revision ID **Default Value: 0nh**

Bit	Attribute	Default	Description
7:0	RO	0nh	**North Bridge Chip Revision Code**

Offset Address: 0B-9h (D0F0)
Class Code **Default Value: 060000h**

Bit	Attribute	Default	Description
23:0	RO	060000h	**Class Code**

Offset Address: 0Ch (D0F0)
Cache Line Size **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Cache Line Size**

Offset Address: 0Dh (D0F0)
PCI Master Latency Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RW	0	**PCI Bus Time Slice for CPU as a Master (in unit of PCI clocks)**
2:0	RO	0	**Reserved** MLT[2:1] is programmable; however, it's read as 0

Offset Address: 0Eh (D0F0)
Header Type **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	—	**Multi-Function Device** 0: if MFUNC (Rx4F[0], the multiple function control bit) is set to 0 1: if MFUNC is set to 1
6:0	RO	0	**Reserved**

Offset Address: 0Fh (D0F0)
Built In Self Test (BIST) **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**BIST Support** Hardwired to 0 (Not supported)
6:0	—	0	**Reserved**

Offset Address: 13-10h (D0F0)
Graphic Aperture Base Configuration **Default Value: 00000008h**

Bit	Attribute	Default	Description
31:22	RW	0	**Programmable Base Address** These bits behave as if hardwired to 0 if GTSZ (Rx94[11:0]) is set to 0. See the following table for details. (Note: this range is defined as prefetchable)
21:4	—	0	**Reserved**—Hardwired to 0
3	RO	1	**Prefetchable** 0: Non-Prefetchable 1: Prefetchable (hardwired)
2:1	RO	0	**Type** Indicates that the address range is in the 32-bit address space
0	RO	0	**Memory Space** Indicates that the address range is in the memory address space.

Table 5. Graphics Aperture Base Address Table

Aperture Base Rx10[31:22]	31	30	29	28			27	26	25	24	23	22	Aperture Size
Aperture Size Rx94[11:0]	11	10	9	8	7	6	5	4	3	2	1	0	
	RW	RW	RW	RW	0	0	RW	RW	RW	RW	RW	RW	**4M**
	RW	RW	RW	RW	0	0	RW	RW	RW	RW	RW	0	**8M**
	RW	RW	RW	RW	0	0	RW	RW	RW	RW	0	0	**16M**
	RW	RW	RW	RW	0	0	RW	RW	RW	0	0	0	**32M**
	RW	RW	RW	RW	0	0	RW	RW	0	0	0	0	**64M**
	RW	RW	RW	RW	0	0	RW	0	0	0	0	0	**128M**
	RW	RW	RW	RW	0	0	0	0	0	0	0	0	**256M**
	RW	RW	RW	0	0	0	0	0	0	0	0	0	**512M**
	RW	RW	0	0	0	0	0	0	0	0	0	0	**1G**
	RW	0	0	0	0	0	0	0	0	0	0	0	**2G <= Max**
	0	0	0	0	0	0	0	0	0	0	0	0	**4G**

Offset Address: 2D-2Ch (D0F0)
Subsystem Vendor ID **Default Value: 00h**

Bit	Attribute	Default	Description
15:0	RW1	0	**Subsystem Vendor ID**

Offset Address: 2F-2Eh (D0F0)
Subsystem ID **Default Value: 00h**

Bit	Attribute	Default	Description
15:0	RW1	0	**Subsystem ID**

Offset Address: 37-34h (D0F0)
Capability Pointer **Default Value: 00000080h**

Bit	Attribute	Default	Description	Mnemonic
31:0	RO	80h	**AGP Capability List Pointer** An offset address from the start of the configuration space	**CAPPTR[7:0]**

Capability Link List

Rx34	Rx80	Rx50	
80	50	NULL	Rx34 -> Rx80 AGP/AGP8X -> Rx50 PMU ->NULL

AGP Drive Control (40-49h)

Offset Address: 40h (D0F0)
AGP Pad Compensation Control / Status **Default Value: 80h**

Bit	Attribute	Default	Description	Mnemonic
7	RW	1	**AGP4X Strobe's Reference Voltage** 0: Strobe signals do not use AGPVREF as input reference voltage (i.e. STB VREF is STB# and vise versa). 1: Strobe signals use AGPVREF as input reference voltage. (Note: this bit is valid only when internal signal, RX4EN or RX8EN, is set to 1; otherwise always use AGPVREF as Strobe signals' reference voltage) **RSTBVREF** **Input Reference Voltage** 1: 0.5VPP = 0.5 * 1.5v 0: NADSTB0, NADSTB1	**RSTBVREF**
6	RW	0	**AGP4X Strobe and GD Pad Driving Strength Control** 0: Driving strength is set to the compensation circuit defaults 1: Driving strength is controlled by Rx41[7:0]	
5:3	RO	—	**AGP Compensation Circuit N Control Output**	
2:0	RO	—	**AGP Compensation Circuit P Control Output**	

Offset Address: 41h (D0F0)
AGP Driving Strength Control **Default Value: 63h**

Bit	Attribute	Default	Description
7:4	RW	6h	**AGP Output Buffer Driving Strength N Control**
3:0	RW	3h	**AGP Output Buffer Driving Strength P Control**

Offset Address: 42h (D0F0)
AGP Pad Driving and Delay Control **Default Value: 08h**

Bit	Attribute	Default	Description	Mnemonic
7	RW	0	**GD / GADSTBx / GC#BE and GSBSTBx / GSBA# Pad Control** **GSBSTBx, GSBA#** **GD, GC#BE, GADSTBx** **0** No Cap No Cap **1** Cap Cap	
6:5	—	0	**Reserved**	
4	RW	0	**GD[31:16] Output Staggered Delay (1 ns)** 0: No delay 1: GD[31:16] is delayed 1 ns	**RGDLY**
3	RW	1	**GD, GADSTBx Slew Rate Control** 0: Disable 1: Enable	
2	—	0	**Reserved**	
1:0	RW	00	**GADSTBx Output Delay** 00: No delay 01: Delayed by 150 ps 10: Delay by 300 ps 11: Delay by 450 ps Note: GADSTB1 and GADSTB1# will be delayed 1 ns more if RGDLY (bit-4) is set to 1.	

Offset Address: 43h (D0F0)
AGP Strobe Drive Strength Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**AGP Strobe Output Buffer Driving Strength N Control**
3:0	RW	0	**AGP Strobe Output Buffer Driving Strength P Control**

Offset Address: 44h (D0F0)
AGP GSBA Pads Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	—	0	**Reserved**
5:0	RW	0	**GSBA Pads Control**

Offset Address: 45h (D0F0)
AGP Data Delay **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	—	0	**Reserved**
5:3	RW	000	**RDS[2] control GD data delay for receiving** 0: 400ps 1: 0ps **RDS[1:0] control GD strobe delay for receiving** 00: 0ps 01: 100ps 10: 200ps 11: 300ps
2:0	RW	000	**RSS[2] Control GSBA data delay for receiving** 0:400ps 1: 0ps **RSS[1:0] Control GSBA strobe delay for receiving** 00:0ps 01:100ps 10:200ps 11:300ps

Miscellaneous Control (4A-4Fh)

Offset Address: 4Ah (D0F0)
AGP Hardware Support I – VPX Mode **Default Value: 1Fh**

Bit	Attribute	Default	Description
7:0	RW	1Fh	**AGP Request Queue Size** The value in this register is valid and effective if RAGPHW (Rx4D[1]) is set to 1.

Offset Address: 4Bh (D0F0)
AGP Hardware Support II – VPX Mode **Default Value: C4h**

This register is used to re-configure the AGP controller. To change the operating mode of the AGP controller, Rx4D[1] must be set to 1.

Bit	Attribute	Default	Description
7	RW	1	**AGP SBA Mode Enable** 0: Disable 1: Enable
6	RW	1	**AGP Enable** 0: Disable 1: Enable
5	—	0	**Reserved**
4	RW	0	**Fast Write Enable** 0: Disable 1: Enable
3	RW	0	**AGP8X Mode Enable** 0: Disable 1: Enable
2	RW	1	**AGP4X Mode Enable** 0: Disable 1: Enable
1	RW	0	**AGP2X Mode Enable** 0: Disable 1: Enable
0	RW	0	**AGP1X Mode Enable** 0: Disable 1: Enable

Offset Address: 4Dh (D0F0)
AGP Capability Header Control **Default Value: 04h**

Bit	Attribute	Default	Description	Mnemonic
7:6	—	0	**Reserved**	
5	RW	0	**GART Access Control** 0: AGP Aperture is enabled through RGTEN (RxBF[7]) 1: AGP Aperture is enabled through either D0F0 Rx90[8] or D1F0 Rx90[8] (decided by RAGPCAP1 (D1F0 RxBF[0])	**RBKGTEN**
4	—	0	**Rx90 RW Function** 0: Disable 1: Enable	
3	RW	0	**AGP Major / Minor Number Control** 0: Major / Minor = 35 1: Major / Minor = 20	**RBKMJMN**
2	RW	1	**Select Rx80 as the AGP20 or AGP30 Header** 0: Rx80 is used as the AGP20 capability header even if the chip is powered up in AGP30 mode 1: Rx80 is used as the AGP30 capability header when the chip is powered up in AGP30 mode	
1	RW	0	**Enable AGP Hardware Registers in Rx4A ~ Rx4B** 0: AGP hardware is configured by register values defined in AGP header (either 3.0 or 2.0) 1: AGP hardware is configured by register values defined in Rx4A ~ Rx4B (used for VPX mode)	**RAGPHW**
0	RZ-XW	0	**Enable AGP Header Status Register Write** 0: Disable (Status registers in the AGP header cannot be modified) 1: Enable (Status registers in the AGP header can be modified)	**RSTATW**

Offset Address: 4Fh (D0F0)
Multiple Function Control **Default Value: 00h**

Bit	Attribute	Default	Description	Mnemonic
7:1	—	0	**Reserved**	
0	RW	0	**Multi-Function Support** 0: Disable; functions 1, 2, 3, 4, 7 cannot be accessed, and the value returned will be 0FFFFFFFFh when accessed 1: Enable; the status will be reflected on Rx0E[7]	**MFUNC**

AGP Extended Power Management Control (50-57h)

Offset Address: 50h (D0F0)
Capability ID **Default Value: 01h**

Bit	Attribute	Default	Description
7:0	RO	01h	**Capability ID**

Offset Address: 51h (D0F0)
Next Pointer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Next Pointer**

Offset Address: 52h (D0F0)
Power Management Capabilities **Default Value: 02h**

Bit	Attribute	Default	Description
7:0	RO	02h	**Power Management Capabilities**

Offset Address: 53h (D0F0)
Power Management Capabilities **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Power Management Capabilities**

Offset Address: 54h (D0F0)

Power Management Control / Status **Default Value: 00h**

Bit	Attribute	Default	Description
7:2	—	0	**Reserved**
1:0	RW	—	**Power State** 00: D0 11: D3 Hot

Offset Address: 55h (D0F0)

Power Management Status **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Power Management Status**

Offset Address: 56h (D0F0)

PCI to PCI bridge Support Extensions **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**PCI to PCI Bridge Support Extensions**

Offset Address: 57h (D0F0)

Power Management Data **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Power Management Data**

AGP 3.0 Configuration (80-AFh)

For registers (e.g. AGP status register) with attribute "XW", it is allowed to write-over the default setting by setting the register RSTATW (status write) at Rx4D[0] to 1

Offset Address: CAPPTR (D0F0_83-80h)

AGP Capability **Default Value: 003n5002h**

Bit	Attribute	Default	Description
31:24	RZ	0	**Always Return 0, write no effect**
23:20	R-IW	0011	**Major Revision**
19:16	R-IW	n	**Minor Revision** The value is determined by RBKMJMN (Rx4D[3]). 0000b: if Rx4D[3] = 1 0101b: if Rx4D[3] = 0
15:8	R-IW	50h	**Pointer to Next Item**
7:0	R-IW	02h	**Capability ID**

Offset Address: CAPPTR + 04h (D0F0_87-84h)

AGP Status **Default Value: 07000A0Bh**

Bit	Attribute	Default	Description	Mnemonic
31:24	R-IW	07h	**Max # of AGP Command Requests**	
23-18	RZ-IW	0	**Reserved**	
17	RZ-XW	0	**Isoch Transaction** 0: Isoch transaction is not supported 1: Supports Isoch transaction	**RISOCH**
16	RZ-XW	0	**Reserved**	
15:13	RZ-XW	0	**Reserved**	
12:10	RZ-XW	010	**Calibrating Cycle** 000 – 4ms 001 – 16ms 010 – 64ms 011 – 256ms Valid when RAGP30 (bit-3) is 1.	
9	R1-XW	1	**Reserved (SBA support is always ON)**	
8	RZ-XW	0	**Coherent Support –** not implemented	
7	R-XW	0	**64-bit GART Entries –** only 32-bit GART entry is supported	
6	R-XW	0	**Support Host GART Translation** 0: Support host GART translation 1: Does not support host GART translation	
5	R-XW	0	**Over 4GB Support** – not implemented	
4	R-XW	0	**Reserved**	
3	R-XW	0	**AGP 3.0 Detected** 0: AGP 2.0 Mode 1: AGP 3.0 Mode Set by strap pin AGP8XDET#	**RAGP30**
2:0	R-XW	011 111	**AGP Data Rate** **If RAGP30 (bit3) is 1,** the default value is 011: supports 4X and 8X data transfer rate. **If RAGP30 (bit3) is 0,** the default value is 111: supports 1X, 2X and 4X data transfer rate.	

Note: 0700_0A0Bh when RAGP30 is 1; 1F00_0207h when RAGP30 is 0.

Offset Address: CAPPTR + 08h (D0F0 8B-88h)

AGP Command **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RZ-IW	0	**Max # of AGP Command Requests**
23:16	RZ-IW	0	**Reserved**
15:13	RZ-IW	0	**Reserved for master devices**
12:10	RW	0	**Calibrating Cycle**
9	RW	0	**SBA Enable** 0: Disable 1: Enable
8	RW	0	**AGP Enable** 0: Disable 1: Enable
7	RW	0	**64-Bit GART** Not supported
6	RZ-MW	0	**Reserved**
5	RW	0	**Over 4G Support** 0: Disable 1: Enable
4	RW	0	**Fast Write Enable** 0: Disable 1: Enable
3	RZ-MW	0	**Reserved**
2:0	RW	0	**AGP Data Transfer Rate** If RAGP30 (Rx84[3]) = 1 001: 4X data transfer rate 010: 8X data transfer rate If RAGP30 (Rx84[3]) = 0, 001: 1X data transfer rate 010: 2X data transfer rate 100: 4X data transfer rate

Offset Address: CAPPTR + 0Ch (D0F0 8F-8Ch)

AGP Isochronous Status **Default Value: 0000 0000h**

AGP isochronous transaction is not supported, therefore, this register is read zero.

Bit	Attribute	Default	Description	Mnemonic
31:24	—	0	**Reserved**	
23:16	R-IW	0	**Maximum Bandwidth** (in unit of 32 bytes) Used for isochronous transactions	
15:8	R-IW	0	**Maximum Number of Isochronus Transactions in a Single Isochronous Period**	
7:6	RZ-IW	00	**Isochronous Payload Sizes Supported** 00: 32,64,128,256 bytes 01: 64,128,256 bytes 10: 128,256 bytes 11: 256 bytes	**ISOCH_Y**
5:3	R-IW	0	**Isochronous Data Transfer Maximum Latency** (in unit of 1 us)	
2	—	0	**Reserved**	
1:0	R-WIC	00	**Isochronous Error Code** 00: No error 01: Isoch Request Overflow 1x: Reserved	

Offset Address: CAPPTR + 10h (D0F0 93-90h)

AGP Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description	Mnemonic
31:10	—	0	**Reserved**	
9	RW	0	**Disable Calibration Cycle**	
8	RW	0	**Enable AGP Aperture** Set to 1 to enable AGP Aperture. Note: RBKGTEN (Rx4D[5]) must be 1 to enable this function.	**APEREN**
7	RW	0	**GTLB Enable** When set to 0, GART TLB entries are invalidated. All AGP aperture access needs to fetch translation table first.	
6:0	—	0	**Reserved**	

Offset Address: CAPPTR + 14h (D0F0_97-94h)

AGP Aperture Size **Default Value: 0001 0F00h**

Bit	Attribute	Default	Description	Mnemonic
31:28	RW	0000	**Aperture Page Size Select** The page size is determined by the formula: 2^[n+12]. Only 4KB page size, PAGESZ=0h, is supported.	**PAGESZ[15:12]**
27	—	0	**Reserved**	
26:16	R-IW	01h	**Page Size Supported** If NEPG[N] is one, which indicates support of page size of (2^(N+12)). Currently only 4KB page size is supported.	**NEPG[10:0]**
15:12	—	0	**Reserved**	
11:0	RW	F00h	**Aperture Size – Default size is 256MB** Refer to Table 6 for detailed setting (Maximum aperture size: 2GB) GTSZ[n]=0 forces APBASE[22+n] to 0 when 0 <= n <= 5 GTSZ[n]=0 forces APBASE[22+n-2] to 0 when 8 <= n <=11 GTSZ[n]=1 allows APBASE[22+n] to be Read/Write-able. GTSZ[11] to 1 and GTSZ[7:6] are hardwired to 0 When RAGP30 (Rx84[3]) is 0, only supports 4MB ~ 256MB.	**GTSZ[11:0]**

Table 6. Aperture Size

Aperture Size \ Rx94[11:0] (GTSZ)	11	10	9	8	7	6	5	4	3	2	1	0
4MB	1	1	1	1	0	0	1	1	1	1	1	1
8MB	1	1	1	1	0	0	1	1	1	1	1	0
16MB	1	1	1	1	0	0	1	1	1	1	0	0
32MB	1	1	1	1	0	0	1	1	1	0	0	0
64M	1	1	1	1	0	0	1	1	0	0	0	0
128M	1	1	1	1	0	0	1	0	0	0	0	0
256M	1	1	1	1	0	0	0	0	0	0	0	0
512M	1	1	1	0	0	0	0	0	0	0	0	0
1G	1	1	0	0	0	0	0	0	0	0	0	0
2G (Max Aperture Size)	1	0	0	0	0	0	0	0	0	0	0	0
4G	0	0	0	0	0	0	0	0	0	0	0	0

Offset Address: CAPPTR + 18h (D0F0_9B–98h)

AGP GART Table Pointer **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:12	RW	0	**GART Table Base Address [31:12]**
11:0	—	0	**Reserved**

Offset Address: CAPPTR + 1Ch (D0F0_9F- 9Ch)

AGP GART Table Pointer High **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Base Address [63:32]** Since OVER4G is not supported, OS should program this register to zero. This register is ignored.

Offset Address: CAPPTR + 20h (D0F0_A3-A0h)

AGP Isochronous Command **Default Value: 0000 0000h**

This register is not accessible since the ISOCH bit is cleared. Read will be return all zeros, write has no effect.

Bit	Attribute	Default	Description
31:8	—	0	**Reserved**
7:6	RW	0	**Isochronous Payload Size** Default is ISOCH_Y (CAPPTR + 0C[7:6])
5:0	—	0	**Reserved**

AGP Enhanced Control (B0-FFh)

Offset Address: B5h (D0F0)

AGP Back Door Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:2	—	0	**Reserved**
1	RW	0	**RAGP30 Software Setup** RAGP30 (Rx84[3]) is over-written by the value of this register bit**.** (i.e. Read Rx84[3] will retrieve the value of RxB5[1]) Bit-0 must be set to 1 to enable this feature.
0	RW	0	**RAGP30 Software Control** 0: Disable 1: Enable, allows RAGP30 to be software programmable

Offset Address: B9h (D0F0)

AGP Mixed Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	—	0	**Reserved**
6	RW	0	**Hold GD Signal Level After De-assertion of RTXRDY** 0: Disable 1: Enable
5:0	—	0	**Reserved**

Offset Address: BCh (D0F0)

AGP Control **Default Value: 00h**

Bit	Attribute	Default	Description	Mnemonic
7	RW	0	**AGP Disable** 0: No 1: Yes, disable AGP	
6	RW	0	**AGP Read Synchronization** 0: Disable 1: Enable	
5	RW	0	**AGP Read Snoop DRAM Post-Write Buffer** 0: Disable 1: Enable	
4	RW	0	**PP2REQ (CPU/PCI1-to-PCI2 REQ) / AGP Read Priority** 1: PP2REQ has higher priority if MGFIFO is not over 24 QW for low priority read, 0: Disable the function.	
3	RW	0	**GRDY 2T Early Control** 0: Disable 1: Enable	
2	RW	0	**Enable FENCE / FLUSH** 0: LPR will be executed in out-of-order mode 1: Enable FENCE / FLUSH. All normal priority AGP operations are executed sequentially.	**RFENCE**
1	RW	0	**GGNT Parking Policy** 0: Non-parking GGNT; GGNT is de-asserted after GFRAME or PIPE assertion, 1: Parking GGNT; after the assertion of GFRAME or PIPE, GGNT is kept asserted till GREQ de-asserted or timeout.	**RPKGNT**
0	RW	0	**AGP to PMSTR or C2P Turn Around Cycle** 0: 2 or 3T 1: 1T	**RGDARB**

Note:
1. When RPKGNT (RxBC[1]) is set to 1, GGNT will remain asserted until either GREQ de-asserts or data phase ready
2. When RGDARB (RxBC[0]) is set to 0, it allow C2P access when the previous PCI master transaction is a delayed transaction.
3: RFENCE (RxBC[2]) when enabled will force all requests executed in-order, which automatically enables FENCE/FLUSH function.
When disable, FENCE/FLUSH function is not guaranteed.

Offset Address: BDh (D0F0)
AGP Miscellaneous Control **Default Value: 02h**

Bit	Attribute	Default	Description
7	RW	0	**AGP Read Data Phase to GGNT Timing** 0: Normal 1: 1T earlier
6	RW	0	**PIPE to AGP Read Data Phase Timing** 0: Normal 1: 1T earlier
5	RW	0	**Disable Input on AGP GD and GCBE Pads** 0: Input disable 1: Input enable
4	RW	0	**AGP Performance Enhancement** 0: Disable 1: Enable
3:0	RW	02h	**AGP Data Phase Latency Timer** (in unit of 4 GCLKs)

Offset Address: BEh (D0F0)
AGP Miscellaneous Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Select NMI / AGPBUSY# Function** 0: NMI 1: AGPBUSY#
6:1	—	0	**Reserved**
0	RW	0	**CPU GART Read and AGP GART Write Coherency Enable** 0: Disable 1: Enable

Offset Address: BFh (D0F0)
AGP 3.0 Control **Default Value: 00h**

Bit	Attribute	Default	Description	Mnemonic
7	RW	0	**Enable CPU/PMSTR GART Access** 0: Disable 1: Enable This control bit is used differently from APEREN of Rx90. Also, Rx4D[5] must be 0 for this control bit to be effective.	**RGTEN**
6	RW	0	**AGP Calibration Enable** 0: Disable 1: Enable	
5	RW	0	**Mix Coherent / Non-coherent Access Enable** 0: Disable 1: Enable	
4	RW	0	**DBI/PIPE Pin Function** 0: DBIH 1: PIPE	
3:0	—	0	**Reserved**	

Offset Address: C0h (D0F0)
AGPC CKG Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00	**CKG Rising-Time Control (R Port)** 00: Default timing 01: Delay by 100 ps 10: Delay by 200 ps 11: Delay by 300 ps
5:4	RW	00	**CKG Falling-Time Control (R Port)** 00: Default timing 01: Delay by 100 ps 10: Delay by 200 ps 11: Delay by 300 ps
3:2	RW	00	**CKG Rising-Time Control (S Port)** 00: Default timing 01: Delay by 100 ps 10: Delay by 200 ps 11: Delay by 300 ps
1:0	RW	00	**CKG Falling-Time Control (S Port)** 00: Default timing 01: Delay by 100 ps 10: Delay by 200 ps 11: Delay by 300 ps

Offset Address: C1h (D0F0)

AGPC CKG Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	—	0	**Reserved**
3:2	RW	00	**CKG Rising-Time Control (D Port)** 00: Default timing 01: Delay by 100 ps 10: Delay by 200 ps 11: Delay by 300 ps
1:0	RW	00	**CKG Falling-Time Control (D Port)** 00: Default timing 01: Delay by 100 ps 10: Delay by 200 ps 11: Delay by 300 ps

Offset Address: C2h (D0F0)

AGP Miscellaneous Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	—	0	**Reserved**
6	RW	0	**Sync AGP Data** 0: Disable 1: Enable
5:0	—	0	**Reserved**

Device 0 Function 1 (D0F1): Error Reporting

Header Registers (0-3Fh)

Offset Address	Attribute	Default	Description
1 – 0h	RO	1106h	Vendor ID
3 – 2h	RO	1314h	Device ID –Error Reporting
5 – 4h	RO	0006h	PCI Command
7 – 6h	RO	0200h	PCI Status
8h	RO	0	Revision ID
0B – 9h	RO	060000h	Class Code
0Dh	RO	0	Latency Timer
0Eh	RO	01h	Header Type
0Fh	RO	0	BIST
13 – 10h	—	—	Reserved
2D – 2Ch	RW1	0	Subsystem Vendor ID
2F – 2Eh	RW1	0	Subsystem ID
33 – 30h	RO	0	Reserved
37 – 34h	RO	0	Capability Pointer
3F – 38h	—	—	Reserved

V-Link Error Report (50-5Fh)

Offset Address: 58h (D0F1)

V-Link Error Command **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Parity Error / SERR# Report Through NMI** 0: Disable 1: Enable
6	RW	0	**Parity Error / SERR# Report Through V-Link to SB** 0: Disable 1: Enable
5:0	—	0	**Reserved**

Host Bus Error Report (60-6Fh)

Offset Address: 68h (D0F1)

Host Parity Command **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Host Address Parity Generation / Checking** 0: Disable 1: Enable
6	—	0	**Reserved**
5	RW	0	**Host Response Parity Generation** 0: Disable 1: Enable
4:0	—	0	**Reserved**

AGP / PCI2 Non Standard Error Reporting (E0-FFh)

Offset Address: E1h (D0F1)

AGP / PCI2 Error Status **Default Value: 00h**

Bit	Attribute	Default	Description
7:2	—	00	**Reserved**
1:0	RO	00	**Isochronous Error Code from Rx8C[1:0]**

Offset Address: E8h (D0F1)

AGP / PCI2 Error Report Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	—	0	**Reserved**
4	RW	0	**Parity Error Report When AGP Data Parity Error Detected** 0: Disable 1: Enable
3:0	—	0	**Reserved**

Device 0 Function 2 (D0F2): Host Bus Control

Header Registers (0-3Fh)

Offset Address	Attribute	Default	Description
1 – 0h	RO	1106h	Vendor ID
3 – 2h	RO	2314h	Device ID –Host Interface
5 – 4h	RO	0006h	PCI Command
7 – 6h	RO	0200h	PCI Status
8h	RO	00	Revision ID
0B – 9h	RO	060000h	Class Code
0C	RO	00	Cache Line Size
0Dh	RO	00	Latency Timer
0Eh	RO	00	Header Type
0Fh	RO	00	BIST
13 – 10h	—	—	Reserved
2D – 2Ch	RW1	00	Subsystem Vendor ID
2F – 2Eh	RW1	00	Subsystem ID
33 – 30h	RO	00	Reserved
37 – 34h	RO	00	Capability Pointer
3F – 38h	—	—	Reserved

Host CPU Control (50-5Fh)

Offset Address: 50h (D0F2)

Request Phase Control **Default Value: 00h**

Bit	Attribute	Default	Description	Mnemonic
7	RO	dip	**IOQ (In-Order Queue) Depth** (Powell) 0: 1 level 1: 8 level Default sets from the inverse of the VD2 signal during system initialization. For strap pin information, check the Strap Pin table for details.	
6	RO	dip	**Dual CPU** 0: Single CPU 1: Dual CPU Default sets from the VD7 signal during system initialization. For strap pin information, check the Strap Pin table for details.	
5	—	0	**Reserved**	
4:0	RW	0	**Dynamic Defer Snoop Stall Count** Value for the Defer Snoop Stall Counter. The timer starts counting at the beginning of the snoop phase of C2P cycle; it increases one for every 2 HCLKs. If the C2P cycle is pending when the timer expires, and there are pending ADS#, a Defer/Retry response will be replied to the host. For medium decoding PCI slave device; the optimal value for DEFTIM is 8.	**DEFTIM[4:0]**

Table 7. Dynamic Defer Snoop Stall Table

Timer Expire	New Pending ADS#	PCI Completion	Action
No	-	No	Snoop stall till PCI complete
No	-	Yes	Normal Data Response
Yes	No	No	Snoop stall till either arrival of new pending ADS# or PCI complete
Yes	No	Yes	Normal Data Response
Yes	Yes	No	Defer/Retry Response
Yes	Yes	Yes	Normal Data Response

Offset Address: 51h (D0F2)
CPU Interface Control **Default Value: 00h**

Bit	Attribute	Default	Description	Mnemonic
7	RW	0	**Fast Ready for CPU Memory Read Cycle** 0: Disable, wait until all 8QWs are received before DRDY# assertion 1: Enable, DRDY# assertion timing is set up through Rx60-67	
6	RW	0	**Read Around Write** 0: Disable 1: Enable	**RAW**
5	RW	0	**Host Controller DRAM Request Queue Control (DRQCTL)** 0: Disable DRQCTL pipeline 1: Enable DRQCTL pipeline	
4	RW	0	**CPU to PCI Read Defer** 0: Disable 1: Enable	
3	RW	0	**2 Defer/ Retry Entries** 0: Disable 1: Enable	
2	RW	0	**2 Defer / Retry Entries Sharing** 0: One entry for each processor 1: Each entry is shared by the two processors	
1	RW	0	**PCI Master Pipelined Access** 0: Disable 1: Enable	
0	—	0	**Reserved**	

Offset Address: 52h (D0F2)
CPU Interface Control **Default Value: 00h**

Bit	Attribute	Default	Description	Mnemonic
7	RW	0	**Enable CPU Read / Write DRAM 0WS for Back-to-Back Pipeline Access** 0: Disable 1: Enable	
6	RW	0	**HREQ# (Host Continuous DRAM Ownership) / HPRI (Host High Priority DRAM Request) Assertion to DRAM Controller** 0: Disable 1: Enable assertion of HREQ# / HPRI to DRAM Controller for efficient memory utilization / faster data access.	
5	RW	0	**AGTL+ Pullup Enable** 0: Disable 1: Enable Default sets from the inverse of the VD3 signal during system initialization. For strap pin information, check the Strap Pin table for details.	
4	—	0	**Reserved**	
3	RW	0	**Write Retire Policy After 2 Writes** 0: Disable 1: Enable	**RFRAW**
2	—	0	**Reserved**	
1	RW	0	**Consecutive Speculative Read** 0: Disable 1: Enable	
0	RW	0	**Speculative Read** 0: Disable 1: Enable	

Offset Address: 53h (D0F2)
Arbitration **Default Value: 00h**

Bit	Attribute	Default	Description	Mnemonic
7:4	RW	0	**Host Timer (in unit of 4 HCLKs)** Host Timer guarantees a time slot of P6TIM * 4 HCLK for pipelined CPU's ADS#.	**P6TIM[3:0]**
3:0	RW	0	**BPRI# Timer (in unit of 4 HCLKs)** BPRI# timer guarantees a time slot of PRITIM*4 HCLK for pending master requests.	**PRITIM[3:0]**

Offset Address: 54h (D0F2)
Miscellaneous Control **Default Value: 00h**

Bit	Attribute	Default	Description	Mnemonic
7:5	RO	00	**CPU FSB Frequency** (Powell) 000: 100MHz 001: 133MHz All others: Reserved Default sets from the VD[0] signals during system initialization. For strap pin information, check the Strap Pin table for details.	
4	RW	0	**Burst 8QW Host Memory Access** 0: Disable 1: Enable	
3	RW	0	**Host-Memory DRDY# Assertion Adjustment** 0: Normal mode, no adjustment 1: Special mode This bit's setting should follow **RDRDYLPH / RDRDYQPH / RDRDYPH_WS** (Rx60 - Rx67) settings. **Check Rx55[1] for details of DRDY# assertion adjustment.**.	**RFASTH**
2	RW	0	**PCI Master 8QW Memory Access** 0: Disable 1: Enable	
1	RW	0	**Memory-to-Host Conversion Circuit** 0: Transparent mode 1: Sync 1T in certain clock phases Transparent mode, the default operating mode, is faster than Sync mode.	
0	RW	0	**PCI2 Operating Mode** (for EOI message processing) 0: AGP mode 1: VPX mode	

Offset Address: 55h (D0F2)
Miscellaneous Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	—	0	**Warm CPU Reset (CPURST#) Trigger** Write 0->1 transition will trigger warm CPURST#
6	RW	1	**Reserved**
5	RW	0	**CLK4XEN Assertion Control** 0: Disable 1: Enable; CLK4XEN is asserted on the entire request cycle.
4	RW	0	**Fast Command 8QW Pre-fetch** 0: Disable 1: Enable
3	—	0	**Reserved**
2	RW	0	**Medium Threshold for Write Policy** (see ROPTW (Rx56[7:4]) for details) 0: Disable medium threshold 1: Add a medium threshold in Write Queue to enable earlier memory write. Refers to Rx5D for write policy.
1	RW	0	**DRDY# Early / Late Assertion** 0: 2T early 1: 2T late This bit is effective when RFASTH (Rx54[3]) is 1.
0	—	0	**Reserved**

Offset Address: 56h (D0F2)
Write Policy **Default Value: 00h**

Bit	Attribute	Default	Description	Mnemonic
7:4	RW	0	**Medium Threshold for Write Policy**	**ROPTW[3:0]**
3:0	—	0	**Reserved**	

Offset Address: 57h (D0F2)
Miscellaneous Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RW	001	**DRAM Operating Frequency** 000: 100MHz 001: 133MHz 010: 166MHz 011: 200MHz 100: 266MHz 101: 333MHz 110/111: Reserved
4:0	—	0	**Reserved**

Offset Address: 59h (D0F2)
CPU Miscellaneous Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	—	0	**Reserved**
0	RW	0	**Lowest-Priority IPI (Inter-Processor Interrupt) Support** 0: Disable 1: Enable

Offset Address: 5Ch (D0F2)
CPU Miscellaneous Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	—	0	**Reserved**
4	RW	0	**APIC Data Bit 11 (D11) Mask** 0: D11 is not masked 1: D11 is masked to 0
3	RW	0	**APIC Redirection Hint Information Obtained From** 0: Address filed 1: Data field
2	RW	0	**APIC Destination Mode Information Obtained From** 0: Address field 1: Data field
1	RW	0	**APIC Cluster Mode Support** 0: Disable 1: Enable
0	RW	0	**Redirect Lowest Priority APIC Requests to CPU0 (i.e. CPU0 is treated as the lowest priority processor)** 0: Disable 1: Enable.

Offset Address: 5Dh (D0F2)
Write Policy **Default Value: 00h**

Bit	Attribute	Default	Description	Mnemonic
7:4	RW	0	**Write Request High Water Mark**	**RWLM[3:0]**
3:0	RW	0	**Write Request Low Water Mark**	**RWBS[3:0]**

Table 8. CPU Write Request Policy

RAW (Rx51[6])	RFRAW (Rx52[3])	RWLM (Rx5D[7:4])	RWBS (Rx5D[3:0])	Write Policy
1	0	x	x	Will not handle write request until FIFO is full
1	1	4	2	Will process write request when write request number equals to RWLM, and stop processing write request when write request number drops to RWBS.

Offset Address: 5Eh (D0F2)
Bandwidth Timer **Default Value: 00h**

Bit	Attribute	Default	Description	Mnemonic
7:4	RW	0	**Host Bandwidth Timer Limit**	**RHBWTM[3:0]**
3:0	RW	0	**DRAM Bandwidth Timer Limit**	**RDBWTM[3:0]**

Offset Address: 5Fh (D0F2)
CPU Miscellaneous Control **Default Value: 00h**

Bit	Attribute	Default	Description	Mnemonic
7	RW	0	**Off Page Definition: Same Bank Different Sub-Bank Considered as Off-Page** 0: Disable 1: Enable (suggested setting) Set to 1 will reduce burst length of posted-write for better performance	
6	RW	0	**Back-to-back Fast Read** (Burst C2P and C2M read) 0: Disable 1: Enable (suggested setting)	
5:4	—	0	**Warm CPU reset(CPURST#) duration control** 00: 512us 01: 1024us 10: 1523us 11: 2048us	
3	RW	0	**Pipeline APIC / Master Transaction** 0: APIC requests will not be pipelined with master requests. 1: APIC requests can be pipelined with normal master requests. This bit must be set to 0.	
2	RW	0	**Host Bandwidth Timer** 0: Disable 1: Enable Host Bandwidth Timer Limit is set up by RHBWTM[3:0] (Rx5E[7:4]).	**RHOSTBW**
1	RW	0	**DRAM Bandwidth Timer** 0: Disable 1: Enable DRAM Bandwidth Timer Limit is set up by RDBWTM[3:0] (Rx5E[3:0]).	**RDRAMBW**
0	RW	0	**CPU Access DRAM Read after Write Enhancement** 0: Disable 1: Enable	

Table 9. Host / DRAM Bandwidth Setting Policy

RHOSTBW (Rx5F[2])	RDRAMBW (Rx5F[1])	Host / DRAM Bandwidth Setting Policy
0	0	Disable the new DRAM/Host Bandwidth Arbiter
0	1	Refers to the DRAM Bandwidth Timer
1	0	Refers to the HOST Bandwidth Timer
1	1	Dynamically toggles between the two Host/Dram bandwidth timers. Both timers, RHBWTM and RDBWTM are used by the arbitration logic.

Host Interface DRDY# Timing Control (60-6Fh)

Offset Address: 60h (D0F2)
Line DRDY# Timing Control 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	0	**Read Line Phase 4 Wait State**
5:4	RW	0	**Read Line Phase 3 Wait State**
3:2	RW	0	**Read Line Phase 2 Wait State**
1:0	RW	0	**Read Line Phase 1 Wait State**

Offset Address: 61h (D0F2)
Line DRDY# Timing Control 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	0	**Read Line Phase 8 Wait State**
5:4	RW	0	**Read Line Phase 7 Wait State**
3:2	RW	0	**Read Line Phase 6 Wait State**
1:0	RW	0	**Read Line Phase 5 Wait State**

Offset Address: 62h (D0F2)
Line DRDY# Timing Control 3 **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	—	0	**Reserved**
3:2	RW	0	**Read Line Phase 10 Wait State**
1:0	RW	0	**Read Line Phase 9 Wait State**

Offset Address: 63h (D0F2)
QW DRDY# Timing Control 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	0	**Read QW Phase 4 Wait State**
5:4	RW	0	**Read QW Phase 3 Wait State**
3:2	RW	0	**Read QW Phase 2 Wait State**
1:0	RW	0	**Read QW Phase 1 Wait State**

Offset Address: 64h (D0F2)
QW DRDY# Timing Control 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	0	**Read QW Phase 8 Wait State**
5:4	RW	0	**Read QW Phase 7 Wait State**
3:2	RW	0	**Read QW Phase 6 Wait State**
1:0	RW	0	**Read QW Phase 5 Wait State**

Offset Address: 65h (D0F2)
QW DRDY# Timing Control 3 **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	—	0	**Reserved**
3:2	RW	0	**Read QW Phase 10 Wait State**
1:0	RW	0	**Read QW Phase 9 Wait State**

Offset Address: 66h (D0F2)
Read Line Burst DRDY# Timing Control 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Phase 8 Wait State**
6	RW	0	**Phase 7 Wait State**
5	RW	0	**Phase 6 Wait State**
4	RW	0	**Phase 6 Wait State**
3	RW	0	**Phase 4 Wait State**
2	RW	0	**Phase 3 Wait State**
1	RW	0	**Phase 2 Wait State**
0	RW	0	**Phase 1 Wait State**

Offset Address: 67h (D0F2)
Read Line Burst DRDY# Timing Control 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7	—	0	**Turnomg on this register will turn off the pad not used and it will also turn off HD[63:32]# pad when operate in V4-lite mode.**
6			**Disable BREQ0# control of Host Interface dynamic clock wakeup.**
5	RW	0	**Phase 10 Wait State**
4	RW	0	**Phase 9 Wait State**
3:0	—	0	**Reserved**

Note: Check BIOS Porting Guide for RDRDY register settings.

Offset Address: 6F-68h (D0F2)
APIC CPU Priority **Default Value: 00h**

Offset Address	Attribute	Default	Description
6Fh	RO	0	**Priority of CPU ID#7**
6Eh	RO	0	**Priority of CPU ID#6**
6Dh	RO	0	**Priority of CPU ID#5**
6Ch	RO	0	**Priority of CPU ID#4**
6Bh	RO	0	**Priority of CPU ID#3**
6Ah	RO	0	**Priority of CPU ID#2**
69h	RO	0	**Priority pf CPU ID#1**
68h	RO	0	**Priority of CPU ID#0**

Host AGTL+ I/O Circuit (70-7Fh)

Offset Address: 70h (D0F2)
Host Address Pad (2x) Pullup Driving **Default Value: 00h**

Bit	Attribute	Default	Description
7	—	0	**Reserved**
6:4	RW	0	**2X Address Strobe Pad Pullup Driving – (HADSTB1#, HADSTB0#)**
3	—	0	**Reserved**
2:0	RW	0	**2X Address Pad Pullup Driving – (HA[31:3]#, HREQ[4:0]#)**

Offset Address: 71h (D0F2)
Host Address Pad (2x) Pulldown Driving **Default Value: 00h**

Bit	Attribute	Default	Description
7	—	0	**Reserved**
6:4	RW	0	**2X Address Strobe Pad Pulldown Driving – (HADSTB1#, HADSTB0#)**
3	—	0	**Reserved**
2:0	RW	0	**2X Address Pad Pulldown Driving – (HA[31:3]#, HREQ[4:0]#)**

Offset Address: 72h (D0F2)
Host Data Pad (4x) Pullup Driving **Default Value: 00h**

Bit	Attribute	Default	Description
7	—	0	**Reserved**
6:4	RW	0	**4X Data Strobe Pad Pulldown Driving – (HDSTB[3:0]N#, HDSTB[3:0]P#)**
3	—	0	**Reserved**
2:0	RW	0	**4X Data Pad Pulldown Driving – (HD[63:0]#, HDBI[3:0]#)**

Offset Address: 73h (D0F2)
Host Data (4x) Pulldown Driving **Default Value: 00h**

Bit	Attribute	Default	Description
7	—	0	**Reserved**
6:4	RW	0	**4X Data Strobe Pad Pulldown Driving – (HDSTB[3:0]N#, HDSTB[3:0]P#)**
3	—	0	**Reserved**
2:0	RW	0	**4X Data Pad Pulldown Driving – (HD[63:0]#, HDBI[3:0]#)**

Offset Address: 74h (D0F2)
Miscellaneous Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	—	0	**Reserved**
5	RW	0	**HD[63:48]#, HD[31:16]#, HDBI[3,1]# Output Stagger Delay 1ns** 0: No delay 1: 1ns delay
4	RW	0	**HA[31:17]# Output Stagger Delay** 0: No delay 1: 1ns delay
3:2	RW	00	**HDSTB[3:0]N#, HDSTB[3:0]P# Extra Output Delay** 00: No delay 01: 150 ps 10: 300 ps 11: 450 ps
1:0	RW	00	**HADSTB1#, HADSTB0# Extra Output Delay** 00: No delay 01: 150 ps 10: 300 ps 11: 450 ps

Offset Address: 75h (D0F2)
AGTL+ I/O Circuit **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**AGTL+ 4X Input: Add Delay to Filter Noise (TR3 Control)** 0: Disable 1: Enable
6	RW	0	**AGTL+ 2X Input: Add Delay to Filter Noise (TR3 Control)** 0: Disable 1: Enable
5	RW	0	**AGTL+ Slew Rate** 0: Disable 1: Enable
4	RW	0	**Relative Input Delay Between Data And Strobe Signals** This bit, together with Rx74[7:6], is used to fine tune the relative input delay between data and strobe signals.
3	RW	0	**Input Always Pullup (PULLUP)** 0: Disable 1: Enable
2	RW	0	**AGTL+ TR Function (always pullup) for STROBE** 0: Disable 1: Enable
1	RW	0	**AGTL+ TR Function (always pullup) for DATA** 0: Disable 1: Enable
0	RW	0	**AGTL+ Dynamic Compensation** 0: Disable 1: Enable

Offset Address: 76h (D0F2)
AGTL+ Compensation Status **Default Value: 00h**

Bit	Attribute	Default	Description	Mnemonic
7	RW	0	**Auto-compensation Driving** 1: Enable Auto mode	
6:4	RO	0	**AGTL+ Compensation Result**	**RPOSDRV[2:0]**
3	RW	0	**AGTL+ POS Function** 1: Power-down AGTL+ input when not in input mode	
2	—	0	**Reserved**	
1	RW	0	**Disable DBI Function** 0: Enable DBI 1: Disable DBI (DBI always high including DBI double-check)	
0	RW	0	**DBI Function** 0: Minimize data change count (through data comparison with previous data) 1: Minimize AGTL+ pulldown count	

Offset Address: 77h (D0F2)
AGTL+ Auto Compensation Offset **Default Value: 00h**

Bit	Attribute	Default	Description	Mnemonic
7:4	RW	0	**2X AGTL+ IO Pad Driving Offset to Compensation Result (Rx76[6:4])**	**RGTLOST2X[3:0]**
3:0	RW	0	**4X AGTL+ IO Pad Driving Offset to Compensation Result (Rx76[6:4])** Note: The actual driving to GTL pad is RPOSDRV+RGTLOST2X or RPOSDRV+RGTLOST4X. RGTLOST2X/RGTLOST4X can be either positive or negative offset; negative offset is represented in 2's complement, so the driving offset value ranges from –8 to +7.	**RGTLOST4X[3:0]**

Offset Address: 78h (D0F2)

Host FSB CKG Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00	**CKG Falling-Time Control for Host Interface (S port)** 00: Default timing 01: Delay by 100 ps 10: Delay by 200 ps 11: Delay by 300 ps
5:4	RW	00	**CKG Rising-Time Control for Host Interface (S port)** 00: Default timing 01: Delay by 100 ps 10: Delay by 200 ps 11: Delay by 300 ps
3:2	RW	00	**CKG Falling-Time Control for Host Interface** 00: Default timing 01: Delay by 100 ps 10: Delay by 200 ps 11: Delay by 300 ps
1:0	RW	00	**CKG Rising-Time Control for Host Interface** 00: Default timing 01: Delay by 100 ps 10: Delay by 200 ps 11: Delay by 300 ps

Offset Address: 79h (D0F2)

Address / Address Clock Output Delay Control **Default Value: AAh**

Bit	Attribute	Default	Description
7:6	RW	10	**Group 0 Address Output Delay** 00: Delay = Td -0.3ns 01: Delay = Td -0.15ns 10: Delay = Td 11: Delay = Td + 0.15ns Delay (Td) = 650ps (min), 750ps (typ), 850ps (max) from CK to CKO0~CKO18
5:4	RW	10	**Group 0 Address Clock Output Delay** 00: Delay = Td -0.3ns 01: Delay = Td -0.15ns 10: Delay = Td 11: Delay = Td + 0.15ns Delay (Td) = 650ps (min), 750ps (typ), 850ps (max) from CK to CKO0~CKO18
3:2	RW	10	**Group 1 Address Output Delay** 00: Delay = Td -0.3ns 01: Delay = Td -0.15ns 10: Delay = Td 11: Delay = Td + 0.15ns Delay (Td) = 650ps (min), 750ps (typ), 850ps (max) from CK to CKO0~CKO18
1:0	RW	10	**Group 1 Address Clock Output Delay** 00: Delay = Td -0.3ns 01: Delay = Td -0.15ns 10: Delay = Td 11: Delay = Td + 0.15ns Delay (Td) = 650ps (min), 750ps (typ), 850ps (max) from CK to CKO0~CKO18

Offset Address: 7Ah (D0F2)

Address Strobe Input Delay Control **Default Value: 24h**

Bit	Attribute	Default	Description
7:6	—	0	**Reserved**
5:3	RW	100	**HASTB0 Address Strobe Input Delay** Default value 100 will let HASTB0 balance with address group0 data. Value greater than 100 will delay HASTB0 about 100ps per scale. Value less than 100 will early HASTB0 about 100ps per scale.
2:0	RW	100	**HASTB1 Address Strobe Input Delay** Default value 100 which should let HASTB1 balance with address group1 data. Value greater than 100 will delay HASTB1 about 100ps per scale. Value less than 100 will early HASTB1 about 100ps per scale.

Offset Address: 7Bh (D0F2)

Address CKG Rising / Falling Time Control **Default Value: 55h**

Bit	Attribute	Default	Description
7:6	RW	01	**Group 0 Address CKG Falling-Time Control** 00: Default timing 01: Delay by 100 ps 10: Delay by 200 ps 11: Delay by 300 ps
5:4	RW	01	**Group 0 Address CKG Rising-Time Control** 00: Default timing 01: Delay by 100 ps 10: Delay by 200 ps 11: Delay by 300 ps
3:2	RW	01	**Group 1 Address CKG Falling-Time Control** 00: Default timing 01: Delay by 100 ps 10: Delay by 200 ps 11: Delay by 300 ps
1:0	RW	01	**Group 1 Address CKG Rising-Time Control** 00: Default timing 01: Delay by 100 ps 10: Delay by 200 ps 11: Delay by 300 ps

Offset Address: 7Ch (D0F2)

Address CKG Clock Rising / Falling Time Control **Default Value: 55h**

Bit	Attribute	Default	Description
7:6	RW	01	**Group 0 Address Clock CKG Falling-Time Control** 00: Default timing 01: Delay by 100 ps 10: Delay by 200 ps 11: Delay by 300 ps
5:4	RW	01	**Group 0 Address Clock CKG Rising-Time Control** 00: Default timing 01: Delay by 100 ps 10: Delay by 200 ps 11: Delay by 300 ps
3:2	RW	01	**Group 1 Address CKG Falling-Time Control** 00: Default timing 01: Delay by 100 ps 10: Delay by 200 ps 11: Delay by 300 ps
1:0	RW	01	**Group 1 Address CKG Rising-Time Control** 00: Default timing 01: Delay by 100 ps 10: Delay by 200 ps 11: Delay by 300 ps

Device 0 Function 3 (D0F3): DRAM Bus Control

Header Registers (0–3Fh)

Offset Address	Attribute	Default	Description
1 – 0h	RO	1106h	Vendor ID
3 – 2h	RO	3208h	Device ID – DRAM Control
5 – 4h	RO	0006h	PCI Command
7 – 6h	RO	0200h	PCI Status
8h	RO	00	Revision ID
0B – 9h	RO	060000h	Class Code
0Dh	RO	00	Latency Timer
0Eh	RO	00	Header Type
0Fh	RO	00	BIST
13-10h	—	—	Reserved
2D – 2Ch	RW1	00	Subsystem Vendor ID
2F – 2Eh	RW1	00	Subsystem ID
33 – 30h	RO	00	Reserved
37 – 34h	RO	00	Capability Pointer
3F – 38h	—	—	Reserved

Note: All Function 3, DRAM Controller, registers are implemented in Powell.

DRAM Rank (Row) Ending Address (40–4Fh)

Offset Address: 47-40h (D0F3)

DRAM Rank Ending Address **Default Value: 0100 0000h**

Offset Address	Attribute	Default	Description
40h	RW	01h	**Virtual Rank 0 Ending Address (HA[31:26]#)**
41h	RW	00h	**Virtual Rank 1 Ending Address (HA[31:26]#)**
42h	RW	00h	**Virtual Rank 2 Ending Address (HA[31:26]#)**
43h	RW	00h	**Virtual Rank 3 Ending Address (HA[31:26]#)**

Offset Address: 4F-48h (D0F3)

DRAM Rank Beginning Address **Default Value: 0000 0000 h**

Offset Address	Attribute	Default	Description
48h	RW	00h	**Virtual Rank 0 Beginning Address (HA[31:26]#)**
49h	RW	00h	**Virtual Rank 1 Beginning Address (HA[31:26]#)**
4Ah	RW	00h	**Virtual Rank 2 Beginning Address (HA[31:26]#)**
4Bh	RW	00h	**Virtual Rank 3 Beginning Address (HA[31:26]#)**

MA Map / Command Rate (50–53h)

Offset Address: 51-50h (D0F3)

DRAM MA Map Type **Default Value: 0022h**

Bit	Attribute	Default	Description
15: 8	—	0	**Reserved**
7:5	RW	001	**Rank 0/1 MA Map Type**
4	RW	0	**Rank 0/1 1T Command Rate** 0: Disable (2T command) 1: 1T command
3:1	RW	001	**Rank 2/3 MA Map Type**
0	RW	0	**Rank 2/3 1T Command Rate** 0: Disable (2T command) 1: 1T command

Table 10. Rank MA Map Type Table

Rank MA Map Type	0	1	2	3	4	5	6	7
Bank Address Bits	2	2	2	2	Rsvd	3	3	3
Row Address Bits	13-12	14-12	15-12	15-13		15-12	15-12	15-13
Column Address Bits	9	10	11	12		10	11	12
DRAM Size (Byte)	128M-64M	512M-128M	2G-256M	4G-1G		2G-256M	4G-512M	8G-2G

Offset Address: 52h (D0F3)

Bank Interleave Address Select **Default Value: 11h**

Bit	Attribute	Default	Description	Mnemonic
7	—	0	**Reserved**	**—**
6:4	RW	001	**BA0 Address Select**	**RBA0SEL_[2:0]**
3	—	0	**Reserved**	**—**
2:0	RW	001	**BA1 Address Select**	**RBA1SEL_[2:0]**

Note: Refer to Bank Interleave Address Table below.

Offset Address: 53h (D0F3)

Bank / Rank Interleave Address Select **Default Value: 10h**

Bit	Attribute	Default	Description	Mnemonic
7	RW	0	**BA2 Support (turn on if any 8BK-device exists)**	
6:4	RW	001	**BA2 Address Select**	**RBA2SEL_[2:0]**
3:2	RW	000	**Rank Interleave Address Bit 1 (RA1) Select**	**RINLV1SEL_[1:0]**
1:0	RW	00	**Rank Interleave Address Bit 0 (RA0) Select**	**RINLV0SEL_[1:0]**

Table 11. DRAM Bank Address Table

RBAxSEL_[2:0] where x=0, 1, 2	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**
BA2 RBA2SEL_[2:0] (Rx53[6:4])	A14	A15	A18	A19	rsvd	rsvd	rsvd	rsvd
BA1 RBA1SEL_[2:0] (Rx52[2:0])	A12	A14	A16	A18	A20	rsvd	rsvd	rsvd
BA0 RBA0SEL_[2:0] (Rx52[6:4])	rsvd	A13	A15	A17	A19	rsvd	rsvd	rsvd

Table 12. Rank Interleave Address Table

RINLVxSEL_[1:0] where x=0, 1	**0**	**1**	**2**	**3**
Rank Interleave Address Bit 1 RINLV1SEL_[1:0] (Rx53[3:2])	A14	A16	A18	A20
Rank Interleave Address Bit 0 RINLV0SEL_[1:0] (Rx53[1:0])	A15	A17	A19	A21

Notes. 1. Rank Interleave Address Bit 2 is fixed at A6.
2. BA2, BA1, BA0, INLV1, INLV0 should select 5 different address bits for Rx53[7] =1
3. BA1, BA0, INLV1, INLV0 should select 4 different address bits for Rx53[7]=0

Physical-to-Virtual Rank Mapping (54–57h)

Offset Address: 54h (D0F3)
Physical-to-Virtual Rank Mapping 1 **Default Value: 81h**

Bit	Attribute	Default	Description
7	RW	1	**Enable Physical Rank 0** 0: Disable 1: Enable the rank
6:4	RW	000	**Virtual Rank Number of Physical Rank 0**
3	RW	0	**Enable Physical Rank 1** 0: Disable 1: Enable the rank
2:0	RW	001	**Virtual Rank Number of Physical Rank 1**

Offset Address: 55h (D0F3)
Physical-to-Virtual Rank Mapping 2 **Default Value: 23h**

Bit	Attribute	Default	Description
7	RW	0	**Enable Physical Rank 2** 0: Disable 1: Enable the rank
6:4	RW	010	**Virtual Rank Number of Physical Rank 2**
3	RW	0	**Enable Physical Rank 3** 0: Disable 1: Enable the rank
2:0	RW	011	**Virtual Rank Number of Physical Rank 3**

Offset Address: 56h (D0F3)
Physical-to-Virtual Rank Mapping 3 **Default Value: C5h**

Bit	Attribute	Default	Description
7	RW	1	**Enable Physical Rank 4** 0: Disable 1: Enable the rank
6:4	RW	100	**Virtual Rank Number of Physical Rank 4**
3	RW	0	**Enable Physical Rank 5** 0: Disable 1: Enable the rank
2:0	RW	101	**Virtual Rank Number of Physical Rank 5**

Offset Address: 57h (D0F3)
Physical-to-Virtual Rank Mapping 4 **Default Value: 67h**

Bit	Attribute	Default	Description
7	RW	0	**Enable Physical Rank 6** 0: Disable 1: Enable the rank
6:4	RW	110	**Virtual Rank Number of Physical Rank 6**
3	RW	0	**Enable Physical Rank 7** 0: Disable 1: Enable the rank
2:0	RW	111	**Virtual Rank Number of Physical Rank 7**

Virtual Rank Interleave Address Select / Enable (58–5Fh)

Offset Address: 58h (D0F3)

Virtual Rank Interleave Address Select / Enable – Rank 0 **Default Value: 00h**

Bit	Attribute	Default	Description	Mnemonic
7	—	0	**Reserved**	
6:4	RW	000	**Rank #0 Interleave Address Select (RINLV0AS[2:0])** This 3-bits field determines the Rank Interleave Address of Rank #0. If RINLV0ASn is 1 (where n = 0, 1, 2), the corresponding Rank Interleave Address bit of Rank 0 is 1, and vice versa.	**RINLV0AS[2:0]**
3	—	0	**Reserved**	
2:0	RW	000	**Rank #0 Interleave Address Enable (RINLV0AEN[2:0])** 0: Mask 1: Enable This 3-bits field determines if the Rank Interleave Address of Rank #0 to be masked (used) or not. If RINLV0AENn is 0 (where n = 0, 1, 2), the corresponding Rank Interleave Address bit will be masked (ignored), and vice versa.	**RINLV0AEN[2:0]**

Offset Address: 59h (D0F3)

Virtual Rank Interleave Address Select / Enable – Rank 1 **Default Value: 00h**

Bit	Attribute	Default	Description	Mnemonic
7	—	0	**Reserved**	
6:4	RW	000	**Rank #1 Interleave Address Select** See the description on Rank 0 (Rx58).	**RINLV1AS[2:0]**
3	—	0	**Reserved**	
2:0	RW	000	**Rank #1 Interleave Address Enable** See the description on Rank 0 (Rx58).	**RINLV1AEN[2:0]**

Offset Address: 5Ah (D0F3)

Virtual Rank Interleave Address Select / Enable – Rank 2 **Default Value: 00h**

Bit	Attribute	Default	Description	Mnemonic
7	—	0	**Reserved**	
6:4	RW	000	**Rank #2 Interleave Address Select** See the description on Rank 0 (Rx58).	**RINLV2AS[2:0]**
3	—	0	**Reserved**	
2:0	RW	000	**Rank #2 Interleave Address Enable** See the description on Rank 0 (Rx58).	**RINLV2AEN[2:0]**

Offset Address: 5Bh (D0F3)

Virtual Rank Interleave Address Select / Enable – Rank 3 **Default Value: 00h**

Bit	Attribute	Default	Description	Mnemonic
7	—	0	**Reserved**	
6:4	RW	000	**Rank #3 Interleave Address Select** See the description on Rank 0 (Rx58).	**RINLV3AS[2:0]**
3	—	0	**Reserved**	
2:0	RW	000	**Rank #3 Interleave Address Enable** See the description on Rank 0 (Rx58).	**RINLV3AEN[2:0]**

Following is an example, which shows a possible register settings for a system with 2 double-sided DIMM installed.

(1) Rx53[3:2] (RINLV1SEL_[1:0]) = 2 and Rx53[1:0] (RINLV0SEL_<1:0>)=2 selects A6, A18, A19 as the Rank Interleave Address for the system.

(2) If the settings on the Rank Interleave Address Selection of Rank 0, 1, 2, 3 (Rx58-5B[6:4]) are
Rx58[6:4] (RINLV0AS) = 001b
Rx59[6:4] (RINLV1AS) = 000b
Rx5A[6:4] (RINLV2AS) = 010b
Rx5B[6:4] (RINLV3AS) = 011b

And if the Rank Interleave Address Enable of Rank 0, 1, 2, 3 (Rx58-5B[2:0]) are
Rx58[2:0] (RINLV0AEN) = 011b
Rx59[2:0] (RINLV1AEN) = 011b
Rx5A[2:0] (RINLV2AEN) = 011b
Rx5B[2:0] (RINLV3AEN) = 011b

With the above register settings, Rank Interleave Address 2, A6, is ignored for the system, and the four ranks of the system are decided by A18 and A19 as shown in the following table.

A18	A19	Selected Rank
0	0	Rank#1
0	1	Rank#0
1	0	Rank#2
1	1	Rank#3

DRAM Timing (60–64h)

Offset Address: 60h (D0F3)

DRAM Pipeline Turn-Around Setting **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**0ws Back-to-Back Write to Different DDR Rank** 0: Disable 1: Enable
6	RW	0	**Fast Read-to-Read Turn Around** 0: Disable 1: Enable (DQS post-amble overlap with preamble)
5	RW	0	**Fast Read-to-Write Turn Around** 0: Disable 1: Enable
4	RW	0	**Fast Write-to-Read Turn Around** 0: Disable 1: Enable
3:2	—	00	**Reserved**
1	RW	0	**0ws DRAM Channel Switching Between Read Cycles** 0: Disable 1: Enable This function is valid in 64-Bit mode.
0	RW	0	**0ws DRAM Channel Switching Between Write Cycles** 0: Disable 1: Enable This function is valid in 64-bit mode.

Offset Address: 61h (D0F3)

DRAM Timing for All Ranks **Default Value: 44h**

Bit	Attribute	Default	Description
7:6	RW	01b	**Write Recovery Time (tWR) –** 00: 2T 01: 3T 10: 4T 11: 5T
5:0	RW	04h	**Refresh-to-Active or Refersh-to-Refresh (tRFC)** 00: 8T 01h: 9T … 0nh: (8+n)T 3eh: 70T 3f:h: 71T

Offset Address: 62h (D0F3)
DRAM Timing for All Ranks **Default Value: 21h**

Bit	Attribute	Default	Description
7:4	RW	0010b	**Active-to-Precharge (tRAS)** 0000: 5T 0001: 6T … 0nh: (5+n)T 1110: 19T 1111: 20T
3	RW	0	**Enable DDR2 8-Bank Device Timing Constraint (tRRD and tRP).**
2:0	RW	001	**CAS Latency** DDR DDR2 000 1.5 2 001 2 3 010 2.5 4 011 3 5 1xx reserved reserved

Offset Address: 63h (D0F3)
DRAM Timer for All Ranks **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00	**Active-to-Active Period (tRRD)** 00: 2T 01: 3T 10: 4T 11: 5T
5:4	—	00	**Reserved**
3	RW	0	**Read-to-Precharge Delay (tRTP)** 0: 2T 1: 3T
2	—	0	**Reserved**
1	RW	0	**Write to Read Command Delay (tWTR)** DDR DDR2 0 1T 2T 1 2T 3T
0	—	0	Reserved

Offset Address: 64h (D0F3)
DRAM Timer for All Ranks **Default Value: 04h**

Bit	Attribute	Default	Description
7:6	RW	00	**Active to Read or Write Delay (tRCD)** 00: 2T 01: 3T 10: 4T 11: 5T
5	—	0	**Reserved**
4	RW	0	**CKE Minimum Pulse Width** 0: 2T 1: 3T This function is valid when RDYNCKE=1 (F4RXA1[6])
3:2	RW	01	**Precharge Period (tPR)** 00: 2T 01: 3T 10: 4T 11: 5T
1	—	0	**Reserved**
0	RW	0	**Exit Precharge/Active Power Down to Any Command Delay** 0: 1T 1: 2T This function is valid when RDYNCKE=1 (F4RXA1[6])

DRAM Queue / Arbitration (65–67h)

Offset Address: 65h (D0F3)
DRAM Arbitration Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**AGP Timer** (unit of 4 DCLKS) DRAMC time slot allocated for AGP device.
3:0	RW	0	**Host Timer** (unit of 4 DCLKS) DRAMC time slot allocated for Host.

Offset Address: 66h (D0F3)
DRAM Queue / Arbitration **Default Value: 00h**

Bit	Attribute	Default	Description	Mnemonic
7	RW	0	**DRAMC Queue Size Greater Than 2** 0: No 1: Yes	
6	RW	0	**DRAMC Queue Size Not Equal To 4** 0: No 1: Yes To setup DRAMC queue size of 2, set Rx66[7:6] to 2'b00; sets Rx66[7:6] to 2'b11 for queue size of 3; sets Rx[7:6] to 2'b10 for queue size of 4.	
5:4	RW	00	**Arbitration Parking Policy** 00: Park at the last bus owner 01: Park at CPU 10: Park at AGP 11: Reserved	
3:0	RW	0000	**Priority Promotion Timer** (in unit of 4 DCLKs) A DRAM request is promoted to become a high priority request when it is pending over PTIM*4 DRAM cycles.	**PTIM[3:0]**

Offset Address: 67h (D0F3)
DIMM Command / Address Selection **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	—	00	**Reserved**
3:2	RW	0	**DIMM 1 Command / Address Selection**
1:0	RW	0	**DIMM 0 Command / Address Selection**

DRAM Control (68–69h)

Offset Address: 68h (D0F3)
DDR Page Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0000	**Page Register Life Timer (in unit of 16 DCLKs)** When timer expired, the expired page will be closed.
3:0	RW	0000	**DRAM Expired Page Threshold** Close expired pages with precharge-all command when the number of expired pages exceeds the value.

Offset Address: 69h (D0F3)
DDR Page Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	0	**Bank Interleave** 00: No interleave 01: 2-bank 10: 4-bank 11: 8 bank
5	RW	0	**Enable Bank Address Scramble** When set to 1, BA0=A13^A15^A17^A19, BA1=A12^A14^A16^A18^A20
4	RW	0	**Auto-Precharge for TLB Read and CPU Write-Back** 0: Disable 1: Enable
3:2	—	0	**Reserved**
1	RW	0	**Keep Page Active When Cross Bank** 0: Disable 1: Enable
0	RW	0	**Multiple Page Mode** 0: Disable 1: Enable

Refresh Control (6A–6Bh)

Offset Address: 6Ah (D0F3)
Refresh Counter **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Refresh Counter (**in unit of 16 DRAM CLKs**)** When set to 00, DRAM refresh is disabled

Offset Address: 6Bh (D0F3)
DRAM Miscellaneous Control **Default Value: 10h**

Bit	Attribute	Default	Description
7	RW	0	**DQS Input DLL Adjustment** 0: Disable 1: Enable
6	RW	0	**DQS Output DLL Adjustment** 0: Disable 1: Enable
5	RW	0	**Burst Refresh** 0: Disable 1: Enable
4	RW	1	**DLL Manual Reset** 0: Disable 1: Enable
3	RW	0	**Enable Memory Size Detection, MA 32/16 33/17 Swap** 0: Disable 1: Enable
2:0	RW	0	**SDRAM Operation Mode Select** 000: Normal SDRAM Mode 001: NOP Command Enable 010: All-Banks-Precharge Command Enable. 011: MRS to SCMD 100: CBR, CAS-before-RAS refresh, Cycle Enable 101: Reserved 11x: Reserved

DDR SDRAM Control (6C–6Fh)

Offset Address: 6Ch (D0F3)

DRAM Type **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**DDR2 DRAM Support** 0: Disable DDR2 1: Enable DDR2
6	RO	—	**Memory Type Detected (through pin: MEMDET)** 0: DDR 1: DDR2
5	—	0	**Reserved**
4	RW	0	**Disable DQM pins**
3	RW	0	**SDRAM Effective Burst Length** For 64-bit mode ranks, SDRAM MRS 0: BL4 1: BL8
2:0	—	0	**Reserved**

Offset Address: 6Dh (D0F3)

Reserved **Default Value: C0h**

Bit	Attribute	Default	Description
7:6	—	11	**Reserved**
5:0	—	00	**Reserved**

Note: If ODT is not supported, the registers can be programmed, i.e. the function of MD/CS mapping can work.

Offset Address: 6Fh (D0F3)

Miscellaneous Control **Default Value: 40h**

Bit	Attribute	Default	Description
7	RW	0	**Non-ONBD Protection for GART Table Fetching** 0: Disable 1: Enable
6	RW	1	**DRAM-Side-Input-Pointer Non-Return-Zero Mode** 0: Disable 1: Enable Enable to avoid overwrite data
5	RW	0	**Disallow the 2nd Cycle of a 2T Command Overlapped with Command of Different Type on a Different MA/SCMD Bus** 0: Allow 1: Not allow Sets this bit to 1 when read-modify-write mode is enabled (for example, ECC mode).
4	RW	0	**Read-Modify-Write (RMW) Option** When enabled, RMW is processed in relaxed mode.
3	RW		**Applying Same-Channel IO Turn-Around Constraints between Different Channels**
2	RW	0	**Exclusive SCMD Buses** When enabled, the two SCMD buses are exclusive, do not have commands in the same cycle.
1	—	0	**Reserved**
0	RW	0	**GART Table Access Option** When enabled, GART Table accessing is in relaxed mode. Set this bit to 1 in DDR400 mode.

DRAM Signal Timing Control (70–7Fh)

Offset Address: 73 - 70h (D0F3)

MD / DQS Output Delay Control **Default Value: 0000 0000h**

Offset Address	Attribute	Default	Description
71h	RW	0	**Channel A MD Output Delay**
70h	RW	0	**Channel A DQS Output Delay**

Note: these delay registers are in Gray code format.

Offset Address: 74h (D0F3)
DQS Output Clock Phase Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	—	0	**Reserved**
2:0	RW	0	**Initial Phase of Internal Clocks for DQS Output on Channel A** Each steps increase a phase of 1/8 T

Offset Address: 75h (D0F3)
DQ Output Clock Phase Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	—	0	**Reserved**
2:0	RW	0	**Initial Phase of Internal Clocks for DQ Output on Channel A** Each steps increase a phase of 1/8 T

Offset Address: 76h (D0F3)
Write Data Phase Control **Default Value: 00h**

Bit	Attribute	Default	Description	Mnemonic
7	RW	0	**1 More Pipeline Stage on Write Data Path** Will provide safer timing margin but lower performance.	—
6	—	0	**Reserved**	—
5	RW	0	**DQ/DQS output clocks bypass delay component (RX70-73 functionless)**	—
4	—	0	**Reserved**	—
3:2	RW	00	**Advance Write Phase Signals to Make Room for the Long Bus Delay** 00: Normal mode 01: Advance 1 cycle 10: Advance 2 cycle 11: Forbidden The 2 bits must be used with Bit [1:0] (RDWPH[1:0]).	—
1:0	RW	00	**Write MD/DQS/CAS Output Timing Range Control** Each increased step delays the output range by 1/4 T.	**RDWPH[1:0]**

Offset Address: 77h (D0F3)
DQS Input Delay Calibration **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Manual DQS Input Delay Setting** 0:Auto 1: Manual
6	—	0	**Reserved**
5:0	RW	0	**DDR DQS Input Delay** This is the base delay value of DQS input signal in Gray code format. The reading value depends on Rx77[7]. If Rx77[7] = 0 (auto mode), DLL calibration result is returned when read.

Offset Address: 78h (D0F3)
Channel A DQS Input Capture Range Control **Default Value: 80h**

Bit	Attribute	Default	Description
7	RW	1	**Manual DQS Input Capture Range Setting for Channel A** 0: Auto 1: Manual
6	RW	0	**Enable DQS Input Capture Range Detection for Channel A**
5:0	RW	00	**DQS Input Capture Range for Channel A** **Bit [5:4]** 00: 1T prior to 1st DQS rising edge 01: at 1st DQS rising edge 10: 1T after 11: Reserved **Bit [3:1] 1/8T delay** **Bit [0] 0.35ns fine tune delay**

Offset Address: 7Ah (D0F3)
DQS Input Capture Range Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	—	0	**Reserved**
3	RW	0	**Select DQS Input Pin as Input Capture Range Detection Signal** 0: DQSA0 1: DQSA4
2:0	RW	000	**DQS Input Capture Range Offset Value for Channel A** 1/8T per step, 2's complement

Offset Address: 7Bh (D0F3)
Read Data Phase Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	—	0	**Reserved**
6:4	RW	000	**MD Input Data Push Timing Control** 00: Start moving data into internal buffer 1T after the 1st DRAM strobe 01: 1.5T 10: 2T 11: 2.5T
3:1	—	0	**Reserved**
0	RW	0	**Extend DQS Input Capture Range 1/2T Earlier**

Read-Only Control (7C-7Fh)

Offset Address: 7Ch (D0F3)
Channel A DQS Input Delay Offset Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6:0	RW	0	**Channel A DQS Input Delay Offset (In two's complement)** This is the offset values (in 2's complement format) from the base delay value (Rx77[5:0]) for Channel A DIMM.

Shadow RAM Control (80–83h)

Offset Address: 80h (D0F3)
Page-C ROM Shadow Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00	**CC000-CFFFFh Memory Space Access Control** 00: Read / Write Disable 01: Write Enable 10: Read Enable 11: Read / Write Enable
5:4	RW	00	**C8000-CBFFFh Memory Space Access Control**
3:2	RW	00	**C4000-C7FFFh Memory Space Access Control**
1:0	RW	00	**C0000-C3FFFh Memory Space Access Control**

Offset Address: 81h (D0F3)
Page-D ROM Shadow Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00	**DC000-DFFFFh Memory Space Access Control** 00: Read / Write Disable 01: Write Enable 10: Read Enable 11: Read / Write Enable
5:4	RW	00	**D8000-DBFFFh Memory Space Access Control**
3:2	RW	00	**D4000-D7FFFh Memory Space Access Control**
1:0	RW	00	**D0000-D3FFFh Memory Space Access Control**

Offset Address: 82h (D0F3)
Page-E ROM Shadow Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00	**EC000-EFFFFh Memory Space Access Control** 00: Read / Write Disable 01: Write Enable 10: Read Enable 11: Read / Write Enable
5:4	RW	00	**E8000-EBFFFh Memory Space Access Control**
3:2	RW	00	**E4000-E7FFFh Memory Space Access Control**
1:0	RW	00	**E0000-E3FFFh Memory Space Access Control**

Offset Address: 83h (D0F3)
Page-F ROM, Memory Hole and SMI Decoding **Default Value: 00h**

Bit	Attribute	Default	Description	Mnemonic
7:6	—	0	**Reserved**	
5:4	RW	00	**F0000-FFFFFh Memory Space Access Control** 00: Read / Write Disable 01: Write Enable 10: Read Enable 11: Read / Write Enable	
3:2	RW	00	**Memory Hole** 00: None 01: 512K – 640K 10: 15M – 16M (1M) 11: 14M – 16M (2M)	
1	RW	0	**Disable Data Access on SMRAM (Page A, B) in SM Mode** 0: In SM mode, page A,B CPU Data R/W cycles are forwarded to the memory controller. 1: In SM mode, page A,B CPU Data R/W cycles are forwarded to the PCI bus Notes: 1. This bit is effective when Rx83[0] is set to 0. 2. SMRAM page A,B Code R/W cycles are always forwarded to the memory controller in SM mode.	**RABKDOFF**
0	RW	0	**Enable Page A, B DRAM Access In Normal Mode** 0: Page A, B CPU R/W cycles could be forwarded to memory controller or PCI bus depends on the setting of RABKDOFF (bit 1), the CPU operating mode (Normal or SM mode) as well as the type (Code or Data) of the CPU cycle. 1: Page A, B CPU R/W cycles (Code and Data) are always (in either Normal or SM mode) forwarded to the memory controller. Check the following table for details.	**RRWABK**

Table 13. CPU-to-SMRAM Cycle Flow

RABKDOFF (Rx83[1])	RRWABK (Rx83[0])	CPU MODE	Target of CODE Acces Cycle	Target of DATA Access Cycle
x	0	Normal	PCI	PCI
0	0	SMM	DRAM	DRAM
1	0	SMM	DRAM	PCI
x	1	Normal / SMM	DRAM	DRAM

DRAM Above 4G Support (84-8D)

Offset Address: 84h (D0F3)
Low Top Address - Low **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0000	**Low Top Address - A[23:20]**
3:0	—	0000	**Reserved**

Offset Address: 85h (D0F3)
Low Top Address - High **Default Value: FFh**

Bit	Attribute	Default	Description
7:0	RW	FFh	**Low Top Address – A[31:24]**

Offset Address: 86h (D0F3)
SMM and APIC Decoding **Default Value: 01h**

Bit	Attribute	Default	Description	Mnemonic
7:6	—	0	**Reserved**	
5	RW	0	**APIC Lowest Interrupt Arbitration** 0: Disable 1: Enable	
4	RW	0	**IO APIC Decoding** 0: Cycles accessing FECx_xxxxh are passed to PCI1 1: Cycles accessing FEC7_FFFFh - FEC0_0000h are passed to PCI1; cycles accessing FECF_FFFFh - FEC8_0000h access cycles are passed to PCI2.	
3	RW	0	**MSI Support (Processor Message Enable)** 0: Cycles accessing FEEx_xxxxh from masters are passed to PCI1 (PCIC will not claim) 1: Cycles accessing FEEx_xxxxh from masters are passed to the Host side for snooping	
2	RW	0	**Top 1MB SM Memory Enable** 0: Disable 1: Enable TSMMA[31:20] = {LOWTOPA[31:24],4'h0} – {FBSZ[2:0],1'b0}; OSLOWTOPA[31:20] = TSMMA[31:20] – RTSMMEN	**RTSMMEN**
1	—	0	**Reserved**	
0	RW	1	**Compatible SMM Enable** 0: Disable 1: Enable	

Offset Address: 89-88h (D0F3)
Misc. DRAM Address Setting **Default Value:0000h**

Bit	Attribute	Default	Description
15:11	—	0	**Reserved**
10:0	RW	0	**The Address Next to the Last Valid DRAM Address**

Offset Address: 8Ch (D0F3)
DQS Output Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:2	—	0	**Reserved**
1	RW	0	**MD/DQS Earlier Output Enable** MDOE 1/2T earlier DQSOE 1/2T earlier if RDSOLNGPRE=0
0	RW	0	**DQS Earlier Output Enable** DQSOE 1/4T earlier if RDSOLNGPRE2=1

DRAM Clocking Control (90-9F)

Offset Address: 90h (D0F3)

DRAM Clock Operation Mode and Frequency **Default Value: 01h**

Bit	Attribute	Default	Description
7:3	—	00h	**Reserved**
2:0	RW	001	**DRAM Operating Frequency** 000: 100MHz 001: 133MHz 010: 166MHz 011: 200MHz 100: 266MHz 101: 333MHz 110/111: Reserved

Offset Address: 92h (D0F3)

CS/CKE Clock Phase Control **Default Value: 00h**

Bit	Attribute	Default	Description
6:3	RW	00	**Reserved**
2:0	RW	0	**Channel A Sampling Clock Phase Select for CS/CKE** Each step increases a phase of 1/8 T

Offset Address: 93h (D0F3)

SCMD/MA Clock Phase Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	—	00	**Reserved**
2:0	RW	0	**Channel A Sampling Clock Phase Select for SCMD/MA** Each step increases a phase of 1/8 T

Offset Address: 94h (D0F3)

DCLKO Feedback Mode Output Control **Default Value: 01h**

Bit	Attribute	Default	Description
7:3	—	00	**Reserved**
2:0	RW	001	**DCLKO Feedback Mode Output Control** For Rx90[6] (RNODCLKIN) = 0 mode, if DCLKOA is fed back to DCLKIA, each increased step makes DCLKOB earlier; if DCLKOB is fed back to DCLKIA, each increased step delays DCLKOA (1/8T per step).

UMA Registers (A0–A5h)

Offset Address: A1-A0h (D0F3)

CPU Direct Access Frame Buffer Control **Default Value: 00h**

Bit	Attribute	Default	Description
15	RW	0	**VGA enable**
14:12	RW	0	**Frame buffer size selection** 100: 16M 101: 32M 110: 64M Others: Reserved
11:1	RW	0	**A<31:21>**
0			**CPU direct access frame buffer enable**

Offset Address: A2h (D0F3)

VGA Timer I **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**VGA high priority timer (unit of 16 DCLK)**
3:0	RW	0	**VGA Timer (unit of 16 DCLK)**

Offset Address: A3h (D0F3)

VGA Timer II **Default Value: 00h**

Bit	Attribute	Default	Description
7:2	—	0	**Reserved**
1:0	RW	0	**Probing signal select**

Offset Address: A5-A4h (D0F3)

GFX Misc. **Default Value: 00h**

Bit	Attribute	Default	Description
15:14	—	0	**Reserved**
13	RW	0	**Reset internal GFX by BIOS**
12	—	0	**Reserved**
11:10	RW	0	**Fine tune GFX PCICLK** 00: default; 01: delay 0.1 ns; 10: early 0.15 ns; 11: early 0.3 ns
9:8	RW	0	**Fine tune GFX MCK** 00: default; 01: delay 0.1 ns; 10: early 0.15 ns; 11: early 0.3 ns
7:5	—	0	**Reserved**
4	RW	0	**GRLD delay 1 cycle (GFX low priority read data 1T delay)** 0: no delay; 1: delay 1T
3:2	—	0	**Reserved**
1			**Enable AGP DIO (PAD) clock**
0			**GFX data delay to sync with clock (0:no sync, 1:sync with clock)**

GMINT and AGPCINT Registers (B0–B8h)

Offset Address: B1-B0h (D0F3)

GMINT Misc. **Default Value: 00h**

Bit	Attribute	Default	Description
15:12	RW	0	**Switching timer from high channel to low channel (unit of 16 DCLK)**
11:8	RW	0	**Switching timer from low channel to high channel (unit of 16 DCLK)**
7	RW	0	**Disable synced registers for GFX request-related signals to GMINT** 0: sync 1T, 1: bypass sync logic
6	RW	0	**Allow GMINT low channel issue 8QW request** (Coordinate with f2rx54<4>)
5	RW	0	**Allow GMINT high channel issue 8QW request** (Coordinate with f2rx54<4>)
4:3	—	0	**Reserved**
2:0	RW	0	**Frame buffer rank**

Offset Address: B8h (D0F3)

AGPCINT Misc. **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	—	0	**Reserved**
3	RW	0	**Allow AGPCINT issue 8QW request** (Coordinate with f2rx54<4>)
2	RW	0	**GFX AGP read data sync 1T**
1	RW	0	**Disable AGPCINT pipe mode**
0	RW	0	**Reserved**

DDR2 – I/O Pad Control (D0–D3h)

Offset Address: D0h (D0F3)

DQ / DQS Termination Strength Manual Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**DQ/DQS Pull-up Termination Strength Manual Setting**
3:0	RW	0	**DQ/DQS Pull-down Termination Strength Manual Setting**

Offset Address: D1h (D0F3)

DQ / DQS Termination Strength Status **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**DQ/DQS Pull-up Termination Strength Auto-comp Value**
3:0	RO	0	**DQ/DQS Pull-down Termination Strength Auto-comp Value**

Offset Address: D2h (D0F3)

DQ Driving Strength Status **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**DQ Pull-up Driving Strength Auto-comp Value**
3:0	RO	0	**DQ Pull-down Driving Strength Auto-comp Value**

Offset Address: D3h (D0F3)

Compensation Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:2	—	0	**Reserved**
1	RW	0	**DDR Compensation Auto Mode** 1: Disable Auto Mode 0: Enable Auto Mode If DDR Compensation and DDR Auto Compensation are both enabled, the ODT settings for all DRAM pads are from auto-comp circuit (RxD1); otherwise, if Auto Compensation is disabled, the ODT settings are from manual setting (RxD0).
0	RW	0	**DDR Compensation** 1: Enable 0: Disable Disable DDR Compensation provides a power saving mode, however, the values of RxD1 and RxD2 should be ignored.

Note: The DQ driving bits of RxD2 is the result of the auto-comp circuit; however, there is no "auto-mode" for the DQ/DQB driving control since it depends on the actual number of ranks in the DRAM data channel

DDR2 - ODT Control (D4–D7h)

Offset Address: D4h (D0F3)

ODT Pullup / Pulldown Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Enable NB pad ODT** 1: Enable ODT when reading data 0: Disable ODT unless RxD4[3:0] is not equal to 0
6:4	—	0	**Reserved**
3	RW	0	**ODT Pullup Enable**
2	—	0	**Reserved**
1	RW	0	**ODT Pulldown Enable**
0	—	0	**Reserved**

Offset Address: D5h (D0F3)

ODT Driving and Range Select **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Channel-A DQ ODT Driving Select** 0: Weak driving, for DDR or DDR2 without series resistance on MB 1: Strong driving for DDR2 with series resistance on MB
6	—	0	**Reserved**
5	RW	0	**Channel-A DQS ODT Driving Select**
4	—	0	**Reserved**
3	RW	0	**Channel-A DQ ODT Range Select** 1: 75 ohm 0: 150 ohm
2	—	0	**Reserved**
1	RW	0	**Channel-A DQS ODT Range Select** 1: 75 ohm 0: 150 ohm
0	—	0	**Reserved**

Offset Address: D6h (D0F3)
ODT Driving and Range Select **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**DCLKOA ODT Driving Select (DS)**
6	—	0	**Reserved**
5	RW	0	**SCMD/MAA Driving Select**
4	—	0	**Reserved**
3	RW	0	**CKEA Driving Select**
2	—	0	**Reserved**
1	RW	0	**CKEA ODT Range Select (RS)**
0	—	0	**Reserved**

Offset Address: D8h (D0F3)
ODT Lookup Table for Channel A **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	0	**Rank 3 ODT Signal Selection** 00:ODTA0 01: ODTA1 10:ODTA2 11: ODTA3
5:4	RW	0	**Rank 2 ODT Signal Selection**
3:2	RW	0	**Rank 1 ODT Signal Selection**
1:0	RW	0	**Rank 0 ODT Signal Selection**

Offset Address: DAh (D0F3)
SDRAM ODT Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**DDR2 SDRAM ODT Control** 0: Disable 1: Enable
6:1	—	0	**Reserved**
0	RW	0	**Channel A Differential DQS Input** 0: Disable 1: Enable

Offset Address: DCh (D0F3)
Channel A DQ/DQS CKG Output Delay Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00	**DQ/DQS Delay Control for Group A3** 00: Default 01: Delays100ps 10: Delays 200ps 11: Delays 300ps
5:4	RW	00	**DQ/DQS Delay Control for Group A2**
3:2	RW	00	**DQ/DQS Delay Control for Group A1**
1:0	RW	00	**DQ/DQS Delay Control for Group A0**

Offset Address: DDh (D0F3)
Channel A DQ/DQS CKG Output Delay Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00	**DQ/DQS Delay Control for Group A7** 00: Default 01: Delays100ps 10: Delays 200ps 11: Delays 300ps
5:4	RW	00	**DQ/DQS Delay Control for Group A6**
3:2	RW	00	**DQ/DQS Delay Control for Group A5**
1:0	RW	00	**DQ/DQS Delay Control for Group A4**

DRAM Driving Control(E0–EFh)

Table 14. Physical Pin to Driving Group Mapping Table

Physical Pins	DCLKA	CKEA	CSA	MAA	DQA	DQSA	MPD/DQMA
Driving Group	DCLKA	CSA	CSA	MAA	DQA	DQSA	DQA

Offset Address: E0h (D0F3)
DRAM Driving – Group DQSA **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**DQSA - PMOS Driving**
3:0	RW	0	**DQSA - NMOS Driving**

Offset Address: E2h (D0F3)
DRAM Driving – Group DQA (MD, MPD, DQS, DQM) **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**DQA - PMOS Driving**
3:0	RW	0	**DQA - NMOS Driving**

Offset Address: E4h (D0F3)
DRAM Driving – Group CSA (CS, DQM, MPD) **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**CSA – PMOS Driving**
3:0	RW	0	**CSA – NMOS Driving**

Offset Address: E6h (D0F3)
DRAM Driving – Group DCLKA **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**DCLKA – PMOS Driving**
3:0	RW	0	**DCLKA – NMOS Driving**

Offset Address: E8h (D0F3)
DRAM Driving – Group MAA **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**MAA – PMOS Driving**
3:0	RW	0	**MAA – NMOS Driving**

Offset Address: EAh (D0F3)
DRAM Driving – Group SCMDA **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**SCMDA – PMOS Driving**
3:0	RW	0	**SCMDA – NMOS Driving**

Offset Address: ECh (D0F3)

Channel-A DQS / DQ CKG Duty Cycle Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00	**DQS CKG Falling Edge Control** 00: Default 01: Falling edge delays 100 ps 10: Falling edge delays 200 ps 11: Falling edge delays 300 ps
5:4	RW	00	**DQS CKG Rising Edge Control** 00: Default 01: Rising edge delays 100 ps 10: Rising edge delays 200 ps 11: Rising edge delays 300 ps
3:2	RW	00	**DQ CKG Falling Edge Control** 00: Default 01: Falling edge delays 100 ps 10: Falling edge delays 200 ps 11: Falling edge delays 300 ps
1:0	RW	00	**DQ CKG Rising Edge Control** 00: Default 01: Rising edge delays 100 ps 10: Rising edge delays 200 ps 11: Rising edge delays 300 ps

Offset Address: EEh (D0F3)

DCLK Output Duty Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00	**Duty Control for DCLKA** 00: Default 01: Falling edge delays 100 ps 10: Falling edge delays 200 ps 11: Falling edge delays 300 ps
5:4	RW	00	**Duty Control for DCLKA** 00: Default 01: Rising edge delays 100 ps 10: Rising edge delays 200 ps 11: Rising edge delays 300 ps
3:0	—	0	**Reserved**

Offset Address: EFh (D0F3)

DQS CKG Input Delay Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	—	0	**Reserved**
5:4	RW	00	**Duty Control for DQSA** 00: -150 ps 01: 0 ps 10: 150 ps 11: 300 ps
3:0	—	0	**Reserved**

Device 0 Function 4 (D0F4): Power Management Control

Header Registers (0-3Fh)

Offset Address	Attribute	Default	Description
1 – 0h	RO	1106h	Vendor ID
3 – 2h	RO	4314h	Device ID –Power Management Control
5 – 4h	RO	0006h	PCI Command
7 – 6h	RO	0200h	PCI Status
8h	RO	00	Revision ID
0B – 9h	RO	060000h	Class Code
0Dh	RO	00	Latency Timer
0Eh	RO	00	Header Type
0Fh	RO	00	BIST
13 – 10h	—	—	Reserved
2D – 2Ch	RW1	00	Subsystem Vendor ID
2F – 2Eh	RW1	00	Subsystem ID
33 – 30h	RO	00	Reserved
37 – 34h	RO	00	Capability Pointer
3F – 38h	—	—	Reserved

Power Management Control (A0–EFh)

Offset Address: A0h (D0F4)

Power Management Mode **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Dynamic Power Management** 0: Disable 1: Enable
6	RW	0	**Power Management during HALT / SHUTDOWN** 0: Disable 1: Enable
5	RW	0	**Power Management during STPCLK** 0: Disable 1: Enable
4	RW	0	**Power Management during SUSSTAT** 0: Disable 1: Enable
3:0	—	0	**Reserved**

Offset Address: A1h (D0F4)

DRAM Power Management **Default Value: 00h**

Bit	Attribute	Default	Description
7	—	0	**Reserved**
6	RW	0	**Dynamic CKE When DRAM Idle** 0: Disable 1: Enable
5	RW	0	**Dynamic DRAM I/O Pad Power-Down (i.e. Float)** 0: Disable 1: Enable
4:0	—	0	**Reserved**

Note: The DRAM power management mode is defined as HALT/SHUTDOWN, STPCLK and SUSSTAT triggered

Offset Address: A2h (D0F4)
Dynamic Clock Stop Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Host Interface Power Management** 0: Disable 1: Enable
6	RW	0	**DRAM Interface Power Management** 0: Disable 1: Enable
5	RW	0	**V-Link Interface Power Management** 0: Disable 1: Enable
4	RW	0	**AGP Interface Power Management** 0: Disable 1: Enable
3	RW	0	**PCI2 Interface Power Management** 0: Disable 1: Enable
2	RW	0	**Graphics Interface (GMINT) Power Management** 0: Disable 1: Enable
1	RW	0	**VKCFG Interface Power Management** 0: Disable 1: Enable
0	RW	0	**Host Fast Power-Management (DADS Fast Timing)** 0: Disable 1: Enable

Offset Address: A3h (D0F4)
Clock Gathering Control 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	Using BREQ0# to predict CPU transaction and do more aggressive dynamic clock, basic this clock replace nearly all free-running clock inside CPU Interface
6	RW	0	**Wait up RRDY clock for DRAM controller**
5	RW	0	**Host C2P Clock Gating** 0: Disable 1: Enable
4	RW	0	**Dynamic Clock Gating for C2P1 Transaction inside CPU Interface** 0: Disable 1: Enable
3	RW	0	**Enable dynamic clock gating for C2P2 transaction inside CPU Interface** 0: Disable 1: Enable
2	RW	0	**Host P2C Clock Gating** 0: Disable 1: Enable
1:0	—	0	**Reserved**

Offset Address: A4h (D0F4)
Clock Gathering Control 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Dynamic Read Clock Gating** 0: Disable 1: Enable
6	RW	0	**Dynamic Write Clock Gating** 0: Disable 1: Enable
5	RW	0	**Dynamic Page Table Clock Gating** 0: Disable 1: Enable
4	RW	0	**Dynamic GART Table Clock Gating** 0: Disable 1: Enable
3	RW	0	**Latch queue write-enable dynamic clock gating inside P6IF, include IOQ, PWQ, PAQ** 0: Disable 1: Enable
2	RW	0	**DIO, PAD Related Dynamic Clock Gating, include 2X in/out CCLK, 1X clock for PAD** 0: Disable 1: Enable
1	RW	0	**Dynamic MA/SCMD Clock on MA/SCMD Pads** 0: Disable 1: Enable
0	—	0	**Reserved**

Offset Address: A5h (D0F4)
Clock Gathering Control 3 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**V-Link Dynamic Clock** 0: Disable 1: Enable
6	RW	0	**Pcic P2C Clock Gating** 0: Disable 1: Enable
5	RW	0	**Pcic P2P Clock Gating** 0: Disable 1: Enable
4	RW	0	**Pcic C2P Clock Gating** 0: Disable 1: Enable
3:0	—	0	**Reserved**

Offset Address: A6h (D0F4)
Clock Gathering Control 4 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**GMINT Dynamic Clock** 0: Disable 1: Enable
6	RW	0	**GMINT Read Clock Gating** 0: Disable 1: Enable
5	RW	0	**GMINT Write Clock Gating** 0: Disable 1: Enable
4	RW	0	**1'b1 -> power down the AGP PADs' input differential comparator when idle**
3	—	0	**Reserved**
2	RW	0	**AGPCINT Dynamic Clock** 0: Disable 1: Enable
1	RW		**PCIC Dynamic Clock** 0: Disable 1: Enable
0			**DBX Dynamic Clock** 0: Disable 1: Enable

Offset Address: A7h (D0F4)
Clock Gathering Control 5 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Graphics DCLK Clock Gating** 0: Disable 1: Enable
6	RW	0	**GFX GCLK Clock Gating** 0: Disable 1: Enable
5:4	RW	0	**Reserved**
3	RW	0	**System memory self-refresh with frame buffer being pre-charged.** 0: Disable 1: Enable
2:0	—	0	**Reserved**

Offset Address: A8h (D0F4)
C0T State Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**C0 Throttling State**
6	RW	0	**DIMM self-refresh in C0T state with GFX in D3 state** 0: Disable 1: Enable
5	RW	0	**DIMM self-refresh in C0T state with GFX in vertical blanking** 0: Disable 1: Enable
4	RW	0	**Non-page Mode in C0T** 0: Disable 1: Enable
3	RW	0	**DRAM throttle in C0T**
2	—	0	**Disableg PLL in C0T state with GFX_ENGC3ST || GFX_VBLANK**
1	RW	0	**PLL at C0T state when internal GFX enters D3 state**

Offset Address: A9h (D0F4)

C1 State Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**C1 state** 0: Disable 1: Enable
6	RW	0	**DIMM self-refresh in C1 state with GFX in D3 state** 0: Disable 1: Enable
5	RW	0	**DIMM self-refresh in C1 state with GFX in vertical blanking** 0: Disable 1: Enable
4	RW	0	**Non-page Mode in C1** 0: Disable 1: Enable
3	RW	0	**DRAM throttle in C1** 0: Disable 1: Enable
2	RW	0	**Disable PLL in C2 state with GFX_ENGC3ST || GFX_VBLANK** 0: Enable 1: Disable
1	RW	0	**Disable PLL at C1 state when internal GFX enters D3 state** 0: Enable 1: Disable
0	—	0	**Reserved**

Offset Address: AAh (D0F4)

C2 State Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**C2 State** 0: Disable 1: Enable
6	RW	0	**DIMM self-refresh in C2 state with GFX in D3 state** 0: Disable 1: Enable
5	RW	0	**DIMM self-refresh in C2 state with GFX in vertical blanking** 0: Disable 1: Enable
4	RW	0	**Non-page Mode in C2** 0: Disable 1: Enable
3	RW	0	**DRAM throttle in C2** 0: Disable 1: Enable
2	RW	0	**Disable PLL in C2 state with GFX_ENGC3ST || GFX_VBLANK** 0: Enable 1: Disable
1	RW	0	**Disable PLL at C2 state when internal GFX enters D3 state** 0: Enable 1: Disable
0	—	0	**Reserved**

Offset Address: ABh (D0F4)

C3 State Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**C3 state** 0: Disable 1: Enable
6	RW	0	**DIMM self-refresh in C3 state with GFX in D3 state** 0: Disable 1: Enable
5	RW	0	**DIMM self-refresh in C3 state with GFX in vertical blanking** 0: Disable 1: Enable
4	RW	0	**Non-page Mode in C3** 0: Disable 1: Enable
3	RW	0	**DRAM throttle in C3** 0: Disable 1: Enable
2	RW	0	**Disable PLL in C3 state with GFX_ENGC3ST || GFX_VBLANK** 0: Enable 1: Disable
1	RW	0	**Disable PLL at C3 state when internal GFX enters D3 state** 0: Enable 1: Disable
0	—	0	**Reserved**

Offset Address: ACh (D0F4)
C3D State Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**C3d State** 0: Disable 1: Enable
6	RW	0	**DIMM self-refresh in C3D state with GFX in D3 state** 0: Disable 1: Enable
5	RW	0	**DIMM self-refresh in C3D state with GFX in vertical blankin** 0: Disable 1: Enable **g**
4	RW	0	**Non-page Mode in C3D** 0: Disable 1: Enable
3	RW	0	**DRAM throttle in C3D** 0: Disable 1: Enable
2	RW	0	**Disable PLL in C3D state with GFX_ENGC3ST || GFX_VBL ANK** 0: Enable 1: Disable
1	RW	0	**Disable PLL at C3D state when internal GFX enters D3 state** 0: Enable 1: Disable
0	—	0	**Reserved**

Offset Address	Attribute	Default	Description
ADh	RW	00h	**ACPI IO Base Register** **CPU Interface knows LVL2 (RPMIOBA + 'h14) register is read**
AEh	RW	00h	**ACPI IO Base Register** **CPU Interface knows LVL2 (RPMIOBA + 'h14) register is read**

Offset Address: AFh (D0F4)
V-Link / Graphics Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**New V-Link Reconnecting Protocol.**
6:0	—	0	**Reserved**

Offset Address: DF-D0h (D0F4)
BIOS Extended Scratch Registers D **Default Value: 00h**

Offset Address	Attribute	Default	Description
DF – D0h	RW	0	**BIOS Extended Scratch Registers D**

Offset Address: EF-E0h (D0F4)
BIOS Extended Scratch Registers E **Default Value: 00h**

Offset Address	Attribute	Default	Description
EF – E0h	RW	0	**BIOS Extended Scratch Registers E**

Device 0 Function 7 (D0F7): V-Link North Bridge and South Bridge Control

Header Registers (0-3Fh)

Offset Address	Attribute	Default	Description
1 – 0h	RO	1106h	Vendor ID
3 – 2h	RO	7314h	Device ID –V-Link Control
5 – 4h	RO	0006h	PCI Command
7 – 6h	RO	0200h	PCI Status
8h	RO	00	Revision ID
0B – 9h	RO	060000h	Class Code
0Dh	RO	00	Latency Timer
0Eh	RO	00	Header Type
0Fh	RO	00	BIST
13 – 10h	—	—	Reserved
2D – 2Ch	RW1	00	Subsystem Vendor ID
2F – 2Eh	RW1	00	Subsystem ID
33 – 30h	—	00	Reserved
37 – 34h	RO	00	Capability Pointer
3F – 38h	—	—	Reserved

V-Link Control Interface (40–5Fh)

Offset Address: 40h (D0F7)

V-Link Specification ID **Default Value: 1nh**

Bit	Attribute	Default	Description	Mnemonic
7:0	RO	1nh	**Revision ID** The value of NVRID[3:0] depends on the type of SB which is paired with this chip.	**NVRID**

Offset Address: 41h (D0F7)

NB V-Link Capability **Default Value: 19h**

Bit	Attribute	Default	Description
7:6	—	0	**Reserved**
5	RO	0	**16-Bit Bus Width** 0: Not supported 1: Supported
4	RO	1	**8-Bit Width** 0: Not supported 1: Supported
3	RO	1	**4X Rate** 0: Not supported 1: Supported
2	RO	0	**2X Rate** 0: Not supported 1: Supported
1	—	0	**Reserved**
0	RO	1	**8X Rate** 0: Not supported 1: Supported

Offset Address: 42h (D0F7)

NB Downlink (C2P) Configuration **Default Value: 88h**

Bit	Attribute	Default	Description
7:4	RW	8h	**C2P, DNCMD, Maximum Request Depth** 0000: depth of 1 … 1111: depth of 16
3:0	RW	8h	**C2P Maximum Write Buffer Size** (from 1 to 16 DW)

Offset Address: 43h (D0F7)
NB Uplink (P2C) Status I **Default Value: 80h**

Bit	Attribute	Default	Description
7:4	RO	8h	**P2C, UPCMD, Maximum Pending Request Depth**
3:0	—	0	**Reserved**

Offset Address: 44h (D0F7)
NB Uplink (P2C) Status II **Default Value: 82h**

Bit	Attribute	Default	Description
7:4	RO	8h	**P2C Write Buffer Size** (max # of lines)
3:0	RO	2h	**P2P Write Buffer Size** (max # of lines)

Offset Address: 45h (D0F7)
NB V-Link Arbiter Timer **Default Value: 44h**

Bit	Attribute	Default	Description	Mnemonic
7:4	RW	4h	**V-Link Arbiter Timer for Normal Priority Request from SB** 0000: 0 VCLK 1000: 8*4 VCLK 0001: 1*4 VCLK 1001: 16*4 VCLK 0010: 2*4 VCLK 1010: 32*4 VCLK 0011: 3*4 VCLK 1011: 64*4 VCLK 0100: 4*4 VCLK 11--: NB holds the bus as long as there is pending downstream request	**RNNTM[3:0]**
3:0	RW	4h	**V-Link Arbiter Timer for High Priority Request from SB** 0000: 0 VCLK 1000: 8*2 VCLK 0001: 1*2 VCLK 1001: 16*2 VCLK 0010: 2*2 VCLK 1010: 32*2 VCLK 0011: 3*2 VCLK 1011: 64*2 VCLK 0100: 4*2 VCLK 11--: NB holds the bus as long as there is pending downstream request Note: see Table 15 for more details	**RNHTM[3:0]**

Offset Address: 46h (D0F7)
NB V-Link Miscellaneous Control **Default Value: 00h**

Bit	Attribute	Default	Description	Mnemonic
7	RW	0	**Down Stream High Priority** 0: Disable high priority down command 1: Enable high priority down command	
6	RW	0	**C2P Request Priority** 0: Normal priority for C2P request 1: High priority for C2P request	
5:4	RW	0	**Options of Combining Multiple STPGNT Cycles Into a V-Link Command** 00: Compatible mode: a V-Link command per STPGNT cycle 01: Combines 2 STPGNT cycles into a V-Link command 10: Combines 3 STPGNT cycles into a V-Link command 11: Combines 4 STPGNT cycles into a V-Link command	
3:2	RW	0	**V-Link Master Read/Write Access Ordering Rules** 00: High Priority Read allows to pass Normal Read (but not pass Write) 01: Read (High/Normal) allows to pass Write (High Priority R>Normal Priority R>Write) 1x: Read / Write are executed in order	**RINORDER**
1	RW	0	**Read Around Write** 0: Read always pass Write, if RINORDER (bit3) is 0 1: Allows up to 8 Read-Around-Write cycles before flushing the pending write, if bit 3 (RINORDER) is 0 **Read Around Write is disabled if bit3,(RINODER) is set to 1**	
0	—	0	**Reserved**	

Offset Address: 47h (D0F7)

NB V-Link Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	—	0	**Reserved**
5	RW	0	**C2P Read Acknowledge Return Priority** 0: V-Link decodes C2P Read ACK command right when it's received 1: C2P Read ACK waits till pending P2C write cycles are all flushed
4	—	0	**Reserved**
3	RW	0	**Dynamic STOP on Down Strobe** 0: Disable 1: Enable
2	RW	0	**Auto-Disconnect** 0: Disable 1: Enable
1	RW	0	**V-Link Disconnect Sequence for STPGNT Cycle** 0: Disable 1: Enable
0	RW	0	**V-Link Disconnect Sequence for HALT cycle** 0: Disable 1: Enable

Offset Address: 48h (D0F7)

V-Link Configuration – NB / SB **Default Value: 18h**

This register is used to configure V-Link bus controller on both North and South bridge chips.

Bit	Attribute	Default	Description	Mnemonic
7	RW	0	**Parity Check** 0: Disable 1: Enable	
6:5	—	0	**Reserved**	
4	RW	1	**8-Bit Width** 0: Disable 1: Enable	
3	RW	1	**4X Rate** 0: Disable 1: Enable	
2	—	0	**Reserved**	
1	RW	0	**V-Link Split Bus** 0: Disable 1: Enable Always set this bit to 1.	**RVKSPLT**
0	RW	0	**8X Rate** 0: Disable 1: Enable	**R8XVK**

	X: Multiples of 66MHz cycle	Bus Width	R8XVK – 8X (Rx48 bit-0)	RVKSPLT – Split Bus (Rx48 bit-1)
Mode0 - 8-bit VD Half Duplex	4X	8-bit ⬍	0	0
Mode1 – 8-bit VD Full Duplex	8X	4-bit ▲▼	1	1

Procedure to Enable / Disable V-Link-8X Mode:

1. BIOS sets Rx48[0] to 1
2. Hardware will automatically enter a disconnect sequence, and then both NB/SB will start V-LINK 8X mode. Then normal operation is then resumed.
3. To return to V-Link 4X mode, BIOS sets Rx48[0] to 0
4. Step 2. is then repeated.

Offset Address: 49h (D0F7)
SB V-Link Capability **Default Value: 19h**

Bit	Attribute	Default	Description
7:6	—	0	**Reserved**
5	RO	0	**16-Bit Width** 0: Not supported 1: Supported
4	RO	1	**8-Bit Width** 0: Not supported 1: Supported
3	RO	1	**4X Rate** 0: Not supported 1: Supported
2	RO	0	**2X Rate** 0: Not supported 1: Supported
1	—	0	**Reserved**
0	RO	1	**8X Rate** 0: Not supported 1: Supported

Offset Address: 4Ah (D0F7)
SB Downlink (C2P) Status **Default Value: 88h**

Bit	Attribute	Default	Description
7:4	RO	8h	**C2P, DNCMD, Maximum Request Depth** 0000: depth of 1 … 1111: depth of 16
3:0	RO	8h	**C2P Maximum Write Buffer Size** (from 1 to 16 DW)

Offset Address: 4Bh (D0F7)
SB Uplink (P2C) Configuration I **Default Value: 80h**

Bit	Attribute	Default	Description
7:4	RW	8h	**P2C, UPCMD, Maximum Pending Request Depth**
3:0	—	0	**Reserved**

Offset Address: 4Ch (D0F7)
SB Uplink (P2C) Configuration II **Default Value: 82h**

Bit	Attribute	Default	Description
7:4	RW	8h	**P2C Write Buffer Size** (max # of lines)
3:0	RW	2h	**P2P Write Buffer Size** (max # of lines)

Offset Address: 4Dh (D0F7)
SB V-Link Arbiter Timer **Default Value: 44h**

Bit	Attribute	Default	Description
7:4	RW	0100	**V-Link Arbiter Timer for Normal Priority Request from NB** 0000: 0 VCLK 1000: 8*4 VCLK 0001: 1*4 VCLK 1001: 16*4 VCLK 0010: 2*4 VCLK 1010: 32*4 VCLK 0011: 3*4 VCLK 1011: 64*4 VCLK 0100: 4*4 VCLK 11--: SB holds the bus as long as there is pending upstream request …….
3:0	RW	0100	**V-Link Arbiter Timer for High Priority Request from NB** 0000: 0 VCLK 1000: 8*2 VCLK 0001: 1*2 VCLK 1001: 16*2 VCLK 0010: 2*2 VCLK 1010: 32*2 VCLK 0011: 3*2 VCLK 1011: 64*2 VCLK 0100: 4*2 VCLK 11--: SB holds the bus as long as there is pending upstream request ……

Table 15. V-Link Bus Timer Operation

RNNTM[3:0] (Rx45[7:4])	RNHTM[3:0] (Rx45[3:0])	SB Request Priority	When to Relinquish the Occupied V-Link Bus
0000	0000	Normal/high	Immediately
0000	0001,0010,…	Normal/high	Immediately
0000	11xx	Normal/high	Immediately
0001,0010,…	0000	High	Immediately
0001,0010,…	0000	Normal	Wait for Normal timer expired
0001,0010,…	0001,0010,…	High	Wait for either Normal or high timer expired
0001,0010,…	0001,0010,…	Normal	Wait for Normal timer expired
0001,0010,…	11xx	Normal/high	Wait for Normal timer expired
11xx	0000	High	Immediately
11xx	0000	Normal	Wait until there is no internal request
11xx	0001,0010,…	High	Wait for High timer expired
11xx	0001,0010,…	Normal	Wait until there is no internal request
11xx	11xx	Normal/high	Wait until there is no internal request

Offset Address: 4Eh (D0F7)

SB Peripheral Device's Bus Priority **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**1394 Priority** 0: Low Priority 1: High Priority
6	RW	0	**NIC Priority** 0: Low Priority 1: High Priority
5	—	0	**Reserved**
4	RW	0	**USB Priority** 0: Low Priority 1: High Priority
3	—	0	**Reserved**
2	RW	0	**IDE Priority** 0: Low Priority 1: High Priority
1	RW	0	**AC97-ISA Priority** 0: Low Priority 1: High Priority
0	RW	0	**PCI1 Priority** 0: Low Priority 1: High Priority

Offset Address: 4Fh (D0F7)

SB V-Link Miscellaneous Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Upstream High Priority Command** 0: Disable 1: Enable high priority up command
6:4	—	0	**Reserved**
3	RW	0	**Dynamic STOP on Up Strobe** 0: Disable 1: Enable
2:1	—	0	**Reserved**
0	RW	0	**C2P Cycle Wait Till P2C Write Flushed** (except C2P Post-Write) 0: Disable 1: Enable

Offset Address: 57h (D0F7)

DRAM Last Rank Ending Address (HA[31:24]#) **Default Value: 01h**

Bit	Attribute	Default	Description
7:0	RO	01	**The Ending Address, HA[31:24]#, of the Last DRAM Rank**

Shadow RAM Control (61-6Fh)

Offset Address: 61h (D0F7)

Page-C ROM Shadow Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	0	**CC000-CFFFFh** 00: Read / Write Disable 01: Write Enable 10: Read Enable 11: Read / Write Enable
5:4	RW	0	**C8000-CBFFFh** 00: Read / Write Disable 01: Write Enable 10: Read Enable 11: Read / Write Enable
3:2	RW	0	**C4000-C7FFFh** 00: Read / Write Disable 01: Write Enable 10: Read Enable 11: Read / Write Enable
1:0	RW	0	**C0000-C3FFFh** 00: Read / Write Disable 01: Write Enable 10: Read Enable 11: Read / Write Enable

Offset Address: 62h (D0F7)

Page-D ROM Shadow Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	0	**DC000-DFFFFh** 00: Read / Write Disable 01: Write Enable 10: Read Enable 11: Read / Write Enable
5:4	RW	0	**D8000-DBFFFh** 00: Read / Write Disable 01: Write Enable 10: Read Enable 11: Read / Write Enable
3:2	RW	0	**D4000-D7FFFh** 00: Read / Write Disable 01: Write Enable 10: Read Enable 11: Read / Write Enable
1:0	RW	0	**D0000-D3FFFh** 00: Read / Write Disable 01: Write Enable 10: Read Enable 11: Read / Write Enable

Offset Address: 63h (D0F7)

Page- F ROM, Memory Hole and SMM Cycle Decoding **Default Value: 00h**

Bit	Attribute	Default	Description	Mnemonic
7:6	—	0	**Reserved**	
5:4	RW	0	**F0000-FFFFFh** 00: Read / Write Disable 01: Write Enable 10: Read Enable 11: Read / Write Enable	
3:2	RW	0	**Memory Hole** 00 - None 01 - 512K - 640K 10 - 15M - 16M (1M) 11 - 14M - 16M (2M)	
1	RW	0	**Disable Data Access on SMRAM (Page A, B) in SM mode** 0: In SM mode, page A,B CPU **Data** R/W cycles are forwarded to NB memory controller. 1: In SM mode, page A,B CPU **Data** R/W cycles are forwarded to PCI bus (SMRAM page A,B **Code** R/W cycles are always forwarded to memory controller).	**RABKDOFF**
0	RW	0	**Enable Page A, B DRAM Access In Normal Mode** 0: Page A, B CPU R/W cycles could be forwarded to memory controller or PCI bus depends on the setting of RABKDOFF (bit[1]) and the CPU operating mode (Normal or SM mode) as well as the type (Code or Data) of the CPU cycle.. 1: Page A, B CPU R/W cycles (Code and Data) are always (in either Normal or SM mode) forwarded to NB memory controller. Check the following table for details.	**RRWABK**

Offset Address: 64h (D0F7)
Page-E ROM Shadow Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	0	**EC000-DFFFFh** 00: Read / Write Disable 01: Write Enable 10: Read Enable 11: Read / Write Enable
5:4	RW	0	**E8000-DBFFFh** 00: Read / Write Disable 01: Write Enable 10: Read Enable 11: Read / Write Enable
3:2	RW	0	**E4000-D7FFFh** 00: Read / Write Disable 01: Write Enable 10: Read Enable 11: Read / Write Enable
1:0	RW	0	**E0000-D3FFFh** 00: Read / Write Disable 01: Write Enable 10: Read Enable 11: Read / Write Enable

RABKDOFF (Rx63[1])	RRWABK (Rx63[0])	CPU MODE	Target of CODE Access Cycle	Target of DATA Access Cycle
x	0	Normal	PCI	PCI
0	0	SMM	DRAM	DRAM
1	0	SMM	DRAM	PCI
x	1	Normal / SMM	DRAM	DRAM

Host-PCI Bridge Control (70-7Fh)

Offset Address: 70h (D0F7)
PCI Buffer Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**CPU to PCI Post-Write (SB/NB)** 0: Disable 1: Enable
6	—	0	**Reserved**
5:4	RW	0	**PCI Master to DRAM Prefetch Control** x0: Always prefetch x1: Prefetch disabled
3:2	—	0	**Reserved**
1	RW	0	**Delayed Transaction** 0: Disable 1: Enable
0	—	0	**Reserved**

Offset Address: 71h (D0F7)
CPU to PCI Flow Control I **Default Value: 48h**

Bit	Attribute	Default	Description
7	RW1C	—	**Retry Status** 0: No retry occurred 1: Retry occurred (write 1 to clear)
6	RW	1	**Action When Retry Timeout** 0: No action taken except recoding status 1: Flush buffer (write) or return FFFFFFFFh (read)
5:4	RW	0	**Retry Count and Retry Back off** 00: Retry up to 2 times, back off CPU 01: Retry up to16 times, back off CPU 10: Retry up to 4 times, back off CPU 11: Retry up to 64 times, back off CPU
3	RW	1	**PCI Burst Enable** 0: Disable 1: Enable
2	—	0	**Reserved**
1	RW	0	**Compatible TYPE#1 Configuration Cycle** 0: Disable (Fixed AD31) 1: Enable
0	RW	0	**IDSEL for NB and SB** 0: AD11(NB), AD12 (SB) 1: AD30 (NB), AD31(SB)

Offset Address: 73h (D0F7)
PCI Master Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	—	0	**Reserved**
6	RW	0	**PCI Master 1-Wait-State Write** 0: Zero wait state 1: One wait state
5	RW	0	**PCI Master 1-Wait-State Read** 0: Zero wait state 1: One wait state
4	RW	0	**WSC#** 0: Disable 1: Enable
3:1	—	0	**Reserved**
0	RW	0	**PCI Master Broken Timer Enable** 0: Disabled 1: Enabled, PCI Controller will reenter arbitration state if FRAME# is not asserted 16 PCICLKs after bus is granted.

Offset Address: 75h (D0F7)
PCI Arbitration **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Arbitration Mode** 0: REQ-based (arbitrate when REQ# is de-asserted) 1: Frame-based (arbitrate when FRAME# is asserted)
6:4	RW	0	**CPU Latency MLT2, MLT1, MLT0**
3	—	0	**Reserved**
2:0	RW	000	**PCI Master Bus Time-out** 000 - Disable 001 – 1 x16 PCLK 010 – 2x16 PCLK 011 – 3 x16 PCLK … 111 – 7 x16 PCLK

Offset Address: 76h (D0F7)
PCI Arbitration **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Port 22 IO Cycle Control (SB)** 0: CPU port 22 IO cycles are forwarded to the PCI bus 1: CPU port 22 IO cycles are processed internally
6	—	0	**Reserved**
5:4	RW	00	**Master / CPU Priority Rotation Policy** 00 - Disable 01 - Grant to CPU after every PCI master grant 10 - Grant to CPU after every 2 PCI master grants 11 - Grant to CPU after every 3 PCI master grants
3:2	RW	00	**REQx# to RQ4 Mapping Scheme** 00 - REQ4# as RQ4 01 - REQ0# as RQ4 10 - REQ1# as RQ4 11 - REQ2# as RQ4
1	—	0	**Reserved**
0	RW	0	**Enable RQ4 as the High Priority Master** 0: Disable 1: Enable

GART Operation (80-B3h)

Offset Address: 84h (D0F7)

Graphic Aperture Size **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	000h	**Graphics Aperture Size** **AGP20 mode:** **Bit[7:0]** **Aperture Size** 00111111 4M 00111110 8M 00111100 16M 00111000 32M 00110000 64M 00100000 128M 00000000 256M When GART is enabled, Rx77[1] of the South Bridge is set to 1; if AGP20 mode is enabled, Rx77[2] of the South Bridge is set to 0.

Offset Address: 88h (D0F7)

Graphic Aperture Translation Look-Aside Table Base Register **Default Value: 00h**

Bit	Attribute	Default	Description
7:2	—	0	**Reserved**
1	RW	0	**GART Window Access** 0: Disable 1: Enable
0	—	0	**Reserved**

Offset Address: 95-94h (D0F7)

AGP30 Graphic Aperture Size **Default Value: 0000h**

Bit	Attribute	Default	Description
15:12	—	0	**Reserved**
11:0	RW	000h	**Graphics Aperture Size** **AGP30 mode:** **Bit[11:0]** **Aperture Size** 111100111111 4M 111100111110 8M 111100111100 16M 111100111000 32M 111100110000 64M 111100100000 128M 111100000000 256M 111000000000 512M 110000000000 1 G 100000000000 2 G ← maximum supported size 000000000000 4 G When GART is enabled, Rx77[1] of the South Bridge is set to 1; if AGP30 mode is enabled, Rx77[2] of the South Bridge is set to 1.

Offset Address: B0h (D0F7)

V-Link CKG Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00	**Rising-Time Control for V-Link (R-Port)**
5:4	RW	00	**Falling-Time Control for V-Link (R-Port)**
3:2	RW	00	**Rising-Time Control for V-Link (S-Port)**
1:0	RW	00	**Falling-Time Control for V-Link (S-Port)**

Offset Address: B1h (D0F7)
V- Link CKG Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	—	**Reserved**
3:2	RW	00	**Rising-Time Control for V-Link (D-Port)**
1:0	RW	00	**Falling-Time Control for V-Link (D-Port)**

Offset Address: B3h (D0F7)
V-Link Auto Compensation Transmation Resistor Status **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**P resistor checking flag for the termination Resistor in the NB.** 0: abnormal condition occurred. 1: normal operation.
6	RO	0	**N resistor checking flag for the termination Resistor in the NB.** 0: abnormal condition occurred. 1: normal operation.
5	RO	0	**P Pull down driving checking flag for the termination Resistor in the NB.** 0: abnormal condition occurred. 1: normal operation.
4	RO	0	**N Pull down driving checking flag for NB.** 0: abnormal condition occurred. 1: normal operation.
3	—	0	**Reserved**
2:0	RO	0	**NB V-Link Autocomp termination Resistor Value of the NB.** 000: largest Resistor 111: smallest Resistor

V-Link North Bridge Driving Control (B4-B7h)

Offset Address: B4h (D0F7)
NB V-Link Compensation Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	**V-Link Auto-compensation PMOS Output Value**
4	RW	0	**VKCOMP Reference Voltage for VLINK at 4X Mode** 0: VREF4X = 0.75V 1: VREF4X = 0.9V
3:1	RO	0	**V-Link Auto-compensation NMOS Output Value**
0	RO	0	**Compensation Option** 0: Use Auto Compensation (value is kept in bits 7:5) 1: Use Manual setting (use the values of RxB5 and RxB6)

Offset Address: B5h (D0F7)
NB V-Link Driving Control - Strobe **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RW	0	**Manual Setting - NB V-Link Strobe Pullup (PMOS)**
4	—	0	**Reserved**
3:1	RW	0	**Manual Setting - NB V-Link Strobe Pulldown (NMOS)**
0	—	0	**Reserved**

Offset Address: B6h (D0F7)
NB V-Link Driving Control - Data **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RW	0	**Manual Setting - NB V-Link Data Pullup (PMOS)**
4	—	0	**Reserved**
3:1	RW	0	**Manual Setting - NB V-Link Data Pulldown (NMOS)**
0	—	0	**Reserved**

Offset Address: B7h (D0F7)
NB V-Link Receiving Strobe Delay **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	—	0	**V-Link manual termination resistor value** 000: Largest Resister. 111: Smallest Resister
4:3	—	00	**Reserved**
2:0	RW	000	**NB V-Link Receiving Strobe Delay** 000: No delay 001: Delay 0.3 ns 010: Delay 0.2 ns 101: Delay 0.1 ns 110: Delay more than 0.2 ns

V-Link South Bridge Driving Control (B8-BBh)

Offset Address: B8h (D0F7)
SB V-Link Compensation Control **Default Value: 00h**

For 8X Capable South Bridges (VT8237R Plus):

Bit	Attribute	Default	Description
7:5	RO	0	**V-Link Auto Compensation PMOS Output Value**
4:1	—	0	**Reserved**
0	RW	0	**Compensation Selection** 0: Use Auto Compensation (value is kept in bits 7:5) 1: Use Manual setting (use the values of RxB9 - RxBB)

For 4X-Only South Bridges (VT8233):

Bit	Attribute	Default	Description
7:6	RO	0	**V-Link Auto Compensation Output Value**
5	RW	0	**Pull Up Compensation Selection** 0: Auto Compensation (value is kept in bits 7:6) 1: Manual Setting (use the value defined in bits 3:2)
4	RW	0	**Pull Down Compensation Selection** 0: Auto Compensation (value is kept in bits 7:6) 1: Manual Setting (use the values defined in bits 1:0)
3:2	RW	0	**Manual Setting - Pull Up Compensation Value**
1:0	RW	0	**Manual Setting - Pull Down Compensation Value**

Offset Address: B9h (D0F7)
SB V-Link Driving Control – Strobe **Default Value: 00h**

For 8X Capable South Bridges (VT8237R Plus):

Bit	Attribute	Default	Description
7:5	RW	0	**Manual Setting - SB V-Link Strobe Pullup (PMOS)**
4	—	0	**Reserved**
3:1	RW	0	**Manual Setting - SB V-Link Strobe Pulldown (NMOS)**
0	—	0	**Reserved**

For 4X-Only South Bridges (VT8233):

Bit	Attribute	Default	Description
7:6	RW	0	**Manual Setting - SB V-Link Strobe Pullup**
5:4	RW	0	**Manual Setting - SB V-Link Strobe Pulldown**
3:1	RO	—	**Reserved**
0	RW	0	**V-Link Slew Rate Control** 0: Disable 1: Enable

DRAM Above 4G Support (E4-EFh)

Offset Address: E4h (D0F7)

Low Top Address - Low **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Low Top Address – A[23:20]**
3:0	RW	0	**DRAM Granularity** (Powell) **RMEMUNIT** / **Total DRAM less than** / **Granularity** 0 – 4G – 16M 1 – 8G – 32M 2 – 16G – 64M 3 – 32G – 128M 4 – 64G – 256M

Offset Address: E5h (D0F7)

Low Top Address - High **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Low Top Address – A[31:24]**

Offset Address: E6h (D0F7)

SMM and APIC Decoding **Default Value: 01h**

Bit	Attribute	Default	Description
7:6	—	0	**Reserved**
5	RW	0	**APIC Lowest Interrupt Arbitration** 0: Disable 1: Enable
4	RW	0	**IO APIC Decoding** 0: Cycles accessing FECx_xxxx are passed to PCI1 1: Cycles accessing FEC7_FFFF - FEC0_0000 are passed to PCI1; cycles accessing FECF_FFFF - FEC8_0000 are passed to PCI2.
3	RW	0	**MSI Support (Processor Message Enable)** 0: Cycles accessing FEEx_xxxx from masters are passed to PCI1 (PCIC will not claim) 1: Cycles accessing FEEx_xxxx from masters are passed to the Host side for snooping
2	RW	0	**Top SMM Enable** 0: Disable 1: Enable TSMMA[31:20] = {LOWTOPA[31:24],4'h0} – {FBSZ[2:0],1'b0}; OSLOWTOPA[31:20] = TSMMA[31:20] – RTSMMEN
1	—	0	**High SMM**
0	RW	1	**Compatible SMM Enable** 0: Disable 1: Enable

Device 1 Function 0 (D1F0): PCI to PCI Bridge

This configuration is provided to facilitate the configuration of the second PCI bus (AGP) without requiring new enumeration code. This function is represented as device number 1, function 0.

Header Registers (0-3Fh)

Offset Address	Attribute	Default	Description
1–0h	RO	1106h	**Vendor ID**
3–2h	RO	B198h	**Device ID**

Offset Address: 5-4h (D1F0)

PCI Command **Default Value: 0007h**

Bit	Attribute	Default	Description
15:10	—	0	**Reserved**
9	RO	0	**Fast Back-to-Back Cycle Enable** Hardwired to 0. (Disable)
8	RO	0	**SERR# Enable** Hardwired to 0 (Disable)
7	RO	0	**Address / Data Stepping** Hardwired to 0 (Not supported)
6	RW	0	**Parity Checking** 0: Ignore parity errors 1: Perform parity check and take normal action on detected parity errors
5	RO	0	**VGA Palette Snooping** Hardwired to 0 (Not supported).
4	RO	0	**Memory Write and Invalidate** Hardwired to 0 (Not supported)
3	RO	0	**Respond To Special Cycle** Hardwired to 0 (Does not monitor special cycles)
2	RW	1	**Bus Master** 0: Never behaves as a bus master 1: Enable to operate as a bus master on the secondary interface
1	RW	1	**Memory Space Access** 0: Does not respond to memory space access 1: Responds to memory space access
0	RW	1	**I/O Space Access** 0: Does not respond to I/O space access 1: Responds to I/O space access

Offset Address: 7-6h (D1F0)

PCI Status **Default Value: 0230h**

Bit	Attribute	Default	Description
15	RO	0	**Parity Error Detected** Reserved
14	RO	0	**SERR# Detected** Reserved
13	RO	0	**Set When Terminated with Master-Abort, Except Special Cycle** 0: No abort received 1: Transaction aborted by the master
12	RO	0	**Set When Received a Target-Abort** 0: No abort received 1: Transaction aborted by the target
11	RO	0	**Set When Signaled a Target-Abort** NB never signals Target Abort
10-9	RO	01	**DEVSEL# Timing** 00: Fast 01: Medium (default) 10: Slow 11: Reserved
8	RO	0	**Set When Set or Observed SERR# and Parity Error** Reserved
7	RO	0	**Capable of Accepting Fast Back-to-Back as a Target** Reserved
6	RO	0	**User Definable Features** Reserved
5	RO	1	**66 MHz Capable**
4	RO	1	**Support New Capability List**
3:0	—	0	**Reserved**

Offset Address: 8h (D1F0)

Revision ID **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	00h	**Revision ID**

Offset Address: 0B-9h (D1F0)

Class Code **Default Value: 060400h**

Bit	Attribute	Default	Description
23:0	RO	060400h	**Class Code**

Offset Address: 0Eh (D1F0)

Header Type **Default Value: 01h**

Bit	Attribute	Default	Description
7:0	RO	01h	**Header Type** It adheres to the PCI-PCI Bridge Configuration

Offset Address: 0Fh (D1F0)

Built In Self Test (BIST) **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**BIST Support**

Offset Address: 13-10h (D1F0)
Graphic Aperture Base Configuration **Default Value: 0000 0008h**

Bit	Attribute	Default	Description
31:22	RW	0	**Programmable Base Address** The aperture base address bit acts as if hardwired to 0 if the corresponding GTSZ1[11:0] (Rx94[11:0]) bit is 0. If RAGPCAP1 (RxBF[0]) is set to 0, this register is forced to zero. Note: this range is defined as prefetchable
21:4	—	0	**Reserved** (Hardwire to 0)
3	RO	1	**Prefetchable**
2:1	RO	0	**Type** Indicates that the address range is in the 32-bit address space
0	RO	0	**Memory Space**

Offset Address: 18h (D1F0)
Primary Bus Number **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	00	**Primary Bus Number** Primary Bus Number is fixed at 0 internally; this register setting is ignored.

Offset Address: 19h (D1F0)
Secondary Bus Number **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	00	**Secondary Bus Number** Secondary Bus Number is used when converting Type#1 configuration cycles to TYPE#0 configuration cycles.

Offset Address: 1Ah (D1F0)
Subordinate Bus Number **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	00	**Subordinate Bus Number** PCI2 uses Subordinate Bus Number to decide if Type#1 command passing is allowed

Offset Address: 1Ch (D1F0)
IO Base **Default Value: F0h**

Bit	Attribute	Default	Description
7:4	RW	1111	**IO Address Bit[15:12] – inclusive**
3:0	RO	0	**IO Addressing Capability**

Offset Address: 1Dh (D1F0)
IO Limit **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**IO Address Bit[15:12] – inclusive**
3:0	RO	0	**IO Addressing Capability**

Offset Address: 1F-1Eh (D1F0)
Secondary Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15:8	—	0	**Reserved**
7:4	RW	0	**Secondary Status** If R2NDSTAT = 0 (Rx44[4]) : Read this register has 0 returned If R2NDSTAT = 1: Read this register has contents of Rx7-Rx6 (PCI Status Register) returned
3:0	—	0	**Reserved**

Offset Address: 21-20h (D1F0)
Memory Base **Default Value: FFF0h**

Bit	Attribute	Default	Description
15:4	RW	0FFFh	**Memory Address Bit [31:20]** – inclusive (address [19:0] is not decoded)
3:0	—	0	**Reserved**

Offset Address: 23-22h (D1F0)
Memory Limit **Default Value: 0000h**

Bit	Attribute	Default	Description
15:4	RW	0	**Memory Address Bit [31:20]** – inclusive (address [19:0] is not decoded)
3:0	—	0	**Reserved**

Offset Address: 25-24h (D1F0)
Prefetchable Memory Base **Default Value: FFF0h**

Bit	Attribute	Default	Description
15:4	RW	0FFFh	**Memory Address Bit [31:20]** – inclusive
3:0	—	0	**Reserved**

Offset Address: 27-26h (D1F0)
Prefetchable Memory Limit **Default Value: 0000h**

Bit	Attribute	Default	Description
15:4	RW	0	**Memory Address Bit [31:20]** – inclusive
3:0	—	0	**Reserved**

Offset Address: 34h (D1F0)
Capability Pointer **Default Value: 70h**

Bit	Attribute	Default	Description
7:0	RO	70h	**AGP Capability List Pointer**

Offset Address: 3F-3Eh (D1F0)
PCI-to-PCI Bridge Control **Default Value: 0000h**

Bit	Attribute	Default	Description	Mnemonic
15:14	—	0	**Reserved**	
3	RW	0	**Enable VGA Compatible I/O and Memory Address Range** 0: Do not forward VGA compatible memory and I/O cycles to PCI2 1: Forward VGA compatible memory and I/O cycles to PCI2	**RVGA2**
2	RW	0	**Block ISA I/O Cycles** 0: Forward all I/O cycles with address in the range defined by the I/O base and I/O Limit to PCI2 1: Do not forward ISA I/O cycles with address in the top 768 bytes of each 1Kbyte block	**RISA2**
1:0	RO	0	**Reserved**	

If RVGA2 is set to 1, the following VGA compatible I/O and memory access will be forwarded to PCI2
- Memory: in the range of A0000h to BFFFFh
- I/O: where A[9:0] in the ranges of 3BBh-3B0h and 3DFh-3C0h; A[15:10] are not decoded

If RISA2 is set to 1, NB will not forward cycles to AGP if A[9:0] is in the range of 3ffh-100h even if address are within the range defined by the RIOBS and RIOLM.

Second PCI Bus Control (40-6Fh)

Offset Address: 40h (D1F0)

CPU to PCI Flow Control I **Default Value: 00h**

Bit	Attribute	Default	Description	Mnemonic
7	RW	0	**CPU to PCI Post-Write** 0: Disable 1: Enable C2P posted cycle could be delayed by PCI master cycles (i.e. PCI master access is allowed even if C2P buffer is not flushed).	
6	RW	0	**CPU to PCI One Wait State Burst Write** 0: Disable 1: Enable	
5:4	RW	0	**Read Prefetch Control** x0: Always prefetch x1: Disable prefetch	
3	—	0	**Reserved**	
2	RW	0	**MDA Resource Location** (Note: the setting on this register bit overwrites the settings on the IO/Memory's Base and Limit of the other devices) 0: AGP/PCI2; forward MDA access cycles to AGP/PCI2 1: PCI1; forward MDA access cycles to PCI1 MDA Resources include: **Memory**: B0000h-B7FFFFh, **I/O**: 3B4h, 3B5h, 3B8h, 3B9h, 3BAh, 3BFh. Check the following table for the function of register bits, RVGA2 and RMDA.	**RMDA**
1	RW	0	**PCI2 Master Read Caching** 0: Disable 1: Enable	
0	RW	0	**PCI2 Delay Transaction** 0: Disable 1: Enable	

Address	RVGA2 Rx3E[3]	RMDA Rx40[2]	Cycle Destination
Memory: AFFFFh-A0000h	0	-	PCI1
	1	-	PCI2
Memory: MDA (BFFFFh-B0000h)	1	0	PCI2
	1	1	PCI1
	0	-	PCI1
IO:[3BBh,3B0h] except MDA	0	-	PCI1
	1	-	PCI2
IO: MDA	1	0	PCI2
	0	-	PCI1
	1	1	PCI1
IO: [3DFh,3C0h]	1	-	PCI2
	0	-	PCI1

Notes:

1. If RISA2 is set to 1, NB will not forward cycles to AGP if A[9:0] is in the range of 3ffh-100h even if address are within the range defined by the RIOBS and RIOLM.
2. If both RVGA2 and RMDA are set to 1, VGA is on PCI2 and MDA is put on PCI1. VGA palette snooping is not supported in PCI2.

Offset Address: 41h (D1F0)
CPU to PCI Flow Control II **Default Value: 08h**

Bit	Attribute	Default	Description
7	RO	0	**Retry Status** 0: No retry occurred 1: Retry occurred (write 1 to clear)
6	RW	0	**Action When Retry Timeout** 0: No action taken except recording status 1: Flush buffer (write) or return FFFFFFFFh (read)
5:4	RW	0	**Retry Count** 00: Retry 2 times, back off CPU 01: Retry 4 times, back off CPU 10: Retry 16 times, back off CPU 11: Retry 64 times, back off CPU
3	RW	1	**C2P Burst Timeout Enable** 0: Disable 1: Enable
2	—	0	**Reserved**
1	RW	0	**Invalidate PCI2 Read Buffer Data (read caching data) when C2P Cycle Arrived** 0: Disable 1: Enable
0	RW	0	**Read Burst on PCI2** 0: Disable 1: Enable

Offset Address: 42h (D1F0)
PCI Master Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved** (must be set to 1)
6	RW	0	**PCI Master 1-Wait State Write** 0: Disable 1: Enable
5:	RW	0	**PCI Master 1-Wait State Read** 0: Disable 1: Enable
4	RW	0	**Break Consecutive PCI Master Access** 0: Disable 1: Enable
3	—	0	**Reserved**
2	RW	0	**Claim the IO R/W and Memory Read Cycles** 0: Disable 1: Enable
1	RW	0	**Claim the Local APIC FEEx_xxxx Cycles** 0: Disable 1: Enable
0	—	0	**Reserved**

Offset Address: 43h (D1F0)
PCI2 Timer **Default Value: 22h**

Bit	Attribute	Default	Description
7:4	RW	2h	**Host to PCI2 Time Slot** 0: Disable (no timer) 1: 16 GCLKs 2: 32 GCLKs … 0Fh: 128GCLKs
3:0	RW	2h	**PCI2 Master Time Slot** 0: Disable (no timer) 1: 16 GCLKs 2: 32 GCLKs … 0Fh: 128 GCLKs

Offset Address: 44h (D1F0)
PCI2 Miscellaneous Control **Default Value: 20h**

Bit	Attribute	Default	Description	Mnemonic
7:6	—	0	**Reserved**	
5	RW	1	**Power Management Capability Support** 0: Read Rx34 as 00 1: Read Rx34 as 80h	
4	RW	0	**Rx1F-Rx1E Read Returned Value** 0: Rx1F-Rx1E always read as 00 1: Rx1F-Rx1E read will receive the values in Rx07-Rx06	**R2NDSTAT**
3:0	—	0	**Reserved**	

Offset Address: 45h (D1F0)
Fast Write Control **Default Value: 72h**

Bit	Attribute	Default	Description
7	RW	0	**Force Fast Write Cycle QW Aligned** (if Rx45[6] = 0) 0: Disable (DW aligned) 1: Enable (force QW aligned)
6	RW	1	**Merge Multiple Host Transactions into A Fast Write Transaction (Burst)** 0: Disable 1: Enable (QW aligned)
5:3	—	110	**Reserved**
2	RW	0	**Fast Write Burst Length Limit: 4T** 0: Disable 1: Enable
1	RW	1	**Fast Write: Fast Back to Back** 0: Disable 1: Enable
0	RW	0	**Fast Write Initial Block: 1-Wait State** 0: Disable 1: Enable

Offset Address: 46h (D1F0)
PCI-to-PCI Bridge Device ID (Low Byte) **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Device ID for P2P Bridge Low Byte (ID[7:0])**

Offset Address: 47h (D1F0)
PCI-to-PCI Bridge Device ID (High Byte) **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Device ID for P2P Bridge High Byte (ID[15:8])**

Power Management Capability (70-77h)

Offset Address: 70h (D1F0)
Capability ID **Default Value: 01h**

Bit	Attribute	Default	Description
7:0	RO	01	**Capability ID**

Offset Address: 71h (D1F0)
Next Pointer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	00	**Next Pointer** If RAGPCAP1 (RxBF[0]) = 0, Next Pointer is 00; If RAGPCAP1 (RxBF[0]) = 1, Next Pointer is 80h

Offset Address: 72h (D1F0)
Power Management Capabilities **Default Value: 02h**

Bit	Attribute	Default	Description
7:0	RO	2h	**Power Management Capabilities**

Offset Address: 73h (D1F0)
Power Management Capabilities **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	00	**Power Management Capabilities**

Offset Address: 74h (D1F0)
Power Management Control / Status **Default Value: 00h**

Bit	Attribute	Default	Description
7:2	—	00	**Reserved**
1:0	RW	—	**Power State** 00: D0 11: D3 hot

Offset Address: 75h (D1F0)
Power Management Status **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	00	**Power Management Status**

Offset Address: 76h (D1F0)
PCI to PCI Bridge Support Extensions **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	00	**PCI to PCI Bridge Support Extensions**

Offset Address: 77h (D1F0)
Power Management Data **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	00	**Power Management Data**

AGP 3.0 Configuration (80-A3h)

New AGP Capability Header

The original AGP capability is stored in Device 0, Function0. For adapting the new AGP capability header for multiple AGP devices, the AGP capability header is moved to Device1, Function0 (D1F0). The related registers are also moved including RX10~RX13, the AGP Aperture base address, and RX40~RX43, the hardware settings for the AGP pads. To be backward compatible, the default of AGP capability location will remain the same, in D0F0, as it was before. However, if D1F0 RXBF[0], RAGPCAP1, is set to 1, the AGP settings will be controlled by D1F0. See the following table for the function of RXBF[0].

	RAGPCAP1=0	RAGPCAP1=1
D0F0 Rx13~Rx10	GTBS[31:22]	00000000
D0F0 Rx34	->Rx80->Rx50->NULL	->Rx50->NULL
D1F0 Rx13~Rx10	00000000	GTBS[31:22]
D1F0 Rx34	->Rx70->NULL	->Rx70->Rx80->NULL
AGP Pads Hardware Setting	D0F0 Rx40~Rx43	D1F0 RxB0~RxB3

Rx80 is the AGP pointer, however, it could be associated with AGP2.0 header or AGP 3.0 header depends on the setting on system mode selection register bit, RAGP30, from strapping. For all of the read-only registers (e.g. AGP status registers, major/minor ID, Capability ID), the default settings could be over written through the register bit RSTATW (Rx4D[0]) in device0, function0 for the original AGP capability header, or through the register bit RSTATW1 (RxBD[0]) in device1, function 0 for the new AGP capability header. And for software backward compatible, there are RAGPCAP30 and RAGP30 to control certain bits in Rx80-Rx8B, which are reserved in AGP20 mode.

Depends on the settings on RAGP30CAP and RAGP30, the controller could be connected to the registers described in either AGP30 or AGP20 header; however, to support AGP fanout mode in VPX mode, the controller must be operated at a different mode than what has been described in the AGP header; register D0F0 Rx4D[1], RAGPHW, and D1F0 RxBD[1], RAGPHW1, are used to support this mode.

Offset Address: CAPPTR (D1F0 83-80h)

AGP Identifier **Default Value: 0035 000Eh**

Bit	Attribute	Default	Description
31:24	RZ	0	**Always Return 0, write has no effect**
23:20	R-IW	3h	**Major Revision**
19:16	R-IW	5h	**Minor Revision** If RBKMJMN1 (RxBD[3]) is 0: 'b0101 If RBKMJMN1 (RxBD[3]) is 1: 'b0000.
15:8	R-IW	00	**Pointer to Next Item**
7:0	R-IW	0Eh	**Capability ID**

Offset Address: CAPPTR + 04h (D1F0_87-84h)

AGP Status **Default Value: 0700 0A0Bh**

Bit	Attribute	Default	Description	Mnemonic
31:24	R-IW	07	**Max # of AGP Command Requests**	
23-18	RZ-IW	0	**Reserved**	
17	RZ-XW	0	**Isoch Transaction** 0: Does not support Isoch transaction. 1: Support Isoch transaction	**RISOCH1**
16	—	0	**Reserved (for future 64-bit AGP)**	
15:13	RZ-XW	0	**Reserved**	
12:10	RZ-XW	010	**Calibrating Cycle** 000 – 4ms 001 – 16ms 010 – 64ms 011 – 256ms Valid when RAGP30 (bit-3) is 1.	
9	R1-XW	1	**SBA Support** Always on.	
8	RZ-XW	0	**Coherent Support** Not supported	
7	R-XW	0	**64-bit GART Entry** Support 32-bit GART entry only.	
6	R-XW	0	**Host GART Translation** 0: Support host GART translation 1: Do not do host GART translation	
5	R-XW	0	**Over 4GB Support** Not Supported	
4	R-XW	0	**Fast Write Support**	
3	R-XW	0	**AGP 8x Detected** Set by strap pin AGP8XDET# 0: AGP 2.0 Mode 1: AGP 3.0 Mode	**RAGP30**
2:0	R-XW	011 111	**AGP Data Rate** **If RAGP30 (bit-3) is 1,** default is 011: supports 4X and 8X data transfer rate. **If RAGP30 (bit-3) is 0,** default is 111: supports 1X, 2X and 4X data transfer rate.	

Offset Address: CAPPTR + 08h (D1F0_8B-88h)

AGP Command **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RZ-IW	0	**Max # of AGP Command Requests**
23:13	—	0	**Reserved**
12:10	RW	0	**Calibrating Cycle**
9	RW	0	**SBA Enable** Always on.
8	RW	0	**AGP Enable** 0: Disable 1: Enable
7	RW	0	**64-bit GART** Not supported
6	RZ-MW	0	**Reserved**
5	RW	0	**Over 4G Support** Not Supported
4	RW	0	**Fast Write Enable** 0: Disable 1: Enable
3	—	0	**Reserved**
2:0	RW	0	**Data Rate** If RAGP30 (D1F0 Rx87-84[3]) = 1, 001: 4X data transfer rate 010: 8X data transfer rate If RAGP30 (D1F0 Rx87-84[3]) = 0, 001: 1X data transfer rate 010: 2X data transfer rate 100: 4X data transfer rate

Offset Address: CAPPTR + 0Ch (D1F0_8F-8Ch)

AGP Isochronous Status **Default Value: 00000000h**

Isochronous is not supported, therefore, this register is read zero.

Bit	Attribute	Default	Description
31:24	—	0	**Reserved**
23:16	R-IW	0	**Maximum Bandwidth** (in unit of 32 bytes) Used for isochronous transactions.
15:8	R-IW	0	**Maximum Number of Isochronous Transaction in a Single Isochronous Period**
7:6	RZ-IW	0	**Isochronous Payload Sizes Supported** 00: 32,64,128,256 bytes 01: 64,128,256 bytes 10: 128,256 bytes 11: 256 bytes
5:3	R-IW	00	**Maximum Isochronous Data Transfer Latency** (in unit of 1 us)
2	—	0	**Reserved**
1:0	R-WIC	0	**Isochronous Error Code** 00: No error 01: Isoch Request Overflow 1x: Reserved

Offset Address: CAPPTR + 10h (D1F0_93-90h)

AGP Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:10	—	0	**Reserved**
9	RW	0	**Disable Calibration Cycle**
8	RW	0	**Enable AGP Aperture** Set to 1 to enable AGP Aperture. Note: Both RBKGTEN (D0F0 Rx4D[5]) and RAGPCAP1 (RxBF[0]) must be 1 to enable this function.
7	RW	0	**GTLB Enable** When set to 0, GART TLB entries are invalidated. All AGP aperture access needs to fetch the translation table first.
6:0	—	0	**Reserved**

Offset Address: CAPPTR + 14h (D1F0_97-94h)

AGP Aperture Size **Default Value: 0001 0F00h**

Bit	Attribute	Default	Description	Mnemonic
31:28	RW	0	**Aperture Page Size Select** Where n is the value of this register.Only 4KB page size, PAGESZ1=0000h, is supported.	**PAGESZ1[15:12]**
27	—	0	**Reserved**	
26:16	R-IW	01	**Page Size Supported** If NEPG1[N] is 1, which indicates support of page size of (2^(N+12)). Currently only 4KB page size is supported.	**NEPG1[10:0]**
15:12	—	0	**Reserved**	
11:0	RW	0F00h	**Aperture Size** (Default size is 256M) For 0<=n=<5 APSIZE[n]=0 forces Aperture Base Address [22+n] to 0 APSIZE[1]=1 allows Aperture Base Address [22+n] R/W For 8<=n=<11 APSIZE[n]=0 forces Aperture Base Address [22+n-2] to 0	

Table 16. Aperture Size

Aperture Size \ GTSZ1[11:0]	11	10	9	8	7	6	5	4	3	2	1	0
4MB	1	1	1	1	0	0	1	1	1	1	1	1
8MB	1	1	1	1	0	0	1	1	1	1	1	0
16MB	1	1	1	1	0	0	1	1	1	1	0	0
32MB	1	1	1	1	0	0	1	1	1	0	0	0
64M	1	1	1	1	0	0	1	1	0	0	0	0
128M	1	1	1	1	0	0	1	0	0	0	0	0
256M	1	1	1	1	0	0	0	0	0	0	0	0
512M	1	1	1	0	0	0	0	0	0	0	0	0
1G	1	1	0	0	0	0	0	0	0	0	0	0
2G (Maximum Aperture Size)	1	0	0	0	0	0	0	0	0	0	0	0
4G	0	0	0	0	0	0	0	0	0	0	0	0

Offset Address: CAPPTR + 18h (D1F0_9B-98h)
AGP GART Table Pointer **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:12	RW	0	**GART Table Base Address [31:12]**
11:0	—	0	**Reserved**

Offset Address: CAPPTR + 1Ch (D1F0_9F-9Ch)
AGP GART Table Pointer High **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Base Address [63:32]** Since OVER 4G is not supported, OS should write all zeros to this register. This register is ignored.

Offset Address: CAPPTR + 20h (D1F0_A3-A0h)
AGP Isochronous Command **Default Value: 0000 0000h**

Isochronous is not supported, therefore, this register is read zero

Bit	Attribute	Default	Description
31:8	—	0	**Reserved**
7:6	RW	0	**Isochronous Pay Load Size** Default is ISOCH_Y
5:0	—	0	**Reserved**

AGP 4X / AGP 8X Compensation Circuits (B0-B9h)

Offset Address: B0h (D1F0)
AGP PAD Compensation Control / Status **Default Value: 80h**

Bit	Attribute	Default	Description	Mnemonic
7	RW	1	**AGP4X Strobe's Reference Voltage** 0: Strobe signals, GADSTB[1:0]; do not use AGPVREF as input reference voltage. 1: Strobe signals use AGPVREF as input reference voltage. (Note: this bit is valid only when internal signal, RX4EN or RX8EN, is set to 1; otherwise always use AGPVREF as Strobe signals' reference voltage) **RSTBVREF1** **Input Reference Voltage** 1 0.5VPP = 0.5 * 1.5v 0 NADSTB0, NADSTB1	**RSTBVREF1**
6	RW	0	**AGP4X Strobe and GD Pad Driving Strength Control** 0: Driving strength is set to compensation circuit defaults 1: Driving strength is controlled by RxB1[7:0]	
5:3	RO	xxx	**AGP Compensation Circuit N Control Output**	
2:0	RO	xxx	**AGP Compensation Circuit P Control Output**	

Offset Address: B1h (D1F0)
AGP Compensation Driving Strength Control **Default Value: 63h**

Bit	Attribute	Default	Description
7:4	RW	6h	**AGP Output Buffer Driving Strength N Control**
3:0	RW	3h	**AGP Output Buffer Driving Strength P Control**

Offset Address: B2h (D1F0)
AGP Pad Driving and Delay Control **Default Value: 08h**

Bit	Attribute	Default	Description	Mnemonic
7	RW	0	**GD / GADSTBx / GC#BE and GSBSTBx / GSBA# Pad Control** **GSBSTBx, GSBA GD, GC#BE, GADSTBx** **0** No Cap No Cap **1** Cap Cap	
6:5	RW	0	**GD, GC#BE Receive Strobe Delay** 00: Delay by –150 ps 01: No delay 10: Delay by 150 ps 11: Delay by 300 ps	
4	RW	0	**GD[31:16] Output Staggered Delay (1 ns)** 0: No delay 1: GD[31:16] is delayed by 1 ns	**RGDLY1**
3	RW	1	**GD, GADSTBx Slew Rate Control** 0: Disable 1: Enable	
2	RW	0	**GSBA Receive Strobe Delay** 0: No Delay 1: Delay by 150 ps	
1:0	RW	0	**GADSTBx Output Delay** 00: No delay 01: Delay by 150 ps 10: Delay by 300 ps 11: Delay by 450 ps Note: GADSTB1 and GADSTB1# will be delayed 1 ns more if RGDLY1 (bit-4) is set to 1.	

Offset Address: B3h (D1F0)
AGP Strobe Drive Strength **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**AGP Strobe Output Buffer Driving Strength N Control**
3:0	RW	0	**AGP Strobe Output Buffer Driving Strength P Control**

Offset Address: B4h (D1F0)
AGP GSBA Pads Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	—	0	**Reserved**
2:0	RW	0	**GSBA Pads Control**

Offset Address: B5h (D1F0)
AGP Back Door Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:2	—	0	**Reserved**
1	RW	0	**RAGP30 Software Setup** RAGP30 (Rx84[3]) is over-written by the value of this register bit**.** (i.e. Read Rx84[3] will retrieve the value of RxB5[1]) Bit-0 must be set to 1 to enable this feature.
0	RW	0	**RAGP30 Software Control** 0: Disable 1: Enable, allows RAGP30 to be software programmable

Miscellaneous Control (BA-BFh)

Offset Address: BAh (D1F0)
AGP Hardware Support I – VPX Mode **Default Value: 1Fh**

Bit	Attribute	Default	Description
7:0	RW	1Fh	**AGP Request Queue Size** This register is effective if RxBD[1] is set to 1.

Offset Address: BBh (D1F0)

AGP Hardware Support II – VPX Mode **Default Value: C4h**

This register is used to re-configure the AGP controller. To reconfigure the AGP controller, RxBD[1] must be set to 1.

Bit	Attribute	Default	Description
7	RW	1	**AGP SBA Mode Enable** 0: Disable 1: Enable
6	RW	1	**AGP Enable** 0: Disable 1: Enable
5	—	0	**Reserved**
4	RW	0	**Fast Write Enable** 0: Disable 1: Enable
3	RW	0	**AGP8X Mode Enable** 0: Disable 1: Enable
2	RW	1	**AGP4X Mode Enable** 0: Disable 1: Enable
1	RW	0	**AGP2X Mode Enable** 0: Disable 1: Enable
0	RW	0	**AGP1X Mode Enable** 0: Disable 1: Enable

Offset Address: BDh (D1F0)

AGP Capability Header Control **Default Value: 04h**

Bit	Attribute	Default	Description	Mnemonic
7:5	—	0	**Reserved**	
4	RW	0	**Enable Rx90[31:10] and Rx90[6:0] RW Attribute** 0: Disable, read only 1: Enable	
3	RW	0	**AGP Major / Minor number Control** 0: Major/Minor = 35h 1: Major/Minor = 20h	**RBKMJMN1**
2	RW	1	**Select Rx80 as the AGP20 or AGP30 Header** 0: Rx80 is used as the AGP20 capability header even if the chip is powered up in a AGP30 mode 1: Rx80 is used as the AGP30 capability header when the chip is powered up in AGP30 mode	
1	RW	0	**Enable AGP Hardware Registers in RxBA ~ RxBB** 0: AGP hardware is configured by register values defined in the AGP header (either 3.0 or 2.0) 1: AGP hardware is configured by register values defined in RxBA ~ RxBB (used in VPX mode)	
0	RW	0	**Enable AGP Header Status Register Write** 0: Disable (Status registers in the AGP header cannot be modified). 1: Enable (Status registers in the AGP header can be modified).	

Offset Address: BFh (D1F0)

Miscellaneous **Default Value: 00h**

Bit	Attribute	Default	Description	Mnemonic
7:1	—	0	**Reserved**	
0	RW	0	**AGP Capability Header** 0: AGP capability header is in device0 function0; D1F0 Rx80 ~ RxA0 will be hidden. 1: AGP capability header is as described in D1F0 Rx80 ~ RxA0.	**RAGPCAP1**

RAGPCAP1's Effects on The Other Parts of The Design

	RAGPCAP1 = 0	RAGPCAP1=1
D0F0 Rx13~Rx10	GTBS[31:22]	00000000
D0F0 Rx34	->Rx80->Rx50->NULL	->Rx50->NULL
D1F0 Rx13~Rx10	00000000	GTBS[31:22]
D1F0 Rx34	->Rx70->NULL	->Rx70->Rx80->NULL
AGP Pad Hardware Setting	D0F0 Rx40~Rx43	D1F0 RxB0~RxB3

ELECTRICAL SPECIFICATIONS

Power Characteristics

DDR

T_C = 0-85^{O}C, V_{RAIL} = V_{CC} +/- 5%, V_{CORE} = 1.5V +/- 5%, GND=0V

Condition: DDR400 and Power Management On

Symbol	Parameter	Typ	Max	Unit
I_{CC33}	Power Supply Current - Internal Logic & I/O Interface	98	100	mA
I_{CCSUS}	Power Supply Current - Suspend Power	1.95	2	mA
I_{CCTT}	Power Supply Current - CPU Interface Termination	80	106	mA
I_{CCCORE}	Power Supply Current – Core Logic	867	1016	mA
I_{CCMCK}	Power Supply Current - DRAM Clock Logic	747	860	mA
I_{CCQ}	Power Supply Current - AGP 1.5V Power	17	19	mA
I_{CCVL}	Power Supply Current – Vlink I/O Power	10	11	mA
P_D	Power Dissipation	2.6	3.6	W

DDR2

$_C$ = 0-85^{O}C, V_{RAIL} = V_{CC} +/- 5%, V_{CORE} = 1.5V +/- 5%, GND=0V
Condition: DDR2-533 and Power Management On

Symbol	Parameter	Typ	Max	Unit
I_{CC33}	Power Supply Current - Internal Logic & I/O Interface	109	112	mA
I_{CCSUS}	Power Supply Current - Suspend Power	2	2.1	mA
I_{CCTT}	Power Supply Current - CPU Interface Termination	37	95	mA
I_{CCCORE}	Power Supply Current – Core Logic	796	1104	mA
I_{CCMCK}	Power Supply Current - DRAM Clock Logic	389	526	mA
I_{CCQ}	Power Supply Current - AGP 1.5V Power	17	22	mA
I_{CCVL}	Power Supply Current – Vlink I/O Power	9	12	mA
P_D	Power Dissipation	2.4	3.2	W

Package Thermal Simulation

Heat sink is required for this chip.

Package Specification	Simulation Result	
	Thermal Characterization (unit: ºC/W)	
	Vflow (m/s)	θja
HSBGA 37.5 x 37.5 mm	0.00	13.51
	1.00	11.61
	2.00	10.56
	4.00	9.57
	θjc	5.56
	θjb	7.74

Vflow (m/s): Velocity of external flow passing by the package

T_j (°C): Junction temperature

T_a (°C): Ambient temperature

T_cx (°C): Temperature on whole top surface equal to ambient temperature

θjc (°C/W): Junction-to-case thermal resistance

θjc = (T_j-T_cx) / Power where Tcase equal to Ta

θja (°C/W): Junction-to-ambient thermal resistance

θja = (T_j-T_a) / Power

θjb (°C/W): Junction-to-board thermal resistance

MECHANICAL SPECIFICATIONS

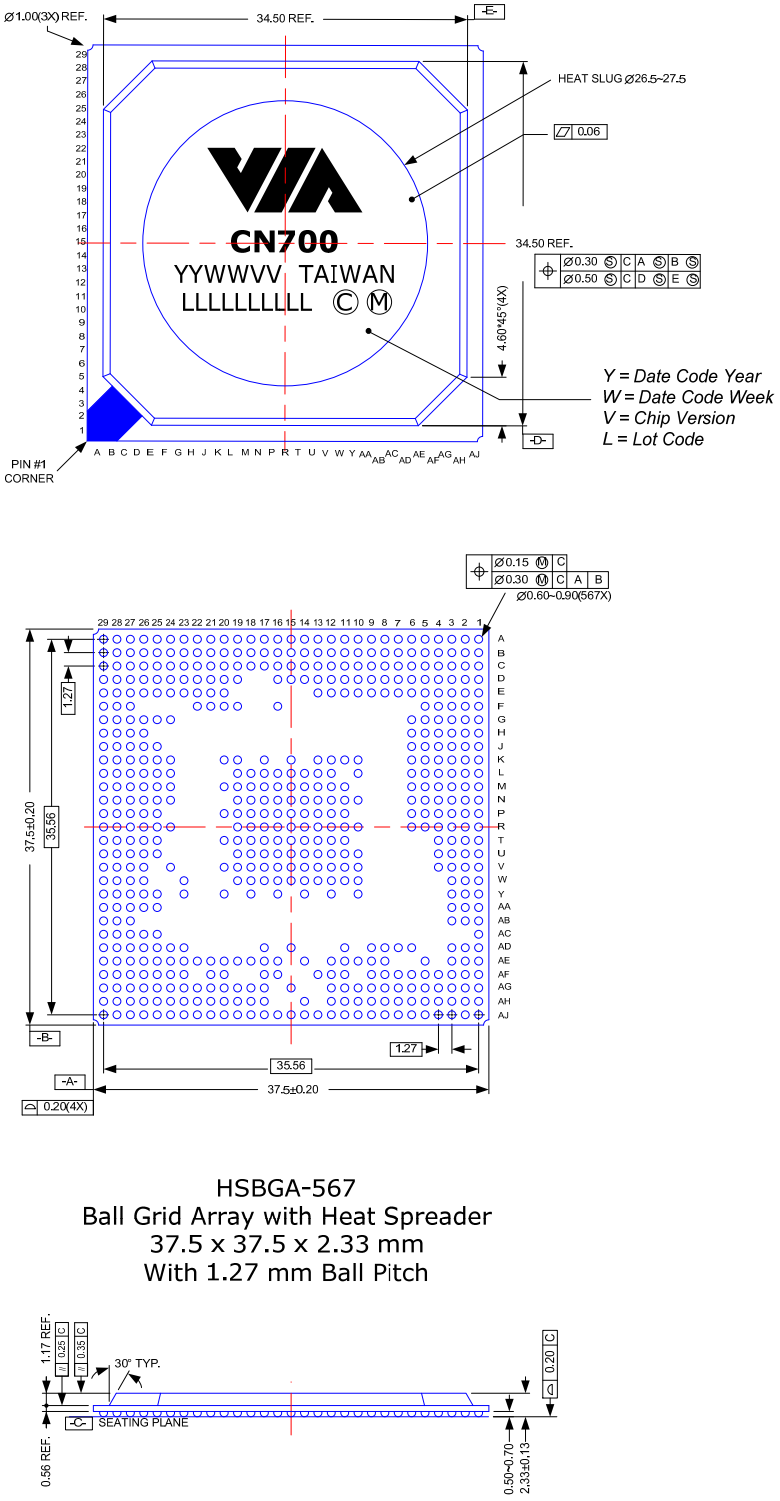
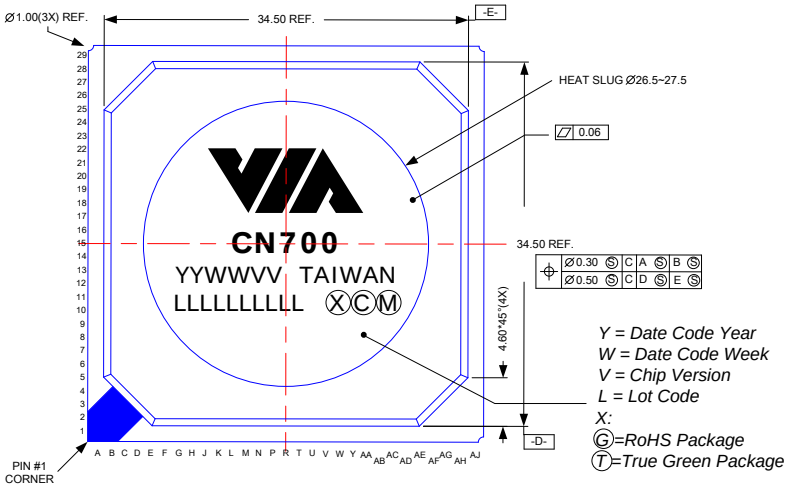
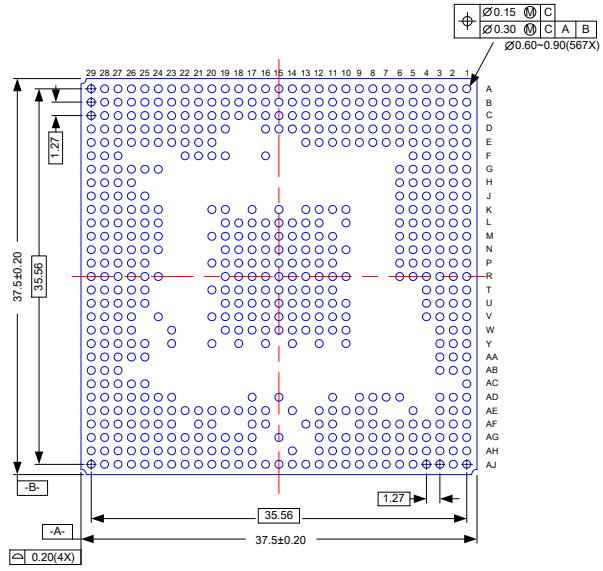


Figure 3. Mechanical Specifications - 567-Pin HSBGA Ball Grid Array Package with Heat Spreader





HSBGA-567
Ball Grid Array with Heat Spreader
37.5 x 37.5 x 2.33 mm
With 1.27 mm Ball Pitch

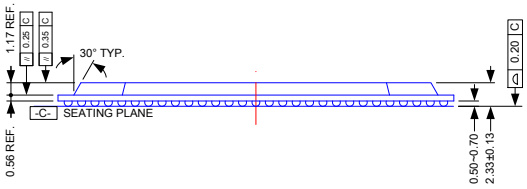


Figure 4. RoHS and True Green Mechanical Specifications - 567-Pin HSBGA Ball Grid Array Package with Heat Spreader