



Data Sheet

VT8251 South Bridge *A Highly Integrated Peripheral Controller*

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VIA TECHNOLOGIES, INC.

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VT8251 SOUTH BRIDGE

Two 1-Lane PCIe Ports
Eight USB 2.0 / USB 1.1 Ports
Four Serial ATA / RAID Ports
10 / 100 MAC with MII Interface
Dual Channel UltraDMA-133 EIDE Controller
High Definition Audio & AC97-Link Interface
LPC, SMBus, Serial IRQ, PnP, ACPI
1 GB/Sec Ultra V-Link Interface
Enhanced Power Management

PRODUCT FEATURES

- **Enhances Features of VIA VT8251**

- Supports two 1-Lane PCI Express ports
- Up to seven PCI 2.3 compliant devices
- Up to four S-ATA hard disk drives
- High definition audio with 192 KHz sampling rate, 24-bit per sample and up to 8 channels
- Enhanced AC97 v2.3 compliant audio interface with 96 KHz sampling rate and 20-bit per sample
- Sophisticated power management functions

- **Inter-operable with a wide variety of VIA North Bridges**

- Combines with PT890 / K8T890 for high performance Pentium 4 / Athlon 64 (Opteron) based server / workstation / desktop designs
- Combines with PT880 / KT600 / KT880 / K8T800 for performance Pentium 4 / Athlon / Athlon 64 (Opteron) based desktop designs
- Combines with PM880 / PM800 / KM400A for value Pentium 4 / Athlon based desktop designs
- Combines with PN880 / PN800 / KN400A for complete Pentium 4 / Athlon based mobile designs
- Combines with CN400 for complete featured, power efficient VIA C3 based desktop / mobile / embedded designs

- **High Bandwidth 1 GB/sec Ultra V-Link Controller**

- Supports 16-bit, 66 MHz, 4x and 8x transfer modes, Ultra V-Link interface with 1 GB/sec maximum bandwidth
 - Full duplex, with separate 8-bit Up and Down data path and command / strobe, in 8x mode
 - Half duplex, with 16-bit data bus, in 4x mode
- Supports high priority read/write channels for isochronous peripherals
- Request / Data split transaction
- Transaction assurance for V-Link Host to Client access eliminates V-Link Host-Client Retry cycles
- Intelligent V-Link transaction protocol to minimize data wait-state, throttle transfer latency to avoid data overflow
- Highly efficient V-Link arbitration with minimum overhead
- Auto connect / reconnect capability and dynamic stop for minimum power consumption

- **Advanced High Bandwidth PCI Express Interface**

- PCI Express 1.0a support
- Supports two 1-Lane ports or one 2-Lane port
- Supports interconnect power management
- Supports Hot Plug
- Loop-back testing mode for easy debugging mode for PCI Express

- **Ultra DMA-133 / 100 / 66 / 33 Bus Master EIDE Controller**

- Dual channel hard disk controller supporting up to four Enhanced IDE devices
- Data transfer rate up to 133 MB/sec to cover PIO mode 4, multi-word DMA mode 2, and UltraDMA-133 interface
- Dual DMA engines for concurrent dual channel operation
- Full scatter gather capability
- Supports ATAPI compliant devices including DVD devices
- Supports PCI native and ATA compatibility modes
- Bus master programming interface for SFF-8038i rev.1.0 and Windows-95 compliant
- Complete software driver support

- **Serial ATA / RAID Controller**

- Complies with Serial ATA Specification Revision 1.0
- Complies with Serial ATA II Specification
- Supports up to 4 S-ATA devices: 4 SATA II AHCI Bus Masters or 2 SATA I Bus Masters
- Integrated S-ATA PHY supporting 1.5 Gbit/s and 3 Gbit/s transfer rate
- Supports up to 32 entries command queue for each device
- Supports port multiplier
- Supports multiple RAID configurations - including RAID Level 0, RAID Level 1, RAID Level 0+1 and JBOD

- **10 / 100 Ethernet MAC**

- IEEE 802.3 compliant 10 / 100 Mbps Ethernet MAC for full and half duplex operations
- Standard MII interface to external PHYceiver
- Serial EEPROM interface

- **Universal Serial Bus Controller**

- Eight USB 2.0 ports with integrated PHY
- One USB 2.0 root hub and four USB 1.1 root hubs
- USB 2.0 and Enhanced Host Controller Interface (EHCI) v1.0 compliant
- USB 1.1 and Universal Host Controller Interface (UHCI) v1.1 compatible
- Legacy keyboard and PS/2 mouse support
- One USB 2.0 debug port

- **High Definition (HD) Audio Controller**

- High performance audio controller with 192 KHz sample rate, 24-bit per sample and up to 8 channels
- Microsoft UAA (Universal Audio Architecture) driver support
- Up to four independent playback streams and audio codecs
- Multiple recording channels for array microphone
- Supports jack sensing / retasking

- **AC'97 / MC'97 Controllers**

- AC97 2.3 compliant supporting 20-bit sampling, Double Rate S/PDIF mode and Jack Sense
- AC-Link interface to up to three AC / AMC / AC+MC CODEC with sample rate up to 96KHZ
- Supports 4 DX Sound stereo streams, 6-channel 3D audio and S/PDIF playback channels
- Supports 2 recording channels
- Programmable 8/16/20-bit, mono/stereo PCM data format support
- MC'97 modem controller supports up to V.92 standard
- Modem controller supported by all HSP modem companies

- **System Management Bus Interface**

- Compliant with System Management Bus (SMBus) Revision 2.0
- I²C devices compatible
- Supports SMBus Address Resolution Protocol (ARP) by using host commands through software
- Supports slave interface for external SMBus masters to control resume events
- Supports Alert On LAN II through a SMBus-interfaced register

- **Concurrent PCI Bus Controller**

- PCI 2.3 compliant, 33MHz, 32 bit, 3.3V PCI interface with 5V tolerant inputs
- Supports up to seven PCI masters
- Zero wait state PCI master and slave burst transfer rate, with up to 132 MB/sec data transfer rate
- PCI master snoop ahead and snoop filtering
- Byte merging in the write buffers to reduce the number of PCI cycles
- Supports delay transaction
- Transaction timer for fair arbitration between PCI masters
- Symmetric arbitration between Host / PCI bus for optimized system performance
- Complete steerable PCI interrupts

- **Sophisticated Mobile Power Management**

- ACPI 2.0 and APM v1.2 Compliant
- Supports OnNow power management
- Supports Intel Enhanced SpeedStepTM with dedicated pins
- Supports PCI Express WAKE suspend resume event
- Supports CPU clock throttling and clock stop during ACPI C0 / C1 / C2 / C3 states
- Supports PCI clock run, Power Management Enable (PME) control, and PCI / CPU clock generator stop control
- Supports multiple system suspend types: power-on suspends (POS) with flexible CPU / PCI bus reset options, suspend to DRAM (STR), and suspend to disk (soft-off), all with hardware automatic wake-up
- Multiple suspend power plane controls and suspend status indicators
- Integrates an idle timer, a peripheral timer and a general purpose timer, plus a 24/32-bit ACPI compliant timer
- Supports normal, doze, sleep, suspend and conserve modes
- Global and local device power control
- Supports system event monitoring with two event classes
- Primary and secondary interrupt differentiation for individual channels
- Dedicated input pins for power and sleep buttons, external modem ring indicator, and notebook lid open/close for system wake-up
- Multiple internal and external SMI sources for flexible power management models
- Thermal alarm on external temperature sensing circuit
- I/O pad leakage control

- **Plug and Play Functions**

- Steerable PCI interrupts
- Steerable interrupts for integrated peripheral controllers
- Microsoft Windows XPTM, Windows NTTM, Windows 2000TM, Windows 98TM and plug and play BIOS compliant

- **Integrated Legacy Functions**

- Integrated Keyboard Controller with PS/2 mouse and password wake-up support
- Integrated DS12885-style Real Time Clock with extended 256 byte CMOS RAM, Day / Month Alarm and century field
- Integrated DMA, timer, and interrupt controller
- Serial IRQ for docking and non-docking applications
- Fast reset and Gate A20 operation

- **Built-in NAND-tree pin scan test capability**
- **0.15um, 1.5V, low power CMOS process**
- **Single chip 31 x 31 mm, 1.0 mm ball pitch, 645 HSBGA**

VT8251 SYSTEM OVERVIEW

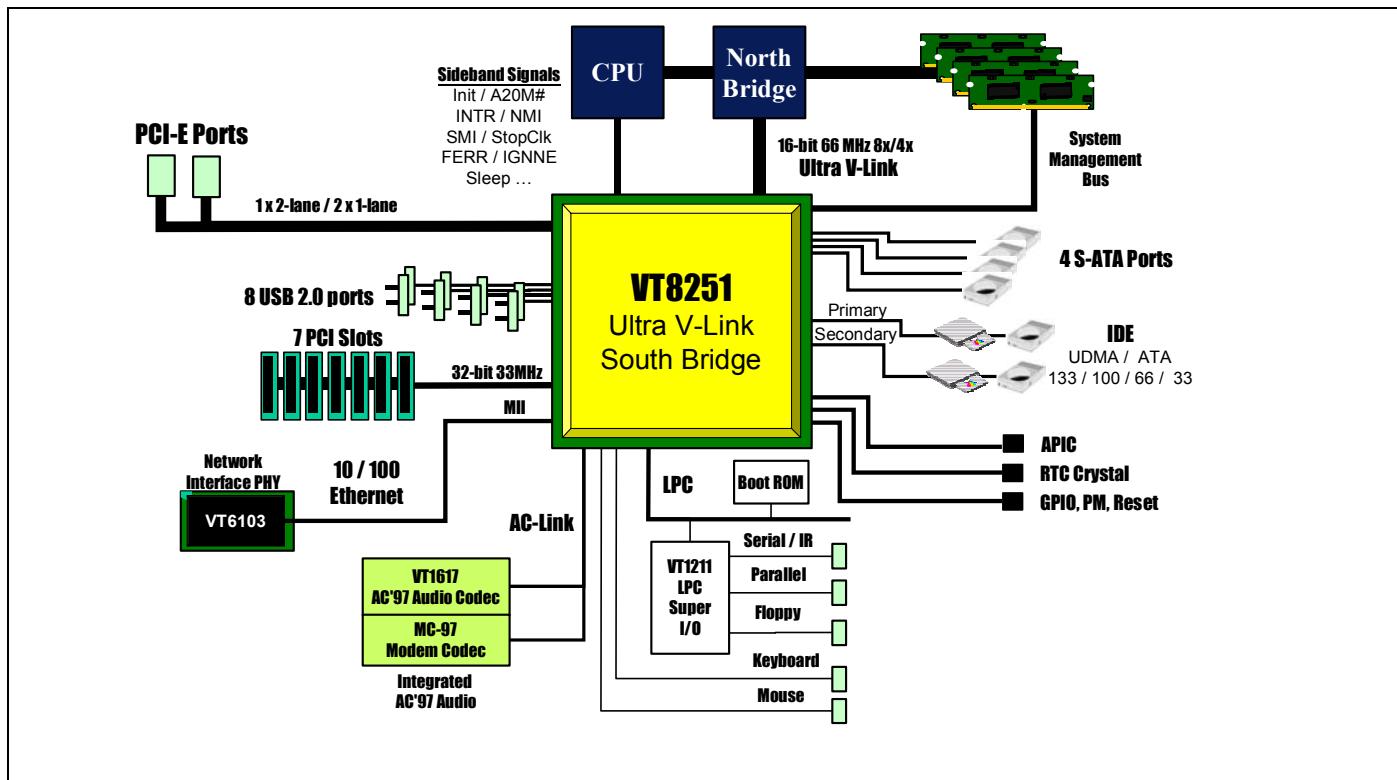


Figure 1. VT8251 System Block Diagram

The VT8251 interfaces to the companion North Bridge chip through the Ultra V-Link interface with up to 1 GB/sec data transfer rate. Two 1-Lane PCI Express ports are provided for high-speed peripheral devices. The VT8251 allows combining the two 1-Lane PCIe ports into a 2-Lane port for peripheral that requires extra bandwidth. For standard 33 MHz PCI devices, the VT8251 supports up to seven PCI master devices.

In addition, the VT8251 integrates extensive peripheral controllers for modern, state-of-the-art PC systems:

- **Four-port Serial ATA / RAID Controller**

The Serial ATA / RAID controller supports RAID Level 0, RAID Level 1, RAID Level 0+1 and JBOD, and complies with Serial ATA Specification Revision 1.0, and Serial ATA II specification. The Serial ATA controller is configurable and can be configured to support either 4 Serial ATA II master ports or 2/2 Serial ATA I master/slave ports with 3.0 Gbits/sec and 1.5 Gbits/sec data transfer rates.

- **Dual-channel Enhanced IDE Controller**

In addition to standard PIO and DMA mode operation, the VT8251 also supports the UltraDMA-133, 100, 66, and 33 standards, allows reliable data transfer rates up to 133 MB/sec. The IDE controller is SFF-8038i v1.0 and Microsoft Windows-family compliant.

- **IEEE 802.3 compliant 10 / 100 Mbps Ethernet MAC with MII interface to external PHYceiver**

- **Universal Serial Bus Controller with eight USB 2.0 ports**

The VT8251 USB controller includes four USB 1.1 root hubs, a USB 2.0 root hub, and eight USB 2.0 ports with integrated physical layer transceivers. Hot plug and isochronous peripherals are supported. Support of legacy keyboard and mouse is implemented so that legacy software could run transparently.

- **Integrated AC97-link Controller**

The AC-link controller can be used to attach an audio codec (AC), a modem codec (MC), an audio modem codec (AMC) or a combination of ACs and a single MC.

- **Full System Management Bus (SMBus) interface**

- **Keyboard controller with PS/2 mouse support**

- **Real Time Clock with 256 bytes extended CMOS**

In addition to the standard ISA RTC functionality, the integrated RTC also includes the date alarm, century field and other enhancements for compatibility with the ACPI standard.

- **Notebook-class, sophisticated Power Management Unit compliant with ACPI and legacy APM requirements**

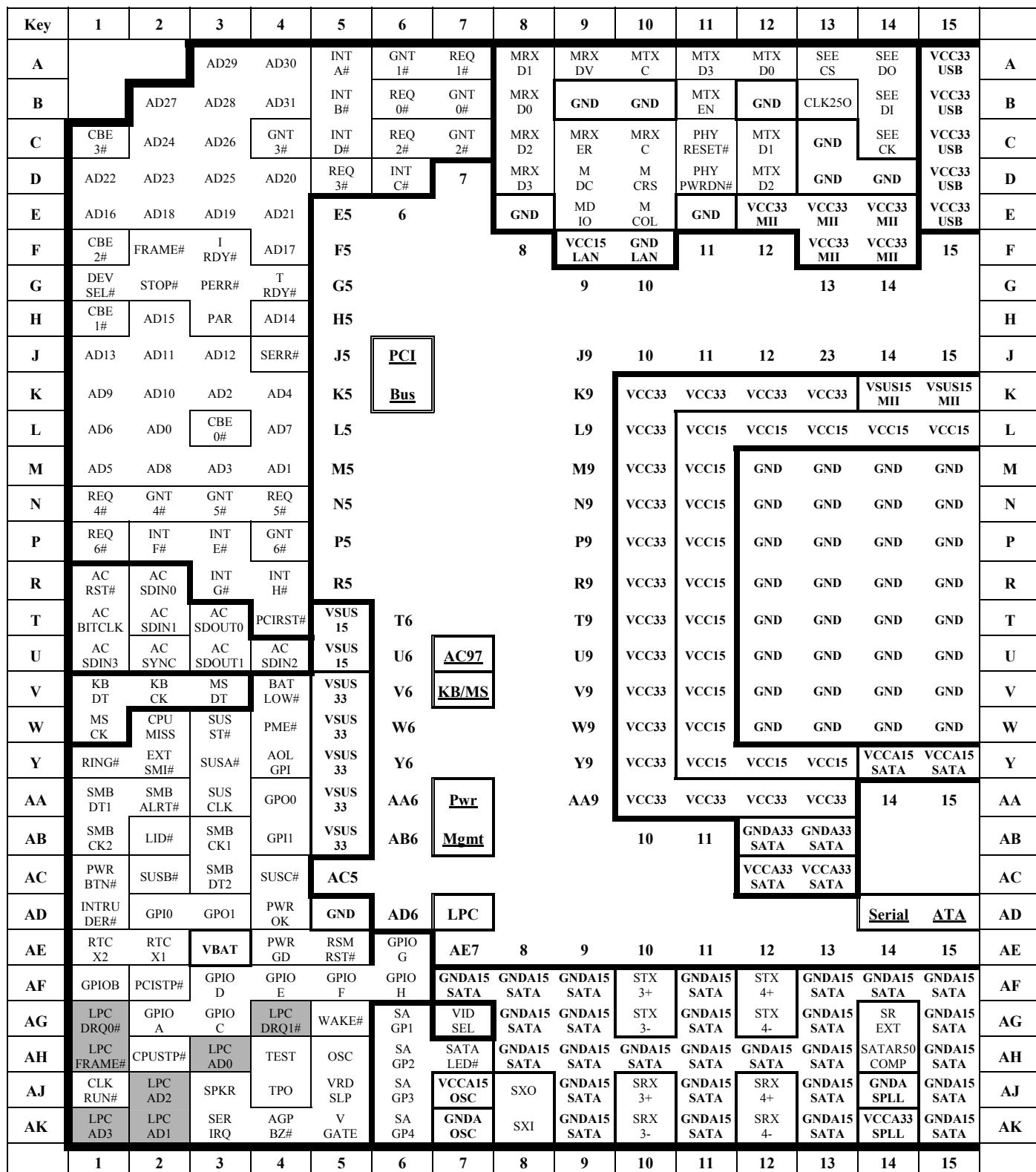
Multiple sleep states (POS, STR and STD) are supported with hardware automatic wake-up. Additional functionality includes event monitoring, CPU clock throttling and stop, PCI bus clock stop control, modular power, clock and leakage control, hardware-based and software-based event handling, general purpose I/O, chip select and external SMI.

- **Plug and Play functions with steerable PCI interrupts**

The PnP function allows complete steerability of PCI interrupts and integrated peripheral interrupts to system interrupt channel. One additional steerable interrupt channel is provided to allow plug and play and re-configurability of on-board peripherals for Windows family compliance.

The VT8251 also enhances the functionality of standard integrated peripherals. The integrated interrupt controller supports both edge and level triggered interrupts channel by channel. The integrated DMA controller supports type-F DMA in addition to standard ISA DMA modes. Compliant with the PCI v2.3 specification, the VT8251 supports delayed transactions so that slower internal ISA peripherals do not block the traffic of the PCI bus. Special circuitry is built in to allow concurrent operation without causing deadlock in a PCI-to-PCI bridge environment.

PINOUTS

Figure 2. VT8251 Ball Diagram (Top View)


Note: LPC pins are marked in gray.

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30		
A	GND USB	USB P7+	GND USB	USB P5+	GND USB	USB P3+	GND USB	USB P1+	GND USB	USB OC4#	USB OC6#	USB OC2#	USB OC0#	USB OC1#		A	
B	GND USB	USB P7-	GND USB	USB P5-	GND USB	USB P3-	GND USB	USB P1-	GND USB	USB OC5#	USB OC7#	USB OC3#	GPO9 GND	GND		B	
C	GND USB	GND USB	GND USB	GND USB	GND USB	GND USB	GND USB	GND USB	GND USB	VCCA15 REXT	VCCA15 PLLUSB	GND	GPI9 GND	GND		C	
D	GND USB	USB P6+	GND USB	USB P4+	GND USB	USB P2-	GND USB	USB P0-	GND USB	VCCA33 PLLUSB	GNDA15 PLLUSB	VSUS15 USB	GND GNDA PE1	VCCA33 PE1		D	
E	GND USB	USB P6-	GND USB	USB P4-	GND USB	USB P2+	GND USB	USB P0+	GND USB	GNDA33 PLLUSB	USB CLK	GND	PE CLK-	PE CLK+		E	
F	VSUS15 USB	17	18	19	20	21	22	23	F24	25	26	PE RX2-	PE RX2+	PE TX2+	PE TX2-	F	
G	16								G24	VCC33 PE	VCC33 PE	VCC33 PE				G	
H									H24	VCC33 PE	VCC33 PE	GND	PE TX1-	PE TX1+	GND	H	
J	16	17	18	19	20	21	J22			VSUS15 PE	PE REXT	GNDA PE	VCCA33 PE	GND		J	
K	VCC33 USB	VCC33 USB	VCC33 USB	VCC33 USB	VCC15	GND	K22			VCC33 PE	PE COMP	VCC33 PE	GND	GND		K	
L	GND USB	GND USB	GND USB	GND USB	VCC15	VCC33 PE	L22	PCI	L24	VCC33 PE	VCC33 PE	GND	V D13	V D12	GND	L	
M	GND GND	GND GND	GND GND	GND GND	VCC15	VCC33 PE	M22	Express		M25	VL COMPP	VL COMPP	V D09	V D08	VPAR		M
N	GND GND	GND GND	GND GND	GND GND	VCC15	VCC33 PE	N22			N25	VCC15 VL	VCC15 VL	V D04	V D05	V D01		N
P	GND GND	GND GND	GND GND	GND GND	VCC15	VCC15 VL	P22		P24	VL VREF	VCC15 VL	GND	VBE#	V D00	GND	P	
R	GND GND	GND GND	GND GND	GND GND	VCC15	VCC15 VL	R22		R24	VCC15 VL	DN STB+	DN STB+	UP STB+	UP STB-		R	
T	GND GND	GND GND	GND GND	GND GND	VCC15	VCC15 VL	T22		T24	VCC15 VL	DN CMD	VD 07	VD 03	VD 02		T	
U	GND GND	GND GND	GND GND	GND GND	VCC33	VCC15 VL	U22	V-	U24	VD10	GND	UP CMD	VD 06	GND		U	
V	GND GND	GND GND	GND GND	GND GND	VCC15	VCC33	V22	Link	V24	GND PLL	VCC15 PLL	V CLK	VD 15	VD 14	VD 11		V
W	GND GND	GND GND	GND GND	GND GND	VCC15	VCC33	Y22		W24	VCC15 VL	VCC15 VL	VCC15 VL	VCC15 VL	VCC15 VL	VCC15 VL		W
Y	VCCA15 SATA	VCC15	VCC15	VCC15	VCC15	VCC33	Y22		Y24	VCC15 VL	VCC15 VL	VCC15 VL	VCC15 VL	VCC15 VL	GHI#		Y
AA	16	17	VCC33	VCC33	VCC33	VCC33	AA2	APIC	GND	INTR	INIT#	APIC D0	APIC D1	DP SLP#			AA
AB							AB22	CPU		AB25	PD A2	PD A0	FERR#	SMI#	NMI		AB
AC								PIDE	GND	PD CS1#	GND	A20M#	STP CLK#	SLP#		AC	
AD								SIDE		AD25	PD IOR#	PD IOW#	APIC CLK	THRM TRIP#	IGN NE#		AD
AE	16	17	18	19						AE25	PD IORDY	PD DACK#	PCI CLK	PD A1	IRQ14		AE
AF	STX 1+	GNDA15 SATA	STX 2+	GNDA15 SATA			21	22	GND	GND	SD A2	PD D8	GND	PD D15	GND		AF
AG	STX 1-	GNDA15 SATA	STX 2-	GNDA15 SATA			20		SD	SD	SD D13	IRQ 15	SD A0	PD D4	PD D1		AG
AH	GNDA15 SATA	GNDA15 SATA	GNDA15 SATA	GNDA15 SATA				SD	SD	SD D2	SD D0	SD IOW#	PD D9	PD D12		AH	
AJ	SRX 1+	GNDA15 SATA	SRX 2+	GNDA15 SATA				SD	SD	SD D11	GND	SD D14	GND	PD D7	PD D5		AJ
AK	SRX 1-	GNDA15 SATA	SRX 2-	GNDA15 SATA				SD	SD	SD D4	SD D9	SD D12	SD D1	SD IOR#	SD CS3#		AK
	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30		

Pin List

Table 1. Pin List (Listed by Pin Number)

Pin#	Pin Name	Pin#	Pin Name	Pin#	Pin Name	Pin#	Pin Name	Pin#	Pin Name
A03	AD29	C10	MRXC	E19	USBP4-	K15	VSUS15MII	N15	GND
A04	AD30	C11	PHYRESET#	E20	GNDUSB	K16	VCC33USB	N16	GND
A05	INTA#	C12	MTXD1	E21	USBP2+	K17	VCC33USB	N17	GND
A06	GNT1#	C13	GND	E22	GNDUSB	K18	VCC33USB	N18	GND
A07	REQ1#	C14	SEECK	E23	USBP0+	K19	VCC33USB	N19	GND
A08	MRXD1	C15	VCC33USB	E24	GNDUSB	K20	VCC15	N20	VCC15
A09	MRXDV	C16	GNDUSB	E25	GNDA33PLLUSB	K21	GND	N21	VCC33PE
A10	MTXC	C17	GNDUSB	E26	USBCLK	K23	GND	N26	VCC15VL
A11	MTXD3	C18	GNDUSB	E27	GND	K24	GND	N27	VD4
A12	MTXD0	C19	GNDUSB	E28	PECLK-	K25	VCC33PE	N28	VD5
A13	SEECS	C20	GNDUSB	E29	PECLK+	K26	PECOMP	N29	VD1
A14	SEEDO	C21	GNDUSB	E30	GND	K27	VCC33PE	P01	REQ6#
A15	VCC33USB	C22	GNDUSB	F01	CBE2#	K28	GND	P02	INTF#
A16	GNDUSB	C23	GNDUSB	F02	FRAME#	K29	GND	P03	INTE#
A17	USBP7+	C24	GNDUSB	F03	IRDY#	L01	AD6	P04	GNT6#
A18	GNDUSB	C25	USBREXT	F04	AD17	L02	AD0	P10	VCC33
A19	USBP5+	C26	VCCA15PLLUSB	F09	VCC15LAN	L03	CBE0#	P11	VCC15
A20	GNDUSB	C27	GND	F10	GNDLAN	L04	AD7	P12	GND
A21	USBP3+	C28	GPI9	F13	VCC33MII	L10	VCC33	P13	GND
A22	GNDUSB	C29	GND	F14	VCC33MII	L11	VCC15	P14	GND
A23	USBP1+	C30	GND	F16	VSUS15USB	L12	VCC15	P15	GND
A24	GNDUSB	D01	AD22	F27	PERX2-	L13	VCC15	P16	GND
A25	USBOC4#	D02	AD23	F28	PERX2+	L14	VCC15	P17	GND
A26	USBOC6#	D03	AD25	F29	PETX2+	L15	VCC15	P18	GND
A27	USBOC2#	D04	AD20	F30	PETX2-	L16	GNDUSB	P19	GND
A28	USBOC0#	D05	REQ3#	G01	DEVSEL#	L17	GNDUSB	P20	VCC15
A29	USBOC1#	D06	INTC#	G02	STOP#	L18	GNDUSB	P21	VCC15VL
B02	AD27	D08	MRXD3	G03	PERR#	L19	GNDUSB	P25	VLVREF
B03	AD28	D09	MDC	G04	TRDY#	L20	VCC15	P26	VCC15VL
B04	AD31	D10	MCRS	G25	VCC33PE	L21	VCC33PE	P27	GND
B05	INTB#	D11	PHYPWRDN#	G26	VCC33PE	L25	VCC33PE	P28	VBE#
B06	REQ0#	D12	MTXD2	G27	VCC33PE	L26	VCC33PE	P29	VD0
B07	GNT0#	D13	GND	G29	PERX1-	L27	GND	P30	GND
B08	MRXD0	D14	GND	G30	PERX1+	L28	VD13	R01	ACRST#
B09	GND	D15	VCC33USB	H01	CBE1#	L29	VD12	R02	ACSDIN0
B10	GND	D16	GNDUSB	H02	AD15	L30	GND	R03	INTG#
B11	MTXEN	D17	USBP6+	H03	PAR	M01	AD5	R04	INTH#
B12	GND	D18	GNDUSB	H04	AD14	M02	AD8	R10	VCC33
B13	CLK250	D19	USBP4+	H25	VCC33PE	M03	AD3	R11	VCC15
B14	SEEDI	D20	GNDUSB	H26	VCC33PE	M04	AD1	R12	GND
B15	VCC33USB	D21	USBP2-	H27	GND	M10	VCC33	R13	GND
B16	GNDUSB	D22	GNDUSB	H28	PETX1-	M11	VCC15	R14	GND
B17	USBP7-	D23	USBP0-	H29	PETX1+	M12	GND	R15	GND
B18	GNDUSB	D24	GNDUSB	H30	GND	M13	GND	R16	GND
B19	USBP5-	D25	VCCA33PLLUSB	J01	AD13	M14	GND	R17	GND
B20	GNDUSB	D26	GNDA15PLLUSB	J02	AD11	M15	GND	R18	GND
B21	USBP3-	D27	VSUS15USB	J03	AD12	M16	GND	R19	GND
B22	GNDUSB	D28	GND	J04	SERR#	M17	GND	R20	VCC15
B23	USBP1-	D29	GNDAPE1	J23	GND	M18	GND	R21	VCC15VL
B24	GNDUSB	D30	VCCA33PE1	J24	GND	M19	GND	R25	VCC15VL
B25	USBOC5#	E01	AD16	J25	VSUS15PE	M20	VCC15	R26	DNSTB+
B26	USBOC7#	E02	AD18	J26	PEREXT	M21	VCC33PE	R27	DNSTB-
B27	USBOC3#	E03	AD19	J27	GNDAPE	M26	VLCOMPP	R28	UPSTB+
B28	GPO9	E04	AD21	J28	VCCA33PE	M27	VD9	R29	UPSTB-
B29	GND	E08	GND	J29	GND	M28	VD8	T01	ACBITCLK
B30	GND	E09	MDIO	J30	GND	M29	VPAR	T02	ACSDIN1
C01	CBE3#	E10	MCOL	K01	AD9	N01	REQ4#	T03	ACSDOUT0
C02	AD24	E11	GND	K02	AD10	N02	GNT4#	T04	PCIRST#
C03	AD26	E12	VCC33MII	K03	AD2	N03	GNT5#	T05	VSUS15
C04	GNT3#	E13	VCC33MII	K04	AD4	N04	REQ5#	T10	VCC33
C05	INTD#	E14	VCC33MII	K10	VCC33	N10	VCC33	T11	VCC15
C06	REQ2#	E15	VCC33USB	K11	VCC33	N11	VCC15	T12	GND
C07	GNT2#	E16	GNDUSB	K12	VCC33	N12	GND	T13	GND
C08	MRXD2	E17	USBP6-	K13	VCC33	N13	GND	T14	GND
C09	MRXER	E18	GNDUSB	K14	VSUS15MII	N14	GND	T15	GND

Pin#	Pin Name	Pin#	Pin Name	Pin#	Pin Name	Pin#	Pin Name	Pin#	Pin Name
T16	GND	W12	GND	AB13	GNDA33SATA	AF19	GNDA15SATA	AH27	PDD9
T17	GND	W13	GND	AB18	GNDA33SATA	AF23	GND	AH28	PDD12
T18	GND	W14	GND	AB19	GNDA33SATA	AF24	GND	AH29	PDD2
T19	GND	W15	GND	AB26	PDA2	AF25	SDA2	AH30	PDD13
T20	VCC15	W16	GND	AB27	PDA0	AF26	PDD8	AJ01	CLKRUN#
T21	VCC15VL	W17	GND	AB28	FERR#	AF27	GND	AJ02	LPCAD2
T25	VCC15VL	W18	GND	AB29	SMI#	AF28	PDD15	AJ03	SPKR
T26	DNCMD	W19	GND	AB30	NMI	AF29	PDDREQ	AJ04	TPO
T27	VD7	W20	VCC15	AC01	PWRBTN#	AF30	GND	AJ05	VRDSDL
T28	VD3	W21	VCC33	AC02	SUSB#	AG01	LPCDRQ0#	AJ06	SAGP3
T29	VD2	W25	VCC15VL	AC03	SMBDT2	AG02	GPIOA	AJ07	VCCA15OSC
U01	ACSDIN3	W26	VCC15VL	AC04	SUSC#	AG03	GPIOC	AJ08	SXO
U02	ACSYNC	W27	VCC15VL	AC12	VCCA33SATA	AG04	LPCDRQ1#	AJ09	GNDA15SATA
U03	ACSDOUT1	W28	VCC15VL	AC13	VCCA33SATA	AG05	WAKE#	AJ10	SRX3+
U04	ACSDIN2	W29	VCC15VL	AC18	VCCA33SATA	AG06	SAGP1	AJ11	GNDA15SATA
U05	VSUS15	W30	VCC15VL	AC19	VCCA33SATA	AG07	VIDSEL	AJ12	SRX4+
U10	VCC33	Y01	RING#	AC24	GND	AG08	GNDA15SATA	AJ13	GNDA15SATA
U11	VCC15	Y02	EXTSMI#	AC25	PDCS1#	AG09	GNDA15SATA	AJ14	GNDASPLL
U12	GND	Y03	SUSA#	AC26	PDCS3#	AG10	STX3-	AJ15	GNDA15SATA
U13	GND	Y04	AOLGPI	AC27	GND	AG11	GNDA15SATA	AJ16	SRX1+
U14	GND	Y05	VSUS33	AC28	A20M#	AG12	STX4-	AJ17	GNDA15SATA
U15	GND	Y10	VCC33	AC29	STPCLK#	AG13	GNDA15SATA	AJ18	SRX2+
U16	GND	Y11	VCC15	AC30	SLP#	AG14	SREXT	AJ19	GNDA15SATA
U17	GND	Y12	VCC15	AD01	INTRUDER#	AG15	GNDA15SATA	AJ20	GND
U18	GND	Y13	VCC15	AD02	GPI0	AG16	STX1-	AJ21	SDD6
U19	GND	Y14	VCCA15SATA	AD03	GPO1	AG17	GNDA15SATA	AJ22	SDD11
U20	VCC15	Y15	VCCA15SATA	AD04	PWROK	AG18	STX2-	AJ23	GND
U21	VCC33	Y16	VCCA15SATA	AD05	GND	AG19	GNDA15SATA	AJ24	SDD14
U25	VCC15VL	Y17	VCC15	AD26	PDIOR#	AG21	SDD5	AJ25	SDDREQ
U26	VD10	Y18	VCC15	AD27	PDIOW#	AG22	SDD10	AJ26	GND
U27	GND	Y19	VCC15	AD28	APICLK	AG23	SDD13	AJ27	PDD7
U28	UPCMD	Y20	VCC15	AD29	THRMRTRIP#	AG24	IRQ15	AJ28	PDD5
U29	VD6	Y21	VCC33	AD30	IGNNE#	AG25	SDA0	AJ29	GND
U30	GND	Y25	VCC15VL	AE01	RTCX2	AG26	SDCS1#	AJ30	PDD3
V01	KBDT	Y26	VCC15VL	AE02	RTCTX1	AG27	PDD4	AK01	LPCAD3
V02	KBCK	Y27	VCC15VL	AE03	VBAT	AG28	PDD1	AK02	LPCAD1
V03	MSDT	Y28	VCC15VL	AE04	PWRGD	AG29	PDD14	AK03	SERIRQ
V04	BATLOW#	Y29	VCC15VL	AE05	RSMRST#	AG30	PDD0	AK04	AGPBZ#
V05	VSUS33	Y30	GHI#	AE06	GPIOG	AH01	LPCFRAME#	AK05	VGATE
V10	VCC33	AA01	SMBDT1	AE23	SDDACK#	AH02	CPUSTP#	AK06	SAGP4
V11	VCC15	AA02	SMBALRT#	AE24	SDA1	AH03	LPCADO	AK07	GNDOSC
V12	GND	AA03	SUSCLK	AE26	PDIORDY	AH04	TEST	AK08	SXI
V13	GND	AA04	GPO0	AE27	PDDACK#	AH05	OSC	AK09	GNDA15SATA
V14	GND	AA05	VSUS33	AE28	PCICLK	AH06	SAGP2	AK10	SRX3-
V15	GND	AA10	VCC33	AE29	PDA1	AH07	SATALED#	AK11	GNDA15SATA
V16	GND	AA11	VCC33	AE30	IRQ14	AH08	GNDA15SATA	AK12	SRX4-
V17	GND	AA12	VCC33	AF01	GPIOB	AH09	GNDA15SATA	AK13	GNDA15SATA
V18	GND	AA13	VCC33	AF02	PCISTP#	AH10	GNDA15SATA	AK14	VCCA33SPLL
V19	GND	AA18	VCC33	AF03	GPIOD	AH11	GNDA15SATA	AK15	GNDA15SATA
V20	VCC15	AA19	VCC33	AF04	GPIOE	AH12	GNDA15SATA	AK16	SRX1-
V21	VCC33	AA20	VCC33	AF05	GPIOF	AH13	GNDA15SATA	AK17	GNDA15SATA
V25	GNDPLL	AA21	VCC33	AF06	GPIOH	AH14	SATAR50COMP	AK18	SRX2-
V26	VCC15PLL	AA24	GND	AF07	GNDA15SATA	AH15	GNDA15SATA	AK19	GNDA15SATA
V27	VCLK	AA25	INTR	AF08	GNDA15SATA	AH16	GNDA15SATA	AK20	SDD7
V28	VD15	AA26	INIT#	AF09	GNDA15SATA	AH17	GNDA15SATA	AK21	SDD9
V29	VD14	AA27	APICD0	AF10	STX3+	AH18	GNDA15SATA	AK22	SDD4
V30	VD11	AA28	APICD1	AF11	GNDA15SATA	AH19	GNDA15SATA	AK23	SDD12
W01	MSCK	AA29	DPSLP#	AF12	STX4+	AH20	GND	AK24	SDD1
W02	CPUMISS	AB01	SMBCK2	AF13	GNDA15SATA	AH21	SDD8	AK25	SDD15
W03	SUSST#	AB02	LID#	AF14	GNDA15SATA	AH22	SDD3	AK26	SDIOR#
W04	PME#	AB03	SMBCK1	AF15	GNDA15SATA	AH23	SDD2	AK27	SDCS3#
W05	VSUS33	AB04	GPI1	AF16	STX1+	AH24	SDD0	AK28	PDD6
W10	VCC33	AB05	VSUS33	AF17	GNDA15SATA	AH25	SDIOW#	AK29	PDD10
W11	VCC15	AB12	GNDA33SATA	AF18	STX2+	AH26	SDIORDY	AK30	PDD11

Table 2. Pin List (Listed by Pin Name)

Pin#	Pin Name	Pin#	Pin Name	Pin#	Pin Name	Pin#	Pin Name	Pin#	Pin Name
AC28	A20M#	AA24	GND	P19	GND	AH11	GNDA15SATA	A06	GNT1#
T01	ACBITCLK	AC24	GND	P27	GND	AH12	GNDA15SATA	C07	GNT2#
R01	ACRST#	AC27	GND	P30	GND	AH13	GNDA15SATA	C04	GNT3#
R02	ACSDIN0	AD05	GND	R12	GND	AH15	GNDA15SATA	N02	GNT4#
T02	ACSDIN1	AF23	GND	R13	GND	AH16	GNDA15SATA	N03	GNT5#
U04	ACSDIN2	AF24	GND	R14	GND	AH17	GNDA15SATA	P04	GNT6#
U01	ACSDIN3	AF27	GND	R15	GND	AH18	GNDA15SATA	AD02	GPI0
T03	ACSDOUT0	AF30	GND	R16	GND	AH19	GNDA15SATA	AB04	GPI1
U03	ACSDOUT1	AH20	GND	R17	GND	AJ09	GNDA15SATA	C28	GPI9
U02	ACSYNC	AJ20	GND	R18	GND	AJ11	GNDA15SATA	AG02	GPIOA
L02	AD0	AJ23	GND	R19	GND	AJ13	GNDA15SATA	AF01	GPIOB
M04	AD1	AJ26	GND	T12	GND	AJ15	GNDA15SATA	AG03	GPIOC
K03	AD2	AJ29	GND	T13	GND	AJ17	GNDA15SATA	AF03	GPIOD
M03	AD3	B09	GND	T14	GND	AJ19	GNDA15SATA	AF04	GPIOE
K04	AD4	B10	GND	T15	GND	AK09	GNDA15SATA	AF05	GPIOF
M01	AD5	B12	GND	T16	GND	AK11	GNDA15SATA	AE06	GPIOG
L01	AD6	B29	GND	T17	GND	AK13	GNDA15SATA	AF06	GPIOH
L04	AD7	B30	GND	T18	GND	AK15	GNDA15SATA	AA04	GPO0
M02	AD8	C13	GND	T19	GND	AK17	GNDA15SATA	AD03	GPO1
K01	AD9	C27	GND	U12	GND	AK19	GNDA15SATA	B28	GPO9
K02	AD10	C29	GND	U13	GND	E25	GNDA33PLLUSB	AD30	IGNNE#
J02	AD11	C30	GND	U14	GND	AB12	GNDA33SATA	AA26	INIT#
J03	AD12	D13	GND	U15	GND	AB13	GNDA33SATA	A05	INTA#
J01	AD13	D14	GND	U16	GND	AB18	GNDA33SATA	B05	INTB#
H04	AD14	D28	GND	U17	GND	AB19	GNDA33SATA	D06	INTC#
H02	AD15	E08	GND	U18	GND	AK07	GNDAOSC	C05	INTD#
E01	AD16	E11	GND	U19	GND	J27	GNDAPE	P03	INTE#
F04	AD17	E27	GND	U27	GND	D29	GNDAPE1	P02	INTF#
E02	AD18	E30	GND	U30	GND	AJ14	GNDASPLL	R03	INTG#
E03	AD19	H27	GND	V12	GND	F10	GNDLAN	R04	INTH#
D04	AD20	H30	GND	V13	GND	V25	GNDPLL	AA25	INTR
E04	AD21	J23	GND	V14	GND	A16	GNDUSB	AD01	INTRUDER#
D01	AD22	J24	GND	V15	GND	A18	GNDUSB	F03	IRDY#
D02	AD23	J29	GND	V16	GND	A20	GNDUSB	AE30	IRQ14
C02	AD24	J30	GND	V17	GND	A22	GNDUSB	AG24	IRQ15
D03	AD25	K21	GND	V18	GND	A24	GNDUSB	V02	KBCK
C03	AD26	K23	GND	V19	GND	B16	GNDUSB	V01	KBDT
B02	AD27	K24	GND	W12	GND	B18	GNDUSB	AB02	LID#
B03	AD28	K28	GND	W13	GND	B20	GNDUSB	AH03	LPCAD0
A03	AD29	K29	GND	W14	GND	B22	GNDUSB	AK02	LPCAD1
A04	AD30	L27	GND	W15	GND	B24	GNDUSB	AJ02	LPCAD2
B04	AD31	L30	GND	W16	GND	C16	GNDUSB	AK01	LPCAD3
AK04	AGPBZ#	M12	GND	W17	GND	C17	GNDUSB	AG01	LPCDRQ0#
Y04	AOLGPI	M13	GND	W18	GND	C18	GNDUSB	AG04	LPCDRQ1#
AD28	APICCLK	M14	GND	W19	GND	C19	GNDUSB	AH01	LPCFRAME#
AA27	APICD0	M15	GND	D26	GNDA15PLLUSB	C20	GNDUSB	E10	MCOL
AA28	APICD1	M16	GND	AF07	GNDA15SATA	C21	GNDUSB	D10	MCRS
V04	BATLOW#	M17	GND	AF08	GNDA15SATA	C22	GNDUSB	D09	MDC
L03	CBE0#	M18	GND	AF09	GNDA15SATA	C23	GNDUSB	E09	MDIO
H01	CBE1#	M19	GND	AF11	GNDA15SATA	C24	GNDUSB	C10	MRXC
F01	CBE2#	M12	GND	AF13	GNDA15SATA	D16	GNDUSB	B08	MRXD0
C01	CBE3#	N13	GND	AF14	GNDA15SATA	D18	GNDUSB	A08	MRXD1
B13	CLK25O	N14	GND	AF15	GNDA15SATA	D20	GNDUSB	C08	MRXD2
AJ01	CLKRUN#	N15	GND	AF17	GNDA15SATA	D22	GNDUSB	D08	MRXD3
W02	CPUMISS	N16	GND	AF19	GNDA15SATA	D24	GNDUSB	A09	MRXDV
AH02	CPUSTP#	N17	GND	AG08	GNDA15SATA	E16	GNDUSB	C09	MRXER
G01	DEVSEL#	N18	GND	AG09	GNDA15SATA	E18	GNDUSB	W01	MSCK
T26	DNCMD	N19	GND	AG11	GNDA15SATA	E20	GNDUSB	V03	MSDT
R27	DNSTB-	P12	GND	AG13	GNDA15SATA	E22	GNDUSB	A10	MTXC
R26	DNSTB+	P13	GND	AG15	GNDA15SATA	E24	GNDUSB	A12	MTXD0
AA29	DPSLP#	P14	GND	AG17	GNDA15SATA	L16	GNDUSB	C12	MTXD1
Y02	EXTSMI#	P15	GND	AG19	GNDA15SATA	L17	GNDUSB	D12	MTXD2
AB28	FERR#	P16	GND	AH08	GNDA15SATA	L18	GNDUSB	A11	MTXD3
F02	FRAME#	P17	GND	AH09	GNDA15SATA	L19	GNDUSB	B11	MTXEN
Y30	GHI#	P18	GND	AH10	GNDA15SATA	B07	GNT0#	AB30	NMI

Pin#	Pin Name	Pin#	Pin Name	Pin#	Pin Name	Pin#	Pin Name	Pin#	Pin Name
AH05	OSC	AK06	SAGP4	AC04	SUSC#	Y12	VCC15	K27	VCC33PE
H03	PAR	AH07	SATALED#	AA03	SUSCLK	Y13	VCC15	L21	VCC33PE
AE28	PCICLK	AH14	SATAR50COMP	W03	SUSST#	Y17	VCC15	L25	VCC33PE
T04	PCIRST#	AG25	SDA0	AK08	SXI	Y18	VCC15	L26	VCC33PE
AF02	PCISTP#	AE24	SDA1	AJ08	SXO	Y19	VCC15	M21	VCC33PE
AB27	PDA0	AF25	SDA2	AH04	TEST	Y20	VCC15	N21	VCC33PE
AE29	PDA1	AG26	SDCS1#	AD29	THRMTRIP#	F09	VCC15LAN	A15	VCC33USB
AB26	PDA2	AK27	SDCS3#	AJ04	TPO	V26	VCC15PLL	B15	VCC33USB
AC25	PDCS1#	AH24	SDD0	G04	TRDY#	N26	VCC15VL	C15	VCC33USB
AC26	PDCS3#	AK24	SDD1	U28	UPCMD	P21	VCC15VL	D15	VCC33USB
AG30	PDD0	AH23	SDD2	R29	UPSTB-	P26	VCC15VL	E15	VCC33USB
AG28	PDD1	AH22	SDD3	R28	UPSTB+	R21	VCC15VL	K16	VCC33USB
AH29	PDD2	AK22	SDD4	E26	USBCLK	R25	VCC15VL	K17	VCC33USB
AJ30	PDD3	AG21	SDD5	A28	USBOC0#	T21	VCC15VL	K18	VCC33USB
AG27	PDD4	AJ21	SDD6	A29	USBOC1#	T25	VCC15VL	K19	VCC33USB
AJ28	PDD5	AK20	SDD7	A27	USBOC2#	U25	VCC15VL	AJ07	VCCA15OSC
AK28	PDD6	AH21	SDD8	B27	USBOC3#	W25	VCC15VL	C26	VCCA15PLLUSB
AJ27	PDD7	AK21	SDD9	A25	USBOC4#	W26	VCC15VL	Y14	VCCA15SATA
AF26	PDD8	AG22	SDD10	B25	USBOC5#	W27	VCC15VL	Y15	VCCA15SATA
AH27	PDD9	AJ22	SDD11	A26	USBOC6#	W28	VCC15VL	Y16	VCCA15SATA
AK29	PDD10	AK23	SDD12	B26	USBOC7#	W29	VCC15VL	J28	VCCA33PE
AK30	PDD11	AG23	SDD13	D23	USBP0-	W30	VCC15VL	D30	VCCA33PE1
AH28	PDD12	AJ24	SDD14	E23	USBP0+	Y25	VCC15VL	D25	VCCA33PLLUSB
AH30	PDD13	AK25	SDD15	B23	USBP1-	Y26	VCC15VL	AC12	VCCA33SATA
AG29	PDD14	AE23	SDDACK#	A23	USBP1+	Y27	VCC15VL	AC13	VCCA33SATA
AF28	PDD15	AJ25	SDDREQ	D21	USBP2-	Y28	VCC15VL	AC18	VCCA33SATA
AE27	PDDACK#	AK26	SDIOR#	E21	USBP2+	Y29	VCC15VL	AC19	VCCA33SATA
AF29	PDDREQ	AH26	SDIORDY	B21	USBP3-	AA10	VCC33	AK14	VCCA33SPLL
AD26	PDIOR#	AH25	SDIOW#	A21	USBP3+	AA11	VCC33	V27	VCLK
AE26	PDIORDY	C14	SEECK	E19	USBP4-	AA12	VCC33	P29	VD0
AD27	PDIOW#	A13	SEECS	D19	USBP4+	AA13	VCC33	N29	VD1
E28	PECLK-	B14	SEEDI	B19	USBP5-	AA18	VCC33	T29	VD2
E29	PECLK+	A14	SEEDO	A19	USBP5+	AA19	VCC33	T28	VD3
K26	PECOMP	AK03	SERIRQ	E17	USBP6-	AA20	VCC33	N27	VD4
J26	PEREXT	J04	SERR#	D17	USBP6+	AA21	VCC33	N28	VD5
G03	PERR#	AC30	SLP#	B17	USBP7-	K10	VCC33	U29	VD6
G29	PERX1-	AA02	SMBALRT#	A17	USBP7+	K11	VCC33	T27	VD7
G30	PERX1+	AB03	SMBCK1	C25	USBREXT	K12	VCC33	M28	VD8
F27	PERX2-	AB01	SMBCK2	AE03	VBAT	K13	VCC33	M27	VD9
F28	PERX2+	AA01	SMBDT1	P28	VBE#	L10	VCC33	U26	VD10
H28	PETX1-	AC03	SMBDT2	K20	VCC15	M10	VCC33	V30	VD11
H29	PETX1+	AB29	SMI#	L11	VCC15	N10	VCC33	L29	VD12
F30	PETX2-	AJ03	SPKR	L12	VCC15	P10	VCC33	L28	VD13
F29	PETX2+	AG14	SREXT	L13	VCC15	R10	VCC33	V29	VD14
D11	PHYPWRDN#	AK16	SRX1-	L14	VCC15	T10	VCC33	V28	VD15
C11	PHYRESET#	AJ16	SRX1+	L15	VCC15	U10	VCC33	AK05	VGATE
W04	PME#	AK18	SRX2-	L20	VCC15	U21	VCC33	AG07	VIDSEL
AC01	PWRBTN#	AJ18	SRX2+	M11	VCC15	V10	VCC33	M26	VLCOMPP
AE04	PWRGD	AK10	SRX3-	M20	VCC15	V21	VCC33	P25	VLVREF
AD04	PWROK	AJ10	SRX3+	N11	VCC15	W10	VCC33	M29	VPAR
B06	REQ0#	AK12	SRX4-	N20	VCC15	W21	VCC33	AJ05	VRDSLP
A07	REQ1#	AJ12	SRX4+	P11	VCC15	Y10	VCC33	T05	VSUS15
C06	REQ2#	G02	STOP#	P20	VCC15	Y21	VCC33	U05	VSUS15
D05	REQ3#	AC29	STPCLK#	R11	VCC15	E12	VCC33MII	K14	VSUS15MII
N01	REQ4#	AG16	STX1-	R20	VCC15	E13	VCC33MII	K15	VSUS15MII
N04	REQ5#	AF16	STX1+	T11	VCC15	E14	VCC33MII	J25	VSUS15PE
P01	REQ6#	AG18	STX2-	T20	VCC15	F13	VCC33MII	D27	VSUS15USB
Y01	RING#	AF18	STX2+	U11	VCC15	F14	VCC33MII	F16	VSUS15USB
AE05	RSMRST#	AG10	STX3-	U20	VCC15	G25	VCC33PE	AA05	VSUS33
AE02	RTCX1	AF10	STX3+	V11	VCC15	G26	VCC33PE	AB05	VSUS33
AE01	RTCX2	AG12	STX4-	V20	VCC15	G27	VCC33PE	V05	VSUS33
AG06	SAGP1	AF12	STX4+	W11	VCC15	H25	VCC33PE	W05	VSUS33
AH06	SAGP2	Y03	SUSA#	W20	VCC15	H26	VCC33PE	Y05	VSUS33
AJ06	SAGP3	AC02	SUSB#	Y11	VCC15	K25	VCC33PE	AG05	WAKE#

PIN DESCRIPTIONS

V-Link Pin Descriptions

V-Link Interface				
Signal Name	Pin #	I/O	Signal Description	Power Plane
VD[15:0]	(see pin list)	IO	Data Bus. All bits 15-0 are implemented for use with VIA North Bridge chips which support this capability (if not, only bits 7-0 are used). VD[7:0] are also used to send strap information to the chipset North Bridge (see strap table below for details). The specific interpretation of these straps is North Bridge chip design dependent.	VCC15VL
VPAR	M29	IO	Parity. If the VPAR function is implemented in a compatible manner on the North Bridge, this pin should be connected to the North Bridge VPAR pin (KT400 / KM400 / KN400, PT400, PT600). If VPAR is not implemented in the North Bridge chip or is incompatible with the VT8251 (4x V-Link North Bridges) connect this pin to an 8.2K pullup to 2.5V (Pro266, Pro266T, KT266, KT266A, KT333, P4X266, PN266, KN266, KM266, P4M266, P4N266). See app note AN222 for details.	VCC15VL
VBE#	P28	IO	Byte Enable. Connect to same named pin on North Bridge.	VCC15VL
VCLK	V27	I	V-Link Clock. 66 MHz. Supplied by clock generator.	VCC33
UPCMD	U28	O	Command from Client-to-Host. Connect to same named pin on North Bridge.	VCC15VL
DNCMD	T26	I	Command from Host-to-Client. Connect to same named pin on North Bridge.	VCC15VL
UPSTB+	R28	O	Strobe from Client-to-Host. Connect to same named pin on North Bridge.	VCC15VL
UPSTB-	R29	O	Complement Strobe from Client-to-Host. Connect to same named pin on North Bridge.	VCC15VL
DNSTB+	R26	I	Strobe from Host-to-Client. Connect to same named pin on North Bridge.	VCC15VL
DNSTB-	R27	I	Complement Strobe from Host-to-Client. Connect to same named pin on North Bridge.	VCC15VL

CPU, CPU Control and APIC Pin Descriptions

CPU Interface				
Signal Name	Pin #	I/O	Signal Description	Power Plane
A20M#	AC28	OD	A20 Mask. Connect to A20 mask input of the CPU to control address bit-20 generation. Logical combination of the A20GATE input (from internal or external keyboard controller) and Port 92 bit-1 (Fast A20).	VCC33
FERR#	AB28	I	Numerical Coprocessor Error. This signal is tied to the coprocessor error signal on the CPU. Internally generates interrupt 13 if active.	VCC33
IGNNE#	AD30	OD	Ignore Numeric Error. This pin is connected to the CPU “ignore error” pin.	VCC33
INIT#	AA26	OD	Initialization. The VT8251 asserts INIT# if it detects a shutdown special cycle on the PCI bus or if a soft reset is initiated by the register	VCC33
INTR	AA25	OD	CPU Interrupt. INTR is driven by the VT8251 to signal the CPU that an interrupt request is pending and needs service.	VCC33
NMI	AB30	OD	Non-Maskable Interrupt. NMI is used to force a non-maskable interrupt to the CPU. The VT8251 generates an NMI when PCI bus SERR# is asserted.	VCC33
SLP#	AC30	OD	Sleep. Used to put the CPU into a sleep state.	VCC33
SMI#	AB29	OD	System Management Interrupt. SMI# is asserted by the VT8251 to the CPU in response to different Power-Management events.	VCC33
STPCLK#	AC29	OD	Stop Clock. This signal is asserted by the VT8251 to throttle the processor clock.	VCC33
THRMTrip#	AD29	I	Thermal Detect Power Down. This signal is to indicate a thermal trip from the processor.	VCC33

Note: Connect each of the above signals to 150 Ω pullup resistors to VCC_CMOS (see Design Guide).

CPU Speed Control Interface				
Signal Name	Pin #	I/O	Signal Description	Power Plane
VGATE / GPI8 / GPO8	AK05	I	Voltage Gate. Signal from the CPU voltage regulator. High indicates the voltage regulator output is stable. VGATE can optionally be used as GPI8 and GPO8.	VCC33
VIDSEL / GPO28	AG07	OD	Voltage Regulator ID Select. Connected to the CPU voltage regulator. Low selects the voltage ID from the CPU; high selects a different fixed voltage ID (the lower voltage used for CPU deep sleep mode). VIDSEL can optionally be used as GPO28.	VCC33
VRDSLP / GPO29	AJ05	OD	Voltage Regulator Deep Sleep. Connected to the CPU voltage regulator. High selects the proper voltage for deep sleep mode. VRDSLP can optionally be used as GPO29.	VCC33
GHI# / GPO22	Y30	OD	CPU Speed Select. Connected to the CPU voltage regulator, used to select high speed or low speed. GHI# can optionally be used as GPO22.	VCC33
DPSLP# / GPO23	AA29	OD	CPU Deep Sleep. DPSLP# can optionally be used as GPO23.	VCC33
CPUMISS / GPI17 / SACSDIN0	W02	I	CPU Missing. Used to detect the physical presence of the CPU chip in its socket. High indicates no CPU present. Connect to the CPUMISS pin of the CPU socket. The state of this pin may be read in the SMBus 2 registers. CPUMISS can optionally be used as GPI17. SACSDIN0 is multiplexed with this pin.	VSUS33
AGPBZ# / GPI6	AK04	I	AGP Busy. Low indicates that an AGP master cycle is in progress (CPU speed transitions will be postponed if this input is asserted low). Connected to the AGP Bus AGPBZ# pin. AGPBZ# can optionally be used as GPI16.	VCC33

Advanced Programmable Interrupt Controller (APIC) Interface				
Signal Name	Pin #	I/O	Signal Description	Power Plane
APICD1 / GPIO11	AA28	O	Internal APIC Data 1.	VCC33
APICD0 / GPIO10	AA27	O	Internal APIC Data 0.	VCC33
APICCLK / GPI19	AD28	I	Internal APIC Clock.	VCC33

PCI Express Pin Descriptions

PCI Express Interface				
Signal Name	Pin #	I/O	Signal Description	Power Plane
PERX2+ PERX2-	F28 F27	I	PCI Express Receive Data 2.	VCC33PE
PERX1+ PERX1-	G30 G29	I	PCI Express Receive Data 1.	VCC33PE
PETX2+ PETX2-	F29 F30	O	PCI Express Transmit Data 2.	VCC33PE
PETX1+ PETX1-	H29 H28	O	PCI Express Transmit Data 1.	VCC33PE
PECLK+ PECLK-	E29 E28	I	PCI Express Clock. These pins receive the 100 MHz clock used by the internal PCI Express logic. Multiplied up to 2.5 GHz on-chip for use by the integrated PCI Express PHY to transmit / receive data.	VCC33PE

PCI Bus Pin Descriptions

PCI Bus Interface				
Signal Name	Pin #	I/O	Signal Description	Power Plane
AD[31:0]	(see pin list)	IO	Address / Data Bus. Multiplexed address and data. The address is driven with FRAME# assertion and data is driven or received in following cycles.	VCC33
CBE[3:0]#	C01, F01, H01, L03	IO	Command / Byte Enable. The command is driven with FRAME# assertion. Byte enables corresponding to supplied or requested data are driven on following clocks.	VCC33
DEVSEL#	G01	IO	Device Select. The VT8251 asserts this signal to claim PCI transactions through positive or subtractive decoding. As an input, DEVSEL# indicates the response to a VT8251-initiated transaction and is also sampled when decoding whether to subtractively decode the cycle.	VCC33
FRAME#	F02	IO	Frame. Assertion indicates the address phase of a PCI transfer. Negation indicates that one more data transfer is desired by the cycle initiator.	VCC33
IRDY#	F03	IO	Initiator Ready. Asserted when the initiator is ready for data transfer.	VCC33
TRDY#	G04	IO	Target Ready. Asserted when the target is ready for data transfer.	VCC33
STOP#	G02	IO	Stop. Asserted by the target to request the master to stop the current transaction.	VCC33
SERR#	J04	I	System Error. SERR# can be pulsed active by any PCI device that detects a system error condition. Upon sampling SERR# active, the VT8251 can be programmed to generate an NMI to the CPU.	VCC33
PERR#	G03	-	Parity Error. PERR#, sustained tri-state, is only for the reporting of data parity errors during all PCI transactions except a Special Cycle.	VCC33
PAR	H03	IO	Parity. A single parity bit is provided over AD[31:0] and C/BE[3:0]#.	VCC33
INTA# INTB# INTC# INTD# INTE#/GPI32	A05 B05 D06 C05 P03	I	PCI Interrupt Request. The INTA# through INTD# pins are typically connected to the PCI bus INTA#/INTD# pins per the table below. BIOS settings must match the physical connection method.	VCC33
INTF#/GPI33	P02		INTA# INTB# INTC# INTD# PCI Slot 1 INTA# INTB# INTC# INTD# PCI Slot 2 INTB# INTC# INTD# INTE# PCI Slot 3 INTC# INTD# INTE# INTF#	
INTG#/GPI34	R03		PCI Slot 4 INTD# INTE# INTF# INTG# PCI Slot 5 INTE# INTF# INTG# INTH# PCI Slot 6 INTF# INTG# INTH# INTA#	
INTH#/GPI35	R04			

PCI Bus Interface (continued)				
Signal Name	Pin #	I/O	Signal Description	Power Plane
REQ6# / GPI16 REQ5# / GPI7, REQ4#, REQ3#, REQ2#, REQ1#, REQ0#	P01 N04 N01 D05 C06 C07 A07 B06	I	PCI Request. These signals connect to the VT8251 from each PCI slot (or each PCI master) to request the PCI bus. REQ6# can optionally be used as GPI16. REQ5# can optionally be used as GPI7.	VCC33
GMT6# / GPO20 GMT5# / GPO7, GMT4#, GMT3#, GMT2#, GMT1#, GMT0#	P04 N03 N02 C04 C07 A06 B07	O	PCI Grant. These signals are driven by the VT8251 to grant PCI access to a specific PCI master. GMT6# can optionally be used as GPO20. GMT5# can optionally be used as GPO7.	VCC33
PCIRST#	T04	O	PCI Reset. This signal is used to reset devices attached to the PCI bus.	VSUS33
PCICLK	AE28	I	PCI Clock. This signal provides timing for all transactions on the PCI Bus.	VCC33
CLKRUN#	AJ01	IO	PCI Bus Clock Run. This signal indicates whether the PCI clock is or will be stopped (high) or running (low). The VT8251 drives this signal low when the PCI clock is running (default on reset) and releases it when it stops the PCI clock. External devices may assert this signal low to request that the PCI clock be restarted or prevent it from stopping. Connect this pin to ground using a 100 Ω resistor if the function is not used.	VCC33

MII, Serial EEPROM and Low Pin Count Pin Descriptions

LAN Controller - Media Independent Interface (MII)					
Signal Name	Pin #	I/O	PU	Signal Description	Power Plane
CLK25O	B13	O	-	Provided a 25MHz Clock to External PHY.	VCC33MII
MCOL	E10	I	PD	MII Collision Detect. From the external PHY.	VCC33MII
MCRS	D10	I	PD	MII Carrier Sense. Asserted by the external PHY when the media is active.	VCC33MII
MDC	D09	O	PD	MII Management Data Clock. Sent to the external PHY as a timing reference for MDIO	VCC33MII
MDIO	E09	IO	PU	MII Management Data I/O. Read from the MDI bit or written to the MDO bit.	VCC33MII
MRXC	C10	I	PD	MII Receive Clock. 2.5 or 25 MHz clock recovered by the PHY.	VCC33MII
MRXD[3-0]	D08, C08, A08, B08	I	PD	MII Receive Data. Parallel receive data lines driven by the external PHY synchronous with MRXC.	VCC33MII
MRXDV	A09	I	PD	MII Receive Data Valid.	VCC33MII
MRXER	C09	I	PD	MII Receive Error. Asserted by the PHY when it detects a data decoding error.	VCC33MII
MTXC	A10	I	PD	MII Transmit Clock. Always active 2.5 or 25 MHz clock supplied by the PHY.	VCC33MII
MTXD[3-0]	A11, D12, C12, A12	O	PD	MII Transmit Data. Parallel transmit data lines synchronized to MTXC.	VCC33MII
MTXEN	B11	O	PD	MII Transmit Enable. Signals that transmit is active from the MII port to the PHY.	VCC33MII
PHYRESET#	C11	O	-	External PHY Reset.	VCC33MII
PHYPWRDN#	D11	O	-	PHY Power Down. Output when PHY is in power state as D1 hot, D2 hot or D3 hot with no PME and WOL enable.	VCC33MII

Serial EEPROM Interface				
Signal Name	Pin #	I/O	Signal Description	Power Plane
SEECS	A13	O	Serial EEPROM Chip Select.	VCC33MII
SEECK	C14	O	Serial EEPROM Clock.	VCC33MII
SEEDO	A14	I	Serial EEPROM Data Output. Connect to EEPROM Data Out pin.	VCC33MII
SEEDI	B14	O	Serial EEPROM Data Input. Connect to EEPROM Data In pin.	VCC33MII

The serial EEPROM Interface signals are disabled if the SEEDI pin is strapped high.

Low Pin Count (LPC) Interface					
Signal Name	Pin #	I/O	PU	Signal Description	Power Plane
LPCAD[3-0]	AK01, AJ02, AK02, AH03	IO	PU	LPC Address / Data.	VCC33
LPCFRAME#	AH01	O	-	LPC Frame.	VCC33
LPCDRQ0#	AG01	I	-	LPC DMA / Bus Master Request 0.	VCC33
LPCDRQ1#	AG04	I	-	LPC DMA / Bus Master Request 1.	VCC33

Note: Connect the LPC interface LPCRST# (LPC Reset) signal to PCIRST#

USB and SMB Pin Descriptions

Universal Serial Bus 2.0 Interface				
Signal Name	Pin #	I/O	Signal Description	Power Plane
USBP0+	E23	IO	USB 2.0 Port 0 Data +	VCC33USB
USBP0-	D23	IO	USB 2.0 Port 0 Data -	VCC33USB
USBP1+	A23	IO	USB 2.0 Port 1 Data +	VCC33USB
USBP1-	B23	IO	USB 2.0 Port 1 Data -	VCC33USB
USBP2+	E21	IO	USB 2.0 Port 2 Data +	VCC33USB
USBP2-	D21	IO	USB 2.0 Port 2 Data -	VCC33USB
USBP3+	A21	IO	USB 2.0 Port 3 Data +	VCC33USB
USBP3-	B21	IO	USB 2.0 Port 3 Data -	VCC33USB
USBP4+	D19	IO	USB 2.0 Port 4 Data +	VCC33USB
USBP4-	E19	IO	USB 2.0 Port 4 Data -	VCC33USB
USBP5+	A19	IO	USB 2.0 Port 5 Data +	VCC33USB
USBP5-	B19	IO	USB 2.0 Port 5 Data -	VCC33USB
USBP6+	D17	IO	USB 2.0 Port 6 Data +	VCC33USB
USBP6-	E17	IO	USB 2.0 Port 6 Data -	VCC33USB
USBP7+	A17	IO	USB 2.0 Port 7 Data +	VCC33USB
USBP7-	B17	IO	USB 2.0 Port 7 Data -	VCC33USB
USBCLK	E26	I	USB 2.0 Clock. 48 MHz clock input for the USB interface	VCC33USB
USBREXT	C25	AI	USB External Resistor	VCC33USB
USBOC0#	A28	I	USB 2.0 Port 0 Over Current Detect. Port 0 is disabled if low.	VCC33USB
USBOC1#	A29	I	USB 2.0 Port 1 Over Current Detect. Port 1 is disabled if low.	VCC33USB
USBOC2#	A27	I	USB 2.0 Port 2 Over Current Detect. Port 2 is disabled if low.	VCC33USB
USBOC3#	B27	I	USB 2.0 Port 3 Over Current Detect. Port 3 is disabled if low.	VCC33USB
USBOC4# / GPI36	A25	I	USB 2.0 Port 4 Over Current Detect. Port 4 is disabled if low.	VCC33USB
USBOC5# / GPI37	B25	I	USB 2.0 Port 5 Over Current Detect. Port 5 is disabled if low.	VCC33USB
USBOC6# / GPI38	A26	I	USB 2.0 Port 6 Over Current Detect. Port 6 is disabled if low.	VCC33USB
USBOC7# / GPI39	B26	I	USB 2.0 Port 7 Over Current Detect. Port 7 is disabled if low.	VCC33USB

System Management Bus (SMB) Interface (I ² C Bus)				
Signal Name	Pin #	I/O	Signal Description	Power Plane
SMBCK1	AB03	OD	SMB / I²C Channel 1 Clock.	VSUS33
SMBCK2 / GPI27 / GPO27	AB01	OD	SMB / I²C Channel 2 Clock. SMBCK2 can optionally be used as GPI27 and GPO27.	VSUS33
SMBDT1	AA01	OD	SMB / I²C Channel 1 Data.	VSUS33
SMBDT2 / GPI26 / GPO26	AC03	OD	SMB / I²C Channel 2 Data. SMBDT2 can optionally be used as GPI26 and GPO26.	VSUS33
SMBALRT#	AA02	I	SMB Alert. Enabled by System Management Bus I/O space. When the chip is enabled to allow it, assertion generates an IRQ or SMI interrupt or a power management resume event. Connect to a 10K ohm pullup to VSUS33 if not used.	VSUS33

Enhanced IDE Interface Pin Descriptions

UltraDMA-133 / 100 / 66 / 33 Enhanced IDE Interface				
Signal Name	Pin #	I/O	Signal Description	Power Plane
PDIORDY / PDDMARDY / PDSTROBE	AE26	I	EIDE Mode: Primary I/O Channel Ready. Device ready indicator UltraDMA Mode: Primary Device DMA Ready. Output flow control. The device may assert DDMARDY to pause output transfers Primary Device Strobe. Input data strobe (both edges). The device may stop DSTROBE to pause input data transfers	VCC33
SDIORDY / SDDMARDY / SDSTROBE	AH26	I	EIDE Mode: Secondary I/O Channel Ready. Device ready indicator UltraDMA Mode: Secondary Device DMA Ready. Output flow control. The device may assert DDMARDY to pause output transfers Secondary Device Strobe. Input data strobe (both edges). The device may stop DSTROBE to pause input data transfers	VCC33
PDIOR# / PHDMARDY / PHSTROBE	AD26	O	EIDE Mode: Primary Device I/O Read. Device read strobe UltraDMA Mode: Primary Host DMA Ready. Primary channel input flow control. The host may assert HDMARDY to pause input transfers Primary Host Strobe. Output data strobe (both edges). The host may stop HSTROBE to pause output data transfers	VCC33
SDIOR# / SHDMARDY / SHSTROBE	AK26	O	EIDE Mode: Secondary Device I/O Read. Device read strobe UltraDMA Mode: Secondary Host DMA Ready. Input flow control. The host may assert HDMARDY to pause input transfers Secondary Host Strobe. Output strobe (both edges). The host may stop HSTROBE to pause output data transfers	VCC33
PDIOW# / PSTOP	AD27	O	EIDE Mode: Primary Device I/O Write. Device write strobe UltraDMA Mode: Primary Stop. Stop transfer: Asserted by the host prior to initiation of an UltraDMA burst; negated by the host before data is transferred in an UltraDMA burst. Assertion of STOP by the host during or after data transfer in UltraDMA mode signals the termination of the burst.	VCC33
SDIOW# / SSTOP	AH25	O	EIDE Mode: Secondary Device I/O Write. Device write strobe UltraDMA Mode: Secondary Stop. Stop transfer: Asserted by the host prior to initiation of an UltraDMA burst; negated by the host before data is transferred in an UltraDMA burst. Assertion of STOP by the host during or after data transfer in UltraDMA mode signals the termination of the burst.	VCC33
PDDREQ	AF29	I	Primary Device DMA Request. Primary channel DMA request	VCC33
SDDREQ	AJ25	I	Secondary Device DMA Request. Secondary channel DMA request	VCC33
PDDACK#	AE27	O	Primary Device DMA Acknowledge. Primary channel DMA acknowledge	VCC33
SDDACK#	AE23	O	Secondary Device DMA Acknowledge. Secondary channel DMA acknowledge	VCC33
IRQ14	AE30	I	Primary Channel Interrupt Request.	VCC33
IRQ15	AG24	I	Secondary Channel Interrupt Request.	VCC33

UltraDMA-133 / 100 / 66 / 33 Enhanced IDE Interface (continued)				
Signal Name	Pin #	I/O	Signal Description	Power Plane
PDCS1#	AC25	O	Primary Master Chip Select. This signal corresponds to CS1FX# on the primary IDE connector.	VCC33
PDCS3#	AC26	O	Primary Slave Chip Select. This signal corresponds to CS3FX# on the primary IDE connector.	VCC33
SDCS1#	AG26	O	Secondary Master Chip Select. This signal corresponds to CS17X# on the secondary IDE connector.	VCC33
SDCS3#	AK27	O	Secondary Slave Chip Select. This signal corresponds to CS37X# on the secondary IDE connector.	VCC33
PDA[2-0]	AB26, AE29, AB27	O	Primary Disk Address. PDA[2:0] are used to indicate which byte in either the ATA command block or control block is being accessed. Strap information is communicated to the North Bridge via VD[6:4].	VCC33
SDA[2-0]	AF25, AE24, AG25	O	Secondary Disk Address. SDA[2:0] are used to indicate which byte in either the ATA command block or control block is being accessed.	VCC33
PDD[15-0]	(see pin list)	IO	Primary Disk Data.	VCC33
SDD[15-0]	(see pin list)	IO	Secondary Disk Data.	VCC33

Serial ATA Pin Descriptions

Serial ATA Interface				
Signal Name	Pin #	I/O	Signal Description	Power Plane
SRX1+	AJ16	I	SATA Port 1 Receive +	VCCA33SATA
SRX1-	AK16	I	SATA Port 1 Receive -	VCCA33SATA
SRX2+	AJ18	I	SATA Port 2 Receive +	VCCA33SATA
SRX2-	AK18	I	SATA Port 2 Receive -	VCCA33SATA
SRX3+	AJ10	I	SATA Port 3 Receive +	VCCA33SATA
SRX3-	AK10	I	SATA Port 3 Receive -	VCCA33SATA
SRX4+	AJ12	I	SATA Port 4 Receive +	VCCA33SATA
SRX4-	AK12	I	SATA Port 4 Receive -	VCCA33SATA
STX1+	AF16	I	SATA Port 1 Transmit +	VCCA33SATA
STX1-	AG16	I	SATA Port 1 Transmit -	VCCA33SATA
STX2+	AF18	I	SATA Port 2 Transmit +	VCCA33SATA
STX2-	AG18	I	SATA Port 2 Transmit -	VCCA33SATA
STX3+	AF10	I	SATA Port 3 Transmit +	VCCA33SATA
STX3-	AG10	I	SATA Port 3 Transmit -	VCCA33SATA
STX4+	AF12	I	SATA Port 4 Transmit +	VCCA33SATA
STX4-	AG12	I	SATA Port 4 Transmit -	VCCA33SATA
SAGP1 / GPI22	AG06	I	SATA Interlock Switch Status. Input driving high level to indicate that an interlock switch attached to the port has been open or closed. SAGP[4:1] can optionally be used as GPIOs.	VCC33
SAGP2 / GPI23	AH06	I		
SAGP3 / GPI28	AJ06	I		
SAGP4 / GPI29	AK06	I		
SXI	AK08	I	SATA Crystal In.	VCC15OSC
SXO	AJ08	O	SATA Crystal Out.	VCC15OSC
SREXT	AG14	AI	SATA External Resistor.	VCCA33SATA
SATALED#	AH07	O	SATA LED.	VCC33

High Definition (HD) Audio / AC'97 Audio and Modem Pin Descriptions

Primary Audio Interface (for HD Audio / AC97 Audio)					
Signal Name	Pin #	I/O	High Definition Audio Signal Description	AC97 Signal Description	Power Plane
ACRST#	R01	O	High Definition Audio Reset.	AC97 Reset.	VSUS33
ACBITCLK	T01	I	High Definition Audio Bit Clock. 24.00 MHz.	AC97 Bit Clock. 12.288MHz.	VCC33
ACSYNC	U02	O	High Definition Audio Sync. 48 KHz Frame Sync and outbound tag signal.	AC97 Sync. 48KHz Sync Pulse.	VCC33
ACSDOUT0	T03	O	High Definition Audio Serial Data Output 0. Bussed serial data output signal 0.	AC97 Serial Data Output 0.	VCC33
ACSDOUT1 / GPO21 / SACSDOUT	U03	O	-	AC97 Serial Data Output 1.	VCC33
ACSDIN0	R02	I	High Definition Audio Serial Data Input 0. Point-to-point serial data input signal 0.	AC97 Serial Data Input 0.	VSUS33
ACSDIN1	T02	I	High Definition Audio Serial Data Input 1. Point-to-point serial data input signal 1.	AC97 Serial Data Input 1.	VSUS33
ACSDIN2 / PCS0# / GPI20	U04	I	High Definition Audio Serial Data Input 2. Point-to-point serial data input signal 2.	AC97 Serial Data Input 2.	VSUS33
			ACSDIN2 is multiplexed with PCS0#. ACSDIN2 can optionally be used as GPI20.		
ACSDIN3 / PCS1# / GPI21	U01	I	High Definition Audio Serial Data Input 3 Point-to-point serial data input signal 3.	AC97 Serial Data Input 3.	VSUS33
			ACSDIN3 is multiplexed with this pin PCS1#. ACSDIN3 can optionally be used as GPI21.		

Note: The supply voltage for ACSDIN0-1 is VSUS33 so these inputs can support wake-up on modem ring.

Secondary Audio Interface (for AC97 Audio / Modem)				
Signal Name	Pin #	I/O	AC97 Signal Description	Power Plane
SACRST# / GPIO12 / GPIOE	AF04	O	AC97 Reset.	VSUS33
SACBITCLK / GPIO13 / GPIOF	AF05	I	AC97 Bit Clock. 12.288MHz.	VSUS33
SACSYNC / GPIO14 / GPIOG	AE06	O	AC97 Sync. 48KHz Sync Pulse.	VSUS33
SACSDIN0 / GPI17 / CPUMISS	W02	I	AC97 Serial Data Input 0.	VSUS33
SACSDOUT / GPO21 / ACSDOUT1	U03	O	AC97 Serial Data Output.	VCC33

Note: 1. When the primary audio interface is implemented as HD audio interface, the secondary audio interface can be implemented as AC97 audio interface.

2. When the primary audio interface is implemented as AC97 audio interface, the secondary audio interface can be implemented as MC97 modem interface.

Serial IRQ and PC / PCI DMA Pin Descriptions

Serial IRQ				
Signal Name	Pin #	I/O	Signal Description	Power Plane
SERIRQ	AK03	I	Serial IRQ. This pin has an external pull-up resistor.	VCC33

PC / PCI DMA Pin Descriptions

PC / PCI DMA				
Signal Name	Pin #	I/O	Signal Description	Power Plane
PCREQA / GPIOA24 / GPO24 (GPIOA)	AG02	I	PC / PCI Request A. It can be used as GPIOs if not needed for Request A.	VCC33
PCREQB / GPIOB25 / GPO25 (GPIOB)	AF01	I	PC / PCI Request B. It can be used as GPIOs if not needed for Request B.	VCC33
PCGNTA / GPIOC30 / GPO30 (GPIOC)	AG03	O	PC / PCI Grant A. It can be used as GPIOs if not needed for Grant A.	VCC33
PCGNTB / GPIOD31 / GPO31 (GPIOD)	AF03	O	PC / PCI Grant B. It can be used as GPIOs if not needed for Grant B.	VCC33

Internal Keyboard Controller and Speaker Pin Descriptions

Internal Keyboard Controller					
Signal Name	Pin #	I/O	PU	Signal Description	Power Plane
MSCK	W01	IO	PU	Mouse Clock. From internal mouse controller.	VSUS33
MSDT	V03	IO	PU	Mouse Data. From internal mouse controller.	VSUS33
KBCK	V02	IO	PU	Keyboard Clock. From internal keyboard controller.	VSUS33
KBDT	V01	IO	PU	Keyboard Data. From internal keyboard controller.	VSUS33

Speaker Interface

Speaker				
Signal Name	Pin #	I/O	Signal Description	Power Plane
SPKR	AJ03	O	Speaker. Strap low to enable (high to disable) CPU frequency strapping.	VCC33

Programming Chip Selects Pin Descriptions

Programmable Chip Selects				
Signal Name	Pin #	I/O	Signal Description	Power Plane
PCS0# / ACSDIN2 / GPIO20	U04	O	Programmable Chip Select 0. ACSDIN2 is multiplexed with this pin. PCS0# can optionally be used as GPIO20.	VSUS33
PCS1# / ACSDIN3 / GPIO21	U01	O	Programmable Chip Select 1. ACSDIN3 is multiplexed with this pin. PCS1# can optionally be used as GPIO21.	VSUS33

General Purpose Inputs Pin Descriptions

General Purpose Inputs				
Signal Name	Pin #	I/O	Signal Description	Power Plane
GPI0	AD02	I	General Purpose Input 0.	VBAT
GPI1	AB04	I	General Purpose Input 1.	VSUS33
GPI2 / EXTSMI#	Y02	I	General Purpose Input 2.	VSUS33
GPI3 / RING#	Y01	I	General Purpose Input 3.	VSUS33
GPI4 / LID#	AB02	I	General Purpose Input 4.	VSUS33
GPI5 / BATLOW#	V04	I	General Purpose Input 5.	VSUS33
GPI6 / AGPBZ#	AK04	I	General Purpose Input 6.	VCC33
GPI7 / REQ5#	N04	I	General Purpose Input 7.	VCC33
GPI8 / GPO8 / VGATE	AK05	I	General Purpose Input 8.	VCC33
GPI9	C28	I	General Purpose Input 9.	VCC33USB
GPI16 / REQ6#	P01	I	General Purpose Input 16.	VCC33
GPI17 / CPUMISS / SACSDIN0	W02	I	General Purpose Input 17.	VSUS33
GPI18 / THRM# / AOLGPI	Y04	I	General Purpose Input 18.	VSUS33
GPI19 / APICLK	AD28	I	General Purpose Input 19.	VCC33
GPI20 / ACSDIN2 / PCS0#	U04	I	General Purpose Input 20.	VSUS33
GPI21 / ACSDIN3 / PCS1#	U01	I	General Purpose Input 21.	VSUS33
GPI22 / SAGP1	AG06	I	General Purpose Input 22.	VCC33
GPI23 / SAGP2	AH06	I	General Purpose Input 23.	VCC33
GPI28 / SAGP3	AJ06	I	General Purpose Input 28.	VCC33
GPI29 / SAGP4	AK06	I	General Purpose Input 29.	VCC33
GPI32 / INTE#	P03	I	General Purpose Input 32.	VCC33
GPI33 / INTF#	P02	I	General Purpose Input 33.	VCC33
GPI34 / INTG#	R03	I	General Purpose Input 34.	VCC33
GPI35 / INTH#	R04	I	General Purpose Input 35.	VCC33
GPI36 / USBOC4#	A25	I	General Purpose Input 36.	VCC33USB
GPI37 / USBOC5#	B25	I	General Purpose Input 37.	VCC33USB
GPI38 / USBOC6#	A26	I	General Purpose Input 38.	VCC33USB
GPI39 / USBOC7#	B26	I	General Purpose Input 39.	VCC33USB

General Purpose Outputs Pin Descriptions

General Purpose Outputs				
Signal Name	Pin #	I/O	Signal Description	Power Plane
GPO0	AA04	O	General Purpose Output 0.	VSUS33
GPO1	AD03	O	General Purpose Output 1.	VSUS33
GPO2 / SUSA#	Y03	O	General Purpose Output 2.	VSUS33
GPO3 / SUSST#	W03	O	General Purpose Output 3.	VSUS33
GPO4 / SUSCLK	AA03	O	General Purpose Output 4.	VSUS33
GPO5 / CPUSTP#	AH02	O	General Purpose Output 5.	VCC33
GPO6 / PCIISTP#	AF02	O	General Purpose Output 6.	VCC33
GPO7 / GNT5#	N03	O	General Purpose Output 7.	VCC33
GPO8 / GPI8 / VGATE	AK05	O	General Purpose Output 8.	VCC33
GPO9	B28	O	General Purpose Output 9.	VCC33USB
GPO20 / GNT6#	P04	OD	General Purpose Output 20.	VCC33
GPO21 / ACSDOUT1/ SACSDOUT	U03	OD	General Purpose Output 21.	VCC33
GPO22 / GHI#	Y30	OD	General Purpose Output 22.	VCC33
GPO23 / DPSLP#	AA29	OD	General Purpose Output 23.	VCC33
GPO28 / VIDSEL	AG07	OD	General Purpose Output 28.	VCC33
GPO29 / VRDSL	AJ05	OD	General Purpose Output 29.	VCC33

General Purpose Inputs / Outputs Pin Descriptions

General Purpose I/O				
Signal Name	Pin #	I/O	Signal Description	Power Plane
GPIO10 / APICD0	AA27	IO	General Purpose I/O 10.	VCC33
GPIO11 / APICD1	AA28	IO	General Purpose I/O 11.	VCC33
GPIO12 / GPIOE / SACRST#	AF04	IO	General Purpose I/O E / 12.	VSUS33
GPIO13 / GPIOF / SACBITCLK	AF05	IO	General Purpose I/O F / 13.	VSUS33
GPIO14 / GPIOG / SACYNC	AE06	IO	General Purpose I/O G / 14.	VSUS33
GPIO15 / GPIOH	AF06	IO	General Purpose I/O H / 15.	VSUS33
GPIO24 / GPIOA / PCREQA	AG02	IO	General Purpose I/O A / 24.	VCC33
GPIO25 / GPIOB / PCREQB	AF01	IO	General Purpose I/O B / 25.	VCC33
GPIO26 / SMBDT2	AC03	IO	General Purpose I/O 26.	VSUS33
GPIO27 / SMBCK2	AB01	IO	General Purpose I/O 27.	VSUS33
GPIO30 / GPIOC / PCGNTA	AG03	IO	General Purpose I/O C / 30.	VCC33
GPIO31 / GPIOD / PCGNTB	AF03	IO	General Purpose I/O D / 31.	VCC33

Power Management and Event Pin Descriptions

Power Management and Event Detection				
Signal Name	Pin #	I/O	Signal Description	Power Plane
PWRBTN#	AC01	I	Power Button. Used by the Power Management subsystem to monitor an external system on/off button or switch. Internal logic powered by VSUS33.	VSUS33
SLPBTN# / VGATE GPI8 / GPO8	AK05	I	Sleep Button. Used by the Power Management subsystem to monitor an external sleep button or switch. VGATE is multiplexed with this pin.	VCC33
RSMRST#	AE05	I	Resume Reset. Resets the internal logic connected to the VSUS33 power plane and also resets portions of the internal RTC logic. Internal logic powered by VBAT.	VBAT
EXTSMI# / GPI2	Y02	IO	External System Management Interrupt. When enabled to allow it, a falling edge on this input causes an SMI# to be generated to the CPU to enter SMI mode. EXTSMI# can optionally be used as GPI2	VSUS33
PME#	W04	I	Power Management Event.	VSUS33
SMBALRT#	AA02	I	SMB Alert. When programmed to allow it, assertion generates an IRQ, SMI, or power management event.	VSUS33
LID# / GPI4	AB02	I	Notebook Computer Display Lid Open / Closed Monitor. Used by the Power Management subsystem to monitor the opening and closing of the display lid of notebook computers. Can be used to detect either low-to-high or high-to-low transitions to generate an SMI#. LID# can optionally be used as GPI4.	VSUS33
INTRUDER#	AD01	I	Intrusion Indicator.	VBAT
THRM# / GPI18 / AOLGPI	Y04	I	Thermal Alarm Monitor. This signal is to enable the throttling mode for the duty cycle control of stop clock. AOLGPI is multiplexed with this pin. THRM# can optionally be used as GPI18.	VSUS33
RING# / GPI3	Y01	I	Ring Indicator. May be connected to external modem circuitry to allow the system to be re-activated by a received phone call. RING# can optionally be used as GPI3.	VSUS33
BATLOW# / GPI5	V04	I	Battery Low Indicator. BATLOW# can optionally be used as GPI5.	VSUS33
WAKE#	AG05	I	For a Wakeup Event.	VSUS33
CPUSTP# / GPO5	AH02	O	CPU Clock Stop. Signals the system clock generator to disable the CPU clock outputs. Not connected if not used.	VCC33
PCISTP# / GPO6	AF02	O	PCI Clock Stop. Signals the system clock generator to disable the PCI clock outputs. Not connected if not used.	VCC33

Power Management and Event Detection				
Signal Name	Pin #	I/O	Signal Description	Power Plane
SUSA# / GPO2	Y03	O	Suspend Plane A Control. Asserted during power management POS, STR, and STD suspend states. Used to control the primary power plane.	VSUS33
SUSB#	AC02	O	Suspend Plane B Control. Asserted during power management STR and STD suspend states. Used to control the secondary power plane.	VSUS33
SUSC#	AC04	O	Suspend Plane C Control. Asserted during power management STD suspend state. Used to control the tertiary power plane. Also connected to ATX power-on circuitry.	VSUS33
SUSST# / GPO3	W03	O	Suspend Status 1. Typically connected to the North Bridge to provide information on host clock status. Asserted when the system may stop the host clock, such as Stop Clock or during POS, STR, or STD suspend states.	VSUS33
SUSCLK	AA03	O	Suspend Clock. 32.768 KHz output clock for use by the North Bridge for DRAM refresh purposes. Stopped during Suspend-to-Disk and Soft-Off modes.	VSUS33
CPUMISS / GPI17/ SACSDIN0	W02	I	CPU Missing. Used to detect the physical presence of the CPU chip in its socket. High indicates no CPU present. Connect to the CPUMISS pin of the CPU socket. The state of this pin may be read in the SMBus 2 registers. This pin may be used as CPUMISS and GPI17 at the same time.	VSUS33
AOLGPI / GPI18 / THRM#	Y04	I	Alert On LAN. The state of this pin may be read in the SMBus 2 registers. This pin may be used as AOLGPI, GPI18 and THRM# all at the same time.	VSUS33

Clocks, Resets and Power Status Pin Descriptions

Resets, Clocks and Power Status				
Signal Name	Pin #	I/O	Signal Description	Power Plane
PWRGD	AE04	I	Power Good. Connected to the Power Good signal on the Power Supply. Internal logic powered by VBAT.	VBAT
PWROK	AD04	O	Power OK. Internal logic powered by VSUS33.	VSUS33
PCIRST#	T04	O	PCI Reset. Active low reset signal for the PCI bus. The VT8251 will assert this pin during power-up or from the control register.	VSUS33
OSC	AH05	I	Oscillator. 14.31818 MHz clock signal used by the internal Timer.	VCC33
RTCX1	AE02	I	RTC Crystal Input: 32.768 KHz crystal or oscillator input. This input is used for the internal RTC and power-well power management logic and is powered by VBAT.	VBAT
RTCX2	AE01	O	RTC Crystal Output: 32.768 KHz crystal output. Internal logic powered by VBAT.	VBAT
TEST	AH04	I	Test.	VSUS33
TPO	AJ04	O	Test Pin Output. Output pin for test mode.	VCC33

Compensation and Reference Voltage Pin Descriptions

Compensation and Reference Voltage				
Signal Name	Pin #	I/O	Signal Description	Power Plane
VLCOMPP	M26	AI	V-Link Compensation.	VCC15VL
VLVREF	P25	P	V-Link Voltage Reference. See Design Guide.	VCC15VL
PECOMP	K26	AI	PCI Express Port Compensation.	VCC33PE
PEREXT	J26	AI	PCI Express Port External Resistor.	VCC33PE
SATAR50COMP	AH14	IO	Serial ATA Auto Compensation. Connect to a 250 ohm pulldown to GND.	VCCA33SATA

Analog Power Pin Descriptions

Analog Power and Ground			
Signal Name	Pin #	I/O	Signal Description
VCC33USB	(see pin list)	P	USB 2.0 Differential Output Power. 3.3V $\pm 5\%$. Power for USB differential outputs (USBP0+, P0-, P1+, P1-, P2+, P2-, P3+, P3-, P4+, P4-, P5+, P5-, P6+, P6-, P7+, P7-). Connect to VSUS33 through a ferrite bead.
GNDUSB	(see pin list)	P	USB 2.0 Differential Output Ground. Connect to GND through a ferrite bead.
VCCA15PLLUSB	C26	P	USB 2.0 PLL Analog Voltage. Connect to VCC through a ferrite bead.
VCCA33PLLUSB	D25	P	USB 2.0 PLL Analog Voltage. Connect to VCC through a ferrite bead.
GNDA15PLLUSB	D26	P	USB 2.0 PLL Analog Ground. Connect to GND through a ferrite bead.
GNDA33PLLUSB	E25	P	USB 2.0 PLL Analog Ground. Connect to GND through a ferrite bead.
VCC15PLL	V26	P	PLL Analog Power. 1.5V $\pm 5\%$. Connect to VCC through a ferrite bead.
GNDPLL	V25	P	PLL Analog Ground. Connect to GND through a ferrite bead.
VCCA15OSC	AJ07	P	SATA Oscillator Power. 1.5V $\pm 5\%$ (VSUS15 power plane).
GNDAOSC	AK07	P	SATA Oscillator Ground.
VCCA15SATA	Y14-16	P	Serial ATA Analog Power. 1.5V $\pm 5\%$.
VCCA33SATA	AC12-13, AC18-19	P	Serial ATA Analog Power. 3.3V $\pm 5\%$.
GNDA15SATA	(see pin list)	P	Serial ATA Analog Ground.
GNDA33SATA	AB12-13, AB18-19	P	Serial ATA Analog Ground.
VCCA33SPLL	AK14	P	Serial ATA PLL Analog Power. 3.3V $\pm 5\%$.
GNDASPLL	AJ14	P	Serial ATA PLL Analog Ground.
VCCA33PE	J28	P	Power for PCI Express Port 0 Clock PLL. 3.3V $\pm 5\%$.
VCCA33PE1	D30	P	Power for PCI Express Port 1 Clock PLL. 3.3V $\pm 5\%$.
GNDAPE	J27	P	Ground for PCI Express Port 0 Clock PLL.
GNDAPE1	D29	P	Ground for PCI Express Port 1 Clock PLL.

Digital Power Pin Descriptions

Digital Power and Ground			
Signal Name	Pin #	I/O	Signal Description
VCC33	(see pin list)	P	I/O Power. 3.3V ±5%
VCC15	(see pin list)	P	Core Power. 1.5V ±5%. This supply is turned on only when the mechanical switch on the power supply is turned on and the PWRON signal is conditioned high.
VBAT	AE03	P	RTC Battery. Battery input for internal RTC (RTCX1, RTCX2)
GND	(see pin list)	P	Ground. Connect to primary motherboard ground plane.
VCC33PE	(see pin list)	P	Power for PCI Express I/O Interface Logic. 3.3V ±5%.
VCC15VL	(see pin list)	P	V-Link Power. 1.5V ±5%.
VCC33MII	E12, E13, E14, F13, F14	P	Refer to “LAN Controller – Media Independent Interface (MII)”. 3.3V ±5% Suspend Power for LAN Media Independent Interface (interface to external PHY).
VCC15LAN	F09	P	LAN Suspend Power. 1.5V ±5%. Power for LAN. Connect to VCC through a ferrite bead.
VSUS33	V05, W05, Y05, AA05, AB05	P	Suspend Power. 3.3V ±5%. Always available unless the mechanical switch of the power supply is turned off. If the “soft-off” state is not implemented, then this pin can be connected to VCC33.
VSUS15	T05, U05	P	Suspend Power. 1.5V ±5%.
VSUS15PE	J25	P	PCI Express Suspend Power. 1.5V ±5%.
VSUS15USB	F16, D27	P	USB Suspend Power. 1.5V ±5%.
VSUS15MII	K14, K15	P	LAN MII Suspend Power. 1.5V ±5%.
GNDLAN	F10	P	LAN Ground. Connect to GND through a ferrite bead.
GNDUSB	(see pin list)	P	USB 2.0 Differential Output Ground. Connect to GND through a ferrite bead.

Strap Pin Descriptions

Strap Pins					
(External pullup / pulldown straps are required to select "H" / "L")					
Strap Pins for VT8251 Configuration					
Signal	Pin#	Function	Description	Status Bit	Note
SPKR	AJ03	CPU Frequency Strapping	L: Enable CPU frequency strapping H: Disable CPU frequency strapping Default setting: Disable	-	
ACSDOUT0	T03	Auto Reboot	L: Enable auto reboot H: Disable auto reboot Default setting: Disable	-	
SEEDI	B14	Use Serial External LAN EEPROM	L: Enable. Use external EEPROM H: Disable. Do not use external EEPROM Default setting: Enable (pull low)	-	
ACSYNC	U02	LPC FWH Command	L: Enable LPC FWH command H: Disable LPC FWH command Default setting: Disable	-	
PDCS1#	AC25	SATA Spin Up Mode	L: Enable SATA spin up mode H: Disable SATA spin up mode Default setting: Disable	-	
PDDACK#	AE27	PCI Express Debugging Mode	L: Enable PCI Express debugging mode H: Disable PCI Express debugging mode Default setting: Disable	-	
SUSA#	Y03	Notebook / Desktop LAN Reset	L: Notebook LAN reset H: Desktop LAN reset	-	
Strap Pins for North Bridge ("NB") Configuration					
PDCS3#	AC26	NB Configuration	PDCS3# signal state is reflected on signal pin VD7 during power up for North Bridge configuration.	-	Check the North Bridge DS for details
PDA2	AB26	NB Configuration	PDA2 signal state is reflected on signal pin VD6 during power up for North Bridge configuration.	-	Check the North Bridge DS for details -
PDA1	AE29	NB Configuration	PDA1 signal state is reflected on signal pin VD5 during power up for North Bridge configuration.	-	Check the North Bridge DS for details -
GPIOD / PCGNTB	AF03	NB Configuration	GPIOD/PCGNTB signal state is reflected on signal pin VD3 during power up for North Bridge configuration.	-	Check the North Bridge DS for details -
GPIOB / PCREQB	AF01	NB Configuration	GPIOB/PCREQB signal state is reflected on signal pin VD2 during power up for North Bridge configuration.	-	Check the North Bridge DS for details -
PDA0, GPIOA / PCREQA, GPIOC / PCGNTA	AB27 AG02 AG03	NB Configuration	PDA0, GPIOA/PCREQA and GPIOC/PCGNTA signal states are reflected on signal pins VD4, VD1 and VD0 during power up for North Bridge configuration.	-	Check the North Bridge DS for details -

Summary of Internal Pull-Up / Pull-Down Resistor Implementation

Internal Pullups are present on pins SERIRQ and LPCAD[3:0]

Internal Pulldowns are present on all LAN signals except MDIO. MDIO is an internal pull-up signal.

GPIO Multiplexed Pin Selection Table

GPI Multiplexed Pin Selection						
Signal Name	Pin#	Mux Pin	Power	Register Setting	Default Function	Default Value
GPIO0	AD2	-	VBAT	-	GPIO0	Hi-Z
GPIO1	AB4	-	VSUS33	-	GPIO1	Hi-Z
GPIO2	Y2	EXTSMI#	VSUS33	-	EXTSMI	Defined
GPIO3	Y1	RING#	VSUS33	-	RING	Defined
GPIO4	AB2	LID#	VSUS33	-	LID	Defined
GPIO5	V4	BATLOW#	VSUS33	-	BATLOW	Defined
GPIO6	AK4	AGPBZ#	VCC33	-	AGPBZ	Defined
GPIO7	N4	REQ5#	VCC33	RxE4[2]	GPIO7	Hi-Z
GPIO8	AK5	GPO8 SLPBTN# VGATE	VCC33	RxE4[3]	GPIO8	Hi-Z
GPIO9	C28	-	VCC33USB	-	GPIO9	Hi-Z
GPIO10	AA27	GPO10 APICD0	VCC33	~(~APIC Index Rx3[0] & Rx58[6] & ACPI_Rx4D[2])	GPIO10	Hi-Z
GPIO11	AA28	GPO11 APICD1	VCC33	~(~APIC Index Rx3[0] & Rx58[6] & ACPI_Rx4D[3])	GPIO11	Hi-Z
GPIO12	AF4	GPIOE GPO12 SACRST#	VSUS33	Rx94[3]	GPIO12	Hi-Z
GPIO13	AF5	GPIOF GPO13 SACBITCLK	VSUS33	Rx94[3]	GPIO13	Hi-Z
GPIO14	AE6	GPO14 GPIOG SACSYNC	VSUS33	Rx94[3]	GPIO14	Hi-Z
GPIO15	AF6	GPIOH GPO15	VSUS33	Rx94[3]	GPIO15	Hi-Z
GPIO16	P1	REQ6#	VCC33	~RxE4[2]	GPIO16	Hi-Z
GPIO17	W2	CPUMISS SACSDIN0	VSUS33	-	CPUMISS	Defined
GPIO18	Y4	THRM# AOLGPI	VSUS33	-	AOLGPI	Defined
GPIO19	AD28	APICLK	VCC33	-	APICLK	Defined
GPIO20	U4	ACSDIN2 PCS0#	VSUS33	Rx97[0] & ~RxE5[1]	ACSDIN2	Defined
GPIO21	U1	ACSDIN3 PCS1#	VSUS33	Rx97[0] & ~RxE5[2]	ACSDIN3	Defined
GPIO22	AG6	SAGP1	VCC33	Dev 15 Fun 0 Rx4B[0]	GPIO22	Hi-Z
GPIO23	AH6	SAGP2	VCC33	Dev 15 Fun 0 Rx4B[1]	GPIO23	Hi-Z
GPIO24	AG2	GPO24 GPIOA PCREQA	VCC33	~Rx53[7] & ACPI_Rx4F[0]	GPIO24	Hi-Z
GPIO25	AF1	GPO25 GPIOB PCREQB	VCC33	~Rx58[7] & ACPI_Rx4F[1]	GPIO25	Hi-Z
GPIO26	AC3	GPO26 SMBDT2	VSUS33	Rx95[2] & ~Rx95[3]	SMBDT2	Defined

GPI Multiplexed Pin Selection (Continued)						
Signal Name	Pin#	Mux Pin	Power	Register Setting	Default Function	Default Value
GPI27	AB1	GPO27 SMBCK2	VSUS33	Rx95[2] & ~Rx95[3]	SMBCK2	Defined
GPI28	AJ6	SAGP3 GPO28	VCC33	Dev 15 Fun 0 Rx4B[2]	GPI28	Hi-Z
GPI29	AK6	SAGP4 GPO28	VCC33	Dev 15 Fun0 Rx4B[3]	GPI29	Hi-Z
GPI30	AG3	GPO30 GPIOC PCGNTA	VCC33	~Rx53[7] & ACPI_Rx4F[6]	GPI30	Hi-Z
GPI31	AF3	GPO31 GPIOD PCGNTB	VCC33	~Rx58[7] & ACPI_RX4F[7]	GPI31	Hi-Z
GPI32	P3	INTE#	VCC33		GPI32	Hi-Z
GPI33	P2	INTF#	VCC33		GPI33	Hi-Z
GPI34	R3	INTG#	VCC33		GPI34	Hi-Z
GPI35	R4	INTH#	VCC33		GPI35	Hi-Z
GPI36	A25	USBOC4#	VCC33USB		USBOC4#	Hi-Z
GPI37	B25	USBOC5#	VCC33USB		USBOC5#	Hi-Z
GPI38	A26	USBOC6#	VCC33USB		USBOC6#	Hi-Z
GPI39	B26	USBOC7#	VCC33USB		USBOC7#	Hi-Z

GPO Multiplexed Pin Selection							
Signal Name	Pin#	Mux Pin	Power	Register Setting	Default Function	Default Value	Output Type
GPO0	AA4	-	VSUS33	-	GPO0	High	TTL
GPO1	AD3	-	VSUS33	-	GPO1	High	TTL
GPO2	Y3	SUSA#	VSUS33	Rx94[2]	SUSA#	Defined	TTL
GPO3	W3	SUSST#	VSUS33	Rx94[4]	SUSST#	Defined	TTL
GPO4	AA3	SUSCLK	VSUS33	Rx95[1]	SUSCLK	Defined	TTL
GPO5	AH2	CPUSTP#	VCC33	RxE4[0]	CPUSTP#	Defined	TTL
GPO6	AF2	PCISTP#	VCC33	RxE4[1]	PCISTP#	Defined	TTL
GPO7	N3	GNT5	VCC33	~RxE4[2]	GPO7	High	TTL
GPO8	AK5	GPIO8 VGATE SLPBTN#	VCC33	RxE4[3]	GPIO8	Hi-Z	TTL
GPO9	B28	-	VCC33USB	-	GPO9	High	TTL
GPO10	AA27	GPIO10 APICD0	VCC33	~(~APIC Index Rx03[0] & Rx58[6])	GPIO10	Hi-Z	OD
GPO11	AA28	GPIO11 APICD1	VCC33	~(~APIC Index Rx03[0] & RX58[6])	GPIO11	Hi-Z	OD
GPO12	AF4	GPIO12 GPIOE SACRST#	VSUS33	Rx94[3]	GPIO12	Hi-Z	TTL
GPO13	AF5	GPIO13 GPIOF SACBITCLK	VSUS33	Rx94[3]	GPIO13	Hi-Z	TTL
GPO14	AE6	GPIO14 GPIOG SACYNC	VSUS33	Rx94[3]	GPIO14	Hi-Z	TTL
GPO15	AF6	GPIO15 GPIOH	VSUS33	Rx94[3]	GPIO15	Hi-Z	TTL

GPO Multiplexed Pin Selection (Continued)							
Signal Name	Pin#	Mux Pin	Power	Register Setting	Default Function	Default Value	Output Type
GPO20	P4	GNT6#	VCC33	~RxE4[2]	GPO20	High	TTL
GPO21	U3	ACSDOUT1 SACSDOUT	VCC33	RxE4[4]	SDOUT1	Defined	
GPO22	Y30	GHI#	VCC33	RxE5[3]	GHI#	Defined	OD
GPO23	AA29	DPSLP#	VCC33	RxE5[3]	DPSLP	Defined	OD
GPO24	AG2	GPI24 GPIOA PCREQA	VCC33	~Rx53[7]	GPI24	Hi-Z	OD
GPO25	AF1	GPI25 GPIOB PCREQB	VCC33	~Rx58[7]	GPI25	Hi-Z	OD
GPO26	AC3	GPI26 SMBDT2	VSUS33	Rx95[2] & Rx95[3]	SMBDT2	Defined	OD
GPO27	AB1	GPI27 SMBCK2	VSUS33	Rx95[2] & Rx95[3]	SMBCK2	Defined	OD
GPO28	AG7	VIDSEL	VCC33	RxE5[3] & ~RxE5[0]	VIDSEL	Defined	OD
GPO29	AJ5	VRDSLP	VCC33	RxE5[3]	VRDSLP	Defined	OD
GPO30	AG3	GPI30 GPIOC PCGNTA	VCC33	~Rx53[7]	GPI30	Hi-Z	OD
GPO31	AF3	GPI31 PCGNTB GPIOD	VCC33	~Rx58[7]	GPI31	Hi-Z	OD

Note: 1. Register bits referenced above are Device 17 Function 0 unless indicated otherwise.

2. Power: VCC33 : 3.3V
 VSUS33 : Suspend Power
 VCC33USB : USB 3.3V Suspend Power
 VBAT : RTC Power (3.0V)
3. Output Type: OD : Open Drain
 TTL : TTL Level

REGISTER OVERVIEW

In the register descriptions, column “Default” indicates the default value of register bit. While column “Attribute” indicates access type of register bit.

Abbreviations

Attribute Definitions

Read / Write Attribute: Read / write attributes may be used together to specify combined attributes

RO:	Read Only
RZ:	Read as Zero
R1:	Read as 1
WO/W1:	Write Once then Read Only after that
RW1C:	Write of “1” clears bit to zero.
IW:	Ignore Write
MW:	Must Write back what is read
XW:	Backdoor Write
W:	Write Only. (register value can not be read by the software)
RsvdP:	Reserved. Must do a read-modify-write to preserve the bit values.
RsvdZ:	Reserved. Must write 0's.
RSM:	Bits are resume-well.
“-”:	Reserved (essentially the same as RO). Please do not program it.

Sticky Attributes: adding a “S” in tail to indicate a sticky register, which means that register will not be set or altered by hot reset.

Ex. **RWS:** Sticky-Read/Write. **ROS:** Sticky-Read Only. **RW1CS:** Sticky-Write-1-to-Clear.

Default Value Definitions

Dip:	means the default value is set by dip switch or strapping.
HwInit:	Hardware initialized; bit default value is set by hardware.

PCI Device & Function Definitions

There are seven PCI devices and up to 17 PCI functions are implemented in this chip. To specifically identify a PCI function, the following abbreviations will be applied in subsequent sections.

B0D15F0: Bus 0, Device 15, Function 0 – Serial ATA Controller

B0D15F1: Bus 0, Device 15, Function 1 – Parallel ATA Controller

B0D16F0: Bus 0, Device 16, Function 0 – USB 1.1 UHCI Ports 0-1

B0D16F1: Bus 0, Device 16, Function 1 – USB 1.1 UHCI Ports 2-3

B0D16F2: Bus 0, Device 16, Function 2 – USB 1.1 UHCI Ports 4-5

B0D16F3: Bus 0, Device 16, Function 3 – USB 1.1 UHCI Ports 6-7

B0D16F4: Bus 0, Device 16, Function 4 – USB 2.0 UHCI Ports 0-7

B0D17F0: Bus 0, Device 17, Function 0 – Bus Controller and Power Management

B0D17F5: Bus 0, Device 17, Function 5 – AC97 Audio Codec Controller

B0D17F6: Bus 0, Device 17, Function 6 – MC97 Modem Codec Controller

B0D17F7: Bus 0, Device 17, Function 7 – Ultra V-Link Control

B0D18F0: Bus 0, Device 18, Function 0 – VIA LAN Controller

B0D19F0: Bus 0, Device 19, Function 0 – PCI-to-PCIe Bridge

B0D19F1: Bus 0, Device 19, Function 1 – PCI-to-PCI Bridge

BnD0F0: Bus n, Device 0, Function 0 – PCI-to PCI Bridge – PCI Express Root Port 0 (x2 or x1 Line Width)

BnD0F1: Bus n, Device 0, Function 1 – PCI-to PCI Bridge – PCI Express Root Port 1 (x1 Lane Width)

BnD1F0: Bus n, Device 1, Function 0 – High Definition Audio Controller

PCI Express Port & Register Block Definitions

PEG: PCI Express Port G

PE0/PE1/PE2/PE3: PCI Express Port 0 / 1 / 2 / 3

RCRB: PCI Express Root Complex Register Block (in PCI-to PCIe Bridge)

Other Abbreviations

HDAC: High Definition Audio Controller

PMIO: ACPI I/O

MMIO: Memory Mapped I/O

SMIO: System Management I/O

Memory Mapped Registers

Memory Address	Function	Size
FEC00000	APIC Index	8 bit
FEC00010	APIC Data	32 bit
FEC00020	APIC IRQ Pin Assertion	8 bit
FEC00040	APIC EOI	8 bit

System I/O Map

Port	Function	Actual Port Decoding
00-1F	Master DMA Controller	0000 0000 000x xxxx
20-3F	Master Interrupt Controller	0000 0000 001x xxxx
40-5F	Timer / Counter	0000 0000 010x xxxx
60-6F	Keyboard Controller	0000 0000 0110 xxxx
(60h)	KBC Data	0000 0000 0110 x0x0
(61h)	Misc Functions & Speaker Control	0000 0000 0110 xxx1
(64h)	KBC Command / Status	0000 0000 0110 x1x0
70-77	RTC/CMOS/NMI-Disable	0000 0000 0111 0xxx
78-7F	-available for system use	0000 0000 0111 1xxx
80	-reserved- (debug port)	0000 0000 1000 0000
81-8F	DMA Page Registers	0000 0000 1000 xxxx
90-91	-available for system use-	0000 0000 1001 000x
92	System Control	0000 0000 1001 0010
93-9F	-available for system use	0000 0000 1001 xxxx
A0-BF	Slave Interrupt Controller	0000 0000 101x xxxx
C0-DF	Slave DMA Controller	0000 0000 110x xxxx
E0-FF	-available for system use	0000 0000 111x xxxx
100-CF7	-available for system use*	
CF8-CFB	PCI Configuration Address	0000 1100 1111 10xx
CFC-CFF	PCI Configuration Data	0000 1100 1111 11xx
D00-FFFF	-available for system use-	

REGISTER DESCRIPTIONS

Legacy I/O Ports

This group of registers includes the DMA Controllers, Interrupt Controllers, and Timer/Counters as well as a number of miscellaneous ports originally implemented using discrete logic on original PC/AT motherboards. All of the registers listed are integrated on-chip. These registers are implemented in a precise manner for backwards compatibility with previous generations of PC hardware. These registers are listed for information purposes only. Detailed descriptions of the actions and programming of these registers are included in numerous industry publications (duplication of that information here is beyond the scope of this document). All of these registers reside in I/O space.

Miscellaneous Functions and System Control

I/O Port Address: 61h

Miscellaneous Functions & Speaker Control

Default Value: 00h

Bit	Attribute	Default	Description
7	RO	0	SERR# Status 0: SERR# has not been asserted Note: This bit is set when the PCI bus SERR# signal is asserted. Once set, this bit may be cleared by setting bit-2 of this register. Bit-2 should be cleared to enable recording of the next SERR# (i.e., bit-2 must be set to 0 to enable this bit to be set). IOCHK# Status 0: IOCHK# has not been asserted 1: IOCHK # was asserted by an ISA agent Note: This bit is set when the ISA bus IOCHCK# signal is asserted. Once set, this bit may be cleared by setting bit-3 of this register. Bit-3 should be cleared to enable recording of the next IOCHCK# (i.e., bit-3 must be set to 0 to enable this bit to be set). IOCHCK# generates NMI to the CPU if NMI is enabled.
6	RO	0	Timer/Counter 2 Output This bit reflects the output of Timer/Counter 2 without any synchronization.
5	RO	0	Refresh Detected This bit toggles on every rising edge of the ISA bus REFRESH# signal.
4	RO	0	IOCHK# Enable 0: Enable (see bit-6 above) 1: Disable (force IOCHCK# inactive and clear any "IOCHCK# Active" condition in bit-6)
3	RW	0	SERR# Enable 0: Enable (see bit-7 above) 1: Disable (force SERR# inactive and clear any "SERR# Active" condition in bit-7)
2	RW	0	Speaker Enable 0: Disable 1: Enable Timer/Counter 2 output to drive SPKR pin
1	RW	0	Timer/Counter 2 Enable 0: Disable 1: Enable Timer/Counter 2
0	RW	0	

I/O Port Address: 92h

System Control

Default Value: 00h

Bit	Attribute	Default	Description
7:2	—	0	Reserved
1	RW	0	A20 Address Line Enable 0: A20 disabled / forced 0 (real mode) 1: A20 address line enabled
0	RW	0	High Speed Reset 0: Normal 1: Briefly pulse system reset to switch from protected mode to real mode

Keyboard Controller I/O Registers

The keyboard controller handles the keyboard and mouse interfaces. Two ports are used: port 60h and port 64h. Reads from port 64h return a status byte. Writes to port 64h are command codes (see command code list following the register descriptions). Input and output data is transferred via port 60h.

A “Control” register is also available. It is accessible by writing commands 20h / 60h to the command port (port 64h); the control byte is written by first sending 60h to the command port, then sending the control byte value. The control register may be read by sending a command of 20h to port 64h, waiting for “Output Buffer Full” status = 1, then reading the control byte value from port 60h.

Traditional (non-integrated) keyboard controllers have an “Input Port” and an “Output Port” that control pins dedicated to specific functions. In the integrated version, connections are hard wired as listed below. Outputs are “open-collector” so to allow input on one of these pins, the output value for that pin would be set high (non-driving) and the desired input value read on the input port. These ports are defined as follows:

Bit	Input Port
0	Keyboard Data In
1	Mouse Data In
Bit	Output Port
0	System Reset (1 = Execute Reset)
1	Gate A20 (1 = A20 Enabled)
2	Mouse Data Out
3	Mouse Clock Out
6	Keyboard Clock Out
7	Keyboard Data Out
Bit	Test Port
0	Keyboard Clock In
1	Mouse Clock In

Hardwired Internal Connections

Keyboard Data Out (Open Collector) <=> Keyboard Data In

Keyboard Clock Out (Open Collector) <=> Keyboard Clk In

Mouse Data Out (Open Collector) <=> Mouse Data In

Mouse Clock Out (Open Collector) <=> Mouse Clock In

Keyboard OBF Interrupt => IRQ1

Mouse OBF Interrupt => IRQ12

Input / Output / Test Port Command Codes

C0h transfers input port data to the output buffer.

D0h copies output port values to the output buffer.

E0h transfers test input port data to the output buffer.

The above definitions are provided for reference only as actual keyboard and mouse control is no longer performed bit-by bit using the above ports but controlled directly by keyboard / mouse controller internal logic. Data is sent and received using the command codes listed on the following page.

I/O Port Address: 60h**Keyboard Controller Input / Output Buffer**

Bit	Attribute	Description
7:0	WO	Keyboard Controller Input Buffer Only write to port 60h if port 64h bit-1 = 0 (1=full).
7:0	RO	Keyboard Controller Output Buffer Only read from port 60h if port 64h bit-0 = 1 (0=empty).

I/O Port Address: 64h
Keyboard / Mouse Status
Default Value: 00h

Bit	Attribute	Default	Description
7	RO	0	Parity Error 0: No parity error (odd parity received) 1: Even parity occurred on last byte received from keyboard / mouse
6	RO	0	General Receive / Transmit Timeout 0: No Error 1: Error
5	RO	0	Mouse Output Buffer Full 0: Mouse output buffer empty 1: Mouse output buffer holds mouse data
4	RO	0	Keylock Status 0: Locked 1: Free
3	RO	0	Command / Data 0: Last write was data write 1: Last write was command write
2	RO	0	System Flag 0: Power-On Default 1: Self Test Successful
1	RO	0	Input Buffer Full 0: Input Buffer Empty 1: Input Buffer Full
0	RO	0	Keyboard Output Buffer Full 0: Keyboard Output Buffer Empty 1: Keyboard Output Buffer Full

KBC Control Register (R/W via Commands 20h/60h)

Bit	Attribute	Default	Description
7	—	0	Reserved
6	RW	1	PC Compatibility 0: Disable scan conversion 1: Convert scan codes to PC format; convert 2-byte break sequences to 1-byte PC-compatible break codes
5	RW	0	Mouse Interface 0: Enable 1: Disable
4	RW	0	Keyboard Interface 0: Enable 1: Disable
3	—	0	Reserved
2	RO	0	System Flag This bit may be read back as status register bit-2
1	RW	0	Mouse Interrupts 0: Disable 1: Enable - Generate interrupt on IRQ12 when mouse data comes into output buffer
0	RW	0	Keyboard Interrupts 0: Disable 1: Enable - Generate interrupt on IRQ1 when output buffer has been written.

I/O Port Address: 64h
Keyboard / Mouse Command

This port is used to send commands to the keyboard / mouse controller. The command codes recognized by the VT8251 are listed in the table below.

Table 3. Keyboard Controller Command Codes

Code	Keyboard Command Code Description
20h	Read Control Byte (next byte is Control Byte)
21-3Fh	Read SRAM Data (next byte is Data Byte)
60h	Write Control Byte (next byte is Control Byte)
61-7Fh	Write SRAM Data (next byte is Data Byte)
A1h	Output Keyboard Controller Version #
A4h	Test if Password is installed (always returns F1h to indicate not installed)
A7h	Disable Mouse Interface
A8h	Enable Mouse Interface
A9h	Mouse Interface Test (puts test results in port 60h) Value: 0=OK, 1=clk stuck low, 2=clk stuck high, 3=data stuck lo, 4=data stuck hi, FF=general error
AAh	KBC self test (returns 55h if OK, FCh if not)
ABh	Keyboard Interface Test (see A9h Mouse Test)
ADh	Disable Keyboard Interface
AEh	Enable Keyboard Interface
AFh	Return Version #
C0h	Read Input Port (read input data to output buffer)
C1h	Poll Input Port (read Mouse Data In continuously to status bit 5)
C8h	Unblock Mouse Output (use before D1 to change active mode)
C9h	Reblock Mouse Output (protection mechanism for D1)
CaH	Read Mode (output KBC mode info to port 60 output buffer: bit-0=0 if ISA, 1 if PS/2)
D0h	Read Output Port (copy output port values to port 60)
D1h	Write Output Port (data byte following is written to keyboard output port as if it came from keyboard)
D2h	Write Keyboard Output Buffer & clear status bit-5 (write following byte to keyboard)
D3h	Write Mouse Output Buffer & set status bit-5 (write following byte to mouse; put value in mouse input buffer so it appears to have come from the mouse)
D4h	Write Mouse (write following byte to mouse)
E0h	Read Keyboard Clock In and Mouse Clock In (return in bits 0-1 respectively of response byte)
Exh	Set Mouse Clock Out per command bit 3 Set Mouse Data Out per command bit 2 Set Gate A20 per command bit 1
Fxh	Pulse Mouse Clock Out low for 6usec per cmd bit 3 Pulse Mouse Data Out low for 6usec per cmd bit 2 Pulse Gate A20 low for 6usec per command bit 1 Pulse System Reset low for 6usec per cmd bit 0

All other codes not listed are undefined.

DMA Controller I/O Registers (00-8Fh)

I/O Ports Address: 0F-00h

Master DMA Controller

Channels 0-3 of the Master DMA Controller control System DMA Channels 0-3. There are 16 Master DMA Controller registers:

I/O Address Bits 15-0	Attribute	Description
0000 0000 000x 0000	RW	Ch 0 Base / Current Address
0000 0000 000x 0001	RW	Ch 0 Base / Current Count
0000 0000 000x 0010	RW	Ch 1 Base / Current Address
0000 0000 000x 0011	RW	Ch 1 Base / Current Count
0000 0000 000x 0100	RW	Ch 2 Base / Current Address
0000 0000 000x 0101	RW	Ch 2 Base / Current Count
0000 0000 000x 0110	RW	Ch 3 Base / Current Address
0000 0000 000x 0111	RW	Ch 3 Base / Current Count
0000 0000 000x 1000	RW	Status / Command
0000 0000 000x 1001	WO	Write Request
0000 0000 000x 1010	WO	Write Single Mask
0000 0000 000x 1011	WO	Write Mode
0000 0000 000x 1100	WO	Clear Byte Pointer F/F
0000 0000 000x 1101	WO	Master Clear
0000 0000 000x 1110	WO	Clear Mask
0000 0000 000x 1111	RW	R/W All Mask Bits

I/O Ports Address: DF- C0h

Slave DMA Controller

Channels 0-3 of the Slave DMA Controller control System DMA Channels 4-7. There are 16 Slave DMA Controller registers:

I/O Address Bits 15-0	Attribute	Description
0000 0000 1100 000x	RW	Ch 4 Base / Current Address
0000 0000 1100 001x	RW	Ch 4 Base / Current Count
0000 0000 1100 010x	RW	Ch 5 Base / Current Address
0000 0000 1100 011x	RW	Ch 5 Base / Current Count
0000 0000 1100 100x	RW	Ch 6 Base / Current Address
0000 0000 1100 101x	RW	Ch 6 Base / Current Count
0000 0000 1100 110x	RW	Ch 7 Base / Current Address
0000 0000 1100 111x	RW	Ch 7 Base / Current Count
0000 0000 1101 000x	RW	Status / Command
0000 0000 1101 001x	WO	Write Request
0000 0000 1101 010x	WO	Write Single Mask
0000 0000 1101 011x	WO	Write Mode
0000 0000 1101 100x	WO	Clear Byte Pointer F/F
0000 0000 1101 101x	WO	Master Clear
0000 0000 1101 110x	WO	Clear Mask
0000 0000 1101 111x	WO	Read/Write All Mask Bits

Note that not all bits of the address are decoded.

The Master and Slave DMA Controllers are compatible with the Intel 8237 DMA Controller chip. Detailed description of 8237 DMA controller operations can be obtained from the Intel Peripheral Components Data Book and numerous other industry publications.

I/O Ports Address: 8F-80h
DMA Page Registers

There are eight DMA Page Registers, one for each DMA channel. These registers provide bits 16-23 of the 24-bit address for each DMA channel (bits 0-15 are stored in registers in the Master and Slave DMA Controllers). They are located at the following I/O Port addresses:

I/O Address Bits 15-0	Attribute	Description
0000 0000 1000 0111	RW	Channel 0 DMA Page (M-0)
0000 0000 1000 0011	RW	Channel 1 DMA Page (M-1)
0000 0000 1000 0001	RW	Channel 2 DMA Page (M-2)
0000 0000 1000 0010	RW	Channel 3 DMA Page (M-3)
0000 0000 1000 1111	RW	Channel 4 DMA Page (S-0)
0000 0000 1000 1011	RW	Channel 5 DMA Page (S-1)
0000 0000 1000 1001	RW	Channel 6 DMA Page (S-2)
0000 0000 1000 1010	RW	Channel 7 DMA Page (S-3)

DMA Controller Shadow Registers

The DMA Controller shadow registers are enabled by setting B0D17F0 Rx40 bit 1. If the shadow registers are enabled, they are read back at the indicated I/O port instead of the standard DMA controller registers (writes are unchanged).

Port Address	Attribute	Description
Port 0	RO	Channel 0 Base Address
Port 1	RO	Channel 0 Byte Count
Port 2	RO	Channel 1 Base Address
Port 3	RO	Channel 1 Byte Count
Port 4	RO	Channel 2 Base Address
Port 5	RO	Channel 2 Byte Count
Port 6	RO	Channel 3 Base Address
Port 7	RO	Channel 3 Byte Count
Port 8	RO	1st Read Channel 0-3 Command Register
Port 8	RO	2nd Read Channel 0-3 Request Register
Port 8	RO	3rd Read Channel 0 Mode Register
Port 8	RO	4th Read Channel 1 Mode Register
Port 8	RO	5th Read Channel 2 Mode Register
Port 8	RO	6th Read Channel 3 Mode Register
Port F	RO	Channel 0-3 Read All Mask
Port C4	RO	Channel 5 Base Address
Port C6	RO	Channel 5 Byte Count
Port C8	RO	Channel 6 Base Address
Port CA	RO	Channel 6 Byte Count
Port CC	RO	Channel 7 Base Address
Port CE	RO	Channel 7 Byte Count
Port D0	RO	1st Read Channel 4-7 Command Register
Port D0	RO	2nd Read Channel 4-7 Request Register
Port D0	RO	3rd Read Channel 4 Mode Register
Port D0	RO	4th Read Channel 5 Mode Register
Port D0	RO	5th Read Channel 6 Mode Register
Port D0	RO	6th Read Channel 7 Mode Register
Port DE	RO	Channel 4-7 Read All Mask

Interrupt Controller I/O Registers (20-A1h)

I/O Ports Address: 21-20h

Master Interrupt Controller

I/O Address Bits 15-0	Attribute	Description
0000 0000 001x xxx0	RW	Master Interrupt Control
0000 0000 001x xxx1	RW	Master Interrupt Mask

Note that not all bits of the address are decoded.

The Master Interrupt Controller is compatible with the Intel 8259 Interrupt Controller chip. Detailed descriptions of 8259 Interrupt Controller operations can be obtained from the Intel Peripheral Components Data Book and numerous other industry publications.

I/O Ports Address: A1-A0h

Slave Interrupt Controller

The Slave Interrupt Controller controls system interrupt channels 8-15. The slave system interrupt controller also occupies two register locations:

I/O Address Bits 15-0	Attribute	Description
0000 0000 101x xxx0	RW	Slave Interrupt Control
0000 0000 101x xxx1	RW	Slave Interrupt Mask

Note that not all address bits are decoded.

The Slave Interrupt Controller is compatible with the Intel 8259 Interrupt Controller chip. Detailed descriptions of 8259 Interrupt Controller operation can be obtained from the Intel Peripheral Components Data Book and numerous other industry publications.

Interrupt Controller I/O Registers (20-A1h)

The following shadow registers are enabled by setting B0D17F0 Rx40[1]. If the shadow registers are enabled, they are read back at the indicated I/O port instead of the standard interrupt controller registers (writes are unchanged).

I/O Ports Address: 20h

Master Interrupt Control Shadow

I/O Ports Address: A0h

Slave Interrupt Control Shadow

Bit	Attribute	Description
7	—	Reserved
6	RO	OCW3 bit 2 (POLL)
5	RO	OCW3 bit 0 (RIS)
4	RO	OCW3 bit 5 (SMM)
3	—	OCW2 bit 7 (R)
2	RO	ICW4 bit 4 (SFNM)
1	RO	ICW4 bit 1 (AEOI)
0	RO	ICW1 bit 3 (LTIM)

I/O Ports Address: 21h
Master Interrupt Mask Shadow
I/O Ports Address: A1h
Slave Interrupt Mask Shadow

Bit	Attribute	Default	Description
7:5	—	0	Reserved
4:0	RO	—	T7-T3 of Interrupt Vector Address

Timer / Counter Registers (40-43h)
I/O Ports Address: 43-40h
Timer / Counter I/O Registers

There are 4 Timer / Counter registers:

I/O Address Bits 15-0	Attribute	Description
0000 0000 010x xx00	RW	Timer / Counter 0 Count
0000 0000 010x xx01	RW	Timer / Counter 1 Count
0000 0000 010x xx10	RW	Timer / Counter 2 Count
0000 0000 010x xx11	WO	Timer / Counter Cmd Mode

Note that not all bits of the address are decoded.

The Timer / Counters are compatible with the Intel 8254 Timer / Counter chip. Detailed descriptions of 8254 Timer / Counter operation can be obtained from the Intel Peripheral Components Data Book and numerous other industry publications..

Timer / Counter Shadow Registers

The following shadow registers are enabled for readback by setting B0D17F0 Rx40[1]. If the shadow registers are enabled, they are read back at the indicated I/O port instead of the standard timer / counter registers (writes are unchanged).

Port Address	Attribute	Description
Port 40	RO	Counter 0 Base Count Value (LSB 1st MSB 2nd)
Port 41	RO	Counter 1 Base Count Value (LSB 1st MSB 2nd)
Port 42	RO	Counter 2 Base Count Value (LSB 1st MSB 2nd)

CMOS / RTC I/O Registers (70-75h)
I/O Ports Address: 70h
CMOS Address

Bit	Attribute	Default	Description
7	RW	1	NMI Disable 0: Enable NMI Generation. NMI is asserted on encountering SERR# on the PCI bus. 1: Disable NMI Generation
6:0	RW	—	CMOS Address (lower 128 bytes)

I/O Ports Address: 71h
CMOS Data

Bit	Attribute	Default	Description
7:0	RW	0	CMOS Data (128 bytes)

Note: Ports 70-71 may be accessed if Device 17 Function 0 Rx51 bit-3 is set to one to select the internal RTC. If Rx51 bit-3 is set to zero, accesses to ports 70-71 will be directed to an external RTC.

I/O Ports Address: 74h
CMOS Address

Bit	Attribute	Default	Description
7:0	RW	0	CMOS Address (256 bytes)

I/O Ports Address: 75h
CMOS Data

Bit	Attribute	Default	Description
7:0	RW	0	CMOS Data (256 bytes)

Note: Ports 74-75 may be accessed only if B0D17F0 Rx4E bit-3 (Port 74/75 Access Enable) is set to one to enable port 74/75 access.

Note: Ports 70-71 are compatible with PC industry-standards and may be used to access the lower 128 bytes of the 256-byte on-chip CMOS RAM. Ports 74-75 may be used to access the full on-chip extended 256-byte space in cases where the on-chip RTC is disabled.

Note: The system Real Time Clock (RTC) is part of the “CMOS” block. The RTC control registers are located at specific offsets in the CMOS data area (0-0Dh and 7D-7Fh). Detailed descriptions of CMOS / RTC operation and programming can be obtained from the VIA VT82887 Data Book or numerous other industry publications. For reference, the definition of the RTC register locations and bits are summarized in the following table:

Table 4. CMOS Register Summary

Offset	Description		
	Register Function	Binary Range	BCD Range
00	Seconds	00-3Bh	00-59h
01	Seconds Alarm	00-3Bh	00-59h
02	Minutes	00-3Bh	00-59h
03	Minutes Alarm	00-3Bh	00-59h
04	Hours	am 12hr 01-1Ch pm 12hr 81-8Ch 24hr: 00-17h	01-12h 81-92h 00-23h
05	Hours Alarm	am 12hr:01-1Ch pm 12hr: 81-8Ch 24hr: 00-17h	01-12h 81-92h 00-23h
06	Day of the Week	Mon=1: 01-07h	01-07h
07	Day of the Month	01-1Fh	01-31h
08	Month	01-0Ch	01-12h
09	Year	00-63h	00-99h

Table 5. CMOS Register Summary (Continue)

Register Function		Bit Description		
0A	Register A	7:	UIP	Update In Progress
		6:4:	DV2-0	Divide (010=ena osc & keep time)
		3:0:	RS3-0	Rate Select for Periodic Interrupt
0B	Register B	7:	SET	Inhibit Update Transfers
		6:	PIE	Periodic Interrupt Enable
		5:	AIE	Alarm Interrupt Enable
		4:	UIE	Update Ended Interrupt Enable
		3:	SQWE	No function (read/write bit)
		2:	DM	Data Mode (0=BCD; 1=Binary)
		1:	24/12	Hours Byte Format
0C	Register C	0:	DSE	Daylight Savings Enable
		7:	IRQF	Interrupt Request Flag
		6:	PF	Periodic Interrupt Flag
		5:	AF	Alarm Interrupt Flag
		4:	UF	Update Ended Flag
0D	Register D	3:0		Unused (always read 0)
		7:	VRT	Reads 1 if VBAT voltage is OK
0E-7C Software-Defined Storage Registers				
Offset	Extended Function	Binary Range		BCD Range
7D	Date Alarm	01		01-31h
7E	Month Alarm	01		01-12h
7F	Century Field	13		19-20h

Keyboard / Mouse Wakeup Index / Data Registers (2E-2Fh)

The Keyboard / Mouse Wakeup registers are accessed by performing I/O operations to / from an index / data pair of registers in system I/O space at port addresses 2Eh and 2Fh. The registers accessed using this mechanism are used to initialize Keyboard / Mouse Wakeup functions at index values in the range of E0-EF.

Keyboard / Mouse Wakeup initialization is accomplished in three steps:

- 1) Enter initialization mode (set Function 0 Rx51[1] = 1)
- 2) Initialize the chip
 - a) Write index to port 2Eh
 - b) Read / write data from / to port 2Fh
 - c) Repeat a and b for all desired registers

Exit initialization mode (set Function 0 Rx51[1] = 0)

I/O Ports Address: 2Eh

Keyboard Wakeup Index

Bit	Attribute	Default	Description
7:0	RW	0	Index Value Function 0 PCI configuration space register Rx51[1] must be set to 1 to enable access to the configuration registers.

I/O Ports Address: 2Fh

Keyboard Wakeup Data

Bit	Attribute	Default	Description
7:0	RW	0	Data Value

Keyboard / Mouse Wakeup Registers

These registers are accessed via the port 2E / 2F index / data register pair with Function 0 Rx51[1] = 1 using the indicated index values below

Offset Address: E0h

Keyboard / Mouse Wakeup Enable

Default Value: 08h

Bit	Attribute	Default	Description
7:5	—	0	Reserved. Always reads 0
4	—	0	Reserved (Do not program)
3	RW	1	Win98 Keyboard Power Key Wake-up 0: Disable 1: Enable
2	RW	0	Password Wake-up 0: Disable 1: Enable
1	RW	0	PS/2 Mouse Wake-up 0: Disable 1: Enable
0	RW	0	Keyboard Wake-up 0: Disable 1: Enable

Offset Address: E1h

Keyboard Wakeup Scan Code Set 0

Default Value: F0h

Bit	Attribute	Default	Description
7:0	RW	F0h	Keyboard Wakeup First Reference Scan Code Write 00 means that Keyboard supports any key wake up

Offset Address: E2h

Keyboard Wakeup Scan Code Set 1

Default Value: 00h

Bit	Attribute	Default	Description
7:0	RW	00h	Keyboard Wakeup Second Reference Scan Code Write 00 means that PS/2 mouse supports any key wakeup

Offset Address: E3h

Keyboard Wakeup Scan Code Set 2

Default Value: 00h

Bit	Attribute	Default	Description
7:0	RW	00h	Keyboard Wakeup Third Reference Scan Code

Offset Address: E4h

Keyboard Wakeup Scan Code Set 3

Default Value: 00h

Bit	Attribute	Default	Description
7:0	RW	00h	Keyboard Wakeup Fourth Reference Scan Code

Offset Address: E5h

Keyboard Wakeup Scan Code Set 4

Default Value: 00h

Bit	Attribute	Default	Description
7:0	RW	00h	Keyboard Wakeup Fifth Reference Scan Code

Offset Address: E6h

Keyboard Wakeup Scan Code Set 5

Default Value: 00h

Bit	Attribute	Default	Description
7:0	RW	00h	Keyboard Wakeup Sixth Reference Scan Code

Offset Address: E7h
Keyboard Wakeup Scan Code Set 6
Default Value: 00h

Bit	Attribute	Default	Description
7:0	RW	00h	Keyboard Wakeup Seventh Reference Scan Code

Offset Address: E8h
Keyboard Wakeup Scan Code Set 7
Default Value: 00h

Bit	Attribute	Default	Description
7:0	RW	00h	Keyboard Wakeup Eighth Reference Scan Code

Offset Address: E9h
Mouse Wakeup Scan Code Set 1
Default Value: 09h

Bit	Attribute	Default	Description
7:0	RW	09h	Mouse Wakeup Scan Code Set 1

Offset Address: EAh
Mouse Wakeup Scan Code Set 2
Default Value: 00h

Bit	Attribute	Default	Description
7:0	RW	00h	Mouse Wakeup Scan Code Set 2

Offset Address: EBh
Mouse Wakeup Scan Code Mask
Default Value: 00h

Bit	Attribute	Default	Description
7:0	RW	00h	Mouse Wakeup Scan Code Mask

Memory Mapped I/O APIC Registers

The IO APIC registers are accessed by an indirect addressing scheme using Index Registers and Data Registers that are mapped into memory space.

Memory Address: FEC00000h

APIC Index

Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:8	—	00h	Reserved
7:0	RW	0	I/O APIC Index 8-bit pointer to the I/O APIC register

Memory Address: FEC00010h

APIC Data

Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:0	RW	00h	I/O APIC Data This is a 32-bit register for the data to be read or written to the I/O APIC indirect register pointed by the Index Register.

Memory Address: FEC00020h

APIC IRQ Pin Assertion

Default Value: nnh

Bit	Attribute	Default	Description
7:5	—	0	Reserved
4:0	WO	nnh	IRQ Number Bits 4:0 written to this register contain the IRQ number for this interrupt. The only valid values are 0-23.

Memory Address: FEC00040h

APIC EOI

Default Value: nnh

Bit	Attribute	Default	Description
7:0	WO	nnh	Redirection Entry Clear When a write is issued to this register, the I/O APIC will check this field and compare it with the vector field for each entry in the I/O Redirection Table. When a match is found, the “RemoteIRR” (Indexed I/O APIC Rx10-3F[14]) bit for that I/O Redirection Entry will be cleared.

Indexed I/O APIC Registers

Index: 0h

I/O APIC Identification

Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:28	—	00h	Reserved
27:24	RW	0	I/O APIC Identification Software must program this value before using the I/O APIC.
23:0	—	00h	Reserved

Index: 1h

I/O APIC Version

Default Value= 0017 8003h

Bit	Attribute	Default	Description
31:24	—	00h	Reserved
23:16	RO	17h	Maximum Redirection Entry This value is equal to the number of interrupt input pins for the I/O APIC minus one. For this I/O APIC, the value is 17h.
15	RO	1b	PCI IRQ This bit is set to 1 to indicate that this version of the I/O APIC implements the IRQ Assertion register and that PCI devices are allowed to write to it to cause interrupt.
14:8	—	00h	Reserved
7:0	RO	03h	APIC Version The implementation version for this I/O APIC is 03h

Index: 2h

I/O APIC Arbitration

Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:28	—	00h	Reserved
27:24	RO	000	I/O APIC Arbitration ID
23:0	—	00h	Reserved

Index: 3h

Boot Configuration

Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:1	—	00h	Reserved
0	RW	0	Delivery Type 0: Interrupt Delivery Mechanism is via the APIC Serial Bus 1: Interrupt Delivery Mechanism is a Front-side Bus Message

Index: 3F-10h
I/O Redirection Table
Default Value: nnn1 nnnn nnnn nnnnh

There are 16 64-bit I/O Redirection Table entry registers. Each register is a dedicated entry for each interrupt input signal.

Table 6. I/O Redirection Table

Index	Function
11-10h	I/O APIC Redirection – APIC IRQ0
13-12h	I/O APIC Redirection – APIC IRQ1
15-14h	I/O APIC Redirection – APIC IRQ2
17-16h	I/O APIC Redirection – APIC IRQ3
19-18h	I/O APIC Redirection – APIC IRQ4
1B-1Ah	I/O APIC Redirection – APIC IRQ5
1C-1Dh	I/O APIC Redirection – APIC IRQ6
1E-1Fh	I/O APIC Redirection – APIC IRQ7
21-20h	I/O APIC Redirection – APIC IRQ8
23-22h	I/O APIC Redirection – APIC IRQ9
25-24h	I/O APIC Redirection – APIC IRQ10
27-26h	I/O APIC Redirection – APIC IRQ11
29-28h	I/O APIC Redirection – APIC IRQ12
2B-2Ah	I/O APIC Redirection – APIC IRQ13
2D-2Ch	I/O APIC Redirection – APIC IRQ14
2F-2Eh	I/O APIC Redirection – APIC IRQ15
31-30h	I/O APIC Redirection – APIC IRQ16
33-32h	I/O APIC Redirection – APIC IRQ17
35-34h	I/O APIC Redirection – APIC IRQ18
37-36h	I/O APIC Redirection – APIC IRQ19
39-38h	I/O APIC Redirection – APIC IRQ20
3B-3Ah	I/O APIC Redirection – APIC IRQ21
3D-3Ch	I/O APIC Redirection – APIC IRQ22
3F-3Eh	I/O APIC Redirection – APIC IRQ23

Bit	Attribute	Default	Description						
63:56	RW	nnh	<p>Destination Field In Physical Mode (bit 11=0), bits [59:56] contain an APIC ID. In Logical Mode (bit 11=1), bits [63:56] of the Destination Field specify the logical destination address.</p> <table> <tr> <td>Destination Mode IOREDTBLx[11]</td> <td>Logical Destination Address</td> </tr> <tr> <td>0: Physical Mode</td> <td>IOREDTBLx[59:56] = APIC ID</td> </tr> <tr> <td>1: Logical Mode</td> <td>IOREDTBLx[63:56] = Set of processors</td> </tr> </table>	Destination Mode IOREDTBLx[11]	Logical Destination Address	0: Physical Mode	IOREDTBLx[59:56] = APIC ID	1: Logical Mode	IOREDTBLx[63:56] = Set of processors
Destination Mode IOREDTBLx[11]	Logical Destination Address								
0: Physical Mode	IOREDTBLx[59:56] = APIC ID								
1: Logical Mode	IOREDTBLx[63:56] = Set of processors								
55:17	—	0	Reserved						
16	RW	0	<p>Interrupt Mask 0: Not Mask 1: Masked</p>						
15	RW	0	<p>Trigger Mode Indicates the type of signal on the interrupt pin that triggers an interrupt. 1: Level Sensitive 0: Edge Sensitive.</p>						
14	RO	—	<p>Remote IRR This bit is used for level triggered interrupts. Its meaning is undefined for edge triggered interrupts. For level triggered interrupts, this bit is set to 1 when local APIC(s) accept the level interrupt sent by the IOAPIC. 0: EOI message with a matching interrupt vector is received from a local APIC 1: Level sensitive interrupt sent by IOAPIC accepted by local APIC(s)</p>						
13	RW	0	<p>Interrupt Input Pin Polarity Specifies the polarity of the interrupt signal. 0: High active 1: Low active</p>						
12	RO	—	<p>Delivery Status Contains the current status of the delivery of this interrupt. 0: Idle (there is currently no activity for this interrupt.) 1: Send Pending (the interrupt has been injected but its delivery is temporarily held either because the APIC bus is busy or because the receiving APIC unit can not currently accept the interrupt).</p>						
11	RW	0	<p>Destination Mode Determines the interpretation of the Destination field. 0: Physical Mode 1: Logical Mode.</p>						
10:8	RW	000	<p>Delivery Mode Specify how the APICs listed in the destination field should act upon reception of this signal. 000: Fixed 001: Lowest Priority 010: SMI 011: Reserved 100: NMI 101: INIT 110: Reserved 111: ExtINT</p>						
7:0	RW	nnh	<p>Interrupt Vector Contain the interrupt vector for this interrupt. Vector values range from 10h to FEh.</p>						

Configuration Space I/O

Configuration space accesses for all functions use PCI configuration mechanism 1 (see PCI specification revision 2.2 for more details). The ports respond only to double-word accesses. Byte or word accesses will be passed on unchanged

I/O Port Address: CFB-CF8h

PCI Configuration Address

Default Value: 0000 0000h

Bit	Attribute	Default	Description
31	RW	0	Configuration Space Enable 0: Disabled 1: Convert configuration data port writes to configuration cycles on the PCI bus
30:24	—	0	Reserved (always reads 0)
23:16	RW	0	PCI Bus Number Used to choose a specific PCI bus in the system
15:11	RW	0	Device Number Used to choose a specific device in the system (devices 0 and 1 are defined)
10:8	RW	0	Function Number Used to choose a specific function if the selected device supports multiple functions
7:2	RW	0	Register Number (also called the "Offset") Used to select a specific DWORD in the configuration space
1:0	RW	0	Fixed (always reads 0)

I/O Port Address: CFF-CFCh

PCI Configuration Data

Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:0	RW	0	PCI Configuration Data

Note. Refer to PCI Bus Specification Version 2.2 for further details on operation of the above configuration registers.

Bus 0 Device 15 Function 0 (B0D15F0): Serial ATA Controller

Header Registers (0-4Fh)

Offset Address: 1-0h (B0D15F0)

Vendor ID
Default Value: 1106h

Bit	Attribute	Default	Description
15:0	RO	1106h	Vendor ID

Offset Address: 3-2h (B0D15F0)

Device ID
Default Value: 3349h

Bit	Attribute	Default	Description
15:0	RO	3349h	Device ID

Offset Address: 5-4h (B0D15F0)

PCI Command
Default Value: 00h

Bit	Attribute	Default	Description
15:11	—	0	Reserved
10	RW	0	Interrupt Disable
9:7	—	0	Reserved
6	RO	0	Parity Error Response
5	RO	0	VGA Palette Snooping (Reserved)
4	RO	0	Memory Write and Invalidate
3	RO	0	Respond to Special Cycle
2	RW	0	Bus Master
1	RW	0	Memory Space Access
0	RW	0	I/O Space Access When the “I/O Space” bit is disabled, the device will not respond to I/O addresses.

Offset Address: 7-6h (B0D15F0)

PCI Status
Default Value: 0210h

Bit	Attribute	Default	Description
15	RO	0	Detect Parity Error
14	RO	0	Signaled System Error (SERR#)
13	RW1C	0	Received Master Abort
12	RW1C	0	Received Target Abort
11	RO	0	Signaled Target Abort
10:9	RO	01	DEVSEL# Timing 01: Medium (default)
8	RO	0	Master Data Parity Detected
7	RO	0	Fast Back-to-Back Capability
6	—	0	Reserved
5	RO	0	66 MHz Capable
4	RO	1	Power Management Capability List
3	RO	0	Interrupt Status
2:0	—	0	Reserved

Offset Address: 8h (B0D15F0)

Revision ID
Default Value: 00h

Bit	Attribute	Default	Description
7:0	RO	00h	Revision Code for SATA Controller Logic Block

Offset Address: 9h (B0D15F0)
Programming Interface
Default Value: 8Fh

Bit	Attribute	Default	Description
Configuration 1(When RX0A = 06h or 04h)			
7:0	RO	01	Programming Interface 00: The read value for RAID controller 01: The read value for AHCI controller If RX0A = 06h, this register will be read as 01h. If RX0A is 8'h04, this register will be read as 00h. If RX0A is 8'h01, this register will be read as Configuration 2.
Configuration 2 (When RX0A = 01h)			
7	RO	1	Master IDE Device
6:4	RO	0	Fixed at 0
3	RO	1	Programmable Indicator – Secondary
2	RW	1	Channel Operating Mode – Secondary 0: Compatible Mode 1: Native Mode
1	RO	1	Programmable Indicator – Primary
0	RW	1	Channel Operating Mode – Primary 0: Compatible Mode 1: Native Mode

Rx9h is set to 00 to read value for RAID controller.

Offset Address: 0Ah (B0D15F0)
Sub Class Code
Default Value: 06h

Bit	Attribute	Default	Description
7:0	RO	06h	Sub Class 01: IDE Controller 04: RAID Controller 06: SATA Controller

Offset Address: 0Bh (B0D15F0)
Base Class Code
Default Value: 01h

Bit	Attribute	Default	Description
7:0	RO	01h	Base Class 01: Mass Storage Controller

Offset Address: 0Ch (B0D15F0)
Cache Line Size
Default Value: 00h

Bit	Attribute	Default	Description
7:0	RO	00	Cache Line Size Fixed at 0

Offset Address: 0Dh (B0D15F0)
Latency Timer
Default Value: 20h

Bit	Attribute	Default	Description
7:4	RW	2h	Latency Timer
3:0	RO	0h	Fixed at 0

Offset Address: 0Eh (B0D15F0)
Header Type
Default Value: 80h

Bit	Attribute	Default	Description
7	RO	1	Multiple Function Device
6:0	RO	0	Fixed at 0

Offset Address: 13-10h (B0D15F0)
SATA I Primary Data / Command Base Address
Default Value: 0000 01F1

Specifies an 8 byte I/O address space.

Bit	Attribute	Default	Description
31:16	—	0	Reserved (Must be set to 0)
15:0	RW	01F1	Port Address Bit 2:0 fixed at 001b.

Offset Address: 17-14h (B0D15F0)
SATA I Primary Control / Status Base Address
Default Value: 0000 03F5h

Specifies a 4 byte I/O address space of which only the third byte is active.

Bit	Attribute	Default	Description
31:16	—	0	Reserved (Must be set to 0)
15:0	RW	03F5h	Port Address Bit 1:0 fix at 01b.

Offset Address: 1B-18h (D15F0)
SATA I Secondary Data / Command Base Address
Default Value: 0000 0171h

Specifies an 8 byte I/O address space.

Bit	Attribute	Default	Description
31:16	—	0	Reserved (Must be set to 0)
15:0	RW	0171h	Port Address Bit 2:0 fixed at 001b.

Offset Address: 1F-1Ch (D15F0)
SATA I Secondary Control / Status Base Address
Default Value: 0000 0375h

Specifies a 4 byte I/O address space of which only the third byte is active.

Bit	Attribute	Default	Description
31:16	—	0	Reserved (Must be set to 0)
15:0	RW	0375h	Port Address Bit 1:0 fix at 01b.

Offset Address: 23-20h (D15F0)
SATA I Bus Master Control Register Base Address
Default Value: 0000 CC01h

Specifies a 16 byte I/O address space.

Bit	Attribute	Default	Description
31:16	—	0	Reserved (Must be set to 0)
15:0	RW	CC01h	Port Address Bit 3:0 fix at 001b.

Offset Address: 27-24h (B0D15F0)
AHCI Base Address
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:10	RW	0	Base Address of Register Memory Space
9:4	—	0	Reserved
3	RO	0	Prefetchable Indicates this range is not pre-fetchable.
2:1	RO	0	Type Indicates this range can be mapped anywhere in 32-bit address space
0	RO	0	Resource Type Indicator Indicates a request for register memory space 00-1F Generic host control 20-FF Reserved 100-17F Port 0 port control registers (128 bytes) 180-1FF Port 1 port control registers (128 bytes) 200-27F Port 2 port control registers (128 bytes) 280-2FF Port 3 port control registers (128 bytes)

Offset Address: 2D-2Ch (B0D15F0)
Subsystem Vendor ID
Default Value: 1106h

Bit	Attribute	Default	Description
15:0	RO	1106h	Subsystem Vendor ID The read back value can be changed by writing to RxD4-D5

Offset Address: 2F-2Eh (B0D15F0)
Subsystem ID
Default Value: 3349h

Bit	Attribute	Default	Description
15:0	RO	3349h	Subsystem ID The read back value can be changed by writing to RxD6-D7

Offset Address: 34h (B0D15F0)
Power Management Capabilities Pointer
Default Value: C0h

Bit	Attribute	Default	Description
7:0	RO	C0h	Power Management Capabilities Pointer

Offset Address: 3Ch (B0D15F0)
Interrupt Line
Default Value: 00h

Bit	Attribute	Default	Description
7:4	—	0	Reserved
3:0	RW	0	IDE Interrupt Routing If [7:4] is set to Fh, route to IRQ0. Others are decoded to IRQ0~IRQ15.

Offset Address: 3Dh (B0D15F0)
Interrupt Pin
Default Value: 02h

Bit	Attribute	Default	Description
7:0	RO	02h	Interrupt Routing Mode (INTA# used) 00: Legacy Mode Interrupt Routing Others: Native Mode Interrupt Routing

Offset Address: 3Eh (B0D15F0)
Minimum Grant
Default Value: 00h

Bit	Attribute	Default	Description
7:0	RO	00h	Minimum Grant

Offset Address: 3Fh (B0D15F0)
Minimum Grant
Default Value: 00h

Bit	Attribute	Default	Description
7:0	RO	00h	Maximum Latency

Offset Address: 40h (B0D15F0)
SATA Channel Enable
Default Value: 63h

Bit	Attribute	Default	Description
7:4	RO	6h	Chip ID
3:2	—	0	Reserved
1	RW	1	SATA Primary Channel Enable 0: Disable 1: Enable
0	RW	1	SATA Secondary Channel Enable 0: Disable 1: Enable

Offset Address: 41h (B0D15F0)
SATA Interrupt Gating
Default Value: 13h

Bit	Attribute	Default	Description
7:5	—	0	Reserved
4	RW	1	SATA II AHCI Interrupt Gating Enable (Interrupt will be asserted when data are all flushed)
3	RW	0	PERR Check 0: Disable 1: Enable
2	RW	0	SERR Check 0: Disable 1: Enable
1	RW	1	SATA I Primary Channel Interrupt Gating (Interrupt will be asserted when data are all flushed) 0: Disable 1: Enable
0	RW	1	SATA I Secondary Channel Interrupt Gating (Interrupt will be asserted when data are all flushed) 0: Disable 1: Enable

Offset Address: 42h (B0D15F0)
Native Mode Enable
Default Value: F1h

Bit	Attribute	Default	Description
7	RW / RO	1	Primary Channel I/O Native Mode 0: Disable 1: Enable RO when Rx0A is 06h or 04h.
6	RW / RO	1	Secondary Channel I/O Native Mode 0: Disable 1: Enable RO when Rx0A is 06h or 04h.
5	RW / RO	1	Primary Channel Interrupt Native Mode 0: Disable 1: Enable RO when Rx0A is 06h or 04h.
4	RW / RO	1	Secondary Channel Interrupt Native Mode 0: Disable 1: Enable RO when Rx0A is 06h or 04h.
3:2	—	00	Reserved
1:0	RW	01b	DEVSEL Timing

Offset Address: 43h (B0D15F0)
FIFO Threshold Control
Default Value: 44h

Bit	Attribute	Default	Description
7	—	0	Reserved
6:4	RW	100b	Primary Channel Threshold Control
3	—	0	Reserved
2:0	RW	100b	Secondary Channel Threshold Control FIFO size: 128 DW 000: Zero Threshold 001: 1/8 011: 3/8 101: 5/8 111: 7/8
			010: 1/4 100: 1/2 110: 3/4

Offset Address: 44h (B0D15F0)
Miscellaneous Control I
Default Value: 07h

Bit	Attribute	Default	Description
7	—	0	Reserved
6	RW	0	Master Read Cycle IRDY# Wait States
5	RW	0	Master Write Cycle IRDY# Wait States
4	—	0	Reserved
3	RW	0	Bus Master IDE Status Register Read Retry 0: Disable 1: Enable
2	RW	1	Change Drive to Clear all FIFO Internal States 0: Disable 1: Enable
1	RW	1	Split 2 Channel Request 0: Disable 1: Enable
0	RW	1	TP Layer Back to Idle When Link Layer is Idle 0: Disable 1: Enable

Offset Address: 45h (B0D15F0)
Miscellaneous Control II
Default Value: AFh

Bit	Attribute	Default	Description
7	RW	1	Sub Class (Rx0A) Write Protect 0: Rx0A Write Enable 1: Rx0A Write Disable
6	RW	0	Clock Gating 0: Disable 1: Enable
5	RW	1	Latency Timer 0: Disable 1: Enable Set to 1 only when GNT is deasserted for better performance.
4	RW	0	Interrupt Line (Rx3C) Write Protect 0: Rx3C Write Enable 1: Rx3C Write Disable
3	RW	1	Memory Read Multiple Command 0: Disable 1: Enable
2	RW	1	Memory Write and Invalidate Command 0: Disable 1: Enable
1	RW	1	Primary Channel Read DMA Flush Data After Interrupt 0: Disable 1: Enable
0	RW	1	Secondary Channel Read DMA Flush Data After Interrupt 0: Disable 1: Enable

Offset Address: 46h (B0D15F0)
Miscellaneous Control
Default Value: 08h

Bit	Attribute	Default	Description
7	—	0	Reserved
6	RW	0	Transport Dynamic Clock Gating 0: Disable 1: Enable
5:3	—	001	Reserved
2	RW	0	SATA Read PRD Pipeline Function 0: Disable 1: Enable
1	RW	0	Improve SATA I PIO Performance 0: On 1: Off
0	RW	0	Mask PCI Bus Input Floating Signal (Vector Mode and Test Only) 0: Disable 1: Enable

Offset Address: 48h (B0D15F0)
PHY Wakeup Request Control
Default Value: 00h

Bit	Attribute	Default	Description
7:4	—	0	Reserved
3	RW	0	External PHY Port 4 Wakeup Request
2	RW	0	External PHY Port 3 Wakeup Request
1	RW	0	External PHY Port 2 Wakeup Request
0	RW	0	External PHY Port 1 Wakeup Request

Note: The internal request is triggered by the rising edge of each bit written.

Offset Address: 49h (B0D15F0)
Misc. Registers
Default Value: A0h

Bit	Attribute	Default	Description
7	RW	1	PATA Function 0: Disable (Rx0E[7] will be 0) 1: Enable
6	RW	0	SATA I Master / Master Mode Port Selection 0: Use Port 1 and Port 2 1: Use Port 3 and Port 4
5	RW	1	SATA Ports Master / Slave Configuration 0: Master / Master Configuration 1: Master / Slave Configuration
4:2	—	0	Reserved
1	RW	0	SATA I to Support Port Multiplier (Test Mode Only)
0	RW	0	Force Controller to Enter AHCI Mode

Offset Address: 4Ah (B0D15F0)
AHCI Misc. Registers
Default Value: 14h

Bit	Attribute	Default	Description
7	RW	0	Always Write First D2H to Memory Region (Test Only)
6	RW	0	Pipeline RFIS to Memory Cycle (Test Only)
5	RW	0	Single MSI Assertion Method 0: Generate single MSI by GHC.IS register 1: Generate single MSI by PxIS register
4	RW	1	Fetch All 64 Bytes CFIS Field of Command Table
3	RW	0	AHCI Update Received FIS to Memory Function
2	RW	1	AHCI DMA Update Byte Count Function
1	RW	0	AHCI DMA PRD (Physical Region Descriptor) Pre-fetch Buffer Function
0	RW	0	AHCI Command List CTBA (Command Table Descriptor Base Address) Cache Function

Offset Address: 4Bh (B0D15F0)
AHCI Interlock Switch Pin Output Enable
Default Value: 00h

Bit	Attribute	Default	Description
7	RW	0	Port 4 Interlock Switch Pin Output
6	RW	0	Port 3 Interlock Switch Pin Output
5	RW	0	Port 2 Interlock Switch Pin Output
4	RW	0	Port 1 Interlock Switch Pin Output
3	RW	0	Port 4 Interlock Switch Pin Output Enable
2	RW	0	Port 3 Interlock Switch Pin Output Enable
1	RW	0	Port 2 Interlock Switch Pin Output Enable
0	RW	0	Port 1 Interlock Switch Pin Output Enable

Offset Address: 4Eh (B0D15F0)
SATA I/II Debugging Signals Output Control I
Default Value: 00h

Bit	Attribute	Default	Description
7	RW	0	Enable SATA I/II PHY Port 4 Error Status (2) Output to EEDI Pin
6	RW	0	Enable SATA I/II PHY Port 4 Error Status (1) Output to EEDI Pin
5	RW	0	Enable SATA I/II PHY Port 3 Error Status (2) Output to EEDI Pin
4	RW	0	Enable SATA I/II PHY Port 3 Error Status (1) Output to EEDI Pin
3	RW	0	Enable SATA I/II PHY Port 2 Error Status (2) Output to EEDI Pin
2	RW	0	Enable SATA I/II PHY Port 2 Error Status (1) Output to EEDI Pin
1	RW	0	Enable SATA I/II PHY Port 1 Error Status (2) Output to EEDI Pin
0	RW	0	Enable SATA I/II PHY Port 1 Error Status (1) Output to EEDI Pin

Error status (1): (a) 10 bit to 8 bit error or (b) crc error or (c) disparity error or (d) handshake error

Error status (2): (a) link sequence error or (b) FIS type error or (c) transport port state transmission error

Offset Address: 4Fh (B0D15F0)
SATA I/II Debugging Signals Output Control II
Default Value: 00h

Bit	Attribute	Default	Description
7	RW	0	Output BIST Error Signal to PDDREQ Pin
6	RW	0	Output Device Mode Error Signal to Output Pin (PDDREQ, Test Only)
5:1	—	0	Reserved
0	RW	0	Enable Error Signal Output to EEDI Pin

SATA Transport Control Registers (50-54h)
Offset Address: 50h (B0D15F0)
Software Controllable Power Mode Request
Default Value: 00h

Bit	Attribute	Default	Description
7	RW	0	Internal PHY Port 4 SLUMBER Request
6	RW	0	Internal PHY Port 4 PARTIAL Request
5	RW	0	Internal PHY Port 3 SLUMBER Request
4	RW	0	Internal PHY Port 3 PARTIAL Request
3	RW	0	Internal PHY Port 2 SLUMBER Request
2	RW	0	Internal PHY Port 2 PARTIAL Request
1	RW	0	Internal PHY Port 1 SLUMBER Request
0	RW	0	Internal PHY Port 1 PARTIAL Request

Note: The internal request is triggered by the rising edge of each bit.

Offset Address: 51h (B0D15F0)
Hardware Controllable Power Mode
Default Value: 00h

Bit	Attribute	Default	Description
7	RW	0	Change Drive & Let Idle Device Enter Power Mode 0: Disable 1: Enable
6	RW	0	Change Drive Power Mode Selection for Idle Device 0: Partial 1: Slumber
5	—	0	Reserved
4	RW	0	Enter to Partial Process (Item1) Disabled 0: Disable 1: Enable
3	RW	0	Enter to Slumber Process (Item2) Disabled 0: Disable 1: Enable
2:0	RW	0	Power Clock Select 000 T = 1t 001 T = 2t 1.Power Mode Control Process: Partial will be requested if transport idle for at least 2T. 2.Slumber will be requested if transport layer idle for at least 10 T. (t = 0.425s)

Offset Address: 52h (B0D15F0)
Transport Miscellaneous Control
Default Value: 00h

Bit	Attribute	Default	Description
7	RW	0	Software Issued AHCI DMA Stop (Test Mode Only)
6	RW	0	Transport issues early request to link for better performance
5	RW	0	Reset AHCI transport queue DMA transfer count (Test Only)
4	RW	0	Signal Data FIS Transmission Allow over 8k bytes.
3	RW	0	BIST FIS Controller can accept BIST FIS when behaves as a device (Rx53[1:0] are set). This bit is set only for controller to control BIST FIS self-test.
2	RW	0	SATA Flow Control Water Flag 0: 52DW 1: 40DW
1:0	—	0	Reserved

Offset Address: 53h (B0D15F0)
Device Mode Testing Register – Port 1 and Port 2
Default Value: 00h

Bit	Attribute	Default	Description
7	WO/RO	0	Trigger Port 2 Device Mode Write “1” to trigger device mode memory read based on the address specified in RX93~90 Read value indicates memory read cycle is busy now
6	WO/RO	0	Trigger Port 1 Device Mode Write “1” to trigger device mode memory read based on the address specified in RX93~90 Read value indicates memory read cycle is busy now
5	RO	0	Port 2 CRC Error Status
4	RO	0	Port 1 CRC Error Status
3	RW	0	Port 2 device mode simulation continues when handshake error occurs (but always stop at CRC error)
2	RW	0	Port 1 device mode simulation continues when handshake error occurs (but always stop at CRC error)
1	RW	0	Set Port 2 as Device Controller
0	RW	0	Set Port 1 as Device Controller

Offset Address: 54h (B0D15F0)
Device Mode Testing Register – Port 3 and Port 4
Default Value: 00h

Bit	Attribute	Default	Description
7	WO/RO	0	Trigger Port 4 Device Mode Write “1” to trigger device mode memory read based on the address specified in RX93~90 Read value indicates memory read cycle is busy now
6	WO/RO	0	Trigger Port 3 Device Mode Write “1” to trigger device mode memory read based on the address specified in RX93~90 Read value indicates memory read cycle is busy now
5	RO	0	Port 4 CRC Error Status
4	RO	0	Port 3 CRC Error Status
3	RW	0	Port 4 device mode simulation continues when handshake error occurs (but always stop at CRC error)
2	RW	0	Port 3 device mode simulation continues when handshake error occurs (but always stop at CRC error)
1	RW	0	Set Port 4 as Device Controller
0	RW	0	Set Port 3 as Device Controller

SATA Link Control Registers (55-56h)
Offset Address: 56h (B0D15F0)
SATA Link Control
Default Value: 00h

Bit	Attribute	Default	Description
7:6	—	0	Reserved
5	RW	0	Receive Scrambler 0: Enable 1: Disable
4	RW	0	Transmit Scrambler 0: Enable 1: Disable
3	RW	0	Align Primitive Transmission 0: Enable 1: Disable
2	RW	0	Continue Primitive Transmission 0: Enable 1: Disable
1	RW	0	Continue Primitive after Align 0: Disable 1: Enable
0	RW	0	SATA Link Dynamic Clock Gating 0: Enable 1: Disable

SATA PHY Control Registers (58-5Dh)
Offset Address: 5Ch (B0D15F0)
PHY Control Register 1
Default Value: 00h

Bit	Attribute	Default	Description
7:6	—	0	Reserved
5	RW	0	SATA HY Dynamic Cock Gating
4:0	—	0	Reserved

Offset Address: 5Dh (B0D15F0)
PHY Control Register 2
Default Value: 00h

Bit	Attribute	Default	Description
7	RW	0	Port 4 Disable Support Gen2
6	RW	0	Port 3 Disable Support Gen2
5	RW	0	Port 2 Disable Support Gen2
4	RW	0	Port 1 Disable Support Gen2
3:0	RW	0	Pin Swap Mode {D,C,B,A}

Offset Address: 5Eh (B0D15F0)
PHY Control Register 3

Default Value: 08h

Bit	Attribute	Default	Description	Mnemonic
7:4	—	0	Reserved	
3	RW	1	Retry CDR from phase mode to frequency mode in Gen1 0: Disable 1: Enable	RetryCDR
2	RW	0	Ignore the Squelch Signal After PHYRDY 0: Disable 1: Enable	
1	RW	0	Disable Reduce Speed When Unsolicited COMINIT 0: Disable 1: Enable	
0	RW	0	Force Host Always in Gen2 Speed 0: Disable 1: Enable	

RAMBIST / Misc. Registers (5F-61h)
Offset Address: 5Fh (B0D15F0)
Hot Plug Status

Default Value: 00h

Bit	Attribute	Default	Description
7	RW1C	0	Secondary Channel Slave Plug Out Status
6	RW1C	0	Secondary Channel Slave Plug In Status
5	RW1C	0	Secondary Channel Master Plug Out Status
4	RW1C	0	Secondary Channel Master Plug In Status
3	RW1C	0	Primary Channel Slave Plug Out Status
2	RW1C	0	Primary Channel Slave Plug In Status
1	RW1C	0	Primary Channel Master Plug Out Status
0	RW1C	0	Primary Channel Master Plug In Status

Offset Address: 60h (B0D15F0)
SATA I RAM BIST

Default Value: 00h

Bit	Attribute	Default	Description
7:6	—	0	Reserved
5	RO	0	Secondary RAM BIST Error Status
4	WO/RO	0	Trigger Secondary RAM BIST / Busy Status of RAM BIST
3:2	—	0	Reserved
1	RO	0	Primary RAM BIST Error Status
0	WO/RO	0	Trigger Primary RAM BIST / Busy Status of RAM BIST

Offset Address: 61h (B0D15F0)
SATA II RAM BIST

Default Value: 00h

Bit	Attribute	Default	Description
7	RO	0	Port 4 RAM BIST Error Status
6	WO/RO	0	Trigger Port 4 RAM BIST / Busy Status of RAM BIST
5	RO	0	Port 3 RAM BIST Error Status
4	WO/RO	0	Trigger Port 3 RAM BIST / Busy Status of RAM BIST
3	RO	0	Port 2 RAM BIST Error Status
2	WO/RO	0	Trigger Port 2 RAM BIST / Busy Status of RAM BIST
1	RO	0	Port 1 RAM BIST Error Status
0	WO/RO	0	Trigger Port 1 RAM BIST / Busy Status of RAM BIST

Analog PHY Control (64-75h)
Offset Address: 64h (B0D15F0)
Analog PHY (AFE) Control Register 1
Default Value: 0Ch

Bit	Attribute	Default	Description
7	—	0	Reserved
6	RW	0	CDR Bandwidth Select Bit 1
5	RW	0	CDR Bandwidth Select Bit 0
4	RW	0	Squelch Window Select Bit 1
3	RW	1	Squelch Window Select Bit 0
2	RW	1	Options for CDR Charge Pump Bit 2
1	RW	0	Options for CDR Charge Pump Bit 1
0	RW	0	Options for CDR Charge pump Bit 0

Offset Address: 65h (B0D15F0)
AFE Control Register 2
Default Value: AAh

Bit	Attribute	Default	Description
7	RW	1	Port A Control for Driver Current Source Bit 3
6	RW	0	Port A Control for Driver Current Source Bit 2
5	RW	1	Port A Control for Driver Current Source Bit 1
4	RW	0	Port A Control for Driver Current Source Bit 0
3	RW	1	Port B Control for Driver Current Source Bit 3
2	RW	0	Port B Control for Driver Current Source Bit 2
1	RW	1	Port B Control for Driver Current Source Bit 1
0	RW	0	Port B Control for Driver Current Source Bit 0

Offset Address: 66h (B0D15F0)
AFE Control Register 3
Default Value: AAh

Bit	Attribute	Default	Description
7	RW	1	Port C Control for Driver Current Source Bit 3
6	RW	0	Port C Control for Driver Current Source Bit 2
5	RW	1	Port C Control for Driver Current Source Bit 1
4	RW	0	Port C Control for Driver Current Source Bit 0
3	RW	1	Port D Control for Driver Current Source Bit 3
2	RW	0	Port D Control for Driver Current Source Bit 2
1	RW	1	Port D Control for Driver Current Source Bit 1
0	RW	0	Port D Control for Driver Current Source Bit 0

Offset Address: 67h (B0D15F0)
AFE Control Register 4
Default Value: 66h

Bit	Attribute	Default	Description
7	RW	0	Port A Control for Pre / De-emphasis Level Bit 3
6	RW	1	Port A Control for Pre / De-emphasis Level Bit 2
5	RW	1	Port A Control for Pre / De-emphasis Level Bit 1
4	RW	0	Port A Control for Pre / De-emphasis Level Bit 0
3	RW	0	Port B Control for Pre / De-emphasis Level Bit 3
2	RW	1	Port B Control for Pre / De-emphasis Level Bit 2
1	RW	1	Port B Control for Pre / De-emphasis Level Bit 1
0	RW	0	Port B Control for Pre / De-emphasis Level Bit 0

Offset Address: 68h (B0D15F0)
AFE Control Register 5
Default Value: 66h

Bit	Attribute	Default	Description
7	RW	0	Port C Control for Pre / De-emphasis Level Bit 3
6	RW	1	Port C Control for Pre / De-emphasis Level Bit 2
5	RW	1	Port C Control for Pre / De-emphasis Level Bit 1
4	RW	0	Port C Control for Pre / De-emphasis Level Bit 0
3	RW	0	Port D Control for Pre / De-emphasis Level Bit 3
2	RW	1	Port D Control for Pre / De-emphasis Level Bit 2
1	RW	1	Port D Control for Pre / De-emphasis Level Bit 1
0	RW	0	Port D Control for Pre / De-emphasis Level Bit 0

Offset Address: 69h (B0D15F0)
AFE Control Register 6
Default Value: 00h

Bit	Attribute	Default	Description
7	RW	0	Port A Supports External Interconnect Box-to-Box / Long-Haul (Gen1x or Gen2x Support)
6:4	—	0	Reserved
3	RW	0	Gen1 Port A Enable Pre / De-emphasis
2	RW	0	Gen1 Port B Enable Pre / De-emphasis
1	RW	0	Gen1 Port C Enable Pre / De-emphasis
0	RW	0	Gen1 Port D Enable Pre / De-emphasis

Offset Address: 6Ah (B0D15F0)
AFE Control Register 7
Default Value: 02h

Bit	Attribute	Default	Description
7:4	—	0	Reserved
3	RW	0	Mode Select 0: Auto Mode 1: Manual Mode
2	RW	0	Manual Setting - 50-ohm Termination Bit 2
1	RW	1	Manual Setting - 50-ohm Termination Bit 1
0	RW	0	Manual Setting - 50-ohm Termination Bit 0

Offset Address: 6Bh (B0D15F0)
AFE Control Register 8
Default Value: 0Ah

Bit	Attribute	Default	Description
7:4	—	0	Reserved
3	RO	1	Autocomp Value
2	RO	0	Autocomp Values of Termination Bit 2
1	RO	1	Autocomp Values of Termination Bit 1
0	RO	0	Autocomp Values of Termination Bit 0

Offset Address: 6Ch (B0D15F0)
AFE Control Register 9
Default Value: 00h

Bit	Attribute	Default	Description
7	RW	0	Duty-balance Control Rising Time for Serial Data Port A Bit 1
6	RW	0	Duty-balance Control Rising Time for Serial Data Port A Bit 0
5	RW	0	Duty-balance Control Falling Time for Serial Data Port A Bit 1
4	RW	0	Duty-balance Control Falling Time for Serial Data Port A Bit 0
3	RW	0	Duty-balance Control Rising Time for Serial Data Port B Bit 1
2	RW	0	Duty-balance Control Rising Time for Serial Data Port B Bit 0
1	RW	0	Duty-balance Control Falling Time for Serial Data Port B Bit 1
0	RW	0	Duty-balance Control Falling Time for Serial Data Port B Bit 0

(DR0,DR1)=(0,0) (DF0,DF1)=(1,1) could increase 100ps for high time

(DR0,DR1)=(0,0) (DF0,DF1)=(1,0) could increase 40ps for high time

(DR0,DR1)=(1,1) (DF0,DF1)=(0,0) could increase 100ps for low time

(DR0,DR1)=(1,0) (DF0,DF1)=(0,0) could increase 40ps for high time

Offset Address: 6Dh (B0D15F0)
AFE Control Register 10

Default Value: 00h

Bit	Attribute	Default	Description
7	RW	0	Duty-balance Control Rising Time for Serial Data Port C Bit 1
6	RW	0	Duty-balance Control Rising Time for Serial Data Port C Bit 0
5	RW	0	Duty-balance Control Falling Time for Serial Data Port C Bit 1
4	RW	0	Duty-balance Control Falling Time for Serial Data Port C Bit 0
3	RW	0	Duty-balance Control Rising Time for Serial Data Port D Bit 1
2	RW	0	Duty-balance Control Rising Time for Serial Data Port D Bit 0
1	RW	0	Duty-balance Control Falling Time for Serial Data Port D Bit 1
0	RW	0	Duty-balance Control Falling Time for Serial Data Port D Bit 0

Offset Address: 6Eh (B0D15F0)
AFE Control Register 11

Default Value: 91h

Bit	Attribute	Default	Description
7:4	RW	9h	Port Driver Current Source Bit [3:0] for Gen2
3:2	RW	00b	Reserved
1:0	RW	01b	Squelch Window Select Bit [1:0] forGen2

Misc. Registers (78-87h)
Offset Address: 78h (B0D15F0)
SATA I Primary Channel Transport Status 1

Default Value: 01h

Bit	Attribute	Default	Description
7:5	—	0	Reserved
4	RO	0	Primary Channel DMA Read Device Cycle Active
3	RO	0	Primary Channel DMA Write Device Cycle Active
2	RO	0	Primary Channel SG Operation Active
1	RO	0	Primary Channel Interrupt Status
0	RO	1	Primary Channel FIFO Empty Status

Offset Address: 79h (B0D15F0)
SATA I Primary Channel Transport Status 2

Default Value: 00h

Bit	Attribute	Default	Description
7:5	—	0	Reserved
4	RO	0	Primary Channel Slave Drive Select
3	RO	0	Transmit PIO Data Cycle Active
2	RO	0	Receive PIO Data Cycle Active
1	RO	0	Transmit DMA Data Cycle Active
0	RO	0	Receive DMA Data Cycle Active

Offset Address: 7Ah (B0D15F0)
SATA I Secondary Channel Transport Status 1

Default Value: 01h

Bit	Attribute	Default	Description
7:5	—	0	Reserved
4	RO	0	Secondary Channel DMA Read Device Cycle Active
3	RO	0	Secondary Channel DMA Write Device Cycle Active
2	RO	0	Secondary Channel SG Operation Active
1	RO	0	Secondary Channel Interrupt Status
0	RO	1	Secondary Channel FIFO Empty Status

Offset Address: 7Bh (B0D15F0)
SATA I Secondary Channel Transport Status 2
Default Value: 00h

Bit	Attribute	Default	Description
7:5	—	0	Reserved
4	RO	0	Primary Channel Slave Drive Select
3	RO	0	Transmit PIO Data Cycle Active
2	RO	0	Receive PIO Data Cycle Active
1	RO	0	Transmit DMA Data Cycle Active
0	RO	0	Receive DMA Data Cycle Active

Offset Address: 7Dh (B0D15F0)
External PHY Status
Default Value: 00h

Bit	Attribute	Default	Description
7	RO	0	Internal PHY Port 4 Receive COMINIT
6	RO	0	Internal PHY Port 4 Receive COMWAKE
5	RO	0	Internal PHY Port 3 Receive COMINIT
4	RO	0	Internal PHY Port 3 Receive COMWAKE
3	RO	0	Internal PHY Port 2 Receive COMINIT
2	RO	0	Internal PHY Port 2 Receive COMWAKE
1	RO	0	Internal PHY Port 1 Receive COMINIT
0	RO	0	Internal PHY Port 1 Receive COMWAKE

Offset Address: 80h (B0D15F0)
Port Select
Default Value: 00h

Bit	Attribute	Default	Description
7:2	—	0	Reserved
1:0	RW	0	Port Select for (1) Parsing FIS Number When in Device Mode (2) Rx87-84 Status
		00: Port 1	01: Port 2
		00: Port 3	01: Port 4

Offset Address: 81h (B0D15F0)
Port Select
Default Value: 00h

Bit	Attribute	Default	Description
7:0	RO	0	Parsing FIS Number When in Device Mode The port select is based on Rx80[1:0]

Offset Address: 84h (B0D15F0)
Advanced Host Controller Interface (AHCI) Status 1
Default Value: 00h

Bit	Attribute	Default	Description
7	RO	0	Fixed at 0
6	RO	0	AHCI is fetching command list
5	RO	0	AHCI is fetching command FIS
4	RO	0	AHCI is fetching ATAPI command
3	RO	0	AHCI PRD Operation Active
2	RO	0	AHCI Queue Command Cycle Active
1	RO	0	AHCI RDMA Cycle Active
0	RO	0	AHCI WDMA Cycle Active

Offset Address: 85h (B0D15F0)
AHCI Status 2
Default Value: 00h

Bit	Attribute	Default	Description
7:6	RO	0	Fixed at 0
5	RO	0	AHCI D2H Interrupt Status
4	RO	0	AHCI FIFO Empty Status
3	RO	0	AHCI PRD Prefetch Buffer Empty Status
2	RO	0	AHCI is fetching PRD
1	RO	0	AHCI is transferring PRD data
0	RO	0	AHCI is fetching PRD from internal prefetch buffer

Offset Address: 87-86h (B0D15F0)
AHCI Transport State Machine Encoding Bits
Default Value: 0000h

Bit	Attribute	Default	Description
15:12	RO	0	Fixed at 0
11:0	RO	0	AHCI Transport State Machine Encoding Registers

SATA I SCR Registers (A0-BFh)
Offset Address: A0h (B0D15F0)
Primary Channel Master Device Status (Sstatus)
Default Value: 00h

Bit	Attribute	Default	Description
7:5	—	0	Reserved
4	RO	0	SATA Generation II (3G) Status
3	RO	0	SLUMBER Interface Power Management State
2	RO	0	PARTIAL Interface Power Management State
1	RO	0	PHY Ready Status
0	RO	0	Device Detection Status

Offset Address: A1h (B0D15F0)
Primary Channel Slave Device Status (Sstatus)
Default Value: 00h

Bit	Attribute	Default	Description
7:0	RO	00	Primary Channel Slave Device Status

Offset Address: A2h (B0D15F0)
Secondary Channel Master Device Status (Sstatus)
Default Value: 00h

Bit	Attribute	Default	Description
7:0	RO	00	Secondary Channel Master Device Status

Offset Address: A3h (B0D15F0)
Secondary Channel Slave Device Status (Sstatus)
Default Value: 00h

Bit	Attribute	Default	Description
7:0	RO	00	Secondary Channel Slave Device Status

Offset Address: A4h (B0D15F0)
Primary Channel Master Device Control (Scontrol)
Default Value: 0Ch

Bit	Attribute	Default	Description
7:4	—	0	Reserved
3	RW	1	Transition to SLUMBER Power Management State Disabled
2	RW	1	Transition to PARTIAL Power Management State Disabled
1	RW	0	Disable SATA Interface And Put PHY In Offline Mode
0	RO	0	Perform SATA Interface Communication Initialization Sequence to Establish Communication

Offset Address: A5h (B0D15F0)
Primary Channel Slave Device Control (Scontrol)
Default Value: 0Ch

Bit	Attribute	Default	Description
7:0	RW	0Ch	Primary Channel Slave Device Control

Offset Address: A6h (B0D15F0)
Secondary Channel Master Device Control (Scontrol)
Default Value: 0Ch

Bit	Attribute	Default	Description
7:0	RW	0Ch	Secondary Channel Master Device Control

Offset Address: A7h (B0D15F0)
Secondary Channel Slave Device Control (Scontrol)
Default Value: 0Ch

Bit	Attribute	Default	Description
7:0	RW	0Ch	Secondary Channel Slave Device Control

Offset Address: B3-B0h (B0D15F0)
Primary Channel Master SCR Error
Default Value: 0002 0000h

Bit	Attribute	Default	Description
31:26	—	0	Reserved
25	RW1C	0	Unrecognized FIS Type
24	RW1C	0	Transport State Transition Error
23	RW1C	0	Link Sequence Error
22	RW1C	0	Handshake Error
21	RW1C	0	CRC Error
20	RW1C	0	Disparity Error
19	RW1C	0	10B to 8B Decode Error
18	RW1C	0	COMWAKE Detected
17	RW1C	1	PHY Internal Error
16	RW1C	0	PhyRdy Change ERR: Contains error information for use by host software in determining the appropriate response to the error condition.
15:12	—	0	Reserved
11	RW1C	0	Internal Error
10	RW1C	0	Protocol Error
9	RW1C	0	Non-recovered Persistent Communication or Data Integrity Error
8	RW1C	0	Non-recovered Transient Data Integrity Error
7:2	—	0	Reserved
1	RW1C	0	Recovered Communications Error
0	RW1C	0	Recovered Data Integrity Error

Offset Address: B7-B4h (B0D15F0)
Primary Channel Slave SCR Error
Default Value: 0002 0000h

Bit	Attribute	Default	Description
31:0	RW1C	0002 0000h	Primary Channel Slave SCR Error

Offset Address: BB-B8h (B0D15F0)
Secondary Channel Master SCR Error
Default Value: 0002 0000h

Bit	Attribute	Default	Description
31:0	RW1C	0002 0000h	Secondary Channel Master SCR Error

Offset Address: BF-BCh (B0D15F0)
Secondary Channel Slave SCR Error
Default Value: 0002 0000h

Bit	Attribute	Default	Description
31:0	RW1C	0002 0000h	Secondary Channel Slave SCR Error

Legacy Registers (C0-EBh)
Offset Address: C1-C0h (B0D15F0)
Power Management Capability ID
Default Value: E001h

Bit	Attribute	Default	Description
15:8	RO	E0h	Next Capability The location of the next item in the list is the MSI capability
7:0	RO	01h	Capability ID This pointer is a PCI power management

Offset Address: C3-C2h (B0D15F0)
PME Registers
Default Value: 4002h

Bit	Attribute	Default	Description
15	RO	0	MPE# can be generated from D3 cold
14	RO	1	MPE# can be generated from D3 hot
13	RO	0	D2 is not a supported HBA state
12	RO	0	D1 is not a supported HBA state
11	RO	0	PME# from D0 is not supported
10	RO	0	D2 PM State 0: Not Supported 1: Supported
9	RO	0	D1 PM State 0: Not Supported 1: Supported
8:6	RO	0	Auxiliary Current
5	RO	0	Device Specific Initialization
4	—	0	Reserved
3	RO	0	PME Clock
2:0	RO	010	Power Management Interface Revision Indicates that this function compiles with Revision 1.1 of PCI Power Management Interface Spec.

Offset Address: C5-C4h (B0D15F0)
PME Registers
Default Value: 0000h

Bit	Attribute	Default	Description
15	RW1C	0	PME Status Set when the HBA generates PME#
14:9	—	0	Reserved
8	RW	0	PME Enable
7:2	—	0	Reserved
1:0	RW	0	Power Management Capability Status 00: D0 11: D3 Hot

Offset Address: D1h (B0D15F0)
PATA Enable Method
Default Value: 02h

Bit	Attribute	Default	Description
7:4	—	0	Reserved
3	RW	0	PATA Enable Method 0: PATA will be enabled with RX49[7] = 1 1: PATA will be enabled with RX49[7] = 1 and SATA function enabled
2:0	—	2h	Reserved

Offset Address: D5-D4h (B0D15F0)
Subsystem Vendor ID Back Door Registers
Default Value: 1106h

Bit	Attribute	Default	Description
15:0	RW	1106h	Subsystem Vendor ID (Rx2C-2D) Back Door

Offset Address: D7-D6h (B0D15F0)
Subsystem ID Back Door Registers
Default Value: 3349h

Bit	Attribute	Default	Description
15:0	RW	3349h	Subsystem ID (Rx2E-2F) Back Door

Offset Address: E1-E0h (B0D15F0)
Message Signaled Interrupt Identifiers (MID)
Default Value: 0005h

Bit	Attribute	Default	Description
15:8	RO	0	Next Pointer It is the last item in the list.
7:0	RO	05h	Capability ID

Offset Address: E3-E2h (B0D15F0)
Message Signaled Interrupt Message Control (MC)
Default Value: 0000h

Bit	Attribute	Default	Description
15:8	—	0	Reserved
7	RO	0	64-bit Address Capable
6:4	RW	0	Multiple Message Enable Indicates the number of messages the HBA should assert
3:1	RO	0	Multiple Message Capable Indicates the number of messages the HBA wishes to assert
0	RW	0	MSI Enable

Offset Address: E7-E4h (B0D15F0)
Message Signaled Interrupt Message Address
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:2	RW	0	Address Lower 32 bits of the system specified message address, always DW aligned
10	—	0	Reserved

Offset Address: EB-E8h (B0D15F0)
Message Signaled Interrupt Message Data
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:16	—	0	Reserved
15:0	RW	0	This 16-bit field is programmed by system software if MSI is enabled.

Bus 0 Device 15 Function 1 (B0D15F1) – Enhanced IDE Controller

The Enhanced IDE (Parallel ATA) Controller interface is fully compatible with the SFF 8038i v1.0 specification. There are two sets of software accessible registers -- PCI configuration registers and Bus Master IDE I/O registers. The PCI configuration registers are located in the Bus 0 Device 15 Function 1 PCI configuration space of the VT8251. The Bus Master IDE I/O registers are defined in the SFF8038i v1.0 specification.

Header Registers (0-3Fh)

Offset Address: 1-0h (B0D15F1)

Vendor ID

Default Value: 1106h

Bit	Attribute	Default	Description
15:0	RO	1106h	VIA Technology ID Code

Offset Address: 3-2h (B0D15F1)

Vendor ID

Default Value: 0571h

Bit	Attribute	Default	Description
15:0	RO	0571h	Device ID Code

Offset Address: 5-4h (B0D15F1)

PCI Command

Default Value: 0000h

Bit	Attribute	Default	Description
15:11	—	0	Reserved
10	RW	0	Interrupt Disable
9:3	—	0	Reserved
2	RW	0	Bus Master S/G Operation can be issued only when the “Bus Master” bit is enabled 0: Disable 1: Enable
1	—	0	Reserved
0	RW	0	I/O Space When the “I/O Space” bit is disabled, the device will not respond to any I/O address for both compatible and native mode. 0: Disable 1: Enable

Offset Address: 7-6h (B0D15F1)

Status

Default Value: 0290h

Bit	Attribute	Default	Description
15:14	—	0	Reserved
13	RWC	0	Received Master Abort
12	RWC	0	Received Target Abort
11	—	0	Reserved
10:9	RO	01	DEVSEL# Timing Fixed at 01
8	—	0	Reserved
7	RO	1	Fast Back to Back Capable Fixed at 1
6:5	—	0	Reserved
4	RO	1	Capability List. Fixed at 1
3	RO	0	Interrupt Status
2:0	—	0	Reserved

Offset Address: 8h (B0D15F1)
Revision ID
Default Value: 07h

Bit	Attribute	Default	Description
7:0	RO	07h	Revision ID

Offset Address: 9h (B0D15F1)
Programming Interface
Default Value: 8Ah

Bit	Attribute	Default	Description
7	RO	1	Master IDE Capability Supported Fixed at 1
6:4	—	000	Reserved
3	RO	1	Secondary Channel Native Mode Capability Supported
2	RW	0	Channel Operating Mode – Secondary 0: Compatibility Mode 1: Native PCI Mode
1	RO	1	Primary Channel Native Mode Capability Supported
0	RW	0	Channel Operating Mode – Primary 0: Compatibility Mode 1: Native PCI Mode Note: [7:0] will be RO when Rx0A (Sub Class Code) is RAID Controller (default = 04h)

Offset Address: 0Ah (B0D15F1)
Sub Class Code
Default Value: 01h

Bit	Attribute	Default	Description
7:0	RO	01h	Sub Class Code 01: IDE Controller 04: RAID controller

Offset Address: 0Bh (B0D15F1)
Base Class Code
Default Value: 01h

Bit	Attribute	Default	Description
7:0	RO	01h	Base Class Code Fixed at 01h (mass storage controller)

Offset Address: 0Ch (B0D15F1)
Cache Line Size
Default Value: 00h

Bit	Attribute	Default	Description
7:0	RO	00h	Cache Line Size

Offset Address: 0Dh (B0D15F1)
Latency Timer
Default Value: 00h

Bit	Attribute	Default	Description
7:4	RW	0	Latency Timer
3:0	RO	0	Fixed at 0

Offset Address: 0Eh (B0D15F1)
Header Type
Default Value: 00h

Bit	Attribute	Default	Description
7	RO	0	Multiple Function Device
6:0	RO	0	Fixed at 0

Offset Address: 13-10h (B0D15F1)
Primary Data / Command Base Address
Default Value: 0000 0000h

Specifies an 8 byte I/O address space.

Bit	Attribute	Default	Description
31:16	—	00h	Reserved. Must be 0
15:3	RW	00h	Port Address
2	RO	0	Fixed at 0
1:0	RO	00	I/O Cycle

Note:

1. RO when during Compatibility Mode and its value is always 0000 0000h.
2. Default is 1F1h when during Native Mode.
3. Reset to default (1F1h) when changing from native to compatible if Rx72[5] is set. If Rx72[5] is cleared, this field will be kept when changing from native to compatible.

Offset Address: 17-14h (B0D15F1)
Primary Control / Status Base Address
Default Value: 0000 0000h

Specifies a 4 byte I/O address space.

Bit	Attribute	Default	Description
31:16	—	00h	Reserved. Must be 0
15:2	RW	00h	Port Address
1:0	RO	00	I/O Cycle

Note:

1. RO when during Compatibility Mode and its value is always 0000 0000h.
2. Default is 3F5h when during Native Mode.
3. Only the third byte is active, default: 3F6h
4. Reset to default (3F5h) when changing from native to compatible if Rx72[5] is set. If Rx72[5] is cleared, this field will be kept when changing from native to compatible.

Offset Address: 1B-18h (B0D15F1)
Secondary Data / Command Base Address
Default Value: 0000 0000h

Specifies an 8 byte I/O address space.

Bit	Attribute	Default	Description
31:16	—	00h	Reserved. Must be 0
15:3	RW	00h	Port Address
2	RO	0	Fixed at 0
1:0	RO	00	I/O Cycle

Note:

1. RO when during Compatibility Mode and its value is always 0000 0000h.
2. Default is 171h when during Native Mode.
3. Reset to default (171h) when changing from native to compatible if Rx72[5] is set. If Rx72[5] is cleared, this field will be kept when changing from native to compatible.

Offset Address: 1F-1Ch (B0D15F1)
Secondary Control / Status Base Address
Default Value: 0000 0000h

Specifies a 4 byte I/O address space.

Bit	Attribute	Default	Description
31:16	—	00h	Reserved. Must be 0
15:2	RW	00h	Port Address
1:0	RO	00	I/O Cycle

Note:

1. RO when during Compatibility Mode and its value is always 0000 0000h.
2. Default is 375h when during Native Mode.
3. Only the third byte is active, default: 376h
4. Reset to default (375h) when changing from native to compatible if Rx72[5] is set. If Rx72[5] is cleared, this field will be kept when changing from native to compatible.

Offset Address: 23-20h (B0D15F1)
But Master Control Registers Base Address
Default Value: 0000 CC01h

Specifies a 16 byte I/O address space and detailed information in the next section.

Bit	Attribute	Default	Description
31:16	—	00h	Reserved. Must be 0
15:4	RW	CC0h	Port Address
3:2	RO	00	Fixed at 0
1:0	RO	01	I/O Cycle

Offset Address: 2D-2Ch (B0D15F1)
Subsystem Vendor
Default Value: 1106h

Bit	Attribute	Default	Description
15:0	RO	1106h	Subsystem Vendor ID The read back value can be changed by writing to RxD4-D5

Offset Address: 2F-2Eh (B0D15F1)
Subsystem ID
Default Value: 0571h

Bit	Attribute	Default	Description
15:0	RO	0571h	Subsystem ID The read back value can be changed by writing to RxD6-D7

Offset Address: 34h (B0D15F1)
PCI Power Management Capability Pointer
Default Value: C0h

Bit	Attribute	Default	Description
7:0	RO	C0h	Capability Pointer

Offset Address: 3Ch (B0D15F1)
Interrupt Line
Default Value: 00h

Bit	Attribute	Default	Description
7:4	—	0	Reserved
3:0	RW	0	IDE Interrupt Line Routing (native mode only) If modify bit [7:4] to 1111b, route to IRQ0 Others are decoded to IRQ0 ~ IRQ15

Offset Address: 3Dh (B0D15F1)
Interrupt Pin
Default Value: 00h

Bit	Attribute	Default	Description
7:0	RO	0	Interrupt Pin Routing Mode 01h: Native mode interrupt pin routing 00h: Compatibility mode interrupt pin routing

Offset Address: 3F-3Eh (B0D15F1)
Minimum Grant and Maximum Latency
Default Value: 0000h

Bit	Attribute	Default	Description
15:0	RO	0	Minimum Grant and Maximum Latency

IDE-Controller-Specific Configuration Registers (40-A0h)
Offset Address: 40h (B0D15F1)
Chip Enable
Default Value: 08h

Bit	Attribute	Default	Description
7:2	—	02h	Reserved
1	RW	0	IDE Primary Channel Enable 0: Disable 1: Enable
0	RW	0	IDE Secondary Channel Enable 0: Disable 1: Enable

Offset Address: 41h (B0D15F1)
IDE Configuration
Default Value: 02h

Bit	Attribute	Default	Description
7	RW	0	Primary IDE PIO Read Prefetch Enable 0: Disable 1: Enable
6	RW	0	Primary IDE PIO Post Write Enable 0: Disable 1: Enable
5	RW	0	Secondary IDE PIO Read Prefetch Enable 0: Disable 1: Enable
4	RW	0	Secondary IDE PIO Post Write Enable 0: Disable 1: Enable
3:0	—	0010	Reserved

Offset Address: 42h (B0D15F1)
Miscellaneous Control
Default Value: 09h

Bit	Attribute	Default	Description
7	RW	0	PIO Operating Mode – Primary Channel Selects the mode used in the primary channel for the I/O Base Address (not IRQ routing or sharing) 0: Compatibility Mode (fixed addressing) 1: Native PCI Mode (flexible addressing)
6	RW	0	PIO Operating Mode – Secondary Channel Selects the mode used in the secondary channel for the I/O Base Address (not IRQ routing or sharing) 0: Compatibility Mode (fixed addressing) 1: Native PCI Mode (fixed addressing)
5	RW	0	Interrupt Operation Mode – Primary 0: Compatibility mode (fixed interrupt) 1: Native mode (flexible interrupt)
4	RW	0	Interrupt Operation Mode – Secondary 0: Compatibility mode (fixed interrupt) 1: Native mode (flexible interrupt)
3:0	—	9h	Reserved

Note:

1. Bit [7:4] are read only when Rx0A (Sub Class Code) = 04h (RAID mode)
2. Do not program Rx42[7:4]

Offset Address: 43h (B0D15F1)
FIFO Configuration
Default Value: 05h

Bit	Attribute	Default	Description
7:4	—	0	Reserved
3:2	RW	01	Primary Channel FIFO Threshold Determines the threshold required before the primary channel FIFO is flushed. 00: FIFO flushed when 1/4 full 01: FIFO flushed when 1/2 full 10: FIFO flushed when 3/4 full 11: FIFO flushed when completed full (Can not be used when UDMA is read)
1:0	RW	01	Secondary Channel FIFO Threshold Determines the threshold required before the secondary channel FIFO is flushed 00: FIFO flushed when 1/4 full 01: FIFO flushed when 1/2 full 10: FIFO flushed when 3/4 full 11: FIFO flushed when completed full (Can not be used when UDMA is read)

Note:

1. If RX72[4] = 1, bit 3-0 is only threshold for device to memory transfer.
2. if RX72[4] = 0, bit 3-0 is threshold for both device to memory and memory to device transfer. (default)

Offset Address: 44h (B0D15F1)
Miscellaneous Control
Default Value: 08h

Bit	Attribute	Default	Description
7:5	—	00h	Reserved
4	RW	0	PIO Read Pre-Fetch Byte Counter Determines whether the amount of data prefetched under PIO read is limited 0: Disable (no limit) 1: Enable. The maximum number of bytes that can be prefetched is determined by Rx61-60[11:0] for the Primary channel and Rx69-68[11:0] for the secondary channel
3	RW	1	Bus Master IDE Status Register Read Retry Determines whether a read to the bus master IDE status register is retried when DMA operation is not complete. 0: Disable. Reads will return status even if DMA operation is not complete 1: Enable. Reads of the status register are automatically retried while DMA operation is not complete.
2	RW	0	Packet Command Prefetching Determines whether prefetching is enabled for packet commands. Packet commands are commands for ATAPI, which is used for operating devices such as CD-ROM drives. 0: Disable default 1: Enable
1	—	0	Reserved
0	RW	0	UltraDMA Host Must Wait for First Transfer Before Termination 0: Enable. The UltraDMA host must wait until at least the first transfer is completed before it can terminate a transaction. 1: Disable

Offset Address: 45h (B0D15F1)
Miscellaneous Control
Default Value: 80h

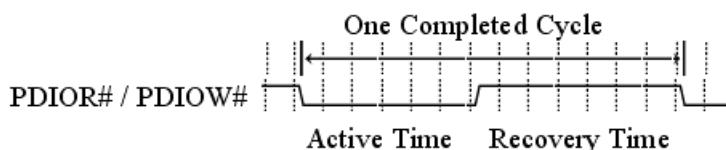
Bit	Attribute	Default	Description
7	RW	1	Rx0A (Sub Class Code) Write Protect 0: Disable (writes to Rx0A are allowed) 1: Enable (writes to Rx0A are ignored)
6	RW	0	Interrupt Steering Swap Controls whether primary and secondary channel interrupts are swapped. 0: Primary channel interrupt is steered to IRQ14, Secondary channel is steered to IRQ15 1: Primary channel interrupt is steered to IRQ15, Secondary channel interrupt is steered to IRQ14
5	—	0	Reserved
4	RW	0	Rx3C (Interrupt Line) Write Protect 0: Disable (writes to Rx3C are allowed) 1: Enable (writes to Rx3C are ignored)
3	RW	0	“Memory-Read-Multiple” Command 0: Disable 1: Enable
2	RW	0	“Memory-Write-and-Invalidate” Command 0: Disable 1: Enable
1	RW	0	Force Internal Clock as 100MHz Clock Source 0: Disable 1: Enable
0	—	0	Reserved

Offset Address: 46h (B0D15F1)
Miscellaneous Control
Default Value: C0h

Bit	Attribute	Default	Description
7	RW	1	Primary Channel Read DMA FIFO Flush 0: Disable 1: Enable. The primary channel DMA FIFO is flushed when an interrupt request is generated
6	RW	1	Secondary Channel Read DMA FIFO Flush 0: Disable 1: Enable. The secondary channel DMA FIFO is flushed when an interrupt request is generated
5:4	—	0	Reserved
3	RW	0	IDE Pipeline Feature Enable for Fetching Scatter / Gather Descriptor Pipeline feature will be enabled when this bit and PCI11 (Rx 50[7] in D17F7) both set to 1.
2	RW	0	Scatter / Gather Descriptor Pre-Fetch Cache Feature Enable
1:0	—	0	Reserved

Offset Address: 4B-48h (B0D15F1)
IDE Drive Timing Control
Default Value: A8A8 A8A8h

The following fields define the Active Pulse Width and Recovery Time for the IDE PDIOR# and PDIOW# signals when accessing the data ports (1F0 and 170):



The actual value for each field is the encoded value in the field plus one and indicates the number of PCI clocks. For example, if the value in the field is 1010b (10 decimal), the active pulse width or recovery time is 11 PCI clocks.

Bit	Attribute	Default	Description
31:28	RW	1010b	Primary Drive 0 Active Pulse Width
27:24	RW	1000b	Primary Drive 0 Recovery Time
23:20	RW	1010b	Primary Drive 1 Active Pulse Width
19:16	RW	1000b	Primary Drive 1 Recovery Time
15:12	RW	1010b	Secondary Drive 0 Active Pulse Width
11:8	RW	1000b	Secondary Drive 0 Recovery Time
7:4	RW	1010b	Secondary Drive 1 Active Pulse Width
3:0	RW	1000b	Secondary Drive 1 Recovery Time

Note: PIO Data Port (1F0 and 170h) access timing control and Multi-Word DMA cycle timing control, timing = (Program Value + 1) * 30 ns.

Offset Address: 4Ch (B0D15F1)
Address Setup Time
Default Value: FFh

The following fields define the Address Setup Time. The Address Setup Time is measured from the point when address signals are stable to the point when PDIOR# and PDIOW# are asserted. The IDE specification requires the setup time to not exceed 1T. However, the VT8251 provides flexibility for devices that may not be able to meet the 1T requirement.

Bit	Attribute	Default	Description
7:6	RW	11	Primary Drive 0 Address Setup Time 00: 1T 10: 3T 11: 4T
5:4	RW	11	Primary Drive 1 Address Setup Time (Slave) 00: 1T 10: 3T 11: 4T
3:2	RW	11	Secondary Drive 0 Address Setup Time (Master) 00: 1T 10: 3T 11: 2T 11: 4T
1:0	RW	11	Secondary Drive 1 Address Setup Time (Slave) 00: 1T 10: 3T 11: 2T 11: 4T

Note: Timing = (Program Value + 1) * 30 ns, 1T = 30ns.

Offset Address: 4Eh (B0D15F1)
Secondary IDE Drive Non-Data Port Access Timing
Default Value: B6h

Bit	Attribute	Default	Description
7:4	RW	0Bh	PDIOR# / PDIOW# Active Pulse Width
3:0	RW	06h	PDIOR# / PDIOW# Recovery Time

Note: Secondary IDE Non-Data Port (171h ~ 177h) access timing control, timing = (Program Value + 1) * 30ns.

Offset Address: 4Fh (B0D15F1)
Primary IDE Drive Non-Data Port Access Timing
Default Value: B6h

Bit	Attribute	Default	Description
7:4	RW	0Bh	PDIOR# / PDIOW# Active Pulse Width
3:0	RW	06h	PDIOR# / PDIOW# Recovery Time

Note: Secondary IDE Non-Data Port (1F1h ~ 1F7h) access timing control, timing = (Program Value + 1) * 30ns.

Offset Address: 50h (B0D15F1)
Secondary IDE Drive 1 (Slave) Ultra DMA Mode Control
Default Value: 07h

Bit	Attribute	Default	Description
7	RW	0	UltraDMA Source Mode Enable 0: Set feature command 1: Register feature command
6	RW	0	UltraDMA Mode Enable 0: Disable 1: Enable
5	RO	0	Current Transfer Mode 0: PIO or DMA Mode 1: UltraDMA Mode
4	RW	0	Cable Type Reporting 0: 40-pin cable is being used 1: 80-pin cable is being used
3:0	RW	0111	Ultra DMA Write Strobe Timing Control 0: (Program Value + 2) * 7.5ns 1: (Program Value + 2) * 10ns (Ultra DMA 100 Using) 2-15: (Program Value + 2) * 7.5ns

Offset Address: 51h (B0D15F1)
Secondary IDE Drive 0 (Master) Ultra DMA Mode Control
Default Value: 07h

Bit	Attribute	Default	Description
7	RW	0	UltraDMA Source Mode Enable 0: Set feature command 1: Register feature command
6	RW	0	UltraDMA Mode Enable 0: Disable 1: Enable
5	RO	0	Current Transfer Mode 0: PIO or DMA Mode 1: UltraDMA Mode
4	RW	0	Cable Type Reporting 0: 40-pin cable is being used 1: 80-pin cable is being used
3:0	RW	0111b	Ultra DMA Write Strobe Timing Control 0: (Program Value + 2) * 7.5ns 1: (Program Value + 2) * 10ns (Ultra DMA 100 Using) 2-15: (Program Value + 2) * 7.5ns

Offset Address: 52h (B0D15F1)
Primary IDE Drive 1 (Slave) Ultra DMA Mode Control
Default Value: 07h

Bit	Attribute	Default	Description
7	RW	0	UltraDMA Source Mode Enable 0: Set Feature Command 1: Register Feature Command
6	RW	0	UltraDMA Mode Enable 0: Disable 1: Enable
5	RO	0	Current Transfer Mode 0: PIO or DMA Mode 1: UltraDMA Mode
4	RW	0	Cable Type Reporting 0: 40-pin cable is being used 1: 80-pin cable is being used
3:0	RW	0111b	Ultra DMA Write Strobe Timing Control 0: (Program Value + 2) * 7.5ns 1: (Program Value + 2) * 10ns (Ultra DMA 100 Using) 2-15: (Program Value + 2) * 7.5ns

Offset Address: 53h (B0D15F1)
Primary IDE Drive 0 (Master) Ultra DMA Mode Control
Default Value: 07h

Bit	Attribute	Default	Description
7	RW	0	UltraDMA Source Mode Enable 0: Set Feature Command 1: Register Feature Command
6	RW	0	UltraDMA Mode Enable 0: Disable 1: Enable
5	RO	0	Current Transfer Mode 0: PIO or DMA Mode 1: UltraDMA Mode
4	RW	0	Cable Type Reporting 0: 40-pin cable is being used 1: 80-pin cable is being used
3:0	RW	0111b	Ultra DMA Write Strobe Timing Control 0: (Program Value + 2) * 7.5ns 1: (Program Value + 2) * 10ns (Ultra DMA 100 Using) 2-15: (Program Value + 2) * 7.5ns

Offset Address: 54h (B0D15F1)
Revision
Default Value: 0Ch

Bit	Attribute	Default	Description
7	RW	0	Enable Legacy IRQ14 or IRQ15 Usage when IDE Channel is disabled 0: Enable. Release IRQ14 when Rx40[1] is cleared, release IRQ15 when Rx40[0] is cleared. 1: Disable
6	—	0	Reserved
5	RW	0	Clear Native Mode Interrupt on Falling Edge of Gated Interrupt 0: Disable 1: Enable. The interrupt will be automatically cleared on the falling edge of the gated interrupt.
4	RW	0	Improve PIO Prefetch and Post-Write Performance 0: Enable. PIO prefetch and post write performance is increased by being given higher throughput 1: Disable
3	RW	1	Memory Prefetch Size This bit determines how many lines are prefetched from memory for IDE transactions. 0: Prefetch 1 line 1: Prefetch 2 lines (16 DoubleWords). This setting improves UDMA100/133 throughput.
2	RW	1	Change Drive Clears All FIFO & Internal States 0: Disable 1: Command switch from one drive to another drive in the same channel terminates all previous outstanding transactions involving the previous drive.
1:0	—	0	Reserved

Offset Address: 55h (B0D15F1)
IDE Clock Gating
Default Value: 00h

Bit	Attribute	Default	Description
7:2	—	0	Reserved
1	RW	0	Dynamic 100/133 MHz Clock Gating 0: Enable 1: Disable
0	RW	0	Dynamic 66 MHz Clock Gating 0: Enable 1: Disable

Offset Address: 61-60h (B0D15F1)
Primary IDE Sector Size
Default Value: 0200h

Bit	Attribute	Default	Description
15:12	—	0	Reserved
11:0	RW	200h	Prefetch Sector Size

Offset Address: 69-68h (B0D15F1)
Secondary IDE Sector Size
Default Value: 0200h

Bit	Attribute	Default	Description
15:12	—	0	Reserved
11:0	RW	200h	Prefetch Sector Size

Offset Address: 70h (B0D15F1)
Primary IDE Status
Default Value: 02h

Bit	Attribute	Default	Description
7	RO	0	Interrupt Status 1: Primary channel interrupt request pending
6	RO	0	PIO Prefetch Status 1: PIO Prefetch transaction in progress
5	RO	0	PIO Post Write Status 1: PIO Post Write transaction in progress
4	RO	0	DMA Read Operation Status 1: DMA Read Prefetch transaction in progress
3	RO	0	DMA Write Operation Status 1: DMA Write transaction in progress
2	RO	0	Bus Master Operation Complete 1: Bus Master transaction in progress
1	RO	1	FIFO Empty Status 1: Primary Channel FIFO empty
0	RO	0	Response to External DMA Request 1: External primary channel DMA request pending

Offset Address: 71h (B0D15F1)
Primary Interrupt Gating
Default Value: 01h

Bit	Attribute	Default	Description
7:1	—	0	Reserved
0	RW	1	Interrupt Gating 0: Disable 1: Enable (IRQ output gated until FIFO empty)

Offset Address: 72h (B0D15F1)
Miscellaneous Control
Default Value: 25h

Bit	Attribute	Default	Description
7:6	—	0	Reserved
5	RW	1	Enable Reset I/O Base Address When Changing from Native Mode to Compatible Mode 0: Disable 1: Enable
4	RW	0	Separate FIFO Threshold Usage Enable 0: Disable 1: Enable
3:2	RW	01	Primary Channel FIFO Threshold (Memory to Device)
1:0	RW	01	Secondary Channel FIFO Threshold (Memory to Device) 00: 1/4 01: 1/2 10 3/4 11 1

Offset Address: 78h (B0D15F1)
Secondary IDE Status
Default Value: 02h

Bit	Attribute	Default	Description
7	RO	0	Interrupt Status 1: Secondary channel interrupt request pending
6	RO	0	PIO Prefetch Status 1: PIO Prefetch transaction in progress
5	RO	0	PIO Post Write Status 1: PIO Post Write transaction in progress
4	RO	0	DMA Read Operation Status 1: DMA Read Prefetch transaction in progress
3	RO	0	DMA Write Operation Status 1: DMA Write transaction in progress
2	RO	0	Bus Master Operation Complete 1: Bus Master transaction in progress
1	RO	1	FIFO Empty Status 1: Primary Channel FIFO empty
0	RO	0	Response to External DMA Request 1: External primary channel DMA request pending

Offset Address: 79h (B0D15F1)
Secondary Interrupt Gating
Default Value: 01h

Bit	Attribute	Default	Description
7:1	—	0	Reserved
0	RW	1	Interrupt Gating 0: Disable 1: Enable (IRQ output gated until FIFO empty)

Offset Address: 83-80h (B0D15F1)
Primary Channel Scatter / Gather Descriptor Address
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:2	RW	0000 0000	Primary Channel Scatter / Gather Descriptor Address [31:2]
1:0	RO	00	Primary Channel Scatter / Gather Descriptor Address [1:0]. Fix at 0

Offset Address: 8B-88h (B0D15F1)
Secondary Channel Scatter / Gather Descriptor Address
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:2	RW	0000 0000	Secondary Channel Scatter / Gather Descriptor Address [31:2]
1:0	RO	00	Secondary Channel Scatter / Gather Descriptor Address [1:0]. Fix at 0

Rx83-80 and Rx8B-88 are used for debugging purposes only.

Offset Address: A0h (B0D15F1)
Test Mode Register
Default Value: 00h

Bit	Attribute	Default	Description
7:1	—	00h	Reserved
0	RW	0	Sector Counter Testing Mode 0: Disable 1: Enable

IDE Power Management Registers (C0-D7h)
Offset Address: C3-C0h (B0D15F1)
PCI Power Management Capability
Default Value: 0002 0001h

Bit	Attribute	Default	Description
31:19	RO	0	PM Capabilities
18:16	RO	010	Version – Indicates PCI PM Spec Rev 1.1 Support
15:8	RO	0	Next Capability
7:0	RO	1	Cap ID

This field reports support details for Power Management Capabilities according to the PCI Power Management specification.

Offset Address: C5-C4h (B0D15F1)
Power Management Control / Status
Default Value: 0000h

Bit	Attribute	Default	Description
15:2	—	00h	Reserved
1:0	RW	00b	Power State 00: D0 10: Reserved 01: Reserved 11: D3 Hot

Offset Address: D5-D4h (B0D15F1)
Subsystem Vendor ID Back Door Registers
Default Value: 1106h

Bit	Attribute	Default	Description
15:0	RW	1106h	Subsystem Vendor ID (Rx2C-2D) Back Door

Offset Address: D7-D6h (B0D15F1)
Subsystem ID Back Door Registers
Default Value: 0571h

Bit	Attribute	Default	Description
15:0	RW	0571h	Subsystem ID (Rx2E-2F) Back Door

Bus Master IDE I/O Registers (0-Fh)

These registers are compliant with the SFF 8038I v1.0 standard. Refer to the SFF 8038I v1.0 specification for further details. Rx 23-20h is Bus Master IDE I/O Registers base address.

I/O Offset	Attribute	Default	Description
0h	RW	00h	Primary Channel Bus Master IDE Command
1h	RO	—	Reserved
2h	RW1C	00h	Primary Channel Bus Master Status
7 – 4h	RW	0000 0000h	Primary Channel Bus Master IDE Descriptor Table Pointer
8h	RW	00h	Secondary Channel Bus Master IDE Command
9h	RO	—	Reserved
0Ah	RW1C	00h	Secondary Channel Bus Master Status
0Bh	RO	—	Reserved
0C – 0Fh	RW	0000 0000h	Secondary Channel Bus Master IDE Descriptor Table Pointer

Bus 0 Device 16 Function 0-3 (D16F0-F3) – USB 1.1 UHCI Ports 0-7

This Universal Serial Bus host controller interface is fully compatible with UHCI specification v1.1. There are two sets of software accessible registers: PCI configuration registers and USB I/O registers. The PCI configuration registers are located in the Bus 0 Device 16 Function 0-3 PCI configuration space of the VT8251. The USB I/O registers are defined in UHCI specification v1.1. The registers are identical in the Bus 0 Device 16 Functions 0-3 where each function controls different USB ports (function 0 for ports 0-1, function 1 for ports 2-3, function 2 for ports 4-5, and function 3 for ports 6-7).

PCI Configuration Space Header (0-3Fh)

Offset Address: 1-0h (B0D16F0-F3)

Vendor ID
Default Value: 1106h

Bit	Attribute	Default	Description
15:0	RO	1106h	VIA Technology ID Code

Offset Address: 3-2h (B0D16F0-F3)

Device ID
Default Value: 3038h

Bit	Attribute	Default	Description
15:0	RO	3038h	Device ID Code

Offset Address: 5-4h (B0D16F0-F3)

Command
Default Value: 0000h

Bit	Attribute	Default	Description
15:11	—	00h	Reserved
10	RW	0	Interrupt Disable
9:5	—	0	Reserved
4	RW	0	Memory Write and Invalidate
3	RO	0	Respond To Special Cycle Hardwired to 0 (Does not monitor special cycles)
2	RW	0	Bus Master
1	RW	0	Memory Space
0	RW	0	I/O Space

Offset Address: 7-6h (B0D16F0-F3)

Status
Default Value: 0210h

Bit	Attribute	Default	Description
15:14	—	0	Reserved
13	RW1C	0	Received Master Abort
12	RW1C	0	Received Target Abort
11	—	0	Reserved
10:9	RO	01	DEVSEL# Timing Fixed at 01 00: Fast 10: Slow 01: Medium 11: Reserved
8:4	RO	01h	Fixed at 01h (for PCI PMI)
3	RW1C	0	Interrupt Status
2:0	RO	00	Fixed at 00h (for PCI PMI)

Offset Address: 8h (B0D16F0-F3)

Revision ID
Default Value: nnh

Bit	Attribute	Default	Description
7:0	RO	nnh	Revision ID

Offset Address: 0B-9h (B0D16F0-F3)
Class Code
Default Value: 0C0300h

Bit	Attribute	Default	Description
23:0	RO	0C0300h	Class Code To indicate the USB1.1 Host Controller

Offset Address: 0Ch (B0D16F0-F3)
Cache Line Size
Default Value: 00h

Bit	Attribute	Default	Description
7:0	RW	00h	Cache Line Size

Offset Address: 0Dh (B0D16F0-F3)
Latency Timer
Default Value: 16h

Bit	Attribute	Default	Description
7:0	RW	16h	Latency Timer

Offset Address: 0Eh (B0D16F0-F3)
Header Type Default
Value: 80h

Bit	Attribute	Default	Description
7:0	RO	80h	Header Type

Offset Address: 0Fh (B0D16F0-F3)
BIST
Default Value: 00h

Bit	Attribute	Default	Description
7:0	RO	00h	BIST (Build In Self Test) Fixed at 00h.

Offset Address: 23-20h (B0D16F0-F3)
USB I/O Register Base Address
Default Value: 0000 FCE1h

Bit	Attribute	Default	Description
31:16	—	00h	Reserved
15:5	RW	07E7h	USB I/O Register Base Address Port Address for the base of the 32-byte USB I/O Register block, corresponding to AD[15:5]
4:0	RO	00001	32 Byte Aligned IO Space

Offset Address: 2D-2Ch (B0D16F0-F3)
Subsystem Vendor ID
Default Value: 1106h

Bit	Attribute	Default	Description
15:0	RO	1106h	Subsystem Vendor ID RW if Rx42[4] = 1

Offset Address: 2F-2Eh (B0D16F0-F3)
Subsystem ID
Default Value: 3038h

Bit	Attribute	Default	Description
15:0	RO	3038h	Subsystem ID RW if Rx42[4] = 1

Offset Address: 34h (B0D16F0-F3)
Power Management Capabilities
Default Value: 80h

Bit	Attribute	Default	Description
7:0	RO	80h	Power Management Capabilities Fixed at 80h.

Offset Address: 3Ch (B0D16F0-F3)
Interrupt Line
Default Value: 00h

Bit	Attribute	Default	Description
7:4	—	0000	Reserved
3:0	RW	0000	USB Interrupt Routing 0000: Disabled 0010: Reserved 0100: IRQ4 0110: IRQ6 1000: IRQ8 1010: IRQ10 1100: IRQ12 1110: IRQ14 0001: IRQ1 0011: IRQ3 0101: IRQ5 0111: IRQ7 1001: IRQ9 1011: IRQ11 1101: IRQ13 1111: Disabled

Offset Address: 3Dh (B0D16F0-F1)
Interrupt Pin
Default Value: 01h

Bit	Attribute	Default	Description
7:0	RO	01h	Interrupt Pin Fixed at 01h (INTA#).

Offset Address: 3Dh (B0D16F2-F3)
Interrupt Pin
Default Value: 02h

Bit	Attribute	Default	Description
7:0	RO	02h	Interrupt Pin Fixed at 02h (INTB#).

USB 1.1-Specific Configuration Registers (40-C1h)
Offset Address: 40h (B0D16F0-F3)
Miscellaneous Control 1
Default Value: 40h

Bit	Attribute	Default	Description
7	—	0	Reserved
6	RW	1	Babble Option This bit controls whether the port is disabled when EOF (End-Of-Frame) babble occurs. Babble is unexpected bus activity that persists into the EOF interval. 0: Automatically disable babbled port when EOF babble occurs 1: Do not disable babbled port
5	—	0	Reserved
4	RW	0	Frame Interval Select 0: 1msec frame time 1: 0.1msec frame time
3	RW	0	USB Data Length Option 0: Supports TD length up to 1280 1: Supports TD length up to 1023
2	RW	0	Improve FIFO Latency 0: Improve latency if packet size < 64 bytes 1: Disable improvement
1	RW	0	DMA Option 0: Enhanced performance (8 DW burst access with better FIFO latency) 1: Normal performance (16 DW burst access with normal FIFO latency)
0	—	0	Reserved

Offset Address: 41h (B0D16F0-F3)
Miscellaneous Control 2
Default Value: 10h

Bit	Attribute	Default	Description
7	RW	0	USB 1.1 Improvement for EOP This bit controls whether USB Specification 1.1 or 1.0 is followed when a stuffing error occurs before an EOP (End-Of-Packet). A stuffing error results when the receiver sees seven consecutive ones in a packet. Under USB specification 1.1, when this occurs in the interval just before an EOP, the receiver will accept the packet. Under USB specification 1.0, the packet is ignored. 0: USB Spec 1.1 Compliant (packet accepted) 1: USB Spec 1.0 Compliant (packet ignored)
6:3	—	0	Reserved
2	RW	0	Trap Option Under the UHCI spec, port 60 / 64 is trapped only when its corresponding enable bits are set. When this bit is set, trap can be set without checking the enable bits. 0: Set trap 60/64 status bits without checking enable bits 1: Set trap 60/64 status bits only when trap 60/64 enable bits are set
1	RW	0	A20Gate Pass Through Option This bit controls whether the A20Gate pass-through sequence (as defined in UHCI) is followed. The A20Gate sequence consists of 4 commands. When this bit is 0, the 4-command sequence is followed. When this bit is 1, the last command (write FFh to port 64) is skipped. 0: A20GATE Pass-through command sequence as defined in UHCI 1: Last command skipped
0	—	0	Reserved

Offset Address: 42h (B0D16F0-F3)
Miscellaneous Control 3
Default Value: 03h

Bit	Attribute	Default	Description
7:5	—	0	Reserved
4	RW	0	Subsystem ID / Subsystem Vender ID Back Door Enable Specifies whether Rx2C~2F are RO or RW 0: Read Only 1: Read / Write
3	—	0	Reserved
2	RW	0	Holding Controller till FIFO Gets Enough Data for Transmission 0: Enable 1: Disable
1:0	—	11b	Reserved. Do not program.

Offset Address: 43h (B0D16F0-F3)
Miscellaneous Control 4
Default Value: 00h

Bit	Attribute	Default	Description
7:4	—	0	Reserved
3	RW	0	Continue Transmitting Erroneous Data When FIFO Underrun 0: Enable 1: Disable
2	RW	0	Issue CRC Error Instead of Stuffing Error on FIFO Underrun 0: Enable 1: Disable
1:0	—	0	Reserved

Offset Address: 48h (B0D16F0-F3)
Miscellaneous Control 5
Default Value: 00h

Bit	Attribute	Default	Description
7:3	—	0	Reserved
2	RW	0	Issue Bad CRC5 in SOF After FIFO Underrun 0: Enable 1: Disable
1	RW	0	Lengthen PreSOF Time The preSOF time point determines whether there is enough time in the remaining frame period to perform a 64-byte transaction. It prevents a packet that may not fit in the remaining frame period from being initiated. This bit controls whether the preSOF time point is moved back so that the preSOF time is lengthened. 0: Disable 1: Enable (PreSOF time lengthened)
0	RW	0	Issue Nonzero Bad CRC Code on FIFO Underrun A FIFO underrun occurs when there is no data in the FIFO to supply data transmission. When this occurs, the south bridge invalidates the data by sending an incorrect CRC code to the device. This bit controls the type of incorrect CRC sent. 0: Non zero CRC (recommended) 1: All zero CRC This option isn't really needed any more as non-zero CRC always works.

Offset Address: 49h (B0D16F0-F3)
Miscellaneous Control 6
Default Value: 0Bh

Bit	Attribute	Default	Description
7:2	—	0	Reserved. Bit 3:2 fixed at 10b.
1	RW	1	EHCI Supports PME Assertion in D3 Cold State 0: Not Supported 1: Supported
0	RW	1	UHCI Supports PME Assertion in D3 Cold State 0: Not Supported 1: Supported

Note: Rx49[2:0] can only be written from function 0. Rx49[2:0] is RO for function 1~3.

Offset Address: 4Ah (B0D16F0-F3)
Miscellaneous Control 7
Default Value: A0h

Bit	Attribute	Default	Description
7:3	RW	14h	USB 1.1 Bus Timeout Parameter
2:1	—	0	Reserved
0	RW	0	Use External 60 MHz Clock Set this bit to use external 60 MHz input clock 0: Disable 1: Enable

Offset Address: 4Bh (B0D16F0-F3)
Miscellaneous Control 8
Default Value: 03h

Bit	Attribute	Default	Description
7:1	—	0	Reserved
0	RW	1	Clock Auto Stop Enable 0: Disable. No Stop 1: Enable. Auto Stop

Offset Address: 60h (B0D16F0-F3)
Serial Bus Release Number
Default Value: 10h

Bit	Attribute	Default	Description
7:0	RO	10h	Release Number Fixed at 10h

Offset Address: 83-80h (B0D16F0-F3)
Power Management Capability
Default Value: FFC2 0001h

Bit	Attribute	Default	Description
31:0	RO	FFC2 0001h	Power Management Capability If 49[0] = 1, this register is fixed at FFC20001h. If 49[0] = 0, this register is fixed at 7E0A0001h.

Offset Address: 85-84h (B0D16F0-F3)
Power Management Capability Status
Default Value: 0000h

Bit	Attribute	Default	Description
15	RWC	0	PME Status 0: Not active 1: Active
14:9	—	0	Reserved
8	RW	0	PME Enable 0: Disable 1: Enable
7:2	—	0	Reserved
1:0	RW	0	Power Management Capability Status 00: D0 01: Reserved 10: Reserved 11: D3 Hot

Offset Address: C1-C0h (B0D16F0-F3)
Legacy Support
Default Value: 2000h

Bit	Attribute	Default	Description
15:0	RO/RW/RW1C	2000h	UHCI v1.1 Compliant Refer to UHCI Spec. for detail.

USB 1.1 I/O Registers (0-13h)

These registers are compliant with the UHCI v1.1 standard. Refer to the UHCI v1.1 specification for further details.

Offset Address	Attribute	Default	Description
1 – 0h	RW	0000h	USB Command
3 – 2h	RW1C	0020h	USB Status
5 – 4h	RW	0000h	USB Interrupt Enable
7 – 6h	RW	0000h	Frame Number
0B – 8h	RW	0000h	Frame List Base Address
0Ch	RW	40h	Start of Frame Modify
0F-0Dh	—	00h	Reserved
11 – 10h	RO/RW/RW1C	0480h	Port 0 Status / Control. Refer to UHCI Spec. for detail.
13 – 12h	RO/RW/RW1C	0480h	Port 1 Status / Control. Refer to UHCI Spec. for detail.

Bus 0 Device 16 Function 4 Registers - USB 2.0 EHCI

This Enhanced Serial Bus host controller interface is fully compatible with EHCI specification v1.0. There are two sets of software accessible registers: PCI configuration registers and EHCI Memory I/O registers. The PCI configuration registers are located in the Bus 0 Device 16 Function 4 PCI configuration space of the VT8251. The EHCI Memory I/O registers are defined in EHCI specification v1.0. The registers in this function control USB 2.0 functions.

PCI Configuration Space Header (0-3Fh)

Offset Address: 1-0h (B0D16F4)

Vendor ID

Default Value: 1106h

Bit	Attribute	Default	Description
15:0	RO	1106h	VIA Technology ID Code

Offset Address: 3-2h (B0D16F4)

Device ID

Default Value: 3104h

Bit	Attribute	Default	Description
15:0	RO	3104h	Device ID Code

Offset Address: 5-4h (B0D16F4)

Command

Default Value: 0000h

Bit	Attribute	Default	Description
15:11	—	0	Reserved
10	RW	0	Interrupt Disable
9:5	—	0	Reserved
4	RW	0	Memory Write and Invalidate
3	—	0	Reserved (special cycle monitoring) Fixed at 0
2	RW	0	Bus Master
1	RW	0	Memory Space
0	RW	0	I/O Space

Offset Address: 7-6h (B0D16F4)

Status

Default Value: 0210h

Bit	Attribute	Default	Description
15:14	—	0	Reserved
13	RW1C	0	Received Master Abort
12	RW1C	0	Received Target Abort
11	—	0	Reserved
10:9	RO	01	DEVSEL# Timing Fixed at 01 00: Fast 10: Slow 01: Medium 11: Reserved
8:4	RO	01h	Fixed at 01h (for PCI PMI).
3	RW1C	0	Interrupt Status
2:0	—	0	Reserved

Offset Address: 8h (B0D16F4)

Revision ID

Default Value: nnh

Bit	Attribute	Default	Description
7:0	RO	nnh	Revision ID

Offset Address: 0B-09h (B0D16F4)
Class Code
Default Value: 0C0320h

Bit	Attribute	Default	Description
23:0	RO	0C0320h	Class Code for USB2.0 EHCI Host Controller

Offset Address: 0Ch (B0D16F4)
Cache Line Size
Default Value: 00h

Bit	Attribute	Default	Description
7:0	RW	00h	Cache Line Size

Offset Address: 0Dh (B0D16F4)
Latency Timer
Default Value: 16h

Bit	Attribute	Default	Description
7:0	RW	16h	Latency Timer

Offset Address: 0Eh (B0D16F4)
Header Type
Default Value: 80h

Bit	Attribute	Default	Description
7:0	RO	80h	Header Type

Offset Address: 0Fh (B0D16F4)
BIST
Default Value: 00h

Bit	Attribute	Default	Description
7:0	RO	00h	BIST (Built In Self Test). Fixed at 00h.

Offset Address: 13-10h (B0D16F4)
EHCI Memory Mapped I/O Base Address
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:8	RW	0	EHCI Memory Mapped I/O Registers Base Address Memory Address for the base of the USB 2.0 EHCI I/O Register block, corresponding to AD[31:8]
7:3	—	0	Reserved
2:1	RO	00	Memory Mapping Reads 00b for 32-bit addressing
0	—	0	Reserved

Offset Address: 2D-2Ch (B0D16F4)
Subsystem Vendor ID
Default Value: 1106h

Bit	Attribute	Default	Description
15:0	RO	1106h	Subsystem Vendor ID. RW if Rx42[4] = 1

Offset Address: 2F-2Eh (B0D16F4)
Subsystem ID
Default Value: 3104h

Bit	Attribute	Default	Description
15:0	RO	3104h	Subsystem ID. RW if Rx42[4] = 1

Offset Address: 34h (B0D16F4)
Power Management Capabilities
Default Value: 80h

Bit	Attribute	Default	Description
7:0	RO	80h	Power Management Capabilities. Fixed at 80h.

Offset Address: 3Ch (B0D16F4)
Interrupt Line
Default Value: 00h

Bit	Attribute	Default	Description
7:4	—	0	Reserved
3:0	RW	0	USB Interrupt Routing 0000: Disabled 0010: Reserved 0100: IRQ4 0110: IRQ6 1000: IRQ8 1010: IRQ10 1100: IRQ12 1110: IRQ14 0001: IRQ1 0011: IRQ3 0101: IRQ5 0111: IRQ7 1001: IRQ9 1011: IRQ11 1101: IRQ13 1111: Disabled

Offset Address: 3Dh (B0D16F4)
Interrupt Pin
Default Value: 03h

Bit	Attribute	Default	Description
7:0	RO	03h	Interrupt Pin. Fixed at 03h.

USB 2.0-Specific Configuration Registers (40-FCh)
Offset Address: 40h (B0D16F4)
Miscellaneous Control 1
Default Value: 00h

Bit	Attribute	Default	Description
7	—	0	Reserved
6	RW	0	Babble Option This bit controls whether the port is disabled when EOF (End-Of-Frame) babble occurs. Babble is unexpected bus activity that persists into the EOF interval. When this bit is 0, the port with the EOF babble is disabled. When it is 1, it is not disabled 0: Automatically disable babbled port when EOF babble occurs 1: Do not disable babbled port
5	—	0	Reserved
4	RW	0	Frame Interval Select 0: 125 us micro-frame time 1: 62.5msec frame time
3:2	—	0	Reserved
1	RW	0	DMA Options 0: 16 DW burst access 1: 8 DW burst access
0	—	0	Reserved

Offset Address: 42h (B0D16F4)
Miscellaneous Control 3
Default Value: 03h

Bit	Attribute	Default	Description
7:5	—	0	Reserved
4	RW	0	Subsystem ID and Subsystem Vendor ID Back Door Enable Specifies whether Rx2C~2F are RO or RW 0: Read Only 1: Read / Write
3:0	—	03h	Reserved

Offset Address: 43h (B0D16F4)
Miscellaneous Control 4
Default Value: 00h

Bit	Attribute	Default	Description
7	RW	0	DIS_TERM_ON_H Disable port 8 internal termination resistor in high-speed mode for system test
6	RW	0	DIS_TERM_ON_G Disable port 7 internal termination resistor in high-speed mode for system test
5	RW	0	DIS_TERM_ON_F Disable port 6 internal termination resistor in high-speed mode for system test
4	RW	0	DIS_TERM_ON_E Disable port 5 internal termination resistor in high-speed mode for system test
3	RW	0	DIS_TERM_ON_D Disable port 4 internal termination resistor in high-speed mode for system test
2	RW	0	DIS_TERM_ON_C Disable port 3 internal termination resistor in high-speed mode for system test
1	RW	0	DIS_TERM_ON_B Disable port 2 internal termination resistor in high-speed mode for system test
0	RW	0	DIS_TERM_ON_A Disable port 1 internal termination resistor in high-speed mode for system test

Offset Address: 48h (B0D16F4)
Miscellaneous Control 5
Default Value: BEh

Bit	Attribute	Default	Description
7	RW	1	USB 2.0 EOP Pattern (FEh) Error Check 0: Disable 1: Enable
6	RW	0	Extra-Handshake Error Checking in Isochronous Transaction 0: Disable 1: Enable
5	RW	1	CCA Burst Access 0: Burst Enable 1: Burst Disable
4	RW	1	USB 2.0 Reference Bus Idle Status Set this bit, the hardware references the bus idle status from PHY to check the start and the end of an incoming packet. 0: Disable 1: Enable
3:2	—	1	Reserved
1	RW	1	USB 2.0 CRC16 Check Enable for Toggle Mismatch 0: Disable 1: Enable
0	—	1	Reserved

Offset Address: 49h (B0D16F4)
Miscellaneous Control 6
Default Value: 60h

Bit	Attribute	Default	Description
7	RW	0	Enable MAC Provides More Delay between Transactions The delay parameter is in D16F0 Rx4A 0: Disable 1: Enable
6	RW	1	Enable MAC Provides Timeout to Device When Receiver Detects Error The delay parameter is in D16F0 Rx51 0: Disable 1: Enable
5	RW	1	Clock Auto Stop 0: Disable. No stop 1: Enable. Auto stop
4	RW	0	Disable Auto Power Down Receiver Squelch Detector 0: Auto power down 1: Always power up
3:0	—	0	Reserved

Offset Address: 4Ah (B0D16F4)
MAC Inter-Transaction Delay Parameter
Default Value: 00h

Bit	Attribute	Default	Description
7:0	RW	00h	MAC Inter-Transaction Delay Parameter

Offset Address: 4Bh (B0D16F4)
MAC Turn Around Time Parameter
Default Value: 09h

Bit	Attribute	Default	Description
7	RW	0	EHCI Sleep Time Change Effective when bit5=1 0: 10us 1: 80us
6	RW	0	SOF Disconnect Detection Period 0: Narrow 1: Not Narrow
5	RW	0	EHCI Sleep Time Select 0: 1us 1: 10us
4	RW	0	Issue UTM_SOF When RUN Bit Clears 0: Issuing 1: Disable Issuing
3:0	RW	9h	USB 2.0 MAC Transmit Turn Around Time Parameter

Offset Address: 4Ch (B0D16F4)
PHY Control
Default Value: 02h

Bit	Attribute	Default	Description
7:4	—	0	Reserved
3	RW	0	Sync-Fast Option 0: Disable 1: Enable
2	RW	0	Sync-Jend Option 0: Disable 1: Enable
1:0	RW	10	Squelch Detector Fine Tune

Offset Address: 4Dh (B0D16F4)
PHY Control
Default Value: 03h

Bit	Attribute	Default	Description
7:2	—	0	Reserved
1	RW	1	USB2.0 UTM TX Speed Up 0: Disable 1: Enable
0	RW	1	USB2.0 EHCI Debug Port Support 0: Disable 1: Enable

Offset Address: 50h (B0D16F4)
Test Command
Default Value: 00h

Bit	Attribute	Default	Description
7	—	0	Reserved
6	RW	0	Force EHCI MAC Transmits Data with Erroneous CRC This is for emulation test purpose. 0: Normal 1: CRC error forced
5:0	—	0	Reserved

Offset Address: 51h (B0D16F4)
USB 2.0 MAC Timeout Parameter
Default Value: 60h

Bit	Attribute	Default	Description
7:0	RW	60h	USB 2.0 Receive Timeout Parameter The unit is byte time. According to the core spec, the host controller or a device expecting a response to a transmission must not timeout the transaction if the inter-packet delays in 736 and 816 bit times. The worst round trip delay is 721 bit times.

Offset Address: 59h (B0D16F4)
PHY Control 2
Default Value: 0Bh

Bit	Attribute	Default	Description
7	RW	0	Disable PHY Auto Power-Down Feature When set this bit, if port is suspended or is not EHCI owned, the port will auto power-down. 0: Auto power-down 1: Disable Auto power-down
6:4	—	0	Reserved
3	RW	1	FastLock DPLL fast lock enable 0: Disable 1: Enable
2	RW	0	DPLL Loop Back Enable 0: Disable 1: Enable
1	RW	1	Disable PHY Receiver Including Squelch Detector Power up Time Improvement 0: Enable improvement 1: Disable improvement
0	—	0	Reserved

Offset Address: 5B-5Ah (B0D16F4)
High-Speed Port Pad Termination Resistor Fine Tune
Default Value: 8888h

Bit	Attribute	Default	Description
15:8	RW	88h	CTRL_A[3:0], CTRL_B[3:0]
7:0	RW	88h	CTRL_C[3:0], CTRL_D[3:0]

Offset Address: 5Ch (B0D16F4)
PHY Control 3
Default Value: 53h

Bit	Attribute	Default	Description
7	RW	0	DPLL Zero Phase Start Select 0: ZPS takes 8-bit times to start 1: ZPS takes 4-bit times to start
6:4	RW	101	Delay DPLL Input Data Control
3:2	RW	00	DPLL Track Speed Select
1:0	RW	11	DPLL Lock Speed Select

Offset Address: 5E-5Dh (B0D16F4)
High-Speed Port Pad Termination Resistor Fine Tune
Default Value: 8888h

Bit	Attribute	Default	Description
15:8	RW	88h	CTRL_G[3:0], CTRL_H[3:0]
7:0	RW	88h	CTRL_E[3:0], CTRL_F[3:0]

Offset Address: 60h (B0D16F4)
Serial Bus Release Number
Default Value: 20h

Bit	Attribute	Default	Description
7:0	RO	20h	Serial Bus Release Number Fixed at 20h for USB2.0.

Offset Address: 61h (B0D16F4)
Frame Length Adjustment
Default Value: 20h

Bit	Attribute	Default	Description
7:6	—	0	Reserved
5:0	RW	20h	Frame Length Adjustment

Offset Address: 63-62h (B0D16F4)
Port Wake Capability
Default Value: 0001h

Bit	Attribute	Default	Description
15:1	RW	00h	Port Wake Capability To support 8 Ports, [8:1] is RW and [15:9] is RO
0	RO	1	Port Wake Capability Implement 1: Port Wake Capability is Implemented. 0: Port Wake Capability is not Implemented.

Offset Address: 6B-68h (B0D16F4)
USB Legacy Support Extended Capability
Default Value: 0000 0001h

Bit	Attribute	Default	Description
31:25	RO	0	Reserved
24	RW	0	HC OS Owned Semaphore
23:17	RO	0	Reserved
16	RW	0	HC BIOS Owned Semaphore
15:8	RO	0	Next EHCI Extended Capability Pointer
7:0	RO	1	Capability ID

Offset Address: 6F-6Ch (B0D16F4)
USB Legacy Support Control / Status
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:0	RO/RW/RWIC	0	USB Legacy Support Control / Status Reference EHCI Spec. for detail.

Offset Address: 80h (B0D16F4)
Power Management Capability ID
Default Value: 01h

Bit	Attribute	Default	Description
7:0	RO	01h	Power Management Capability ID

Offset Address: 81h (B0D16F4)
Next Item Pointer
Default Value: 88h

Bit	Attribute	Default	Description
7:0	RO	88h	Next Item Pointer If Rx4D[0] = 1, this register is fixed at 88h If Rx4D[0] = 0, this register is fixed at 00h

Offset Address: 83-82h (B0D16F4)
Power Management Capability
Default Value: FFC2h

Bit	Attribute	Default	Description
15:0	RO	FFC2h	Power Management Capability If D16F0 Rx49[1]= 1, this register is fixed at FFC2h. If D16F0 Rx49[1]= 0, this register is fixed at 7E0Ah.

Offset Address: 85-84h (B0D16F4)
Power Management Capability Control / Status
Default Value: 0000h

Bit	Attribute	Default	Description
15	RWC	0	PME Status 0: Not active 1: Active
14:9	—	0	Reserved
8	RW	0	PME Enable 0: Disable 1: Enable
7:2	—	00h	Reserved
1:0	RW	0	Power State 00: D0 01: D1 10: D2 11: D3 Hot

Offset Address: 88h (B0D16F4)
Debug Port Capability ID
Default Value: 0Ah

Bit	Attribute	Default	Description
7:0	RO	0Ah	Debug Port Capability ID If Rx4D[0] = 1, this register is fixed at 0Ah If Rx4D[0] = 0, this register is fixed at 00h

Offset Address: 89h (B0D16F4)
Next Item Pointer 2
Default Value: 00h

Bit	Attribute	Default	Description
7:0	RO	00h	Next Item Pointer 2

Offset Address: 8B-8Ah (B0D16F4)
Debug Port Base Offset
Default Value: 02A0h

Bit	Attribute	Default	Description
15:0	RO	02A0h	Debug Port Base Offset If Rx4D[0] = 1, this register is fixed at 02A0h If Rx4D[0] = 0, this register is fixed at 0000h

EHCI USB 2.0 Memory I/O Registers

These registers are compliant with the EHCI v1.0 standard. Refer to the EHCI v1.0 specification for further details.

EHCI Capabilities (0-Bh)

Offset Address	Attribute	Default	Description
0h	RO	10h	Capability Register Length
1h	—	00h	Reserved
3 – 2h	RO	0100h	Interface Version Number
7 – 4h	RO	0010 4208h	Structure Parameters If D16F4 Rx4D[0] = 1, fixed at 0010 4208h If D16F4 Rx4D[0] = 0, fixed at 0000 4208h
0B-8h	RO	0000 6872h	Capability Parameters

Host Controller Operations (10-73h)

Offset Address	Attribute	Default	Description
13-10h	RW	0008 0000h	USB Command
17-14h	RW1C	0000 1000h	USB Status
1B-18h	RW	0000 0000h	USB Interrupt Enable
1F-1Ch	RW	0000 0000h	USB Frame Index
23-20h	RO	0000 0000h	4G Segment Selector
27-24h	RW	0000 0000h	Frame List Base Address
2B-28h	RW	0000 0000h	Next Asynchronous List Address
4F-2Ch	—	00h	Reserved
53-50h	RW	0000 0000h	Configured Flag Registers
57-54h	RW1C	0000 3000h	Port 1 Status / Control
5B-58h	RW1C	0000 3000h	Port 2 Status / Control
5F-5Ch	RW1C	0000 3000h	Port 3 Status / Control
63-60h	RW1C	0000 3000h	Port 4 Status / Control
67-64h	RW1C	0000 3000h	Port 5 Status / Control
6B-68h	RW1C	0000 3000h	Port 6 Status / Control
6F-6Ch	RW1C	0000 3000h	Port 7 Status / Control
73-70h	RW1C	0000 3000h	Port 8 Status / Control

Debug Port Controller Operational Registers (A0-B3h)

Offset Address	Attribute	Default	Description
A3-A0h	RW/RO/RW1C	00h	Debug Port Control / Status
A7-A4h	RW/RO	00h	Debug Port USB PIDs
AF-A8h	RW	FFFF FFFF FFFF FFFFh	Debug Port Data Buffer
B3-B0h	RW/RO	07F01h	Debug Port Device Address

Bus 0 Device 17 Function 0 (B0D17F0) - Bus Control and Power Management

All registers are located in the device 17 function 0 configuration space of the VT8251. These registers are accessed through PCI configuration mechanism #1 via I/O address 0CF8h / 0CFCh.

PCI Configuration Space Header (0-3Fh)

Offset Address	Attribute	Default	Description
1 – 0h	RO	1106h	Vendor ID
3 – 2h	RO	3287h	Device ID

Offset Address: 5-4h (B0D17F0)

Command

Default Value: 0003h

Bit	Attribute	Default	Description
15:7	—	0	Reserved
6	RW	0	Parity Error Response 0: Ignore parity error 1: Normal response
5:4	—	0	Reserved
3	RO	0	Special Cycle Enable 0: Disable 1: Enable
2	RO	0	Bus Master
1	RW	1	Memory Space
0	RW	1	I/O Space

Offset Address: 7-6h (B0D17F0)

Status

Default Value: 0210h

Bit	Attribute	Default	Description
15:	RO	0	Detected Parity Error Set only by the master when it detects a parity error
14	RO	0	Signaled System Error Always reads 0
13	RO	0	Signaled Master Abort Note: Set by master when it receive a target abort reset when writing 1
12	RO	0	Received Target Abort Note: Set by master when it receive a target abort reset when writing 1
11	RO	0	Signaled Target Abort Note: Set by target when it terminates a transaction with target abort reset when writing 1
10:9	RO	01b	DEVSEL# Timing 00:Fast 01:Medium 10: Slow 11: Reserved Note: For target device only
8	RO	0	Data Parity Detected Reads 1 if PERR# is asserted (driven or observed) or a bus master data parity error occurred.
7	RO	0	Fast Back-to-Back Capable
6:0	—	10b	Reserved

Note: 1) These signals come from internal logic

2) For these bits not supported or static, please hardwire to 0/1

Offset Address: 8h (B0D17F0)

Revision ID

Default Value: nnh

Bit	Attribute	Default	Description
7:0	RO	nnh	Revision ID

Offset Address: 0B-9h (B0D17F0)

Class Code

Default Value: 060100h

Bit	Attribute	Default	Description
15:0	RO	060100h	Class Code

Offset Address: 0Eh (B0D17F0)
Header Type
Default Value: 80h

Bit	Attribute	Default	Description
7:0	RO	80h	Header Type Multifunction Device

Offset Address: 2F-2Ch (B0D17F0)
Subsystem ID and Subsystem Vendor ID
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:16	RO	0	Subsystem ID The read back value can be changed by writing to backdoor Rx72-73.
15:0	RO	0	Subsystem Vendor ID The read back value can be changed by writing to backdoor Rx70-71.

Offset Address: 73-70h (B0D17F0)
Subsystem ID and Subsystem Vendor ID Back Door Registers
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:16	RW	0	Subsystem ID (Rx2E-2F) Back Door
15:0	RW	0	Subsystem Vendor ID (Rx2C-2D) Back Door

ISA Bus Control (40-49h)
Offset Address: 40h (B0D17F0)
ISA Bus Control
Default Value: 00h

Bit	Attribute	Default	Description	Mnemonic
7	RW	0	Extra / Normal ISA Command Delay 0: Normal 1: External	
6	RW	0	I/O Recovery Time 0: Disable 1: Enable	RIORCV
5	—	0	Reserved	
4	RW	0	ROM Write 0: Disable 1: Enable	
3	RW	0	Double DMA Clock 0: Disable 1: Enable	
2	RW	0	4D0 / 4D1 Support 0: Disable 1: Enable	
1	RW	0	MEGA Cells (dmac, intc, tmrc) Shadow registers read 0: Disable 1: Enable	
0	RW	0	BCLK = PCLK/2 0: Disable 1: Enable	

Offset Address: 41h (B0D17F0)
ROM Decode Control
Default Value: 80h

Setting these bits to 1 enables the indicated address range to be included in the LPC BIOS ROM address decode:

Bit	Attribute	Default	Description
7	RW	1	000E0000 - 000FFFFF
6	RW	0	FFF0000h - FFF7FFFFh FFB0000h - FFB7FFFFh
5	RW	0	FFE80000h - FFEFFFFFFh FFA80000h - FFAFFFFFFh
4	RW	0	FFE00000h - FFE7FFFFh FFA00000h - FFA7FFFFh
3	RW	0	FFD80000h - FFDFFFFFh FF980000h - FF97FFFFh
2	RW	0	FFD00000h - FFD7FFFFh FF900000h - FF97FFFFh
1	RW	0	FFC80000h - FFCFFFFFFh FF880000h - FF87FFFFh
0	RW	0	FFC00000h - FFC7FFFFh FF800000h - FF87FFFFh

Note: The following memory address range for ROM FFF80000-FFFFFFFFFF, FFB80000-FFBFFFFFF and 000F0000-000FFFFF are decoded

Offset Address: 42h (B0D17F0)
Line Buffer Control
Default Value: 00h

Bit	Attribute	Default	Description
7	RW	0	DMA Line Buffer Controls whether the DMA line buffer is used. 0: Disable 1: Enable (Master DMA waits until the line buffer is full (8 DWords) before transmitting data (bit-6 must also be enabled to insure that there are no coherency issues).
6	RW	0	Gate Interrupt Until Line Buffer Flush Complete This bit should be enabled if bit-7 is enabled. 0: Disable 1: Enable INTR is gated until the line buffer is flushed to insure that there are no coherency issues.
5	RW	0	Flush Line Buffer for Interrupt when DMA is not Granted 0: Disable 1: Enable
4	RW	0	Uninterruptible Burst Read 0: Disable 1: Enable The PCI bus is not granted to DMA until burst read transactions from the north bridge are completed.
3	RW	0	Gate Serial IRQ Until Line Buffer Flush Completed 0: Disable 1: Enable
2	RW	0	IRQ Flush Line Buffer When Grant to DMA Even if DMA is granted with Rx42[5]=1 0: Disable 1: Enable
1:0	—	0	Reserved

Offset Address: 43h (B0D17F0)
Delay Transaction Control
Default Value: 00h

Bit	Attribute	Default	Description
7:4	—	0	Reserved
3	RW	0	Delayed Transactions (PCI Spec Rev 2.1) This bit controls whether delayed transactions (delayed read / write and posted write) are enabled. 0: Disable 1: Enable
2	RW	0	Only Posted Write This bit controls whether posted write is enabled, as opposed to bit-3 which controls whether delayed read / write as well as posted write are enabled. 0: Disable 1: Enable
1	RW	0	Write Delay Transaction Timeout Timer When enabled, if a delayed transaction (write cycle only) is not retried after 2^15 PCI clocks, the transaction is terminated. 0: Disable 1: Enable
0	RW	0	Read Delay Transaction Timeout Timer When enabled, if a delayed transaction (read cycle only) is not retried after 2^15 PCI clocks, the transaction is terminated. 0: Disable 1: Enable

Offset Address: 44h (B0D17F0)
PCI PNP Interrupt Routing INTE/F#
Default Value: 00h

Bit	Attribute	Default	Description
7:4	RW	0	PCI INTF# Routing (Refer to PnP IRQ Routing Table)
3:0	RW	0	PCI INTE# Routing (Refer to PnP IRQ Routing Table)

Offset Address: 45h (B0D17F0)
PCI PNP Interrupt Routing INTG/H#
Default Value: 00h

Bit	Attribute	Default	Description
7:4	RW	0	PCI INTH# Routing (Refer to PnP IRQ Routing Table)
3:0	RW	0	PCI INTG# Routing (Refer to PnP IRQ Routing Table)

Offset Address: 46h (B0D17F0)
PCI INTE-F Interrupt Control
Default Value: 00h

Bit	Attribute	Default	Description
7:5	—	0	Reserved
4	RW	0	PCI INT Sharing Control 0: INTE# shared with INTA# INTF# shared with INTB# INTG# shared with INTC# INTH# shared with INTD# 1: INTE-INTH routing per Rx44-45 The following bits all default to “Non-Invert” triggered (0)
3	RW	0	PCI INTA# Invert / Non-Invert Trigger 0: Non-Invert 1: Invert
2	RW	0	PCI INTB# Invert / Non-Invert Trigger 0: Non-Invert 1: Invert
1	RW	0	PCI INTC# Invert / Non-Invert Trigger 0: Non-Invert 1: Invert
0	RW	0	PCI INTD# Invert / Non-Invert Trigger 0: Non-Invert 1: Invert

Note: For routing control of PCI INTA-INTD, see Device 17 Function 0 Rx54-57 and Table 7.

Offset Address: 48h (B0D17F0)
Read Pass Write Control
Default Value: 0Ch

Bit	Attribute	Default	Description
7	RW	0	FSB Fixed at Low DW 0: Disable (Address Bit-2 not masked) 1: Enable (force A2 from APIC FSB to low) Address bit A2 controls whether data is in the lower (0) or upper (1) doubleword of a quadword sent to the CPU. When this bit is enabled, A2 is masked which means it is always 0 to select the lower doubleword.
6:4	—	0	Reserved
3	RW	1	AC97 / LPC Read Pass Write 0: Disable (a read cannot be performed before a preceding write has been completed) 1: Enable (internal AC97 and LPC devices are allowed to perform a read before a preceding write)
2	RW	1	IDE Read Pass Write 0: Disable (a read cannot be performed before a preceding write has been completed) 1: Enable (the internal IDE controller is allowed to perform a read before a preceding write)
1	RW	0	USB Read Pass Write 0: Disable (a read cannot be performed before a preceding write has been completed) 1: Enable (the internal USB controllers are allowed to perform a read before a preceding write)
0	RW	0	NIC Read Pass Write 0: Disable (a read cannot be performed before a preceding write has been completed) 1: Enable (the internal LAN controller is allowed to perform a read before a preceding write)

Offset Address: 49h (B0D17F0)
SB Peripheral Device Control
Default Value: 20h

Bit	Attribute	Default	Description
7	RW	0	SERR on V-Link Bus Directed to PMU (SMI, SCI) 0: Disable 1: Enable
6	RW	0	South Bridge Internal Master Devices Priority Higher Than External PCI Master 0: Disable 1: Enable Normally priority is the same for internal and external PCI master devices, but when this bit is enabled, internal master devices are given higher priority than external PCI masters (3/4 : 1/4).
5	RW	1	SB Peripheral Device Clean to Mask Off IRQ Controls whether interrupt requests are gated until data is written to memory. 0: Disable 1: Enable
4	RW	0	PCIM Address Stepping 0: Disable 1: Enable
3	RW	0	PCIM Wait State 0: Disable 1: Enable
2	RW	0	WSC Mask Off INTR Controls whether INTR is masked until write snoop is complete. 0: Disable 1: Enable
1:0	—	0	Reserved

LPC Firmware Memory Control (4A-4Bh)
Offset Address: 4Ah (B0D17F0)
LPC Firmware Memory Control 1
Default Value: 00h

Bit	Attribute	Default	Description
7:1	RW	0	LPC Firmware Memory Base Address A[23:17]
0	RW	0	LPC Firmware Memory Programmable IDSEL 0: Disable 1: Enable

Offset Address: 4Bh (B0D17F0)**LPC Firmware Memory Control 2****Default Value: 00h**

Bit	Attribute	Default	Description
7	—	0	Reserved
6:4	RW	0	LPC Firmware Memory Base Address Mask bit-6 = 1 to mask A19 decoding bit-5 = 1 to mask A18 decoding bit-4 = 1 to mask A17 decoding
3:0	RW	0	LPC Firmware Memory IDSEL Value

Miscellaneous Control (4C-4Fh)**Offset Address: 4Ch (B0D17F0)****IDE Interrupt Select****Default Value: 04h**

Bit	Attribute	Default	Description
7:6	RW	0	I/O Recovery Time Select When Rx40[6] is enabled, this field determines the I/O recovery time. 00: 1 Bus Clock 01: 2 Bus Clock 10: 4 Bus Clock 11: 8 Bus Clock
5:4	—	0	Reserved
3:2	RW	01b	IDE Secondary Channel IRQ Routing 00: IRQ14 01: IRQ15 10: IRQ10 11: IRQ11
1:0	RW	0	IDE Primary Channel IRQ Routing 00: IRQ14 01: IRQ15 10: IRQ10 11: IRQ11

Note: When the internal APIC is enabled, internal IRQ routing to the APIC is fixed as follows:

INTA# => IRQ16

INTB# => IRQ17

INTC# => IRQ18

INTD# => IRQ19

IDE IRQ, USB UHCI 1 IRQ, PCIe Root Port 0 IRQ and INTE# => IRQ20

SATA IRQ, USB UHCI 3 IRQ and INTF# => IRQ21

Audio IRQ, USB UHCI 2 IRQ, USB EHCI IRQ, PCIe Root Port 1 IRQ and INTG#: IRQ22

LAN IRQ, Modem IRQ, USB UHCI 4 and INTH# => IRQ23

HD Audio IRQ => Share with INTB# (IRQ17)

Offset Address: 4Dh (B0D17F0)
Miscellaneous Control
Default Value: 00h

Bit	Attribute	Default	Description	Mnemonic
7	RW	00	LPC Firmware Memory 16 Bytes Burst Read 0: Disable 1: Enable	
6	RW	0	LPC Firmware Memory 4 Bytes Burst Read / Write Access 0: Disable 1: Enable	
5	RW1	0	Firmware Memory Burst Detection Write 1 to start to detect the Firmware memory burst ability 0: Complete 1: Incomplete If the LPC Firmware memory support 16 byte burst, the Rx4D[7] will be set to 1 after burst detection complete.. If the LPC Firmware memory support 4 byte burst, the Rx4D[6] will be set 1 after burst detection complete.	
4	RW	0	LPC Firmware Memory IDSEL Value	
3	RW	0	Enable Fixed Path of External Interrupt Delivery Mode Only in APIC Ch0 When Interrupt Controller Has Not Been Masked Yet 0: Disable 1: Enable	
2	RW	0	Serial IRQs Always be Shared in APIC Mode 0: Disable 1: Enable	
1	RW	0	LPC Memory Goes To LPC Firmware Memory Cycle 0: Only ROM Cycle will be transferred to LPC firmware memory cycle 1: All memory cycle will be transferred to LPC firmware cycle	RDISGROM
0	RW	0	LPC TPM Function 0: Disable 1: Enable	

Offset Address: 4Eh (B0D17F0)
Internal RTC Test Mode and Extra Feature Control
Default Value: 00h

Bit	Attribute	Default	Description
7	RW	0	RTC High Bank Rx38-3F R/W Protect 0: Disable (allow R/W) 1: Enable (Protect)
6	RW	0	RTC Low Bank Rx38-3F R/W Protect 0: Disable (allow R/W) 1: Enable (Protect)
5	—	0	Reserved
4	RO	0	Last Port 70/74 Written Status 0: Last write was to port 70 1: Last write was to port 74
3	RW	0	Extra RTC Port 74/75 The RTC is normally accessed through ports 70/74. This bit controls whether two extra ports (74 / 75) can be used to access the RTC. 0: Disable 1: Enable
2:0	—	0	Reserved

Offset Address: 4Fh (B0D17F0)
PCI Bus and CPU Interface Control
Default Value: 00h

Bit	Attribute	Default	Description
7:1	—	0	Reserved
0	RW	0	Software PCI Reset Write 1 to generate PCI reset Software reset also can be produced by writing I/O port CF9, write 1 to I/O port CF9 bit2 to produce software reset. If CF9 bit 1 is 0, INIT will be produced. If CF9 bit 1 is 1, PCIRST will be produced. CF9 bit 1 default value is 1. 0: Disable 1: Enable

Function Control (50-51h)
Offset Address: 50h (B0D17F0)
Function Control 1
Default Value: 00h

Bit	Attribute	Default	Description
7	RW	0	Device 17 Function 6 MC97 0: Enable 1: Disable
6	RW	0	Device 17 Function 5 AC97 0: Enable 1: Disable
5	RW	0	Device 16 Function 1 USB 2 0: Enable 1: Disable
4	RW	0	Device 16 Function 0 USB 1 0: Enable 1: Disable
3	RW	0	Device 15 Function 0 Serial ATA 0: Enable 1: Disable
2	RW	0	Device 16 Function 2 USB 3 0: Enable 1: Disable
1	RW	0	Device 16 Function 4 USB 5 0: Enable 1: Disable
0	RW	0	Device 16 Function 3 USB 4 0: Enable 1: Disable

Offset Address: 51h (B0D17F0)
Function Control 2
Default Value: 1Dh

Bit	Attribute	Default	Description
7:6	—	0	Reserved
5	RW	0	Gating LAN Control Clock When bit-4 of this register is disabled, the LAN function is disabled but the LAN controller clock is not gated automatically. This bit controls whether the clock is actually gated. 0: Disable 1: Enable
4	RW	1	Internal LAN Controller 0: Disable 1: Enable
3	RW	1	Internal RTC 0: Disable 1: Enable
2	RW	1	Internal PS2 Mouse 0: Disable 1: Enable
1	RW	0	Internal KBC Configuration 0: Disable 1: Enable
0	RW	1	Internal Keyboard Controller 0: Disable 1: Enable

Serial IRQ, LPC and PC / PCI DMA Control (52-53h)
Offset Address: 52h (B0D17F0)
Serial IRQ, PCI / DMA Control and LPC Control
Default Value: 00h

Bit	Attribute	Default	Description
7	—	0	Reserved
6	RW	0	LPC Short Wait Abort 0: Disable 1: Enable. During a short wait, the cycle is aborted after 8Ts.
5	RW	0	LPC Frame Wait State 0: Disable 1: Enable
4	RW	0	LPC Stop to Start Frame Wait State 0: Disable. One idle state is inserted between Stop and Start 1: Enable. Stop is followed immediately by Start.
3	RW	0	Serial IRQ 0: Disable 1: Enable. (IRQ asserted via Serial IRQ pin AD9)
2	RW	0	Serial IRQ Quiet Mode 0: Continuous Mode 1: Quiet Mode
1:0	RW	0	Serial IRQ Start-Frame Width 00: 4 PCI Clocks 01: 6 PCI Clocks 10: 8 PCI Clocks 11: 10 PCI Clocks

Offset Address: 53h (B0D17F0)
PC / PCI DMA Control
Default Value: 00h

Bit	Attribute	Default	Description
7	RW	0	Multiplexed Pin Selection for GPIO or PCI Request A 0: AG2=GPIO24, AG3=GPIO30 1: AG2=PCREQA, AG3=PCGNTA
6	RW	0	PCI DMA Channel 7 0: Disable 1: Enable
5	RW	0	PCI DMA Channel 6 0: Disable 1: Enable
4	RW	0	PCI DMA Channel 5 0: Disable 1: Enable
3	RW	0	PCI DMA Channel 3 0: Disable 1: Enable
2	RW	0	PCI DMA Channel 2 0: Disable 1: Enable
1	RW	0	PCI DMA Channel 1 0: Disable 1: Enable
0	RW	0	PCI DMA Channel 0 0: Disable 1: Enable

Plug and Play Control – PCI (54-57h)
Offset Address: 54h (B0D17F0)
PCI Bus and CPU Interface Control
Default Value: 00h

Bit	Attribute	Default	Description
7:4	—	0	Reserved The following bits all default to “Non-Invert” triggered (0)
3	RW	0	PCI INTA# Invert / Non-Invert Trigger 0: Non-Invert 1: Invert
2	RW	0	PCI INTB# Invert / Non-Invert Trigger 0: Non-Invert 1: Invert
1	RW	0	PCI INTC# Invert / Non-Invert Trigger 0: Non-Invert 1: Invert
0	RW	0	PCI INTD# Invert / Non-Invert Trigger 0: Non-Invert 1: Invert

Note: PCI INTA-D# normally connect to PCI interrupt pins INTA-D# (see pin definitions for more information).

Offset Address: 55h (B0D17F0)
PCI PNP Interrupt Routing 1
Default Value: 00h

Bit	Attribute	Default	Description
7:4	RW	0	PCI INTA# Routing (see PnP IRQ routing table)
3:0	—	0	Reserved. Always reads 0

Offset Address: 56h (B0D17F0)
PCI PNP Interrupt Routing 2
Default Value: 00h

Bit	Attribute	Default	Description
7:4	RW	0	PCI INTC# Routing (see PnP IRQ routing table)
3:0	RW	0	PCI INTB# Routing (see PnP IRQ routing table)

Offset Address: 57h (B0D17F0)
PCI PNP Interrupt Routing 3
Default Value: 00h

Bit	Attribute	Default	Description
7:4	RW	0	PCI INTD# Routing (see PnP IRQ routing table)
3:0	—	0	Reserved. Always reads 0

Table 7. PnP IRQ Routing Table

0000	Reserved
0001	IRQ1
0010	Reserved
0011	IRQ3
0100	IRQ4
0101	IRQ5
0110	IRQ6
0111	IRQ7
1000	Reserved
1001	IRQ9
1010	IRQ10
1011	IRQ11
1100	IRQ12
1101	Reserved
1110	IRQ14
1111	IRQ15

Note: When enable internal APIC, PCI devices and internal function IRQ routing as below:

INTA#	IRQ16
INTB#	IRQ17
INTC# HD audio IRQ	IRQ18
INTD#	IRQ19
IDE IRQ, USB UHCI 1 IRQ, PCIe Root Port 0 IRQ and INTE#	IRQ20
SATA IRQ, USB UHCI 3 IRQ and INTF#	IRQ21
Audio IRQ, USB UHCI 2 IRQ, USB EHCI IRQ, PCIe Root Port 1 IRQ and INTG#	IRQ22
LAN IRQ, Modem IRQ, USB UHCI 4 and INTH#	IRQ23

GPIO and Miscellaneous Control (58-5Bh)
Offset Address: 58h (B0D17F0)
Miscellaneous Control 1
Default Value: 00h

Bit	Attribute	Default	Description
7	RW	0	Multiplexed Pin Selection for GPIO or PCI Request B 0: AF1 = GPIO25, AF3 = GPIO31 1: AF1 = PCREQB, AF3 = PCGNTB
6	RW	0	Multiplexed Pin Selection for GPIO or APIC 0: AA27 = GPIO10, AA28 = GPIO11, AD28 = GPI19 1: AA27 = APICD0, AA28 = APICD1, AD28 = APICCLK
5	RW	0	South Bridge Interrupt Cycles Run at 33 MHz 0: Disable 1: Enable
4	RW	0	South Bridge Decode 0: Subtractive 1: Positive
3	RW	0	RTC High Bank Access 0: Disable 1: Enable
2	RW	0	RTC Rx32 Write Protect 0: Disable (not protected) 1: Enable (write protected)
1	RW	0	RTC Rx0D Write Protect 0: Disable (not protected) 1: Enable (write protected)
0	RW	0	RTC Rx32 Map to Century Byte Controls whether RTC Rx32 is mapped to the century byte. 0: Disable 1: Enable

Offset Address: 59h (B0D17F0)
Miscellaneous Control 2
Default Value: 00h

Bit	Attribute	Default	Description
7	RW	0	ROM Memory Cycles Go To LPC 0: Disable (all memory cycles go to LPC) 1: Enable (only ROM memory cycles go to LPC)
6	—	0	Reserved
5	RW	0	LPC RTC 0: Disable 1: Enable
4	RW	0	LPC Keyboard 0: Disable (ISA Keyboard) 1: Enable (LPC Keyboard)
3	RW	0	Port 62h / 66h (MCCS#) to LPC 0: Disable 1: Enable
2	RW	0	Port 62h / 66h (MCCS#) Decoding 0: Disable 1: Enable
1	RW	0	Mask A20M# Active 0: Disable (A20M# act normally) 1: Enable (A20M# signal de-asserted)
0	RW	0	NMI on PCI Parity Error 0: Disable 1: Enable (to generate NMI, Port 61[3] and Port 70[7] must also be set)

Note: To produce NMI correctly, port 61 bit3 must be set to 0 and port 70 bit 7 must be set to 0 since Data parity error report is combined with IOCHK.

Offset Address: 5Ah (B0D17F0)
DMA Bandwidth Control
Default Value: 00h

Bit	Attribute	Default	Description
7	RW	0	DMA Channel 7 Bandwidth 0: Normal 1: Improved
6	RW	0	DMA Channel 6 Bandwidth 0: Normal 1: Improved
5	RW	0	DMA Channel 5 Bandwidth 0: Normal 1: Improved
4	RW	0	DMA Single Transfer Mode Bandwidth 0: Normal 1: Improved
3	RW	0	DMA Channel 3 Bandwidth 0: Normal 1: Improved
2	RW	0	DMA Channel 2 Bandwidth 0: Normal 1: Improved
1	RW	0	DMA Channel 1 Bandwidth 0: Normal 1: Improved
0	RW	0	DMA Channel 0 Bandwidth 0: Normal 1: Improved

Note: The above bits determine if DMA bandwidth is improved for the specified channel. If enabled, bandwidth improvement is accomplished by reducing the transaction latency between the DMA Controller and the LPC Bus Controller.

Offset Address: 5Bh (B0D17F0)
Miscellaneous Control 3
Default Value: 01h

Bit	Attribute	Default	Description
7	RW	0	LPC Firmware Memory Read TRDY 1 Wait State 0: Disable 1: Enable
6	—	0	Reserved
5	RW	0	PCI/DMA Memory Cycles Output to PCI Bus 0: Disable 1: Enable
4	—	0	Reserved
3	RW	0	Bypass APIC De-Assert Message 0: Disable 1: Enable
2	RW	0	APIC LDT Mode 0: Disable 1: Enable
1	RW	0	Multiplexed Pin Selection for INTE# -INTH# or GPI32-35 0: GPI32-35 1: INTE#-INTH#
0	RW	1	Dynamic Clock Stop 0: Disable 1: Enable

Programmable Chip Select Control (5C-66h)
Offset Address: 5D-5Ch (B0D17F0)
PCS 0 I/O Port Address
Default Value: 0000h

Bit	Attribute	Default	Description
15:0	RW	0000h	PCS 0 I/O Port Address

Offset Address: 5F-5Eh (B0D17F0)
PCS 1 I/O Port Address
Default Value: 0000h

Bit	Attribute	Default	Description
15:0	RW	0000h	PCS 1 I/O Port Address

Offset Address: 61-60h (B0D17F0)
PCS 2 I/O Port Address
Default Value: 0000h

Bit	Attribute	Default	Description
15:0	RW	0000h	PCS 2 I/O Port Address

Offset Address: 63-62h (B0D17F0)
PCS 3 I/O Port Address
Default Value: 0000h

Bit	Attribute	Default	Description
15:0	RW	0000h	PCS 3 I/O Port Address

Offset Address: 65-64h (B0D17F0)
PCS I/O Port Address Mask
Default Value: 0000h

Bit	Attribute	Default	Description
15:12	RW	0	PCS 3 I/O Port Address Mask 3-0 0000: Decode range is 1 byte 0011: Decode range is 4 bytes 1111: Decode range is 16 bytes 0001: Decode range is 2 bytes 0111: Decode range is 8 bytes
11:8	RW	0	PCS 2 I/O Port Address Mask 3-0 0000: Decode range is 1 byte 0011: Decode range is 4 bytes 1111: Decode range is 16 bytes 0001: Decode range is 2 bytes 0111: Decode range is 8 bytes
7:4	RW	0	PCS 1 I/O Port Address Mask 3-0 0000: Decode range is 1 byte 0011: Decode range is 4 bytes 1111: Decode range is 16 bytes 0001: Decode range is 2 bytes 0111: Decode range is 8 bytes
3:0	RW	0	PCS 0 I/O Port Address Mask 3-0 0000: Decode range is 1 byte 0011: Decode range is 4 bytes 1111: Decode range is 16 bytes 0001: Decode range is 2 bytes 0111: Decode range is 8 bytes

Offset Address: 66h (B0D17F0)
PCS Control
Default Value: 00h

Bit	Attribute	Default	Description
7:4	—	0	Reserved
3	RW	0	PCS 3 0: Disable 1: Enable
2	RW	0	PCS 2 0: Disable 1: Enable
1	RW	0	PCS 1 0: Disable 1: Enable
0	RW	0	PCS 0 0: Disable 1: Enable

Output Control (67h)
Offset Address: 67h (B0D17F0)
Output Control
Default Value: 04h

Bit	Attribute	Default	Description
7	RW	0	LPC PCS3 0: Disable 1: Enable (PCS3 is on LPC bus)
6	RW	0	LPC PCS2 0: Disable 1: Enable (PCS2 is on LPC bus)
5	RW	0	LPC PCS1 0: Disable 1: Enable (PCS1 is on LPC bus)
4	RW	0	LPC PCS0 0: Disable 1: Enable (PCS0 is on LPC bus)
3	—	0	Reserved
2	RW	1	FERR Voltage 0: 2.5V 1: 1.5V
1:0	RW	0	IDE Pad Driving Select

High Precision Event Timers (HPET) (68-6Bh)
Offset Address: 68h (B0D17F0)
HPET Control
Default Value: 00h

Bit	Attribute	Default	Description
7	RW	0	High Precision Event Timers 0: Disable 1: Enable
6:4	—	0	Reserved
3:0	—	0	Reserved. Always reads 0.

Offset Address: 6B-69h (B0D17F0)
HPET Control
Default Value: 000000h

Bit	Attribute	Default	Description
23:2	RW	0	HPET Memory Base Address [31:10]
1:0	—	0	Reserved

ISA Decoding Control (6C-6Fh)
Offset Address: 6Ch (B0D17F0)
ISA Positive Decoding Control 1
Default Value: 00h

Bit	Attribute	Default	Description
7	RW	0	On-Board I/O (Ports 00-FFh) Positive Decoding 0: Disable 1: Enable
6	RW	0	Microsoft-Sound System I/O Port Positive Decoding 0: Disable 1: Enable (bits 5-4 determine the decode range)
5:4	RW	0	Microsoft Sound System I/O Decode Range 00: 0530h-0537h 01: 0604h-060Bh 10: 0E80-0E87h 11: 0F40h-0F47h
3	RW	0	APIC Positive Decoding 0: Disable 1: Enable
2	RW	0	ROM Positive Decoding 0: Disable 1: Enable
1	RW	0	PCS1# Positive Decoding 0: Disable 1: Enable
0	RW	0	PCS0# Positive Decoding 0: Disable 1: Enable

Offset Address: 6Dh (B0D17F0)
ISA Positive Decoding Control 2
Default Value: 00h

Bit	Attribute	Default	Description
7	RW	0	FDC Positive Decoding 0: Disable 1: Enable
6	RW	0	LPT Positive Decoding 0: Disable 1: Enable
5:4	RW	0	LPT Decode Range 00: 3BCh-3BFh, 7BCh-7Beh 10: 278h-27Fh, 678h-67Ah 01: 378h-37Fh, 778h-77Ah 11: Reserved
3	RW	0	Game Port Positive Decoding 0: Disable 1: Enable
2	RW	0	MIDI Positive Decoding 0: Disable 1: Enable
1:0	RW	0	MIDI Decode Range 00: 300-303h 01: 310-313h 10: 320-323h 11: 330-333h

Offset Address: 6Eh (B0D17F0)
ISA Positive Decoding Control 3
Default Value: 00h

Bit	Attribute	Default	Description
7	RW	0	COM Port B Positive Decoding 0: Disable 1: Enable
6:4	RW	0	COM-Port B Decode Range 000: 3F8h-3FFh (COM1) 001: 2F8h-2FFh (COM2) 010: 220h-227h 011: 228h-22Fh 100: 238h-23Fh 101: 2E8h-2EFh (COM4) 110: 338h-33Fh 111: 3E8h-3EFh (COM3)
3	RW	0	COM Port A Positive Decoding 0: Disable 1: Enable
2:0	RW	0	COM-Port A Decode Range 000: 3F8h-3FFh (COM1) 001: 2F8h-2FFh (COM2) 010: 220h-227h 011: 228h-22Fh 100: 238h-23Fh 101: 2E8h-2EFh (COM4) 110: 338h-33Fh 111: 3E8h-3EFh (COM3)

Offset Address: 6Fh (B0D17F0)
ISA Positive Decoding Control 4
Default Value: 00h

Bit	Attribute	Default	Description
7	—	0	Reserved
6	RW	0	LPC TPM Positive Decoding 0: Disable 1: Enable
5	RW	0	PCS2# and PCS3# Positive Decoding 0: Disable 1: Enable
4	RW	0	I/O Port 0CF9h Positive Decoding 0: Disable 1: Enable
3	RW	0	FDC Decoding Range 0: Primary 1: Secondary
2	RW	0	Sound Blaster Positive Decoding 0: Disable 1: Enable
1:0	RW	0	Sound Blaster Decode Range 00: 220-22F, 230-233h 01: 240-24F, 250-253h 10: 260-26F, 270-273h, 11: 280-28F, 290-293h

PCI I/O Cycle Control (74-7Fh)
Offset Address: 75h (B0D17F0)
ROM Memory Address Range **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	Programmable Firmware Memory IDSEL for All Memory Range When Rx4D[1] (RDISGROM) = 1
3	RW	0	ROM Memory Address Range FF700000-FF7FFFFF FF300000-FF3FFFFF
2	RW	0	ROM Memory Address Range FF600000-FF6FFFFF FF200000-FF2FFFFF
1	RW	0	ROM Memory Address Range FF500000-FF5FFFFF FF100000-FF1FFFFF
0	RW	0	ROM Memory Address Range FF400000-FF4FFFFF FF000000-FF0FFFFF

Offset Address: 76h (B0D17F0)
ROM Memory Address Range **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	Programmable Firmware Memory IDSEL for the Following two 1MB Memory Range FF500000-FF5FFFFF FF100000-FF1FFFFF
3:0	RW	0	Programmable Firmware Memory IDSEL for the Following two 1MB Memory Range FF400000-FF4FFFFF FF000000-FF0FFFFF

Offset Address: 77h (B0D17F0)
ROM Memory Address Range **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	Programmable Firmware Memory IDSEL for the Following two 1MB Memory Range FF700000-FF7FFFFF FF300000-FF3FFFFF
3:0	RW	0	Programmable Firmware Memory IDSEL for the Following two 1MB Memory Range FF600000-FF6FFFFF FF200000-FF2FFFFF

Offset Address: 7Ch (B0D17F0)
ROM Memory Address Range 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	Programmable Firmware Memory IDSEL for the Following two 512K Memory Range FFC80000-FFCFFFFF FF800000-FF8FFFFF
3:0	RW	0	Programmable Firmware Memory IDSEL for the Following two 512K Memory Range FFC00000-FFC7FFFF FF800000-FF87FFFF

Offset Address: 7Dh (B0D17F0)
ROM Memory Address Range 2
Default Value: 00h

Bit	Attribute	Default	Description
7:4	RW	0	Programmable Firmware Memory IDSEL for the Following two 512K Memory Range FFD80000-FFDFFFFF FF980000-FF9FFFFFF
3:0	RW	0	Programmable Firmware Memory IDSEL for the Following two 512K Memory Range FFD00000-FFD7FFFF FF900000-FF97FFFF

Offset Address: 7Eh (B0D17F0)
ROM Memory Address Range 3
Default Value: 00h

Bit	Attribute	Default	Description
7:4	RW	0	Programmable Firmware Memory IDSEL for the Following two 512K Memory Range FFE80000-FFEFFFFFF FFA80000-FFAFFFFFF
3:0	RW	0	Programmable Firmware Memory IDSEL for the Following two 512K Memory Range FFE00000-FFE7FFFF FFA00000-FFA7FFFF

Offset Address: 7Fh (B0D17F0)
ROM Memory Address Range 4
Default Value: 00h

Bit	Attribute	Default	Description
7:4	RO	0	Programmable Firmware Memory IDSEL for the Following two 512K Memory Range FFF80000-FFFFFFFFFF FFB80000-FFBFFFFFF 000E0000-000FFFFF
3:0	RW	0	Programmable Firmware Memory IDSEL for the Following two 512K Memory Range FFF00000-FFF7FFFF FFB00000-FFB7FFFF

Power Management-Specific Configuration Registers (80-C7h)
Offset Address: 80h (B0D17F0)
General Configuration 1
Default Value: 00h

Bit	Attribute	Default	Description
7	—	0	Reserved. Always reads 0
6	RW	0	GP18 (VGATE) as SLPBTN# 0: Disable 1: Enable
5	RW	0	Debounce 0: Disable 1: Enable
4	—	0	Reserved. Always reads 0
3	RW	0	Microsoft Sound Monitor in Audio Access This bit controls whether an I/O access to the sound port sets PMIO Rx33-30[10] (AUD_STS) = 1. 0: Disable 1: Enable
2	RW	0	Game Port Monitor in Audio Access This bit controls whether an I/O access to the game port sets PMIO Rx33-30[10] (AUD_STS) = 1. 0: Disable 1: Enable
1	RW	0	Sound Blaster Monitor in Audio Access This bit controls whether an I/O access to the sound blaster port sets PMIO Rx33-30[10] (AUD_STS) = 1. 0: Disable 1: Enable
0	RW	0	MIDI Monitor in Audio Access This bit controls whether an I/O access to the MIDI port sets PMIO Rx33-30[10] (AUD_STS) = 1. 0: Disable 1: Enable

Offset Address: 81h (B0D17F0)**General Configuration 2****Default Value: 04h**

Bit	Attribute	Default	Description	Mnemonic
7	RW	0	ACPI I/O Enable 0: Disable access to ACPI I/O block 1: Allow access to Power Management I/O Register Block (see offset 4B-48 to set the base address for this register block). The definitions of the registers in the Power Management I/O Register Block are included later in this document, following the Power Management Subsystem overview.	
6:4	—	0	Reserved	
3	RW	0	ACPI Timer with 32 Bit Width	
2	RW	1	RTC Enable Signal Gated with PSON (SUSC#) in Soft-Off Mode This bit controls whether RTC control signals are gated during system suspend state. This is to prevent CMOS and Power-Well register data from being corrupted during system on/off when the control signals (PWRGD) may not be stable. 0: Disable 1: Enable	
1	RW	0	Clock Throttling Clock Select (STPCLK#) This bit controls the timer tick base for the throttle timer. 0: 30 usec (480 usec cycle time when using a 4-bit timer) 1: 1 msec (16 msec cycle time when using a 4-bit timer) The timer tick base can be further lowered to 7.5 usec (120 usec cycle time when using a 4-bit timer) by setting Rx8D[4] = 1. When Rx8D[4] = 1, the setting of this bit is ignored.	STPTB
0	—	0	Reserved. Do not program.	

Offset Address: 82h (B0D17F0)**ACPI Interrupt Select****Default Value: 40h**

Bit	Attribute	Default	Description
7	RO	0	ATX / AT Power Indicator 0: ATX 1: AT
6	RO	1	PSON (SUSC#) Current State During system on/off, this status bit reports whether PSON gating state has been completed, 0 meaning that gating is active now and 1 meaning that gating is complete. Software should not access any CMOS or Power-Well registers until this bit becomes 1 if Rx81[2] = 1 (see register description on previous page). 0: PSON Gating Active 1: PSON Gating Complete
5	—	0	Reserved Always reads 0.
4	RO	0	SUSC# AC-Power-On Default Value This bit is written at RTC Index 0D bit-7. If this bit is 0, the system is configured to "default on" when power is connected.
3:0	RW	0	ACPI IRQ Select This field determines the routing of the ACPI IRQ. 0000: Disabled 0001: IRQ1 0010: Reserved 0011: IRQ3 0100: IRQ4 0101: IRQ5 0110: IRQ6 0111: IRQ7 1000: IRQ8 1001: IRQ9 1010: IRQ10 1011: IRQ11 1100: IRQ12 1101: IRQ13 1110: IRQ14 1111: IRQ15

Offset Address: 85-84h (B0D17F0)
IRQn as Primary Interrupt
Default Value: 0000h

If a device IRQ is enabled as a Primary IRQ, that device's IRQ can be used to generate wake events. The bits in this register are used in conjunction with:

1. PMIO Rx28[7] (PINT1_STS) - Primary Resume Status
2. PMIO Rx2A[7] (IRQRSMEN) - Primary Resume Enable

If a device on one of the IRQ's is set to enable the Primary Interrupt, once the device generates an IRQ, the PMIO Rx28[7] status bit will become 1 to report the occurrence of the Primary IRQ. If PMIO Rx2A[7] is set to 1 to enable Resume-on-Primary-IRQ, the IRQ then becomes a wake event.

Bit	Attribute	Default	Description
15	RW	0	Take IRQ15 as Primary Interrupt Channel 0: Disable 1: Enable
14	RW	0	Take IRQ14 as Primary Interrupt Channel 0: Disable 1: Enable
13	RW	0	Take IRQ13 as Primary Interrupt Channel 0: Disable 1: Enable
12	RW	0	Take IRQ12 as Primary Interrupt Channel 0: Disable 1: Enable
11	RW	0	Take IRQ11 as Primary Interrupt Channel 0: Disable 1: Enable
10	RW	0	Take IRQ10 as Primary Interrupt Channel 0: Disable 1: Enable
9	RW	0	Take IRQ9 as Primary Interrupt Channel 0: Disable 1: Enable
8	RW	0	Take IRQ8 as Primary Interrupt Channel 0: Disable 1: Enable
7	RW	0	Take IRQ7 as Primary Interrupt Channel 0: Disable 1: Enable
6	RW	0	Take IRQ6 as Primary Interrupt Channel 0: Disable 1: Enable
5	RW	0	Take IRQ5 as Primary Interrupt Channel 0: Disable 1: Enable
4	RW	0	Take IRQ4 as Primary Interrupt Channel 0: Disable 1: Enable
3	RW	0	Take IRQ3 as Primary Interrupt Channel 0: Disable 1: Enable
2	—	0	Reserved. Always reads 0
1	RW	0	Take IRQ1 as Primary Interrupt Channel 0: Disable 1: Enable
0	RW	0	Take IRQ0 as Primary Interrupt Channel 0: Disable 1: Enable

Offset Address: 87-86h (B0D17F0)
IRQn as Secondary Interrupt
Default Value: 0000h

For legacy PMU, the bits in this register are used in conjunction with:

1. PMIO Rx28[1] (PSEVTTM) – Secondary Event Timer Timeout Status
2. PMIO Rx2A[1] (PSEVTEN) – SMI on Secondary Event Timer Timeout

Secondary IRQ's are different from Primary IRQ's in that systems that resume due to a Secondary IRQ can return directly to suspend state after the secondary event timer times out. For this to work, PMIO Rx2A[1] needs to be set to one to enable SMI-on-Secondary-Event-Timer-Timeout (when PMIO Rx28[1] = 1). The timer's count value can be set via Rx93-90[27-26].

Bit	Attribute	Default	Description
15	RW	0	Take IRQ15 as Secondary Interrupt Channel 0: Disable 1:Enable
14	RW	0	Take IRQ14 as Secondary Interrupt Channel 0: Disable 1:Enable
13	RW	0	Take IRQ13 as Secondary Interrupt Channel 0: Disable 1:Enable
12	RW	0	Take IRQ12 as Secondary Interrupt Channel 0: Disable 1:Enable
11	RW	0	Take IRQ11 as Secondary Interrupt Channel 0: Disable 1:Enable
10	RW	0	Take IRQ10 as Secondary Interrupt Channel 0: Disable 1:Enable
9	RW	0	Take IRQ9 as Secondary Interrupt Channel 0: Disable 1:Enable
8	RW	0	Take IRQ8 as Secondary Interrupt Channel 0: Disable 1:Enable
7	RW	0	Take IRQ7 as Secondary Interrupt Channel 0: Disable 1:Enable
6	RW	0	Take IRQ6 as Secondary Interrupt Channel 0: Disable 1:Enable
5	RW	0	Take IRQ5 as Secondary Interrupt Channel 0: Disable 1:Enable
4	RW	0	Take IRQ4 as Secondary Interrupt Channel 0: Disable 1:Enable
3	RW	0	Take IRQ3 as Secondary Interrupt Channel 0: Disable 1:Enable
2	—	0	Reserved. Always reads 0
1	RW	0	Take IRQ1 as Secondary Interrupt Channel 0: Disable 1:Enable
0	RW	0	Take IRQ0 as Secondary Interrupt Channel 0: Disable 1:Enable

Offset Address: 89-88h (B0D17F0)
Power Management I/O Base
Default Value: 0001h

Bit	Attribute	Default	Description
15:7	RW	00h	ACPI IO Base Register
6:0	RO	01h	Hardwire to 01h

Offset Address: 8Ah (B0D17F0)
Dynamically Switching Processor Power State
Default Value: 00h

Bit	Attribute	Default	Description	Mnemonic
7:5	—	0	Reserved	
4	RW	0	Down C3 or C4 Mode Enable (C2 to C3/C4) This bit is used in conjunction with bit 3 (PUPC2). If bit 3 is 0, this bit must be 0. 0: VT8251 will not attempt to automatically to a previous C3 or C4 state. 1: VT8251 observes that there are no bus master activities, it can return to a previous C3 or C4 state.	
3	RW	0	Up C2 Mode Enable (C3/C4 to C2) 0: VT8251 will treat Bus Master traffic as a break event and will return from C3/C4 to C0 based on a break event. 1: VT8251 observes a bus master request, it will take the system from a C3 or C4 state to a C2 state and auto enable Bus Masters. This will let snoops and memory access occurs.	PUPC2
2	RW	0	BM_STS Report Disable 0: VT8251 sets PMIO Rx0[4] (BM_STS) if there is bus master activity. 1: VT8251 will not set the PMIO Rx0[4] (BM_STS) if there is bus master activity. Note: 1. It is expected that if bit 3 is set, bit 2 should also be set. 2. PMIO Rx0[4] (BM_STS) will be set by LPC DMA or LPC masters even if this bit is set.	BM_STS_DIS
1:0	—	0	Reserved. Always reads 0	

Offset Address: 8Ch (B0D17F0)
Host Bus Power Management Control
Default Value: 00h

Bit	Attribute	Default	Description																																																																				
7:4	RW	0	Thermal Duty Cycle This field determines the duty cycle of STPCLK# when the THRM# pin is asserted. The STPCLK# duty cycle when THRM# is NOT asserted is controlled by PMIO Rx10[3:0]. The duty cycle indicates the percentage of performance (the lower the percentage, the lower the performance and the higher the power savings). If the Throttling Timer Width (Function 0 Rx8D[6-5]) is set to 3-bit width, bit-0 of this field should be set to 0 (and the performance increment will be 12.5%). If the Throttling Timer Width is set to 2-bit width, bits 1-0 of this field should be set to 0 (and the performance increment will be 25%). Throttling Timer Width <table border="1"> <thead> <tr> <th></th> <th>4-Bit</th> <th>3-Bit</th> <th>2-Bit</th> </tr> </thead> <tbody> <tr><td>0000</td><td>Reserved</td><td>Reserved</td><td>Reserved</td></tr> <tr><td>0001</td><td>6.25%</td><td>Reserved</td><td>Reserved</td></tr> <tr><td>0010</td><td>12.50%</td><td>12.50%</td><td>Reserved</td></tr> <tr><td>0011</td><td>18.75%</td><td>Reserved</td><td>Reserved</td></tr> <tr><td>0100</td><td>25.00%</td><td>25.00%</td><td>25.00%</td></tr> <tr><td>0101</td><td>31.25%</td><td>Reserved</td><td>Reserved</td></tr> <tr><td>0110</td><td>37.50%</td><td>37.50%</td><td>Reserved</td></tr> <tr><td>0111</td><td>43.75%</td><td>Reserved</td><td>Reserved</td></tr> <tr><td>1000</td><td>50.00%</td><td>50.00%</td><td>50.00%</td></tr> <tr><td>1001</td><td>56.25%</td><td>Reserved</td><td>Reserved</td></tr> <tr><td>1010</td><td>62.50%</td><td>62.50%</td><td>Reserved</td></tr> <tr><td>1011</td><td>68.75%</td><td>Reserved</td><td>Reserved</td></tr> <tr><td>1100</td><td>75.00%</td><td>75.00%</td><td>75.00%</td></tr> <tr><td>1101</td><td>81.25%</td><td>Reserved</td><td>Reserved</td></tr> <tr><td>1110</td><td>87.50%</td><td>87.50%</td><td>Reserved</td></tr> <tr><td>1111</td><td>93.75%</td><td>Reserved</td><td>Reserved</td></tr> </tbody> </table>		4-Bit	3-Bit	2-Bit	0000	Reserved	Reserved	Reserved	0001	6.25%	Reserved	Reserved	0010	12.50%	12.50%	Reserved	0011	18.75%	Reserved	Reserved	0100	25.00%	25.00%	25.00%	0101	31.25%	Reserved	Reserved	0110	37.50%	37.50%	Reserved	0111	43.75%	Reserved	Reserved	1000	50.00%	50.00%	50.00%	1001	56.25%	Reserved	Reserved	1010	62.50%	62.50%	Reserved	1011	68.75%	Reserved	Reserved	1100	75.00%	75.00%	75.00%	1101	81.25%	Reserved	Reserved	1110	87.50%	87.50%	Reserved	1111	93.75%	Reserved	Reserved
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0010	12.50%	12.50%	Reserved																																																																				
0011	18.75%	Reserved	Reserved																																																																				
0100	25.00%	25.00%	25.00%																																																																				
0101	31.25%	Reserved	Reserved																																																																				
0110	37.50%	37.50%	Reserved																																																																				
0111	43.75%	Reserved	Reserved																																																																				
1000	50.00%	50.00%	50.00%																																																																				
1001	56.25%	Reserved	Reserved																																																																				
1010	62.50%	62.50%	Reserved																																																																				
1011	68.75%	Reserved	Reserved																																																																				
1100	75.00%	75.00%	75.00%																																																																				
1101	81.25%	Reserved	Reserved																																																																				
1110	87.50%	87.50%	Reserved																																																																				
1111	93.75%	Reserved	Reserved																																																																				
3	RW	0	THRM Enable 0: Disable 1: Enable																																																																				
2	RW	0	Processor Break Event 0: Disable 1: Enable																																																																				
1	RW	0	Disable C3 Auto Master Gating																																																																				
0	—	0	Reserved																																																																				

Offset Address: 8Dh (B0D17F0)
Throttle / Clock Stop Control
Default Value: 00h

Bit	Attribute	Default	Description
7	RW	0	Throttle Timer Reset
6:5	RW	00	Throttle Timer This field determines the number of bits used for the throttle timer, which in conjunction with the throttle timer tick determines the cycle time of STPCLK#. For example, if a 2-bit timer and a 7.5 usec timer tick are selected, the STPCLK# cycle time would be 30 usec ($2^{**}2 \times 7.5$). If a 4-bit timer and a 7.5 usec timer tick is selected, the cycle time would be 120 usec ($2^{**}4 \times 7.5$). 0x: 4-Bit 11: 2-Bit (see also Rx8C[7-4] and PMIO Rx10[3-0])
4	RW	0	Fast Clock (7.5us) as Throttle Timer Tick This bit controls whether the throttle timer tick uses 7.5 usec as its time base (120 usec cycle time when using a 4-bit timer). 0: Timer Tick is selected by Rx81[1] (STPTB) 1: Timer Tick is 7.5 usec (Rx81[1] is ignored)
3	RW	0	SMI# Level Output (Low) 0: Disable 1: Enable (during an SMI event, SMI# is held low until SMI event status is cleared)
2	RW	0	Internal Clock Stop for PCI Idle This bit controls whether the internal PCI clock is stopped when CLKRUN# is high. 0: PCI clock is not stopped 1: PCI clock is stopped
1	RW	0	Internal Clock Stop During C3 This bit controls whether the internal PCI clock is stopped during C3 state. 0: PCI clock is not stopped 1: PCI clock is stopped
0	RW	0	Internal Clock Stop During Suspend This bit controls whether the internal PCI clock is stopped during Suspend state. 0: PCI clock is not stopped 1: PCI clock is stopped

Offset Address: 93-90h (B0D17F0)
GP Timer Control
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:30	RW	0	Conserve Mode Timer Count Value 00: 1/16 second 10: 1 second 01: 1/8 second 11: 1 minute
29	W1C	0	Conserve Mode Status This bit reads 1 when in Conserve Mode
28	RW	0	Conserve Mode This bit controls whether conserve mode (throttling) is enabled. When this bit is set, the system can enter conserve mode when primary activity is not detected within a given time period (determined by bits 31-30 of this register). Primary activity is defined in PMIO Rx33-30. 0: Disable 1: Enable
27:26	RW	0	Secondary Event Timer Count Value 00: 2 milliseconds 10: $\frac{1}{2}$ second 01: 64 milliseconds 11: by EOI + 0.25 milliseconds
25	W1C	0	Secondary Event Occurred Status This bit reads 1 to indicate that a secondary event has occurred (to resume the system from suspend) and the secondary event timer is counting down.
24	RW	0	Secondary Event Timer Enable 0: Disable 1: Enable
23:16	RO/WO	0	GP1 Timer Count Value (base defined by bits 5-4) Write to load count value; Read to get current count
15:8	RO/WO	0	GP0 Timer Count Value (base defined by bits 1-0) Write to load count value; Read to get current count
7	RW	0	GP1 Timer Start On setting this bit to 1, the GP1 timer loads the value defined by bits 23-16 of this register and starts counting down. The GP1 timer is reloaded at the occurrence of certain peripheral events enabled in the GP Timer Reload Enable Register (PMIO Rx38). If no such event occurs and the GP1 timer counts down to zero, then the GP1 Timer Timeout Status bit PMIO Rx28[3] (PGP1TM) is set to one. Additionally, if the GP1 Timer Timeout Enable bit PMIO Rx2A[3] (GP1TMEN) is set, then an SMI is generated.
6	RW	0	GP1 Timer Automatic Reload 0: GP1 Timer stops at 0 1: Reload GP1 timer automatically after counting down to 0
5:4	RW	0	GP1 Timer Tick Select 00: Disable 10: 1 second 01: 1/16 second 11: 1 minute
3	RW	0	GP0 Timer Start On setting this bit to 1, the GP0 timer loads the value defined by bits 15-8 of this register and starts counting down. The GP0 timer is reloaded at the occurrence of certain peripheral events enabled in the GP Timer Reload Enable Register (PMIO Rx38). If no such event occurs and the GP0 timer counts down to zero, then the GP0 Timer Timeout Status bit in PMIO Rx28[2] (PGP0TM) is set to one. Additionally, if the GP0 Timer Timeout Enable bit PMIO Rx2A[2] (GP0TMEN) is set, then an SMI is generated.
2	RW	0	GP0 Timer Automatic Reload 0: GP0 Timer stops at 0 1: Reload GP0 timer automatically after counting down to 0
1:0	RW	0	GP0 Timer Tick Select 00: Disable 10: 1 second 01: 1/16 second 11: 1 minute

Offset Address: 94h (B0D17F0)
Miscellaneous Power Well
Default Value: 80h

Bit	Attribute	Default	Description
7	RW	1	SMBus Clock Select 0: SMBus from divider of 14.318 Mhz 1: SMBus from RTC clock
6	RW	0	Check Power Button Enable for STR / STD Wake-up by PWRBTN# 0: Disable 1: Enable
5	RW	0	Internal PLL Reset During Suspend 0: Disable 1: Enable
4	RW	0	Multiplexed Pins Selection for SUSST# or GPO3 0: Select SUSST# 1: Select GPO3
3	RW	0	Multiplexed Pin Selection for GPIO12-15 0: GPIO[E:H] as GPIO12-15 1: GPIO[E:H] as GPO12-15
2	RW	0	Multiplexed Pins Selection for SUSA# or GPO2 0: Select SUSA# 1: Select GPO2
1:0	RW	0	GPO0 Output Select This field controls the GPO0 output signal for Pulse Width Modulation. 00: GPO0 Fixed Output Level (defined by PMIO Rx4C[0]) 01: GPO0 output is 1 Hz "SLOWCLK" 10: GPO0 output is 4 Hz "SLOWCLK" 11: GPO0 output is 16 Hz "SLOWCLK"

Offset Address: 95h (B0D17F0)
Miscellaneous Power Well Control
Default Value: 40h

Bit	Attribute	Default	Description
7	RW	0	CPUSTRP# to SUSST# Delay Select This bit controls the delay between the deassertion of CPUSTRP# and the deassertion of SUSST# during a resume. 0: 1 msec minimum 1: 125 usec minimum
6	RW	1	SUSST# Deasserted Before PWRGD for STD 0: Disable 1: Enable (SUST# is deasserted before PWRGD when resuming from STD)
5	RW	0	Keyboard / Mouse Port Swap This bit determines whether the keyboard and mouse ports can be swapped. 0: Disable 1: Enable
4	RW	0	PWRGD Reset
3	RW	0	Multiplexed Pin Selection for SMB Channel 2 or GPO 0: Select (SMBDT2, SMBCK2) 1: Select (GPO26, GPO27)
2	RW	0	AOL 2 SMB Slave This bit controls whether external SMB masters can access internal SMB registers (for Alert-On-LAN). 0: Enable 1: Disable
1	RW	0	Multiplexed Pins Selection for SUSCLK or GPO4 0: SUSCLK 1: GPO4
0	RW	0	USB Wakeup for POS / STR / STD / Soft This bit controls whether USB Wakeup is enabled when PMIO Rx21-20[14] (WUSB_STS) = 1. This allows wakeup from STR, STD, Soft Off, and POS. 0: Disable 1: Enable

Offset Address: 96h (B0D17F0)
BATWell
Default Value: 0Fh

Bit	Attribute	Default	Description
7:5	—	0	Reserved. Always reads 0.
4	RW	0	SMB GPOUT6 and GPOUT7 as PWRGD and PWRBTN
3:0	RW	Fh	CPU Frequency Strapping Value Output to NMI, INTR, IGNNE#, and A20M# during RESET# The value written to this field is strapped through NMI, INTR, IGNNE#, and A20M# during RESET# to determine the multiplier for setting the CPU's internal frequency. If the CPU hangs due to inappropriate settings written here, the GP3 timer (second timeout) can be used to initiate a system reboot (PMIO Rx42[2] (GP3TO2EN)= 1). Refer to the BIOS Porting Guide for additional details.

Offset Address: 97h (B0D17F0)
PWRWELL
Default Value: 00h

Bit	Attribute	Default	Description
7:4	—	0	Reserved. Always reads 0
3	RW	0	Disable Waiting PCI Express PME_TOACK Before Entering STR / STD Suspend State 0: Enable 1: Disable
2	RW	0	AC97 and HDAC Pin Definition Will Be the Same As Both Devices Enable
1	RW	0	PCI Express Wake Enable (ACPI IO Rx03[6]) Attribution Option 0:Disable 1: Enable
0	RW	0	Multiplexed Pin Selection for Audio Data or Programmable Chip Select 0: Select (ACSDIN2, ACSDIN3) or (PSC1#, PSC2#). Please refer to RxE5[2:1] for further setting. 1: Select (GPI20, GPI21)

Offset Address: 98h (B0D17F0)
GP2 / GP3 Timer Control
Default Value:00h

Bit	Attribute	Default	Description
7	RW	0	GP3 Timer Start On setting this bit to 1, the GP3 timer loads the value defined by Rx9A and starts counting down. The GP3 timer is reloaded at the occurrence of certain events enabled in the GP Timer Reload Enable Register (PMIO Rx38). If no such event occurs and the GP3 timer counts down to zero, then the GPI3 Timer Timeout Status bit PMIO Rx29-28[13] (PGP3TM) is set to one. Additionally, if the GP3 Timer Timeout Enable bit PMIO Rx2B-2A[13] (GP3Tmen) is set, then an SMI is generated.
6	RW	0	GP3 Timer Automatic Reload 0: GP3 Timer stops at 0 1: Reload GP3 timer automatically after counting down to 0
5:4	RW	0	GP3 Timer Tick Select 00: Disable 10: 1 second 01: 1/16 second 11: 1 minute
3	RW	0	GP2 Timer Start On setting this bit to 1, the GP2 timer loads the value defined by Rx99 and starts counting down. The GP2 timer is reloaded at the occurrence of certain events enabled in the GP Timer Reload Enable Register (PMIO Rx38). If no such event occurs and the GP2 timer counts down to zero, then the GP2 Timer Timeout Status bit PMIO Rx29-28[12] (PGP2TM) is set to one. Additionally, if the GP2 Timer Timeout Enable bit PMIO Rx2B-2A[12] (GP2Tmen) is set, then an SMI is generated.
2	RW	0	GP2 Timer Automatic Reload 0: GP2 Timer stops at 0 1: Reload GP2 timer automatically after counting down to 0
1:0	RW	0	GP2 Timer Tick Select 00: Disable 10: 1 second 01: 1 ms 11: 1 minute

Offset Address: 99h (B0D17F0)
GPI2 Timer
Default Value:00h

Bit	Attribute	Default	Description
7:0	RO/WO	0	Write: GP2 Timer Load Value Read: GP2 Timer Current Count

Offset Address: 9Ah (B0D17F0)
GPI3 Timer
Default Value:00h

Bit	Attribute	Default	Description
7:0	RO/WO	0	Write: GP3 Timer Load Value Read: GP3 Timer Current Count

Offset Address: C3-C0h (B0D17F0)
Power Management Capability
Default Value:0002 0001h

Bit	Attribute	Default	Description
31:16	RO	0002h	Power Management Capability
15:8	RO	0	Next Pointer
7:0	RO	01h	Capability ID

Offset Address: C7-C4h (B0D17F0)
Power Management Capability
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:16	RO	0	Power Management Capability Data
15:8	RO	0	PM CSR P2P Support Extensions
7:0	—	0	PM Control / Status (D0/D3 Only) Bits [7:2] are RO. Bits [1:0] are RW.

System Management Bus-Specific Configuration Registers (D0-E6h)
Offset Address: D1-D0h (B0D17F0)
SMBus I/O Base
Default Value: 0001h

Bit	Attribute	Default	Description
15:4	RW	0	I/O Base (16-byte I/O space)
3:0	RO	01h	Hardwire to 01h

Offset Address: D2h (B0D17F0)
SMBus Host Configuration
Default Value: 0000h

Bit	Attribute	Default	Description	Mnemonic
7: 4	—	0	Reserved. Always reads 0	
3	RW	0	SMBus Alert SCI/SMI Selection 0: SMI 1: SCI	
2	RW	0	SMBus Clock from 64K Source Divider form 14.318Mhz	
1	RW	0	SMBus IRQ Generate SCI Enable	
0	RW	0	SMBus Host Controller Enable 0: Disable SMB controller functions 1: Enable SMB controller functions	SMBEN

Offset Address: D3h (B0D17F0)
SMBus Host Slave Command
Default Value: 00h

Bit	Attribute	Default	Description
7:0	RW	00	SMBus Host Slave Command

Offset Address: D4h (B0D17F0)
SMBus Slave Address for Port 1
Default Value: 00h

Bit	Attribute	Default	Description
7:1	RW	0	SMBus Slave Address for Port 1
0	RW	0	Read / Write for Shadow Port 1

Offset Address: D5h (B0D17F0)
SMBus Slave Address for Port 2
Default Value: 00h

Bit	Attribute	Default	Description
7:1	RW	0	SMBus Slave Address for Port 2
0	RW	0	Read / Write for Shadow Port 2

Offset Address: D6h (B0D17F0)
SMBus Revision ID
Default Value: 00h

Bit	Attribute	Default	Description
7:0	RO	0	SMBus Revision ID

Offset Address: E0h (B0D17F0)
GPI Inversion Control
Default Value: 00h

Bit	Attribute	Default	Description
7:0	RW	0	GPI[27-24] , GPI[19-16] Input Inversion 0: Non-inverted 1: Inverted

Offset Address: E1h (B0D17F0)
GPI Inversion Control
Default Value: 00h

Bit	Attribute	Default	Description
7:0	RW	0	GPI[27-24] , GPI[19-16] SCI / SMI Selection 0: SCI 1: SMI

Offset Address: E2h (B0D17F0)
Internal PCIe and NB PLL Control
Default Value: 00h

Bit	Attribute	Default	Description
7:3	—	0	Reserved
2	RW	0	Enable Internal Hot Plug to Generate SCI/SMI Note: GPI19 SCI/SMI and related bits must be programmed.
1	RW	0	Enable Internal PM_PME to Generate SCI/SMI Note: GPI18 SCI/SMI and related bits must be programmed.
0	—	0	Reserved

Offset Address: E4h (B0D17F0)
Multi Function Select 1
Default Value: 00h

Bit	Attribute	Default	Description
7	RW	0	Fast VR Change Timer RxE5[7] controls the timer select 10/20 us. 0: Disable 1: Enable
6:5	—	0	Reserved
4	RW	0	Multiplexed Pins Selection for ACSDOUT1 or GPO21 0: ACSDOUT1 1: GPO21
3	RW	0	Multiplexed Pin Selection for GPIO18 / SLPBTN# / VGATE or GPIO 0: Select GPIO18 / SLPBTN# / VGATE 1: Select GPO8
2	RW	0	Multiplexed Pins Selection for PCI Request 5/6 or GPIO 0: Select (GPIO7, GPO7), (GPIO16, GPO20) 1: Select (REQ5#/GNT5#), (REQ6#/GNT6#)
1	RW	0	Multiplexed Pins Selection for PCISTP# or GPO6 0: PCISTP# 1: GPO6
0	RW	0	Multiplexed Pins Selection for CPUSTP# or GPO5 0: CPUSTP# 1: GPO5

Offset Address: E5h (B0D17F0)
Multi Function Select 2
Default Value: 00h

Bit	Attribute	Default	Description
7	RW	0	VR Change Timer Select 0: 100 us 1: 200us
6	RW	0	AGPBZ# as Source of Bus Master Status (BM_STS) 0: Disable 1: Enable
5	RW	0	EXT APIC Wake-up from PINTH 0: Disable 1: Enable
4	RW	0	VGATE from GPIO8 0: Disable 1: Enable
3	RW	0	CPU Deep Sleep and Speed Selection 0: GH# / DPSLP# / VIDSEL / VRDSLP 1: GPO22 / GPO23 / GPO28 / GPO29
2	RW	0	Multiplexed Pin Selection for ACSDIN3 or PCS1# 0: Select ACSDIN3 1: Select PCS1# Note: Please set Rx97[0] = 0 to enable this setting.
1	RW	0	Multiplexed Pin Selection for ACSDIN2 or PCS0# 0: Select ACSDIN2 1: Select PCS0# Note: Please set Rx97[0] = 0 to enable this setting.
0	RW	0	Enable SATALED# 0: Disable 1: Enable

Offset Address: E6h (B0D17F0)
Cx State Break Event Enable
Default Value: 00h

Bit	Attribute	Default	Description
7	RW	0	Parallel IDE or SATA Bus Master Break Event Enable 0: Disable 1: Enable
6	RW	0	PCI Express Bus Master Break Event Enable 0: Disable 1: Enable
5	RW	0	PCI Bus Master Break Event Enable 0: Disable 1: Enable
4	RW	—	Reserved
3	RW	0	AGPBZ# Bus Master Break Event Enable 0: Disable 1: Enable
2	RW	0	EHCI Bus Master Break Event Enable 0: Disable 1: Enable
1	RW	0	UHCI Bus Master Break Event Enable 0: Disable 1: Enable
0	RW	0	AC97/HDAC Bus Master Break Event Enable 0: Disable 1: Enable

Watchdog Timer Registers (E8-FCh)
Offset Address: EB-E8h (B0D17F0)
Watchdog Timer Memory Base
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:8	RW	0	Watchdog Timer Memory Base
7:0	RO	0	Hardwire to 00h

Offset Address: ECh (B0D17F0)
Watchdog Timer Control & C3 Latency Control
Default Value: 00h

Bit	Attribute	Default	Description
7:4	—	0	Reserved
3	RW	0	Extend C3 SLP De-assert to STPCLK# De-assert Time If PMIO Rx10[6] is set, extends to 30us. If not, extends to 15us.
2	RW	0	C3 VID / FID Latency Reduce to 5 us
1	RW	0	Watch Dog Timer Enable If set, can be reset only by PCIRST# 0: Disable 1: Enable
0	RW	0	Watchdog Timer Memory 0: Disable 1: Enable

ACPI IO Space Register (PMIO 0-0Bh)
Offset Address: 1-0h (PMIO)
Power Management Status
Default Value: 0000h

The bits in this register are set only by hardware and can be reset by software by writing a one to the desired bit position.

Bit	Attribute	Default	Description	Mnemonic
15	RW1C	0	Wakeup Status This bit is set when the system is in the suspend state and an enabled resume event occurs. Upon setting this bit, the system automatically transitions from the suspend state to the normal working state (from C3 to C0 for the processor).	
14	RW1C	0	PCI Express Wake Status	
13:12	—	0	Reserved	
11	RW1C	0	Power Status 0: Disable 1: Abnormal power off	
10	RW1C	0	RTC Alarm Status This bit is set when the RTC generates an alarm (on assertion of the RTC IRQ signal).	
9	RW1C	0	Sleep Button Status (GP18) This bit is set when the sleep button is pressed (SLPBTN# signal asserted low).	
8	RW1C	0	Power Button Status This bit is set when the PWRBTN# signal is asserted low. If the PWRBTN# signal is held low for more than four seconds, this bit is cleared, the Power Button Status bit is set, and the system will transition into the soft off state.	
7:6	—	0	Reserved	
5	RW1C	0	Global Status This bit is set by hardware when the BIOS Release bit is set (typically by an SMI routine to release control of the SCI / SMI lock). When this bit is cleared by software (by writing a one to this bit position) the BIOS Release bit is also cleared at the same time by hardware.	
4	RW1C	0	Bus Master Status This bit is set when a system bus master requests the system bus. All PCI master, ISA master and ISA DMA devices are included.	BM_STS
3:1	—	0	Reserved	
0	RW1C	0	ACPI Timer Carry Status The bit is set when the 23rd (31st) bit of the 24 (32) bit ACPI power management timer changes.	

Offset Address: 3-2h (PMIO)
Power Management Enable
Default Value: 0100h

The bits in this register correspond to the bits in the Power Management Status Register at offset 1-0.

Bit	Attribute	Default	Description
15	—	0	Reserved
14	RW	0	PCI Express Wake 0: Disable 1: Enable
13:11	—	0	Reserved
10	RW	0	RTC Alarm Enable This bit may be set to trigger either an SCI or an SMI (depending on the setting of the SCI Enable bit) to be generated when the RTC Status bit is set.
9	RW	0	Sleep Button Enable This bit may be set to trigger either an SCI or an SMI when the Sleep Button Status bit is set.
8	RW	1	Power Button This bit may be set to trigger either an SCI or an SMI (depending on the setting of the SCI Enable bit) to be generated when the Power Button Status bit is set.
7:6	—	0	Reserved
5	RW	0	Global Enable This bit may be set to trigger either an SCI or an SMI (depending on the setting of the SCI Enable bit) to be generated when the Global Status bit is set.
4:1	—	0	Reserved
0	RW	0	ACPI Timer Enable This bit may be set to trigger either an SCI or an SMI (depending on the setting of the SCI Enable bit) to be generated when the Timer Status bit is set.

Offset Address: 5-4h (PMIO)
Power Management Control
Default Value: 0000h

The bits in this register correspond to the bits in the Power Management Status Register at offset 1-0.

Bit	Attribute	Default	Description	Mnemonic
15	WO	0	Soft Resume This bit is used to allow a system using an AT power supply to operate as if an ATX power supply were being used. Refer to the BIOS Porting Guide for implementation details. 0: Disable 1: Enable	
14	—	0	Reserved	
13	WO	—	Sleep Enable This is a write-only bit; reads from this bit always return zero. Writing a one to this bit causes the system to sequence into the sleep (suspend) state defined by the Sleep Type field.	SLP_EN
12:10	RW	0	Sleep Type 000: Normal On 001: Suspend to RAM (STR) 010: Suspend to Disk (STD) (also called Soft Off). The VCC power plane is turned off while the VSUS33 and VBAT planes remain on. 011: Reserved 100: Power On Suspend without Reset 101: Power On Suspend with CPU/PCI Reset 11x: Reserved In any sleep state, there is minimal interface between powered and non-powered planes so that the effort for hardware design may be well managed.	
9	—	0	Reserved	
8	RW	0	STD Command Generates System Reset Only 0: Disable 1: Enable (STD command generates a system reset and not STD)	
7:3	—	0	Reserved	
2	WO	—	Global Release This bit is set by ACPI software to indicate the release of the SCI / SMI lock. Upon setting of this bit, the hardware automatically sets the BIOS Status bit. The bit is cleared by hardware when the BIOS Status bit is cleared by software. Note that the setting of this bit will cause an SMI to be generated if the BIOS Enable bit PMIO Rx2A[5] (BIOS_EN) is set.	
1	RW	0	Bus Master Reload This bit controls whether bus master requests (PMIO Rx00[4] = 1) transition the processor from C3 to C0 state. 0: Bus master requests are ignored by power management logic 1: Bus master requests transition the processor from the C3 state to the C0 state	
0	RW	0	SCI / SMI Select This bit controls whether SCI or SMI is generated for power management events triggered by the Power Button, Sleep Button, and RTC (when PMIO Rx1-0 bits 8, 9, or 10 equal one). 0: Generate SMI 1: Generate SCI Note that certain power management events can be programmed individually to generate an SCI or SMI independent of the setting of this bit (refer to the General Purpose SCI Enable and General Purpose SMI Enable registers at PMIO Rx22 and 24). Also, Timer Status & Global Status always generate SCI and BIOS Status always generates SMI.	

Offset Address: 0B-8h (PMIO)
ACPI Timer
Default Value: 0000h

Bit	Attribute	Default	Description
31:24	RO	0	Extended Timer Value This field reads back 0 if the 24-bit timer option is selected (Rx81 bit-3).
23:0	RO	0	Timer Value This read-only field returns the running count of the power management timer. This is a 24/32-bit counter that runs off a 3.579545 MHz clock, and counts while in the S0 (working) system state. The timer is reset to an initial value of zero during a reset, and then continues counting until the 14.31818 MHz input to the chip is stopped. If the clock is restarted without a reset, then the counter will continue counting from where it stopped.

Processor Power Management Registers (PMIO 10-16h)
Offset Address: 13-10h (PMIO)
Processor Control
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:12	—	0	Reserved
11	RW	0	Disable PCISTP# When CLKRUN# is De-asserted 0: Disable 1: Enable
10	RW	0	PCI Bus Clock Run Without Stop 0: CLKRUN# is always asserted 1: CLKRUN# will be de-activated after the PCI bus is idle for 26 clocks
9	RW	0	Host Clock Stop (CPUSTP#) This bit controls whether CPUSTP# is asserted in C3 and S1 states. Normally CPUSTP# is not asserted in C3 and S1 states, only STPCLK# is asserted. 0: CPUSTP# will not be asserted in C3 and S1 states (only STPCLK# is asserted) 1: CPUSTP# will be asserted in C3 and S1 states
8	RW	0	Assert SLP# for Processor Level 3 Read This bit controls whether SLP# is asserted in C3 state. 0: SLP# is not asserted in C3 state 1: SLP# is asserted in C3 state Used with Intel CPUs only.
7	RW	0	Lower CPU Voltage (VRDSLP Active) During C3 / S1 This bit controls whether the CPU voltage is lowered when in C3/S1 state. The voltage is lowered using the VRDSLP signal to the voltage regulator. PMIO RxE5[3] must be 0 to enable the voltage change function. Bits 8 and 9 of this register must also be set to 1. 0: Disable (normal voltage during C3/S1) 1: Enable (lower voltage during C3/S1) Note: 1. Enable to enter a C4 state in C3 command read and set Rx11[0] and Rx11[1] is a suggestion. 2. Reading LVL4 (Rx16) is the same behavior as reading LVL3 and set this bit. 3. VRDSLP will be active in either this bit set in C3 or LVL4 register read.
6	RW	0	SUSST# Assertion for C3 / C4 State
5	—	0	Reserved
4	RW	0	Throttling Enable Setting this bit starts clock throttling (modulating the STPCLK# signal) regardless of the CPU state. The throttling duty cycle is determined by bits 3-0 of this register.
3:0	RW	0	Throttling Duty Cycle

Offset Address: 14h (PMIO)
Processor Level 2
Default Value: 00h

Bit	Attribute	Default	Description
7:0	RO	0	Processor Level 2

Offset Address: 15h (PMIO)
Processor Level 3
Default Value: 00h

Bit	Attribute	Default	Description
7:0	RO	0	Processor Level 3

Offset Address: 16h (PMIO)
Processor Level 4
Default Value: 00h

Bit	Attribute	Default	Description
7:0	RO	0	Processor Level 4

General Purpose Power Management Registers (PMIO 20-52h)**Offset Address: 21-20h (PMIO)****General Purpose Status****Default Value: 0000h**

Bit	Attribute	Default	Description	Mnemonic
15	RW1C	0	SATA PME Status	
14	RW1C	0	USB Wake-Up in Suspend For STR / STD / Soff	WUSB_STS
13	RW1C	0	AC97 / HDAC Wake-Up Status Can be set only in suspend mode	
12	RW1C	0	Battery Low Status Set when the BATLOW# input is asserted low.	
11	RW1C	0	LID Status Set when the LID input detects the edge selected by Rx2C bit-7 0: Rising 1: Falling	
10	RW1C	0	Thermal Detect Status Set when the THRM# input detects the edge selected by Rx2C bit-6 0: Rising 1: Falling	
9	RW1C	0	Mouse Controller PME Status	
8	RW1C	0	Ring Status Set when the RING# input is asserted low.	
7	RW1C	0	GP3 Timer Timeout Status	PGP3TM
6	RW1C	0	INTRUDER# Status Set when the INTRUDER# pin is asserted low.	
5	RW1C	0	PME# Status Set when the PME# pin is asserted low.	
4	RW1C	0	EXTSMI# Status Set when the EXTSMI# pin is asserted low.	
3	RW1C	0	Internal LAN PME Status Set when the internal LAN PME signal is asserted.	
2	RW1C	0	Internal Keyboard Controller PME Status Set when the internal KBC PME signal is asserted.	
1	RW1C	0	GPI1 Status Set when the GPI1 pin is asserted low.	
0	RW1C	0	GPI0 Status Set when the GPIO pin is asserted low.	

Note that the above bits correspond one for one with the bits of the General Purpose SCI Enable and General Purpose SMI Enable registers at offsets 22 and 24: An SCI or SMI is generated if the corresponding bit of the General Purpose SCI or SMI Enable registers, respectively, is set to one. The above bits are set by hardware only and can only be cleared by writing a one to the desired bit.

Offset Address: 23-22h (PMIO)**General Purpose SCI / RESUME Enable****Default Value: 0000h**

Bit	Attribute	Default	Description
15	RW	0	Enable SCI on SATA PME
14	RW	0	Enable SCI on USB Wake Up
13	RW	0	Enable SCI on AC97/HDAC Wake Up
12	RW	0	Enable SCI on BATLOW#
11	RW	0	Enable SCI on LID
10	RW	0	Enable SCI on THRM Status
9	RW	0	Enable SCI on Mouse PME Status
8	RW	0	Enable SCI on RING
7	RW	0	Enable SCI on GP3 Timer Timeout
6	RW	0	Enable SCI on INTRUDER# Asserted
5	RW	0	Enable SCI on PME#
4	RW	0	Enable SCI on EXTSMI#
3	RW	0	Enable SCI on Internal LAN PME
2	RW	0	Enable SCI on Internal KBC PME
1	RW	0	Enable SCI on GPI1#
0	RW	0	Enable SCI on GPIO#

Offset Address: 25-24h (PMIO)
General Purpose SMI / RESUME Enable
Default Value: 0000h

Bit	Attribute	Default	Description
15	RW	0	Enable SMI on SATA PME Status
14	RW	0	Enable SMI on USB Wake Up
13	RW	0	Enable SMI on AC97/HDAC Wake Up
12	RW	0	Enable SMI on BATLOW
11	RW	0	Enable SMI on LID
10	RW	0	Enable SMI on THRM Status
9	RW	0	Enable SMI on Mouse PME Status
8	RW	0	Enable SMI on RING
7	—	0	Reserved
6	RW	0	Enable SMI on INTRUDER# Asserted
5	RW	0	Enable SMI on PME#
4	RW	0	Enable SMI on EXTSMI#
3	RW	0	Enable SMI on Internal LAN PME
2	RWC	0	Enable SMI on Internal KBC PME
1	RWC	0	Enable SMI on GPI1#
0	RWC	0	Enable SMI on GPIO#

Offset Address: 29-28h (PMIO)
Global Status
Default Value: 0000h

Bit	Attribute	Default	Description	Mnemonic
15	RW1C	0	GPIO Range 1 Access Status	PCS1_STS
14	RW1C	0	GPIO Range 0 Access Status	PCS0_STS
13	RW1C	0	GP3 Timer Timeout Status	PGP3TM
12	RW1C	0	GP2 Timer Timeout Status	PGP2TM
11	RW1C	0	SERIRQ SMI Status	
10	RW1C	0	Rx5[6] (SLP_EN) Write SMI Status This bit reports whether Rx5[6] is written. If Rx2B[3] is set to enable SMI, an SMI is generated when this bit = 1.	
9	RW1C	0	THRMTRIP# Activity Status	
8	RW1C	0	CLKRUN# Resume Status This bit is set when PCI bus peripherals wake up the system by asserting CLKRUN#	
7	RW1C	0	Primary IRQ/INIT/NMI/SMI Resume Status This bit is set at the occurrence of primary IRQs as defined in Rx85-84 of PCI configuration space	PINT1_STS
6	RW1C	0	Software SMI Status This bit is set when the SMI Command port (Rx2F) is written.	
5	RW1C	0	BIOS Status This bit is set when the Global Release bit is set to one (typically by the ACPI software to release control of the SCI/SMI lock). When this bit is reset (by writing a one to this bit position) the Global Release bit is reset at the same time by hardware.	
4	RW1C	0	Legacy USB Status This bit is set when a legacy USB event occurs. This is normally used for USB keyboards.	
3	RW1C	0	GP1 Timer Time Out Status This bit is set when the GP1 timer times out.	*PGP1TM
2	RW1C	0	GP0 Timer Time Out Status This bit is set when the GP0 timer times out.	*PGP0TM
1	RW1C	0	Secondary Event Timer Time Out Status This bit is set when the secondary event timer times out.	*PSEVTTM
0	RO	0	Primary Activity Status This bit can be cleared by writing 1 to ACPI IO Rx30-33	*PACT_STS

Note that SMI can be generated based on the setting of any of the above bits (see the Rx2A Global Enable register bit descriptions).

The bits in this register are set by hardware only and can only be cleared by writing a one to the desired bit position.
The bits in this register are for SMI's only while the bits in Rx21-20 are for SMI's and SCI's

Offset Address: 2B-2Ah (PMIO)
Global Enable
Default Value: 0200h

Bit	Attribute	Default	Description	Mnemonic
15	RW	0	SMI Enable on GPIO Range 1 Access	
14	RW	0	SMI Enable on GPIO Range 0 Access	
13	RW	0	SMI Enable on GP3 Timer Timeout	GP3TMEN
12	RW	0	SMI Enable on GP2 Timer Timeout	GP2TMEN
11	RW	0	SMI Enable on SERIRQ SMI	
10	RW	0	SMI Enable on PMIO Rx5 6 (SLP_EN) Write	
9	RW	1	THRMTRIP# Activity Power Off Enable	
8	RW	0	CLKRUN# Resume Enable This bit may be set to trigger an SMI to be generated when the CLKRUN# Resume Status bit is set.	
7	RW	0	Primary IRQ/INIT/NMI/SMI resume enable in POS state This bit may be set to trigger an SMI to be generated when the Primary IRQ / INIT / NMI / SMI Resume Status bit is set.	IRQRSMEN
6	RW	0	SMI Enable on Software SMI This bit may be set to trigger an SMI to be generated when the Software SMI Status bit is set.	
5	RW	0	SMI Enable on BIOS This bit may be set to trigger an SMI to be generated when the BIOS Status bit is set.	BIOS_EN
4	RW	0	SMI Enable on Legacy USB This bit may be set to trigger an SMI to be generated when the Legacy USB Status bit is set.	
3	RW	0	SMI Enable on GP1 Timer Timeout This bit may be set to trigger an SMI to be generated when the GP1 Timer Timeout Status bit is set.	GP1TMEN
2	RW	0	SMI Enable on GP0 Timer Timeout This bit may be set to trigger an SMI to be generated when the GP0 Timer Timeout Status bit is set.	GP0TMEN
1	RW	0	SMI Enable on Secondary Event Timeout This bit may be set to trigger an SMI to be generated when the Secondary Event Timer Timeout Status bit is set.	PSEVTEN
0	RW	0	SMI Enable on Primary Activity This bit may be set to trigger an SMI to be generated when the Primary Activity Status bit is set.	

Offset Address: 2D-2Ch (PMIO)
Global Control
Default Value: 0000h

Bit	Attribute	Default	Description
15:14	—	0	Reserved
13	RW	0	GPI18 / GPI19 SCI/SMI Enable
12	RW	0	NB SERR SCI/SMI Enable (routing to GPIO17) (If set, NB SERR generates SCI/SMI via GPIO17)
11	RW	0	IDE Secondary Bus Power-Off 0: Disable 1: Enable
10	RW	0	IDE Primary Bus Power-Off 0: Disable 1: Enable
9	—	0	Reserved
8	RW1C	0	SMI Active Status 0: SMI Inactive 1: SMI Active. If the SMI Lock bit is set, this bit needs to be written with a 1 to clear it before the next SMI can be generated.
7	RW	0	LID# Triggering Polarity 0: Rising Edge 1: Falling Edge
6	RW	0	THRM# Triggering Polarity 0: Rising Edge 1: Falling Edge
5	RW	0	Battery Low Resume Disable 0: Enable resume 1: Disable resume from suspend when BATLOW# is asserted
4:3	—	0	Reserved
2	RW	0	Power Button Triggering Select 0: SCI/SMI generated by PWRBTN# rising edge 1: SCI/SMI generated by PWRBTN# falling edge Set to zero to avoid the situation where the Power Button Status bit is set to wake up the system then reset again by PBOR Status to switch the system into the soft-off state.
1	RW	0	BIOS Release This bit is set by legacy software to indicate release of the SCI/SMI lock. Upon setting of this bit, hardware automatically sets the Global Status bit. This bit is cleared by hardware when the Global Status bit cleared by software. Note that if the Global Enable bit is set (Power Management Enable register Rx2[5]), then setting this bit causes an SCI to be generated (because setting this bit causes the Global Status bit to be set).
0	RW	0	SMI Enable 0: Disable all SMI generation 1: Enable SMI generation

Offset Address: 2Fh (PMIO)
SMI Command
Default Value: 00h

Bit	Attribute	Default	Description
7:0	RW	00h	SMI Command Writing to this port generates SMI

Offset Address: 33-30h (PMIO)
Primary Activity Detect Status
Default Value: 0000 0000h

These bits correspond to the Primary Activity Detect Enable bits in Rx37-34. If the corresponding bit is set in that register, setting of a bit below will cause the Primary Activity Status (PACT_STS) bit to be set (PMIO Rx28[0]). All bits in this register default to 0, are set by hardware only, and may only be cleared by writing 1s to the desired bit.

Bit	Attribute	Default	Description	Mnemonic
31:11	—	0	Reserved	
10	RW1C	0	Audio Status Set if Audio is accessed.	AUD_STS
9	RW1C	0	Keyboard Controller Access Status Set if the KBC is accessed via I/O port 60h.	KBC_STS
8	RW1C	0	VGA Access Status Set if the VGA port is accessed via I/O ports 3B0-3DFh or memory space A0000-BFFFFh.	VGA_STS
7	RW1C	0	LPT Port Status Set if the parallel port is accessed via I/O ports 278-27Fh or 378-37Fh (LPT2 or LPT1).	
6	RW1C	0	Serial Port B Access Status Set if the serial port is accessed via I/O ports 2F8-2FFh or 2E8-2Efh (COM2 and COM4 respectively).	COMB_STS
5	RW1C	0	Serial Port A Access Status Set if the serial port is accessed via I/O ports 3F8-3FFh or 3E8-3EFh (COM1 and COM3, respectively).	COMA_STS
4	RW1C	0	Floppy Access Status Set if the floppy controller is accessed via I/O ports 3F0-3F5h or 3F7h.	FDC_STS
3	RW1C	0	Secondary IDE Access Status Set if the IDE controller is accessed via I/O ports 170-177h or 376h.	SIDE_STS
2	RW1C	0	Primary IDE Access Status Set if the IDE controller is accessed via I/O ports 1F0-1F7h or 3F6h.	PIDE_STS
1	RW1C	0	Primary Interrupt Activity Status Set on the occurrence of a primary interrupt (enabled via the "Primary Interrupt Channel" register at Device 17 Function 0 PCI configuration register offset 84h).	PINT_STS
0	RW1C	0	PCI Master Access Status Set on the occurrence of PCI master activity.	DRQ_STS

Note: Setting of Primary Activity Status (PACT_STS) may be done to enable a "Primary Activity Event": An SMI will be generated if the Primary Activity Enable bit is set (PMIO Rx2A[0]) and/or the GP0 timer will be reloaded if the "GP0 Timer Reload on Primary Activity" bit is set (PMIO Rx38[0]).

Note: Bits 2-9 above also correspond to bits of GP Timer Reload Enable register Rx38: If bits are set in that register, setting a corresponding bit in this register will cause the GP1 timer to be reloaded.

Offset Address: 37-34h (PMIO)
Primary Activity Detect Enable
Default Value: 0000 0000h

These bits correspond to the Primary Activity Detect Status bits in Rx33-30. Setting of any of these bits also sets the Primary Activity Status (PACT_STS) bit (PMIO Rx28[0]) which causes the GP0 timer to be reloaded (if the Primary Activity GP0 Enable bit is set) or generates an SMI (if Primary Activity Enable is set).

Bit	Attribute	Default	Description
31:11	—	0	Reserved
10	RW	0	SMI on Audio Status 0: Don't set PMIO Rx29-28[0] (PACT_STS) if Rx33-30[10] (AUD_STS) is set 1: Set PACT_STS if AUD_STS is set
9	RW	0	SMI on Keyboard Controller Status 0: Don't set PACT_STS if Rx33-30[9] (KBC_STS) is set 1: Set PACT_STS if KBC_STS is set
8	RW	0	SMI on VGA Status 0: Don't set PACT_STS if Rx33-30[8] (VGA_STS) is set 1: Set PACT_STS if VGA_STS is set
7	RW	0	SMI on LPT Status
6	RW	0	SMI on Serial Port B Status 0: Don't set PACT_STS if Rx33-30[6] (COMB_STS) is set 1: Set PACT_STS if COMB_STS is set
5	RW	0	SMI on Serial Port A Status 0: Don't set PACT_STS if Rx33-30[5] (COMA_STS) is set 1: Set PACT_STS if COMA_STS is set
4	RW	0	SMI on Floppy Status 0: Don't set PACT_STS if Rx33-30[4] (FDC_STS) is set 1: Set PACT_STS if FDC_STS is set
3	RW	0	SMI on Secondary IDE Status 0: Don't set PACT_STS if Rx33-30[3] (SIDE_STS) is set 1: Set PACT_STS if SIDE_STS is set
2	RW	0	SMI on Primary IDE Status 0: Don't set PACT_STS if Rx33-30[2] (PIDE_STS) is set 1: Set PACT_STS if PIDE_STS is set
1	RW	0	SMI on Primary IRQ Status 0: Don't set PACT_STS if Rx33-30 [1] (PINT_STS) is set 1: Set PACT_STS if PINT_STS is set
0	RW	0	SMI on PCI Master Status 0: Don't set PACT_STS if Rx33-30[0] (DRQ_STS) is set 1: Set PACT_STS if DRQ_STS is set

Offset Address: 3B-38h (PMIO)
GP Timer Reload Enable
Default Value: 0000 0000h

All bits in this register default to 0 on power up.

Bit	Attribute	Default	Description
31:8	—	0	Reserved
7	RW	0	GP1 Timer Reload on KBC Access 0: Normal GP1 Timer Operation 1: Setting of KBC_STS causes the GP1 timer to reload.
6	RW	0	GP1 Timer Reload on Serial Port Access 0: Normal GP1 Timer Operation 1: Setting of COMA_STS or COMB_STS causes the GP1 timer to reload.
5	—	0	Reserved
4	RW	0	GP1 Timer Reload on VGA Access 0: Normal GP1 Timer Operation 1: Setting of VGA_STS causes the GP1 timer to reload.
3	RW	0	GP1 Timer Reload on Drive Access 0: Normal GP1 Timer Operation 1: Setting of FDC_STS, SIDE_STS, or PIDE_STS causes the GP1 timer to reload.
2	RW	0	GP3 Timer Reload on GPIO Range 1 Access 0: Normal GP3 Timer Operation 1: Setting of Rx29-28[15] (PCS1_STS) causes the GP3 timer to reload.
1	RW	0	GP2 Timer Reload on GPIO Range 0 Access 0: Normal GP2 Timer Operation 1: Setting of Rx29-28[14] (PCS0_STS) causes the GP2 timer to reload.
0	RW	0	GP0 Timer Reload on Primary Activity 0: Normal GP0 Timer Operation 1: Setting of PMIO Rx29-28[0] (PACT_STS) causes the GP0 timer to reload. Primary activities are enabled via the Primary Activity Detect Enable register (offset 37-34) with status recorded in the Primary Activity Detect Status register (offset 33-30).

Offset Address: 40h (PMIO)
Extend SMI/IO Trap Status
Default Value: 00h

Bit	Attribute	Default	Description	Mnemonic
7:5	—	0	Reserved	
4	RW1C	0	BIOS Write Access Status	BIOSW_STS
3	RW1C	0	GP3 Timer Second Timeout With No Cycles 0: Disable 1: Enable (GP3 timer timed out twice with no cycles in between)	
2	RW1C	0	GP3 Timer Second Timeout Status	GP3TO2_STS
1	RW1C	0	GPIO Range 3 Access Status	PCS3_STS
0	RW1C	0	GPIO Range 2 Access Status	PCS2_STS

Offset Address: 42h (PMIO)
Extend SMI/IO Trap Enable
Default Value: 04h

Bit	Attribute	Default	Description	Mnemonic
7:5	—	0	Reserved	
4	RW	0	SMI on BIOS Write Access This bit controls whether SMI is generated when BIOS Write Access Status Rx40[4] (BIOSW_STS) = 1. 0: Disable 1: Enable (can be reset only by PCI Reset)	
3	RW	0	GP3 Timer Second Timeout Override Enable 0: Enable GP3 timer second timeout reset, only when Rx42[2] (GP3TO2EN) set and SDOUT0 strapping to 0 1: Enable GP3 timer second timeout reset anyway, (override Rx42[2] and strapping)	
2	RW	1	GP3 Timer Second Timeout Reboot This bit controls whether the system is rebooted when the GP3 timer times out twice (Rx40[2] (GP3TO2_STS) = 1). 0: Disable 1: Enable	GP3TO2EN
1	RW	0	SMI on GPIO Range 3 Access This bit controls whether SMI is generated when GPIO range 3 is accessed (Rx40[1] (PCS3_STS) = 1) 0: Disable 1: Enable	
0	RW	0	SMI on GPIO Range 2 Access This bit controls whether SMI is generated when GPIO range 2 is accessed (Rx40[0] (PCS2_STS) = 1) 0: Disable 1: Enable	

Offset Address: 45-44h (PMIO)
EXTSMI and Miscellaneous Input Value
Default Value: 0000h

Bit	Attribute	Default	Description
15:13	—	0	Reserved
12	RO	0	Latest PCSn by IOR/IOW Status 0: IOR 1: IOW
11	RO	0	FM SMI or Serial SMI Status
10	—	0	Reserved
9	RO	0	SMBUS IRQ Status
8	RO	0	SMBUS Resume Status
7	RO	0	PM_PME Message Status
6	RO	0	PCI Express Hot Plug Status
5:0	—	0	Reserved

Offset Address: 47h (PMIO)
Extend General Purpose Input
Default Value: FFh

Bit	Attribute	Default	Description
7:0	RO	FFh	General Purpose Input (GPI[39:32])

Offset Address: 4B-48h (PMIO)
General Purpose Input
Default Value: nnnn nnnnh

Bit	Attribute	Default	Description
31:0	RO	nnnn nnnnh	General Purpose Input (GPI[31:0])

Offset Address: 4F-4Ch (PMIO)
General Purpose Output
Default Value: 03FF FFFFh

Reads from this register return the last value written (held on chip). Some GPIO pins can be used as both input and output. The output type of these pins is OD (open drain) so to use one of these pins as an input pin, a one must be written to the corresponding bit of this register.

Bit	Attribute	Default	Description
31:0	RW	03FFF FFFFh	General Purpose Output

Offset Address: 50h (PMIO)
GPI Change Status
Default Value: 00h

Bit	Attribute	Default	Description
7:0	RWIC	0	GPI [27:24], GPI[19:16] Pin Change Status

Note: 1. GPI17 / NB SERR:

If ACPI IO Rx2D[4] set, NB SERR status reflects in GPI17_STS, GPI17 event will be garterd.

2. GPI18 / PM_PME:

If ACPI IO Rx2D[5] set, GPI18 status reflects in GPI18_STS, PM_PME status reflects in GPI18_STS also.

3. GPI19 / HotPlug:

If ACPI IO Rx2D[5] set, GPI19 status reflects in GPI19_STS, Hot Plug status reflects in GPI19_STS also.

Offset Address: 52h (PMIO)
GPI Change SCI/SMI Enable
Default Value: 00h

Bit	Attribute	Default	Description
7:0	RW	0	GPI [27:24], GPI[19:16] Pin Change SCI / SMI 0: SCI on pin input change 1: SMI on pin input change

IO Trap Registers (PMIO 54-5Dh)
Offset Address: 57-54h (PMIO)
I/O Trap PCI Data
Default Value: nnnn nnnnh

Bit	Attribute	Default	Description
31:0	RO	nnnn nnnnh	PCI Data During I/O Trap SMI

Offset Address: 59-58h (PMIO)
I/O Trap PCI I/O Address
Default Value: nnnnh

Bit	Attribute	Default	Description
15:0	RO	nnnnh	PCI Address During I/O Trap SMI

Offset Address: 5Ah (PMIO)
I/O Trap PCI Command / Byte Enable
Default Value: nnh

Bit	Attribute	Default	Description
7:4	RO	nh	PCI Command Type During I/O Trap SMI
3:0	RO	nh	PCI Byte Enable During I/O Trap SMI

Offset Address: 5Ch (PMIO)
CPU Performance
Default Value: 00h

Bit	Attribute	Default	Description
7:1	—	0	Reserved.
0	RW	0	CPU Frequency Select 0: High 1: Low

Offset Address: 5Dh (PMIO)
Scratch Register
Default Value: 00h

Bit	Attribute	Default	Description
7:0	RW	00h	Scratch Register

Watchdog Timer Memory Base (MMIO 0-7h)
Offset Address: 3-0h (MMIO)
Watchdog Control / Status
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:8	—	0	Reserved
7	WO	0	Watchdog Trigger
6:4	—	0	Reserved
3	RO	0	Watchdog Disable
2	RW	0	Watchdog Action 0: Reset 1: Power off
1	RW1C	0	Watchdog Fired
0	RW	0	Watchdog Enable 0: Stop Watchdog 1: Run Watchdog

Offset Address: 7-4h (MMIO)
Count
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:10	—	0	Reserved
9:0	WO	0	Count Register

System Management Bus I/O Space Registers (SMIO 0-Fh)

The base address for these registers is defined in RxD1-D0 of the Device 17 Function 0 PCI configuration registers. The System Management Bus I/O space is enabled for access by the system if Device 17 Function 0 RxD2[0] (SMBEN) = 1.

Offset Address: 0h (SMIO)

SMBus Host Status

Default Value: 00h

Bit	Attribute	Default	Description	Mnemonic
7	—	0	Reserved	
6	RW1C	0	SMB Semaphore This bit is used as a semaphore among various independent software threads that may need to use the Host SMBus logic and has no effect on hardware. After reset, this bit reads 0. Writing 1 to this bit causes the next read to return 0, then all reads after that return 1. Writing 0 to this bit has no effect. Software can therefore write 1 to request control and if readback is 0 then it will own usage of the host controller.	
5	—	0	Reserved	
4	RW1C	0	Failed Bus Transaction 0: SMBus interrupt not caused by failed bus transaction 1: SMBus interrupt caused by failed bus transaction. This bit may be set when SMIO Rx2[1] (KILL) is set and can be cleared by writing a 1 to this bit position.	FAILED
3	RW1C	0	Bus Collision 0: SMBus interrupt not caused by transaction collision 1: SMBus interrupt caused by transaction collision. This bit is only set by hardware and can be cleared by writing a 1 to this bit position.	
2	RW1C	0	Device Error 0: SMBus interrupt not caused by generation of an SMBus transaction error 1: SMBus interrupt caused by generation of an SMBus transaction error (illegal command field, unclaimed host-initiated cycle, or host device timeout). This bit is only set by hardware and can be cleared by writing a 1 to this bit position.	
1	RW1C	0	SMBus Interrupt 0: SMBus interrupt not caused by host command completion 1: SMBus interrupt caused by host command completion. This bit is only set by hardware and can be cleared by writing a 1 to this bit position.	
0	RO	0	Host Busy 0: SMBus controller host interface is not processing a command 1: SMBus host controller is busy processing a command. None of the other SMBus registers should be accessed if this bit is set.	HOST_BUSY

Offset Address: 1h (SMIO)
SMBus Slave Status
Default Value: 00h

Bit	Attribute	Default	Description
7:6	—	0	Reserved
5	RW1C	0	Alert Status 0: SMBus interrupt not caused by SMBALRT# signal 1: SMBus interrupt caused by SMBALRT# signal. This bit will be set only if the Alert Enable bit in SMIO Rx8[3] (ALERT_EN) is set. This bit is only set by hardware and can be cleared by writing a 1 to this bit position.
4	RW1C	0	Shadow 2 Status 0: SMBus interrupt not caused by address match to SMBus Shadow Address Port 2 1: SMBus interrupt or resume event caused by slave cycle address match to SMBus Shadow Address Port 2. This bit is only set by hardware and can be cleared by writing a 1 to this bit position.
3	RW1C	0	Shadow 1 Status 0: SMBus interrupt not caused by address match to SMBus Shadow Address Port 1 1: SMBus interrupt or resume event caused by slave cycle address match to SMBus Shadow Address Port 1. This bit is only set by hardware and can be cleared by writing a 1 to this bit position.
2	RW1C	0	Slave Status 0: SMBus interrupt not caused by slave event match 1: SMBus interrupt or resume event caused by slave cycle event match of the SMBus Slave Command Register at SMIO RxD3 (command match) and the SMBus Slave Event Register at SMIO Rx0A (data event match). This bit is only set by hardware and can be cleared by writing a 1 to this bit position.
1	—	0	Reserved
0	RO	0	Slave Busy 0: SMBus controller slave interface is not processing data 1: SMBus controller slave interface is busy receiving data. None of the other SMBus registers should be accessed if this bit is set.

Offset Address: 2h (SMIO)
SMBus Host Control
Default Value: 00h

Bit	Attribute	Default	Description	Mnemonic
7	—	0	Reserved	
6	RW	0	Start 0: Writing 0 has no effect 1: Start Execution of Command Writing a 1 to this bit causes the SMBus controller host interface to initiate execution of the command programmed in the SMBus Command Protocol field (bits 4-2). All necessary registers should be programmed prior to writing a 1 to this bit. The Host Busy bit SMIO Rx0[0] (HOST_BUSY) can be used to identify when the SMBus controller has completed command execution.	
5:2	RW	0	SMBus Command Protocol Selects the type of command the SMBus host controller will execute. Reads or Writes are determined by Rx4[0] (SMB_RW). Protocol 0000: Quick 0001: Byte 0010: Byte Data 0011: Word Data 0100: Process Call 0101: Block 0110: I2C with 10-bit Address 0111: Reserved 10xx: Reserved 1100: I2C Process Call 1101: I2C Block 1110: I2C with 7-bit Address 1111: Universal	
1	RW	0	Kill Transaction in Progress 0: Normal host controller operation 1: Stop host transaction currently in progress. Setting this bit also sets the status bit SMIO Rx0[4] (FAILED) and asserts the interrupt selected by the SMB Interrupt Select bit SMIO RxD2[3] (SMB_INTSEL)	KILL
0	RW	0	Interrupt Enable 0: Disable interrupt generation 1: Enable generation of interrupts on completion of the current host transaction.	

Offset Address: 3h (SMIO)
SMBus Host Command
Default Value: 00h

Bit	Attribute	Default	Description
7:0	RW	0	SMBus Host Command This field contains the data transmitted in the command field of the SMBus host transaction.

Offset Address: 4h (SMIO)
SMBus Host Address
Default Value: 00h

The contents of this register are transmitted in the address field of the SMBus host transaction.

Bit	Attribute	Default	Description	Mnemonic
7:1	RW	0	SMBus Address This field contains the 7-bit address of the targeted slave device.	
0	RW	0	SMBus Read or Write 0: Execute a WRITE command 1: Execute a READ command	*SMB_RW

Offset Address: 5h (SMIO)
SMBus Host Data 0
Default Value: 00h

The contents of this register are transmitted in the Data 0 field of SMBus host transaction writes. On reads, Data 0 bytes are stored here.

Bit	Attribute	Default	Description
7:0	RW	0	SMBus Data 0 For Block Write commands, this field is programmed with the block transfer count (a value between 1 and 32). Counts of 0 or greater than 32 are undefined. For Block Read commands, the count received from the SMBus device is stored here.

Offset Address: 6h (SMIO)
SMBus Host Data 1
Default Value: 00h

The contents of this register are transmitted in the Data 1 field of SMBus host transaction writes. On reads, Data 1 bytes are stored here.

Bit	Attribute	Default	Description
7:0	RW	0	SMBus Data 1 This register should be programmed with the value to be transmitted in the Data 1 field of an SMBus host interface transaction

Offset Address: 7h (SMIO)
SMBus Block Data
Default Value: 00h

Reads and writes to this register are used to access the 32-byte block data storage array. An internal index pointer is used to address the array. It is reset to 0 by reads of the SMIO Rx2 and incremented automatically by each access to this register. The transfer of block data into (read) or out of (write) this storage array during an SMBus transaction always starts at index address 0.

Bit	Attribute	Default	Description
7:0	RW	0	SMBus Block Data

Offset Address: 8h (SMIO)
SMBus Slave Control
Default Value: 00h

Reads and writes to this register are used to access the 32-byte block data storage array. An internal index pointer is used to address the array. It is reset to 0 by reads of the SMIO Rx2 and incremented automatically by each access to this register. The transfer of block data into (read) or out of (write) this storage array during an SMBus transaction always starts at index address 0.

Bit	Attribute	Default	Description	Mnemonic
7:4	—	0	Reserved	
3	RW	0	SMBus Alert Enable 0: Disable 1: Enable generation of an interrupt or resume event on the assertion of the SMBALRT# signal	ALERT_EN
2	RW	0	SMBus Shadow Port 2 Enable 0: Disable 1: Enable generation of an interrupt or resume event on external SMBus master generation of a transaction with an address that matches the SMBus Slave Shadow Port 2 register (SMIO RxD5).	
1	RW	0	SMBus Shadow Port 1 Enable 0: Disable 1: Enable generation of an interrupt or resume event on external SMBus master generation of a transaction with an address that matches the SMBus Slave Shadow Port 1 register (SMIO RxD4).	
0	RW	0	SMBus Slave Enable 0: Disable 1: Enable generation of an interrupt or resume event on external SMBus master generation of a transaction with an address that matches the SMBus host controller slave port of 10h, a command field which matches the SMBus Slave Command register (SMIO RxD3), and a match of one of the corresponding enabled events in the SMBus Slave Event Register (SMIO Rx0A).	

Offset Address: 9h (SMIO)
SMBus Shadow Command
Default Value: 00h

This register is used to store command values for external SMBus master accesses to the host slave and slave shadow ports.

Bit	Attribute	Default	Description
7:0	RO	0	Shadow Command This field contains the command value which was received during an external SMBus master access whose address field matched the host slave address (10h) or one of the slave shadow port addresses.

Offset Address: 0B-0Ah (SMIO)
SMBus Slave Event
Default Value: 0000h

This register is used to enable generation of interrupt or resume events for accesses to the host controller's slave port.

Bit	Attribute	Default	Description
15:0	RW	0	SMBus Slave Event This field contains data bits used to compare against incoming data to the SMBus Slave Data Register (SMIO Rx0C). When a bit in this register is set and the corresponding bit in the Slave Data register is also set, an interrupt or resume event will be generated if the command value matches the value in the SMBus Slave Command register and the access was to SMBus host address 10h.

Offset Address: 0D-0Ch (SMIO)
SMBus Slave Data
Default Value: 0000h

This register is used to store data values for external SMBus master accesses to the shadow ports or the SMBus host controller's slave port.

Bit	Attribute	Default	Description
15:0	RO	0	SMBus Slave Data This field contains the data value which was transmitted during an external SMBus master access whose address field matched one of the slave shadow port addresses or the SMBus host controller slave port address of 10h.

System Management Bus-Specific Configuration Registers (SMIO D0-54h)
Offset Address: D1-D0h (SMIO)
SMBus I/O Base Address
Default Value: 0000h

Bit	Attribute	Default	Description
15:4	RW	0	Index Register Base Address Correspond to I/O address signals AD[15:4] respectively
3:0	—	0	Reserved. Read as 0

Offset Address: D2h (SMIO)
SMBus Host Configuration
Default Value: 00h

Bit	Attribute	Default	Description	Mnemonic
7:4	—	0	Reserved. Read as 0	
3	RW	0	SMBus Slave Interface Interrupt Select Select SCI / SMI generated by the SMBus controller. 0: SMI 1: SCI	SMB_INTRESEL
2	—	0	Reserved	
1			SMBus Host Interface Interrupt Control 0: Disable SCI 1: Enable SCI	
0	RW	0	SMBus Host Slave Command 0: Disable 1: Enable SMB Controller Host Interface	

Offset Address: D3 (SMIO)
SMBus Slave Command
Default Value: 00h

Bit	Attribute	Default	Description
7:0	RW	00	SMBus Host Slave Command Specifies the command values to be matched for SMBus master accesses to the SMBus controller host slave interface (SMBus port 10h).

Offset Address: D4h (SMIO)
SMBus Slave Shadow Port 1
Default Value: 00h

Bit	Attribute	Default	Description
7:1	RW	0	SMBus Slave Address for Shadow Port 1 Specifies the address used to match against incoming SMBus addresses for shadow port 1
0	RW	0	Read / Write for Shadow Port 1 This bit must be programmed to 0 since SMBus slave controller only responds to Word Write transactions.

Offset Address: D5h (SMIO)
SMBus Slave Shadow Port 2
Default Value: 00h

Bit	Attribute	Default	Description
7:1	RW	0	SMBus Slave Address for Shadow Port 2 Specifies the address used to match against incoming SMBus addresses for shadow port 2.
0	RW	0	Read / Write for Shadow Port 2 This bit must be programmed to 0 since SMBus slave controller only responds to Word Write transactions.

Offset Address: D6h (SMIO)
SMBus Revision Identification
Default Value: 00h

Bit	Attribute	Default	Description
7:0	RO	0	Revision ID This register returns the current revision ID for the SMBus Host/Slave controller.

Offset Address: 54h (SMIO)
SMBus Revision Identification
Default Value: 80h

Bit	Attribute	Default	Description
7	RO	0	SMBus Clock Source Select 0: From 14MHz 1: From RTC Clock
6:0	—	0	Reserved

Bus 0 Device 17 Function 5 (B0D17F5) – AC97 Audio Controller

The audio controller interface is hardware compatible with AC97. The PCI configuration registers for the audio controller are located in the function 5 PCI configuration space. The I/O registers are located in the system I/O space.

PCI Configuration Space Header (0-3Fh)

Offset Address	Attribute	Default	Description
1 – 0h	RO	1106h	Vendor ID
3 – 2h	RO	3059h	Device ID
5 – 4h	RW	0000h	Command
7 – 6h	RO	0210h	Status
8h	RO	70h	Revision ID
0B-9h	RO	040100h	Class Code
0D	RO	00	Latency Timer
0Eh	RO	00h	Header Type (Multifunction Device)
0Fh	RO	00h	BIST
13-10h	RW	0000 0001h	Base Address 0 (SGD Control / Status)
1F-14h	RO	00h	Reserved
2F – 2Ch	RO	00h	Subsystem ID / Subsystem Vendor ID This register is RW if function 5 Rx42[5] = 1
33-30h	RO	00h	Expansion ROM
34h	RO	C0	Capture Pointer
3Ch	RW	00h	Interrupt Line
3Dh	RO	03h	Interrupt Pin
3Eh	RO	00h	Minimum Grant
3Fh	RO	00h	Maximum Latency

Offset Address: 5-4h (B0D17F5)

Command

Default Value: 0000h

Bit	Attribute	Default	Description
15:11	—	00	Reserved
10	RW	0	Interrupt Disable
9	RO	0	Fast Back-to-Back
8	RO	0	SERR# Enable
7	RO	0	Address Stepping
6	RO	0	Parity Error Response
5	RO	0	VGA Palette Snoop
4	RO	0	Memory Write and Invalidate
3	RO	0	Special Cycle Monitoring
2	RW	0	Bus Master
1	RO	0	Memory Space
0	RW	0	I/O Space

Offset Address: 7-6h (B0D17F5)

Status

Default Value: 0210h

Bit	Attribute	Default	Description
15	RO	0	Detect Parity Error
14	RO	0	Signaled System Error
13	RO	0	Receive Master Abort
12	RO	0	Receive Target Abort
11	RO	0	Signaled Target Abort
10:9	RO	01	DEVSEL# Timing
8	RO	0	Data Parity Detected
7	RO	0	Fast B-to-B Capable
6:5	—	0	Reserved
4	RO	1	PM 1.1 Support
3	RO	0	Interrupt Status
2:0	—	0	Reserved

Configuration Space Audio Codec-Specific Registers (40-C7h)
Offset Address: 40h (B0D17F5)
AC 97 Interface Status Register
Default Value: 00h

Bit	Attribute	Default	Description
7:6	—	0	Reserved
5	RO	0	Secondary CODEC CID=11b Ready 0: Codec Not Ready 1: Codec Ready (Audio Controller can access codec)
4	RO	0	Secondary CODEC CID=10b Ready 0: Codec Not Ready 1: Codec Ready (Audio Controller can access codec)
3	—	0	Reserved
2	RO	0	Secondary CODEC CID=01b Ready 0: Codec Not Ready 1: Codec Ready (Audio Controller can access codec)
1	RO	0	AC97 is in Low Power Mode 0: AC97 Codecs not in low-power mode 1: AC97 Codecs in low-power mode This bit reports 1 when Rx26[12] of the codecs is 1. It is used to determine whether the bit-clock should be gated.
0	RO	0	Primary CODEC Ready 0: Codec Not Ready 1: Codec Ready (Audio Controller can access codec)

Offset Address: 41h (B0D17F5)
AC97 Interface Control Register
Default Value: 00h

Bit	Attribute	Default	Description
7	RW	0	AC-Link Interface 0: Disable AC-Link Interface 1: Enable AC-Link Interface
6	RW	0	AC-Link Reset 0: Assert AC-Link Reset (At least 1 us to reset AC97 Codec) 1: De-assert AC-Link Reset
5	RW	0	AC-Link Sync AC97 Controller uses this bit for wake up from power down mode. Min. 4 frame time following the power down was triggered, and drive SYNC high for min. 1us (to wake up CODEC) 0: De-assert (release SYNC) 1: Force SYNC high
4	RW	0	AC-Link Serial Data Out 0: Release SD_OUT 1: Force SD_OUT high
3	RW	0	Variable-Sample-Rate On-Demand Mode 0: Disable variable sample rate ON_DEMAND mode 1: Enable variable sample rate ON DEMAND mode
2	RW	0	AC-Link outputs RD Channel PCM Data
1	RW	0	Free Running Clock 0: Dynamic Stop Clock 1: Free Running Clock
0	—	0	Reserved

Offset Address: 42h (B0D17F5)
Function Enable
Default Value: 00h

Bit	Attribute	Default	Description
7:6	—	0	Reserved
5	RW	0	Device 17 Function 5 Subsystem ID and Subsystem Vendor ID Back Door Enable Specifies whether Device 17 Function 5 Rx2C~2F are RO or RW 0: Device 17 Function 5 Rx2C-2F RO 1: Device 17 Function 5 Rx2C-2F RW
4:0	—	0	Reserved

Offset Address: 4Ch (B0D17F5)
DXS Channel Volume
Default Value: 00h

Bit	Attribute	Default	Description
7:6	—	0	Reserved
5:0	RO	0	DX0-DX3 Volume in SRC

Offset Address: C3-C0h (B0D17F5)
Power Management Capability
Default Value: 0602 0001h

Bit	Attribute	Default	Description
31:0	RO	0602 0001h	Power Management Capability

Offset Address: C7-C4h (B0D17F5)
Power State
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:2	RO	0000 0000h	Power Management Capability
1:0	RW	00	Power State 00: D0 10: D2 01: D1 11: D3

I/O Space Register Base 0 (x0-xFh)
DXS Channel 0-3 SGD Registers (x = 0-3)
Offset Address: x0h
DXSx Channel SGD Status

Bit	Attribute	Default	Description
7	RO	—	SGD Active 0: SGD has completed or been terminated 1: SGD Active
6:5	—	0	Reserved
4	RO	—	Current SGD Index Equals Stop Index 0: SGD index not equal to stop index 1: SGD index being processed equals the stop index. This bit differs from bit-2 of this register in that this bit becomes 1 as soon as the SGD reaches the index equal to the stop index. Bit-2 becomes 1 after the SGD finishes processing the index equal to the stop index. So this bit will always turn on before bit-2.
3	RO	—	SGD Trigger Queued This bit reports whether the trigger used to restart the SGD operation is queued (I/O Offset x1[1] = 1 while the SGD engine is running). 0: SGD trigger not queued 1: SGD trigger queued (when SGD reaches EOL, it will restart).
2	RWC	—	SGD Stop Interrupt Status 1: SGD finished the index equal to the stop index set in xB-x8[31-24].
1	RWC	—	SGD EOL (End Of Link) 1: Block is the last of the link. May be used by software as a signal to generate an interrupt request if I/O Offset x1[1] = 1.
0	RWC	—	SGD Flag 1: Block complete. May be used by software as a signal to generate an interrupt request if I/O Offset x1[0] = 1.

Offset Address: x1h
DXSx Channel SGD Control
Default Value: 00h

Bit	Attribute	Default	Description
7	WO	0	SGD Start (Always reads 0) 0: No effect 1: Start SGD operation
6	WO	0	SGD Terminate (Always reads 0) The SGD pointer reset to bits base address 0: No effect 1: Start SGD operation
5	RW	0	SGD Auto-Start 0: Stop at EOL 1: Auto Restart at EOL
4	—	0	Reserved
3	RW	0	SGD Pause 0: Release pause and resume the transfer 1: Pause SGD read operation (SGD pointer stays at the current address). SGD will finish transferring the current block before pausing.
2	RW	0	Interrupt on Stop Index = Current Index and End of Block Controls whether an interrupt is generated when the current index equals the stop index (x0[2] = 1). 0: Disable 1: Enable
1	RW	0	Interrupt on EOL at End of Block Controls whether an interrupt is generated on EOL (x0[1] = 1). 0: Disable 1: Enable
0	RW	0	Interrupt on FLAG at End-of-Block Controls whether an interrupt is generated on FLAG (x0[0] = 1). 0: Disable 1: Enable

Offset Address: x2h
DXS Left Channel x Volume
Default Value: 3Fh

Bit	Attribute	Default	Description
7:6	—	0	Reserved
5:0	RW	111111	Left Volume Control 000000: 0db 011111: -46.5db 000111: -10.5db 111111: muted (instead -94.5 db)

Offset Address: x3h
DXS Right Channel x Volume
Default Value: 3Fh

Bit	Attribute	Default	Description
7:6	—	0	Reserved
5:0	RW	111111	Right Volume Control 000000: 0db 011111: -46.5db 000111: -10.5db 111111: muted (instead -94.5 db)

Offset Address: x7-x4h
SGD Table Pointer
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:0	RW	00000000	SGD Table Pointer Base Address (even address)

Offset Address: x8-xBh
StopIndex / DataType / SampleRate
Default Value: FF0F FFFFh

Bit	Attribute	Default	Description
31:24	RW	FFh	SGD Stop Index Setting SGD operation will stop at the end of the entry
23:22	—	0	Reserved
21	RW	0	0: 8-bit 1: 16-bit
20	RW	0	0: 8-bit 1: 16-bit
19:0	RW	FFFFFh (48K)	DXSx Channel Sample Rate This field allows the sample rate converter to know the sample rate of an incoming sample so the converter can properly convert the sample into the required 48 KHz sample output. Program as (220 / 48.000) * Sample Rate

Offset Address: xF-xCh
SGD Current Count

Bit	Attribute	Default	Description
31:24	RO	—	Current SGD Index This field reports the index the SGD engine is currently processing.
23:0	RO	—	Current SGD Count This field reports the count remaining in the current entry being processed. For example, if 10 bytes of a 30-byte count have been transferred, this field would read 20 to indicate 20 bytes remaining.

3D Channel SGD Control / Status (40-4Fh)
Offset Address: 40h
3D Channel SGD Status
Default Value: 00h

Bit	Attribute	Default	Description
7	RO	0	SGD Active 0: SGD has completed or been terminated 1: SGD Active
6:5	—	0	Reserved
4	RO	0	Current SGD Index Equals Stop Index 0: SGD index not equal to stop index 1: SGD index being processed equals the stop index. This bit differs from bit-2 of this register in that this bit becomes 1 as soon as the SGD reaches the index equal to the stop index. Bit-2 becomes 1 after the SGD finishes processing the index equal to the stop index. So this bit will always turn on before bit-2.
3	RO	0	SGD Trigger Queued This bit reports whether the trigger used to restart the SGD operation is queued (I/O Offset 41[1] = 1 while the SGD engine is running). 0: SGD trigger not queued 1: SGD trigger queued (when SGD reaches EOL, it will restart).
2	RW1C	—	SGD Stop Interrupt Status 1: Current SGD Stop is set Write 1 to clear, also clear the interrupt (if Rx41[2] (RSTOPINT) is set)
1	RW1C	—	SGD EOL (End Of Link) 1: Current SGD EOL is set Write 1 to clear, also clear the interrupt (if Rx41[1] (REOLINT) is set)
0	RW1C	—	SGD Flag 1: Flag is set Write 1 to clear, also clear the interrupt (if Rx41[0] (RFLAGINT) is set)

Offset Address: 41h
3D Channel SGD Control
Default Value: 00h

Bit	Attribute	Default	Description
7	WO	0	SGD Start (Always reads 0) 0: No effect 1: Start SGD operation
6	WO	0	SGD Terminate (Always reads 0) 0: No effect 1: Terminate SGD operation
5	RW	0	SGD Auto-Start 0: Stop at EOL 1: Auto Restart at EOL
4	RW	0	Center / LFE Playback Order 0: Keep Center & LFE playback order (3,4,7,8,6,9) 1: Swap Center & LFE playback order (3,4,7,8,9,6)
3	RW	0	SGD Pause 0: Release pause and resume the transfer 1: Pause SGD read operation (SGD pointer stays at the current address). SGD will finish transferring the current block before pausing.
2	RW	0	Interrupt on Stop Index = Current Index and End of Block Controls whether an interrupt is generated when the current index equals the stop index (Rx40[2] = 1). 0: Disable 1: Enable
1	RW	0	Interrupt on EOL at End of Block Controls whether an interrupt is generated on EOL (Rx40[1] = 1). 0: Disable 1: Enable
0	RW	0	Interrupt on FLAG at End-of-Block Controls whether an interrupt is generated on FLAG (Rx40[0] = 1). 0: Disable 1: Enable

Offset Address: 42h
3D Channel SGD Format
Default Value: 00h

Bit	Attribute	Default	Description
7	RW	0	PCM Format Selects the PCM format used by the controller to process the incoming sample. 0: 8-bit 1: 16-bit
6:4	RW	000	Number of Channels Supported 001: One Channel 010: Two Channels 100: Four Channels 110: Six Channels
3:0	—	0	Reserved

Offset Address: 43h
DRA Register
Default Value: 00h

Bit	Attribute	Default	Description
7:4	—	0	Reserved
3	RW	0	8 Channels Playback (3/4/6/9/7/8/10/11) 0: Enable 8 CH 1: Disable 8 CH
2	RW	0	Secondary SDOUT Pin 0: AC97 has 1 SDOUT pin 1: AC97 has 2 SDOUT pin (for VT1617) Sample N is put in master sdout slot (3,4,7,8,6,9) Sample N+1 is put in slave sdout slot (3,4,7,8,6,9)
1	RW	0	Double Rate Audio Mode 0: Disable 1: Enable total valid sample number of each frame is (2 * CNO) if Rx49[3] (ENSPDIF)=1 & Rx49[2] (DRS)=1 hardware will ignore DRA bit, and using 3D engine to transfer S/PDIF data {DRS, DRA, SNO} slot valid 5'b0_0_001 3,4 (mono) 5'b0_0_010 3,4 (stereo) 5'b0_0_100 3,4,7,8 5'b0_0_110 3,4,7,8,6,9 5'b0_1_010 3,4,7,8 (for AC97 2.3) 5'b0_1_011 3,4,6,10,11,12 (for AC97 2.3)
0	RW	0	3D Engine Data Format 0: See RX42[7] 1: 20-bit

Offset Address: 47-44h
SGD Table Pointer
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:0	RW	00	SGD Table Pointer Base Address (even address)

Offset Address: 4B-48h
SGD SLOT-Select
Default Value: FF00 0000h

Bit	Attribute	Default	Description
31:24	RW	FFh	Stop Entry Index
23:0	—	0	Reserved

Offset Address: 4F-4Ch
SGD Count Pointer
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:24	RO	0	Current SGD Index
23:0	RO	0	Current SGD Count

Table 8. Playback Mode Configuration

SDDOUT1_EN	DRA Rx43[1]	SP_EN	DRS Rx49[2]	Playback Mode
	■			PCM double rate audio
	■	■		PCM double rate audio & S/PDIF
		■		S/PDIF
		■	■	S/PDIF double rate
■				PCM 6-ch 96k
■	■			PCM 6-ch 96k
■		■		PCM 6-ch 96k & S/PDIF in slot 10/11
■		■	■	PCM 6-ch 96k & S/PDIF 96k Sdout_0-----(pcm sample N) (s/pdif sample N) Sdout_1-----(pcm sample N+1) (s/pdif sample N+1)

Write Channel 0 SGD Registers (60-6Fh)
Offset Address: 60h
Write Channel SGD Status

Bit	Attribute	Default	Description
7	RO	—	SGD Active 0: SGD has completed or been terminated 1: SGD Active
6	RO	—	SGD Paused 0: SGD not paused 1: SGD Paused
5	—	0	Reserved
4	RO	—	Current SGD Index Equals Stop Index 0: SGD index not equal to stop index 1: SGD index being processed equals the stop index. This bit differs from bit-2 of this register in that this bit becomes 1 as soon as the SGD reaches the index equal to the stop index. Bit-2 becomes 1 after the SGD finishes processing the index equal to the stop index. So this bit will always turn on before bit-2.
3	RO	—	SGD Trigger Queued This bit reports whether the trigger used to restart the SGD operation is queued (I/O Offset 61[1] = 1 while the SGD engine is running). 0: SGD trigger not queued 1: SGD trigger queued (when SGD reaches EOL, it will restart).
2	RW1C	—	SGD Stop Interrupt Status R: 1: Current SGD Flag is set. Write 0: No effect Write 1 to clear
1	RW1C	—	SGD EOL (End Of Link) R: 1: Current SGD Flag is set. Clear the interrupt if I/O Offset 61[1] (WEOLINT) is set Write 0: No effect Write 1 to clear
0	RW1C	—	SGD Flag R: 1: Current SGD Flag is set Write 0: No effect Write 1 to clear. SGD continues the next block and clear the interrupt if I/O Offset 61[0] (WFLANGINT) = 1.

Offset Address: 61h
Write Channel SGD Control

Bit	Attribute	Default	Description
7	RW1C	—	SGD Start (Always reads 0) 0: No effect 1: Start SGD operation
6	RW1C	—	SGD Terminate (Always reads 0) 0: No effect 1: Terminate SGD operation
5	RW	—	SGD Auto-Start 0: Stop at EOL 1: Auto Restart at EOL
4	—	0	Reserved
3	RW	—	SGD Pause 0: Release pause and resume the transfer 1: Pause SGD read operation (SGD pointer stays at the current address). SGD will finish transferring the current block before pausing.
2	RW	—	Interrupt on STOP at End of Transfer 0: Disable 1: Enable
1	RW	—	Interrupt on EOL at End of Transfer Controls whether an interrupt is generated on EOL (60[1] = 1). 0: Disable 1: Enable
0	RW	—	Interrupt on FLAG at End-of-Block Controls whether an interrupt is generated on FLAG (60[0] = 1). 0: Disable 1: Enable

Offset Address: 62h
Write Channel 0 SGD Format
Default Value: 00h

Bit	Attribute	Default	Description
7	—	0	Reserved
6	RW	0	Recording FIFO 0: Disable 1: Enable
5:0	—	0	Reserved

Offset Address: 63h
Write Channel 0 Input Select
Default Value: 00h

Bit	Attribute	Default	Description
7:3	—	0	Reserved
2	RW	0	Input Source Select 0: Line In (Slot 3, 4) 1: Mic In (Slot 6)
1:0	RW	00	Recording Source Select 00: Primary Codec 10: Secondary Codec 10 01 Secondary Codec 01 11: Secondary Codec 11

Offset Address: 67-64h
SGD Table Pointer
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:0	RW	00	SGD Table Pointer Base Address (even address)

Offset Address: 6B-68h
SGD Slot-Select
Default Value: FF00 0000h

Bit	Attribute	Default	Description
31:24	RW	FFh	SGD Stop Entry Index
23:22	—	0	Reserved
21	RW	0	PCM Format 0: 8bits 1: 16bits
20	RW	0	PCM Format 0: MONO# Format 1: STEREO
19:0	—	0	Reserved

Offset Address: 6F-6Ch
SGD Table Pointer
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:24	RO	—	Current SGD Index This field reports the index the SGD engine is currently processing.
23:0	RO	—	Current SGD Count This field reports the count remaining in the current entry being processed. For example, if 10 bytes of a 30-byte count have been transferred, this field would read 20 to indicate 20 bytes remaining.

Table 9. Scatter-Gather DMA Table Format

	31	30	29	28:24	23:16	15:8	7:0
High DW	EOL	FLAG	STOP	Reserved	BASE COUNT [23:0]		
Low DW	BASE ADDRESS [31:0]						

Register name	Description	Width
EOL	End of Link If set, indicate this block is the last one if xEOLINT is set, the SGD issues Interrupt at the end of the transfer	1
FLAG	Block Flag if xFLAGINT is set, the SGD issues Interrupt at the end of this block	1
STOP*	STOP at end of the block *Only supported in MODEM channels	1
BASE COUNT	Base Byte Count of the Block	24
BASE ADDRESS	Base Address of the Block	32

Codec Command / Status SGD Register (80-AFh)

This register may be accessed from either function 5 or 6.

Offset Address: 83-80h
AC97 Controller Command
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:30	RW	0	Codec ID 00: Select Primary Codec 10: Select Secondary Codec 10 01: Select Secondary Codec 11: Select Secondary Codec
29	W1C	0	Codec 11 Data / Status / Index Valid 0: Not Valid 1: Valid (OK to Read bits 0-23)
28	W1C	0	Codec 10 Data / Status / Index Valid 0: Not Valid 1: Valid (OK to Read bits 0-23)
27	W1C	0	Codec 01 Data / Status / Index Valid 0: Not Valid 1: Valid (OK to Read bits 0-23)
26	—	0	Reserved
25	W1C	0	Codec 00 Data / Status / Index Valid 0: Not Valid 1: Valid (OK to Read bits 0-23)
24	W1C	0	AC97 Controller Busy 0: Codec is ready for a register access command 1: AC97 Controller is sending a command to the codec (commands are not accepted)
23	RW	0	Codec Register Read / Write Mode 0: Select Codec register write mode 1: Select Codec register read mode
22:16	RW	0	Codec Register Index [7:1] Index of the AC97 codec register to access (in the attached codec). Data must be written before or at the same time as Index because writing to the index triggers the AC97 controller to access the addressed codec register over the AC-link interface.
15:0	RW	0	AC97 Command / Status Register Data Write 0's in read command

Note: 1. For accessing codec registers protocol information, please refer to the AC97 spec.

2. The DATA must be written before or at the same time as INDEX

3. Write any value to INDEX byte will trigger the AC-Link to access the AC97 CODEC registers

4. AC97 Controller will not accept command while in busy state (i.e. bit24 = 1)

5. ECHO_INDEX and STA_DATA are valid only when STA_VLD or STA_VLD1 is 1

6. Write 1 to corresponding bit will clear Valid Bit (bit 25 and 27).

Offset Address: 87-84h
Scatter-Gather Global IRQ
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31	RO	0	Shadow RX70[7]
30	RO	0	Shadow RX70[2]
29	RO	0	Shadow RX70[1]
28	RO	0	Shadow RX70[0]
27	RO	0	Shadow RX60[7]
26	RO	0	Shadow RX60[2]
25	RO	0	Shadow RX60[1]
24	RO	0	Shadow RX60[0]
23	RO	0	Shadow RXA0[7]
22	RO	0	Shadow RXA0[6]
21	RO	0	Shadow RXA0[5]
20	RO	0	Shadow RXA0[4]
19	RO	0	Shadow RX60[7]
18	RO	0	Shadow RX60[2]
17	RO	0	Shadow RX60[1]
16	RO	0	Shadow RX60[0]
15	RO	0	Shadow RX30[7]
14	RO	0	Shadow RX30[2]
13	RO	0	Shadow RX30[1]
12	RO	0	Shadow RX30[0]
11	RO	0	Shadow RX20[7]
10	RO	0	Shadow RX20[2]
9	RO	0	Shadow RX20[1]
8	RO	0	Shadow RX20[0]
7	RO	0	Shadow RX10[7]
6	RO	0	Shadow RX10[2]
5	RO	0	Shadow RX10[1]
4	RO	0	Shadow RX10[0]
3	RO	0	Shadow RX00[7]
2	RO	0	Shadow RX00[2]
1	RO	0	Shadow RX00[1]
0	RO	0	Shadow RX00[0]

Offset Address: 8C-88h
DX and 3D Audio FIFO Count

Offset Address	Attribute	Default	Description
88h	RO	00h	DX0 FIFO Count Total Valid Data Bytes in DX0 Engine
89h	RO	00h	DX1 FIFO Count Total Valid Data Bytes in DX1 Engine
8Ah	RO	00h	DX2 FIFO Count Total Valid Data Bytes in DX2 Engine
8Bh	RO	00h	DX3 FIFO Count Total Valid Data Bytes in DX3 Engine
8Ch	RO	00h	3D Audio FIFO Count Total Valid Data Bytes in 3D Audio Engine

Offset Address: 9F-90h
Mapped from Function 5/6 Rx40-4F

Offset Address: A0h
Jack Sense Interrupt
Default Value: 00h

Bit	Attribute	Default	Description
7	RW	0	Jack Sense Status for sdin_3 (W12C) 0: No jack be inserted 1: Detect jack be inserted
6	RW	0	Jack Sense Status for sdin_2(W12C) 0: No jack be inserted 1: Detect jack be inserted
5	RW	0	Jack Sense Status for sdin_1(W12C) 0: No jack be inserted 1: Detect jack be inserted
4	RW	0	Jack Sense Status for sdin_0(W12C) 0: No jack be inserted 1: Detect jack be inserted
3	RW	0	Jack Sense from sdin_3 Interrupt 0: Disable 1: Enable
2	RW	0	Jack Sense from sdin_2 Interrupt 0: Disable 1: Enable
1	RW	0	Jack Sense from sdin_1 Interrupt 0: Disable 1: Enable
0	RW	0	Jack Sense from sdin_0 Interrupt 0: Disable 1: Enable

Offset Address: AE-AFh
Shadow Function 6 Rx8E-8F
Default Value: 00h

Bit	Attribute	Default	Description
15:0	RO	00	Shadow Function 6 Rx8E-8F 0: Disable modem interrupt 1: Enable modem interrupt when GPI change status

Note: JS and modem GPI are mutually exclusive. For example, controller will consider sdinx slot12 data is audio interrupt status when user enable jack sense interrupt no matter modem GPI interrupt is enabled or not.

Bus 0 Device 17 Function 6 Registers - AC97 Modem Controller

The modem controller interface is hardware compatible with AC97. The PCI configuration registers for the modem controller are located in the function 6 PCI configuration space. The I/O registers are located in the system I/O space.

PCI Configuration Space Header (0-3Fh)

Offset Address	Attribute	Default	Description
1 – 0h	RO	1106h	Vendor ID
3 – 2h	RO	3068h	Device ID
5 – 4h	RW	0000h	Command
7 – 6h	RO	0210h	Status
8h	RO	80h	Revision ID
9-0Bh	RO	0780000h	Class Code
0Dh	RO	00h	Latency Time
0Eh	RO	00h	Header Type
0Fh	RO	00h	BIST
13-10h	RW	00000001h	Base Address 0 (SGD Control / Status)
27-14h	—	0	Reserved
33-30h	RO	00h	Expansion ROM
34h	RO	D0h	Capture Pointer
3B-35h	—	0	Reserved
3Ch	RW	00h	Interrupt Line
3Dh	RO	04h	Interrupt Pin
3Eh	RO	00h	Minimum Grant
3Fh	RO	00h	Maximum Latency

Offset Address: 5-4h (B0D17F6)

Command

Default Value: 0000h

Bit	Attribute	Default	Description
15:11	—	00	Reserved
10	RW	0	Interrupt Disable
9	RO	0	Fast Back-to-Back
8	RO	0	SERR# Enable
7	RO	0	Address Stepping
6	RO	0	Parity Error Response
5	RO	0	VGA Palette Snoop
4	RO	0	Memory Write and Invalidate
3	RO	0	Special Cycle Monitoring
2	RW	0	Bus Master
1	RO	0	Memory Space
0	RW	0	I/O Space

Offset Address: 7-6h (B0D17F6)
Status
Default Value: 0210h

Bit	Attribute	Default	Description
15	RO	0	Detect Parity Error
14	RO	0	Signaled System Error
13	RO	0	Receive Master Abort
12	RO	0	Receive Target Abort
11	RO	0	Signaled Target Abort
10:9	RO	01	DEVSEL# Timing
8	RO	0	Data Parity Detected
7	RO	0	Fast Back-to-Back Capable
6:5	—	0	Reserved
4	RO	1	PM 1.1 Support
3	RO	0	Interrupt Status
2:0	—	0	Reserved

Configuration Space Modem Codec-Specific Registers (40-D7h)
Offset Address: 40h (B0D17F6)
AC 97 Interface Status Register
Default Value: 00h

Bit	Attribute	Default	Description
7:6	—	0	Reserved
5	RO	0	Secondary CODEC CID=11b Ready 0: Codec Not Ready 1: Codec Ready (Audio Controller can access codec)
4	RO	0	Secondary CODEC CID=10b Ready 0: Codec Not Ready 1: Codec Ready (Audio Controller can access codec)
3	—	0	Reserved
2	RO	0	Secondary CODEC CID=01b Ready 0: Codec Not Ready 1: Codec Ready (Audio Controller can access codec)
1	RO	0	AC97 is in Low Power Mode 0: AC97 Codecs not in low-power mode 1: AC97 Codecs in low-power mode This bit reports 1 when Rx26[12] of the codecs is 1. It is used to determine whether the bit-clock should be gated.
0	RO	0	Primary CODEC Ready 0: Codec Not Ready 1: Codec Ready (Audio Controller can access codec)

Offset Address: 41h (B0D17F6)
AC97 Interface Control Register
Default Value: 00h

This register is also can be written from function 5.

Bit	Attribute	Default	Description
7	RW	0	AC-Link Interface 0: Disable AC-Link Interface 1: Enable AC-Link Interface
6	RW	0	AC-Link Reset 0: Assert AC-Link Reset (used for cold reset) 1: De-assert AC-Link Reset
5	RW	0	AC-Link Sync 0: De-assert (release SYNC) AC97 Controller use this bit for wake up from power down mode. Min. 4 frame time following the power down was triggered , and drive SYNC high for min. 1us (to wake up CODEC) 1: Force SYNC high
4	RW	0	AC-Link Serial Data Out 0: Release SD_OUT 1: Force SD_OUT high
3:0	—	0	Reserved

Offset Address: 44h (B0D17F6)
MC97 Interface Control
Default Value: 00h

Mapped RO to function 5 (RW in func 6) for status reporting.

Bit	Attribute	Default	Description
7	RW	0	AC-Link Interface for Slot-5 (Modem) 0: Disable 1: Enable
6	RW	0	Secondary Codec Support 0: Disable 1: Enable
5	RW	0	Function 6 Configuration Register Rx9-0Bh Writable 0: Device 17 Function 6 Rx9-0Bh RO 1: Device 17 Function 6 Rx9-0Bh RW
4	RW	0	Function 6 Configuration Register Rx2C-2Fh Writable 0: Device 17 Function 6 Rx2C-2F RO 1: Device 17 Function 6 Rx2C-2F RW
3	RW	0	Sync This bit reports whether there is activity in function 6 (modem). When function 5 (audio) enters low-power state and wants to gate bit-clock, software needs to check this bit to see whether bit-clock can actually be gated, as function 6 shares the same bit-clock. 0: Function 6 activity in progress that requires bit-clock 1: Function 6 does not need bit-clock so bit-clock can be gated
2	RW	0	AC97 Supports Modem Power States D1/D2 0: Can't support D1/D2 power states 1: Support D1/D2 power states
1:0	—	0	Reserved

Offset Address: D3-D0h (B0D17F6)
Power Management Capability
Default Value: 0002 0001h

Bit	Attribute	Default	Description
31:0	RO	0002 0001h	Power Management Capability If Rx44[2]=0 , 00020001h If Rx44[2]=1 , 06020001h

Offset Address: D7-D4h (B0D17F6)
Power State
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:2	RO	0	Power Management Capability
1:0	RW	00	Power State 00: D0 10: D2 01: D1 11: D3

I/O Base 0 Registers-Modem Scatter / Gather DMA (40-87h)
Modem SGD Read Channel Registers (40-87h)
Offset Address: 40h
Modem SGD Read Channel Status
Default Value: 00h

Bit	Attribute	Default	Description
7	RO	0	SGD Active 0: SGD has completed or been terminated 1: SGD Active
6	RO	0	SGD Paused 0: SGD not paused 1: SGD Paused
5:4	—	0	Reserved
3	RO	0	SGD Trigger Queued This bit reports whether the trigger used to restart the SGD operation is queued (I/O Offset 41[1] = 1 while the SGD engine is running). 0: SGD trigger not queued 1: SGD trigger queued (when SGD reaches EOL, it will restart).
2	W1C	0	SGD Stop Interrupt Status SGD finished the index equal to the stop index set in 4B-48[31-24].
1	W1C	0	SGD EOL (End Of Link) Block is the last of the link. May be used by software as a signal to generate an interrupt request if I/O Offset 41[1] = 1.
0	W1C	0	SGD Flag Block complete. May be used by software as a signal to generate an interrupt request if I/O Offset 41[0] = 1.

Offset Address: 41h
Modem SGD Read Channel Status
Default Value: 00h

Bit	Attribute	Default	Description
7	WO	0	SGD Start 0: No effect 1: Start SGD read channel operation
6	WO	0	SGD Terminate 0: No effect 1: Terminate SGD read channel operation
5:4	—	0	Reserved (Do not Program)
3	RW	0	SGD Pause 0: Release SGD read channel pause and resume the transfer from the paused line 1: Pause SGD read channel operation (SGD read channel pointer stays at the current address)
2:1	—	0	Reserved
0	RW	0	Modem SGD Read Reset 0: Normal Operation 1: Reset Modem SGD read channel operation

Offset Address: 42h
Modem SGD Read Channel Type
Default Value: 00h

Bit	Attribute	Default	Description
7	RW	0	Auto-Start SGD at EOL 0: Stop at EOL 1: Auto restart at EOL
6:4	—	0	Reserved
3:2	RW	00	Interrupt Select This bit determines the timing of interrupt generation when bit-1 or bit-0 of this register are equal to 1. 00: Interrupt at PCI Read of Last Line 01: Interrupt at Last Sample Sent 10: Interrupt at Less Than One Line to Send 11: -reserved-
1	RW	0	Interrupt on EOL at End of Block 0 Disable 1: Enable
0	RW	0	Interrupt on FLAG at End-of-Block 0 Disable 1: Enable

Offset Address: 47-44h
Modem SGD R Ch Table Pointer Base
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:0	RW	0000 0000h	W: SGD Table Pointer Base Address (even address) R: Current Pointer Address

Offset Address: 4F-4Ch
Modem SGD R Ch Current Count
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:24	RO	—	Current Modem SGD Read Channel Index This field reports the index the SGD engine is currently processing.
23:0	RO	—	Current Modem SGD Read Channel Count This field reports the count remaining in the current entry being processed. For example, if 10 bytes of a 30-byte count have been transferred, this field would read 20 to indicate 20 bytes remaining.

Offset Address: 50h
Modem SGD Read Channel Status
Default Value: 00h

Bit	Attribute	Default	Description
7	RW	0	SGD Active 0: SGD has completed or been terminated 1: SGD Active
6	RO	0	SGD Paused 0: SGD not paused 1: SGD Paused
5:4	RO	0	Reserved
3	RO	0	SGD Trigger Queued This bit reports whether the trigger used to restart the SGD operation is queued (I/O Offset 41[1] = 1 while the SGD engine is running). 0: SGD trigger not queued 1: SGD trigger queued (when SGD reaches EOL, it will restart).
2	RO	0	Reserved
1	RW1C	0	SGD EOL (End Of Link) Block is the last of the link. May be used by software as a signal to generate an interrupt request if I/O Offset 52[1] (MWEOLINT) = 1.
0	RW1C	0	SGD Flag 1: Flag is set Write 1 to clear, also clear the interrupt (if I/O Offset Rx52[0] (MWFLAGINT) is set)

Offset Address: 51h
Modem SGD Write Channel Control
Default Value: 00h

Bit	Attribute	Default	Description
7	WO	0	SGD Start 0: No effect 1: Start SGD write channel operation
6	WO	0	SGD Terminate 0: No effect 1: Terminate SGD write channel operation
5:4	—	0	Reserved
3	RW	0	SGD Pause 0: Release SGD write channel pause and resume the transfer from the paused line 1: Pause SGD write channel operation (SGD write channel pointer stays at current address)
2	—	0	Reserved
1	RW	0	Reset Modem SGD Write Operation
0	—	0	Reserved

Offset Address: 52h
Modem SGD Write Channel Type
Default Value: 00h

Bit	Attribute	Default	Description
7	RW	0	Auto-Start SGD at EOL 0: Stop at EOL 1: Auto restart at EOL
6:2	—	0	Reserved
1	RW	0	Interrupt on EOL at End of Block 0 Disable 1: Enable
0	RW	0	Interrupt on FLAG at End-of-Block 0 Disable 1: Enable

Offset Address: 57-54h
Modem SGD W Ch Table Pointer Base
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:0	RW	0000 0000h	W: SGD Table Pointer Base Address (even address) R: Current Pointer Address

Offset Address: 5C-5Eh
Modem SGD W Ch Current Count
Default Value: 00 0000h

Bit	Attribute	Default	Description
23:0	RO	0	Current SGD Count This field reports the count remaining in the current entry being processed. For example, if 10 bytes of a 30-byte count have been transferred, this field would read 20 to indicate 20 bytes remaining.

Offset Address: 5Fh
Current Modem SGD Write Channel Index
Default Value: 00h

Bit	Attribute	Default	Description
7:0	RO		Current SGD Index This field reports the index the SGD engine is currently processing.

Offset Address: 87-85h
Scatter-Gather Global IRQ
Default Value: 00 0000h

Bit	Attribute	Default	Description
23:22	—	0	Reserved
21	RO	0	Modem Write SGD Active Shadow
20	RO	0	Modem Read SGD Active Shadow
19:18	—	0	Reserved
17	RO	0	Modem Write SGD Stop Shadow
16	RO	0	Modem Read SGD Stop Shadow
15:14	—	0	Reserved
13	RO	0	Modem Write SGD EOL Shadow
12	RO	0	Modem Read SGD EOL Shadow
11:10	—	0	Reserved
9	RO	0	Modem Write SGD Flag Shadow
8	RO	0	Modem Read SGD Flag Shadow
7:1	—	0	Reserved
0	RO	0	Sdin slot12[0] status. (controller will not issue interrupt)

MC97 GPIO Registers Accessing Port (88-8Fh)

Offset Address: 8B-88h

GPIO Registers (SLOT12)

Default Value: 0000 0000h

This register may be accessed from either function 5 or 6

Bit	Attribute	Default	Description
31:16	RW1C	0	GPI Interrupt Status Read: GPI[15-0] Interrupt Status Write: 1 to clear
15:0	RW	0	Codec GPIO Read: Reflect status of Codec GPIO[15-0] Write: Triggers AC-Link slot-12 output to codec

Offset Address: 8F-8Ch

GPIO Registers (SLOT12)

Default Value: 0000 0000h

This register may be accessed from either function 5 or 6

Bit	Attribute	Default	Description
31:16	RW	0	Interrupt on GPI[15-0] Change of Status 0 Disable 1: Enable
15:0	—	0	Reserved

Mapped Registers and MISC Control Registers (90-E7h)

Offset Address: 9F-90h

Mapped from Function 5/6 Rx40-4F

Default Value: 00h

Offset Address: E7h

MC97 Early Master Control

Bit	Attribute	Default	Description
7:1	—	0	Reserved
0	RW	0	MC97 Early Master Transaction Reflects to PMIO Rx0[4] (BM_STS) 0: Disable 1: Enable

Bus 0 Device 17 Function 7 (B0D17F7): Ultra V-LINK Control

This configuration is provided to facilitate the configuration of the South Bridge V-Link controller without requiring new enumeration code. This function is represented as bus number 0, device number 17, function 7.

Header Registers (0-3Fh)

Offset Address	Attribute	Default	Description
1 – 0h	RO	1106h	Vendor ID
3 – 2h	RO	287Eh	Device ID

Offset Address: 5-4h (B0D17F7)

PCI Command

Default Value: 0000h

Bit	Attribute	Default	Description
15:10	—	0	Reserved
9	RO	0	Fast Back-to-Back Cycle Enable Hardwired to 0.
8	RW	0	SERR# Enable Hardwired to 0.
7	—	0	Reserved
6	RW	0	Parity Error Response 0: Ignore parity errors 1: Perform parity check and take normal action on detected parity errors
5	RO	0	VGA Palette Snooping Hardwired to 0.
4	RO	0	Memory Write and Invalidate Hardwired to 0
3	RO	0	Respond To Special Cycle Hardwired to 0.
2	RW	0	Bus Master 0: Never behaves as a bus master 1: Enable to operate as a bus master on the secondary interface
1	RW	0	Memory Space Access 0: Does not respond to memory space access 1: Responds to memory space access
0	RO	0	I/O Space Access 0: Does not respond to I/O space access 1: Responds to I/O space access

Offset Address: 7-6h (B0D17F7)

PCI Status

Default Value: 0210h

Bit	Attribute	Default	Description
15	RW1C	0	Parity Error Detected Set by PERRS, reset by writing 1.
14	RW1C	0	SERR# Detected Note. Set if ECC error
13	RW1C	0	Set When Terminated with Master-Abort, Except Special Cycle 0: No abort received 1: Transaction aborted by the master
12	RW1C	0	Set When Received a Target-Abort 0: No abort received 1: Transaction aborted by the target
11	RO	0	Set When Signaled a Target-Abort
10-9	RO	01	DEVSEL# Timing 00: Fast 01: Medium (default) 10: Slow 11: Reserved
8	RW1C	0	Set When Set or Observed SERR# and Parity Error Reserved
7	RO	0	Capable of Accepting Fast Back-to-Back as a Target Reserved
6	—	0	Reserved
5	RO	0	66 MHz Capable
4	RO	1	Support New Capability List
3:0	—	0	Reserved

Offset Address: 8h (B0D17F7)
Revision ID
Default Value: 00h

Bit	Attribute	Default	Description
7:0	RO	0	Revision ID

Offset Address: 0B-9h (B0D17F7)
PCI Header Registers
Default Value: 068000h

Bit	Attribute	Default	Description
23:0	RO	068000h	Class Code

Offset Address: 0Dh (B0D17F7)
Latency Timer
Default Value: 00h

Bit	Attribute	Default	Description	Mnemonic
7:0	RW	00h	Latency Timer Bit 2-0 (MLT[2:0]): reserved (RO), guarantee time slice for CPU master	MLT[7:0]

Offset Address: 0Eh (B0D17F7)
Header Type
Default Value: 00h

Bit	Attribute	Default	Description
7:0	RO	00h	Header Type It adheres to the Type 0 PCI Configuration.

Offset Address: 0Fh (B0D17F7)
Built In Self Test (BIST)
Default Value: 00h

Bit	Attribute	Default	Description
7	RO	0	BIST Support
6:0	—	0	Reserved

Offset Address: 2D-2Ch (B0D17F7)
Subsystem Vendor ID
Default Value: 1106h

Bit	Attribute	Default	Description
15:0	RO	1106h	Subsystem Vendor ID

Offset Address: 2E-2Fh (B0D17F7)
Subsystem ID
Default Value: 287Eh

Bit	Attribute	Default	Description
15:0	RO	287Eh	Subsystem ID

Offset Address: 34h (B0D17F7)
Capability Pointer
Default Value: 58h

Bit	Attribute	Default	Description
7:0	RO	58h	Capability Pointer Byte offset into configuration space to capability list

V-Link Control Interface (40–52h)
Offset Address: 40h (B0D17F7)
V-Link Specification ID
Default Value: F7h

Bit	Attribute	Default	Description
7:4	—	Fh	Reserved
3:0	RO	7h	South Bridge Revision ID 0 & F: Means the old version of 8 bits, the operating mode is determined by RX48[0] (R8XVK) 1: means the support of V-Link capability is up to mode 1. 2: the support of V-Link capability is up to mode 2. 3: the support of V-Link capability is up to mode 3. 4: the support of V-Link capability is up to mode 4. 5: the support of high priority upstream read. 6: the support of high priority upstream read and write.

Table 10. V-Link Modes Supported

	X: Multiples of 66Mhz cycle	Bus Width	RSVKH _W (B0D17F7 Rx4F[5])	RSVKH _R (B0D17F7 Rx4F[4])	R8XVK (B0D17F7 Rx48[0])	RX16VK (B0D17F7 Rx48[5])	RVKSP (B0D17F7 Rx48[1])
Mode 0	4X	8-bit	X	X	0	0	-
Mode 1	8X	4-bit	X	X	1	0	1
Mode 2	8X	8-bit	X	X	1	0	0
Mode 3	4X	16-bit	X	X	0	1	0
Mode 4	8X	8-bit	X	X	1	1	1
Mode 5	High-Priority Read		0	1	X	X	X
Mode 6	High-Priority Read & Write		1	1	X	X	X
Mode 7	RCRB Supported				B0D19F0 RX44~46 ≠ 0		

Offset Address: 41h (B0D17F7)
Reserved
Default Value: 24h

Bit	Attribute	Default	Description
7:0	RO	24h	Reserved

Offset Address: 43h (B0D17F7)
Reserved
Default Value: 80h

Bit	Attribute	Default	Description
7:0	RO	80h	Reserved

Offset Address: 44h (B0D17F7)
Reserved
Default Value: 82h

Bit	Attribute	Default	Description
7:0	RO	82h	Reserved

Offset Address: 48h (B0D17F7)
V-Link Configuration – SB
Default Value: 1Ah

This register is used to configure V-Link bus controller on South bridge chips.

Bit	Attribute	Default	Description
7	RW	0	Parity Check 0: Disable 1: Enable
6	—	0	Reserved
5	RW	0	16-Bit Width 0: Disable 1: Enable
4	RW	1	8-Bit Width 0: Disable 1: Enable
3	RW	1	4X Rate 0: Disable 1: Enable
2	RW	0	2X Rate 0: Disable 1: Enable
1	RW	1	V-Link Split Bus 0: Disable 1: Enable
0	RW	0	8X Rate 0: Disable 1: Enable

Offset Address: 49h (B0D17F7)
V-Link Capability - SB
Default Value: 3Bh

Bit	Attribute	Default	Description
7	RW1C	0	V-Link Parity Error Detected
6	—	0	Reserved
5	RO	1	16-Bit Bus Width 0: Not Support 1: Support
4	RO	1	8-Bit Bus Width 0: Not Support 1: Support
3	RO	1	4X Rate 0: Not Support 1: Support
2	RO	0	2X Rate 0: Not Support 1: Support
1	RO	1	V-Link Split Bus Native 8X Mode Support 0: Not Support 1: Support
0	RO	1	8X Rate 0: Not Support 1: Support

Offset Address: 4Ah (B0D17F7)
SB Downlink (C2P) Status
Default Value: 88h

Bit	Attribute	Default	Description
7:4	RO	8h	C2P Request Depth Max # of DNCMD (C2P) requests 0000 - depth of 1 ... 1111 - depth of 16
3:0	RO	8h	C2P Write Buffer Size Max # of DW, depth from 1 to 16

Offset Address: 4Bh (B0D17F7)
SB Uplink (P2C) Configuration I
Default Value: 80h

Bit	Attribute	Default	Description
7:4	RW	8h	P2C Request Depth Max # of outstanding UPCMD (P2C) requests 0000: 16 level (only VT8251) 0001: 1 level 0010: 2 level 0011: 3 level 0100: 4 level 0101: 5 level 0110: 6 level 0111: 7 level 1000: 8 level 1111: 15 level
3:2	—	0	Reserved
1:0	RW	00	High Priority P2C Request Depth 00: 1 levels 01: 4 levels 10: 8 levels 11: 16 levels

Offset Address: 4Ch (B0D17F7)
SB Uplink (P2C) Configuration II
Default Value: 82h

Bit	Attribute	Default	Description
7:4	RW	8h	P2C Write Buffer Size (max # of lines)
3:0	RW	2h	P2P Write Buffer Size (max # of lines)

Offset Address: 4Dh (B0D17F7)
SB V-Link Bus Timer
Default Value: 44h

Bit	Attribute	Default	Description	Mnemonic
7:4	RW	0100	V-Link Bus Timer Used by SB When NB Normal Priority Request Arrived 0000: 0 VCLK 0001: 1*4 VCLK 0010: 2*4 VCLK 0011: 3*4 VCLK 0100: 4*4 VCLK ... 1000: 8*4 VCLK 1001: 16*4 VCLK 1010: 32*4 VCLK 1011: 64*4 VCLK 11--: SB holds the bus as long as there is pending upstream request	RSNTM [3:0]
3:0	RW	0100	V-Link Bus Timer Used by SB When NB High Priority Request Arrived 0000: 0 VCLK 0001: 1*2 VCLK 0010: 2*2 VCLK 0011: 3*2 VCLK 0100: 4*2 VCLK ... 1000: 8*2 VCLK 1001: 16*2 VCLK 1010: 32*2 VCLK 1011: 64*2 VCLK 11--: SB holds the bus as long as there is pending upstream request	RSHTM [3:0]

Table 11. SB V-Link Bus Timer Operation

RSNTM[3:0] (Rx4D[7:4])	RSHTM[3:0] (Rx4D[3:0])	NB Request Priority	SB When to Relinquish V-Link Bus
0000	xxxx	Normal / high	Immediately
0001,0010,...	0000	High	Immediately
0001,0010,...	0001,0010,...	High	Wait for either Normal or high timer expired
0001,0010,...	00xx	Normal	Wait for Normal timer expired
0001,0010,...	11xx	Normal / high	Wait for Normal timer expired
11xx	0000	High	Immediately
11xx	0000	Normal	Wait until there is no more pending upstream request
11xx	0001,0010,...	High	Wait for High timer expired
11xx	0001,0010,...	Normal	Wait until there is no more pending upstream request
11xx	11xx	Normal / high	Wait until there is no more pending upstream request

Offset Address: 4Eh (B0D17F7)
V-LINK Feature Control
Default Value: 00h

Bit	Attribute	Default	Description
7	RW	0	Downstream DAC Cycle Supported 0: Disable 1: Enable
6:1	—	0	Reserved
0	RW	0	Hand Shake V-Link Re-connection Scheme

Offset Address: 4Fh (B0D17F7)
SB V-Link Miscellaneous Control
Default Value: 00h

Bit	Attribute	Default	Description	Mnemonic
7	RW	0	Up Stream High Priority Command 0: Disable 1: Enable high priority up command	
6	RW	0	Enable PCI to PCI Bridge Header for External PCI Bus 0: Disable 1: Enable	
5	RW	0	Upstream High Priority Write Request 0: High Priority Write Request not supported 1: High Priority Write Request Enabled	RSVKHW
4	RW	0	Upstream High Priority Read Request 0: High Priority Read Request not supported 1: High Priority Read Request Enabled	RSVKHR
3	RW	0	Dynamic STOP on Up Strobe 0: Disable 1: Enable	
2	RW	0	Hide C2P Cycle for Internal Devices on PCI BUS When set to 1, only cycles that act with the external PCI devices will appear on the PCI Bus.	
1	RW	0	Support Extended Configuration Space Up to 4096 bytes	
0	RW	0	CPU to PCI Cycle Wait Till P2C Write Flushed (except C2P Post-Write) 0: Disable. CPU to PCI Read Ack (C2PRA) is not blocked. 1: Enable. C2PRA wait for SB PCI Bus (PCI1) P2C write FIFO empty.	RP2CFLSH

Offset Address: 50h (B0D17F7)
SB Peripheral Device's Bus Priority
Default Value: 00h

Bit	Attribute	Default	Description
7	RW	0	Enable SB Internal Device Arbitration Controller Two-Level Pipe Line Read
6	RW	0	NIC Priority 0: Low Priority 1: High Priority
5	RW	0	SATA Priority 0: Low Priority 1: High Priority
4	RW	0	USB Priority 0: Low Priority 1: High Priority
3	—	0	Reserved
2	RW	0	IDE Priority 0: Low Priority 1: High Priority
1	RW	0	AC97_ISA 0: Low Priority 1: High Priority
0	RW	0	PCI1 0: Low Priority 1: High Priority

Offset Address: 51h (B0D17F7)
P2P Bridge Related Control
Default Value: 00h

Bit	Attribute	Default	Description
7	RW	0	Enable Subtract Decode for P2P Cycle 0: Disable 1: Enable
6:4	—	0	Reserved
3	RW	0	D0F0 Rx4-7 Read as D17F7 Rx4-7 0: Disable 1: Enable
2	RW	0	PCI-to-PCI Bridge (D19F1) Rx9 Reads as 01h 0: Disable 1: Enable
1:0	—	0	Reserved

Offset Address: 52h (B0D17F7)
Miscellaneous Control
Default Value: 00h

Bit	Attribute	Default	Description
7	RW	0	Root Port 0 (BnD0F0) Rx3D Reads as 00h 0:Disable 1:Enable
6	RW	0	Root Port 1 (BnD0F1) Rx3D Reads as 00h 0:Disable 1:Enable
5:0	—	0	Reserved

DRAM Configuration (56-57h)
Offset Address: 56h (B0D17F7)
DRAM Ending for Bank 6
Default Value: 01h

Bit	Attribute	Default	Description
7:0	RW	01h	DRAM Bank 6 Ending Address (HA[31:24])

Offset Address: 57h (B0D17F7)
DRAM Ending for Bank 7
Default Value: 01h

Bit	Attribute	Default	Description
7:0	RW	01h	DRAM Bank 7 Ending Address (HA[31:24])

Interrupt Discovery and Configuration Capability Block (58-5Fh)
Offset Address: 58h (B0D17F7)
Capability ID
Default Value: 08h

Bit	Attribute	Default	Description
7:0	RO	08h	Capability ID

Offset Address: 59h (B0D17F7)
Next Pointer
Default Value: 00h

Bit	Attribute	Default	Description
7:0	RO	00h	Next Pointer. Null

Offset Address: 5Ah (B0D17F7)
Interrupt Register Index
Default Value: 01h

Bit	Attribute	Default	Description
7:0	RW	01h	Interrupt Register Index

Offset Address: 5Bh (B0D17F7)
Capability Type
Default Value: 80h

Bit	Attribute	Default	Description
7:0	RO	80h	Capability Type

Offset Address: 5F-5Ch (B0D17F7)
Interrupt Register Data Port
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:0	RO	00h	Interrupt Register Data Port

Shadow RAM Control (61-64h)
Offset Address: 61h (B0D17F7)
Page-C ROM Shadow Control
Default Value: 00h

Bit	Attribute	Default	Description
7:6	RW	00	CC000-CFFFFh Memory Space Access Control 00: Read / Write Disable 01: Write Enable 10: Read Enable 11: Read / Write Enable
5:4	RW	00	C8000-CBFFFh Memory Space Access Control
3:2	RW	00	C4000-C7FFFh Memory Space Access Control
1:0	RW	00	C0000-C3FFFh Memory Space Access Control

Offset Address: 62h (B0D17F7)
Page-D ROM Shadow Control
Default Value: 00h

Bit	Attribute	Default	Description
7:6	RW	00	DC000-DFFFFh Memory Space Access Control 00: Read / Write Disable 01: Write Enable 10: Read Enable 11: Read / Write Enable
5:4	RW	00	D8000-DBFFFh Memory Space Access Control
3:2	RW	00	D4000-D7FFFh Memory Space Access Control
1:0	RW	00	D0000-D3FFFh Memory Space Access Control

Offset Address: 63h (B0D17F7)
Page-E/F ROM, Memory Hole and SMI Decoding
Default Value: 00h

Bit	Attribute	Default	Description	Mnemonic
7:6	—	0	Reserved	
5:4	RW	00	F0000-FFFFFh Memory Space Access Control	
3:2	RW	00	Memory Hole 00: None 10: 15M – 16M (1M) 01: 512K – 640K 11: 14M – 16M (2M)	
1	RW	0	Disable Data Access on SMRAM (Page A, B) in SM mode 0: In SM mode, page A,B CPU Data R/W cycles are forwarded to the memory controller. 1: In SM mode, page A,B CPU Data R/W cycles are forwarded to the PCI bus Notes: 1. This bit is effective when Rx83[0] is set to 0. 2. SMRAM page A,B Code R/W cycles are always forwarded to the memory controller in SM mode.	RABKDOFF
0	RW	0	Enable Page A, B DRAM Access In Normal Mode 0: Page A, B CPU R/W cycles could be forwarded to memory controller or PCI bus depends on the setting of RABKDOFF (bit 1), the CPU operating mode (Normal or SM mode) as well as the type (Code or Data) of the CPU cycle. 1: Page A, B CPU R/W cycles (Code and Data) are always (in either Normal or SM mode) forwarded to the memory controller.	RRWABK

Offset Address: 64h (B0D17F7)
Page-E ROM Shadow Control
Default Value: 00h

Bit	Attribute	Default	Description
7:6	RW	00	EC000-EFFFFh Memory Space Access Control 00: Read / Write Disable 01: Write Enable 10: Read Enable 11: Read / Write Enable
5:4	RW	00	E8000-EBFFFh Memory Space Access Control
3:2	RW	00	E4000-E7FFFh Memory Space Access Control
1:0	RW	00	E0000-E3FFFh Memory Space Access Control

Host PCI Bridge Control (70-7Fh)
Offset Address: 70h (B0D17F7)
CPU to PCI Flow Control I
Default Value: 00h

Bit	Attribute	Default	Description
7	RW	0	CPU to PCI Post-Write 0: Disable C2P posted cycle could be delayed by PCI master cycles (i.e. PCI master access is allowed even if C2P buffer is not flushed). 1: Enable
6	RW	0	Back Off PCI Master PCI to CPU Read (P2CR) While Data not Return and PCI Time-Out PCI timer is at Rx75[2:0]
5:4	RW	0	PCI Master to DRAM Prefetch Control x0: Always prefetch x1: Disable prefetch
3	RW	0	PCI Short Latency for Read Back off PCI master once the read data not return.
2	RW	0	PCI to CPU Write Merge into 8QW for CCA
1	RW	0	Delay Transaction 0: Disable 1: Enable
0	RW	0	Cacheline Size 0: 4QW 1: 8QW

Offset Address: 71h (B0D17F7)
CPU to PCI Flow Control II
Default Value: 48h

Bit	Attribute	Default	Description
7	RW1C	0	Retry Status 0: No retry occurred 1: Retry occurred
6	RW	1	Action When Retry Timeout 0: Retry forever (record status only) 1: Flush buffer (write) or return 0xFFFFFFFFh (read)
5:4	RW	0	Retry Count and Retry Back off 00: Retry 2 times, back off CPU 10: Retry 4 times, back off CPU 01: Retry 16 times, back off CPU 11: Retry 64 times, back off CPU
3	RW	1	PCI Burst Timeout Enable 0: Disable 1: Enable
2	—	0	Reserved
1	RW	0	Compatible TYPE#1 Configuration Cycle AD31 0: Fix AD31 1: Support Type1 configuration cycle
0	—	0	Reserved

Offset Address: 72h (B0D17F7)
PCI P2C Read Caching and Prefetch Control
Default Value: 00h

Bit	Attribute	Default	Description
7	RW	0	No Arbitration on PCI Bus during PCI-DMA
6	RW	0	V-Link Downstream Command / Data 1T Faster 0: Decode V-Link down command after 1T sync. 1: Decode V-Link down command in 1T
5	RW	0	Conservative Read Caching Flush previous prefetched data when PCI master changes or starting address is not consecutive.
4	RW	0	P2C Write Merge for PCI1
3	RW	0	P2CR Residue Data Flushed by the Next P2CR FRAME 0: Prefetch data invalidate if FRAME de-assert without STOP 1: Prefetch data invalidate if C2P cycles
2	RW	0	PCI Master Read Prefetch Data Residual
1:0	RW	0	P2CR FIFO Prefetch Depth 00: Prefetch if outstanding read <= 1 line 01: Prefetch if outstanding read <= 2 line: RPF2LN 10: Prefetch if outstanding read <= 3 line: RPF3LN 11: Prefetch if outstanding read <= 5 line: RPF5LN

Offset Address: 73h (B0D17F7)
PCI Master Control
Default Value: 00h

Bit	Attribute	Default	Description
7	—	0	Reserved
6	RW	0	PCI Master 1-Wait State Write 0: 0WS 1: 1WS
5	RW	0	PCI Master 1-Wait State Read 0: 0WS 1: 1WS
4	RW	0	Disable Wait Flush Request (WFLUSHREQ) Blocking PCI to CPU Write (P2CW) Cycle
3	RW	0	PCI to CPU Read (P2CR) Caching Flush by NB SPCYC
2:1	—	0	Reserved
0	RW	0	PCI Master Broken Timer Enable 0: Disable 1: Enabled. Force into arbitration when there is no FRAME# 16 PCICLK after GNT

Offset Address: 74h (B0D17F7)
South Bridge V-Link Register
Default Value: 00h

Bit	Attribute	Default	Description
7	RW	0	Disable Dynamic CCA Clock Stop
6	RW	0	Disable Dynamic PCI Clock Stop (include VKCKG)
5	RW	0	Dynamic SVCTL Clock Stop
4	RW	0	LOCKCYC Flush P2C Cycles Before C2P
3	RW	0	LOCKCYC Block P2C Cycles
2	RW	0	APIC FSB Directly up to V-Link, not on PCI
1	RW	0	V-Link Pad Dynamic Turn Off IE Port
0	RW	0	V-Link P2C Write Data Queue Full Bug Fix

Offset Address: 75h (B0D17F7)
PCI Arbitration 1
Default Value: 00h

Bit	Attribute	Default	Description
7	RW	0	Arbitration Mode 0: REQ-based (arbitrate at end of REQ#) 1: Frame-based (arbitrate at FRAME# asserts)
6:4	RW	0	CPU Latency MLT2, MLT1, MLT0
3	RW	0	Disable PCI master time-out / Enable new grant mechanism
2:0	RW	000	PCI Master Bus Timeout 000: Disable 001: 1x16 PCLK 010: 2x16 PCLKs 011: 3x16 PCLKs 111: 7 x 16 PCLK

Offset Address: 76h (B0D17F7)
PCI Arbitration 2
Default Value: 00h

Bit	Attribute	Default	Description
7	RW	0	IO Port 22 Enable (SB) 0: CPU access to IO address 22 is passed on to the PCI bus 1: CPU access to IO address 22 is processed internally IO
6	RW	0	PCI Bus Parking at the Last PCI Master
5:4	RW	00	Master Priority Rotation Control 00: Disable 01: Grant to CPU after every PCI master grant 10: Grant to CPU after every 2 PCI master grant 11: Grant to CPU after every 3 PCI master grant
3:2	RW	0	Selected REQ as RQ4 00: REQ4 01: REQ0 10: REQ1 11: REQ2
1	—	0	Reserved
0	RW	0	Enable RQ4 as High Priority Master 0: Disable 1: Enable

Offset Address: 77h (B0D17F7)
PCI Traffic Control
Default Value: 00h

Bit	Attribute	Default	Description
7	—	0	Reserved
6	RW	0	C2PRA Blocked by PCI1 FIFO Empty Instead of PCI to CPU Write Ack (P2CWA) if Bit 6 = 1 C2PRA is blocked by P2CWA when RX4F[0] = 1. Note: it needs to work with Rx4F[0] ((RP2CFLSH)) assert.
5	RW	0	Put APIC Address Bit 2 to Bit 0 for Information Lost Due to QW-based Address.
4:3	RW	00	Read FIFO Timer 00: No timer 10: Timeout after 4ms 01: Timeout after 1ms 11: Timeout after 16ms
2	RW	0	GART Table 3.0, else 2.0 Format
1	RW	0	GART Table Enable for South Bridge
0	—	0	Reserved

Offset Address: 78h (B0D17F7)
PCI PAD Control
Default Value: 01h

Bit	Attribute	Default	Description
7	RW	0	Data Pad (AD, PAR) Driving Control
6	RW	0	Data Pad (AD, PAR) Slew Rate Control
5	RW	0	Strobe Pad (GNT) Driving Control
4	RW	0	Strobe Pad (GNT) Slew Rate Control
3:2	RW	0	Data in Delay
1	—	0	Reserved
0	RO	1	Bridge is V2X Capable Always reads 1

Offset Address: 79h (B0D17F7)
PCI V2X Data / Strobe Out Delay Control
Default Value: 00h

Bit	Attribute	Default	Description
7	RW	0	Data Out Change Based Clock 0: Data out changed by internal clock 1: Data out changed by external PCICLK
6:4	RW	0	Data Out Delay 000: No delay 010: Delay 1.3ns 100: Delay 3.1ns 110: Delay 4.4ns 001: Delay 0.7ns 011: Delay 2.0ns 101: Delay 3.8ns 111: Delay 5.1ns
3	RW	0	Strobe Out Source Clock 0: Strobe out from internal clock 1: Strobe out from external PCICLK
2:0	RW	0	Strobe Out Delay 000: No delay 010: Delay 1.3ns 100: Delay 3.1ns 110: Delay 4.4ns 001: Delay 0.7ns 011: Delay 2.0ns 101: Delay 3.8ns 111: Delay 5.1ns

Offset Address: 7Ah (B0D17F7)
PCI V2X Device Capability
Default Value: 00h

Bit	Attribute	Default	Description
7	RW	0	PREQ's Device is V2X Capability
6	RW	0	REQ6's Device is V2X Capability
5	RW	0	REQ5's Device is V2X Capability
4	RW	0	REQ4's Device is V2X Capability
3	RW	0	REQ3's Device is V2X Capability
2	RW	0	REQ2's Device is V2X Capability
1	RW	0	REQ1's Device is V2X Capability
0	RW	0	REQ0's Device is V2X Capability 0: No capability of V2X 1: With capability of V2X

Offset Address: 7Bh (B0D17F7)
REQ Status
Default Value: 00h

Bit	Attribute	Default	Description
7	RO	0	PREQ Status
6	RO	0	REQ6 Status
5	RO	0	REQ5 Status
4	RO	0	REQ4 Status
3	RO	0	REQ3 Status
2	RO	0	REQ2 Status
1	RO	0	REQ1 Status
0	RO	0	REQ0 Status 0: Inactive 1: Active

Offset Address: 7Ch (B0D17F7)
LDT Related Control
Default Value: 00h

Bit	Attribute	Default	Description
7	—	0	Reserved
6	RW	0	Enable Warm Reset When Host Bus Error Occurs 0: V3_HOST_SERR not result to warm reset 1: V3_HOST_SERR result to warm reset. Allow system back from LDT sync flood error.
5	RW	0	Enable Clear CFGCS for Each Configuration Cycle 0: CFC IO cycle not clears CFGCS 1: CFC IO cycle always clears CFGCS. Allow CPU issue CF8/CFC IO cycles without confused with configuration cycles.
4	RW	0	Enable LDT STPGNT Block C2P Response 0: C2P response not blocked by STPCLK/SMI message 1: C2P response blocked by STPCLK/SMI message. Avoid CPU from execution the next instruction when entering suspend mode or system management mode.
3	RW	0	Enable LDT APIC Mode 0: Cfg of 59~5F not remapping to I/O APIC cycle 1: Cfg of 59~5F mapping to I/O APIC cycle
2	RW	0	Enable NMI / SMI / INIT for FSB 0: NMI / SMI / INIT to CPU through external pins 1: NMI / SMI / INIT to CPU through front side bus delivery
1	RW	0	Enable Upstream Message 0: STPCLK/A20G/IGNNE to CPU through external pins 1: STPCLK/A20G/IGNNE to CPU through up message
0	RW	0	Enable LDT Mode 0: FERR from external pin. 1: FERR from downstream message

Offset Address: 7Eh (B0D17F7)
Virtual Channel 0 Arbitration Promoting Timer
Default Value: 00h

Bit	Attribute	Default	Description
7:5	RW	0	Normal Priority REQ Promote Timer 000: Disable 010: 240ns ... 001: 120ns 011: 360ns 111: 840ns
4:0	—	0	Reserved

Offset Address: 7Fh (B0D17F7)
Virtual Channel 1 Arbitration Promoting Timer
Default Value: 00h

Bit	Attribute	Default	Description
7:5	RW	0	High Priority REQ Promote Timer 000: Disable 010: 240ns ... 001: 120ns 011: 360ns 111: 840ns
4:0	—	0	Reserved

GART Operation (80-95h)
Offset Address: 83-80h (B0D17F7)
Graphic Aperture Base Configuration
Default Value: 0000 0008h

Bit	Attribute	Default	Description
31:28	RW	0	Upper Programmable Base Address
27:20	RW	0	Lower Programmable Base Address The aperture base address bit acts as if hardwired to 0 if Rx84[7:0] (GTSZ[27:20]) is 0.
19:0	RO	0008h	Reserved. Do not program. Indicate that Graphic Aperture range alignment in 1M Bytes. Bit 3 indicates that Graphic Aperture range is pre-fetchable.

Table 12. Graphics Aperture Base Address Table

Graphics Aperture Base Rx80[27:20]	27	26	25	24	23	22	21	20	
Graphics Aperture Size Rx84[7:0]	7	6	5	4	3	2	1	0	Graphics Aperture Size
	RW	1M							
	RW	0	2M						
	RW	RW	RW	RW	RW	RW	0	0	4M
	RW	RW	RW	RW	RW	0	0	0	8M
	RW	RW	RW	RW	0	0	0	0	16M
	RW	RW	RW	0	0	0	0	0	32M
	RW	RW	0	0	0	0	0	0	64M
	RW	0	0	0	0	0	0	0	128M
	0	0	0	0	0	0	0	0	256G

Note: This range is defined prefetchable.

Offset Address: 84h (B0D17F7)
Graphic Aperture Size
Default Value: 00h

Bit	Attribute	Default	Description
7:0	RW	0	Graphic Aperture Size 11111111: 1M 11111100: 4M 11110000: 16M 11000000: 64M 00000000: 256M

Offset Address: 8B-88h (B0D17F7)
Graphic Aperture Translation Look-Aside Table Base Address
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:12	RW	0	Pointer to the Base of the Translation Table Used to Map Addresses in Aperture Range
11:2	—	0	Reserved
1	RW	0	Enable Graphic Aperture Address A[31:28]
0	—	0	Reserved

Offset Address: 95-94h (B0D17F7)
Graphic Aperture Size for AGP3.0
Default Value: 0000h

Bit	Attribute	Default	Description
15:12	—	0	Reserved
11:0	RW	0	Graphic Aperture Size for AGP3.0 111100111111: 4M 111100111100: 16M 111100110000: 64M 111100000000: 256M 110000000000: 1G 000000000000: 4G
			111100111110: 8M 111100111000: 32M 111100100000: 128M 111000000000: 512M 100000000000: 2G <= Max

V-Link 8X Compensation Circuit (B7-BDh)
Offset Address: B7h (B0D17F7)
VCKKG Output Duty Cycle Setting
Default Value: 00h

Bit	Attribute	Default	Description
7	RW	0	SB V-Link Output Strobe Rise Time Control [1]
6	RW	0	SB V-Link Output Strobe Rise Time Control [0]
5	RW	0	SB V-Link Output Strobe Fall Time Control [1]
4	RW	0	SB V-Link Output Strobe Fall Time Control [0]
3	RW	0	SB V-Link Output R-port Rise Time Control [1]
2	RW	0	SB V-Link Output R-port Rise Time Control [0]
1	RW	0	SB V-Link Output R-port Fall Time Control [1]
0	RW	0	SB V-Link Output R-port Fall Time Control [0]

Offset Address: B8h (B0D17F7)
SB V-Link Compensation Control
Default Value: 00h

Bit	Attribute	Default	Description
7:5	RO	0	V-Link Auto-Compensation PMOS Output Value
4	—	0	Reserved
3:1	RO	0	V-Link Auto-Compensation NMOS Output Value
0	—	0	Reserved

Offset Address: B9h (B0D17F7)
SB V-Link Manual Driving Control - Strobe
Default Value: 00h

Bit	Attribute	Default	Description
7:5	RW	0	Manual Setting - SB V-Link Strobe Pullup (PMOS)
4	—	0	Reserved
3:1	RW	0	Manual Setting - SB V-Link Strobe Pulldown (NMOS)
0	—	0	Reserved

Offset Address: BAh (B0D17F7)
SB V-Link Manual Driving Control - Data
Default Value: 00h

Bit	Attribute	Default	Description
7:5	RW	0	Manual Setting - SB V-Link Data Pullup (PMOS)
4	—	0	Reserved
3:1	RW	0	Manual Setting - SB V-Link Data Pulldown (NMOS)
0	—	0	Reserved

Offset Address: BBh (B0D17F7)
V-Link PAD Related Register
Default Value: 00h

Bit	Attribute	Default	Description	Mnemonic
7	RW	0	Compensation Selection 0: Auto compensation (values in RxB8[7:5]) 1: Manual setting (use the values in RxB9-BA)	
6	RW	0	SB V-Link Output Data Rising Time Control [1]	
5	RW	0	SB V-Link Output Data Rising Time Control [0]	
4	RW	0	SB V-Link Output Data Falling Time Control [1]	
3	RW	0	SB V-Link Output Data Falling Time Control [0]	
2	RW	0	SB V-Link Input Reference Voltage Select in 4X If Bit 2 (VREF4XSEL) = 1, VREF4X=0.9V If Bit 2 (VREF4XSEL) = 0, VREF4X=0.75V	VREF4XSEL
1:0	RW	0	SB V-Link VKCKG Delay Control RSVKDS[1:0] Input strobe (DNSTB) delay 00: 0.3ns 01: 0.4ns 10: 0.5ns 11: 0.6ns	RSVKDS[1:0]

Offset Address: BCh (B0D17F7)
V-Link Auto Compensation Termination Resistor Status
Default Value: 00h

Bit	Attribute	Default	Description
7	RO	0	N Resistor Check Flag for the SB Termination Resistor 0: Abnormal condition occurred 1: Normal operation
6	RO	0	P Resistor Check Flag for the SB Termination Resistor 0: Abnormal condition occurred 1: Normal operation
5	RO	0	N Pull Down Driving Check Flag for the SB Termination Resistor 0: Abnormal condition occurred 1: Normal operation.
4	RO	0	P Pull Down Driving Check Flag for the SB Termination Resistor 0: Abnormal condition occurred 1: Normal operation.
3	—	0	Reserved
2:0	RO	0	SB V-Link Autocomp Termination Resistor Value 000: Largest Resistor ... 111: Smallest Resistor

Offset Address: BDh (B0D17F7)
V-Link Manual Termination Resistor Value
Default Value: 00h

Bit	Attribute	Default	Description
7:3	—	0	Reserved
2:0	RW	000	V-Link Manual Termination Resistor Value 000: Largest Resistor ... 111: Smallest Resistor

DRAM Above 4G Support (E4-E6h)
Offset Address: E4h (B0D17F7)
Low Top Address - Low
Default Value: 00h

Bit	Attribute	Default	Description																		
7:4	RW	0	Low Top Address - Low																		
3:0	RW	0	DRAM Granularity - (Powell) <table> <thead> <tr> <th>Total DRAM RMEMUNIT</th> <th>less than</th> <th>Granularity</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>4G</td> <td>16M</td> </tr> <tr> <td>1</td> <td>8G</td> <td>32M</td> </tr> <tr> <td>2</td> <td>16G</td> <td>64M</td> </tr> <tr> <td>3</td> <td>32G</td> <td>128M</td> </tr> <tr> <td>4</td> <td>64G</td> <td>256M</td> </tr> </tbody> </table> RANK Ending Address Formula: $\text{ENDxA}[35:24] = \text{RENDxA} \ll \text{RMEMUNIT}; (\text{x} = 0,1,2,3,4,5,6,7)$	Total DRAM RMEMUNIT	less than	Granularity	0	4G	16M	1	8G	32M	2	16G	64M	3	32G	128M	4	64G	256M
Total DRAM RMEMUNIT	less than	Granularity																			
0	4G	16M																			
1	8G	32M																			
2	16G	64M																			
3	32G	128M																			
4	64G	256M																			

Offset Address: E5h (B0D17F7)
Low Top Address - High
Default Value: 00h

Bit	Attribute	Default	Description	Mnemonic
7:0	RW	00h	Low Top Address – High	RLOWTOPA [31:24]

Offset Address: E6h (B0D17F7)
SMM and APIC Decoding
Default Value: 01h

Bit	Attribute	Default	Description	Mnemonic
7:5	—	0	Reserved	
4	RW	0	IO APIC Decoding 0: Cycles accessing FECx xxxx are passed to PCI1 1: Cycles accessing FEC7_FFFF - FEC0_0000 are passed to PCI1. Cycles accessing to FECF_FFFF - FEC8_0000 are passed to PCI2.	
3	RW	0	MSI Support (Processor Message Enable) 0: Cycles accessing FEEx xxxx from masters are passed to PCI1 (PCIC will not claim) 1: Cycles accessing FEEx xxxx from masters are passed to the Host side for snooping	
2	RW	0	Top SMM Enable 0: Disable 1: Enable	RTSMMEN
1	RW	0	High SMM Enable	
0	RW	1	Compatible SMM Enable 0: Disable 1: Enable	

Bus 0 Device 18 Function 0 (B0D18F0): LAN Controller

All registers are located in the Device 18 Function 0 PCI configuration space of the VT8251. These registers are accessed through PCI configuration mechanism #1 via I/O address CF8 / CFC.

PCI Configuration Space Header Registers (0-3Dh)

Offset Address	Attribute	Default	Description
1 – 0h	RO	1106h	Vendor ID
3 – 2h	RO	3065h	Device ID
5 – 4h	RW	00h	Command
7 – 6h	RO	0400h	Status
8h	RO	7Ch	Revision ID
9h	RO	00h	Program Interface
0Ah	RO	00h	Sub Class Code
0Bh	RO	00h	Class Code
0Ch	RW	00h	Cache Line Size
0Dh	RW	00h	Latency Timer
0Eh	RO	00h	Header Type
0Fh	RO	00h	BIST
13 – 10h	RW	0000 0000h	I/O Base Address
17 – 14h	RW	0000 0000h	Memory Base Address
2B – 28h	RW	0000 0000h	Card Bus CIS Pointer
33 – 30h	RW	0000 0000h	Expansion ROM Base
34h	RO	40h	Capabilities Offset
3Ch	RW	00h	Interrupt Line
3Dh	RO	01h	Interrupt Pin

Offset Address: 5-4h (B0D18F0)

Command

Default Value: 0000h

Bit	Attribute	Default	Description
15:11	—	00h	Reserved. Always reads 0
10	RW	0	Interrupt Disable
9:3	—	00h	Reserved. Always reads 0
2	RW	0	Bus Master Always reads 0
1	RW	0	Memory Space Always reads 0
0	RW	0	I/O Space

Offset Address: 7-6h (B0D18F0)

Status

Default Value: 0410h

Bit	Attribute	Default	Description
15	RO	0	Detected Parity Error Always reads 0
14	RO	0	Signalled System Error Always reads 0
13	RO	0	Received Master Abort Always reads 0
12	RO	0	Received Target Abort Always reads 0
11	RO	0	Signalled Target Abort Always reads 0
10:9	RO	10	DEVSEL# Timing Fixed at 10 (slow)
8	RO	0	Data Parity Detected
7	RO	0	Fast Back-to-Back Capable
6	RO	0	Reserved
5	RO	0	66 MHz Capable
4	RO	1	Capabilities (e.g. PCI Power Management)
3	RO	0	Interrupt Status
2:0	—	0	Reserved

Offset Address: 0Ch (B0D18F0)
Cache Line Size

This register must be implemented by master devices that can generate the memory-write-and-invalidate command.

Offset Address: 0Dh (B0D18F0)
Latency Timer

This register must be implemented as writable by any master that can burst more than two data phases.

Offset Address: 34h (B0D18F0)
Capabilities Offset
Default Value: 40h

Bit	Attribute	Default	Description
7:0	RO	0	Capabilities Offset Offset into the LAN function PCI space pointing to the location of the first item in the function's capability list.

Offset Address: 3Ch (B0D18F0)
Interrupt Line
Default Value: 00h

Bit	Attribute	Default	Description
7:4	—	00h	Reserved Always reads 0
3:0	RW	0000	LAN Interrupt Routing 0000: Disabled 0010: Reserved 0100: IRQ4 0110: IRQ6 1000: IRQ8 1010: IRQ10 1100: IRQ12 1110: IRQ14 APIC (See Device 17 Function 0 Rx58[6]) x000: IRQ16 x010: IRQ18

Offset Address: 3Dh (B0D18F0)
Interrupt Pin
Default Value: 01h

Bit	Attribute	Default	Description
7:0	RO	01h	Interrupt Routing Mode 00h: Legacy mode interrupt routing 01h: Native mode interrupt routing

LAN-Specific PCI Configuration Registers (40-50h)
Offset Address: 40h (B0D18F0)
Capability ID
Default Value: 01h

Bit	Attribute	Default	Description
7:0	RO	01h	Capability ID Identifies the linked list item as being PCI power management registers Always reads 01h

Offset Address: 41h (B0D18F0)
Next Item Pointer
Default Value: 00h

Bit	Attribute	Default	Description
7:0	RO	00h	Next Item Pointer Always reads 00h Offset into the LAN function PCI space pointing to the location of the next item in the function's capability list.

Offset Address: 43-42h (B0D18F0)
Power Management Configuration
Default Value: 3C02h

Bit	Attribute	Default	Description
15:11	RO	11110	Power State In Which LAN Can Assert PME# 1xxxx: PME# can be asserted from D3C x1xxx: PME# can be asserted from D3H xx1xx: PME# can be asserted from D2 xxx1x: PME# can be asserted from D1 xxxx1: PME# can be asserted from D0
10	RO	0	D2 PM State 0: Not Supported 1: Supported
9	RO	0	D1 PM State 0: Not Supported 1: Supported
8:6	RO	0	PCI 3.3V Auxiliary Current Requirements Always reads 0
5	RO	0	Device-Specific Initialization Always reads 0
4	—	0	Reserved
3	RO	0	PME# Operation Uses PCI Clock 0: No PCI clock req'd for PME# generation 1: PME# generated using PCI clock
2:0	RO	010	Power Management Interface Revision Readback of 010b indicates compliance with revision 1.1 of the power management interface specification

Offset Address: 47-44h (B0D18F0)
Power Management Control / Status
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:0	RWC	0000 0000h	Control / Status (See Power Management Specification 1.0)

Offset Address: 50h (B0D18F0)
Mode 0
Default Value: 00h

Bit	Attribute	Default	Description
7:4	—	0	Reserved. Do not program.
3	RW	0	PHY Power Down 0: No PHY power down generation 1: Software force PHY power down
2:0	—	0	Reserved. Do not program.

LAN I/O Registers (0-FFh)
Offset Address: 5-0h (B0D18F0)
Ethernet Address

Unless the EEPROM is disabled, the Ethernet Address is loaded to this register from the EEPROM every time the system starts up.

Offset Address: 6h (B0D18F0)
Receive Control
Default Value: 00h

Bit	Attribute	Default	Description
7:5	RW	00h	Reserved Do not program
4	RW	0	Physical Address Packets Accepted 0: Packets with a physical destination address are not accepted 1: All packets with a physical destination address are accepted
3	RW	0	Broadcast Packets Accepted 0: Broadcast packets are rejected 1: Broadcast packets are accepted
2	RW	0	Multicast Packets Accepted 0: Multicast packets are rejected 1: Multicast packets are accepted
1	RW	0	Small Packets Accepted 0: Packets smaller than 64 bytes are rejected 1: Packets smaller than 64 bytes are accepted
0	RW	0	Error Packets Accepted 0: Packets with receive errors are rejected 1: Packets with receive errors are accepted

Offset Address: 7h (B0D18F0)
Transmit Control
Default Value: 00h

Bit	Attribute	Default	Description
7:3	—	00h	Reserved
2:1	RW	00	Transmit Loopback Mode 00: Normal 01: Internal loopback (signal is looped back to the host from the MAC) 10: MII loopback (signal is looped back to the host from the PHY) 11: reserved- (do not program)
0	—	0	Reserved

Offset Address: 8h (B0D18F0)
Command 1
Default Value: 00h

Bit	Attribute	Default	Description
7	—	0	Reserved
6	RW	0	Receive Poll Demand If this bit is set to 1, the Receive Descriptor (RD) will be polled once (this bit will be cleared by hardware after the polling is complete)
5	RW	0	Transmit Poll Demand If this bit is set to 1, the Transmit Descriptor (TD) will be polled once (this bit will be cleared by hardware after the polling is complete)
4	RW	0	Transmit Process 0: Transmit engine disabled 1: Transmit engine enabled (transmit may occur)
3	RW	0	Receive Process 0: Receive disabled 1: Receive enabled
2	RW	0	Stop NIC 0: NIC enabled 1: NIC disabled (transmit/receive cannot occur)
1	RW	0	Start NIC 0: No command entered 1: Start the NIC
0	—	0h	Reserved Do not program

Offset Address: 9h (B0D18F0)
Command 2
Default Value: 08h

Bit	Attribute	Default	Description
7	RW	0	Software Reset 0: No reset 1: Reset the MAC
6	RW	0	Receive Poll Demand 2 This bit functions the same as Rx8[6]. The function can be enabled by setting either bit (for backward compatibility).
5	RW	0	Transmit Poll Demand 2 This bit functions the same as Rx8[5]. The function can be enabled by setting either bit (for backward compatibility).
4	—	0	Reserved
3	RW	1	TD / RD Auto Polling 0: Enable (polling interval is determined by Rx6F[2:0]) 1: Disable
2	RW	0	Full Duplex 0: Set MAC to half duplex mode 1: Set MAC to full duplex mode
1:0	—	00	Reserved (Do not program)

Offset Address: 0Ch (B0D18F0)
Interrupt Status 1
Default Value: 00h

Bit	Attribute	Default	Description
7	RW	0	CRC or Miss Packet Tally Counter Overflow Set if either counter overflows (both counters are 16 bits)
6	RW	0	PCI Bus Error Set if PCI bus error occurred.
5	RW	0	Receive Buffer Link Error Set when there is not enough buffer space for a packet requiring multiple buffers.
4	—	00	Reserved (Do not program)
3	RW	0	Transmit Error (Packet Transmit Aborted) Set due to excessive collisions (more than 16), transmit underflow, or transmit data linking error
2	RW	0	Receive Error Set due to CRC error, frame alignment error, FIFO overflow, or received data linking error
1	RW	0	Packet Transmitted Successfully
0	RW	0	Packet Received Successfully

Offset Address: 0Dh (B0D18F0)
Interrupt Status 2
Default Value: 00h

Bit	Attribute	Default	Description
7	RW	0	General Purpose Interrupt This bit is set when there is a general purpose interrupt event (Rx84). This bit is set when any bit in Rx84 equals one and when its corresponding mask bit in Rx86 also equals one.
6	RW	0	Port State Change (PHY)
5	RW	0	Transmit Abort Due to Excessive Collisions Set when there is a transmit error that is due to excessive collisions. Alternatively, Rx0C[3] is set for all transmit errors.
4	—	0	Receive Buffer Full Set when there is no more buffer space available in system memory.
3	RW	0	Receive Packet Race Set when there is not enough room in the FIFO to receive an additional packet.
2	RW	0	Receive FIFO Overflow
1:0	—	00	Reserved

Offset Address: 0Eh (B0D18F0)
Interrupt Mask 1
Default Value: 00h

Bits correspond to the bits in Interrupt Status Register 1. An interrupt is generated when corresponding bits in both registers equal 1.

Bit	Attribute	Default	Description
7:0	RW	0	Interrupt Mask 1

Offset Address: 0Fh (B0D18F0)
Interrupt Mask 2
Default Value: 00h

Bits correspond to the bits in Interrupt Status Register 2. An interrupt is generated when corresponding bits in both registers equal 1.

Bit	Attribute	Default	Description
7:0	RW	0	Interrupt Mask 2

Offset Address: 17-10h (B0D18F0)
Multicast Address
Default Value: 0000 0000 0000 0000h

The value in this register determines which Multicast addresses are received.

Bit	Attribute	Default	Description
63:0	RW	0	Multicast Address

Offset Address: 1B-18h (B0D18F0)
RX Address
Default Value: 0000 0000h

This register reports the transmit transcriptor address that is being accessed.

Bit	Attribute	Default	Description
31:0	RW	0	RX Address

Offset Address: 1F-1Ch (B0D18F0)
TX Address
Default Value: 0000 0000h

This register reports the transmit transcriptor address that is being accessed.

Bit	Attribute	Default	Description
31:0	RW	0	TX Address

Offset Address: 23-20h (B0D18F0)
Receive Status
Default Value: 0000 0400h

Bit	Attribute	Default	Description
31	RW	0	Descriptor Owner 0: Descriptor Owned By Host (NIC cannot access descriptor) 1: Descriptor Owned by NIC (NIC can access descriptor) Note: This bit has no default so must be set by the driver at initialization.
30:27	—	0	Reserved
26:16	RO	0	Received. Packet Length
15	RO	0	Received. Packet Successfully
14	—	0	Reserved
13	RO	0	NIC Accepted Multicast Packet
12	RO	0	NIC Accepted Broadcast Packet
11	RO	0	NIC Accepted Physical Address Packet
10	RO	1	Chain Buffer Set if packet too large to occupy a single receive descriptor.
9:8	RO	0	Buffer Descriptor Start / End For packets too large to fit into a single receive descriptor and thus occupy multiple RD's, this field reports whether this RD is the start, middle or end. 00: Chain Buffer Middle Descriptor 01: Chain Buffer End Descriptor 10: Chain Buffer Start Descriptor 11: Single Buffer Descriptor (packet occupies only one descriptor)
7	—	0	Reserved
6	RO	0	System Error
5	RO	0	Runt Packet (< 64 bytes)
4	RO	0	Long Packet (> 2500 bytes)
3	RO	0	FIFO Overflow Error
2	RO	0	Frame Alignment Error
1	RO	0	CRC Error
0	RO	0	Receiver Error

Offset Address: 27-24h (B0D18F0)
Rx Data Buffer Control
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:11	—	0	Reserved
10:0	RO	0	Rx Data Buffer Size The receive data buffer size for this descriptor. The total byte count of the entire frame will be stored in the last descriptor.

Offset Address: 2B-28h (B0D18F0)
Rx Data Buffer Start Address
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:0	RO	00h	Rx Data Buffer Start Address

Offset Address: 2F-2Ch (B0D18F0)
Rx Data Buffer Branch Address
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:0	RO	00h	Rx Data Buffer Branch Address

Note: Rx20-2F reflect values from the RD being accessed.

Offset Address: 43-40h (B0D18F0)
Transmit Status
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31	RW	0	Descriptor Owner 0: Descriptor Owned By Host (NIC cannot access descriptor) 1: Descriptor Owned by NIC (NIC can access descriptor) This bit has no default so must be set by the driver at initialization.
30:16	—	0	Reserved
15	RO	0	Transmit Error 0: Transmit Successful 1: Excessive Collisions During Transmit Attempt
14	—	0	Reserved
13	RO	0	System Error
12	RO	0	Invalid TD Format or Structure or TD Overflow
11	RO	0	Reserved
10	RO	0	Carrier Sense Lost During Transmit
9	RO	0	Out of Window Collision (collision outside initial 64 bytes)
8	RO	0	Transmit Abort (Excessive Collisions)
7	RO	0	CD Heartbeat Issued (10BaseT Only)
6:5	—	0	Reserved
4	RO	0	Collision Detected During Transmit
3:0	RO	0	Collision Retry Count

Offset Address: 47-44h (B0D18F0)
Tx Data Buffer Control
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:24	—	0	Reserved
23	RO	0	Send-Complete Interrupt 0: Interrupt not generated 1: Interrupt generated after send complete
22	RO	0	End of Transmit Packet For packets too large to fit into a single transmit descriptor and thus occupy multiple TD's, this bit reports whether this TD is the End TD. 0: This TD is not the End TD 1: This TD is the End TD
21	RO	0	Start of Transmit Packet For packets too large to fit into a single transmit descriptor and thus occupy multiple TD's, this bit reports whether this TD is the Start TD. 0: This TD is not the Start TD 1: This TD is the Start TD
20:17	—	0	Reserved
16	RO	0	Disable CRC Generation
15	RO	0	Chain Buffer
14:11	—	0	Reserved
10:0	RO	0	Tx Data Buffer Size The transmit data buffer size for this descriptor. The total byte count of the entire frame will be stored in the last descriptor

Offset Address: 4B-48h (B0D18F0)
Tx Data Buffer Start Address
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:0	RO	0	Tx Data Buffer Start Address

Offset Address: 4F-4Ch (B0D18F0)
Tx Data Buffer Branch Address
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:4	RO	0	Tx Data Buffer Branch Address
3:1	—	0	Reserved
0	RO	0	Tx Interrupt Enable 0: Issue interrupt for this packet 1: No interrupt generated

Offset Address: 6Ch (B0D18F0)
PHY Address
Default Value: 01h

Bit	Attribute	Default	Description
7:6	RW	00	MII Management Polling Timer Interval (Polling PHY) 00: 1024 MDC Clock Cycles 01: 512 MDC Clock Cycles 10: 128 MDC Clock Cycles 11: 64 MDC Clock Cycles MDC is an internal clock with a 960 ns cycle time.
5	RW	0	Accelerate MDC Speed 0: Normal 1: 4x Accelerated
4:0	RW	01h	Extended PHY Device Address Stored from EEPROM during power-up or EEPROM auto-reload but can be programmed by software

Offset Address: 6Dh (B0D18F0)
MII Status
Default Value: 13h

Bit	Attribute	Default	Description
7	RW	0	PHY Reset 0: PHY reset not asserted 1: PHY reset asserted
6:5	—	0	Reserved
4	RW	1	PHY Option 0: PHY address updated from EEPROM 1: Use default PHY address of 0001h
3	RW	0	PHY Device Received Error 0: No MII error 1: MII Error
2	—	0	Reserved
1	RW	1	Link Failure 0: Link successful 1: Link unsuccessful (no connection)
0	RW	1	PHY Speed 0: 100 Mb 1: 10 Mb

Offset Address: 6Eh (B0D18F0)
Buffer Control 1
Default Value: 00h

Bit	Attribute	Default	Description				
7:3	—	0	Reserved	Always reads 0			
2:0	RW	000	DMA Length	000:32 bytes	8 DW	001:64 bytes	16 DW
				010:128 bytes	32 DW	011:256 bytes	64 DW
				100:512 bytes	128 DW	101:1024 bytes	256 DW
				11x:Store & Forward			

Offset Address: 6Fh (B0D18F0)
Buffer Control 2
Default Value: 00h

Bit	Attribute	Default	Description			
7:3	—	0	Reserved			
2:0	RW	000	Polling Interval Timer	This field determines the polling interval when TX / RX Auto-Polling is enabled (LAN I/O Rx09[3]=0).	000: 2 ¹³ V-Link Clocks	001: 2 ¹⁵ V-Link Clocks
				001: V-Link Clocks	001: 2 ¹² V-Link Clocks	001: 2 ¹⁰ V-Link Clocks
				001: 2 ¹¹ V-Link Clocks	001: 2 ⁹ V-Link Clocks	001: 2 ⁸ V-Link Clocks

Offset Address: 70h (B0D18F0)
MII Management Port Command
Default Value: 00h

Bit	Attribute	Default	Description	
7	RW	0	MII (PHY) Auto Polling	0: Disable 1: Enable (polling interval determined by Rx6C[7:6])
6	RW	0	PHY Read	Every time this bit is set to one, the PHY is read once. The address read is determined by Rx71[4:0] and the data is stored in Rx73-72. 0: Disable 1: Enable
5	RW	0	PHY Write	Every time this bit is set to one, the PHY is written once. The address written is determined by Rx71[4:0] and the value in Rx73-72 will be written to the PHY. 0: Disable 1: Enable
4	RW	0	PHY Direct Programming Mode	0: Disable (bits 3-0 are ignored, see bits 6-5) 1: Enable (bits 6-5 are ignored, see bits 2-0)
3	RW	0	MDIO Output Enable Indicator	
2	RW	0	PHY Direct Programming Write Data Out	During direct programming (write), the value in this bit is written to the PHY every time bit-0 of this register (the “clock”) toggles.
1	RO	0	PHY Direct Programming Read Data In	During direct programming (read), every time the “clock” (bit-0) toggles, the value from the PHY is stored in this bit.
0	RW	0	PHY Direct Programming Clock	This bit acts as the clock during direct reads from and direct writes to the PHY.

Offset Address: 71h (B0D18F0)
MII Management Port Address
Default Value: 81h

Bit	Attribute	Default	Description
7	RW	1	Polling Status 0: Polling mechanism is busy (polling can't be initiated) 1: Polling mechanism is idle (polling can be initiated)
6	—	0	Polling Type 0: Poll One Cycle 1: Auto polling – close the pause function at bit-5
5	RW	0	Polling Complete 0: Polling not complete 1: Polling complete (auto polling data ready)
4:0	RW	01h	MII Management Port Address Bits 4-0 This field contains the address of the PHY register to be read or written.

Offset Address: 73-72h (B0D18F0)
MII Management Port Data
Default Value: 0000h

After a PHY read, the data read from the PHY is stored in this register. For writes to the PHY, the data to be written is placed in this register.

Bit	Attribute	Default	Description
15:0	RW	00h	MII Management Port Data

Offset Address: 74h (B0D18F0)
EEPROM Command / Status
Default Value: 00h

Bit	Attribute	Default	Description
7	RO	0	EEPROM Program Complete Set when EEPROM loading is complete.
6	RW	0	EEPROM Embedded Program Enable When this bit is set, configuration data (in Rx6E, 6F, 74, 78, 79, 7A, and 7B) will start to be programmed into the EEPROM.
5	RW	0	Dynamically Reload EEPROM Content When this bit toggles, the Ethernet ID (Rx5-0) is reloaded from EEPROM.
4	RW	0	EEPROM Direct Program Mode 0: Disable 1: Enable
3	RW	0	EEPROM Direct Programming Chip Select This bit must be set to allow programming of the EEPROM using bits 2-0
2	RW	0	EEPROM Direct Programming Clock This bit acts as the clock for direct programming of the EEPROM.
1	RW	0	EEPROM Direct Programming Write Data During direct programming (write), the value in this bit is presented to the EEPROM Data In pin and written to the EEPROM every time bit-2 of this register (the “clock”) toggles.
0	RO	0	EEPROM Direct Programming Read Data During direct programming (read), every time bit-2 of this register (the “clock”) toggles, the value on the EEPROM Data Out pin is stored in this bit.

Offset Address: 78h (B0D18F0)
EEPROM Control
Default Value: 00h

Bit	Attribute	Default	Description
7	RW	1	EEPROM Embedded & Direct Programming 0: Disable (EEPROM cannot be programmed) 1: Enable (allow EEPROM to be programmed)
6	RW	0	Extension Clock 0: Disable 1: Enable (the clock to the EEPROM is sent prior to the start of data to allow more time for the EEPROM to return to the ready state)
5:0	—	0	Reserved

Offset Address: 79h (B0D18F0)
Configuration 1
Default Value: 00h

Bit	Attribute	Default	Description
7	RW	0	Transmit Frame Queueing 0: Enable (frames from the PCI bus can be queued in the transmit FIFO – a maximum of 2 packets may be queued) 1: Disable
6	RW	0	Data Parity Generation and Checking This bit controls whether PCI parity is enabled. 0: Disable 1: Enable
5	RW	0	Memory-Read-Line Supported This bit controls whether PCI Memory-Read-Line is supported. 0: Disable 1: Enable
4	RW	0	Transmit FIFO DMA Interleaved to Receiving FIFO DMA After 32 DW Transaction This bit controls whether during a transmit, priority can be given to a receive transaction. 0: Disable 1: Enable (during a transmit, if a receive request is seen, the transmit is paused after 32 DW's and priority is given to the receive)
3	RW	0	Receive FIFO DMA Interleaved to Transmitting FIFO DMA After 32 DW Transaction This bit controls whether during a receive, priority can be given to a transmit transaction. 0: Disable 1: Enable (during a receive, if a transmit request is seen, the receive is paused after 32 DW's and priority is given to the transmit)
2	RW	0	Memory Read Wait States (for ISA only) 0: None 1: Insert one wait state 2222
1	RW	0	Memory Write Wait States (for ISA only) 0: None 1: Insert one wait state 2222
0	RW	0	Latency Timer This bit controls whether PCI Delayed Transactions are enabled. 0: Disable 1: Enable

Offset Address: 7Ah (B0D18F0)
Configuration 2
Default Value: 00h

Bit	Attribute	Default	Description
7	—	0	Reserved. Always reads 0
6	RW	0	Unused BootROM Address MA This bit controls whether unused BootROM memory address bits are tied high. 0: Not tied high 1: Tied high
5	RW	0	Delayed Transactions for BootROM Memory Read This bit controls whether PCI delayed transactions are enabled. 0: Disable 1: Enable
4:0	—	0	Reserved. Always reads 0

Offset Address: 7Bh (B0D18F0)
Configuration 3
Default Value: 00h

Bit	Attribute	Default	Description
7	RW	0	Memory Mapped I/O Access 0: Disable 1: Enable
6:4	—	0	Reserved. Do not program.
3	RW	0	Backoff Algorithm 0: Fixed 1: Random
2:1	—	00	Reserved. Do not program.
0	RW	0	Backoff Algorithm Optional 0: Disable 1: Enable

Offset Address: 80h (B0D18F0)
Default Value: 00h
Miscellaneous 1

Bit	Attribute	Default	Description
7:4	—	0	Reserved. Always reads 0
3	RW	0	Full Duplex Flow Control 0: Disable 1: Enable
2	RW	0	Half Duplex Flow Control 0: Disable 1: Enable
1	RW	0	Soft Timer 0 Status / Start 0: Timer Counting (write 0 after time out to start timer counting) 1: Timer Timed Out
0	RW	0	Soft Timer 0 Enable 0: Disable 1: Enable timer to count

Offset Address: 81h (B0D18F0)
Default Value: 00h
Miscellaneous 2

Bit	Attribute	Default	Description
7	—	0	Reserved
6	RW	0	Force Software Reset Setting this bit resets the MAC. This bit functions differently from Rx09[7] in that when Rx09[7] is set, the MAC will reset only after all state machines are in idle mode (all on-going transactions have been completed). When this bit is set, the MAC will be reset regardless of the status of the state machines. This bit is used when Rx09[7] cannot force a reset due to issues with the state machines. 0: Normal 1: Force Reset
5	—	0	Reserved (Do Not Program)
4:1	—	0	Reserved. Always reads 0
0	RW	0	Soft Timer 1 Enable 0: Disable 1: Enable timer to count

Offset Address: 83h (B0D18F0)
Default Value: 00h
Sticky Hardware Control

Bit	Attribute	Default	Description
7	RO	0	Legacy WOL Status (for software reference) This bit reports whether legacy WOL is supported. 0: Disable 1: Enable timer to count
6:4	—	0	Reserved
3	RO	0	Legacy WOL Status This bit is set when there is a legacy WOL event. 0: No legacy WOL event occurred 1: Legacy WOL event occurred
2	RW	0	Legacy WOL Enable This bit controls whether legacy WOL is a wake event. 0: Disable (if a wake event is detected (bit-3 = 1), PME# will not be asserted) 1: Enable (if a wake event is detected (bit-3 = 1), PME# will be asserted)
1:0	RW	0	Sticky DS Shadow This field reports the current power management state of the device. 00: D0 State 01: D1 State 10: D2 State 11: D3 State

Offset Address: 84h (B0D18F0)
MII Interrupt Status
Default Value: 00h

The bits in this register correspond to bits in the MII Interrupt Mask register (Rx86). An interrupt is generated when corresponding bits in both registers equal one.

Bit	Attribute	Default	Description
7	RW1C	0	Power Event Report in Test Mode
6	RW	0	User Defined Host Driven Interrupt
5	—	0	Reserved Always reads 0
4	RW1C	0	Suspend Mode MII Polling Status Change
3	RW1C	0	Transmit Data Write Buffer Queue Race Will be set by transmit shutdown
2	—	0	Reserved Always reads 0
1	RW1C	0	Soft Timer 1 Timeout
0	RW1C	0	Soft Timer 0 Timeout All bits above: write 0 to clear the interrupt

Offset Address: 86h (B0D18F0)
MII Interrupt Mask
Default Value: 00h

The bits in this register correspond to bits in the MII Interrupt Status register (Rx84). An interrupt is generated when corresponding bits in both registers equal one.

Bit	Attribute	Default	Description
7	RW	0	Interrupt on MII Interrupt Status (Rx84) Bit-7
6	RW	0	Interrupt on MII Interrupt Status (Rx84) Bit-6
5	—	0	Reserved Always reads 0
4	RW	0	Interrupt on MII Interrupt Status (Rx84) Bit-4
3	RW	0	Interrupt on MII Interrupt Status (Rx84) Bit-3
2	—	0	Reserved Always reads 0
1	RW	0	Interrupt on MII Interrupt Status (Rx84) Bit-1
0	RW	0	Interrupt on MII Interrupt Status (Rx84) Bit-0 0: Disable 1: Enable

Offset Address: 93h (B0D18F0)
Flash Checksum
Default Value: 00h

This register stores the checksum from the EEPROM after programming.

Bit	Attribute	Default	Description
15:0	RW	0	EEPROM Checksum

Offset Address: 95-94h (B0D18F0)
Suspend Mode MII Address
Default Value: 0000h

Bit	Attribute	Default	Description
15:0	RW	0	MII Address During Suspend Functionally, this field is the same as Rx71[4:0]. However, during suspend state this field is used because Rx71[4:0] cannot be accessed.

Offset Address: 99-98h (B0D18F0)
Pause Timer
Default Value: 0000h

Bit	Attribute	Default	Description
15:0	RW	0	Pause Timer Value This field is used for full duplex flow control. When the Receive FIFO is nearly full, The transmitter can send a pause frame to the transmitting side (generally a switch) to request a pause. The length of pause time is determined by this field.

Offset Address: 9Ah (B0D18F0)
Pause Status
Default Value: 00h

Bit	Attribute	Default	Description
7:1	—	0	Reserved
0	RW	0	Pause Status 0: Not paused 1: Paused

Offset Address: 9D-9Ch (B0D18F0)
Soft Timer 0
Default Value: 0000h

Bit	Attribute	Default	Description
7:0	RW	0	Soft Timer 0 Count Value This field reports the count value of soft timer 0.

Offset Address: 9F-9Eh (B0D18F0)
Soft Timer 1
Default Value: 0000h

Bit	Attribute	Default	Description
7:0	RW	0	Soft Timer 1 Count Value This field reports the count value of soft timer 1.

Offset Address: A0h (B0D18F0)
Wake On LAN Control Set
Default Value: 00h

Bit	Attribute	Default	Description
7:0	RW	0	Wake on LAN Control Set

Offset Address: A4h (B0D18F0)
Wake On LAN Control Clear
Default Value: 00h

Bit	Attribute	Default	Description
7	RW	0	Link Off Detected (determines whether the system wakes up from link off detection)
6	RW	0	Link On Detected (determines whether the system wakes up from link on detection)
5	—	0	Magic Packet Filter (determines whether the system wakes up when a Magic Packet is detected)
4	RW	0	Unicast Filter (determines whether the system wakes up when a Unicast Packet is detected)
3	RW	0	CRC3 Pattern Match Filtering (determines whether the system wakes up when packet matching CRC3 pattern is detected)
2	—	0	CRC2 Pattern Match Filtering (determines whether the system wakes up when packet matching CRC2 pattern is detected)
1	RW	0	CRC1 Pattern Match Filtering (determines whether the system wakes up when packet matching CRC1 pattern is detected)
0	RW	0	CRC0 Pattern Match Filtering (determines whether the system wakes up when packet matching CRC0 pattern is detected) All bits above: 0: Disable 1: Enable

Offset Address: A1h (B0D18F0)
Power Configuration Set
Default Value: 00h

Bit	Attribute	Default	Description
7:0	RW	0	Power Configuration Set

Offset Address: A5h (B0D18F0)
Power Configuration Clear
Default Value: 00h

Bit	Attribute	Default	Description
7:6	—	0	Reserved
5	—	0	WOL Type 0: Driven by Level 1: Driven By Pulse
4	RW	0	Legacy WOL 0: Disable 1: Enable
3:2	—	0	Reserved
1:0	RW	0	Reserved (Do not program)

Offset Address: A3h (B0D18F0)
Wake On LAN Configuration Set
Default Value: 00h

Bit	Attribute	Default	Description
7:0	RW	0	Wake On LAN Configuration Set

Offset Address: A7h (B0D18F0)
Wake On LAN Configuration Clear
Default Value: 00h

Bit	Attribute	Default	Description
7	RW	0	Force Power Management Enable over PME Enable Bit (Legacy Use Only)
6	RW	0	Full Duplex During Suspend
5	RW	0	Accept Multicast During Suspend This bit controls whether multicast packets are accepted during suspend state. Whether a multicast packet will actually wake up the system depends on whether the packet is a type of packet set to wake up the system, as determined by RxA0[5:0].
4	RW	0	Accept Broadcast During Suspend This bit controls whether broadcast packets are accepted during suspend state. Whether a broadcast packet will actually wake up the system depends on whether the packet is a type of packet set to wake up the system, as determined by RxA0[5:0].
3	RW	0	MDC Acceleration
2	RW	0	Extend Clock During Suspend When enabled, the clock to the PHY is sent prior to the start of data to allow more time for the PHY to return to ready state.
1:0	RW	0	Reserved (Do not program)

Offset Address: B3-B0h (B0D18F0)
Pattern CRC0
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:0	RW	0	CRC0 Pattern

Offset Address: B7-B4h (B0D18F0)
Pattern CRC1
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:0	RW	0	CRC1 Pattern

Offset Address: BB-B8h (B0D18F0)
Pattern CRC2
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:0	RW	0	CRC2 Pattern

Offset Address: BF-BCh (B0D18F0)
Pattern CRC3
Default Value: 0000 0000h

Bit	Attribute	Default	Description
127:0	RW	0	CRC3 Pattern

Offset Address: CF-C0h (B0D18F0)
Byte Mask 0
Default Value: 00h

Bit	Attribute	Default	Description
127:0	RW	0	Byte Mask 0

Offset Address: DF-D0h (B0D18F0)
Byte Mask 1
Default Value: 00h

Bit	Attribute	Default	Description
127:0	RW	0	Byte Mask 1

Offset Address: EF-E0h (B0D18F0)
Byte Mask 2
Default Value: 00h

Bit	Attribute	Default	Description
127:0	RW	0	Byte Mask 2

Offset Address: FF-F0h (B0D18F0)
Byte Mask 3
Default Value: 00h

Bit	Attribute	Default	Description
127:0	RW	0	Byte Mask 3

Bus 0 Device 19 Function 0 (B0D19F0): PCI to PCIe Bridge
Header Registers (0–46h)

Offset Address	Attribute	Default	Description
1 – 0h	RO	1106h	Vendor ID
3 – 2h	RO	287bh	Device ID

Offset Address: 5–4h (B0D19F0)
PCI Command
Default Value: 0000h

Bit	Attribute	Default	Description
15:10	—	0	Reserved
9	RO	0	Fast Back-to-Back Cycle Enable Hardwired to 0.
8	RW	0	SERR# Enable Hardwired to 0.
7	—	0	Reserved
6	RW	0	Parity Checking 0: Ignore parity errors 1: Perform parity check and take normal action on detected parity errors
5:4	—	0	Reserved
3	RO	0	Respond To Special Cycle Hardwired to 0.
2	RW	0	Bus Master 0: Never behaves as a bus master 1: Enable to operate as a bus master on the secondary interface
1	RW	0	Memory Space Access 0: Does not respond to memory space access 1: Responds to memory space access
0	RW	0	I/O Space Access 0: Does not respond to I/O space access 1: Responds to I/O space access

Offset Address: 7–6h (B0D19F0)
PCI Status
Default Value: 0200h

Bit	Attribute	Default	Description
15	RW1C	0	Parity Error Detected Set by PERRS, reset by writing 1.
14	RW1C	0	SERR# Detected
13	RW1C	0	Set When Terminated with Master-Abort, Except Special Cycle 0: No abort received 1: Transaction aborted by the master
12	RW1C	0	Set When Received a Target-Abort 0: No abort received 1: Transaction aborted by the target
11	RO	0	Set When Signaled a Target-Abort
10:9	RO	01	DEVSEL# Timing 00: Fast 01: Medium (default) 10: Slow 11: Reserved
8	RW1C	0	Set When Set or Observed SERR# and Parity Error Reserved
7	RO	0	Capable of Accepting Fast Back-to-Back as a Target Reserved
6:0	—	0	Reserved

Offset Address: 08h (B0D19F0)
Revision ID
Default Value: 00h

Bit	Attribute	Default	Description
7:0	RO	00h	Revision ID

Offset Address: 0B-09h (B0D19F0)
Class Code
Default Value: 060400h

Bit	Attribute	Default	Description
23:0	RO	060400h	Class Code

Offset Address: 0Dh (B0D19F0)
Latency Timer
Default Value: 00h

Bit	Attribute	Default	Description	Mnemonic
7:0	RO	00h	Latency Timer MLT[2:0] (Bit2-0): Reserved (RO), guarantee time slice for CPU master Note: MLT[2:1] (Bit2:1) is writable, however it is always read 0.	MLT[7:3]

Offset Address: 0Eh (B0D19F0)
Header Type
Default Value: 00h

Bit	Attribute	Default	Description
7:0	RO	00h	Header Type

Offset Address: 0Fh (B0D19F0)
Built In Self Test (BIST)
Default Value: 00h

Bit	Attribute	Default	Description
7	RO	0	BIST Support
6:0	—	0	Reserved

Offset Address: 18h (B0D19F0)
Primary Bus Number
Default Value: 00h

Bit	Attribute	Default	Description
7:0	RW	00h	Primary Bus Number

Offset Address: 19h (B0D19F0)
Secondary Bus Number
Default Value: 00h

Bit	Attribute	Default	Description
7:0	RW	00h	Secondary Bus Number

Offset Address: 1Ah (B0D19F0)
Subordinate Bus Number
Default Value: 00h

Bit	Attribute	Default	Description
7:0	RW	00h	Subordinate Bus Number

Offset Address: 1Bh (B0D19F0)
Master Latency Timer
Default Value: 00h

Bit	Attribute	Default	Description
7:0	RO	00h	Master Latency Timer

Offset Address: 1Ch (B0D19F0)
IO Base Address
Default Value: 00h

Bit	Attribute	Default	Description
7:4	RW	0	IO Base Address
3:0	—	0	Reserved

Offset Address: 1Dh (B0D19F0)
IO Limit Address
Default Value: 00h

Bit	Attribute	Default	Description
7:4	RW	0	IO Limit Address
3:0	—	0	Reserved

Offset Address: 1Eh (B0D19F0)
Secondary Status Register 1
Default Value: 80h

Bit	Attribute	Default	Description
7	RO	1	Fast Back to Back Cycle
6	—	0	Reserved
5	RO	0	66MHz Capability
4:0	—	0	Reserved

Offset Address: 1Fh (B0D19F0)
Secondary Status Register 2
Default Value: 00h

Bit	Attribute	Default	Description
7	RW1C	0	Detected Parity Error
6	RW1C	0	Received System Error
5	RW1C	0	Received Master Abort
4	RW1C	0	Received Target Abort
3	RO	0	Signaled Target Abort
2:1	RO	0	DEVSEL# Timing Status
0	RW1C	0	Master Data Parity Error Detected

Offset Address: 23-20h (B0D19F0)
Memory Limit and Base
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:20	RW	0	Memory Limit
19:16	—	0	Reserved
15:4	RW	0	Memory Base
3:0	—	0	Reserved

Offset Address: 27-24h (B0D19F0)
Prefetchable Memory Limit and Base
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:20	RW	0	Prefetchable Memory Limit
19:16	—	0	Reserved
15:4	RW	0	Prefetchable Memory Base
3:0	—	0	Reserved

Offset Address: 2F-28h (B0D19F0)
Prefetchable Upper Limit and Base
Default Value: 0000 0000 0000 0000h

Bit	Attribute	Default	Description
63:36	RO	0	Prefetchable Limit Upper 32 Bits [31:4]
35:32	RO	0	Prefetchable Limit Upper 32 Bits [3:0]
31:4	RO	0	Prefetchable Base Upper 32 Bits [31:4]
3:0	RO	0	Prefetchable Base Upper 32 Bits [3:0]

Offset Address: 33-30h (B0D19F0)
Capability Pointer
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:16	RO	0	IO Limit Upper 16 Bits
15:0	RO	0	IO Base Upper 16 Bits

Offset Address: 3F-3Eh (B0D19F0)
Bridge Control
Default Value: 0000h

Bit	Attribute	Default	Description
15:12	—	0	Reserved
11	RW	0	Discard Timer SERR# Enable
10	RW1C	0	Discard Timer Status
9	RW	0	Secondary Discard Timer
8	RW	0	Primary Discard Timer
7	RO	0	Fast Back-to-Back Enable
6	RW	0	Secondary Bus Reset
5	RW	0	Master Abort Mode
4	RW	0	VGA 16-bit Decode
3	RW	0	VGA Enable
2	RW	0	ISA Enable
1	RW	0	SERR# Enable
0	RW	0	Parity Error Response Enable

Offset Address: 40h (B0D19F0)
PCI Express Related Control
Default Value: 02h

Bit	Attribute	Default	Description
7:6	RW	0	Extended CFG Mode 00: Extended CFG mode is off. 01: FF_0xxx_xxxx and FF_1xxx_xxxx from K8 side to support extended CFG. 10: Capability header for extended configuration address support. 11: Memory mapped extended CFG address supported, RX41[7:0] should also be programmed.
5	RW	0	Enable the Capability / Status Write of the PCIe Root Port Configuration Capability
4	RW	0	Set this Bit Indicates the Connecting NB is with RCRB Space
3:1	RW	001	Charge Pump Current Control
0	RW	0	Charge Pump Style Control

Offset Address: 41h (B0D19F0)
Memory Mapped Extended CFG Address
Default Value: 00h

Bit	Attribute	Default	Description
7:0	RW	0	Extended Configuration Address for A[35:28] 00: No extended configuration address else: Extended configuration address A[35:28] from host side

Offset Address: 42h (B0D19F0)
PCI Express Device Enable and Power Management
Default Value: 0Eh

Bit	Attribute	Default	Description
7	—	0	Reserved
6	RW	0	Enable Dynamic Clock STOP for PE0 Port
5	RW	0	Enable Dynamic Clock STOP for PE1 Port
4	RW	0	Enable Dynamic Power Management
3	RW	1	Disable High Definition Audio Controller (HDAC)
2	RW	1	Disable PCI Express Root Port 0
1	RW	1	Disable PCI Express Root Port 1
0	RW	0	Disable the Downstream Set Slot Power Limit Message 0: Enable, the set slot power limit message can be sent. 1: Disable, the set slot power limit message cannot be sent.

Offset Address: 43h (B0D19F0)
PCI Express Device Power Management
Default Value: 06h

Bit	Attribute	Default	Description
7:3	—	0	Reserved
2	RW	1	Dynamic Clock Enable for PCI Express 250MHz Clock, Root Port 0
1	RW	1	Dynamic Clock Enable for PCI Express 250MHz Clock, Root Port 1
0	RW	0	Configuration BIST Mode

Offset Address: 46~44h (B0D19F0)
Memory Mapped Extended RCRB Base Address
Default Value: 000000h

Bit	Attribute	Default	Description	Mnemonic
23:0	RW	00h	Memory Mapped Extended RCRB Base Address 00: No RCRB is supported Note: RCRB address is composed by Rx46-44 (RXRCRBA[35:12]) and register – map to address [11:2]. If RCRB addressing is enabled, Rx46-44 (RXRCRBA[35:12]) = 00 and the CPU will issue cycles with address = {RXRCRBA } and up to access the RCRB of this chip; However, the first meaningful register is at 'h000.	RXRCRBA[35:12]

Root Complex Register Block

A memory space defined in PCI-to-PCIe (B0D19F0) RX46~44.

Virtual Channel Capability (000-00Fh)
Offset Address: 003-000h (RCRB)
Virtual Channel Enhanced Capability Header
Default Value: 1001 0002h

Bit	Attribute	Default	Description
31:20	RO	100h	Next Capability Offset
19:16	RO	1h	Capability Version
15:0	RO	0002h	PCI Express Extended Capability ID

Offset Address: 007-004h (RCRB)
Port VC Capability 1
Default Value: 0000 0801h

Bit	Attribute	Default	Description
31:12	—	0	Reserved
11:10	RO	10	Port Arbitration Table Entry Size To allow up to 5 ports
9:8	RO	0	Reference Clock Reserved for root port
7	—	0	Reserved
6:4	RO	0	Low Priority Extended VC Count
3	—	0	Reserved
2:0	RO	001	Extended VC Count Indicate VC1 exists.

Offset Address: 00B-008h (RCRB)
Port VC Capability 2
Default Value: 0000 0001h

Bit	Attribute	Default	Description
31:24	RO	00h	VC Arbitration Table 00 for table is not present
23:8	—	0	Reserved
7:0	RO	01h	VC Arbitration Capability Fixed at hardware fixed arbitration support.

Offset Address: 00D-00Ch (RCRB)
Port VC Control
Default Value: 0000h

Bit	Attribute	Default	Description
15:4	—	0	Reserved
3:1	RO	0	VC Arbitration Select Reserved
0	RO	0	Load VC Arbitration Table Reserved

Offset Address: 00F-00Eh (RCRB)
Port VC Status
Default Value: 0000h

Bit	Attribute	Default	Description
15:1	—	0	Reserved
0	RO	0	VC Arbitration Table Status Reserved

VC0 Resource (010-01Bh)
Offset Address: 013-010h (RCRB)
VC Resource Capability (VC0)
Default Value: 0000 0001h

Bit	Attribute	Default	Description
31:24	RO	00h	Port Arbitration Table (VC0) The table is not present.
23	—	0	Reserved
22:16	RO	00h	Maximum Time Slots (TL) Reserved since the arbitration is fixed.
15	RO	0	Reject Snoop Transactions
14	RO	0	Advanced Packet Switching Reserved
13:8	—	0	Reserved
7:0	RO	01h	Port Arbitration Capability Non-configurable hardware fixed arbitration support

Offset Address: 017-014h (RCRB)
VC Resource Control (VC0)
Default Value: 8000 00FFh

Bit	Attribute	Default	Description
31	RO	1	VC Enable
30:27	—	0	Reserved
26:24	RO	0	VC ID
23:20	—	0	Reserved
19:17	RW	0	Port Arbitration Select Port arbitration scheme is fixed
16	RO	0	Load Port Arbitration Table Reserved
15:8	—	0	Reserved
7:0	RW Bit 0: RO	FFh	TC/VC Mapping This field indicates the TCs that are mapped to VC0. If bit [n] is 1, the corresponding traffic class TCn is mapped to VC0 ($0 \leq n \leq 7$). Default is TC0, TC1, TC2, TC3, C4, TC5, TC6 and TC7 are all mapped to VC0. Note: Bit0 is hardwired to 1 (i.e. TC0 is always mapped to VC0).

Offset Address: 01B-018h (RCRB)
VC Resource Status (VC0)
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:18	—	0	Reserved
17	RO	0	VC Negotiation Pending (TL)
16	RO	0	Port Arbitration Table Status Reserved
15:0	—	0	Reserved

VC1 Resource (01C-027h)
Offset Address: 01F-01Ch (RCRB)
VC Resource Capability (VC0)
Default Value: 3000 001Eh

Bit	Attribute	Default	Description
31:24	RO	30h	Port Arbitration Table Offset (VC1)
23	—	0	Reserved
22:16	RO	00h	Maximum Time Slots (TL)
15	RO	0	Reject Snoop Transactions
14	RO	0	Advanced Packet Switching Reserved
13:8	—	0	Reserved
7:0	RO	1Eh	Port Arbitration Capability For support WRR-32, WRR-64, WRR-128, Time-Based WRR-128

The RX027~RX020 registers will exist only when Rx004[0] is programmed to 1. If Rx004[0] = 0, all the following contents will be read as 0.

Offset Address: 023-020h (RCRB)
VC Resource Control (VC1)
Default Value: 0108 0000h

Bit	Attribute	Default	Description
31	RW	0	VC Enable
30:27	—	0	Reserved
26:24	RW	1h	VC ID
23:20	—	0	Reserved
19:17	RW	4h	Port Arbitration Select For TWRR
16	RO	0	Load Port Arbitration Table
15:8	—	0	Reserved
7:0	RW Bit 0: RO	00h	TC/VC Mapping This field indicates the TCs that are mapped to VC1. If bit [n] is 1, the corresponding traffic class TCn is mapped to VC1 ($0 \leq n \leq 7$). Default is TC0, TC1, TC2, TC3, C4, TC5, TC6 and TC7 are all mapped to VC0. Note: Bit0 is hardwired to 0 (i.e. TC0 is always mapped to VC0).

Offset Address: 027-024h (RCRB)
VC Resource Status (VC1)
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:18	—	0	Reserved
17	RO	0	VC Negotiation Pending (TL)
16	RO	0	Port Arbitration Table Status
15:0	—	0	Reserved

Port Arbitration for VC1 (030h-06F)
Offset Address: 033-030h (RCRB)
Port Arbitration Table 1
Default Value: 0000 0000h

Bit	Attribute	Default	Description			
31:28	RW	0	Phase 7			
			0: Idle	1: RP0	2: RP1	
			3: HDAC	4: PCI Slots	5~F:	Internal Devices.
27:24	RW	0	Phase 6			
23:20	RW	0	Phase 5			
19:16	RW	0	Phase 4			
15:12	RW	0	Phase 3			
11:8	RW	0	Phase 2			
7:4	RW	0	Phase 1			
3:0	RW	0	Phase 0			

Offset Address: 037-034h (RCRB)
Port Arbitration Table 2
Default Value: 0000 0000h

Bit	Attribute	Default	Description			
31:28	RW	0	Phase 15			
27:24	RW	0	Phase 14			
23:20	RW	0	Phase 13			
19:16	RW	0	Phase 12			
15:12	RW	0	Phase 11			
11:8	RW	0	Phase 10			
7:4	RW	0	Phase 9			
3:0	RW	0	Phase 8			

Offset Address: 03B-038h (RCRB)
Port Arbitration Table 3
Default Value: 0000 0000h

Bit	Attribute	Default	Description			
31:28	RW	0	Phase 23			
27:24	RW	0	Phase 22			
23:20	RW	0	Phase 21			
19:16	RW	0	Phase 20			
15:12	RW	0	Phase 19			
11:8	RW	0	Phase 18			
7:4	RW	0	Phase 17			
3:0	RW	0	Phase 16			

Offset Address: 03F-03Ch (RCRB)
Port Arbitration Table 4
Default Value: 0000 0000h

Bit	Attribute	Default	Description			
31:28	RW	0	Phase 31			
27:24	RW	0	Phase 30			
23:20	RW	0	Phase 29			
19:16	RW	0	Phase 28			
15:12	RW	0	Phase 27			
11:8	RW	0	Phase 26			
7:4	RW	0	Phase 25			
3:0	RW	0	Phase 24			

Offset Address: 043-040h (RCRB)
Port Arbitration Table 5
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:28	RW	0	Phase 39
27:24	RW	0	Phase 38
23:20	RW	0	Phase 37
19:16	RW	0	Phase 36
15:12	RW	0	Phase 35
11:8	RW	0	Phase 34
7:4	RW	0	Phase 33
3:0	RW	0	Phase 32

Offset Address: 047-044h (RCRB)
Port Arbitration Table 6
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:28	RW	0	Phase 47
27:24	RW	0	Phase 46
23:20	RW	0	Phase 45
19:16	RW	0	Phase 44
15:12	RW	0	Phase 43
11:8	RW	0	Phase 42
7:4	RW	0	Phase 41
3:0	RW	0	Phase 40

Offset Address: 04B-048h (RCRB)
Port Arbitration Table 7
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:28	RW	0	Phase 55
27:24	RW	0	Phase 54
23:20	RW	0	Phase 53
19:16	RW	0	Phase 52
15:12	RW	0	Phase 51
11:8	RW	0	Phase 50
7:4	RW	0	Phase 49
3:0	RW	0	Phase 48

Offset Address: 04F-04Ch (RCRB)
Port Arbitration Table 8
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:28	RW	0	Phase 63
27:24	RW	0	Phase 62
23:20	RW	0	Phase 61
19:16	RW	0	Phase 60
15:12	RW	0	Phase 59
11:8	RW	0	Phase 58
7:4	RW	0	Phase 57
3:0	RW	0	Phase 56

Offset Address: 053-050h (RCRB)
Port Arbitration Table 9
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:28	RW	0	Phase 71
27:24	RW	0	Phase 70
23:20	RW	0	Phase 69
19:16	RW	0	Phase 68
15:12	RW	0	Phase 67
11:8	RW	0	Phase 66
7:4	RW	0	Phase 65
3:0	RW	0	Phase 64

Offset Address: 057-054h (RCRB)
Port Arbitration Table 10
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:28	RW	0	Phase 79
27:24	RW	0	Phase 78
23:20	RW	0	Phase 77
19:16	RW	0	Phase 76
15:12	RW	0	Phase 75
11:8	RW	0	Phase 74
7:4	RW	0	Phase 73
3:0	RW	0	Phase 72

Offset Address: 05B-058h (RCRB)
Port Arbitration Table 11
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:28	RW	0	Phase 87
27:24	RW	0	Phase 86
23:20	RW	0	Phase 85
19:16	RW	0	Phase 84
15:12	RW	0	Phase 83
11:8	RW	0	Phase 82
7:4	RW	0	Phase 81
3:0	RW	0	Phase 80

Offset Address: 05F-05Ch (RCRB)
Port Arbitration Table 12
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:28	RW	0	Phase 95
27:24	RW	0	Phase 94
23:20	RW	0	Phase 93
19:16	RW	0	Phase 92
15:12	RW	0	Phase 91
11:8	RW	0	Phase 90
7:4	RW	0	Phase 89
3:0	RW	0	Phase 88

Offset Address: 063-060h (RCRB)
Port Arbitration Table 13
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:28	RW	0	Phase 103
27:24	RW	0	Phase 102
23:20	RW	0	Phase 101
19:16	RW	0	Phase 100
15:12	RW	0	Phase 99
11:8	RW	0	Phase 98
7:4	RW	0	Phase 97
3:0	RW	0	Phase 96

Offset Address: 067-064h (RCRB)
Port Arbitration Table 14
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:28	RW	0	Phase 111
27:24	RW	0	Phase 110
23:20	RW	0	Phase 109
19:16	RW	0	Phase 108
15:12	RW	0	Phase 107
11:8	RW	0	Phase 106
7:4	RW	0	Phase 105
3:0	RW	0	Phase 104

Offset Address: 06B-068h (RCRB)
Port Arbitration Table 15
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:28	RW	0	Phase 119
27:24	RW	0	Phase 118
23:20	RW	0	Phase 117
19:16	RW	0	Phase 116
15:12	RW	0	Phase 115
11:8	RW	0	Phase 114
7:4	RW	0	Phase 113
3:0	RW	0	Phase 112

Offset Address: 06F-06Ch (RCRB)
Port Arbitration Table 16
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:28	RW	0	Phase 127
27:24	RW	0	Phase 126
23:20	RW	0	Phase 125
19:16	RW	0	Phase 124
15:12	RW	0	Phase 123
11:8	RW	0	Phase 122
7:4	RW	0	Phase 121
3:0	RW	0	Phase 120

Root Complex Topology Capability List (100-14Fh)
Offset Address: 103-100h (RCRB)
Root Complex Link Declaration Capabilities Header
Default Value: 0001 0005h (B0D19F0 Rx40[4]=0)
1A01 0005h (B0D19F0 Rx40[4]=1)

Bit	Attribute	Default	Description
31:20	RO	000h 1A0h	Next Capability Default value = 000h when B0D19F0 Rx40[4]=0. Default value = 1A0h when B0D19F0 Rx40[4]=1.
19:16	RO	1h	Capability Version
15:0	RO	0005h	Capability ID

Offset Address: 107-104h (RCRB)
Element Self Description
Default Value: 0001 0301h

Bit	Attribute	Default	Description	Mnemonic
31:24	RO	0	Port Number	
23:16	RO	01h	Component ID	RRCRB_CID [7:0]
15:8	RO	03h	Number of Link Entries	
7:4	—	0	Reserved	
3:0	RO	1h	Element Type 0h: Configuration Space Element 1h: System egress port or internal sink 2h: Internal Root Complex Link	

Offset Address: 113-110h (RCRB)
Root Port 0 Descriptor
Default Value: 0101 0003h

Bit	Attribute	Default	Description
31:24	RO	01	Target Port Number for Root Port 0 Indicate the port number of RCRB
23:16	RO	01h	Target Component ID
15:2	—	0	Reserved
1	RO	1	Link Type Indicate the link points to a root port
0	RO	1	Link Valid

Offset Address: 11F-118h (RCRB)
Root Port 0 Base Address
Default Value: 0000 0000 0000 0000h

Bit	Attribute	Default	Description
63:28	—	0	Reserved
27:20	RO	0	Bus Number Must match PCI-to-PCIe Bridge (B0D19F0) Rx19 value. The value is automatically sync with PCI-to-PCIe Bridge (B0D19F0) Rx19 value.
19:15	RO	0	Device Number
14:12	RO	0	Function Number
11:0	—	0	Reserved

Offset Address: 123-120h (RCRB)
Root Port 1 Descriptor
Default Value: 0201 0003h

Bit	Attribute	Default	Description
31:24	RO	02h	Target Port Number for Root Port 1
23:16	RO	01h	Target Component ID
15:2	—	0	Reserved
1	RO	1	Link Type Indicates the link point to a root port
0	RO	1	Link Valid

Offset Address: 12F-128h (RCRB)
Root Port 1 Base Address
Default Value: 0000 0000 0000 1000h

Bit	Attribute	Default	Description
63:28	—	0	Reserved
27:20	RO	0	Bus Number Must match PCI-to-PCIe Bridge (B0D19F0) Rx19 value. The value is automatically sync with PCI-to-PCIe Bridge (B0D19F0) Rx19 value.
19:15	RO	0	Device Number
14:12	RO	1h	Function Number
11:0	—	0	Reserved

Offset Address: 133-130h (RCRB)
HDAC Descriptor
Default Value: 0301 0003h

Bit	Attribute	Default	Description
31:24	RO	03h	Target Port Number for High Definition Audio Controller (HDAC)
23:16	RO	01h	Target Component ID
15:2	—	0	Reserved
1	RO	1	Link Type Indicates the link points to a root port
0	RO	1	Link Valid

Offset Address: 13F-138h (RCRB)
HDAC Base Address
Default Value: 0000 0000 0000 8000h

Bit	Attribute	Default	Description
63:32	—	0	Reserved
27:20	RO	0	Bus Number Must match PCI-to-PCIe Bridge (B0D19F0) Rx19 value. The value is automatically sync with PCI-to-PCIe Bridge (B0D19F0) Rx19 value.
19:15	RO	1h	Device Number
14:12	RO	0	Function Number
11:0	—	0	Link Valid

The following space (Rx140-Rx1AB) is not available when there is no RCRB in NB (PCI-to-PCIe B0D19F0 Rx40[4] = 0). If there is no RCRB in NB, the following registers will be all read as zeros)

Offset Address: 143-140h (RCRB)
Upstream Link Descriptor
Default Value: 0601 0001h

Bit	Attribute	Default	Description
31:24	RO	06h	Target Port Number
23:16	RO	01h	Target Component ID
15:2	—	0	Reserved
1	RO	0	Link Type Indicates the link points to RCRB in NB.
0	RO	1	Link Valid

Offset Address: 14F-148h (RCRB)
Upstream Link Base Address
Default Value: 0000 0000 0000 0000h

Bit	Attribute	Default	Description
63:36	RO	0	Base Address Upper
35:0	RO	0	Base Address Lower

Internal Link Capabilities List (1A0-1ABh)
Offset Address: 1A3-1A0h (RCRB)
Internal Link Capability Header
Default Value: 0001 0006h

Bit	Attribute	Default	Description
31:20	RO	000h	Next Capability Offset
19:16	RO	01h	Capability Version
15:0	RO	0006h	Capability ID

Offset Address: 1A7-1A4h (RCRB)
Link Capabilities
Default Value: 0000 2421h

Bit	Attribute	Default	Description
31:18	—	0	Reserved
17:15	RO	0	L1 Exit Latency Do not support
14:12	RO	2h	L0s Exit Latency Indicates that exit latency is 128ns to less than 256ns
11:10	RO	01	Active State Link PM Support
9:4	RO	2h	Maximum Link Width Indicates the maximum link width is 2 ports => 2 lanes
3:0	RO	1h	Maximum Link Speed Indicates the link speed is 2.5Gb/s

Offset Address: 1A9-1A8h (RCRB)
Link Control
Default Value: 0002h

Bit	Attribute	Default	Description
15:8	—	0	Reserved
7	RW	0	Extended Synch When set, forces extended transmission of FTS ordered sets when exiting L0s prior to entering L0
6:2	—	0	Reserved
1:0	RW	10	Active State Link PM Control 00: Disabled 01: L0s entry enabled 10: Reserved 11: Reserved

Offset Address: 1AB-1AAh (RCRB)**Link Status****Default Value: 0021h**

Bit	Attribute	Default	Description
15:10	—	0	Reserved
9:4	RO	02h	Negotiated Link Width
3:0	RO	1h	Link Speed. Link is 2.5Gb/s

Bus 0 Device 19 Function 1 (B0D19F1): PCI to PCI Bridge

Header Registers (0-40h)

Offset Address	Attribute	Default	Description
1 – 0h	RO	1106h	Vendor ID
3 – 2h	RO	287ah	Device ID

Offset Address: 5-4h (B0D19F1)

PCI Command

Default Value: 0000h

Bit	Attribute	Default	Description	Mnemonic
15:10	—	0	Reserved	
9	RO	0	Fast Back-to-Back Cycle Enable Hardwired to 0.	
8	RW	0	SERR# Enable	
7	—	0	Reserved	
6	RW	0	Parity Checking 0: Ignore parity errors 1: Perform parity check and take normal action on detected parity errors	RPTYERR1
5:4	—	0	Reserved	
3	RO	0	Respond To Special Cycle Hardwired to 0.	
2	RW	0	Bus Master 0: Never behaves as a bus master 1: Enable to operate as a bus master on the secondary interface	
1	RW	0	Memory Space Access 0: Does not respond to memory space access 1: Responds to memory space access	
0	RW	0	I/O Space Access 0: Does not respond to I/O space access 1: Responds to I/O space access	

Offset Address: 7-6h (B0D19F1)

PCI Status

Default Value: 0200h

Bit	Attribute	Default	Description
15	RW1C	0	Parity Error Detected Set by PERRS, reset by writing 1.
14	RW1C	0	SERR# Detected
13	RW1C	0	Set When Terminated with Master-Abort, Except Special Cycle 0: No abort received 1: Transaction aborted by the master
12	RW1C	0	Set When Received a Target-Abort 0: No abort received 1: Transaction aborted by the target
11	RO	0	Set When Signaled a Target-Abort NB never signals Target Abort
10:9	RO	01	DEVSEL# Timing 00: Fast 01: Medium (default) 10: Slow 11: Reserved
8	RW1C	0	Set When Set or Observed SERR# and Parity Error Reserved
7	RO	0	Capable of Accepting Fast Back-to-Back as a Target Reserved
6:0	—	0	Reserved

Offset Address: 08h (B0D19F1)

Revision ID

Default Value: 00h

Bit	Attribute	Default	Description
7:0	RO	0	Revision ID

Offset Address: 0B-09h (B0D19F1)
Class Code
Default Value: 060400h

Bit	Attribute	Default	Description
23:0	RO	060400h	Class Code

Offset Address: 0Dh (B0D19F1)
Latency Timer
Default Value: 00h

Bit	Attribute	Default	Description	Mnemonic
7:0	RO	00h	Latency Timer MLT[2:0] (Bit2-0): Reserved (RO), guarantee time slice for CPU master Note: MLT[2:1] (Bit2:1) is writable, however it is always read 0.	MLT[7:3]

Offset Address: 0Eh (B0D19F1)
Header Type
Default Value: 81h

Bit	Attribute	Default	Description
7:0	RO	81h	Header Type

Offset Address: 0Fh (B0D19F1)
Built In Self Test (BIST)
Default Value: 00h

Bit	Attribute	Default	Description
7	RO	0	BIST Support
6:0	—	0	Reserved

Offset Address: 18h (B0D19F1)
Primary Bus Number
Default Value: 00h

Bit	Attribute	Default	Description
7:0	RW	00h	Primary Bus Number

Offset Address: 19h (B0D19F1)
Secondary Bus Number
Default Value: 00h

Bit	Attribute	Default	Description
7:0	RW	00h	Secondary Bus Number

Offset Address: 1Ah (B0D19F1)
Subordinate Bus Number
Default Value: 00h

Bit	Attribute	Default	Description
7:0	RW	00h	Subordinate Bus Number

Offset Address: 1Bh (B0D19F1)
Master Latency Timer
Default Value: 00h

Bit	Attribute	Default	Description
7:0	RO	00h	Master Latency Timer

Offset Address: 1Ch (B0D19F1)
IO Base Address
Default Value: 00h

Bit	Attribute	Default	Description
7:4	RW	0	IO Base Address
3:0	—	0	Reserved

Offset Address: 1Dh (B0D19F1)
IO Limit Address
Default Value: 00h

Bit	Attribute	Default	Description
7:4	RW	0	IO Limit Address
3:0	—	0	Reserved

Offset Address: 1Eh (B0D19F1)
Secondary Status Register 1
Default Value: 00h

Bit	Attribute	Default	Description
7	RO	0	Fast Back to Back Cycle
6	—	0	Reserved
5	RO	0	66MHz Capability
4:0	—	0	Reserved

Offset Address: 1Fh (B0D19F1)
Secondary Status Register 2
Default Value: 00h

Bit	Attribute	Default	Description
7	RW1C	0	Detected Parity Error
6	RW1C	0	Received System Error
5	RW1C	0	Received Master Abort
4	RW1C	0	Received Target Abort
3	RO	0	Signaled Target Abort
2:1	RO	0	DEVSEL# Timing Status
0	RW1C	0	Master Data Parity Error Detected

Offset Address: 23-20h (B0D19F1)
Memory Limit and Base
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:20	RW	0	Memory Limit
19:16	—	0	Reserved
15:4	RW	0	Memory Base
3:0	—	0	Reserved

Offset Address: 27-24h (B0D19F1)
Prefetchable Memory Limit and Base
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:20	RW	0	Prefetchable Memory Limit
19:16	—	0	Reserved
15:4	RW	0	Prefetchable Memory Base
3:0	—	0	Reserved

Offset Address: 2F-28h (B0D19F1)
Prefetchable Upper Limit and Base
Default Value: 0000 0000 0000 0000h

Bit	Attribute	Default	Description
63:36	RO	0	Prefetchable Limit Upper 32 Bits
35:32	RO	0	Prefetchable Limit Upper 32 Bits [3:0]
31:4	RO	0	Prefetchable Base Upper 32 Bits [31:4]
3:0	RO	0	Prefetchable Base Upper 32 Bits [3:0]

Offset Address: 33-30h (B0D19F1)
Capability Pointer
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:16	RO	0	IO Limit Upper 16 Bits
15:0	RO	0	IO Base Upper 16 Bits

Offset Address: 3F-3Eh (B0D19F1)
Bridge Control
Default Value: 0000h

Bit	Attribute	Default	Description
15:12	—	0	Reserved
11	RW	0	Discard Timer SERR# Enable
10	RW1C	0	Discard Timer Status
9	RW	0	Secondary Discard Timer
8	RW	0	Primary Discard Timer
7	RO	0	Fast Back-to-Back Enable
6	RW	0	Secondary Bus Reset
5	RW	0	Master Abort Mode
4	RW	0	VGA 16-bit Decode
3	RW	0	VGA Enable
2	RW	0	ISA Enable
1	RW	0	SERR# Enable
0	RW	0	Parity Error Response Enable

Offset Address: 40h (B0D19F1)
External PCI Device Enable Control
Default Value: 00h

Bit	Attribute	Default	Description
7	—	0	Reserved
6	RW	0	Hide AD25 on External PCI Bus When Assert
5	RW	0	Hide AD24 on External PCI Bus When Assert
4	RW	0	Hide AD23 on External PCI Bus When Assert
3	RW	0	Hide AD22 on External PCI Bus When Assert
2	RW	0	Hide AD21 on External PCI Bus When Assert
1	RW	0	Hide AD20 on External PCI Bus When Assert
0	RW	0	Hide AD19 on External PCI Bus When Assert

Bus n Device 0 Function 0 (BnD0F0) – PCI Express Root Port 0 (PCI-to-PCI Virtual Bridge)

Bus n Device 0 Function 0, a 2-Lane PCI Express root port. All registers are located in PCI configuration space and should be programmed using PCI configuration mechanism 1 through I/O registers CF8 / CFC with bus number n, device number 0 and function number 0. Registers over 256 bytes, i.e., RX100~RXFFF, can be programmed with MMIO mechanism.

Header Registers (0-3Fh)

Offset Address	Attribute	Default	Description
1 – 0h	RO	1106h	Vendor ID
3 – 2h	RO	287Ch	Device ID

Offset Address: 5-4h (BnD0F0)

Command Register

Default Value: 0000h

Bit	Attribute	Default	Description	Mnemonic
15:11	—	0	Reserved	
10	RW	0	Interrupt Disabled Set when the device is prevented from generating INTx messages	
9	—	0	Reserved	
8	RW	0	SERR# Enable 0: Disable error report 1: Enable reporting of non-fatal and fatal errors	RSERR_PE0
7	—	0	Reserved	
6	RW	0	Parity Error Response 0: Ignore parity errors & continue 1: Take normal action on detected parity errors	RPTYERR_PE0
5:3	—	0	Reserved	
2	RW	0	Bus Master Enable 0: Disable 1: Enable Controls the ability to forward Memory and I/O Read/Write requests in the upstream direction. Disabling this bit disables MSI messages.	
1	RW	0	Memory Space 0: Ignore downstream memory transactions; memory cycles with address falling in the claimed range will be forwarded to the PCI Bus. 1: Enable downstream memory cycle to this port if its address falling in the claimed range of this device.	
0	RW	0	I/O Space 0: Ignore downstream I/O transactions; I/O cycles with address falling in the claimed range will be forwarded to the PBI Bus. 1: Enable downstream I/O cycle to this port if its address falling in the claimed range of this device.	

Offset Address: 7-6h (BnD0F0)
Status Register
Default Value: 0010h

Bit	Attribute	Default	Description
15	RW1C	0	Detected Parity Error This bit is set whenever a poisoned TLP is received, regardless the state of Parity Error Enabled (Rx4[6])
14	RW1C	0	Signaled System Error This bit is set when: A device sends an ERR_FATAL or ERR_NONFATAL message Rx4[8] = 1
13	RW1C	0	Received Master Abort This bit is set when receiving a completion with Unsupported Request Completion Status
12	RW1C	0	Received Target Abort This bit is set when receiving a completion with Completer Abort Completion Status
11	RW1C	0	Signaled Target Abort This bit is set when completing a Request with Completer Abort Completion Status
10:9	—	0	Reserved (Always 0)
8	RW1C	0	Master Data Parity Error This bit is set if Parity Error Enable bit (Rx4[6]) is set and either one of the following two conditions occurs: Requestor receives a Completion marked poisoned Requestor poisons a write Request
7:5	—	0	Reserved
4	RO	1	Capabilities List Indicates the presence of an extended capability list item. Always set to 1 for PCI Express device
3	RO	0	Interrupt Status Indicate an INTx message is pending internally (TL)
2:0	—	0	Reserved

Offset Address: 8h (BnD0F0)
Revision ID
Default Value: 00h

Bit	Attribute	Default	Description
7:0	RO	00h	Revision Code

Offset Address: 0B-9h (BnD0F0)
Class Code
Default Value: 060400h

Bit	Attribute	Default	Description
23:0	RO	060400h	Class Code

Offset Address: 0Ch (BnD0F0)
Cache Line Size
Default Value: 00h

Bit	Attribute	Default	Description
7:0	RO	00	Cache Line Size

Offset Address: 0Dh (BnD0F0)
Master Latency Timer
Default Value: 00h

Bit	Attribute	Default	Description
7:0	—	00	Reserved (Hardwired to 0)

Offset Address: 0Eh (BnD0F0)
Header Type
Default Value: 81h

Bit	Attribute	Default	Description
7:0	RO	81h	Header Type Code A multiple function device.

Offset Address: 0Fh (BnD0F0)
Built In Self Test (BIST)
Default Value: 00h

Bit	Attribute	Default	Description
7:0	RO	0	BIST Support

Offset Address: 17-10h (BnD0F0)
Base Address
Default Value: 0000 0000 0000 0000h

Bit	Attribute	Default	Description
63:0	RO	00h	Base Address. Reserved.

Offset Address: 18h (BnD0F0)
Primary Bus Number
Default Value: 00h

Bit	Attribute	Default	Description
7:0	RW	00h	Primary Bus Number

Offset Address: 19h (BnD0F0)
Secondary Bus Number
Default Value: 00h

Bit	Attribute	Default	Description
7:0	RW	00h	Secondary Bus Number

Offset Address: 1Ah (BnD0F0)
Subordinate Bus Number
Default Value: 00h

Bit	Attribute	Default	Description
7:0	RW	00h	Subordinate Bus Number

Offset Address: 1Bh (BnD0F0)
Subordinate Bus Number
Default Value: 00h

Bit	Attribute	Default	Description
7:0	RO	00h	Secondary Latency Timer. Reserved

Offset Address: 1Ch (BnD0F0)
I/O Base
Default Value: F0h

Bit	Attribute	Default	Description
7:4	RW	1111	I/O Base (AD[15:12] - inclusive) This bridge will forward the cycles from primary side to PCI if the IO address AD[15:12] is between IO base and IO limit (Rx1D)
3:0	RO	0	I/O Addressing Capability 0 means IO addressing is 16-bit only.

Offset Address: 1Dh (BnD0F0)
I/O Limit
Default Value: 00h

Bit	Attribute	Default	Description	Mnemonic
7:4	RW	0	I/O Limit (AD[15:12] - inclusive) This bridge will forward the cycles from primary side to end point if the IO address is between IO base (Rx1C) and IO limit	RIOLM_PE0 _ [15:12]
3:0	RO	0	I/O Addressing Capability 0 means IO addressing is 16-bit only.	

Offset Address: 1F-1Eh (BnD0F0)
Secondary Status
Default Value: 0000h

Bit	Attribute	Default	Description
15	RW1C	0	Detected Parity Error This bit is set when secondary side receives a poisoned TLP regardless of Rx4[6]
14	RW1C	0	Received System Error This bit is set when Rx4[8] is 1 and a device sends an ERR_FATAL or ERR_NONFATAL message.
13	RW1C	0	Received Master Abort
12	RW1C	0	Received Target Abort
11	RW1C	0	Signaled Target Abort
10:9	—	0	Reserved
8	RW1C	0	Master Data Parity Error This bit is set if Parity Error Enable bit (Rx4[6]) is set and either one of the following two conditions occurs: 1. Requestor receives a Completion marked poisoned. 2. Requestor poisons a write Request
7:0	—	0	Reserved

Offset Address: 21-20h (BnD0F0)
Memory Base
Default Value: FFF0h

Bit	Attribute	Default	Description
15:4	RW	FFFh	Memory Base (AD[31:20] – inclusive) The address [19:0] is not decoded.
3:0	RO	0000	Reserved Always reads 0.

Offset Address: 23-22h (BnD0F0)
Memory Limit
Default Value: 0000h

Bit	Attribute	Default	Description
15:4	RW	000h	Memory Limit (AD[31:20] – inclusive) The address [19:0] is not decoded.
3:0	—	0000	Reserved Always reads 0.

Offset Address: 25-24h (BnD0F0)
Prefetchable Memory Base
Default Value: FFF0h

Bit	Attribute	Default	Description
15:4	RW	FFFh	Prefetchable Memory Base AD[31:20]
3:0	—	0000	Reserved Always reads 0.

Offset Address: 27-26h (BnD0F0)
Prefetchable Memory Limit
Default Value: 0000h

Bit	Attribute	Default	Description
15:4	RW	000h	Prefetchable Memory Limit AD[31:20]
3:0	—	0000	Reserved Always reads 0.

Offset Address: 2B-28h (BnD0F0)
Prefetchable Memory Upper Base
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:4	RO	00h	Reserved Always reads 0.
3:0	RW	0000	AD[35:32] This chip supports up to 16G

Offset Address: 2F-2Ch (BnD0F0)
Prefetchable Memory Upper Limit
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:4	—	00h	Reserved Always reads 0.
3:0	RW	0000	AD[35:32] This chip supports up to 16G

Offset Address: 31-30h (BnD0F0)
I/O Base Upper
Default Value: 0000h

Bit	Attribute	Default	Description
15:0	RO	00h	I/O Base Upper 16 bits Address

Offset Address: 33-32h (BnD0F0)
I/O Base Limit
Default Value: 0000h

Bit	Attribute	Default	Description
15:0	RO	00h	I/O Limit Upper 16 bits Address

Offset Address: 34h (BnD0F0)
Capability Pointer
Default Value: 40h

Contains an offset from the start of configuration space.

Bit	Attribute	Default	Description
7:0	RO	40h	Capability Pointer Always reads 40h. Capability Pointer link list: Rx34 → Rx40 → Rx68 → Rx70 → NULL

Offset Address: 3Ch (BnD0F0)
Interrupt Line
Default Value: 00h

Bit	Attribute	Default	Description
7:0	RW	00h	INT Line (For Software Use Only)

Offset Address: 3Dh (BnD0F0)
Interrupt Pin
Default Value: 01h

Bit	Attribute	Default	Description
7:0	RO	01h	INT Pin 01: INTA

Offset Address: 3F-3Eh (BnD0F0)
Bridge Control
Default Value: 0000h

Bit	Attribute	Default	Description
15:7	—	0	Reserved
6	RW	0	Secondary Bus Reset 0: No reset 1: Triggers a warm reset on the corresponding PCI Express Port
5	—	0	Reserved
4	RW	0	Base VGA 16 bits Decode 0: All VGA alias range will be forwarded 1: Only forward base VGA range (Alias range will not be forwarded)
3	RW	0	VGA Compatible I/O and Memory Address Range 0: Do not forward VGA compatible memory and I/O 1: Forward VGA compatible memory and I/O Note: VGA addresses are memory A0000-BFFFFh and I/O addresses 3B0-3BBh, 3C0-3CFh and 3D0-3DFh (10-bit decode). "Mono" text mode uses B0000-B7FFFh and "Color" Text Mode uses B8000-BFFFFh. Graphics modes use Axxxxh. Mono VGA uses I/O addresses 3Bx-3Cxh and Color VGA uses 3Cx-3Dxh. If an MDA is present, a VGA will not use the 3Bxh I/O addresses and B0000-B7FFFh memory space; if not, the VGA will use those addresses to emulate MDA modes.
2	RW	0	Block/Forward ISA I/O Cycles 0: Forward all I/O cycles with address in the range defined by the I/O Base and I/O Limit 1: Do not forward ISA I/O that are in the top 768 bytes of each 1K byte block address range
1	RW	0	SERR Enable Controls the forwarding of ERR_COR, ERR_NONFATAL and ERR_FATAL from secondary to primary 0: Disable 1: Enable
0	RW	0	Parity Error Response Enable 0: Ignore the response to poisoned TLPs 1: Enable the response to poisoned TLPs

PCI Express Capability Registers (40-63h)
Offset Address: 41-40h (BnD0F0)
PCI Express List
Default Value: 6810h

Bit	Attribute	Default	Description
15:8	RO	68h	Next Pointer
7:0	RO	10h	Capability ID

Offset Address: 43-42h (BnD0F0)
PCI Express Capabilities
Default Value: 0041h

Bit	Attribute	Default	Description
15:14	—	0	Reserved
13:9	RO	00h	Interrupt Message Number
8	RO	0	Slot Implemented This bit when set indicates that the PCI Express Link associated with this Port is connected to a slot (as compared to being connected to an integrated component or being disabled),
7:4	RO	0100	Device / Port Type 0100b: Root Port of PCI Express Root Complex
3:0	RO	1	Capability Version

Offset Address: 47-44h (BnD0F0)
Device Capabilities
Default Value: 0000 0nn1h

Bit	Attribute	Default	Description
31:28	—	0	Reserved
27:26	RO	0	Captured Slot Power Limit Scale
25:18	RO	00h	Captured Slot Power Limit Value
17:15	—	000	Reserved
14	RO	0	Power Indicator Present
13	RO	0	Attention Indicator Present
12	RO	0	Attention Button Present
11:9	RO	111	Endpoint L1 Acceptable Latency 111b: more than 64us
8:6	RO	HwInit	Endpoint L0s Acceptable Latency
5		0	Extended Tag Field Supported 0: 5-bit Tag field supported 1: 8-bit Tag field supported
4:3	RO	00	Phantom Functions Supported Reserved
2:0	RW	001	Max Payload Size Supported 001b: 32OW (256 bytes)

Offset Address: 49-48h (BnD0F0)
Device Control
Default Value: 0000h

Bit	Attribute	Default	Description
15	—	0	Reserved
14:12	RO	000	Max Read Request Size 000b: 128 bytes This field sets the maximum Read Request size for the device as a Requestor.
11	RO	0	Enable No Snoop If this bit is set to 1, the device is permitted to set the No Snoop bit in the Requestor Attributes of the transactions it initiate that do not require hardware enforced cache coherency.
10	RO	0	Auxiliary Power PM Enable This bit when set enables device to draw AUX power independent of PME AUX power.
9	RO	0	Phantom Functions Enable Not supported.
8	RO	0	Extended Tag Field Enable Not supported.
7:5	RW	0	Max Payload Size Maximum TLP payload size.
4	RW	0	Enable Relaxed Ordering If this bit is set to 1, the device is permitted to set the Relaxed Ordering bit in the Requestor Attributes of the transactions it initiate that do not require strong write ordering.
3	RW	0	Unsupported Request Reporting Enable
2	RW	0	Fatal Error Reporting Enable For a Root Port, the reporting of Fatal errors is internal to the root. No external ERR_FATAL message is generated.
1	RW	0	Non-Fatal Error Reporting Enable For a Root Port, the reporting of Non-Fatal errors is internal to the root. No external ERR_NONFATAL message is generated.
0	RW	0	Correctable Error Reporting Enable For a Root Port, the reporting of correctable errors is internal to the root. No external ERR_COR message is generated.

Offset Address: 4B-4Ah (BnD0F0)
Device Status
Default Value: 0010h

Bit	Attribute	Default	Description
15:6	—	0	Reserved
5	RO	0	Transactions Pending This bit when set indicates that the Port has issued Non-Posted Requests on its own behalf (using the Port's own Requestor ID) which have not been completed.
4	RO	1	AUX Power Detected
3	RW1C	0	Unsupported Request Detected
2	RW1C	0	Fatal Error Detected (TL)
1	RW1C	0	Non-Fatal Error Detected (TL)
0	RW1C	0	Correctable Error Detected (TL)

Offset Address: 4F-4Ch (BnD0F0)
Link Capabilities
Default Value: 0100 0C21h

Bit	Attribute	Default	Description
31:24	RO	01h	Port Number This field indicates the PCI Express Port number for the given PCI Express Link.
23:18	—	0	Reserved
17:15	RO	0	L1 Exit Latency 000: less than 1us. The value reported indicates the length of time this Port requires to complete transition from L1 to L0.
14:12	RO	0	L0s Exit Latency 000: less than 64ns. The value reported indicates the length of time this Port requires to complete transition from L0s to L0.
11:10	RO	11	Active State Link PM (ASPM) Support 11b: L0s and L1 supported. This field indicates the level of ASPM supported on the PCI Express Link.
9:4	RO	02h	Maximum Link Width 04h: x4 Link width
3:0	RO	1	Maximum Link Speed 0001b: 2.5Gb/s Link speed

Offset Address: 51-50h (BnD0F0)
Link Control
Default Value: 0000h

Bit	Attribute	Default	Description	Mnemonic
15:8	—	00	Reserved	
7	RW	0	Extended Synch 0: FCU Timer limit is 30us 1: FCU Timer limit is 120us	LCES_PEO
6	RW	0	Common Clock Configuration 0: Indicates that this Port and the component on the opposite end of the Link are operating with asynchronous reference clock. 1: Indicates that this Port and the component on the opposite end of the Link are operating with a distributed common reference clock.	
5	RW	0	Retrain Link A write of 1 to this bit initiates Link retrained by directing the Physical Layer LTSSM to the Recovery state.	
4	RW	0	Link Disable This bit disables the Link when set to 1.	
3	RO	0	Read Completion Boundary 0: 64 byte	
2	—	0	Reserved	
1:0	RW	00	Link Active State PM (ASPM) Control 00b: Disabled 10b: L1 Entry Enabled 01b: L0s Entry Enabled 11b: L0s and L1 Entry Enabled	

Offset Address: 53-52h (BnD0F0)
Link Status
Default Value: 0nn1h

Bit	Attribute	Default	Description
15:13	—	0	Reserved
12	RO	0	Slot Clock Configuration 0: Use an independent clock irrespective of the presence of a reference on the connector. 1: Use the same physical reference clock that the platform provides on the connector.
11	RO	0	Link Training This bit indicated that Link training is in progress (Physical Layer LTSSM is in Configuration or Recovery state) or that 1b was written to the Retrain Link bit but Link training has not yet begun. Hardware clears this bit once Link training is complete.
10	RO	0	Training Error Set when a Link training error occurred. Cleared by hardware upon successfully training of the Link to the L0 Link state.
9:4	RO	HwInit	Negotiated Link Width 000001: x1 000010: x2 000100: x4 001000: x8 010000: x16
3:0	RO	0001	Link Speed 0001: 2.5Gb/s negotiated link speed.

Offset Address: 57-54h (BnD0F0)
Slot Capabilities
Default Value: 0000 0060h

Bit	Attribute	Default	Description
31:19	RO	00h	Physical Slot Number Physical slot number attached to the Port.
18:17	—	0	Reserved
16:15	RO	0	Slot Power Limit Scale Write to the field causes the Port to send the Set_Slot_Power_Limit message.
14:7	RO	00h	Slot Power Limit Value Write to the field causes the Port to send the Set_Slot_Power_Limit message.
6	RO	1	Hot-plug Capable
5	RO	1	Hot-plug Surprise
4	RO	0	Power Indicator Present
3	RO	0	Attention Indicator Present
2	RO	0	MRL Sensor Present
1	RO	0	Power Controller Present
0	RO	0	Attention Button Present

Offset Address: 59-58h (BnD0F0)
Slot Control
Default Value: 0000h

Bit	Attribute	Default	Description
15:11	—	0	Reserved
10	RO	0	Power Controller Control 0: Power On 1: Power Off
9:8	RW	0	Power Indicator Control 00: Reserved 01: On 10: Blink 11: Off Writes to this field cause the Port to send the appropriate POWER_INDICATOR_* Message.
7:6	RW	0	Attention Indicator Control 00: Reserved 01: On 10: Blink 11: Off Writes to this field cause the Port to send the appropriate ATTENTION_INDICATOR_* Message.
5	RW	0	Hot-Plug Interrupt Enable This bit when set enables generation of Hot-Plug interrupt on enabled Hot-Plug events.
4	RW	0	Command Completed Interrupt Enable This bit when set enables the generation of Hot-Plug interrupt when a command is completed by the Hot-Plug controller.
3	RW	0	Presence Detect Changed Enable This bit when set enables the generation of Hot-Plug interrupt or Wakeup event on a presence detect changed event.
2	RO	0	MRL Sensor Changed Enable
1	RO	0	Power Fault Detected Enable
0	RW	0	Attention Button Pressed Enable This bit when set enables the generation of Hot-Plug interrupt or Wakeup event on an Attention Button pressed event.

Offset Address: 5A-5Bh (BnD0F0)
Slot Status
Default Value: 0000h

Bit	Attribute	Default	Description
15:7	—	0	Reserved
6	RO	0	Presence Detect State 0: Slot empty 1: Card present in slot
5	RO	0	MRL Sensor State
4	RW1C	0	Command Completed
3	RW1C	0	Presence Detect Changed
2	RO	0	MRL Sensor Changed
1	RO	0	Power Fault Detected
0	RW1C	0	Attention Button Pressed

Offset Address: 5D-5Ch (BnD0F0)
Root Control
Default Value: 0000h

Bit	Attribute	Default	Description
15:4	—	0	Reserved
3	RW	0	PME Interrupt Enable 0: Disable 1: Enable interrupt generation upon receipt of a PME message as reflected in the PME status register bit. A PME interrupt is also generated if the PME status register bit is set when this bit is set from a cleared state.
2	RW	0	System Error on Fatal Error Enable 0: Disable 1: Enable generation of a System Error if a Fatal Error (ERR_FATAL) is reported by any of the devices in the hierarchy associated with the Root Port, or by the Root Port itself.
1	RW	0	System Error on Non-Fatal Error Enable 0: Disable 1: Enable generation of a System Error if a Non-Fatal Error (ERR_NONFATAL) is reported by any of the devices in the hierarchy associated with the Root Port, or by the Root Port itself.
0	RW	0	System Error on Correctable Error Enable 0: Disable 1: Enable generation of a System Error if a Correctable Error (ERR_COR) is reported by any of the devices in the hierarchy associated with the Root Port, or by the Root Port itself.

Offset Address: 63-60h (BnD0F0)
Root Status
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:18	—	0	Reserved
17	RO	0	PME Pending 0: No pending PME 1: Indicates that another PME is pending when the PME Status (bit 16) is set.
16	RW1C	0	PME Status Indicates that the PME was asserted by the Requestor ID indicated in PME Requestor ID (bit[15:0]).
15:0	RO	00h	PME Requestor ID The Requestor ID of the last PME Requestor.

PCI Power Management Capability Structure Registers (68-6Fh)
Offset Address: 6B-68h (BnD0F0)
Power Management Capabilities
Default Value: C800 7001h

Bit	Attribute	Default	Description
31:27	RW	11001	PME Support Bit 31, 30 and 27 are set to 1b (PME Message will be forwarded).
26	RW	0	D2 Support
25	RW	0	D1 Support
24:22	RO	0	AUX Current
21	RW	0	Device Specific Initialization
20:19	—	0	Reserved
18:16	RO	010	Version
15:8	RO	70h	Next Capability Pointer
7:0	RO	01h	Capability ID

Offset Address: 6F-6Ch (BnD0F0)
Power Management Status/Control
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:24	RO	00h	Power Management Data
23:16	—	0	Reserved
15	RW1CS	0	PME Status This bit's setting is not modified by hot, warm, or cold reset.
14:13	RO	0	Data Scale
12:9	RO	0	Data Select
8	RWS	0	PME Enable This bit's setting is not modified by hot, warm, or cold reset.
7:2	—	0	Reserved
1:0	RW	0	Power State

PCI Message Signal Interrupt (MSI) Capability Structure Registers (70-87h)
Offset Address: 73-70h (BnD0F0)
MSI Capability Support
Default Value: 0180 0005h

Bit	Attribute	Default	Description
31:25	—	0	Reserved
24	RO	1	This MSI capability supports pre-vector masking capability
23	RO	1	This MSI capability supports 64 bit message address only
22:20	RW	000	Multiple Message Enable 000: 1 message allocated 010: 4 message allocated 100: 16 message allocated 11x: Reserved 001: 2 message allocated 011: 8 message allocated 101: 32 message allocated
19:17	RO	000	Multiple Message Capable 000: 1 message requested 010: 4 message allocated 100: 16 message requested 11x: Reserved 001: 2 message requested 011: 8 message allocated 101: 32 message requested
16	RW	0	MSI Enable 0: This Port is prohibited from using MSI to request service 1: This Port is permitted to use MSI to request service.
15:8	RO	00h	Next Capability Pointer
7:0	RO	05h	Capability ID

Offset Address: 77-74h (BnD0F0)
System-Specified Message Address - Low
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:2	RW	00h	System-Specified Message Address Bit [31:2]
1:0	RO	00	System-Specified Message Address Bit [1:0] These bits will always read as 0

Offset Address: 7B-78h (BnD0F0)
System-Specified Message Address - High
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:4	RW	00h	System-Specified Message Address Bit [63:36]
3:0	RW	0	System-Specified Message Address Bit [35:32]

Offset Address: 7D-7Ch (BnD0F0)
Message Data
Default Value: 0000h

Bit	Attribute	Default	Description
15:0	RW	0	Message Data The message data is to be put on data [15:0] of MSI cycles

Offset Address: 83-80h (BnD0F0)
Message Mask Control
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:1	RO	00h	Mask Bit
0	RW	0	Mask Bit for Message 0

Offset Address: 87-84h (BnD0F0)
Message Pending Status
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:1	RO	00h	Pending Bit
0	RO	0	Pending Bit for Message 0

PCI Express Transaction Layer Registers (A0-A4h)
Offset Address: A0h (BnD0F0)
Downstream Control I
Default Value: 01h

Bit	Attribute	Default	Description
7	RW	0	Downstream Cycles Have Traffic Class TC1 0: Disabled 1: Enabled.
6	RW	0	Downstream Cycles Have Attribute "No Snoop" Set 0: Disabled 1: Enabled.
5	RW	0	Downstream Cycles Have Attribute "Relaxed Ordering" Set 0: Disabled 1: Enabled.
4	RW	0	Downstream Lock Cycle Support 0: Disabled 1: Enabled.
3	RW	0	Downstream Arbitration Scheme 0: Fixed priority: VC1 CPL > VC0 CPL > Down Stream Command 1: Round Robin arbitration priority between VC1 CPL, VC0 CPL and Down Stream Command
2	RW	0	Downstream Post-Write Allowed to Pass IOW 0: Not allowed. 1: Allowed.
1	RW	0	Downstream Post-Write Allowed to Pass Read 0: Not allowed. 1: Allowed.
0	RW	1	Downstream Pipeline 0: Disabled 1: Enabled.

Offset Address: A1h (BnD0F0)
Downstream Control II
Default Value: 04h

Bit	Attribute	Default	Description
7	RW1C	0	Downstream Configuration Completion Status 0: Normal completion. 1: At least one configuration request ended with a CRS (Configuration Request Retry Status) completion.
6:3	—	0	Reserved
2:0	RW	100	C2P Read Completion Timeout Timer 000: Reserved 001: 1ms 010: Reserved 011: 10ms (Spec. lower bound) 100: 30ms 101: 50ms (Spec. higher bound) 110: 100ms 111: Reserved

Offset Address: A4h (BnD0F0)
Upstream Control
Default Value: 10h

Bit	Attribute	Default	Description
7	RW	0	Upstream Address A35~A31 Forced to 0 0: Disabled. 1: Enabled for system testing or loop back mode test. The upcoming data may be checked in the system memory
6	RW	0	Prevent Upstream Write FIFO from Being Overwritten
5	RW	0	Upstream Checking Malformed TLP through "Byte Enable Rule" And "Over 4K Boundary Rule" 0: Disabled. 1: Enabled.
4	RW	1	Downstream Read Wait Till The Upstream Write Data Flushed 0: Disabled. 1: Enabled.
3:2	—	0	Reserved
1	RW	0	Allows TL Map Non-Snoop Upstream Request to VC1 Request Queue Output to the Central Traffic Controller When VC1 Do Not Exist in the Capability Header (software has to program Rx144[0] = 0) 0: Disabled. 1: Enabled. (Note that when this bit is 1, the RxA4[0] have to be 0).
0	RW	0	Disable Virtual Channel 1 Support (i.e. VC1's data FIFO is used by VC0) 0: No, data FIFO of VC1 is used by VC1 1: Disable VC1, data FIFO of VC1 is reallocated to VC0, which doubles the size of VC0 data FIFO.

PCI Express Data Link Layer Registers (B0-B6h)
Offset Address: B0h (BnD0F0)
Ack / Nak Latency Timer Limit
Default Value: 3Bh

Bit	Attribute	Default	Description	Mnemonic
7:0	RW	3Bh	Timer Limit for Ack / Nak Latency Timer and Update FC Latency Timer (in unit of 250MHz) 00: 4 x 1 Clocks 02: 4 x 3 Clocks. On: 4 x (n+1) Clocks	RACKLTLM_PE0[7:0] 01: 4 x 2 Clocks ... FF: 4 x 256 Clocks.

Offset Address: B1h (BnD0F0)
Replay Timer Limit
Default Value: 59h

Bit	Attribute	Default	Description
7:0	RW	59h	Replay Timer Limit (In unit of 250MHz) 00: 8 x 1 Clocks 02: 8 x 3 Clocks On: 8 x (n+1) Clocks

Offset Address: B2h (BnD0F0)
FCU Control and Status
Default Value: 40h

Bit	Attribute	Default	Description
7	RO	0	FCU Timeout Status 1 means the FCU timeout has occurred
6	RW	1	FCU Receive Timer Enable Control 0: Disable the timeout mechanism 1: Enable the timeout mechanism
5	RW	0	FCU Receive Timer Limit 0: Timeout limit of 200us 1: Timeout limit of 300us
4	RW	0	FCU Receive Timer Reset Control 0: Timer reset by FCI/FCU only 1: Timer reset by any received DLLPs
3:1	—	0	Reserved
0	RW	0	DL & TL Reset Upstream Related Logic When Retrain Is Going On

Offset Address: B3h (BnD0F0)
Replay Timer Control
Default Value: 80h

Bit	Attribute	Default	Description
7:6	RW	10	Replay Timer Control while Rewind (resend those DLLPs which do not have corresponding ACK/NAK received) 00: Hold Replay Timer during rewind. 01: During rewind, if ACK/NAK comes in, reset and hold the Replay Timer. 10: During rewind, reset and hold the Replay Timer as long as the Retry Buffer is empty. 11: Reserved.
5:3	—	0	Reserved
2:0	RW	000	Count of Replay Timer Expired During RXL0s (Receiving Physical in L0s state) Before Resend the TLP When Rx50[7], LCES_PE0, is set to 0: 000: Wait forever for the Acknowledge from the device side 001: Resend the TLP after 1 x Replay timer expired 010: Resend the TLP after 2 x Replay timer expired 011: Resend the TLP after 4 x Replay timer expired 100: Resend the TLP after 8 x Replay timer expired 101: Resend the TLP after 16 x Replay timer expired 110: Resend the TLP after 32 x Replay timer expired 111: Resend the TLP after 64 x Replay timer expired When RX50[7], LCES_PE0, is set to 1: 000: Wait forever for the Acknowledge from the device side 001: Resend the TLP after 16 x Replay timer expired 010: Resend the TLP after 32 x Replay timer expired 011: Resend the TLP after 64 x Replay timer expired 100: Resend the TLP after 128 x Replay timer expired 101: Resend the TLP after 256 x Replay timer expired 110: Resend the TLP after 512 x Replay timer expired 111: Resend the TLP after 1024 x Replay timer expired

Offset Address: B4h (BnD0F0)
Arbitration Control
Default Value: 00h

Bit	Attribute	Default	Description
7:4	—	0	Reserved
3	RW	0	TLP vs. Flow Control Initialization for VC0 in Arbitration Priority 0: TLP is not allowed to pass FCI2 for VC0 1: TLP is allowed to pass FCI2 for VC0
2:0	RW	000	Data Link TX Packets Arbitration Scheme 000: Round Robin 001: Reserved. 010: Strict priority: TLP > ACK/NAK > FCU 011: Strict priority: TLP > FCU > ACK/NAK 100: Strict priority: ACK/NAK > TLP > FCU 101: Strict priority: ACK/NAK > FCU > TLP 110: Strict priority: FCU > TLP > ACK/NAK 111: Strict priority: FCU > ACK/NAK > TLP

Offset Address: B5h (BnD0F0)
FCU Control
Default Value: 00h

Bit	Attribute	Default	Description
7	—	0	Reserved
6	RW	0	FCU (Flow Control Unit) Timer Control 0: Update flow control credit when either Transaction Layer requested packets being sent or when FCU timer expired 1: Update flow control credit only when FCU timer expired
5:4	RW	00	ACK DLLP Collapse Method 00: Send ACK when the latency timer RACKLTL (RxB0) expired. 01: Send ACK every 4 correct TLP has been received 10: Send ACK every 8 correct TLP has been received 11: Send ACK every 16 correct TLP has been received
3:2	—	0	Reserved
1	RW	0	FCI (Flow Control Initialization) Process End Condition 0: Complete FCI process when TLP/FCU has been received 1: Do not complete FCI process even when TLP/FCU has been received
0	RW	0	VC1 FCI DLLP Transmission Scheme 0: Transmit FCI DLLP only when FCI timer expired 1: Transmit FCI DLLP continuously as long as the FCI process is not finished

Offset Address: B6h (BnD0F0)
Transaction / Link Layer Checking Control
Default Value: 03h

Bit	Attribute	Default	Description
7:5	—	0	Reserved
4	RW	0	VC Negotiate Pending Control for VC1 0: Assert VC negotiation pending after VC1 is enabled 1: Assert VC negotiation pending after RESET is de-asserted
3	—	0	Reserved
2	RW	0	ECRC Checking Control for the Case of TD equals to1 but no ECRC field in TLP 0: Ignore the error 1: Report error to Transaction Layer, which will mark the TLP as a Malformed TLP
1	RW	1	Length Malform Report Control 0: Do not report length malform to Transaction Layer 1: Report length malform to Transaction Layer
0	RW	1	LCRC Checking Control 0: Do not check LCRC 1: Check LCRC

PCI Express Physical Layer Registers (C0-C7h)
Offset Address: C3-C0h (BnD0F0)
PHY Control
Default Value: 0001 0003h

Bit	Attribute	Default	Description
31:25	—	0	Reserved
24	RW	0	Bypass PHYES Receiver Detect Function 0: RCVDOUT is derived from PHYES 1: Bypass receiver detect; RCVDOUT = 1
23:17	—	0	Reserved
16	RW	1	State Machine LTSSM Enters Detect. Active from Detect Quiet 0: Wait for the electrical idle signal from the PHYES or 12ms after RESET# becomes inactive. 1: Always wait for 12ms after the RESET# becomes inactive.
15:14	RW	00	Auto/Manual Configuration for Root Port 1 and 2 00: Auto negotiation 01: 2x1 negotiation 10: 1x2, 1x1 negotiation 11: 1x4 negotiation
13	—	0	Reserved
12:8	RW	00	PHY Lane Configuration Setting 10000: Reserved 01000: Reserved 00100: Reserved 00010: 2x with normal lane connection 00001: 1x with normal lane connection 01111: Reserved 10111: Reserved 11011: Reserved 11101: 2x with reverse lane connection 11110: 1x with reverse lane connection 10101: Force into L0S state, for testing measurement used only 00000: Use PHY negotiation Other values are not allowed.
7	RW	0	Quick Timeout Counter Setting When set to 1, the following timeout will be shorter: TIMEOUT_2MS → TIMEOUT_4US TIMEOUT_12MS → TIMEOUT_24US TIMEOUT_24MS → TIMEOUT_48US TIMEOUT_48MS → TIMEOUT_96US TIMEOUT_1024TS → TIMEOUT_32TS Receiver Detection: 15x1024ns → 1x1024ns
6	RW	0	Disable Data Scrambling / Descrambling 0: Enable data scrambling 1: Disable data scrambling
5:3	RW	000	Loopback Mode Selection This setting is applied to lane 16 ~ 19 in x4 mode, lane 16 ~ 17 in x2 mode, lane 16 in x1 mode. 000 : No loop back 001: PHYLS loopback from TX end to RX end 010: PHYES loopback from TX end to RX end 011: Reserved 100: Reserved 101: PHYLS loopback from RX end to TX end 110: PHYES loopback from RX end to TX end 111: Reserved
2:0	RW	011	COMMA Detection Window 0, 1: Illegal values Others: delay number of T to determine correct lane-to-lane deskew value

Offset Address: C7-C4h (BnD0F0)
Elastic Buffer Base Registers for Lane 0 - 1
Default Value: 0000 0044h

Bit	Attribute	Default	Description
31:7	—	0	Reserved
6:4	RW	4h	Elastic Buffer Base Register for Lane 1 0, 1, 7: Illegal values Others: delay numbers of T for elastic buffer operations
3	—	0	Reserved
2:0	RW	4h	Elastic Buffer Base Register for Lane 0 0, 1, 7: Illegal values Others: delay numbers of T for elastic buffer operations

PCI Express Power Management Module Registers (D0-D3h)
Offset Address: D3-D0h (BnD0F0)
PMC Control
Default Value: 0000 0050h

Bit	Attribute	Default	Description
31:24	RW	00h	Idle Period to Enter ASL1 Minimum time period is 128ns 00: 128ns 02: 3x128ns FF: 256x128ns
23:16	RW	00h	Idle Period to Enter L0s Minimum time period is 128ns (L0SLIM_PEO = 00) 00: 128ns 02: 3x128ns FF: 256x128ns
15	RW1C	0	Error Status Report This bit is set when device cannot have electrical idle after the waiting period programmed at RxD1[6:4] expired.
14	—	0	Reserved
13:12	RW	0	Electrical Idle Waiting Period before Move to L1 State (after issue ACK to the L1 request from the device). 00: Always wait for electrical idle 10: Wait 64 clock
11:10	—	0	Reserved
9:8	RW	0	Downstream Cycles Triggered C2P Cycles, Period of Staying at L0 Before Returned to L1 for PHY (when PMU is in non-D0 state) 00: immediately 10: 1 32QW +1cfgW or message+ delay10T
7	—	0	Reserved
6:4	RW	101	Timeout Period This timer is used when waiting for ACK from a device after issued PME_TURNOFF message to notify the device to move to power down mode. 000: 1us 010: 4us 100: 16us 110: 64us
3:2	—	0	Reserved
1	RW	0	Link Loopback 0: Normal operation 1: Direct device to enter Loopback mode, receiving data in the device will be sent to the transmit side
0	RW	0	LTSSM State During Link Reconfigure Link Width 0: When reconfigure link width, LTSSM must be in Detect state 1: When reconfigure link width, LTSSM can be in Configuration state

PCI Express Message Controller Related Registers (D8h)
Offset Address: D8h (BnD0F0)
PMC Express Message Status
Default Value: 00h

Bit	Attribute	Default	Description
7	RW1C	0	Excessive Errors Occurred But Not Reported in The MSGC 0: Normal operation. 1: There are errors not reported to the system
6:0	—	0	Reserved

PCI Express Electrical PHY Registers (E1-E4h)
Offset Address: E1h (BnD0F0)
PHYES Module Related Control
Default Value: 08h

Bit	Attribute	Default	Description
7:5	—	0	Reserved
4	RW	0	Receiving Polarity Change Control 0: Have the same polarity on the loop-back/received data 1: Have reverse polarity on the loop-back/received data
3:2	RW	10	Squelch Window Select (64~175mv)
1	RW	0	Electrical Idle State Exit Condition: Number of Non Idle Signal Detected Before Exit Idle State 0: 2 bits. 1: 10 bits.
0	RW	0	Electrical Idle State Enter Condition: Number of Idle Signal Detected Before Enter Idle State 0: 2 bits 1: 10 bits

Offset Address: E2h (BnD0F0)
PHYES Module Control – Rx/Tx I
Default Value: 00h

Bit	Attribute	Default	Description
7:6	—	0	Reserved
5	RW	0	PHYES Clock Buffer Power Down on Lane 0-1 0: All enable 1: Power down
4	RW	0	Clock Routing Impact on the TXPLL for the 2 Lanes 0: All enable 1: Lane 1 power down.
3:2	RW	00	Receiver Input Rise Delay (duty cycle adjustment for the 2 lanes) 00: 0 ps 10: 40 ps 11: 80 ps
1:0	RW	00	Receiver Input Fall Delay (duty cycle adjustment for the 2 lanes) 00: 0 ps 10: 40 ps 11: 80 ps

Offset Address: E3h (BnD0F0)
PHYES Module Control – Rx/Tx II
Default Value: 02h

Bit	Attribute	Default	Description	Mnemonic
7	RW	0	PCI Express Pads Driving Control 0: Autocomp 1: Manual setting through bits [2:0]	
6:5	RW	0	Filter Depth Valid only when RxE3[4] (CDRTYPE) = 0 00: Filter depth = 1 10: Filter depth = 8 01: Filter depth = 4 11: Filter depth = 12	
4	RW	0	CRD Type 0: New CDR type with filter 1: Original scheme	CDRTYPE0
3	RW	0	CDR Filter Depth 0: Filter depth = 3 1: Filter depth = 2	
2:0	RW	010	Lane 0 -1 Termination Resistance Selection Resistance Range: 62Ω (000b) ~ 43Ω (111b) Default: 50Ω (010b)	

Offset Address: E4h (BnD0F0)
PHYES Module Control – Rx/Tx III
Default Value: 44h

Bit	Attribute	Default	Description
7:4	RW	4h	Pre/De-Emphasis Level Selection
3:0	RW	4h	Driver Current Source Selection

PCI Express Electrical PHY Test Registers (F0-F7h)
Offset Address: F3-F0h (BnD0F0)
PHY Test
Default Value: 0600 0000h

Bit	Attribute	Default	Description	Mnemonic
31	RW	0	Electrical PHY Test Mode Enable Program this bit to 1 to start Electrical PHY test	
30:28	—	0	Reserved	
27:24	RW	6	Test Pattern Check Length Number of T when the receiving side starts to check transmitted and received patterns Suggested Value Settings: (Lane 0 for example) LPBK_SEL_PEO_[2:0] (RxCO[5:3]) = 001b: EB_BASE_00_PEO_[2:0] (RxC4[2:0]) + 2 LPBK_SEL_PEO_[2:0] (RxCO[5:3]) = 010b: EB_BASE_00_PEO_[2:0] (RxC4[2:0]) + 2 + (Loopback Path Latency/4ns) + 1	
23:20	RW	0	Select Test Pattern 0000: Reserved 0001: User define, use RxF4[25:16] 0010: K28.5 test bit sequence 0011: K28.7 test bit sequence 0100: K test for differential pair current 0101: J test for differential pair current 0110: D21.5 test bit sequence 0111: D30.3 test bit sequence 1000: Ten contiguous run of 3 test bit sequence 1001: Low transition density test bit sequence 1010: Half-rate/quarter-rate test bit sequence 1011: Low frequency spectral test bit sequence 1100: Simultaneous switching test bit sequence 1101: Reserved 1110: Reserved 1111: Reserved	MODESEL_PEO_[3:0]
19:18	—	0	Reserved	
17:16	RW	0	Select Lane for Loop Back Test 00: Loop back test on lane0 01: Loop back test on lane1 10: Reserved 11: Reserved	
15:8	RW	00	Repeated Count of the Test Pattern (as selected in RxF0[23:20]) 00~0Bh: Illegal.value 0Ch: Test pattern repeats 12 times 0Dh: Test pattern repeats 13 times ... FFh: Test pattern repeats 255 times	
7:1	—	0	Reserved	
0	RO	0	Electrical PHY Test Error 1 indicates that there is an error detected in the receiving side during the loop back test	

Offset Address: F7-F4h (BnD0F0)
PHY Test Symbol
Default Value: 0000 0000h

Bit	Attribute	Default	Description	Mnemonic
31:26	—	0	Reserved	
25:16	RW	00h	Transmitted Symbol when EPHYTST_PE0 (RxF0[31]) is set to 1 00 when EPHYTST_PE0 is 0	TPHYTXD_PE0_[9:0]
15:10	—	0	Reserved	
9:0	RO	00h	Received Symbol when EPHYTST_PE0 (RxF0[31]) is set to 1 00 when EPHYTST_PE0 is 0	

Bus n Device 0 Function 0 (BnD0F0) – PCI Express Root Port 0 Extended Space

Registers defined in the Extended Space can be accessed through PCI Express Enhanced Configuration Access Mechanism, which utilizes a flat memory-mapped address space to access the configuration registers. Please check PCI Express Specification for the detail information.

Advanced Error Reporting Capability (100-137h)

Offset Address: 103-100h (BnD0F0)

Advanced Error Reporting Enhanced Capability Header

Default Value: 1401 0001h

Bit	Attribute	Default	Description
31:20	RO	140h	Next Capability Offset
19:16	RO	1h	Capability Version
15:0	RO	0001h	PCI Express Extended Capability ID

Offset Address: 107-104h (BnD0F0)

Uncorrectable Error Status

Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:21	—	0	Reserved
20	RW1CS	0	Unsupported Request Error Status (TL)
19	RW1CS	0	ECRC Error Status (TL)
18	RW1CS	0	Malformed TLP Status (TL)
17	RW1CS	0	Receiver Overflow Status (TL)
16	RW1CS	0	Unexpected Completion Status (TL)
15	RW1CS	0	Completer Abort Status (TL)
14	RW1CS	0	Completion Timeout Status (TL)
13	RW1CS	0	Flow Control Protocol Error Status (TL)
12	RW1CS	0	Poisoned TLP Status (TL)
11:5	—	0	Reserved
4	RW1CS	0	Data Link Protocol Error Status (DLL)
3:1	—	0	Reserved
0	RW1CS	0	Training Error Status (PHY)

Offset Address: 10B-108h (BnD0F0)

Uncorrectable Error Mask

Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:21	—	0	Reserved
20	RWS	0	Unsupported Request Error Mask (TL)
19	RWS	0	ECRC Error Mask (TL)
18	RWS	0	Malformed TLP Mask (TL)
17	RWS	0	Receiver Overflow Mask (TL)
16	RWS	0	Unexpected Completion Mask (TL)
15	RWS	0	Completed Abort Mask (TL)
14	RWS	0	Completion Timeout Mask (TL)
13	RWS	0	Flow Control Protocol Error Mask (TL)
12	RWS	0	Poisoned TLP Mask (TL)
11:5	—	0	Reserved
4	RWS	0	Data Link Protocol Error Mask (DLL)
3:1	—	0	Reserved
0	RWS	0	Training Error Mask (PHY)

Offset Address: 10F-10Ch (BnD0F0)
Uncorrectable Error Severity
Default Value: 0006 2011h

Bit	Attribute	Default	Description
31:21	—	0	Reserved
20	RWS	0	Unsupported Request Error Severity (TL)
19	RWS	0	ECRC Error Severity (TL)
18	RWS	1	Malformed TLP Severity (TL)
17	RWS	1	Receiver Overflow Error Severity (TL)
16	RWS	0	Unexpected Completion Error Severity (TL)
15	RWS	0	Completed Abort Error Severity (TL)
14	RWS	0	Completion Timeout Error Severity (TL)
13	RWS	1	Flow Control Protocol Error Severity (TL)
12	RWS	0	Poisoned TLP Severity (TL)
11:5	—	0	Reserved
4	RWS	1	Data Link Protocol Error Severity (DLL)
3:1	—	0	Reserved
0	RWS	1	Training Error Severity (PHY)

Offset Address: 113-110h (BnD0F0)
Correctable Error Status
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:13	—	0	Reserved
12	RW1CS	0	Replay Timer Timeout Status (DLL)
11:9	—	0	Reserved
8	RW1CS	0	REPLAY_NUM Rollover Status (DLL)
7	RW1CS	0	Bad DLLP Status (DLL)
6	RW1CS	0	Bad TLP Status (DLL)
5:1	—	0	Reserved
0	RW1CS	0	Receiver Error Status (PHY)

Offset Address: 117-114h (BnD0F0)
Correctable Error Mask
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:13	—	0	Reserved
12	RWS	0	Replay Timer Timeout Mask (DLL)
11:9	—	0	Reserved
8	RWS	0	REPLAY_NUM Rollover Mask (DLL)
7	RWS	0	Bad DLLP Mask (DLL)
6	RWS	0	Bad TLP Mask (DLL)
5:1	—	0	Reserved
0	RWS	0	Receiver Error Mask (PHY)

Offset Address: 11B-118h (BnD0F0)
Advanced Error Capabilities and Control
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:9	—	0	Reserved
8	RWS	0	ECRC Check Enable (TL)
7	RO	0	ECRC Check Capable (TL)
6	RWS	0	ECRC Generation Enable (TL)
5	RO	0	ECRC Generation Capable (TL)
4:0	ROS	0	First Error Pointer (TL)

Offset Address: 12B-11Ch (BnD0F0)
Header Log (TL)
Default Value: 00h

Register Offset Address	Attribute	Default	Description
11F - 11C	ROS	00h	Header Log Register 1st DW
123 - 120	ROS	00h	Header Log Register 2nd DW
127 - 124	ROS	00h	Header Log Register 3rd DW
12B - 128	ROS	00h	Header Log Register 4th DW

Offset Address: 12F-12Ch (BnD0F0)
Root Error Command
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:3	—	0	Reserved
2	RW	0	Fatal Error Reporting Enable
1	RW	0	Non-Fatal Error Reporting Enable
0	RW	0	Correctable Error Reporting Enable

Offset Address: 133-130h (BnD0F0)
Root Error Status
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:27	RO	00h	Advanced Error Interrupt Message Number (TL)
26:7	—	0	Reserved
6	RW1CS	0	Fatal Error Messages Received (TL)
5	RW1CS	0	Non-Fatal Error Messages Received (TL)
4	RW1CS	0	First Uncorrectable Fatal Error Message Received (TL) Set to 1 when the first Uncorrectable Error Message received is for a Fatal Error
3	RW1CS	0	Multiple ERR_FATAL/NONFATAL Received (TL)
2	RW1CS	0	ERR_FATAL/NONFATAL Received (TL)
1	RW1CS	0	Multiple ERR_COR Received (TL)
0	RW1CS	0	ERR_COR Received (TL)

Offset Address: 137-134h (BnD0F0)
Error Source Identification
Default Value: 0000 0000h

This register is updated regardless of the settings of Root Control register and the Root Error Command register.

Bit	Attribute	Default	Description
31:16	ROS	0000	ERR_FATAL/NONFATAL Source Identification (TL)
15:0	ROS	0000	ERR_COR Source Identification (TL)

Virtual Channel Capability (140-14Fh)

Virtual Channel Capability is defined for Egress direction of the device. For Root Port, since only VC0 is defined, there is no implementation of VC Arbitration Table and Port Arbitration Table.

Offset Address: 140-143h (BnD0F0)
Virtual Channel Enhanced Capability
Default Value: 1801 0002h

Bit	Attribute	Default	Description
31:20	RO	180h	Next Capability Offset
19:16	RO	1h	Capability Version
15:0	RO	0002h	PCI Express Extended Capability ID

Offset Address: 147-144h (BnD0F0)
Port VC Capability I
Default Value: 0000 0001h

Bit	Attribute	Default	Description	Mnemonic
31:12	—	0	Reserved	
11:10	RO	0	Port Arbitration Table Entry Size Reserved for root port	
9:8	RO	0	Reference Clock Reserved for root port	
7	—	0	Reserved	
6:4	RO	0	Low Priority Extended VC Count	
3	—	0	Reserved	
2:0	RO	1h	Extended VC Count	VCAEVCC PE0 [2:0]

Offset Address: 14B-148h (BnD0F0)
Port VC Capability II
Default Value: 0000 0001h

Bit	Attribute	Default	Description
31:24	RO	00h	VC Arbitration Table Offset 00 since only VC0 is defined
23:8	—	0	Reserved
7:0	RO	01h	VC Arbitration Capability

Offset Address: 14D-14Ch (BnD0F0)
Port VC Control
Default Value: 0000h

Bit	Attribute	Default	Description
15:4	—	0	Reserved
3:1	RW	0	VC Arbitration Select
0	RW	0	Load VC Arbitration Table

Offset Address: 14F-14Eh (BnD0F0)
Port VC Status
Default Value: 0000h

Bit	Attribute	Default	Description
15:1	—	0	Reserved
0	RO	0	VC Arbitration Table Status

VC0 Resource (150-15Bh)
Offset Address: 150-153h (BnD0F0)
VC Resource Capability (VC0)
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:24	RO	00h	Port Arbitration Table Offset (VC0)
23	—	0	Reserved
22:16	RO	00h	Maximum Time Slots (TL)
15	RO	0	Reject Snoop Transactions
14	RO	0	Advanced Packet Switching
13:8	—	0	Reserved
7:0	RO	00h	Port Arbitration Capability

Offset Address: 157-154h (BnD0F0)
VC Resource Control (VC0)
Default Value: 8000 00FFh

Bit	Attribute	Default	Description
31	RO	1	VC Enable
30:27	—	0	Reserved
26:24	RO	0	VC ID
23:20	—	0	Reserved
19:17	RW	0	Port Arbitration Select
16	RW	0	Load Port Arbitration Table
15:8	—	0	Reserved
7:0	RW Bit 0: RO	FFh	TC/VC Mapping This field indicates the TCs that are mapped to VC0. If bit [n] is 1, the corresponding traffic class TCn is mapped to VC0 (0 <= n <= 7). Default is TC0, TC1, TC2, TC3, C4, TC5, TC6 and TC7 are all mapped to VC0. Note: Bit0 is hardwired to 1 (i.e. TC0 is always mapped to VC0).

Offset Address: 15B-158h (BnD0F0)
VC Resource Status (VC0)
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:18	—	0	Reserved
17	RO	0	VC Negotiation Pending (TL)
16	RO	0	Port Arbitration Table Status
15:0	—	0	Reserved

VC1 Resource (15C-167h)

The following registers exist only when Rx144[0] is programmed to 1. If Rx144[0]=0, all the following content will be read as 0.

Offset Address: 15F-15Ch (BnD0F0)
VC Resource Capability (VC1)
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:24	RO	00h	Port Arbitration Table Offset (VC1)
23	—	0	Reserved
22:16	RO	00h	Maximum Time Slots (TL)
15	RO	0	Reject Snoop Transactions
14	RO	0	Advanced Packet Switching
13:8	—	0	Reserved
7:0	RO	00h	Port Arbitration Capability

Offset Address: 163-160h (BnD0F0)
VC Resource Control (VC1)
Default Value: 0100 0000h

Bit	Attribute	Default	Description
31	RW	0	VC Enable
30:27	—	0	Reserved
26:24	RW	1	VC ID
23:20	—	0	Reserved
19:17	RW	0	Port Arbitration Select
16	RW	0	Load Port Arbitration Table
15:8	—	0	Reserved
7:0	RW Bit 0: RO	00h	TC/VC Mapping This field indicates the TCs that are mapped to VC1. If bit [n] is 1, the corresponding traffic class TCn is mapped to VC1 (0 <= n <= 7). Default is TC0, TC1, TC2, TC3, C4, TC5, TC6 and TC7 are all mapped to VC0. Note: Bit0 is hardwired to 0 (i.e. TC0 is always mapped to VC0).

Offset Address: 167-164h (BnD0F0)
VC Resource Status (VC1)
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:18	—	0	Reserved
17	RO	0	VC Negotiation Pending (TL)
16	RO	0	Port Arbitration Table Status
15:0	—	0	Reserved

Root Complex Topology Capability (180-19Bh)
Offset Address: 183-180h (BnD0F0)
Root Complex Link Declaration Capabilities Header
Default Value: 0001 0005h

Bit	Attribute	Default	Description
31:20	RO	0	Next Capability
19:16	RO	1h	Capability Version
15:0	RO	005h	Capability ID

Offset Address: 187-184h (BnD0F0)
Element Self Description
Default Value: 0101 0100h

Bit	Attribute	Default	Description
31:24	RO	01h	Port Number (Root Port I)
23:16	RO	01h	Component ID This field returns the value of RRCRB_CID. It is in the same component as SB's RCRB.
15:8	RO	01h	Number of Link Entries
7:4	—	00h	Reserved
3:0	RO	00h	Element Type 000: Configuration space element 001: System egress port or internal sink 010: Internal root complex link

Offset Address: 193-190h (BnD0F0)
Upstream Link Descriptor
Default Value: 0001 0001h

Bit	Attribute	Default	Description
31:24	RO	00	Target Port Number Indicate the port number of RCRB
23:16	RO	01h	Target Component ID . The value of RCRB Index 104[23:16] (RRCRB_CID)
15:2	—	0	Reserved
1	RO	0	Link Type. Indicates the link points to RCRB
0	RO	1	Link Valid

Offset Address: 19B-194h (BnD0F0)
Upstream Link Base Address
Default Value: 0000 0000 0000 0000h

Bit	Attribute	Default	Description
63:32	RO	0	Base Address Upper The value of B0D19F0 Rx44-46 [23:20] (RXRCRBA_[35:32])
31:0	RO	0	Base Address Lower The value of B0D19F0 Rx44-46 [19:16] (RXRCRBA_[31:28])

Bus n Device 0 Function 1 (BnD0F1) – PCI Express Root Port 1 (PCI-to-PCI Virtual Bridge)

Bus n Device 0 Function 1, an optional 1-Lane PCI Express root port. Registers listed in this section are located in PCI configuration space and should be programmed using PCI configuration mechanism 1 through I/O registers CF8 / CFC with bus number n, device number 0 and function number 1. Registers over 256bytes, i.e. RX100~RXFFF, can be programmed by MMIO mechanism.

Header Registers (0-3Fh)

Offset Address	Attribute	Default	Description
1 – 0h	RO	1106h	Vendor ID
3 – 2h	RO	287Dh	Device ID

Offset Address: 5-4h (BnD0F1)

Command Register

Default Value: 0000h

Bit	Attribute	Default	Description
15:11	—	0	Reserved
10	RW	0	Interrupt Disabled Set when the device is prevented from generating INTx messages
9	—	0	Reserved
8	RW	0	SERR# Enable 0: Disable error report 1: Enable reporting of non-fatal and fatal errors
7	—	0	Reserved
6	RW	0	Parity Error Response 0: Ignore parity errors & continue 1: Take normal action on detected parity errors
5:3	—	0	Reserved
2	RW	0	Bus Master Enable 0: Disable 1: Enable Controls the ability to forward Memory and I/O Read/Write requests in the upstream direction. Disabling this bit disables MSI messages.
1	RW	0	Memory Space 0: Ignore downstream memory transactions; memory cycles with address falling in the claimed range will be forwarded to the PCI Bus 1: Enable downstream memory cycle to this port if its address falling in the claimed range of this device.
0	RW	0	I/O Space 0: Ignore downstream I/O transactions; I/O cycles with address falling in the claimed range will be forwarded to the PCI Bus. 1: Enable downstream I/O cycle to this port if its address falling in the claimed range of this device.

Offset Address: 7-6h (BnD0F1)
Status Register
Default Value: 0010h

Bit	Attribute	Default	Description
15	RW1C	0	Detected Parity Error This bit is set whenever a poisoned TLP is received, regardless the state of Parity Error Enabled (Rx4[6])
14	RW1C	0	Signaled System Error This bit is set when: A device sends an ERR_FATAL or ERR_NONFATAL message Rx4[8] = 1
13	RW1C	0	Received Master Abort This bit is set when receiving a completion with Unsupported Request Completion Status
12	RW1C	0	Received Target Abort This bit is set when receiving a completion with Completer Abort Completion Status
11	RW1C	0	Signaled Target Abort This bit is set when completing a Request with Completer Abort Completion Status
10:9	—	0	Reserved (Always 0)
8	RW1C	0	Master Data Parity Error This bit is set if Parity Error Enable bit (Rx4[6]) is set and either one of the following two conditions occurs: Requestor receives a Completion marked poisoned Requestor poisons a write Request
7:5	—	0	Reserved
4	RO	1	Capabilities List Indicates the presence of an extended capability list item. Always set to 1 for PCI Express device
3	RO	0	Interrupt Status Indicate an INTx message is pending internally (TL)
2:0	—	0	Reserved

Offset Address: 8h (BnD0F1)
Revision ID
Default Value: 00h

Bit	Attribute	Default	Description
7:0	RO	00h	Revision Code

Offset Address: 0B-9h (BnD0F1)
Class Code
Default Value: 060400h

Bit	Attribute	Default	Description
23:0	RO	060400h	Class Code

Offset Address: 0Ch (BnD0F1)
Cache Line Size
Default Value: 00h

Bit	Attribute	Default	Description
7:0	RO	00	Cache Line Size

Offset Address: 0Dh (BnD0F1)
Master Latency Timer
Default Value: 00h

Bit	Attribute	Default	Description
7:0	RO	00	Reserved (Hardwired to 0)

Offset Address: 0Eh (BnD0F1)
Header Type
Default Value: 81h

Bit	Attribute	Default	Description
7:0	RO	81h	Header Type Code A multiple function device.

Offset Address: 0Fh (BnD0F1)
Built In Self Test (BIST)
Default Value: 00h

Bit	Attribute	Default	Description
7:0	RO	0	BIST Support

Offset Address: 17-10h (BnD0F1)
Base Address Register
Default Value: 00h

Bit	Attribute	Default	Description
63:0	—	00h	Base Address Register

Offset Address: 18h (BnD0F1)
Primary Bus Number
Default Value: 00h

Bit	Attribute	Default	Description
7:0	RW	00h	Primary Bus Number

Offset Address: 19h (BnD0F1)
Secondary Bus Number
Default Value: 00h

Bit	Attribute	Default	Description
7:0	RW	00h	Secondary Bus Number

Offset Address: 1Ah (BnD0F1)
Subordinate Bus Number
Default Value: 00h

Bit	Attribute	Default	Description
7:0	RW	00h	Subordinate Bus Number

Offset Address: 1Bh (BnD0F1)
Subordinate Bus Number
Default Value: 00h

Bit	Attribute	Default	Description
7:0	RO	00h	Secondary Latency Timer, Reserved

Offset Address: 1Ch (BnD0F1)
I/O Base
Default Value: F0h

Bit	Attribute	Default	Description
7:4	RW	1111	I/O Base (AD[15:12] - inclusive) This bridge will forward the cycles from primary side to PCI if the IO address AD[15:12] is between IO base and IO limit (Rx1D)
3:0	RO	0	I/O Addressing Capability 0 means IO addressing is 16-bit only.

Offset Address: 1Dh (BnD0F1)
I/O Limit
Default Value: 00h

Bit	Attribute	Default	Description
7:4	RW	0	I/O Limit (AD[15:12] - inclusive) This bridge will forward the cycles from primary side to PCI if the IO address is between IO base (RX1C) and IO limit
3:0	RO	0	I/O Addressing Capability 0 means IO addressing is 16-bit only.

Offset Address: 1F-1Eh (BnD0F1)
Secondary Status
Default Value: 0000h

Bit	Attribute	Default	Description
15	RW1C	0	Detected Parity Error This bit is set when secondary side receives a poisoned TLP regardless of Rx4[6]
14	RW1C	0	Received System Error This bit is set when Rx4[8] is 1 and a device sends an ERR_FATAL or ERR_NONFATAL message.
13	RW1C	0	Received Master Abort
12	RW1C	0	Received Target Abort
11	RW1C	0	Signaled Target Abort
10:9	—	0	Reserved
8	RW1C	0	Master Data Parity Error This bit is set if Parity Error Enable bit (Rx4[6]) is set and either one of the following two conditions occurs: 1. Requestor receives a Completion marked poisoned. 2. Requestor poisons a write Request
7:0	—	0	Reserved

Offset Address: 21-20h (BnD0F1)
Memory Base
Default Value: FFF0h

Bit	Attribute	Default	Description
15:4	RW	FFFh	Memory Base (AD[31:20] – inclusive) The address [19:0] is not decoded.
3:0	RO	0000	Reserved

Offset Address: 23-22h (BnD0F1)
Memory Limit
Default Value: 0000h

Bit	Attribute	Default	Description
15:4	RW	000h	Memory Limit (AD[31:20] – inclusive) The address [19:0] is not decoded.
3:0	RO	0000	Reserved

Offset Address: 25-24h (BnD0F1)
Prefetchable Memory Base
Default Value: FFF0h

Bit	Attribute	Default	Description
15:4	RW	FFFh	Prefetchable Memory Base AD[31:20]
3:0	RO	0000	Reserved

Offset Address: 27-26h (BnD0F1)
Prefetchable Memory Limit
Default Value: 0000h

Bit	Attribute	Default	Description
15:4	RW	000h	Prefetchable Memory Limit AD[31:20]
3:0	RO	0000	Reserved

Offset Address: 2B-28h (BnD0F1)
Prefetchable Memory Upper Base
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:4	RO	00h	Reserved
3:0	RW	0000	AD[35:32] This chip supports up to 16G

Offset Address: 2F-2Ch (BnD0F1)
Prefetchable Memory Upper Limit
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:4	RO	00h	Reserved
3:0	RW	0000	AD[35:32] This chip supports up to 16G

Offset Address: 31-30h (BnD0F1)
I/O Base Upper
Default Value: 0000h

Bit	Attribute	Default	Description
15:0	RO	00h	I/O Base Upper 16 bits Address

Offset Address: 33-32h (BnD0F1)
I/O Base Limit
Default Value: 0000h

Bit	Attribute	Default	Description
15:0	RO	00h	I/O Limit Upper 16 bits Address

Offset Address: 34h (BnD0F1)
Capability Pointer
Default Value: 40h

Contains an offset from the start of configuration space.

Bit	Attribute	Default	Description
7:0	RO	40h	Capability Pointer Always reads 40h. Capability Pointer link list: Rx34 → Rx40 → Rx68 → Rx70 → NULL

Offset Address: 3Ch (BnD0F1)
Interrupt Line
Default Value: 00h

Bit	Attribute	Default	Description
7:0	RW	00h	INT Line (For Software Use Only)

Offset Address: 3Dh (BnD0F1)
Interrupt Pin
Default Value: 01h

Bit	Attribute	Default	Description
7:0	RO	01h	INT Pin 01: INTA

Offset Address: 3F-3Eh (BnD0F1)
Bridge Control
Default Value: 0000h

Bit	Attribute	Default	Description
15:7	—	00h	Reserved
6	RW	0	Secondary Bus Reset 0: No reset 1: Triggers a warm reset on the corresponding PCI Express Port
5	—	0	Reserved
4	RW	0	Base VGA 16 bits Decode 0: All VGA alias range will be forwarded 1: Only forward base VGA range (Aliased range will not be forwarded)
3	RW	0	VGA Compatible I/O and Memory Address Range 0: Do not forward VGA compatible memory and I/O 1: Forward VGA compatible memory and I/O Note: VGA addresses are memory A0000-BFFFFh and I/O addresses 3B0-3BBh, 3C0-3CFh and 3D0-3DFh (10-bit decode). "Mono" text mode uses B0000-B7FFFh and "Color" Text Mode uses B8000-BFFFFh. Graphics modes use Axxxxh. Mono VGA uses I/O addresses 3Bx-3Cxh and Color VGA uses 3Cx-3Dxh. If an MDA is present, a VGA will not use the 3Bxh I/O addresses and B0000-B7FFFh memory space; if not, the VGA will use those addresses to emulate MDA modes.
2	RW	0	Block/Forward ISA I/O Cycles 0: Forward all I/O cycles with address in the range defined by the I/O Base and I/O Limit 1: Do not forward ISA I/O that are in the top 768 bytes of each 1K byte block address range
1	RW	0	SERR Enable Controls the forwarding of ERR_COR, ERR_NONFATAL and ERR_FATAL from secondary to primary 0: Disable 1: Enable
0	RW	0	Parity Error Response Enable 0: Ignore the response to poisoned TLPs 1: Enable the response to poisoned TLPs

PCI Express Capability Registers (40-63h)
Offset Address: 41-40h (BnD0F1)
PCI Express List
Default Value: 6810h

Bit	Attribute	Default	Description
15:8	RO	68h	Next Pointer
7:0	RO	10h	Capability ID

Offset Address: 43-42h (BnD0F1)
PCI Express Capabilities
Default Value: 0041h

Bit	Attribute	Default	Description
15:14	—	0	Reserved
13:9	RO	0	Interrupt Message Number
8	RO	0	Slot Implemented This bit when set indicates that the PCI Express Link associated with this Port is connected to a slot (as compared to being connected to an integrated component or being disabled).
7:4	RO	0100	Device / Port Type 0100b: Root Port of PCI Express Root Complex
3:0	RO	1	Capability Version

Offset Address: 47-44h (BnD0F1)
Device Capabilities
Default Value: 0000 0nn1h

Bit	Attribute	Default	Description
31:28	—	0	Reserved
27:26	RO	0	Captured Slot Power Limit Scale
25:18	RO	0	Captured Slot Power Limit Value
17:15	—	000	Reserved
14	RO	0	Power Indicator Present
13	RO	0	Attention Indicator Present
12	RO	0	Attention Button Present
11:9	RO	111	Endpoint L1 Acceptable Latency 111b: more than 64us
8:6	RO	HwInit	Endpoint L0s Acceptable Latency
5	RO	0	Extended Tag Field Supported 0: 5-bit Tag field supported 1: 8-bit Tag field supported
4:3	RO	00	Phantom Functions Supported
2:0	RO	001	Max Payload Size Supported 001b: 32QW (256 bytes)

Offset Address: 49-48h (BnD0F1)
Device Control
Default Value: 0000h

Bit	Attribute	Default	Description
15	—	0	Reserved
14:12	RO	000	Max Read Request Size 000b: 128 bytes This field sets the maximum Read Request size for the device as a Requestor.
11	RO	0	Enable No Snoop If this bit is set to 1, the device is permitted to set the No Snoop bit in the Requestor Attributes of the transactions it initiate that do not require hardware enforced cache coherency.
10	RO	0	Auxiliary Power PM Enable This bit when set enables device to draw AUX power independent of PME AUX power.
9	RO	0	Phantom Functions Enable Not supported.
8	RO	0	Extended Tag Field Enable Not supported.
7:5	RW	0	Max Payload Size Maximum TLP payload size.
4	RW	0	Enable Relaxed Ordering If this bit is set to 1, the device is permitted to set the Relaxed Ordering bit in the Requestor Attributes of the transactions it initiate that do not require strong write ordering.
3	RW	0	Unsupported Request Reporting Enable
2	RW	0	Fatal Error Reporting Enable For a Root Port, the reporting of Fatal errors is internal to the root. No external ERR_FATAL message is generated.
1	RW	0	Non-Fatal Error Reporting Enable For a Root Port, the reporting of Non-Fatal errors is internal to the root. No external ERR_NONFATAL message is generated.
0	RW	0	Correctable Error Reporting Enable For a Root Port, the reporting of correctable errors is internal to the root. No external ERR_COR message is generated.

Offset Address: 4B-4Ah (BnD0F1)
Device Status
Default Value: 0010h

Bit	Attribute	Default	Description
15:6	—	0	Reserved
5	RO	0	Transactions Pending This bit when set indicates that the Port has issued Non-Posted Requests on its own behalf (using the Port's own Requestor ID) which have not been completed.
4	RO	1	AUX Power Detected
3	RWIC	0	Unsupported Request Detected
2	RWIC	0	Fatal Error Detected (TL)
1	RWIC	0	Non-Fatal Error Detected (TL)
0	RWIC	0	Correctable Error Detected (TL)

Offset Address: 4F-4Ch (BnD0F1)
Link Capabilities
Default Value: 0200 0C11h

Bit	Attribute	Default	Description
31:24	RO	02h	Port Number This field indicates the PCI Express Port number for the given PCI Express Link.
23:18	—	0	Reserved
17:15	RO	000	L1 Exit Latency 000: less than 1us. The value reported indicates the length of time this Port requires to complete transition from L1 to L0.
14:12	RO	000	L0s Exit Latency 000: less than 64ns. The value reported indicates the length of time this Port requires to complete transition from L0s to L0.
11:10	RO	11	Active State Link PM (ASPM) Support 11b: L0s and L1 supported. This field indicates the level of ASPM supported on the PCI Express Link.
9:4	RO	01h	Maximum Link Width 010000: x16 Link width 0000001b: x1 Link width
3:0	RO	1	Maximum Link Speed 0001b: 2.5Gb/s Link speed

Offset Address: 51-50h (BnD0F1)
Link Control
Default Value: 0000h

Bit	Attribute	Default	Description
15:8	—	0	Reserved
7	RW	0	Extended Synch 0: FCU Timer limit is 30us 1: FCU Timer limit is 120us
6	RW	0	Common Clock Configuration 0: Indicates that this Port and the component on the opposite end of the Link are operating with asynchronous reference clock. 1: Indicates that this Port and the component on the opposite end of the Link are operating with a distributed common reference clock.
5	RW	0	Retrain Link A write of 1 to this bit initiates Link retrained by directing the Physical Layer LTSSM to the Recovery state.
4	RW	0	Link Disable This bit disables the Link when set to 1.
3	RO	0	Read Completion Boundary 0: 64 byte
2	—	0	Reserved
1:0	RW	00	Link Active State PM (ASPM) Control 00b: Disabled 01b: L0s Entry Enabled 10b: L1 Entry Enabled 11b: L0s and L1 Entry Enabled

Offset Address: 53-52h (BnD0F1)
Link Status
Default Value: 0nn1h

Bit	Attribute	Default	Description
15:13	—	0	Reserved
12	RO	0	Slot Clock Configuration 0: Use an independent clock irrespective of the presence of a reference on the connector. 1: Use the same physical reference clock that the platform provides on the connector.
11	RO	0	Link Training This bit indicated that Link training is in progress (Physical Layer LTSSM is in Configuration or Recovery state) or that 1b was written to the Retrain Link bit but Link training has not yet begun. Hardware clears this bit once Link training is complete.
10	RO	0	Training Error Set when a Link training error occurred. Cleared by hardware upon successfully training of the Link to the L0 Link state.
9:4	RO	xxxxxx	Negotiated Link Width 000001: x1 000010: x2 000100: x4 001000: x8 010000: x16
3:0	RO	0001	Link Speed 0001: 2.5Gb/s negotiated Link speed.

Offset Address: 57-54h (BnD0F1)

Slot Capabilities

Default Value: 0000 0060h

Bit	Attribute	Default	Description
31:19	RO	00h	Physical Slot Number Physical slot number attached to the Port.
18:17	—	0	Reserved
16:15	RO	0	Slot Power Limit Scale Write to the field causes the Port to send the Set_Slot_Power_Limit message.
14:7	RO	00h	Slot Power Limit Value Write to the field causes the Port to send the Set_Slot_Power_Limit message.
6	RO	1	Hot-plug Capable
5	RO	1	Hot-plug Surprise
4	RO	0	Power Indicator Present
3	RO	0	Attention Indicator Present
2	RO	0	MRL Sensor Present
1	RO	0	Power Controller Present
0	RO	0	Attention Button Present

Offset Address: 59-58h (BnD0F1)

Slot Control

Default Value: 0000h

Offset Address: 5A-5Bh (BnD0F1)

Slot Status

Default Value: 0000h

Bit	Attribute	Default	Description
15:7	—	0	Reserved
6	RO	0	Presence Detect State 0: Slot empty 1: Card present in slot
5	RO	0	MRL Sensor State
4	RW1C	0	Command Completed
3	RW1C	0	Presence Detect Changed
2	RO	0	MRL Sensor Changed
1	RO	0	Power Fault Detected
0	RW1C	0	Attention Button Pressed

Offset Address: 5D-5Ch (BnD0F1)
Root Control
Default Value: 0000h

Bit	Attribute	Default	Description
15:4	—	0	Reserved
3	RW	0	PME Interrupt Enable 0: Disable 1: Enable interrupt generation upon receipt of a PME message as reflected in the PME status register bit. A PME interrupt is also generated if the PME status register bit is set when this bit is set from a cleared state.
2	RW	0	System Error on Fatal Error Enable 0: Disable 1: Enable generation of a System Error if a Fatal Error (ERR_FATAL) is reported by any of the devices in the hierarchy associated with the Root Port, or by the Root Port itself.
1	RW	0	System Error on Non-Fatal Error Enable 0: Disable 1: Enable generation of a System Error if a Non-Fatal Error (ERR_NONFATAL) is reported by any of the devices in the hierarchy associated with the Root Port, or by the Root Port itself.
0	RW	0	System Error on Correctable Error Enable 0: Disable 1: Enable generation of a System Error if a Correctable Error (ERR_COR) is reported by any of the devices in the hierarchy associated with the Root Port, or by the Root Port itself.

Offset Address: 63-60h (BnD0F1)
Root Status
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:18	—	0	Reserved
17	RO	0	PME Pending 0: No pending PME 1: Indicates that another PME is pending when the PME Status (bit 16) is set.
16	RW1C	0	PME Status Indicates that the PME was asserted by the Requestor ID indicated in PME Requestor ID (bit[15:0]).
15:0	RO	00h	PME Requestor ID The Requestor ID of the last PME Requestor.

PCI Power Management Capability Structure Registers (68-6Fh)
Offset Address: 6B-68h (BnD0F1)
Power Management Capabilities
Default Value: C802 7001h

Bit	Attribute	Default	Description
31:27	RW	11001	PME Support Bit 31, 30 and 27 are set to 1b (PME Message will be forwarded).
26	RW	0	D2 Support
25	RW	0	D1 Support
24:22	RO	0	AUX Current
21	RW	0	Device Specific Initialization
20:19	—	0	Reserved
18:16	RO	010	Version
15:8	RO	70h	Next Capability Pointer
7:0	RO	01h	Capability ID

Offset Address: 6F-6Ch (BnD0F1)
Power Management Status/Control
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:24	RO	00h	Power Management Data
23:16	RO	—	Reserved
15	RW1CS	0	PME Status This bit's setting is not modified by hot, warm, or cold reset.
14:13	RO	0	Data Scale
12:9	RO	0	Data Select
8	RWS	0	PME Enable This bit's setting is not modified by hot, warm, or cold reset.
7:2	RO	0	Reserved
1:0	RW	0	Power State

PCI Message Signal Interrupt (MSI) Capability Structure Registers (70-87h)
Offset Address: 73-70h (BnD0F1)
MSI Capability Support
Default Value: 0180 0005h

Bit	Attribute	Default	Description
31:25	—	0	Reserved
24	RW	1	This MSI capability supports pre-vector masking capability
23	RO	1	This MSI Capability Supports 64 bit Message Address Only
22:20	RW	000	Multiple Message Enable 000: 1 message allocated 010: 4 message allocated 100: 16 message allocated 11x: Reserved 001: 2 message allocated 011: 8 message allocated 101: 32 message allocated
19:17	RO	000	Multiple Message Capable 000: 1 message requested 010: 4 message allocated 100: 16 message requested 11x: Reserved 001: 2 message requested 011: 8 message allocated 101: 32 message requested
16	RW	0	MSI Enable 0: This Port is prohibited from using MSI to request service 1: This Port is permitted to use MSI to request service.
15:8	RO	00h	Next Capability Pointer
7:0	RO	05h	Capability ID

Offset Address: 77-74h (BnD0F1)
System-Specified Message Address - Low
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:2	RW	00h	System-Specified Message Address Bit [31:2]
1:0	RO	00	System-Specified Message Address Bit [1:0] These bits will always read as 0

Offset Address: 7B-78h (BnD0F1)
System-Specified Message Address - High
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:4	RO	00h	System-Specified Message Address Bit [63:36] These bits will always read as 0 since this chip supports address up to A35.
3:0	RW	0	System-Specified Message Address Bit [35:32]

Offset Address: 7D-7Ch (BnD0F1)
Message Data
Default Value: 0000h

Bit	Attribute	Default	Description
15:0	RW	0	Message Data The message data is to be put on data [15:0] of MSI cycles

Offset Address: 83-80h (BnD0F1)
Message Mask Control
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:1	RO	00h	Mask Bit
0	RW	0	Mask Bit for Message 0

Offset Address: 87-84h (BnD0F1)
Message Pending Status
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:1	RO	00h	Pending Bit
0	RO	0	Pending Bit for Message 0

PCI Express Transaction Layer Registers (A0-A4h)
Offset Address: A0h (BnD0F1)
Downstream Control I
Default Value: 01h

Bit	Attribute	Default	Description
7	RW	0	Downstream Cycles Have Traffic Class TC1 0: Disabled 1: Enabled.
6	RW	0	Downstream Cycles Have Attribute “No Snoop” Set 0: Disabled 1: Enabled.
5	RW	0	Downstream Cycles Have Attribute “Relaxed Ordering” Set 0: Disabled 1: Enabled.
4	RW	0	Downstream Lock Cycle Support 0: Disabled 1: Enabled.
3	RW	0	Downstream Arbitration Scheme 0: Fixed priority: VC1 CPL > VC0 CPL > Down Stream Command 1: Round Robin arbitration priority between VC1 CPL, VC0 CPL and Down Stream Command
2	RW	0	Downstream Post-Write Allowed to Pass IOW 0: Not allowed. 1: Allowed.
1	RW	0	Downstream Post-Write Allowed to Pass Read 0: Not allowed. 1: Allowed.
0	RW	1	Downstream Pipeline 0: Disabled 1: Enabled.

Offset Address: A1h (BnD0F1)
Downstream Control II
Default Value: 04h

Bit	Attribute	Default	Description
7	RWIC	0	Downstream Configuration Completion Status 0: Normal completion. 1: At least one configuration request ended with a CRS (Configuration Request Retry Status) completion.
6:4	—	0	Reserved
3	RW	0	C2P Read Completion Timer for Vector Development Mode: When this bit is set to 1, the timer defined in RxA1[2:0] becomes: 0xx: 1us 1xx: 3us
2:0	RW	100	C2P Read Completion Timeout Timer 000: Reserved 001: 1ms 010: Reserved 011: 10ms (Spec. lower bound) 100: 30ms 101: 50ms (Spec. higher bound) 110: 100ms 111: Reserved

Offset Address: A4h (BnD0F1)
Upstream Control
Default Value: 10h

Bit	Attribute	Default	Description
7	RW	0	Upstream Address A35~A31 Forced to 0 0: Disabled 1: Enabled for system testing or loop back mode test. The upcoming data may be checked in the system memory
6	RW	0	Prevent Upstream Write FIFO from Being Overwritten
5	RW	0	Upstream Checking Malformed TLP through “Byte Enable Rule” And “Over 4K Boundary Rule” 0: Disabled 1: Enabled
4	RW	1	Downstream Read Wait Till The Upstream Write Data Flushed 0: Disabled 1: Enabled
3:2	—	0	Reserved
1	RW	0	VC1 was not existed in the capability header (software have to program RX144[0] = 0), but Transaction Layer is allowed to map Non-Snoop upstream request to the VC1 request queue output to the PXPTRF. Note that when this bit is 1, the RXA4[0] have to be 0. 0: Disabled 1: Enabled
0	RW	0	Virtual Change 1 Disable. VC1’s data FIFO will be used for VC0. 0: DATA FIFO of VC1 used by VC1 1: DATA FIFO of VC1 used by VC0, the DATA FIFO of VC0 become 2 times larger.

PCI Express Data Link Layer Registers (B0-B6h)
Offset Address: B0h (BnD0F1)
Ack/Nak Latency Timer Limit
Default Value: 3Bh

Bit	Attribute	Default	Description	Mnemonic
7:0	RW	3Bh	Timer Limit for Ack/Nak Latency Timer and Update FC Latency Timer (in unit of 250MHz) 00: 4 x 1 Clocks 02: 4 x 3 Clocks. 0n: 4 x (n+1) Clocks	RACKLTLM_PE1[7:0]

Offset Address: B1h (BnD0F1)
Replay Timer Limit
Default Value: 59h

Bit	Attribute	Default	Description
7:0	RW	59h	Replay Timer Limit (In unit of 250MHz) 00: 8 x 1 Clocks 02: 8 x 3 Clocks 0n: 8 x (n+1) Clocks

Offset Address: B2h (BnD0F1)
FCU Control and Status
Default Value: 40h

Bit	Attribute	Default	Description
7	RO	0	FCU Timeout Status 1 means the FCU timeout has occurred
6	RW	1	FCU Receive Timer Enable Control 0: Disable the timeout mechanism 1: Enable the timeout mechanism
5	RW	0	FCU Receive Timer Limit 0: Timeout limit of 200us 1: Timeout limit of 300us
4	RW	0	FCU Receive Timer Reset Control 0: Timer reset by FCI/FCU only 1: Timer reset by any received DLLPs
3:1	—	0	Reserved
0	RW	0	DL & TL Reset Upstream Related Logic When Retrain Is Going On.

Offset Address: B3h (BnD0F1)
Replay Timer Control
Default Value: 10h

Bit	Attribute	Default	Description
7:6	RW	10	Replay Timer Control while Rewind (resend those DLLPs which do not have corresponding ACK/NAK received) 00: Hold Replay Timer during rewind. 01: During rewind, if ACK/NAK comes in, reset and hold the Replay Timer. 10: During rewind, reset and hold the Replay Timer as long as the Retry Buffer is empty. 11: Reserved.
5:3	—	0	Reserved
2:0	RW	000	Count of Replay Timer Expired During RXL0s (Receiving Physical in L0s state) Before Resend the TLP When Rx50[7], LCES_PE1, is set to 0: 000: Wait forever for the Acknowledge from the device side 001: Resend the TLP after 1 x Replay timer expired 010: Resend the TLP after 2 x Replay timer expired 011: Resend the TLP after 4 x Replay timer expired 100: Resend the TLP after 8 x Replay timer expired 101: Resend the TLP after 16 x Replay timer expired 110: Resend the TLP after 32 x Replay timer expired 111: Resend the TLP after 64 x Replay timer expired When RX50[7], LCES_PE1, is set to 1: 000: Wait forever for the Acknowledge from the device side 001: Resend the TLP after 16 x Replay timer expired 010: Resend the TLP after 32 x Replay timer expired 011: Resend the TLP after 64 x Replay timer expired 100: Resend the TLP after 128 x Replay timer expired 101: Resend the TLP after 256 x Replay timer expired 110: Resend the TLP after 512 x Replay timer expired 111: Resend the TLP after 1024 x Replay timer expired

Offset Address: B4h (BnD0F1)
Arbitration Control
Default Value: 00h

Bit	Attribute	Default	Description
7:4	—	0	Reserved
3	RW	0	TLP vs. Flow Control Initialization for VC0 in Arbitration Priority 0: TLP is not allowed to pass FCI2 for VC0 1: TLP is allowed to pass FCI2 for VC0
2:0	RW	000	Data Link TX Packets Arbitration Scheme 000: Round Robin 001: Reserved. 010: Strict priority: TLP > ACK/NAK > FCU 011: Strict priority: TLP > FCU > ACK/NAK 100: Strict priority: ACK/NAK > TLP > FCU 101: Strict priority: ACK/NAK > FCU > TLP 110: Strict priority: FCU > TLP > ACK/NAK 111: Strict priority: FCU > ACK/NAK > TLP

Offset Address: B5h (BnD0F1)
FCU Control
Default Value: 00h

Bit	Attribute	Default	Description
7	—	0	Reserved
6	RW	0	FCU (Flow Control Unit) Timer Control 0: Update flow control credit when either Transaction Layer requested packets being sent or when FCU timer expired 1: Update flow control credit only when FCU timer expired
5:4	RW	00	ACK DLLP Collapse Method 00: Send ACK when the latency timer RACKLTLM (RxB0) expired. 01: Send ACK every 4 correct TLP has been received 10: Send ACK every 8 correct TLP has been received 11: Send ACK every 16 correct TLP has been received
3:2	—	0	Reserved
1	RW	0	FCI (Flow Control Initialization) Process End Condition 0: Complete FCI process when TLP/FCU has been received 1: Do not complete FCI process even when TLP/FCU has been received
0	RW	0	VC1 FCI DLLP Transmission Scheme 0: Transmit FCI DLLP only when FCI timer expired 1: Transmit FCI DLLP continuously as long as the FCI process is not finished

Offset Address: B6h (BnD0F1)
Transaction / Link Layer Checking Control
Default Value: 03h

Bit	Attribute	Default	Description
7:5	—	0	Reserved
4	RW	0	VC Negotiate Pending Control for VC1 0: Assert VC negotiation pending after VC1 is enabled 1: Assert VC negotiation pending after RESET is de-asserted
3	—	0	Reserved
2	RW	0	ECRC Checking Control for the Case of TD equals to1 but no ECRC field in TLP 0: Ignore the error 1: Report error to Transaction Layer, which will mark the TLP as a Malformed TLP
1	RW	1	Length Malform Report Control 0: Do not report length malform to Transaction Layer 1: Report length malform to Transaction Layer
0	RW	1	LCRC Checking Control 0: Do not check LCRC 1: Check LCRC

PCI Express Physical Layer Registers (C0-C7h)
Offset Address: C3-C0h (BnD0F1)
PHY Control
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:8	—	0	Reserved
7	RW	0	Quick Timeout Counter Setting When set to 1, The following timeout will be shorter when set: TIMEOUT_2MS → TIMEOUT_4US TIMEOUT_12MS → TIMEOUT_24US TIMEOUT_24MS → TIMEOUT_48US TIMEOUT_48MS → TIMEOUT_96US TIMEOUT_1024TS → TIMEOUT_32TS
6	RW	0	Disable Data Scrambling/Descrambling 0: Enable 1: Disable
5:3	RW	000	Loopback Mode Selection This setting is applied to Lane 1 000 : No loop back 001: PHYLS loopback from TX end to RX end 010: PHYES loopback from TX end to RX end 011: Reserved 100: Reserved 101: PHYLS loopback from RX end to TX end 110: PHYES loopback from RX end to TX end 111: Reserved
2:0	—	0	Reserved

Offset Address: C7-C4h (BnD0F1)
Elastic Buffer Base Registers for Lane 0
Default Value: 0000 0004h

Bit	Attribute	Default	Description
31:3	—	0	Reserved
2:0	RW	4	Elastic Buffer Base Register for Lane 0 0, 1, 7: Illegal values Others: delay numbers of T for elastic buffer operations

PCI Express Power Management Module Registers (D0-D3h)
Offset Address: D3-D0h (BnD0F1)
PMC Control
Default Value: 0000 0050h

Bit	Attribute	Default	Description	Mnemonic
31:24	RW	00h	Idle Period for Entering ASL1 Minimum time period is 128ns 00: 128ns 02: 3x128ns FF: 256x128ns	01: 2x128ns
23:16	RW	00h	Idle Period for Entering L0s Minimum time period is 128ns (LOSLIM_PE1 = 00) 00: 128ns 02: 3x128ns FF: 256x128ns	01: 2x128ns
15	RW1C	0	Error Status Report This bit is set when device cannot have electrical idle after the waiting period programmed at RxDI[6:4] expired.	
14	—	0	Reserved	
13:12	RW	0	Electrical Idle Waiting Period before Move to L1 State (after issue ACK to the L1 request from the device). 00: Always wait for electrical idle 10: Wait 64 clock	01: Wait 32 clock 11: Reserved
11:10	—	0	Reserved	
9:8	RW	0	Downstream Cycles Triggered C2P Cycles, Period of Staying at L0 Before Returned to L1 for PHY (when PMU is in non-D0 state) 00: Immediately 01: 1 cfgW or message + delay10T 10: 1 32QW +1cfgW or message+ delay10T 11: 2 32QW +1 cfgW or message +delay10T	
7	—	0	Reserved	
6:4	RW	101	Timeout Timer Period This timer is used when waiting for ACK from a device after issued PME_TURNOFF message to notify the device to move to power down mode. 000: 1us 010: 4us 100: 16us 110: 64us	001: 2us 011: 8us 101: 32us 111: 128us
3:2	—	0	Reserved	
1	RW	0	Link Loopback 0: Normal operation 1: Direct device to enter Loopback mode, receiving data in the device will be sent to the transmit side	
0	RW	0	LTSSM State During Link Reconfigure Link Width 0: When reconfigure link width, LTSSM must be in Detect state 1: When reconfigure link width, LTSSM can be in Configuration state	

PCI Express Message Controller Related Registers (D8h)
Offset Address: D8h (BnD0F1)
PMC Express Message Status
Default Value: 00h

Bit	Attribute	Default	Description
7	RW1C	0	Excessive Errors Happened Occurred But Not Reported in The MSGC 0: Normal operation. 1: There are errors not reported to the system
6:0	—	0	Reserved

PCI Express Electrical PHY Registers (E1h)
Offset Address: E1h (BnD0F1)
PHYES Module Related Control
Default Value: 08h

Bit	Attribute	Default	Description
7:5	—	0	Reserved
4	RW	0	Receiving Polarity Change Control 0: Have the same polarity on the loop-back/received data. 1: Have reverse polarity on the loop-back/received data.
3:2	RW	10	Squelch Window Select. (64-175mv)
1	RW	0	Electrical Idle State Exit Condition: Number of Non Idle Signal Detected Before Exit Idle State 0: 2 bits. 1: 10 bits.
0	RW	0	Electrical Idle State Enter Condition: Number of Idle Signal Detected Before Enter Idle State 0: 2 bits 1: 10 bits

Bus n Device 0 Function 1 (BnD0F1) – PCI Express Root Port 1 Extended Space

Registers defined in the Extended Space can be accessed through PCI Express Enhanced Configuration Access Mechanism, which utilizes a flat memory-mapped address space to access the configuration registers. Please check PCI Express Specification for the detail information.

Advanced Error Reporting Capability (100-137h)

Offset Address: 103-100h (BnD0F1)

Advanced Error Reporting Enhanced Capability Header

Default Value: 1401 0001h

Bit	Attribute	Default	Description
31:20	RO	140h	Next Capability Offset
19:16	RO	1h	Capability Version
15:0	RO	0001h	PCI Express Extended Capability ID

Offset Address: 107-104h (BnD0F1)

Uncorrectable Error Status

Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:21	—	0	Reserved
20	RW1CS	0	Unsupported Request Error Status (TL)
19	RW1CS	0	ECRC Error Status (TL)
18	RW1CS	0	Malformed TLP Status (TL)
17	RW1CS	0	Receiver Overflow Status (TL)
16	RW1CS	0	Unexpected Completion Status (TL)
15	RW1CS	0	Completer Abort Status (TL)
14	RW1CS	0	Completion Timeout Status (TL)
13	RW1CS	0	Flow Control Protocol Error Status (TL)
12	RW1CS	0	Poisoned TLP Status (TL)
11:5	—	0	Reserved
4	RW1CS	0	Data Link Protocol Error Status (DLL)
3:1	—	0	Reserved
0	RW1CS	0	Training Error Status (PHY)

Offset Address: 10B-108h (BnD0F1)

Uncorrectable Error Mask

Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:21	—	0	Reserved
20	RWS	0	Unsupported Request Error Mask (TL)
19	RWS	0	ECRC Error Mask (TL)
18	RWS	0	Malformed TLP Mask (TL)
17	RWS	0	Receiver Overflow Mask (TL)
16	RWS	0	Unexpected Completion Mask (TL)
15	RWS	0	Completed Abort Mask (TL)
14	RWS	0	Completion Timeout Mask (TL)
13	RWS	0	Flow Control Protocol Error Mask (TL)
12	RWS	0	Poisoned TLP Mask (TL)
11:5	—	0	Reserved
4	RWS	0	Data Link Protocol Error Mask (DLL)
3:1	—	0	Reserved
0	RWS	0	Training Error Mask (PHY)

Offset Address: 10F-10Ch (BnD0F1)
Uncorrectable Error Severity
Default Value: 0006 2011h

Bit	Attribute	Default	Description
31:21	—	0	Reserved
20	RWS	0	Unsupported Request Error Severity (TL)
19	RWS	0	ECRC Error Severity (TL)
18	RWS	1	Malformed TLP Severity (TL)
17	RWS	1	Receiver Overflow Error Severity (TL)
16	RWS	0	Unexpected Completion Error Severity (TL)
15	RWS	0	Completed Abort Error Severity (TL)
14	RWS	0	Completion Timeout Error Severity (TL)
13	RWS	1	Flow Control Protocol Error Severity (TL)
12	RWS	0	Poisoned TLP Severity (TL)
11:5	—	0	Reserved
4	RWS	1	Data Link Protocol Error Severity (DLL)
3:1	—	0	Reserved
0	RWS	1	Training Error Severity (PHY)

Offset Address: 113-110h (BnD0F1)
Correctable Error Status
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:13	—	0	Reserved
12	RW1CS	0	Replay Timer Timeout Status (DLL)
11:9	—	0	Reserved
8	RW1CS	0	REPLAY_NUM Rollover Status (DLL)
7	RW1CS	0	Bad DLLP Status (DLL)
6	RW1CS	0	Bad TLP Status (DLL)
5:1	—	0	Reserved
0	RW1CS	0	Receiver Error Status (PHY)

Offset Address: 117-114h (BnD0F1)
Correctable Error Mask
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:13	—	0	Reserved
12	RWS	0	Replay Timer Timeout Mask (DLL)
11:9	—	0	Reserved
8	RWS	0	REPLAY_NUM Rollover Mask (DLL)
7	RWS	0	Bad DLLP Mask (DLL)
6	RWS	0	Bad TLP Mask (DLL)
5:1	—	0	Reserved
0	RWS	0	Receiver Error Mask (PHY)

Offset Address: 11B-118h (BnD0F1)
Advanced Error Capabilities and Control
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:9	—	0	Reserved
8	RWS	0	ECRC Check Enable (TL)
7	RO	0	ECRC Check Capable (TL)
6	RWS	0	ECRC Generation Enable (TL)
5	RO	0	ECRC Generation Capable (TL)
4:0	ROS	0	First Error Pointer (TL)

Offset Address: 12B-11Ch (BnD0F1)
Header Log (TL)

Register Offset Address	Attribute	Default	Description
11F - 11C	ROS	00h	Header Log Register 1st DW
123 - 120	ROS	00h	Header Log Register 2nd DW
127 - 124	ROS	00h	Header Log Register 3rd DW
12B - 128	ROS	00h	Header Log Register 4th DW

Offset Address: 12F-12Ch (BnD0F1)
Root Error Command
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:3	—	0	Reserved
2	RW	0	Fatal Error Reporting Enable
1	RW	0	Non-Fatal Error Reporting Enable
0	RW	0	Correctable Error Reporting Enable

Offset Address: 133-130h (BnD0F1)
Root Error Status
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:27	RO	00h	Advanced Error Interrupt Message Number (TL)
26:7	—	0	Reserved
6	RW1CS	0	Fatal Error Messages Received (TL)
5	RW1CS	0	Non-Fatal Error Messages Received (TL)
4	RW1CS	0	First Uncorrectable Fatal Error Message Received (TL) Set to 1 when the first Uncorrectable Error Message received is for a Fatal Error
3	RW1CS	0	Multiple ERR_FATAL/NONFATAL Received (TL)
2	RW1CS	0	ERR_FATAL/NONFATAL Received (TL)
1	RW1CS	0	Multiple ERR_COR Received (TL)
0	RW1CS	0	ERR_COR Received (TL)

Offset Address: 137-134h (BnD0F1)
Error Source Identification
Default Value: 0000 0000h

This register is updated regardless of the settings of Root Control register and the Root Error Command register

Bit	Attribute	Default	Description
31:16	ROS	0000	ERR_FATAL/NONFATAL Source Identification (TL)
15:0	ROS	0000	ERR_COR Source Identification (TL)

Virtual Channel Capability (140-14F)

Virtual Channel Capability is defined for Egress direction of the device. For Root Port, since only VC0 is defined, there is no implementation of VC Arbitration Table and Port Arbitration Table.

Offset Address: 140-143h (BnD0F1)
Virtual Channel Enhanced Capability
Default Value: 1801 0002h

Bit	Attribute	Default	Description
31:20	RO	180h	Next Capability Offset
19:16	RO	1h	Capability Version
15:0	RO	0002h	PCI Express Extended Capability ID

Offset Address: 147-144h (BnD0F1)
Port VC Capability I
Default Value: 0000 0001h

Bit	Attribute	Default	Description
31:12	—	0	Reserved
11:10	RO	0	Port Arbitration Table Entry Size Reserved for root port
9:8	RO	0	Reference Clock Reserved for root port
7	—	0	Reserved
6:4	RO	0	Low Priority Extended VC Count
3	—	0	Reserved
2:0	RO	1h	Extended VC Count

Offset Address: 14B-148h (BnD0F1)
Port VC Capability II
Default Value: 0000 0001h

Bit	Attribute	Default	Description
31:24	RO	00h	VC Arbitration Table Offset 00 since only VC0 is defined
23:8	—	0	Reserved
7:0	RO	01h	VC Arbitration Capability Reserved since Low Priority Extended Count (Rx144[6:4]) is 0.

Offset Address: 14D-14Ch (BnD0F1)
Port VC Control
Default Value: 0000h

Bit	Attribute	Default	Description
15:4	—	0	Reserved
3:1	RW	0	VC Arbitration Select
0	RW	0	Load VC Arbitration Table

Offset Address: 14F-14Eh (BnD0F1)
Port VC Status
Default Value: 0000h

Bit	Attribute	Default	Description
15:1	—	0	Reserved
0	RO	0	VC Arbitration Table Status

VC0 Resource (150-15Bh)
Offset Address: 153-150h (BnD0F1)
VC Resource Capability (VC0)
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:24	RO	00h	Port Arbitration Table Offset (VC0)
23	—	0	Reserved
22:16	RO	00h	Maximum Time Slots (TL)
15	RO	0	Reject Snoop Transactions
14	RO	0	Advanced Packet Switching
13:8	—	0	Reserved
7:0	RO	00h	Port Arbitration Capability

Offset Address: 157-154h (BnD0F1)
VC Resource Control (VC0)
Default Value: 8000 00FFh

Bit	Attribute	Default	Description
31	RO	1	VC Enable
30:27	—	0	Reserved
26:24	RO	0	VC ID
23:20	—	0	Reserved
19:17	RW	0	Port Arbitration Select
16	RW	0	Load Port Arbitration Table
15:8	—	0	Reserved
7:0	RW Bit 0: RO	FFh	TC/VC Mapping This field indicates the TCs that are mapped to VC0. If bit [n] is 1, the corresponding traffic class TCn is mapped to VC0 ($0 \leq n \leq 7$). Default is TC0, TC1, TC2, TC3, C4, TC5, TC6 and TC7 are all mapped to VC0. Note: Bit0 is hardwired to 1 (i.e. TC0 is always mapped to VC0).

Offset Address: 15B-158h (BnD0F1)
VC Resource Status (VC0)
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:18	—	0	Reserved
17	RO	0	VC Negotiation Pending (TL)
16	RO	0	Port Arbitration Table Status
15:0	—	0	Reserved

VC1 Resource (15C-167h)

The following registers will exist only when Rx144[0] is programmed to 1. If Rx144[0] = 0, all the following contents will be read as 0.

Offset Address: 15F-15Ch (BnD0F1)
VC Resource Capability (VC0)
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:24	RO	00h	Port Arbitration Table Offset (VC1)
23	—	0	Reserved
22:16	RO	00h	Maximum Time Slots (TL)
15	RO	0	Reject Snoop Transactions
14	RO	0	Advanced Packet Switching
13:8	—	0	Reserved
7:0	RO	00h	Port Arbitration Capability

Offset Address: 163-160h (BnD0F1)
VC Resource Control (VC1)
Default Value: 0100 0000h

Bit	Attribute	Default	Description
31	RW	0	VC Enable
30:27	—	0	Reserved
26:24	RW	1	VC ID
23:20	—	0	Reserved
19:17	RW	0	Port Arbitration Select
16	RW	0	Load Port Arbitration Table
15:8	—	0	Reserved
7:0	RW Bit 0: RO	FFh	TC/VC Mapping This field indicates the TCs that are mapped to VC0. If bit [n] is 1, the corresponding traffic class TCn is mapped to VC1 ($0 \leq n \leq 7$). Default is TC0, TC1, TC2, TC3, C4, TC5, TC6 and TC7 are all mapped to VC1. Note: Bit0 is hardwired to 1 (i.e. TC0 is always mapped to VC0).

Offset Address: 167-164h (BnD0F1)
VC Resource Status (VC1)
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:18	—	0	Reserved
17	RO	0	VC Negotiation Pending (TL)
16	RO	0	Port Arbitration Table Status
15:0	—	0	Reserved

Root Complex Topology Capability List (180-19Bh)
Offset Address: 183-180h (BnD0F1)
Root Complex Link Declaration Capabilities Header
Default Value: 0001 0005h

Bit	Attribute	Default	Description
31:20	RW	00	Next Capability
19:16	RO	1h	Capability Version
15:0	RO	0005h	Capability ID

Offset Address: 187-184h (BnD0F1)
Element Self Description
Default Value: 0201 0100h

Bit	Attribute	Default	Description
31:24	RO	02h	Port Number (Root Port 2)
23:16	RO	01h	Component ID This field returns the value of RRCRB_CID. It is in the same component as SB's RCRB.
15:8	RO	01h	Number of Link Entries
7:4	—	0	Reserved
3:0	RO	0	Element Type 0h: Configuration Space Element 1h: System egress port or internal sink 2h: Internal Root Complex Link

Offset Address: 193-190h (BnD0F1)
Upstream Link Descriptor
Default Value: 0001 0001h

Bit	Attribute	Default	Description
31:24	RO	0	Target Port Number Indicate the port number of RCRB
23:16	RO	01h	Target Component ID The value of RRCRB_CID.
15:2	—	0	Reserved
1	RO	0	Link Type Indicate the link points to RCRB
0	RO	1	Link Valid

Offset Address: 19B-194h (BnD0F1)
Upstream Link Base Address
Default Value: 0000 0000h

Bit	Attribute	Default	Description
63:32	RO	0	Base Address Upper The value of B0D19F0 Rx44-46 [23:20] (RXRCRBA_[35:32])
31:0	RO	0	Base Address Lower The value of B0D19F0 Rx44-46 (RXRCRBA_[31:28])

HDAC: High Definition Audio Controller PCI Express Configuration Space

Header Registers (0-3Fh)

Offset Address: 1-0h (HDAC)

Vendor ID

Default Value: 1106h

Bit	Attribute	Default	Description
15:0	RO	1106h	Vendor ID

Offset Address: 3-2h (HDAC)

Device ID

Default Value: 3288h

Bit	Attribute	Default	Description
15:0	RO	3288h	Device ID

Offset Address: 5-4h (HDAC)

PCI Command

Default Value: 0000h

Bit	Attribute	Default	Description
15:11	—	0	Reserved
10	RW	0	Interrupt Disable
9	RO	0	Fast Back to Back
8	RO	0	SERR# Enable
7	RO	0	Address Stepping
6	RO	0	Parity Error Response
5	RO	0	VGA Palette Snooping
4	RO	0	Memory Write and Invalidate
3	RO	0	Respond to Special Cycle
2	RW	0	Bus Master
1	RW	0	Memory Space Access
0	RO	0	I/O Space Access

Offset Address: 7-6h (HDAC)

PCI Status

Default Value: 0010h

Bit	Attribute	Default	Description
15	RO	0	Detect Parity Error
14	RO	0	Signaled System Error (SERR#)
13	RO	0	Received Master Abort
12	RO	0	Received Target Abort
11	RO	0	Signaled Target Abort
10:9	RO	00	DEVSEL# Timing
8	RO	0	Data Parity Detected
7	RO	0	Fast Back-to-Back Capability
6:5	—	0	Reserved
4	RO	1	Capability List
3	RO	0	Interrupt Status
2:0	—	0	Reserved

Offset Address: 8h (HDAC)

Revision ID

Default Value: 00h

Bit	Attribute	Default	Description
7:0	RO	00h	Revision ID

Offset Address: 0B-9h (HDAC)
Class Code
Default Value: 040300h

Bit	Attribute	Default	Description
15:0	RO	040300h	Class Code

Offset Address: 0Ch (HDAC)
Cache Line Size
Default Value: 00h

Bit	Attribute	Default	Description
7:0	RW	00h	Cache Line Size

Offset Address: 0Dh (HDAC)
Latency Timer
Default Value: 00h

Bit	Attribute	Default	Description
7:0	RO	00h	Latency Timer

Offset Address: 0Eh (HDAC)
Header Type
Default Value: 00h

Bit	Attribute	Default	Description
7:0	RO	00h	Header Type

Offset Address: 0Fh (HDAC)
Built In Self Test
Default Value: 00h

Bit	Attribute	Default	Description
7:0	RO	00h	Built In Self Test

Offset Address: 13-10h (HDAC)
HDAC Lower Base Address
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:14	RW	0	Lower Base Address 16 KB are requested by hardwaring [13:4] to 0s
13:4	RO	0	Hardwired to 0
3	RO	0	Not Prefetchable
2:1	RO	0	Address Range Can be located anywhere in 64 bit address space
0	RO	0	Space Type: memory space

Offset Address: 17-14h (HDAC)
HDAC Upper Base Address
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:0	RO	0	HDAC Upper Base Address

Offset Address: 2D-2Ch (HDAC)
Subsystem Vendor ID
Default Value: 1106h

Bit	Attribute	Default	Description
15:0	RO	1106h	Subsystem Vendor ID RW if Rx40[0] (EN2CW : CFGRX2C~2F) = 1

Offset Address: 2F-2Eh (HDAC)
Subsystem ID
Default Value: 3288h

Bit	Attribute	Default	Description
15:0	RO	3288h	Subsystem ID RW if Rx40[0] (EN2CW : CFGRX2C~2F) = 1

Offset Address: 33-30h (HDAC)
Expansion ROM
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:0	RO	0	Expansion ROM

Offset Address: 34h (HDAC)
Capabilities Pointer
Default Value: 50h

Bit	Attribute	Default	Description
7:0	RO	50h	Capabilities Pointer Points to the power management capability

Offset Address: 3Ch (HDAC)
Interrupt Line
Default Value: 00h

Bit	Attribute	Default	Description
7:0	RW	00h	Interrupt Line

Offset Address: 3Dh (HDAC)
Interrupt Pin
Default Value: 01h

Bit	Attribute	Default	Description
7:0	RO	01h	Interrupt Pin

HDAC PCIe Extended Configuration Space (40-260h)
Offset Address: 40h (HDAC)
Back Door Enable
Default Value: 00h

Bit	Attribute	Default	Description	Mnemonic
7:1	—	0	Reserved	
0	RW	0	Subsystem ID / Subsystem Vender ID Back Door Enable Specifies whether Rx2C~2F are RO or RW 0: Read Only 1: Read / Write	*EN2CW : CFGRX2C~2F

Offset Address: 41h (HDAC)
HDAC Control
Default Value: 00h

Bit	Attribute	Default	Description
7:1	—	0	Reserved
0	RW	0	Dynamic Stop 1:Dynamic stop clock 0: Free running

Offset Address: 44h (HDAC)
Traffic Class Select
Default Value: 00h

Bit	Attribute	Default	Description
7:3	—	0	Reserved
2:0	RW	0	HDAC Traffic Class Assignment 000: TC0 001: TC1 010: TC2 011: TC3 100: TC4 101: TC5 110: TC6 111: TC7

Offset Address: 51-50h (HDAC)
PCI Power Management Capabilities ID
Default Value: 6001h

Bit	Attribute	Default	Description
15:8	RO	60h	Point to the Next Capability Structure (MSI)
7:0	RO	01h	PCI Power Management Capability

Offset Address: 53-52h (HDAC)
PCI Power Management Capabilities
Default Value: C842h

Bit	Attribute	Default	Description
15:11	RO	19h	PME Can Be Generated from D3 and D0 State
10	RO	0	D2 State is not Supported
9	RO	0	D1 State is not Supported
8:6	RO	001b	Report D3 Max Suspend Current
5	RO	0	No Device-Specific Initialization is Required
4	—	0	Reserved
3	RO	0	Hardwired to 0
2:0	RO	010b	Support PCI Power 1.1 Specific

Offset Address: 57-54h (HDAC)
Power Management Control and Status
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:24	RO	0	Hardwired to 0
23	RO	0	Hardwired to 0
22	RO	0	Hardwired to 0
21:16	—	0	Reserved
15	RW1C RWM	0	PMES This bit is set when the HDAC controller would normally assert the PME# independent of the state of the PMEE. This bit is in resume well.
14:9	—	0	Reserved
8	RWS RSM	0	PMEE Enable PME wake up, if PMES is set. This bit is in resume well
7:2	—	0	Reserved
1:0	RW	0	Power State This field is used both to determinate the current power state and to set a new power state. 00b: D0 11b: D3 If software attempts to write a value of 10b or 01b into this field, the write operation must complete normally; however, no state change will occur.

Offset Address: 61-60h (HDAC)
MSI Capability ID
Default Value: 7005h

Bit	Attribute	Default	Description
15:8	RO	70h	Point to the Next Capability Structure (PCI Express)
7:0	RO	05h	MSI Capability

Offset Address: 63-62h (HDAC)
MSI Message Control
Default Value: 0000h

Bit	Attribute	Default	Description
15:8	—	0	Reserved
7	RO	0	64 Bit Address Capability
6:4	RO	0	Multiple Message Enable Normally this is a R/W register, but software will always read 000b to indicate only 1 message is supported.
3:1	RO	0	Hardwired to 0 Indicating Request for 1 Message
0	RW	0	MSI Enable 0: A MSI will be generated instead of an INTx 1: A MSI will not be generated.

Offset Address: 67-64h (HDAC)
MSI Message Lower Address
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:2	RW	0	Message Lower Address
1:0	—	0	Reserved

Offset Address: 6B-68h (HDAC)
MSI Message Upper Address
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:4	—	0	Reserved
3:1	RO	0	Message Upper Address

Offset Address: 6D-6Ch (HDAC)
MSI Data
Default Value: 0000h

Bit	Attribute	Default	Description
15:0	RW	0	Data Used for MSI Message

Offset Address: 71-70h (HDAC)
PCI Express Capability ID
Default Value: 0010h

Bit	Attribute	Default	Description
15:8	RO	0	The Last Capability Structure in the List
7:0	RO	10h	PCI Express Capability

Offset Address: 73-72h (HDAC)
PCI Express Capability
Default Value: 0001h

Bit	Attribute	Default	Description
15:4	RO	0	Hardwired to 0
3:0	RO	01h	Capability Version #1

Offset Address: 77-74h (HDAC)
Device Capabilities
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:0	RO	0	Device Capabilities Hardwired to 0

Offset Address: 79-78h (HDAC)
Device Control
Default Value: 0000h

Bit	Attribute	Default	Description
15	—	0	Reserved
14:12	RO	0	Hardwired to 0
11	RO	0	Snoop
10:0	RO	0	Hardwired to 0

Offset Address: 7B-7Ah (HDAC)
Device Status
Default Value: 0010h

Bit	Attribute	Default	Description
15:6	—	0	Reserved
5	RO	0	Transaction Pending 0: All non-posted requests have been executed 1: Some non-posted request have not been completed
4	RO	1	Hardwired to 1
3:0	RO	0	Hardwired to 0

Offset Address: 103-100h (HDAC)
Virtual Channel Enhanced Capability
Default Value: 1301 0002h

Bit	Attribute	Default	Description
31:20	RO	130h	Next Capability Pointer Hardwired to 130h. Point to the next capability header, which is the Root Complex link declaration enhanced capability header
19:16	RO	01h	Hardwired to 1
15:0	RO	0002h	Hardwired to 2

Offset Address: 107-104h (HDAC)
Port VC Capability 1
Default Value: 0000 0001h

Bit	Attribute	Default	Description
31:12	—	0	Reserved
11:3	RO	0	Hardwired to 0
2:0	RO	001b	Indicates that one extended VC is supported by the controller

Offset Address: 10B-108h (HDAC)
Port VC Capability 2
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:24	RO	0	Hardwired to 0. Indicates that a VC arbitration table is not present
23:8	—	0	Reserved
7:0	RO	0	Hardwired to 0

Offset Address: 10D-10Ch (HDAC)
Port VC Control
Default Value: 0000h

Bit	Attribute	Default	Description
15:0	—	0	Reserved

Offset Address: 10F-10Eh (HDAC)
Port VC Status
Default Value: 0000h

Bit	Attribute	Default	Description
15:1	—	0	Reserved
0	RO	0	Hardwired to 0. VC arbitration table is not present

Offset Address: 113-110h (HDAC)
VC0 Resource Capability
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:0	RO	0	Hardwired to 0. This field is not valid for endpoint devices.

Offset Address: 117-114h (HDAC)
VC0 Resource Control
Default Value: 8000 00FFh

Bit	Attribute	Default	Description
31	RO	1b	VC0 Enable. Hardwired to 1 for VC0
30:27	—	0	Reserved
26:24	RO	0	VC0 ID. Hardwired to 0 since this field is assigned to VC0.
23:20	—	0	Reserved
19:16	RO	0	Hardwired to 0
15:8	—	0	Reserved
7:0	RW	FF	TC/VC0 Map Bit 0 is Hardwired to 1 since TC0 is always mapped to VC0. Bit[7:1] are implemented as RW bits

Offset Address: 11B-11Ah (HDAC)
VC0 Resource Status
Default Value: 0000h

Bit	Attribute	Default	Description
15:2	—	0	Reserved
1	RO	0	Hardwired to 0. This bit is not applied to integrated device.
0	RO	0	Hardwired to 0. This bit is not valid for endpoint devices.

Offset Address: 11F-11Ch (HDAC)
VC1 Resource Capability
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:0	RO	0	Hardwired to 0. This bit is not valid for endpoint devices

Offset Address: 123-120h (HDAC)
VC1 Resource Control
Default Value: 0001 0000h

Bit	Attribute	Default	Description
31	RW	0	VC1 Enable. When set to 1, VC1 is enabled.
30:27	—	0	Reserved
26:24	RW	001b	VC1 ID. This field assigns a VC ID to the VC1 resource. This field is not used by the HDAC hardware, but it is RW to avoid confusing software.
23:20	—	0	Reserved
19:16	RO	0	Hardwired to 0. This bit is not valid for endpoint devices.
15:8	—	0	Reserved
7:0	RW	0	TC/VC1 Map This field indicates the TCs that are mapped to the VC1 resource. Bit0 is hardwired to 0 indicating that it cannot be mapped to VC1. Bit[7:1] are implemented as RW bits. This field is not used by hardware, but it is RW to avoid confusing software.

Offset Address: 127-126h (HDAC)
VC1 Resource Status
Default Value: 0000h

Bit	Attribute	Default	Description
15:2	—	0	Reserved
1:0	RO	0	Hardwired to 0. This bit is not valid for endpoint devices.

Offset Address: 133-130h (HDAC)
Root Complex Link Declaration Enhanced Capability Header Register
Default Value: 0001 0005h

Bit	Attribute	Default	Description
31:16	RO	0001h	Next Capability. Hardwired to 0001h.
15:0	RO	0005h	PCI Express Extended Capability ID. Hardwired to 0005h.

Offset Address: 137-134h (HDAC)
Element Self Description
Default Value: 0301 0100h

Bit	Attribute	Default	Description
31:24	RO	03h	Port Number Hardwired to 03h indicating HDAC controller is assigned as port #5.
23:16	RO	01h	Component ID. Hardwired to 01h.
15:8	RO	01h	Number of Link Entries. Hardwired to 01h.
7:4	—	0	Reserved
3:0	RO	0	Element Type. The HDAC controller is an integrated root complex device, this field reports a value of 0h

Offset Address: 143-140h (HDAC)
Link 1 Description
Default Value: 0001 0001h

Bit	Attribute	Default	Description
31:24	RO	00	Target Port Number. Hardwired to 00h.
23:16	RO	01h	Component ID. Hardwired to 01h.
15:2	—	0	Reserved
1	RO	0	Link Type. Indicates that the link points to RCRB.
0	RO	1h	Link Valid

Offset Address: 14B-148h (HDAC)
Link 1 Low Address
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:12	RO	0	Link 1 Lower Address. Hardwired to match RXRCRBA[31:12].
11:0	RO	0	Reserved. Always reads 0.

Offset Address: 14F-14Ch (HDAC)
Link 1 Upper Address
Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:4	RO	0	Reserved. Always reads 0
3:0	RO	0	Link 1 Upper Address. Hardwired to match RXRCRBA[35:32].

Offset Address: 200h (HDAC)
BIST Control
Default Value: 00h

Bit	Attribute	Default	Description
7:3	—	0	Reserved
2	RW	0	BIST Clock Switch. Must be done before enabling playback / recoding run bit.
1	RW	0	Playback BIST Run Bit Software can only write 1 to enable BIST process. Read back as 0 indicates BIST process has completed.
0	RW	0	Recoding BIST Run Bit Software can only write 1 to enable BIST process. Read back as 0 indicates BIST process has completed.

Offset Address: 214-210h (HDAC)
BIST Playback Pattern
Default Value: 00 0000 0000h

Bit	Attribute	Default	Description
39:34	—	0	Reserved
33:0	RW	0	Playback BIST Pattern.

Offset Address: 224-220h (HDAC)
BIST Recording Pattern
Default Value: 00 0000 0000h

Bit	Attribute	Default	Description
39:34	—	0	Reserved
33:0	RW	0	Recording BIST Pattern.

Offset Address: 231-230h (HDAC)
SRAMs (Playback Related Only) Direct Read/Write Access
Default Value: 0000h

Bit	Attribute	Default	Description
15:12	—	0	Reserved
11	RW	0	SRAM_RUN_PLAY Enable the direct access operation
10	RW	0	SRAM_WR_PLAY 1: Indicates a write 0: Indicates a read
9:8	RW	0	SRAM_EXTSEL_PLAY Indicates the selected SRAM among the four SRAMs 00: SRAM 0 01: SRAM 1 10: SRAM 2 11: SRAM 4
7:6	—	0	Reserved
5:0	RW	0	SRAM_ADDR_PLAY The accessing address of the selected SRAM

Offset Address: 233-232h (HDAC)
SRAMs (Record Related Only) Direct Read/Write Access
Default Value: 0000h

Bit	Attribute	Default	Description
15:12	—	0	Reserved
11	RW	0	SRAM_RUN_REC Enable the direct access operation
10	RW	0	SRAM_WR_REC 1: Indicates a write 0: Indicates a read
9:8	RW	0	SRAM_EXTSEL_REC Indicates the selected SRAM among the four SRAMs 00: SRAM 0 01: SRAM 1 10: SRAM 2 11: SRAM 4
7:5	—	0	Reserved
4:0	RW	0	SRAM_ADDR_REC The accessing address of the selected SRAM

Offset Address: 244-240h (HDAC)
BIST Playback Data Check
Default Value: 00 0000 0000h

Bit	Attribute	Default	Description
39:34	—	0	Reserved
33:0	RO	0	Playback Data Read from SRAM

Offset Address: 254-250h (HDAC)
BIST Recording Data Check
Default Value: 00 0000 0000h

Bit	Attribute	Default	Description
39:34	—	0	Reserved
33:0	RO	0	Recording Data Read from SRAM

Offset Address: 260h (HDAC)
BIST Error Status
Default Value: 00h

Bit	Attribute	Default	Description
7	RO	0	BIST_ERR_SRAM3_PLAY
6	RO	0	BIST_ERR_SRAM2_PLAY
5	RO	0	BIST_ERR_SRAM1_PLAY
4	RO	0	BIST_ERR_SRAM0_PLAY
3	RO	0	BIST_ERR_SRAM3_REC
2	RO	0	BIST_ERR_SRAM2_REC
1	RO	0	BIST_ERR_SRAM1_REC
0	RO	0	BIST_ERR_SRAM0_REC

High Definition Audio Controller (HDAC)

This section describes the memory mapped High Definition Audio Controller register interface. Please refer to High Definition Audio Specification 1.0 for details.

Global Capabilities and Control (0-1Bh)
Offset Address: 1-0h
Global Capabilities – GCAP
Default Value: 4401h

Bit	Attribute	Default	Description	Mnemonic
15:12	RO	4h	Number of Output Streams Supported 0100b: 4 output streams supported	OSS
11:8	RO	4h	Number of Input Streams Supported 0100b: 4 input streams supported	ISS
7:3	RO	0	Number of Bidirectional Streams Supported 00000b: No bidirectional stream supported	BSS
2:1	RO	0	Number of Serial Data Out Signals 00: 1 SDO 01: 2 SDOs 10: 4 SDOs 11: Reserved	NSDO
0	RO	1	64 Bit Address Supported 0: Only 32-bit addressing is available. 1: 64 bit addressing is supported.	64OK

Offset Address: 3-2h
Version Number
Default Value: 0100h

Bit	Attribute	Default	Description	Mnemonic
15:8	RO	01h	Major Version	VMAJ
7:0	RO	00h	Minor Version	VMIN

The version number “0100h” indicates this chip complies with High Definition Audio Specification Rev 1.0.

Offset Address: 7-4h
Payload Capability
Default Value: 001D 003Ch

Bit	Attribute	Default	Description	Mnemonic
31:16	RO	001Dh	Input Payload Capability 1Dh: 29-word payload (464 bits) Note: this does not include bandwidth used for command and control.	INPAY
15:0	RO	003Ch	Output Payload Capability 3Ch: 60-word payload (960 bits)	OUTPAY

Offset Address: 0B-8h
Global Control – GCTL
Default Value: 0000 000nh

Bit	Attribute	Default	Description	Mnemonic
31:9	RsvdP	0	Reserved	
8	RW	0	Accept Unsolicited Response Enable 0: Unsolicited response from codec are not accepted 1: Unsolicited response from codec are accepted by the controller	UNSOL
7:2	RsvdP	0	Reserved	
1	RW	0	Flush Control Writing a 1 to this bit initiates a flush.	*FCNTRL
0	RWS	HwInit	Controller Reset For read: 0: In reset state For write: 0: Reset the controller	CRST
			1: Controller is ready for operations. 1: Exit the reset state	

Offset Address: 0D-0Ch
Wake Enable – WAKEEN
Default Value: 0000h

Bit	Attribute	Default	Description	Mnemonic
15:4	RsvdP	0	Reserved	
3:0	RW, RSM	0	SDIN Wake Enable Flags 0:Disable 1: Allow the associated SDIN signal to generate a wake or processor interrupt The bit[i] corresponds to SDIN[i] signal.	SDI3WEN SDI2WEN SDI1WEN SDI0WEN

Offset Address: 0F-0Eh
State Change Status – STATESTS
Default Value: 0000h

Bit	Attribute	Default	Description	Mnemonic
15:4	RsvdZ	0	Reserved	
3:0	RW1CS, RSM	0	SDIN State Change Status Flags 0:No state change 1: The associated SDIN signal received a “State Change” event. The bit[i] corresponds to SDIN[i] signal.	DI3WAKE SDI2WAKE SDI1WAKE SDI0WAKE

Offset Address: 11-10h
Global Status – GSTS
Default Value: 0000h

Bit	Attribute	Default	Description	Mnemonic
15:2	RsvdZ	0	Reserved	
1	RW1C	0	Flush Status 0: No flush cycle completed 1: Flush cycle completed This bit is set to 1 by the hardware to indicate that the flush cycle initiated when the Rx8[1] (FCNTRL) was has completed. Software must write 1 to clear this bit before the next time Rx8[1] is set to clear the bit.	FSTS
0	RsvdZ	0	Reserved	

Offset Address: 1B-18h
Stream Payload Capability
Default Value: 0000 0000h

Bit	Attribute	Default	Description	Mnemonic
31:16	RO	0000h	Input Stream Payload Capability 1Dh: 29-word payload	OUTSTRMPAY
15:0	RO	0000h	Output Stream Payload Capability 3Ch: 60-word payload	INSTRMPAY

Interrupt Control (20-27h)
Offset Address: 23-20h
Interrupt Control – INTCTL
Default Value: 0000 0000h

Bit	Attribute	Default	Description	Mnemonic
31	RW	0	Global Interrupt Enable 0: Disable 1: Enable device interrupt generation	GIE
30	RW	0	Controller Interrupt Enable 0: Disable 1: Enable controller general interrupts	CIE
29:8	RsvdP	0	Reserved	
7:4	RW	0	Stream Interrupt Enable – for Output Stream [3:0] 0: Disable 1: Enable	SIE[7:4]
3:0	RW	0	Stream Interrupt Enable – for Input Stream [3:0] 0: Disable 1: Enable	SIE[3:0]

Offset Address: 27-24h
Interrupt Status – INTSTS
Default Value: 0000 0000h

Bit	Attribute	Default	Description	Mnemonic
31	RO	0	Global Interrupt Status This bit is an OR of all the interrupt status bit in this register. 0: No interrupt occurred 1: Some interrupt(s) occurred	GIS
30	RW1C	0	Controller Interrupt Status 0: No interrupt occurred 1: Some interrupt(s) occurred	CIS
29:8	RsvdP	0	Reserved	
7:4	RW1C	0	Stream Interrupt Status – for Output Stream [3:0] 0: No interrupt occurred 1: Interrupt occurred	SIS[7:4]
3:0	RW1C	0	Stream Interrupt Status – for Input Stream [3:0] 0: No interrupt occurred 1: Interrupt occurred	SIS[3:0]

Synchronization Control (30-3Bh)
Offset Address: 33-30h
Wall Clock Counter
Default Value: 0000 0000h

Bit	Attribute	Default	Description	Mnemonic
31:0	RO	0	Wall Clock Counter 32 bits counter that is incremented at the link bitclk rate and rolls over from FFFF_FFFFh to 0000_0000h. This counter will roll over to zero with a period of approximately 179 seconds.	WCounter

Offset Address: 3B-38h
Stream Synchronization – SSYNC
Default Value: 0000 0000h

Bit	Attribute	Default	Description	Mnemonic
31:8	RsvdP	0	Reserved	
7:4	RW	0	Stream Synchronization Bits – for Input Stream [3:0] 0: Do not block data 1: Blocks data from sending on or receiving from the link	*SSYNC [7:4]
3:0	RW	0	Stream Synchronization Bits – for Output Stream [3:0] 0: Do not block data 1: Blocks data from sending on or receiving from the link	*SSYNC [3:0]

CORB (Command Output Ring Buffer) Control (40-4Eh)
Offset Address: 43-40h
CORB Lower Base Address – CORBLBASE
Default Value: 0000 0000h

Bit	Attribute	Default	Description	Mnemonic
31:7	RW	0	CORB (Command Output Ring Buffer) Lower Base Address Lower address of the Command Output Ring Buffer	CORBLBASE
6:0	—	0	Reserved Hardwired to 0. 128 byte alignment	

Offset Address: 47-44h
CORB Upper Base Address – CORBUBASE
Default Value: 0000 0000h

Bit	Attribute	Default	Description	Mnemonic
31:4	—	0	Reserved Hardwired to 0.	
3:0	RW	0	CORB Upper Base Address Upper 32 bits of address of the Command Output Ring Buffer	CORBUBASE

Offset Address: 49-48h
CORB Write Pointer
Default Value: 0000h

Bit	Attribute	Default	Description	Mnemonic
15:8	RsvdP	0	Reserved	
7:0	RW	0	CORB Write Pointer Software write the last valid CORB entry offset into this field in Dword granularity. The DMA engine fetches commands from the CORB until the read point matches the write pointer. The field may be written while the DMA engine is running	CORBWP

Offset Address: 4B-4Ah
CORB Read Pointer
Default Value: 0000h

Bit	Attribute	Default	Description	Mnemonic
15	RW	0	CORB Read Pointer Reset Writes a 1 to reset the CORB Read Pointer to 0. DMA engine must be stopped prior to resetting the read pointer or else DMA transfer may be corrupted. This bit will always be read 0.	CORBRPRST
14:8	RsvdP	0	Reserved	
7:0	RO	0	CORB Read Pointer Software read this field to determine how many commands it can write to the CORB without overrunning. The value read indicates the CORB read pointer offset in Dword granularity. The offset entry read from this field has been successfully fetched by the DMA controller and may be overwritten by software. Supports up to 256 CORB entries (256*4B = 1KB) in the cyclic buffer.	CORBRP

Offset Address: 4Ch
CORB Control – CORBCTL
Default Value: 00h

Bit	Attribute	Default	Description	Mnemonic
7:2	RsvdP	0	Reserved	
1	RW	0	Enable CORB DMA Engine 0: DMA Stop 1: DMA Run (when read pointer lags write pointer). Software must read the value back.	CORBRUN
0	RW	0	CORB Memory Error Interrupt Enable 0: Disable 1: Enable	CMEIE

Offset Address: 4Dh
CORB Status – CORBSTS
Default Value: 00h

Bit	Attribute	Default	Description	Mnemonic
7:1	RsvdP	0	Reserved	
0	RW1C	0	CORB Memory Error Indication 0: No error 1: Error detected. The controller has detected an error in the pathway between the controller and memory.	CMEI

Offset Address: 4Eh
CORB Size – CORBSIZE
Default Value: 42h

Bit	Attribute	Default	Description	Mnemonic
7:4	RO	0100b	CORB Size Capability 0100: 256 entries (1024B)	CORBSZCAP
3:2	RsvdP	0	Reserved	
1:0	RW	10b	CORB Size 00: 2 entries (8 bytes) 10: 256 entries (1 KB)	CORBSIZE
			01: 16 entries (64 bytes) 11: Reserved	

RIRB (Response Input Ring Buffer) Control (50-5Eh)
Offset Address: 53-50h
RIRB Lower Base Address – RIRBLBASE
Default Value: 0000 0000h

Bit	Attribute	Default	Description	Mnemonic
31:7	RW	0	RIRB (Response Input Ring Buffer) Lower Base Address Lower address of the Response Input Ring Buffer	RIRBLBASE
6:0	—	0	Reserved Hardwired to 0. 128 byte alignment	

Offset Address: 57-54h
RIRB Upper Base Address – RIRBUBASE
Default Value: 0000 0000h

Bit	Attribute	Default	Description	Mnemonic
31:4	—	0	Reserved Hardwired to 0.	
3:0	RW	0	RIRB Upper Base Address Upper 32 bits of address of the Response Input Output Ring Buffer	RIRBUBASE

Offset Address: 59-58h
RIRB Write Pointer – RIRBWP
Default Value: 0000h

Bit	Attribute	Default	Description	Mnemonic
15	RW	0	RIRB Write Pointer Reset Writes a 1 to reset the RIRB Write Pointer to 0. The DMA engine must be stopped prior to resetting the write pointer or else DMA transfer may be corrupted. This bit always read as 0.	RIRBWRST
14:8	RsvdP	0	Reserved	
7:0	RO	0	RIRB Write Pointer Indicates the last valid RIRB entry written by the DMA controller. Software reads this field determining how many responses it can read from the RIRB. The value read indicates the RIRB write pointer offset in 2 Dword units. Supports up to 256 RIRB entries in the cyclic buffer.	RIRBWP

Offset Address: 5B-5Ah
Response Interrupt Count – RINTCNT
Default Value: 0000h

Bit	Attribute	Default	Description	Mnemonic
15:8	RsvdP	0	Reserved	
7:0	RW	0	N Response Interrupt Count 00h: 256 responses 01h .. FFh: 1 .. 255 responses The DMA engine should be stopped when changing this field or else an interrupt may be lost.	RINTCNT

Offset Address: 5Ch
RIRB Control – RIRBCTL
Default Value: 00h

Bit	Attribute	Default	Description	Mnemonic
7:3	RsvdP	0	Reserved	
2	RW	0	Response Overrun Interrupt Control 0: Disable 1: Enable	RIRBOIC
1	RW	0	Enable RIRB DMA Engine 0: DMA Stop 1: DMA Run (when response queue not empty)	RIRBDMAEN
0	RW	0	Response Interrupt Control 0: Disable 1: Enable. Generate an interrupt after N number of response are sent to the RIRB buffer or when an empty response slot is encountered on all SDINx input after a frame which returned a response. The N counter is reset when the interrupt is generated.	RINTCTL

Offset Address: 5Dh
RIRBSTS – RIRB Status
Default Value: 00h

Bit	Attribute	Default	Description	Mnemonic
7:3	RsvdZ	0	Reserved	
2	RW1C	0	Response Overrun Interrupt Status Hardware sets this bit to 1 when an overrun occurs in the RIRB. An interrupt may be generated if the response overrun interrupt control bit is set. 0: No overrun 1: Overrun occurred	RIRBOIS
1	RsvdZ	0	Reserved	
0	RW1C	0	Response Interrupt Hardware sets this bit to 1 when an interrupt has been generated after N number of response are sent to the RIRB buffer or when an empty response slot is encountered on all SDINx inputs. 0: No response interrupt 1: Response interrupt occurred	RINTFL

Offset Address: 5Eh
RIRB Size – RIRBSIZE
Default Value: 42h

Bit	Attribute	Default	Description	Mnemonic
7:4	RO	0100b	RIRB Size Capability 0100: 256 entries (2048B)	RIRBSZCAP
3:2	RsvdP	0	Reserved	
1:0	RW	10b	RIRB Size 00: 2 entries (16 bytes) 01: 16 entries (128 bytes) 10: 256 entries (2 KB) 11: Reserved	RIRBSIZE

Immediate Command Control (60-69h)
Offset Address: 63-60h
Immediate Command Input / Output Interface
Default Value: 0000 0000h

Bit	Attribute	Default	Description	Mnemonic
31:0	RW	0	Immediate Command Write The written value will be sent out over the link in the next available frame. Reads always return 0's. Software must ensure that the ICB bit in the immediate command status register is cleared before writing a value into this register or undefined behavior will result.	ICW

Offset Address: 67-64h
Immediate Response Input Interface
Default Value: 0000 0000h

Bit	Attribute	Default	Description	Mnemonic
31:0	RO	0	Immediate Response Read Reads return the last response came over the link.	IRR

Offset Address: 69-68h
Immediate Command Status
Default Value: 0000h

Bit	Attribute	Default	Description	Mnemonic
15:8	RsvdZ	0	Reserved	
7:4	RO	0	Immediate Response Result Address The latched codec address	IRRADD
3	RO	0	Immediate Response Result Unsolicited 0: A solicited response latched 1: An unsolicited response latched	IRRUNSOL
2	RsvdZ	0	Reserved	
1	RW1C	0	Immediate Result Valid 0: No new response 1: A new response arrived. This bit is set to 1 by hardware when a new response has been received.	IRV
0	RO	0	Immediate Command Busy 0: Ready for accepting an immediate command 1: Not ready Software must wait until this bit becomes 0 before writing a value in Rx63-60 (ICW).	ICB

Stream Descriptors (80-17Fh)

Stream Descriptor Control

Default Value: 00 0000h

- Offset Address 82-80h: Input Stream 0**
- Offset Address A2-A0h: Input Stream 1**
- Offset Address C2-C0h: Input Stream 2**
- Offset Address E2-E0h: Input Stream 3**
- Offset Address 102-100h: Output Stream 0**
- Offset Address 122-120h: Output Stream 1**
- Offset Address 143-140h: Output Stream 2**
- Offset Address 163-160h: Output Stream 3**

Bit	Attribute	Default	Description	Mnemonic
23:20	RW	0h	Stream ID A tag corresponds to the transferred data on the link 0: Unused 1..0Fh: Stream 1 .. 15	SID
19	RO	0	Bidirectional Direction Control Hardwired to 0. Bidirectional engine is not supported. 0: Configures as input engine (Read Only for non-bidirectional engines) 1: Configures as output engine	DIR
18	RO	0	Traffic Priority Hardwired to 0. The traffic will be handled on a best effort basis. 0: Handles on a “best effort” basis 1: Handles as preferred traffic	TP
17:16	RO	0	Stripe Control Hardwired to 0 indicating that the controller supports 1 SDO line. 00: 1 SDO 01: 2 SDOs 10: 4 SDOs (Read Only for input streams)	STRIPE
15:5	RsvdP	0	Reserved	
4	RW	0	Descriptor Error Interrupt Enable Controls whether an interrupt is generated when the descriptor error status bit is set. 0: Disable 1: Enable	DEIE
3	RW	0	FIFO Error Interrupt Enable Controls whether the occurrence of a FIFO error (underrun/overrun) will cause an interrupt or not. 0: Disable 1: Enable	FEIE
2	RW	0	Interrupt On Completion Enable Controls whether an interrupt occurs when a buffer completion with the IOC bit set in its descriptor. 0: Disable 1: Enable.	IOCE
1	RW	0	Stream Run 0: DMA disable. The DMA engine associated with this input stream will be disabled. If the corresponding Rx38 (SSYNC) bit is 0, input stream data will be taken from the link and moved to the FIFO and an overrun may occurs. 1: DMA enable. The DMA engine associated with this input stream will be enabled to transfer data in the FIFO to main memory.	RUN
0	RW	0	Stream Reset For read: 0: Ready (not in reset state) 1: In reset state For write: 0: Exit reset 1: Reset the steam	SRST

Stream Descriptor Status
Default Value: 00h

Offset Address 83h: Input Stream 0
 Offset Address A3h: Input Stream 1
 Offset Address C3h: Input Stream 2
 Offset Address E3h: Input Stream 3
 Offset Address 103h: Output Stream 0
 Offset Address 123h: Output Stream 1
 Offset Address 143h: Output Stream 2
 Offset Address 163h: Output Stream 3

Bit	Attribute	Default	Description	Mnemonic
7:6	RsvdZ	0	Reserved	
5	RO	0	FIFO Ready For an output stream: 0: Not enough data for transferring 1: The output DMA FIFO contains enough data to transfer For an input stream: This bit is not meaningful for input an input stream. Therefore, it is always read 0 for input streams.	FIFORDY
4	RW1C	0	Descriptor Error 0: No error 1: Error occurred	DESE
3	RW1C	0	FIFO Error For an input stream, it indicates a FIFO overrun occurring while run bit is set. For an output stream, it indicates a FIFO underrun occurring while there are still buffers to send. 0: No error 1: Error occurred	FIFOE
2	RW1C	0	Buffer Completion Interrupt Status 0: Not completed 1: Buffer operation completed	BCIS
1:0	RsvdZ	0	Reserved	

Stream Descriptor Link Position in Buffer
Default Value: 0000 0000h

Offset Address 87-84h: Input Stream 0
 Offset Address A7-A4h: Input Stream 1
 Offset Address C7-C4h: Input Stream 2
 Offset Address E7-E4h: Input Stream 3
 Offset Address 107-104h: Output Stream 0
 Offset Address 127-124h: Output Stream 1
 Offset Address 147-144h: Output Stream 2

Bit	Attribute	Default	Description	Mnemonic
31:0	RO	0	Link Position in Buffer Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the cyclic buffer length register and then wrap to 0.	LPIB

Stream Descriptor Cyclic Buffer Length
Default Value: 0000 0000h

Offset Address 8B-88h: Input Stream 0
 Offset Address AB-A8h: Input Stream 1
 Offset Address CB-C8h: Input Stream 2
 Offset Address EB-E8h: Input Stream 3
 Offset Address 10B-108h: Output Stream 0
 Offset Address 12B-128h: Output Stream 1
 Offset Address 14B-148h: Output Stream 2
 Offset Address 16B-168h: Output Stream 3

Bit	Attribute	Default	Description	Mnemonic
31:0	RW	0	Cyclic Buffer Length Indicates the number of bytes in the completed cyclic buffer. Link position in buffer will be reset when it reaches this value.	CBL

Stream Descriptor Last Valid Index

Default Value: 0000h

Offset Address 8D-8Ch: Input Stream 0
Offset Address AD-ACh: Input Stream 1
Offset Address CD-CCh: Input Stream 2
Offset Address ED-ECh: Input Stream 3
Offset Address 10D-10Ch: Output Stream 0
Offset Address 12D-12Ch: Output Stream 1
Offset Address 14D-14Ch: Output Stream 2
Offset Address 16D-16Ch: Output Stream 3

Bit	Attribute	Default	Description	Mnemonic
15:8	RsvdP	0	Reserved	
7:0	RW	0	Last Valid Index	LVI

Stream Descriptor FIFO Size

Offset Address 91-90h: Input Stream 0
Offset Address B1-B0h: Input Stream 1
Offset Address D1-D0h: Input Stream 2
Offset Address E1-E0h: Input Stream 3
Offset Address 111-110h: Output Stream 0
Offset Address 131-130h: Output Stream 1
Offset Address 151-150h: Output Stream 2
Offset Address 171-170h: Output Stream 3

Input Stream Default Value: 0000h

Output Stream Default value: 00C0h

Bit	Attribute	Default	Description	Mnemonic
Input Stream				
15:8	—	0	Reserved	
7:0	RW	60h	FIFO Size The max number of bytes that can be fetched by the controller at one time.	FIFOSZ
Output Stream				
15:9	—	0	Reserved	
8:0	RW	C0h	FIFO Size The max number of bytes that can be fetched by the controller at one time. Note: Bit 8 can <i>only</i> be modified together with [7:0]	FIFOSZ

Stream Descriptor Format
Default Value: 0000h

Offset Address 93-92h: Input Stream 0
Offset Address B3-B2h: Input Stream 1
Offset Address D3-D2h: Input Stream 2
Offset Address F3-F2h: Input Stream 3
Offset Address 113-112h: Output Stream 0
Offset Address 133-132h: Output Stream 1
Offset Address 153-152h: Output Stream 2
Offset Address 173-172h: Output Stream 3

Bit	Attribute	Default	Description	Mnemonic
15	RW	0	PCM 0: PCM 1: Non PCM	PCM
14	RW	0	Sample Base Rate 0: 48 KHz 1: 44.1 KHz	BASE
13:11	RW	0	Sample Base Rate Multiple 000: x1 001: x2 011: x4 Others (100 .. 111) : Reserved	MUL
10:8	RW	0	Sample Base Rate Divisor 0nh: Divided by (n+1), where 0<=n <=7	DIV
7	RsvdP	0	Reserved	
6:4	RW	0	Bits per Sample 000: 8 bits 001: 16 bits 011: 24 bits 100: 32 bits Others (101 .. 111): Reserved	BITS
3:0	RW	0	Number of Channels 0nh: (n+1) channels, where 0<=n <=15	CHNO

Stream Descriptor BDL Pointer Lower Base Address
Default Value: 0000 0000h

Offset Address 9B-98h: Input Stream 0
Offset Address BB-B8h: Input Stream 1
Offset Address DB-D8h: Input Stream 2
Offset Address FB-F8h: Input Stream 3
Offset Address 11B-118h: Output Stream 0
Offset Address 13B-138h: Output Stream 1
Offset Address 15B-158h: Output Stream 2
Offset Address 17B-178h: Output Stream 3

Bit	Attribute	Default	Description	Mnemonic
31:7	RW	0	Buffer Descriptor List Lower Base Address	BDLLBASE
6:0	RO	0	Unimplemented Bits Hardwired to 0 for 128 bytes alignment	

Stream Descriptor BDL Pointer Upper Base Address
Default Value: 0000 0000h

Offset Address 9F-9Ch: Input Stream 0
Offset Address BF-BCh: Input Stream 1
Offset Address DF-DCh: Input Stream 2
Offset Address FF-FCh: Input Stream 3
Offset Address 11F-11Ch: Output Stream 0
Offset Address 13F-13Ch: Output Stream 1
Offset Address 15F-15Ch: Output Stream 2
Offset Address 17F-17Ch: Output Stream 3

Bit	Attribute	Default	Description	Mnemonic
31:0	RW	0	Buffer Descriptor List Upper Base Address	BDLUBASE

Alias Registers (2030-2167h)
Offset Address: 2033-2030h (HDAC)
Wall Clock Counter Alias – WALCLKA
Default Value: 0000 0000h

Bit	Attribute	Default	Description	Mnemonic
31:0	RO	0	Wall Clock Counter Alias	Wcounter

Stream Descriptor Link Position in Buffer Alias
Default Value: 0000 0000h
Offset Address 2087-2084h: Input Stream 0
Offset Address 20A7-20A4h: Input Stream 1
Offset Address 20C7-20C4h: Input Stream 2
Offset Address 20E7-20E4h: Input Stream 3
Offset Address 2107-2104h: Output Stream 0
Offset Address 2127-2124h: Output Stream 1
Offset Address 2147-2144h: Output Stream 2
Offset Address 2167-2164h: Output Stream 3

Bit	Attribute	Default	Description	Mnemonic
31:0	RO	0	Link Position in Buffer n Alias An alias of the link position in buffer register for each stream descriptor	LPIB

ELECTRICAL SPECIFICATIONS

Power Sequence

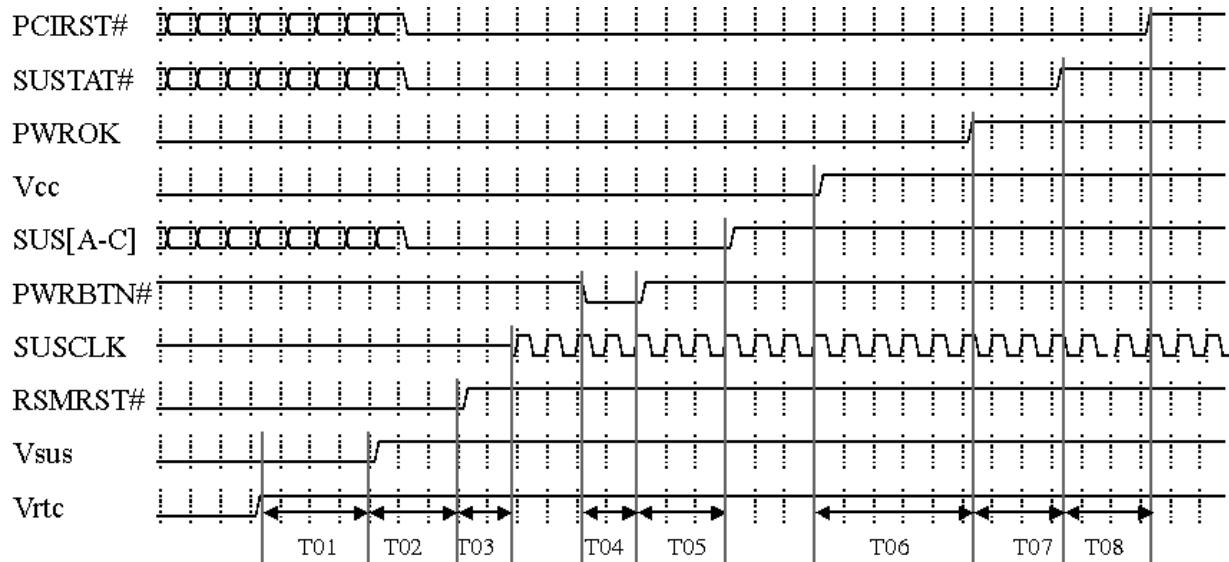


Figure 3. Power On Sequence and Reset Signal Timing

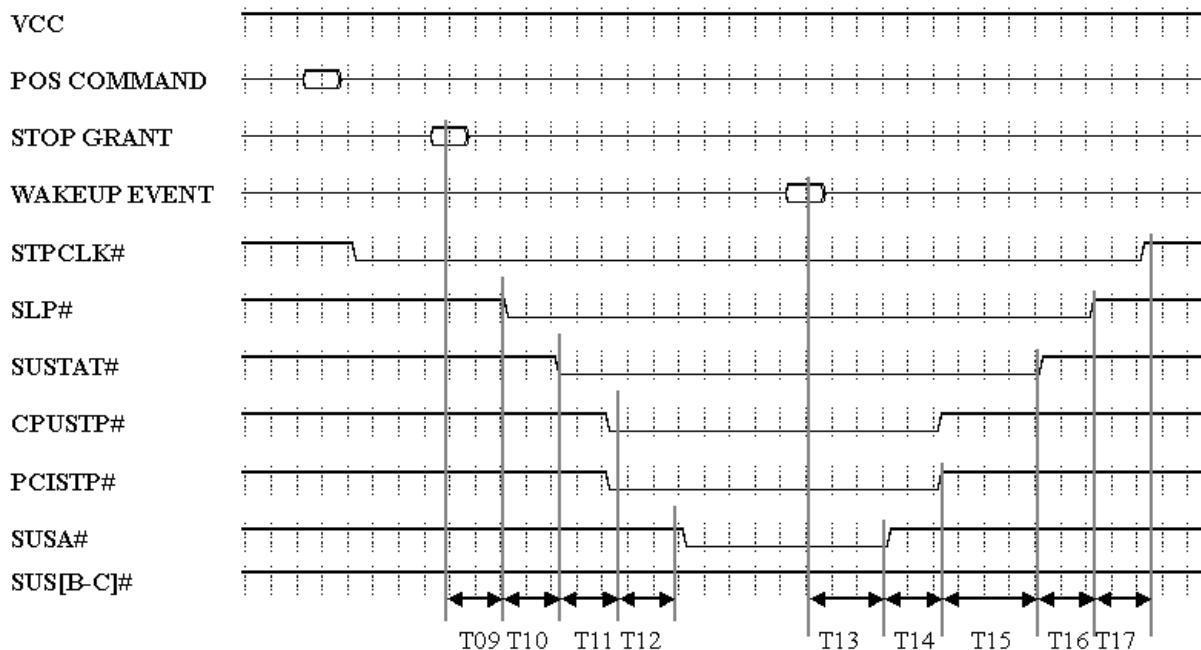


Figure 4. Power On Suspend & Resume Sequence without RESET

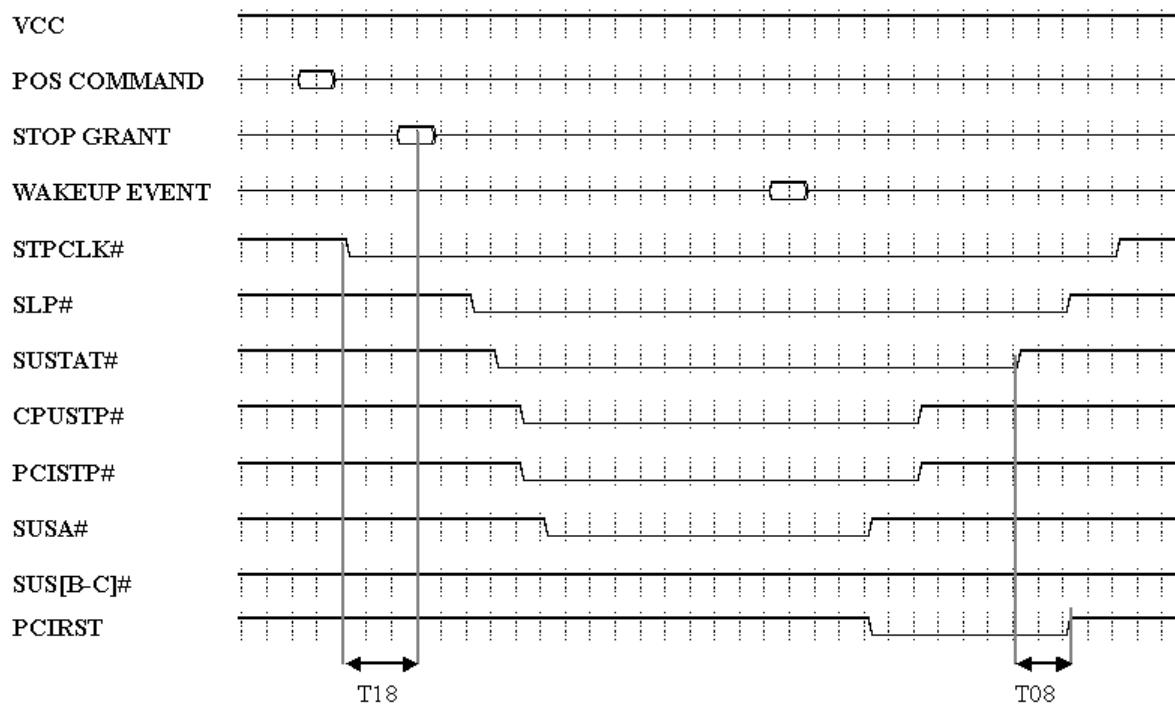


Figure 5. Power On Suspend & Resume Sequence with RESET

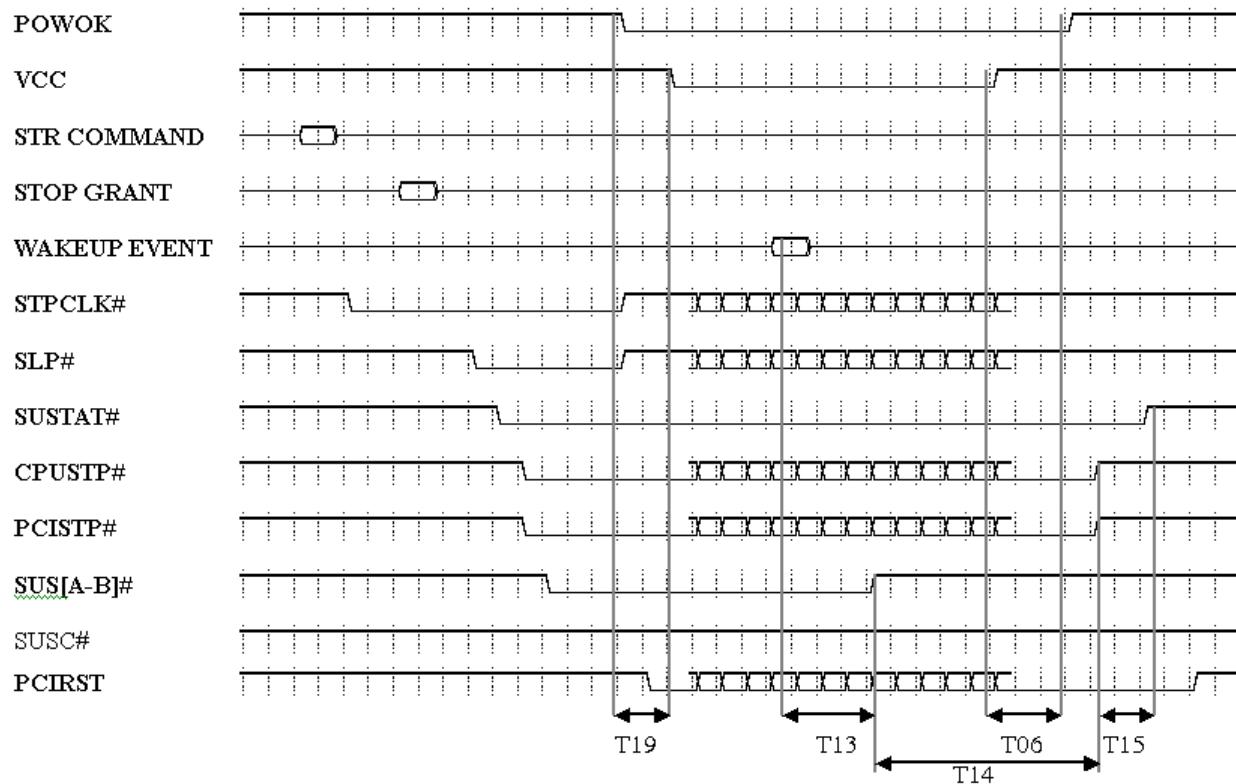
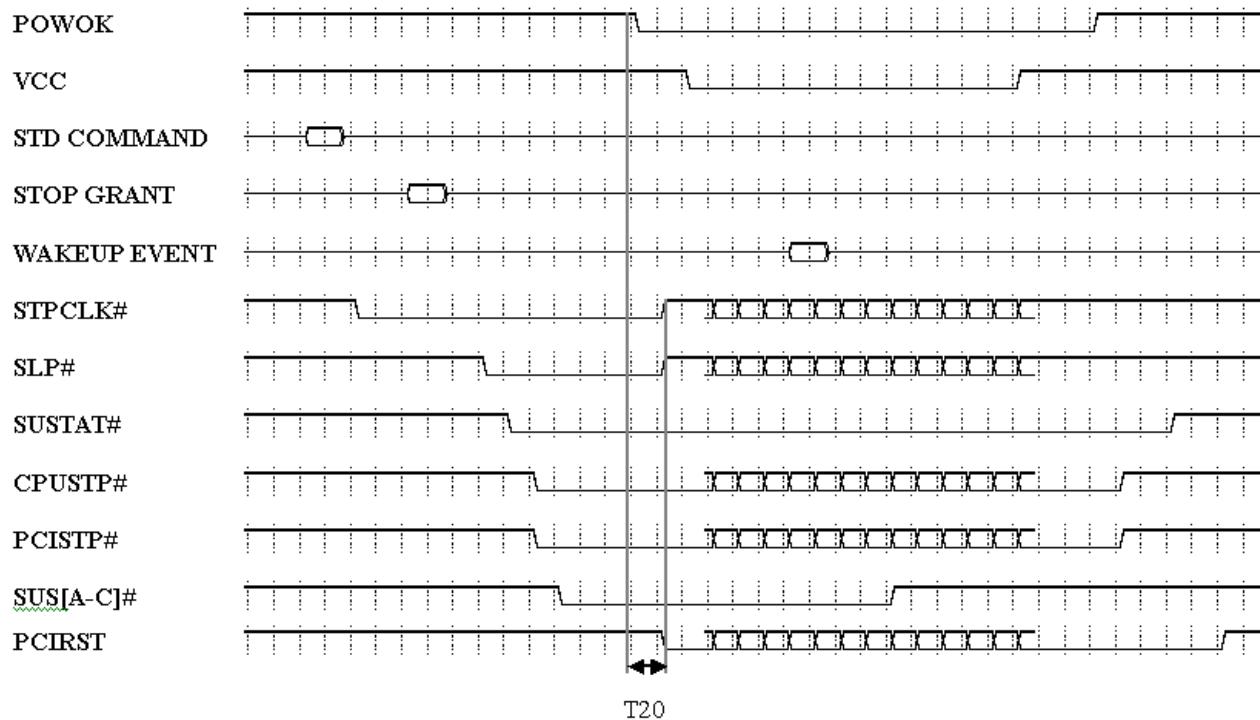
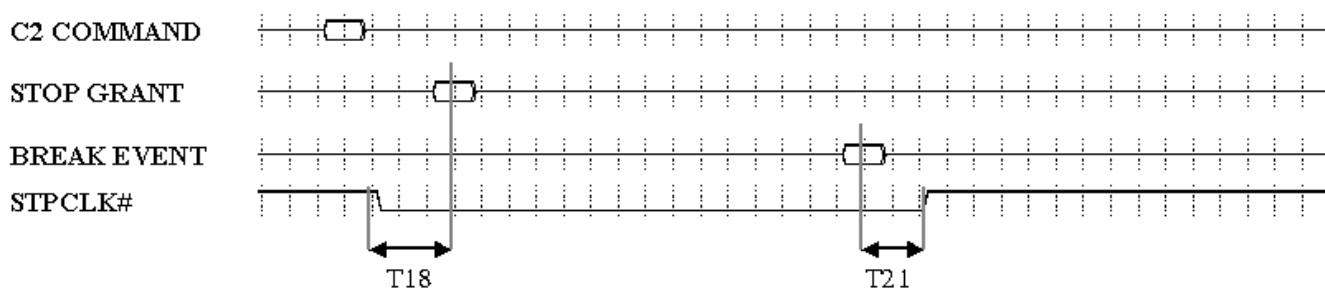


Figure 6. Suspend to RAM & Resume Sequence


Figure 7. Suspend to DISK & Resume Sequence

Figure 8. CPU C2 & Resume Sequence

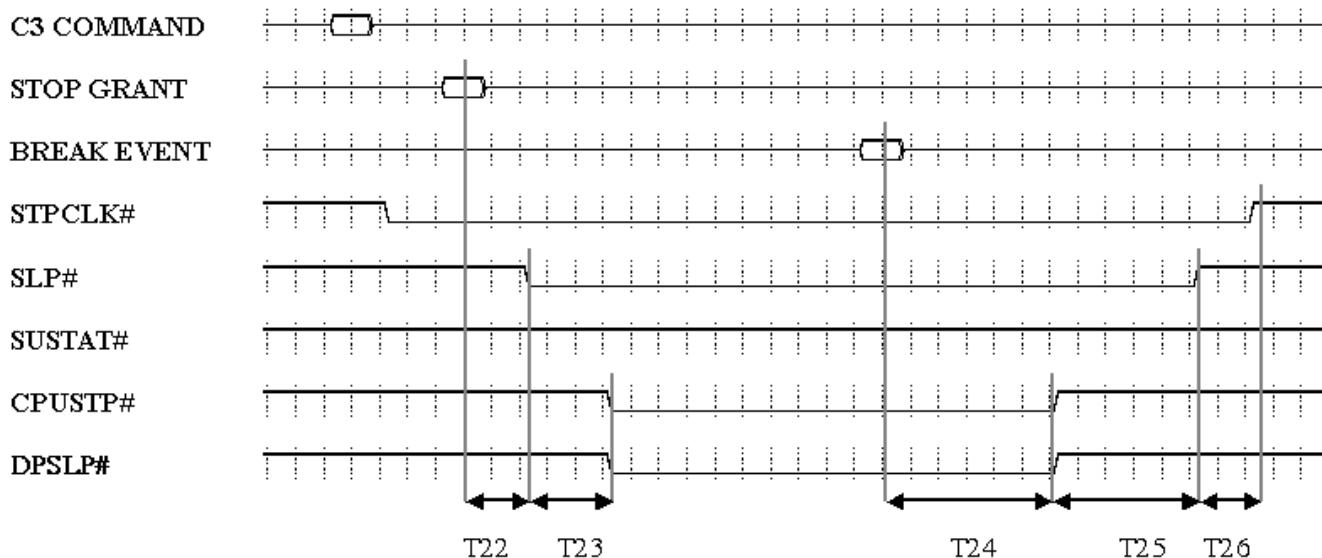


Figure 9. CPU C3 & Resume Sequence without SUSTAT#

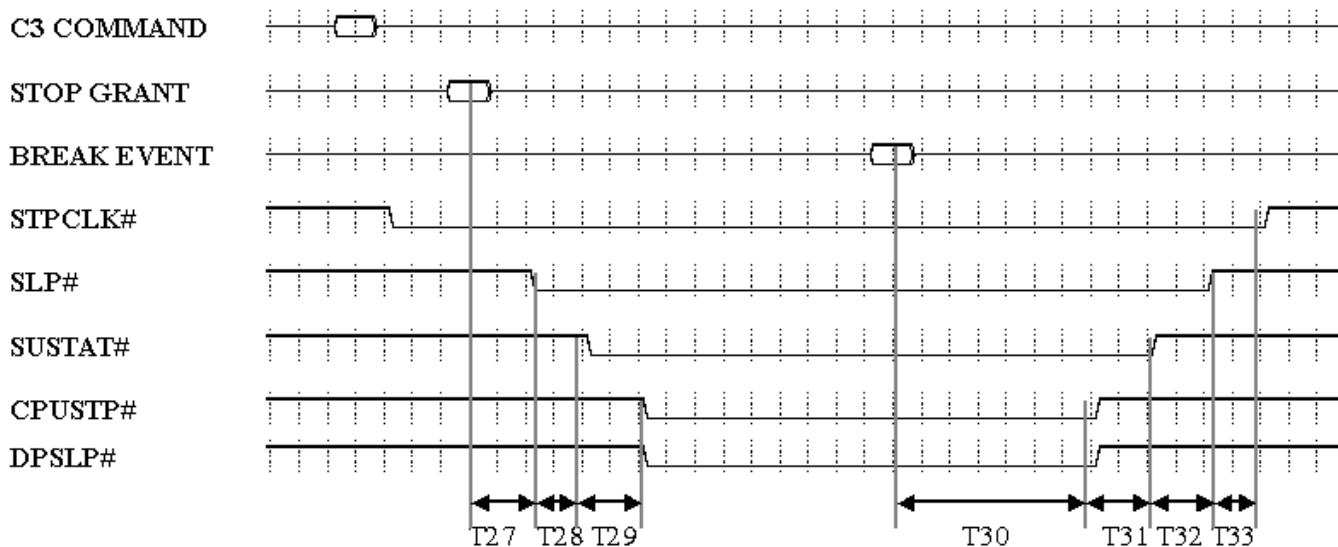


Figure 10. CPU C3 & Resume Sequence with SUSTAT#

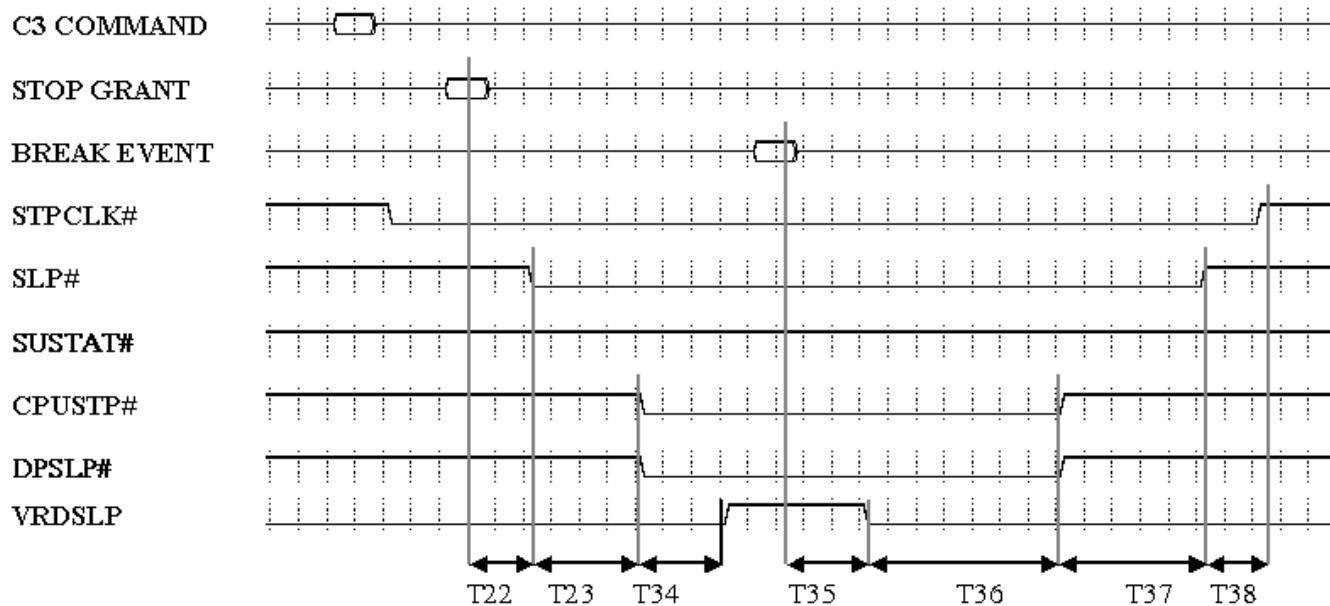


Figure 11. CPU C4 & Resume Sequence without SUSTAT#

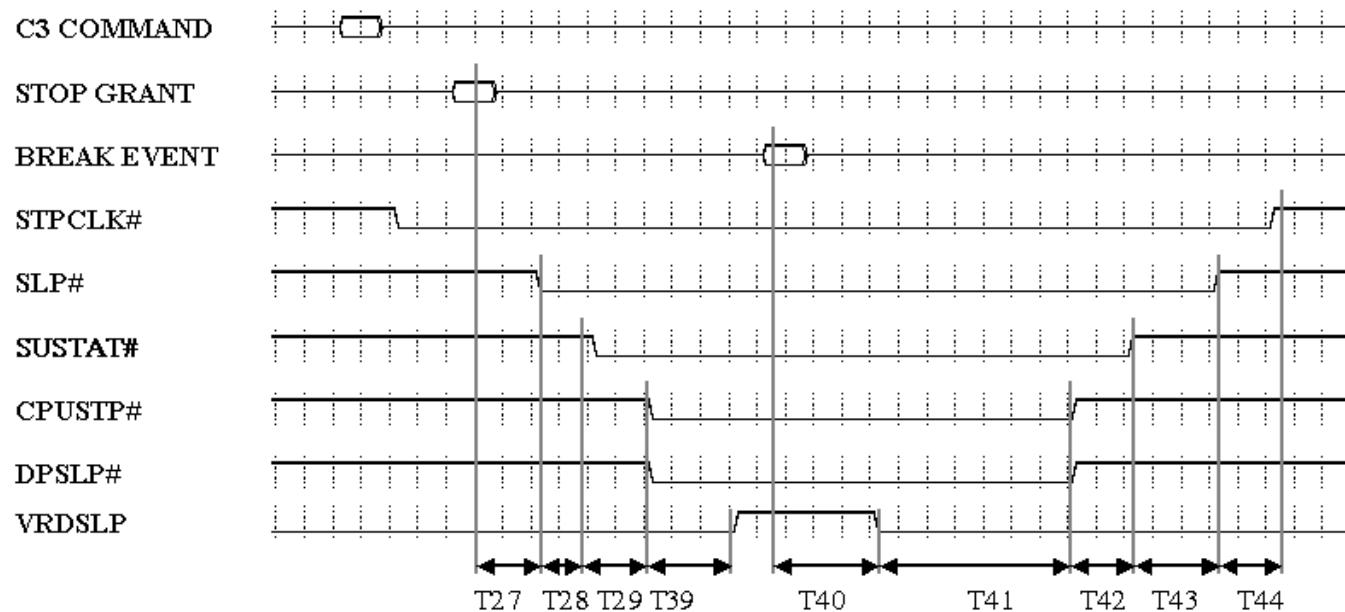
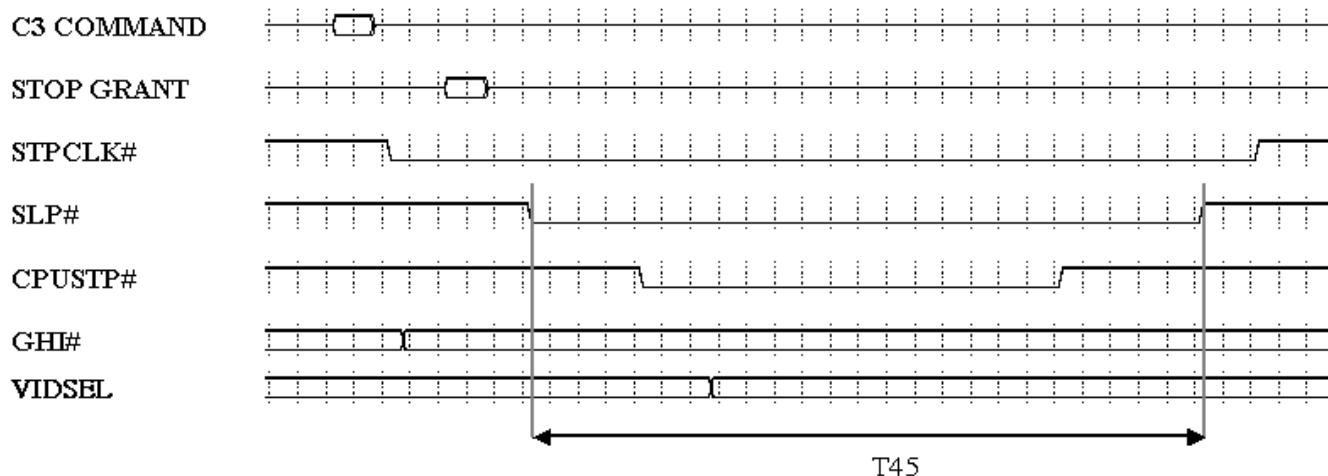


Figure 12. CPU C4 & Resume Sequence with SUSTAT#


Figure 13. CPU Speedstep & Resume Sequence
Table 13. Power Sequence

Symbol	Parameter	Min	Max	Unit	Note
T01	Vrtc supply active to Vsus supply active	0	—	ms	1
T02	Vsus supply active to RSMRST# inactive	10	—	ms	
T03	RSMRST# inactive to SUSCLK running	—	—	ms	
T04	PWRBTN# active width	1	—	RTCCLK	2
T05	PWRBTN# rising to SUS[A-C] inactive	4	5	RTCCLK	
T06	Vcc supply active to PWROK active	99	—	ms	
T07	PWROK active to SUSTAT# inactive	32	38	RTCCLK	
T08	SUSTAT# inactive to PCIRST# inactive	2	3	RTCCLK	
T09	STOP GRANT to SLP# active	—	1	RTCCLK	
T10	SLP# active to SUSTAT# active	—	1	RTCCLK	
T11	SUSTAT# active to CPUSTP# or PCISTP# active	—	1	RTCCLK	
T12	CPUSTP# or PCISTP# active to SUS[A-C] active	—	1	RTCCLK	
T13	WAKEUP event to SUS[A-C] inactive	—	2	RTCCLK	
T14	SUS[A-C] inactive to CPUSTP#/PCISTP# inactive	16	32	ms	3
T15	CPUSTP# and PCISTP# inactive to SUSTAT# inactive	1	2	ms	4
T16	SUSTAT# inactive to SLP# inactive	—	1	RTCCLK	5
T17	SLP# inactive to STPCLK# inactive	—	1	RTCCLK	6
T18	STPCLK# active to STOP GRANT command	N/A	N/A		7
T19	PWROK inactive to Vcc supply inactive	20	—	ns	
T20	PWROK inactive to SLP# or STPCLK# inactive	20	—	ns	
T21	Break event to STPCLK# inactive	2	—	PCICLK	
T22	STOP GRANT to SLP# active	7.5	—	us	
T23	SLP# active to CPUSTP# active	11.25	—	us	
T24	Break event to CPUSTP# inactive	7.5	—	us	
T25	CPUSTP# inactive to SLP# inactive	7.5	—	us	
T26	SLP# inactive to STPCLK# inactive	7.5	—	us	
T27	STOP GRANT to SLP# active	15	—	us	

Symbol	Parameter	Min	Max	Unit	Note
T28	SLP# active to SUSTAT# active	15	—	us	
T29	SUSTAT# active to CPUSTP# active	22.5	—	us	
T30	Break event to CPUSTP# inactive	15	—	us	
T31	CPUSTP# inactive to SUSTAT# inactive	15	—	us	
T32	SUSTAT# inactive to SLP# inactive	15	—	us	
T33	SLP# inactive to STPCLK# inactive	15	—	us	
T34	CPUSTP# active to VRDSLP active	3.75	—	us	
T35	Break event to VRDSLP inactive	—	7.5	us	
T36	VRDSLP inactive to CPUSTP# inactive	50	—	us	
T37	CPUSTP# inactive to SLP# inactive	7.5	—	us	
T38	SLP# inactive to STPCLK# inactive	7.5	—	us	
T39	CPUSTP# active to VRDSLP active	7.5	—	us	
T40	Break event to VRDSLP inactive	—	15	us	
T41	VRDSLP inactive to CPUSTP# inactive	100	—	us	
T42	CPUSTP# inactive to SUSTAT# inactive	15	—	us	
T43	SUSTAT# inactive to SLP# inactive	15	—	us	
T44	SLP# inactive to STPCLK# inactive	15	—	us	
T45	SLP# asserted time		—		8

Note :

1. The Vsus supplies never be active while the Vrtc supply is inactive. Likewise, the Vcc supplies must never be active while the Vsus supplies are inactive.
2. If PWRBTN de-bounce circuit enable through B0D17F0 Rx80[5], the minimum active time is 16 ms to filter out mechanical switch bounce.
3. If B0D17F0 Rx95[7] is set, the minimum delay is 1ms and the maximum delay is 2ms.
4. If B0D17F0 Rx95[7] is set, the minimum delay is 125 us and the maximum delay is 250 us.
5. SLP# is de-asserted if SUSTAT# is inactive or reset when PWROK is inactive.
6. STPCLK# is de-asserted if SLP# is inactive or reset when PWROK is inactive.
7. The STPCLK# assertion will trigger the processor to send a stop grant acknowledge cycle. The timing for this cycle is dependent on the processor and the memory controller.
8. {RxE5[7], RxE4[7], RxEC[2]}= {0,0,1}, min= 2.7 us, max=3.4 us
{RxE5[7], RxE4[7], RxEC[2]}= {0,0,0}, min= 120 us, max=160 us
{RxE5[7], RxE4[7], RxEC[2]}= {0,1,0}, min= 13 us, max=18 us
{RxE5[7], RxE4[7], RxEC[2]}= {1,0,0}, min= 240 us, max=290 us
{RxE5[7], RxE4[7], RxEC[2]}= {1,1,0}, min= 26 us, max=31 us

MECHANICAL SPECIFICATIONS

Y = Date Code Year
 W = Date Code Week
 V = Chip Version
 L = Lot Code

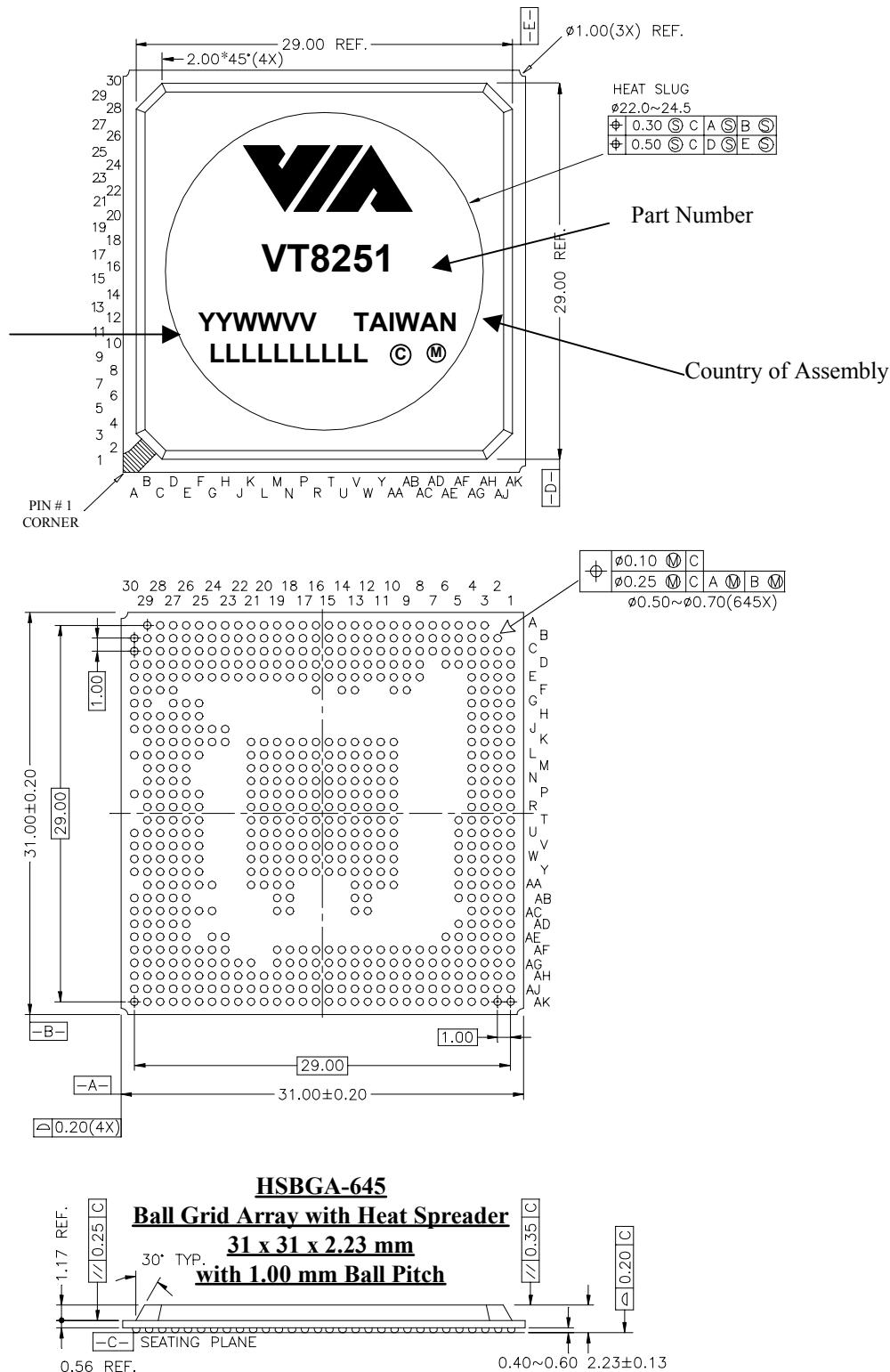


Figure 14. Mechanical Specifications – HSBGA-645 Ball Grid Array Package

Y = Date Code Year
 W = Date Code Week
 V = Chip Version
 L = Lot Code

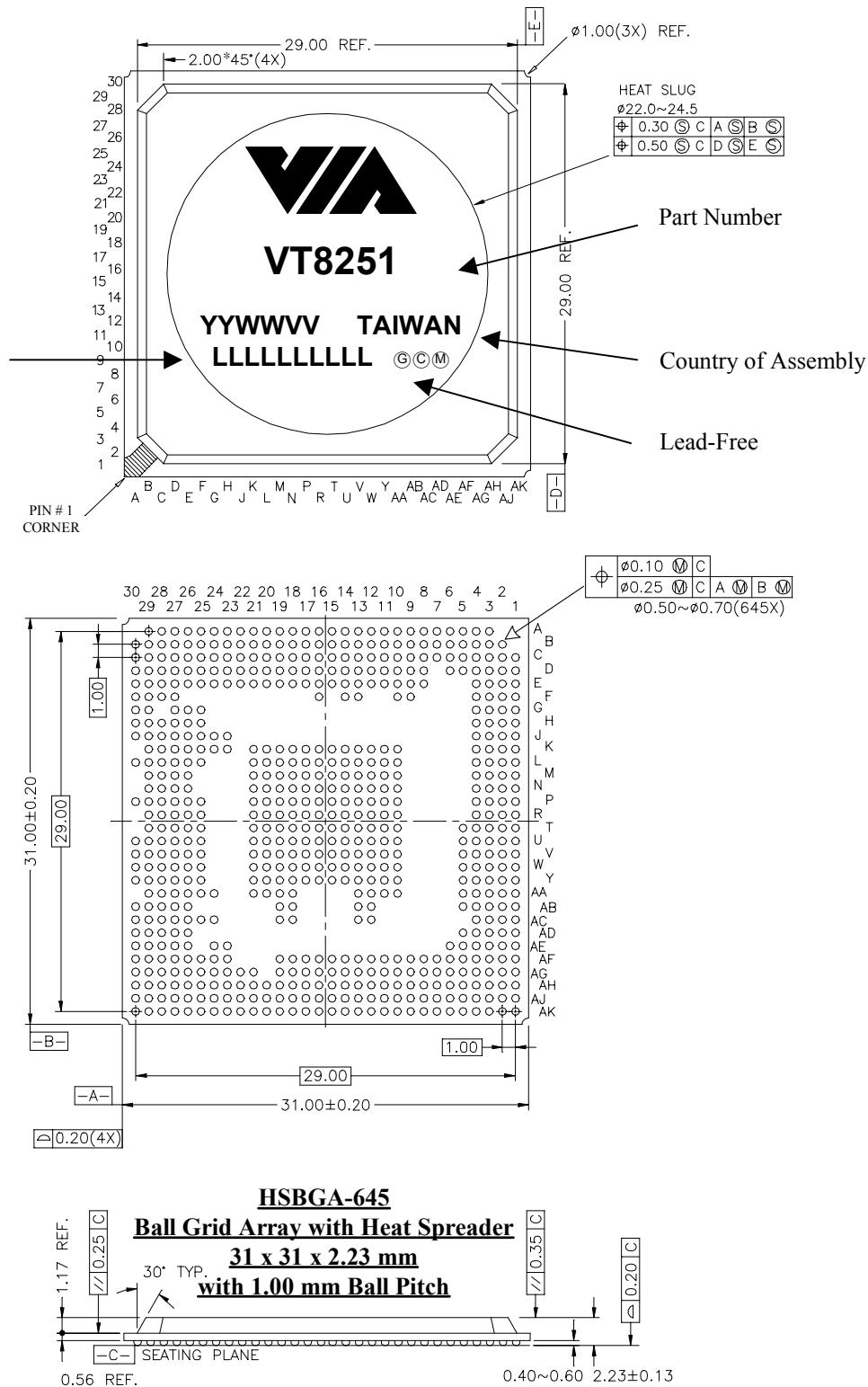


Figure 15. Lead-Free Mechanical Specifications – HSBGA-645 Ball Grid Array Package