



VT8363A

KT133A Athlon™ North Bridge

**Single-Chip North Bridge
for Socket-A Based Athlon™ CPUs
with 200 / 266 MHz Front Side Bus
for Desktop PC Systems
with AGP4x and PCI
plus Advanced Memory Controller
supporting PC133 / PC100 SDRAM & VCM**

**Preliminary Revision 0.1
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REVISION HISTORY

Document Release	Date	Revision	Initials
0.1	10/9/00	<p>Created from VT8363 data sheet rev 1.0</p> <p>Fixed typographical errors in GPIPE# and GRBF# pin descriptions</p> <p>Removed FPG/EDO information</p> <p>Updated Device 0 register descriptions: Rx8, 54[5-4], 55[4], 56-58, 60, 63[1-0], 67, 68[7,4-3,1-0], 69[7-6], 6C[5-4], 76[5-4], 79[7-3,0], 7B, 80[15-8], AC[6], AD[6-5], AF, B0[7], B2[3], B3, B5, B6[6-5], B8, F6</p> <p>Updated Device 1 register descriptions: Rx2, 34, 44[5]</p> <p>Removed ambient temp spec and changed case operating temp spec to 85 C</p> <p>Created separate table for power specs</p> <p>Fixed pin 1 orientation in mechanical diagram</p>	DH

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VIA VT8363A KT133A AMD ATHLON™ NORTH BRIDGE

Single-Chip North Bridge
for Socket-A (Socket-462) Based Athlon CPUs
with 200 / 266 MHz Front Side Bus
for Desktop PC Systems
with AGP 4x and PCI
plus Advanced Memory Controller
supporting PC133 / PC100 SDRAM and VCM

- **High Performance and High Integration Athlon AGP 4x / PC133 Chipset with Advanced System Power Management**

- **KT133A** Chipset: **VT8363A** system controller and **VT82C686A** PCI to ISA bridge
- Single chip Athlon system controller with 64-bit Socket-A Athlon CPU, 64-bit system memory, 32-bit PCI and 32-bit AGP interfaces
- PCI-to-ISA bridge chip includes UltraDMA-33/66 EIDE, 4 USB Ports, Integrated Super-I/O, AC97 / MC97 link (for Audio and Modem support), Hardware Monitoring, Power Management, and Keyboard / PS2-Mouse Interfaces plus RTC / CMOS on chip
- Supports separately powered 3.3V (5V tolerant) interface to system memory, AGP, and PCI bus
- Modular power management and clock control for advanced system power management

- **High Performance Athlon CPU Interface**

- Supports Socket-A (Socket-462) AMD Athlon processors with 200 and 266 MHz Front Side Bus
- HSTL-like 1.5V high-speed transceiver logic signal levels
- Independent address, data, and snoop interfaces
- 100 and 133 MHz DDR (Double Data Rate) transfer on Athlon CPU address and data buses
- Built-in PLL (Phase Lock Loop) circuitry for optimal skew control within and between clocking regions
- Four-entry command queue to accommodate maximum CPU throughput
- Four-entry probe queue to stores probes from the system to the processor
- Twenty four-entry processor system data and control queue to store system data control commands in two separate read and write buffers for data movement in and out of processor interface
- Supports WC (Write Combining) cycles
- Sleep mode support
- System management interrupt, memory remap and STPCLK mechanism

• Full Featured Accelerated Graphics Port (AGP) Controller

- Synchronous and pseudo-synchronous with the host CPU bus with optimal skew control

<u>PCI</u>	<u>AGP</u>	<u>CPU</u>	<u>Mode</u>
33 MHz	66 MHz	100 MHz DDR	3x synchronous
- AGP v2.0 compliant
- Supports SideBand Addressing (SBA) mode (non-multiplexed address / data)
- Supports 66 MHz 1x, 2x and 4x modes for AD and SBA signaling
- Pipelined split-transaction long-burst transfers up to 1GB/sec
- Thirty-two level read request queue
- Four level posted-write request queue
- Thirty-two level (quadwords) read data FIFO (256 bytes)
- Sixteen level (quadwords) write data FIFO (128 bytes)
- Intelligent request reordering for maximum AGP bus utilization
- Supports Flush/Fence commands
- Graphics Address Relocation Table (GART)
 - One level TLB structure
 - Sixteen entry fully associative page table
 - LRU replacement scheme
- Windows 95 OSR-2 VXD and integrated Windows 98 / Windows 2000 miniport driver support

• Concurrent PCI Bus Controller

- PCI buses are synchronous / pseudo-synchronous to host CPU bus
- 33 MHz operation on the primary PCI bus
- 66 MHz PCI operation on the AGP bus
- PCI-to-PCI bridge configuration on the 66MHz PCI bus
- Supports up to five PCI masters
- Peer concurrency
- Concurrent multiple PCI master transactions; i.e., allow PCI masters from both PCI buses active at the same time
- Zero wait state PCI master and slave burst transfer rate
- PCI to system memory data streaming up to 132Mbyte/sec
- Two lines (32 double-words) of CPU to PCI posted write buffers
- Byte merging in the write buffers to reduce the number of PCI cycles and to create further PCI bursting possibilities
- Enhanced PCI command optimization (MRL, MRM, MWI, etc.)
- Thirty-two levels (double-words) of post write buffers from PCI masters to DRAM
(two cache lines / 16 double-words for PCI bus, two cache lines / 16 double-words for Athlon processor interface)
- Sixteen levels (double-words) of prefetch buffers from DRAM for access by PCI masters
- Delay transaction from PCI master accessing DRAM
- Read caching for PCI master reading DRAM
- Transaction timer for fair arbitration between PCI masters (granularity of two PCI clocks)
- Symmetric arbitration between Host/PCI bus for optimized system performance
- Complete steerable PCI interrupts
- PCI-2.2 compliant, 32 bit 3.3V PCI interface with 5V tolerant inputs

- **Advanced High-Performance DRAM Controller**

- Supports PC133 and PC100 SDRAM and Virtual Channel Memory (VCM) SDRAM up to 3 DIMMs
- Concurrent CPU, AGP, and PCI access
- Different DRAM types may be used in mixed combinations
- Different DRAM timing for each bank
- Dynamic Clock Enable (CKE) control for SDRAM power reduction in high speed systems
- Mixed 1M / 2M / 4M / 8M / 16M / 32MxN DRAMs
- Support up to 1.5 GB memory space (256Mb DRAM technology)
- Flexible row and column addresses
- 64-bit data width and 3.3V DRAM interface
- Programmable I/O drive capability for MA, command, and MD signals
- Two-bank interleaving for 16Mbit SDRAM support
- Two-bank and four bank interleaving for 64Mbit SDRAM support
- Supports maximum 16-bank interleave (i.e., 16 pages open simultaneously); banks are allocated based on LRU
- Independent SDRAM control for each bank
- Seamless DRAM command scheduling for maximum DRAM bus utilization (e.g., precharge other banks while accessing the current bank)
- Four cache lines (32 quadwords) of CPU to DRAM write buffers
- Four cache lines (32 quadwords) of CPU to DRAM read prefetch buffers
- Read around write capability for non-stalled CPU read
- Burst read and write operation
- BIOS shadow at 16KB increment
- Decoupled and burst DRAM refresh with staggered RAS timing
- CAS before RAS or self refresh

- **Advanced System Power Management Support**

- Dynamic power down of SDRAM (CKE)
- PCI and AGP bus clock run and clock generator control
- VTT suspend power plane preserves memory data
- Suspend-to-DRAM and Self-Refresh operation
- SDRAM self-refresh power down
- 8 bytes of BIOS scratch registers
- Low-leakage I/O pads

- **Built-in NAND-tree pin scan test capability**

- **3.3V, 0.35um, high speed / low power CMOS process**

- **35 x 35 mm, 552 pin BGA Package**

OVERVIEW

The **KT133A** chipset (**VT8363A** north bridge and **VT82C686A** south bridge) is a high performance, cost-effective and energy efficient system controller for the implementation of AGP / PCI / ISA desktop personal computer systems based on 64-bit Socket-A (AMD Athlon) processors. The VT8363A supports FSB speeds of 200 and 266 MHz.

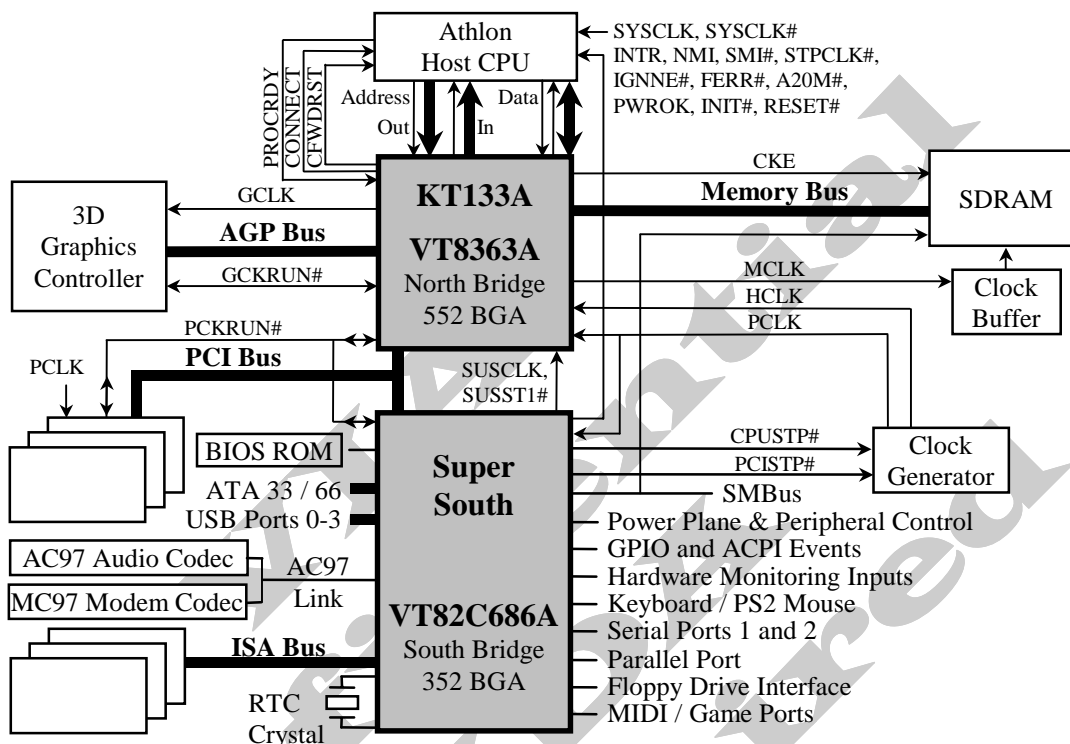


Figure 1. KT133A System Block Diagram Using the VT82C686A South Bridge

The KT133A chip set consists of the VT8363A system controller (552 pin BGA) and the VT82C686A PCI to ISA bridge (352 pin BGA). The system controller provides superior performance between the CPU, DRAM, AGP bus, and PCI bus with pipelined, burst, and concurrent operation.

The VT8363A supports eight banks of DRAMs up to 1.5 GB. The DRAM controller supports standard Synchronous DRAM (SDRAM) and Virtual Channel SDRAM (VC SDRAM), in a flexible mix / match manner. The Synchronous DRAM interface allows zero wait state bursting between the DRAM and the data buffers at 66/100/133 MHz. The six banks of DRAM can be composed of an arbitrary mixture of 1M / 2M / 4M / 8M / 16M / 32MxN DRAMs.

The VT8363A system controller also supports full AGP v2.0 capability for maximum bus utilization including 1x, 2x and 4x mode transfers, SBA (SideBand Addressing), Flush/Fence commands, and pipelined grants. An eight level request queue plus a four level post-write request queue with thirty-two and sixteen quadwords of read and write data FIFO's respectively are included for deep pipelined and split AGP transactions. A single-level GART TLB with 16 full associative entries and flexible CPU / AGP / PCI remapping control is also provided for operation under protected mode operating environments. Both Windows-95 VXD and Windows-98 / Windows 2000 miniport drivers are supported for interoperability with major AGP-based 3D and DVD-capable multimedia accelerators.

The VT8363A supports two 32-bit 3.3 / 5V system buses (one AGP and one PCI) that are synchronous / pseudo-synchronous to the CPU bus. The chip also contains a built-in bus-to-bus bridge to allow simultaneous concurrent operations on each bus. Five levels (doublewords) of post write buffers are included to allow for concurrent CPU and PCI operation. For PCI master operation, forty-eight levels (doublewords) of post write buffers and sixteen levels (doublewords) of prefetch buffers are included for concurrent PCI bus and DRAM/cache accesses. The chip also supports enhanced PCI bus commands such as Memory-Read-Line, Memory-

Read-Multiple and Memory-Write-Invalid commands to minimize snoop overhead. In addition, advanced features are supported such as snoop ahead, snoop filtering, L1/L2 write-back forward to PCI master, and L1/L2 write-back merged with PCI post write buffers to minimize PCI master read latency and DRAM utilization. Delay transaction and read caching mechanisms are also implemented for further improvement of overall system performance.

The 352-pin Ball Grid Array VT82C686A PCI to ISA bridge supports four levels (doublewords) of line buffers, type F DMA transfers and delay transaction to allow efficient PCI bus utilization and (PCI-2.1 compliant). The VT82C686A also includes an integrated keyboard controller with PS2 mouse support, integrated DS12885 style real time clock with extended 256 byte CMOS RAM, integrated master mode enhanced IDE controller with full scatter / gather capability and extension to UltraDMA-33/66 for 33/66 MB/sec transfer rate, integrated USB interface with root hub and four function ports with built-in physical layer transceivers, Distributed DMA support, and OnNow / ACPI compliant advanced configuration and power management interface. The VT82C686A also includes an AC97 / MC97 link for interface to external audio and modem codecs, and all "Super-I/O" functions (serial ports, parallel port, and floppy drive interface and game port).

For sophisticated power management, KT133A provides independent clock stop control for the CPU / SDRAM, PCI, and AGP buses and Dynamic CKE control for powering down of the SDRAM. A separate suspend-well plane is implemented for the SDRAM control signals for Suspend-to-DRAM operation. The VT82C686A also includes a complete hardware monitoring subsystem for monitoring and control of internal and external (motherboard and system) conditions including voltages, temperatures, fan speeds, switch open/close states, etc. Coupled with the VT82C686A south bridge chip, a complete power conscious PC main board can be implemented with no external TTLs.

The KT133A chipset is ideal for high performance, high quality, high energy efficient and high integration desktop AGP / PCI / ISA computer systems.

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PINOUTS

Figure 2. VT8363A KT133A Ball Diagram (Top View)

Key	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	
A	NC	GND	AIN 14#	AIN CLK#	AIN 9#	AIN 3#	AIN 11#	D11#	D0#	DICLK 0#	D5#	D7#	D18#	D20#	D22#	D40#	D43#	D44#	D47#	D56#	D59#	D62#	DICLK 3#	D49#	DOCLK 3#	AOUT 3#	
B	NC	NC	AIN 12#	GND	AIN 13#	AIN 2#	GND	D9#	D3#	GND	D4#	D6#	GND	D19#	DOCLK 1#	GND	D42#	DICLK 2#	GND	D39#	D60#	GND	D63#	D53#	GND	AOUT 2#	
C	NC	NC	NC	PROC RDY	AIN 10#	AIN 4#	AIN 5#	D14#	D13#	D2#	D25#	D16#	D17#	D21#	D23#	D41#	D34#	D45#	D38#	D57#	D58#	D52#	D55#	AOUT 4#	AOUT 6#	AOUT 9#	
D	NC	NC	NC	NC	CONNECT	VTT	AIN 6#	DOCLK 0#	VTT	D12#	D15#	VTT	D28#	D29#	VTT	D30#	D33#	VTT	D37#	D36#	VTT	D54#	AOUT 11#	AOUT 10#	AOUT CLK#	AOUT 12#	
E	NC	NC	NC	NC	CKFDRST	DIN VAL#	AIN 8#	AIN 7#	D10#	D8#	D1#	D27#	D26#	D31#	DICLK 1#	DOCLK 2#	D35#	D51#	D46#	D48#	D61#	S2K COMP	VTT	AOUT 5#	VTT	AOUT 7#	
F	SCAN IN1	SCAN IN0	NC	NC	SCAN IN2	VCC3	GND	VTT	GND	S2K VREF	VTT	GND	D24#	VTT	D32#	GND	VTT	D50#	GND	S2K VREF	S2K GND	S2K VCC	S2K VREF	AOUT 8#	AOUT 13#	AOUT 14#	
G	NC	SCAN IN3	GND	NC	NC	SCAN OUT1	G7	8	9	10	11	12	13	14	15	16	17	18	19	G20	GND HCK	HCLK	MD1	MD32	MD0	MD33	
H	SCAN IN4	SCAN IN5	SCAN OUT0	NC	SCAN OUT2	VCC3	H	CPU Pins										H									
J	SCAN ENA	SCAN IN7	SCAN IN6	DFT IN	NC	GND	J	VCC3 VTT VCC3 VCC3 VTT VTT VCC3 VCC3 VTT VTT										J									
K	SCAN OUT4	SCAN OUT5	SCAN OUT6	NC	NC	SCAN OUT3	K	VCC3 K10 11 12 13 14 15 16 K17 VCC3										K									
L	P GNT#	SCAN OUT7	GND	P REQ#	NC	VCC3	L	VCC3 L GND GND GND GND GND GND L VCC3										L									
M	GNT 3#	REQ 4#	GNT 4#	REQ 3#	GNT 0#	GND	M	VCC3 M GND GND GND GND GND GND M VCC3										M									
N	REQ 1#	GNT 1#	REQ 2#	VCC3	GNT 2#	REQ 0#	N	PCI Pins VCC3 N GND GND GND GND GND GND N VCC3										DRAM Pins N									
P	AD29	AD26	AD25	AD31	AD28	VCC3	P	VCC3 P GND GND GND GND GND GND P VCC3										Pins P									
R	AD24	AD23	GND	AD30	AD27	GND	R	VCC3 R GND GND GND GND GND GND R VCC3										R									
T	AD20	AD22	CBE 3#	AD21	FRM#	I RDY#	T	VCC3 T GND GND GND GND GND GND T VCC3										T									
U	AD16	AD18	AD19	AD17	CBE 2#	WSC#	U	VCC3 U10 11 12 13 14 15 16 U17 VCC3										U									
V	LOCK#	SERR#	DEV SEL#	STOP#	T RDY#	VCC3	V	VCC Q VCC3 VCC Q VCC Q VCC3 VCC Q VCC3 VCC Q VCC3 VCC3										V									
W	AD15	PAR	GND	CBE 1#	AD10	GND	W	AGP Pins										W									
Y	AD13	AD11	AD12	AD14	AD9	GND	Y7	8	9	10	11	12	13	14	15	16	17	18	19	Y20	GND	CS4#	CS5#	GND	CS0#	CS1#	
AA	CBE0#	AD8	AD7	AD6	PCLK	VCC3	VCC Q	GND	GRBF#	VCC Q	GND	VCC Q	GND	VCC GCK	VCC Q	GND	VCC QQ	VCC Q	GND	VSUS 3	VCC3	DQM 1	DQM 0	DQM 5	CS3#	CS2#	
AB	AD4	AD5	GND	PCK RUN#	RE SET#	G GNT#	GDS1 1	ST1	ST2	G FRM#	GI RDY#	G STOP#	G DSEL#	G CLK	GND GCK	GD2	GND QQ	N COMP	SUS ST#	MD62	MD58	MD16	MD48	SWEA# strap	CKE0 SWEC#	DQM 4	
AC	AD2	AD3	AD0	AD1	VCC Q	ST0	GDS 1#	VCC Q	G PIPE#	G WBF#	VCC Q	GT RDY#	G PAR	VCC Q	GCLK F	GD8	VCC Q	P COMP	PWR OK	MD59	MD26	MD56	MD21	MD17	MD49	CKE2 SWEB#	
AD	SBA 1	SBA 0	SBA 3	SBA 7	G REQ#	GD30	GD26	GBE 3#	GD23	GD19	GD17	GBE 1#	GD12	GD11	GDS0	GBE 0#	GD4	GD1	MD30	MD28	GND	MD24	MD22	GND	MD18	MD50	
AE	SBA 2	GND	SBA 5	SBA 6	GND	GD28	GD25	GND	GD21	GD18	GND	GBE 2#	GD14	GND	GDS0#	GD6	GND	GD0	MD63	MD61	MD27	MD25	MD55	MD53	MD19	MD51	
AF	SBS	SBS#	SBA 4	GD31	GD29	GD27	GD24	GD22	GD20	AGP VREF	GD16	GD15	GD13	GD10	GD9	GD7	GD5	GD3	MD31	MD29	MD60	MD57	MD23	MD54	MD20	MD52	

Table 1. VT8363A KT133A Pin List (Numerical Order)

Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name
A01	NC	D03	NC	G05	NC	P01	IO AD29	Y23	O CS5# / RAS5#	AC25	IO MD49
A02	P GND	D04	NC	G06	O SCANOUT1	P02	IO AD26	Y24	P GND	AC26	O CKE2 / SWE#
A03	O AIN14#	D05	O CONNECT	G21	P GNDHCK	P03	IO AD25	Y25	O CS0# / RAS0#	AD01	I SBA1
A04	O AINCLK#	D06	P VTT	G22	I HCLK	P04	IO AD31	Y26	O CS1# / RAS1#	AD02	I SBA0
A05	O AIN09#	D07	O AIN06#	G23	IO MD01	P05	IO AD28	AA01	IO CBE0#	AD03	I SBA3
A06	O AIN03#	D08	I DOCLK0#	G24	IO MD32	P06	P VCC3	AA02	IO AD08	AD04	I SBA7
A07	O AIN11#	D09	P VTT	G25	IO MD00	P21	P GNDMCK	AA03	IO AD07	AD05	I GREO#
A08	IO D11#	D10	IO D12#	G26	IO MD33	P22	P VCCMCK	AA04	IO AD06	AD06	IO GD30
A09	IO D00#	D11	IO D15#	H01	I SCANIN4	P23	I MCLKF	AA05	I PCLK	AD07	IO GD26
A10	O DICLK0#	D12	P VTT	H02	I SCANIN5	P24	IO MD15	AA06	P VCC3	AD08	IO GBE3#
A11	IO D05#	D13	IO D28#	H03	O SCANOUT0	P25	O SCAS# / strap	AA07	P VCCQ	AD09	IO GD23
A12	IO D07#	D14	IO D29#	H04	NC	P26	O CKE3 / SCASB#	AA08	P GND	AD10	IO GD19
A13	IO D18#	D15	P VTT	H05	O SCANOUT2	R01	IO AD24	AA09	I GRBF#	AD11	IO GD17
A14	IO D20#	D16	IO D30#	H06	P VCC3	R02	IO AD23	AA10	P VCCQ	AD12	IO GBE1#
A15	IO D22#	D17	IO D33#	H21	P GND	R03	P GND	AA11	P GND	AD13	IO GD12
A16	IO D40#	D18	P VTT	H22	P VCCHCK	R04	IO AD30	AA12	P VCCQ	AD14	IO GD11
A17	IO D43#	D19	IO D37#	H23	I TESTIN	R05	IO AD27	AA13	P GND	AD15	IO GD50
A18	IO D44#	D20	IO D36#	H24	IO MD34	R06	P GND	AA14	P VCCGCK	AD16	IO GBE0#
A19	IO D47#	D21	P VTT	H25	IO MD35	R21	P VCC3	AA15	P VCCO	AD17	IO GD4
A20	IO D56#	D22	IO D54#	H26	IO MD02	R22	O MCLK	AA16	P GND	AD18	IO GD1
A21	IO D59#	D23	I AOUT11#	J01	I SCANENA	R23	O DOM2 / CAS2#	AA17	P VCCO	AD19	IO MD30
A22	IO D62#	D24	I AOUT10#	J02	I SCANIN7	R24	O DQM7 / CAS7#	AA18	P VCCQ	AD20	IO MD28
A23	O DICLK3#	D25	I AOUTCLK#	J03	I SCANIN6	R25	O CKE1 / SCASC#	AA19	P GND	AD21	P GND
A24	IO D49#	D26	I AOUT12#	J04	I DFTIN	R26	O DQM3 / CAS3#	AA20	P VSUS3	AD22	IO MD24
A25	I DOCLK3#	E01	NC	J05	NC	T01	IO AD20	AA21	P VCC3	AD23	IO MD22
A26	I AOUT03#	E02	NC	J06	P GND	T02	IO AD22	AA22	O DQM1 / CAS1#	AD24	P GND
B01	NC	E03	NC	J21	P VCC3	T03	IO CBE3#	AA23	O DOM0 / CAS0#	AD25	IO MD18
B02	NC	E04	NC	J22	IO MD04	T04	IO AD21	AA24	O DQM5 / CAS5#	AD26	IO MD50
B03	O AIN12#	E05	O CFWDRST	J23	IO MD06	T05	IO FRAME#	AA25	O CS3# / RAS3#	AE01	I SBA2
B04	P GND	E06	O DINVAL#	J24	P GND	T06	IO IRDY#	AA26	O CS2# / RAS2#	AE02	P GND
B05	O AIN13#	E07	O AIN08#	J25	IO MD03	T21	P GND	AB01	IO AD04	AE03	I SBA5
B06	O AIN02#	E08	O AIN07#	J26	IO MD36	T22	O MA03 / strap	AB02	IO AD05	AE04	I SBA6
B07	P GND	E09	IO D10#	K01	O SCANOUT4	T23	P VCC3	AB03	P GND	AE05	P GND
B08	IO D09#	E10	IO D08#	K02	O SCANOUT5	T24	P GND	AB04	IO PCKRUN#	AE06	IO GD28
B09	IO D03#	E11	IO D01#	K03	O SCANOUT6	T25	O CKE4 / SRASC#	AB05	I RESET#	AE07	IO GD25
B10	P GND	E12	IO D27#	K04	NC	T26	O DQM6 / CAS6#	AB06	O GGNT#	AE08	P GND
B11	IO D04#	E13	IO D26#	K05	NC	U01	IO AD16	AB07	IO GDS1	AE09	IO GD21
B12	IO D06#	E14	IO D31#	K06	O SCANOUT3	U02	IO AD18	AB08	O ST1	AE10	IO GD18
B13	P GND	E15	O DICLK1#	K21	P VCC3	U03	IO AD19	AB09	O ST2	AE11	P GND
B14	IO D19#	E16	I DOCLK2#	K22	IO MD39	U04	IO AD17	AB10	IO GFRM#	AE12	IO GBE2#
B15	I DOCLK1#	E17	IO D35#	K23	IO MD07	U05	IO CBE2#	AB11	IO GIRDY#	AE13	IO GD14
B16	P GND	E18	IO D51#	K24	IO MD37	U06	O WSC#	AB12	IO GSTOP#	AE14	P GND
B17	IO D42#	E19	IO D46#	K25	IO MD05	U21	O MA07 / strap	AB13	IO GDSSEL#	AE15	IO GD50#
B18	O DICLK2#	E20	IO D48#	K26	IO MD38	U22	O MA05 / strap	AB14	O GCLK	AE16	IO GD6
B19	P GND	E21	IO D61#	L01	O PGNT#	U23	O MA01# / strap	AB15	P GNDGCK	AE17	P GND
B20	IO D39#	E22	I S2KCOMP	L02	O SCANOUT7	U24	O MA00 / strap	AB16	IO GD2	AE18	IO GD0
B21	IO D60#	E23	P VTT	L03	P GND	U25	O SRASA# / strap	AB17	P GNDQ	AE19	IO MD63
B22	P GND	E24	I AOUT05#	L04	I PREQ#	U26	O CKE5 / SRASB#	AB18	I NCMP	AE20	IO MD61
B23	IO D63#	E25	P VTT	L05	NC	V01	IO LOCK#	AB19	I SUSST#	AE21	IO MD27
B24	IO D53 #	E26	I AOUT07#	L06	P VCC3	V02	IO SERR#	AB20	IO MD62	AE22	IO MD25
B25	P GND	F01	I SCANIN1	L21	P GND	V03	IO DEVSEL#	AB21	IO MD58	AE23	IO MD55
B26	I AOUT02#	F02	I SCANIN0	L22	IO MD09	V04	IO STOP#	AB22	IO MD16	AE24	IO MD53
C01	NC	F03	NC	L23	IO MD42	V05	IO TRDY#	AB23	IO MD48	AE25	IO MD19
C02	NC	F04	NC	L24	IO MD40	V06	P VCC3	AB24	O SWEA# / strap	AE26	IO MD51
C03	NC	F05	I SCANIN2	L25	IO MD08	V21	P VCC3	AB25	O CKE0 / SWEC#	AF01	I SBS
C04	I PROCRDY	F06	P VCC3	L26	IO MD41	V22	O MA06 / strap	AB26	O DQM4 / CAS4#	AF02	I SBS#
C05	O AIN10#	F07	P GND	M01	O GNT3#	V23	O MA04 / strap	AC01	IO AD02	AF03	I SBA4
C06	O AIN04#	F08	P VTT	M02	I REQ4#	V24	O MA09 / strap	AC02	IO AD03	AF04	IO GD31
C07	O AIN05#	F09	P GND	M03	O GNT4#	V25	O MA08 / strap	AC03	IO AD00	AF05	IO GD29
C08	IO D14#	F10	P S2KVREF	M04	I REQ3#	V26	O MA02 / strap	AC04	IO AD01	AF06	IO GD27
C09	IO D13#	F11	P VTT	M05	O GNT0#	W01	IO AD15	AC05	P VCCO	AF07	IO GD24
C10	IO D02#	F12	P GND	M06	P GND	W02	IO PAR	AC06	O ST0	AF08	IO GD22
C11	IO D25#	F13	IO D24#	M21	P VCC3	W03	P GND	AC07	IO GDS1#	AF09	IO GD20
C12	IO D16#	F14	P VTT	M22	IO MD45	W04	IO CBE1#	AC08	P VCCQ	AF10	P AGPVREF
C13	IO D17#	F15	IO D32#	M23	IO MD10	W05	IO AD10	AC09	I GPIPE#	AF11	IO GD16
C14	IO D21#	F16	P GND	M24	P GND	W06	P GND	AC10	I GWBF#	AF12	IO GD15
C15	IO D23#	F17	P VTT	M25	IO MD11	W21	P VCC3	AC11	P VCCO	AF13	IO GD13
C16	IO D41#	F18	IO D50#	M26	IO MD43	W22	O MA14 / strap	AC12	IO GTRDY#	AF14	IO GD10
C17	IO D34#	F19	P GND	N01	I REO1#	W23	O MA13 / strap	AC13	IO GPAR /	AF15	IO GD9
C18	IO D45#	F20	P S2KVREF	N02	O GNT1#	W24	O MA12 / strap	AC14	P VCCQ	AF16	IO GD7
C19	IO D38#	F21	P S2KGND	N03	I REQ2#	W25	O MA11 / strap	AC15	I GCLKF	AF17	IO GD5
C20	IO D57#	F22	P S2KVCC	N04	P VCC3	W26	O MA10 / strap	AC16	IO GD8	AF18	IO GD3
C21	IO D58#	F23	P CLKVREF	N05	O GNT2#	Y01	IO AD13	AC17	P VCCO	AF19	IO MD31
C22	IO D52#	F24	I AOUT08#	N06	I REQ0#	Y02	IO AD11	AC18	I PCOMP	AF20	IO MD29
C23	IO D55#	F25	I AOUT13#	N21	IO MD13	Y03	IO AD12	AC19	I PWROK	AF21	IO MD60
C24	I AOUT04#	F26	I AOUT14#	N22	IO MD14	Y04	IO AD14	AC20	IO MD59	AF22	IO MD57
C25	I AOUT06#	G01	NC	N23	IO MD46	Y05	IO AD09	AC21	IO MD26	AF23	IO MD23
C26	I AOUT09#	G02	I SCANIN3	N24	IO MD47	Y06	P GND	AC22	IO MD56	AF24	IO MD54
D01	NC	G03	P GND	N25	IO MD44	Y21	P GND	AC23	IO MD21	AF25	IO MD20
D02	NC	G04	NC	N26	IO MD12	Y22	O CS4# / RAS4#	AC24	IO MD17	AF26	IO MD52

Center VCC25 Pins (26 pins): J9,11-12,15-16, K9,18, L9,18, M9,18, N9,18, P9,18, R9,18, T9,18, U9,18, V10,13,15,17-18
 Center GND Pins (36 pins): L11-16, M11-16, N11-16, P11-16, R11-16, T11-16

Center VCCQ Pins (5 pins): V9,11-12,14,16
 Center VTT Pins (5 pins): J10, 13-14, 17-18

Table 2. VT8363A KT133A Pin List (Alphabetical Order)

Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name
AC03	IO AD00	A09	IO D00#	AA24	O DOM5 / CAS5#	Y24	P GND	AC21	IO MD26	AD01	I SBA1
AC04	IO AD01	E11	IO D01#	T26	O DQM6 / CAS6#	AA08	P GND	AE21	IO MD27	AE01	I SBA2
AC01	IO AD02	C10	IO D02#	R24	O DQM7 / CAS7#	AA11	P GND	AD20	IO MD28	AD03	I SBA3
AC02	IO AD03	B09	IO D03#	T05	IO FRAME#	AA13	P GND	AF20	IO MD29	AF03	I SBA4
AB01	IO AD04	B11	IO D04#	AD16	IO GBE0#	AA16	P GND	AD19	IO MD30	AE03	I SBA5
AB02	IO AD05	A11	IO D05#	AD12	IO GBE1#	AA19	P GND	AF19	IO MD31	AE04	I SBA6
AA04	IO AD06	B12	IO D06#	AE12	IO GBE2#	AB03	P GND	G24	IO MD32	AD04	I SBA7
AA03	IO AD07	A12	IO D07#	AD08	IO GBE3#	AD21	P GND	G26	IO MD33	AF01	I SBS
AA02	IO AD08	E10	IO D08#	AB14	O GCLK	AD24	P GND	H24	IO MD34	AF02	I SBS#
Y05	IO AD09	B08	IO D09#	AC15	I GCLKF	AE02	P GND	H25	IO MD35	J01	I SCANENA
W05	IO AD10	E09	IO D10#	AE18	IO GD0	AE05	P GND	J26	IO MD36	F02	I SCANIN0
Y02	IO AD11	A08	IO D11#	AD18	IO GD1	AE08	P GND	K24	IO MD37	F01	I SCANIN1
Y03	IO AD12	D10	IO D12#	AB16	IO GD2	AE11	P GND	K26	IO MD38	F05	I SCANIN2
Y01	IO AD13	C09	IO D13#	AF18	IO GD3	AE14	P GND	K22	IO MD39	G02	I SCANIN3
Y04	IO AD14	C08	IO D14#	AD17	IO GD4	AE17	P GND	L24	IO MD40	H01	I SCANIN4
W01	IO AD15	D11	IO D15#	AF17	IO GD5	AB15	P GNDGCK	L26	IO MD41	H02	I SCANIN5
U01	IO AD16	C12	IO D16#	AE16	IO GD6	G21	P GNDHCK	L23	IO MD42	J03	I SCANIN6
U04	IO AD17	C13	IO D17#	AF16	IO GD7	P21	P GNDMCK	M26	IO MD43	J02	I SCANIN7
U02	IO AD18	A13	IO D18#	AC16	IO GD8	D02	P GNDPLL1	N25	IO MD44	H03	O SCANOUT0
U03	IO AD19	R14	IO D19#	AF15	IO GD9	D03	P GNDPLL2	M22	IO MD45	G06	O SCANOUT1
T01	IO AD20	A14	IO D20#	AF14	IO GD10	AB17	P GNDPO	N23	IO MD46	H05	O SCANOUT2
T04	IO AD21	C14	IO D21#	AD14	IO GD11	M05	O GNT0#	N24	IO MD47	K06	O SCANOUT3
T02	IO AD22	A15	IO D22#	AD13	IO GD12	N02	O GNT1#	AB23	IO MD48	K01	O SCANOUT4
R02	IO AD23	C15	IO D23#	AF13	IO GD13	N05	O GNT2#	AC25	IO MD49	K02	O SCANOUT5
R01	IO AD24	F13	IO D24#	AE13	IO GD14	M01	O GNT3#	AD26	IO MD50	K03	O SCANOUT6
P03	IO AD25	C11	IO D25#	AF12	IO GD15	M03	O GNT4#	AE26	IO MD51	L02	O SCANOUT7
P02	IO AD26	E13	IO D26#	AF11	IO GD16	AC13	IO GPAR / GCKRUN#	AF26	IO MD52	P25	O SCASA#/strap
R05	IO AD27	E12	IO D27#	AD11	IO GD17	AC09	I GPIPE#	AE24	IO MD53	V02	IO SERR#
P05	IO AD28	D13	IO D28#	AE10	IO GD18	K05	O GPOUT	AF24	IO MD54	U25	O SRASA#/strap
P01	IO AD29	D14	IO D29#	AD10	IO GD19	AA09	I GRBF#	AE23	IO MD55	AC06	O ST0
R04	IO AD30	D16	IO D30#	AF09	IO GD20	AD05	I GREQ#	AC22	IO MD56	AB08	O ST1
P04	IO AD31	E14	IO D31#	AE09	IO GD21	AB12	IO GSTOP#	AF22	IO MD57	AB09	O ST2
AF10	P AGPVREF	F15	IO D32#	AF08	IO GD22	AC12	IO GTRDY#	AB21	IO MD58	V04	IO STOP#
B06	O AIN02#	D17	IO D33#	AD09	IO GD23	AC10	I GWBF#	AC20	IO MD59	AB19	I SUSST#
A06	O AIN03#	C17	IO D34#	AF07	IO GD24	G22	I HCLK	AF21	IO MD60	AB24	O SWEA#/strap
C06	O AIN04#	E17	IO D35#	AE07	IO GD25	T06	IO IRDY#	AE20	IO MD61	H23	I TESTIN
C07	O AIN05#	D20	IO D36#	AD07	IO GD26	V01	IO LOCK#	AB20	IO MD62	V05	IO TRDY#
D07	O AIN06#	D19	IO D37#	AF06	IO GD27	U24	O MA00 / strap	AE19	IO MD63	F06	P VCC3
E08	O AIN07#	C19	IO D38#	AE06	IO GD28	U23	O MA01# / strap	A01	NC	H06	P VCC3
E07	O AIN08#	B20	IO D39#	AF05	IO GD29	V26	O MA02 / strap	B01	NC	J21	P VCC3
A05	O AIN09#	A16	IO D40#	AD06	IO GD30	T22	O MA03 / strap	B02	NC	K21	P VCC3
C05	O AIN10#	C16	IO D41#	AF04	IO GD31	V23	O MA04 / strap	C01	NC	L06	P VCC3
A07	O AIN11#	R17	IO D42#	AD15	IO GDS0	U22	O MA05 / strap	C02	NC	M21	P VCC3
B03	O AIN12#	A17	IO D43#	AE15	IO GDS0#	V22	O MA06 / strap	C03	NC	N04	P VCC3
R05	O AIN13#	A18	IO D44#	AB07	IO GDS1	U21	O MA07 / strap	D01	NC	P06	P VCC3
A03	O AIN14#	C18	IO D45#	AC07	IO GDS1#	V25	O MA08 / strap	D04	NC	R21	P VCC3
A04	O AINCLK#	E19	IO D46#	AB13	IO GDSEL#	V24	O MA09 / strap	E01	NC	T23	P VCC3
B26	I AOUT02#	A19	IO D47#	AB10	IO GFRM#	W26	O MA10 / strap	E02	NC	V06	P VCC3
A26	I AOUT03#	E20	IO D48#	AB06	O GGNT#	W25	O MA11 / strap	E03	NC	V21	P VCC3
C24	I AOUT04#	A24	IO D49#	AB11	IO GIRDY#	W24	O MA12 / strap	E04	NC	W21	P VCC3
E24	I AOUT05#	F18	IO D50#	A02	P GND	W23	O MA13 / strap	F03	NC	AA06	P VCC3
C25	I AOUT06#	E18	IO D51#	B04	P GND	W22	O MA14 / strap	F04	NC	AA21	P VCC3
E26	I AOUT07#	C22	IO D52#	R07	P GND	P23	I MCLKF	G01	NC	AA14	P VCCGCK
F24	I AOUT08#	B24	IO D53 #	B10	P GND	R22	O MCLK	G04	NC	H22	P VCCCHK
C26	I AOUT09#	D22	IO D54#	R13	P GND	G25	IO MD00	G05	NC	P22	P VCCMCK
D24	I AOUT10#	C23	IO D55#	B16	P GND	G23	IO MD01	H04	NC	AA07	P VCCO
D23	I AOUT11#	A20	IO D56#	B19	P GND	H26	IO MD02	J05	NC	AA10	P VCCQ
D26	I AOUT12#	C20	IO D57#	B22	P GND	J25	IO MD03	K04	NC	AA12	P VCCQ
F25	I AOUT13#	C21	IO D58#	B25	P GND	J22	IO MD04	L05	NC	AA15	P VCCQ
F26	I AOUT14#	A21	IO D59#	F07	P GND	K25	IO MD05	AB18	I NCOMP	AA18	P VCCO
D25	I AOUTCLK#	B21	IO D60#	F09	P GND	J23	IO MD06	W02	IO PAR	AC05	P VCCO
AA01	IO CBE0#	E21	IO D61#	F12	P GND	K23	IO MD07	AB04	IO PCKRUN#	AC08	P VCCO
W04	IO CBE1#	A22	IO D62#	F16	P GND	L25	IO MD08	AA05	I PCLK	AC11	P VCCQ
U05	IO CBE2#	B23	IO D63#	F19	P GND	L22	IO MD09	AC18	I PCOMP	AC14	P VCCO
T03	IO CBE3#	V03	IO DEVSEL#	G03	P GND	M23	IO MD10	L01	O PGNT#	AC17	P VCCO
E05	O CFWRDST	J04	I DFTIN	H21	P GND	M25	IO MD11	L04	I PREO#	AA17	P VCCOO
AB25	O CKE0 / SWEC#	A10	O DICLK0#	J06	P GND	N26	IO MD12	C04	I PROCRDY	AA20	P VSUS3
R25	O CKE1 / SCASC#	F15	O DIC1 K1#	J24	P GND	N21	IO MD13	AC19	I PWROK	D06	P VTT
AC26	O CKE2 / SWEB#	B18	O DICLK2#	L03	P GND	N22	IO MD14	N06	I REO0#	D09	P VTT
T26	O CKE3 / SCASB#	A23	O DICLK3#	L21	P GND	P24	IO MD15	N01	I REQ1#	D12	P VTT
T25	O CKE4 / SRASC#	E06	O DINVAL#	M06	P GND	AB22	IO MD16	N03	I REQ2#	D15	P VTT
U26	O CKE5 / SRASB#	D08	I DOCLK0#	M24	P GND	AC24	IO MD17	M04	I REQ3#	D18	P VTT
F23	P CLKVREF	B15	I DOCLK1#	R03	P GND	AD25	IO MD18	M02	I REQ4#	D21	P VTT
D05	O CONNECT	E16	I DOCLK2#	R06	P GND	AE25	IO MD19	AB05	I RESET#	F23	P VTT
Y25	O CS0# / RAS0#	A25	I DOCLK3#	T21	P GND	AF25	IO MD20	E22	I S2KCOMP	E25	P VTT
Y26	O CS1# / RAS1#	AA23	O DOM0 / CAS0#	T24	P GND	AC23	IO MD21	F21	P S2KGNL	F08	P VTT
AA26	O CS2# / RAS2#	AA22	O DOM1 / CAS1#	W03	P GND	AD23	IO MD22	F22	P S2KVCC	F11	P VTT
AA25	O CS3# / RAS3#	R23	O DOM2 / CAS2#	W06	P GND	AF23	IO MD23	F10	P S2KVREF	F14	P VTT
Y22	O CS4# / RAS4#	R26	O DQM3 / CAS3#	Y06	P GND	AD22	IO MD24	F20	P S2KVREF	F17	P VTT
Y23	O CS5# / RAS5#	AB26	O DOM4 / CAS4#	Y21	P GND	AE22	IO MD25	AD02	I SBA0	U06	O WSC#

Center VCC25 Pins (26 pins): J9,11-12,15-16, K9,18, L9,18, M9,18, N9,18, P9,18, R9,18, T9,18, U9,18, V10,13,15,17-18

Center GND Pins (36 pins): L11-16, M11-16, N11-16, P11-16, R11-16, T11-16

Center VCCQ Pins (5 pins): V9,11-12,14,16

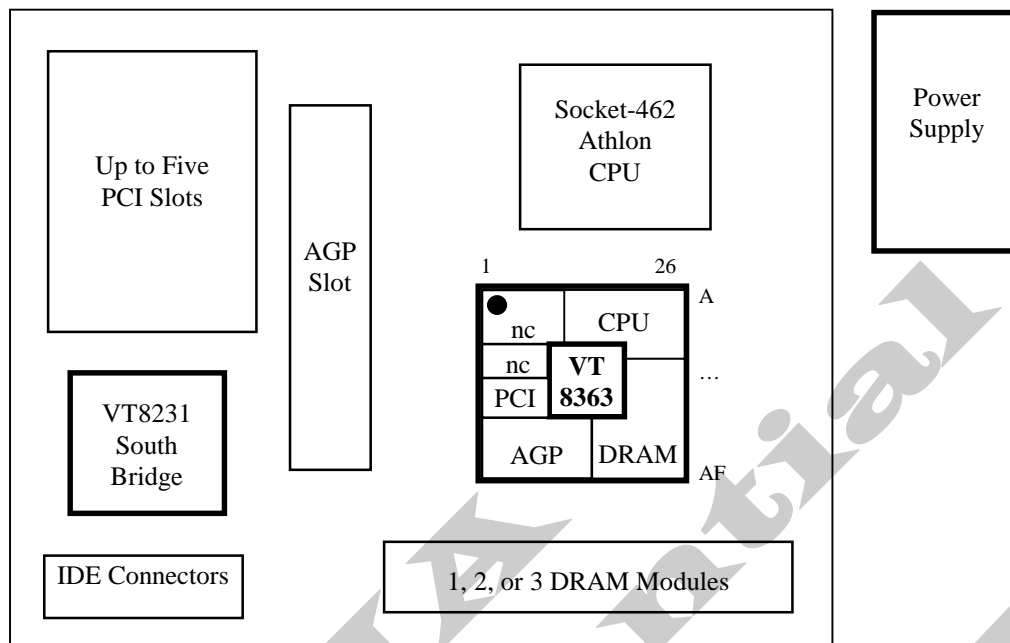
Center VTT Pins (5 pins): J10, 13-14, 17-18

PIN DESCRIPTIONS

Table 3. VT8363A KT133A Pin Descriptions

CPU Interface			
Signal Name	Pin #	I/O	Signal Description
CFWDRST	E5	O	CLK Forward Reset. Reset the CLK forward circuitry for the Athlon™ interface.
CONNECT	D5	O	Connect. Used for power management and CLK-forward initialization at reset.
PROCRDY	C4	I	Processor Ready. Used for power management and CLK-forward initialization at reset.
AIN[14-2]#	(see pin list)	O	Host CPU Address / Command Output. Unidirectional system address / command interface to the processor from the system controller. It is used to transfer probes or data movement commands into the processor during PCI-to-DRAM cycles to snoop the CPU internal Cache. AIN[14:2]# is skew-aligned with the forward clock, AINCLK#
AINCLK#	A4	O	Host CPU Address Output Clock. Single-ended forwarded clock for the AIN[14:2]# bus that is driven by the system controller. Both rising and falling edges are used to transfer addresses or commands to the processor.
AOUT[14-2]#	(see pin list)	I	Host CPU Address Input. Unidirectional system address / command interface from the processor to the system controller. It is used to transfer processor commands or probes responses to the system controller. AOUT[14:2]# is skew-aligned with the forward clock, AOUTCLK#
AOUTCLK#	D25	I	Host CPU Address Input Clock. Single-ended forwarded clock for the AOUT[14:2]# bus that is driven by the processor. Both rising and falling edges are used to transfer commands or probe responses.
D[63-0]#	(see pin list)	IO	Host CPU Data. Bi-directional interface between the processor and the system controller for data movement. D[63:0]# bus is skew-aligned with either the DCLK[3:0]# or DOCLK[3:0]# forward clocks.
DCLK[3-0]#	A23, B18, E15, A10	O	Host CPU Data Input Clock. Single-ended forwarded clocks for the D[63:0]# bus, driven by the system controller to the processor. Each 16-bit data word is skew-aligned with one of these clocks. Both rising and falling edges are used to transfer data to the processor.
DOCLK[3-0]#	A25, E16, B15, D8	I	Host CPU Data Output Clock. Single-ended forwarded clocks for the D[63:0]# bus, driven by the processor to the system controller. Each 16-bit data word is skew-aligned with one of these clocks. Both rising and falling edges are used to transfer data to the system controller.
DINVAL#	E6	O	Host CPU Data Read In Valid. Driven by the system controller to control the flow of data into the processor. DINVAL# can be used to introduce an arbitrary number of cycles between octawords into the processor.

The pinouts were defined assuming the ATX PCB layout model shown below (and general pin layout shown) as a guide for PCB component placement. Other PCB layouts (AT, LPX, and NLX) were also considered and can typically follow the same general component placement.



DRAM Interface																																											
Signal Name	Pin #	I/O	Signal Description																																								
MD[63:0]	(see pinout tables)	IO	Memory Data. These signals are connected to the DRAM data bus.																																								
MA14 / strap, MA13 / strap, MA12 / strap, MA11 / strap, MA10 / strap, MA9 / strap, MA8 / strap, MA7 / strap, MA6 / strap, MA5 / strap, MA4 / strap, MA3 / strap, MA2 / strap, MA1 / strap, MA0 / strap	W22 W23 W24 W25 W26 V24 V25 U21 V22 U22 V23 T22 V26 U23 U24	O / I	Memory Address. DRAM address lines <table> <thead> <tr> <th>Strap</th><th>Register</th><th>Description</th><th>Settings</th></tr> </thead> <tbody> <tr> <td>MA14</td><td>Rx68[0]</td><td>CPU Clock Frequency</td><td>0=100, 1=66</td></tr> <tr> <td>MA13-12</td><td>RxB4[5-4]</td><td>Internal Pullup Strength</td><td>11=Auto, ~11=Strap</td></tr> <tr> <td>MA11</td><td>RxB6[7]</td><td>S2K Edge/Central DQ</td><td>1=Edge</td></tr> <tr> <td>MA10-9</td><td>RxB4[1-0]</td><td>Output Drive Strength</td><td>0=Auto, ~0=Strap</td></tr> <tr> <td>MA8-4</td><td>RxB6[4-0]</td><td>S2K Strobe Delay</td><td>0=Auto, ~0=Strap</td></tr> <tr> <td>MA3-0</td><td>RxB3[7-4]</td><td>CPU Clock Divide</td><td>0=11, 1=11.5, 2=12, 3=12.5, 4=5, 5=5.5, 6=6.7=6.5, 8=7.9=7.5, 10=8, 11=8.5, 12=9, 13=9.5, 14=10, 15=10.5</td></tr> <tr> <td>SRASA#</td><td>RxB2[5]</td><td>S2K Slew Rate Control</td><td>1=Disable</td></tr> <tr> <td>SCASA#</td><td>RxB3[1]</td><td>Fast Command</td><td>1=Enable</td></tr> <tr> <td>SWEA#</td><td>RxB6[5]</td><td>CPU Edge/Center DQ</td><td>1=Center</td></tr> </tbody> </table> <p>Strap option default values are all 0 (internally pulled down)</p>	Strap	Register	Description	Settings	MA14	Rx68[0]	CPU Clock Frequency	0=100, 1=66	MA13-12	RxB4[5-4]	Internal Pullup Strength	11=Auto, ~11=Strap	MA11	RxB6[7]	S2K Edge/Central DQ	1=Edge	MA10-9	RxB4[1-0]	Output Drive Strength	0=Auto, ~0=Strap	MA8-4	RxB6[4-0]	S2K Strobe Delay	0=Auto, ~0=Strap	MA3-0	RxB3[7-4]	CPU Clock Divide	0=11, 1=11.5, 2=12, 3=12.5, 4=5, 5=5.5, 6=6.7=6.5, 8=7.9=7.5, 10=8, 11=8.5, 12=9, 13=9.5, 14=10, 15=10.5	SRASA#	RxB2[5]	S2K Slew Rate Control	1=Disable	SCASA#	RxB3[1]	Fast Command	1=Enable	SWEA#	RxB6[5]	CPU Edge/Center DQ	1=Center
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CS[5:0]#	Y23, Y22, AA25, AA26, Y26, Y25	O	Chip Select. Chip select of each bank.																																								
DQM[7:0]	R24, T26, AA24, AB26, R26, R23, AA22, AA23	O	Data Mask. Data mask of each byte lane																																								
SRASA# / strap	U25	O	Row Address Command Indicator. (see Device 0 RxB2[5])																																								
SCASA# / strap	P25	O	Column Address Command Indicator. (see Device 0 RxB3[1])																																								
SWEA# / strap	AB24	O	Write Enable Command Indicator. (see Device 0 RxB6[5])																																								
CKE0 / SWEC#, CKE1 / SCASC#, CKE2 / SWEB#, CKE3 / SCASB#, CKE4 / SRASC#, CKE5 / SRASB#	AB25 R25 AC26 P26 T25 U26	O	Clock Enables. Clock enables for each DRAM bank for powering down the SDRAM or clock control for reducing power usage and for reducing heat / temperature in high-speed memory systems.																																								

PCI Bus Interface			
Signal Name	Pin #	I/O	Signal Description
AD[31:0]	(see pinout tables)	IO	Address/Data Bus. The standard PCI address and data lines. The address is driven with FRAME# assertion and data is driven or received in following cycles.
CBE[3:0]#	T3, U5, W4, AA1	IO	Command/Byte Enable. Commands are driven with FRAME# assertion. Byte enables corresponding to supplied or requested data are driven on following clocks.
FRAME#	T5	IO	Frame. Assertion indicates the address phase of a PCI transfer. Negation indicates that one more data transfer is desired by the cycle initiator.
IRDY#	T6	IO	Initiator Ready. Asserted when the initiator is ready for data transfer.
TRDY#	V5	IO	Target Ready. Asserted when the target is ready for data transfer.
STOP#	V4	IO	Stop. Asserted by the target to request the master to stop the current transaction.
DEVSEL#	V3	IO	Device Select. This signal is driven by the VT8363A when a PCI initiator is attempting to access main memory. It is an input when the VT8363A is acting as a PCI initiator.
PAR	W2	IO	Parity. A single parity bit is provided over AD[31:0] and C/BE[3:0].
SERR#	V2	IO	System Error. The VT8363A will pulse this signal when it detects a system error condition.
LOCK#	V1	IO	Lock. Used to establish, maintain, and release resource lock.
PREQ#	L4	I	South Bridge Request. This signal comes from the South Bridge. PREQ# is the South Bridge request for the PCI bus.
PGNT#	L1	O	South Bridge Grant. This signal driven by the VT8363A to grant PCI access to the South Bridge.
REQ[4:0]#	M2, M4, N3, N1, N6	I	PCI Master Request. PCI master requests for PCI.
GNT[4:0]#	M3, M1, N5, N2, M5	O	PCI Master Grant. Permission is given to the master to use PCI.
PCLK	AA5	I	PCI Clock. From external clock generator.
PCKRUN#	AB4	IO	PCI Clock Run. May be used to stop PCI clock.
WSC#	U6	O	Write Snoop Complete. Sideband PCI signal (used on the planar only in multiprocessor configurations) asserted to indicate that all snoop activity on the CPU bus initiated by the last PCI-to-DRAM write is complete and that it is safe to send an APIC interrupt message. Basically this signal is always active except when PCI master write data is not flushed.

AGP Bus Interface			
Signal Name	Pin #	I/O	Signal Description
GD[31:0]	(see pinout tables)	IO	Address/Data Bus. The standard AGP/PCI address and data lines. The address is driven with GDS0# and GDS1# assertion for AGP transfers and is driven with GFRM# assertion for PCI transfers.
GDS0	AD15	IO	Bus Strobe 0 (AGP transactions only). Provides timing for 2x data transfer mode on AD[15:0]. The agent that is providing the data drives this signal.
GDS0#	AE15	IO	Bus Strobe 0 complement and Bus Strobe 0 (AGP transactions only). Provides timing for 4x data transfer mode on AD[15:0]. The agent that is providing the data drives this signal.
GDS1	AB7	IO	Bus Strobe 1 (AGP transactions only). Provides timing for 2x data transfer mode on AD[31:16]. The agent that is providing the data drives this signal.
GDS1#	AC7	IO	Bus Strobe 1 complement and Bus Strobe 1 (AGP transactions only). Provides timing for 4x data transfer mode on AD[31:16]. The agent that is providing the data drives this signal.
GBE[3:0]#	AD8, AE12, AD12, AD16	IO	Command/Byte Enable. AGP: These pins provide command information (different commands than for PCI) driven by the master (graphics controller) when requests are being enqueued using PIPE#. These pins provide valid byte information during AGP write transactions and are driven by the master. The target (this chip) drives these lines to "0000" during the return of AGP read data, but the state of these pins is ignored by the AGP master. PCI: Commands are driven with GFRM# assertion. Byte enables corresponding to supplied or requested data are driven on following clocks.
GFRM#	AB10	IO	Frame (PCI transactions only). Assertion indicates the address phase of a PCI transfer. Negation indicates that one more data transfer is desired by the cycle initiator.
GIRDY#	AB11	IO	Initiator Ready AGP: For write operations, the assertion of this pin indicates that the master is ready to provide <i>all</i> write data for the current transaction. Once this pin is asserted, the master is not allowed to insert wait states. For read operations, the assertion of this pin indicates that the master is ready to transfer a subsequent block of read data. The master is <i>never</i> allowed to insert a wait state during the initial block of a read transaction. However, it may insert wait states after each block transfers. PCI: Asserted when the initiator is ready for data transfer.
GTRDY#	AC12	IO	Target Ready: AGP: Indicates that the target is ready to provide read data for the entire transaction (when the transaction can complete within four clocks) or is ready to transfer a (initial or subsequent) block of data when the transfer requires more than four clocks to complete. The target is allowed to insert wait states after each block transfers on both read and write transactions. PCI: Asserted when the target is ready for data transfer.
GSTOP#	AB12	IO	Stop (PCI transactions only). Asserted by the target to request the master to stop the current transaction.
GDSEL#	AB13	IO	Device Select (PCI transactions only). This signal is driven by the VT8363A when a PCI initiator is attempting to access main memory. It is an input when the VT8363A is acting as PCI initiator. Not used for AGP cycles.

Note: Clocking of the AGP interface is performed with GCLK; see the clock pin group for descriptions of the clock pins.

Note: PCB Layout Guidelines (reference from AGP specification)

- Total motherboard trace length 10" max, trace impedance = 65 ohms \pm 15 ohms, minimize signal crosstalk
- Trace lengths within groups matched to within 2 inches or better
Groups are:
 - GDS0#, GDS0, GD15-0, GBE1-0#
 - GDS1#, GDS1, GD31-16, GBE3-2#
 - SBS#, SBS, SBA7-0
- Ground isolation should be provided around GDS0#, GDS0, GDS1# and GDS1 to prevent crosstalk with GD[31:0]. Ideally ground traces should be provided adjacent to GDSn# on the same signal layer, but at a minimum wider spaces should be provided on either side (e.g., 16 mil spaces on either side of GDSn# if GDSn# signal traces are 8 mil).

AGP Bus Interface (continued)			
Signal Name	Pin #	IO	Signal Description
GPIPE#	AC9	I	Pipelined Request. Asserted by the master (graphics controller) to indicate that a full-width request is to be enqueued by the target VT8363A. The master enqueues one request each rising edge of GCLK while GPIPE# is asserted. When GPIPE# is deasserted no new requests are enqueued across the AD bus.
GRBF#	AA9	I	Read Buffer Full. Indicates if the master (graphics controller) is ready to accept previously requested low priority read data. When GRBF# is asserted, the VT8363A will not return low priority read data to the master.
GWBF#	AC10	I	Write Buffer Full.
SBA[7:0]	AD4, AE4, AE3, AF3, AD3, AE1, AD1, AD2	I	SideBand Address. Provides an additional bus to pass address and command information from the master (graphics controller) to the target (the VT8363A). These pins are ignored until enabled.
SBS	AF1	I	Sideband Strobe. Provides timing for SBA[7:0] (driven by the master)
SBS#	AF2	I	Sideband Strobe complement and SBS . Provides timing for SBA[7:0] (driven by the master) when 4x timing is supported.
ST[2:0]	AB9, AB8, AC6	O	Status (AGP only). Provides information from the arbiter to a master to indicate what it may do. Only valid while GGNT# is asserted. 000 Indicates that previously requested low priority read or flush data is being returned to the master (graphics controller). 001 Indicates that previously requested high priority read data is being returned to the master. 010 Indicates that the master is to provide low priority write data for a previously enqueued write command. 011 Indicates that the master is to provide high priority write data for a previously enqueued write command. 100 Reserved. (arbiter must not issue, may be defined in the future). 101 Reserved. (arbiter must not issue, may be defined in the future). 110 Reserved. (arbiter must not issue, may be defined in the future). 111 Indicates that the master (graphics controller) has been given permission to start a bus transaction. The master may enqueue AGP requests by asserting PIPE# or start a PCI transaction by asserting GFRM#. ST[2:0] are always outputs from the VT8363A and inputs to the master.
GREQ#	AD5	I	Request. Master request for AGP.
GGNT#	AB6	O	Grant. Permission is given to the master to use AGP.
GPAR / GCKRUN#	AC13	IO	Rx78[1]=0: AGP Parity. A single parity bit is provided over GD[31:0] and GBE[3:0]. Rx78[1]=1: AGP Clock Run. Used to stop the AGP bus clock to reduce bus power usage.
GCLK	AB14	O	AGP Clock. Generated by on-chip clock logic.
GCLKF	AC15	I	AGP Clock Feedback. Connect to GCLK.

Note: For PCI operation on the AGP bus, the following pins are not required:

- PERR# (parity and error reporting not required on transient data devices such as graphics controllers)
- LOCK# (no lock requirement on AGP)
- IDSEL (internally connected to AD16 on AGP-compliant masters)

Note: Separate system interrupts are not provided for AGP. The AGP connector provides interrupts via PCI bus INTA-B#.

Note: The AGP bus supports only one master directly (REQ[3:0]# and GNT[3:0]# are not provided). External logic is required to implement additional master capability. Note that the arbitration mechanism on the AGP bus is different from the PCI bus.

Note: A separate reset is not required for the AGP bus (RESET# resets both PCI and AGP buses)

Note: Two mechanisms are provided by the AGP bus to enqueue master requests: GPIPE# (to send addresses multiplexed on the AD lines) and the SBA port (to send addresses unmultiplexed). AGP masters implement one or the other or select one at initialization time (they are not allowed to change during runtime). Therefore only one of the two will be used and the signals associated with the other will not be used. Therefore the VT8363A has an internal pullup on GRBF# to maintain it in the de-asserted state in case it is not implemented on the master device.

Test Functions			
Signal Name	Pin #	I/O	Signal Description
TESTIN	H23	I	PLL Test Input. Normally connected to VCC3.

Clock / Reset Control			
Signal Name	Pin #	I/O	Signal Description
HCLK	G22	I	Host Clock. This pin receives the host CPU clock (66 / 100 / 133 MHz). This clock is used by all VT8363A logic that is in the host CPU domain. The memory interface logic will also use this clock if selected (memory system timing can alternately be selected to use the AGP bus clock). The CPU clock must lead the AGP clock by 0.2 ± 0.5 nsec.
PCLK	AA5	I	PCI Clock. This pin receives a buffered host clock divided-by-6 to create 33 MHz. This clock is used by all of the VT8363A logic that is in the PCI clock domain. This clock input must be 33 MHz maximum to comply with PCI specification requirements and must be synchronous with the host CPU clock, HCLK. The host CPU clock must lead the PCI clock by 1.5 ± 0.5 nsec.
GCLK	AB14	O	AGP Clock. This pin drives the AGP bus clock (66 MHz). This clock is used by all VT8363A logic that is in the AGP clock domain. The AGP clock is synchronous to the 200 MHz host CPU clock.
GCLKF	AC15	I	AGP Clock Feedback. Connect to GCLK.
MCLK	R22	O	DRAM Clock. Output from internal clock generator to the external clock buffer.
MCLKF	P23	I	DRAM Clock Feedback. Input from MCLK via the external clock buffer.
RESET#	AB5	I	Reset. Input from south bridge chip. When asserted, this signal resets the VT8363A and sets all register bits to the default value. The rising edge of this signal is used to sample all power-up strap options
PWROK	AC19	I	Power OK.
SUSST#	AB19	I	Suspend Status. For implementation of the Suspend-to-DRAM feature. Connect to an external pullup to disable.

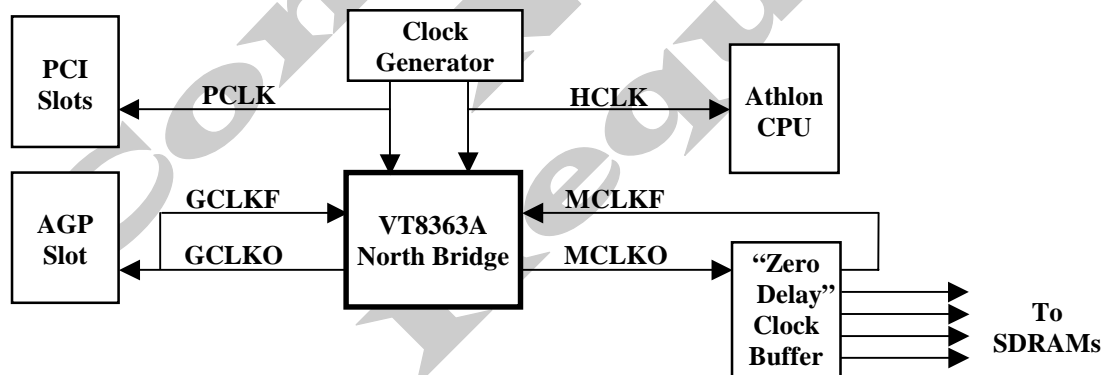


Figure 3. CPU / SDRAM / AGP / PCI Clock Connections

Power, Ground, and Test			
Signal Name	Pin #	I/O	Signal Description
VCC3	(see pin list)	P	Power for Internal Logic and I/O Interface Logic (3.3V \pm 5%).
VSUS3	AA20	P	Suspend Power (3.3V \pm 5%).
VTT	D6, D9, D12, D15, D18, D21, E23, E25, F8, F11, F14, F17, J10, J13, J14, J17, J18	P	CPU Interface Termination Voltage (x.xV \pm 0.xV).
GND	(see pin list)	P	Ground
S2KVREF	F10, F20	P	S2K Voltage Reference.
S2KCOMP	E22	I	S2K Compensation.
S2KVCC	F22	P	S2K Power.
S2KGND	F21	P	S2K Ground.
CLKVREF	F23	P	Clock Voltage Reference.
VCCHCK	H22	P	Host CPU Clock Power (3.3V \pm 5%). For Host CPU clock logic.
GNDHCK	G21	P	Host CPU Clock Ground. Connect to main ground plane.
VCCMCK	P22	P	DRAM Clock Power (3.3V \pm 5%). For DRAM clock deskew logic.
GNDMCK	P21	P	DRAM Clock Ground. Connect to main ground plane.
VCCGCK	AA14	P	AGP Clock Power (3.3V \pm 5%). For AGP clock deskew logic
GNDGCK	AB15	P	AGP Clock Ground. Connect to main ground plane.
VCCQ	V9, V11, V12, V14, V16, AA7, AA10, AA12, AA15, AA18, AC5, AC8, AC11, AC14, AC17	P	AGP 1.5V Power.
VCCQQ	AA17	P	AGP Quiet Power.
GNDQQ	AB17	P	AGP Quiet Ground.
AGPVREF	AF10	P	AGP Voltage Reference. 0.39 VCC3 to 0.41 VCC3. Typical value is 1.32V (0.40 times 3.3V). This can be provided with a resistive divider on VCC3 using 270 ohm and 180 ohm (2%) resistors.
NCOMP	AB18	I	AGP N Compensation. Connect to VCCQ through a 60 ohm resistor.
PCOMP	AC18	I	AGP P Compensation. Connect to GND through a 60 ohm resistor.
DFTIN	J4	I	DFT In.
SCANENA	J1	I	Scan Enable.
SCANIN[7-0]	J2, J3, H2, H1, G2, F5, F1, F2	I	Scan In.
SCANOUT[7-0]	L2, K3-K1, K6, H5, G6, H3	O	Scan Out.

REGISTERS

Register Overview

The following tables summarize the configuration and I/O registers of the VT8363A. These tables also document the power-on default value ("Default") and access type ("Acc") for each register. Access type definitions used are RW (Read/Write), RO (Read/Only), "—" for reserved / used (essentially the same as RO), and RWC (or just WC) (Read / Write 1's to Clear individual bits). Registers indicated as RW may have some read-only bits that always read back a fixed value (usually 0 if unused); registers designated as RWC or WC may have some read-only or read write bits (see individual register descriptions following these tables for details). All offset and default values are shown in hexadecimal unless otherwise indicated.

Table 4. VT8363A Registers

VT8363A I/O Ports

Port #	I/O Port	Default	Acc
22	PCI / AGP Arbiter Disable	00	RW
CFB-8	Configuration Address	0000 0000	RW
CFF-C	Configuration Data	0000 0000	RW

VT8363A Device 0 Registers - Host Bridge
Header Registers

Offset	Configuration Space Header	Default	Acc
1-0	Vendor ID	1106	RO
3-2	Device ID	0305	RO
5-4	Command	0006	RW
7-6	Status	0210	WC
8	Revision ID	8n	RO
9	Program Interface	00	RO
A	Sub Class Code	00	RO
B	Base Class Code	06	RO
C	-reserved-	00	—
D	Latency Timer	00	RW
E	Header Type	00	RO
F	Built In Self Test (BIST)	00	RO
13-10	Graphics Aperture Base	0000 0008	RW
14-2B	-reserved-	00	—
2D-2C	Subsystem Vendor ID	0000	W1
2F-2E	Subsystem ID	0000	W1
30-33	-reserved-	00	—
37-34	Capability Pointer	0000 00A0	RO
38-3F	-reserved-	00	—

Device-Specific Registers

Offset	Host CPU Protocol Control	Default	Acc
50	S2K Timing Control I	00	RW
51	S2K Timing Control II	00	RW
52	S2K Timing Control III	70	RW
53	BIU Arbitration Control	00	RW
54	BIU Control	00	RW
55	Debug (Do Not Program)	-	—

Device-Specific Registers (continued)

Offset	DRAM Control	Default	Acc
56-57	-reserved-	00	—
59-58	MA Map Type	0040	RW
5F-5A	DRAM Row Ending Address:		
5A	Bank 0 Ending (HA[31:24])	01	RW
5B	Bank 1 Ending (HA[31:24])	01	RW
5C	Bank 2 Ending (HA[31:24])	01	RW
5D	Bank 3 Ending (HA[31:24])	01	RW
5E	Bank 4 Ending (HA[31:24])	01	RW
5F	Bank 5 Ending (HA[31:24])	01	RW
60	DRAM Type	00	RW
61	ROM Shadow Control C0000-CFFFF	00	RW
62	ROM Shadow Control D0000-DFFFF	00	RW
63	ROM Shadow Control E0000-FFFFF	00	RW
64	DRAM Timing for Banks 0,1	EC	RW
65	DRAM Timing for Banks 2,3	EC	RW
66	DRAM Timing for Banks 4,5	EC	RW
67	-reserved-	00	—
68	DRAM Control	00	RW
69	DRAM Clock Select	00	RW
6A	DRAM Refresh Counter	00	RW
6B	DRAM Arbitration Control	01	RW
6C	SDRAM Control	00	RW
6D	DRAM Control Drive Strength	00	RW
6E-6F	-reserved-	00	—

Offset	PCI Bus Control	Default	Acc
70	PCI Buffer Control	00	RW
71	CPU to PCI Flow Control 1	00	RW
72	CPU to PCI Flow Control 2	00	RW
73	PCI Master Control 1	00	RW
74	PCI Master Control 2	00	RW
75	PCI Arbitration 1	00	RW
76	PCI Arbitration 2	00	RW
77	Chip Test (do not program)	00	RW
78	PMU Control	00	RW
79	PMU Control	00	RW
7A	Miscellaneous Control	00	RW
7B	PCI Master Access Control	00	RW
7C-7D	-reserved-	00	—
7E-7F	PLL Test Mode (do not program)	00	RW

Device 0 Device-Specific Registers (continued)

Offset	GART/TLB Control	Default	Acc
83-80	GART/TLB Control	0000 0000	RW
84	Graphics Aperture Size	00	RW
85-87	-reserved-	00	—
8B-88	Gr. Aperture TLB Base Register Base	0000 0000	RW
8C-9F	-reserved-	00	—

Offset	AGP Control	Default	Acc
A0	AGP ID	02	RO
A1	AGP Next Item Pointer	C0	RO
A2	AGP Specification Revision	20	RO
A3	-reserved-	00	—
A7-A4	AGP Status	1F00 0203	RO
AB-A8	AGP Command	0000 0000	RW
AC	AGP Control	00	RW
AD	AGP Latency Timer	02	RW
AE	AGP Miscellaneous Control	00	RW
AF	AGP Strobe Drive Strength	00	RW
B0	AGP Pad Control / Status	8x	RW
B1	AGP Drive Strength	63	RW
B2	AGP Pad Drive / Delay Control	00	RW
B3	-reserved-	00	—

Offset	CPU Strapping/S2K Compensation	Default	Acc
B3	CPU Strapping Control	strapping	RO
B4	S2K Compensation Strapping	strapping	RO
B5	S2K Compensation Result 1	00	RO
B6	S2K Compensation Result 2	00	RO
B7	S2K Compensation Result 3	00	RO
B8	S2K Compensation Result 4	00	RO
B9-BF	-reserved-	00	—

Device 0 Device-Specific Registers (continued)

Offset	Power Management & MiscControl	Default	Acc
C0	Power Management Capability ID	01	RO
C1	Power Management New Pointer	00	RO
C2	Power Management Capabilities I	02	RO
C3	Power Management Capabilities II	00	RO
C4	Power Management Control / Status	00	RW
C5	Power Management Status	00	RO
C6	PCI-to-PCI Bridge Support Extension	00	RO
C7	Power Management Data	00	RO
C8-DF	-reserved-	00	—
E0	Miscellaneous Control	00	RW
E1-EF	-reserved-	00	—
F0	BIOS Scratch Register 0	00	RW
F1	BIOS Scratch Register 1	00	RW
F2	BIOS Scratch Register 2	00	RW
F3	BIOS Scratch Register 3	00	RW
F4	BIOS Scratch Register 4	00	RW
F5	BIOS Scratch Register 5	00	RW
F6	Revision ID Backdoor	00	RW
F7	Foundry ID	FoundryID	RW
F8	DRAM Arbitration Timer	00	RW
F9-FB	-reserved-	0000	RW
FC	Back-Door Control 1	00	RW
FD	Back-Door Control 2	00	RW
FF-FE	Back-Door Device ID	0000	RW

VT8363A Device 1 - PCI-to-PCI Bridge
Header Registers

Offset	Configuration Space Header	Default	Acc
1-0	Vendor ID	1106	RO
3-2	Device ID	8305	RO
5-4	Command	0007	RW
7-6	Status	0230	WC
8	Revision ID	nn	RO
9	Program Interface	00	RO
A	Sub Class Code	04	RO
B	Base Class Code	06	RO
C	-reserved-	00	—
D	Latency Timer	00	RW
E	Header Type	01	RO
F	Built In Self Test (BIST)	00	RO
10-17	-reserved-	00	—
18	Primary Bus Number	00	RW
19	Secondary Bus Number	00	RW
1A	Subordinate Bus Number	00	RW
1B	Secondary Latency Timer	00	RO
1C	I/O Base	F0	RW
1D	I/O Limit	00	RW
1F-1E	Secondary Status	0000	RO
21-20	Memory Base	FFF0	RW
23-22	Memory Limit (Inclusive)	0000	RW
25-24	Prefetchable Memory Base	FFF0	RW
27-26	Prefetchable Memory Limit	0000	RW
28-2B	-reserved-	00	—
2D-2C	Subsystem Vendor ID	0000	RW
2F-2E	Subsystem ID	0000	RW
30-33	-reserved-	00	—
34	Capability Pointer	00	RO
35-3D	-reserved-	00	—
3F-3E	PCI-to-PCI Bridge Control	00	RW

Device-Specific Registers

Offset	AGP Bus Control	Default	Acc
40	CPU-to-AGP Flow Control 1	00	RW
41	CPU-to-AGP Flow Control 2	00	RW
42	AGP Master Control	00	RW
43	AGP Master Latency Timer	00	RW
44	Back-Door Register Control	00	RW
45	Fast Write Control	72	RW
47-46	PCI-to-PCI Bridge Device ID	0000	RW
48-7F	-reserved-	00	—
80	Capability ID	01	RO
81	Next Pointer	00	RO
82	Power Management Capabilities 1	02	RO
83	Power Management Capabilities 2	00	RO
84	Power Management Control / Status	00	RW
85	Power Management Status	00	RO
86	PCI-PCI Bridge Support Extensions	00	RO
87	Power Management Data	00	RO
88-FF	-reserved-	00	—

Miscellaneous I/O

One I/O port is defined in the VT8363A: Port 22.

Port 22 – PCI / AGP Arbiter DisableRW

- 7-2 Reserved** always reads 0
- 1 AGP Arbiter Disable**
 - 0 Respond to GREQ# signaldefault
 - 1 Do not respond to GREQ# signal
- 0 PCI Arbiter Disable**
 - 0 Respond to all REQ# signalsdefault
 - 1 Do not respond to any REQ# signals, including PREQ#

This port can be enabled for read/write access by setting bit-7 of Device 0 Configuration Register 78.

Configuration Space I/O

All registers in the VT8363A (listed above) are addressed via the following configuration mechanism:

Mechanism #1

These ports respond only to double-word accesses. Byte or word accesses will be passed on unchanged.

Port CFB-CF8 - Configuration Address..... RW

- 31 Configuration Space Enable**
 - 0 Disabled default
 - 1 Convert configuration data port writes to configuration cycles on the PCI bus

30-24 Reserved always reads 0

23-16 PCI Bus Number

Used to choose a specific PCI bus in the system

15-11 Device Number

Used to choose a specific device in the system (devices 0 and 1 are defined for the VT8363A)

10-8 Function Number

Used to choose a specific function if the selected device supports multiple functions (only function 0 is defined for the VT8363A).

7-2 Register Number (also called the "Offset")

Used to select a specific DWORD in the VT8363A configuration space

1-0 Fixed always reads 0

Port CFF-CFC - Configuration Data..... RW

Refer to PCI Bus Specification Version 2.1 for further details on operation of the above configuration registers.

Register Descriptions

Device 0 Header Registers - Host Bridge

All registers are located in PCI configuration space. They should be programmed using PCI configuration mechanism 1 through CF8 / CFC with bus number, function number, and device number equal to zero.

Device 0 Offset 1-0 - Vendor ID (1106h).....RO

15-0 ID Code (reads 1106h to identify VIA Technologies)

Device 0 Offset 3-2 - Device ID (0305h).....RO

15-0 ID Code (reads 0305h to identify the VT8363A)

Device 0 Offset 5-4 -Command (0006h).....RW

15-10 Reserved always reads 0

9 Fast Back-to-Back Cycle Enable RO

- 0 Fast back-to-back transactions only allowed to the same agentdefault
- 1 Fast back-to-back transactions allowed to different agents

8 SERR# Enable..... RO

- 0 SERR# driver disableddefault
 - 1 SERR# driver enabled
- (SERR# is used to report parity errors if bit-6 is set).

7 Address / Data Stepping RO

- 0 Device never does steppingdefault
- 1 Device always does stepping

6 Parity Error Response.....RW

- 0 Ignore parity errors & continuedefault
- 1 Take normal action on detected parity errors

5 VGA Palette Snoop RO

- 0 Treat palette accesses normallydefault
- 1 Don't respond to palette accesses on PCI bus

4 Memory Write and Invalidate Command..... RO

- 0 Bus masters must use Mem Writedefault
- 1 Bus masters may generate Mem Write & Inval

3 Special Cycle Monitoring RO

- 0 Does not monitor special cyclesdefault
- 1 Monitors special cycles

2 PCI Bus Master RO

- 0 Never behaves as a bus master
- 1 Can behave as a bus masterdefault

1 Memory Space..... RO

- 0 Does not respond to memory space
- 1 Responds to memory spacedefault

0 I/O Space RO

- 0 Does not respond to I/O spacedefault
- 1 Responds to I/O space

Device 0 Offset 7-6 - Status (0210h)..... RWC

15 Detected Parity Error

- 0 No parity error detected default
- 1 Error detected in either address or data phase.
This bit is set even if error response is disabled (command register bit-6).write one to clear

14 Signaled System Error (SERR# Asserted)

..... always reads 0

13 Signaled Master Abort

- 0 No abort received default
- 1 Transaction aborted by the master
.....write one to clear

12 Received Target Abort

- 0 No abort received default
- 1 Transaction aborted by the target.....
.....write one to clear

11 Signaled Target Abort..... always reads 0

- 0 Target Abort never signaled

10-9 DEVSEL# Timing

- 00 Fast
- 01 Medium..... always reads 01
- 10 Slow
- 11 Reserved

8 Data Parity Error Detected

- 0 No data parity error detected default
- 1 Error detected in data phase. Set only if error response enabled via command bit-6 = 1 and VT8363A was initiator of the operation in which the error occurred.write one to clear

7 Fast Back-to-Back Capable always reads 0

6 User Definable Features..... always reads 0

5 66MHz Capable..... always reads 0

4 Supports New Capability list always reads 1

3-0 Reserved always reads 0

Device 0 Offset 8 - Revision ID (08nh)..... RO

7-0 Chip Revision Code ..always reads 08nh (n=rev code)

Device 0 Offset 9 - Programming Interface (00h) RO

7-0 Interface Identifier always reads 00

Device 0 Offset A - Sub Class Code (00h)..... RO

7-0 Sub Class Codereads 00 to indicate Host Bridge

Device 0 Offset B - Base Class Code (06h)..... RO

7-0 Base Class Code ..reads 06 to indicate Bridge Device

Device 0 Offset D - Latency Timer (00h) RW

Specifies the latency timer value in PCI bus clocks.

7-3 Guaranteed Time Slice for CPU..... default=0

2-0 Reserved (fixed granularity of 8 clks) .. always read 0
Bits 2-1 are writeable but read 0 for PCI specification compatibility. The programmed value may be read back in Offset 75 bits 5-4 (PCI Arbitration 1).

Device 0 Host Bridge Header Registers (continued)
Device 0 Offset E - Header Type (00h).....RO

7-0 Header Type Codereads 00: single function

Device 0 Offset F - Built In Self Test (BIST) (00h).....RO

7 BIST Supportedreads 0: no supported functions

6-0 Reserved always reads 0

Device 0 Offset 13-10 - Graphics Aperture Base
(00000008h)RW

31-28 Upper Programmable Base Address Bits..... def=0

27-20 Lower Programmable Base Address Bits def=0

These bits behave as if hardwired to 0 if the corresponding Graphics Aperture Size register bit (Device 0 Offset 84h) is 0.

27	26	25	24	23	22	21	20	(This Register)
<u>7</u>	<u>6</u>	<u>5</u>	<u>4</u>	<u>3</u>	<u>2</u>	<u>1</u>	<u>0</u>	(Gr Aper Size)
RW	RW	RW	RW	RW	RW	RW	RW	1M
RW	RW	RW	RW	RW	RW	RW	0	2M
RW	RW	RW	RW	RW	RW	0	0	4M
RW	RW	RW	RW	RW	0	0	0	8M
RW	RW	RW	RW	0	0	0	0	16M
RW	RW	RW	0	0	0	0	0	32M
RW	RW	0	0	0	0	0	0	64M
RW	0	0	0	0	0	0	0	128M
0	0	0	0	0	0	0	0	256M

19-0 Reserved always reads 00008

Note: The locations in the address range defined by this register are prefetchable.

Device 0 Offset 2D-2C – Subsystem Vendor ID (0000h)R/W1

15-0 Subsystem Vendor ID..... default = 0

This register may be written once and is then read only.

Device 0 Offset 2F-2E – Subsystem ID (0000h)..... R/W1

15-0 Subsystem ID default = 0

This register may be written once and is then read only.

Device 0 Offset 37-34 - Capability Pointer (000000A0h) RO

Contains an offset from the start of configuration space.

31-0 AGP Capability List Pointer always reads A0h

Device 0 Configuration Registers - Host Bridge

These registers are normally programmed once at system initialization time.

Host CPU Control
Device 0 Offset 50 – S2K Timing Control I.....RW

The contents of this register are preserved during suspend. Bits 5-0 have no default value. When the system is first powered up, S2K timing (SIP) is determined by an internal ROM. After power up, the user can change the timing (the SIP) by programming SDCout, SDCin, Dinit, Ainit, and MuxPreLd, then setting bit-7 of this register, then generating a system reset by programming SB.

7 Disable ROM Table

- 0 Read SDCout, SDCin, Dinit, Ainit, MuxPreLd, and WrDataDly values from internal ROMdefault
- 1 Normal read of SDCout, SDCin, Dinit, Ainit, MuxPreLd, and WrDataDly values from fields of registers Rx50-52

6 Reserved always reads 0

5-4 Read Data Delay (SDCOutDelay)..... (SDCout)
3-0 Write Data Delay (SDCInDelay) (SDCin)
Device 0 Offset 51 – S2K Timing Control II.....RW

The contents of this register are preserved during suspend. The fields in this register have no default value.

7-6 North Bridge Data Receiver Mux Initial Count..... (Dinit)
5-4 North Bridge Address Receiver Mux Initial Count (Ainit)
3 Reserved always reads 0

2-0 CPU Data / Address Mux Preload Count (MuxPreLd)
Device 0 Offset 52 – S2K Timing Control III.....RW

The contents of this register are preserved during suspend. Bits 2-0 have no default value.

7 Disconnect Enable When STPGNT Detected
6 Write to Read Delay default = 1

5-4 Read to Write Delay default = 11b

3 1ns Skew Between Even / Odd Clock Group For Data (Strapped from MAB3)

- 0 Disabledefault if no strap on MAB3
- 1 Enable

2-0 Write Data Delay from SYSDC to CPU Data Output (WrDataDly)
Device 0 Offset 53 – BIU Arbitration Control RW
7-6 Max of Contiguous Probe SysDC Before Switch to Other Type of SysDC
5-3 Max of Contiguous Read SysDC Before Switch to Other Type of SysDC
2-0 Max of Contiguous Write SysDC Before Switch to Other Type of SysDC
Device 0 Offset 54 – BIU Control..... RW
7 SDRAM Self-Refresh When Disconnected

- 0 Disable..... default
- 1 Enable

6 Probe Next Tag State T1 When PCI Master Read Cacheing Enabled

- 0 Disable..... default
- 1 Enable

5 S2K Data Input Buffer

- 0 Disable..... default
- 1 Enable

4 S2K Data Output Enable Timing

- 0 1T Setup / Hold default
- 1 1/2T Setup / Hold

3 DRAM Speculative Read for PCI Master Read (Before Probe Result is Known)

- 0 Disable..... default
- 1 Enable

2 PCI Master Pipeline Request

- 0 Disable..... default
- 1 Enable

1 PCI-to-CPU / CPU-to-PCI (P2C / C2P) Concurrency

- 0 Disable..... default
- 1 Enable

0 Fast Write-to-Read Turnaround

- 0 Disable..... default
- 1 Enable

Device 0 Offset 55 – Debug RW
7-0 Reserved (do not program)..... default = 0

DRAM Control

These registers are normally set at system initialization time and not accessed after that during normal system operation. Some of these registers, however, may need to be programmed using specific sequences during power-up initialization to properly detect the type and size of installed memory (refer to the VIA Technologies VT8363A BIOS porting guide for details).

Table 5. System Memory Map

Space	Start	Size	Address Range	Comment
DOS	0	640K	00000000-0009FFFF	Cacheable
VGA	640K	128K	000A0000-000BFFFF	Used for SMM
BIOS	768K	16K	000C0000-000C3FFF	Shadow Ctrl 1
BIOS	784K	16K	000C4000-000C7FFF	Shadow Ctrl 1
BIOS	800K	16K	000C8000-000CBFFF	Shadow Ctrl 1
BIOS	816K	16K	000CC000-000CFFFF	Shadow Ctrl 1
BIOS	832K	16K	000D0000-000D3FFF	Shadow Ctrl 2
BIOS	848K	16K	000D4000-000D7FFF	Shadow Ctrl 2
BIOS	864K	16K	000D8000-000DBFFF	Shadow Ctrl 2
BIOS	880K	16K	000DC000-000DFFFF	Shadow Ctrl 2
BIOS	896K	64K	000E0000-000EFFFF	Shadow Ctrl 3
BIOS	960K	64K	000F0000-000FFFFF	Shadow Ctrl 3
Sys	1MB	—	00100000-DRAM Top	Can have hole
Bus	D Top		DRAM Top-FFFFFFFFFF	
Init	4G-64K	64K	FFFEFFFFFF-FFFFFFFF	000Fxxxx alias

Device 0 Offset 59-58 - DRAM MA Map Type (0040h).RW

- 15-13 Bank 5/4 MA Map Type (see below)**
- 12 Bank 5/4 Virtual Channel Enable**..... def=0
- 11-8 Reserved** def = 0
- 7-5 Bank 1/0 MA Map Type**
- 000 16Mbit SDRAM.....default
- 001 -reserved-
- 01x -reserved-
- 100 64Mbit / 128Mbit SDRAM
- 101 256Mbit x 32 SDRAM
- 110 256Mbit x 16 SDRAM
- 111 256Mbit x 8 or x 4 SDRAM
- 4 Bank 1/0 Virtual Channel Enable**..... def=0
- 3-1 Bank 3/2 MA Map Type (see above)**
- 0 Bank 3/2 Virtual Channel Enable**..... def=0

Device 0 Offset 5F-5A – DRAM Row Ending Address:

Offset 5A – Bank 0 Ending (HA[31:24]) (01h) RW

Offset 5B – Bank 1 Ending (HA[31:24]) (01h) RW

Offset 5C – Bank 2 Ending (HA[31:24]) (01h) RW

Offset 5D – Bank 3 Ending (HA[31:24]) (01h) RW

Offset 5E – Bank 4 Ending (HA[31:24]) (01h) RW

Offset 5F – Bank 5 Ending (HA[31:24]) (01h) RW

Note : BIOS is required to fill the ending address registers for all banks even if no memory is populated. The endings have to be in incremental order.

Device 0 Offset 60 – DRAM Type (00h)..... RW

7-6 DRAM Type for Bank 7/6

- 00 -reserved- default
- 01 -reserved-
- 10 -reserved-
- 11 SDRAM

5-4 DRAM Type for Bank 5/4..... default=00

3-2 DRAM Type for Bank 3/2..... default=00

1-0 DRAM Type for Bank 1/0..... default=00

Table 6. Memory Address Mapping Table

MA:	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
16Mb (0xx)				11	22	21	20	19	18	17	16	15	14	13	12	11x10, 11x9, 11x8
64/128Mb (100) 2/4 bank	24	13	12	11	PC	24	23	10	9	8	7	6	5	4	3	x4: 14x10 x8: 14x9
256Mb (101) 2/4B	25	24	13	12	22	21	20	19	18	17	16	15	14	11	23	x32: 14x8
256Mb (110) 2/4B	26	24	13	12	22	21	20	19	18	17	16	15	14	11	23	x16: 14x9
256Mb (111) 2/4B	27	24	13	12	22	21	20	19	18	17	16	15	14	11	23	x8: 14x10 x4: 14x11

"PC" = "Precharge Control" (refer to SDRAM specifications)

Device 0 Offset 61 - Shadow RAM Control 1 (00h)RW

- 7-6 CC000h-CFFFFh**
 00 Read/write disabledefault
 01 Write enable
 10 Read enable
 11 Read/write enable
- 5-4 C8000h-CBFFFh**
 00 Read/write disabledefault
 01 Write enable
 10 Read enable
 11 Read/write enable
- 3-2 C4000h-C7FFFh**
 00 Read/write disabledefault
 01 Write enable
 10 Read enable
 11 Read/write enable
- 1-0 C0000h-C3FFFh**
 00 Read/write disabledefault
 01 Write enable
 10 Read enable
 11 Read/write enable

Device 0 Offset 62 - Shadow RAM Control 2 (00h)RW

- 7-6 DC000h-DFFFFh**
 00 Read/write disabledefault
 01 Write enable
 10 Read enable
 11 Read/write enable
- 5-4 D8000h-DBFFFh**
 00 Read/write disabledefault
 01 Write enable
 10 Read enable
 11 Read/write enable
- 3-2 D4000h-D7FFFh**
 00 Read/write disabledefault
 01 Write enable
 10 Read enable
 11 Read/write enable
- 1-0 D0000h-D3FFFh**
 00 Read/write disabledefault
 01 Write enable
 10 Read enable
 11 Read/write enable

Device 0 Offset 63 - Shadow RAM Control 3 (00h)..... RW

- 7-6 E0000h-EFFFFh**
 00 Read/write disable default
 01 Write enable
 10 Read enable
 11 Read/write enable
- 5-4 F0000h-FFFFFh**
 00 Read/write disable default
 01 Write enable
 10 Read enable
 11 Read/write enable
- 3-2 Memory Hole**
 00 None default
 01 512K-640K
 10 15M-16M (1M)
 11 14M-16M (2M)
- 1 A,BK Direct SMRAM Access**
 0 **Enable** default
 1 **Disable**
- 0 A,BK DRAM Access**
 0 **Disable** default
 1 **Enable**

Device 0 Offset 64 - DRAM Timing for Banks 0,1 (ECh)RW
Device 0 Offset 65 - DRAM Timing for Banks 2,3 (ECh)RW
Device 0 Offset 66 - DRAM Timing for Banks 4,5 (ECh)RW
Settings for Registers 67-64

- 7 Precharge Command to Active Command Period**
 0 TRP = 2T
 1 TRP = 3T default
- 6 Active Command to Precharge Command Period**
 0 TRAS = 5T
 1 TRAS = 6T default
- 5-4 CAS Latency**
 00 1T
 01 2T
 10 3T default
 11 reserved
- 3 DIMM Type**
 0 Standard
 1 Registered default
- 2 SDRAM: ACTIVE Command to CMD Command**
 0 2T
 1 3T default
- 2 VCM SDRAM: Prefetch Read Latency**
 0 4T
 1 3T default
- 1-0 Bank Interleave**
 00 No Interleave default
 01 2-way
 10 4-way
 11 Reserved

Device 0 Offset 68 - DRAM Control (00h)RW

- 7 **Reserved** always reads 0
- 6 **Bank Page Control**
 - 0 Allow only pages of the same bank active.. def.
 - 1 Allow pages of different banks to be active
- 5-3 **Reserved** always reads 0
- 2 **Burst Refresh**
 - 0 Disabledefault
 - 1 Enable (burst 4 times)
- 1 **Reserved** always reads 0
- 0 **System Frequency Divider** RO
 Latched from MA14 at the rising edge of RESET#.
 - 0 CPU Frequency =100 MHz (200 MHz FSB)
no strap default
 - 1 CPU Frequency =133 MHz (266 MHz FSB)

Note: See also Rx69[6]

Note: PCI and AGP bus frequencies are 33 and 66 MHz respectively independent of the setting of this bit

Device 0 Offset 69 – DRAM Clock Select (00h) RW

- 7 **Reserved** always reads 0
 - 6 **DRAM Operating Frequency Faster Than CPU**
 - 0 DRAM Same As or Equal to CPU..... default
 - 1 DRAM Faster Than CPU by 33 MHz
- | <u>Rx68[0]</u> | <u>Rx69[6]</u> | <u>CPU / DRAM</u> |
|----------------|----------------|-------------------|
| 0 | 0 | 100 / 100 |
| 0 | 1 | 100 / 133 |
| 1 | 0 | 133 / 133 (def) |
| 1 | 1 | -reserved- |
- 5 **Write Recovery Time For Write With Auto-Precharge**
 - 0 1T default
 - 1 2T
 - 4 **DRAM Controller Command Register Output**
 - 0 Disable..... default
 - 1 Enable
 - 3 **Fast DRAM Precharge for Different Bank**
 - 0 Disable..... default
 - 1 Enable
 - 2 **DRAM 4K Page Enable (for 64Mbit DRAM)**
 - 0 Disable..... default
 - 1 Enable
 - 1 **DIMM Type**
 - 0 Unbuffered..... default
 - 1 Registered
 - 0 **AutoPrecharge on CPU Writeback / TLB Lookup**
 - 0 Disable..... default
 - 1 Enable

Device 0 Offset 6A - Refresh Counter (00h).....RW

- 7-0 Refresh Counter** (in units of 16 CPUCLKs)
- 00 DRAM Refresh Disableddefault
 - 01 32 CPUCLKs
 - 02 48 CPUCLKs
 - 03 64 CPUCLKs
 - 04 80 CPUCLKs
 - 05 96 CPUCLKs
 -

The programmed value is the desired number of 16-CPUCLK units minus one.

Device 0 Offset 6B - DRAM Arbitration Control (01h) RW

- 7-6 Arbitration Parking Policy**
- 00 Park at last bus owner default
 - 01 Park at CPU side
 - 10 Park at AGP side
 - 11 Reserved
- 5 Fast Read to Write turn-around**
- 0 Disable..... default
 - 1 Enable
- 4 Reserved**always reads 0
- 3 MD Bus Second Level Strength Control**
- 0 Normal slew rate control..... default
 - 1 More slew rate control
- 2 CAS Bus Second Level Strength Control**
- 0 Normal slew rate control..... default
 - 1 More slew rate control
- 1 AGP Pad Slew Rate Control**
- 0 Disable..... default
 - 1 Enable
- 0 Multi-Page Open**
- 0 Disable (page registers marked invalid and no page register update which causes non page-mode operation)
 - 1 Enable default

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Device 0 Offset 6C - SDRAM Control (00h).....RW

- 7 MA Control** default = 0
- 6 SRASA / SCASA / SWEA Control** default = 0
- 5-4 Reserved** always reads 0
- 3 Fast TLB Lookup**
 - 0 Disabledefault
 - 1 Enable
- 2-0 SDRAM Operation Mode Select**
 - 000 Normal SDRAM Modedefault
 - 001 NOP Command Enable
 - 010 All-Banks-Precharge Command Enable
(CPU-to-DRAM cycles are converted
to All-Banks-Precharge commands).
 - 011 MSR Enable
CPU-to-DRAM cycles are converted to
commands and the commands are driven on
MA[14:0]. The BIOS selects an appropriate
host address for each row of memory such that
the right commands are generated on
MA[14:0].
 - 100 CBR Cycle Enable (if this code is selected,
CAS-before-RAS refresh is used; if it is not
selected, RAS-Only refresh is used)
 - 101 Reserved
 - 11x Reserved

Device 0 Offset 6D - DRAM Drive Strength (00h)..... RW

- 7 ESDRAM Memory Type**
 - 0 Disable..... default
 - 1 Enable
- 6-5 Delay DRAM Read Latch**
 - 00 No Delay..... default
 - 01 0.5 ns
 - 10 1.0 ns
 - 11 1.5 ns
- 4 Memory Data Drive (MD, MECC)**
 - 0 6 mA default
 - 1 8 mA
- 3 SDRAM Command Drive (SRAS#, SCAS#, SWE#)**
 - 0 16mA default
 - 1 24mA
- 2 Memory Address Drive (MA, WE#)**
 - 0 16mA default
 - 1 24mA
- 1 CAS# Drive**
 - 0 8 mA default
 - 1 12 mA
- 0 RAS# Drive**
 - 0 16mA default
 - 1 24mA

PCI Bus Control

These registers are normally programmed once at system initialization time.

Device 0 Offset 70 - PCI Buffer Control (00h).....RW

- 7 CPU to PCI Post-Write**
 - 0 Disabledefault
 - 1 Enable
- 6 PCI Master to DRAM Post-Write**
 - 0 Disabledefault
 - 1 Enable
- 5 Reserved** always reads 0
- 4 PCI Master to DRAM Prefetch**
 - 0 Disabledefault
 - 1 Enable
- 3 Enhance CPU-to-PCI Write**
 - 0 Normal operationdefault
 - 1 Reduce 1 cycle when the CPU-to-PCI buffer becomes available after being full (PCI and AGP buses)
- 2 PCI Master Read Caching**
 - 0 Disabledefault
 - 1 Enable
- 1 Delay Transaction**
 - 0 Disabledefault
 - 1 Enable
- 0 Slave Device Stopped Idle Cycle Reduction**
 - 0 Normal Operation.....default
 - 1 Reduce 1 PCI idle cycle when stopped by a slave device (PCI and AGP buses)

Device 0 Offset 71 - CPU to PCI Flow Control 1 (00h) . RW

- 7 Dynamic Burst**
 - 0 Disable..... default
 - 1 Enable (see note under bit-3 below)
 - 6 Byte Merge**
 - 0 Disable..... default
 - 1 Enable
 - 5 Reserved** always reads 0
 - 4 PCI I/O Cycle Post Write**
 - 0 Disable..... default
 - 1 Enable
 - 3 PCI Burst**
 - 0 Disable..... default
 - 1 Enable (bit7=1 will override this option)
- | bit-7 | bit-3 | Operation |
|-------|-------|---|
| 0 | 0 | Every write goes into the write buffer and no PCI burst operations occur. |
| 0 | 1 | If the write transaction is a burst transaction, the information goes into the write buffer and burst transfers are later performed on the PCI bus. If the transaction is not a burst, PCI write occurs immediately (after a write buffer flush). |
| 1 | x | Every write transaction goes to the write buffer; burstable transactions will then burst on the PCI bus and non-burstable won't. This is the normal setting. |
- 2 PCI Fast Back-to-Back Write**
 - 0 Disable..... default
 - 1 Enable
 - 1 Quick Frame Generation**
 - 0 Disable..... default
 - 1 Enable
 - 0 1 Wait State PCI Cycles**
 - 0 Disable..... default
 - 1 Enable

Device 0 Offset 72 - CPU to PCI Flow Control 2 (00h) RWC

- 7 Retry Status**
 - 0 No retry occurreddefault
 - 1 Retry occurred..... **write 1 to clear**
- 6 Retry Timeout Action**
 - 0 Retry Forever (record status only).....default
 - 1 Flush buffer for write or return all 1s for read
- 5-4 Retry Limit**
 - 00 Retry 2 timesdefault
 - 01 Retry 16 times
 - 10 Retry 4 times
 - 11 Retry 64 times
- 3 Clear Failed Data and Continue Retry**
 - 0 Flush the entire post-write bufferdefault
 - 1 When data is posting and master (or target) abort fails, pop the failed data if any, and keep posting
- 2 CPU Backoff on PCI Read Retry Failure**
 - 0 Disabledefault
 - 1 Backoff CPU when reading data from PCI and retry fails
- 1 Reduce 1T for FRAME# Generation**
 - 0 Disabledefault
 - 1 Enable
- 0 Reduce 1T for CPU read PCI slave**
 - 0 DisableDefault
 - 1 Enable

Device 0 Offset 73 - PCI Master Control 1 (00h)..... RW

- 7 Reserved** always reads 0
- 6 PCI Master 1-Wait-State Write**
 - 0 Zero wait state TRDY# response default
 - 1 One wait state TRDY# response
- 5 PCI Master 1-Wait-State Read**
 - 0 Zero wait state TRDY# response default
 - 1 One wait state TRDY# response
- 4 Reserved** always reads 0
- 3 Assert STOP# after PCI Master Write Timeout**
 - 0 Disable..... default
 - 1 Enable
- 2 Assert STOP# after PCI Master Read Timeout**
 - 0 Disable..... default
 - 1 Enable
- 1 LOCK# Function**
 - 0 Disable..... default
 - 1 Enable
- 0 PCI Master Broken Timer Enable**
 - 0 Disable..... default
 - 1 Enable. Force into arbitration when there is no FRAME# 16 PCICLK's after the grant.

Device 0 Offset 74 - PCI Master Control 2 (00h)..... RW

- 7 PCI Master Read Prefetch by Enhance Command**
 - 0 Always Prefetch default
 - 1 Prefetch only if Enhance command
- 6 Reserved (Do Not Program)** default = 0
- 5 Reserved** always reads 0
- 4 Dummy Request**..... default = 0
- 3 PCI Delay Transaction Timeout**
 - 0 Disable..... default
 - 1 Enable
- 2 Backoff CPU Immediately on CPU-to-AGP**
 - 0 Disable..... default
 - 1 Enable
- 1-0 CPU/PCI Master Latency Timer Control**
 - 00 AGP master reloads MLT timer default
 - 01 AGP master falling edge reloads MLT timer
 - 10 AGP master rising edge resets timer to 00 and AGP master falling edge reloads MLT timer
 - 11 Reserved (do not program)

Device 0 Offset 75 - PCI Arbitration 1 (00h)RW

- 7 Arbitration Mechanism**
 - 0 PCI has prioritydefault
 - 1 Fair arbitration between PCI and CPU
- 6 Arbitration Mode**
 - 0 REQ-based (arbitrate at end of REQ#)....default
 - 1 Frame-based (arbitrate at FRAME# assertion)
- 5-4 Latency Timer** read only, reads Rx0D bits 2:1
- 3-0 PCI Master Bus Time-Out**
(force into arbitration after a period of time)
 - 0000 Disabledefault
 - 0001 1x32 PCICLKs
 - 0010 2x32 PCICLKs
 - 0011 3x32 PCICLKs
 - 0100 4x32 PCICLKs
 -
 - 1111 15x32 PCICLKs

Device 0 Offset 76 - PCI Arbitration 2 (00h)..... RW

- 7 PCI CPU-to-PCI Post-Write Retry Failed**
 - 0 Continue retry attempt default
 - 1 Go to arbitration
- 6 CPU Latency Timer Bit-0**RO
 - 0 CPU has at least 1 PCLK time slot when CPU has PCI bus
 - 1 CPU has no time slot
- 5-4 Master Priority Rotation Control**
 - 00 Disable..... default
 - 01 Grant to CPU after every PCI master grant
 - 10 Grant to CPU after every 2 PCI master grants
 - 11 Grant to CPU after every 3 PCI master grants

With setting 01, the CPU will always be granted access after the current bus master completes, no matter how many PCI masters are requesting. With setting 10, if other PCI masters are requesting during the current PCI master grant, the highest priority master will get the bus after the current master completes, but the CPU will be guaranteed to get the bus after that master completes. With setting 11, if other PCI masters are requesting, the highest priority will get the bus next, then the next highest priority will get the bus, then the CPU will get the bus. In other words, with the above settings, even if multiple PCI masters are continuously requesting the bus, the CPU is guaranteed to get access after every master grant (01), after every other master grant (10) or after every third master grant (11).
- 3-2 REQn# to REQ4# Mapping**
 - 00 REQ4#
 - 01 REQ0#
 - 10 REQ1#
 - 11 REQ2#
- 1 CPU QW or High DW Read Accesses to PCI Slave Allowed To Be Backed Off**
 - 0 Disable..... default
 - 1 Enable
- 0 REQ4# Is High Priority Master**
 - 0 Disable..... default
 - 1 Enable

Device 0 Offset 77 - Chip Test Mode (00h)..... RW

- 7-0 Reserved (do not use)** default=0

Device 0 Offset 78 - PMU Control I (00h).....RW

- 7 I/O Port 22 Access**
 - 0 CPU access to I/O address 22h is passed on to the PCI busdefault
 - 1 CPU access to I/O address 22h is processed internally
- 6 Suspend Refresh Type**
 - 0 CBR Refreshdefault
 - 1 Self Refresh
- 5 Reserved** always reads 0
- 4 Dynamic Clock Control**
 - 0 Normal (clock is always running).....default
 - 1 Clock to various internal functional blocks is disabled when those blocks are not being used
- 3 Reserved** always reads 0
- 2 GSTOP# Assertion**
 - 0 Disable (GSTOP# is always high).....default
 - 1 Enable (GSTOP# could be low)
- 1 Reserved** always reads 0
- 0 Memory Clock Enable (CKE) Function**
 - 0 CKE Function Disable.....default
 - 1 CKE Function Enable

Device 0 Offset 79 - PMU Control 2 (00h)RW

- 7-3 Reserved** always reads 0
- 2 Indicate SIO Request to DRAM Controller**
 - 0 Disabledefault
 - 1 Enable
- 1 Reserved** always reads 0
- 0 2T Rate Snoop Write Enable To Invalidate Read Data Caching Support**
 - 0 Disabledefault
 - 1 Enable

Device 0 Offset 7A – Miscellaneous Control (00h)..... RW

- 7 No Time-Out Arbitration for Consecutive Frame Accesses**
 - 0 Enable default
 - 1 Disable
- 6-5 Reserved** always reads 0
- 4 Invalidate PCI / AGP Buffered (Cached) Read Data for CPU to PCI / AGP Accesses**
 - 0 Disable..... default
 - 1 Enable
- 3 Background PCI-to-PCI Write Cycle Mode**
 - 0 Disable..... default
 - 1 Enable
- 2-1 Reserved** always reads 0
- 0 South Bridge PCI Master Force Timeout When PCI Master Occupancy Timer Is Up**
 - 0 Disable..... default
 - 1 Enable

Device 0 Offset 7B – PCI Master Access Control (00h) RW

- 7-2 Reserved** always reads 0
- 1 PCI Master Access Head / Tail Select**
 - 0 Tail default
 - 1 Head
- 0 Reserved** always reads 0

Device 0 Offset 7E – DLL/PLL Test Mode 1 (00h) RW

- 7-0 Reserved (do not use)** default=0

Device 0 Offset 7F – DLL/PLL Test Mode 2 (00h) RW

- 7-0 Reserved (do not use)** default=0

GART / Graphics Aperture Control

The function of the Graphics Address Relocation Table (GART) is to translate virtual 32-bit addresses issued by an AGP device into 4K-page based physical addresses for system memory access. In this translation, the upper 20 bits (A31-A12) are remapped, while the lower 12 address bits (A11-A0) are used unchanged.

A one-level fully associative lookup scheme is used to implement the address translation. In this scheme, the upper 20 bits of the virtual address are used to point to an entry in a page table located in system memory. Each page table entry contains the upper 20 bits of a physical address (a "physical page" address). For simplicity, each page table entry is 4 bytes. The total size of the page table depends on the GART range (called the "aperture size") which is programmable in the VT8363A.

This scheme is shown in the figure below.

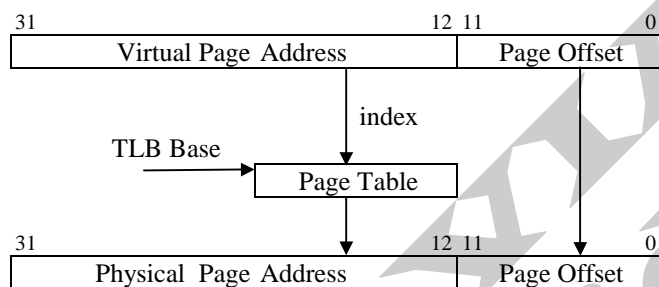


Figure 4. Graphics Aperture Address Translation

Since address translation using the above scheme requires an access to system memory, an on-chip cache (called a "Translation Lookaside Buffer" or TLB) is utilized to enhance performance. The TLB in the VT8363A contains 16 entries. Address "misses" in the TLB require an access of system memory to retrieve translation data. Entries in the TLB are replaced using an LRU (Least Recently Used) algorithm.

Addresses are translated only for accesses within the "Graphics Aperture" (GA). The Graphics Aperture can be any power of two in size from 1MB to 256MB (i.e., 1MB, 2MB, 4MB, 8MB, etc). The base of the Graphics Aperture can be anywhere in the system virtual address space on an address boundary determined by the aperture size (e.g., if the aperture size is 4MB, the base must be on a 4MB address boundary). The Graphics Aperture Base is defined in register offset 10 of device 0. The Graphics Aperture Size and TLB Table Base are defined in the following register group (offsets 84 and 88 respectively) along with various control bits.

Device 0 Offset 83-80 - GART/TLB Control (00000000h) RW

- 31-16 Reserved** always reads 0
- 15 Page TLB Bank Test Data 1 (AND Function) ...RO**
- 14 Page TLB Bank Test Data 0 (OR Function)RO**
- 13 Page LRU ParityRO**
- 12 GART TLB LRU ParityRO**
- 11 GART TLB Test Data 1 (AND Function)RO**
- 10 GART TLB Test Data 0 (OR Function)RO**
- 9 Page TLB Test Data 1 (AND Function)RO**
- 8 Page TLB Test Data 0 (OR Function)RO**
- 7 Flush Page TLB**
- 0 Disabledefault
- 1 Enable
- 6-4 Reserved (always program to 0) RW**
- 3 PCI Master Address Translation for GA Access**
- 0 Addresses generated by PCI Master accesses of the Graphics Aperture will not be translateddefault
- 1 PCI Master GA addresses will be translated
- 2 AGP Master Address Translation for GA Access**
- 0 Addresses generated by AGP Master accesses of the Graphics Aperture will not be translateddefault
- 1 AGP Master GA addresses will be translated
- 1 CPU Address Translation for GA Access**
- 0 Addresses generated by CPU accesses of the Graphics Aperture will not be translated def
- 1 CPU GA addresses will be translated
- 0 AGP Address Translation for GA Access**
- 0 Addresses generated by AGP accesses of the Graphics Aperture will not be translated def
- 1 AGP GA addresses will be translated

Note: For any master access to the Graphics Aperture range, snoop will not be performed.

Device 0 Offset 84 - Graphics Aperture Size (00h) RW

- 7-0 Graphics Aperture Size**
- 11111111 1M
- 11111110 2M
- 11111100 4M
- 11111000 8M
- 11110000 16M
- 11100000 32M
- 11000000 64M
- 10000000 128M
- 00000000 256M

Offset 8B-88 - GA Translation Table Base (00000000h) RW

- 31-12 Graphics Aperture Translation Table Base.**
 Pointer to the base of the translation table in system memory used to map addresses in the aperture range (the pointer to the base of the "Directory" table).
- 11-3 Reserved**always reads 0
- 2 One Cycle TLB Flush**
- 0 Disable default
- 1 Enable
- 1 Graphics Aperture Enable**
- 0 Disable default
- 1 Enable
- Note: To disable the Graphics Aperture, set this bit to 0 and set all bits of the Graphics Aperture Size to 0. To enable the Graphics Aperture, set this bit to 1 and program the Graphics Aperture Size to the desired aperture size.
- 0 Reserved**always reads 0

AGP Control

Device 0 Offset A3-A0 - AGP Capability Identifier

(0020C002h)RO

- 31-24 **Reserved** always reads 00
- 23-20 **Major Specification Revision** ... always reads 0010b
Major rev # of AGP spec that device conforms to
- 19-16 **Minor Specification Revision** ... always reads 0000b
Minor rev # of AGP spec that device conforms to
- 15-8 **Pointer to Next Item**.....always reads C0 (last item)
- 7-0 **AGP ID** .. (always reads 02 to indicate it is AGP)

Device 0 Offset A7-A4 - AGP Status (1F000203h)RO

- 31-24 **Maximum AGP Requests** always reads 1Fh†
Max # of AGP requests the device can manage (32)
† See also RxFC[1] and RxFD[4-0]
- 23-10 **Reserved**always reads 0s
- 9 **Supports SideBand Addressing** always reads 1
- 8-6 **Reserved**always reads 0s
- 5 **4G Supported**(can be written at RxAE[5])
- 4 **Fast Write Supported**(can be written at RxAE[4])
- 3 **Reserved**always reads 0s
- 2 **4X Rate Supported**..... (can be written at RxAE[2])
- 1 **2X Rate Supported**..... (can be written at RxAC[3])
- 0 **1X Rate Supported**..... always reads 1

Device 0 Offset AB-A8 - AGP Command (00000000h) . RW

- 31-24 **Request Depth** (reserved for target).. always reads 0s
- 23-10 **Reserved** always reads 0s
- 9 **SideBand Addressing Enable**
 - 0 Disable..... default
 - 1 Enable
- 8 **AGP Enable**
 - 0 Disable..... default
 - 1 Enable
- 7-6 **Reserved** always reads 0s
- 5 **4G Enable**
 - 0 Disable..... default
 - 1 Enable
- 4 **Fast Write Enable**
 - 0 Disable..... default
 - 1 Enable
- 3 **Reserved** always reads 0s
- 2 **4X Mode Enable**
 - 0 Disable..... default
 - 1 Enable
- 1 **2X Mode Enable**
 - 0 Disable..... default
 - 1 Enable
- 0 **1X Mode Enable**
 - 0 Disable..... default
 - 1 Enable

Device 0 Offset AC - AGP Control (00h)RW

- 7 **Reserved** always reads 0
- 6 **CPU Stall on AGP Command FIFO GART Address Request**
 - 0 Disabledefault
 - 1 Enable
- 5 **AGP Read Snoop DRAM Post-Write Buffer**
 - 0 Disabledefault
 - 1 Enable
- 4 **GREQ# Priority Becomes Higher When Arbiter is Parked at AGP Master**
 - 0 Disabledefault
 - 1 Enable
- 3 **2X Rate Supported** (read also at RxA4[1])
 - 0 Not supporteddefault
 - 1 Supported
- 2 **LPR In-Order Access (Force Fence)**
 - 0 Fence/Flush functions not guaranteed. AGP read requests (low/normal priority and high priority) may be executed before previously issued write requests.....default
 - 1 Force all requests to be executed in order (automatically enables Fence/Flush functions). Low (i.e., normal) priority AGP read requests will never be executed before previously issued writes. High priority AGP read requests may still be executed prior to previously issued write requests as required.
- 1 **AGP Arbitration Parking**
 - 0 Disabledefault
 - 1 Enable (GGNT# remains asserted until either GREQ# de-asserts or data phase ready)
- 0 **AGP to PCI Master or CPU to PCI Turnaround Cycle**
 - 0 2T or 3T Timing.....default
 - 1 1T Timing

Device 0 Offset AD – AGP Latency Timer (02h) RW

- 7 **Reserved** always reads 0
- 6 **AGP Data / Strobe Input Buffer**
 - 0 Disable..... default
 - 1 Enable
- 5 **Hold Last GD Output Data**
 - 0 Disable..... default
 - 1 Enable
- 4 **Choose First or Last Ready of DRAM**
 - 0 Last ready chosen default
 - 1 First ready chosen
- 3-0 **AGP Data Phase Latency Timer** default = 02h

Device 0 Offset AE – AGP Miscellaneous Control (00h)RW

- 7-6 **Reserved** always reads 0
- 5 **Greater Than 4GB Supported**
 - 0 Disable..... default
 - 1 Enable
- 4 **Fast Write Supported**
 - 0 Fast Write not supported..... default
 - 1 Fast Write supported
- 3 **Reserved** always reads 0
- 2 **4x Rate Supported**
 - 0 4x Rate not supported default
 - 1 4x Rate supported
- 1-0 **Reserved** always reads 0

Device 0 Offset AF – AGP Strobe Drive Strength RW

- 7-4 **AGP Strobe Output Buffer Drive Strength N Ctrl**
- 3-0 **AGP Strobe Output Buffer Drive Strength P Ctrl**

Device 0 Offset B0 – AGP Pad Control / Status (8xh)....RW

- 7 AGP Strobe VREF Control**
 - 0 STB VREF is STB# and vice versa
 - 1 STB VREF is AGPREFdefault
- 6 AGP 4x Strobe & GD Pad Drive Strength**
 - 0 Drive strength set to compensation circuit default.....default
 - 1 Drive strength controlled by RxB1[7-0]
- 5-3 AGP Compensation Circuit N Control Output .RO**
- 2-0 AGP Compensation Circuit P Control Output .RO**

Device 0 Offset B1 – AGP Drive Strength (63h).....RW

- 7-4 AGP Output Buffer Drive Strength N Ctrl ...def=6**
- 3-0 AGP Output Buffer Drive Strength P Ctrl....def=3**

Device 0 Offset B2 – AGP Pad Drive / Delay Control ... RW

- 7 GD/GBE/GDS, SBA/SBS Control**
 - 1.5V (Bit-1 = 0)**
 - 0 SBA/SBS = no cap default
 - GD/GBE/GDS = no cap
 - 1 SBA/SBS = no cap
 - GD/GBE/GDS = **cap**
 - 3.3V (Bit-1 = 1)**
 - 0 SBA/SBS = **cap** default
 - GD/GBE/GDS = no cap
 - 1 SBA/SBS = **cap**
 - GD/GBE/GDS = **cap**
- 6 Reserved** always reads 0
- 5 S2K Slew Rate Controlstrapped from SRASA#**
 - 0 Enable default
 - 1 Disable
- 4 GD[31-16] Staggered Delay**
 - 0 None default
 - 1 GD[31:16] delayed by 1 ns
- 3 Reserved** always reads 0
- 2 AGP Preamble Control**
 - 0 Disable..... default
 - 1 Enable
- 1 AGP Voltage**
 - 0 1.5V default
 - 1 3.3V
- 0 GDS Output Delay**
 - 0 None default
 - 1 GDS[1-0] & GDS[1-0]# delayed by 0.4 ns
(GDS1 & GDS1# will be delayed an additional 1ns if bit-4 = 1)

Device 0 Offset B3 – CPU Strapping Control.....RO

- 7-3 CPU Clock Division ..4 lsbs set from MA3-0 straps**
 00000 11 no strap default
 00001 11.5
 00010 12
 00011 12.5
 00100 5
 00101 5.5
 00110 6
 00111 6.5
 01000 7
 01001 7.5
 01010 8
 01011 8.5
 01100 9
 01101 9.5
 01110 10
 01111 10.5
 10000 3
 10001 3.5
 10010 4
 10011 4.5
 101xx -reserved-
2 S2K Compensation Drive Strength
 0 Strapdefault
 1 Auto Calculate
1 Fast Address Out Decode
 set from ROMSIP, otherwise 0
 0 Normalno strap default
 1 Fast
0 S2K Compensation Circuit
 0 Enable on Reset.....default
 1 Enable on Disconnect

Device 0 Offset B4 – S2K Compensation Strapping.....RW

- 7 Internal Pullup Strength Select**
 0 Per strapping on MA[13-12] (see bits 5-4).. def
 1 Auto Mode
6 Reserved always reads 0
5-4 Internal Pullup Strength set from MA[13-12] straps
 00 Strapping Modeno strap default
 01 Strapping Mode
 10 Strapping Mode
 11 Auto Mode
3 Output Drive Strength Select
 0 Per strapping on MA[10-9] (see bits 1-0).... def
 1 Auto Mode
2 Reserved always reads 0
1-0 Output Drive Strength set from MA[10-9] strap
 00 Auto Modeno strap default
 01 Strapping Mode
 10 Strapping Mode
 11 Strapping Mode

Device 0 Offset B5 – S2K Compensation Result 1 RO

- 7-4 Pullup Autocompensation Result** default = 0
3-0 Pulldown Autocompensation Result default = 0

Device 0 Offset B6 – S2K Compensation Result 2 RO

- 7 S2K Edge DQ Mode**set from MA11 strap
 0 Central DQ..... default
 1 Edge DQ
6-5 Reservedalways reads 0
4-0 S2K Strobe Delay (EdgeDQ)
 set from MA[8-4] straps
 0 Auto Mode..... no-strap default
 ~0 Strapping Mode

Device 0 Offset B7 – S2K Compensation Result 3 RO

- 7-5 Reserved**always reads 0
4-0 S2K Strobe Delay from DLL Counter (Auto)
 default = 0

Device 0 Offset B8 – S2K Compensation Result 4 RO

- 7 S2K Compensation Circuit Trigger**
6 DLL Autodetect..... RO
5 Delay Compensation Counter Control
4-3 S2K Pad AC Coupling to VREF Signal in Address / Data Output Clock
2-0 S2K Pad Slew Rate Ctrl (7h is strongest).... def=7h

Device 0 Offset C0 – Power Management Capability IDRO

7-0 Capability ID always reads 01h

Device 0 Offset C1 – Power Management New Pointer..RO

7-0 New Pointeralways reads 00h (“Null” Pointer)

Device 0 Offset C2 – Power Mgmt Capabilities I.....RO

7-0 Power Management Capabilities.. always reads 02h

Device 0 Offset C3 – Power Mgmt Capabilities II.....RO

7-0 Power Management Capabilities.. always reads 00h

Device 0 Offset C4 – Power Mgmt Control / Status.....RW

7-2 Reserved always reads 0

1-0 Power State

00 D0default
 01 -reserved-
 10 -reserved-
 11 D3 Hot

Device 0 Offset C5 – Power Management StatusRO

7-0 Power Management Status..... always reads 00h

Device 0 Offset C6 – PCI-to-PCI Bridge Support Ext. ...RO

7-0 P2P Bridge Support Extensions.... always reads 00h

Device 0 Offset C7 – Power Management Data.....RO

7-0 Power Management Data always reads 00h

Device 0 Offset E0 – Miscellaneous Control (00h)RW

7 AGP Pad Power Down

0 Disabledefault
 1 Enable

6 Reserved (do not program) must be 0

5 Internal Graphics AGP/PCI Concurrent..... def = 0

4 CKE Drive Select default = 0

3-1 Frame Buffer Bank Location default = 0

0 Latch DRAM Data Using

0 Internal DRAM DCLK.....default
 1 External Feedback DRAM DCLK

Device 0 Offset F0 – BIOS Scratch Register 0 RW

7-0 No hardware function default = 0

Device 0 Offset F1 – BIOS Scratch Register 1 RW

7-0 No hardware function default = 0

Device 0 Offset F2 – BIOS Scratch Register 2 RW

7-0 No hardware function default = 0

Device 0 Offset F3 – BIOS Scratch Register 3 RW

7-0 No hardware function default = 0

Device 0 Offset F4 – BIOS Scratch Register 4 RW

7-0 No hardware function default = 0

Device 0 Offset F5 – BIOS Scratch Register 5 RW

7-0 No hardware function default = 0

Device 0 Offset F6 – Revision ID Backdoor RW

7-0 Revision ID Rx8 default = 0

Device 0 Offset F7 – Foundry ID..... RW

7-0 No hardware function default = foundry ID

Device 0 Offset F8 – DRAM Arbitration Timer (00h)... RW

7-4 AGP Timer (units of 4 DCLKs)..... default = 0

3-0 Host CPU Timer (units of 4 DCLKs)..... default = 0

Device 0 Offset FC – Back Door Control 1 (00h)..... RW

7-4 Priority Timer default = 0

3-2 Probe Signal Select default = 0

1 Back-Door Max # of AGP Requests..... default = 0

0 Read of RxA7 always returns a value of 1111b (32 requests) default
 1 Read of RxA7 returns the value programmed in RxFD[4-0]

0 Back-Door Device ID Enable..... default = 0

0 Use Rx3-2 value for Rx3-2 readback..... default
 1 Use RxFE-FF Back-Door Device ID for Rx3-2 read

Device 0 Offset FD – Back-DoorControl 2 (00h) RW

7-5 Reserved always reads 0

4-0 Max # of AGP Requests default = 0

00000 1 Request

00001 2 Requests

00010 3 Requests

... ..

11111 32 Requests

(see also RxA7 and RxFC[1])

Device 0 Offset FF-FE – Back-Door Device ID (0000h) RW

15-0 Back-Door Device ID..... default=00

Device 1 Header Registers - PCI-to-PCI Bridge

All registers are located in PCI configuration space. They should be programmed using PCI configuration mechanism 1 through CF8 / CFC with bus number of 0 and function number equal to 0 and device number equal to one.

Device 1 Offset 1-0 - Vendor ID (1106h).....RO

15-0 ID Code (reads 1106h to identify VIA Technologies)

Device 1 Offset 3-2 - Device ID (8305h).....RO

15-0 ID Code (reads 8305h to identify the VT8363A PCI-to-PCI Bridge device)

Device 1 Offset 5-4 - Command (0007h).....RW

- 15-10 Reserved** always reads 0
- 9 Fast Back-to-Back Cycle Enable** RO
- 0 Fast back-to-back transactions only allowed to the same agentdefault
- 1 Fast back-to-back transactions allowed to different agents
- 8 SERR# Enable**..... RO
- 0 SERR# driver disableddefault
- 1 SERR# driver enabled
- (SERR# is used to report parity errors if bit-6 is set).
- 7 Address / Data Stepping** RO
- 0 Device never does steppingdefault
- 1 Device always does stepping
- 6 Parity Error Response**.....RW
- 0 Ignore parity errors & continuedefault
- 1 Take normal action on detected parity errors
- 5 VGA Palette Snoop (Not Supported)**..... RO
- 0 Treat palette accesses normallydefault
- 1 Don't respond to palette writes on PCI bus (10-bit decode of I/O addresses 3C6-3C9 hex)
- 4 Memory Write and Invalidate Command**..... RO
- 0 Bus masters must use Mem Writedefault
- 1 Bus masters may generate Mem Write & Inval
- 3 Special Cycle Monitoring** RO
- 0 Does not monitor special cyclesdefault
- 1 Monitors special cycles
- 2 Bus Master**RW
- 0 Never behaves as a bus master
- 1 Enable to operate as a bus master on the primary interface on behalf of a master on the secondary interfacedefault
- 1 Memory Space**.....RW
- 0 Does not respond to memory space
- 1 Enable memory space accessdefault
- 0 I/O Space**RW
- 0 Does not respond to I/O space
- 1 Enable I/O space accessdefault

Device 1 Offset 7-6 - Status (Primary Bus) (0230h).... RWC

- 15 Detected Parity Error** always reads 0
- 14 Signaled System Error (SERR#)** always reads 0
- 13 Signaled Master Abort**
- 0 No abort received default
- 1 Transaction aborted by the master with Master-Abort (except Special Cycles) write 1 to clear
- 12 Received Target Abort**
- 0 No abort received default
- 1 Transaction aborted by the target with Target-Abort write 1 to clear
- 11 Signaled Target Abort**..... always reads 0
- 10-9 DEVSEL# Timing**
- 00 Fast
- 01 Medium always reads 01
- 10 Slow
- 11 Reserved
- 8 Data Parity Error Detected** always reads 0
- 7 Fast Back-to-Back Capable** always reads 0
- 6 User Definable Features**..... always reads 0
- 5 66MHz Capable**..... always reads 1
- 4 Supports New Capability list**..... always reads 1
- 3-0 Reserved** always reads 0

Device 1 Offset 8 - Revision ID (00h) RO

7-0 VT8363A Chip Revision Code (00=First Silicon)

Device 1 Offset 9 - Programming Interface (00h) RO

This register is defined in different ways for each Base/Sub-Class Code value and is undefined for this type of device.

7-0 Interface Identifier always reads 00

Device 1 Offset A - Sub Class Code (04h) RO

7-0 Sub Class Code .reads 04 to indicate PCI-PCI Bridge

Device 1 Offset B - Base Class Code (06h)..... RO

7-0 Base Class Code.. reads 06 to indicate Bridge Device

Device 1 Offset D - Latency Timer (00h) RO

7-0 Reserved always reads 0

Device 1 Offset E - Header Type (01h) RO

7-0 Header Type Code..... reads 01: PCI-PCI Bridge

Device 1 Offset F - Built In Self Test (BIST) (00h) RO

- 7 BIST Supported**..... reads 0: no supported functions
- 6 Start Test** write 1 to start but writes ignored
- 5-4 Reserved** always reads 0
- 3-0 Response Code**..... 0 = test completed successfully

Device 1 Offset 18 - Primary Bus Number (00h)RW

7-0 Primary Bus Number default = 0

This register is read write, but internally the chip always uses bus 0 as the primary.

Device 1 Offset 19 - Secondary Bus Number (00h).....RW

7-0 Secondary Bus Number default = 0

Note: AGP must use these bits to convert Type 1 to Type 0.

Device 1 Offset 1A - Subordinate Bus Number (00h).....RW

7-0 Primary Bus Number default = 0

Note: AGP must use these bits to decide if Type 1 to Type 1 command passing is allowed.

Device 1 Offset 1B – Secondary Latency Timer (00h)RO

7-0 Reserved always reads 0

Device 1 Offset 1C - I/O Base (f0h).....RW

7-4 I/O Base AD[15:12] default = 1111b

3-0 I/O Addressing Capability default = 0

Device 1 Offset 1D - I/O Limit (00h).....RW

7-4 I/O Limit AD[15:12] default = 0

3-0 I/O Addressing Capability default = 0

Device 1 Offset 1F-1E - Secondary Status (0000h).....RO

15-0 Rx44[4] = 0: No Function (always reads 0)
Rx44[4] = 1: Read same value as Rx7-6 (Pri Status)

Device 1 Offset 21-20 - Memory Base (fff0h).....RW

15-4 Memory Base AD[31:20] default = FFFh

3-0 Reserved always reads 0

Device 1 Offset 23-22 - Memory Limit (Inclusive) (0000h) RW

15-4 Memory Limit AD[31:20] default = 0

3-0 Reserved always reads 0

Device 1 Offset 25-24 - Prefetchable Memory Base (fff0h) RW

15-4 Prefetchable Memory Base AD[31:20] default = FFFh

3-0 Reserved always reads 0

Device 1 Offset 27-26 - Prefetchable Memory Limit
(0000h)RW

15-4 Prefetchable Memory Limit AD[31:20] default = 0

..... default = 0

3-0 Reserved always reads 0

Device 1 Offset 2D-2C – Subsystem Vendor ID (0000h) RW
Device 1 Offset 2F-2E – Subsystem ID (0000h)RW
Device 1 Offset 34 – Capability Pointer (00h)RO

7-0 Capability Pointer always reads 00h

Device 1 Offset 3F-3E – PCI-to-PCI Bridge Control
(0000h) RW

15-4 Reserved always reads 0

3 VGA-Present on AGP

0 Forward VGA accesses to PCI Bus default

1 Forward VGA accesses to AGP Bus

Note: VGA addresses are memory A0000-BFFFFh and I/O addresses 3B0-3BBh, 3C0-3CFh and 3D0-3DFh (10-bit decode). "Mono" text mode uses B0000-B7FFFh and "Color" Text Mode uses B8000-BFFFFh. Graphics modes use Axxxxh. Mono VGA uses I/O addresses 3Bx-3Cxh and Color VGA uses 3Cx-3Dxh. If an MDA is present, a VGA will not use the 3Bxh I/O addresses and B0000-B7FFFh memory space; if not, the VGA will use those addresses to emulate MDA modes.

2 Block / Forward ISA I/O Addresses

0 Forward all I/O accesses to the AGP bus if they are in the range defined by the I/O Base and I/O Limit registers (device 1 offset 1C-1D)

..... default

1 Do not forward I/O accesses to the AGP bus that are in the 100-3FFh address range even if they are in the range defined by the I/O Base and I/O Limit registers.

1-0 Reserved always reads 0

Device 1 Configuration Registers - PCI-to-PCI Bridge
AGP Bus Control
Device 1 Offset 40 - CPU-to-AGP Flow Control 1 (00h) RW

- 7 CPU-AGP Post Write**
 0 Disabledefault
 1 Enable
- 6 CPU-AGP Dynamic Burst**
 0 Disabledefault
 1 Enable
- 5 CPU-AGP One Wait State Burst Write**
 0 Disabledefault
 1 Enable
- 4 AGP to DRAM Prefetch**
 0 Disabledefault
 1 Enable
- 3 CPU to AGP Post Write Halt**
 0 Disabledefault
 1 Enable
 If set to 1, CPU-to-PCI posted cycles can be delayed for PCI master accesses (i.e., PCI master access is allowed even if the CPU-to-PCI buffer is not flushed)
- 2 MDA Present on AGP**
 0 Forward MDA accesses to AGPdefault
 1 Forward MDA accesses to PCI
 Note: Forward despite IO / Memory Base / Limit
 Note: MDA (Monochrome Display Adapter) addresses are memory addresses B0000h-B7FFFh and I/O addresses 3B4-3B5h, 3B8-3BAh, and 3BFh (10-bit decode). 3BC-3BE are reserved for printers.
 Note: If Rx3E bit-3 is 0, this bit is a don't care (MDA accesses are forwarded to the PCI bus).
- 1 AGP Master Read Caching**
 0 Disabledefault
 1 Enable
- 0 AGP Delay Transaction**
 0 Disabledefault
 1 Enable

Table 7. VGA/MDA Memory/IO Redirection

<u>3E[3]</u>	<u>40[2]</u>	<u>VGA</u>	<u>MDA</u>	<u>Axxxx</u>	<u>B0000</u>	<u>3Cx</u>	
<u>VGA</u>	<u>MDA</u>	<u>is</u>	<u>is</u>	<u>B8xxx</u>	<u>-B7FFF</u>	<u>3Dx</u>	<u>3Bx</u>
<u>Pres.</u>	<u>Pres.</u>	<u>on</u>	<u>on</u>	<u>Access</u>	<u>Access</u>	<u>I/O</u>	<u>I/O</u>
0	-	PCI	PCI	PCI	PCI	PCI	PCI
1	0	AGP	AGP	AGP	AGP	AGP	AGP
1	1	AGP	PCI	AGP	PCI	AGP	PCI

Device 1 Offset 41 - CPU-to-AGP Flow Control 2 (00h) RW

- 7 Retry Status**
 0 No retry occurred default
 1 Retry Occurred**write 1 to clear**
- 6 Retry Timeout Action**
 0 No action taken except to record status def
 1 Flush buffer for write or return all 1s for read
- 5-4 Retry Count**
 00 Retry 2, backoff CPU default
 01 Retry 4, backoff CPU
 10 Retry 16, backoff CPU
 11 Retry 64, backoff CPU
- 3 Post Write Data on Abort**
 0 Flush entire post-write buffer on target-abort or master abort default
 1 Pop one data output on target-abort or master-abort
- 2 CPU Backoff on AGP Read Retry Timeout**
 0 Disable default
 1 Enable
- 1-0 Reserved**always reads 0

Device 1 Offset 42 - AGP Master Control (00h) RW

- 7 Read Prefetch for Enhance Command**
 0 Always Perform Prefetch default
 1 Prefetch only if Enhance Command
- 6 AGP Master One Wait State Write**
 0 Disable default
 1 Enable
- 5 AGP Master One Wait State Read**
 0 Disable default
 1 Enable
- 4 Reserved**always reads 0
- 3 AGP Delay Transaction Timeout**
 0 Disable default
 1 Enable
- 2 Prefetch Disable when Delay Transaction Occurs**
 0 Normal operation default
 1 Disable prefetch when doing fast response to the previous delay transaction or doing read caching
- 1 Reserved**always reads 0
- 0 Generate STOP# When AGP Master Access Crosses Cache Line Boundary**
 0 Disable default
 1 Enable

Device 1 Offset 43 - AGP Master Latency Timer (00h) RW

- 7-4 Host to AGP Time Slot**
 0 Disable (no timer).....default
 1 16 GCLKs
 2 32 GCLKs

 F 240 GCLKs
- 3-0 AGP Master Time Slot**
 0 Disable (no timer).....default
 1 16 GCLKs
 2 32 GCLKs

 F 240 GCLKs

Device 1 Offset 44 – Backdoor Register Control (00h) .RW

- 7-6 Reserved** always reads 0
- 5 Rx34 Capability Back Door**
- 4 Reflect Rx7-6 Status in Rx1F-1E**
 0 Disable (Rx1F-1E always reads 0)default
 1 Enable (Rx1F-1E reads same as Rx7-6)
- 3-2 Rx83[2-1] Back Door Value**
- 1 Rx82[5] Back Door Value (Device Specific Intfc)**
- 0 Back Door Register Enable for AGP Device ID (Rx47-46)**
 0 Disabledefault
 1 Enable

Device 1 Offset 45 – Fast Write Control (72h)..... RW

- 7 Force Fast Write Cycle to be QW Aligned**
 (if Rx45[6] = 0)
 0 Disable..... default
 1 Enable
- 6 Merge Multiple CPU Transactions Into One Fast Write Burst Transaction**
 0 Disable
 1 Enable default
- 5 Merge Multiple CPU Write Cycles To Memory Offset 23-20 Into Fast Write Burst Cycles**
 (if Rx45[6] = 0)
 0 Disable
 1 Enable default
- 4 Merge Multiple CPU Write Cycles To Prefetchable Memory Offset 27-24 Into Fast Write Burst Cycles** (if Rx45[6] = 0)
 0 Disable
 1 Enable default
- 3 Reserved** always reads 0
- 2 Fast Write Burst 4T Max (No Slave Flow Control)**
 0 Disable..... default
 1 Enable
- 1 Fast Write Fast Back to Back**
 0 Disable
 1 Enable default
- 0 Fast Write Initial Block 1 Wait State**
 0 Disable..... default
 1 Enable

Rx45 Bits	CPU Write Address in Mem1	CPU Write Address in Mem2	Fast Write Cycle Alignment
7-4			
x1xx	-	-	QW aligned, burstable
0000	-	-	DW aligned, nonburstable
x010	0	0	n/a
0010	0	1	DW aligned, non-burstable
x010	1	-	QW aligned, burstable
x001	0	0	n/a
x001	-	1	QW aligned, burstable
0001	1	0	DW aligned, non-burstable
x011	0	0	n/a
x011	1	-	QW aligned, burstable
x011	0	1	QW aligned, burstable
1000	-	-	QW aligned, non-burstable
1010	0	1	QW aligned, non-burstable
1001	1	0	QW aligned, non-burstable

Device 1 Offset 47-46 – PCI-to-PCI Bridge Device ID...RW

15-0 PCI-to-PCI Bridge Device ID..... default = 0000

Device 1 Offset 80 – Capability ID (01h) RO

7-0 Capability ID always reads 01h

Device 1 Offset 81 – Next Pointer (00h)..... RO

7-0 Next Pointer: Null..... always reads 00h

Device 1 Offset 82 – Power Mgmt Capabilities 1 (02h).. RO

7-6 Power Mgmt Capabilities always reads 0

5 Power Mgmt Capabilities .programmed via Rx44[1]

4-0 Power Mgmt Capabilities always reads 02h

Device 1 Offset 83 – Power Mgmt Capabilities 2 (00h).. RO

7-3 Power Mgmt Capabilities always reads 0

2-1 Power Mgmt Capabilitiesprogrammed via Rx44[3-2]

0 Power Mgmt Capabilities always reads 0

Device 1 Offset 84 – Power Mgmt Ctrl/Status (00h)..... RW

7-2 Reserved always reads 0

1-0 Power State

00 D0 default

01 -reserved-

10 -reserved-

11 D3 Hot

Device 1 Offset 85 – Power Mgmt Status (00h)..... RO

7-0 Power Mgmt Status default = 00

Device 1 Offset 86 – P2P Br. Support Extensions (00h). RO

7-0 P2P Bridge Support Extensions..... default = 00

Device 1 Offset 87 – Power Management Data (00h) RO

7-0 Power Management Data..... default = 00

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Min	Max	Unit
Case operating temperature	0	110	°C
Storage temperature	-55	125	°C
Input voltage	-0.5	5.5	Volts
Output voltage ($V_{CC} = 3.1 - 3.6V$)	-0.5	$V_{CC} + 0.5$	Volts

Note: Stress above the conditions listed may cause permanent damage to the device. Functional operation of this device should be restricted to the conditions described under operating conditions.

DC Characteristics

$T_C -0-85^{\circ}C$, $V_{CC}=5V \pm 5\%$, $GND=0V$

Symbol	Parameter	Min	Max	Unit	Condition
V_{IL}	Input low voltage	-0.50	0.8	V	
V_{IH}	Input high voltage	2.0	$V_{CC}+0.5$	V	
V_{OL}	Output low voltage	-	0.45	V	$I_{OL}=4.0mA$
V_{OH}	Output high voltage	2.4	-	V	$I_{OH}=-1.0mA$
I_{IL}	Input leakage current	-	± 10	μA	$0 < V_{IN} < V_{CC}$
I_{OZ}	Tristate leakage current	-	± 20	μA	$0.45 < V_{OUT} < V_{CC}$

Power Characteristics

T_C -0-85°C, V_{CC} =5V+/-5%, GND=0V

Symbol	Parameter	Typ	Max	Unit	Condition
I_{CC3}	Power Supply Current – VCC3			mA	Max operating frequency
I_{SUS3}	Power Supply Current – VSUS3			mA	Max operating frequency
I_{TT}	Power Supply Current – VTT			mA	Max operating frequency
I_{CCS2K}	Power Supply Current – S2KVCC			mA	Max operating frequency
I_{CCQ}	Power Supply Current – VCCQ			mA	Max operating frequency
I_{CCQQ}	Power Supply Current – VCCQQ			mA	Max operating frequency
I_{CCHCK}	Power Supply Current – VCCHCK			mA	Max operating frequency
I_{CCMCK}	Power Supply Current – VCCMCK			mA	Max operating frequency
I_{CCGCK}	Power Supply Current – VCCGCK			mA	Max operating frequency
I_{CCS2KV}	Power Supply Current – S2KVREF			uA	Max operating frequency
I_{CCAGPV}	Power Supply Current – AGPVREF			uA	Max operating frequency
I_{CLKV}	Power Supply Current – CLKVREF			uA	Max operating frequency
I_{CC}	Power Dissipation		3.5	W	Max operating frequency

AC Timing Specifications

AC timing specifications provided are based on external zero-pf capacitance load. Min/max cases are based on the following table:

Table 8. AC Timing Min / Max Conditions

Parameter	Min	Max	Unit
3.3V Power (VCC3, VSUS3, VTT, VCCHCK, VCCMCK, VCCGCK)	3.135	3.465	Volts
1.5V Power (VCCQ, VCCQQ)	1.425	1.575	Volts
Case Temperature	0	85	°C

Drive strength for each output pin is programmable. See Rx6D for details.

MECHANICAL SPECIFICATIONS

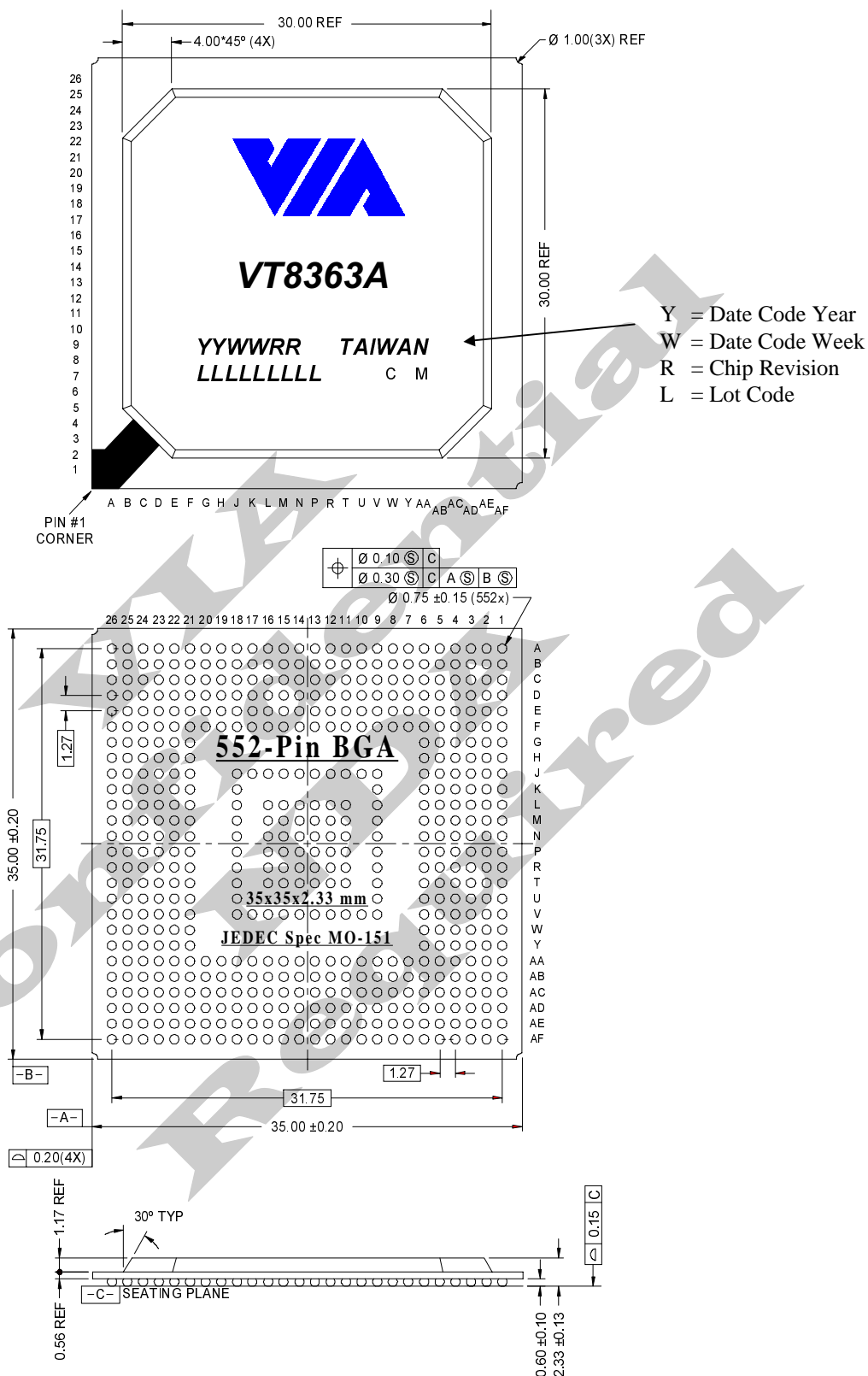


Figure 5. Mechanical Specifications - 552-Pin Ball Grid Array Package