Data Sheet

CN896
North Bridge

with PCI Express and Chrome9™ HC IGP

Preliminary Revision 0.6
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VIA TECHNOLOGIES, INC.

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REVISION HISTORY

Document Release	Date	Revision	Initials
0.5	6/2/06	Initial Internal Release	JY
0.51	6/12/06	Updated power plane for signal RESET# to VCCMEM Updated frame buffer size to 64/128/256 Updated Registers — D0F0 Rx5-4[6]: Updated bit description and attribute — D0F0 Rx7-6[13]: Updated attribute — D0F0 Rx93-90[7]: Modified default value — D0F0 RxB9[7]: Updated attribute — D0F0 RxBE: Added this register — D0F2 Rx7D[1]: Reserved — D0F3 Rx74[6:4]: Reserved — D0F5 Rx80[4]: Added this register — D0F6 Rx33-30: Reserved — D1F0 Rx48: Added this register — D2/D3F0 Rx4F-4C[9:4]: Updated bit description — D2/D3F0 RxE1[1:0]: Updated bit description Added Ultra V-Link mode in Table 19	JY
0.52	8/2/06	Updated DVP0 descriptions Updated Register — D0F3 RxB0-BF: Added registers — D0F5 Rx44[4]: Added registers — D2/D3F0 Rx4C[14:12] Updated default value to 011b — D2/D3F0 RxA3[0]: Updated default value to 0 — D2/D3F0 RxA4[0]: Updated registers description — D2F0 RxA6[7]: Updated bit description — D2/D3F0 RxA7[7]: Updated bit description — D2/D3F0 Rx190[15:2]: Changed attribute to RO	JY
0.53	8/11/06	Updated Strap Signals — DVP2D11: Not compulsory pull down — VD02: Pull down to 12-level deep Updated Register — D0F2 Rx50[7]: Updated bit description	JY
0.54	8/29/06	Updated system block diagram Removed DVP 0 support	JY
0.6	12/22/06	Updated cover page, header and legal page Updated FSB support and SB support Changed core power to 1.6V Updated Registers: — Updated register overview — Added D0F0 Rx40 and Rx41 — Reserved D0F2 Rx58 — Added D0F2 Rx74[7:6] and RxB2[7] — Reserved D0F3 Rx67[7:6], Rx6C[5, 2:0], Rx98[4] — Modified the attribute of D0F3 Rx77[5:0] — Added D0F3 RxA5-A0 — Updated the default values of D0F3 RxD6, RxE6 — Modified D0F5 Rx6B-68[23:0] and Rx6F-6C[23:0] — Updated the default values of D0F7 RxB0, RxB6 — Updated D1F0 Rx3F-3E[11, 9:8] — Updated the default values of D0F7 RxB0, RxB6 — Updated the default values of D2F0 / D3F0 Rx43-42, Rx47-44, Rx49-48 and Rx10F-10C — Modified bit descriptions of D2F0 / D3F0 RxB4[2:0] — Modified the attribute of D2F0 Rx14C[0] — Added D2F0 / D3F0 Rx193-190[15:2] — Modified the attributes of RCRB-H / RCRB-V Rx00C[3:1]	EY

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

CN896 NORTH BRIDGE

400 MHz Front Side Bus
Two PCI Express Ports: 16-Lane & 1-Lane
Integrated Chrome9™ HC IGP & Video Controller
Advanced 64-bit DDR2 / DDR SDRAM Controller
1 GB/Sec Ultra V-Link Interface

PRODUCT FEATURES

- **Defines Highly Integrated Solutions for Value Embedded PC Designs**
  - High Performance UMA North Bridge: Integrated VIA C7 North Bridge with 400 MHz FSB support, PCI Express bus controller and Chrome9™ HC IGP & Video controllers
  - Advanced 64-bit SDRAM controller supporting DDR2 667 / 533 / 400 and DDR 400 / 333 SDRAM
  - Combines with VIA VT8237S and VT8251 South Bridges for integrated 10/100 LAN, Serial ATA, ATA133 IDE, USB 2.0, High Definition Audio Codec and LPC
  - 37.5 x 37.5mm HSBGA package (Ball Grid Array with Heat Spreader) with 951 balls and 1.00 mm ball pitch
- **High Performance CPU Interface**
  - Supports 400 MHz FSB
  - Supports DBI (Dynamic Bus Inversion)
  - Supports Trust configuration cycle
  - Deep In-Order command Queue (IOQ)
  - Integrated CPU-to-DRAM write buffers and CPU-to-DRAM read prefetch buffers
  - Built-in Phase Lock Loop circuitry for optimal skew control within and between clocking regions
- **Advanced High Bandwidth PCI Express Interface**
  - Supports PCI Express 1.1
  - Supports up to two PCI Express ports
    - 1st port: a 16-Lane port for high end graphics interface
      - Configurable lane width, 16 / 8 / 4 / 2 / 1, through hand-shaking for transfer rate up to 4 GB/sec bidirectional
      - Supports two upstream virtual channels
    - 2nd port: a 1-Lane port for peripheral devices
  - Supports interconnect power management
  - Supports polarity reversal
  - Supports Trust configuration cycle
  - Supports Hot Plug
  - Loop-back testing mode for easy debugging mode for PCI Express

- **Advanced High-Performance DDR2 / DDR SDRAM Controller**
  - Supports two operating modes:
    - DDR2 Mode
      - Supports DDR2 667 / 533 / 400 memory
      - Supports mixed 64 / 128 / 256 / 512 / 1024 / 2048 x 8/16 DDR2 SDRAMs
      - Supports 2 unbuffered double-sided DIMMs and up to 4 GB of physical memory
      - Supports CL 2 / 3 / 4 / 5 for DDR2 667 / 533 / 400
    - DDR Mode
      - Supports DDR 400 / 333 memory
      - Supports mixed 64 / 128 / 256 / 512 / 1024 Mb x 8/16 DDR SDRAMs
      - Supports 2 unbuffered double-sided DIMMs and up to 4 GB of physical memory
      - Supports CL 2 / 2.5 for DDR 333, CL 2.5 / 3 for DDR 400
  - Programmable I/O drive capability for memory address, data and control signals
  - DRAM interface pseudo-synchronous with host CPU for optimal memory performance
  - Concurrent CPU, PCIe, internal graphics controller and Ultra V-Link access for minimum memory access latency
  - Rank interleave and up to16-bank page interleave (i.e., 16 pages open simultaneously) based on LRU to effectively reduce memory access latency
  - Seamless DRAM command scheduling for maximum DRAM bus utilization (e.g., precharge other banks while accessing the current bank)
  - CPU Read-Around-Write capability for non-stalled operation
  - Speculative DRAM read before snoop result to reduce PCI master memory read latency
  - Supports Burst Read and Write operations with burst length of 4 or 8
  - Optional dynamic Clock Enable (CKE) control for DRAM power reduction during normal system state (S0)
  - Supports self-refresh and CAS-before-RAS DRAM refresh with staggered RAS timing
- **High Bandwidth 1 GB/Sec "Ultra V-Link" Host Controller**
  - Supports 16-bit 66 MHz, 4x and 8x transfer modes, Ultra V-Link Host interface with 1 GB/sec total bandwidth
  - Full duplex transfers with separate command / strobe for 4x and 8x mode
  - Request / Data split transaction
  - Transaction assurance for V-Link Host to Client access eliminates V-Link Host-Client Retry cycles
  - Intelligent V-Link transaction protocol to minimize data wait-state, throttle transfer latency and avoid data overflow
  - Highly efficient V-Link arbitration with minimum overhead
- **Advanced System Power Management Support**
  - ACPI 2.0 and PCI Bus Power Management 1.1 compliant
  - Supports Suspend-to-DRAM (STR) and DRAM self refresh
  - Supports dynamic Clock Enable (CKE) control for DRAM power reduction during normal system state (S0)
  - Supports SMI, SMM and STPCLK mechanisms
  - Low-leakage I/O pads

- **Chrome9™ HC Integrated Graphics with 2D / 3D / Video Controllers**
  - Optimized Unified Memory Architecture (UMA)
  - Supports 64 / 128 / 256 MB Frame Buffer Size
  - Graphics engine clocks up to 250 MHz decoupled from memory clock
  - Internal AGP 8x performance
  - Two 128-bit internal data paths between North Bridge and graphics core for frame buffer and texture /command access
  - PCI v2.2 Host Bus compliant
  - AGP v3.5 compliant

2D Acceleration Features

- 128-bit 2D graphics engine
- Supports ROP3, 256 operations
- Supports 8bpp, 15/16bpp and 32bpp color depth modes
- BitBLT (Bit Block Transfer) functions, including alpha BLTs
- Color expansion, source Color Key and destination Color Key
- Bresenham line drawing / style line function
- Transparency mode
- Window clipping
- Text function

3D Acceleration Features

- DirectX 9.0 programmable graphics engine
- 1 Pixel Shader (PS 2.0)
- Internal full ARGB 10-10-10-10 format for high rendering quality
- 96-bit (4xFP24) Pixel Precision
- Pixel Shader Supports 16 Concurrent Texture Map References Per Rendering Pass
- Shadow Volume Acceleration (2-Sided Stencil)
- Unconditional Non-Power-Of-2 Textures
- MIP-Mapped Volume/Cube Maps
- Floating Point Render Target/Texture Formats
- Vertex Cache
- Color buffer with sRGB format supported and blending with color fields 1.0
- Supports various texture formats, including 16/32bpp RGB, 32bpp sRGB, YUV422, V410, compressed texture (DXTC) and depth texture
- Video Texture supported with programmable de-Gamma (up to Gamma 3.0)
- Multiple Render Target (MRT) up to 4
- Perspective Color, Fog, texture
- High Quality texture filtering with bi-linear, tri-linear, anisotropy (up to 16x by trilinear), or programmable 4x4 filter (Gaussian filter, HP filter, LP filter)
- Supports 2048x2048x32bpp

Hi Definition Video Processor Features

- Supports Chronmotion Programmable Video Engine
- Integrated 3D and Video Processing Through Pixel Shader Engine
- Bob, Weave and Medium Filter de-interlacing modes
- High Quality Video Scaling Engine Supports Input up to 1920 Pixels Wide
- Supports Microsoft VMR Through Front-End Video Scaling, Color Space Conversion and Blending

- **Extensive Display Support for External Video Output**
  - A dedicated CRT interface
  - An PCIe-multiplexed 12-bit (DVP1 port) interface to external DVI transmitter or LVDS transmitter
  - A dedicated (DVP2 port) TV-Out interface to TV encoder

CRT Display

- CRT display interface with 24-bit true-color RAMDAC up to 300 MHz pixel rate with gamma correction capability
- Supports CRT resolutions up to 1920x1440

DVI Transmitter Interface

- 12-bit, 1.5V low-swing, DVO interface for connecting DVI Monitor through DVI transmitter
- 12-bit DDR and clock rate up to 165 MHz
- Built-in digital phase adjuster to fine tune signal timing between clock and data bus

TV-Out Interface

- 12-bit Interface to an external TV encoder for SDTV or HDTV display

LVDS Transmitter Interface

- 12-bit DDR interface with LVDS transmitter

DuoView+™ Capability

- Supports multi-monitor and extended desktop for Windows 98/ME and XP
- Provides two independent display engines, each of which can display completely different information at different resolutions, pixel depths and refresh rates
- Improved display flexibility with simultaneous CRT / DVI, CRT / TV, DVI / TV and other combined operations

Full Software Support

- Microsoft DirectX 7.0, DirectX 8.0 and DirectX 9.0 compatible
- Supports OpenGL™
- Drivers for major operating systems and APIs: Windows® 9x/ME, Windows 2000, Windows XP, Direct3D™, DirectDraw™ and DirectShow™, and OpenGL™ ICD for Windows 9x/ME and XP
- Windows NT 4.0 Standard VGA driver support

- **Advanced Graphics Power Management Support**
  - Built-in reference voltage generator and monitor sense circuits
  - Automatic panel power sequencing and VESA DPMS (Display Power Management Signaling) CRT power-down
  - External I/O signal controlling enabling graphics accelerator into standby / suspend-off state
  - Auto clock gating for each engine to achieve power saving
  - I^2C Serial Bus and DDC Monitor Communications for CRT Plug-and-Play configuration

CN896 System Overview

The CN896 is a high performance, cost-effective and energy efficient UMA North Bridge with integrated Chrome9™ HC graphics / video controller used for the implementation of embedded systems based on VIA C7 processors.

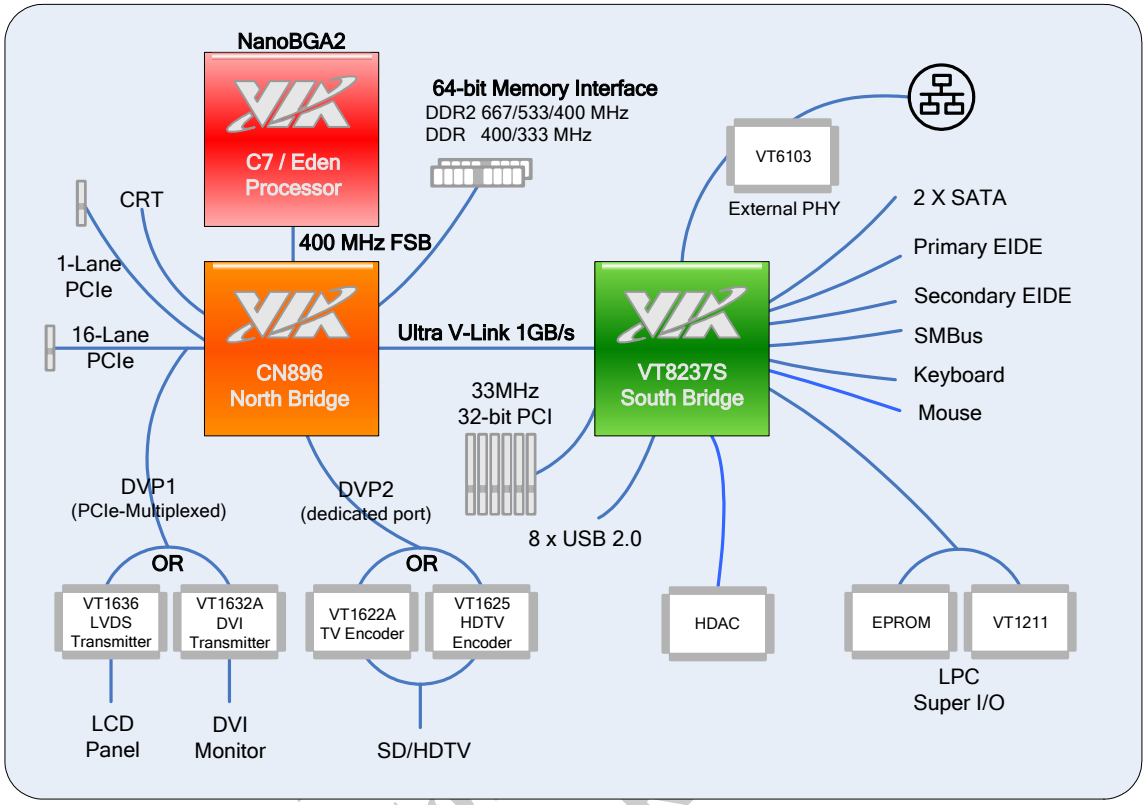


Figure 1. System Block Diagram

The complete embedded chipset consists of the CN896 North Bridge and the VT8237S South Bridge. The CN896 integrates VIA's most advanced system controller with high-performance Chrome9™ HC 3D / 2D graphics and video controller, LCD panel, DVI monitor and TV-Out interfaces. The CN896 provides superior performance between the CPU, PCIe, DRAM, V-Link and internal AGP 8x graphics controller with pipelined, burst and concurrent operation. The VT8237S is a highly integrated peripheral controller which integrates Serial ATA, Ultra DMA IDE, High-Speed USB 2.0, 10/100Mb LAN controller, HDAC and system power management controllers in a single chip.

CN896 Overview

The CN896 supports VIA C7 processors. The CN896 implements a deep In-Order Queue to improve the system performance for multi-threaded software applications. DBI and V4 bus protocol is supported which effectively reduce overall system power consumption.

The CN896 includes a PCI Express 1.1 compliant PCI Express controller, which supports up to two high bandwidth PCIe ports. A 16-Lane port, with up to 4 GB/sec bi-directional data transfer rate, is implemented to support high-end PCI Express compliant graphics controller, and another 1-Lane port designed for PCIe peripheral devices.

The CN896 supports 64-bit memory data bus access and up to 2 double-sided DDR2 667 / 533 / 400 or DDR 400 / 333 SDRAM SODIMM for 4 GB maximum physical memory. The DRAM interface allows zero wait-state data transfer bursting between the DRAM and memory controller's data buffers. The DRAM controller can run either synchronous or pseudo-synchronous with the host CPU bus.

The CN896 North Bridge interfaces to the South Bridge through a high speed (up to 1 GB/sec) 8x 66 MHz Data Transfer interconnect bus called Ultra V-Link interface. Deep pre-fetch and post-write buffers are included to allow for concurrent CPU

and V-Link operation. The combined CN896 North Bridge and VT8237S South Bridge system supports enhanced PCI bus commands such as "Memory-Read-Line", "Memory-Read-Multiple" and "Memory-Write-Invalid" commands to minimize snoop overhead. In addition, advanced features are supported such as CPU write-back forward to PCI master and CPU write-back merged with PCI post-write buffers to minimize PCI master read latency and DRAM utilization. Delay transaction mechanism is also implemented for further improvement of overall system performance.

System Power Management

For sophisticated power management, the CN896 supports dynamic CKE control to minimize DDR SDRAM power consumption during normal system state (S0). A separate suspend power plane is implemented for the memory control logic for Suspend-to-DRAM state. The CN896 graphics controller implements dynamic clock gating for inactive functions to achieve maximum power saving. The system can be switched to standby or suspend states to further reduce power consumption when idle. VESA DPMS (Display Power Management Signaling) CRT power-down is supported. Coupled with the VT823S South Bridge chip, a complete power conscious PC main board can be implemented with no external glue logic.

3D Graphics Engine

Featuring an integrated 128-bit 3D graphics engine, the CN896 North Bridge utilizes a single cycle architecture that provides high performance along with superior image quality. Several new features enhance the 3D architecture, including single-pass multitexturing, anisotropic filtering, and an 8-bit stencil buffer. The chip also offers the industry's only simultaneous usage of single-pass multitexturing and single-cycle trilinear filtering – enabling stunning image quality without performance loss. Image quality is further enhanced with true 32-bit color rendering throughout the 3D pipeline to produce more vivid and realistic images. The advanced triangle setup engine provides realistic user experiences in games and other interactive 3D applications. The 3D engine is optimized for AGP texturing from system memory.

2D Graphics Engine

The CN896 North Bridge's advanced 128-bit 2D graphics engine delivers high-speed 2D acceleration for productivity applications. The enhanced 2D architecture with direct access frame buffer capability optimizes UMA performance and provides acceleration of all color depths.

MPEG Video Playback

The CN896 North Bridge provides the ideal architecture for high quality MPEG-2 based video applications. For MPEG playback, the integrated video accelerator offloads the CPU by performing the motion compensation tasks, while its enhanced scaling algorithm delivers incredible full-screen video playback.

LCD, DVI Monitor and TV Output Display Support

The CN896 provides two "Digital Video Port" interfaces (DVP1 and DVP2). Multiplexing display functions with the PCIe bus allows the system to support an external PCIe connector for future performance upgrades by adding an external graphics controller. It also allows add-in cards to be designed with a PCIe-compatible connector for implementation of the display interface logic to reduce cost in the base configuration. In value-compatible connector configurations, external upgrade capability is not normally required by the system, allowing all the PCIe pins to be used for implementation of flexible display functions.

DVP2 may be configured for support of an external TV encoder (such as the VT1622A and VT1622AM), an external HDTV encoder (such as the VT1625 and VT1625M).

DVP1 implements a 12-bit interface that is designed to drive a Flat Panel Display via an external LVDS transmitter chip (such as the VT1636) or an external DVI transmitter chip (such as VT1632A). A wide variety of LCD panels are supported including VGA, SVGA, XGA, SXGA+ and up to UXGA-resolution TFT color panels in DDR (2 pixels / clock) mode. UXGA and higher resolutions require dual-edge data transfer (DDR) mode, which is supported by the VIA VT1636 LVDS transmitter chip.

The flexible display configurations of the CN896 allow support of a LCD Panel (LVDS interface), or DVI monitor (DVI interface), TV display and CRT display at the same time. Internally the CN896 North Bridge provides two separate display engines, so if two display devices are connected, each can display completely different information at different resolutions, pixel depths and refresh rates. If more than two display devices are connected, the additional displays must have the same resolution, pixel depth and refresh rate as one of the first two. The maximum display resolutions supported for one display device are listed in the table below. If more than one display is implemented (i.e. if both display engines are functioning at the same time), then

available memory bandwidth may limit the display resolutions supported on one or both displays. This will be dependent on many factors including primarily clock rates and memory speeds (contact VIA for additional information).

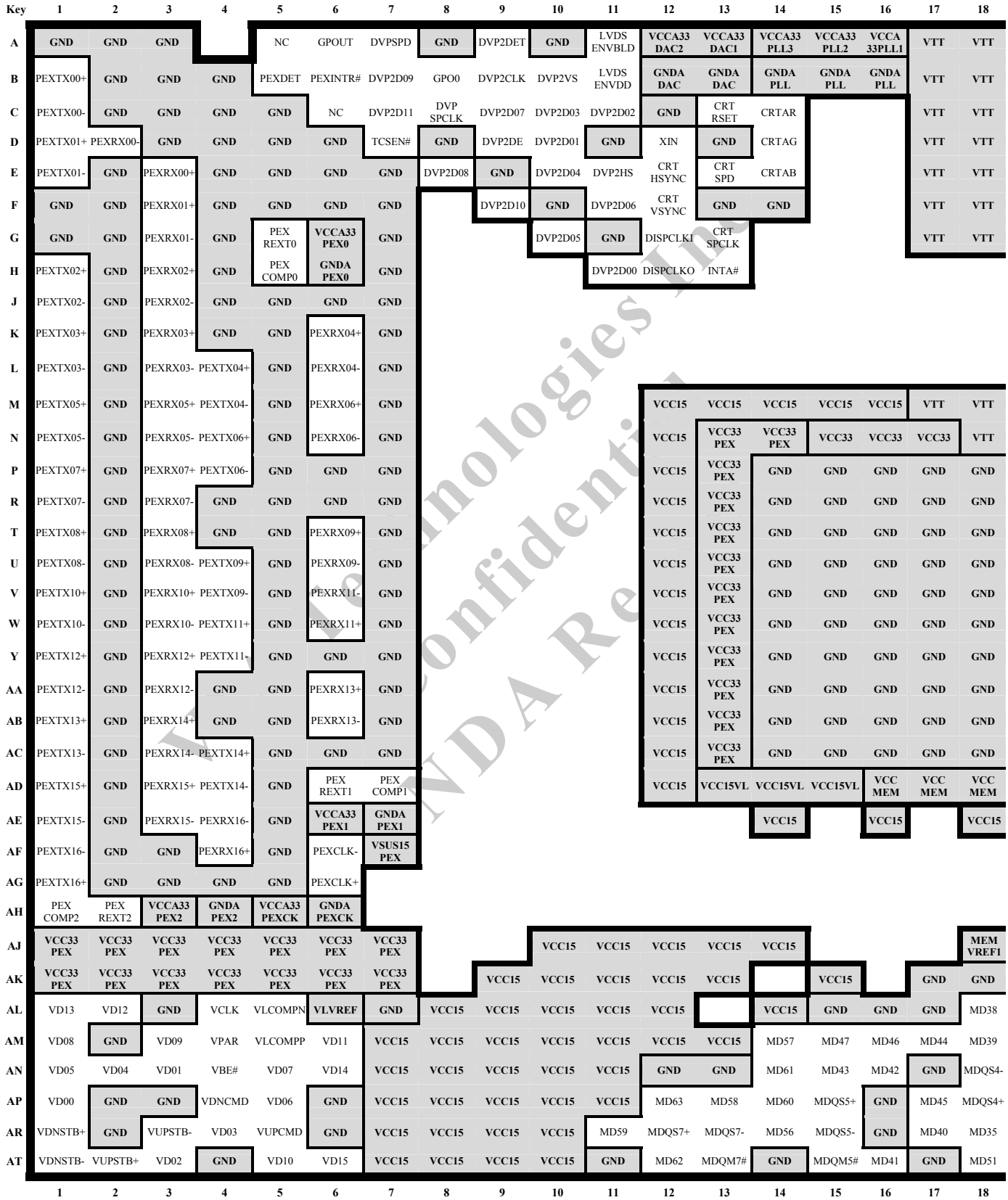
High Screen Resolution Display Support

Resolutions Supported	Resolution Name	Pixel Depths Supported	System Memory Frame Buffer Size		
			64MB	128MB	256MB
640x480 (4:3)	VGA	8 / 16 / 32	✔	✔	✔
800x600 (4:3)	SVGA	8 / 16 / 32	✔	✔	✔
1024x768 (4:3)	XGA	8 / 16 / 32	✔	✔	✔
1280x1024 (5:4)	SXGA	8 / 16 / 32	✔	✔	✔
1400x1050 (4:3)	SXGA+	8 / 16 / 32	✔	✔	✔
1600x1200 (4:3)	UXGA, UXGA+	8 / 16 / 32	✔	✔	✔
1920x1440 (4:3)		8 / 16 / 32	✔	✔	✔

Table 1. Supported CRT Resolutions

BALL DIAGRAM AND BALL LISTS

Figure 2. CN896 Ball Diagram (Top View) – PCI Interface Enabled



Key	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
A	GND	GND	GND		NC	GPOUT	DVPSPD	GND	DVP2DET	GND	LVDS ENVBLD	VCCA33 DAC2	VCCA33 DAC1	VCCA33 PLL3	VCCA33 PLL2	VCCA 33PLL1	VTT	VTT
B	PEXTX00+	GND	GND	GND	PEXDET	PEXINTR#	DVP2D09	GPO0	DVP2CLK	DVP2VS	LVDS ENVDD	GNDA DAC	GNDA DAC	GNDA PLL	GNDA PLL	GNDA PLL	VTT	VTT
C	PEXTX00-	GND	GND	GND	GND	NC	DVP2D11	DVP SPCLK	DVP2D07	DVP2D03	DVP2D02	GND	CRT RSET	CRTAR			VTT	VTT
D	PEXTX01+	PEXRX00-	GND	GND	GND	GND	TCSEN#	GND	DVP2DE	DVP2D01	GND	XIN	GND	CRTAG			VTT	VTT
E	PEXTX01-	GND	PEXRX00+	GND	GND	GND	GND	DVP2D08	GND	DVP2D04	DVP2HS	CRT HSYNC	CRT SPD	CRTAB			VTT	VTT
F	GND	GND	PEXRX01+	GND	GND	GND	GND		DVP2D10	GND	DVP2D06	CRT VSYNC	GND	GND			VTT	VTT
G	GND	GND	PEXRX01-	GND	PEX REXT0	VCCA33 PEX0	GND			DVP2D05	GND	DISPCLKI	CRT SPCLK				VTT	VTT
H	PEXTX02+	GND	PEXRX02+	GND	PEX COMP0	GNDA PEX0	GND				DVP2D00	DISPCLKO	INTA#					
J	PEXTX02-	GND	PEXRX02-	GND	GND	GND	GND											
K	PEXTX03+	GND	PEXRX03+	GND	GND	PEXRX04+	GND											
L	PEXTX03-	GND	PEXRX03-	PEXTX04+	GND	PEXRX04-	GND											
M	PEXTX05+	GND	PEXRX05+	PEXTX04-	GND	PEXRX06+	GND					VCC15	VCC15	VCC15	VCC15	VCC15	VTT	VTT
N	PEXTX05-	GND	PEXRX05-	PEXTX06+	GND	PEXRX06-	GND					VCC15	VCC33 PEX	VCC33 PEX	VCC33	VCC33	VCC33	VTT
P	PEXTX07+	GND	PEXRX07+	PEXTX06-	GND	GND	GND					VCC15	VCC33 PEX	GND	GND	GND	GND	GND
R	PEXTX07-	GND	PEXRX07-	GND	GND	GND	GND					VCC15	VCC33 PEX	GND	GND	GND	GND	GND
T	PEXTX08+	GND	PEXRX08+	GND	GND	PEXRX09+	GND					VCC15	VCC33 PEX	GND	GND	GND	GND	GND
U	PEXTX08-	GND	PEXRX08-	PEXTX09+	GND	PEXRX09-	GND					VCC15	VCC33 PEX	GND	GND	GND	GND	GND
V	PEXTX10+	GND	PEXRX10+	PEXTX09-	GND	PEXRX11-	GND					VCC15	VCC33 PEX	GND	GND	GND	GND	GND
W	PEXTX10-	GND	PEXRX10-	PEXTX11+	GND	PEXRX11+	GND					VCC15	VCC33 PEX	GND	GND	GND	GND	GND
Y	PEXTX12+	GND	PEXRX12+	PEXTX11-	GND	GND	GND					VCC15	VCC33 PEX	GND	GND	GND	GND	GND
AA	PEXTX12-	GND	PEXRX12-	GND	GND	PEXRX13+	GND					VCC15	VCC33 PEX	GND	GND	GND	GND	GND
AB	PEXTX13+	GND	PEXRX14+	GND	GND	PEXRX13-	GND					VCC15	VCC33 PEX	GND	GND	GND	GND	GND
AC	PEXTX13-	GND	PEXRX14-	PEXTX14+	GND	GND	GND					VCC15	VCC33 PEX	GND	GND	GND	GND	GND
AD	PEXTX15+	GND	PEXRX15+	PEXTX14-	GND	PEX REXT1	PEX COMP1					VCC15	VCC15VL	VCC15VL	VCC15VL	VCC MEM	VCC MEM	VCC MEM
AE	PEXTX15-	GND	PEXRX15-	PEXRX16-	GND	VCCA33 PEX1	GNDA PEX1							VCC15		VCC15		VCC15
AF	PEXTX16-	GND	GND	PEXRX16+	GND	PEXCLK-	VSUS15 PEX											
AG	PEXTX16+	GND	GND	GND	GND	PEXCLK+												
AH	PEX COMP2	PEX REXT2	VCCA33 PEX2	GNDA PEX2	VCCA33 PEXCK	GNDA PEXCK												
AJ	VCC33 PEX	VCC33 PEX	VCC33 PEX	VCC33 PEX	VCC33 PEX	VCC33 PEX	VCC33 PEX			VCC15	VCC15	VCC15	VCC15	VCC15				MEM VREF1
AK	VCC33 PEX	VCC33 PEX	VCC33 PEX	VCC33 PEX	VCC33 PEX	VCC33 PEX	VCC33 PEX		VCC15	VCC15	VCC15	VCC15	VCC15		VCC15		GND	GND
AL	VD13	VD12	GND	VCLK	VLCOMPN	VLVREF	GND	VCC15	VCC15	VCC15	VCC15	VCC15		VCC15	GND	GND	GND	MD38
AM	VD08	GND	VD09	VPAR	VLCOMPP	VD11	VCC15	VCC15	VCC15	VCC15	VCC15	VCC15	VCC15	MD57	MD47	MD46	MD44	MD39
AN	VD05	VD04	VD01	VBE#	VD07	VD14	VCC15	VCC15	VCC15	VCC15	VCC15	GND	GND	MD61	MD43	MD42	GND	MDQS4-
AP	VD00	GND	GND	VDNCMD	VD06	GND	VCC15	VCC15	VCC15	VCC15	VCC15	MD63	MD58	MD60	MDQS5+	GND	MD45	MDQS4+
AR	VDNSTB+	GND	VUPSTB-	VD03	VUPCMD	GND	VCC15	VCC15	VCC15	VCC15	MD59	MDQS7+	MDQS7-	MD56	MDQS5-	GND	MD40	MD35
AT	VDNSTB-	VUPSTB+	VD02	GND	VD10	VD15	VCC15	VCC15	VCC15	VCC15	GND	MD62	MDQM7#	GND	MDQM5#	MD41	GND	MD51
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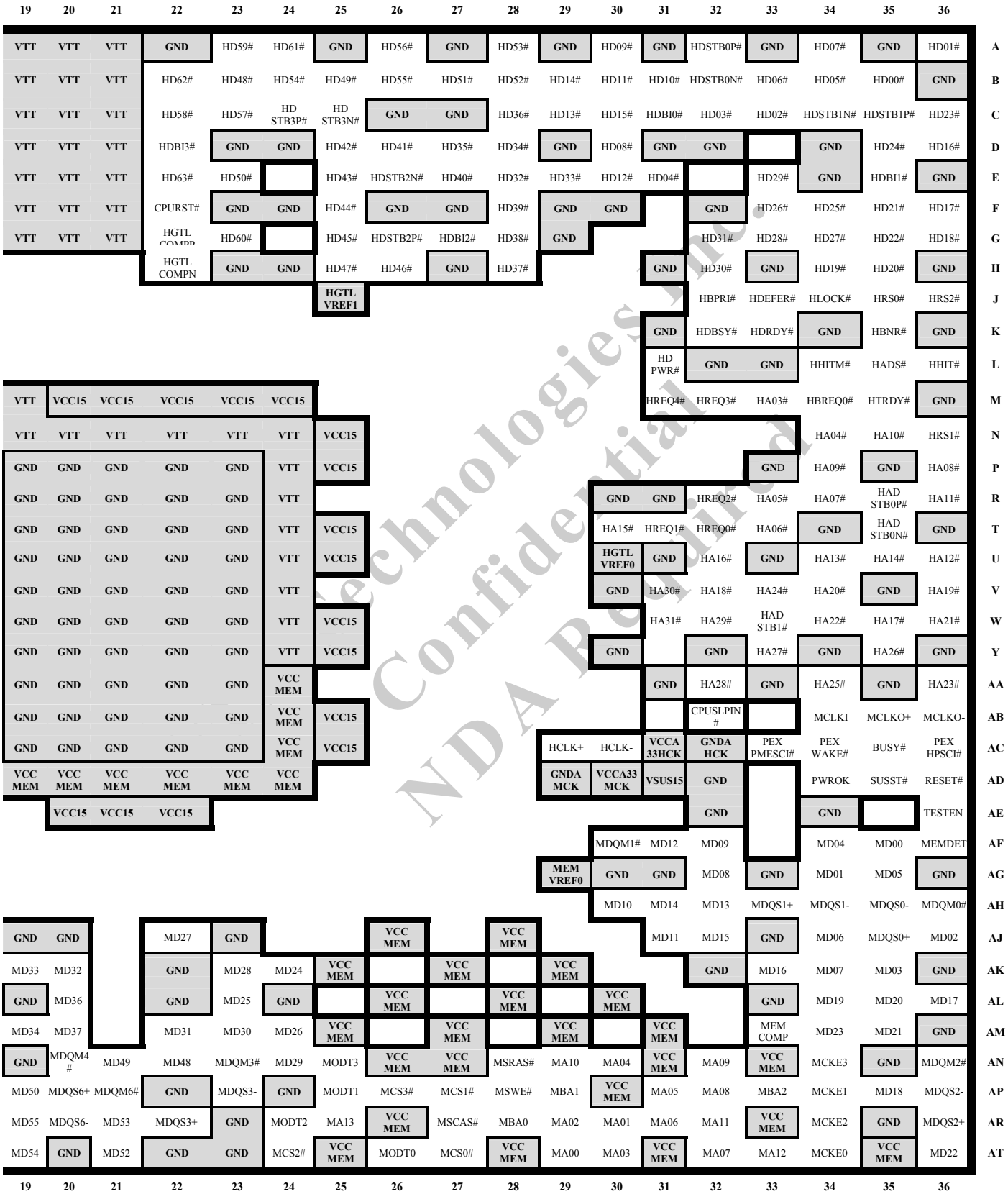

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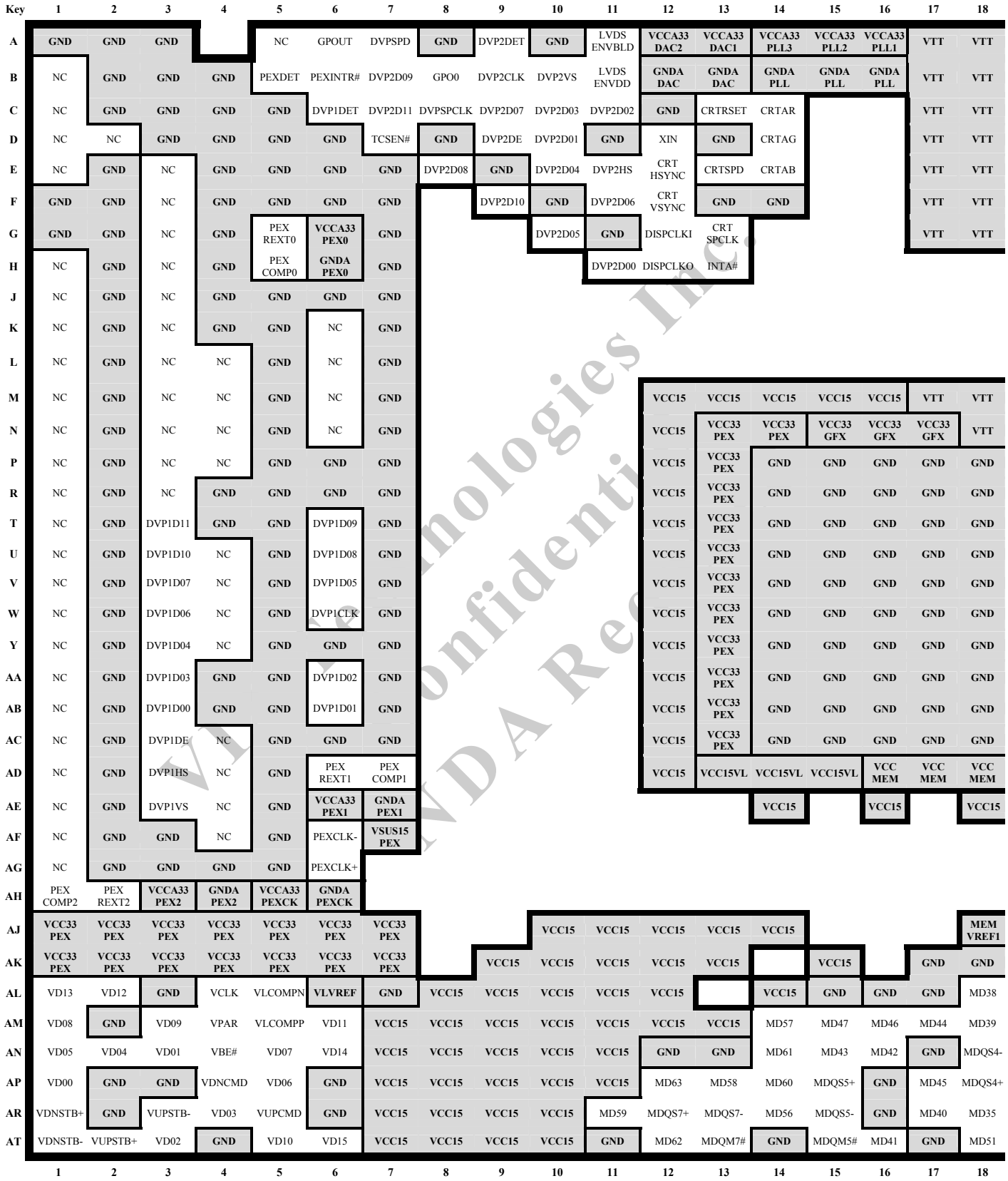
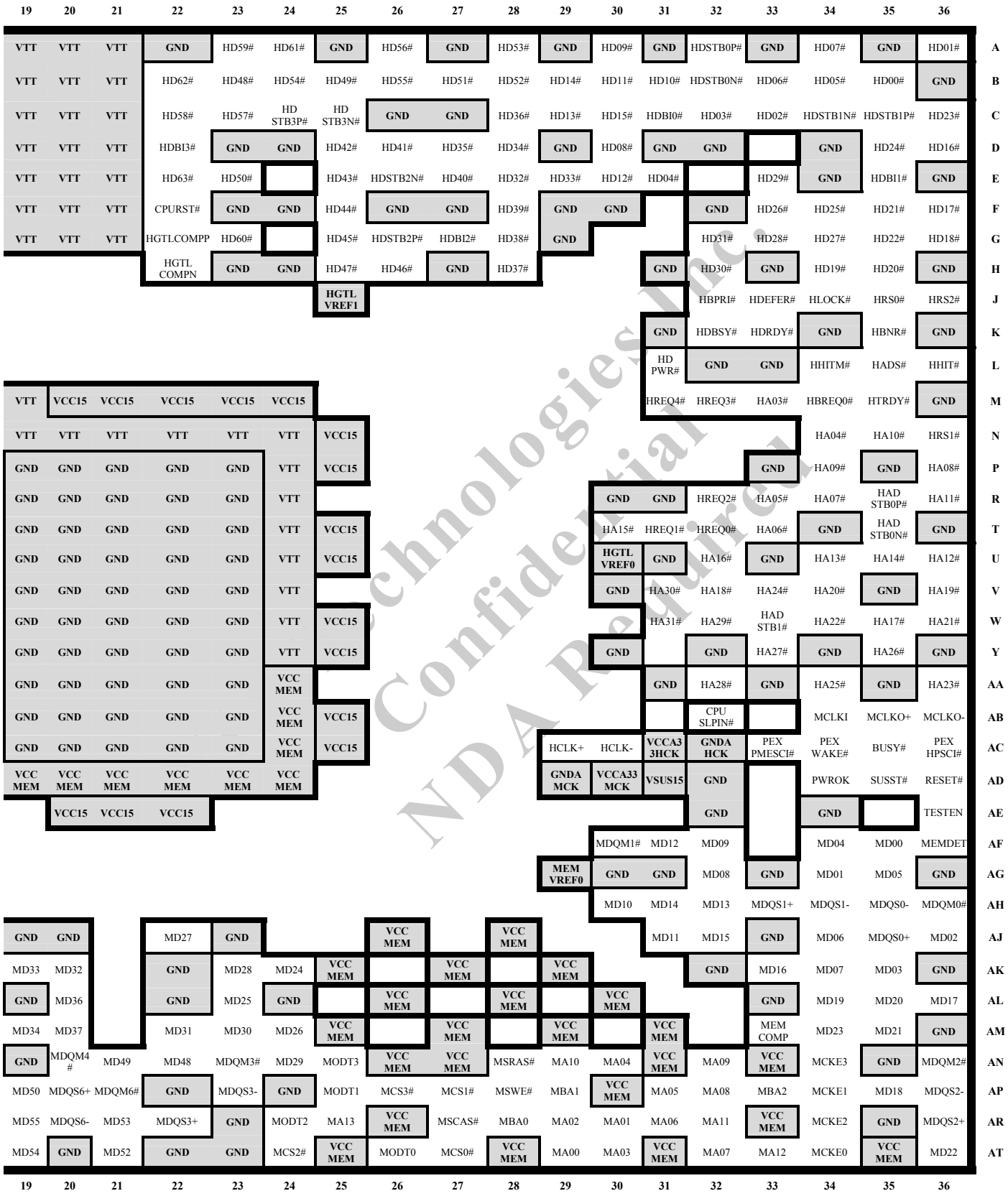
VTT	VTT	VTT	GND	HD59#	HD61#	GND	HD56#	GND	HD53#	GND	HD09#	GND	HDSTB0P#	GND	HD07#	GND	HD01#	A
VTT	VTT	VTT	HD62#	HD48#	HD54#	HD49#	HD55#	HD51#	HD52#	HD14#	HD11#	HD10#	HDSTB0N#	HD06#	HD05#	HD00#	GND	B
VTT	VTT	VTT	HD58#	HD57#	HD STB3P#	HD STB3N#	GND	GND	HD36#	HD13#	HD15#	HDBI0#	HD03#	HD02#	HDSTB1N#	HDSTB1P#	HD23#	C
VTT	VTT	VTT	HDBI3#	GND	GND	HD42#	HD41#	HD35#	HD34#	GND	HD08#	GND	GND		GND	HD24#	HD16#	D
VTT	VTT	VTT	HD63#	HD50#		HD43#	HDSTB2N#	HD40#	HD32#	HD33#	HD12#	HD04#		HD29#	GND	HDBI1#	GND	E
VTT	VTT	VTT	CPURST#	GND	GND	HD44#	GND	GND	HD39#	GND	GND		GND	HD26#	HD25#	HD21#	HD17#	F
VTT	VTT	VTT	HGTL COMPP	HD60#		HD45#	HDSTB2P#	HDBI2#	HD38#	GND			HD31#	HD28#	HD27#	HD22#	HD18#	G
			HGTL COMPN	GND	GND	HD47#	HD46#	GND	HD37#			GND	HD30#	GND	HD19#	HD20#	GND	H
						HGTL VREF1							HBPRI#	HDEFER#	HLOCK#	HRS0#	HRS2#	J
												GND	HDBSY#	HDRDY#	GND	HBNR#	GND	K
												HD PWR#	GND	GND	HHITM#	HADS#	HHIT#	L
VTT	VCC15	VCC15	VCC15	VCC15	VCC15							HREQ4#	HREQ3#	HA03#	HBREQ0#	HTRDY#	GND	M
VTT	VTT	VTT	VTT	VTT	VTT	VCC15									HA04#	HA10#	HRS1#	N
GND	GND	GND	GND	GND	VTT	VCC15								GND	HA09#	GND	HA08#	P
GND	GND	GND	GND	GND	VTT						GND	GND	HREQ2#	HA05#	HA07#	HAD STB0P#	HA11#	R
GND	GND	GND	GND	GND	VTT	VCC15					HA15#	HREQ1#	HREQ0#	HA06#	GND	HAD STB0N#	GND	T
GND	GND	GND	GND	GND	VTT	VCC15					HGTL VREF0	GND	HA16#	GND	HA13#	HA14#	HA12#	U
GND	GND	GND	GND	GND	VTT						GND	HA30#	HA18#	HA24#	HA20#	GND	HA19#	V
GND	GND	GND	GND	GND	VTT	VCC15						HA31#	HA29#	HAD STB1#	HA22#	HA17#	HA21#	W
GND	GND	GND	GND	GND	VTT	VCC15					GND		GND	HA27#	GND	HA26#	GND	Y
GND	GND	GND	GND	GND	VCC MEM							GND	HA28#	GND	HA25#	GND	HA23#	AA
GND	GND	GND	GND	GND	VCC MEM	VCC15							CPUSLPIN#		MCLKI	MCLKO+	MCLKO-	AB
GND	GND	GND	GND	GND	VCC MEM	VCC15					HCLK+	HCLK-	VCCA 33HCK	GNDA HCK	PEX PMESCI#	PEX WAKE#	BUSY#	PEX HPSCI#	AC
VCC MEM	VCC MEM	VCC MEM	VCC MEM	VCC MEM	VCC MEM						GNDA MCK	VCCA33 MCK	VSUS15	GND		PWROK	SUSST#	RESET#	AD
	VCC15	VCC15	VCC15											GND		GND		TESTEN	AE
												MDQM1#	MD12	MD09		MD04	MD00	MEMDET	AF
										MEM VREF0		GND	GND	MD08	GND	MD01	MD05	GND	AG
												MD10	MD14	MD13	MDQS1+	MDQS1-	MDQS0-	MDQM0#	AH
GND	GND		MD27	GND		VCC MEM		VCC MEM					MD11	MD15	GND	MD06	MDQS0+	MD02	AJ
MD33	MD32		GND	MD28	MD24	VCC MEM		VCC MEM		VCC MEM				GND	MD16	MD07	MD03	GND	AK
GND	MD36		GND	MD25	GND		VCC MEM		VCC MEM		VCC MEM				GND	MD19	MD20	MD17	AL
MD34	MD37		MD31	MD30	MD26	VCC MEM		VCC MEM		VCC MEM		VCC MEM			MEM COMP	MD23	MD21	GND	AM
GND	MDQM4#	MD49	MD48	MDQM3#	MD29	MODT3	VCC MEM	VCC MEM	MSRAS#	MA10	MA04	VCC MEM	MA09	VCC MEM	MCKE3	GND	MDQM2#	AN
MD50	MDQS6+	MDQM6#	GND	MDQS3-	GND	MODT1	MCS3#	MCS1#	MSWE#	MBA1	VCC MEM	MA05	MA08	MBA2	MCKE1	MD18	MDQS2-	AP
MD55	MDQS6-	MD53	MDQS3+	GND	MODT2	MA13	VCC MEM	MSCAS#	MBA0	MA02	MA01	MA06	MA11	VCC MEM	MCKE2	GND	MDQS2+	AR
MD54	GND	MD52	GND	GND	MCS2#	VCC MEM	MODT0	MCS0#	VCC MEM	MA00	MA03	VCC MEM	MA07	MA12	MCKE0	VCC MEM	MD22	AT
19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	

Figure 3. CN896 Ball Diagram (Top View) – Display Function Enabled on PCI Express Interface



Key	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
A	GND	GND	GND		NC	GPOUT	DVPSPD	GND	DVP2DET	GND	LVDS ENVBLD	VCCA33 DAC2	VCCA33 DAC1	VCCA33 PLL3	VCCA33 PLL2	VCCA33 PLL1	VTT	VTT
B	NC	GND	GND	GND	PEXDET	PEXINTR#	DVP2D09	GPO0	DVP2CLK	DVP2VS	LVDS ENVDD	GNDA DAC	GNDA DAC	GNDA PLL	GNDA PLL	GNDA PLL	VTT	VTT
C	NC	GND	GND	GND	GND	DVP1DET	DVP2D11	DVPSPCLK	DVP2D07	DVP2D03	DVP2D02	GND	CRTRSET	CRTAR			VTT	VTT
D	NC	NC	GND	GND	GND	GND	TCSEN#	GND	DVP2DE	DVP2D01	GND	XIN	GND	CRTAG			VTT	VTT
E	NC	GND	NC	GND	GND	GND	GND	DVP2D08	GND	DVP2D04	DVP2HS	CRT HSYNC	CRTSPD	CRTAB			VTT	VTT
F	GND	GND	NC	GND	GND	GND	GND		DVP2D10	GND	DVP2D06	CRT VSYNC	GND	GND			VTT	VTT
G	GND	GND	NC	GND	PEX REXT0	VCCA33 PEX0	GND			DVP2D05	GND	DISPCLKI	CRT SPCLK				VTT	VTT
H	NC	GND	NC	GND	PEX COMP0	GNDA PEX0	GND				DVP2D00	DISPCLKO	INTA#					
J	NC	GND	NC	GND	GND	GND	GND											
K	NC	GND	NC	GND	GND	NC	GND											
L	NC	GND	NC	NC	GND	NC	GND											
M	NC	GND	NC	NC	GND	NC	GND					VCC15	VCC15	VCC15	VCC15	VCC15	VTT	VTT
N	NC	GND	NC	NC	GND	NC	GND					VCC15	VCC33 PEX	VCC33 PEX	VCC33 GFX	VCC33 GFX	VCC33 GFX	VTT
P	NC	GND	NC	NC	GND	GND	GND					VCC15	VCC33 PEX	GND	GND	GND	GND	GND
R	NC	GND	NC	GND	GND	GND	GND					VCC15	VCC33 PEX	GND	GND	GND	GND	GND
T	NC	GND	DVP1D11	GND	GND	DVP1D09	GND					VCC15	VCC33 PEX	GND	GND	GND	GND	GND
U	NC	GND	DVP1D10	NC	GND	DVP1D08	GND					VCC15	VCC33 PEX	GND	GND	GND	GND	GND
V	NC	GND	DVP1D07	NC	GND	DVP1D05	GND					VCC15	VCC33 PEX	GND	GND	GND	GND	GND
W	NC	GND	DVP1D06	NC	GND	DVP1CLK	GND					VCC15	VCC33 PEX	GND	GND	GND	GND	GND
Y	NC	GND	DVP1D04	NC	GND	GND	GND					VCC15	VCC33 PEX	GND	GND	GND	GND	GND
AA	NC	GND	DVP1D03	GND	GND	DVP1D02	GND					VCC15	VCC33 PEX	GND	GND	GND	GND	GND
AB	NC	GND	DVP1D00	GND	GND	DVP1D01	GND					VCC15	VCC33 PEX	GND	GND	GND	GND	GND
AC	NC	GND	DVP1DE	NC	GND	GND	GND					VCC15	VCC33 PEX	GND	GND	GND	GND	GND
AD	NC	GND	DVP1HS	NC	GND	PEX REXT1	PEX COMP1					VCC15	VCC15VL	VCC15VL	VCC15VL	VCC MEM	VCC MEM	VCC MEM
AE	NC	GND	DVP1VS	NC	GND	VCCA33 PEX1	GNDA PEX1							VCC15		VCC15		VCC15
AF	NC	GND	GND	NC	GND	PEXCLK-	VSUS15 PEX											
AG	NC	GND	GND	GND	GND	PEXCLK+												
AH	PEX COMP2	PEX REXT2	VCCA33 PEX2	GNDA PEX2	VCCA33 PEXCK	GNDA PEXCK												
AJ	VCC33 PEX	VCC33 PEX	VCC33 PEX	VCC33 PEX	VCC33 PEX	VCC33 PEX	VCC33 PEX			VCC15	VCC15	VCC15	VCC15	VCC15				MEM VREF1
AK	VCC33 PEX	VCC33 PEX	VCC33 PEX	VCC33 PEX	VCC33 PEX	VCC33 PEX	VCC33 PEX		VCC15	VCC15	VCC15	VCC15	VCC15		VCC15		GND	GND
AL	VD13	VD12	GND	VCLK	VLCOMPN	VLVREF	GND	VCC15	VCC15	VCC15	VCC15	VCC15		VCC15	GND	GND	GND	MD38
AM	VD08	GND	VD09	VPAR	VLCOMPP	VD11	VCC15	VCC15	VCC15	VCC15	VCC15	VCC15	VCC15	MD57	MD47	MD46	MD44	MD39
AN	VD05	VD04	VD01	VBE#	VD07	VD14	VCC15	VCC15	VCC15	VCC15	VCC15	GND	GND	MD61	MD43	MD42	GND	MDQS4-
AP	VD00	GND	GND	VDNCMD	VD06	GND	VCC15	VCC15	VCC15	VCC15	VCC15	MD63	MD58	MD60	MDQS5+	GND	MD45	MDQS4+
AR	VDNSTB+	GND	VUPSTB-	VD03	VUPCMD	GND	VCC15	VCC15	VCC15	VCC15	MD59	MDQS7+	MDQS7-	MD56	MDQS5-	GND	MD40	MD35
AT	VDNSTB-	VUPSTB+	VD02	GND	VD10	VD15	VCC15	VCC15	VCC15	VCC15	GND	MD62	MDQM7#	GND	MDQM5#	MD41	GND	MD51
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18



19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	
VTT	VTT	VTT	GND	HD59#	HD61#	GND	HD56#	GND	HD53#	GND	HD09#	GND	HDSTB0P#	GND	HD07#	GND	HD01#	A
VTT	VTT	VTT	HD62#	HD48#	HD54#	HD49#	HD55#	HD51#	HD52#	HD14#	HD11#	HD10#	HDSTB0N#	HD06#	HD05#	HD00#	GND	B
VTT	VTT	VTT	HD58#	HD57#	HD STB3P#	HD STB3N#	GND	GND	HD36#	HD13#	HD15#	HDBI0#	HD03#	HD02#	HDSTB1N#	HDSTB1P#	HD23#	C
VTT	VTT	VTT	HDBI3#	GND	GND	HD42#	HD41#	HD35#	HD34#	GND	HD08#	GND	GND		GND	HD24#	HD16#	D
VTT	VTT	VTT	HD63#	HD50#		HD43#	HDSTB2N#	HD40#	HD32#	HD33#	HD12#	HD04#		HD29#	GND	HDBI1#	GND	E
VTT	VTT	VTT	CPURST#	GND	GND	HD44#	GND	GND	HD39#	GND	GND		GND	HD26#	HD25#	HD21#	HD17#	F
VTT	VTT	VTT	HGTLCOMPP	HD60#		HD45#	HDSTB2P#	HDBI2#	HD38#	GND			HD31#	HD28#	HD27#	HD22#	HD18#	G
			HGTL COMPN	GND	GND	HD47#	HD46#	GND	HD37#			GND	HD30#	GND	HD19#	HD20#	GND	H
						HGTL VREF1							HBPRI#	HDEFER#	HLOCK#	HRS0#	HRS2#	J
												GND	HDBSY#	HDRDY#	GND	HBNR#	GND	K
												HD PWR#	GND	GND	HHITM#	HADS#	HHIT#	L
VTT	VCC15	VCC15	VCC15	VCC15	VCC15							HREQ4#	HREQ3#	HA03#	HBREQ0#	HTRDY#	GND	M
VTT	VTT	VTT	VTT	VTT	VTT	VCC15									HA04#	HA10#	HRS1#	N
GND	GND	GND	GND	GND	VTT	VCC15								GND	HA09#	GND	HA08#	P
GND	GND	GND	GND	GND	VTT							GND	GND	HREQ2#	HA05#	HA07#	HAD STB0P#	HA11#	R
GND	GND	GND	GND	GND	VTT	VCC15						HA15#	HREQ1#	HREQ0#	HA06#	GND	HAD STB0N#	GND	T
GND	GND	GND	GND	GND	VTT	VCC15						HGTL VREF0	GND	HA16#	GND	HA13#	HA14#	HA12#	U
GND	GND	GND	GND	GND	VTT							GND	HA30#	HA18#	HA24#	HA20#	GND	HA19#	V
GND	GND	GND	GND	GND	VTT	VCC15							HA31#	HA29#	HAD STB1#	HA22#	HA17#	HA21#	W
GND	GND	GND	GND	GND	VTT	VCC15						GND		GND	HA27#	GND	HA26#	GND	Y
GND	GND	GND	GND	GND	VCC MEM								GND	HA28#	GND	HA25#	GND	HA23#	AA
GND	GND	GND	GND	GND	VCC MEM	VCC15								CPU SLPIN#		MCLKI	MCLKO+	MCLKO-	AB
GND	GND	GND	GND	GND	VCC MEM	VCC15						HCLK+	HCLK-	VCCA3 3HCK	GNDA HCK	PEX PMESCI#	PEX WAKE#	BUSY#	PEX HPSCI#	AC
VCC MEM	VCC MEM	VCC MEM	VCC MEM	VCC MEM	VCC MEM							GNDA MCK	VCCA33 MCK	VSUS15	GND		PWROK	SUSST#	RESET#	AD
	VCC15	VCC15	VCC15											GND		GND		TESTEN	AE
											MDQM1#	MD12	MD09			MD04	MD00	MEMDET	AF
										MEM VREF0	GND	GND	MD08	GND	MD01	MD05	GND	AG
											MD10	MD14	MD13	MDQS1+	MDQS1-	MDQS0-	MDQM0#	AH
GND	GND		MD27	GND			VCC MEM		VCC MEM			MD11	MD15	GND	MD06	MDQS0+	MD02	AJ
MD33	MD32		GND	MD28	MD24	VCC MEM		VCC MEM		VCC MEM			GND	MD16	MD07	MD03	GND	AK
GND	MD36		GND	MD25	GND		VCC MEM		VCC MEM		VCC MEM			GND	MD19	MD20	MD17	AL
MD34	MD37		MD31	MD30	MD26	VCC MEM		VCC MEM		VCC MEM		VCC MEM		MEM COMP	MD23	MD21	GND	AM
GND	MDQM4 #	MD49	MD48	MDQM3#	MD29	MODT3	VCC MEM	VCC MEM	MSRAS#	MA10	MA04	VCC MEM	MA09	VCC MEM	MCKE3	GND	MDQM2#	AN
MD50	MDQS6+	MDQM6#	GND	MDQS3-	GND	MODT1	MCS3#	MCS1#	MSWE#	MBA1	VCC MEM	MA05	MA08	MBA2	MCKE1	MD18	MDQS2-	AP
MD55	MDQS6-	MD53	MDQS3+	GND	MODT2	MA13	VCC MEM	MSCAS#	MBA0	MA02	MA01	MA06	MA11	VCC MEM	MCKE2	GND	MDQS2+	AR
MD54	GND	MD52	GND	GND	MCS2#	VCC MEM	MODT0	MCS0#	VCC MEM	MA00	MA03	VCC MEM	MA07	MA12	MCKE0	VCC MEM	MD22	AT
19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	

Signal Ball List

Table 2. Ball List (Listed by Ball Name) - PCI Express Interface Enabled

Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name
AC35	BUSY#	W32	HA29#	B23	HD48#	AN32	MA09	AT16	MD41	AF06	PEXCLK-	R01	PEXTX07-
F22	CPURST#	V31	HA30#	B25	HD49#	AN29	MA10	AN16	MD42	AG06	PEXCLK+	P01	PEXTX07+
AB32	CPUSLPIN#	W31	HA31#	E23	HD50#	AR32	MA11	AN15	MD43	H05	PEXCOMP0	U01	PEXTX08-
E14	CRTAB	L35	HADS#	B27	HD51#	AT33	MA12	AM17	MD44	AD07	PEXCOMP1	T01	PEXTX08+
D14	CRTAG	T35	HADSTB0N#	B28	HD52#	AR25	MA13	AP17	MD45	AH01	PEXCOMP2	V04	PEXTX09-
C14	CRTAR	R35	HADSTB0P#	A28	HD53#	AR28	MBA0	AM16	MD46	B05	PEXDET	U04	PEXTX09+
E12	CRTHSYNC	W33	HADSTB1#	B24	HD54#	AP29	MBA1	AM15	MD47	AC36	PEXHPSCI#	W01	PEXTX10-
C13	CRTRSET	K35	HBNR#	B26	HD55#	AP33	MBA2	AN22	MD48	B06	PEXINTR#	V01	PEXTX10+
G13	CRTSPCLK	J32	HBPRI#	A26	HD56#	AT34	MCKE0	AN21	MD49	AC33	PEXPMESCI#	Y04	PEXTX11-
E13	CRTSPD	M34	HBREQ0#	C23	HD57#	AP34	MCKE1	AP19	MD50	G05	PEXREXT0	W04	PEXTX11+
F12	CRTVSYNC	AC30	HCLK-	C22	HD58#	AR34	MCKE2	AT18	MD51	AD06	PEXREXT1	AA01	PEXTX12-
G12	DISPCLKI	AC29	HCLK+	A23	HD59#	AN34	MCKE3	AT21	MD52	AH02	PEXREXT2	Y01	PEXTX12+
H12	DISPCLKO	B35	HD00#	G23	HD60#	AB34	MCLKI	AR21	MD53	D02	PEXRX00-	AC01	PEXTX13-
B09	DVP2CLK	A36	HD01#	A24	HD61#	AB36	MCLKO-	AT19	MD54	E03	PEXRX00+	AB01	PEXTX13+
H11	DVP2D00	C33	HD02#	B22	HD62#	AB35	MCLKO+	AR19	MD55	G03	PEXRX01-	AD04	PEXTX14-
D10	DVP2D01	C32	HD03#	E22	HD63#	AT27	MCS0#	AR14	MD56	F03	PEXRX01+	AC04	PEXTX14+
C11	DVP2D02	E31	HD04#	C31	HDBI0#	AP27	MCS1#	AM14	MD57	J03	PEXRX02-	AE01	PEXTX15-
C10	DVP2D03	B34	HD05#	E35	HDBI1#	AT24	MCS2#	AP13	MD58	H03	PEXRX02+	AD01	PEXTX15+
E10	DVP2D04	B33	HD06#	G27	HDBI2#	AP26	MCS3#	AR11	MD59	L03	PEXRX03-	AF01	PEXTX16-
G10	DVP2D05	A34	HD07#	D22	HDBI3#	AF35	MD00	AP14	MD60	K03	PEXRX03+	AG01	PEXTX16+
F11	DVP2D06	D30	HD08#	K32	HDBSY#	AG34	MD01	AN14	MD61	L06	PEXRX04-	AC34	PEXWAKE#
C09	DVP2D07	A30	HD09#	J33	HDEFER#	AJ36	MD02	AT12	MD62	K06	PEXRX04+	AD34	PWROK
E08	DVP2D08	B31	HD10#	L31	HDPWR#	AK35	MD03	AP12	MD63	N03	PEXRX05-	AD36	RESET#
B07	DVP2D09	B30	HD11#	K33	HDRDY#	AF34	MD04	AH36	MDQM0#	M03	PEXRX05+	AD35	SUSST#
F09	DVP2D10	E30	HD12#	B32	HDSTB0N#	AG35	MD05	AF30	MDQM1#	N06	PEXRX06-	D07	TCSEN#
C07	DVP2D11	C29	HD13#	A32	HDSTB0P#	AJ34	MD06	AN36	MDQM2#	M06	PEXRX06+	AE36	TESTEN
D09	DVP2DE	B29	HD14#	C34	HDSTB1N#	AK34	MD07	AN23	MDQM3#	R03	PEXRX07-	AN04	VBE#
A09	DVP2DET	C30	HD15#	C35	HDSTB1P#	AG32	MD08	AN20	MDQM4#	P03	PEXRX07+	AL04	VCLK
E11	DVP2HS	D36	HD16#	E26	HDSTB2N#	AF32	MD09	AT15	MDQM5#	U03	PEXRX08-	AP01	VD00
B10	DVP2VS	F36	HD17#	G26	HDSTB2P#	AH30	MD10	AP21	MDQM6#	T03	PEXRX08+	AN03	VD01
C08	DVPSPCLK	G36	HD18#	C25	HDSTB3N#	AJ31	MD11	AT13	MDQM7#	U06	PEXRX09-	AT03	VD02
A07	DVPSPD	H34	HD19#	C24	HDSTB3P#	AF31	MD12	AH35	MDQS0-	T06	PEXRX09+	AR04	VD03
B08	GPO0	H35	HD20#	H22	HGTLCOMPN	AH32	MD13	AJ35	MDQS0+	W03	PEXRX10-	AN02	VD04
A06	GPOUT	F35	HD21#	G22	HGTLCOMPP	AH31	MD14	AH34	MDQS1-	V03	PEXRX10+	AN01	VD05
M33	HA03#	G35	HD22#	U30	HGTLVREF0	AJ32	MD15	AH33	MDQS1+	V06	PEXRX11-	AP05	VD06
N34	HA04#	C36	HD23#	J25	HGTLVREF1	AK33	MD16	AP36	MDQS2-	W06	PEXRX11+	AN05	VD07
R33	HA05#	D35	HD24#	L36	HHIT#	AL36	MD17	AR36	MDQS2+	AA03	PEXRX12-	AM01	VD08
T33	HA06#	F34	HD25#	L34	HHITM#	AP35	MD18	AP23	MDQS3-	Y03	PEXRX12+	AM03	VD09
R34	HA07#	F33	HD26#	J34	HLOCK#	AL34	MD19	AR22	MDQS3+	AB06	PEXRX13-	AT05	VD10
P36	HA08#	G34	HD27#	T32	HREQ0#	AL35	MD20	AN18	MDQS4-	AA06	PEXRX13+	AM06	VD11
P34	HA09#	G33	HD28#	T31	HREQ1#	AM35	MD21	AP18	MDQS4+	AC03	PEXRX14-	AL02	VD12
N35	HA10#	E33	HD29#	R32	HREQ2#	AT36	MD22	AR15	MDQS5-	AB03	PEXRX14+	AL01	VD13
R36	HA11#	H32	HD30#	M32	HREQ3#	AM34	MD23	AP15	MDQS5+	AE03	PEXRX15-	AN06	VD14
U36	HA12#	G32	HD31#	M31	HREQ4#	AK24	MD24	AR20	MDQS6-	AD03	PEXRX15+	AT06	VD15
U34	HA13#	E28	HD32#	J35	HRS0#	AL23	MD25	AP20	MDQS6+	AE04	PEXRX16-	AP04	VDNCMD
U35	HA14#	E29	HD33#	N36	HRS1#	AM24	MD26	AR13	MDQS7-	AF04	PEXRX16+	AT01	VDNSTB-
T30	HA15#	D28	HD34#	J36	HRS2#	AJ22	MD27	AR12	MDQS7+	C01	PEXTX00-	AR01	VDNSTB+
U32	HA16#	D27	HD35#	M35	HTRDY#	AK23	MD28	AM33	MEMCOMP	B01	PEXTX00+	AL05	VLCOMPN
W35	HA17#	C28	HD36#	H13	INTA#	AN24	MD29	AF36	MEMDET	E01	PEXTX01-	AM05	VLCOMPP
V32	HA18#	H28	HD37#	A11	LVDSENVBLD	AM23	MD30	AG29	MEMVREF0	D01	PEXTX01+	AL06	VLVREF
V36	HA19#	G28	HD38#	B11	LVDSENVDD	AM22	MD31	AJ18	MEMVREF1	J01	PEXTX02-	AM04	VPAR
V34	HA20#	F28	HD39#	AT29	MA00	AK20	MD32	AT26	MODT0	H01	PEXTX02+	AR05	VUPCMD
W36	HA21#	E27	HD40#	AR30	MA01	AK19	MD33	AP25	MODT1	L01	PEXTX03-	AR03	VUPSTB-
W34	HA22#	D26	HD41#	AR29	MA02	AM19	MD34	AR24	MODT2	K01	PEXTX03+	AT02	VUPSTB+
AA36	HA23#	D25	HD42#	AT30	MA03	AR18	MD35	AN25	MODT3	M04	PEXTX04-	D12	XIN
V33	HA24#	E25	HD43#	AN30	MA04	AL20	MD36	AR27	MSCAS#	L04	PEXTX04+		
AA34	HA25#	F25	HD44#	AP31	MA05	AM20	MD37	AN28	MSRAS#	N01	PEXTX05-		
Y35	HA26#	G25	HD45#	AR31	MA06	AL18	MD38	AP28	MSWE#	M01	PEXTX05+		
Y33	HA27#	H26	HD46#	AT32	MA07	AM18	MD39	A05	NC	P04	PEXTX06-		
AA32	HA28#	H25	HD47#	AP32	MA08	AR17	MD40	C06	NC	N04	PEXTX06+		

Table 3. Signal Ball List - Display Functions Enabled on PCI Express Interface (Listed by Ball Name)

Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name
AC35	BUSY#	U36	HA12#	G32	HD31#	M31	HREQ4#	AK24	MD24	AR20	MDQS6-	U01	NC
F22	CPURST#	U34	HA13#	E28	HD32#	J35	HRS0#	AL23	MD25	AP20	MDQS6+	U04	NC
AB32	CPUSLPIN#	U35	HA14#	E29	HD33#	N36	HRS1#	AM24	MD26	AR13	MDQS7-	V01	NC
E14	CRTAB	T30	HA15#	D28	HD34#	J36	HRS2#	AJ22	MD27	AR12	MDQS7+	V04	NC
D14	CRTAG	U32	HA16#	D27	HD35#	M35	HTRDY#	AK23	MD28	AM33	MEMCOMP	W01	NC
C14	CRTAR	W35	HA17#	C28	HD36#	H13	INTA#	AN24	MD29	AF36	MEMDET	W04	NC
E12	CRTHSYNC	V32	HA18#	H28	HD37#	A11	LVDSENVBLD	AM23	MD30	AG29	MEMVREF0	Y01	NC
C13	CRTRSET	V36	HA19#	G28	HD38#	B11	LVDSENVDD	AM22	MD31	AJ18	MEMVREF1	Y04	NC
E13	CRTSPD	V34	HA20#	F28	HD39#	AT29	MA00	AK20	MD32	AT26	MODT0	AF06	PEXCLK-
G13	CRTSPDCLK	W36	HA21#	E27	HD40#	AR30	MA01	AK19	MD33	AP25	MODT1	AG06	PEXCLK+
F12	CRTVSYNC	W34	HA22#	D26	HD41#	AR29	MA02	AM19	MD34	AR24	MODT2	H05	PEXCOMP0
G12	DISPCLKI	AA36	HA23#	D25	HD42#	AT30	MA03	AR18	MD35	AN25	MODT3	AD07	PEXCOMP1
H12	DISPCLKO	V33	HA24#	E25	HD43#	AN30	MA04	AL20	MD36	AR27	MSCAS#	AH01	PEXCOMP2
W06	DVP1CLK	AA34	HA25#	F25	HD44#	AP31	MA05	AM20	MD37	AN28	MSRAS#	B05	PEXDET
AB03	DVP1D00	Y35	HA26#	G25	HD45#	AR31	MA06	AL18	MD38	AP28	MSWE#	AC36	PEXHPSCI#
AB06	DVP1D01	Y33	HA27#	H26	HD46#	AT32	MA07	AM18	MD39	K03	NC	B06	PEXINTR#
AA06	DVP1D02	AA32	HA28#	H25	HD47#	AP32	MA08	AR17	MD40	N06	NC	AC33	PEXPMESCI#
AA03	DVP1D03	W32	HA29#	B23	HD48#	AN32	MA09	AT16	MD41	M06	NC	G05	PEXREXT0
Y03	DVP1D04	V31	HA30#	B25	HD49#	AN29	MA10	AN16	MD42	N03	NC	AD06	PEXREXT1
V06	DVP1D05	W31	HA31#	E23	HD50#	AR32	MA11	AN15	MD43	M03	NC	AH02	PEXREXT2
W03	DVP1D06	L35	HADS#	B27	HD51#	AT33	MA12	AM17	MD44	L06	NC	AC34	PEXWAKE#
V03	DVP1D07	T35	HADSTB0N#	B28	HD52#	AR25	MA13	AP17	MD45	K06	NC	AD34	PWROK
U06	DVP1D08	R35	HADSTB0P#	A28	HD53#	AR28	MBA0	AM16	MD46	J03	NC	AD36	RESET#
T06	DVP1D09	W33	HADSTB1#	B24	HD54#	AP29	MBA1	AM15	MD47	H03	NC	AD35	SUSST#
U03	DVP1D10	K35	HBNR#	B26	HD55#	AP33	MBA2	AN22	MD48	G03	NC	D07	TCSEN#
T03	DVP1D11	J32	HBPRI#	A26	HD56#	AT34	MCKE0	AN21	MD49	F03	NC	AE36	TESTEN
AC03	DVP1DE	M34	HBREQ0#	C23	HD57#	AP34	MCKE1	AP19	MD50	D02	NC	AN04	VBE#
AD03	DVP1HS	AC30	HCLK-	C22	HD58#	AR34	MCKE2	AT18	MD51	E03	NC	AL04	VCLK
AE03	DVP1VS	AC29	HCLK+	A23	HD59#	AN34	MCKE3	AT21	MD52	P03	NC	AP01	VD00
B09	DVP2CLK	B35	HD00#	G23	HD60#	AB34	MCLKI	AR21	MD53	R03	NC	AN03	VD01
H11	DVP2D00	A36	HD01#	A24	HD61#	AB36	MCLKO-	AT19	MD54	A05	NC	AT03	VD02
D10	DVP2D01	C33	HD02#	B22	HD62#	AB35	MCLKO+	AR19	MD55	AA01	NC	AR04	VD03
C11	DVP2D02	C32	HD03#	E22	HD63#	AT27	MCS0#	AR14	MD56	AB31	NC	AN02	VD04
C10	DVP2D03	E31	HD04#	C31	HDBI0#	AP27	MCS1#	AM14	MD57	AC01	NC	AN01	VD05
E10	DVP2D04	B34	HD05#	E35	HDBI1#	AT24	MCS2#	AP13	MD58	AC04	NC	AP05	VD06
G10	DVP2D05	B33	HD06#	G27	HDBI2#	AP26	MCS3#	AR11	MD59	AD01	NC	AN05	VD07
F11	DVP2D06	A34	HD07#	D22	HDBI3#	AF35	MD00	AP14	MD60	AD04	NC	AM01	VD08
C09	DVP2D07	D30	HD08#	K32	HDBSY#	AG34	MD01	AN14	MD61	AE01	NC	AM03	VD09
E08	DVP2D08	A30	HD09#	J33	HDEFER#	AJ36	MD02	AT12	MD62	AE04	NC	AT05	VD10
B07	DVP2D09	B31	HD10#	L31	HDPWR#	AK35	MD03	AP12	MD63	AF01	NC	AM06	VD11
F09	DVP2D10	B30	HD11#	K33	HDRDY#	AF34	MD04	AH36	MDQM0#	AF04	NC	AL02	VD12
C07	DVP2D11	E30	HD12#	B32	HDSTB0N#	AG35	MD05	AF30	MDQM1#	AG01	NC	AL01	VD13
D09	DVP2DE	C29	HD13#	A32	HDSTB0P#	AJ34	MD06	AN36	MDQM2#	B01	NC	AN06	VD14
A09	DVP2DET	B29	HD14#	C34	HDSTB1N#	AK34	MD07	AN23	MDQM3#	C01	NC	AT06	VD15
E11	DVP2HS	C30	HD15#	C35	HDSTB1P#	AG32	MD08	AN20	MDQM4#	D01	NC	AP04	VDNCMD
B10	DVP2VS	D36	HD16#	E26	HDSTB2N#	AF32	MD09	AT15	MDQM5#	E01	NC	AT01	VDNSTB-
C06	DVPDET	F36	HD17#	G26	HDSTB2P#	AH30	MD10	AP21	MDQM6#	H01	NC	AR01	VDNSTB+
C08	DVPSPCLK	G36	HD18#	C25	HDSTB3N#	AJ31	MD11	AT13	MDQM7#	J01	NC	AL05	VLCOMPN
A07	DVPSPD	H34	HD19#	C24	HDSTB3P#	AF31	MD12	AH35	MDQS0-	K01	NC	AM05	VLCOMPP
B08	GPO0	H35	HD20#	H22	HGTLCOMPN	AH32	MD13	AJ35	MDQS0+	L01	NC	AL06	VLVREF
A06	GPOUT	F35	HD21#	G22	HGTLCOMPP	AH31	MD14	AH34	MDQS1-	L03	NC	AM04	VPAR
M33	HA03#	G35	HD22#	U30	HGTLVREF0	AJ32	MD15	AH33	MDQS1+	L04	NC	AR05	VUPCMD
N34	HA04#	C36	HD23#	J25	HGTLVREF1	AK33	MD16	AP36	MDQS2-	M01	NC	AR03	VUPSTB-
R33	HA05#	D35	HD24#	L36	HHIT#	AL36	MD17	AR36	MDQS2+	M04	NC	AT02	VUPSTB+
T33	HA06#	F34	HD25#	L34	HHITM#	AP35	MD18	AP23	MDQS3-	N01	NC	D12	XIN
R34	HA07#	F33	HD26#	J34	HLOCK#	AL34	MD19	AR22	MDQS3+	N04	NC		
P36	HA08#	G34	HD27#	T32	HREQ0#	AL35	MD20	AN18	MDQS4-	P01	NC		
P34	HA09#	G33	HD28#	T31	HREQ1#	AM35	MD21	AP18	MDQS4+	P04	NC		
N35	HA10#	E33	HD29#	R32	HREQ2#	AT36	MD22	AR15	MDQS5-	R01	NC		
R36	HA11#	H32	HD30#	M32	HREQ3#	AM34	MD23	AP15	MDQS5+	T01	NC		

Table 4. Power / Ground Ball List

Ball Name	Ball Numbers
VTT	A17, A18, A19, A20, A21, B17, B18, B19, B20, B21, C17, C18, C19, C20, C21, D17, D18, D19, D20, D21, E17, E18, E19, E20, E21, F17, F18, F19, F20, F21, G17, G18, G19, G20, G21, M17, M18, M19, N18, N19, N20, N21, N22, N23, N24, P24, R24, T24, U24, V24, W24, Y24
VCCMEM	AA24, AB24, AC24, AD16, AD17, AD18, AD19, AD20, AD21, AD22, AD23, AD24, AJ26, AJ28, AK25, AK27, AK29, AL26, AL28, AL30, AM25, AM27, AM29, AM31, AN26, AN27, AN31, AN33, AP30, AR26, AR33, AT25, AT28, AT31, AT35
VCC15	AA12, AB12, AB25, AC12, AC25, AD12, AE14, AE16, AE18, AE20, AE21, AE22, AJ10, AJ11, AJ12, AJ13, AJ14, AK09, AK10, AK11, AK12, AK13, AK15, AL08, AL09, AL10, AL11, AL12, AL14, AM07, AM08, AM09, AM10, AM11, AM12, AM13, AN07, AN08, AN09, AN10, AN11, AP07, AP08, AP09, AP10, AP11, AR07, AR08, AR09, AR10, AT07, AT08, AT09, AT10, M12, M13, M14, M15, M16, M20, M21, M22, M23, M24, N12, N25, P12, P25, R12, T12, T25, U12, U25, V12, W12, W25, Y12, Y25
VCC15VL	AD13, AD14, AD15
VCC33PEX	AA13, AB13, AC13, AJ01, AJ02, AJ03, AJ04, AJ05, AJ06, AJ07, AK01, AK02, AK03, AK04, AK05, AK06, AK07, N13, N14, P13, R13, T13, U13, V13, W13, Y13
VCC33GFX	N15, N16, N17
VSUS15	AD31
VSUS15PEX	AF07
GND	A01, A02, A03, A08, A10, A22, A25, A27, A29, A31, A33, A35, AA02, AA04, AA05, AA07, AA14, AA15, AA16, AA17, AA18, AA19, AA20, AA21, AA22, AA23, AA31, AA33, AA35, AB02, AB04, AB05, AB07, AB14, AB15, AB16, AB17, AB18, AB19, AB20, AB21, AB22, AB23, AC02, AC05, AC06, AC07, AC14, AC15, AC16, AC17, AC18, AC19, AC20, AC21, AC22, AC23, AD02, AD05, AD32, AE02, AE05, AE32, AE34, AF02, AF03, AF05, AG02, AG03, AG04, AG05, AG30, AG31, AG33, AG36, AJ19, AJ20, AJ23, AJ33, AK17, AK18, AK22, AK32, AK36, AL03, AL07, AL15, AL16, AL17, AL19, AL22, AL24, AL33, AM02, AM36, AN12, AN13, AN17, AN19, AN35, AP02, AP03, AP06, AP16, AP22, AP24, AR02, AR06, AR16, AR23, AR35, AT04, AT11, AT14, AT17, AT20, AT22, AT23, B02, B03, B04, B36, C02, C03, C04, C05, C12, C26, C27, D03, D04, D05, D06, D08, D11, D13, D23, D24, D29, D31, D32, D34, E02, E04, E05, E06, E07, E09, E34, E36, F01, F02, F04, F05, F06, F07, F10, F13, F14, F23, F24, F26, F27, F29, F30, F32, G01, G02, G04, G07, G11, G29, H02, H04, H07, H23, H24, H27, H31, H33, H36, J02, J04, J05, J06, J07, K02, K04, K05, K07, K31, K34, K36, L02, L05, L07, L32, L33, M02, M05, M07, M36, N02, N05, N07, P02, P05, P06, P07, P14, P15, P16, P17, P18, P19, P20, P21, P22, P23, P33, P35, R02, R04, R05, R06, R07, R14, R15, R16, R17, R18, R19, R20, R21, R22, R23, R30, R31, T02, T04, T05, T07, T14, T15, T16, T17, T18, T19, T20, T21, T22, T23, T34, T36, U02, U05, U07, U14, U15, U16, U17, U18, U19, U20, U21, U22, U23, U31, U33, V02, V05, V07, V14, V15, V16, V17, V18, V19, V20, V21, V22, V23, V30, V35, W02, W05, W07, W14, W15, W16, W17, W18, W19, W20, W21, W22, W23, Y02, Y05, Y06, Y07, Y14, Y15, Y16, Y17, Y18, Y19, Y20, Y21, Y22, Y23, Y30, Y32, Y34, Y36
VCCA33HCK	AC31
GNDAHCK	AC32
VCCA33MCK	AD30
GNDAMCK	AD29
VCCA33PLL[3:1]	A14, A15, A16
GNDAPLL	B14, B15, B16
VCCA33DA[2:1]	A12, A13
GNDADAC	B12, B13
GNDAPEX[2:0]	AH04, AE07, H06
GNDAPEXCK	AH06
VCCA33PEX[2:0]	AH03, AE06, G06
VCCA33PEXCK	AH05

Signal Descriptions

CPU Interface Signal Descriptions

CPU Interface				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
HA[31:03]#	(see ball lists)	IO	**Host CPU Address Bus.** Connect to the address bus of the host CPU. Inputs during CPU cycles and driven by the North Bridge during cache snooping operations.	**VTT**
HADSTB0N# **HADSTB1#** **HADSTB0P#** **(HADSTB0#)**	R35 T35 W33	IO	**Host Address Strobe.** **(V4 Host Protocol)** HADSTB0P# / HADSTB0N# are negative-edge going data strobes used to latch HA[30, 16:03]# and HREQ[2:0] on even and odd data beat transfers respectively. **(P4 Host Protocol)** Source synchronous strobes used to transfer HA[31:03]# and HREQ[4:0]# at a 2x transfer rate. HADSTB1# is the strobe for HA[31:17]# and HADSTB0P# is the strobe for HA[16:03] and HREQ[4:0]#.	**VTT**
HD[63:00]#	(see ball lists)	IO	**Host CPU Data.** These signals are connected to the CPU data bus.	**VTT**
HDBI[3:0]#	D22, G27, E35, C31	IO	**Host CPU Dynamic Bus Inversion.** Driven along with HD[63:0]# to indicate if the associated signals are inverted or not. Used to limit the number of simultaneously switching signals to 8 for the associated 16-bit data pin group (HDBI3# for HD[63:48]#, HDBI2# for HD[47:32]#, HDBI1# for HD[31:16]#, and HDBI0# for HD[15:0]#). HDBIn# is asserted such that the number of data bits driven low for the corresponding group does not exceed 8.	**VTT**
HDSTB[3:0]P# **HDSTB[3:0]N#**	C24, G26, C35, A32 C25, E26, C34, B32	IO	**Host CPU Differential Data Strobes.** Source synchronous strobes used to transfer HD[63:0]# and HDBI[3:0]# at a 4x transfer rate. HDSTB3P# / HDSTB3N# are the strobes for HD[63:48]# & HDBI3#; HDSTB2P# / HDSTB2N# are the strobes for HD[47:32]# & HDBI2#; HDSTB1P# / HDSTB1N# are the strobes for HD[31:16]# & HDBI1#; and HDSTB0P# / HDSTB0N# are the strobes for HD[15:0]# & HDBI0#.	**VTT**
HADS#	L35	IO	**Address Strobe**. The CPU asserts HADS# in T1 of the CPU bus cycle.	**VTT**
HDBSY#	K32	IO	**Data Bus Busy**. Used by the data bus owner to hold the data bus for transfers requiring more than one cycle.	**VTT**
HDRDY#	K33	IO	**Data Ready**. Asserted for each cycle that data is transferred.	**VTT**
HHIT#	L36	IO	**Hit**. Indicates that a caching agent holds an unmodified version of the requested line. Also driven in conjunction with HHITM# by the target to extend the snoop window.	**VTT**
HHITM#	L34	IO	**Hit Modified**. Asserted by the CPU to indicate that the address is modified in the L1 cache and needs to be written back.	**VTT**
HLOCK#	J34	IO	**Host Lock**. All CPU cycles sampled with the assertion of HLOCK# and ADS# until the negation of HLOCK# must be atomic.	**VTT**
HREQ[4:0]#	M31, M32, R32, T31, T32	IO	**Request Command**. Asserted during both clocks of the request phase. In the first clock, the signals define the transaction type to a level of detail that is sufficient to begin a snoop request. In the second clock, the signals carry additional information to define the complete transaction type.	**VTT**
HTRDY#	M35	O	**Host Target Ready**. Indicates that the target of the processor transaction is able to enter the data transfer phase.	**VTT**

Note: Clocking of the CPU interface is performed with HCLK+ and HCLK– (see clock signal description group).

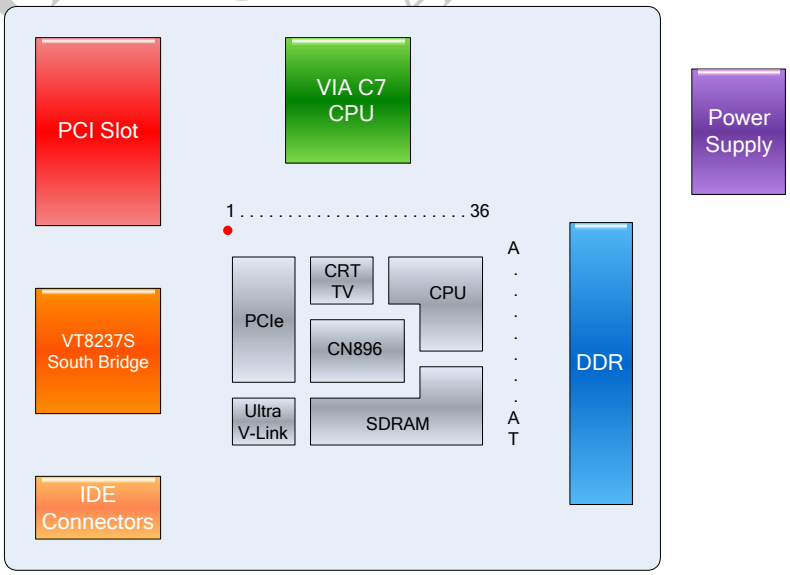
Note: Internal pullup resistors are provided on all AGTL+ interface signals. If the CPU does not have internal pullups, these North Bridge internal pullups may be enabled to allow the interface to meet AGTL+ bus interface specs (see VD3 strap).

Note: I/O pads for the above signals are powered by VTT. Input voltage levels are referenced to GTLVREF.

CPU Interface (continued)				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
HRS[2:0]#	J36, N36, J35	O	**Response Signals**. Indicates the type of response per the table below: **HRS[2:0]# / Response type** 000 Idle State 001 Retry Response 010 Defer Response 011 Reserved 100 Hard Failure 101 Normal Without Data 110 Implicit Writeback 111 Normal With Data	**VTT**
HDPWR#	L31	O	**Data Bus Power Reduction.** Request to reduce power on the mobile CPU data bus input buffer. Connect to mobile CPU if used.	**VTT**
HBREQ0#	M34	IO	**Bus Request 0.** Bus request output to CPU.	**VTT**
HBPRI#	J32	O	**Priority Agent Bus Request**. The owner of this signal will always be the next bus owner. This signal has priority over symmetric bus requests and causes the current symmetric owner to stop issuing new transactions unless the HLOCK# signal is asserted. The CN896 drives this signal to gain control of the processor bus.	**VTT**
HBNR#	K35	IO	**Block Next Request**. Used to block the current request bus owner from issuing new requests. This signal is used to dynamically control the processor bus pipeline depth.	**VTT**
HDEFER#	J33	O	**Defer**. The CN896 uses a dynamic deferring policy to optimize system performance. The CN896 also uses the HDEFER# signal to indicate a processor retry response.	**VTT**
CPURST#	F22	O	**CPU Reset.** Reset output to CPU. External pullup and filter capacitor to ground should be provided per CPU manufacturer's recommendations.	**VTT**

Note: I/O pads for the above signals are powered by VTT. Input voltage levels are referenced to GTLVREF.

The pinouts were defined assuming the ATX PCB layout model shown below (and general pin layout shown) as a guide for PCB component placement. Other PCB layouts (AT, LPX, and NLX) were also considered and can typically follow the same general component placement.



DDR SDRAM Memory Controller Signal Descriptions

DRAM Interface				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
MD[63:00]	(see ball lists)	IO	**Memory Data.** These signals are connected to the DRAM data bus.	**VCCMEM**
MA[13:00]	(see ball lists)	O	**Memory Address.** DRAM address lines.	**VCCMEM**
HSRAS#, HSCAS#, **HSWE#**	AN28, AR27, AP28	O	**Row Address, Column Address and Write Enable Command Indicator Set.**	**VCCMEM**
MBA[0:2]	AR28, AP29, AP33	O	**Bank Address:** defines which bank will receive an ACTIVE, READ, WRITE, or PRECHARGE command.	**VCCMEM**
MCS[3:0]#	AP26, AT24, AP27, AT27	O	**Chip Select.** Chip select of each bank.	**VCCMEM**
MDQM[7:0]#	AT13, AP21, AT15, AN20, AN23, AN36, AF30, AH36	O	**DDR Data Mask.** Data mask of each byte lane.	**VCCMEM**
MDQS[7:0]+/-	(see ball lists)	IO	**DDR Data Strobe.** Data strobe of each byte.	**VCCMEM**
MCKE[3:0]	AN34, AR34, AP34, AT34	O	**Clock Enables.** Clock enables for each DRAM bank for powering down the SDRAM or clock control for reducing power usage and for reducing heat / temperature in high-speed memory systems.	**VCCMEM**
MEMDET	AF36	I	**Memory Detect:** Strap low for DDR.	**VCCMEM**
MODT[3:0]	AN25, AR24, AP25, AT26	O	**On Die Termination.** Enables termination resistance internal to the DDR2 SDRAM	**VCCMEM**

Note: I/O pads for all SDRAM signals are powered by VCCMEM. MD / MDQS input voltage levels are referenced to MEMVREF.

PCI Express Interface

PCI Express (PCIe) Port G				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
PEXRX[15:00]+/–	(see ball lists)	I	**PCI Express Port G Differential Receive Data [15:00].** These signals are multiplexed with Digital Video Port signals.	**VCC33PEX**
PEXTX[15:00]+/–	(see ball lists)	O	**PCI Express Port G Differential Transmit Data [15:00].**	**VCC33PEX**

PCI Express (PCIe) Port 0				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
PEXRX16+/–	AF04, AE04	I	**PCI Express Port 0 Differential Receive Data 0.**	**VCC33PEX**
PEXTX16+/–	AG01, AF01	O	**PCI Express Port 0 Differential Transmit Data 0.**	**VCC33PEX**

Ultra V-Link Signal Descriptions

Ultra V-Link Interface				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
VD[15:00]	(see ball list)	IO	**V-Link Data Bus.** Used to transfer data between the North Bridge and the South Bridge.	**VCC15VL**
VPAR	AM04	IO	**Parity.**	**VCC15VL**
VBE#	AN04	IO	**V-Link Byte Enable.**	**VCC15VL**
VUPCMD	AR05	I	**V-Link Command from Client (South Bridge) to Host (North Bridge).**	**VCC15VL**
VUPSTB+	AT02	I	**V-Link Strobe from Client to Host.**	**VCC15VL**
VUPSTB–	AR03	I	**V-Link Complement Strobe from Client to Host.**	**VCC15VL**
VDNCMD	AP04	O	**V-Link Command from Host (North Bridge) to Client (South Bridge).**	**VCC15VL**
VDNSTB+	AR01	O	**V-Link Strobe from Host to Client.**	**VCC15VL**
VDNSTB–	AT01	O	**V-Link Complement Strobe from Host to Client.**	**VCC15VL**

CRT and Serial Bus Signal Descriptions

CRT Interface				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
CRTAR	C14	AO	**Analog Red.** Analog red output to the CRT monitor.	**VCC33DAC**
CRTAB	E14	AO	**Analog Blue.** Analog blue output to the CRT monitor.	**VCC33DAC**
CRTAG	D14	AO	**Analog Green.** Analog green output to the CRT monitor.	**VCC33DAC**
CRTHSYNC	E12	O	**Horizontal Sync.** Output to CRT.	**VCC33GFX**
CRTVSYNC	F12	O	**Vertical Sync.** Output to CRT.	**VCC33GFX**
CRTRSET	C13	AI	**Reference Resistor.** Tie to GND through an external 80.6Ω 1% resistor to control the RAMDAC full-scale current value.	**VCC33GFX**

SMB / I2C Interface				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
CRTSPCLK **CRTSPD** **DVPSPCLK** **DVPSPD**	G13 E13 C08 A07	IO	**Serial Port (SMB / I2C) Clock and Data.** The SPCLKn pins are the clocks for serial data transfer. The SPDn pins are the data signals used for serial data transfer.	**VCC33GFX**

Dedicated Digital Video Port (DVP2) Interface

TV-Out Interface				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
DVP2D[11:00]	(see ball lists)	O	**TV encoder Data Output**	**VCC33GFX**
DVP2HS	E11	O	**TV encoder Horizontal Sync.**	**VCC33GFX**
DVP2VS	B10	O	**TV encoder Vertical Sync.**	**VCC33GFX**
DVP2CLK	B09	O	**TV encoder Clock.**	**VCC33GFX**
TVCLKR/DVP 2DET	A09	I	**TV encoder clock return.**	**VCC33GFX**
DVP2DE	D09	O	**TV encoder Data Enable.**	**VCC33GFX**

Flat Panel Power Control				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
LVDSENVDD	B11	O	**Enable Panel VDD Power.**	**VCC33GFX**
LVDSENVBLD	A11	O	**Enable Panel Back Light.**	**VCC33GFX**

PCIe-multiplexed Digital Video Port 1 (DVP1) Interface

The DVP1 Digital Video Port is supported through multiplexing with PCIe signals. It can be configured as either a LVDS transmitter or a DVI Transmitter interface port.

LVDS Transmitter					
Signal Name	**PCIe Name**	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
DVP1D00	**PEXRX14+**	AB03	O	**Data.**	**VCC33PEX**
DVP1D01	**PEXRX13–**	AB06			
DVP1D02	**PEXRX13+**	AA06			
DVP1D03	**PEXRX12–**	AA03			
DVP1D04	**PEXRX12+**	Y03			
DVP1D05	**PEXRX11–**	V06			
DVP1D06	**PEXRX10–**	W03			
DVP1D07	**PEXRX10+**	V03			
DVP1D08	**PEXRX09–**	U06			
DVP1D09	**PEXRX09+**	T06			
DVP1D10	**PEXRX08–**	U03			
DVP1D11	**PEXRX08+**	T03			
DVP1VS	**PEXRX15–**	AE03	O	**Vertical Sync.**	**VCC33PEX**
DVP1HS	**PEXRX15+**	AD03	O	**Horizontal Sync.**	**VCC33PEX**
DVP1DE	**PEXRX14–**	AC03	O	**Data Enable.**	**VCC33PEX**
DVP1CLK	**PEXRX11+**	W06	O	**Clock Out.** Output to TV Encoder. Internal pull down.	**VCC33PEX**

DVI Transmitter					
Signal Name	**PCIe Name**	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
DVP1D0	**PEXRX14+**	AB03	O	**Data.**	**VCC33PEX**
DVP1D1	**PEXRX13–**	AB06			
DVP1D2	**PEXRX13+**	AA06			
DVP1D3	**PEXRX12–**	AA03			
DVP1D4	**PEXRX12+**	Y03			
DVP1D5	**PEXRX11–**	V06			
DVP1D6	**PEXRX10–**	W03			
DVP1D7	**PEXRX10+**	V03			
DVP1D8	**PEXRX9–**	U06			
DVP1D9	**PEXRX9+**	T06			
DVP1D10	**PEXRX8–**	U03			
DVP1D11	**PEXRX8+**	T03			
DVP1VS	**PEXRX15–**	AE03	O	**Vertical Sync.**	**VCC33PEX**
DVP1HS	**PEXRX15+**	AD03	O	**Horizontal Sync.**	**VCC33PEX**
DVP1DE	**PEXRX14–**	AC03	O	**Data Enable.**	**VCC33PEX**
DVP1DET	**NC**	L03	I	**Display Detect.**	**VCC33GFX**
DVP1CLK	**PEXRX11+**	W06	O	**Clock Out.**	**VCC33PEX**

Clock Signal Descriptions

Clock				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
VCLK	AL04	I	**V-Link Clock.** This signal receives the 66 MHz clock used to generate the internal clocks required by V-Link interface between the North Bridge and South Bridge.	**VCC15VL**
HCLK+	AC29	I	**Host Clock.** This signal receives the host CPU clock (100 / 133 / 166 / 200 MHz). This clock is used by all CN896 logic that is in the host CPU domain.	**VTT**
HCLK–	AC30	I	**Host Clock Complement.** Used for Quad Data Transfer on host CPU bus.	**VTT**
PEXCLK+ **PEXCLK–**	AG06 AF06	I	**PCI Express Differential Clock.** These signals receive the 100 MHz clock used by the internal PCI Express logic. Multiplied up to 2.5 GHz on-chip for use by the integrated PCI Express PHY to transmit / receive data.	**VCCA33PEX**
MCLKO+	AB35	O	**Memory (SDRAM) Clock.** Output from internal clock generator to external memory interface clock buffer (if required for fanout)	**VCCMEM**
MCLKO-	AB36	O	**Memory (SDRAM) Clock Complement.**	**VCCMEM**
MCLKI	AB34	I	**Memory (SDRAM) Clock Feedback.** Input from MCLKO.	**VCCMEM**
DISPCLKI	G12	I	**Dot Clock (Pixel Clock) In.** Used for external EMI reduction circuit if used. Connect to **GND** if external EMI reduction circuit not implemented.	**VCC33GFX**
DISPCLKO	H12	O	**Dot Clock (Pixel Clock) Out.** Used for external EMI reduction circuit if used. NC if external EMI reduction circuit not implemented.	**VCC33GFX**

Reset, Power Control, GPIO, Interrupt and Test Signal Descriptions

Resets, Power Control, General Purpose I/O, Interrupts and Test				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
XIN	D12	I	**Reference Frequency Input.** External 14.31818 MHz clock source. All internal graphics controller clocks are synthesized on chip using this frequency as a reference.	**VCC33GFX**
PWROK	AD34	I	**Power OK.** Connect to South Bridge and Power Good circuitry.	**VSUS15**
SUSST#	AD35	I	**Suspend Status.** For implementation of the Suspend-to-DRAM feature. Connect to an external pull-up to disable.	**VSUS15**
RESET#	AD36	I	**Reset.** Input from the South Bridge chip. When asserted, this signal resets the CN896 and sets all register bits to the default value. The rising edge of this signal is used to sample all power-up strap options	**VCCMEM**
CPUSLPIN#	AB32	I	Input from SLP# of South Bridge chip. This signal is used to inform North Bridge when the processor is in C3/C4 state.	**VTT**
BUSY#	AC35	O	**Busy.** Indicates that master cycles are pending in the chip. Used by the power management system to avoid changing the system power state while a master cycle is in progress.	**VCCMEM**
GPOUT	A06	O	**General Purpose Output.** This signal reflects the state of SRD[0].	**VCC33GFX**
GPO0	B08	O	**General Output Port.** When SR1A[4] is cleared, this pin reflects the state of CR5C[0].	**VCC33GFX**
PEXWAKE#	AC34	OD	**PCI Express Wake.** Indicates that a system wake event has occurred on the PCI Express bus. Used to waken the chip from deep sleep mode (S3 / S4 / S5 states). Wire-OR with other system WAKE# signals (including PEWAKE# on the PCI Express bus connector) and connect to the South Bridge PME input.	**VSUS15**
PEXPMESCI#	AC33	OD	**PCI Express PME SCI.** System Control Interrupt to indicate Power Management Event. Connect to South Bridge SCI input (GPIO pin).	**VSUS15**
PEXHPSCI#	AC36	OD	**PCI Express Hot-Plug SCI.** System Control Interrupt to indicate Hot Plug occurred. Connect to South Bridge SCI input (GPIO pin).	**VSUS15**
PEXINTR#	B06	OD	**PCI Express Interrupt.** Connect to South Bridge interrupt input to indicate that an interrupt condition was detected on PCI Express bus or the internal APIC.	**VCC33PEX**
INTA#	H13	O	**Interrupt.** PCI interrupt output (handled by the interrupt controller in the South Bridge)	**VCC33GFX**
TESTEN	AE36	I	**Test Enable.** This signal is used for testing. Pull down for normal operation.	**VCCMEM**
PEXDET	B05	I	**PCI Express Detect.** Used to determine the presence of an external PCI Express device.	**VCC33GFX**

Trusted Platform Module Signal Descriptions

Trusted Platform Module (TPM)				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
TCSEN#	D07	I	**Trusted Configuration Space Enable.**	**VCC33**

Compensation Signal Descriptions

Compensation				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
VLCOMPP	AM05	AI	**V-Link P Compensation.**	**VCC15VL**
VLCOMPN	AL05	AI	**V-Link N Compensation.**	**VCC15VL**
HGTLCOMPP	G22	AI	**AGTL P Compensation.**	**VTT**
HGTLCOMPN	H22	AI	**AGTL N Compensation.**	**VTT**
MEMCOMP	AM33	AI	**DRAM Compensation.** Memory interface IO buffer calibration.	**VCCMEM**
PEXCOMP0	H05	AI	**PCI Express Port G Compensation 0.**	**VCC33PEX**
PEXREXT0	G05	AI	**PCI Express Port G External Resistor 0.**	**VCC33PEX**
PEXCOMP1	AD07	AI	**PCI Express Port G Compensation 1.**	**VCC33PEX**
PEXREXT1	AD06	AI	**PCI Express Port G External Resistor 1.**	**VCC33PEX**
PEXCOMP2	AH01	AI	**PCI Express Port 0 Compensation.**	**VCC33PEX**
PEXREXT2	AH02	AI	**PCI Express Port 0 External Resistor.**	**VCC33PEX**

Reference Voltage Signal Descriptions

Reference Voltages				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
HGTLVREF[1:0]	J25, U30	P	**Host CPU Interface AGTL+ Voltage Reference.** 2/3 VTT ±2% typically derived using a resistive voltage divider. See Design Guide.	**VTT**
MEMVREF[1:0]	AJ18, AG29	P	**Memory Voltage Reference.** ½ VCCMEM ±2% typically derived using a resistive voltage divider. See Design Guide.	**VCCMEM**
VLVREF	AL06	P	**V-Link Voltage Reference.** 0.45V ±2% derived using a resistive voltage divider. See Design Guide.	**VCC15VL**

Power/Ground Descriptions

Analog Power / Ground			
Signal Name	**Ball #**	**I/O**	**Signal Description**
VCCA33HCK	AC31	P	**Power for Host CPU Clock PLL** (3.3V ±5%). 400 MHz for CPU / DRAM frequencies of multiples of 100, 133, 166 and 200 MHz.
GNDAHCK	AC32	P	**Ground for Host CPU Clock PLL.** Connect to main ground plane.
VCCA33MCK	AD30	P	**Power for Memory Clock PLL** (3.3V ±5%)
GNDAMCK	AD29	P	**Ground for Memory Clock PLL.** Connect to main ground plane.
VCCA33PLL[3:1]	A14, A15, A16	P	**Power for Graphics Controller PLL** (3.3V ±5%).
GNDAPLL	B14, B15, B16	P	**Ground for Graphics Controller PLL.** Connect to main ground plane.
VCCA33DAC[2:1]	A12, A13	P	**Power for DAC.** (3.3V ±5%)
GNDADAC	B12, B13	P	**Ground for DAC.** Connect to main ground plane.
GNDAPEX[2:0]	AH04, AE07, H06	P	**Ground for PCI Express Ports.**
GNDAPEXCK	AH06	P	**Ground for PCI Express Clock.**
VCCA33PEX[2:0]	AH03, AE06, G06	P	**Power for PCI Express Port.**
VCCA33PEXCK	AH05	P	**Power for PCI Express Clock.**

Digital Power / Ground			
Signal Name	**Ball #**	**I/O**	**Signal Description**
VTT	(see ball lists)	P	**Power** for **CPU I/O Interface Logic.** Voltage is CPU dependent. See Design Guide for details.
VCCMEM	(see ball lists)	P	**Power** for **Memory I/O Interface Logic.** 2.5V±5%. (DDR) / 1.8V±5%. (DDR2)
VCC15VL	AD13, AD14, AD15	P	**Power** for **V-Link I/O Interface Logic.** 1.5V ±5%
VCC33PEX	(see ball lists)	P	**Power for PCIe I/O Interface Logic.** 3.3V ±5%
VCC33GFX	N15, N16, N17	P	**Power for Graphics Display I/O Logic.** 3.3V ±5%
VCC15	(see ball lists)	P	**Core Power.** 1.6V ±5%
VSUS15	AD31	P	**Suspend Power.** 1.5V ±5%
VSUS15PEX	AF07	P	**PCI Express Suspend Power.** 1.5V ±5%
GND	(see ball lists)	P	**Digital Ground.** Connect to main ground plane.

Strap Signal Descriptions

Strap Signals (External pullup / pulldown straps are required to select "H" / "L")			
Signal	**Actual Strap Pin**	**Function**	**Description**
DVP2D[03:00]		Panel Type	Reserved for customer definition Pull down if not used
DVP2D04		Port Muxing	L: Dual 12-Bit DVI Interface H: One 24-Bit Panel Interface
DVP2D05		DVP2 Configuration	L: DVI Interface H: TV Encoder
DVP2D06		DVP2 Enable	L: Disable H: Enable
DVP2D07		GFX Clock Select (VCLK/LCDCK/ECK)	L: Refer Internal PLL H: From External
DVP2D10		CPUCK/MCK Select	L: From NB H: From External
DVP2D[08,09,11]		-reserved-	Must pull down (Except DVP2D11)
VD07	PDCS3#	V-Link Reference Voltage Select (4x)	L: 0.75V H: 0.9V
VD06	PDA2	V4 Capability	L: Disable H: Enable
VD05	PDA1	V4-Lite Capability	L: Disable H: Enable
VD04	PDA0	-reserved-	Must pull low.
VD03	GPIOD	AGTL+ Pullups	L: Enable internal AGTL+ Pullups H: Disable internal AGTL+ Pullups
VD02	GPIOB	IOQ Depth	L: 12-level deep H: 1-level deep
VD[01:00]	GPIOA, GPIOC	FSB Frequency	LL: 100 MHz LH: 133 MHz HL: 200 MHz HH: Auto Mode (166 MHz can be obtained in this mode)

Note:
VD[07:00] are sampled during system initialization; the actual signals are located on the South Bridge chip.

REGISTER OVERVIEW

In the register descriptions, column "Default" indicates the power-on default value of register bit(s), while column "Attribute" indicates access type of register bit.

Abbreviation

Read / Write Attributes: read / write attributes may be used together to specify combined attributes

- **RO:** Read Only.
- **RZ:** Read as Zero.
- **R1:** Read as 1.
- **WO:** Write Only. (register value cannot be read by the software)
- **IW:** Ignore Write.
- **MW:** Must Write back what is read.
- **XW:** Backdoor Write.
- **RW:** Read / Write.
- **RW1:** Write Once then Read Only after that.
- **RW1C:** Read / Write of "1" clears bit to zero.
- **RsvdP**: Reserved. Must do a read-modify-write to preserve the bit values.
- **RsvdZ**: Reserved. Must write 0's.
- **RSM**: Bits are in resume-well.

Sticky Attributes: adding a "S" in tail to indicate a sticky register, which means that register will not be set or altered by hot reset.
Ex. RWS: Sticky-Read/Write. **ROS**: Sticky-Read Only. **RW1CS**: Sticky-Write-1-to-Clear.

Default Value Definitions

- **Dip**: means the default value is set by dip switch or strapping.
- **HwInit**: Hardware initialized; bit default value is set by hardware.

PCI Device & Function Definitions

To specifically identify a PCI function, the following abbreviations will be applied in subsequent sections.

D0F0: Device 0, Function 0 – Host Control

D0F1: Device 0, Function 1 – Error Reporting

D0F2: Device 0, Function 2 – Host Bus Control

D0F3: Device 0, Function 3 – DRAM Bus Control

D0F4: Device 0, Function 4 – Power Management Control

D0F5: Device 0, Function 5 – APIC and Central Traffic Control

D0F6: Device 0, Function 6 – Scratch Registers

D0F7: Device 0, Function 7 – V-Link Control

D1F0: Device 1, Function 0 – PCI-to-PCI Bridge – PCI2

D2F0: Device 2, Function 0 – PCI-to-PCI Bridge – PCI Express Root Port G

D3F0: Device 3, Function 0 – PCI-to-PCI Bridge – PCI Express Root Port 0

PCI Express Port & Register Block Definitions

PEG: PCI Express Port G

PE0: PCI Express Port 0

RCRB: PCI Express Root Complex Register Block

Miscellaneous I/O

I/O Port Address: 22h
PCI Arbiter Disable **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RO	0	**Reserved**
0	RW	0	**PCI Arbiter Control** 0: Enable PCI1 Bus Arbiter (arbiter will respond to REQ# assertion) 1: Disable PCI1 Bus Arbiter (arbiter will not respond to PCI-1 REQ# and PREQ# assertion)

PCI Configuration Space I/O

All north bridge's PCI space registers are addressed via the following configuration mechanism:

Mechanism #1

These ports respond only to double-word accesses. Byte or word accesses will be passed on unchanged.

I/O Port Address: CFB-CF8h
PCI Configuration Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RW	0	**Configuration Space Enable** 0: Disabled 1: Convert configuration data port writes to configuration cycles on the PCI bus
30:24	RO	0	**Reserved** (always reads 0)
23:16	RW	0	**PCI Bus Number** Used to choose a specific PCI bus in the system
15:11	RW	0	**Device Number** Used to choose a specific device in the system
10:8	RW	0	**Function Number** Used to choose a specific function if the selected device supports multiple functions
7:2	RW	0	**Register Number (also called the "Offset")** Used to select a specific DWORD in the configuration space
1:0	RW	0	**Fixed** (always reads 0)

I/O Port Address: CFF-CFCh
PCI Configuration Data **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**PCI Configuration Data**

Note: Refer to PCI Bus Specification Version 2.3 for further details on operation of the above configuration registers.

REGISTER DESCRIPTIONS

Device 0 Function 0 (D0F0): Host Controller

Device 0 Function 0, a host controller, is connected to the PCI bus through AD11 as the IDSEL.
All registers are located in PCI configuration space and should be programmed using PCI configuration mechanism 1 through I/O registers CF8 / CFC with bus number 0, device number 0 and function number 0.

Header Registers (0-3Fh)

Offset Address: 1-0h (D0F0)

Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**VIA Technologies ID Code**

Offset Address: 3-2h (D0F0)

Device ID **Default Value: 0364h**

Bit	Attribute	Default	Description
15:0	RO	0364h	**Device ID**

Offset Address: 5-4h (D0F0)

PCI Command **Default Value: 0006h**

Bit	Attribute	Default	Description
15:10	RO	0	**Reserved**
9	RO	0	**Fast Back-to-Back Cycle Enable** Hardwired to 0. (Disable)
8	RO	0	**SERR# Enable** Hardwired to 0 (Not supported)
7	RO	0	**Address / Data Stepping** Hardwired to 0 (Not supported)
6	RO/RW	0	**Parity Checking** 0: Ignore parity errors 1: Perform parity check and take normal action on detected parity errors When D0F7 RxA0[1] = 0, D0F0 Rx04[6] is RO. When D0F7 RxA0[1] = 1, D0F0 Rx04[6] is RW.
5	RO	0	**VGA Palette Snooping** Hardwired to 0 (Not implemented)
4	RO	0	**Memory Write and Invalidate** Hardwired to 0 (Not supported)
3	RO	0	**Respond To Special Cycle** Hardwired to 0 (Does not monitor special cycles)
2	RO	1b	**PCI Master Function** Hardwired to 1 (May behave as a bus master)
1	RO	1b	**Memory Space Access** Hardwired to 1 (Responds to memory space access)
0	RO	0	**I/O Space Access** Hardwired to 0 (Does not respond to I/O space)

Offset Address: 7-6h (D0F0)
PCI Status **Default Value: 0210h**

Bit	Attribute	Default	Description
15	RW1C	0	**Detect Parity Error** 0: No parity error detected 1: Error detected in either address or data phase
14	RO	0	**Signaled System Error (SERR#)**
13	RO/RW1C	0	**Set when terminated with Master-Abort, except special cycle** 0: No abort received 1: Transaction aborted by the master
12	RW1C	0	**Set when received a Target-Abort** 0: No abort received 1: Transaction aborted by the target
11	RO	0	**Set when signaled a Target-Abort** NB never signals Target Abort
10:9	RO	01b	**DEVSEL# Timing** 00: Fast 01: Medium 10: Slow 11: Reserved
8	RW1C	0	**Set when set or observed SERR# and Parity Error** (See D0F0 Rx4[6] for details) 0: Disable 1: Enable
7	RO	0	**Capable of Accepting fast back-to-back as a target** Hardwired to 0 (Not implemented)
6	RO	0	**User Definable Features** Hardwired to 0
5	RO	0	**66 MHz Capable** Hardwired to 0 (Not implemented)
4	RO	1b	**Support New Capability List**
3:0	RO	0	**Reserved**

Offset Address: 8h (D0F0)
Revision ID **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Revision Code**

Offset Address: 0B-9h (D0F0)
Class Code **Default Value: 06 0000h**

Bit	Attribute	Default	Description
23:0	RO	060000h	**Class Code**

Offset Address: 0Ch (D0F0)
Cache Line Size **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Cache Line Size**

Offset Address: 0Dh (D0F0)
PCI Master Latency Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RW	0	**PCI Bus Time Slice for CPU as a Master** (in unit of PCI clocks)
2:0	RO	0	**Reserved** D0F0 Rx0D[2:1] is programmable; however, it's read as 0

Offset Address: 0Eh (D0F0)
Header Type **Default Value: 00 or 80h**

Bit	Attribute	Default	Description
7:0	RO	00 or 80h	**Header Type** It could be 80h when D0F0 Rx4F[0] = 1

Offset Address: 0Fh (D0F0)
Built In Self Test (BIST) **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**BIST Support** Hardwired to 0 (Not supported)
6:0	RO	0	**Reserved**

Offset Address: 13-10h (D0F0)
Graphic Aperture Base Configuration **Default Value: 0000 0008h**

Bit	Attribute	Default	Description
31:22	RW	0	**Programmable Base Address** These bits behave as if hardwired to 0 if D0F0 Rx94[11:0] is set to 0. See the following Graphics Aperture Base Address Table for details. (Note: this range is defined as prefetchable)
21:4	RO	0	**Reserved** Hardwired to 0
3	RO	1b	**Prefetchable**
2:1	RO	0	**Type** Indicate that the address range is in the 32-bit address space
0	RO	0	**Memory Space** Indicates that the address range is in the memory address space.

Table 5. Graphics Aperture Base Address Table

Aperture Base Rx10[31:22]	31	30	29	28			27	26	25	24	23	22	Aperture Size
Aperture Size Rx94[11:0]	11	10	9	8	7	6	5	4	3	2	1	0	
	RW	RW	RW	RW	0	0	RW	RW	RW	RW	RW	RW	4M
	RW	RW	RW	RW	0	0	RW	RW	RW	RW	RW	0	8M
	RW	RW	RW	RW	0	0	RW	RW	RW	RW	0	0	16M
	RW	RW	RW	RW	0	0	RW	RW	RW	0	0	0	32M
	RW	RW	RW	RW	0	0	RW	RW	0	0	0	0	64M
	RW	RW	RW	RW	0	0	RW	0	0	0	0	0	128M
	RW	RW	RW	RW	0	0	0	0	0	0	0	0	256M
	RW	RW	RW	0	0	0	0	0	0	0	0	0	512M
	RW	RW	0	0	0	0	0	0	0	0	0	0	1G
	RW	0	0	0	0	0	0	0	0	0	0	0	2G –Max Size
	0	0	0	0	0	0	0	0	0	0	0	0	4G

Offset Address: 2D-2Ch (D0F0)
Subsystem Vendor ID **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW1	0	**Subsystem Vendor ID**

Offset Address: 2F-2Eh (D0F0)
Subsystem ID **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW1	0	**Subsystem ID**

Offset Address: 33-30h (D0F0) - Reserved

Offset Address: 34h (D0F0)
Capability Pointer **Default Value: 80h**

Bit	Attribute	Default	Description
7:0	RO	80h	**AGP Capability List Pointer** An offset address from the start of the configuration space See the following Rx34 Capability Pointer Table for details.

Table 6. AGP Capability Pointer

RX34	RX81	RX51	
80	51	NULL	RX34 -> RX81 AGP/AGP8X -> RX51 PMU ->NULL

Offset Address: 3F-35h (D0F0) – Reserved

AGP4X/AGP8X Compensation Circuits (40-49h)

Offset Address: 40h (D0F0)
AGP Pad Compensation Control / Status **Default Value: 80h**

Bit	Attribute	Default	Description
7	RW	1b	**AGP4X Strobe's Reference Voltage** 0: Strobe signals do not use AGPVREF as input reference voltage (i.e. STB VREF is STB# and vise versa). 1: Strobe signals use AGPVREF as input reference voltage. (Note: This bit is valid only in 4x and 8x mode. Otherwise always use AGPVERF as strobe signals)
6	RW	0	**AGP4X Strobe and GD Pad Driving Strength Control** 0: Driving strength is set to compensation circuit defaults 1: Driving strength is controlled by Rx41[7:0]
5:3	RO	0	**AGP Compensation Circuit N Control Output**
2:0	RO	0	**AGP Compensation Circuit P Control Output**

Offset Address: 41h (D0F0)
AGP Driving Strength Control **Default Value: 63h**

Bit	Attribute	Default	Description
7:4	RW	6h	**AGP Output Buffer Driving Strength N Control**
3:0	RW	3h	**AGP Output Buffer Driving Strength P Control**

Offset Address: 49-42h (D0F0) – Reserved

Miscellaneous Control (4A-4Fh)

Offset Address: 4C-4Ah (D0F0) – Reserved

Offset Address: 4Dh (D0F0)
AGP Capability Header Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RO	0	**Reserved**
0	RW	0	**Enable AGP Header Status Register Write** 0: Disable (Status registers in the AGP header cannot be modified) 1: Enable (Status registers in the AGP header can be modified)

Offset Address: 4Eh (D0F0) – Reserved

Offset Address: 4Fh (D0F0)
Multiple Function Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RO	0	**Reserved**
0	RW	0	**Multi-Function Support** 0: Disable. Functions 1, 2, 3, 4, 7 cannot be accessed, and the value returned will be FFFF FFFFh when accessed 1: Enable. This bit's setting will be reflected on D0F0 Rx0E[7]

AGP Extended Power Management Control (50–57h)

Offset Address: 50h (D0F0)
Capability ID **Default Value: 01h**

Bit	Attribute	Default	Description
7:0	RO	01h	**Capability ID**

Offset Address: 51h (D0F0)
Next Pointer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Next Pointer**

Offset Address: 52h (D0F0)
Power Management Capabilities **Default Value: 02h**

Bit	Attribute	Default	Description
7:0	RO	02h	**Power Management Capabilities**

Offset Address: 53h (D0F0)
Power Management Capabilities **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Power Management Capabilities**

Offset Address: 54h (D0F0)
Power Management Control / Status **Default Value: 0nh**

Bit	Attribute	Default	Description
7:2	RO	0	**Reserved**
1:0	RW	n	**Power State** 00: D0 11: D3 Hot

Offset Address: 55h (D0F0)
Power Management Status **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Power Management Status**

Offset Address: 56h (D0F0)
PCI to PCI Bridge Support Extensions **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**PCI to PCI Bridge Support Extensions**

Offset Address: 57h (D0F0)
Power Management Data **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Power Management Data**

Offset Address: 7F-58h (D0F0) – Reserved

AGP 3.0 Configuration (80–A3h)

Offset Address: CAPPTR (D0F0_83-80h)
Capability Pointer **Default Value: 0035 5002h**

Bit	Attribute	Default	Description
31:24	RZ	0	**Always Return 0 (write no effect)**
23:20	R-IW	3h	**Major Revision**
19:16	R-IW	0h 5h	**Minor Revision** The value of D0F0 Rx80[19:16] is determined by Rx4D[3] to define either 0000b or 0101b.
15:8	R-IW	50h	**Pointer to Next Item**
7:0	R-IW	02h	**Capability ID**

Offset Address: CAPPTR + 04h (D0F0_87-84h)
AGP Status **Default Value: 0700 020nh**

Bit	Attribute	Default	Description
31:24	R-XW	07h	**Max # of AGP Command Requests**
23-18	RZ-XW	0	**Reserved**
17	RZ-XW	0	**Isochronous Transaction** 0: Isochronous transaction is not supported 1: Supports Isochronous transaction
16	RZ-XW	0	**Reserved** (for future 64-bit AGP)
15:13	RZ-XW	0	**Optimum Asynchronous Request Size** Suggested setting is 010b or 2^(2+4) = 64 bytes for 8QW access
12:10	RZ-XW	000b	**Calibrating Cycle** 000: 4ms 001: 16ms 010: 64ms 011: 256ms Valid when bit 3 is 1.
9	R1-XW	1b	**Reserved**
8	RZ-XW	0	**Coherent Support** Not implemented
7	R-XW	0	**64-bit GART Entries** Support 32-bit GART entry only
6	R-XW	0	**Host GART Translation** 0: Support host GART translation 1: Does not support host GART translation
5	R-XW	0	**Over 4GB Support** – not implemented
4	R-XW	0	**Reserved**
3	R-XW	0	**AGP 3.0 Detected** 0: AGP 2.0 Mode 1: AGP 3.0 Mode
2:0	R-XW	011b 111b	If bit 3 is 1, the default value is 011: supports 4X and 8X data transfer rate. If bit 3 is 0, the default value is 111: supports 1X, 2X and 4X data transfer rate.

Offset Address: CAPPTR + 08h (D0F0_8B-88h)

AGP Command **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RZ-IW	0	**Max # of AGP Command Requests**
23:17	RZ-IW	0	**Reserved**
16	RZ-MW	0	**Reserved**
15:13	RZ-IW	0	**Reserved for Master Devices**
12:10	RW	0	**Calibrating Cycle** Set if D0F0 Rx84[3] is 1. 000: 4 ms 001: 16 ms 010: 64 ms 011: 256 ms
9	RW	0	**SBA Enable** 0: Disable 1: Enable
8	RW	0	**AGP Enable** 0: Disable 1: Enable
7	RW	0	**64-Bit GART** Not supported
6	RZ-MW	0	**Reserved**
5	RW	0	**Over 4G Support** 0: Disable 1: Enable
4	RW	0	**Fast Write Enable** 0: Disable 1: Enable
3	RZ-MW	0	**Reserved**
2:0	RW	0	**AGP Data Transfer Rate** If D0F0 Rx84[3] = 1 001: 4X data transfer rate 010: 8X data transfer rate If D0F0 Rx84[3] = 0 001: 1X data transfer rate 010: 2X data transfer rate 100: 4X data transfer rate

Offset Address: CAPPTR + 0Ch: (D0F0_8F-8Ch)

AGP Isochronous Status **Default Value: 0000 0000h**

This register can only be accessed if D0F0 Rx86[2] is set. Otherwise, all registers are RZ.

Bit	Attribute	Default	Description
31:24	RZ-IW	0	**Reserved**
23:16	R-IW	0	**Maximum Bandwidth (in unit of 32 bytes)** Shared by both asynchronous and isochronous transactions
15:8	R-IW	0	**Maximum Number of Isochronous Transactions in a Single Isochronous Period**
7:6	R-IW	00b	**Isochronous Payload Size Supported** 00: 32,64,128,256 bytes 01: 64,128,256 bytes 10: 128,256 bytes 11: 256 bytes
5:3	R-IW	0	**Isochronous Data Transfer Maximum Latency (in unit of 1 us)**
2	RZ-IW	0	**Reserved**
1:0	RW1C	00b	**Isochronous Error Code** 00: No error 01: Isoch Request Overflow 1x: Reserved

Offset Address: CAPPTR + 10h (D0F0_93-90h)

AGP Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:10	RZ	0	**Reserved**
9	RW	0	**Disable Calibration Cycle**
8	RW	0	**Enable AGP Aperture (Enable CPU/PMSTR GART Access)** This register controls the reading of D0F0 Rx13-10.
7	RW	0	**GTLB Enable** When set to 0, GART TLB entries are invalidated. All AGP aperture accesses need to fetch translation table first.
6:0	RZ	0	**Reserved**

Offset Address: CAPPTR + 14h (D0F0_97-94h)

AGP Aperture Size **Default Value: 0001 0F00h**

Bit	Attribute	Default	Description
31:28	RW	0	**Aperture Page Size Select** The page size is determined by the formula: 2^[n+12] Default 0000b, only 4KB is supported.
27	RZ	0	**Reserved**
26:16	R-IW	01h	**Page Size Supported** If bit N is 1, which indicates support of page size of (2^(N+12)). Currently only 4K page size is supported.
15:12	RZ	0	**Reserved**
11:0	RW	F00h	**Aperture Size – Default size is 256MB** Refer to Aperture Size table for detailed setting (Maximum aperture size: 2GB) D0F0 Rx97-94[n] =0 forces APBASE[22+n] to 0 when 0 <= n <= 5 D0F0 Rx97-94[n] =0 forces APBASE[22+n-2] to 0 when 8 <= n <=11 D0F0 Rx97-94[n] =1 allows APBASE[22+n] to be Read/Write-able. Bit 11 is hardwired to 1 and bit [7:6] are hardwired to 00. Support maximum 2G Aperture size When D0F0 Rx84[3] is 0, it only supports 4MB ~ 256MB.

Table 7. Aperture Size

Aperture Size \ D0F0 Rx94[11:0]	11	10	9	8	7	6	5	4	3	2	1	0
4MB	1	1	1	1	0	0	1	1	1	1	1	1
8MB	1	1	1	1	0	0	1	1	1	1	1	0
16MB	1	1	1	1	0	0	1	1	1	1	0	0
32MB	1	1	1	1	0	0	1	1	1	0	0	0
64M	1	1	1	1	0	0	1	1	0	0	0	0
128M	1	1	1	1	0	0	1	0	0	0	0	0
256M	1	1	1	1	0	0	0	0	0	0	0	0
512M	1	1	1	0	0	0	0	0	0	0	0	0
1G	1	1	0	0	0	0	0	0	0	0	0	0
2G (Max Aperture Size)	1	0	0	0	0	0	0	0	0	0	0	0
4G	0	0	0	0	0	0	0	0	0	0	0	0

Offset Address: CAPPTR + 18h (D0F0_9B-98h)

AGP GART Table Pointer **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:12	RW	0	**GART Table Base Address [31:12]**
11:0	RZ	0	**Reserved**

Offset Address: CAPPTR + 1Ch (D0F0_9F-9Ch)

AGP GART Table Pointer High **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Base Address [63:32]** Since OVER4G is not supported, OS should program this register to zero. This register is ignored.

Offset Address: CAPPTR + 20h (D0F0_A3-A0h)

AGP Isochronous Command **Default Value: 0000 0000h**

This register is not accessible since the ISOCH bit is cleared. Read will be return all zeros, write has no effect.

Bit	Attribute	Default	Description
31:8	RZ-IW	0	**Reserved**
7:6	RW	0	**Isochronous Payload Size** Default is D0F0 Rx CAPPTR + 0C [7:6](Rx8C)
5:0	RZ-IW	0	**Reserved**

Offset Address: AF-A4h (D0F0) – Reserved

AGP Enhanced Control (B0–BEh)

Offset Address: B8-B0h (D0F0) – Reserved

Offset Address: B9h (D0F0)
AGP Mixed Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**FIFO Depth Control** 0: Normal FIFO Depth - 64 QW, isochronous FIFO Depth - 32 QW 1: Normal FIFO Depth - 96 QW, isochronous FIFO Depth - 0 QW
6:0	RO	0	**Reserved**

Offset Address: BB-BAh (D0F0) – Reserved

Offset Address: BCh (D0F0)
AGP Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6	RW	0	**AGP Read Synchronization** 0: Disable 1: Enable
5	RW	0	**AGP Read Snoop DRAM Post-Write Buffer** 0: Disable 1: Enable
4:2	RO	0	**Reserved**
1	RW	0	**GGNT Parking Policy** 0: Non-parking GGNT; GGNT is de-asserted after GFRAME or PIPE assertion. 1: Parking GGNT; after the assertion of GFRAME or PIPE, GGNT is kept asserted till GREQ de-asserted or timeout.
0	RO	0	**Reserved**

Offset Address: BDh (D0F0) – Reserved

Offset Address: BEh (D0F0)
AGP Miscellaneous Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RO	0	**Reserved**
0	RW	0	**CPU GART Read and AGP GART Write Coherency Enable** 0: Disable 1: Enable

Offset Address: FF-BFh (D0F0) – Reserved

Device 0 Function 1 (D0F1): Error Reporting

Header Registers (0-3Fh)

Offset Address: 1-0h (D0F1)
Vendor ID — **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**Vendor ID**

Offset Address: 3-2h (D0F1)
Device ID — **Default Value: 1364h**

Bit	Attribute	Default	Description
15:0	RO	1364h	**Device ID**

Offset Address: 5-4h (D0F1)
PCI Command — **Default Value: 0006h**

Bit	Attribute	Default	Description
15:0	RO	0006h	**PCI Command**

Offset Address: 7-6h (D0F1)
PCI Status — **Default Value: 0200h**

Bit	Attribute	Default	Description
15:0	RO	0200h	**PCI Status**

Offset Address: 8h (D0F1)
Revision ID — **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Revision ID**

Offset Address: 0B-9h (D0F1)
Class Code — **Default Value: 06 0000h**

Bit	Attribute	Default	Description
23:0	RO	060000h	**Class Code**

Offset Address: 0Ch (D0F1) – Reserved

Offset Address: 0Dh (D0F1)
Latency Timer — **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Latency Timer**

Offset Address: 0Eh (D0F1)
Header Type — **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Header Type**

Offset Address: 0Fh (D0F1)
BIST **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**BIST**

Offset Address: 13-10h (D0F1) – Reserved

Offset Address: 2D-2C (D0F1)
Subsystem Vendor ID **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW1	0	**Subsystem Vendor ID**

Offset Address: 2F-2E (D0F1)
Subsystem ID **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW1	0	**Subsystem ID**

Offset Address: 33-30 (D0F1) – Reserved

Offset Address: 34 (D0F1)
Capability Pointer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Capability Pointer - Byte offset into configuration space to capability list**

Offset Address: 3F-35 (D0F1) – Reserved

Offset Address: 4F-40h (D0F1) – Reserved

V-Link Error Report (50-5Fh)

Offset Address: 57-50h (D0F1) – Reserved

Offset Address: 58h (D0F1)
V-Link Error Command **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Parity Error / SERR Report Through NMI** 0: Disable 1: Enable
6	RW	0	**Parity Error / SERR Report Through V-Link to SB** 0: Disable 1: Enable
5:0	RO	0	**Reserved**

Offset Address: 5F-59h (D0F1) – Reserved

Host Bus Error Report (60-6Fh)

Offset Address: 67-60h (D0F1) – Reserved

Offset Address: 68h (D0F1)

Host Parity Command **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Host Address Parity Generation and Check (AP[1:0]#)** 0: Disable 1: Enable
6	RO	0	**Reserved**
5	RW	0	**Host Response Parity Generation (RSP#)** 0: Disable 1: Enable
4	RO	0	**Reserved**
3	RW	0	**Parity Test Mode** 0: Disable (normal mode) 1: Enable (invert the parity bit)
2:0	RO	0	**Reserved**

Offset Address: 6F-69h (D0F1) – Reserved

Offset Address: DF-70h (D0F1) – Reserved

AGP / PCI2 Non Standard Error Reporting (E0-FFh)

Offset Address: E0h (D0F1) – Reserved

Offset Address: E1h (D0F1)

AGP / PCI2 Error Status **Default Value: 00h**

Bit	Attribute	Default	Description
7:2	RO	0	**Reserved**
1:0	RO	0	**Isochronous Error Code (see D0F0 Rx8C[1:0])**

Offset Address: E7-E2h (D0F1) – Reserved

Offset Address: E8h (D0F1)

AGP / PCI2 Error Report Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4	RW	0	**Parity Error Report for AGP Data Parity Error** 0: Disable 1: Enable
3:0	RO	0	**Reserved**

Offset Address: FF-E9h (D0F1) – Reserved

Device 0 Function 2 (D0F2): Host Bus Control

Header Registers (0-3Fh)

Offset Address: 1-0h (D0F2)
Vendor ID — **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**Vendor ID**

Offset Address: 3-2h (D0F2)
Device ID — **Default Value: 2364h**

Bit	Attribute	Default	Description
15:0	RO	2364h	**Device ID**

Offset Address: 5-4h (D0F2)
PCI Command — **Default Value: 0006h**

Bit	Attribute	Default	Description
15:0	RO	0006h	**PCI Command**

Offset Address: 7-6h (D0F2)
PCI Status — **Default Value: 0200h**

Bit	Attribute	Default	Description
15:0	RO	0200h	**PCI Status**

Offset Address: 8h (D0F2)
Revision ID — **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Revision ID**

Offset Address: 0B-9h (D0F2)
Class Code — **Default Value: 06 0000h**

Bit	Attribute	Default	Description
23:0	RO	060000h	**Class Code**

Offset Address: 0Ch (D0F2)
Cache Line Size — **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Cache Line Size**

Offset Address: 0Dh (D0F2)
Latency Timer — **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Latency Timer**

Offset Address: 0Eh (D0F2)
Header Type **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Header Type**

Offset Address: 0Fh (D0F2)
Built In Self Test (BIST) **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**BIST**

Offset Address: 13-10h (D0F2) – Reserved

Offset Address: 2D-2Ch (D0F2)
Subsystem Vendor ID **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW1	0	**Subsystem Vendor ID**

Offset Address: 2F-2Eh (D0F2)
Subsystem ID **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW1	0	**Subsystem ID**

Offset Address: 33-30h (D0F2) – Reserved

Offset Address: 34h (D0F2)
Capability Pointer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Capability Pointer - Byte offset into configuration space to capability list**

Offset Address: 3F-35h (D0F2) – Reserved

Offset Address: 4F-40h (D0F2) – Reserved

Host CPU Control (50-5Fh)

Offset Address: 50h (D0F2)

Request Phase Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	dip	**IOQ (In-Order Queue) Depth** 0: 1-level 1: 12-level Default sets from the inverse of the VD2 signal during system initialization. For strap pin information, check the Strap Pin table for details.
6	RO	dip	**Dual CPU** 0: Single CPU 1: Dual CPU Default value is set by strapping VD7.
5	RO	0	**Reserved** Must set to zero.
4:0	RW	0	**Dynamic Defer Snoop Stall Count** Value for the Defer Snoop Stall Counter. The timer starts counting at the beginning of the snoop phase of C2P cycle; it increases one for every 2 HCLKs. If the C2P cycle is pending when the timer expired, and there are pending ADS, a Defer/Retry response will be replied to the host. For medium decoding PCI slave device; the optimal value for bit0-4 is 8.

Table 8. Dynamic Defer Snoop Stall Table

Timer Expired	New Pending ADS	PCI Completion	Action
No	-	No	Snoop stall till PCI complete
No	-	Yes	Normal Data Response
Yes	No	No	Snoop stall till either arrival of new pending ADS or PCI complete
Yes	No	Yes	Normal Data Response
Yes	Yes	No	Defer/Retry Response
Yes	Yes	Yes	Normal Data Response

Offset Address: 51h (D0F2)

CPU Interface Control 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Fast Ready for CPU Memory Read Cycle** 0: Disable, wait until all 8QWs are received before DRDY assertion 1: Enable, DRDY assertion timing is set up through Rx60-67
6	RW	0	**Read Around Write** 0: Disable 1: Enable
5	RW	0	**Host Controller DRAM Request Queue Control (DRQCTL)** 0: Disable pipelined DRQCTL 1: Enable pipelined DRQCTL
4	RW	0	**CPU to PCI Read Defer** 0: Disable 1: Enable
3	RW	0	**2 Defer/ Retry Entries** 0: Disable 1: Enable
2	RW	0	**2 Defer / Retry Entries Sharing** 0: One entry for each processor 1: Each entry is shared by the two processors
1	RW	0	**PCI Master Pipeline Access** 0: Disable 1: Enable
0	RO	0	**Reserved**

Offset Address: 52h (D0F2)
CPU Interface Control 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**CPU Read / Write DRAM 0WS for Back-to-Back Pipeline Access** 0: Disable 1: Enable
6	RW	0	**HREQ (Host Continuous DRAM Ownership) / HPRI (Host High Priority DRAM Request) Assertion to DRAM Controller** 0: Disable 1: Enable assertion of HREQ / HPRI to DRAM controller for efficient memory utilization / faster memory data access.
5	RO	0	**AGTL+ Pullup Enable** 0: Disable 1: Enable Default sets from the inverse of the VD3 signal during system initialization. For strap pin information, check the Strap Pin table for details.
4	RO	0	**Reserved**
3	RW	0	**Write Retire Policy After 2 Writes** 0: Disable 1: Enable
2	RW	0	**2 Level Defer Queue With Lock Cycle** 0: Disable 1: Enable
1	RW	0	**Consecutive Speculative Read** 0: Disable 1: Enable
0	RW	0	**Speculative Read** 0: Disable 1: Enable

Offset Address: 53h (D0F2)
Arbitration **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Host Occupancy Timer** (in unit of 4 HCLKs) Host Occupancy timer guarantees a time slot of Rx53[7:4]* 4 HCLK for pipelined CPU's ADS.
3:0	RW	0	**Master Occupancy Timer** (in unit of 4 HCLKs) Master Occupancy timer guarantees a time slot of Rx53[3:0]*4 HCLK for pending master requests.

Offset Address: 54h (D0F2)
Miscellaneous Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	000b	**CPU FSB Frequency (Powell)** 000: 100MHz 001: 133MHz 010: 166MHz 011: 200MHz 100: Reserved 101: Reserved
4	RW	0	**Burst 8QW Host to Memory Access** 0: Disable 1: Enable This bit must be set to 1 in 128-bit DRAM mode.
3	RW	0	**Host-Memory DRDY Assertion Adjustment** 0: Normal mode, no adjustment 1: Special mode (1T earlier) This bit's setting should follow Rx60~Rx67 settings. Check Rx55[1] for details of DRDY assertion adjustment.
2	RW	0	**PCI Master 8QW Memory Access** 0: Disable 1: Enable
1	RW	0	**Memory-to-Host Conversion Circuit** 0: Sync 1T in certain clock phases 1: Transparent mode
0	RO	0	**Reserved**

Offset Address: 55h (D0F2)
Miscellaneous Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Warm CPU Reset (CPURST#) Trigger** Write 0 → 1 transition will trigger warm CPURST# Firmware will have to reset this bit to "0" before trigger another CPURST#.
6	RO	0	**Reserved**
5	RW	0	**Early Read Data Ready Signal for Host Interface DRDY table** 0: 2T early 1: 3T early
4:3	RO	0	**Reserved**
2	RW	0	**Medium Threshold for Write Policy** 0: Disable medium threshold 1: Add a medium threshold, defined by Rx56, in Write Queue to enable earlier memory write. See Rx56[7:4] for details.
1	RW	0	**Host-Memory DRDY Assertion 2T Adjustment** 0: 2T early 1: 2T late
0	RO	0	**Reserved**

Offset Address: 56h (D0F2)
Write Policy **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Medium Threshold for Write Policy**
3	RO	0	**Reserved**
2	RW	0	**TL Request 1T Pipeline** 0: Disable 1: Enable
1	RO	dip	**V4-Lite Capability** 0: Disable 1: Enable Default value is set by strapping VD[5].
0	RO	dip	**V4 Capability** 0: Disable 1: Enable Default value is set by strapping VD[6].

Offset Address: 57h (D0F2)
Miscellaneous Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	000b	**DRAM Bus Frequency** 000: 100MHz 001: 133MHz 010: 166MHz 011: 200MHz 100: 266MHz 101: 333MHz
4	RW	0	**Enable Fast TRDY Feature of V4 Protocol** 0: Disable 1: Enable You can only turn on this bit in V4 mode (excluding V4-lite), enable fast TRDY feature of V4 protocol. Suggest set to 1.
3	RW	0	**Insert Wait State for First Write Data** 0: Disable 1: Enable You can only turn on this when bit 4 = 1. When CPU operates on very low speed, it may insert wait state for 1st write data, chipset needs to turn on this bit to support this case.
2	RW	0	**DPWR# Assertion Policy** 0: Always assert DPWR# (no gating) 1: Dynamic DPWR# assertion (Dynamic gating)
1	RW	0	**DPWR# Assertion Control** (Activate if bit 2 is enabled) 0: Assert DPWR# for both read / write cycles 1: Assert DPWR# for read / APIC write cycles
0	RW	0	**Enable Sync. DADS Mode** 0: Disable 1: Enable In Host / Memory Asynchronous mode, set this bit to 1. Keep this bit at 0 in synchronous mode for better performance.

Offset Address: 58h (D0F2) – Reserved

Offset Address: 59h (D0F2)
CPU Miscellaneous Control **Default Value: 40h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6	RO	1b	**Reserved**
5	RW	0	**Sync. Host Memory Request with Memory Clock (for Dynamic CKE)** 0: Disable (when the host clock rate is the same as the memory clock rate) 1: Enable (when the host clock rate is not the same as the memory clock rate)
4:3	RW	00	**P6IF Has High Priority Request** 0 X : Dynamic 1 0 : P6IF does not have high priority request 1 1 : P6IF always have high priority request
2	RO	0	**Automatic DRDY Table Adjustment for CPU Cycle and Master Cycle.**
1	RO	0	**Reserved**
0	RW	0	**Lowest-Priority IPI (Inter-Processor Interrupt) Support** 0: Disable 1: Enable

Offset Address: 5Ch (D0F2)
CPU Miscellaneous Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4	RW	0	**Enable Patching D11 from Reserved to Set When Logic Mode APIC**
3	RW	0	**APIC Redirection Hint Information Obtained From** 0: Address filed 1: Data field
2	RW	0	**APIC Destination Mode Information Obtained From** 0: Address field 1: Data field
1	RW	0	**APIC Cluster Mode Support** 0: Disable 1: Enable
0	RW	0	**Redirect Lowest Priority APIC Requests to CPU0** (i.e. CPU0 is treated as the lowest priority processor) 0: Disable 1: Enable

Offset Address: 5Dh (D0F2)
Write Policy **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Write Request High Threshold**
3:0	RW	0	**Write Request Low Threshold**

Table 9. CPU Write Request Policy

Rx51[6]	Rx52[3]	Rx5D[7:4]	Rx5D[3:0]	Write Policy
1	0	x	x	Will not handle write request until FIFO is full
1	1	4	2	Will start processing write request when write request count reaches Rx5D[7:4], and stop processing write request when write request count drops to Rx5D[3:0].

Offset Address: 5Eh (D0F2)
Bandwidth Timers **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Host Bandwidth Timer**
3:0	RW	0	**DRAM Bandwidth Timer**

Offset Address: 5Fh (D0F2)
CPU Miscellaneous Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6	RW	0	**Reorder Retry Queue Enable** 0: Retried CPU transaction always complete in order 1: Allow second entry of retried (IOW/MEMW) transaction to complete before first queued entry
5:4	RW	00b	**Warm CPU Reset (CPURST#) Duration Control** 00: 512us 01: 1024us 10: 1523us 11: 2048us
3	RW	0	**Pipeline APIC / Master Transaction** 0: APIC requests will not be pipelined with master requests. 1: APIC requests can be pipelined with normal master requests. This bit must be set to 0.
2	RW	0	**Host Bandwidth Restriction** 0: Disable 1: Enable Host Bandwidth Timer is set up by Rx5E[7:4].
1	RW	0	**DRAM Bandwidth Restriction** 0: Disable 1: Enable DRAM Bandwidth Timer is set up by Rx5E[3:0].
0	RW	0	**Enable Relaxed DBSY# CPU Timing Workaround** 0: Workaround disabled 1: Workaround enabled

Table 10. Host / DRAM Bandwidth Policy

Rx5F[2]	Rx5F[1]	Host / DRAM Bandwidth Setting Policy
0	0	Disable the new DRAM/Host Bandwidth Arbiter
0	1	Use the DRAM Bandwidth Timer only
1	0	Use the HOST Bandwidth Timer only
1	1	Dynamically toggles between the Host and Dram bandwidth timers. Both timers, Rx5E[7:4] and Rx5E[3:0] are used by the arbitration logic.

Host Interface DRDY Timing Control (60-6Fh)

Offset Address: 60h (D0F2)
Line DRDY Timing Control 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	0	**Read Line Phase 4 Wait State**
5:4	RW	0	**Read Line Phase 3 Wait State**
3:2	RW	0	**Read Line Phase 2 Wait State**
1:0	RW	0	**Read Line Phase 1 Wait State**

Offset Address: 61h (D0F2)
Line DRDY Timing Control 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	0	**Read Line Phase 8 Wait State**
5:4	RW	0	**Read Line Phase 7 Wait State**
3:2	RW	0	**Read Line Phase 6 Wait State**
1:0	RW	0	**Read Line Phase 5 Wait State**

Offset Address: 62h (D0F2)
Line DRDY Timing Control 3 **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3:2	RW	0	**Read Line Phase 10 Wait State**
1:0	RW	0	**Read Line Phase 9 Wait State**

Offset Address: 63h (D0F2)
QW DRDY Timing Control 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	0	**Read QW Phase 4 Wait State**
5:4	RW	0	**Read QW Phase 3 Wait State**
3:2	RW	0	**Read QW Phase 2 Wait State**
1:0	RW	0	**Read QW Phase 1 Wait State**

Offset Address: 64h (D0F2)
QW DRDY Timing Control 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	0	**Read QW Phase 8 Wait State**
5:4	RW	0	**Read QW Phase 7 Wait State**
3:2	RW	0	**Read QW Phase 6 Wait State**
1:0	RW	0	**Read QW Phase 5 Wait State**

Offset Address: 65h (D0F2)
QW DRDY Timing Control 3 **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3:2	RW	0	**Read QW Phase 10 Wait State**
1:0	RW	0	**Read QW Phase 9 Wait State**

Offset Address: 66h (D0F2)
Read Line Burst DRDY Timing Control 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Phase 8 Wait State**
6	RW	0	**Phase 7 Wait State**
5	RW	0	**Phase 6 Wait State**
4	RW	0	**Phase 5 Wait State**
3	RW	0	**Phase 4 Wait State**
2	RW	0	**Phase 3 Wait State**
1	RW	0	**Phase 2 Wait State**
0	RW	0	**Phase 1 Wait State**

Offset Address: 67h (D0F2)
Read Line Burst DRDY Timing Control 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Turn Off Unused Host Interface IO Pads in V4 Mode** 0: Disable 1: Enable When enabled, it will turn off unused pads (HA31, HA29~HA17, HREQ4~HREQ3) in V4 Mode. "Turn off IO pads" means that both input enable and output enable signals are de-asserted. When V4-Lite mode is on, pads HD63~HD32 are also turned off.
6	RW	0	**Trigger Method for Host IO Pads Activation** 0: Use BREQ0 to control (activate and inactivate) host IO pads. 1: Use ADS1 to control (activate and inactivate) host IO pads.
5	RW	0	**Phase 10 Wait State**
4	RW	0	**Phase 9 Wait State**
3:0	RO	0	**Reserved**

Offset Address: 68h (D0F2)
APIC CPU Priority 0 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Priority of CPU ID#0**

Offset Address: 69h (D0F2)
APIC CPU Priority 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Priority of CPU ID#1**

Offset Address: 6Ah (D0F2)
APIC CPU Priority 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Priority of CPU ID#2**

Offset Address: 6Bh (D0F2)
APIC CPU Priority 3 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Priority of CPU ID#3**

Offset Address: 6Ch (D0F2)
APIC CPU Priority 4 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Priority of CPU ID#4**

Offset Address: 6Dh (D0F2)
APIC CPU Priority 5 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Priority of CPU ID#5**

Offset Address: 6Eh (D0F2)
APIC CPU Priority 6 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Priority of CPU ID#6**

Offset Address: 6Fh (D0F2)
APIC CPU Priority 7 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Priority of CPU ID#7**

Host AGTL+ I/O Circuit (70–B3h)

Offset Address: 70h (D0F2)
Host Address Pad (2x) Pullup Driving **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6:4	RW	dip	**2X Address Strobe Pad Pullup Driving – (HADSTB1#, HADSTB0#)**
3	RO	0	**Reserved**
2:0	RW	dip	**2X Address Pad Pullup Driving – (HA[31:3], HREQ[4:0])**

Offset Address: 71h (D0F2)
Host Address Pad (2x) Pulldown Driving **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6:4	RW	dip	**2X Address Strobe Pad Pulldown Driving – (HADSTB1#, HADSTB0#)**
3	RO	0	**Reserved**
2:0	RW	dip	**2X Address Pad Pulldown Driving – (HA[31:3], HREQ[4:0])**

Offset Address: 72h (D0F2)
Host Data Pad (4x) Pullup Driving **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6:4	RW	dip	**4X Data Strobe Pad Pulldup Driving – (HDSTB[3:0]N#, HDSTB[3:0]P#)**
3	RO	0	**Reserved**
2:0	RW	dip	**4X Data Pad Pullup Driving – (D[63:0], DBI[3:0])**

Offset Address: 73h (D0F2)
Host Data (4x) Pulldown Driving **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6:4	RW	dip	**4X Data Strobe Pad Pulldown Driving – (HDSTB[3:0]N#, HDSTB[3:0]P#)**
3	RO	0	**Reserved**
2:0	RW	dip	**4X Data Pad Pulldown Driving – (D[63:0], DBI[3:0])**

Offset Address: 74h (D0F2)
Memory Interface Timing Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Control Non-posted Write Cycle Defer or Retry on Host Bus** 0 :Defer 1: Retry
6	RW	0	**Control if CPU's Special Cycle is Non-posted or Posted on Host Bus** 0 : Posted 1: Non-posted
5	RW	0	**HD[63:48], HD[31:16], DBI[3,1] Output Stagger Delay (1 ns)** 0: No delay 1: 1 ns delay
4	RW	0	**HA[31:17] Output Stagger Delay** 0: No delay 1: 1 ns delay
3:2	RW	00b	**HDSTB[3:0]N#, HDSTB[3:0]P# Extra Output Delay** 00: No delay 01: 150 ps 10: 300 ps 11: 450 ps
1:0	RW	00b	**HADSTB1#, HADSTB0# Extra Output Delay** 00: No delay 01: 150 ps 10: 300 ps 11: 450 ps

Offset Address: 75h (D0F2)
AGTL+ I/O Circuit **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RO	00b	**Reserved**
5	RW	0	**AGTL+ Slew Rate** 0: Disable 1: Enable
4:3	RO	0	**Reserved**
2	RW	0	**AGTL+ TR Function (always pullup) for STROBE** 0: Disable 1: Enable
1	RW	0	**AGTL+ TR Function (always pullup) for DATA** 0: Disable 1: Enable
0	RW	0	**AGTL+ Dynamic Compensation** 0: Disable 1: Enable

Offset Address: 76h (D0F2)
AGTL+ Compensation Status **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Auto-compensation Driving** 1: Enable Auto mode
6:4	RO	0	**AGTL+ Compensation Result**
3	RW	0	**AGTL+ POS Function** 1: Power-down AGTL+ input when idle
2	RO	0	**Reserved**
1	RW	0	**Disable DBI Function** 0: Enable DBI 1: Disable DBI (DBI always high including DBI double-check)
0	RW	0	**DBI Functional Mode** 0: Minimize data change count (through data comparison with previous data) 1: Minimize AGTL+ pulldown count

Offset Address: 77h (D0F2)
AGTL+ Auto Compensation Offset **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Address IO Pad Driving Offset to AGTL+ Compensation Result (Rx76[6:4])**
3:0	RW	0	**Data IO Pad Driving Offset to AGTL+ Compensation Result (Rx76[6:4])** Note: The actual driving to GTL pad is Rx76[6:4] + bit 7-4 or Rx76[6:4]+ bit 3-0. Bit 7-4/bit 3-0 can be either positive or negative offset; negative offset is represented in 2's complement, so the driving offset value ranges from –8 to +7.

Offset Address: 78h (D0F2)
Host FSB CKG Control 1 **Default Value: 55h**

Bit	Attribute	Default	Description
7:6	RW	01b	**CKG Falling-Time Control for Host Interface (S port)** 00: Default timing 01: Delay by 100 ps 10: Delay by 200 ps 11: Delay by 300 ps
5:4	RW	01b	**CKG Rising-Time Control for Host Interface (S port)** 00: Default timing 01: Delay by 100 ps 10: Delay by 200 ps 11: Delay by 300 ps
3:2	RW	01b	**CKG Falling-Time Control for Host Interface** 00: Default timing 01: Delay by 100 ps 10: Delay by 200 ps 11: Delay by 300 ps
1:0	RW	01b	**CKG Rising-Time Control for Host Interface** 00: Default timing 01: Delay by 100 ps 10: Delay by 200 ps 11: Delay by 300 ps

Offset Address: 79h (D0F2)

Address CKG Rising / Falling Time Control 1 **Default Value: 55h**

Bit	Attribute	Default	Description
7:6	RW	01b	**Output Address Delay Register of Group 0** 00: Td –300 ps 01: Td –150 ps 10: Td 11: Td + 0.150 ps Delay (Td) = 650 ps (min), 750 ps (typ), 850 ps (max) from CK to CKO0~CKO18, respectively
5:4	RW	01b	**Output Address Clock Delay Register of Group 0** 00: Td –300 ps 01: Td –150 ps 10: Td 11: Td + 150 ps Delay (Td) = 650 ps (min), 750 ps (typ), 850 ps (max) from CK to CKO0~CKO18, respectively
3:2	RW	01b	**Output Address Delay Register of Group 1** 00: Td –300 ps 01: Td –150 ps 10: Td 11: Td + 150 ps Delay (Td) = 650 ps (min), 750 ps (typ), 850 ps (max) from CK to CKO0~CKO18, respectively
1:0	RW	01b	**Output Address Clock Delay Register of Group 1** 00: Td –300 ps 01: Td –150 ps 10: Td 11: Td + 150 ps Delay (Td) = 650 ps (min), 750 ps (typ), 850 ps (max) from CK to CKO0~CKO18, respectively

Offset Address: 7Ah (D0F2)

Input Address Strobe Delay Control **Default Value: 24h**

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved**
5:3	RW	100b	**Input Address Strobe Delay for Group 0** The three bits finetune HASTB0 input delay with respect to address group0 data. Value 100b should let HASTB0 balance with address group0 data. Value larger than 100 will early HASTB0 about 100ps per scale. Value smaller than 100 will delay HASTB0 about 100ps per scale. 000 – delay(data) = delay(strobe) – 400 ps 001 – delay(data) = delay(strobe) – 300 ps 010 – delay(data) = delay(strobe) – 200 ps 011 – delay(data) = delay(strobe) –100 ps 100 – delay(data) = delay(strobe) 101 – delay(data) = delay(strobe) + 100 ps 110 – delay(data) = delay(strobe) + 200 ps 111 – delay(data) = delay(strobe) + 300 ps
2:0	RW	100b	**Input Address Strobe Delay for Group 1** The three bits finetune HASTB1 input delay with respect to address group1 data. Value 100b should let HASTB1 balance with address group1 data. Value larger than 100 will early HASTB1 about 100ps per scale. Value smaller than 100 will delay HASTB1 about 100ps per scale 000 – delay(data) = delay(strobe) – 400 ps 001 – delay(data) = delay(strobe) – 300 ps 010 – delay(data) = delay(strobe) – 200 ps 011 – delay(data) = delay(strobe) – 100 ps 100 – delay(data) = delay(strobe) 101 – delay(data) = delay(strobe) + 100 ps 110 – delay(data) = delay(strobe) + 200 ps 111 – delay(data) = delay(strobe) + 300 ps

Offset Address: 7Bh (D0F2)

Address CKG Rising / Falling Time Control 2 **Default Value: 55h**

Bit	Attribute	Default	Description
7:6	RW	01b	**Group 0 Address CKG Falling-Time Control** 00: Default timing 01: Delay by 100 ps 10: Delay by 200 ps 11: Delay by 300 ps
5:4	RW	01b	**Group 0 Address CKG Rising-Time Control** 00: Default timing 01: Delay by 100 ps 10: Delay by 200 ps 11: Delay by 300 ps
3:2	RW	01b	**Group 1 Address CKG Falling-Time Control** 00: Default timing 01: Delay by 100 ps 10: Delay by 200 ps 11: Delay by 300 ps
1:0	RW	01b	**Group 1 Address CKG Rising-Time Control** 00: Default timing 01: Delay by 100 ps 10: Delay by 200 ps 11: Delay by 300 ps

Offset Address: 7Ch (D0F2)

Address CKG Clock Rising / Falling Time Control **Default Value: 55h**

Bit	Attribute	Default	Description
7:6	RW	01b	**Group 0 Address Clock CKG Falling-Time Control** 00: Default timing 01: Delay by 100 ps 10: Delay by 200 ps 11: Delay by 300 ps
5:4	RW	01b	**Group 0 Address Clock CKG Rising-Time Control** 00: Default timing 01: Delay by 100 ps 10: Delay by 200 ps 11: Delay by 300 ps
3:2	RW	01b	**Group 1 Address CKG Falling-Time Control** 00: Default timing 01: Delay by 100 ps 10: Delay by 200 ps 11: Delay by 300 ps
1:0	RW	01b	**Group 1 Address CKG Rising-Time Control** 00: Default timing 01: Delay by 100 ps 10: Delay by 200 ps 11: Delay by 300 ps

Offset Address: 7Dh (D0F2)

Host Data Receiving Strobe Delay Control **Default Value: 90h**

Bit	Attribute	Default	Description
7:5	RW	100b	**Control Relative Delay between Data/Strobe Input Delay for HD[15:0]** 000 – delay(data) = delay(strobe) – 200 ps 001 – delay(data) = delay(strobe) – 150 ps 010 – delay(data) = delay(strobe) – 100 ps 011 – delay(data) = delay(strobe) – 50 ps 100 – delay(data) = delay(strobe) 101 – delay(data) = delay(strobe) + 50 ps 110 – delay(data) = delay(strobe) + 100 ps 111 – delay(data) = delay(strobe) + 150 ps
4:2	RW	100b	**Control Relative Delay between Data/Strobe Input Delay for HD[31:16]** 000 – delay(data) = delay(strobe) – 200 ps 001 – delay(data) = delay(strobe) – 150 ps 010 – delay(data) = delay(strobe) – 100 ps 011 – delay(data) = delay(strobe) – 50 ps 100 – delay(data) = delay(strobe) 101 – delay(data) = delay(strobe) + 50 ps 110 – delay(data) = delay(strobe) + 100 ps 111 – delay(data) = delay(strobe) + 150 ps
1	RO	0	**Reserved**
0	RW	0	**BREQ Parking Control** 0: BREQ0 always assert, better performance 1: BREQ0 CPU will dynamic assert / deassert BREQ0 signal

Offset Address: 7F-7Eh (D0F2) – Reserved

Offset Address: 80h (D0F2)
Host Data Receiving Strobe Delay Control **Default Value: 24h**

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved**
5:3	RW	100b	**Control Relative Delay between Data/Strobe Input Delay for HD[47:32]** 000 – delay(data) = delay(strobe) – 200 ps 001 – delay(data) = delay(strobe) – 150 ps 010 – delay(data) = delay(strobe) – 100 ps 011 – delay(data) = delay(strobe) – 50 ps 100 – delay(data) = delay(strobe) 101 – delay(data) = delay(strobe) + 50 ps 110 – delay(data) = delay(strobe) + 100 ps 111 – delay(data) = delay(strobe) + 150 ps
2:0	RW	100b	**Control Relative Delay between Data/Strobe Input Delay for HD[63:48]** 000 – delay(data) = delay(strobe) – 200 ps 001 – delay(data) = delay(strobe) – 150 ps 010 – delay(data) = delay(strobe) – 100 ps 011 – delay(data) = delay(strobe) – 50 ps 100 – delay(data) = delay(strobe) 101 – delay(data) = delay(strobe) + 50 ps 110 – delay(data) = delay(strobe) + 100 ps 111 – delay(data) = delay(strobe) + 150 ps

Offset Address: 81h (D0F2)
Host FSB CKG Control 2 **Default Value: 55h**

Bit	Attribute	Default	Description
7:6	RW	01b	**CKG Falling-Time Control for Host Interface (S port)** 00: Default timing 01: Delay by 100 ps 10: Delay by 200 ps 11: Delay by 300 ps
5:4	RW	01b	**CKG Rising-Time Control for Host Interface (S port)** 00: Default timing 01: Delay by 100 ps 10: Delay by 200 ps 11: Delay by 300 ps
3:2	RW	01b	**CKG Falling-Time Control for Host Interface** 00: Default timing 01: Delay by 100 ps 10: Delay by 200 ps 11: Delay by 300 ps
1:0	RW	01b	**CKG Rising-Time Control for Host Interface** 00: Default timing 01: Delay by 100 ps 10: Delay by 200 ps 11: Delay by 300 ps

Offset Address: 82h (D0F2)
Host FSB CKG Control 3 **Default Value: 55h**

Bit	Attribute	Default	Description
7:6	RW	01b	**CKG Falling-Time Control for Host Interface (S port)** 00: Default timing 01: Delay by 100 ps 10: Delay by 200 ps 11: Delay by 300 ps
5:4	RW	01b	**CKG Rising-Time Control for Host Interface (S port)** 00: Default timing 01: Delay by 100 ps 10: Delay by 200 ps 11: Delay by 300 ps
3:2	RW	01b	**CKG Rising-Time Control for Host Interface** 00: Default timing 01: Delay by 100 ps 10: Delay by 200 ps 11: Delay by 300 ps
1:0	RW	01b	**CKG Rising-Time Control for Host Interface** 00: Default timing 01: Delay by 100 ps 10: Delay by 200 ps 11: Delay by 300 ps

Offset Address: 83h (D0F2)
Host FSB CKG Control 4 **Default Value: 55h**

Bit	Attribute	Default	Description
7:6	RW	01b	**CKG Falling-Time Control for Host Interface (S port)** 00: Default timing 01: Delay by 100 ps 10: Delay by 200 ps 11: Delay by 300 ps
5:4	RW	01b	**CKG Rising-Time Control for Host Interface (S port)** 00: Default timing 01: Delay by 100 ps 10: Delay by 200 ps 11: Delay by 300 ps
3:2	RW	01b	**CKG Rising-Time Control for Host Interface** 00: Default timing 01: Delay by 100 ps 10: Delay by 200 ps 11: Delay by 300 ps
1:0	RW	01b	**CKG Rising-Time Control for Host Interface** 00: Default timing 01: Delay by 100 ps 10: Delay by 200 ps 11: Delay by 300 ps

Offset Address: 8F-84h (D0F2) – Reserved

Offset Address: 90h (D0F2)
Early CPU-to-DRAMC Read Data Ready Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:2	RO	0	**Reserved**
1:0	RW	00b	**Early CPU-to-DRAMC Read Data Ready Control** 00: 2T Early Read Ready 01: 3T Early Read Ready 10: 4T Early Read Ready 11: 5T Early Read Ready

Offset Address: AF-91h (D0F2) – Reserved

Offset Address: B0h (D0F2)
Timing Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Reorder function of CPU to DRAM read in DBX to optimize 266/333 DBX timing** 0: Disable 1: Enable In DCLK333, it should be set to 0. In other cases, it can be toggled.
6	RW	0	**Optimize conversion time for 200/333 and 266/333** 0: Disable 1: Enable In normal case, it should be set to 0 as the timing can be met.
5:0	RO	0	**Reserved**

Offset Address: B1h (D0F2) - Reserved

Offset Address: B2h (D0F2)
New Feature **Default Value: 0nh**

Bit	Attribute	Default	Description
7	RW	0	**Retry Brant Trace Message after First Lock** 0: Disable 1: Enable
6:4	RO	0	**Reserved**
3:1	RO	n	**GTL Compensation Result**
0	RO	0	**Reserved**

Offset Address: B3h (D0F2)

Pad Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0h	**Reserved**
3:2	RW	00b	**Bdgtl2xd Program Delay** 00: 1000 ps 01: 100 ps 10: 200 ps 11: 300 ps
1:0	RW	00b	**Bdgtl4xd Program Delay** 00: 1000 ps 01: 100 ps 10: 200 ps 11: 300 ps

Offset Address: FF-B4h (D0F2) – Reserved

Device 0 Function 3 (D0F3): DRAM Bus Control

Header Registers (0–3Fh)

Offset Address: 1-0h (D0F3)
Vendor ID — **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**Vendor ID**

Offset Address: 3-2h (D0F3)
Device ID — **Default Value: 3364h**

Bit	Attribute	Default	Description
15:0	RO	3364h	**Device ID**

Offset Address: 5-4h (D0F3)
PCI Command — **Default Value: 0006h**

Bit	Attribute	Default	Description
15:0	RO	0006h	**PCI Command**

Offset Address: 7-6h (D0F3)
PCI Status — **Default Value: 0200h**

Bit	Attribute	Default	Description
15:0	RO	0200h	**PCI Status**

Offset Address: 8h (D0F3)
Revision ID — **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Revision ID**

Offset Address: 0B-9h (D0F3)
Class Code — **Default Value: 06 0000h**

Bit	Attribute	Default	Description
23:0	RO	060000h	**Class Code**

Offset Address: 0Ch (D0F3) – Reserved

Offset Address: 0Dh (D0F3)
Latency Timer — **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Latency Timer**

Offset Address: 0Eh (D0F3)
Header Type — **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Header Type**

Offset Address: 0Fh (D0F3)
Built In Self Test (BIST) **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**BIST**

Offset Address: 13-10h (D0F3) – Reserved

Offset Address: 2D-2Ch (D0F3)
Subsystem Vendor ID **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW1	0	**Subsystem Vendor ID**

Offset Address: 2F-2Eh (D0F3)
Subsystem ID **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW1	0	**Subsystem ID**

Offset Address: 33-30h (D0F3) – Reserved

Offset Address: 34h (D0F3)
Capability Pointer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Capability Pointer**

Offset Address: 3F-35h (D0F3) – Reserved

DRAM Rank Ending Address (40–47h)

Offset Address: 40h (D0F3)
DRAM Rank 0 Ending Address **Default Value: 01h**

Bit	Attribute	Default	Description
7:0	RW	01h	**Virtual Rank 0 Ending Address (HA[33:26])**

Offset Address: 41h (D0F3)
DRAM Rank 1 Ending Address **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Virtual Rank 1 Ending Address (HA[33:26])**

Offset Address: 42h (D0F3)
DRAM Rank 2 Ending Address **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Virtual Rank 2 Ending Address (HA[33:26])**

Offset Address: 43h (D0F3)
DRAM Rank 3 Ending Address **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	Virtual Rank 3 Ending Address (HA[33:26])

Offset Address: 47-44h (D0F3) – Reserved

DRAM Rank Beginning Address (48–4Fh)

Offset Address: 48h (D0F3)
DRAM Rank 0 Beginning Address **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	Virtual Rank 0 Beginning Address (HA[33:26])

Offset Address: 49h (D0F3)
DRAM Rank 1 Beginning Address **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	Virtual Rank 1 Beginning Address (HA[33:26])

Offset Address: 4Ah (D0F3)
DRAM Rank 2 Beginning Address **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	Virtual Rank 2 Beginning Address (HA[33:26])

Offset Address: 4Bh (D0F3)
DRAM Rank 3 Beginning Address **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	Virtual Rank 3 Beginning Address (HA[33:26])

Offset Address: 4F-4Ch (D0F3) – Reserved

MA Map / Command Rate (50–53h)

Offset Address: 51-50h (D0F3)

DRAM MA Map Type **Default Value: 2222h**

Bit	Attribute	Default	Description
15:13	RO	001b	**Reserved** (Do not program)
12	RO	0	**Reserved**
11:9	RO	001b	**Reserved** (Do not program)
8	RO	0	**Reserved**
7:5	RW	001b	**Rank 0/1 MA Map Type**
4	RW	0	**Rank 0/1 1T Command Rate** 0: Disable (2T command) 1: 1T command
3:1	RW	001b	**Rank 2/3 MA Map Type**
0	RW	0	**Rank 2/3 1T Command Rate** 0: Disable (2T command) 1: 1T command

Table 11. Rank MA Map Type Table

Rank MA Map Type	0	1	2	3	4	5	6	7
Bank Address Bits	2	2	2	2	Rsvd	3	3	3
Row Address Bits	13-12	14-12	15-12	15-13		15-12	15-12	15-13
Column Address Bits	9	10	11	12		10	11	12
DRAM Size (Byte)	128M-64M	512M-128M	2G-256M	4G-1G		2G-256M	4G-512M	8G-2G

Offset Address: 52h (D0F3)

Bank Interleave Address Select **Default Value: 11h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6:4	RW	001b	**BA0 Address Select**
3	RO	0	**Reserved**
2:0	RW	001b	**BA1 Address Select**

Note: Refer to Bank Interleave Address Table below.

Offset Address: 53h (D0F3)

Bank / Rank Interleave Address Select **Default Value: 10h**

Bit	Attribute	Default	Description
7	RW	0	**BA2 Support (turn on if any 8BK-device exists)**
6:4	RW	001b	**BA2 Address Select**
3:2	RW	00	**Rank Interleave Address Bit 1 (RA1) Select**
1:0	RW	00	**Rank Interleave Address Bit 0 (RA0) Select**

Table 12. DRAM Bank Address Table

Bank[n] Address Select where x=0, 1, 2	0	1	2	3	4	5	6	7
BA2 Rx53[6:4]	A14	A15	A18	A19	rsvd	rsvd	rsvd	rsvd
BA1 Rx52[2:0]	A12	A14	A16	A18	A20	rsvd	rsvd	rsvd
BA0 Rx52[6:4]	rsvd	A13	A15	A17	A19	rsvd	rsvd	rsvd

Table 13. Rank Interleave Address Table

Rank Interleave[n] Address Select where x=0, 1	0	1	2	3
Rank Interleave Address Bit 1 Rx53[3:2]	A14	A16	A18	A20
Rank Interleave Address Bit 0 Rx53[1:0]	A15	A17	A19	A21

Notes. 1. Rank Interleave Address Bit 2 is fixed at A6.
2. BA2, BA1, BA0, INLV1, INLV0 should select 5 different address bits for Rx53[7] =1
3. BA1, BA0, INLV1, INLV0 should select 4 different address bits for Rx53[7] =0

Physical-to-Virtual Rank Mapping (54–57h)

Offset Address: 54h (D0F3)
Physical-to-Virtual Rank Mapping 1 **Default Value: 81h**

Bit	Attribute	Default	Description
7	RW	1b	**Enable Physical Rank 0** 0: Disable 1: Enable
6:4	RW	0	**Virtual Rank Number of Physical Rank 0**
3	RW	0	**Enable Physical Rank 1** 0: Disable 1: Enable
2:0	RW	001b	**Virtual Rank Number of Physical Rank 1**

Offset Address: 55h (D0F3)
Physical-to-Virtual Rank Mapping 2 **Default Value: 23h**

Bit	Attribute	Default	Description
7	RW	0	**Enable Physical Rank 2** 0: Disable 1: Enable
6:4	RW	010b	**Virtual Rank Number of Physical Rank 2**
3	RW	0	**Enable Physical Rank 3** 0: Disable 1: Enable
2:0	RW	011b	**Virtual Rank Number of Physical Rank 3**

Offset Address: 57-56h (D0F3) – Reserved

Virtual Rank Interleave Address Select / Enable (58–5Fh)

Offset Address: 58h (D0F3)
Virtual Rank Interleave Address Select / Enable – Rank 0 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6:4	RW	000b	**Rank #0 Interleave Address Select (RINLV0AS[2:0])** This 3-bits field determines the Rank Interleave Address of Rank #0. If RINLV0ASn is 1 (where n = 0, 1, 2), the corresponding Rank Interleave Address bit of Rank 0 is 1, and vice versa.
3	RO	0	**Reserved**
2:0	RW	000b	**Rank #0 Interleave Address Enable (RINLV0AEN[2:0])** 0: Mask 1: Enable This 3-bits field determines if the Rank Interleave Address of Rank #0 to be masked (used) or not. If RINLV0AENn is 0 (where n = 0, 1, 2), the corresponding Rank Interleave Address bit will be masked (ignored), and vice versa.

Offset Address: 59h (D0F3)

Virtual Rank Interleave Address Select / Enable – Rank 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6:4	RW	0	**Rank #1 Interleave Address Select** See the description on Rank 0 (Rx58).
3	RO	0	**Reserved**
2:0	RW	0	**Rank #1 Interleave Address Enable** See the description on Rank 0 (Rx58).

Offset Address: 5Ah (D0F3)

Virtual Rank Interleave Address Select / Enable – Rank 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6:4	RW	0	**Rank #2 Interleave Address Select** See the description on Rank 0 (Rx58).
3	RO	0	**Reserved**
2:0	RW	0	**Rank #2 Interleave Address Enable** See the description on Rank 0 (Rx58).

Offset Address: 5Bh (D0F3)

Virtual Rank Interleave Address Select / Enable – Rank 3 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6:4	RW	0	**Rank #3 Interleave Address Select** See the description on Rank 0 (Rx58).
3	RO	0	**Reserved**
2:0	RW	0	**Rank #3 Interleave Address Enable** See the description on Rank 0 (Rx58).

Offset Address: 5F-5Ch (D0F3)- Reserved

Following is an example, which shows a possible register settings for a system with 2 double-sided DIMM installed.

(1) Rx53[3:2] = 2 and Rx53[1:0] = 2 select A6, A18, A19 as the Rank Interleave Address for the system.

(2) If the settings on the Rank Interleave Address Selection of Rank 0, 1, 2, 3 (Rx58-5B[6:4]) are
Rx58[6:4] = 001b
Rx59[6:4] = 000b
Rx5A[6:4] = 010b
Rx5B[6:4] = 011b

And if the Rank Interleave Address Enable of Rank 0, 1, 2, 3 (Rx58-5B[2:0]) are
Rx58[2:0] = 011b
Rx59[2:0] = 011b
Rx5A[2:0] = 011b
Rx5B[2:0] = 011b

With the above register settings, Rank Interleave Address 2, A6, is ignored for the system, and the four ranks of the system are decided by A18 and A19 as shown in the following table.

A18	A19	Selected Rank
0	0	Rank#1
0	1	Rank#0
1	0	Rank#2
1	1	Rank#3

DRAM Timing (60–64h)

Offset Address: 60h (D0F3)

DRAM Pipeline Turn-Around Setting **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**0ws Back-to-Back Write to Different DDR Rank** 0: Disable 1: Enable
6	RW	0	**Fast Read-to-Read Turn Around** 0: Disable 1: Enable (DQS post-amble overlap with preamble)
5	RW	0	**Fast Read-to-Write Turn Around** 0: Disable 1: Enable
4	RW	0	**Fast Write-to-Read Turn Around** 0: Disable 1: Enable
3:2	RO	0	**Reserved**
1	RW	0	**0ws DRAM Channel Switching Between Read Cycles** 0: Disable 1: Enable
0	RW	0	**0ws DRAM Channel Switching Between Write Cycles** 0: Disable 1: Enable

Offset Address: 61h (D0F3)

DRAM Timing for All Ranks **Default Value: 04h**

Bit	Attribute	Default	Description
7:6	RW	00	**Active-to-Active Period (tRRD)** 00: 2T 01: 3T 10: 4T 11: 5T
5:0	RW	04h	**Refresh-to-Active or Refersh-to-Refresh (tRFC)** 00: 8T 01h: 9T … 0nh: (8+n)T 3eh: 70T 3f:h: 71T

Offset Address: 62h (D0F3)
DRAM Timing for All Ranks **Default Value: 21h**

Bit	Attribute	Default	Description
7:4	RW	0010b	**Active-to-Precharge (tRAS)** 0000: 5T 0001: 6T … 0nh: (5+n)T 1110: 19T 1111: 20T
3	RW	0	**Enable DDR2 8-Bank Device Timing Constraint (tRRD and tRP).**
2:0	RW	001b	**CAS Latency** DDR DDR2 000 1.5 2 001 2 3 010 2.5 4 011 3 5 1xx reserved 6

Offset Address: 63h (D0F3)
DRAM Timer for All Ranks **Default Value: 20h**

Bit	Attribute	Default	Description
7:5	RW	001b	**Write Recovery Time (tWR)** 000: 2T 001: 3T 010: 4T 011: 5T 100: 6T
4	RO	0	**Reserved**
3	RW	0	**Read-to-Precharge Delay (tRTP)** 0: 2T 1: 3T
2	RO	0	**Reserved**
1:0	RW	00b	**Write to Read Command Delay (tWTR)** DDR DDR2 00 1T 2T 01 2T 3T 10 3T 4T 11 4T 5T

Offset Address: 64h (D0F3)
DRAM Timer for All Ranks **Default Value: 22h**

Bit	Attribute	Default	Description
7:5	RW	001b	**Active to Read or Write Delay (tRCD)** 000: 2T 001: 3T 010: 4T 011: 5T 100: 6T
4	RW	0	**CKE Minimum Pulse Width** 0: 2T 1: 3T This function is valid when D0F4 RxA1[6] = 1
3:1	RW	001b	**Precharge Period (tPR)** 000: 2T 001: 3T 010: 4T 011: 5T 100: 6T
0	RW	0	**Exit Precharge/Active Power Down to Any Command Delay** 0: 1T 1: 2T This function is valid when D0F4 RxA1[6] = 1

DRAM Queue / Arbitration (65–67h)

Offset Address: 65h (D0F3)
DRAM Arbitration Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**AGP Timer** (in unit of 4 DCLKS) DRAMC time slot allocated for AGP device.
3:0	RW	0	**Host Timer** (in unit of 4 DCLKS) DRAMC time slot allocated for Host.

Offset Address: 66h (D0F3)
DRAM Queue / Arbitration **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**DRAMC Queue Size Greater Than 2** 0: No 1: Yes
6	RW	0	**DRAMC Queue Size Not Equal To 4** 0: No 1: Yes To setup DRAMC queue size of 2, set Rx66[7:6] to 2'b00; sets Rx66[7:6] to 2'b11 for queue size of 3; sets Rx[7:6] to 2'b10 for queue size of 4.
5:4	RW	00b	**Arbitration Parking Policy** 00: Park at the last bus owner 01: Park at CPU 10: Park at AGP 11: Park at VGA
3:0	RW	0	**Priority Promotion Timer** (in unit of 4 DCLKs) A DRAM request is promoted to become a high priority request when it is pending over PTIM*4 DRAM cycles.

Offset Address: 67h (D0F3)
DIMM Command / Address Selection **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RO	0	Reserved
5:4	RW	00b	**DIMM 2 Command / Address Selection** 00: SCMD/MA Bus A; 01: SCMD/MA Bus B 10: Reserved 11: Reserved
3:2	RW	0	**DIMM 1 Command / Address Selection**
1:0	RW	0	**DIMM 0 Command / Address Selection**

DRAM Control (68–69h)

Offset Address: 68h (D0F3)
DDR Page Control 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**DRAM Expired Page Threshold** Close expired pages with precharge-all command when the number of expired pages exceeds the value.
3:0	RW	0	**Page Register Life Timer** (in unit of 16 DCLKs) When timer expired, the expired page will be closed.

Offset Address: 69h (D0F3)
DDR Page Control 2 **Default Value: 82h**

Bit	Attribute	Default	Description
7:6	RW	10b	**Bank Interleave** 00: No interleave 01: 2-bank 10: 4-bank 11: 8-bank
5	RW	0	**Enable Bank Address Scramble**
4	RW	0	**Auto-Precharge for TLB Read and CPU Write-Back** 0: Disable 1: Enable
3	RW	0	**Option of Dynamic page-clock** 0: Dynamic Page Clock 1: Dynamic DRAM Clock
2	RW	0	**Reserved**
1	RW	1b	**Keep Page Active When Cross Bank** 0: Disable 1: Enable
0	RW	0	**Multiple Page Mode** 0: Disable 1: Enable

Refresh Control (6A–6Bh)

Offset Address: 6Ah (D0F3)
Refresh Counter **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Refresh Counter** (in unit of 16 DRAM CLKs) When set to 00, DRAM refresh is disabled

Offset Address: 6Bh (D0F3)
DRAM Miscellaneous Control **Default Value: 10h**

Bit	Attribute	Default	Description
7	RW	0	**DQS Input DLL Adjustment** 0: Disable 1: Enable
6	RW	0	**DQS Output DLL Adjustment** 0: Disable 1: Enable
5	RW	0	**Burst Refresh** 0: Disable 1: Enable
4	RW	1b	**DLL Manual Reset** 0: Disable 1: Enable
3	RW	0	**Enable Memory Size Detection, MA 32/16 33/17 Swap** 0: Disable 1: Enable
2:0	RW	000b	**SDRAM Operation Mode Select** 000: Normal SDRAM Mode 001: NOP Command Enable 010: All-Banks-Precharge Command Enable. 011: MRS to SCMD 100: CBR, CAS-before-RAS refresh, Cycle Enable 101: Reserved 11x: Reserved

DDR SDRAM Control (6C–6Fh)

Offset Address: 6Ch (D0F3)

DRAM Type **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**DDR2 DRAM Support** 0: Disable DDR2 1: Enable DDR2
6	RO	0	**Memory Type Detected** (through pin: MEMDET) 0: DDR 1: DDR2
5	RO	0	**Reserved**
4	RW	0	**Disable DQM Signals** 0: Enable 1: Disable
3	RW	0	**SDRAM Effective Burst Length** For 64-bit mode ranks, SDRAM MRS 0: BL4 1: BL8
2:0	RO	0	**Reserved**

Offset Address: 6Dh (D0F3)

DQ Channel Select **Default Value: C0h**

Bit	Attribute	Default	Description
7	RO	1b	**Reserved** (Do not program)
6	RO	1b	**Reserved** (Do not program)
5	RW	0	**DQ Channel Select for DIMM#1** 0: Channel A 1: Channel B
4	RW	0	**DQ Channel Select for DIMM#0** 0: Channel A 1: Channel B
3:0	RW	0	**Reserved**

Note: If ODT is not supported, the registers can be programmed, i.e. the function of MD/CS mapping can work.

Offset Address: 6Eh (D0F3)

DRAM Control **Default Value: 08h**

Bit	Attribute	Default	Description
7	RW	0	**MPD Disable** 0: Enable 1: Disable
6:5	RO	0	**Reserved**
4	RW	0	**Non-Page Mode Support** 0: Disable 1: Enable
3	RW	1b	**Enable 1 Pipeline Stage on DRAM Command Path** 0: Disable 1: Enable 1 pipeline stage on DRAM command (CS/SCMD/MA) path.
2:0	RO	0	**Reserved**

Table 14. DQM Signal Function

DRAM Configuration	DQM Pin Function	Rx6C[4]	Rx6E[7]
DDR w/o ECC x8	Data Mask	0	1

Offset Address: 6Fh (D0F3)
Miscellaneous Control **Default Value: 42h**

Bit	Attribute	Default	Description
7	RW	0	**Non-ONBD Protection for GART Table Fetching** 0: Disable 1: Enable
6	RW	1b	**DRAM-Side-Input-Pointer Non-Return-Zero Mode** 0: Disable 1: Enable Enable to avoid overwrite data
5	RW	0	**Disallow the 2nd Cycle of a 2T Command Overlapped with Command of Different Type on a Different MA/SCMD Bus** 0: Allow 1: Not allow Sets this bit to 1 when read-modify-write mode is enabled (for example, ECC mode).
4	RW	0	**Read-Modify-Write (RMW) Option** When enabled, RMW is processed in relaxed mode.
3	RW	0	**Applying Same-Channel IO Turn-Around Constraints between Different Channels**
2	RW	0	**Exclusive SCMD Buses** When enabled, the two SCMD buses are exclusive, do not have commands in the same cycle.
1	RW	1b	**Compact Refresh Mode** Skip CS for non-existing rank while refresh 0: Disable 1: Enable
0	RW	0	**GART Table Access Option** When enabled, GART Table accessing is in relaxed mode. Set this bit to 1 in DDR400 mode.

DRAM Signal Timing Control (70–7Fh)

Offset Address: 70h (D0F3)
DQS Output Delay Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**DQS Output Delay**

Offset Address: 71h (D0F3)
MD Output Delay Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**MD Output Delay**

Offset Address: 73-72h (D0F3) – Reserved

Offset Address: 74h (D0F3)
DQS Output Clock Phase Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RO	0	**Reserved**
2:0	RW	0	**Initial Phase of Internal Clocks for DQS Output** Each steps increase a phase of 1/8 T

Offset Address: 75h (D0F3)
DQ Output Clock Phase Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RO	0	**Reserved**
2:0	RW	0	**Initial Phase of Internal Clocks for DQ Output** Each steps increase a phase of 1/8 T

Offset Address: 76h (D0F3)
Write Data Phase Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**1 More Pipeline Stage on Write Data Path** Will provide safer timing margin.
6	RW	0	**1 More Pipeline Stage on Write Data Path** Will provide safer timing margin for DDR2-667 and above.
5	RW	0	**DQ/DQS Output Clocks Bypass Delay Component** (i.e. when enabled, Rx70-73 becomes functionless
4	RO	0	**Reserved**
3:2	RW	00b	**Advance Write Phase Signals to Make Room for the Long Bus Delay** The 2 bits must be used with bit [1:0] 00: Normal mode 01: Advance 1 cycle 10: Advance 2 cycle 11: Forbidden
1:0	RW	0	**Write MD/DQS/CAS Output Timing Range Control** Each increased step delays the output range by 1/4 T.

Offset Address: 77h (D0F3)
DQS Input Delay Calibration **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Manual DQS Input Delay Setting** 0:Auto 1: Manual
6	RO	0	**Reserved**
5:0	RO/RW	0	**DDR DQS Input Delay** This is the base delay value of DQS input signal in unsigned binary format. The reading value depends on Rx77[7]. If Rx77[7] = 0 (auto mode), DLL calibration result is returned when read. When Rx77[7] = 0, RO When Rx77[7] = 1, RW

Offset Address: 78h (D0F3)
DQS Input Capture Range Control **Default Value: 80h**

Bit	Attribute	Default	Description
7	RW	1b	**Manual DQS Input Capture Range Setting** 0: Auto 1: Manual
6	RW	0	**Enable DQS Input Capture Range Detection**
5:0	RW	00h	**DQS Input Capture Range** **Bit [5:4]** 00: 1T prior to 1st DQS rising edge 01: at 1st DQS rising edge 10: 1T after 11: Reserved **Bit [3:1]** Each unit adds 1/8T delay **Bit [0]** Add 0.35ns fine tune delay

Offset Address: 79h (D0F3) – Reserved

Offset Address: 7Ah (D0F3)
DQS Input Capture Range Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3	RW	0	**Select DQS Input Pin as Input Capture Range Detection Signal** 0: DQSA0 1: DQSA4
2:0	RW	0	**DQS Input Capture Range Offset Value** 1/8T per step, 2's complement

Offset Address: 7Bh (D0F3)
Read Data Phase Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6:4	RW	000b	**MD Input Data Push Timing Control** 000: Start moving data into internal buffer 1T after the 1st DRAM strobe 001: 1.5T 010: 2T 011: 2.5T 100: 3 101: 3.5T 110: 4T 111: 4.5T
3:1	RO	0	**Reserved**
0	RW	0	**Extend DQS Input Capture Range 1/2T Earlier**

Read-Only Control (7C-7Fh)

Offset Address: 7Ch (D0F3)
DQS Input Delay Offset Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6:0	RW	0	**DQS Input Delay Offset** (In two's complement) This is the offset values (in 2's complement format) from the base delay value (Rx77[5:0]) DIMM.

Offset Address: 7F-7Dh (D0F3) – Reserved

Shadow RAM Control (80–83h)

Offset Address: 80h (D0F3)
Page-C ROM Shadow Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00b	**CC000-CFFFFh Memory Space Access Control** 00: Read / Write Disable 01: Write Enable 10: Read Enable 11: Read / Write Enable
5:4	RW	0	**C8000-CBFFFh Memory Space Access Control**
3:2	RW	0	**C4000-C7FFFh Memory Space Access Control**
1:0	RW	0	**C0000-C3FFFh Memory Space Access Control**

Offset Address: 81h (D0F3)
Page-D ROM Shadow Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00b	**DC000-DFFFFh Memory Space Access Control** 00: Read / Write Disable 01: Write Enable 10: Read Enable 11: Read / Write Enable
5:4	RW	0	**D8000-DBFFFh Memory Space Access Control**
3:2	RW	0	**D4000-D7FFFh Memory Space Access Control**
1:0	RW	0	**D0000-D3FFFh Memory Space Access Control**

Offset Address: 82h (D0F3)
Page-E ROM Shadow Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00b	**EC000-EFFFFh Memory Space Access Control** 00: Read / Write Disable 01: Write Enable 10: Read Enable 11: Read / Write Enable
5:4	RW	0	**E8000-EBFFFh Memory Space Access Control**
3:2	RW	0	**E4000-E7FFFh Memory Space Access Control**
1:0	RW	0	**E0000-E3FFFh Memory Space Access Control**

Offset Address: 83h (D0F3)
Page-F ROM, Memory Hole and SMI Decoding **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved**
5:4	RW	00b	**F0000-FFFFFh Memory Space Access Control** 00: Read / Write Disable 01: Write Enable 10: Read Enable 11: Read / Write Enable
3:2	RW	00b	**Memory Hole** 00: None 01: 512K – 640K 10: 15M – 16M (1M) 11: 14M – 16M (2M)
1	RW	0	**Disable Data Access on SMRAM (Page A, B) in SM Mode** 0: In SM mode, page A,B CPU Data R/W cycles are forwarded to the memory controller. 1: In SM mode, page A,B CPU Data R/W cycles are forwarded to the PCI bus Notes: 1. This bit is effective when Rx83[0] is set to 0. 2. SMRAM page A,B Code R/W cycles are always forwarded to the memory controller in SM mode.
0	RW	0	**Enable Page A, B DRAM Access In Normal Mode** 0: Page A, B CPU R/W cycles could be forwarded to memory controller or PCI bus depends on the setting of RABKDOFF (bit 1), the CPU operating mode (Normal or SM mode) as well as the type (Code or Data) of the CPU cycle. 1: Page A, B CPU R/W cycles (Code and Data) are always (in either Normal or SM mode) forwarded to the memory controller. Check the following table for details.

Table 15. CPU-to-SMRAM Cycle Flow

Rx83[1]	Rx83[0]	CPU MODE	Target of CODE Acces Cycle	Target of DATA Access Cycle
X	0	Normal	PCI	PCI
0	0	SMM	DRAM	DRAM
1	0	SMM	DRAM	PCI
x	1	Normal / SMM	DRAM	DRAM

DRAM Above 4G Support (84-8C)

Offset Address: 84h (D0F3)

Low Top Address - Low **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Low Top Address - A[23:20]**
3:0	RO	0	**Reserved**

Offset Address: 85h (D0F3)

Low Top Address - High **Default Value: FFh**

Bit	Attribute	Default	Description
7:0	RW	FFh	**Low Top Address – A[31:24]**

Offset Address: 86h (D0F3)

SMM and APIC Decoding **Default Value: 01h**

Bit	Attribute	Default	Description
7:6	RW	00b	**Top SM Memory Size** 00: 1M 01: 2M 10: 4M 11: 8M
5	RW	0	**APIC Lowest Interrupt Arbitration** 0: Disable 1: Enable
4	RW	0	**IO APIC Decoding** 0: Cycles accessing FECx_xxxxh are passed to PCI1 1: Cycles accessing FEC7_FFFFh - FEC0_0000h are passed to PCI1; cycles accessing FECF_FFFFh - FEC8_0000h access cycles are passed to PCI2.
3	RW	0	**MSI Support (Processor Message Enable)** 0: Cycles accessing FEEx_xxxxh from masters are passed to PCI1 (PCIC will not claim) 1: Cycles accessing FEEx_xxxxh from masters are passed to the Host side for snooping
2	RW	0	**Top 1MB SM Memory Enable** 0: Disable 1: Enable
1	RO	0	**Reserved**
0	RW	1b	**Compatible SMM Enable** 0: Disable 1: Enable

Offset Address: 89-88h (D0F3)

Misc. DRAM Address Setting **Default Value:0000h**

Bit	Attribute	Default	Description
15:11	RO	0	**Reserved**
10:0	RO	0	**The Address Next to the Last Valid DRAM Address**

Offset Address: 8Ch (D0F3)

DQS Output Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:2	RO	0	**Reserved**
1	RW	0	**MD/DQS Earlier Output Enable** DQ Output Enable (MDOE) 1/2T earlier DQS Output Enable (DQSOE) 1/2T earlier if bit 0
0	RW	0	**DQS Earlier Output Enable** DQSOE 1/4T earlier if bit 1 =1

Offset Address: 8F-8Dh (D0F3) – Reserved

DRAM Clocking Control (90-9F)

Offset Address: 90h (D0F3)

DRAM Clock Operation Mode and Frequency **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**DCLK Switch to Non-Feedback Mode** 0: Feedback mode 1: Non-feedback mode (feed-forward mode). There is no need to feed DCLKO back through MCLKIN port.
6:3	RO	0	**Reserved**
2:0	RW	000b	**DRAM Operating Frequency** 000: 100MHz 001: 133MHz 010: 166MHz 011: 200MHz 100: 266MHz 101: 333MHz 110: Reserved 111: Reserved

Offset Address: 91h (D0F3)

DCLK (MCLK) Phase Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RO	0	**Reserved**
2:0	RW	0	**DCLKOA Phase Select** Each step increases 1/8T

Offset Address: 92h (D0F3)

CS/CKE Clock Phase Control **Default Value: 30h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6:4	RO	011b	**Reserved** (Do not program)
3	RO	0	**Reserved**
2:0	RW	0	**Sampling Clock Phase Select for CS/CKE** Each step increases a phase of 1/8 T

Offset Address: 93h (D0F3)

SCMD/MA Clock Phase Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RO	0	**Reserved**
2:0	RW	0	**Sampling Clock Phase Select for SCMD/MA** Each step increases a phase of 1/8 T

Offset Address: 94h (D0F3)

DCLKO Feedback Mode Output Control **Default Value: 01h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6:4	RW	0	**DCLKO Feedback Mode Output Control** For Rx90[7] = 0 mode, if DCLKOA is fed back to DCLKIA, each increased step delays DCLKOB; if DCLKOB is fed back to DCLKIA, each increased step makes DCLKOA earlier (1/8T per step).
3	RO	0	**Reserved**
2:0	RW	001b	**DCLKO Feedback Mode Output Control** For Rx90[7] = 0 mode, if DCLKOA is fed back to DCLKIA, each increased step makes DCLKOB earlier; if DCLKOB is fed back to DCLKIA, each increased step delays DCLKOA (1/8T per step).

Offset Address: 97-95h (D0F3) – Reserved

Offset Address: 98h (D0F3)
DRAMC Pipeline Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Pipelining Stage on Request Page Decoding** Improves DRAMC internal timing for DDR2-667 and above, but increase latency.
6	RW	0	**2T Page Close Rate** Improves DRAMC internal timing for DDR2-667 and above when D0F3 Rx68[3:0]!= 0.
5	RW	0	**2T Command Scheduling** Improves DRAMC internal timing for DDR2-667 and above when Rx50 = 1, but may affect performance.
4	RO	0	**Reserved**
3	RW	0	**2T Command Scheduling for Non-Valid Request Queue** Improves DRAMC internal timing for DDR2-667 and above, but may affect performance.
2:0	RO	0	**Reserved**

Offset Address: 9Ch (D0F3)
ODT Lookup Table **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00b	**Rank 3 ODT Signal Selection** 00:ODTA0 01: ODTA1 10:ODTA2 11: ODTA3
5:4	RW	0	**Rank 2 ODT Signal Selection**
3:2	RW	0	**Rank 1 ODT Signal Selection**
1:0	RW	0	**Rank 0 ODT Signal Selection**

Offset Address: 9Dh (D0F3) – Reserved

Offset Address: 9Eh (D0F3)
SDRAM ODT Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**DDR2 SDRAM ODT Control** 0: Disable 1: Enable
6	RW	0	**2T Write Command when Rx50 (Rank 1T Command) =1** 0: Disable 1: Enable
5:4	RW	00b	**Add MD Bus Turn Around Wait State for DDR2 ODT** 00: Disable 01: 1T wait state 10: 2T wait state 11: 3T wait state
3:1	RO	0	**Reserved**
0	RW	0	**Differential DQS Input** 0: Disable 1: Enable

Offset Address: 9Fh (D0F3)
SDRAM ODT Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00b	**DDR2 SDRAM ODT Write Cycle Late Extension** 00: Disable 01: 1T extension 10: 2T extension 11: 3T extension
5:4	RW	00b	**DDR2 SDRAM ODT Read Cycle Late Extension** 00: Disable 01: 1T extension 10: 2T extension 11: 3T extension
3:2	RO	0	**Reserved**
1:0	RW	00b	**DDR2 SDRAM ODT Early Extension** 00: Disable 01: 1T extension 10: 2T extension 11: 3T extension

UMA Registers (A0–AFh)

Offset Address: A1-A0h (D0F3)

CPU Direct Access Frame Buffer Control **Default Value: 00h**

Bit	Attribute	Default	Description
15	RW	0	**VGA Enable** 0: Disable 1: Enable
14:12	RW	000b	**Frame Buffer Size Selection** 000: none 001: 8M 010: 16M 011: 32M 100: 64M 101: 128M 110: 256M 111: 512M
11:1	RW	0	**A[31:21]**
0	RW	0	**CPU Direct Access Frame Buffer Enable** 0: Disable 1: Enable

Offset Address: A2h (D0F3)

VGA Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**VGA High Priority Timer** (unit of 16 DCLK)
3:0	RW	0	**VGA Timer** (unit of 16 DCLK)

Offset Address: A3h (D0F3) – Reserved

Offset Address: A5-A4h (D0F3)

GFX Misc. **Default Value: 00h**

Bit	Attribute	Default	Description
15:14	RO	0	**Reserved**
13	RW	0	**Reset Internal GFX by BIOS** 0: Not reset 1: Reset
12	RO	0	**Reserved**
11:10	RW	00b	**Fine Tune GFX PCICLK** 00: Default 01: Delay 100 ps 10: Early 150 ps 11: Early 300 ps
9:8	RW	00b	**Fine Tune GFX MCK** 00: Default 01: Delay 100 ps 10: Early 150 ps 11: Early 300 ps
7:5	RO	0	**Reserved**
4	RW	0	**GRLD Delay 1 Cycle** (GFX Low Priority Read Data 1T Delay) 0: No delay 1: Delay 1T
3	RW	0	**Turn Off LANE8~15 PCIE_16LANE_nopad to Save Power Consumption** 0: Turn on 1: Turn off
2	RW	0	**Turn Off LANE0~7 PCIE_16LANE_nopad to Save Power Consumption** 0: Turn on 1: Turn off
1	RO	0	**Reserved**
0	RW	0	**GFX Data Delay to Sync with Clock** 0: No sync 1: Sync with clock

Offset Address: AF-A6h (D0F3) – Reserved

GMINT and AGPCINT Registers (B0–BFh)

Offset Address: B1-B0h (D0F3)

GMINT Misc. **Default Value: 0000h**

Bit	Attribute	Default	Description
15:12	RW	0	**Switching Timer from High Channel to Low Channel** (in unit of 16 DCLK)
11:8	RW	0	**Switching Timer from Low Channel to High Channel** (in unit of 16 DCLK)
7	RW	0	**Disable Synced Registers for GFX Request-Related Signals to GMINT** 0: Sync 1T 1: Bypass sync logic
6	RW	0	**Allow GMINT Low Channel Issue 8QW Request** (Coordinate with D0F2 Rx54[4].)
5	RW	0	**Allow GMINT High Channel Issue 8QW Request** (Coordinate with D0F2 Rx54[4].)
4	RO	0	**Power-Management of GMINT Read Cycle**
3	RW	0	**Improve GMINT Arbitration Performance** 0: Disable 1: Enable arbitration policy of priority agent bus request/symmetric bus agent request
2:0	RW	0	**Frame Buffer Rank**

Offset Address: B2h (D0F3)

AGPCINT Misc. **Default Value: A0h**

Bit	Attribute	Default	Description
7	RW	1b	**AGPCINT to GFX Interface Power Management Enable** 0: Disable 1: Enable
6	RW	0	**GADS from AGPC Will Be Strict Priority** 0: Disable 1: Enable (Cooperate with RxB2[5])
5	RW	1b	**RAGPPRI Enable** 0: Disable 1: Enable (When GRPI wants to come from GADSH, this bit should be de-asserted)
4	RW	0	**MGFIFO Level Control** 0: No limitation on the number of levels 1: 14 levels
4	RO	0	**Reserved**
3	RW	0	**Allow AGPCINT Issue 8QW Request** (Coordinate with D0F2 Rx54[4])
2	RW	0	**GFX AGP Read Data Sync 1T**
1	RW	0	**AGPCINT Pipe Mode Disable** 0: Enable 1: Disable
0	RO	0	**Reserved**

Offset Address: BF-B3h (D0F3) – Reserved

DDR2 – I/O Pad Termination and Driving Control (D0–DFh)

Offset Address: D0h (D0F3)

DQ / DQS Termination Strength Manual Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**DQ/DQS Pull-up Termination Strength Manual Setting**
3:0	RW	0	**DQ/DQS Pull-down Termination Strength Manual Setting**

Offset Address: D1h (D0F3)

DQ / DQS Termination Strength Status **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**DQ/DQS Pull-up Termination Strength Auto-comp Value**
3:0	RO	0	**DQ/DQS Pull-down Termination Strength Auto-comp Value**

Offset Address: D2h (D0F3)
DQ Driving Strength Status **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**DQ Pull-up Driving Strength Auto-comp Value**
3:0	RO	0	**DQ Pull-down Driving Strength Auto-comp Value**

Offset Address: D3h (D0F3)
Compensation Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:2	RO	0	**Reserved**
1	RW	0	**Disable DDR Compensation Auto Mode** 0: Enable Auto Mode 1: Disable Auto Mode If DDR Compensation and DDR Auto Compensation are both enabled, the ODT settings for all DRAM pads are from auto-comp circuit (RxD1); otherwise, if Auto Compensation is disabled, the ODT settings are from manual setting (RxD0).
0	RW	0	**Enable DDR Compensation** 0: Disable 1: Enable Disable DDR Compensation provides a power saving mode, however, the values of RxD1 and RxD2 should be ignored.

Note: The DQ driving bits of RxD2 is the result of the auto-comp circuit; however, there is no "auto-mode" for the DQ/DQB driving control since it depends on the actual number of ranks in the DRAM data channel

Offset Address: D4h (D0F3)
ODT Pullup / Pulldown Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Enable NB Pad ODT** 1: Enable ODT when reading data 0: Disable ODT unless RxD4[3:0] is not equal to 0
6	RW	0	**Enable DDR Pad Static Termination** 1: Enable 0: Disable
5	RW	0	**Enable MCLKI ODT** 1: Enable 0: Disable
4	RO	0	**Reserved**
3	RW	0	**ODT Pullup Enable**
2	RO	0	**Reserved**
1	RW	0	**Pulldown Enable**
0	RO	0	**Reserved**

Offset Address: D5h (D0F3)
DQ / DQS Burst Function and ODT Range Select **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**DQ Burst Function** 1: Enable 0: Disable
6	RO	0	**Reserved**
5	RW	0	**DQS Burst Function**
4	RO	0	**Reserved**
3	RW	0	**DQ ODT Range Select** 1: 75 ohm 0: 150 ohm
2	RO	0	**Reserved**
1	RW	0	**DQS ODT Range Select**
0	RO	0	**Reserved**

Offset Address: D6h (D0F3)
DCLK / SCMD / CS Driving Select **Default Value: 80h**

Bit	Attribute	Default	Description
7	RW	1b	**DCLKOA Driving Select** 0: Weak driving for DDR or DDR2 without series resistance on MB 1: Strong driving for DDR2 with series resistance on MB
6	RO	0	**Reserved**
5	RW	0	**SCMD/MA Driving Select**
4	RO	0	**Reserved**
3	RW	0	**CKE/CS Driving Select**
2:0	RO	0	**Reserved**

Offset Address: D7h (D0F3)
SCMD/MA Burst Function **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**SCMD/MA Burst Function Enable**
6:1	RO	0	**Reserved**
0	RW	0	**DCLKI ODT Range Select**

Offset Address: D8h (D0F3)
DCLKI Termination Strength **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**DCLKI Pull-up Termination Strength**
3:0	RW	0	**DCLKI Pull-down Termination Strength**

DRAM Driving Control (E0–EBh)

Table 16. Physical Pin to Driving Group Mapping Table

Physical Pins	DCLK	CKE	CS	MA	DQ	DQS	MPD/DQM
Driving Group	DCLK	CS	CS	MA	DQ	DQS	DQ

Offset Address: E0h (D0F3)
DRAM Driving **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**PMOS Driving**
3:0	RW	0	**NMOS Driving**

Offset Address: E1h (D0F3) – Reserved

Offset Address: E2h (D0F3)
DRAM Driving – Group DQ (MD, MPD, DQS, DQM) **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**PMOS Driving**
3:0	RW	0	**NMOS Driving**

Offset Address: E3h (D0F3) – Reserved

Offset Address: E4h (D0F3)
DRAM Driving – Group CS (CS, DQM, MPD) **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**PMOS Driving**
3:0	RW	0	**NMOS Driving**

Offset Address: E5h (D0F3) – Reserved

Offset Address: E6h (D0F3)
DRAM Driving – Group DCLK **Default Value: 88h**

Bit	Attribute	Default	Description
7:4	RW	1000b	**PMOS Driving**
3:0	RW	1000b	**NMOS Driving**

Offset Address: E7h (D0F3) – Reserved

Offset Address: E8h (D0F3)
DRAM Driving – Group SCMD/MA **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**PMOS Driving**
3:0	RW	0	**NMOS Driving**

Offset Address: EB-E9h (D0F3) – Reserved

DRAM CKG Control (EC–EFh)

Offset Address: ECh (D0F3)
DQS / DQ CKG Output Duty Cycle Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00b	**DQS CKG Falling Edge Control** 00: Default 01: Falling edge delays 100 ps 10: Falling edge delays 200 ps 11: Falling edge delays 300 ps
5:4	RW	00b	**DQS CKG Rising Edge Control** 00: Default 01: Rising edge delays 100 ps 10: Rising edge delays 200 ps 11: Rising edge delays 300 ps
3:2	RW	00b	**DQ CKG Falling Edge Control** 00: Default 01: Falling edge delays 100 ps 10: Falling edge delays 200 ps 11: Falling edge delays 300 ps
1:0	RW	00b	**DQ CKG Rising Edge Control** 00: Default 01: Rising edge delays 100 ps 10: Rising edge delays 200 ps 11: Rising edge delays 300 ps

Offset Address: ED (D0F3) – Reserved

Offset Address: EEh (D0F3)
DCLK Output Duty Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00b	**Duty Control for DCLK** 00: Default 01: Falling edge delays 100 ps 10: Falling edge delays 200 ps 11: Falling edge delays 300 ps
5:4	RW	00b	**Duty Control for DCLK** 00: Default 01: Rising edge delays 100 ps 10: Rising edge delays 200 ps 11: Rising edge delays 300 ps
3:0	RO	0	**Reserved**

Offset Address: EFh (D0F3)
DQ CKG Input Delay Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved**
5:4	RW	00b	**Delay Control for MDA** 00: -150 ps 01: 0 ps 10: 150 ps 11: 300 ps
3:0	RO	0	**Reserved**

DQ / DQS CKG Output Delay Control (F0–F7h)

Offset Address: F0-F3h (D0F3)
DQ/DQS CKG Output Delay Control **Default Value: 00h**

Bit	Attribute	Default	Description
31	RO	0	**Reserved**
30:28	RW	000b	**DQ/DQS Delay Control for Group A7** 000: Default 001: Delay 60 ps 010: Delay 120 ps 011: Delay 180 ps 100: Delay 240 ps 101: Delay 300 ps 110: Delay 360 ps 111: Delay 420 ps
27	RO	0	**Reserved**
26:24	RW	0	**DQ/DQS Delay Control for Group A6**
23	RO	0	**Reserved**
22:20	RW	0	**DQ/DQS Delay Control for Group A5**
19	RO	0	**Reserved**
18:16	RW	0	**DQ/DQS Delay Control for Group A4**
15	RO	0	**Reserved**
14:12	RW	0	**DQ/DQS Delay Control for Group A3**
11	RO	0	**Reserved**
10:8	RW	0	**DQ/DQS Delay Control for Group A2**
7	RO	0	**Reserved**
6:4	RW	0	**DQ/DQS Delay Control for Group A1**
3	RO	0	**Reserved**
2:0	RW	0	**DQ/DQS Delay Control for Group A0**

Offset Address: F9-F4 (D0F3) – Reserved

DDR2 – DQ De-Skew Control (FA–FFh)

Offset Address: FAh (D0F3)

DQ De-Skew Function Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Enable DQ Input De-Skew Circuit** 0: Disable 1: Enable
6	RW	0	**Manual DQ Output Delay Setting** 0: Auto 1: Manual
5	RW	0	**Manual DQ Input Delay Setting** 0: Auto 1: Manual
4	RW	0	**Manual Setting for RX / TX Select** 0: RX 1: TX
3	RW	0	**Manual Setting DQ Channel Select** 0: Channel A 1: Channel B
2:0	RW	000b	**Manual Setting DQ Group Select** 000: DQ[7:0] 001: DQ[15:8] … 110: DQ[55:48] 111: DQ[63:56]

Offset Address: FBh (D0F3)

DQS Delay Control **Default Value: 30h**

Bit	Attribute	Default	Description
7	W/R0	0	**Bypass DQ / DQS Delay in CKG** 0: Disable 1: Enable
6:4	W/R0	011b	**EPLL Feed-Back Clock Tree Delay Control** Each bit for 60ps 000: No delay 001: Delay 60ps 010: Delay 120ps 011: Delay 180ps .i: Delay i*60 ps
3:0	RW	0	**DQS Delay Setting** Use with FA[4:0] to set DQS input / output delay value (binary, 25ps/step) to a DQS bit. The reading value depends on RxFA[6:4]. If RxFA[5]=0 (auto mode), PD compensation result is returned when read.

Offset Address: FC-FFh (D0F3)

DQ Delay Setting **Default Value: 00h**

Bit	Attribute	Default	Description
31:0	RW	0	**DQ Delay Setting** Use with FA[4:0] to set DQ input / output delay value (binary, 25ps/step) to a DQ group. The reading value depends on RxFA[6:4]. If RxFA[5]=0 (auto mode), PD compensation result is returned when read.

Note: DQ de-skew function operating procedure

1. Set DRAM in low-speed mode; prepare training data in DRAM
2. Set RxFA[5]=0 (auto mode), set RxFA[7]=1 (PD enable)
3. Read training data from DRAM
4. Set RxFA[7]=0 (PD disable)
5. Configuration read RxFB[3:0], RxFC-FF for each DQ group
6. Set RxFA[4]=0, configuration write RxFB[3:0], RxFC-FF for each DQ group
7. Set RxFA[4]=1, configuration write RxFB[3:0], RxFC-FF for each DQ group
8. Set RxFA[6]=1 (manual mode)

Device 0 Function 4 (D0F4): Power Management Control

Header Registers (0-3Fh)

Offset Address: 1-0h (D0F4)
Vendor ID — **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**Vendor ID**

Offset Address: 3-2h (D0F4)
Device ID — **Default Value: 4364h**

Bit	Attribute	Default	Description
15:0	RO	4364h	**Device ID**

Offset Address: 5-4h (D0F4)
PCI Command — **Default Value: 0006h**

Bit	Attribute	Default	Description
15:0	RO	0006h	**PCI Command**

Offset Address: 7-6h (D0F4)
PCI Status — **Default Value: 0020h**

Bit	Attribute	Default	Description
15:0	RO	0020h	**PCI Status**

Offset Address: 8h (D0F4)
Revision ID — **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Revision ID**

Offset Address: 0B-9h (D0F4)
Class Code — **Default Value: 06 0000h**

Bit	Attribute	Default	Description
23:0	RO	060000h	**Class Code**

Offset Address: 0Ch (D0F4) – Reserved

Offset Address: 0Dh (D0F4)
Latency Timer — **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Latency Timer**

Offset Address: 0Eh (D0F4)
Header Type — **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Header Type**

Offset Address: 0Fh (D0F4)
BIST **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**BIST**

Offset Address: 13-10h (D0F4) – Reserved

Offset Address: 2D-2C (D0F4)
Subsystem Vendor ID **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW1	0	**Subsystem Vendor ID**

Offset Address: 2F-2E (D0F4)
Subsystem ID **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW1	0	**Subsystem ID**

Offset Address: 33-30 (D0F4) – Reserved

Offset Address: 34 (D0F4)
Capability Pointer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Capability Pointer** – byte offset into configuration space to capability list

Offset Address: 3F-35 (D0F4) – Reserved

Offset Address: 8F-40h (D0F4) – Reserved

New Power Management Control (9F-90h)

Offset Address: 90h (D0F4)
New Power Management Mode **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Dynamic Clock Enable of PXPTRF** 0: Disable 1: Enable
6	RW	0	**Dynamic Clock Enable of CCLK** 0: Disable 1: Enable
5	RW	0	**Dynamic Clock Enable of GCLK** 0: Disable 1: Enable
4	RW	0	**Dynamic Clock Enable of ECLK** 0: Disable 1: Enable
3	RW	0	**Dynamic Clock Enable of DCLK** 0: Disable 1: Enable
2:0	RO	0	**Reserved**

Offset Address: 9F-91h (D0F4) – Reserved

Power Management Control (A0–AFh)

Offset Address: A0h (D0F4)

Power Management Mode **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Dynamic Power Management** 0: Disable 1: Enable
6	RW	0	**Power Management during HALT / SHUTDOWN** 0: Disable 1: Enable
5	RW	0	**Power Management during STPCLK** 0: Disable 1: Enable
4	RW	0	**Power Management during SUSSTAT** 0: Disable 1: Enable
3:0	RO	0	**Reserved**

Offset Address: A1h (D0F4)

DRAM Power Management **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Enable DRAM Self-Refresh During Power-Management Mode** 0: Disable 1: Enable
6	RW	0	**Dynamic CKE When DRAM Idle** 0: Disable 1: Enable Note: Before entering STR Mode, please turn off this bit.
5	RW	0	**Dynamic DRAM I/O Pad Power-Down** (i.e. float) 0: Disable 1: Enable
4:0	RO	0	**Reserved**

Note: The DRAM power management mode is defined as HALT / SHUTDOWN, STPCLK and SUSSTAT triggered

Offset Address: A2h (D0F4)

Dynamic Clock Stop Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Host Interface Power Management** 0: Disable 1: Enable
6	RW	0	**DRAM Interface Power Management** 0: Disable 1: Enable
5	RW	0	**V-Link Interface Power Management** 0: Disable 1: Enable
4	RW	0	**AGP Interface Power Management** 0: Disable 1: Enable
3	RW	0	**PCI2 Interface Power Management** 0: Disable 1: Enable
2	RW	0	**Graphics Interface (GMINT) Power Management** 0: Disable 1: Enable
1	RW	0	**VKCFG Interface Power Management** 0: Disable 1: Enable
0	RW	0	**Host Fast Power-Management (DADS Fast Timing)** 0: Disable 1: Enable

Offset Address: A3h (D0F4)
P6IF Dynamic Clock Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Using BREQ to Predict CPU Transaction and Do More Aggressive Dynamic Clock** This clock basically replaces nearly all free-running clock inside P6IF. 0: Disable 1: Enable
6	RW	0	**Wait up RRDY Clock for DRAM Controller** 0: Disable 1: Enable
5	RW	0	**Enable Host C2P Clock Gating** 0: Disable 1: Enable
4	RW	0	**Enable Dynamic Clock Gating for C2P1 Transaction Inside P6IF** 0: Disable 1: Enable
3	RW	0	**Enable Dynamic Clock Gating for C2P2 Transaction Inside P6IF** 0: Disable 1: Enable
2	RW	0	**Enable Host P2C Clock Gating** 0: Disable 1: Enable
1	RW	0	**Turn off Register Initialization Logic after Chip Power-On Completed** 0: Disable 1: Enable
0	RW	0	**Enable Dynamic Gating Clock Phase Signal** Reserved 0: Disable 1: Enable

Offset Address: A4h (D0F4)
DRAM Dynamic Clock Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Enable DRAMC Read Clock Gating** 0: Disable 1: Enable
6	RW	0	**Enable DRAMC Write Clock Gating** 0: Disable 1: Enable
5	RW	0	**Enable DRAMC Page Table Clock Gating** 0: Disable 1: Enable
4	RW	0	**Enable DRAMC GART TLB Clock Gating** 0: Disable 1: Enable
3	RW	0	**Enable Latch Queue Write-Enable Dynamic Clock Gating Inside P6IF, Including IOQ, PWQ and PAQ** 0: Disable 1: Enable
2	RW	0	**Enable DIO and PAD Related Dynamic Clock Gating, Including 2X in/out CCLK and 1X Clock for PAD** 0: Disable 1: Enable
1	RW	0	**Enable Dynamic MA/SCMD Clock on MA/SCMD Pads** 0: Disable 1: Enable
0	RW	0	**Enable DBX CMFIFO PUSH Dynamic Clock** 0: Disable 1: Enable

Offset Address: A5h (D0F4)
V-Link Dynamic Clock Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6	RW	0	**Enable PCIC P2C Clock Gating** 0: Disable 1: Enable
5	RW	0	**Enable PCIC P2P Clock Gating** 0: Disable 1: Enable
4	RW	0	**Enable PCIC C2P Clock Gating** 0: Disable 1: Enable
3:0	RO	0	**Reserved**

Offset Address: A6h (D0F4)
GMINT Dynamic Clock Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Enable GMINT Dynamic Clock** 0: Disable 1: Enable
6	RW	0	**Enable GMINT Read Clock Gating** 0: Disable 1: Enable
5	RW	0	**Enable GMINT Write Clock Gating** 0: Disable 1: Enable
4	RW	0	**Power down the AGP Pads' Input Differential Comparator when Idle** 0: Disable 1: Enable
3	RW	0	**Enable NVC Dynamic Clock** 0: Disable 1: Enable
2	RW	0	**Enable AGPCINT Dynamic Clock** 0: Disable 1: Enable
1	RW	0	**Enable GPCI Dynamic Clock** 0: Disable 1: Enable
0	RW	0	**Enable DBX Dynamic Clock** 0: Disable 1: Enable

Offset Address: A7h (D0F4)
Enable System Memory Self-Refresh with Frame Buffer Being Pre-Charged **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3	RW	0	**Enable System Memory Self-Refresh with Frame Buffer Being Pre-Charged** 0: Disable 1: Enable
2:0	RO	0	**Reserved**

Offset Address: A8h (D0F4)
C0T PMU Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Enable C0 Throttling State** 0: Disable 1: Enable
6	RW	0	**Enable DIMM Self-Refresh in C0T State with GFX in D3 State** 0: Disable 1: Enable
5	RW	0	**Enable DIMM Self-Refresh in C0T State with GFX in Vertical Blanking** 0: Disable 1: Enable
4	RW	0	**Enable Non-Page Mode in C0T** 0: Disable 1: Enable
3	RW	0	**Enable DRAM Throttle in C0T** 0: Disable 1: Enable
2	RW	0	**Disable PLL in C0T State with GFX_ENGC3ST || GFX_VBLANK**
1	RW	0	**Disable PLL in C0T State When Internal GFX Enters D3 State**
0	RO	0	**Reserved**

Offset Address: A9h (D0F4)
C1 PMU Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Enable C1 Throttling State** 0: Disable 1: Enable
6	RW	0	**Enable DIMM Self-Refresh in C1 State with GFX in D3 State** 0: Disable 1: Enable
5	RW	0	**Enable DIMM Self-Refresh in C1 State with GFX in Vertical Blanking** 0: Disable 1: Enable
4	RW	0	**Enable Non-Page Mode in C1** 0: Disable 1: Enable
3	RW	0	**Enable DRAM Throttle in C1** 0: Disable 1: Enable
2	RW	0	**Disable PLL in C1 State with GFX_ENGC3ST || GFX_VBLANK**
1	RW	0	**Disable PLL in C1 State When Internal GFX Enters D3 State**
0	RO	0	**Reserved**

Offset Address: AAh (D0F4)

C2 PMU Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Enable C2 Throttling State** 0: Disable 1: Enable
6	RW	0	**Enable DIMM Self-Refresh in C2 State with GFX in D3 State** 0: Disable 1: Enable
5	RW	0	**Enable DIMM Self-Refresh in C2 State with GFX in Vertical Blanking** 0: Disable 1: Enable
4	RW	0	**Enable Non-Page Mode in C2** 0: Disable 1: Enable
3	RW	0	**Enable DRAM Throttle in C2** 0: Disable 1: Enable
2	RW	0	**Disable PLL in C2 State with GFX_ENGC3ST || GFX_VBLANK**
1	RW	0	**Disable PLL in C2 State When Internal GFX Enters D3 State**
0	RO	0	**Reserved**

Offset Address: ABh (D0F4)

C3 PMU Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Enable C3 Throttling State** 0: Disable 1: Enable
6	RW	0	**Enable DIMM Self-Refresh in C3 State with GFX in D3 State** 0: Disable 1: Enable
5	RW	0	**Enable DIMM Self-Refresh in C3 State with GFX in Vertical Blanking** 0: Disable 1: Enable
4	RW	0	**Enable Non-Page Mode in C3** 0: Disable 1: Enable
3	RW	0	**Enable DRAM Throttle in C3** 0: Disable 1: Enable
2	RW	0	**Disable PLL in C3 State with GFX_ENGC3ST || GFX_VBLANK**
1	RW	0	**Disable PLL in C3 State When Internal GFX Enters D3 State**
0	RO	0	**Reserved**

Offset Address: ACh (D0F4)

C3D PMU Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Enable C3D Throttling State** 0: Disable 1: Enable
6	RW	0	**Enable DIMM Self-Refresh in C3D State with GFX in D3 State** 0: Disable 1: Enable
5	RW	0	**Enable DIMM Self-Refresh in C3D State with GFX in Vertical Blanking** 0: Disable 1: Enable
4	RW	0	**Enable Non-Page Mode in C3D** 0: Disable 1: Enable
3	RW	0	**Enable DRAM Throttle in C3D** 0: Disable 1: Enable
2	RW	0	**Disable PLL in C3D State with GFX_ENGC3ST || GFX_VBLANK**
1	RW	0	**Disable PLL in C3D State When Internal GFX Enters D3 State**
0	RO	0	**Reserved**

Offset Address: AE-ADh (D0F4)

ACPI I/O Base **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW	0	**ACPI I/O Base** P6IF knows LVL2 (RxAE-AD + 14h) register is read

Offset Address: AFh (D0F4)
New PMU Feature **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**New V-Link Reconnecting Protocol**
6:4	RO	0	**Reserved**
3	RW	0	**Reduce GFX Lower Bound for Accumulating More Frame-Buffer Requests** 0: Disable 1: Enable
2:0	RO	0	**Reserved**

Offset Address: B1-B0h (D0F4) – Reserved

Offset Address: B2h (D0F4)
MA/SCMD Pad Toggle Reduction **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Enable MA/SCMD Toggle Reduction, i.e. MA/SCMD Not Switch If Not Accessed** 0: Disable 1: Enable
6:0	RO	0	**Reserved**

Offset Address: B3h (D0F4) – Reserved

Offset Address: B4h (D0F4)
Host Pad Dynamic Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**When turned on, it will dynamic enable input differential buffer for HD pad.** 0: Disable 1: Enable
6	RW	0	**When turned on, it will use BREQ to dynamic enable input differential buffer for HA and HREQ pad.** Refer to D0F2 Rx7D[0] and D0F2 Rx67[6]. 0: Disable 1: Enable
5	RW	0	**Enable Report PMU Status to I/O Port D0F4 RxB5[7:0]** Set to 0 in normal mode. 0: Disable 1: Enable
4:0	RO	0	**Reserved**

Offset Address: B5h (D0F4)
PMU Debug Base **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Define I/O Address Where the Debug Card Located**

Offset Address: B7-B6h (D0F4) – Reserved

Offset Address: B8h (D0F4)
Dynamic Clock Stop for New Modules **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Enable Dynamic Clock STOP for PEG Port for PHY** 0: Disable 1: Enable
6	RW	0	**Enable Dynamic Clock STOP for PE0 Port for PHY** 0: Disable 1: Enable
5	RW	0	**Enable Dynamic Clock STOP for PXPTRF (Central Traffic Controller)** 0: Disable 1: Enable
4	RW	0	**Enable Dynamic Clock STOP for PEG Port** 0: Disable 1: Enable
3:1	RO	0	**Reserved**
0	RW	0	**Enable Dynamic Clock STOP for PE0 Port** 0: Disable 1: Enable

Offset Address: BA-B9h (D0F4)

System Power Management **Default Value: 0400h**

Bit	Attribute	Default	Description
15	RW	0	**C2 Gate Free Running Clock** 0: Disable 1: Enable
14	RW	0	**C3 Gate Free Running Clock** 0: Disable 1: Enable
13	RO	0	**Reserved**
12	RW	0	**C3 When GFX Has Entered D3 Status Disable PLL** 0: Disable 1: Enable
11:8	RW	4h	**PLL STABLE Counter**
7:0	RW	0	**PLL STABLE Counter (Unit: 15ns)**

Offset Address: CF-BBh (D0F4) – Reserved

Device 0 Function 5 (D0F5): APIC and Central Traffic Control

Header Registers (0–3Fh)

Offset Address: 1-0h (D0F5)
Vendor ID — **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**Vendor ID**

Offset Address: 3-2h (D0F5)
Device ID — **Default Value: 5364h**

Bit	Attribute	Default	Description
15:0	RO	5364h	**Device ID**

Offset Address: 5-4h (D0F5)
PCI Command — **Default Value: 0006h**

Bit	Attribute	Default	Description
15:0	RO	0006h	**PCI Command**

Offset Address: 7-6h (D0F5)
PCI Status — **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RO	0	**PCI Status**

Offset Address: 8h (D0F5)
Revision ID — **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Revision ID**

Offset Address: 0B-9h (D0F5)
Class Code — **Default Value: 08 0020h**

Bit	Attribute	Default	Description
23:0	RO	080020h	**Class Code**

Offset Address: 0Ch (D0F5) – Reserved

Offset Address: 0Dh (D0F5)
Latency Timer — **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Latency Timer**

Offset Address: 0Eh (D0F5)
Header Type — **Default Value: 80h**

Bit	Attribute	Default	Description
7:0	RO	80h	**Header Type**

Offset Address: 0Fh (D0F5)
BIST **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**BIST**

Offset Address: 13-10h (D0F5) – Reserved

Offset Address: 2D-2C (D0F5)
Subsystem Vendor ID **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW1	0	**Subsystem Vendor ID**

Offset Address: 2F-2E (D0F5)
Subsystem ID **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW1	0	**Subsystem ID**

Offset Address: 33-30 (D0F5) – Reserved

Offset Address: 34 (D0F5)
Capability Pointer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Capability Pointer**

Offset Address: 3F-35 (D0F5) – Reserved

Legacy APIC Base I/O Registers (40–5Fh)

Offset Address: 40h (D0F5)
APIC Legacy Configuration **Default Value: 4Ch**

Bit	Attribute	Default	Description
7	RW	0	**Legacy APIC** 0: Disable 1: Enable. Range FECxyz00 to FECxyzFF, where x,y,z are defined in Rx40[3:0] and Rx41[7:0].
6	RO	1b	**Reserved** (Do Not Program)
5	RW	0	**Issues MSI Cycle for the Interrupt Deassertions** 0: Disable. There will be no corresponding MSI cycle for IRQ deassertion. 1: Enable. IRQ assertion and de-assertion will both issue MSI cycle out.
4	RO	0	**Reserved**
3:0	RW	Ch	**APIC Legacy Address Range - x**

Offset Address: 41h (D0F5)
APIC Legacy Address Range – y / z **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**APIC Legacy Address Range - y**
3:0	RW	0	**APIC Legacy Address Range - z**

Offset Address: 42h (D0F5)

APIC Interrupt Control **Default Value: 03h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3	RW	0	**Disable INTx Transparent Mode** 0: Enable Transparent mode 1: Disable Transparent mode
2	RW	0	**APIC Nonshare Mode Enable**
1	RW	1b	**Interrupt Disable Function of the APIC Module** 0: Disable 1: Enable
0	RW	1b	**Boot Interrupt Function** 0: Disable 1: Enable

Offset Address: 43h (D0F5) – Reserved

Offset Address: 44h (D0F5)

Miscellaneous Control **Default Value: 02h**

Bit	Attribute	Default	Description
7	RW	0	**PCIe Upstream Cycle Reduces 1T** 0: PCIe upstream cycle does not reduce 1T. 1: PCIe upstream cycle reduces 1T.
6:5	RO	0	**Reserved**
4	RW	0	**Hot-Plug Toggle** 0: PEHPSCI cannot be toggled when PCIe card is plugged in. 1: PEHPSCI can be toggled when PCIe card is plugged in.
3	RW	0	**Upstream MSI Cycle Flushes the Upstream VC1 Write** 0: Disable 1: Enable
2	RW	0	**Reserved**
1	RW	1b	**DV1 Enable** 0: Disable 1: Enable
0	RW	0	**APIC Data Voltage for CPU Voltage Select** 0: 2.5V 1: 1.5V

Offset Address: 5F-45h (D0F5) – Reserved

Central Traffic - Downstream Control (60–7Fh)

Offset Address: 60h (D0F5)

Extended CFG Address Support **Default Value: 20h**

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved**
5	RW	1b	**Convert Device2 CF8 Cycles to Device1 while Passing it to the SB** (in PCIe Mode) 0: CF8 access cycles are passed to the SB normally. 1: CF8 with data[15:11]=00010 will be changed to data[15:11]=00001.
4	RW	0	**CF8 Byte Write Enable** 0: Only supports CF8 write with all BE active. 1: Allow CF8 write with partial BE active.
3	RW	0	**For Device 2 and Device 3, Configuration Cycles to the Secondary Bus behind the P2P Bridge** 0: Configuration cycles for all the devices will be passed through. 1: Only configuration cycles for device 0 will be passed to the secondary bus, configuration cycles for device 1 and above will be passed to SB.
2	RO	0	**Reserved**
1:0	RW	00b	**Extended CFG Mode** 00: Extended CFG mode is off 01: Reserved 10: Capability header for extended configuration address support 11: Memory mapped extended CFG address supported (Rx61[7:0] should also be programmed.)

Offset Address: 61h (D0F5)
Memory Mapped Extended CFG Address **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Extended Configuration Address - A[35:28]** 00h: No extended configuration address. Else: Extended configuration address A[35:28] from host side.

Offset Address: 63-62h (D0F5) – Reserved

Offset Address: 64h (D0F5)
Miscellaneous **Default Value: 33h**

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved**
5	RW	1b	**Upstream MSI Cycles Force Flush of the Queued P2C Write Data** 0: Disable 1: Enable Note: Upstream MSI cycles include FEEx_xxxx from the internal APIC and cycles with address as programmed in D2, D3F0 Rx74-7B
4	RW	1b	**Downstream C2P Forces Flush of the Upstream P2C Write to the Host Side before Return LRDY to the Host Side** 0: Disable 1: Enable Note: C2P Downstream cycles include MEMR, IOR and IOW
3:2	RO	0	**Reserved**
1	RW	1b	**Downstream Write Request Timing** 0: Waits for the write data to issue downstream request. 1: Issues downstream request once request from the host is received
0	RW	1b	**Traffic Controller Downstream Cycles Are Processed in Order** 0: Disable. Downstream post write transaction will not be issued out until the data phase of the previous read transaction is finished. 1: Enable. Downstream post write transaction can be issued out before the completion of the data phase of the previous read transaction.

Offset Address: 65h (D0F5) – Reserved

Offset Address: 66h (D0F5)
Miscellaneous **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Trusted Configuration Space Base Address**

Offset Address: 67h (D0F5) – Reserved

Offset Address: 6B-68h (D0F5)
Memory Mapped Extended RCRB-H Base Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RO	0	**Reserved**
23:0	RW	0	**RCRB-H Base Address**

Offset Address: 6F-6Ch (D0F5)
Memory Mapped Extended RCRB-V Base Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RO	0	**Reserved**
23:0	RW	0	**RCRB-V Base Address**

Offset Address: 7F-70h (D0F5) – Reserved

Central Traffic - Upstream Control (80-85h)

Offset Address: 80h (D0F5)

Central Traffic-Upstream Control **Default Value: 95h**

Bit	Attribute	Default	Description
7	RO	1b	**PCI Express Graphic Device Support** 0: AGP interface supported 1: PCI Express (PEG Port) interface supported
6	RW	0	**VC1 Upstream Path** 0: VC1 requests are forwarded to the host side (snoop). 1: VC1 requests are forwarded to the DRAMC side.
5	RW	0	**CPU-to-DRAM Post Write FIFO Snoop Policy for Upstream Request to DRAMC** 0: Upstream requests are sent to DRAMC directly. 1: Upstream requests to DRAMC have to wait for the snoop result.
4	RW	1b	**AGP Upstream Path** 0: AGP requests are forwarded to the host side (snoop) 1: AGP requests are forwarded to the DRAMC side (non snoop)
3	RW	0	**Upstream Request 1T Earlier** 0: Normal latency for upstream request. 1: Reduced 1T latency for upstream request.
2	RW	1b	**Host Side Upstream Write** Transaction end with 1T earlier notice. 0: Disable 1: Enable
1	RW	0	**Host Side Upstream Read Data Returning Path** 0: 2 levels of synchronous FIFO 1: 1 level synchronous FIFO
0	RW	1b	**Host Side Upstream Write, Data Return with a 1T Notice** 0: Disable 1: Enable

Offset Address: 81h (D0F5)

PCIe Upstream/Downstream Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved**
5	RW	0	**Downstream to PCIe Initial Write Ready Asserted 1T Earlier** 0: Disable 1: Enable
4:0	RO	0	**Reserved**

Offset Address: 82h (D0F5)

Central Traffic Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved**
5	RW	0	**PCIe VC1 Read/Write Ordering Rule** 0: Obey PCIe VC1 read/write ordering rule 1: PCIe VC1 read cycle can pass VC1 write cycle
4	RW	0	**PCIe VC1 Command Rate** 0: PCIe VC1 read/write 2T command rate 1: PCIe VC1 read 2T command rate, but write 1T command rate
3	RW	0	**AGP Read/Write Ordering Rule** 0: Obey AGP read/write ordering rule 1: AGP read cycle can pass AGP write cycle
2	RW	0	**AGP Read/Write Command Rate** 0: AGP read/write 2T command rate 1: AGP read 2T command rate, but, write 1T command rate
1	RW	0	**Fair Arbitration Latency for the Host Side Arbitration Unit at RCRB-H Rx230-23D** 0: 2T 1: 1T
0	RW	0	**Port Arbitration Latency for the Port Arbitration Unit at RCRB-H 210-219** 0: 2T 1: 1T

Offset Address: 9F-83h (D0F5) – Reserved

PCIe Message Controller and Power Management (A0–F0h)

Offset Address: A0h (D0F5)

PCIe PMU Control and Status **Default Value: 00h**

Bit	Attribute	Default	Description
7	RWS	0	**PEWAKE# Activation Control** 0: PEWAKE# function is disabled 1: PEWAKE# function is enabled
6	RW	0	**PEPMESCI# (System Control Interrupt) Activation Control** 0: PEPMESCI function is disabled 1: PEPMESCI function is enabled
5	RW	0	**PEHPSCI# (System Control Interrupt) Activation Control** 0: PEHPSCI# function is disabled 1: PEHPSCI# function is enabled
4	RW1C	0	**PEG L2L3 PME Acknowledge Status** 0: Disable 1: 1 indicates that upon RxF0[7] is set to 1. PEG goes to L2L3 ready state and PME_TO_ACK message has returned from the device at PEG.
3:1	RO	0	**Reserved**
0	RW1C	0	**PE0 L2L3 PME Acknowledge Status** 0: Disable 1: 1 indicates that upon RxF0[7] is set to 1. PE0 goes to L2L3 ready state and PME_TO_ACK message has returned from the device at PE0.

Offset Address: A1h (D0F5)

PCIe PMU Status **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**PM_PME Message Status** 0: No PM_PME message 1: At least one PM_PME message was received at the PCIe ports. Note: Wake up the system through either PEWAKE# or PEPMESCI# depends on the settings on RxA0[7:6].
6	RO	0	**Reserved**
5	RO	0	**Hot Plug Event Status** 0: No Hot Plug event 1: At least one Hot Plug event was received at the PCIe ports. Note: This event is triggered by RxA0[5] for PEHPSCI# activation control.)
4:0	RO	0	**Reserved**

Offset Address: A2h (D0F5)

PMU Downstream Address [15:8] **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	00h	**Downstream Address Bits [15:8]** This register is used for monitoring S3/S4/S5 downstream command. Refers to RxA3[7] for address [7].

Offset Address: A3h (D0F5)
PMU Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Downstream Address Bit [7]** This bit is used for monitoring S3/S4/S5 downstream command. Refers to RxA2 for address [15:8].
6:3	RO	0	**Reserved**
2	RW	0	**ARBDIS Signal Control** 0: Disable the ARBDIS signal 1: Enable the ARBDIS signal
1	RW	0	**AGPBSY Signal Control** 0: Disable the AGPBSY 1: Enable the AGPBSY
0	RW	0	**Monitor S3/S4/S5 Command** 0: Disable 1: Enable When enabled, the controller will monitor S3/S4/S5 commands (e.g. IOW 4005, 24h or 28h) in the following procedure: 1. The controller receives the STPGNT cycles from the CPU 2. The controller triggers MSGC to issue PME_TURNOFF message to PCIe devices (Dev2, Dev3) 3. The controller waits for the acknowledge from all the devices to issue the STPGNT cycle received in step 1 to SB.

Offset Address: EF-A4h (D0F5) – Reserved

Offset Address: F0h (D0F5)
PMU Control **Default Value: 62h**

Bit	Attribute	Default	Description
7	RW	0	**PCIe Device Power Management Control** 0: Disable 1: Enable Programmed this bit to 1 will trigger a PME_TURNOFF message to be sent to PEG and PE0, where devices are activated. This bit has to be programmed to 0 before it can be programmed to 1 again.
6	RW	1b	**Device 0 Function 6 Exists or Not**
5	RW	1b	**Device 2 Exists or Not**
4	RW	0	**Device 3 Function 3 Exists or Not**
3	RW	0	**Device 3 Function 2 Exists or Not**
2	RW	0	**Device 3 Function 1 Exists or Not**
1	RW	1b	**Device 3 Function 0 Exists or Not**
0	RW	0	**Reserved**

Offset Address: FF-F1h (D0F5) – Reserved

Device 0 Function 6 (D0F6): Scratch Registers

Header Registers (0–3Fh)

Offset Address: 1-0h (D0F6)
Vendor ID — **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**Vendor ID**

Offset Address: 3-2h (D0F6)
Device ID — **Default Value: 6364h**

Bit	Attribute	Default	Description
15:0	RO	6364h	**Device ID**

Offset Address: 5-4h (D0F6)
PCI Command — **Default Value: 0006h**

Bit	Attribute	Default	Description
15:0	RO	0006h	**PCI Command**

Offset Address: 7-6h (D0F6)
PCI Status — **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RO	0000h	**PCI Status**

Offset Address: 8h (D0F6)
Revision ID — **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Revision ID**

Offset Address: 0B-9h (D0F6)
Class Code — **Default Value: 06 000h**

Bit	Attribute	Default	Description
23:0	RO	060000h	**Class Code**

Offset Address: 0Ch (D0F6)- Reserved

Offset Address: 0Dh (D0F6)
Latency Timer — **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Latency Timer**

Offset Address: 0Eh (D0F6)
Header Type — **Default Value: 80h**

Bit	Attribute	Default	Description
7:0	RO	80h	**Header Type**

Offset Address: 0Fh (D0F6)
BIST **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**BIST**

Offset Address: 13-10h (D0F6) – Reserved

Offset Address: 2D-2Ch (D0F6)
Subsystem Vendor ID **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW1	0	**Subsystem Vendor ID**

Offset Address: 2F-2Eh (D0F6)
Subsystem ID **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW1	0	**Subsystem ID**

Offset Address: 33-30h (D0F6) – Reserved

Offset Address: 34h (D0F6)
Capability Pointer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Capability Pointer**

Offset Address: 3F-35h (D0F6) – Reserved

Scratch Registers (7F–40h)

Offset Address: 4F-40h (D0F6)
BIOS Scratch Register 1 **Default Value: 0h**

Bit	Attribute	Default	Description
127:0	RW	0	**BIOS Scratch Register**

Offset Address: 5F-50h (D0F6)
BIOS Scratch Register 2 **Default Value: 0h**

Bit	Attribute	Default	Description
127:0	RW	0	**BIOS Scratch Register**

Offset Address: 6F-60h (D0F6)
BIOS Scratch Register 3 **Default Value: 0h**

Bit	Attribute	Default	Description
127:0	RW	0	**BIOS Scratch Register**

Offset Address: 7F-70h (D0F6)
BIOS Scratch Register 4 **Default Value: 0h**

Bit	Attribute	Default	Description
127:0	RW	0	**BIOS Scratch Register**

Offset Address: BF-80h (D0F6) – Reserved

Hash Data Control Registers (C0–FFh) – Reserved

Device 0 Function 7 (D0F7): V-Link North Bridge and South Bridge Control

Header Registers (0–3Fh)

Offset Address: 1-0h (D0F7)
Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**Vendor ID**

Offset Address: 3-2h (D0F7)
Device ID **Default Value: 7364h**

Bit	Attribute	Default	Description
15:0	RO	7364h	**Device ID**

Offset Address: 5-4h (D0F7)
PCI Command **Default Value: 0006h**

Bit	Attribute	Default	Description
15:0	RO	0006h	**PCI Command**

Offset Address: 7-6h (D0F7)
PCI Status **Default Value: 0200h**

Bit	Attribute	Default	Description
15:0	RO	0200h	**PCI Status**

Offset Address: 8h (D0F7)
Revision ID **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Revision ID**

Offset Address: 0B-9h (D0F7)
Class Code **Default Value: 06 0000h**

Bit	Attribute	Default	Description
15:0	RO	060000h	**Class Code**

Offset Address: 0Ch (D0F7) - Reserved

Offset Address: 0Dh (D0F7)
Latency Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Latency Timer**

Offset Address: 0Eh (D0F7)
Header Type **Default Value: 80h**

Bit	Attribute	Default	Description
7:0	RO	80h	**Header Type**

Offset Address: 0Fh (D0F7)
BIST **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**BIST**

Offset Address: 13-10h (D0F7) – Reserved

Offset Address: 2D-2Ch (D0F7)
Subsystem Vendor ID **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW1	0	**Subsystem Vendor ID**

Offset Address: 2F-2Eh (D0F7)
Subsystem ID **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW1	0	**Subsystem ID**

Offset Address: 33-30h (D0F7)
Reserved **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**Reserved**

Offset Address: 34h (D0F7)
Capability Pointer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Capability Pointer – byte offset into configuration space to capability list**

Offset Address: 3F-35h (D0F7) – Reserved

V-Link Control Interface (40–6Fh)

Offset Address: 40h (D0F7)
V-Link Specification ID **Default Value: 70h**

Bit	Attribute	Default	Description
7:0	RO	70h	**Revision ID**

Offset Address: 41h (D0F7)
NB V-Link Capability **Default Value: 19h**

Bit	Attribute	Default	Description
7	RW	0	**PEPMESCI, PEHPSCI and BUSY Special Command Translated to SB Support** 0: Not supported 1: Supported
6	RW	0	**Downstream DAC Cycle Supported** 0: Disable 1: Enable
5	RO	0	**Reserved**
4	RO	1b	**8-Bit Width** 0: Not supported 1: Supported
3	RO	1b	**4X Rate** 0: Not supported 1: Supported
2	RO	0	**2X Rate** 0: Not supported 1: Supported
1	RO	0	**Reserved**
0	RO	1b	**8X Rate** 0: Not supported 1: Supported

Offset Address: 42h (D0F7)
NB Downlink (C2P) Configuration **Default Value: 88h**

Bit	Attribute	Default	Description
7:4	RW	1000b	**C2P, DNCMD, Maximum Pending Request Depth** Maximum # of pending DNCMD, C2P, requests. 0000: 1 level 0001: 1 levels 0010: 2 levels 0011: 3levels … 1000: 8 levels …
3:0	RW	1000b	**C2P Maximum Write Buffer Size (from 1 to 16 DW)** 0000: 1 DW 0010: 2 DW 0011: 3 DW 0100: 4 DW … 1000: 9 DW … 1111: 16 DW

Offset Address: 43h (D0F7)
NB Uplink (P2C) Status 1 **Default Value: 88h**

Bit	Attribute	Default	Description
7:4	RO	8h	**P2C, UPCMD, Maximum Pending Request Depth** 0: 16 levels 1: 1 level ... n: n levels, where 0 < n <= 0Fh
3	RW	1b	**P2P Cycle Control** 0: P2P cycle using P2C cmd will not be discarded. 1: P2P cycle using P2C cmd from SB is discarded.
2:0	RO	0	**Reserved**

Offset Address: 44h (D0F7)
NB Uplink (P2C) Status 2 **Default Value: 82h**

Bit	Attribute	Default	Description
7:4	RO	1000b	**P2C Write Buffer Size (max # of lines)** 0000: 16 lines (64 QW) 0001: 1 line (4 QW) … 1000: 8 lines (32 QW) … 1111: 15 lines (60 QW)
3:0	RO	2h	**P2P Write Buffer Size (max # of lines)** 0000: 0 line (0 QW) 0001: 1 line (4 QW) 0010: 2 lines (8 QW) Others: Reserved

Offset Address: 45h (D0F7)

NB V-Link Arbiter Timer **Default Value: 44h**

Bit	Attribute	Default	Description
7:4	RW	0100b	**V-Link Arbiter Timer for Normal Priority Request from SB** 0000: 0 VCLK 0001: 1*4 VCLK 0010: 2*4 VCLK 0011: 3*4 VCLK 0100: 4*4 VCLK … 1000: 8*4 VCLK 1001: 16*4 VCLK 1010: 32*4 VCLK 1011: 64*4 VCLK 11xx: NB holds the bus as long as there is pending downstream request
3:0	RW	0100b	**V-Link Arbiter Timer for High Priority Request from SB** 0000: 0 VCLK 0001: 1*2 VCLK 0010: 2*2 VCLK 0011: 3*2 VCLK 0100: 4*2 VCLK … 1000: 8*2 VCLK 1001: 16*2 VCLK 1010: 32*2 VCLK 1011: 64*2 VCLK 11xx: NB holds the bus as long as there is pending downstream request Note: See "NB V-Link Bus Arbitration" table for more details.

Table 17. NB V-Link Bus Arbitration

Rx45[7:4]	Rx45[3:0]	SB Request Priority	NB When to Relinquish the Occupied V-Link Bus
0000	xxxx	Normal / High	Immediately
0001,0010,…	0000	High	Immediately
0001,0010,…	0001,0010,…	High	Wait for either Normal or High timer expired
0001,0010,…	00xx	Normal	Wait for Normal timer expired
0001,0010,…	11xx	Normal / High	Wait for Normal timer expired
11xx	0000	High	Immediately
11xx	0000	Normal	Wait until no more pending downstream request
11xx	0001,0010,…	High	Wait for High timer expired
11xx	0001,0010,…	Normal	Wait until no more pending downstream request
11xx	11xx	Normal / High	Wait until no more pending downstream request

Offset Address: 46h (D0F7)

NB V-Link Miscellaneous Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Downstream Read Data Return High Priority** 0: High priority down command disable 1: High priority down command enable
6	RW	0	**C2P High Priority** 0: C2P cycle treat as normal priority 1: C2P cycle treat as high priority Note: To enable this function, bit 7 must be set to 1.
5:4	RW	00b	**Options of Combining Multiple STPGNT Cycles into a V-Link Command** 00: Compatible mode: a V-Link command per STPGNT cycle 01: Combines 2 STPGNT cycles into a V-Link command 10: Combines 3 STPGNT cycles into a V-Link command 11: Combines 4 STPGNT cycles into a V-Link command
3:2	RW	00b	**V-Link Master Read/Write Access Ordering Rules** 00: High Priority Read allows to pass Normal Read (but not pass Write) 01: Read (High/Normal) allows to pass Write (High Priority R>Normal Priority R>Write) 1x: Read / Write are executed in order
1	RW	0	**Read Around Write** 0: Read always pass Write, if bit 3 is 0. 1: Allows up to 8 Read-Around-Write cycles before flushing the pending write, if bit 3 is 0. **Read Around Write is disabled if bit 3 is set to 1.**
0	RW	0	**Generate the Snoop Results to SB** 1: Always generates compare result to SB 0: Disable passing compare result to SB when the P2CR cycle is still in NB in order to reduce the traffic on V-Link and avoid unnecessary condition

Table 18. Interpretation on Rx46[7:6]

Rx46[7]	Rx46[6]	P2CHR	C2P
0	0	Normal	Normal
1	0	Priority	Normal
1	1	Priority	Priority
0	1	Illegal	Illegal

Offset Address: 47h (D0F7)

NB V-Link Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Upstream High-Priority Write Request Stream** 0: No high-priority write request stream. 1: Enable support of high-priority write request stream. When V-Link is not operated at 8X (and above), the high-priority write request is always disabled no matter what the setting of this bit is.
6	RW	0	**Upstream High-Priority Read Request Stream** 0: No high-priority read request stream. 1: Enable high-priority read request stream.
5	RW	0	**C2P Read L1RDY Return Priority** 0: V-Link decodes C2P Read ACK command right when it's received. 1: C2P Read ACK command will be handled till pending P2C write cycles are all flushed.
4	RW	0	**CF8h Configuration Cycle Address Bit[27:24] Usage** 0: Normal PCI usage 1: Address bit[27:24] are used as extended register address bit[11:8]
3	RW	0	**Dynamic STOP on Down Strobe** 0: Disable 1: Enable
2	RW	0	**Auto-Disconnect** 0: Disable 1: Enable
1	RW	0	**V-Link Disconnect Sequence for STPGNT Cycle** 0: Disable 1: Enable
0	RW	0	**V-Link Disconnect Sequence for HALT Cycle** 0: Disable 1: Enable

Offset Address: 48h (D0F7)

V-Link Configuration – NB / SB **Default Value: 38h**

This register is used to configure V-Link bus controller on both North and South bridge chips.

Bit	Attribute	Default	Description
7	RW	0	**Parity Check** 0: Disable 1: Enable
6	RO	0	**Reserved**
5	RW	1b	**16-Bit Width** 0: Disable 1: Enable
4	RW	1b	**8-Bit Width** 0: Disable 1: Enable
3	RW	1b	**4X Rate** 0: Disable 1: Enable
2	RO	0	**Reserved**
1	RW	0	**V-Link Split Bus** 0: Disable 1: Enable
0	RW	0	**8X Rate** 0: Disable 1: Enable

Table 19. V-Link Data Transfer Modes

Mode	Speed (Multiples of 66MHz Cycle)	Data Size	Duplex	D0F7 Rx48[0] – 8X	D0F7 Rx48[5]	D0F7 Rx48[1] – Split Bus
0	4X	8-bit	Half Duplex	0	0	0
1	8X	4-bit	Full Duplex	1	0	1
2	8X	8-bit	Half Duplex	1	0	0
3	4X	16-bit	Half Duplex	0	1	0
4	8X	16-bit	Full Duplex	1	1	1

Offset Address: 49h (D0F7)
SB V-Link Capability **Default Value: 19h**

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved**
5	RO	0	**16-bit Bus Width Support** 0: Disable 1: Enable
4	RO	1b	**8-bit Width Support** 0: Disable 1: Enable
3	RO	1b	**4X Rate Support** 0: Disable 1: Enable
2	RO	0	**2X Rate Support** 0: Disable 1: Enable
1	RO	0	**Reserved**
0	RO	1b	**8X Rate Support** 0: Disable 1: Enable

Offset Address: 4Ah (D0F7)
SB Downlink (C2P) Status **Default Value: 88h**

Bit	Attribute	Default	Description
7:4	RO	1000b	**C2P Request Depth (max # of DNCMD (C2P) requests)** 0000: Depth of 1 0001: Depth of 2 0010: Depth of 3 … 1000: Depth of 9 … 1111: Depth of 16
3:0	RO	1000b	**C2P Write Buffer Size (max # of DW, depth from 1 to 16)** 0000: Depth of 1 0001: Depth of 2 0010: Depth of 3 … 1000: Depth of 9 … 1111: Depth of 16

Offset Address: 4Bh (D0F7)
SB Uplink (P2C) Command 1 **Default Value: 80h**

Bit	Attribute	Default	Description
7:4	RO	8h	**P2C Request Depth (max # of outstanding UPCMD (P2C) requests)**
3:0	RO	0	**Reserved**

Offset Address: 4Ch (D0F7)
SB Uplink (P2C) Command 2 **Default Value: 82h**

Bit	Attribute	Default	Description
7:4	RO	8h	**P2C Write Buffer Size (max # of lines)**
3:0	RO	2h	**P2P Write Buffer Size (max # of lines)**

Offset Address: 4Dh (D0F7)
SB V-Link Bus Timer **Default Value: 44h**

Bit	Attribute	Default	Description
7:4	RO	0100b	**Timer for Normal Priority Request from NB** 0000: Immediately 0001: 1*4 VCLK 0010: 2*4 VCLK 0011: 3*4 VCLK 0100: 4*4 VCLK … 1000: 8*4 VCLK 1001: 16*4 VCLK 1010: 32*4 VCLK 1011: 64*4 VCLK 11xx: Own the bus as long as there is request
3:0	RO	0100b	**Timer for High Priority Request from NB** 0000: Immediately 0001: 1*2 VCLK 0010: 2*2 VCLK 0011: 3*2 VCLK 0100: 4*2 VCLK … 1000: 8*2 VCLK 1001: 16*2 VCLK 1010: 32*2 VCLK 1011: 64*2 VCLK 11xx: Own the bus as long as there is request Note: See "NB V-Link Bus Arbitration" table for more details.

Offset Address: 4Eh (D0F7)
CCA Master High Priority **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**1394 High Priority**
6	RO	0	**NIC High Priority**
5	RO	0	**Reserved**
4	RO	0	**USB High Priority**
3	RO	0	**Reserved**
2	RO	0	**IDE High Priority**
1	RO	0	**AC97-ISA High Priority**
0	RO	0	**PCI1 High Priority**

Offset Address: 4Fh (D0F7)
SB V-Link Misc. Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Upstream Command High Priority** 0: High priority up command disable 1: High priority up command enable
6:4	RO	0	**Reserved**
3	RO	0	**Enable Dynamic STOP of Up Strobe**
2:1	RO	0	**Reserved**
0	RO	0	**C2P Cycle Wait for P2C Write Flush, Except C2P Post-Write**

Procedure to Enable / Disable V-Link-8X Mode:

1. BIOS sets Rx48[0] to 1.
2. Hardware will automatically enter a disconnect sequence, and then both NB/SB will start V-Link 8X mode. Then normal operation is then resumed.
3. To return to V-Link 4X mode, BIOS sets Rx48[0] to 0.
4. Step 2 is then repeated.

Offset Address: 56-50h (D0F7) – Reserved

Offset Address: 57h (D0F7)
Last Bank Ending **Default Value: 01h**

Bit	Attribute	Default	Description
7:0	RO	01h	**Last Bank Ending** Programmed to SB.

Offset Address: 60-58h (D0F7) – Reserved

Offset Address: 61h (D0F7)
C-ROM Shadow Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00b	**CC000-CFFFF** 00: Read/write disable 01: Write enable 10: Read enable 11: Read/write enable
5:4	RW	0	**C8000-CBFFFF**
3:2	RW	0	**C4000-C7FFFF**
1:0	RW	0	**C0000-C3FFFF**

Offset Address: 62h (D0F7)
D-ROM Shadow Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	0	**DC000-DFFFF**
5:4	RW	0	**D8000-DBFFF**
3:2	RW	0	**D4000-D7FFF**
1:0	RW	0	**D0000-D3FFF**

Offset Address: 63h (D0F7)
F-ROM, Memory Hole and SMI Decoding **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved**
5:4	RW	0	**F0000-FFFFF**
3:2	RW	00b	**Memory Hole** 00: None 01: 512K – 640K 10: 15M – 16M (1M) 11: 14M – 16M (2M)
1	RW	0	**Disable A,BK Direct Access SMRAM Direct Access**
0	RW	0	**Enable A,BK DRAM Access**

Offset Address: 64h (D0F7)
E-ROM Shadow Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	0	**EC000-EFFFF**
5:4	RW	0	**E8000-EBFFF**
3:2	RW	0	**E4000-E7FFF**
1:0	RW	0	**E0000-E3FFF**

Rx63[1]	Rx63[0]	CPUMODE	CODE	DATA
0	0	Norm	PCI	PCI
0	0	SMM	DRAM	DRAM
0	1	Norm	DRAM	DRAM
0	1	SMM	DRAM	DRAM
1	0	Norm	PCI	PCI
1	0	SMM	DRAM	PCI
1	1	Norm	DRAM	DRAM
1	1	SMM	DRAM	DRAM

Offset Address: 6F-65h (D0F7) – Reserved

Host-PCI Bridge Control (70-7Fh)

Offset Address: 70h (D0F7)

PCI Buffer Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**CPU to PCI Post-Write Enable** (both SB/NB) 0: Disable 1: Enable
6	RO	0	**Reserved**
5:4	RW	00b	**PCI Master to DRAM Prefetch Control** 00: Always prefetch 10: Prefetch only for enhanced command x1: Prefetch disable
3	RO	0	**Reserved**
2	RW	0	**PCI Master Read Buffering**
1	RW	0	**Delayed Transaction Enable**
0	RO	0	**Reserved**

Offset Address: 71h (D0F7)

CPU to PCI Flow Control **Default Value: 48h**

Bit	Attribute	Default	Description
7	W1C	0	**Retry Status** 0: No retry occurred 1: Retry occurred (write 1 to clear)
6	RW	1b	**Retry Timeout Action** 0: Retry forever (record status only) 1: Flush buffer or return FFFFFFFF for read
5:4	RW	00b	**Retry Count and Retry Backoff** 00: Retry 2 times, boff CPU 01: Retry 16 times 10: Retry 4 times 11: Retry 64 times
3	RW	1b	**PCI Burst Enable**
2	RO	0	**Reserved**
1	RW	0	**Compatible TYPE#1 Configuration Cycle AD31**
0	RW	0	**IDSEL Control** 0: AD11, AD12 1: AD30, AD31

Offset Address: 72h (D0F7) – Reserved

Offset Address: 73h (D0F7)

PCI Master Control #1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Read Buffering Scheme** 0: Use old PCI master read buffering scheme 1: Use new PCI master read buffering scheme
6	RW	0	**PCI master 1-Wait-State Write** 0: OWS 1: 1WS
5	RW	0	**PCI Master 1-Wait-State Read**
4	RW	0	**WSC# enable**
3:1	RO	0	**Reserved**
0	RW	0	**PCI Master Broken Timer Enable** 0: Disable 1: Enabled. Force into arbitration when there is no FRAME# 16 PCICLK after GNT

Offset Address: 74h (D0F7) – Reserved

Offset Address: 75h (D0F7)
PCI Arbitration 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Arbitration Mode** 0: REQ-based (arbitrate at end of REQ#) 1: Frame-based (arbitrate at FRAME# asserts)
6:4	RW	0	**CPU Latency MLT2, MLT1, MLT0**
3	RO	0	**Reserved**
2:0	RW	000b	**PCI Master Bus Time-Out** 000: Disable 001: 1 x 16 PCLK 010: 2 x 16 PCLKs 011: 3 x 16 PCLKs 111: 7 x 16 PCLKs

Offset Address: 76h (D0F7)
PCI Arbitration 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**SB I/O Port 22 Enable** 0: CPU access to I/O address 22h is passed on to the PCI bus 1: CPU access to I/O address 0022h is processed internally I/O
6	RO	0	**Reserved**
5:4	RW	00b	**Master Priority Rotation Control** 00: Disable 01: Grant to CPU after every PCI master grant 10: Grant to CPU after every 2 PCI master grant 11: Grant to CPU after every 3 PCI master grant
3:2	RW	00b	**Select REQ[n] as RQ4** 00: REQ4 01: REQ0 10: REQ1 11: REQ2
1	RO	0	**Reserved**
0	RW	0	**Enable RQ4 as High Priority Master** 0: Disable 1: Enable

Offset Address: 7F-77h (D0F7) – Reserved

GART Operation (80-9Fh)

Offset Address: 83-80h (D0F7) – Reserved

Offset Address: 84h (D0F7)
Graphic Aperture Size **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Graphic Aperture Size** In AGP20 mode, bit [7:0]: 0000 0000: 256M 0010 0000: 128M 0011 0000: 64M 0011 1000: 32M 0011 1100: 16M 0011 1110: 8M 0011 1111: 4M Note: Please set D17F7 Rx77[1]=1 and D17F7 Rx77[2]=0 to enable this function.

Offset Address: 87-85h (D0F7) – Reserved

Offset Address: 88h (D0F7)
Graphic Aperture Translation Look-Aside Table Base **Default Value: 00h**

Bit	Attribute	Default	Description
7:2	RO	0	**Reserved**
1	RW	0	**Enable GART Window Access**
0	RO	0	**Reserved**

Offset Address: 9F-89h (D0F7) – Reserved

V-Link Related Registers for North Bridges (A0-B7h)

Offset Address: A0h (D0F7)
NVC Configure **Default Value: 00h**

Bit	Attribute	Default	Description
7:2	RO	0	**Reserved**
1	RW	0	**Data Source of Some of the Configuration Read to D0F0 or D0F7** 0: Configuration read cycles to D0F0 or D0F7, some of the data will return from SB (like Rx05-06, Rx70-7F…). 1: Data of configuration read cycles to D0Fx will always return from NB.
0	RW	0	**While returning the P2C read ACK to SB, the NVC can start to issue the next read request to reduce the P2C read latency** 0: Disable 1: Enable

Offset Address: AF-A1h (D0F7) – Reserved

Offset Address: B0h (D0F7)
V-Link CKG Control **Default Value: A0h**

Bit	Attribute	Default	Description
7	RW	0	**Rising-Time Control for V-Link #1 (R-Port)**
6	RW	0	**Rising-Time Control for V-Link #0 (R-Port)**
5	RW	0	**Falling-Time Control for V-Link #1 (R-Port)**
4	RW	0	**Falling-Time Control for V-Link #0 (R-Port)**
3	RW	1b	**Rising-Time Control for V-Link #1 (S-Port)**
2	RW	0	**Rising-Time Control for V-Link #0 (S-Port)**
1	RW	1b	**Falling-Time Control for V-Link #1 (S-Port)**
0	RW	0	**Falling-Time Control for V-Link #0 (S-Port)**

Offset Address: B1h (D0F7)
V- Link CKG Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3	RW	0	**Rising-Time Control for V-Link #1 (D-Port)**
2	RW	0	**Rising-Time Control for V-Link #0 (D-Port)**
1	RW	0	**Falling-Time Control for V-Link #1 (D-Port)**
0	RW	0	**Falling-Time Control for V-Link #0 (D-Port)**

Offset Address: B2h (D0F7) – Reserved

Offset Address: B3h (D0F7)

V-Link Auto Compensation Termination Resistor Status **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved**
5	RO	0	**P Pull Down Driving Check Flag for the NB Termination Resistor** 0: Abnormal condition occurred 1: Normal operation.
4	RO	0	**N Pull Down Driving Check Flag for the NB Termination Resistor** 0: Abnormal condition occurred 1: Normal operation.
3	RO	0	**Reserved**
2:0	RO	000b	**NB V-Link Autocomp Termination Resistor Value** 000: Largest resistor … 111: Smallest resistor

V-Link North Bridge Driving Control (B4–B7h)

Offset Address: B4h (D0F7)

NB V-Link Compensation Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	**V-Link Auto-Compensation PMOS Output Value**
4	RO	0	**Reference Voltage of the VKCOMP in 4X V-Link Mode** 0: VREF4X=0.75V 1: VREF4X=0.9V
3:1	RO	0	**V-Link Auto-Compensation NMOS Output Value**
0	RO	0	**Compensation Option** 0: Use Auto Compensation (value is kept in bits [7:6]) 1: Use Manual setting (use the values of RxB5 and RxB6)

Offset Address: B5h (D0F7)

NB V-Link Manual Driving Control - Strobe **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RW	0	**Manual Setting - NB V-Link Strobe Pullup (PMOS)**
4	RO	0	**Reserved**
3:1	RW	0	**Manual Setting - NB V-Link Strobe Pulldown (NMOS)**
0	RO	0	**Reserved**

Offset Address: B6h (D0F7)

NB V-Link Manual Driving Control - Data **Default Value: 88h**

Bit	Attribute	Default	Description
7:5	RW	100b	**Manual Setting - NB V-Link Data Pullup (PMOS)**
4	RO	0	**Reserved**
3:1	RW	100b	**Manual Setting - NB V-Link Data Pulldown (NMOS)**
0	RO	0	**Reserved**

Offset Address: B7h (D0F7)
NB V-Link Receiving Strobe Delay **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RW	000b	**V-Link Manual Termination Resistor Value** 000: Largest resistor ... 111: Smallest resistor
4:3	RO	0	**Reserved**
2:0	RW	0	**NB V-Link Receiving Strobe Delay** Control relative delay between data/strobe input delay. 000: Delay(data) = delay(strobe) + 4*step 001: Delay(data) = delay(strobe) + 3*step 010: Delay(data) = delay(strobe) + 2*step 011: Delay(data) = delay(strobe) + 1*step 100: Delay(data) = delay(strobe) 101: Delay(data) + 1*step = delay(strobe) 110: Delay(data) + 2*step = delay(strobe) 111: Delay(data) + 3*step = delay(strobe) Each "step" is 100ps for ff-ss case of process.

V-Link South Bridge Driving Control (B8-B9h) - For 8X Capability SB

Offset Address: B8h (D0F7)
SB V-Link Compensation Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	**V-Link Auto-Compensation PMOS Output Value**
4:1	RO	0	**Reserved**
0	RW	0	**Compensation Selection** 0: Auto-compensation (value is kept in bits [7:5] and [3:1]) 1: Manual setting (through RxB9-BB)

Offset Address: B9h (D0F7)
SB V-Link Driving Control – Strobe **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RW	0	**SB V-Link Strobe Pullup Manual Setting - PMOS**
4	RO	0	**Reserved**
3:1	RW	0	**SB V-Link Strobe Pulldown Manual Setting - NMOS**
0	RO	0	**Reserved**

V-Link South Bridge Driving Control (B8-B9h) - For 4X Capability SB

Offset Address: B8h (D0F7)
SB V-Link Compensation Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RO	0	**V-Link Auto-Compensation Output Value**
5	RW	0	**Pull-up Compensation Selection** 0: Auto compensation (values in RxB8[7:6]) 1: Manual setting (use the values in RxB8[3:2])
4	RW	0	**Pull-down Compensation Selection** 0: Auto compensation (values in RxB8[7:6]) 1: Manual setting (use the values in RxB8[1:0])
3:2	RW	0	**Pull-up Compensation Manual Setting**
1:0	RW	0	**Pull-down Compensation Manual Setting**

Offset Address: B9h (D0F7)
SB V-Link Driving Control – Strobe **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RW	0	**SB V-Link Strobe Pullup Manual Setting**
4	RO	0	**Reserved**
3:1	RW	0	**SB V-Link Strobe Pulldown Manual Setting**
0	RO	0	**Reserved**

Offset Address: E3-BAh (D0F7) – Reserved

DRAM Above 4G Support (E4-EF)

Offset Address: E4h (D0F7)
Low Top Address - Low **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Low Top Address - Low**
3:0	RW	0	**DRAM Granularity - (Powell)** RMEMUNIT / Total DRAM Less than / Granularity 0: 4G / 16M 1: 8G / 32M 2: 16G / 64M 3: 32G / 128M 4: 64G / 256M RANK Ending Address Formula: END7A[35:24] = RENDxA << RMEMUNIT

Offset Address: E5h (D0F7)
Low Top Address - High **Default Value: FFh**

Bit	Attribute	Default	Description
7:0	RW	FFh	**Low Top Address – High**

Offset Address: E6h (D0F7)
SMM and APIC Decoding **Default Value: 01h**

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved**
5	RW	0	**APIC Lowest Interrupt Arbitration** 0: Disable 1: Enable
4	RW	0	**I/O APIC Decoding** 0: Access to FECx_xxxx will go to PCI1 1: Access to FEC7_FFFF - FEC0_0000 go to PCI1; access to FECF_FFFF - FEC8_0000 go to PCI2.
3	RW	0	**MSI Support (Processor Message Enable)** 0: Cycles accessing FEEx_xxxx from masters are passed to PCI1 (PCIC will not claim) 1: Cycles accessing FEEx_xxxx from masters are passed to the Host side for snooping
2	RW	0	**Top SMM Enable** 0: Disable 1: Enable
1	RW	0	**High SMM Enable**
0	RW	1b	**Compatible SMM Enable** 0: Disable 1: Enable

Offset Address: EF-E7h (D0F7) – Reserved

Offset Address: FF-F0h (D0F7) – Reserved

Device 1 Function 0 (D1F0): PCI to PCI Bridge

This configuration is provided to facilitate the configuration of the second PCI bus (AGP) without requiring new enumeration code. This function is represented as device number 1, function 0.

Header Registers (0–3Fh)

Offset Address: 1-0h (D1F0)

Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**Vendor ID**

Offset Address: 3-2h (D1F0)

Device ID **Default Value: B198h**

Bit	Attribute	Default	Description
15:0	RO	B198h	**Device ID**

Offset Address: 5-4h (D1F0)

PCI Command **Default Value: 0007h**

Bit	Attribute	Default	Description
15:10	RO	0	**Reserved**
9	RO	0	**Fast Back-to-Back Cycle Enable** Hardwired to 0.
8	RO	0	**SERR# Enable** Hardwired to 0.
7	RO	0	**Address / Data Stepping** Hardwired to 0.
6	RW	0	**Parity Checking** 0: Ignore parity errors 1: Perform parity check and take normal action on detected parity errors
5	RO	0	**VGA Palette Snooping** Hardwired to 0.
4	RO	0	**Memory Write and Invalidate**
3	RO	0	**Respond to Special Cycle** Hardwired to 0.
2	RW	1b	**Bus Master** 0: Never behaves as a bus master 1: Enable to operate as a bus master on the secondary interface
1	RW	1b	**Memory Space Access** 0: Does not respond to memory space access 1: Responds to memory space access
0	RW	1b	**I/O Space Access** 0: Does not respond to I/O space access 1: Responds to I/O space access

Offset Address: 7-6h (D1F0)

PCI Status **Default Value: 0230h**

Bit	Attribute	Default	Description
15	RO	0	**Parity Error Detected** Reserved
14	RO	0	**SERR# Detected** Reserved
13	RO	0	**Set When Terminated with Master-Abort, Except Special Cycle** 0: No abort received 1: Transaction aborted by the master
12	RO	0	**Set When Received a Target-Abort** 0: No abort received 1: Transaction aborted by the target
11	RO	0	**Set When Signaled a Target-Abort** NB never signals Target Abort
10:9	RO	01b	**DEVSEL# Timing** 00: Fast 01: Medium 10: Slow 11: Reserved
8	RO	0	**Set When Set or Observed SERR# and Parity Error** Reserved
7	RO	0	**Capable of Accepting Fast Back-to-Back as a Target** Reserved
6	RO	0	**User Definable Features**
5	RO	1b	**66 MHz Capable**
4	RO	1b	**Support New Capability List**
3:0	RO	0	**Reserved**

Offset Address: 08h (D1F0)

Revision ID **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Revision ID**

Offset Address: 0B-09h (D1F0)

Class Code **Default Value: 06 0400h**

Bit	Attribute	Default	Description
23:0	RO	060400h	**Class Code**

Offset Address: 0Ch (D1F0) - Reserved

Offset Address: 0Dh (D1F0)

Latency Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Latency Timer** Reserved

Offset Address: 0Eh (D1F0)

Header Type **Default Value: 01h**

Bit	Attribute	Default	Description
7:0	RO	01h	**Header Type** It adheres to the PCI-PCI Bridge Configuration

Offset Address: 0Fh (D1F0)

Built-In Self Test (BIST) **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Built In Self Test (BIST)**

Offset Address: 13-10h (D1F0)
Graphic Aperture Base Configuration **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:4	RO	0	**Reserved**
3	RO	0	**Prefetchable**
2:1	RO	0	**Type** Indicates that the address range is in the 32-bit address space.
0	RO	0	**Memory Space**

Offset Address: 17-14h (D1F0) – Reserved

Offset Address: 18h (D1F0)
Primary Bus Number **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	00h	**Primary Bus Number**

Offset Address: 19h (D1F0)
Secondary Bus Number **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Secondary Bus Number** Secondary Bus Number is used when converting Type#1 configuration cycles to TYPE#0 configuration cycles.

Offset Address: 1Ah (D1F0)
Subordinate Bus Number **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Subordinate Bus Number** PCI2 uses Subordinate Bus Number to decide if Type#1 command is passed to the PCI2 Bus.

Offset Address: 1Bh (D1F0)
Secondary Latency Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Secondary Latency Timer** Reserved

Offset Address: 1Ch (D1F0)
I/O Base **Default Value: F0h**

Bit	Attribute	Default	Description
7:4	RW	Fh	**I/O Address Bit[15:12] – Inclusive**
3:0	RO	0	**I/O Addressing Capability**

Offset Address: 1Dh (D1F0)
I/O Limit **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**I/O Address Bit[15:12] – Inclusive**
3:0	RO	0	**I/O Addressing Capability**

Offset Address: 1F-1Eh (D1F0)
Secondary Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RO	0	**Secondary Status** If D1F0 Rx44[4] = 0: Read this register has 0 returned. If D1F0 Rx44[4] = 1: Read this register has contents of Rx7-6 returned.

Offset Address: 21-20h (D1F0)
Memory Base **Default Value: FFF0h**

Bit	Attribute	Default	Description
15:4	RW	FFFh	**Memory Address Bit[31:20] – Inclusive** (address [19:0] is not decoded)
3:0	RO	0	**Reserved**

Offset Address: 23-22h (D1F0)
Memory Limit **Default Value: 0000h**

Bit	Attribute	Default	Description
15:4	RW	0	**Memory Address Bit[31:20] – Inclusive** (address [19:0] is not decoded)
3:0	RO	0	**Reserved**

Offset Address: 25-24h (D1F0)
Prefetchable Memory Base **Default Value: FFF0h**

Bit	Attribute	Default	Description
15:4	RW	FFFh	**Memory Address Bit[31:20]**
3:0	RO	0	**Reserved**

Offset Address: 27-26h (D1F0)
Prefetchable Memory Limit **Default Value: 0000h**

Bit	Attribute	Default	Description
15:4	RW	0	**Memory Address Bit[31:20]**
3:0	RO	0	**Reserved**

Offset Address: 33-28h (D1F0) – Reserved

Offset Address: 34h (D1F0)
Capability Pointer **Default Value: 70h or 80h**

Bit	Attribute	Default	Description
7:0	RO	70h or 80h	**AGP Capability List Pointer** 70h, if Rx48[0] is 0. 80h, if Rx48[0] is 1.

Offset Address: 3D-35h (D1F0) – Reserved

Offset Address: 3F-3Eh (D1F0)
PCI-to-PCI Bridge Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15:12	RO	0	**Reserved**
11	RW	0	**Enable Discard Timer SERR#** 0: Disable 1: Enable
10	RO	0	**Reserved**
9	RW	0	**Enable Secondary Discard Timer** 0: Disable 1: Enable
8	RW	0	**Enable Primary Discard Timer** 0: Disable 1: Enable
7	RO	0	**Reserved**
6	RW	0	**Secondary Bus Reset**
5	RO	0	**Reserved**
4	RW	0	**Base VGA 16 Bits Decode** 0: All VGA alias range will be forwarded. 1: Only forward base VGA range (Alias range will not be forwarded).
3	RW	0	**Enable VGA Compatible I/O and Memory Address Range** 0: Do not forward VGA compatible memory and I/O cycles to PCI2. 1: Forward VGA compatible memory and I/O cycles to PCI2.
2	RW	0	**Block ISA I/O Cycles** 0: Forward all I/O cycles with address in the range defined by the I/O Base and I/O Limit to PCI2. 1: Do not forward ISA I/O cycles with address in the top 768 bytes of each 1Kbyte block.
1	RW	0	**Forward Lower Side PCI SERR# to Upper Side** Status is reported on Rx7[6].
0	RW	0	**Enable Parity Error Response**

Second PCI Bus Control (40–6Fh)

Offset Address: 40h (D1F0)
CPU to PCI Flow Control 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**CPU to PCI Post-Write** 0: Disable 1: Enable C2P posted cycle could be delayed by PCI master cycles (i.e. PCI master access is allowed even if C2P buffer is not flushed).
6	RW	0	**CPU to PCI 1-Wait State Burst Write** 0: Disable 1: Enable
5:4	RW	0	**Read Prefetch Control** x0: Always prefetch x1: Disable prefetch
3	RO	0	**Reserved**
2	RW	0	**MDA Resource Location** (Note: The setting on this register bit overwrites the settings on the IO/Memory's Base and Limit of the other devices.) 0: AGP/PCI2; forward MDA access cycles to AGP/PCI2. 1: PCI1; forward MDA access cycles to PCI1. MDA Resources include: Memory: B0000h-B7FFFFh, I/O: 3B4h, 3B5h, 3B8h, 3B9h, 3BAh and 3BFh. Check the following table for the function of register bits: D1F0 Rx3E[3] and D1F0 Rx40[2].
1	RW	0	**PCI2 Master Read Caching** 0: Disable 1: Enable
0	RW	0	**PCI2 Delay Transaction** 0: Disable 1: Enable

Address	Rx3E[3]	Rx40[2]	Cycle Destination
Memory: AFFFFh-A0000h	0	-	PCI1
	1	-	PCI2
Memory: MDA (BFFFFh-B0000h)	1	0	PCI2
	1	1	PCI1
	0	-	PCI1
IO:[3BBh,3B0h] except MDA	0	-	PCI1
	1	-	PCI2
IO: MDA	1	0	PCI2
	0	-	PCI1
	1	1	PCI1
IO: [3DFh,3C0h]	1	-	PCI2
	0	-	PCI1

Notes:
1. If Rx3E[2] is set to 1, NB will not forward cycles to AGP if A[9:0] is in the range of 3ffh-100h even if address are within the range defined by the Rx1C[7:4] and Rx1D[7:4].

2. If both Rx3E[3] and Rx40[2] are set to 1, VGA is on PCI2 and MDA is put on PCI1. VGA palette snooping is not supported in PCI2.

Offset Address: 41h (D1F0)
CPU to PCI Flow Control 2

Default Value: 08h

Bit	Attribute	Default	Description
7	RO	0	**Retry Status** 0: No retry occurred 1: Retry occurred (write 1 to clear)
6	RW	0	**Action When Retry Timeout** 0: No action taken except recording status 1: Flush buffer (write) or return FFFF FFFFh (read)
5:4	RW	00b	**Retry Count** 00: Retry 2 times, back off CPU 01: Retry 4 times, back off CPU 10: Retry 16 times, back off CPU 11: Retry 64 times, back off CPU
3	RW	1b	**C2P Burst Timeout Enable** 0: Disable 1: Enable
2	RO	0	**Reserved**
1	RW	0	**Invalidate PCI1/PCI2 Read Buffer Data (read caching data) when C2P Cycle Arrived** 0: Disable 1: Enable
0	RO	0	**Reserved**

Offset Address: 42h (D1F0)
PCI Master Control

Default Value: 00h

Bit	Attribute	Default	Description
7	RW	0	When AGPC gets read data returned, it may signal PCI2 to do delay transaction or do disconnect to the current PCI master cycles, so that the AGP master's performance won't be blocked by the PCI master cycles.
6	RW	0	**PCI Master 1-Wait State Write** 0: Disable 1: Enable
5	RW	0	**PCI Master 1-Wait State Read** 0: Disable 1: Enable
4	RW	0	**Break Consecutive PCI Master Access** 0: Disable 1: Enable
3	RO	0	**Reserved**
2	RW	0	**PCI2 Claims the I/O R/W and Memory Read Cycles** 0: Disable 1: Enable
1	RW	0	**PCI2 Claims the Local APIC FEEx_xxxx Cycles** 0: Disable 1: Enable
0	RO	0	**Reserved**

Offset Address: 43h (D1F0)
PCI2 Timer **Default Value: 22h**

Bit	Attribute	Default	Description
7:4	RW	2h	**Host to PCI2 Time Slot** 0: Disable (no timer) 1: 16 GCLKs 2: 32 GCLKs … Fh: 128 GCLKs
3:0	RW	2h	**PCI2 Master Time Slot** 0: Disable (no timer) 1: 16 GCLKs 2: 32 GCLKs … Fh: 128 GCLKs

Offset Address: 44h (D1F0)
PCI2 Miscellaneous Control **Default Value: 20h**

Bit	Attribute	Default	Description
7	RW	0	**Revision ID Write Enable** 0: Disable 1: Rx8 can be revised; read from Rx8 will receive the revised value.
6	RO	0	**Reserved**
5	RW	1b	**Power Management Capability Support** 0: Read Rx34 as 00h. 1: Read Rx34 as 80h. Rx1F-1E reflect the status in Rx7-6.
4	RW	0	**Rx1F-Rx1E Read Returned Value** 0: Rx1F-1E always read as 0 1: Rx1F-1E read will receive the values in Rx7-6
3:0	RW	0	**Reserved**

Offset Address: 45h (D1F0) – Reserved

Offset Address: 46h (D1F0)
PCI-to-PCI Bridge Device ID (Low Byte) **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Device ID for P2P Bridge Low Byte (ID[7:0])**

Offset Address: 47h (D1F0)
PCI-to-PCI Bridge Device ID (High Byte) **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Device ID for P2P Bridge High Byte (ID[15:8])**

Offset Address: 48h (D1F0)
Miscellaneous Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RO	0	**Reserved**
0	RW	0	**Report AGP Capability in Device 1 instead of Device 0** 0 : Disable 1: Enable Note:D1F0 Rx13-10 will be programmable and fed. Rx80 AGP capability header will be added in the capability list directly by Rx34 of Device 1.

Offset Address: 6F-49h (D1F0) – Reserved

Power Management Capability (70-77h)

Offset Address: 70h (D1F0)
Capability ID **Default Value: 01h**

Bit	Attribute	Default	Description
7:0	RO	01h	**Capability ID**

Offset Address: 71h (D1F0)
Next Pointer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Next Pointer: NULL**

Offset Address: 72h (D1F0)
Power Management Capabilities 1 **Default Value: 02h**

Bit	Attribute	Default	Description
7:0	RO	02h	**Power Management Capabilities**

Offset Address: 73h (D1F0)
Power Management Capabilities 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Power Management Capabilities**

Offset Address: 74h (D1F0)
Power Management Control / Status **Default Value: 00h**

Bit	Attribute	Default	Description
7:2	RO	0	**Reserved**
1:0	RW	00b	**Power State** 00: D0 11: D3 hot

Offset Address: 75h (D1F0)
Power Management Status **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Power Management Status**

Offset Address: 76h (D1F0)
PCI to PCI Bridge Support Extensions **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**PCI to PCI Bridge Support Extensions**

Offset Address: 77h (D1F0)
Power Management Data **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Power Management Data**

Offset Address: 7F-78h (D1F0) – Reserved

Device 2 Function 0 (D2F0) – PCI Express Root Port G (PCI-to-PCI Virtual Bridge)

Device 2 Function 0, a 16-Lane PCI Express Root Port, is connected to the PCI bus through AD13 as the IDSEL.
All registers are located in PCI configuration space and should be programmed using PCI configuration mechanism 1 through I/O registers CF8 / CFC with bus number 0, device number 2 and function number 0.

Header Registers (0-3Fh)

Offset Address: 1-0h (D2F0)
Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**Vendor ID**

Offset Address: 3-2h (D2F0)
Device ID **Default Value: A364h**

Bit	Attribute	Default	Description
15:0	RO	A364h	**Device ID**

Offset Address: 5-4h (D2F0)
Command Register **Default Value: 0000h**

Bit	Attribute	Default	Description
15:11	RO	0	**Reserved**
10	RW	0	**Interrupt Disable** Set when the device is prevented from generating INTx messages.
9	RO	0	**Reserved**
8	RW	0	**SERR# Enable** 0: Disable error report 1: Enable reporting of non-fatal and fatal errors
7	RO	0	**Reserved**
6	RW	0	**Parity Error Response** 0: Ignore parity errors & continue 1: Take normal action on detected parity errors
5:3	RO	0	**Reserved**
2	RW	0	**Bus Master Enable** 0: Disable 1: Enable Controls the ability to forward Memory and I/O Read/Write requests in the upstream direction. Disabling this bit disables MSI messages.
1	RW	0	**Memory Space** 0: Ignore downstream memory transactions; memory cycles with address falling in the claimed range will be forwarded to the SB 1: Enable downstream memory cycle to this port if its address falling in the claimed range of this device.
0	RW	0	**I/O Space** 0: Ignore downstream I/O transactions; I/O cycles with address falling in the claimed range will be forwarded to the SB. 1: Enable downstream I/O cycle to this port if its address falling in the claimed range of this device.

Offset Address: 7-6h (D2F0)
Status Register **Default Value: 0010h**

Bit	Attribute	Default	Description
15	RW1C	0	**Detected Parity Error** This bit is set whenever a poisoned TLP is received, regardless the state of Parity Error Enabled (Rx4[6])
14	RW1C	0	**Signaled System Error** This bit is set when: A device sends an ERR_FATAL or ERR_NONFATAL message Rx4[8] = 1
13	RW1C	0	**Received Master Abort** This bit is set when receiving a completion with Unsupported Request Completion Status
12	RW1C	0	**Received Target Abort** This bit is set when receiving a completion with Completer Abort Completion Status
11	RW1C	0	**Signaled Target Abort** This bit is set when completing a Request with Completer Abort Completion Status
10:9	RO	0	**Reserved** Always reads 0
8	RW1C	0	**Master Data Parity Error** This bit is set if Parity Error Enable bit (Rx4[6]) is set and either one of the following two conditions occurs: Requestor receives a Completion marked poisoned Requestor poisons a write Request
7:5	RO	0	**Reserved**
4	RO	1b	**Capabilities List** Indicate the presence of an extended capability list item. Always set to 1 for PCI Express device
3	RO	0	**Interrupt Status** Indicate an INTx message is pending internally
2:0	RO	0	**Reserved**

Offset Address: 8h (D2F0)
Revision ID **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Revision Code**

Offset Address: 0B-9h (D2F0)
Class Code **Default Value: 06 0400h**

Bit	Attribute	Default	Description
23:0	RO	060400h	**Class Code**

Offset Address: 0Ch (D2F0)
Cache Line Size **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Cache Line Size** Reserved

Offset Address: 0Dh (D2F0)
Master Latency Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Master Latency Timer** Reserved

Offset Address: 0Eh (D2F0)
Header Type **Default Value: 01h**

Bit	Attribute	Default	Description
7:0	RO	01h	**Header Type**

Offset Address: 0Fh (D2F0)
Built In Self Test (BIST) **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**BIST Support**

Offset Address: 17-10h (D2F0)
Base Address Register **Default Value: 0000 0000 0000 0000h**

Bit	Attribute	Default	Description
63:0	RO	0	**Base Address**

Offset Address: 18h (D2F0)
Primary Bus Number **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Primary Bus Number**

Offset Address: 19h (D2F0)
Secondary Bus Number **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Secondary Bus Number**

Offset Address: 1Ah (D2F0)
Subordinate Bus Number **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Subordinate Bus Number**

Offset Address: 1Bh (D2F0)
Secondary Latency Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Secondary Latency Timer –** Reserved (Hardwired to 0)

Offset Address: 1Ch (D2F0)
I/O Base **Default Value: F0h**

Bit	Attribute	Default	Description
7:4	RW	Fh	**I/O Base (AD[15:12] - Inclusive)** This bridge will forward the cycles from primary side to PCI if the I/O address AD[15:12] is between I/O base and I/O limit (Rx1D[7:4]).
3:0	RO	0	**I/O Addressing Capability** 0 means I/O addressing is 16-bit only.

Offset Address: 1Dh (D2F0)
I/O Limit **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**I/O Limit (AD[15:12] - Inclusive)** This bridge will forward the cycles from primary side to PCI if the I/O address is between I/O base (Rx1C) and I/O limit.
3:0	RO	0	**I/O Addressing Capability** 0 means I/O addressing is 16-bit only.

Offset Address: 1F-1Eh (D2F0)
Secondary Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15	RW1C	0	**Detected Parity Error** This bit is set when secondary side receives a poisoned TLP regardless of Rx4[6].
14	RW1C	0	**Received System Error** This bit is set when 1. A device sends an ERR_FATAL or ERR_NONFATAL message 2. Rx4[8] is 1
13	RW1C	0	**Received Master Abort**
12	RW1C	0	**Received Target Abort**
11	RW1C	0	**Signaled Target Abort**
10:9	RO	0	**Reserved**
8	RW1C	0	**Master Data Parity Error** This bit is set if Parity Error Enable bit (Rx4[6]) is set and either one of the following two conditions occurs: 1. Requestor receives a Completion marked poisoned. 2. Requestor poisons a write Request
7:0	RO	0	**Reserved**

Offset Address: 21-20h (D2F0)
Memory Base **Default Value: FFF0h**

Bit	Attribute	Default	Description
15:4	RW	FFFh	**Memory Base (AD[31:20] – Inclusive)** The address bits [19:0] is not decoded.
3:0	RO	0	**Reserved**

Offset Address: 23-22h (D2F0)
Memory Limit **Default Value: 0000h**

Bit	Attribute	Default	Description
15:4	RW	0	**Memory Limit (AD[31:20])** The address [19:0] is not decoded.
3:0	RO	0	**Reserved**

Offset Address: 25-24h (D2F0)
Prefetchable Memory Base **Default Value: FFF1h**

Bit	Attribute	Default	Description
15:4	RW	FFFh	**Prefetchable Memory Base AD[31:20]**
3:0	RO	1b	**Reserved** (Do not program)

Offset Address: 27-26h (D2F0)
Prefetchable Memory Limit **Default Value: 0001h**

Bit	Attribute	Default	Description
15:4	RW	0	**Prefetchable Memory Limit AD[31:20]**
3:0	RO	1b	**Reserved** (Do not program)

Offset Address: 2B-28h (D2F0)
Prefetchable Memory Upper Base **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:4	RO	0	**Reserved**
3:0	RW	0	**AD[35:32]** This chip supports up to 16G.

Offset Address: 2F-2Ch (D2F0)
Prefetchable Memory Upper Limit **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:4	RO	0	**Reserved**
3:0	RW	0	**AD[35:32]** This chip supports up to 16G.

Offset Address: 31-30h (D2F0)
I/O Base Upper **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RO	0	**I/O Base Upper 16 Bits Address for PCI**

Offset Address: 33-32h (D2F0)
I/O Limit Upper **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RO	0	**I/O Limit Upper 16 Bits Address for PCI**

Offset Address: 34h (D2F0)
Capability Pointer **Default Value: 40h**

This register contains the offset address from the start of the configuration space.

Bit	Attribute	Default	Description
7:0	RO	40h	**Capability Pointer** Capability Pointer: Rx34 → Rx40 → Rx68 → Rx70 → Rx88 → Rx98 → NULL

Offset Address: 3B-35h (D2F0) – Reserved

Offset Address: 3Ch (D2F0)
Interrupt Line **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**INT Line** (For Software Use Only)

Offset Address: 3Dh (D2F0)
Interrupt Pin **Default Value: 01h**

Bit	Attribute	Default	Description
7:0	RO	01h	**INT Pin = INTA**

Offset Address: 3F-3Eh (D2F0)
Bridge Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15:7	RO	0	**Reserved**
6	RW	0	**Secondary Bus Reset** 0: No reset 1: Triggers a warm reset on the corresponding PCI Express Port
5	RO	0	**Reserved**
4	RW	0	**Base VGA 16 Bits Decode** 0: All VGA alias range will be forwarded 1: Only forward base VGA range (Alias range will not be forwarded)
3	RW	0	**VGA Compatible I/O and Memory Address Range** 0: Do not forward VGA compatible memory and I/O 1: Forward VGA compatible memory and I/O Note: VGA addresses are memory A0000-BFFFFh and I/O addresses 3B0-3BBh, 3C0-3CFh and 3D0-3DFh (10-bit decode). "Mono" text mode uses B0000-B7FFFh and "Color" Text Mode uses B8000-BFFFFh. Graphics modes use Axxxxh. Mono VGA uses I/O addresses 3Bx-3Cxh and Color VGA uses 3Cx-3Dxh. If an MDA is present, a VGA will not use the 3Bxh I/O addresses and B0000-B7FFFh memory space; if not, the VGA will use those addresses to emulate MDA modes.
2	RW	0	**Block/Forward ISA I/O Cycles** 0: Forward all I/O cycles with address in the range defined by the I/O Base and I/O Limit 1: Do not forward ISA I/O that are in the top 768 bytes of each 1K byte block address range
1	RW	0	**SERR Enable** Controls the forwarding of ERR_COR, ERR_NONFATAL and ERR_FATAL from secondary to primary 0: Disable 1: Enable
0	RW	0	**Parity Error Response Enable** 0: Ignore the response to poisoned TLPs 1: Enable the response to poisoned TLPs

PCI Express Capability Registers (40-67h)

Offset Address: 41-40h (D2F0)
PCI Express List **Default Value: 6810h**

Bit	Attribute	Default	Description
15:8	RO	68h	**Next Pointer**
7:0	RO	10h	**Capability ID**

Offset Address: 43-42h (D2F0)
PCI Express Capabilities **Default Value: 0141h**

Bit	Attribute	Default	Description
15	RO	0	**Reserved**
14	RO	0	**TCS Routing Supported**
13:9	RO	0	**Interrupt Message Number**
8	RO	1b	**Slot Implemented** This bit when set indicates that the PCI Express Link associated with this Port is connected to a slot (as compared to being connected to an integrated component or being disabled),
7:4	RO	4h	**Device / Port Type** 0100b: Root Port of PCI Express Root Complex
3:0	RO	1h	**Capability Version**

Offset Address: 47-44h (D2F0)

Device Capabilities **Default Value: 0000 8001h**

Bit	Attribute	Default	Description
31:28	RO	0	**Reserved**
27:26	RO	0	**Captured Slot Power Limit Scale** Reserved. For upstream port only
25:18	RO	0	**Captured Slot Power Limit Value** Reserved. For upstream port only
17:16	RO	0	**Reserved**
15	RO	1b	**Role-Based Error Reporting**
14	RO	0	**Power Indicator Present** Reserved. For upstream port or endpoint only
13	RO	0	**Attention Indicator Present** Reserved. For upstream port or endpoint only
12	RO	0	**Attention Button Present** Reserved. For upstream port or endpoint only
11:9	RO	0	**Endpoint L1 Acceptable Latency**
8:6	RO	0	**Endpoint L0s Acceptable Latency**
5	RO	0	**Extended Tag Field Supported** 0: 5-bit Tag field supported 1: 8-bit Tag field supported
4:3	RO	0	**Phantom Functions Supported** Reserved
2:0	RO	001b	**Max Payload Size Supported** 001b: 32QW (256 bytes)

Offset Address: 49-48h (D2F0)

Device Control **Default Value: 0810h**

Bit	Attribute	Default	Description
15	RO	0	**Reserved**
14:12	RO	000b	**Max Read Request Size** 000b: 128 bytes This field sets the maximum Read Request size for the device as a Requestor.
11	RW	1b	**Enable No Snoop** 0: Disable 1: Enable. If this bit is set to 1, the device is permitted to set the No Snoop bit in the Requestor Attributes of the transactions it initiate that do not require hardware enforced cache coherency.
10	RWS	0	**Auxiliary Power PM Enable** This bit when set enables device to draw AUX power independent of PME AUX power.
9	RO	0	**Phantom Functions Enable** Not supported.
8	RO/RW	0	**Extended Tag Field Enable** For Rx44[5], D2F0 Rx44-47[5] = 0 →RO For Rx44[5], D2F0 Rx44-47[5] = 1 →RW
7:5	RW	000b	**Max Payload Size** Maximum TLP payload size.
4	RW	1b	**Enable Relaxed Ordering** 0: Disable 1: Enable. If this bit is set to 1, the device is permitted to set the Relaxed Ordering bit in the Requestor Attributes of the transactions it initiate that do not require strong write ordering.
3	RW	0	**Unsupported Request Reporting Enable**
2	RW	0	**Fatal Error Reporting Enable** For a Root Port, the reporting of Fatal errors is internal to the root. No external ERR_FATAL message is generated.
1	RW	0	**Non-Fatal Error Reporting Enable** For a Root Port, the reporting of Non-Fatal errors is internal to the root. No external ERR_NONFATAL message is generated.
0	RW	0	**Correctable Error Reporting Enable** For a Root Port, the reporting of correctable errors is internal to the root. No external ERR_COR message is generated.

Offset Address: 4B-4Ah (D2F0)

Device Status **Default Value: 0010h**

Bit	Attribute	Default	Description
15:6	RO	0	**Reserved**
5	RO	0	**Transactions Pending** This bit when set indicates that the Port has issued Non-Posted Requests on its own behalf (using the Port's own Requestor ID) which have not been completed.
4	RO	1b	**AUX Power Detected**
3	RW1C	0	**Unsupported Request Detected**
2	RW1C	0	**Fatal Error Detected**
1	RW1C	0	**Non-Fatal Error Detected**
0	RW1C	0	**Correctable Error Detected**

Offset Address: 4F-4Ch (D2F0)

Link Capabilities **Default Value: 0018 3D01h**

Bit	Attribute	Default	Description
31:24	RO	0	**Port Number** This field indicates the PCI Express Port number for the given PCI Express Link.
23:21	RO	0	**Reserved**
20	RO	1b	**Data Link Layer Link Active Reporting Capable**
19	RO	1b	**Surprise Down Error Reporting Capable**
18	RO	0	**Clock Power Management**
17:15	RO	0	**L1 Exit Latency**
14:12	RO	011b	**L0s Exit Latency**
11:10	RO	11b	**Active State Link PM (ASPM) Support**
9:4	RO	010000b	**Maximum Link Width** 0: 010000b (x16 lanes) 1: 000001b (x1 lane)
3:0	RO	0001b	**Maximum Link Speed** 0001b: 2.5Gb/s Link speed

Offset Address: 51-50h (D2F0)

Link Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15:9	RO	0	**Reserved**
8	RO	0	**Enable Clock Power Management**
7	RW	0	**Extended Synch** 0: FCU Timer limit is 30us 1: FCU Timer limit is 120us
6	RW	0	**Common Clock Configuration** 0: Indicates that this Port and the component on the opposite end of the Link are operating with asynchronous reference clock. 1: Indicates that this Port and the component on the opposite end of the Link are operating with a distributed common reference clock.
5	RW1C	0	**Retrain Link** Link retrain is initiated by writing 1 to this bit. This will direct the Physical Layer LTSSM to the Recovery state.
4	RW	0	**Link Disable** This bit disables the link when set to 1.
3	RO	0	**Read Completion Boundary** 0: 64 byte
2	RO	0	**Reserved**
1:0	RW	00b	**Active State Link PM (ASPM) Control** 00: Disabled 01: L0s Entry Enabled 10: L1 Entry Enabled 11: L0s and L1 Entry Enabled

Offset Address: 53-52h (D2F0)

Link Status **Default Value: 0nn1h**

Bit	Attribute	Default	Description
15:14	RO	0	**Reserved**
13	RO	0	**Data Link Layer Link Active**
12	RO	1b	**Slot Clock Configuration** 0: Use an independent clock irrespective of the presence of a reference on the connector. 1: Use the same physical reference clock that the platform provides on the connector.
11	RO	0	**Link Training** This bit indicated that Link training is in progress (Physical Layer LTSSM is in Configuration or Recovery state) or that 1b was written to the Retrain Link bit but Link training has not yet begun. Hardware clears this bit once Link training is complete.
10	RO	0	**Training Error** Set when a Link training error occurred. Cleared by hardware upon successfully training of the Link to the L0 Link state.
9:4	RO	HwInit	**Negotiated Link Width** 000001: x1 000010: x2 000100: x4 001000: x8 010000: x16
3:0	RO	0001b	**Link Speed** 0001: 2.5Gb/s negotiated Link speed.

Offset Address: 57-54h (D2F0)

Slot Capabilities **Default Value: 0000 0060h**

Bit	Attribute	Default	Description
31:19	RO	0	**Physical Slot Number** Physical slot number attached to the Port.
18	RO	0	**No Command Completed Support**
17	RO	0	**Electromechanical Interlock Present**
16:15	RO	0	**Slot Power Limit Scale**
14:7	RO	0	**Slot Power Limit Value**
6	RO	1b	**Hot-plug Capable**
5	RO	1b	**Hot-plug Surprise**
4	RO	0	**Power Indicator Present**
3	RO	0	**Attention Indicator Present**
2	RO	0	**MRL Sensor Present**
1	RO	0	**Power Controller Present**
0	RO	0	**Attention Button Present**

Offset Address: 59-58h (D2F0)

Slot Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15:13	RO	0	**Reserved**
12	RW	0	**Slot Control Register, Data Link Layer State Changed Enable** 0: Disable 1: Enable
11	RO	0	**Electromechanical Interlock Control**
10	RO	0	**Power Controller Control** 0: Power On 1: Power Off
9:8	RW	00b	**Power Indicator Control** 00: Reserved 01: On 10: Blink 11: Off Writes to this field cause the Port to send the appropriate POWER_INDICATOR_* Message.
7:6	RW	00b	**Attention Indicator Control** 00: Reserved 01: On 10: Blink 11: Off Writes to this field cause the Port to send the appropriate ATTENTION_INDICATOR_* Message.
5	RW	0	**Hot-Plug Interrupt Enable** This bit when set enables generation of Hot-Plug interrupt on enabled Hot-Plug events.
4	RW	0	**Command Completed Interrupt Enable** This bit when set enables the generation of Hot-Plug interrupt when a command is completed by the Hot-Plug controller.
3	RW	0	**Presence Detect Changed Enable** This bit when set enables the generation of Hot-Plug interrupt or Wakeup event on a presence detect changed event.
2	RO	0	**MRL Sensor Changed Enable**
1	RO	0	**Power Fault Detected Enable**
0	RW	0	**Attention Button Pressed Enable** This bit when set enables the generation of Hot-Plug interrupt or Wakeup event on an Attention Button pressed event.

Offset Address: 5B-5Ah (D2F0)

Slot Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15:9	RO	0	**Reserved**
8	RW1C	0	**Data Link Layer State Changed**
7	RO	0	**Reserved**
6	RO	0	**Presence Detect State** 0: Slot empty 1: Card present in slot
5	RO	0	**MRL Sensor State** Reserved
4	RW1C	0	**Command Completed**
3	RW1C	0	**Presence Detect Changed**
2	RO	0	**MRL Sensor Changed**
1	RO	0	**Power Fault Detected**
0	RW1C	0	**Attention Button Pressed**

Offset Address: 5D-5Ch (D2F0)
Root Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15:5	RO	0	**Reserved**
4	RO	0	**CRS Software Visibility Enable**
3	RW	0	**PME Interrupt Enable** 0: Disable 1: Enable interrupt generation upon receipt of a PME message as reflected in the PME status register bit. A PME interrupt is also generated if the PME status register bit is set when this bit is set from a cleared state.
2	RW	0	**System Error on Fatal Error Enable** 0: Disable 1: Enable generation of a System Error if a Fatal Error (ERR_FATAL) is reported by any of the devices in the hierarchy associated with the Root Port, or by the Root Port itself.
1	RW	0	**System Error on Non-Fatal Error Enable** 0: Disable 1: Enable generation of a System Error if a Non-Fatal Error (ERR_NONFATAL) is reported by any of the devices in the hierarchy associated with the Root Port, or by the Root Port itself.
0	RW	0	**System Error on Correctable Error Enable** 0: Disable 1: Enable generation of a System Error if a Correctable Error (ERR_COR) is reported by any of the devices in the hierarchy associated with the Root Port, or by the Root Port itself.

Offset Address: 5Eh (D2F0)
CRS Visibility Control **Default Value: 0000h**

Bit	Attribute	Default	Description
7:1	RO	0	**Reserved**
0	RO	0	**CRS Software Visibility Enable**

Offset Address: 5Fh (D3F0) – Reserved

Offset Address: 63-60h (D2F0)
Root Status **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:18	RO	0	**Reserved**
17	RO	0	**PME Pending** 0: No pending PME 1: Indicates that another PME is pending when the PME Status (bit 16) is set.
16	RW1C	0	**PME Status** Indicates that the PME was asserted by the Requestor ID indicated in PME Requestor ID (bit[15:0]).
15:0	RO	0	**PME Requestor ID** The Requestor ID of the last PME Requestor.

Offset Address: 64-67h (D2F0) – Reserved

PCI Power Management Capability Structure Registers (68-6Fh)

Offset Address: 6B-68h (D2F0)

Power Management Capabilities **Default Value: C822 7001h**

Bit	Attribute	Default	Description
31:27	RO	19h	**PME Support** Bit 31, 30 and 27 are set to 1b (PME Message will be forwarded).
26	RO	0	**D2 Support**
25	RO	0	**D1 Support**
24:22	RO	0	**AUX Current**
21	RO	1b	**Device Specific Initialization**
20:19	RO	0	**Reserved**
18:16	RO	010b	**Version**
15:8	RO	70h	**Next Pointer**
7:0	RO	01h	**Capability ID**

Offset Address: 6F-6Ch (D2F0)

Power Management Status/Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RO	0	**Power Management Data**
23:16	RO	0	**Reserved**
15	RW1CS	0	**PME Status** This bit's setting is not modified by hot, warm, or cold reset.
14:13	RO	0	**Data Scale**
12:9	RO	0	**Data Select**
8	RWS	0	**PME Enable** This bit's setting is not modified by hot, warm, or cold reset.
7:2	RO	0	**Reserved**
1:0	RW	0	**Power State**

PCI Message Signal Interrupt (MSI) Capability Structure Registers (70-87h)

Offset Address: 73-70h (D2F0)

MSI Capability Support **Default Value: 0180 8805h**

Bit	Attribute	Default	Description
31:25	RO	0	**Reserved**
24	RO	1b	**This MSI capability supports pre-vector masking capability**
23	RO	1b	**This MSI capability supports 64 bit message address only**
22:20	RW	000b	**Multiple Message Enable** 000: 1message allocated 001: 2 message allocated 010: 4 message allocated 011: 8 message allocated 100: 16 message allocated 101: 32 message allocated 11x: Reserved
19:17	RO	000b	**Multiple Message Capable** 000: 1message requested 001: 2 message requested 010: 4 message requested 011: 8 message requested 100: 16 message requested 101: 32 message requested 11x: Reserved
16	RW	0	**MSI Enable** 0: This Port is prohibited from using MSI to request service 1: This Port is permitted to use MSI to request service.
15:8	RO	88h	**Next Capability Pointer**
7:0	RO	05h	**Capability ID**

Offset Address: 77-74h (D2F0)
System-Specified Message Address - Low **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:2	RW	0	**System-Specified Message Address Bit [31:2]**
1:0	RO	0	**System-Specified Message Address Bit [1:0]** These bits will always read as 0

Offset Address: 7B-78h (D2F0)
System-Specified Message Address - High **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:4	RW	0	**System-Specified Message Address Bit [63:36]** The chip supports address up to A35.
3:0	RW	0	**System-specified Message Address [35:32]**

Offset Address: 7D-7Ch (D2F0)
Message Data **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW	0	**Message Data** The message data is to be put on data [15:0] of MSI cycles

Offset Address: 7F-7Eh (D2F0) – Reserved

Offset Address: 83-80h (D2F0)
Message Mask Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:1	RO	0	**Reserved**
0	RW	0	**Mask Bit for Message 0**

Offset Address: 87-84h (D2F0)
Message Pending Status **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:1	RO	0	**Reserved**
0	RO	0	**Pending Bit for Message 0**

HyperTransport Message Signal Interrupt (MSI) Capability Registers (88-97h)

Offset Address: 8B-88h (D2F0)
Capability Support **Default Value: A802 9808h**

Bit	Attribute	Default	Description
31:27	RO	10101b	**Capability Type**
26:18	RO	000000	**This MSI capability supports pre-vector masking capability**
17	RO	1b	**Fixed, the HT-MSI this chip support is only for MSI address like 00000000_FEEx_xxxx.**
16	RW	0	**MSI Enable** 0: This port is prohibited from using MSI to request service. 1: This port is permitted to use MSI to request service.
15:8	RO	98h	**Next Pointer**
7:0	RO	08h	**Capability ID**

Offset Address: 97-8Ch (D2F0) – Reserved

Subsystem ID and Subsystem Vendor ID Capability Registers (98-9Fh)

Offset Address: 99-98h (D2F0)

Capability Support **Default Value: 000Dh**

Bit	Attribute	Default	Description
15:8	RO	0	**Next Pointer**
7:0	RO	0Dh	**Capability ID**

Offset Address: 9D-9Ch (D2F0)

Subsystem Vendor ID Control **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**Subsystem Vendor ID**

Offset Address: 9F-9Eh (D2F0)

Subsystem ID Control **Default Value: C323h**

Bit	Attribute	Default	Description
15:0	RO	C323h	**Subsystem ID**

PCI Express Transaction Layer Registers (A0-A7h)

Offset Address: A0h (D2F0)

Downstream Control 1 **Default Value: 01h**

Bit	Attribute	Default	Description
7	RW	0	**Downstream Cycles Have Traffic Class TC1** 0: Disabled 1: Enabled.
6	RW	0	**Downstream Cycles Have Attribute "No Snoop" Set** 0: Disabled 1: Enabled
5	RW	0	**Downstream Cycles Have Attribute "Relaxed Ordering" Set** 0: Disabled 1: Enabled
4	RW	0	**Downstream Lock Cycle Support** 0: Disabled 1: Enabled
3	RW	0	**Downstream Arbitration Scheme** 0: Fixed priority: VC1 CPL > VC0 CPL > Down Stream Command 1: Round Robin arbitration priority between VC1 CPL, VC0 CPL and Down Stream Command
2	RW	0	**Downstream Post-Write Allowed to Pass IOW** 0: Not allowed. 1: Allowed
1	RW	0	**Downstream Post-Write Allowed to Pass Read** 0: Not allowed. 1: Allowed
0	RW	1b	**Downstream Pipeline** 0: Disabled 1: Enabled

Offset Address: A1h (D2F0)

Downstream Control 2 **Default Value: 14h**

Bit	Attribute	Default	Description
7	RW1C	0	**Downstream Configuration Completion Status** 0: Normal completion. 1: At least one configuration request ended with a CRS (Configuration Request Retry Status) completion.
6	RO	0	**Reserved**
5	RW	0	**Data Return of Upstream Read Requests** 0: The chip always checks CPL credit unless the endpoint advertises infinite CPL credits. 1: The chip does not check CPL credit even when endpoint advertises finite CPL credits.
4	RW	1b	**Transaction Layer Downstream does not check downstream PH credit for PME_TURN_OFF message as the PCIe v1.1 spec requirement** 0: Disable 1: Enable
3	RW	000b	**C2P Read Completion Timer for Vector Development Mode** When this bit is set to 1, the timer defined in RxA1[2:0] becomes: 000: 1us 001: 3us 010: 10us 011: 20us 100: 50us 101: 100us 110: 200us 111: 500us
2:0	RW	100b	**C2P Read Completion Timeout Timer** 000: Reserved 001: 1ms 010: Reserved 011: 10ms (Spec. lower bound) 100: 30ms 101: Reserved 110: Reserved 111: Reserved

Offset Address: A2h (D2F0)

Downstream Control 3 **Default Value: 30h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6:4	RW	011b	**Waiting for GNT Timer for Priority Arbitration Mode** If GNT timer of VC0/C2P request expires, VC0/C2P request will become higher priority Priority VC1 > VC0 > C2P request when set RxA0[3]=0 000: 4ns 001: 16ns 010: 32ns 011: 64ns 100: 96ns 101: 128ns 110: 256ns 111: 512ns
3	RO	0	**Reserved**
2	RW	0	**Pending C2P NP cycle blocks L1 entry** 0: Disable. L1 entry won't consider C2P NP completion 1: Enable. L1 entry will need to wait for C2P NP completion
1:0	RW	00b	**Downstream Arbitration Parking** 00: GNT park on the last request source 01: GNT park on VC1 completion. If VC1 is not enabled (or no VC1), park on VC0 completion 10: GNT park on VC0 completion 11: GNT park on C2P request

Offset Address: A3h (D2F0)

Downstream Control 4 **Default Value: FCh**

Bit	Attribute	Default	Description
7:4	RW	1111b	**Retry Buffer Level:** 0000: 2-level 0001: 4-level 0010: 6-level 0011: 8-level 0100: 10-level 0101: 12-level 0110: 14-level 0111: 16-level 1000: 18-level 1001: 20-level 1010: 22-level 1011: 24-level 1100: 26-level 1101: 28-level 1110: 30-level 1111: 32-level
3	RW	1b	**Downstream Read Retry Time Out Control in DL_Down State** 0: Disable downstream read retry time out. If RxA3[0] is set to 1, downstream read request will always wait for DL_DLUp assertion then retry. 1: Enable downstream read retry time out (when RxA3[0] is set to 1 and RxA3[1] is set to 0). The timer is the same as completion time out timer. After time out, this read request will not be retried again even DL_DLUp assertion.
2	RW	1b	**Downstream Cycle Control/Latency Improvement** 0: Disable downstream HPOP/DPOP assert at the same time 1: Enable downstream HPOP/DPOP assert at the same time
1	RW	0	**CPL Timer Control** 0: Enable. Refer to D2F0 RxA1[2:0], D3F0RxA1[2:0] 1: Disable
0	RW	0	**Downstream Read Cycle Retry** 0: When DL_DOWN is asserted, transaction layer returns "FF" to PXPTRF for C2P read cycle. 1: When DL_DOWN is asserted, transaction layer holds C2P read cycle and this incompletes C2P read cycle will be retried when DL_UP is asserted.

Offset Address: A4h (D2F0)

Upstream Control **Default Value: 5Ch**

Bit	Attribute	Default	Description
7	RW	0	**Upstream Address A35~A31 Forced to 0** 0: Disabled. 1: Enabled for system testing or loop back mode test. The upcoming data may be checked in the system memory
6	RW	1b	**A guard bit for improving timing to prevent upstream write FIFO from begin overwritten**
5	RW	0	**Upstream Checking Malformed TLP through "Byte Enable Rule" and "Over 4K Boundary Rule"** 0: Disabled. 1: Enabled.
4	RW	1b	**Downstream Read Wait till the Upstream Write Data Flushed** 0: Disabled. 1: Enabled.
3	RW	1b	**Infinite Flow Control** 0: Current Design 1: CPLH & CPLD & NPD Become Infinite mode
2	RW	1b	**Flow Control Update for Each Header** 0: Update header credit whenever received two TLPHs 1: Update header credit whenever received TLPH (including PH, NPH and CPLH)
1	RW	0	**VC1 Request Queue Usage (when VC1 is disabled in the capability header; i.e. Rx144[0] = 0)** 0: Disabled 1: Enabled. It allows Transaction Layer map non-snoop upstream request through VC1 Request Queue to the Central Traffic Controller (Note that when this bit is 1, bit-0 has to be 0).
0	RW	0	**C2P Completion Timeout Timer Value Control When PHY Retrain Link or In Configuration State** 0: Keep the timeout value 1: Reset the timeout value

Offset Address: A5h (D2F0)
Credit Advertisement Control **Default Value: FFh**

Bit	Attribute	Default	Description
7:4	RW	1111b	**Upstream Posted (write) Data FIFO Size, and the Initial PD Credit Value** 0011: 4-line upstream write FIFO size, and initial PD credit = 'h20 0010: 3-line upstream write FIFO size, and initial PD credit = 'h10 0001: 2-line upstream write FIFO size, and initial PD credit = 'h8 0000: 1-line upstream write FIFO size, and initial PD credit = 'h4
3:0	RW	1111b	**Upstream PH Header Queues Size, and the Initial PH Credit** 0011: 8-level PH header queue, and initial PH credit = 'h8 0010: 4-level PH header queue, and initial PH credit = 'h4 0001: 2-level PH header queue, and initial PH credit = 'h2 0000: 1-level PH header queue, and initial PH credit = 'h1

Offset Address: A6h (D2F0)
Credit Advertisement Control **Default Value: 7Fh**

Bit	Attribute	Default	Description
7	RW	0	**NPH Initial Credit** 1: Enable NPH/NPD credit to device and improve PCI Express performance only when RxA6[3:0] is 1111b and RxA4[3] is 1b. 0: Disable if RxA6[3:0] is not 1111b, or when RxA4[3] is not 1b or when both of them.
6:4	RW	111b	**Upstream Read CPL Header Size** 111: 256QW 32-level 110: 224QW 28-level 101: 192QW 24-level 100: 160QW 20-level 011: 128QW 16-level 010: 96QW 12-level 001: 64QW 8-level 000: 32QW 4-level
3:0	RW	1111b	**Upstream Non-Posted Request Queue Size, and Initial NPH Credit Value** 0011: 8-level NPH header queue, and initial NPH credit = 'h8 0010: 4-level NPH header queue, and initial NPH credit = 'h4 0001: 2-level NPH header queue, and initial NPH credit = 'h2 0000: 1-level NPH header queue, and initial NPH credit = 'h1

Offset Address: A7h (D2F0)
Upstream Performance Control **Default Value: 04h**

Bit	Attribute	Default	Description
7	RW	0	**Transaction layer patch MSI cycle low address is masked bug register. The value of Revision Code bit 7(RX08[7]) in this root port should be the same as this register.** 0: Transaction layer mask low address[4:2] for both MSI and other P2C cycles. 1: Transaction layer does not mask low address[4:2] for both MSI and other P2C cycles.
6	RO	0	**Reserved**
5	RW	0	**Transaction layer header queue pre-load design dynamic clock enable for power management** 1: Turn on the transaction layer header queue pre-load design dynamic clock enable. 0: Otherwise
4	RW	0	**Upstream Read FIFO Entry Release Timing** 0: Upstream read FIFO entry release when the last data pop into retry data FIFO. 1: Upstream read FIFO entry release when the first data pop into retry data FIFO
3	RW	0	**Downstream Read Data Wait for Previous Upstream Write Complete** 0: Disable 1: Enable
2	RW	1b	**Upstream Requests Read and Write Orders** 0: Upstream requests are served in order. 1: Upstream write always pass upstream read.
1	RW	0	**Upstream Read Data TLP Return Policy** 0: One upstream request with over 16DW length or non-8-QW boundary alignment must be split into multiple CPL TLPs. 1: Multiple CPL TLPs which belong to the same upstream request can be merged into one single CPL TLP.
0	RW	0	**Upstream Write Cycle will be 4QW Align** 0: Disable 1: Enable

Offset Address: A8-AFh (D2F0) – Reserved

Note: The default value is "1"
If we want to program the value to "0', we should follow the following in sequence.
1. Must in Non-QUICK mode simulation.
2. Set Rx50[4] = 1 (disable link).
3. Program RxA4[3] = 0.
4. Enable Link, clear register Rx50[4] = 0, re-do flow control initialization.

PCI Express Data Link Layer Registers (B0-B8h)

Offset Address: B0h (D2F0)

Ack/Nak Latency Timer Limit **Default Value: 0Ch**

Bit	Attribute	Default	Description
7:0	RW	0Ch	**Timer Limit for Ack/Nak Latency Timer and Update FC Latency Timer (in unit of 250MHz)** 00: 4 x 1 Clocks 01: 4 x 2 Clocks 02: 4 x 3 Clocks. 0n: 4 x (n+1) Clocks FF: 4 x 256 Clocks.

Offset Address: B1h (D2F0)

Replay Timer Limit **Default Value: 12h**

Bit	Attribute	Default	Description
7:0	RW	12h	**Replay Timer Limit (in Unit of 250MHz)** 00: 8 x 1 Clocks 01: 8 x 2 Clocks 02: 8 x 3 Clocks 0n: 8 x (n+1) Clocks FF: 8 x 256 Clocks.

Offset Address: B2h (D2F0)

FCU (Flow Control Unit) Control and Status **Default Value: 40h**

Bit	Attribute	Default	Description
7	RW1C	0	**FCU Timeout Status** 1 Means the FCU timeout has occurred
6	RW	1b	**FCU Receive Timer Enable Control** 0: Disable the timeout mechanism 1: Enable the timeout mechanism
5	RW	0	**FCU Receive Timer Limit** 0: Timeout limit of 200us 1: Timeout limit of 300us
4	RW	0	**FCU Receive Timer Reset Control** 0: Timer reset by FCI/FCU only 1: Timer reset by any received DLLPs
3:1	RO	0	**Reserved**
0	RW	0	**A guard bit for DL and TL to reset upstream related logic when retrain is going on**

Offset Address: B3h (D2F0)
Replay Timer Control **Default Value: 81h**

Bit	Attribute	Default	Description
7:6	RW	10b	**Replay Timer Control While Rewind** (resend those DLLPs which do not have corresponding ACK/NAK received) 00: Hold Replay Timer during rewind. 01: During rewind, if ACK/NAK comes in, reset and hold the Replay Timer. 10: During rewind, reset and hold the Replay Timer as long as the Retry Buffer is empty. 11: Reserved.
5:3	RO	0	**Reserved**
2:0	RW	001b	**Count of Replay Timer Expired During RXL0s (Receiving Physical in L0s state) Before Resend the TLP** **When Rx50[7] is set to 0:** 000: Wait forever for the Acknowledge from the device side 001: Resend the TLP after 1 x Replay timer expired 010: Resend the TLP after 2 x Replay timer expired 011: Resend the TLP after 4 x Replay timer expired 100: Resend the TLP after 8 x Replay timer expired 101: Resend the TLP after 16 x Replay timer expired 110: Resend the TLP after 32 x Replay timer expired 111: Resend the TLP after 64 x Replay timer expired **When RX50[7] is set to 1:** 000: Wait forever for the Acknowledge from the device side 001: Resend the TLP after 16 x Replay timer expired 010: Resend the TLP after 32 x Replay timer expired 011: Resend the TLP after 64 x Replay timer expired 100: Resend the TLP after 128 x Replay timer expired 101: Resend the TLP after 256 x Replay timer expired 110: Resend the TLP after 512 x Replay timer expired 111: Resend the TLP after 1024 x Replay timer expired

Offset Address: B4h (D2F0)
Arbitration Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3	RW	0	**TLP V.S. Flow Control Initialization for VC0 in Arbitration** 0: TLP is not allowed to pass FCI2 for VC0 1: TLP is allowed to pass FCI2 for VC0
2:0	RW	000b	**Data Link TX Packets Arbitration Scheme** 000: Strict priority: NAK or timeout ACK > TLP > FCU > pending ACK 001: Reserved. 010: Strict priority: TLP > NAK or timeout / pending ACK > FCU 011: Strict priority: TLP > FCU > NAK or timeout / pending ACK 100: Strict priority: NAK or timeout / pending ACK > TLP > FCU 101: Strict priority: NAK or timeout / pending ACK > FCU > TLP 110: Strict priority: FCU > TLP > NAK or timeout / pending ACK 111: Strict priority: FCU > NAK or timeout ACK > TLP > pending ACK

Offset Address: B5h (D2F0)

FCU Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6	RW	0	**FCU Timer Control** 0: Update flow control credit when either Transaction Layer requested packets being sent or when FCU timer expired 1: Update flow control credit only when FCU timer expired
5:4	RW	00b	**ACK DLLP Collapse Method** 00: Send ACK when the latency timer RxB0 expired. 01: Send ACK every 4 correct TLP has been received 10: Send ACK every 8 correct TLP has been received 11: Send ACK every 16 correct TLP has been received
3:2	RO	0	**Reserved**
1	RW	0	**FCI (Flow Control Initialization) Process End Condition** 0: Complete FCI process when TLP/FCU has been received 1: Do not complete FCI process even when TLP/FCU has been received
0	RW	0	**VC1 FCI DLLP Transmission Scheme** 0: Transmit FCI DLLP only when FCI timer expired 1: Transmit FCI DLLP continuously as long as the FCI process is not finished

Offset Address: B6h (D2F0)

Transaction / Link Layer Checking Control **Default Value: 21h**

Bit	Attribute	Default	Description
7	RW	0	**Nak_Scheduled Flag Control** **Nak_Scheduled Flag is set after a Nak is scheduled by receiving a TLP with CRC or Seq_Num ERROR, and Nak_Scheduled Flag is cleared after receiving a new Ack.** 0: Disable Nak_Scheduled Flag. Schedule Nak regardless of Nak_Scheduled Flag. 1: Enable Nak_Scheduled Flag. Nak can only be scheduled when Nak_Scheduled Flag is cleared.
6:5	RW	01b	**Timeout mechanism for TTLEN. (only in X1/X2)** **When timeout, DL waits for DW boundary and automatically generates a TTL (TLP Tail) to finish the TLP.** 00: wait for 1us 01: wait for 2us 10: wait for 3us 11: wait for 4us
4	RW	0	phyls deskew buffer power management
3:1	RO	0	**Reserved**
0	RW	1b	**LCRC Checking Control** 0: Do not check LCRC 1: Check LCRC

Offset Address: B7h (D2F0) – Reserved

Offset Address: B8h (D2F0)

Data Link Layer Header Position **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RO	0	**Reserved**
0	RW	0	**Data Link Layer Header Position** 0: SDP (Start DLLP) can be in Lane0/4/8/12 1: SDP (Start DLLP) always at Lane0.

Offset Address: BF-B9h (D2F0) – Reserved

PCI Express Physical Layer Registers (C0-CBh)

Offset Address: C3-C0h (D2F0)

PHY Control **Default Value: 0027 0003h**

Bit	Attribute	Default	Description
31:24	RO	0	**PHYLS_STATE Mapping** See the table below.
23:21	RO	0	**Reserved**
20	RW	0	**Bypass PHYES Receiver Detect Function** 0: Derived from PHYES 1: Bypass Receiver Detect
19	RW	0	**State Machine LTSSM Exit POLLING_ACTIVE** 0: LTSSM may exit POLLING_ACTIVE when receiving 8 TS after sending more than 1024 TS 1: LTSSM always waits for 24 ms timeout to exit POLLING_ACTIVE.
18	RW	1b	**Scheme to Enter L1/L23 Entry** 0: Wait IDLE ordered set to enter L1/L23 entry 1: Wait electrical idle and ignore IDLE ordered set to enter L1/L23
17	RW	1b	**Running Disparity Check** 0: Disable 1: Enable
16	RW	1b	**State machine LTSSM enter Detect.Active from Detect.Quiet** 0: Wait for the Electrical idle signal from the PHYES or 12ms after RESET# becomes inactive 1: Always wait for 12ms after the RESET# becomes inactive
15:13	RO	0	**Reserved**
12:8	RW	0	**PHY Lane Configuration Setting** 10000: x16 with normal connection 01000: x8 with normal connection 00100: x4 with normal connection 00010: x2 with normal connection 00001: x1 with normal connection 01111: x16 with reverse connection 10111: x8 with reverse connection 11011: x4 with reverse connection 11101: x2 with reverse connection 11110: x1 with reverse connection 10101: force into L0s state (for testing and measurement used only) 00000: Use PHY negotiation Other values are not allowed.
7	RW	0	**Quick Timeout Counter Setting** When set to 1, following timeout counters will be shorter: TIMEOUT_2MS → TIMEOUT_4US TIMEOUT_12MS → TIMEOUT_24US TIMEOUT_24MS → TIMEOUT_48US TIMEOUT_48MS → TIMEOUT_96US TIMEOUT_1024TS → TIMEOUT_32TS Receiver Detection: 15x1024ns → 1x1024ns
6	RW	0	**Disable Data Scrambling / Descrambling** 0: Enable 1: Disable
5:3	RW	000b	**Loopback Mode Selection (Applies to All 16 Lanes)** 000: No loopback 001: PHYLS loopback from TX end to RX end 010: PHYES loopback from TX end to RX end 011: External loopback from TX end to RX end 100: Reserved 101: PHYLS loopback from RX end to TX end 110: PHYES loopback from RX end to TX end 111: Reserved
2:0	RW	011b	**COMMA Detection Window** 000, 001: Illegal values Others: Delay number of T to determine correct lane-to-lane deskew value

Table 20. Mapping Table for RxC3[7]

LTSSM states	Binary Coding	Hexadecimal Coding
DETECT_QUIET	8'B0000_0000	8'H00
DETECT_ACTIVE	8'B0000_0001	8'H01
POLLING_ACTIVE	8'B0001_0000	8'H10
POLLING_CONFIGURATION	8'B0001_0001	8'H11
POLLING_SPEED	8'B0001_0010	8'H12
POLLING_COMPLIANCE	8'B0001_0100	8'H14
CONFIGURATION_RCVRCFG_STEP_1	8'B0010_0001	8'H21
CONFIGURATION_RCVRCFG_STEP_2	8'B0010_0010	8'H22
CONFIGURATION_RCVRCFG_STEP_3	8'B0010_0011	8'H23
CONFIGURATION_RCVRCFG_STEP_4	8'B0010_0100	8'H24
CONFIGURATION_RCVRCFG_STEP_5	8'B0010_0101	8'H25
CONFIGURATION_RCVRCFG_STEP_6	8'B0010_0110	8'H26
CONFIGURATION_RCVRCFG_STEP_7	8'B0010_0111	8'H27
CONFIGURATION_IDLE	8'B0010_1000	8'H28
RECOVERY_RCVRLOCK	8'B0011_0000	8'H30
RECOVERY_RCVRCFG	8'B0011_0001	8'H31
RECOVERY_IDLE	8'B0011_0011	8'H33
LOOPBACK_MSTR_ENTRY	8'B0100_0000	8'H40
LOOPBACK_MSTR_ACTIVE	8'B0100_0001	8'H41
LOOPBACK_MSTR_EXIT	8'B0100_0011	8'H43
LOOPBACK_SLAV_ENTRY	8'B0100_0100	8'H44
LOOPBACK_SLAV_ACTIVE	8'B0100_0101	8'H45
LOOPBACK_SLAV_EXIT	8'B0100_0111	8'H47
DISABLED_ENTRY	8'B0101_0000	8'H50
DISABLED_DISABLED	8'B0101_0001	8'H51
HOTRESET_ACTIVE	8'B0110_0000	8'H60
L0L0_TXL0_RXL0	8'B1000_1010	8'H8A
L0L0S_TXL0_RXENTRY	8'B1001_1000	8'H98
L0L0S_TXL0_RXIDLE	8'B1001_1001	8'H99
L0L0S_TXL0_RXFTS	8'B1001_1011	8'H9B
L0SL0_TXENTRY_RXL0	8'B1010_0010	8'HA2
L0SL0_TXIDLE_RXL0	8'B1010_0110	8'HA6
L0SL0_TXFTS_RXL0	8'B1010_1110	8'HAE
L0SL0S_TXENTRY_RXENTRY	8'B1011_0000	8'HB0
L0SL0S_TXENTRY_RXIDLE	8'B1011_0001	8'HB1
L0SL0S_TXENTRY_RXFTS	8'B1011_0011	8'HB3
L0SL0S_TXIDLE_RXENTRY	8'B1011_0100	8'HB4
L0SL0S_TXIDLE_RXIDLE	8'B1011_0101	8'HB5
L0SL0S_TXIDLE_RXFTS	8'B1011_0111	8'HB7
L0SL0S_TXFTS_RXENTRY	8'B1011_1100	8'HBC
L0SL0S_TXFTS_RXIDLE	8'B1011_1101	8'HBD
L0SL0S_TXFTS_RXFTS	8'B1011_1111	8'HBF
L1_ENTRY	8'B1100_0000	8'HC0
L1_IDLE	8'B1100_0001	8'HC1
L23READY_ENTRY	8'B1101_0000	8'HD0
L23READY_IDLE	8'B1101_0001	8'HD1

Offset Address: C7-C4h (D2F0)

Elastic Buffer Base Registers for Lane 0 to 7 **Default Value: 4444 4444h**

Bit	Attribute	Default	Description
31	RO	0	**Reserved**
30:28	RW	4h	**Elastic Buffer Base Register for Lane 7** 0, 1, 7: Illegal values Others: delay numbers of T for elastic buffer operations
27	RO	0	**Reserved**
26:24	RW	4h	**Elastic Buffer Base Register for Lane 6** 0, 1, 7: Illegal values Others: delay numbers of T for elastic buffer operations
23	RO	0	**Reserved**
22:20	RW	4h	**Elastic Buffer Base Register for Lane 5** 0, 1, 7: Illegal values Others: delay numbers of T for elastic buffer operations
19	RO	0	**Reserved**
18:16	RW	4h	**Elastic Buffer Base Register for Lane 4** 0, 1, 7: Illegal values Others: delay numbers of T for elastic buffer operations
15	RO	0	**Reserved**
14:12	RW	4h	**Elastic Buffer Base Register for Lane 3** 0, 1, 7: Illegal values Others: delay numbers of T for elastic buffer operations
11	RO	0	**Reserved**
10:8	RW	4h	**Elastic Buffer Base Register for Lane 2** 0, 1, 7: Illegal values Others: delay numbers of T for elastic buffer operations
7	RO	0	**Reserved**
6:4	RW	4h	**Elastic Buffer Base Register for Lane 1** 0, 1, 7: Illegal values Others: delay numbers of T for elastic buffer operations
3	RO	0	**Reserved**
2:0	RW	4h	**Elastic Buffer Base Register for Lane 0** 0, 1, 7: Illegal values Others: delay numbers of T for elastic buffer operations

Offset Address: CB-C8h (D2F0)

Elastic Buffer Base Registers for Lane 8 to 15 **Default Value: 4444 4444h**

Bit	Attribute	Default	Description
31	RO	0	**Reserved**
30:28	RW	4h	**Elastic Buffer Base Register for Lane 15** 0, 1, 7: Illegal values Others: delay numbers of T for elastic buffer operations
27	RO	0	**Reserved**
26:24	RW	4h	**Elastic Buffer Base Register for Lane 14** 0, 1, 7: Illegal values Others: delay numbers of T for elastic buffer operations
23	RO	0	**Reserved**
22:20	RW	4h	**Elastic Buffer Base Register for Lane 13** 0, 1, 7: Illegal values Others: delay numbers of T for elastic buffer operations
19	RO	0	**Reserved**
18:16	RW	4h	**Elastic Buffer Base Register for Lane 12** 0, 1, 7: Illegal values Others: delay numbers of T for elastic buffer operations
15	RO	0	**Reserved**
14:12	RW	4h	**Elastic Buffer Base Register for Lane 11** 0, 1, 7: Illegal values Others: delay numbers of T for elastic buffer operations
11	RO	0	**Reserved**
10:8	RW	4h	**Elastic Buffer Base Register for Lane 10** 0, 1, 7: Illegal values Others: delay numbers of T for elastic buffer operations
7	RO	0	**Reserved**
6:4	RW	4h	**Elastic Buffer Base Register for Lane 9** 0, 1, 7: Illegal values Others: delay numbers of T for elastic buffer operations
3	RO	0	**Reserved**
2:0	RW	4h	**Elastic Buffer Base Register for Lane 8** 0, 1, 7: Illegal values Others: delay numbers of T for elastic buffer operations

Offset Address: CF-CBh (D2F0) – Reserved

PCI Express Power Management Module Registers (D0-DFh)

Offset Address: D3-D0h (D2F0)

PMC Control **Default Value: 0000 2050h**

Bit	Attribute	Default	Description
31:24	RW	00b	**Idle Period to Enter ASL1** Minimum time period is 128ns 00: 128ns 01: 2x128ns 02: 3x128ns … FF: 256x128ns
23:16	RW	00b	**Idle Period to Enter L0s** Minimum time period is 128ns 00: 128ns 01: 2x128ns 02: 3x128ns … FF: 256x128ns
15	RW1C	0	**Error Status Report** This bit is set when device cannot have electrical idle after the waiting period programmed at RxD1[6:4] expired.
14	RO	0	**Reserved**
13:12	RW	10b	**Electrical Idle Waiting Period before Move to L1 State** (after issue ACK to the L1 request from the device). 00: Always wait for electrical idle 01: Wait 32 clock 10: Wait 64 clock 11: Reserved
11:10	RO	0	**Reserved**
9:8	RW	0	**Downstream Cycles Triggered C2P Cycles, Period of Staying at L0 Before Returned to L1 for PHY** (when PMU is in non-D0 state) 00: immediately 01: 1 cfgW or message + delay10T 10: 1 32QW +1cfgW or message+ delay10T 11: 2 32QW +1 cfgW or message + delay10T
7	RO	0	**Reserved**
6:4	RW	101b	**Timeout Period** This timer is used when waiting for ACK from a device after issued PME_TURNOFF message to notify the device to move to power down mode. 000: 1us 001: 2us 010: 4us 011: 8us 100: 16us 101: 32us 110: 64us 111: 128us
3	RW	0	**Stop Port Clock When No Device On This Port** 0: Disable 1: Enable
2	RW	1b	**Enable Link Retrain when Bad DLLP Is Checked** 0: Disable 1: Enable
1	RW	0	**Link Loopback** 0: Normal operation 1: Direct device to enter Loopback mode, receiving data in the device will be sent to the transmit side
0	RW	0	**Link Reconfigure Link width** Link width reconfiguration is initiated by writing 1 to this bit. This will direct the Physical Layer LTSSM to the Recovery state first, and then to the Configuration state. 0: When Link Reconfigure Link width, LTSSM must be in Detect state 1: When Link Reconfigure Link width, LTSSM can be in Configuration state

Offset Address: D4h (D2F0)

PHYES Module Overall Control – Applied to x16 and x4 PHYES **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Power Management Enable for X1 Notebook** When working in Notebook only supporting PCIe X1, this bit is set to 1. Then the other 15 Lane's clock will be gated to save power.
6	RW	0	**Control FCI Receive Timer (300us)** 0: Disable the timeout mechanism 1: Enable the timeout mechanism
5:2	RO	0	**Reserved**
1	RW	0	**Lane Reversal** 0: Do not support lane reversal Link / Lane number will be sent only on lane0~(maxlinkwidth-1). 1: Support lane reversal. Link / Lane number will be sent on lane0 ~(maxlinkwidth-1), (16-maxlinkwidth)~ 15.
0	RW	0	**Un-negotiated Lanes State during Configuration.Complete** 0: During Configuration. Complete, un-negotiated lanes will be electrical idle. 1: During Configuration. Complete, Link/Lane number will be pad for un-negotiated lanes

Offset Address: D7-D5h (D2F0) – Reserved

Offset Address: D8h (D2F0)

PMC Express Message Status **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW1C	0	**Excessive Errors Occurred But Not Reported in MSGC** 0: Normal operation. 1: There are errors not reported to the system
6:0	RO	0	**Reserved**

Offset Address: DB-D9h (D2F0) – Reserved

Offset Address: DF-DCh (D2F0)

MSI Mapping Capability **Default Value: A802 0008h**

Bit	Attribute	Default	Description
31:27	RO	10101b	**Capability Type**
26:18	RO	0	**Reserved**
17	RO	1b	**Address for mapping MSI is fixed at 0000_0000_FEEx_xxxx and this capability block is one double word.**
16	RW	0	**MSI Enable** 0: This port is prohibited from using MSI to request service 1: This port is permitted to use MSI to request service. Note: this register is connected to GXD6[0] and not used now.
15:8	RO	0	**Next Pointer**
7:0	RO	08h	**Capability ID**

PCI Express Electrical PHY Registers (E0-EAh)

Offset Address: E0h (D2F0)

PHYES Module Overall Control (For Both x16 and x4 PHYES) **Default Value: 0Ch**

Bit	Attribute	Default	Description
7	RW	0	**Enable new PLL_LOCK Scheme to Monitor Any Abnormal Jitter** 0: Disabled 1: Enabled
6:4	RO	0	**Reserved**
3:1	RW	110b	**Charge Pump Current Control**
0	RW	0	**Charge Pump Style Control**

Offset Address: E1h (D2F0)

First 8 Lanes PHYES Module Related Control **Default Value: 07h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4	RW	0	**Receiving Polarity Change Control** 0: Have the same polarity on the loop-back/received data 1: Have reverse polarity on the loop-back/received data
3:2	RW	01b	**Squelch Window Select (64~175mv)**
1	RW	1b	**Electrical Idle Signal De-Assert Condition** 0: Electrical idle signal will be de-asserted at once and remained at least 4ns when electrical idle exit condition is detected. 1: Electrical idle signal will be de-asserted at once and remained at least 16ns when electrical idle exit condition is detected.
0	RW	1b	**Electrical Idle Signal Assert Condition** 0: Electrical idle signal is asserted only when electrical idle condition is detected and remained at least 16ns. 1: Electrical idle signal is asserted at once when the electrical idle condition is detected.

Offset Address: E2h (D2F0)

First 8 Lanes PHYES Module Control – Rx/Tx 1 **Default Value: 81h**

Bit	Attribute	Default	Description
7	RW	1b	**Receiver Termination** 0: Disable 1: Enable
6	RW	0	**Mobile Swing** 0: Disable 1: Enable
5	RW	0	**PHYES Clock Buffer Power Down on Lane 0-7** 0: All enable 1: Power down
4	RW	0	**Lane 4-7 Clock Buffer Power Down** 0: All enable 1: Lane 4-7 power down
3:2	RW	00b	**Receiver Input Rise Delay (duty cycle adjustment for the first 8 lanes)** 00: 0 ps 01: 4 ps 10: 15 ps 11: 50 ps
1:0	RW	01b	**Receiver Input Fall Delay (duty cycle adjustment for the first 8 lanes)** 00: 0 ps 01: 7 ps 10: 24 ps 11: 55 ps

Offset Address: E3h (D2F0)
First 8 Lanes PHYES Module Control – Rx/Tx 2 **Default Value: 9Ah**

Bit	Attribute	Default	Description
7	RW	1b	**PCIe Pads Driving Control** 0: Autocomp 1: Manual setting through bits RxE3[2:0]
6:5	RW	00b	**Filter Depth Valid Only When CDR Type is Set to 0** 00: Filter depth = 2 01: Filter depth = 3 10: Filter depth = 5 11: Filter depth = 7
4	RW	1b	**CDR Type** 0: 1/N type 1: Pseudo 6X scheme
3	RW	1b	**CDR Filter Depth** The bit is only valid when RxE3[4] = 1 0: Filter depth = 6 1: Filter depth = 8
2:0	RW	010b	**First 8 Lanes, Lane 0 – 7, Termination Resistance Selection** Resistance Range: 62Ω (000b) ~ 43Ω (111b) Default: 50Ω (010b)

Offset Address: E4h (D2F0)
First 8 Lanes PHYES Module Control – Rx/Tx 3 **Default Value: 88h**

Bit	Attribute	Default	Description
7:4	RW	8h	**Pre/De-Emphasis Level Selection**
3:0	RW	8h	**Driver Current Source Selection**

Offset Address: E7-E5h (D2F0) – Reserved

Offset Address: E8h (D2F0)
Second 8 Lanes PHYES Module Control – Rx/Tx 1 **Default Value: 81h**

Bit	Attribute	Default	Description
7	RW	1b	**Enable Receiver Termination** 0: Disable 1: Enable
6	RW	0	**Mobile Swing** 0: Disable 1: Enable
5	RO	0	**Reserved**
4	RW	0	**Lane 12-15 Clock Buffer Power Down** 0: All enable 1: Lane 12 - 15 power down
3:2	RW	00b	**Receiver Input Rise Delay (duty cycle adjustment for the second 8 lanes)** 00: 0 ps 01: 4 ps 10: 15 ps 11: 50 ps
1:0	RW	01b	**Receiver Input Fall Delay (duty cycle adjustment for the second 8 lanes)** 00: 0 ps 01: 7 ps 10: 24 ps 11: 55 ps

Offset Address: E9h (D2F0)
Second 8 Lanes PHYES Module Control – Rx/Tx 2 **Default Value: 82h**

Bit	Attribute	Default	Description
7	RW	1	**PCIe Pads Driving Control** 0: Autocomp 1: Manual setting through bits RxE9[2:0]
6	RO	0	**Reserved**
5	RW	0	**Clock Buffer Power Down in PHYES for the Second 8 Lanes** 0: All enable 1: Lane 8 - 15 power down
4:3	RO	0	**Reserved**
2:0	RW	010b	**Second 8 Lanes, Lane 8 –15, Termination Resistance Selection** Resistance Range: 62Ω (000b) - 43Ω (111b) Default: 50Ω (010b)

Offset Address: EAh (D2F0)

Second 8 Lanes PHYES Module Control – Rx/Tx 3 **Default Value: 88h**

Bit	Attribute	Default	Description
7:4	RW	8h	**Pre/De-Emphasis Level Selection**
3:0	RW	8h	**Driver Current Source Selection**

Offset Address: EF-EBh (D2F0) – Reserved

PCI Express Electrical PHY Test Registers (F0-F9h)

Offset Address: F3-F0h (D2F0)

PHY Test **Default Value: 0600 0000h**

Bit	Attribute	Default	Description
31	RW	0	**Electrical PHY Test Mode Enable** Program this bit to 1 to start Electrical PHY test
30:28	RO	0	**Reserved**
27:24	RW	6h	**Test Pattern Check Length** Number of T when the receiving side starts to check transmitted and received patterns Suggested Value Settings: (Lane 0 for example) RxC0[5:3] = 001b: RxC4[2:0] + 2 RxC0[5:3] = 010b: RxC4[2:0] + 2 + (Loopback Path Latency/4ns) + 1
23:20	RW	0	**Select Test Pattern** 0000: Reserved 0001: User define, use RxRxF7-F4[25:16] 0010: K28.5 test bit sequence 0011: K28.7 test bit sequence 0100: K test for differential pair current 0101: J test for differential pair current 0110: D21.5 test bit sequence 0111: D30.3 test bit sequence 1000: Ten contiguous run of 3 test bit sequence 1001: Low transition density test bit sequence 1010: Half-rate/quarter-rate test bit sequence 1011: Low frequency spectral test bit sequence 1100: Simultaneous switching test bit sequence 1101: Reserved 1110: Reserved 1111: Reserved
19:16	RW	0	**Select Lane for Loop Back Test** 0000: Loop back test on lane 0 0001: Loop back test on lane 1 …. 1111: Loop back test on lane 15
15:8	RW	0	**Repeated Count of the Test Pattern (as selected in RxF2[7:4])** 00~0Bh: Illegal. 0Ch: Test pattern repeats 12 times 0Dh: Test pattern repeats 13 times … FFh: Test pattern repeats 255 times
7:0	RO	0	**Reserved**

Offset Address: F7-F4h (D2F0)

PHY Test Symbol **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RO	0	**Electrical PHY Test Error** 1: An error occurred in loop back test mode receiving side
30	RO	0	**Electrical PHY Built-In Self Test Error of Symbol Comparison** That same errors happen or COMMA symbols are never detected during PHYBIST period; reported from PTNCMP
29:26	RO	0	**Reserved**
25:16	RO	00b	**Transmitted Symbol when RxF3[7] is set to 1** 00 when RxF3[7] is 0
15:10	RO	0	**Reserved**
9:0	RO	00b	**Received Symbol when RxF3[7] is set to 1** 00 when RxF3[7] is 0

Offset Address: F9-F8h (D2F0)

PHY BIST Counter Test Mode **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RO	0	**PHY BIST Period Electrical PHY Test Error**

Offset Address: FF-FAh (D2F0) – Reserved

Device 2 Function 0 (D2F0) – PCI Express Root Port G Extended Space

Registers defined in the Extended Space can be accessed through PCI Express Enhanced Configuration Access Mechanism, which utilizes a flat memory-mapped address space to access the configuration registers. Please check PCI Express Specification for the detail information.

PCI Express Extended Capabilities (100-13Fh)

Offset Address: 103-100h (D2F0)

Advance Error Reporting Enhanced Capability Header **Default Value: 1401 0001h**

Bit	Attribute	Default	Description
31:20	RO	140h	**Next Capability Offset**
19:16	RO	1h	**Capability Version**
15:0	RO	0001h	**PCI Express Extended Capability ID**

Offset Address: 107-104h (D2F0)

Uncorrectable Error Status **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:21	RO	0	**Reserved**
20	RW1CS	0	**Unsupported Request Error Status (TL)**
19	RW1CS	0	**ECRC Error Status (TL)**
18	RW1CS	0	**Malformed TLP Status (TL)**
17	RW1CS	0	**Receiver Overflow Status (TL)**
16	RW1CS	0	**Unexpected Completion Status (TL)**
15	RW1CS	0	**Completer Abort Status (TL)**
14	RW1CS	0	**Completion Timeout Status (TL)**
13	RW1CS	0	**Flow Control Protocol Error Status (TL)**
12	RW1CS	0	**Poisoned TLP Status (TL)**
11:6	RO	0	**Reserved**
5	RW1CS	0	**Surprise Down Error Status**
4	RW1CS	0	**Data Link Protocol Error Status (DLL)**
3:1	RO	0	**Reserved**
0	RW1CS	0	**Training Error Status (PHY)**

Offset Address: 10B-108h (D2F0)

Uncorrectable Error Mask **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:21	RO	0	**Reserved**
20	RWS	0	**Unsupported Request Error Mask (TL)**
19	RWS	0	**ECRC Error Mask (TL)**
18	RWS	0	**Malformed TLP Mask (TL)**
17	RWS	0	**Receiver Overflow Mask (TL)**
16	RWS	0	**Unexpected Completion Mask (TL)**
15	RWS	0	**Completed Abort Mask (TL)**
14	RWS	0	**Completion Timeout Mask (TL)**
13	RWS	0	**Flow Control Protocol Error Mask (TL)**
12	RWS	0	**Poisoned TLP Mask (TL)**
11:6	RO	0	**Reserved**
5	RWS	0	**Surprise Down Error Mask**
4	RWS	0	**Data Link Protocol Error Mask (DLL)**
3:1	RO	0	**Reserved**
0	RWS	0	**Training Error Mask (PHY)**

Offset Address: 10F-10Ch (D2F0)

Uncorrectable Error Severity **Default Value: 0006 2031h**

Bit	Attribute	Default	Description
31:21	RO	0	Reserved
20	RWS	0	Unsupported Request Error Severity (TL)
19	RWS	0	ECRC Error Severity (TL)
18	RWS	1b	Malformed TLP Severity (TL)
17	RWS	1b	Receiver Overflow Error Severity (TL)
16	RWS	0	Unexpected Completion Error Severity (TL)
15	RWS	0	Completed Abort Error Severity (TL)
14	RWS	0	Completion Timeout Error Severity (TL)
13	RWS	1b	Flow Control Protocol Error Severity (TL)
12	RWS	0	Poisoned TLP Severity (TL)
11:6	RO	0	Reserved
5	RWS	1b	Surprise Down Error Severity
4	RWS	1b	Data Link Protocol Error Severity (DLL)
3:1	RO	0	Reserved
0	RWS	1b	Training Error Severity (PHY)

Offset Address: 113-110h (D2F0)

Correctable Error Status **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:14	RO	0	Reserved
13	RW1CS	0	Advisory Non-Fatal Error Status
12	RW1CS	0	Replay Timer Timeout Status (DLL)
11:9	RO	0	Reserved
8	RW1CS	0	REPLAY_NUM Rollover Status (DLL)
7	RW1CS	0	Bad DLLP Status (DLL)
6	RW1CS	0	Bad TLP Status (DLL)
5:1	RO	0	Reserved
0	RW1CS	0	Receiver Error Status (PHY)

Offset Address: 117-114h (D2F0)

Correctable Error Mask **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:14	RO	0	Reserved
13	RWS	0	Advisory Non-Fatal Error Mask
12	RWS	0	Replay Timer Timeout Mask (DLL)
11:9	RO	0	Reserved
8	RWS	0	REPLAY_NUM Rollover Mask (DLL)
7	RWS	0	Bad DLLP Mask (DLL)
6	RWS	0	Bad TLP Mask (DLL)
5:1	RO	0	Reserved
0	RWS	0	Receiver Error Mask (PHY)

Offset Address: 11B-118h (D2F0)

Advanced Error Capabilities and Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:9	RO	0	Reserved
8	RWS	0	ECRC Check Enable (TL)
7	RO	0	ECRC Check Capable (TL)
6	RWS	0	ECRC Generation Enable (TL)
5	RO	0	ECRC Generation Capable (TL)
4:0	ROS	0	First Error Pointer (TL)

Offset Address: 11F-11Ch (D2F0)
Header Log Register 1st DW **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	ROS	0	**Header Log Register 1st DW**

Offset Address: 123-120 (D2F0)
Header Log Register 2nd DW **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	ROS	0	**Header Log Register 2nd DW**

Offset Address: 127-124h (D2F0)
Header Log Register 3rd DW **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	ROS	0	**Header Log Register 3rd DW**

Offset Address: 12B-128h (D2F0)
Header Log Register 4th DW **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	ROS	0	**Header Log Register 4th DW**

Offset Address: 12F-12Ch (D2F0)
Root Error Command **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:3	RO	0	**Reserved**
2	RW	0	**Fatal Error Reporting Enable**
1	RW	0	**Non-Fatal Error Reporting Enable**
0	RW	0	**Correctable Error Reporting Enable**

Offset Address: 133-130h (D2F0)
Root Error Status **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:27	RO	0	**Advanced Error Interrupt Message Number (TL)**
26:7	RO	0	**Reserved**
6	RW1CS	0	**Fatal Error Messages Received (TL)**
5	RW1CS	0	**Non-Fatal Error Messages Received (TL)**
4	RW1CS	0	**First Uncorrectable Fatal Error Message Received (TL)** Set to 1 when the first Uncorrectable Error Message received is for a Fatal Error
3	RW1CS	0	**Multiple ERR_FATAL/NONFATAL Received (TL)**
2	RW1CS	0	**ERR_FATAL/NONFATAL Received (TL)**
1	RW1CS	0	**Multiple ERR_COR Received (TL)**
0	RW1CS	0	**ERR_COR Received (TL)**

Offset Address: 137-134h (D2F0)
Error Source Identification **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:16	ROS	0	**ERR_FATAL/NONFATAL Source Identification (TL)**
15:0	ROS	0	**ERR_COR Source Identification (TL)**

Offset Address: 13B-138h (D2F0)
Error Source Identification **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	ROS	0	**Error DLLP log register**

Offset Address: 13C-13Fh (D2F0) – Reserved

Virtual Channel Capability (140-14Fh)

Virtual Channel Capability is defined for Egress direction of the device. For Root Port, since only VC0 is defined.

- VC0 mapping: TC0, TC1, TC2, TC3, TC4, TC5, TC6, TC7
- No VC arbitration table
- No port arbitration table

Offset Address: 143-140h (D2F0)
Virtual Channel Enhanced Capability Header **Default Value: 1801 0002h**

Bit	Attribute	Default	Description
31:20	RO	180h	**Next Capability Offset**
19:16	RO	1h	**Capability Version**
15:0	RO	0002h	**PCI Express Extended Capability ID**

Offset Address: 147-144h (D2F0)
Port VC Capability 1 **Default Value: 0000 0001h**

Bit	Attribute	Default	Description
31:12	RO	0	**Reserved**
11:10	RO	0	**Port Arbitration Table Entry Size** Reserved for root port.
9:8	RO	0	**Reference Clock** Reserved for root port.
7	RO	0	**Reserved**
6:4	RO	0	**Low Priority Extended VC Count**
3	RO	0	**Reserved**
2:0	RO	001b	**Extended VC Count**

Offset Address: 14B-148h (D2F0)
Port VC Capability 2 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RO	00b	**VC Arbitration Table Offset** 00 since only VC0 is defined
23:8	RO	0	**Reserved**
7:0	RO	0	**VC Arbitration Capability** Reserved

Offset Address: 14D-14Ch (D2F0)
Port VC Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15:4	RO	0	**Reserved**
3:1	RW	0	**VC Arbitration Select** Reserved
0	RO	0	**Local VC Arbitration Table** Reserved

Offset Address: 14F-14Eh (D2F0)
Port VC Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15:1	RO	0	**Reserved**
0	RO	0	**VC Arbitration Table Status** Reserved

VC0 Resource (150-15Bh)

Offset Address: 153-150h (D2F0)
VC Resource Capability (VC0) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RO	0	**Port Arbitration Table Offset (VC0)** Reserved for Root Port.
23	RO	0	**Reserved**
22:16	RO	0	**Maximum Time Slots (TL)**
15	RO	0	**Reject Snoop Transactions**
14	RO	0	**Advanced Packet Switching** Reserved
13:8	RO	0	**Reserved**
7:0	RO	0	**Port Arbitration Capability** Reserved for Root Port.

Offset Address: 157-154h (D2F0)
VC Resource Control (VC0) **Default Value: 8000 00FFh**

Bit	Attribute	Default	Description
31	RO	1b	**VC Enable**
30:27	RO	0	**Reserved**
26:24	RO	0	**VC ID**
23:20	RO	0	**Reserved**
19:17	RW	0	**Port Arbitration Select** Reserved for Root Port
16	RO	0	**Load Port Arbitration Table** Reserved for Root Port
15:8	RO	0	**Reserved**
7:0	RW Bit 0: RO	FFh	**TC/VC Mapping** This field indicates the TCs that are mapped to VC0. If bit [n] is 1, the corresponding traffic class TCn is mapped to VC0 (0 <= n <= 7). Default is TC0, TC1, TC2, TC3, C4, TC5, TC6 and TC7 are all mapped to VC0. Note: Bit 0 is hardwired to 1 (i.e. TC0 is always mapped to VC0).

Offset Address: 15B-158h (D2F0)
VC Resource Status (VC0) **Default Value: 0002 0000h**

Bit	Attribute	Default	Description
31:18	RO	0	**Reserved**
17	RO	1b	**VC Negotiation Pending (TL)** This bit indicates whether the Virtual Channel negotiation is in Pending state (set/clear by hardware) 0: Negotiation is complete 1: Negotiation is on-going.
16	RO	0	**Port Arbitration Table Status** Reserved for Root Port
15:0	RO	0	**Reserved**

VC1 Resource (15C-167h)

The following registers exist only when Rx144[0] is programmed to 1. If Rx144[0]=0, all the following content will be read as 0.

Offset Address: 15F-15Ch (D2F0)

VC Resource Capability (VC1) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RO	0	**Port Arbitration Table Offset (VC1)** Reserved for Root Port
23	RO	0	**Reserved**
22:16	RO	0	**Maximum Time Slots (TL)**
15	RO/RW	0	**Reject Snoop Transactions**
14	RO	0	**Advanced Packet Switching** Reserved
13:8	RO	0	**Reserved**
7:0	RO	0	**Port Arbitration Capability** Reserved for Root Port

Offset Address: 163-160h (D2F0)

VC Resource Control (VC1) **Default Value: 0100 0000h**

Bit	Attribute	Default	Description
31	RW	0	**VC Enable**
30:27	RO	0	**Reserved**
26:24	RW	1h	**VC ID**
23:20	RO	0	**Reserved**
19:17	RW	0	**Port Arbitration Select** Reserved for Root Port
16	WO	0	**Load Port Arbitration Table** Reserved for Root Port
15:8	RO	0	**Reserved**
7:0	RW Bit 0: RO	0	**TC/VC Mapping** This field indicates the TCs that are mapped to VC1. If bit [n] is 1, the corresponding traffic class TCn is mapped to VC1 (0 <= n <= 7). Default is TC0, TC1, TC2, TC3, C4, TC5, TC6 and TC7 are all mapped to VC0. Note: Bit0 is hardwired to 0 (i.e. TC0 is always mapped to VC0).

Offset Address: 167-164h (D2F0)

VC Resource Status (VC1) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:18	RO	0	**Reserved**
17	RO	0	**VC Negotiation Pending (TL)** This bit indicates whether the Virtual Channel negotiation is in Pending state (set/clear by hardware) 0: Negotiation is complete 1: Negotiation is on-going.
16	RO	0	**Port Arbitration Table Status** Reserved for Root Port
15:0	RO	0	**Reserved**

Root Complex Topology Capability List Registers (180-19Bh)

Offset Address: 183-180h (D2F0)

Root Complex Link Declaration Capabilities Header **Default Value: 0001 0005h**

Bit	Attribute	Default	Description
31:20	RO	0	**Next Capability**
19:16	RO	1h	**Capability Version**
15:0	RO	0005h	**Capability ID**

Offset Address: 187-184h (D2F0)

Element Self Description Register **Default Value: 0101 0100h**

Bit	Attribute	Default	Description
31:24	RO	01h	**Port Number (Root Port 0)**
23:16	RO	01h	**Component ID**
15:8	RO	01h	**Number of Link Entries**
7:4	RO	0	**Reserved**
3:0	RO	0h	**Element Type** 00: Configuration Space Element 01: System egress port or internal sink 10: Internal Root Complex Link

Offset Address: 193-190h (D2F0)

Upstream Link Descriptor Register **Default Value: 0001 0001h**

Bit	Attribute	Default	Description
31:24	RO	0	**Target Port Number** Indicate the port number of RCRB-H
23:16	RO	01h	**Target Component ID**
15:2	RO	0	**Root Complex Link Declaration Capability**
1	RO	0	**Link Type** Indicates that the link points to RCRB-H
0	RO	1b	**Link Valid**

Offset Address: 19B-194h (D2F0)

Upstream Link Base Address Register **Default Value: 0000 0000 0000 0000h**

Bit	Attribute	Default	Description
63:32	RO	0	**Base Address Upper.**
31:0	RO	0	**Base Address Lower**

Note: Base Address Register value for RCRB-H [63:12]

Offset Address: 19F-19Ch (D2F0) – Reserved

Device 3 Function 0 (D3F0) – PCI Express Root Port 0 (x1) (PCI-to-PCI Virtual Bridge)

Device3 Function 0, a 1-Lane PCI Express root port, is connected to the PCI bus through AD14 as the IDSEL.
All registers are located in PCI configuration space and should be programmed using PCI configuration mechanism 1 through I/O registers CF8 / CFC with bus number 0, device number 3 and function number 0.

Header Registers (0-3Fh)

Offset Address: 1-0h (D3F0)
Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**Vendor ID**

Offset Address: 3-2h (D3F0)
Device ID **Default Value: C364h**

Bit	Attribute	Default	Description
15:0	RO	C364h	**Device ID**

Offset Address: 5-4h (D3F0)
Command Register **Default Value: 0000h**

Bit	Attribute	Default	Description
15:11	RO	0	**Reserved**
10	RW	0	**Interrupt Disabled** Set when the device is prevented from generating INTx messages
9	RO	0	**Reserved**
8	RW	0	**SERR# Enable** 0: Disable error report 1: Enable reporting of non-fatal and fatal errors
7	RO	0	**Reserved**
6	RW	0	**Parity Error Response** 0: Ignore parity errors & continue 1: Take normal action on detected parity errors
5:3	RO	0	**Reserved**
2	RW	0	**Bus Master Enable** 0: Disable 1: Enable Controls the ability to forward Memory and I/O Read/Write requests in the upstream direction. Disabling this bit disables MSI messages.
1	RW	0	**Memory Space** 0: Ignore downstream memory transactions; memory cycles with address falling in the claimed range will be forwarded to the SB 1: Enable downstream memory cycle to this port if its address falling in the claimed range of this device.
0	RW	0	**I/O Space** 0: Ignore downstream I/O transactions; I/O cycles with address falling in the claimed range will be forwarded to the SB. 1: Enable downstream I/O cycle to this port if its address falling in the claimed range of this device.

Offset Address: 7-6h (D3F0)
Status Register **Default Value: 0010h**

Bit	Attribute	Default	Description
15	RW1C	0	**Detected Parity Error** This bit is set whenever a poisoned TLP is received, regardless the state of Parity Error Enabled (Rx4[6])
14	RW1C	0	**Signaled System Error** This bit is set when: 1. A device sends an ERR_FATAL or ERR_NONFATAL message 2. Rx4[8] = 1
13	RW1C	0	**Received Master Abort** This bit is set when receiving a completion with Unsupported Request Completion Status
12	RW1C	0	**Received Target Abort** This bit is set when receiving a completion with Completer Abort Completion Status
11	RW1C	0	**Signaled Target Abort** This bit is set when completing a Request with Completer Abort Completion Status
10:9	RO	0	**Reserved** Always reads 0.
8	RW1C	0	**Master Data Parity Error** This bit is set if Parity Error Enable bit (Rx4[6]) is set and either one of the following two conditions occurs: 1. Requestor receives a Completion marked poisoned 2. Requestor poisons a write Request
7:5	RO	0	**Reserved**
4	RO	1b	**Capabilities List** Indicates the presence of an extended capability list item. Always set to 1 for PCI Express device
3	RO	0	**Interrupt Status** Indicates an INTx message is pending internally (TL)
2:0	RO	0	**Reserved**

Offset Address: 8h (D3F0)
Revision ID **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Revision Code**

Offset Address: 0B-9h (D3F0)
Class Code **Default Value: 06 0400h**

Bit	Attribute	Default	Description
23:0	RO	060400h	**Class Code**

Offset Address: 0Ch (D3F0)
Cache Line Size **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Cache Line Size –** Reserved (No impact on functionality)

Offset Address: 0Dh (D3F0)
Master Latency Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Master Latency Timer –** Reserved (Hardwired to 0)

Offset Address: 0Eh (D3F0)
Header Type **Default Value: 81h**

Bit	Attribute	Default	Description
7:0	RO	81h	**Header Type Code** A multiple function device.

Offset Address: 0Fh (D3F0)
Built In Self Test (BIST) **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**BIST Support**

Offset Address: 17-10h (D3F0)
Base Address **Default Value: 00h**

Bit	Attribute	Default	Description
63:0	RO	0	**Base Address**

Offset Address: 18h (D3F0)
Primary Bus Number **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Primary Bus Number**

Offset Address: 19h (D3F0)
Secondary Bus Number **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Secondary Bus Number**

Offset Address: 1Ah (D3F0)
Subordinate Bus Number **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Subordinate Bus Number**

Offset Address: 1Bh (D3F0)
Secondary Latency Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Secondary Latency Timer** Reserved

Offset Address: 1Ch (D3F0)
I/O Base **Default Value: F0h**

Bit	Attribute	Default	Description
7:4	RW	Fh	**I/O Base (AD[15:12] - inclusive)** This bridge will forward the cycles from primary side to PCI if the IO address AD[15:12] is between IO base and IO limit (Rx1D)
3:0	RO	0	**I/O Addressing Capability** 0 means IO addressing is 16-bit only.

Offset Address: 1Dh (D3F0)
I/O Limit **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**I/O Limit (AD[15:12] - inclusive)** This bridge will forward the cycles from primary side to PCI if the IO address[15:12] is between IO base (Rx1C) and IO limit.
3:0	RO	0	**I/O Addressing Capability** 0 means IO addressing is 16-bit only.

Offset Address: 1F-1Eh (D3F0)
Secondary Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15	RW1C	0	**Detected Parity Error** This bit is set when secondary side receives a poisoned TLP regardless of Rx4[6]
14	RW1C	0	**Received System Error** This bit is set when 1. A device sends an ERR_FATAL or ERR_NONFATAL message 2. Rx4[8] is 1
13	RW1C	0	**Received Master Abort**
12	RW1C	0	**Received Target Abort**
11	RW1C	0	**Signaled Target Abort**
10:9	RO	0	**Reserved**
8	RW1C	0	**Master Data Parity Error** This bit is set if Parity Error Enable bit (Rx4[6]) is set and either one of the following two conditions occurs: 1. Requestor receives a Completion marked poisoned. 2. Requestor poisons a write Request
7:0	RO	0	**Reserved**

Offset Address: 21-20h (D3F0)
Memory Base **Default Value: FFF0h**

Bit	Attribute	Default	Description
15:4	RW	FFFh	**Memory Base (AD[31:20] – inclusive)** The address [19:0] is not decoded.
3:0	RO	0	**Reserved** Always reads 0.

Offset Address: 23-22h (D3F0)
Memory Limit **Default Value: 0000h**

Bit	Attribute	Default	Description
15:4	RW	0	**Memory Limit (AD[31:20])** The address [19:0] is not decoded.
3:0	RO	0	**Reserved** Always reads 0.

Offset Address: 25-24h (D3F0)
Prefetchable Memory Base **Default Value: FFF1h**

Bit	Attribute	Default	Description
15:4	RW	FFFh	**Prefetchable Memory Base AD[31:20]**
3:0	RO	1b	**Reserved** (Do not program)

Offset Address: 27-26h (D3F0)
Prefetchable Memory Limit **Default Value: 0001h**

Bit	Attribute	Default	Description
15:4	RW	0	**Prefetchable Memory Limit AD[31:20]**
3:0	RO	1b	**Reserved** (Do not program)

Offset Address: 2B-28h (D3F0)
Prefetchable Memory Upper Base **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:4	RO	0	**Reserved**
3:0	RW	0	**AD[35:32]** This chip supports up to 16G

Offset Address: 2F-2Ch (D3F0)
Prefetchable Memory Upper Limit **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:4	RO	0	**Reserved**
3:0	RW	0	**AD[35:32]** This chip supports up to16G

Offset Address: 31-30h (D3F0)
I/O Base Upper **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RO	0	**I/O Base Upper 16 bits Address**

Offset Address: 33-32h (D3F0)
I/O Base Limit **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RO	0	**I/O Limit Upper 16 bits Address**

Offset Address: 34h (D3F0)
Capability Pointer **Default Value: 40h**

Contains an offset from the start of configuration space.

Bit	Attribute	Default	Description
7:0	RO	40h	**Capability Pointer** Capability Pointer: Rx34 → Rx40 → Rx68 → Rx70 → Rx88 → Rx98 → NULL

Offset Address: 35-3Bh (D3F0) – Reserved

Offset Address: 3Ch (D3F0)
Interrupt Line **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**INT Line** (For Software Use Only)

Offset Address: 3Dh (D3F0)

Interrupt Pin **Default Value: 01h**

Bit	Attribute	Default	Description
7:0	RO	01h	**INT Pin** 01: INTA

Offset Address: 3F-3Eh (D3F0)

Bridge Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15:7	RO	0	**Reserved**
6	RW	0	**Secondary Bus Reset** 0: No reset 1: Triggers a warm reset on the corresponding PCI Express Port
5	RO	0	**Reserved**
4	RW	0	**Base VGA 16 bits Decode** 0: All VGA alias range will be forwarded 1: Only forward base VGA range (Alias range will not be forwarded)
3	RW	0	**VGA Compatible I/O and Memory Address Range** 0: Do not forward VGA compatible memory and I/O 1: Forward VGA compatible memory and I/O Note: VGA addresses are memory A0000-BFFFFh and I/O addresses 3B0-3BBh, 3C0-3CFh and 3D0-3DFh (10-bit decode). "Mono" text mode uses B0000-B7FFFh and "Color" Text Mode uses B8000-BFFFFh. Graphics modes use Axxxxh. Mono VGA uses I/O addresses 3Bx-3Cxh and Color VGA uses 3Cx-3Dxh. If an MDA is present, a VGA will not use the 3Bxh I/O addresses and B0000-B7FFFh memory space; if not, the VGA will use those addresses to emulate MDA modes.
2	RW	0	**Block/Forward ISA I/O Cycles** 0: Forward all I/O cycles with address in the range defined by the I/O Base and I/O Limit 1: Do not forward ISA I/O that are in the top 768 bytes of each 1K byte block address range
1	RW	0	**SERR Enable** Controls the forwarding of ERR_COR, ERR_NONFATAL and ERR_FATAL from secondary to primary 0: Disable 1: Enable
0	RW	0	**Parity Error Response Enable** 0: Ignore the response to poisoned TLPs 1: Enable the response to poisoned TLPs

PCI Express Capability Registers (40-63h)

Offset Address: 41-40h (D3F0)

PCI Express List **Default Value: 6810h**

Bit	Attribute	Default	Description
15:8	RO	68h	**Next Pointer**
7:0	RO	10h	**Capability ID**

Offset Address: 43-42h (D3F0)

PCI Express Capabilities **Default Value: 0141h**

Bit	Attribute	Default	Description
15	RO	0	**Reserved**
14	RO	0	**TCS Routing Supported**
13:9	RO	0	**Interrupt Message Number**
8	RO	1b	**Slot Implemented** This bit when set indicates that the PCI Express Link associated with this Port is connected to a slot (as compared to being connected to an integrated component or being disabled),
7:4	RO	0100b	**Device / Port Type** 0100b: Root Port of PCI Express Root Complex
3:0	RO	0001b	**Capability Version**

Offset Address: 47-44h (D3F0)
Device Capabilities **Default Value: 0000 8001h**

Bit	Attribute	Default	Description
31:28	RO	0	**Reserved**
27:26	RO	0	**Captured Slot Power Limit Scale** Reserved. For upstream port only.
25:18	RO	0	**Captured Slot Power Limit Value** Reserved. For upstream port only.
17:16	RO	0	**Reserved**
15	RO	1b	**Role-Based Error Reporting**
14	RO	0	**Power Indicator Present** Reserved. For upstream port only.
13	RO	0	**Attention Indicator Present** Reserved. For upstream port only.
12	RO	0	**Attention Button Present** Reserved. For upstream port only.
11:9	RO	0	**Endpoint L1 Acceptable Latency** 111b: more than 64us
8:6	RO	0	**Endpoint L0s Acceptable Latency** Default is set by hardware initial.
5	RO	0	**Extended Tag Field Supported** 0: 5-bit Tag field supported 1: 8-bit Tag field supported
4:3	RO	0	**Phantom Functions Supported** Reserved
2:0	RO	001b	**Max Payload Size Supported** 001b: 32QW (256 bytes)

Offset Address: 49-48h (D3F0)
Device Control **Default Value: 0810h**

Bit	Attribute	Default	Description
15	RO	0	**Reserved**
14:12	RO	000b	**Max Read Request Size** 000: 128 bytes This field sets the maximum Read Request size for the device as a Requestor.
11	RW	1b	**Enable No Snoop** 0: Disable 1: Enable. If this bit is set to 1, the device is permitted to set the No Snoop bit in the Requestor Attributes of the transactions it initiate that do not require hardware enforced cache coherency.
10	RWS	1b	**Auxiliary Power PM Enable** This bit when set enables device to draw AUX power independent of PME AUX power.
9	RO	0	**Phantom Functions Enable**
8	RO/RW	0	**Extended Tag Field Enable** When Rx44[5] is set to 0, this bit is RO When Rx44[5] is set to 1, this bit is RW
7:5	RW	0	**Max Payload Size** Maximum TLP payload size.
4	RW	0	**Enable Relaxed Ordering** 0: Disable 1: Enable. If this bit is set to 1, the device is permitted to set the Relaxed Ordering bit in the Requestor Attributes of the transactions it initiate that do not require strong write ordering.
3	RW	0	**Unsupported Request Reporting Enable**
2	RW	0	**Fatal Error Reporting Enable** For a Root Port, the reporting of Fatal errors is internal to the root. No external ERR_FATAL message is generated.
1	RW	0	**Non-Fatal Error Reporting Enable** For a Root Port, the reporting of Non-Fatal errors is internal to the root. No external ERR_NONFATAL message is generated.
0	RW	0	**Correctable Error Reporting Enable** For a Root Port, the reporting of correctable errors is internal to the root. No external ERR_COR message is generated.

Offset Address: 4B-4Ah (D3F0)

Device Status **Default Value: 0010h**

Bit	Attribute	Default	Description
15:6	RO	0	**Reserved**
5	RO	0	**Transactions Pending** This bit when set indicates that the Port has issued Non-Posted Requests on its own behalf (using the Port's own Requestor ID) which have not been completed.
4	RO	1b	**AUX Power Detected**
3	RW1C	0	**Unsupported Request Detected (TL)**
2	RW1C	0	**Fatal Error Detected (TL)**
1	RW1C	0	**Non-Fatal Error Detected (TL)**
0	RW1C	0	**Correctable Error Detected (TL)**

Offset Address: 4F-4Ch (D3F0)

Link Capabilities **Default Value: 0118 3C11h**

Bit	Attribute	Default	Description
31:24	RO	01h	**Port Number** This field indicates the PCI Express Port number for the given PCI Express Link.
23:21	RO	0	**Reserved**
20	RO	1b	**Data Link Layer Link Active Reporting Capable**
19	RO	1b	**Surprise Down Error Reporting Capable**
18	RO	0	**Clock Power Management**
17:15	RO	000b	**L1 Exit Latency** 000: less than 1us. The value reported indicates the length of time this Port requires to complete transition from L1 to L0.
14:12	RO	011b	**L0s Exit Latency** 000: less than 64ns. The value reported indicates the length of time this Port requires to complete transition from L0s to L0.
11:10	RO	11b	**Active State Link PM (ASPM) Support** 11b: L0s and L1 supported. This field indicates the level of ASPM supported on the PCI Express Link.
9:4	RO	000001b	**Maximum Link Width** 010000b for x16 Link width 000001b for x1 Link width
3:0	RO	1h	**Maximum Link Speed** 1h: 2.5Gb/s Link speed

Offset Address: 51-50h (D3F0)

Link Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15:9	RO	0	**Reserved**
8	RO	0	**Enable Clock Power Management**
7	RW	0	**Extended Synch** 0: FCU Timer limit is 30us 1: FCU Timer limit is 120us
6	RW	0	**Common Clock Configuration** 0: Indicates that this Port and the component on the opposite end of the Link are operating with asynchronous reference clock. 1: Indicates that this Port and the component on the opposite end of the Link are operating with a distributed common reference clock.
5	RW1C	0	**Retrain Link** A write of 1 to this bit initiates Link retrained by directing the Physical Layer LTSSM to the Recovery state.
4	RW	0	**Link Disable** This bit disables the Link when set to 1.
3	RO	0	**Read Completion Boundary** 0: 64 byte
2	RO	0	**Reserved**
1:0	RW	00b	**Link Active State PM (ASPM) Control** 00b: Disabled 01b: L0s Entry Enabled 10b: L1 Entry Enabled 11b: L0s and L1 Entry Enabled

Offset Address: 53-52h (D3F0)

Link Status **Default Value: 0nn1h**

Bit	Attribute	Default	Description
15:14	RO	0	**Reserved**
13	RO	0	**Data Link Layer Link Active**
12	RO	1b	**Slot Clock Configuration (TL)** 0: Use an independent clock irrespective of the presence of a reference on the connector. 1: Use the same physical reference clock that the platform provides on the connector.
11	RO	0	**Link Training (PHY)** This bit indicated that Link training is in progress (Physical Layer LTSSM is in Configuration or Recovery state) or that 1b was written to the Retrain Link bit but Link training has not yet begun. Hardware clears this bit once Link training is complete.
10	RO	0	**Training Error (PHY)** Set when a Link training error occurred. Cleared by hardware upon successfully training of the Link to the L0 Link state.
9:4	RO	HwInit	**Negotiated Link Width (PHY)** Default value set by hardware initial. 000001: x1 000010: x2 000100: x4 001000: x8 010000: x16
3:0	RO	0001b	**Link Speed** 0001: 2.5Gb/s negotiated Link speed.

Offset Address: 57-54h (D3F0)

Slot Capabilities **Default Value: 0000 0060h**

Bit	Attribute	Default	Description
31:19	RO	0	**Physical Slot Number** **Physical slot number attached to the Port.**
18	RO	0	**No Command Completed Support**
17	RO	0	**Electromechanical Interlock Present**
16:15	RO	0	**Slot Power Limit Scale** Reserved
14:7	RO	0	**Slot Power Limit Value** Reserved
6	RO	1b	**Hot-plug Capable** Reserved
5	RO	1b	**Hot-plug Surprise** Reserved
4	RO	0	**Power Indicator Present** Reserved
3	RO	0	**Attention Indicator Present** Reserved
2	RO	0	**MRL Sensor Present** Reserved
1	RO	0	**Power Controller Present** Reserved
0	RO	0	**Attention Button Present** Reserved

Offset Address: 59-58h (D3F0)

Slot Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15:13	RO	0	**Reserved**
12	RW	0	**Slot Control Register: Data Link Layer State Changed Enable** 0: Disable 1: Enable
11	RO	0	**Electromechanical Interlock Control**
10	RO	0	**Power Controller Control** Reserved
9:8	RW	00b	**Power Indicator Control** Reserved
7:6	RW	00b	**Attention Indicator Control** Reserved
5	RW	0	**Hot-Plug Interrupt Enable** Reserved
4	RW	0	**Command Completed Interrupt Enable** Reserved
3	RW	0	**Presence Detect Changed Enable** Reserved
2	RO	0	**MRL Sensor Changed Enable** Reserved
1	RO	0	**Power Fault Detected Enable** Reserved
0	RW	0	**Attention Button Pressed Enable** Reserved

Offset Address: 5B-5Ah (D3F0)

Slot Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15:9	RO	0	**Reserved**
8	RW1C	0	**Slot Status Register: Data Link Layer State Changed**
7	RO	0	**Reserved**
6	RO	0	**Presence Detect State** 0: Slot empty 1: Card present in slot
5	RO	0	**MRL Sensor State** Reserved
4	RW1C	0	**Command Completed**
3	RW1C	0	**Presence Detect Changed**
2	RO	0	**MRL Sensor Changed**
1	RO	0	**Power Fault Detected**
0	RW1C	0	**Attention Button Pressed**

Offset Address: 5D-5Ch (D3F0)
Root Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15:5	RO	0	**Reserved**
4	RO	0	**CRS Software Visibility Enable**
3	RW	0	**PME Interrupt Enable** 0: Disable 1: Enable interrupt generation upon receipt of a PME message as reflected in the PME status register bit. A PME interrupt is also generated if the PME status register bit is set when this bit is set from a cleared state.
2	RW	0	**System Error on Fatal Error Enable** 0: Disable 1: Enable generation of a System Error if a Fatal Error (ERR_FATAL) is reported by any of the devices in the hierarchy associated with the Root Port, or by the Root Port itself.
1	RW	0	**System Error on Non-Fatal Error Enable** 0: Disable 1: Enable generation of a System Error if a Non-Fatal Error (ERR_NONFATAL) is reported by any of the devices in the hierarchy associated with the Root Port, or by the Root Port itself.
0	RW	0	**System Error on Correctable Error Enable** 0: Disable 1: Enable generation of a System Error if a Correctable Error (ERR_COR) is reported by any of the devices in the hierarchy associated with the Root Port, or by the Root Port itself.

Offset Address: 5Eh (D3F0)
CRS Visibility Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RO	0	**Reserved**
0	RO	0	**CRS Software Visibility Enable**

Offset Address: 5Fh (D3F0) – Reserved

Offset Address: 63-60h (D3F0)
Root Status **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:18	RO	0	**Reserved**
17	RO	0	**PME Pending (TL)** 0: No pending PME 1: Indicates that another PME is pending when the PME Status (bit 16) is set.
16	RW1C	0	**PME Status (TL)** Indicates that the PME was asserted by the Requestor ID indicated in PME Requestor ID (bit[15:0]).
15:0	RO	0	**PME Requestor ID (TL)** The Requestor ID of the last PME Requestor.

Offset Address: 67-64h (D3F0) – Reserved

PCI Power Management Capability Structure Registers (68-6Fh)

Offset Address: 6B-68h (D3F0)

Power Management Capabilities **Default Value: C822 7001h**

Bit	Attribute	Default	Description
31:27	RO	19h	**PME Support** Bit 31, 30 and 27 are set to 1b (PME Message will be forwarded).
26	RO	0	**D2 Support**
25	RO	0	**D1 Support**
24:22	RO	0	**AUX Current**
21	RO	1b	**Device Specific Initialization**
20:19	RO	0	**Reserved**
18:16	RO	010b	**Version**
15:8	RO	70h	**Next Capability Pointer**
7:0	RO	01h	**Capability ID**

Offset Address: 6F-6Ch (D3F0)

Power Management Status/Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RO	0	**Power Management Data**
23:16	RO	0	**Reserved**
15	RW1CS	0	**PME Status** This bit's setting is not modified by hot, warm, or cold reset.
14:13	RO	0	**Data Scale**
12:9	RO	0	**Data Select**
8	RWS	0	**PME Enable** This bit's setting is not modified by hot, warm, or cold reset.
7:2	RO	0	**Reserved**
1:0	RW	0	**Power State**

PCI Message Signal Interrupt (MSI) Capability Structure Registers (70-87h)

Offset Address: 73-70h (D3F0)

MSI Capability Support **Default Value: 0180 8805h**

Bit	Attribute	Default	Description
31:25	RO	0	**Reserved**
24	RO	1b	**This MSI capability supports pre-vector masking capability**
23	RO	1b	**This MSI Capability Supports 64 Bit Message Address Only**
22:20	RW	000b	**Multiple Message Enable** 000: 1 message allocated 001: 2 message allocated 010: 4 message allocated 011: 8 message allocated 100: 16 message allocated 101: 32 message allocated 11x: Reserved
19:17	RO	000b	**Multiple Message Capable** 000: 1 message requested 001: 2 message requested 010: 4 message requested 011: 8 message requested 100: 16 message requested 101: 32 message requested 11x: Reserved
16	RW	0	**MSI Enable** 0: This Port is prohibited from using MSI to request service 1: This Port is permitted to use MSI to request service.
15:8	RO	88h	**Next Pointer**
7:0	RO	05h	**Capability ID**

Offset Address: 77-74h (D3F0)
System-Specified Message Address - Low **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:2	RW	0	**System-Specified Message Address Bit [31:2]**
1:0	RO	0	**System-Specified Message Address Bit [1:0]** These bits will always read as 0

Offset Address: 7B-78h (D3F0)
System-Specified Message Address - High **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:4	RW	0	**System-Specified Message Address Bit [63:36]** The chip supports address up to A35.
3:0	RW	0	**System-specified Message Address [35:32]**

Offset Address: 7D-7Ch (D3F0)
Message Data **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW	0	**Message Data** The message data is to be put on data [15:0] of MSI cycles

Offset Address: 7F-7Eh (D3F0) – Reserved

Offset Address: 83-80h (D3F0)
Message Mask Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:1	RO	0	**Reserved**
0	RW	0	**Mask Bit for Message 0**

Offset Address: 87-84h (D3F0)
Message Pending Status **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:1	RO	0	**Reserved**
0	RO	0	**Pending Bit for Message 0**

HyperTransport Message Signal Interrupt (MSI) Capability Structure Registers (88-8Bh)

Offset Address: 8B-88h (D3F0)
MSI Capability Support **Default Value: A802 9808h**

Bit	Attribute	Default	Description
31:27	RO	10101b	**Capability Type**
26:18	RO	0	**This MSI capability support pre-vector masking capability**
17	RO	1b	**HT-MSI this chip support is only for MSI address like 00000000_FEEx_xxxx.**
16	RW	0	**MSI Enable** 0: This port is prohibited from using MSI to request service. 1: This port is permitted to use MSI to request service.
15:8	RO	98h	**Next Pointer**
7:0	RO	08h	**Capability ID**

Offset Address: 97-8Ch (D3F0) – Reserved

Subsystem ID and Subsystem Vendor ID Capability Structure Registers (98-9Fh)

Offset Address: 98h (D3F0)

Capability ID **Default Value: 0Dh**

Bit	Attribute	Default	Description
7:0	RO	0Dh	**Capability ID**

Offset Address: 99h (D3F0)

Next Pointer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Next Pointer**

Offset Address: 9D-9Ch (D3F0)

Subsystem Vendor ID Control **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**Subsystem Vendor ID**

Offset Address: 9F-9Eh (D3F0)

Subsystem ID Control **Default Value: C323h**

Bit	Attribute	Default	Description
15:0	RO	C323h	**Subsystem ID**

PCI Express Transaction Layer Registers (A0-A7h)

Offset Address: A0h (D3F0)

Downstream Control 1 **Default Value: 01h**

Bit	Attribute	Default	Description
7	RW	0	**Downstream Cycles Have Traffic Class TC1** 0: Disabled 1: Enabled
6	RW	0	**Downstream Cycles Have Attribute "No Snoop" Set** 0: Disabled 1: Enabled
5	RW	0	**Downstream Cycles Have Attribute "Relaxed Ordering" Set** 0: Disabled 1: Enabled
4	RW	0	**Downstream Lock Cycle Support** 0: Disabled 1: Enabled
3	RW	0	**Downstream Arbitration Scheme** 0: Fixed priority: VC1 CPL > VC0 CPL > Down Stream Command 1: Round Robin arbitration priority between VC1 CPL, VC0 CPL and Down Stream Command
2	RW	0	**Downstream Post-Write Allowed to Pass IOW** 0: Not allowed. 1: Allowed
1	RW	0	**Downstream Post-Write Allowed to Pass Read** 0: Not allowed. 1: Allowed
0	RW	1b	**Downstream Pipeline** 0: Disabled 1: Enabled

Offset Address: A1h (D3F0)

Downstream Control 2 **Default Value: 14h**

Bit	Attribute	Default	Description
7	RW1C	0	**Downstream Configuration Completion Status** 0: Normal completion. 1: At least one configuration request ended with a CRS (Configuration Request Retry Status) completion.
6	RO	0	**Reserved**
5	RW	0	**For the Data Return of Upstream Read Requests** 0: The chip always checks CPL credit unless when endpoint advertises infinite CPL credits. 1: The chip does not check CPL credit even when endpoint advertises finite CPL credits.
4	RW	1b	**Transaction Layer Downstream Does Not Check Downstream PH Credit for PME_TURN_OFF Message as the PCIe V1.1 Spec requirement** 0: Disable 1: Enable
3	RW	000b	**C2P Read Completion Timer for Vector Development Mode** When this bit is set to 1, the timer defined in RxA1[2:0] becomes: 000: 1us 001: 3us 010: 10us 011: 20us 100: 50us 101: 100us 110: 200us 111: 500us
2:0	RW	100b	**C2P Read Completion Timeout Timer** 000: Reserved 001: 1ms 010: Reserved 011: 10ms (Spec. lower bound) 100: 30ms 101: Reserved 110: Reserved 111: Reserved

Offset Address: A2h (D3F0)

Downstream Control 3 **Default Value: 30h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6:4	RW	011b	**Waiting for GNT Timer for Priority Arbitration Mode** Priority VC1 > VC0 > C2P request when set RxA0[3] = 0. If GNT timer of VC0/C2P request expires, VC0/C2P request will become higher priority. 000: 4ns 001: 16ns 010: 32ns 011: 64ns 100: 96ns 101: 128ns 110: 256ns 111: 512ns
3	RO	0	**Reserved**
2	RW	0	**Pending C2P NP Cycle Blocks L1 Entry** 0: Disable. L1 entry won't consider C2P NP completion 1: Enable. L1 entry will need to wait for C2P NP completions
1:0	RW	00b	**Downstream Arbitration Parking** 00: GNT park on the last request source 01: GNT park on VC1 completion. If VC1 is not enabled (or no VC1), park on VC0 completion 10: GNT park on VC0 completion 11: GNT park on C2P request

Offset Address: A3h (D3F0)

Downstream Control 4 **Default Value: 7Ch**

Bit	Attribute	Default	Description
7:4	RW	0111b	**Retry Buffer Level** Bit 7: Read only 0000: 1-level 0001: 2-level 0010: 3-level 0011: 4-level 0100: 5-level 0101: 6-level 0110: 7-level 0111: 8-level 1xxx: Reserved
3	RW	1b	**Downstream Read Retry Time Out Control. in DL_Down State** 0: Disable downstream read retry time out. If bit 0 is set to 1, downstream read request will always wait for DL_DLUp assertion then retry. 1: Enable downstream read retry time out (when bit 0 is set to 1b and bit 1 is set to 0b). The timer is the same as completion time out timer. After time out, this read request will not be retried again even DL_DLUp assertion.
2	RW	1b	**Downstream Cycle Control/Latency Improvement** 0: Disable downstream HPOP/DPOP assert at the same time 1: Enable downstream HPOP/DPOP assert at the same time
1	RW	0	**CPL Timer Control** 0: Enable. Refer to D3F0 RxA1[2:0] 1: Disable
0	RW	0	**Downstream Read Cycle Retry Register** 0: When DL_DOWN is asserted, transaction layer returns "FF" to PXPTRF for C2P read cycle. 1: When DL_DOWN is asserted, transaction layer holds C2P read cycle and this incompleted C2P read cycle will be retried when DL_UP is asserted.

Offset Address: A4h (D3F0)

Upstream Control **Default Value: 5Ch**

Bit	Attribute	Default	Description
7	RW	0	**Upstream Address A35-A31 Forced to 0** 0: Disabled 1: Enabled for system testing or loop back mode test. The upcoming data may be checked in the system memory
6	RW	1b	**Guard bit for improving timing to prevent upstream write FIFO from being overwritten**
5	RW	0	**Upstream Checking Malformed TLP through "Byte Enable Rule" And "Over 4K Boundary Rule"** 0: Disabled 1: Enabled
4	RW	1b	**Downstream Read Wait Till The Upstream Write Data Flushed** 0: Disabled 1: Enabled
3	RW	1b	**Infinite Flow Control** 0: Advertise credits 2, 4, 1 for CPLH, CPLD, NPD (4DW as the units), update credits when device responds normally 1: CPLH & CPLD & NPD Become Infinite mode
2	RW	1b	**Flow Control Update for Each Header** 0: Current Design (update header credit whenever received two TLPHs 1: Update header credit whenever received TLPH (including PH, NPH and CPLH)
1	RW	0	**VC1 Request Queue Usage (when VC1 is disabled in the capability header; i.e. Rx144[0] = 0)** 0: Disabled 1: Enabled. It allows Transaction Layer map non-snoop upstream request through VC1 Request Queue to the Central Traffic Controller (Note that when this bit is 1, bit-0 has to be 0).
0	RW	0	**C2P Completion Timeout Timer Value Control When PHY Retrain Link or In Configuration State** 0: Keep the timeout value 1: Reset the timeout value

Offset Address: A5h (D3F0)
Credit Advertisement Control **Default Value: FFh**

Bit	Attribute	Default	Description
7:4	RW	1111b	**Upstream Posted (write) Data FIFO Size, and the Initial PD Credit Value** 0011: 4-line upstream write FIFO size, and initial PD credit = ‘h20 0010: 3-line upstream write FIFO size, and initial PD credit = ‘h10 0001: 2-line upstream write FIFO size, and initial PD credit = 'h8 0000: 1-line upstream write FIFO size, and initial PD credit = 'h4
3:0	RW	1111b	**Upstream PH Header Queues Size, and the Initial PH Credit** 0011: 8-level PH header queue, and initial PH credit = 'h8 0010: 4-level PH header queue, and initial PH credit = 'h4 0001: 2-level PH header queue, and initial PH credit = 'h2 0000: 1-level PH header queue, and initial PH credit = ’h1

Offset Address: A6h (D3F0)
Credit Advertisement Control **Default Value: 7Fh**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6:4	RW	111b	**Upstream Read CPL Header Size** 111: 256QW 32-level 110: 224QW 28-level 101: 192QW 24-level 100: 160QW 20-level 011: 128QW 16-level 010: 96QW 12-level 001: 64QW 8-level 000: 32QW 4-level
3:0	RW	1111b	**Upstream Non-Posted Request Queue Size, and Initial NPH Credit Value** 0011: 8-level NPH header queue, and initial NPH credit = 'h8 0010: 4-level NPH header queue, and initial NPH credit = 'h4 0001: 2-level NPH header queue, and initial NPH credit = 'h2 0000: 1-level NPH header queue, and initial NPH credit = ’h1

Offset Address: A7h (D3F0)
Upstream Performance Control **Default Value: 04h**

Bit	Attribute	Default	Description
7	RW	0	**Transaction layer patch MSI cycle low address is masked bug register. The value of Revision Code bit 7 (RX08[7]) in this root port should be the same as this register.** 0: Transaction layer mask low address[4:2] for both MSI and other P2C cycles. 1: Transaction layer does not mask low address[4:2] for both MSI and other P2C cycles.
6	RO	0	**Reserved**
5	RW	0	**Transaction Layer Header Queue Pre-Load Design Dynamic Clock Enable for Power Management** 1: Turn on the transaction layer header queue pre-load design dynamic clock enable. 0: Otherwise
4	RW	0	**Upstream Read FIFO Entry Release Timing** 0: Upstream read FIFO entry release when the last data pop into retry data FIFO. 1: Upstream read FIFO entry release when the first data pop into retry data FIFO. x16/x8 design is recommended to set 1 for better performance.
3	RW	0	**Downstream Read Data Wait for Previous Upstream Write Complete** 0: Disable 1: Enable
2	RW	1b	**Upstream Requests Read and Write Orders** 0: Upstream requests are served in order 1: Upstream write always pass upstream read
1	RW	0	**Upstream Read Data TLP Return Policy** 0: One upstream request with over 16DW length or non-8-QW boundary alignment must be splitted into multiple CPL TLPs. 1: Multiple CPL TLPs belong to the same upstream request can be merged into one single CPL TLP
0	RW	0	**Upstream Write Cycle Will Be 4QW Align** 0: Disable 1: Enable

Offset Address: AF-A8h (D3F0) – Reserved

PCI Express Data Link Layer Registers (B0-B6h)

Offset Address: B0h (D3F0)

Ack / Nak Latency Timer Limit **Default Value: 3Bh**

Bit	Attribute	Default	Description
7:0	RW	3Bh	**Timer Limit for Ack/Nak Latency Timer and Update FC Latency Timer (in unit of 250MHz)** 00: 4 x 1 Clocks 01: 4 x 2 Clocks 02: 4 x 3 Clocks. 0n: 4 x (n+1) Clocks FF: 4 x 256 Clocks.

Offset Address: B1h (D3F0)

Replay Timer Limit **Default Value: 59h**

Bit	Attribute	Default	Description
7:0	RW	59h	**Replay Timer Limit (In unit of 250MHz)** 00: 8 x 1 Clocks 01: 8 x 2 Clocks 02: 8 x 3 Clocks 0n: 8 x (n+1) Clocks FF: 8 x 256 Clocks.

Offset Address: B2h (D3F0)

FCU Control and Status **Default Value: 40h**

Bit	Attribute	Default	Description
7	RW1C	0	**FCI/FCU Timeout Status** 1 means the FCI/FCU timeout has occurred
6	RW	1b	**FCI/FCU Receive Timer Enable Control** 0: Disable the timeout mechanism 1: Enable the timeout mechanism
5	RW	0	**FCI/FCU Receive Timer Limit** 0: Timeout limit of 200us 1: Timeout limit of 300us
4	RW	0	**FCI/FCU Receive Timer Reset Control** 0: Timer reset by FCI/FCU only 1: Timer reset by any received DLLPs
3:1	RO	0	**Reserved**
0	RW	0	**Guard bit for DL and TL to reset upstream related logic when retrain is going on**

Offset Address: B3h (D3F0)
Replay Timer Control **Default Value: 81h**

Bit	Attribute	Default	Description
7:6	RW	10b	**Replay Timer Control While Rewind** Resend those DLLPs which do not have corresponding ACK/NAK received. 00: Hold Replay Timer during rewind. 01: During rewind, if ACK/NAK comes in, reset and hold the Replay Timer 10: During rewind, reset and hold the Replay Timer as long as the Retry Buffer is empty 11: Reserved.
5:3	RO	0	**Reserved**
2:0	RW	001b	**Count of Replay Timer Expired During RXL0s** (Receiving Physical in L0s state) Before Resend the TLP This bit work with Rx50[7] to define the time for repeat the replay. When Rx50[7] is set to 0: 000: Wait forever for the Acknowledge from the device side 001: Resend the TLP after 1 x Replay timer expired 010: Resend the TLP after 2 x Replay timer expired 011: Resend the TLP after 4 x Replay timer expired 100: Resend the TLP after 8 x Replay timer expired 101: Resend the TLP after 16 x Replay timer expired 110: Resend the TLP after 32 x Replay timer expired 111: Resend the TLP after 64 x Replay timer expired When Rx50[7] is set to 1: 000: Wait forever for the Acknowledge from the device side 001: Resend the TLP after 16 x Replay timer expired 010: Resend the TLP after 32 x Replay timer expired 011: Resend the TLP after 64 x Replay timer expired 100: Resend the TLP after 128 x Replay timer expired 101: Resend the TLP after 256 x Replay timer expired 110: Resend the TLP after 512 x Replay timer expired 111: Resend the TLP after 1024 x Replay timer expired

Offset Address: B4h (D3F0)
Arbitration Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3	RW	0	**TLP vs. Flow Control Initialization for VC0 in Arbitration Priority** 0: TLP is not allowed to pass FCI2 for VC0 1: TLP is allowed to pass FCI2 for VC0
2:0	RW	000b	**Data Link TX Packets Arbitration Scheme** 000: Strict priority: NAK or timeout ACK > TLP > FCU > pending ACK 001: Reserved. 010: Strict priority: TLP > NAK or timeout / pending ACK > FCU 011: Strict priority: TLP > FCU > NAK or timeout / pending ACK 100: Strict priority: NAK or timeout / pending ACK > TLP > FCU 101: Strict priority: NAK or timeout / pending ACK > FCU > TLP 110: Strict priority: FCU > TLP > NAK or timeout / pending ACK 111: Strict priority: FCU > NAK or timeout ACK > TLP > pending ACK

Offset Address: B5h (D3F0)

FCU Control **Default Value: 10h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6	RW	0	**FCU Timer Control** 0: Update flow control credit when either Transaction Layer requested packets being sent or when FCU timer expired 1: Update flow control credit only when FCU timer expired
5:4	RW	01b	**ACK DLLP Collapse Method** 00: Send ACK when the latency timer RxB0 expired. 01: Send ACK every 4 correct TLP has been received 10: Send ACK every 8 correct TLP has been received 11: Send ACK every 16 correct TLP has been received
3:2	RO	0	**Reserved**
1	RW	0	**FCI Process End Condition** 0: Complete FCI process when TLP/FCU has been received 1: Do not complete FCI process even when TLP/FCU has been received
0	RW	0	**VC1 FCI DLLP Transmission Scheme** 0: Transmit FCI DLLP only when FCI timer expired 1: Transmit FCI DLLP continuously as long as the FCI process is not finished

Offset Address: B6h (D3F0)

Transaction / Link Layer Checking Control **Default Value: 01h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4	RW	0	**Phyls Deskew Buffer Power Management**
3:1	RO	0	**Reserved**
0	RW	1b	**LCRC Checking Control** 0: Do not check LCRC 1: Check LCRC

Offset Address: BF-B7h (D3F0) – Reserved

PCI Express Physical Layer Registers (C0-C7h)

Offset Address: C3-C0h (D3F0)

PHYLS General Control **Default Value: 0007 0003h**

Bit	Attribute	Default	Description
31:24	RO	0	**PHYLS_STATE Mapping** See the mapping table.
23:21	RO	0	**Reserved**
20	RW	0	**Bypass PHYES Receiver Detect Function** 0: Derived from PHYES 1: Bypass Receiver Detect
19	RW	0	**State Machine LTSSM Exit POLLING_ACTIVE** 0: LTSSM may exit POLLING_ACTIVE when receiving 8 TS after sending more than 1024 TS 1: LTSSM always waits for 24 ms timeout to exit POLLING_ACTIVE.
18	RW	1b	**Scheme to Enter L1/L23 Entry** 0: Wait IDLE ordered set to enter L1/L23 entry 1: Wait electrical idle and ignore IDLE ordered set to enter L1/L23
17	RW	1b	**Running Disparity Check** 0: Disable 1: Enable
16	RW	1b	**State machine LTSSM enter Detect.Active from Detect.Quiet** 0: Wait for the Electrical idle signal from the PHYES or 12ms after RESET# becomes inactive 1: Always wait for 12ms after the RESET# becomes inactive
15:14	RW	00	**Auto/Manual Configuration** 00: Auto negotiation Others: Reserved
13	RO	0	**Reserved**
12:8	RW	00000b	**PHY Lane Configuration Setting** 11111: x1 with normal connection for Root Port 1 PE0 10101: force into L0S state, for testing measurement used only 11000: force into DETECT_QUIET state, for testing measurement used only 11001: force into DETECT_ACTIVE state, for testing measurement used only 00000: Use PHY negotiation Other values are not allowed.
7	RW	0	**Quick Timeout Counter Setting** When set to 1, following timeout counters will be shorter: TIMEOUT_2MS → TIMEOUT_4US TIMEOUT_12MS → TIMEOUT_24US TIMEOUT_24MS → TIMEOUT_48US TIMEOUT_48MS → TIMEOUT_96US TIMEOUT_1024TS → TIMEOUT_32TS Receiver Detection: 15x1024ns → 1x1024ns
6	RW	0	**Disable Data Scrambling / Descrambling** 0: Enable 1: Disable
5:3	RW	000b	**Loopback Mode Selection (Applies to All 16 Lanes)** 000: No loopback 001: PHYLS loopback from TX end to RX end 010: PHYES loopback from TX end to RX end 011: External loopback from TX end to RX end 100: Reserved 101: PHYLS loopback from RX end to TX end 110: PHYES loopback from RX end to TX end 111: Reserved
2:0	RW	011b	**COMMA Detection Window** 000, 001: Illegal values Others: Delay number of T to determine correct lane-to-lane deskew value

Note:
RxC3-C0[15:14] Programming Sequence:
1. Program Dev3Func0 Rx50[4] = 1, must be programmed first
3. Program Dev3Func0 RxC1[7:6] to the desired configuration
5. Program Dev3Func0 Rx50[4] = 0, must be programmed last)

Offset Address: C7-C4h (D3F0)

Elastic Buffer Base Registers for Lane 0 - 3 **Default Value: 0000 4444h**

Bit	Attribute	Default	Description
31:15	RO	0	**Reserved**
14:12	RW	100b	**Elastic Buffer Base Register for Lane 3** 0, 1, 7: Illegal values Others: Delay numbers of T for elastic buffer operations
11	RO	0	**Reserved**
10:8	RW	100b	**Elastic Buffer Base Register for Lane 2** 0, 1, 7: Illegal values Others: Delay numbers of T for elastic buffer operations
7	RO	0	**Reserved**
6:4	RW	100b	**Elastic Buffer Base Register for Lane 1** 0, 1, 7: Illegal values Others: Delay numbers of T for elastic buffer operations
3	RO	0	**Reserved**
2:0	RW	100b	**Elastic Buffer Base Register for Lane 0** 0, 1, 7: Illegal values Others: Delay numbers of T for elastic buffer operations

Offset Address: CF-CBh (D3F0) – Reserved

PCI Express Power Management Module Registers (D0-D3h)

Offset Address: D3-D0h (D3F0)

PMC Control **Default Value: 0000 2050h**

Bit	Attribute	Default	Description
31:24	RW	00h	**Idle Period to Enter ASL1** Minimum time period is 128ns 00: 128ns 01: 2x128ns 02: 3x128ns … FF: 256x128ns
23:16	RW	00h	**Idle Period to Enter L0s** Minimum time period is 128ns 00: 128ns 01: 2x128ns 02: 3x128ns … FF: 256x128ns
15	W1C	0	**Error Status Report** This bit is set when device cannot have electrical idle after the waiting period programmed at RxD1[6:4] expired.
14	RO	0	**Reserved**
13:12	RW	10b	**Electrical Idle Waiting Period before Move to L1 State (after issue ACK to the L1 request from the device).** 00: Always wait for electrical idle 01: Wait 32 clock 10: Wait 64 clock 11: Reserved
11:10	RO	0	**Reserved**
9:8	RW	00b	**Downstream Cycles Triggered C2P Cycles, Period of Staying at L0 Before Returned to L1 for PHY (when PMU is in non-D0 state)** 00: immediately 01: 1 cfgW or message + delay10T 10: 1 32QW +1cfgW or message+ delay10T 11: 2 32QW +1 cfgW or message +delay10T
7	RO	0	**Reserved**
6:4	RW	101b	**Timerout timer for waiting for the acknowledge from the device when issued PME_TURNOFF message to notice the device to go into power down mode.** 000: 1us 001: 2us 010: 4us 011: 8us 100: 16us 101: 32us 110: 64us 111: 128us
3	RW	0	**Stop Port Clock When No Device On This Port** 0: Disable 1: Enable
2	RW	0	**Enable Link Retrain When Bad DLLP Is Checked** 0: Disable 1: Enable
1	RW	0	**Link Loopback** 0: Normal operation 1: Direct device to enter Loopback mode, receiving data in the device will be sent to the transmit side
0	RW	0	**Link Reconfigure Link Width** Link width reconfiguration is initiated by writing 1 to this bit. This will direct the Physical Layer LTSSM to the Recovery state first, and then to the Configuration state. 0: When reconfigure link width, LTSSM must be in Detect state 1: When reconfigure link width, LTSSM can be in Configuration state

Offset Address: D4h (D3F0)

PHYES Module Overall Control – Applied to x16 and x4 PHYES **Default Value: 02h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6	RW	0	**Control FCI Receive Timer (300us)** 0: Disable the timeout mechanism 1: Enable the timeout mechanism
5:2	RO	0	**Reserved**
1	RW	1b	**Lane Reversal** 0: Do not support lane reversal Link / Lane number will be sent only on lane0~(maxlinkwidth-1). 1: Support lane reversal. Link / Lane number will be sent on lane0 ~(maxlinkwidth-1), (16-maxlinkwidth)~ 15.
0	RW	0	**Un-negotiated Lanes State during Configuration.Complete** 0: During Configuration. Complete, un-negotiated lanes will be electrical idle. 1: During Configuration. Complete, Link/Lane number will be pad for un-negotiated lanes

Offset Address: D7-D5h (D2F0) – Reserved

Offset Address: D8h (D3F0)

PMC Express Message Status **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW1C	0	**Excessive Errors Occurred But Not Reported in The MSGC** 0: Normal operation. 1: There are errors not reported to the system
6:0	RO	0	**Reserved**

Offset Address: DF-D9h (D3F0) – Reserved

PCI Express Electrical PHY Registers (E0-E4h)

Offset Address: E0h (D3F0)

PHYES Module Overall Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Enable New PLL_LOCK Scheme to Monitor Any Abnormal Jitter** 0: Disabled 1: Enabled
6:0	RO	0	**Reserved**

Offset Address: E1h (D3F0)

PHYES Module Related Control **Default Value: 0Bh**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4	RW	0	**Receiving Polarity Change Control** 0: Have the same polarity on the loop-back/received data 1: Have reverse polarity on the loop-back/received data
3:2	RW	10b	**Squelch Window Select (64~175mv)**
1	RW	1b	**Electrical Idle Signal De-Assert Condition** 0: Electrical idle signal will be de-asserted at once and remained at least 4ns when electrical idle exit condition is detected. 1: Electrical idle signal will be de-asserted at once and remained at least 16ns when electrical idle exit condition is detected.
0	RW	1b	**Electrical Idle Signal Assert Condition** 0: Electrical idle signal is asserted only when electrical idle condition is detected and remained at least 16ns. 1: Electrical idle signal is asserted at once when the electrical idle condition is detected.

Offset Address: E2h (D3F0)

PHYES Module Control – Rx/Tx 1 **Default Value: 01h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6	RW	0	**Mobile Swing** 0: Disable 1: Enable
5	RW	0	**PHYES Clock Buffer Power Down on Lane 0-3** 0: All enable 1: Power down
4	RW	0	**Lane 2-3 Clock Buffer Power Down** 0: All enable 1: Power down
3:2	RW	00b	**Receiver Input Rise Delay (duty cycle adjustment for the 4 lanes)** 00: 0 ps 01: 4 ps 10: 15 ps 11: 50 ps
1:0	RW	01b	**Receiver Input Fall Delay (duty cycle adjustment for the 4 lanes)** 00: 0 ps 01: 7 ps 10: 24 ps 11: 55 ps

Offset Address: E3h (D3F0)

PHYES Module Control – Rx/Tx 2 **Default Value: 9Ah**

Bit	Attribute	Default	Description
7	RW	1b	**PCIe Pads Driving Control** 0: Autocomp 1: Manual setting through bits [2:0] and RxE2[2:0]
6:5	RW	00b	**Filter Depth Valid Only When CDR Type is set to 0** 00: Filter depth = 2 01: Filter depth = 3 10: Filter depth = 5 11: Filter depth = 7
4	RW	1b	**CDR Type** 0: 1/N type 1: Pseudo 6X scheme
3	RW	1b	**CDR Filter Depth** The bit is only valid when RxE3[4] = 1 0: Filter depth = 6 1: Filter depth = 8
2:0	RW	010b	**Lane 0 –3 Termination Resistance Selection** Resistance Range: 62Ω (000b) ~ 43Ω (111b) Default: 50Ω (010b)

Offset Address: E4h (D3F0)

PHYES Module Control – Rx/Tx 3 **Default Value: 88h**

Bit	Attribute	Default	Description
7:4	RW	8h	**Pre/De-Emphasis Level Selection**
3:0	RW	8h	**Driver Current Source Selection**

Offset Address: EF-E5h (D3F0) – Reserved

PCI Express Electrical PHY Test Registers (F0-F7h)

Offset Address: F3-F0h (D3F0)

PHY Test **Default Value: 0600 0000h**

Bit	Attribute	Default	Description
31	RW	0	**Electrical PHY Test Mode Enable** Program this bit to 1 to start Electrical PHY test
30:28	RO	0	**Reserved**
27:24	RW	0110b	**Test Pattern Check Length** Number of T when the receiving side starts to check transmitted and received patterns Suggested Value Settings: (Lane 0 for example) RxC0[5:3] = 01: RxC4[2:0] + 2 RxC0[5:3] = 10, 11: RxC4[2:0] + 2 + (loopback path latency / 4ns) + 1
23:20	RW	0000b	**Select Test Pattern** 0000: SKP Order-Set 0001: User define, use RxF7-F4[25:16] 0010: K28.5 test bit sequence 0011: K28.7 test bit sequence 0100: K test for differential pair current 0101: J test for differential pair current 0110: D21.5 test bit sequence 0111: D30.3 test bit sequence 1000: Ten contiguous run of 3 test bit sequence 1001: Low transition density test bit sequence 1010: Half-rate/quarter-rate test bit sequence 1011: Low frequency spectral test bit sequence 1100: Simultaneous switching test bit sequence 1101: Reserved 1110: Reserved 1111: Reserved
19:18	RO	0	**Reserved**
17:16	RW	00b	**Select Lane for Loop Back Test** 00: Loop back test on lane 0 01: Loop back test n lane 1 10: Loop back test lane 2 11: Loop back test n lane 3
15:8	RW	0	**Repeated Count of the Test Pattern** (as selected in RxF2[7:4]) 00~0Bh: Illegal value 0Ch: Test pattern repeats 12 times 0Dh: Test pattern repeats 13 times … FFh: Test pattern repeats 255 times
7:0	RO	0	**Reserved**

Offset Address: F7-F4h (D3F0)

PHY Test Symbol **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RO	0	**Electrical PHY Test Error** 1: An error occurred in loop back test mode receiving side
30	RO	0	**Electrical PHY Built-In Self Test Error of Symbol Comparison** That same errors happen or COMMA symbols are never detected during PHYBIST period; reported from PTNCMP
29:26	RO	0	**Reserved**
25:16	RO	0	**Transmitted Symbol when RxF3[7] is set to 1** 00 when RxF3[7] is 0
15:10	RO	0	**Reserved**
9:0	RO	0	**Received Symbol when RxF3[7] is set to 1** 00 when RxF3[7] is 0

Offset Address: F9-F8h (D3F0)

Electrical PHY Test Error Counter During PHYBIST Period **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RO	0	**Electrical PHY Test Error Counter During PHYBIST Period**

Offset Address: FF-FAh (D3F0) – Reserved

Device 3 Function 0 (D3F0) – PCI Express Root Port 1 Extended Space

Registers defined in the Extended Space can be accessed through PCI Express Enhanced Configuration Access Mechanism, which utilizes a flat memory-mapped address space to access the configuration registers. Please check PCI Express Specification for the detail information.

Advanced Error Reporting Capability (100-137h)

Offset Address: 103-100h (D3F0)

Advanced Error Reporting Enhanced Capability Header **Default Value: 1401 0001h**

Bit	Attribute	Default	Description
31:20	RO	140h	**Next Capability Offset**
19:16	RO	1h	**Capability Version**
15:0	RO	0001h	**PCI Express Extended Capability ID**

Offset Address: 107-104h (D3F0)

Uncorrectable Error Status **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:21	RO	0	**Reserved**
20	RW1C	0	**Unsupported Request Error Status (TL)**
19	RW1CS	0	**ECRC Error Status (TL)**
18	RW1CS	0	**Malformed TLP Status (TL)**
17	RW1CS	0	**Receiver Overflow Status (TL)**
16	RW1CS	0	**Unexpected Completion Status (TL)**
15	RW1CS	0	**Completer Abort Status (TL)**
14	RW1CS	0	**Completion Timeout Status (TL)**
13	RW1CS	0	**Flow Control Protocol Error Status (TL)**
12	RW1CS	0	**Poisoned TLP Status (TL)**
11:6	RO	0	**Reserved**
5	RW1CS	0	**Surprise Down Error Status**
4	RW1CS	0	**Data Link Protocol Error Status (DLL)**
3:1	RO	0	**Reserved**
0	RW1CS	0	**Training Error Status (PHY)**

Offset Address: 10B-108h (D3F0)

Uncorrectable Error Mask **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:21	RO	0	**Reserved**
20	RWS	0	**Unsupported Request Error Mask (TL)**
19	RWS	0	**ECRC Error Mask (TL)**
18	RWS	0	**Malformed TLP Mask (TL)**
17	RWS	0	**Receiver Overflow Mask (TL)**
16	RWS	0	**Unexpected Completion Mask (TL)**
15	RWS	0	**Completed Abort Mask (TL)**
14	RWS	0	**Completion Timeout Mask (TL)**
13	RWS	0	**Flow Control Protocol Error Mask (TL)**
12	RWS	0	**Poisoned TLP Mask (TL)**
11:6	RO	0	**Reserved**
5	RWS	0	**Surprise Down Error Mask**
4	RWS	0	**Data Link Protocol Error Mask (DLL)**
3:1	RO	0	**Reserved**
0	RWS	0	**Training Error Mask (PHY)**

Offset Address: 10F-10Ch (D3F0)
Uncorrectable Error Severity **Default Value: 0006 0031h**

Bit	Attribute	Default	Description
31:21	RO	0	Reserved
20	RWS	0	Unsupported Request Error Severity (TL)
19	RWS	0	ECRC Error Severity (TL)
18	RWS	1b	Malformed TLP Severity (TL)
17	RWS	1b	Receiver Overflow Error Severity (TL)
16	RWS	0	Unexpected Completion Error Severity (TL)
15	RWS	0	Completed Abort Error Severity (TL)
14	RWS	0	Completion Timeout Error Severity (TL)
13	RWS	1b	Flow Control Protocol Error Severity (TL)
12	RWS	0	Poisoned TLP Severity (TL)
11:6	RO	0	Reserved
5	RWS	1b	Surprise Down Error Severity
4	RWS	1b	Data Link Protocol Error Severity (DLL)
3:1	RO	0	Reserved
0	RWS	1b	Training Error Severity (PHY)

Offset Address: 113-110h (D3F0)
Correctable Error Status **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:14	RO	0	Reserved
13	RW1CS	0	Advisory Non-Fatal Error Status
12	RW1CS	0	Replay Timer Timeout Status (DLL)
11:9	RO	0	Reserved
8	RW1CS	0	REPLAY_NUM Rollover Status (DLL)
7	RW1CS	0	Bad DLLP Status (DLL)
6	RW1CS	0	Bad TLP Status (DLL)
5:1	RO	0	Reserved
0	RW1CS	0	Receiver Error Status (PHY)

Offset Address: 117-114h (D3F0)
Correctable Error Mask **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:14	RO	0	Reserved
13	RWS	0	Advisory Non-Fatal Error Mask
12	RWS	0	Replay Timer Timeout Mask (DLL)
11:9	RO	0	Reserved
8	RWS	0	REPLAY_NUM Rollover Mask (DLL)
7	RWS	0	Bad DLLP Mask (DLL)
6	RWS	0	Bad TLP Mask (DLL)
5:1	RO	0	Reserved
0	RWS	0	Receiver Error Mask (PHY)

Offset Address: 11B-118h (D3F0)
Advanced Error Capabilities and Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:9	RO	0	Reserved
8	RWS	0	ECRC Check Enable (TL)
7	RO	0	ECRC Check Capable (TL)
6	RWS	0	ECRC Generation Enable (TL)
5	RO	0	ECRC Generation Capable (TL)
4:0	ROS	0	First Error Pointer (TL)

Offset Address: 11F-11Ch (D3F0)
Header Log (TL) 1 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	ROS	0	**Header Log Register 1st DW**

Offset Address: 123-120Ch (D3F0)
Header Log (TL) 2 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	ROS	0	**Header Log Register 2nd DW**

Offset Address: 127-124h (D3F0)
Header Log (TL) 3 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	ROS	0	**Header Log Register 3rd DW**

Offset Address: 12B-128h (D3F0)
Header Log (TL) 4 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	ROS	0	**Header Log Register 4th DW**

Offset Address: 12F-12Ch (D3F0)
Root Error Command **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:3	RO	0	**Reserved**
2	RW	0	**Fatal Error Reporting Enable**
1	RW	0	**Non-Fatal Error Reporting Enable**
0	RW	0	**Correctable Error Reporting Enable**

Offset Address: 133-130h (D3F0)
Root Error Status **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:27	RO	0	**Advanced Error Interrupt Message Number (TL)**
26:7	RO	0	**Reserved**
6	RW1CS	0	**Fatal Error Messages Received (TL)**
5	RW1CS	0	**Non-Fatal Error Messages Received (TL)**
4	RW1CS	0	**First Uncorrectable Fatal Error Message Received (TL)** Set to 1 when the first Uncorrectable Error Message received is for a Fatal Error
3	RW1CS	0	**Multiple ERR_FATAL/NONFATAL Received (TL)**
2	RW1CS	0	**ERR_FATAL/NONFATAL Received (TL)**
1	RW1CS	0	**Multiple ERR_COR Received (TL)**
0	RW1CS	0	**ERR_COR Received (TL)**

Offset Address: 137-134h (D3F0)
Error Source Identification **Default Value: 0000 0000h**

This register is updated regardless of the settings of Root Control register and the Root Error Command register.

Bit	Attribute	Default	Description
31:16	ROS	0	**ERR_FATAL / NONFATAL Source Identification (TL)**
15:0	ROS	0	**ERR_COR Source Identification (TL)**

Offset Address: 13B-138h (D3F0)
Error Source Identification **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	ROS	0	**Error DLLP log register**

Offset Address: 13C-13Fh (D3F0) – Reserved

Virtual Channel Capability (140-14Fh)

Virtual Channel Capability is defined for Egress direction of the device. For Root Port, since only VC0 is defined (VC0 mapping: TC0, TC1, TC2, TC3, TC4, TC5, TC6, TC7), there is no implementation of VC Arbitration Table and Port Arbitration Table.

Offset Address: 143-140h (D3F0)
Virtual Channel Enhanced Capability **Default Value: 1801 0002h**

Bit	Attribute	Default	Description
31:20	RO	180h	**Next Capability Offset**
19:16	RO	1h	**Capability Version**
15:0	RO	0002h	**PCI Express Extended Capability ID**

Offset Address: 147-144h (D3F0)
Port VC Capability 1 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:12	RO	0	**Reserved**
11:10	RO	0	**Port Arbitration Table Entry Size** Reserved for root port
9:8	RO	0	**Reference Clock** Reserved for root port
7	RO	0	**Reserved**
6:4	RO	0	**Low Priority Extended VC Count**
3	RO	0	**Reserved**
2:0	RO	0	**Extended VC Count**

Offset Address: 14B-148h (D3F0)
Port VC Capability 2 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RO	0	**VC Arbitration Table Offset** 00 since only VC0 is defined
23:8	RO	0	**Reserved**
7:0	RO	0	**VC Arbitration Capability**

Offset Address: 14D-14Ch (D3F0)
Port VC Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15:4	RO	0	**Reserved**
3:1	RW	0	**VC Arbitration Select** Reserved
0	RO	0	**Load VC Arbitration Table** Reserved

Offset Address: 14F-14Eh (D3F0)
Port VC Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15:1	RO	0	**Reserved**
0	RO	0	**VC Arbitration Table Status** Reserved

VC0 Resource (150-15Bh)

Offset Address: 150-153h (D3F0)
VC Resource Capability (VC0) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RO	0	**Port Arbitration Table Offset (VC0)** Reserved for root port
23	RO	0	**Reserved**
22:16	RO	0	**Maximum Time Slots (TL)**
15	RO	0	**Reject Snoop Transactions**
14	RO	0	**Advanced Packet Switching** Reserved
13:8	RO	0	**Reserved**
7:0	RO	0	**Port Arbitration Capability** Reserved for root port

Offset Address: 157-154h (D3F0)
VC Resource Control (VC0) **Default Value: 8000 00FFh**

Bit	Attribute	Default	Description
31	RO	1b	**VC Enable**
30:27	RO	0	**Reserved**
26:24	RO	0	**VC ID**
23:20	RO	0	**Reserved**
19:17	RW	0	**Port Arbitration Select** Reserved for root port
16	RO	0	**Load Port Arbitration Table** Reserved for root port
15:8	RO	0	**Reserved**
7:0	RW Bit 0: RO	FFh	**TC/VC Mapping** This field indicates the TCs that are mapped to VC0. If bit [n] is 1, the corresponding traffic class TCn is mapped to VC0 (0 <= n <= 7). Default is TC0, TC1, TC2, TC3, C4, TC5, TC6 and TC7 are all mapped to VC0. Note: Bit0 is hardwired to 1 (i.e. TC0 is always mapped to VC0).

Offset Address: 15B-158h (D3F0)
VC Resource Status (VC0) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:18	RO	0	**Reserved**
17	RO	0	**VC Negotiation Pending (TL)**
16	RO	0	**Port Arbitration Table Status** Reserved for root port
15:0	RO	0	**Reserved**

VC1 Resource (15C-167h)

The following registers exist only when Rx144[0] is programmed to 1. If Rx144[0]=0, all the following content will be read as 0.

Offset Address: 15F-15Ch (D3F0)

VC Resource Capability (VC1) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RO	0	**Port Arbitration Table Offset (VC1)** Reserved for root port
23	RO	0	**Reserved**
22:16	RO	0	**Maximum Time Slots (TL)**
15	RO	0	**Reject Snoop Transactions**
14	RO	0	**Advanced Packet Switching** Reserved for root port
13:8	RO	0	**Reserved**
7:0	RO	0	**Port Arbitration Capability** Reserved for root port

Offset Address: 163-160h (D3F0)

VC Resource Control (VC1) **Default Value: 0100 0000h**

Bit	Attribute	Default	Description
31	RW	0	**VC Enable**
30:27	RO	0	**Reserved**
26:24	RW	1b	**VC ID**
23:20	RO	0	**Reserved**
19:17	RW	0	**Port Arbitration Select** Reserved for root port
16	WO	0	**Load Port Arbitration Table** Reserved for root port
15:8	RO	0	**Reserved**
7:0	RW Bit 0: RO	0	**TC/VC Mapping** This field indicates the TCs that are mapped to VC1. If bit [n] is 1, the corresponding traffic class TCn is mapped to VC1 (0 <= n <= 7). Default is TC0, TC1, TC2, TC3, C4, TC5, TC6 and TC7 are all mapped to VC0. Note: Bit0 is hardwired to 0 (i.e. TC0 is always mapped to VC0).

Offset Address: 167-164h (D3F0)

VC Resource Status (VC1) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:18	RO	0	**Reserved**
17	RO	0	**VC Negotiation Pending (TL)**
16	RO	0	**Port Arbitration Table Status** Reserved for root port
15:0	RO	0	**Reserved**

Offset Address: 17F-168h (D3F0) – Reserved

Root Complex Topology Capability List Registers (180-19Bh)

Offset Address: 183-180h (D3F0)

Root Complex Link Declaration Capabilities Header **Default Value: 0001 0005h**

Bit	Attribute	Default	Description
31:20	RO	0	**Next Capability**
19:16	RO	1h	**Capability Version**
15:0	RO	0005h	**Capability ID**

Offset Address: 187-184h (D3F0)

Element Self Description Register **Default Value: 0201 0100h**

Bit	Attribute	Default	Description
31:24	RO	02h	**Port Number (Root Port 0)**
23:16	RO	01h	**Component ID**
15:8	RO	01h	**Number of Link Entries**
7:4	RO	0	**Reserved**
3:0	RO	0h	**Element Type** 00: Configuration Space Element 01: System egress port or internal sink 10: Internal Root Complex Link

Offset Address: 193-190h (D3F0)

Upstream Link Descriptor Register **Default Value: 0001 0001h**

Bit	Attribute	Default	Description
31:24	RO	0	**Target Port Number** Indicate the port number of RCRB-H
23:16	RO	01h	**Target Component ID**
15:2	RO	0	**Root Complex Link Declaration Capability**
1	RO	0	**Link Type** Indicates that the link points to RCRB-H
0	RO	1b	**Link Valid**

Offset Address: 19B-194h (D3F0)

Upstream Link Base Address Register **Default Value: 0000 0000 0000 0000h**

Bit	Attribute	Default	Description
63:32	RO	0	**Base Address Upper.**
31:0	RO	0	**Base Address Lower**

Note: Base Address Register value for RCRB-H [63:12]

Offset Address: 19F-19Ch (D2F0) – Reserved

PCIe Root Complex Register Block for Host

Virtual Channel Capability (000-00Fh)

Offset Address: 003-000h (RCRB-H)

Virtual Channel Enhanced Capability Header — **Default Value: 0401 0002h**

Bit	Attribute	Default	Description
31:20	RO	040h	**Next Capability Offset**
19:16	RO	1h	**Capability Version**
15:0	RO	0002h	**PCI Express Extended Capability ID**

Offset Address: 007-004h (RCRB-H)

Port VC Capability 1 — **Default Value: 0000 0801h**

Bit	Attribute	Default	Description
31:12	RO	0	**Reserved**
11:10	RO	10b	**Port Arbitration Table Entry Size** The upstream arbitration unit of this chip supports up to 6 ports. 10b indicates the size of port arbitration table entry is 4 bits.
9:8	RO	0	**Reference Clock** Reserved.
7	RO	0	**Reserved**
6:4	RO	0	**Low Priority Extended VC Count**
3	RO	0	**Reserved**
2:0	RO	001b	**Extended VC Count**

Offset Address: 00B-008h (RCRB-H)

Port VC Capability 2 — **Default Value: 0000 0001h**

Bit	Attribute	Default	Description
31:24	RO	00h	**VC Arbitration Table** 00: Table is not present.
23:8	RO	0	**Reserved**
7:0	RO	01h	**VC Arbitration Capability**

Offset Address: 00D-00Ch (RCRB-H)

Port VC Control — **Default Value: 0000h**

Bit	Attribute	Default	Description
15:4	RO	0	**Reserved**
3:1	RW	0	**VC Arbitration Select**
0	RO	0	**Load VC Arbitration Table** Reserved

Offset Address: 00F-00Eh (RCRB-H)

Port VC Status — **Default Value: 0000h**

Bit	Attribute	Default	Description
15:1	RO	0	**Reserved**
0	RO	0	**VC Arbitration Table Status** Reserved

VC0 Resource (010-01Bh)

Offset Address: 013-010h (RCRB-H)

VC Resource Capability (VC0) **Default Value: 0000 0001h**

Bit	Attribute	Default	Description
31:24	RO	0	**Port Arbitration Table (VC0)** Reserved
23	RO	0	**Reserved**
22:16	RO	0	**Maximum Time Slots (TL)** Reserved
15	RO	0	**Reject Snoop Transactions** Reserved
14	RO	0	**Advanced Packet Switching** Reserved
13:8	RO	0	**Reserved**
7:0	RO	01h	**Port Arbitration Capability** T_WRR 128 phase

Offset Address: 017-014h (RCRB-H)

VC Resource Control (VC0) **Default Value: 8000 00FFh**

Bit	Attribute	Default	Description
31	RO	1b	**VC Enable**
30:27	RO	0	**Reserved**
26:24	RO	0	**VC ID**
23:20	RO	0	**Reserved**
19:17	RO	0	**Port Arbitration Select** Reserved
16	RO	0	**Load Port Arbitration Table** Reserved
15:8	RO	0	**Reserved**
7:0	RW Bit 0: RO	FFh	**TC/VC Mapping** This field indicates the TCs that are mapped to VC0. If bit [n] is 1, the corresponding traffic class TCn is mapped to VC0 (0 <= n <= 7). Default is TC0, TC1, TC2, TC3, C4, TC5, TC6 and TC7 are all mapped to VC0. Note: Bit0 is hardwired to 1 (i.e. TC0 is always mapped to VC0).

Offset Address: 01B-018h (RCRB-H)

VC Resource Status (VC0) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:18	RO	0	**Reserved**
17	RO	0	**VC Negotiation Pending (TL)**
16	RO	0	**Port Arbitration Table Status** Reserved
15:0	RO	0	**Reserved**

VC1 Resource (01C-027h)

Rx01C-027h registers exist only when Rx004[0] = 1.

Offset Address: 01F-01Ch (RCRB-H)

VC Resource Capability (VC1) **Default Value: 1000 0010h**

Bit	Attribute	Default	Description
31:24	RO	10h	**Port Arbitration Table Offset (VCN)**
23	RO	0	**Reserved**
22:16	RW	0	**Maximum Time Slots (TL)**
15	RW	0	**Reject Snoop Transactions**
14	RO	0	**Advanced Packet Switching** Reserved
13:8	RO	0	**Reserved**
7:0	RO	10h	**Port Arbitration Capability**

Offset Address: 023-020h (RCRB-H)

VC Resource Control (VC1) **Default Value: 0100 0000h**

Bit	Attribute	Default	Description
31	RO	0	**VC Enable**
30:27	RO	0	**Reserved**
26:24	RO	1h	**VC ID**
23:17	RO	0	**Reserved**
16	RO	0	**Load Port Arbitration Table**
15:8	RO	0	**Reserved**
7:0	RO	0	**TC/VC Mapping** This field indicates the TCs that are mapped to VC1. If bit [n] is 1, the corresponding traffic class TCn is mapped to VC1 (0 <= n <= 7). Default is TC0, TC1, TC2, TC3, C4, TC5, TC6 and TC7 are all mapped to VC0. Note: Bit 0 is hardwired to 0 (i.e. TC0 is always mapped to VC0).

Offset Address: 027-024h (RCRB-H)

VC Resource Status (VC1) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:18	RO	0	**Reserved**
17	RO	0	**VC Negotiation Pending (TL)**
16	RO	0	**Port Arbitration Table Status**
15:0	RO	0	**Reserved**

Root Complex Link Declaration Enhanced Capability (040-04Fh)

Offset Address: 043-040h (RCRB-H)

Root Complex Link Declaration Capabilities Header **Default Value: 0001 0005h**

Bit	Attribute	Default	Description
31:20	RO	0	**Next Capability**
19:16	RO	1h	**Capability Version**
15:0	RO	0005h	**PCI Express Extended Capability ID**

Offset Address: 047-044h (RCRB-H)
Element Self Description **Default Value: 0001 0601h**

Bit	Attribute	Default	Description
31:24	RO	0	**Port Number** 0: Egress port
23:16	RO	01h	**Component ID**
15:8	RO	06h	**Number of Link Entries** 6 Links
7:4	RO	0	**Reserved**
3:0	RO	1h	**Element Type** 0h: Configuration space element 1h: System egress port or internal sink 2h: Internal Root Complex Link

Offset Address: 04F-048h (RCRB-H) – Reserved

Link Entry for PEG (050-05Fh)

Offset Address: 053-050h (RCRB-H)
PEG Link Description **Default Value: 0101 0003h**

Bit	Attribute	Default	Description
31:24	RO	01h	**Target Port Number**
23:16	RO	01h	**Target Component ID**
15:2	RO	0	**Reserved**
1	RO	1b	**Link Type** Link points to PEG.
0	RO	1b	**Link Valid**

Offset Address: 057-054h (RCRB-H) – Reserved

Offset Address: 05F-058h (RCRB-H)
Root Port Graphic Base Address **Default Value: 0000 0000 0001 0000h**

Bit	Attribute	Default	Description
63:28	RO	0	**Reserved**
27:20	RO	0	**Bus Number**
19:15	RO	02h	**Device Number**
14:12	RO	0	**Function Number**
11:0	RO	0	**Reserved**

Link Entry for PE0 (060-06Fh)

Offset Address: 060-063h (RCRB-H)
PE0 Link Description **Default Value: 0201 0003h**

Bit	Attribute	Default	Description
31:24	RO	02h	**Target Port Number**
23:16	RO	01h	**Target Component ID**
15:2	RO	0	**Reserved**
1	RO	1b	**Link Type** Link points to PE0.
0	RO	1b	**Link Valid**

Offset Address: 067-064h (RCRB-H) – Reserved

Offset Address: 06F-068h (RCRB-H)

PE0 Base Address **Default Value: 0000 0000 0001 8000h**

Bit	Attribute	Default	Description
63:28	RO	0	**Reserved**
27:20	RO	0	**Bus Number**
19:15	RO	03h	**Device Number**
14:12	RO	0	**Function Number**
11:0	RO	0	**Reserved**

Offset Address: 09F-070h (RCRB-H) – Reserved

Link Entry for RCRB-V (0A0-0AFh)

Offset Address: 0A3-0A0h (RCRB-H)

Link Description **Default Value: 0601 0001h**

Bit	Attribute	Default	Description
31:24	RO	06h	**Target Port Number**
23:16	RO	01h	**Target Component ID**
15:2	RO	0	**Reserved**
1	RO	0	**Link Type** Link points to RCRB-V.
0	RO	1b	**Link Valid**

Offset Address: 0A7-0A4h (RCRB-H) – Reserved

Offset Address: 0AF-0A8h (RCRB-H)

RCRB-V Base Address **Default Value: 0000 0000 0000 0000h**

Bit	Attribute	Default	Description
63:32	RO	0	**Base Address Upper**
31:0	RO	0	**Base Address Lower**

Virtual Channel Port Arbitration Table for VCN (100h-13F)

Offset Address: 103-100h (RCRB-H)

VCN Port Arbitration Table 1 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:28	RW	0	**Phase 7** 0: Idle or others 1: PEG 2: PE0 3: PE1 4: PE2 5: PE3 6: V-Link 7: AGP
27:24	RW	0	**Phase 6**
23:20	RW	0	**Phase 5**
19:16	RW	0	**Phase 4**
15:12	RW	0	**Phase 3**
11:8	RW	0	**Phase 2**
7:4	RW	0	**Phase 1**
3:0	RW	0	**Phase 0**

Offset Address: 107-104h (RCRB-H)
VCN Port Arbitration Table 2 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:28	RW	0	**Phase 15**
27:24	RW	0	**Phase 14**
23:20	RW	0	**Phase 13**
19:16	RW	0	**Phase 12**
15:12	RW	0	**Phase 11**
11:8	RW	0	**Phase 10**
7:4	RW	0	**Phase 9**
3:0	RW	0	**Phase 8**

Offset Address: 10B-108h (RCRB-H)
VCN Port Arbitration Table 3 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:28	RW	0	**Phase 23**
27:24	RW	0	**Phase 22**
23:20	RW	0	**Phase 21**
19:16	RW	0	**Phase 20**
15:12	RW	0	**Phase 19**
11:8	RW	0	**Phase 18**
7:4	RW	0	**Phase 17**
3:0	RW	0	**Phase 16**

Offset Address: 10F-10Ch (RCRB-H)
VCN Port Arbitration Table 4 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:28	RW	0	**Phase 31**
27:24	RW	0	**Phase 30**
23:20	RW	0	**Phase 29**
19:16	RW	0	**Phase 28**
15:12	RW	0	**Phase 27**
11:8	RW	0	**Phase 26**
7:4	RW	0	**Phase 25**
3:0	RW	0	**Phase 24**

Offset Address: 113-110h (RCRB-H)
VCN Port Arbitration Table 5 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:28	RW	0	**Phase 39**
27:24	RW	0	**Phase 38**
23:20	RW	0	**Phase 37**
19:16	RW	0	**Phase 36**
15:12	RW	0	**Phase 35**
11:8	RW	0	**Phase 34**
7:4	RW	0	**Phase 33**
3:0	RW	0	**Phase 32**

Offset Address: 117-114h (RCRB-H)
VCN Port Arbitration Table 6 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:28	RW	0	**Phase 47**
27:24	RW	0	**Phase 46**
23:20	RW	0	**Phase 45**
19:16	RW	0	**Phase 44**
15:12	RW	0	**Phase 43**
11:8	RW	0	**Phase 42**
7:4	RW	0	**Phase 41**
3:0	RW	0	**Phase 40**

Offset Address: 11B-118h (RCRB-H)
VCN Port Arbitration Table 7 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:28	RW	0	**Phase 55**
27:24	RW	0	**Phase 54**
23:20	RW	0	**Phase 53**
19:16	RW	0	**Phase 52**
15:12	RW	0	**Phase 51**
11:8	RW	0	**Phase 50**
7:4	RW	0	**Phase 49**
3:0	RW	0	**Phase 48**

Offset Address: 11F-11Ch (RCRB-H)
VCN Port Arbitration Table 8 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:28	RW	0	**Phase 63**
27:24	RW	0	**Phase 62**
23:20	RW	0	**Phase 61**
19:16	RW	0	**Phase 60**
15:12	RW	0	**Phase 59**
11:8	RW	0	**Phase 58**
7:4	RW	0	**Phase 57**
3:0	RW	0	**Phase 56**

Offset Address: 123-120h (RCRB-H)
VCN Port Arbitration Table 9 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:28	RW	0	**Phase 71**
27:24	RW	0	**Phase 70**
23:20	RW	0	**Phase 69**
19:16	RW	0	**Phase 68**
15:12	RW	0	**Phase 67**
11:8	RW	0	**Phase 66**
7:4	RW	0	**Phase 65**
3:0	RW	0	**Phase 64**

Offset Address: 127-124h (RCRB-H)
VCN Port Arbitration Table 10 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:28	RW	0	**Phase 79**
27:24	RW	0	**Phase 78**
23:20	RW	0	**Phase 77**
19:16	RW	0	**Phase 76**
15:12	RW	0	**Phase 75**
11:8	RW	0	**Phase 74**
7:4	RW	0	**Phase 73**
3:0	RW	0	**Phase 72**

Offset Address: 12B-128h (RCRB-H)
VCN Port Arbitration Table 11 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:28	RW	0	**Phase 87**
27:24	RW	0	**Phase 86**
23:20	RW	0	**Phase 85**
19:16	RW	0	**Phase 84**
15:12	RW	0	**Phase 83**
11:8	RW	0	**Phase 82**
7:4	RW	0	**Phase 81**
3:0	RW	0	**Phase 80**

Offset Address: 12F-12Ch (RCRB-H)
VCN Port Arbitration Table 12 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:28	RW	0	**Phase 95**
27:24	RW	0	**Phase 94**
23:20	RW	0	**Phase 93**
19:16	RW	0	**Phase 92**
15:12	RW	0	**Phase 91**
11:8	RW	0	**Phase 90**
7:4	RW	0	**Phase 89**
3:0	RW	0	**Phase 88**

Offset Address: 133-130h (RCRB-H)
VCN Port Arbitration Table 13 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:28	RW	0	**Phase 103**
27:24	RW	0	**Phase 102**
23:20	RW	0	**Phase 101**
19:16	RW	0	**Phase 100**
15:12	RW	0	**Phase 99**
11:8	RW	0	**Phase 98**
7:4	RW	0	**Phase 97**
3:0	RW	0	**Phase 96**

Offset Address: 137-134h (RCRB-H)
VCN Port Arbitration Table 14 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:28	RW	0	**Phase 111**
27:24	RW	0	**Phase 110**
23:20	RW	0	**Phase 109**
19:16	RW	0	**Phase 108**
15:12	RW	0	**Phase 107**
11:8	RW	0	**Phase 106**
7:4	RW	0	**Phase 105**
3:0	RW	0	**Phase 104**

Offset Address: 13B-138h (RCRB-H)

VCN Port Arbitration Table 15 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:28	RW	0	**Phase 119**
27:24	RW	0	**Phase 118**
23:20	RW	0	**Phase 117**
19:16	RW	0	**Phase 116**
15:12	RW	0	**Phase 115**
11:8	RW	0	**Phase 114**
7:4	RW	0	**Phase 113**
3:0	RW	0	**Phase 112**

Offset Address: 13F-13Ch (RCRB-H)

VCN Port Arbitration Table 16 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:28	RW	0	**Phase 127**
27:24	RW	0	**Phase 126**
23:20	RW	0	**Phase 125**
19:16	RW	0	**Phase 124**
15:12	RW	0	**Phase 123**
11:8	RW	0	**Phase 122**
7:4	RW	0	**Phase 121**
3:0	RW	0	**Phase 120**

VC Arbitration Timer (200-20Fh)

PCI Express arbitration scheme is based on the same scheme used in the DRAM Controller. A timer named as Occupancy Timer is used to guarantee the number of time slots one requester will be granted when there is no high priority requesters come in. Another timer named as Promote Timer is used for a requester to upgrade its requests to high priority if it is not served after the Promote Timer times out. However, priority request promoted by the expiration of the Promote Timer will be served once only.

Offset Address: 200h (RCRB-H)

VC0 Occupancy Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3:0	RW	0h	**VC0 Occupancy Timer (in unit of 125MHz)** 0000: Timer is off (Arbitration will be based on a fairly RR scheme) 0nh: n x 4 T, where 1< n <= 15

Offset Address: 201h (RCRB-H)

VC0 Promote Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3:0	RW	0h	**VC0 Promote Timer** (in unit of 125MHz) 0000: Timer is off 0nh: n x 4 T, where 1< n <= 15

Offset Address: 202h (RCRB-H)

VC1 Occupancy Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3:0	RW	0h	**VC1 Occupancy Timer** (in unit of 125MHz) 0000: Timer is off (Arbitration will be based on a fairly RR scheme) 0nh: n x 4 T, where 1< n <= 15

Offset Address: 203h (RCRB-H)

VC1 Promote Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3:0	RW	0h	**VC1 Promote Timer** (in unit of 125MHz) 0000: Timer is off 0nh: n x 4 T, where 1< n <= 15

Note: Port arbitration timers defined by registers 202h and 203h are not applicable in current VC1 implementation; currently the VC1 arbitration is in strict priority.

Offset Address: 20F-204h (RCRB-H) – Reserved

Port Arbitration Timer for VC0 (210-219h)

Offset Address: 210h (RCRB-H)

PEG Occupancy Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3:0	RW	0h	**Occupancy Timer** (in unit of 125MHz) 0000: Timer is off (Arbitration will be based on a fairly RR scheme) 0nh: n x 4 T, where 1< n <= 15

Offset Address: 211h (RCRB-H)

PEG Promote Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3:0	RW	0h	**Promote Timer (in unit of 125MHz)** 0000: Timer is off 0nh: n x 4 T, where 1< n <= 15

Offset Address: 212h (RCRB-H)

PE0 Occupancy Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3:0	RW	0h	**Occupancy Timer** (in unit of 125MHz) 0000: Timer is off (Arbitration will be based on a fairly RR scheme) 0nh: n x 4 T, where 1< n <= 15

Offset Address: 213h (RCRB-H)

PE0 Promote Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3:0	RW	0h	**Promote Timer** (in unit of 125MHz) 0000: Timer is off 0nh: n x 4 T, where 1< n <= 15

Offset Address: 229-214h (RCRB-H) – Reserved

Host Side Upstream Arbitration Timers (230-23Fh)

A fair arbitration timer is designed for the upstream traffic, which provides a fair arbitration between PCI express devices and other devices like AGP, PCI2 master, I/O APIC and V-Link. The arbitration scheme also used the one currently implemented in the DRAMC.

Offset Address: 230h (RCRB-H)

PCIe – VC0 Occupancy Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3:0	RW	0h	**Occupancy Timer (in unit of host frequency)** 0000: Timer is off (Arbitration will be based on a fairly RR scheme) 0nh: n x 4 T, where 1< n <= 15

Offset Address: 231h (RCRB-H)

PCIe – VC0 Promote Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3:0	RW	0h	**Promote Timer (in unit of host frequency)** 0000: Timer is off 0nh: n x 4 T, where 1< n <= 15

Offset Address: 232h (RCRB-H)

PCIe – VC1 Occupancy Timer **Default Value: 80h**

Bit	Attribute	Default	Description
7	RW	1b	**PCIe - VC1 Strict Priority** 0: Disable 1: Enable
6:4	RO	0	**Reserved**
3:0	RW	0h	**Occupancy Timer (in unit of host frequency)** 0000: Timer is off (Arbitration will be based on a fairly RR scheme) 0nh: n x 4 T, where 1< n <= 15

Offset Address: 233h (RCRB-H)

PCIe-VC1 Promote Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3:0	RW	0h	**Promote Timer (in unit of host frequency)** 0000: Timer is off 0nh: n x 4 T, where 1< n <= 15

Offset Address: 234h (RCRB-H)

V-Link Arbitration Timer Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Strict Priority to GPCI or NVC (PMADS) Request** 0: Disable 1: Enable
6	RW	0	**High Priority to GPCI or NVC (with PMSIO) Request** 0: Disable 1: Enable
5:4	RO	0	**Reserved**
3:0	RW	0h	**Occupancy Timer (in unit of host frequency)** 0000: Timer is off (Arbitration will be based on a fairly RR scheme) 0nh: n x 4 T, where 1< n <= 15

Offset Address: 235h (RCRB-H)
V-Link Promote Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3:0	RW	0h	**Promote Timer (in unit of host frequency)** 0000: Timer is off 0nh: n x 4 T, where 1< n <= 15

Offset Address: 236h (RCRB-H)
V-Link – VC1 Arbitration Timer Control **Default Value: 80h**

Bit	Attribute	Default	Description
7	RW	1b	**Strict Priority to V-Link – VC1** 0: Disable 1: Enable
6:4	RO	0	**Reserved**
3:0	RW	0h	**Occupancy Timer (in unit of host frequency)** 0000: Timer is off (Arbitration will be based on a fairly RR scheme) 0nh: n x 4 T, where 1< n <= 15

Offset Address: 237h (RCRB-H)
V-Link – VC1 Promote Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3:0	RW	0h	**Promote Timer (in unit of host frequency)** 0000: Timer is off 0nh: n x 4 T, where 1< n <= 15

Offset Address: 238h (RCRB-H)
AGP Arbitration Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Strict Priority to GADS from AGPC** 0: Disable 1: Enable
6	RW	0	**High Priority to GADS with GISOCH Asserted** 0: Disable 1: Enable
5:4	RO	0	**Reserved**
3:0	RW	0h	**Occupancy Timer (in unit of host frequency)** 0000: Timer is off (Arbitration will be based on a fairly RR scheme) 0nh: n x 4 T, where 1< n <= 15

Offset Address: 239h (RCRB-H)
AGP Promote Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3:0	RW	0h	**Promote Timer (in unit of host frequency)** 0000: Timer is off 0nh: n x 4 T, where 1< n <= 15

Offset Address: 23Ah (RCRB-H)
PCI2 / NVC Occupancy Timers **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved**
5:4	RW	00b	**NVC Occupancy Timer (in unit of host frequency)** 00: Timer is off (i.e. 1T Round Robin scheme) 01: 4T 10: 8T 11: 16T
3:2	RO	0	**Reserved**
1:0	RW	00b	**PCI2 Occupancy Timer (in unit of host frequency)** 00: Timer is off (i.e. 1T Round Robin scheme) 01: 4T 10: 8T 11: 16T

Offset Address: 23Bh (RCRB-H)
PCI2 / NVC Promote Timers **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved**
5:4	RW	00b	**NVC Promote Timer (in unit of host frequency)** 00: Timer is off 01: 4T 10: 8T 11: 16T
3:2	RO	0	**Reserved**
1:0	RW	00b	**PCI2 Promote Timer (in unit of host frequency)** 00: Timer is off (i.e. 1T Round Robin scheme) 01: 4T 10: 8T 11: 16T

Offset Address: 23Ch (RCRB-H)
IO APIC Occupancy Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3:0	RW	0h	**Occupancy Timer (in unit of host frequency)** 0000: Timer is off (Arbitration will be based on a fairly RR scheme) 0nh: n x 4 T, where 1< n <= 15

Offset Address: 23Dh (RCRB-H)
IO APIC Promote Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3:0	RW	0h	**Promote Timer (in unit of host frequency)** 0000: Timer is off (Arbitration will be based on a fairly RR scheme) 0nh: n x 4 T, where 1< n <= 15

Offset Address: 23F-23Eh (RCRB-H) - Reserved

DRAM Side Upstream Arbitration Timers (240-245h)

This fair arbitration timer is for upstream traffic to do a fair arbitration between all of the VC1 PCI Express devices and AGP.

Offset Address: 240h (RCRB-H)

PCIe-VC1 Arbitration Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Strict Priority to VC1** 0: Disable 1: Enable
6:4	RO	0	**Reserved**
3:0	RW	0h	**Occupancy Timer (in unit of DRAMC frequency)** 0000: Timer is off (Arbitration will be based on a fairly RR scheme) 0nh: n x 4 T, where 1< n <= 15

Offset Address: 241h (RCRB-H)

PCIe-VC1 Promote Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3:0	RW	0h	**Promote Timer (in unit of DRAMC frequency)** 0000: Timer is off 0nh: n x 4 T, where 1< n <= 15

Offset Address: 243-242h (RCRB-H) – Reserved

Offset Address: 244h (RCRB-H)

AGP Occupancy Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3:0	RW	0h	**Occupancy Timer (in unit of DRAMC frequency)** 0000: Timer is off (Arbitration will be based on a fairly RR scheme) 0nh: n x 4 T, where 1< n <= 15

Offset Address: 245h (RCRB-H)

AGP Promote Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3:0	RW	0h	**Promote Timer (in unit of DRAMC frequency)** 0000: Timer is off 0nh: n x 4 T, where 1< n <= 15

PCIe Root Complex Register Block for V-Link

Virtual Channel Capability (000-00Fh)

Offset Address: 003-000h (RCRB-V)

Virtual Channel Enhanced Capability Header — **Default Value: 0401 0002h**

Bit	Attribute	Default	Description
31:20	RO	040h	**Next Capability Offset**
19:16	RO	1h	**Capability Version**
15:0	RO	0002h	**PCI Express Extended Capability ID**

Offset Address: 007-004h (RCRB-V)

Port VC Capability 1 — **Default Value: 0000 0001h**

Bit	Attribute	Default	Description
31:12	RO	0	**Reserved**
11:10	RO	0	**Port Arbitration Table Entry Size** Reserved
9:8	RO	0	**Reference Clock** Reserved for RCRB-V
7	RO	0	**Reserved**
6:4	RO	0	**Low Priority Extended VC Count** LPVC=0
3	RO	0	**Reserved**
2:0	RO	001b	**Extended VC Count**

Offset Address: 00B-008h (RCRB-V)

Port VC Capability 2 — **Default Value: 0000 0001h**

Bit	Attribute	Default	Description
31:24	RO	0	**VC Arbitration Table Offset** Reserved
23:8	RO	0	**Reserved**
7:0	RO	01h	**VC Arbitration Capability**

Offset Address: 00D-00Ch (RCRB-V)

Port VC Control — **Default Value: 0000h**

Bit	Attribute	Default	Description
15:4	RO	0	**Reserved**
3:1	RW	000b	**VC Arbitration Select**
0	RO	0	**Load VC Arbitration Table** Reserved

Offset Address: 00F-00Eh (RCRB-V)

Port VC Status — **Default Value: 0000h**

Bit	Attribute	Default	Description
15:1	RO	0	**Reserved**
0	RO	0	**VC Arbitration Table Status** Reserved

VC0 Resource (010-01Bh)

Offset Address: 013-010h (RCRB-V)

VC Resource Capability (VC0) **Default Value: 0000 0001h**

Bit	Attribute	Default	Description
31:24	RO	0	**Port Arbitration Table Offset (VC0)** Reserved
23	RO	0	**Reserved**
22:16	RO	0	**Maximum Time Slots (TL)** Reserved
15	RO	0	**Reject Snoop Transactions**
14	RO	0	**Advanced Packet Switching** Reserved
13:8	RO	0	**Reserved**
7:0	RO	01h	**Port Arbitration Capability** Non-configurable hardware fixed arbitration support

Offset Address: 017-014h (RCRB-V)

VC Resource Control (VC0) **Default Value: 8000 00FFh**

Bit	Attribute	Default	Description
31	RO	1b	**VC Enable**
30:27	RO	0	**Reserved**
26:24	RO	0	**VC ID**
23:20	RO	0	**Reserved**
19:17	RW	000b	**Port Arbitration Select**
16	RO	0	**Load Port Arbitration Table** Reserved
15:8	RO	0	**Reserved**
7:0	RW Bit 0: RO	FFh	**TC/VC Mapping** This field indicates the TCs that are mapped to VC0. If bit [n] is 1, the corresponding traffic class TCn is mapped to VC0 (0 <= n <= 7). Default is TC0, TC1, TC2, TC3, C4, TC5, TC6 and TC7 are all mapped to VC0. Note: Bit0 is hardwired to 1 (i.e. TC0 is always mapped to VC0).

Offset Address: 01B-018h (RCRB-V)

VC Resource Status (VC0) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:18	RO	0	**Reserved**
17	RO	0	**VC Negotiation Pending (TL)**
16	RO	0	**Port Arbitration Table Status** Reserved
15:0	RO	0	**Reserved**

VC1 Resource (01C-027h)

The Rx01C - Rx027 registers will exist only when Rx004[0] is programmed to 1.

Offset Address: 01F-01Ch (RCRB-V)

VC Resource Capability (VC1) **Default Value: 0000 0001h**

Bit	Attribute	Default	Description
31:24	RO	00h	**Port Arbitration Table Offset (VC1)** Reserved 00h: NULL
23	RO	0	**Reserved**
22:16	RO	0	**Maximum Time Slots (TL)** Reserved
15	RO	0	**Reject Snoop Transactions**
14	RO	0	**Advanced Packet Switching** Reserved
13:8	RO	0	**Reserved**
7:0	RO	01h	**Port Arbitration Capability**

Offset Address: 023-020h (RCRB-V)

VC Resource Control (VC1) **Default Value: 0100 0000h**

Bit	Attribute	Default	Description
31	RO	0	**VC Enable**
30:27	RO	0	**Reserved**
26:24	RO	1h	**VC ID**
23:17	RO	0	**Reserved**
16	RO	0	**Load Port Arbitration Table** Reserved
15:8	RO	0	**Reserved**
7:0	RO	0	**TC/VC Mapping** This field indicates the TCs that are mapped to VC1. If bit [n] is 1, the corresponding traffic class TCn is mapped to VC1 (0 <= n <= 7). Default is TC0, TC1, TC2, TC3, C4, TC5, TC6 and TC7 are all mapped to VC0. Note: Bit 0 is hardwired to 0 (i.e. TC0 is always mapped to VC0).

Offset Address: 027-024h (RCRB-V)

VC Resource Status (VC1) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:18	RO	0	**Reserved**
17	RO	0	**VC Negotiation Pending (TL)**
16	RO	0	**Port Arbitration Table Status** Reserved for RCRB-V
15:0	RO	0	**Reserved**

Root Complex Link Enhanced Capability (040-0AFh)

Offset Address: 043-040h (RCRB-V)

Root Complex Link Declaration Capabilities Header **Default Value: 0801 0005h**

Bit	Attribute	Default	Description
31:20	RO	080h	**Next Capability Offset**
19:16	RO	1h	**Capability Version**
15:0	RO	0005h	**PCI Express Extended Capability ID**

Offset Address: 047-044h (RCRB-V)

Element Self Description **Default Value: 0601 0202h**

Bit	Attribute	Default	Description
31:24	RO	06h	**Port Number** Port number = 6
23:16	RO	01h	**Component ID**
15:8	RO	02h	**Number of Link Entries** 2 Link
7:4	RO	0	**Reserved**
3:0	RO	2h	**Element Type** 0h: Configuration Space Element 1h: System egress port or internal sink 2h: Internal Root Complex Link

Offset Address: 04F-048h (RCRB-V) – Reserved

Link Entry 1 (050-05Fh)

Offset Address: 053-050h (RCRB-V)

Link Description **Default Value: 0001 0001h**

Bit	Attribute	Default	Description
31:24	RO	0	**Target Port Number**
23:16	RO	01h	**Target Component ID**
15:2	RO	0	**Reserved**
1	RO	0	**Link Type** Type 0 is for RCRB-H.
0	RO	1b	**Link Valid**

Offset Address: 057-054h (RCRB-V) – Reserved

Offset Address: 05F-058h (RCRB-V)

Link Address **Default Value: 0000 0000 0000 0000h**

Bit	Attribute	Default	Description
63:32	RO	0	**Link Address Bits 63:32**
31:0	RO	0	**Link Address Bits 31:0**

Link Entry 2 (060-06Fh)

Offset Address: 063-060h (RCRB-V)

Link Description **Default Value: 0002 0001h**

Bit	Attribute	Default	Description
31:24	RO	0	**Target Port Number** Port 0
23:16	RO	02h	**Target Component ID**
15:2	RO	0	**Reserved**
1	RO	0	**Link Type** Type 0 = RCRB DMI
0	RO	1b	**Link Valid**

Offset Address: 067-064h (RCRB-V) – Reserved

Offset Address: 06F-068h (RCRB-V)

Link Address **Default Value: 0000 0000 0000 0000h**

Bit	Attribute	Default	Description
63:32	RO	0	**Link Address Bits 63:32**
31:0	RO	0	**Link Address Bits 31:0**

Root Complex Internal Link Control Enhanced Capability Header (080-08Bh)

Offset Address: 083-080h (RCRB-V)

Root Complex Link Declaration Enhanced Capability Header **Default Value: 0001 0006h**

Bit	Attribute	Default	Description
31:20	RO	0	**Next Capability Offset**
19:16	RO	1h	**Capability Version**
15:0	RO	0006h	**PCI Express Extended Capability ID**

Offset Address: 087-084h (RCRB-V)

Root Complex Link Capabilities **Default Value: 0000 2421h**

Bit	Attribute	Default	Description
31:18	RO	0	**Reserved**
17:15	RO	0	**L1 Exit Latency**
14:12	RO	010b	**L0s Exit Latency** 010: 128ns to 256ns
11:10	RO	01b	**Active State Link PM Support** L0s and L1 Supported
9:4	RO	02h	**Maximum Link Width** X2
3:0	RO	1h	**Maximum Link Speed** 2.5Gb/s

Offset Address: 089-088h (RCRB-V)

Root Complex Link Control **Default Value: 0000h**

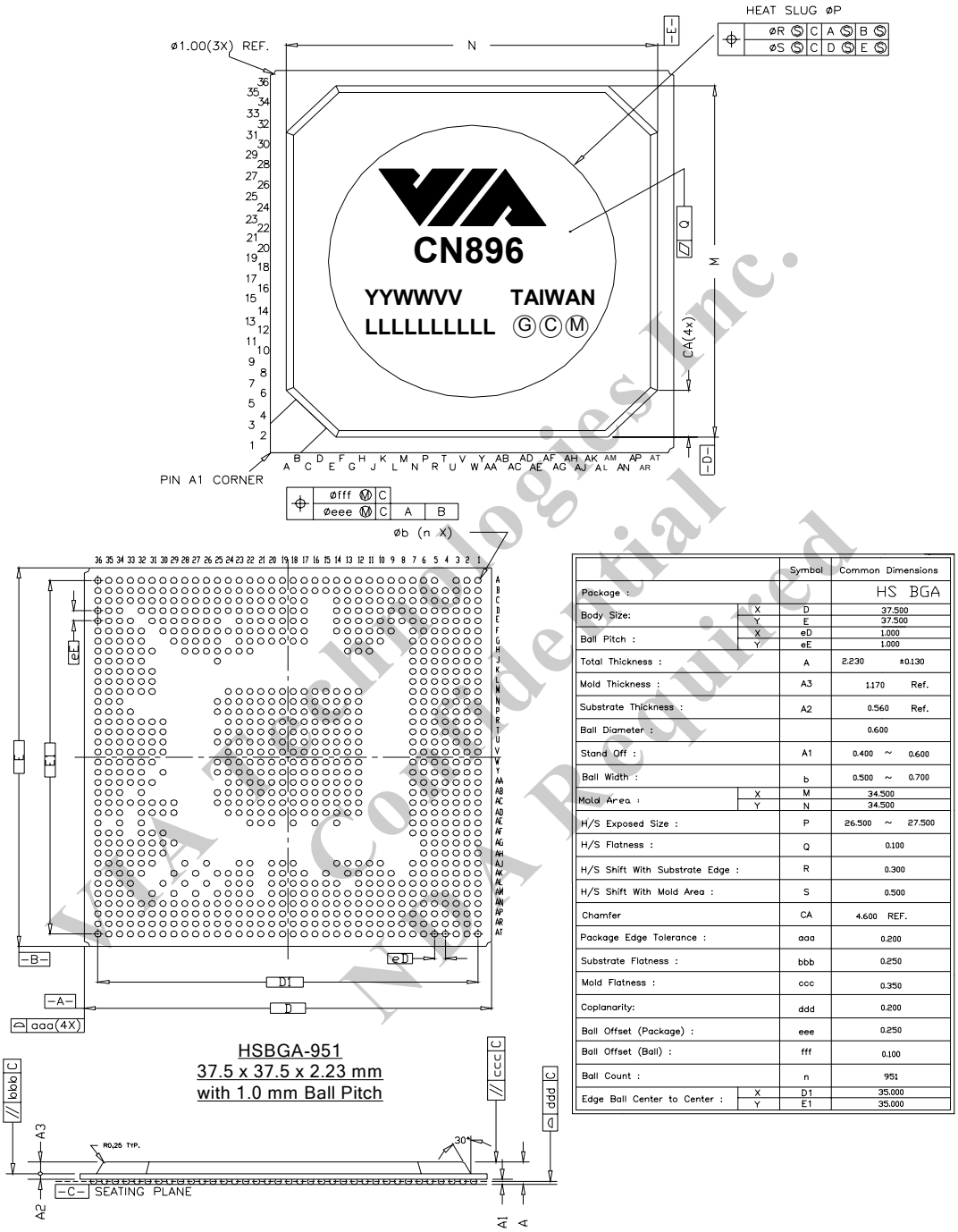
Bit	Attribute	Default	Description
15:8	RO	0	**Reserved**
7	RW	0	**Extended Sync**
6:2	RO	0	**Reserved**
1:0	RW	0	**Active State Link PM Control**

Offset Address: 08B-08Ah (RCRB-V)

Root Complex Link Status **Default Value: 0021h**

Bit	Attribute	Default	Description
15:10	RO	0	**Reserved**
9:4	RO	02h	**Negotiated Link Width** X2
3:0	RO	1h	**Link Speed** 2.5Gb/s

MECHANICAL SPECIFICATIONS



		Symbol	Common Dimensions
Package :			HS BGA
Body Size:	X	D	37.500
	Y	E	37.500
Ball Pitch :	X	eD	1.000
	Y	eE	1.000
Total Thickness :		A	2.230 ±0.130
Mold Thickness :		A3	1.170 Ref.
Substrate Thickness :		A2	0.560 Ref.
Ball Diameter :			0.600
Stand Off :		A1	0.400 ~ 0.600
Ball Width :		b	0.500 ~ 0.700
Mold Area :	X	M	34.500
	Y	N	34.500
H/S Exposed Size :		P	26.500 ~ 27.500
H/S Flatness :		Q	0.100
H/S Shift With Substrate Edge :		R	0.300
H/S Shift With Mold Area :		S	0.500
Chamfer		CA	4.600 REF.
Package Edge Tolerance :		aaa	0.200
Substrate Flatness :		bbb	0.250
Mold Flatness :		ccc	0.350
Coplanarity:		ddd	0.200
Ball Offset (Package) :		eee	0.250
Ball Offset (Ball) :		fff	0.100
Ball Count :		n	951
Edge Ball Center to Center :	X	D1	35.000
	Y	E1	35.000

Figure 4. Lead-Free Mechanical Specifications - HSBGA-951 Ball Grid Array Package with Heat Spreader