Data Sheet

VX800 Series

All-in-One
System Processor

Preliminary Revision 1.25
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VIA TECHNOLOGIES, INC.

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REVISION HISTORY

Document Release	Date	Revision	Initials
1.0	8/27/08	Initial public release	SY
1.1	11/3/08	Added Timing Duration of GPI Pins for SCI/SMI Driven and S3/S4 Wakeup	LW
1.2	12/26/08	Updated Electrical Specifications	LW
1.21	1/12/09	Updated legal page Updated CPU Support in Product Features Updated Electrical characteristics of Clock in Electrical Specifications section Added CBE[3:0]#, GPI1, IRSCLK and SPIDO in Electrical Specifications section Added Total Green Package in Mechnical Specifications section	LW
1.22	1/23/09	Modified T05 in Power On Sequence and Reset Signal Timing in Electrical Specifications section Removed Display Clock In/Out Table in Electrical Specifications section	LW
1.23	2/19/09	Added CRPWREN# in ball lists and its description in Signal Descriptions section Updated the control registers of GPI8	LW
1.24	4/21/09	Updated pin description of PCIRST[1:0]# Added strapping timing under Electrical Specifications section	LW
1.25	6/1/09	Updated integrated LVDS transmitter under the feature section Modified pin description of NAP# Modified S3 timing in Figure 17 Modified package in the Mechanical Specification section	LW

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DOCUMENT INTRODUCTION

This document includes specifications of VX800 Series. Please refer to Table 1 for the specification differences of VX800 and VX800UT products.

Table 1. VX800 Series Feature Comparison Table

Product Model	VX800UT	VX800
FSB Speed (MHz)	533 - 400	800 - 400
Integrated GFX Clock (MHz)	200	250
Memory Type	DDR2 533	DDR2 667
Snapshot Memory	Yes	Yes
PCI Express Ports	3 x 1-lane	1 x 4-lane + 2 x 1-lane
PCI	Yes	Yes
SATA	Yes	Yes
Core Voltage	1.25V	1.5V

VX800 SERIES

ALL-IN-ONE SYSTEM PROCESSOR

800 / 533 / 400 MHz FSB VIA C7 / C7-M / Eden / Nano Processor
DDR2 667 / 533 / 400 SDRAM Controller
Integrated Chrome9 HC3 DX9 3D / 2D Graphics & Video Processor
Unified Video Decoding Accelerator
Three PCI Express Ports
Integrated LVDS Transmitter
Two Serial ATA Ports, Six USB 2.0 / 1.1 Ports
One UltraDMA-133 EIDE Channel
SD / MS / MS Pro / MMC Memory Card Controller, SDIO Ports
PCI 32-bit 33MHz Bus, High Definition Audio Controller
UART Ports, IR, SPI, RTC, LPC and SMBus
ACPI and Sophisticated Power Management

PRODUCT FEATURES

- **Process Technology and Package**
  - ***VX800:*** 0.15um, 1.5V core voltage
  - ***VX800UT:*** 0.15um, 1.25V core voltage
  - 33 x 33mm FCBGA package (Flip Chip Ball Grid Array) with 1236 balls and 0.8 mm ball pitch
- **CPU Interface**
  - ***VX800:*** Supports 800 / 533 / 400 MHz FSB VIA C7 / C7-M / Eden / Nano processor
  - ***VX800UT:*** Supports 533 / 400 MHz FSB VIA C7 / C7-M / Nano processor
- **Memory Sub-system**
  - ***VX800:*** Supports DDR2 667 / 533 / 400 MHz SDRAM
  - ***VX800UT:*** Supports DDR2 533 / 400 MHz SDRAM
  - ***VX800UT:*** Supports FSB / DDR2 synchronous mode only
  - Channel-A (Shared System and Graphics memory)
    - Supports 64 / 32-bit data width
    - Supports 64Mb / 128Mb / 256Mb / 512Mb / 1Gb / 2Gb (x8 / x16 / x32)
    - Supports CL 2 / 3 / 4 / 5
    - Supports 2 unbuffered or register double-sided DIMMs
  - Channel-C (SnapShot memory)
    - Supports 16-bit data width
    - Supports 64Mb / 128Mb / 256Mb / 512Mb (x8 / x16)
    - Supports CL 2 / 3 / 4 / 5

- **Advanced High Bandwidth PCI Express Interface**
  - PCI Express 1.1 support
  - Supports three PCI Express ports

    VX800:
    - 1st port: 4-lane port for graphics or high bandwidth peripheral device
      - Configurable lane width, either 4 or 1.
    - 2nd / 3rd port: 1-lane port for peripheral devices

    VX800UT:
    - Three 1-lane ports for peripheral device
  - Supports interconnect power management
  - Supports polarity inversion
  - Supports Hot Plug
  - Loop-back testing mode for easy debugging mode for PCI Express
- **Chrome9 HC3 Integrated Graphics Processor with 2D / 3D / Video Controllers**
  - Optimized Unified Memory Architecture (UMA)
  - Supports 32 / 64 /128 / 256 MB frame buffers size
  - ***VX800:*** Graphics engine clocks up to 250 MHz decoupled from memory clock
    VX800UT: Graphics engine clocks up to 200 MHz decoupled from memory clock
  - PCI v2.3 Host Bus compliant

2D Graphics Processor

- 128-bit 2D graphics engine
- Hardware 2D rotation
- Supports ROP3, 256 operations
- Supports 8bpp, 15/16bpp and 32bpp color depth modes
- BitBLT (Bit BLock Transfer) functions including alpha BLTs
- True-color hardware cursor (64x64x32bpp) with 256-level blending effect
- Color expansion, source Color Key and destination Color Key
- Bresenham line drawing / style line function
- Transparency mode
- Window clipping
- Text function

3D Graphics Processor

- DirectX 9.0 programmable graphics engine
- 1 Pixel Shader (PS 2.0)
- Internal full ARGB 10-10-10-10 format for high rendering quality
- 96-bit (4xFP24) Pixel Precision
- Pixel Shader supports 16 concurrent texture map references per rendering pass
- Shadow volume acceleration (2-Sided Stencil)
- Unconditional non-power-of-2 textures
- MIP-Mapped volume/cube maps
- Floating point render target/texture formats
- Vertex cache
- Color buffer with sRGB format supported and blending with color field 1.0
- Supports various texture formats, including 16/32bpp RGB, 32bpp sRGB, YUV422, V410, compressed texture (DXTC) and depth texture
- Video texture supported with programmable de-Gamma (up to Gamma 3.0)
- Multiple render target (MRT) up to 4
- Perspective color, fog, texture
- High quality texture filtering with bi-linear, tri-linear, anisotropy (up to 16x by trilinear), or programmable 4x4 filter (Gaussian filter, HP filter, LP filter)
- Supports 2048x2048x32bpp

Hi-Def Video Processor

- Supports Chromotion programmable video engine
- Integrated 3D and video processing through Pixel Shader engine
- Bob, Weave and Medium Filter de-interlacing modes
- High quality video scaling engine supports input up to 1920 pixels wide
- Supports Microsoft VMR through front-end video scaling, color space conversion and blending

Video Capture Capability

- Supports parallel and serial Transport Stream inputs
- Supports 8-bit or 16-bit CCIR656/601input
- Video capture and playback tear free auto flipping
- External Hsync / Vsync support

• Unified Video Decoding Accelerator

MPEG-2 Decoding Mode

- Supports VLD (Various Length Decode)
- Supports iDCT
- Supports motion compensation
- Supports MP@HL

MPEG-4 / DivX Decoding Mode

- Supports MPEG4 (ISO/IEC 14496-2)
- Supports MPEG4 ASP (Advanced Simple Profile) Level 5
- Supports DivX3.11 / DivX4 / DivX5
- Supports XVID
- Supports I, P, and B VOPs
- Supports interlaced frame decoding
- Supports GMC (Global Motion Compensation) L0 / L1
- Supports iDCT
- Supports ¼-pixel MC support
- High video quality and performance

WMV9 / VC1 Decoding Mode

- Accelerates AP@L1 decoding from iDCT to motion compensation
- Supports adaptive macroblock quantization
- Supports variable-sized iDCT Transform
- Supports pre-processing function
- Supports intensity compensation
- Supports 4 MVs and long motion vector mode
- Supports V9 loop filter
- Supports simple and full quarter-pixel motion compensation
- Supports interlace field and frame coding modes
- Video auto-flipping
- Hardware DVD sub-picture blending

- **External Display Support**

CRT Display Interface

- 30-bit true-color RAMDAC up to 350 MHz pixel rate with gamma correction capability
- Supports CRT resolutions up to 1920x1440

LVDS Panel Interface

- Supports panel resolution from VGA through UXGA (1600 x 1200)
- Supports one Dual-Channel panel or two Single-Channel LVDS panels

TTL LCD Panel Interface (DVP1)

- Supports 18-bit TTL LCD panel interface

TV-Out Interface (DVP1)

- 12-bit / 16-bit / 20-bit interface to external TV encoder for NTSC or PAL TV or HDTV display

12-bit DVI Transmitter Interface (DVP1)

- Double-data-rate data transfer with clock rates up to 165 MHz
- Built-in digital phase adjuster to fine-tune signal timing between clock and data bus
- Optional 16-bit ARGB interface (DVP1)
- Video data output to external HDMI (High-Definition Multimedia Interface) transmitter

- **Integrated LVDS Transmitter**

LVDS Transmitter

- Compatible with TIA/EIA-644
- Supports panel resolution from VGA through UXGA (1600 x 1200)
- Supports wide panel resolution up to WUXGA (1920 x 1080)

Supports one Dual-Channel panel or two Single-Channel LVDS panels

- **DuoView+™ Dual Image Capability**
  - WinXP multi-monitor, extended desktop support
  - Two independent display engines which can display completely different information at different resolutions, pixel depths, and refresh rates
  - CRT and LVDS / DVI panel refresh rates are independently programmable for optimum image quality
- **Full Software Support**
  - Microsoft DirectX 7.0, 8.0 and 9.0 compatible
  - Microsoft DirectX Texture Compression (DXTC / S3TC)
  - Supports OpenGL™
  - Drivers for major WinXP APIs: Direct3D™, DirectDraw™, DirectShow™ and OpenGL™ ICD for Windows XP
  - Supports Microsoft Windows Vista and Windows CE
  - Supports Linux
- **Graphics Power Management Support**
  - Supports SnapShot low power display mode
  - Built-in reference voltage generator and monitor sense circuits
  - Automatic panel power sequencing and VESA DPMS (Display Power Management Signaling) CRT power-down
  - External I/O signal controls enabling of graphics accelerator into standby / suspend-off state
  - Dynamic clock gating for inactive functions to achieve maximum power saving
  - Extensive display power management
  - I^2C Serial Bus and DDC / E-DDC Monitor Communications for Plug-and-Play configuration

- **High Definition (HD) Audio Controller**
  - High performance audio controller with 192 KHz sample rate, 32-bit per sample and up to 8 channels
  - Microsoft UAA (Universal Audio Architecture) driver support
  - Up to three independent playback streams and audio codecs
  - Multiple recording channels for array microphone
  - Supports jack sensing / retasking
- **Serial ATA Controller**
  - Supports up to 2 SATA devices
  - ***VX800:*** Integrated SATA PHY supporting 3 Gbit/s transfer rate
  - ***VX800UT:*** Integrated SATA PHY supporting 1.5 Gbit/s transfer rate
  - Complies with Serial ATA II PHY Specification *(VX800)*
  - Complies with Serial ATA Specification Revision 1.0
  - Supports SATA port multiplier functions
- **Ultra DMA-133 / 100 / 66 / 33 Bus Master EIDE**
  - Single channel EIDE controller supporting 2 Enhanced IDE devices
  - Data transfer rate up to 133 MB/sec to cover PIO mode 4, multi-word DMA mode 2, and UltraDMA-133 interface
  - Full scatter gather capability
  - Supports ATAPI compliant devices including DVD devices
  - Supports PCI native and ATA compatibility modes
- **Universal Serial Bus Controller**
  - Six USB 2.0 ports, one USB 2.0 root hub, and three USB 1.1 root hubs
  - USB 2.0 and Enhanced Host Controller Interface (EHCI) v1.0 compliant
  - USB 1.1 and Universal Host Controller Interface (UHCI) v1.1 compliant
  - Legacy keyboard and PS/2 mouse support
  - One USB 2.0 debug port

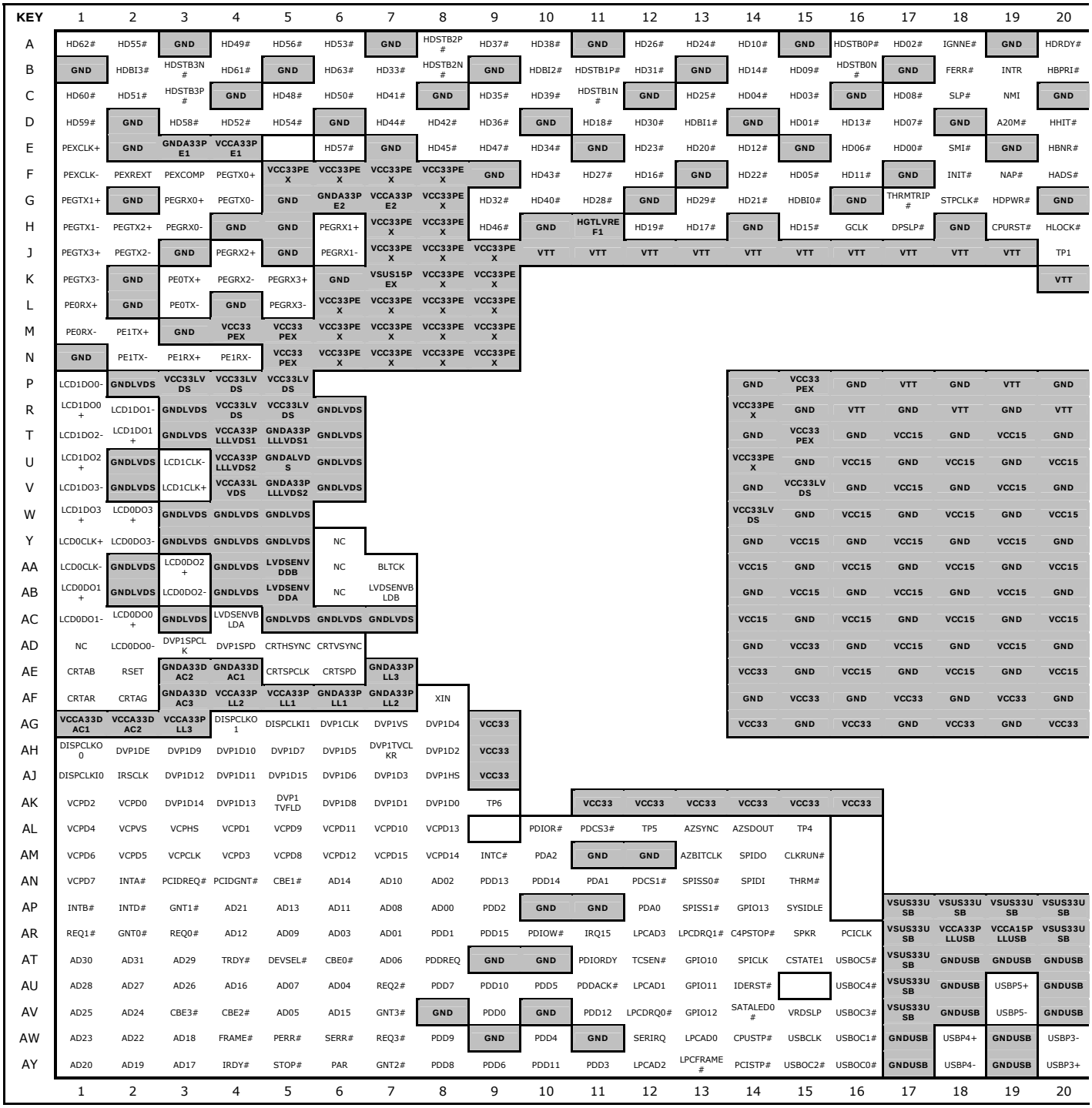
- **SPI Controller**
  - Supports two SPI slave devices
  - Supports SPI flash memory
  - Supports to write 256 bytes in one shot
  - Supports external plug programmer to update BIOS data
  - Supports dynamic clock stop
  - Supports 16-byte data buffer
- **SDIO Host Controller**
  - Compliant with SD Host Controller Standard Specification ver. 1.00 with both DMA and PIO mode.
  - Compliant with SD Memory Card Specification ver. 2.0.
  - Supports SD 1-bit and 4-bit data transfer modes
  - Supports 2 independent SDIO slots
  - Supports up to 7 functions in SDIO 1-bit or 4-bit mode with each slot
  - Supports host clock rate from 187.5KHz to 48MHz
  - Supports High-Speed SDIO card with up to 192Mbit/sec transfer rate
  - Supports multiple block transaction with stop command
  - Supports wakeup control
- **MemoryStick™ (MS) / MemoryStick Pro™ (MS Pro) Interfaces**
  - Complies with MemoryStick interface specification
  - Supports 4-bit and 1-bit MS Pro interface
  - Fully supports Memory Stick Pro TPCs
  - Hardware CRC16 generation and verification
  - Supports multi-page access
  - Supports flash command timeout detection
  - Supports over clock rate up to 48MHz
- **Secure Digital™ (SD) / Multi Media Card™ (MMC) Interfaces**
  - Complies with Secure Digital/MMC interfaces specification
  - Supports 4-bit and 1-bit Secure Digital interface
  - Complies with SD Memory Card Specifications rev. 2.0
  - Command transmit and response receive can be enabled separately
  - Hardware CRC7 generation and verification on CMD
  - Hardware CRC16 generation and verification on DAT
  - Optional single byte/bit operation on both CMD and DAT
  - Data processing in block or byte
  - Supports multiple block transaction with stop command
  - Supports different clock rate from 375 KHz to 48 MHz

- **Concurrent PCI Bus Controller**
  - PCI 2.3 compliant, 33MHz, 32 bit, 3.3V PCI interface with 5V tolerant inputs
  - Supports up to four PCI masters
  - Zero wait state PCI master and slave burst transfer rate, with up to 132 MB/sec data transfer rate
  - PCI master snoop ahead and snoop filtering
  - Byte merging in the write buffers to reduce the number of PCI cycles
  - Supports delay transaction
  - Transaction timer for fair arbitration between PCI masters
  - Symmetric arbitration between Host / PCI bus for optimized system performance
  - Complete steerable PCI interrupts
  - Supports PC / PCI DMA
- **System Management Bus Interface**
  - Compliant with System Management Bus (SMBus) Revision 2.0
  - I^2C devices compatible
  - Supports SMBus Address Resolution Protocol (ARP) by using host commands through software
  - Supports slave interface for external SMBus masters to control resume events
  - Supports Alarm-On-LAN 2 through a SMBus-interfaced register
- **Plug and Play Functions**
  - Steerable PCI interrupts
  - Steerable interrupts for integrated peripheral controllers
  - Microsoft Windows XP plug and play BIOS compliant
- **Integrated Legacy Functions**
  - Integrated Keyboard Controller with PS2 mouse and password wake-up support
  - Integrated two RS-232 serial ports with DMA support (optional)
  - Integrated IR interface (optional)
  - Integrated DS12885-style Real Time Clock with extended 256 byte CMOS RAM, Day / Month Alarm and century field
  - Integrated DMA, timer, and interrupt controller
  - Fast reset and Gate A20 operation
- **Sophisticated Power Management**
  - ACPI 3.0 and APM v1.2 Compliant
  - Supports CPU clock throttling and clock stop during ACPI C2 / C3 / C4 states
  - Supports extensive LCD panel display power management
  - Supports PCI clock run, Power Management Enable (PME) control, and PCI / CPU clock generator stop control
  - Supports multiple system suspend types: Power-on Suspend (POS) with flexible CPU / PCI bus reset options, Suspend to DRAM (STR), and Suspend to Disk (soft-off), all with hardware automatic wake-up
  - Multiple suspend power plane controls and suspend status indicators
  - Integrates an idle timer, a peripheral timer and a general purpose timer, plus a 24/32-bit ACPI compliant timer
  - Supports normal, doze, sleep, suspend and conserve modes
  - Global and local device power control
  - Supports system event monitoring with two event classes
  - Primary and secondary interrupt differentiation for individual channels
  - Dedicated input pins for power and sleep buttons, and external modem ring indicator
  - Multiple internal and external SMI sources for flexible power management models
  - Thermal alarm on external temperature sensing circuit
  - Dynamic clock gating control on functional blocks
  - Dynamic I/O pad driving control
  - I/O pad leakage control
- **Built-in NAND-tree pin scan test capability**

BALLOUTS

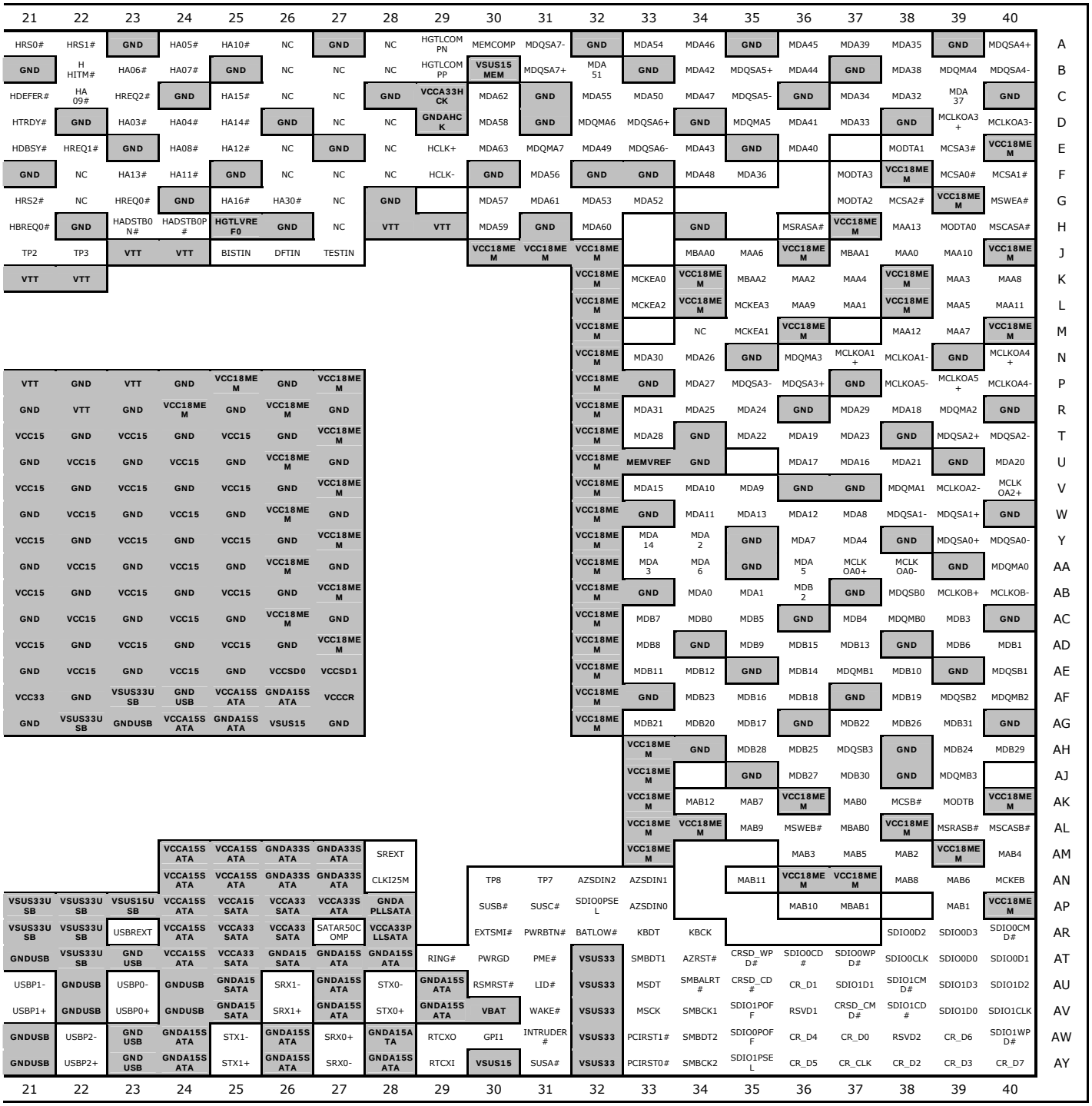
VX800 Ball Map

Figure 1. VX800 Ball Map– Left Side Top View



KEY	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	HD62#	HD55#	GND	HD49#	HD56#	HD53#	GND	HDSTB2P#	HD37#	HD38#	GND	HD26#	HD24#	HD10#	GND	HDSTB0P#	HD02#	IGNNE#	GND	HDRDY#
B	GND	HDBI3#	HDSTB3N#	HD61#	GND	HD63#	HD33#	HDSTB2N#	GND	HDBI2#	HDSTB1P#	HD31#	GND	HD14#	HD09#	HDSTB0N#	GND	FERR#	INTR	HBPRI#
C	HD60#	HD51#	HDSTB3P#	GND	HD48#	HD50#	HD41#	GND	HD35#	HD39#	HDSTB1N#	GND	HD25#	HD04#	HD03#	GND	HD08#	SLP#	NMI	GND
D	HD59#	GND	HD58#	HD52#	HD54#	GND	HD44#	HD42#	HD36#	GND	HD18#	HD30#	HDBI1#	GND	HD01#	HD13#	HD07#	GND	A20M#	HHIT#
E	PEXCLK+	GND	GNDA33PE1	VCCA33PE1		HD57#	GND	HD45#	HD47#	HD34#	GND	HD23#	HD20#	HD12#	GND	HD06#	HD00#	SMI#	GND	HBNR#
F	PEXCLK-	PEXREXT	PEXCOMP	PEGTX0+	VCC33PEX	VCC33PEX	VCC33PEX	VCC33PEX	GND	HD43#	HD27#	HD16#	GND	HD22#	HD05#	HD11#	GND	INIT#	NAP#	HADS#
G	PEGTX1+	GND	PEGRX0+	PEGTX0-	GND	GNDA33PE2	VCA33PE2	VCC33PEX	HD32#	HD40#	HD28#	GND	HD29#	HD21#	HDBI0#	GND	THRMTRIP#	STPCLK#	HDPWR#	GND
H	PEGTX1-	PEGTX2+	PEGRX0-	GND	GND	PEGRX1+	VCC33PEX	VCC33PEX	HD46#	GND	HGTLVREF1	HD19#	HD17#	GND	HD15#	GCLK	DPSLP#	GND	CPURST#	HLOCK#
J	PEGTX3+	PEGTX2-	GND	PEGRX2+	GND	PEGRX1-	VCC33PEX	VCC33PEX	VCC33PEX	VTT	VTT	VTT	VTT	VTT	VTT	VTT	VTT	VTT	VTT	TP1
K	PEGTX3-	GND	PE0TX+	PEGRX2-	PEGRX3+	GND	VSUS15PEX	VCC33PEX	VCC33PEX											VTT
L	PE0RX+	GND	PE0TX-	GND	PEGRX3-	VCC33PEX	VCC33PEX	VCC33PEX	VCC33PEX											
M	PE0RX-	PE1TX+	GND	VCC33PEX	VCC33PEX	VCC33PEX	VCC33PEX	VCC33PEX	VCC33PEX											
N	GND	PE1TX-	PE1RX+	PE1RX-	VCC33PEX	VCC33PEX	VCC33PEX	VCC33PEX	VCC33PEX											
P	LCD1DO0-	GNDLVDS	VCC33LVDS	VCC33LVDS	VCC33LVDS									GND	VCC33PEX	GND	VTT	GND	VTT	GND
R	LCD1DO0+	LCD1DO1-	GNDLVDS	VCC33LVDS	VCC33LVDS	GNDLVDS								VCC33PEX	GND	VTT	GND	VTT	GND	VTT
T	LCD1DO2-	LCD1DO1+	GNDLVDS	VCCA33PLLLVDS1	GNDA33PLLLVDS1	GNDLVDS								GND	VCC33PEX	GND	VCC15	GND	VCC15	GND
U	LCD1DO2+	GNDLVDS	LCD1CLK-	VCCA33PLLLVDS2	GNDALVDS	GNDLVDS								VCC33PEX	GND	VCC15	GND	VCC15	GND	VCC15
V	LCD1DO3-	GNDLVDS	LCD1CLK+	VCCA33LVDS	GNDA33PLLLVDS2	GNDLVDS								GND	VCC33LVDS	GND	VCC15	GND	VCC15	GND
W	LCD1DO3+	LCD0DO3+	GNDLVDS	GNDLVDS	GNDLVDS									VCC33LVDS	GND	VCC15	GND	VCC15	GND	VCC15
Y	LCD0CLK+	LCD0DO3-	GNDLVDS	GNDLVDS	GNDLVDS	NC								GND	VCC15	GND	VCC15	GND	VCC15	GND
AA	LCD0CLK-	GNDLVDS	LCD0DO2+	GNDLVDS	LVDSENVDDB	NC	BLTCK							VCC15	GND	VCC15	GND	VCC15	GND	VCC15
AB	LCD0DO1+	GNDLVDS	LCD0DO2-	GNDLVDS	LVDSENVDDA	NC	LVDSENVBLDB							GND	VCC15	GND	VCC15	GND	VCC15	GND
AC	LCD0DO1-	LCD0DO0+	GNDLVDS	LVDSENVBLDA	GNDLVDS	GNDLVDS	GNDLVDS							VCC15	GND	VCC15	GND	VCC15	GND	VCC15
AD	NC	LCD0DO0-	DVP1SPCLK	DVP1SPD	CRTHSYNC	CRTVSYNC								GND	VCC33	GND	VCC15	GND	VCC15	GND
AE	CRTAB	RSET	GNDA33DAC2	GNDA33DAC1	CRTSPCLK	CRTSPD	GNDA33PLL3							VCC33	GND	VCC15	GND	VCC15	GND	VCC15
AF	CRTAR	CRTAG	GNDA33DAC3	VCCA33PLL2	VCCA33PLL1	GNDA33PLL1	GNDA33PLL2	XIN						GND	VCC33	GND	VCC33	GND	VCC33	GND
AG	VCCA33DAC1	VCCA33DAC2	VCCA33PLL3	DISPCLKO1	DISPCLKI1	DVP1CLK	DVP1VS	DVP1D4	VCC33					VCC33	GND	VCC33	GND	VCC33	GND	VCC33
AH	DISPCLKO0	DVP1DE	DVP1D9	DVP1D10	DVP1D7	DVP1D5	DVP1TVCLKR	DVP1D2	VCC33											
AJ	DISPCLKI0	IRSCLK	DVP1D12	DVP1D11	DVP1D15	DVP1D6	DVP1D3	DVP1HS	VCC33											
AK	VCPD2	VCPD0	DVP1D14	DVP1D13	DVP1TVFLD	DVP1D8	DVP1D1	DVP1D0	TP6		VCC33	VCC33	VCC33	VCC33	VCC33	VCC33				
AL	VCPD4	VCPVS	VCPHS	VCPD1	VCPD9	VCPD11	VCPD10	VCPD13		PDIOR#	PDCS3#	TP5	AZSYNC	AZSDOUT	TP4					
AM	VCPD6	VCPD5	VCPCLK	VCPD3	VCPD8	VCPD12	VCPD15	VCPD14	INTC#	PDA2	GND	GND	AZBITCLK	SPIDO	CLKRUN#					
AN	VCPD7	INTA#	PCIDREQ#	PCIDGNT#	CBE1#	AD14	AD10	AD02	PDD13	PDD14	PDA1	PDCS1#	SPISS0#	SPIDI	THRM#					
AP	INTB#	INTD#	GNT1#	AD21	AD13	AD11	AD08	AD00	PDD2	GND	GND	PDA0	SPISS1#	GPIO13	SYSIDLE		VSUS33USB	VSUS33USB	VSUS33USB	VSUS33USB
AR	REQ1#	GNT0#	REQ0#	AD12	AD09	AD03	AD01	PDD1	PDD15	PDIOW#	IRQ15	LPCAD3	LPCDRQ1#	C4PSTOP#	SPKR	PCICLK	VSUS33USB	VCCA33PLLUSB	VCCA15PLLUSB	VSUS33USB
AT	AD30	AD31	AD29	TRDY#	DEVSEL#	CBE0#	AD06	PDDREQ	GND	GND	PDIORDY	TCSEN#	GPIO10	SPICLK	CSTATE1	USBOC5#	VSUS33USB	GNDUSB	GNDUSB	GNDUSB
AU	AD28	AD27	AD26	AD16	AD07	AD04	REQ2#	PDD7	PDD10	PDD5	PDDACK#	LPCAD1	GPIO11	IDERST#		USBOC4#	VSUS33USB	GNDUSB	USBP5+	GNDUSB
AV	AD25	AD24	CBE3#	CBE2#	AD05	AD15	GNT3#	GND	PDD0	GND	PDD12	LPCDRQ0#	GPIO12	SATALED0#	VRDSLP	USBOC3#	VSUS33USB	GNDUSB	USBP5-	GNDUSB
AW	AD23	AD22	AD18	FRAME#	PERR#	SERR#	REQ3#	PDD9	GND	PDD4	GND	SERIRQ	LPCAD0	CPUSTP#	USBCLK	USBOC1#	GNDUSB	USBP4+	GNDUSB	USBP3-
AY	AD20	AD19	AD17	IRDY#	STOP#	PAR	GNT2#	PDD8	PDD6	PDD11	PDD3	LPCAD2	LPCFRAME#	PCISTP#	USBOC2#	USBOC0#	GNDUSB	USBP4-	GNDUSB	USBP3+
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20

Figure 2. VX800 Ball Map– Right Side Top View



21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	
HRS0#	HRS1#	GND	HA05#	HA10#	NC	GND	NC	HGTLCOMPN	MEMCOMP	MDQSA7-	GND	MDA54	MDA46	GND	MDA45	MDA39	MDA35	GND	MDQSA4+	A
GND	H HITM#	HA06#	HA07#	GND	NC	NC	NC	HGTLCOMPP	VSUS15MEM	MDQSA7+	MDA 51	GND	MDA42	MDQSA5+	MDA44	GND	MDA38	MDQMA4	MDQSA4-	B
HDEFER#	HA 09#	HREQ2#	GND	HA15#	NC	NC	GND	VCCA33HCK	MDA62	GND	MDA55	MDA50	MDA47	MDQSA5-	GND	MDA34	MDA32	MDA 37	GND	C
HTRDY#	GND	HA03#	HA04#	HA14#	GND	NC	NC	GNDAHCK	MDA58	GND	MDQMA6	MDQSA6+	GND	MDQMA5	MDA41	MDA33	GND	MCLKOA3+	MCLKOA3-	D
HDBSY#	HREQ1#	GND	HA08#	HA12#	NC	GND	NC	HCLK+	MDA63	MDQMA7	MDA49	MDQSA6-	MDA43	GND	MDA40		MODTA1	MCSA3#	VCC18MEM	E
GND	NC	HA13#	HA11#	GND	NC	NC	NC	HCLK-	GND	MDA56	GND	GND	MDA48	MDA36		MODTA3	VCC18MEM	MCSA0#	MCSA1#	F
HRS2#	NC	HREQ0#	GND	HA16#	HA30#	NC	GND		MDA57	MDA61	MDA53	MDA52				MODTA2	MCSA2#	VCC18MEM	MSWEA#	G
HBREQ0#	GND	HADSTB0N#	HADSTB0P#	HGTLVREF0	GND	NC	VTT	VTT	MDA59	GND	MDA60		GND		MSRASA#	VCC18MEM	MAA13	MODTA0	MSCASA#	H
TP2	TP3	VTT	VTT	BISTIN	DFTIN	TESTIN			VCC18MEM	VCC18MEM	VCC18MEM		MBAA0	MAA6	VCC18MEM	MBAA1	MAA0	MAA10	VCC18MEM	J
VTT	VTT										VCC18MEM	MCKEA0	VCC18MEM	MBAA2	MAA2	MAA4	VCC18MEM	MAA3	MAA8	K
											VCC18MEM	MCKEA2	VCC18MEM	MCKEA3	MAA9	MAA1	VCC18MEM	MAA5	MAA11	L
											VCC18MEM		NC	MCKEA1	VCC18MEM		MAA12	MAA7	VCC18MEM	M
											VCC18MEM	MDA30	MDA26	GND	MDQMA3	MCLKOA1+	MCLKOA1-	GND	MCLKOA4+	N
VTT	GND	VTT	GND	VCC18MEM	GND	VCC18MEM					VCC18MEM	GND	MDA27	MDQSA3-	MDQSA3+	GND	MCLKOA5-	MCLKOA5+	MCLKOA4-	P
GND	VTT	GND	VCC18MEM	GND	VCC18MEM	GND					VCC18MEM	MDA31	MDA25	MDA24	GND	MDA29	MDA18	MDQMA2	GND	R
VCC15	GND	VCC15	GND	VCC15	GND	VCC18MEM					VCC18MEM	MDA28	GND	MDA22	MDA19	MDA23	GND	MDQSA2+	MDQSA2-	T
GND	VCC15	GND	VCC15	GND	VCC18MEM	GND					VCC18MEM	MEMVREF	GND		MDA17	MDA16	MDA21	GND	MDA20	U
VCC15	GND	VCC15	GND	VCC15	GND	VCC18MEM					VCC18MEM	MDA15	MDA10	MDA9	GND	GND	MDQMA1	MCLKOA2-	MCLK OA2+	V
GND	VCC15	GND	VCC15	GND	VCC18MEM	GND					VCC18MEM	GND	MDA11	MDA13	MDA12	MDA8	MDQSA1-	MDQSA1+	GND	W
VCC15	GND	VCC15	GND	VCC15	GND	VCC18MEM					VCC18MEM	MDA 14	MDA 2	GND	MDA7	MDA4	GND	MDQSA0+	MDQSA0-	Y
GND	VCC15	GND	VCC15	GND	VCC18MEM	GND					VCC18MEM	MDA 3	MDA 6	GND	MDA 5	MCLK OA0+	MCLK OA0-	GND	MDQMA0	AA
VCC15	GND	VCC15	GND	VCC15	GND	VCC18MEM					VCC18MEM	GND	MDA0	MDA1	MDB 2	GND	MDQSB0	MCLKOB+	MCLKOB-	AB
GND	VCC15	GND	VCC15	GND	VCC18MEM	GND					VCC18MEM	MDB7	MDB0	MDB5	GND	MDB4	MDQMB0	MDB3	GND	AC
VCC15	GND	VCC15	GND	VCC15	GND	VCC18MEM					VCC18MEM	MDB8	GND	MDB9	MDB15	MDB13	GND	MDB6	MDB1	AD
GND	VCC15	GND	VCC15	GND	VCCSD0	VCCSD1					VCC18MEM	MDB11	MDB12	GND	MDB14	MDQMB1	MDB10	GND	MDQSB1	AE
VCC33	GND	VSUS33USB	GNDUSB	VCCA15SATA	GNDA15SATA	VCCCR					VCC18MEM	GND	MDB23	MDB16	MDB18	GND	MDB19	MDQSB2	MDQMB2	AF
GND	VSUS33USB	GNDUSB	VCCA15SATA	GNDA15SATA	VSUS15	GND					VCC18MEM	MDB21	MDB20	MDB17	GND	MDB22	MDB26	MDB31	GND	AG
												VCC18MEM	GND	MDB28	MDB25	MDQSB3	GND	MDB24	MDB29	AH
												VCC18MEM		GND	MDB27	MDB30	GND	MDQMB3		AJ
												VCC18MEM	MAB12	MAB7	VCC18MEM	MAB0	MCSB#	MODTB	VCC18MEM	AK
												VCC18MEM	VCC18MEM	MAB9	MSWEB#	MBAB0	VCC18MEM	MSRASB#	MSCASB#	AL
			VCCA15SATA	VCCA15SATA	GNDA33SATA	GNDA33SATA	SREXT					VCC18MEM			MAB3	MAB5	MAB2	VCC18MEM	MAB4	AM
			VCCA15SATA	VCCA15SATA	GNDA33SATA	GNDA33SATA	CLKI25M		TP8	TP7	AZSDIN2	AZSDIN1		MAB11	VCC18MEM	VCC18MEM	MAB8	MAB6	MCKEB	AN
VSUS33USB	VSUS33USB	VSUS15USB	VCCA15SATA	VCCA15SATA	VCCA33SATA	VCCA33SATA	GNDAPLLSATA		SUSB#	SUSC#	SDIO0PSEL	AZSDIN0			MAB10	MBAB1		MAB1	VCC18MEM	AP
VSUS33USB	VSUS33USB	USBREXT	VCCA15SATA	VCCA33SATA	VCCA33SATA	SATAR50COMP	VCCA33PLLSATA		EXTSMI#	PWRBTN#	BATLOW#	KBDT	KBCK				SDIO0D2	SDIO0D3	SDIO0CMD#	AR
GNDUSB	VSUS33USB	GNDUSB	VCCA15SATA	VCCA33SATA	GNDA15SATA	GNDA15SATA	GNDA15SATA	RING#	PWRGD	PME#	VSUS33	SMBDT1	AZRST#	CRSD_WPD#	SDIO0CD#	SDIO0WPD#	SDIO0CLK	SDIO0D0	SDIO0D1	AT
USBP1-	GNDUSB	USBP0-	GNDUSB	GNDA15SATA	SRX1-	GNDA15SATA	STX0-	GNDA15SATA	RSMRST#	LID#	VSUS33	MSDT	SMBALRT#	CRSD_CD#	CR_D1	SDIO1D1	SDIO1CMD#	SDIO1D3	SDIO1D2	AU
USBP1+	GNDUSB	USBP0+	GNDUSB	GNDA15SATA	SRX1+	GNDA15SATA	STX0+	GNDA15SATA	VBAT	WAKE#	VSUS33	MSCK	SMBCK1	SDIO1POFF	RSVD1	CRSD_CMD#	SDIO1CD#	SDIO1D0	SDIO1CLK	AV
GNDUSB	USBP2-	GNDUSB	GNDA15SATA	STX1-	GNDA15SATA	SRX0+	GNDA15ATA	RTCXO	GPI1	INTRUDER#	VSUS33	PCIRST1#	SMBDT2	SDIO0POF F	CR_D4	CR_D0	RSVD2	CR_D6	SDIO1WPD#	AW
GNDUSB	USBP2+	GNDUSB	GNDA15SATA	STX1+	GNDA15SATA	SRX0-	GNDA15SATA	RTCXI	VSUS15	SUSA#	VSUS33	PCIRST0#	SMBCK2	SDIO1PSEL	CR_D5	CR_CLK	CR_D2	CR_D3	CR_D7	AY
21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	

VX800 Signal Ball List

Table 2. VX800 Signal Ball List (Listed by Ball Name)

Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #
A20M#	D19	CRTVSYNC	AD06	GND	AC25	GND	D10
AD00	AP08	CSTATE1 / GPO5	AT15	GND	AC27	GND	D14
AD01	AR07	DEVSEL#	AT05	GND	AC36	GND	D18
AD02	AN08	DFTIN	J26	GND	AC40	GND	D22
AD03	AR06	DISPCLKI0 / VIDEO_GPIO2	AJ01	GND	AD14	GND	D26
AD04	AU06	DISPCLKI1 / VIDEO_GPIO4	AG05	GND	AD16	GND	D31
AD05	AV05	DISPCLKO0 / VIDEO_GPIO3	AH01	GND	AD18	GND	D34
AD06	AT07	DISPCLKO1 / VIDEO_GPIO5	AG04	GND	AD20	GND	D38
AD07	AU05	DPSLP#	H17	GND	AD22	GND	E02
AD08	AP07	DVP1CLK	AG06	GND	AD24	GND	E07
AD09	AR05	DVP1D00 / RI2	AK08	GND	AD26	GND	E11
AD10	AN07	DVP1D01 / DCD2	AK07	GND	AD34	GND	E15
AD11	AP06	DVP1D02 / SOUT2	AH08	GND	AD38	GND	E19
AD12	AR04	DVP1D03 / SIN2	AJ07	GND	AE15	GND	E23
AD13	AP05	DVP1D04 / DTR2	AG08	GND	AE17	GND	E27
AD14	AN06	DVP1D05 / DSR2	AH06	GND	AE19	GND	E35
AD15	AV06	DVP1D06 / RTS2	AJ06	GND	AE21	GND	F09
AD16	AU04	DVP1D07 / CTS2	AH05	GND	AE23	GND	F13
AD17	AY03	DVP1D08 / RI1	AK06	GND	AE25	GND	F17
AD18	AW03	DVP1D09 / DCD1	AH03	GND	AE35	GND	F21
AD19	AY02	DVP1D10 / SOUT1	AH04	GND	AE39	GND	F25
AD20	AY01	DVP1D11 / SIN1	AJ04	GND	AF14	GND	F30
AD21	AP04	DVP1D12 / DTR1	AJ03	GND	AF16	GND	F32
AD22	AW02	DVP1D13 / DSR1	AK04	GND	AF18	GND	F33
AD23	AW01	DVP1D14 / RTS1	AK03	GND	AF20	GND	G02
AD24	AV02	DVP1D15 / CTS1	AJ05	GND	AF22	GND	G05
AD25	AV01	DVP1DE / IRRX2 / ITMOFF	AH02	GND	AF33	GND	G12
AD26	AU03	DVP1HS / IRTX	AJ08	GND	AF37	GND	G16
AD27	AU02	DVP1SPCLK	AD03	GND	AG15	GND	G20
AD28	AU01	DVP1SPD	AD04	GND	AG17	GND	G24
AD29	AT03	DVP1TVCLKR	AH07	GND	AG19	GND	G28
AD30	AT01	DVP1TVFLD	AK05	GND	AG21	GND	H04
AD31	AT02	DVP1VS / IRRX	AG07	GND	AG27	GND	H05
AZBITCLK	AM13	EXTSMI# / GPI5	AR30	GND	AG36	GND	H10
AZRST#	AT34	FERR#	B18	GND	AG40	GND	H14
AZSDIN0	AP33	FRAME#	AW04	GND	AH34	GND	H18
AZSDIN1	AN33	GCLK	H16	GND	AH38	GND	H22
AZSDIN2	AN32	GND	A03	GND	AJ35	GND	H26
AZSDOUT	AL14	GND	A07	GND	AJ38	GND	H31
AZSYNC	AL13	GND	A11	GND	AM11	GND	H34
BATLOW# / GPI4	AR32	GND	A15	GND	AM12	GND	J03
BISTIN	J25	GND	A19	GND	AP10	GND	J05
BLTCK	AA07	GND	A23	GND	AP11	GND	K02
C4PSTOP# / GPO6	AR14	GND	A27	GND	AT09	GND	K06
CBE0#	AT06	GND	A32	GND	AT10	GND	L02
CBE1#	AN05	GND	A35	GND	AV08	GND	L04
CBE2#	AV04	GND	A39	GND	AV10	GND	M03
CBE3#	AV03	GND	AA15	GND	AW09	GND	N01
CLKI25M	AN28	GND	AA17	GND	AW11	GND	N35
CLKRUN#	AM15	GND	AA19	GND	B01	GND	N39
CPURST#	H19	GND	AA21	GND	B05	GND	P14
CPUSTP#	AW14	GND	AA23	GND	B09	GND	P16
CR_CLK / SD_CLK	AY37	GND	AA25	GND	B13	GND	P18
CR_D0 / SD_D0	AW37	GND	AA27	GND	B17	GND	P20
CR_D1 / SD_D1	AU36	GND	AA35	GND	B21	GND	P22
CR_D2 / SD_D2	AY38	GND	AA39	GND	B25	GND	P24
CR_D3 / SD_D3	AY39	GND	AB14	GND	B33	GND	P26
CR_D4 / SD_D4	AW36	GND	AB16	GND	B37	GND	P33
CR_D5 / SD_D5	AY36	GND	AB18	GND	C04	GND	P37
CR_D6 / SD_D6	AW39	GND	AB20	GND	C08	GND	R15
CR_D7 / SD_D7	AY40	GND	AB22	GND	C12	GND	R17
CRSD_CD#	AU35	GND	AB24	GND	C16	GND	R19
CRSD_CMD#	AV37	GND	AB26	GND	C20	GND	R21
CRSD_WPD#	AT35	GND	AB33	GND	C24	GND	R23
CRTAB	AE01	GND	AB37	GND	C28	GND	R25
CRTAG	AF02	GND	AC15	GND	C31	GND	R27
CRTAR	AF01	GND	AC17	GND	C36	GND	R36
CRTHSYNC	AD05	GND	AC19	GND	C40	GND	R40
CRTSPCLK	AE05	GND	AC21	GND	D02	GND	T14
CRTSPD	AE06	GND	AC23	GND	D06	GND	T16

Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #
GND	T18	GNDA33SATA	AM26	HA11#	F24	HD55#	A02
GND	T20	GNDA33SATA	AM27	HA12#	E25	HD56#	A05
GND	T22	GNDA33SATA	AN26	HA13#	F23	HD57#	E06
GND	T24	GNDA33SATA	AN27	HA14#	D25	HD58#	D03
GND	T26	GNDAHCK	D29	HA15#	C25	HD59#	D01
GND	T34	GNDALVDS	U05	HA16#	G25	HD60#	C01
GND	T38	GNDAPLLSATA	AP28	HA30#	G26	HD61#	B04
GND	U15	GNDLVDS	AA02	HADS#	F20	HD62#	A01
GND	U17	GNDLVDS	AA04	HADSTB0N#	H23	HD63#	B06
GND	U19	GNDLVDS	AB02	HADSTB0P#	H24	HDBI0#	G15
GND	U21	GNDLVDS	AB04	HBNR#	E20	HDBI1#	D13
GND	U23	GNDLVDS	AC03	HBPRI#	B20	HDBI2#	B10
GND	U25	GNDLVDS	AC05	HBREQ0#	H21	HDBI3#	B02
GND	U27	GNDLVDS	AC06	HCLK-	F29	HDBSY#	E21
GND	U34	GNDLVDS	AC07	HCLK+	E29	HDEFER#	C21
GND	U39	GNDLVDS	P02	HD00#	E17	HDPWR#	G19
GND	V14	GNDLVDS	R03	HD01#	D15	HDRDY#	A20
GND	V16	GNDLVDS	R06	HD02#	A17	HDSTB0N#	B16
GND	V18	GNDLVDS	T03	HD03#	C15	HDSTB0P#	A16
GND	V20	GNDLVDS	T06	HD04#	C14	HDSTB1N#	C11
GND	V22	GNDLVDS	U02	HD05#	F15	HDSTB1P#	B11
GND	V24	GNDLVDS	U06	HD06#	E16	HDSTB2N#	B08
GND	V26	GNDLVDS	V02	HD07#	D17	HDSTB2P#	A08
GND	V36	GNDLVDS	V06	HD08#	C17	HDSTB3N#	B03
GND	V37	GNDLVDS	W03	HD09#	B15	HDSTB3P#	C03
GND	W15	GNDLVDS	W04	HD10#	A14	HGTLCOMPN	A29
GND	W17	GNDLVDS	W05	HD11#	F16	HGTLCOMPP	B29
GND	W19	GNDLVDS	Y03	HD12#	E14	HGTLVREF0	H25
GND	W21	GNDLVDS	Y04	HD13#	D16	HGTLVREF1	H11
GND	W23	GNDLVDS	Y05	HD14#	B14	HHIT#	D20
GND	W25	GNDUSB	AF24	HD15#	H15	HHITM#	B22
GND	W27	GNDUSB	AG23	HD16#	F12	HLOCK#	H20
GND	W33	GNDUSB	AT18	HD17#	H13	HREQ0#	G23
GND	W40	GNDUSB	AT19	HD18#	D11	HREQ1#	E22
GND	Y14	GNDUSB	AT20	HD19#	H12	HREQ2#	C23
GND	Y16	GNDUSB	AT21	HD20#	E13	HRS0#	A21
GND	Y18	GNDUSB	AT23	HD21#	G14	HRS1#	A22
GND	Y20	GNDUSB	AU18	HD22#	F14	HRS2#	G21
GND	Y22	GNDUSB	AU20	HD23#	E12	HTRDY#	D21
GND	Y24	GNDUSB	AU22	HD24#	A13	IDERST#	AU14
GND	Y26	GNDUSB	AU24	HD25#	C13	IGNNE#	A18
GND	Y35	GNDUSB	AV18	HD26#	A12	INIT#	F18
GND	Y38	GNDUSB	AV20	HD27#	F11	INTA#	AN02
GNDA15SATA	AF26	GNDUSB	AV22	HD28#	G11	INTB#	AP01
GNDA15SATA	AG25	GNDUSB	AV24	HD29#	G13	INTC#	AM09
GNDA15SATA	AT26	GNDUSB	AW17	HD30#	D12	INTD#	AP02
GNDA15SATA	AT27	GNDUSB	AW19	HD31#	B12	INTR	B19
GNDA15SATA	AT28	GNDUSB	AW21	HD32#	G09	INTRUDER# / GPI6	AW31
GNDA15SATA	AU25	GNDUSB	AW23	HD33#	B07	IRDY#	AY04
GNDA15SATA	AU27	GNDUSB	AY17	HD34#	E10	IRQ15	AR11
GNDA15SATA	AU29	GNDUSB	AY19	HD35#	C09	IRSCLK	AJ02
GNDA15SATA	AV25	GNDUSB	AY21	HD36#	D09	KBCK / A20GATE / GPIO5	AR34
GNDA15SATA	AV27	GNDUSB	AY23	HD37#	A09	KBDT / KBC_CPURST# / GPIO4	AR33
GNDA15SATA	AV29	GNT0#	AR02	HD38#	A10	LCD0CLK- / TX2-	AA01
GNDA15SATA	AW24	GNT1#	AP03	HD39#	C10	LCD0CLK+ / TX2+	Y01
GNDA15SATA	AW26	GNT2#	AY07	HD40#	G10	LCD0D0- / TXC-	AD02
GNDA15SATA	AW28	GNT3#	AV07	HD41#	C07	LCD0D0+ / TXC+	AC02
GNDA15SATA	AY24	GPI1	AW30	HD42#	D08	LCD0D1- / TX0-	AC01
GNDA15SATA	AY26	GPIO10 / PCIERST0#	AT13	HD43#	F10	LCD0D1+ / TX0+	AB01
GNDA15SATA	AY28	GPIO11 / PCIERST1#	AU13	HD44#	D07	LCD0D2- / TX1-	AB03
GNDA33DAC1	AE04	GPIO12	AV13	HD45#	E08	LCD0D2+ / TX1+	AA03
GNDA33DAC2	AE03	GPIO13	AP14	HD46#	H09	LCD0D3-	Y02
GNDA33DAC3	AF03	HA03#	D23	HD47#	E09	LCD0D3+	W02
GNDA33PE1	E03	HA04#	D24	HD48#	C05	LCD1CLK-	U03
GNDA33PE2	G06	HA05#	A24	HD49#	A04	LCD1CLK+	V03
GNDA33PLL1	AF06	HA06#	B23	HD50#	C06	LCD1D0-	P01
GNDA33PLL2	AF07	HA07#	B24	HD51#	C02	LCD1D0+	R01
GNDA33PLL3	AE07	HA08#	E24	HD52#	D04	LCD1D1-	R02
GNDA33PLLLVDS1	T05	HA09#	C22	HD53#	A06	LCD1D1+	T02
GNDA33PLLLVDS2	V05	HA10#	A25	HD54#	D05	LCD1D2-	T01

Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #
LCD1D2+	U01	MCSB#	AK38	MDB05	AC35	MSRASA#	H36
LCD1D3-	V01	MDA00	AB34	MDB06	AD39	MSRASB#	AL39
LCD1D3+	W01	MDA01	AB35	MDB07	AC33	MSWEA#	G40
LID# / GPI7	AU31	MDA02	Y34	MDB08	AD33	MSWEB#	AL36
LPCAD0	AW13	MDA03	AA33	MDB09	AD35	NAP#	F19
LPCAD1	AU12	MDA04	Y37	MDB10	AE38	NC	A26
LPCAD2	AY12	MDA05	AA36	MDB11	AE33	NC	A28
LPCAD3	AR12	MDA06	AA34	MDB12	AE34	NC	AA06
LPCDRQ0#	AV12	MDA07	Y36	MDB13	AD37	NC	AB06
LPCDRQ1#	AR13	MDA08	W37	MDB14	AE36	NC	AD01
LPCFRAME#	AY13	MDA09	V35	MDB15	AD36	NC	B26
LVDSENVBLDA	AC04	MDA10	V34	MDB16	AF35	NC	B27
LVDSENVBLDB	AB07	MDA11	W34	MDB17	AG35	NC	B28
LVDSENVDDA	AB05	MDA12	W36	MDB18	AF36	NC	C26
LVDSENVDDB	AA05	MDA13	W35	MDB19	AF38	NC	C27
MAA00	J38	MDA14	Y33	MDB20	AG34	NC	D27
MAA01	L37	MDA15	V33	MDB21	AG33	NC	D28
MAA02	K36	MDA16	U37	MDB22	AG37	NC	E26
MAA03	K39	MDA17	U36	MDB23	AF34	NC	E28
MAA04	K37	MDA18	R38	MDB24	AH39	NC	F22
MAA05	L39	MDA19	T36	MDB25	AH36	NC	F26
MAA06	J35	MDA20	U40	MDB26	AG38	NC	F27
MAA07	M39	MDA21	U38	MDB27	AJ36	NC	F28
MAA08	K40	MDA22	T35	MDB28	AH35	NC	G22
MAA09	L36	MDA23	T37	MDB29	AH40	NC	G27
MAA10	J39	MDA24	R35	MDB30	AJ37	NC	H27
MAA11	L40	MDA25	R34	MDB31	AG39	NC	M34
MAA12	M38	MDA26	N34	MDQMA0	AA40	NC	Y06
MAA13	H38	MDA27	P34	MDQMA1	V38	NMI	C19
MAB00	AK37	MDA28	T33	MDQMA2	R39	PAR	AY06
MAB01	AP39	MDA29	R37	MDQMA3	N36	PCICLK	AR16
MAB02	AM38	MDA30	N33	MDQMA4	B39	PCIDGNT# / GPIO9	AN04
MAB03	AM36	MDA31	R33	MDQMA5	D35	PCIDREQ# / GPIO8	AN03
MAB04	AM40	MDA32	C38	MDQMA6	D32	PCIRST0#	AY33
MAB05	AM37	MDA33	D37	MDQMA7	E31	PCIRST1#	AW33
MAB06	AN39	MDA34	C37	MDQMB0	AC38	PCISTP#	AY14
MAB07	AK35	MDA35	A38	MDQMB1	AE37	PDA0	AP12
MAB08	AN38	MDA36	F35	MDQMB2	AF40	PDA1	AN11
MAB09	AL35	MDA37	C39	MDQMB3	AJ39	PDA2	AM10
MAB10	AP36	MDA38	B38	MDQSA0-	Y40	PDCS1#	AN12
MAB11	AN35	MDA39	A37	MDQSA0+	Y39	PDCS3#	AL11
MAB12	AK34	MDA40	E36	MDQSA1-	W38	PDD00	AV09
MBAA0	J34	MDA41	D36	MDQSA1+	W39	PDD01	AR08
MBAA1	J37	MDA42	B34	MDQSA2-	T40	PDD02	AP09
MBAA2	K35	MDA43	E34	MDQSA2+	T39	PDD03	AY11
MBAB0	AL37	MDA44	B36	MDQSA3-	P35	PDD04	AW10
MBAB1	AP37	MDA45	A36	MDQSA3+	P36	PDD05	AU10
MCKEA0	K33	MDA46	A34	MDQSA4-	B40	PDD06	AY09
MCKEA1	M35	MDA47	C34	MDQSA4+	A40	PDD07	AU08
MCKEA2	L33	MDA48	F34	MDQSA5-	C35	PDD08	AY08
MCKEA3	L35	MDA49	E32	MDQSA5+	B35	PDD09	AW08
MCKEB	AN40	MDA50	C33	MDQSA6-	E33	PDD10	AU09
MCLKOA0-	AA38	MDA51	B32	MDQSA6+	D33	PDD11	AY10
MCLKOA0+	AA37	MDA52	G33	MDQSA7-	A31	PDD12	AV11
MCLKOA1-	N38	MDA53	G32	MDQSA7+	B31	PDD13	AN09
MCLKOA1+	N37	MDA54	A33	MDQSB0	AB38	PDD14	AN10
MCLKOA2-	V39	MDA55	C32	MDQSB1	AE40	PDD15	AR09
MCLKOA2+	V40	MDA56	F31	MDQSB2	AF39	PDDACK#	AU11
MCLKOA3-	D40	MDA57	G30	MDQSB3	AH37	PDDREQ	AT08
MCLKOA3+	D39	MDA58	D30	MEMCOMP	A30	PDIOR#	AL10
MCLKOA4-	P40	MDA59	H30	MEMVREF	U33	PDIORDY	AT11
MCLKOA4+	N40	MDA60	H32	MODTA0	H39	PDIOW#	AR10
MCLKOA5-	P38	MDA61	G31	MODTA1	E38	PE0RX-	M01
MCLKOA5+	P39	MDA62	C30	MODTA2	G37	PE0RX+	L01
MCLKOB-	AB40	MDA63	E30	MODTA3	F37	PE0TX-	L03
MCLKOB+	AB39	MDB00	AC34	MODTB	AK39	PE0TX+	K03
MCSA0#	F39	MDB01	AD40	MSCASA#	H40	PE1RX-	N04
MCSA1#	F40	MDB02	AB36	MSCASB#	AL40	PE1RX+	N03
MCSA2#	G38	MDB03	AC39	MSCK / IRQ1	AV33	PE1TX-	N02
MCSA3#	E39	MDB04	AC37	MSDT / IRQ12	AU33	PE1TX+	M02

Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #
PEGRX0-	H03	SPISS1# / GPO2	AP13	VCC15	AD19	VCC18MEM	K38
PEGRX0+	G03	SPKR / GPO7 / SATALED1#	AR15	VCC15	AD21	VCC18MEM	L32
PEGRX1-	J06	SREXT	AM28	VCC15	AD23	VCC18MEM	L34
PEGRX1+	H06	SRX0-	AY27	VCC15	AD25	VCC18MEM	L38
PEGRX2-	K04	SRX0+	AW27	VCC15	AE16	VCC18MEM	M32
PEGRX2+	J04	SRX1-	AU26	VCC15	AE18	VCC18MEM	M36
PEGRX3-	L05	SRX1+	AV26	VCC15	AE20	VCC18MEM	M40
PEGRX3+	K05	STOP#	AY05	VCC15	AE22	VCC18MEM	N32
PEGTX0-	G04	STPCLK#	G18	VCC15	AE24	VCC18MEM	P25
PEGTX0+	F04	STX0-	AU28	VCC15	T17	VCC18MEM	P27
PEGTX1-	H01	STX0+	AV28	VCC15	T19	VCC18MEM	P32
PEGTX1+	G01	STX1-	AW25	VCC15	T21	VCC18MEM	R24
PEGTX2-	J02	STX1+	AY25	VCC15	T23	VCC18MEM	R26
PEGTX2+	H02	SUSA# / GPO0	AY31	VCC15	T25	VCC18MEM	R32
PEGTX3-	K01	SUSB# / GPO8	AP30	VCC15	U16	VCC18MEM	T27
PEGTX3+	J01	SUSC# / GPO9	AP31	VCC15	U18	VCC18MEM	T32
PERR#	AW05	SYSIDLE / GPO10	AP15	VCC15	U20	VCC18MEM	U26
PEXCLK-	F01	TCSEN#	AT12	VCC15	U22	VCC18MEM	U32
PEXCLK+	E01	TESTIN	J27	VCC15	U24	VCC18MEM	V27
PEXCOMP	F03	THRM# / GPI9	AN15	VCC15	V17	VCC18MEM	V32
PEXREXT	F02	THRMTRIP# / GPIO7	G17	VCC15	V19	VCC18MEM	W26
PME#	AT31	TP1	J20	VCC15	V21	VCC18MEM	W32
PWRBTN#	AR31	TP2	J21	VCC15	V23	VCC18MEM	Y27
PWRGD	AT30	TP3	J22	VCC15	V25	VCC18MEM	Y32
REQ0#	AR03	TP4	AL15	VCC15	W16	VCC33	AD15
REQ1#	AR01	TP5	AL12	VCC15	W18	VCC33	AE14
REQ2#	AU07	TP6	AK09	VCC15	W20	VCC33	AF15
REQ3#	AW07	TP7	AN31	VCC15	W22	VCC33	AF17
RING# / CRPWREN# / GPI8	AT29	TP8	AN30	VCC15	W24	VCC33	AF19
RSET	AE02	TRDY#	AT04	VCC15	Y15	VCC33	AF21
RSMRST#	AU30	USBCLK	AW15	VCC15	Y17	VCC33	AG09
RSVD1	AV36	USBOC0#	AY16	VCC15	Y19	VCC33	AG14
RSVD2	AW38	USBOC1#	AW16	VCC15	Y21	VCC33	AG16
RTCXI	AY29	USBOC2#	AY15	VCC15	Y23	VCC33	AG18
RTCXO	AW29	USBOC3#	AV16	VCC15	Y25	VCC33	AG20
SATALED0# / GPO4	AV14	USBOC4#	AU16	VCC18MEM	AA26	VCC33	AH09
SATAR50COMP	AR27	USBOC5#	AT16	VCC18MEM	AA32	VCC33	AJ09
SDIO0CD#	AT36	USBP0-	AU23	VCC18MEM	AB27	VCC33	AK11
SDIO0CLK	AT38	USBP0+	AV23	VCC18MEM	AB32	VCC33	AK12
SDIO0CMD#	AR40	USBP1-	AU21	VCC18MEM	AC26	VCC33	AK13
SDIO0D0	AT39	USBP1+	AV21	VCC18MEM	AC32	VCC33	AK14
SDIO0D1	AT40	USBP2-	AW22	VCC18MEM	AD27	VCC33	AK15
SDIO0D2	AR38	USBP2+	AY22	VCC18MEM	AD32	VCC33	AK16
SDIO0D3	AR39	USBP3-	AW20	VCC18MEM	AE32	VCC33LVDS	P03
SDIO0POFF	AW35	USBP3+	AY20	VCC18MEM	AF32	VCC33LVDS	P04
SDIO0PSEL	AP32	USBP4-	AY18	VCC18MEM	AG32	VCC33LVDS	P05
SDIO0WPD#	AT37	USBP4+	AW18	VCC18MEM	AH33	VCC33LVDS	R04
SDIO1CD#	AV38	USBP5-	AV19	VCC18MEM	AJ33	VCC33LVDS	R05
SDIO1CLK	AV40	USBP5+	AU19	VCC18MEM	AK33	VCC33LVDS	V15
SDIO1CMD#	AU38	USBREXT	AR23	VCC18MEM	AK36	VCC33LVDS	W14
SDIO1D0	AV39	VBAT	AV30	VCC18MEM	AK40	VCC33PEX	F05
SDIO1D1	AU37	VCC15	AA14	VCC18MEM	AL33	VCC33PEX	F06
SDIO1D2	AU40	VCC15	AA16	VCC18MEM	AL34	VCC33PEX	F07
SDIO1D3	AU39	VCC15	AA18	VCC18MEM	AL38	VCC33PEX	F08
SDIO1POFF	AV35	VCC15	AA20	VCC18MEM	AM33	VCC33PEX	G08
SDIO1PSEL	AY35	VCC15	AA22	VCC18MEM	AM39	VCC33PEX	H07
SDIO1WPD#	AW40	VCC15	AA24	VCC18MEM	AN36	VCC33PEX	H08
SERIRQ	AW12	VCC15	AB15	VCC18MEM	AN37	VCC33PEX	J07
SERR#	AW06	VCC15	AB17	VCC18MEM	AP40	VCC33PEX	J08
SLP#	C18	VCC15	AB19	VCC18MEM	E40	VCC33PEX	J09
SMBALRT#	AU34	VCC15	AB21	VCC18MEM	F38	VCC33PEX	K08
SMBCK1	AV34	VCC15	AB23	VCC18MEM	G39	VCC33PEX	K09
SMBCK2 / GPIO1	AY34	VCC15	AB25	VCC18MEM	H37	VCC33PEX	L06
SMBDT1	AT33	VCC15	AC14	VCC18MEM	J30	VCC33PEX	L07
SMBDT2 / GPIO0	AW34	VCC15	AC16	VCC18MEM	J31	VCC33PEX	L08
SMI#	E18	VCC15	AC18	VCC18MEM	J32	VCC33PEX	L09
SPICLK / GPIO6	AT14	VCC15	AC20	VCC18MEM	J36	VCC33PEX	M04
SPIDI / GPI0	AN14	VCC15	AC22	VCC18MEM	J40	VCC33PEX	M05
SPIDO / GPO1	AM14	VCC15	AC24	VCC18MEM	K32	VCC33PEX	M06
SPISS0# / GPO3	AN13	VCC15	AD17	VCC18MEM	K34	VCC33PEX	M07

Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #
VCC33PEX	M08	VSUS33	AV32				
VCC33PEX	M09	VSUS33	AW32				
VCC33PEX	N05	VSUS33	AY32				
VCC33PEX	N06	VSUS33USB	AF23				
VCC33PEX	N07	VSUS33USB	AG22				
VCC33PEX	N08	VSUS33USB	AP17				
VCC33PEX	N09	VSUS33USB	AP18				
VCC33PEX	P15	VSUS33USB	AP19				
VCC33PEX	R14	VSUS33USB	AP20				
VCC33PEX	T15	VSUS33USB	AP21				
VCC33PEX	U14	VSUS33USB	AP22				
VCCA15PLLUSB	AR19	VSUS33USB	AR17				
VCCA15SATA	AF25	VSUS33USB	AR20				
VCCA15SATA	AG24	VSUS33USB	AR21				
VCCA15SATA	AM24	VSUS33USB	AR22				
VCCA15SATA	AM25	VSUS33USB	AT17				
VCCA15SATA	AN24	VSUS33USB	AT22				
VCCA15SATA	AN25	VSUS33USB	AU17				
VCCA15SATA	AP24	VSUS33USB	AV17				
VCCA15SATA	AP25	VTT	H28				
VCCA15SATA	AR24	VTT	H29				
VCCA15SATA	AT24	VTT	J10				
VCCA33DAC1	AG01	VTT	J11				
VCCA33DAC2	AG02	VTT	J12				
VCCA33HCK	C29	VTT	J13				
VCCA33LVDS	V04	VTT	J14				
VCCA33PE1	E04	VTT	J15				
VCCA33PE2	G07	VTT	J16				
VCCA33PLL1	AF05	VTT	J17				
VCCA33PLL2	AF04	VTT	J18				
VCCA33PLL3	AG03	VTT	J19				
VCCA33PLLLVDS1	T04	VTT	J23				
VCCA33PLLLVDS2	U04	VTT	J24				
VCCA33PLLSATA	AR28	VTT	K20				
VCCA33PLLUSB	AR18	VTT	K21				
VCCA33SATA	AP26	VTT	K22				
VCCA33SATA	AP27	VTT	P17				
VCCA33SATA	AR25	VTT	P19				
VCCA33SATA	AR26	VTT	P21				
VCCA33SATA	AT25	VTT	P23				
VCCCR	AF27	VTT	R16				
VCCSD0	AE26	VTT	R18				
VCCSD1	AE27	VTT	R20				
VCPCLK / DSR2 / PTS0CLK	AM03	VTT	R22				
VCPD00 / RI1 / PTS0D0	AK02	WAKE# / GPI2	AV31				
VCPD01 / DCD1 / PTS0D1	AL04	XIN	AF08				
VCPD02 / SOUT1 / PTS0D2	AK01						
VCPD03 / SIN1/ PTS0D3	AM04						
VCPD04 / DTR1 / PTS0D4	AL01						
VCPD05 / DSR1 / PTS0D5	AM02						
VCPD06 / RTS1 / PTS0D6	AM01						
VCPD07 / CTS1 / PTS0D7	AN01						
VCPD08 / SIN2 / PTS0ERR	AM05						
VCPD09 / SOUT2 / STSLVLD	AL05						
VCPD10 / DCD2 / STS1SYNC	AL07						
VCPD11 / RI2 / STS1CLK	AL06						
VCPD12 / IRTX / STS1ERR	AM06						
VCPD13 / IRRX	AL08						
VCPD14 / IRRX2 / ITMOFF	AM08						
VCPD15 / DTR2 / STS1D	AM07						
VCPHS / CTS2 / PTS0VLD	AL03						
VCPVS / RTS2 / PTS0SYNC	AL02						
VRDSLP	AV15						
VSUS15	AG26						
VSUS15	AY30						
VSUS15MEM	B30						
VSUS15PEX	K07						
VSUS15USB	AP23						
VSUS33	AT32						
VSUS33	AU32						

Table 3. VX800 Signal Ball List (Listed by Ball Number)

Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name
A01	HD62#	B31	MDQSA7+	D21	HTRDY#	F13	GND
A02	HD55#	B32	MDA51	D22	GND	F14	HD22#
A03	GND	B33	GND	D23	HA03#	F15	HD05#
A04	HD49#	B34	MDA42	D24	HA04#	F16	HD11#
A05	HD56#	B35	MDQSA5+	D25	HA14#	F17	GND
A06	HD53#	B36	MDA44	D26	GND	F18	INIT#
A07	GND	B37	GND	D27	NC	F19	NAP#
A08	HDSTB2P#	B38	MDA38	D28	NC	F20	HADS#
A09	HD37#	B39	MDQMA4	D29	GNDAHCK	F21	GND
A10	HD38#	B40	MDQSA4-	D30	MDA58	F22	NC
A11	GND	C01	HD60#	D31	GND	F23	HA13#
A12	HD26#	C02	HD51#	D32	MDQMA6	F24	HA11#
A13	HD24#	C03	HDSTB3P#	D33	MDQSA6+	F25	GND
A14	HD10#	C04	GND	D34	GND	F26	NC
A15	GND	C05	HD48#	D35	MDQMA5	F27	NC
A16	HDSTB0P#	C06	HD50#	D36	MDA41	F28	NC
A17	HD02#	C07	HD41#	D37	MDA33	F29	HCLK-
A18	IGNNE#	C08	GND	D38	GND	F30	GND
A19	GND	C09	HD35#	D39	MCLKOA3+	F31	MDA56
A20	HDRDY#	C10	HD39#	D40	MCLKOA3-	F32	GND
A21	HRS0#	C11	HDSTB1N#	E01	PEXCLK+	F33	GND
A22	HRS1#	C12	GND	E02	GND	F34	MDA48
A23	GND	C13	HD25#	E03	GNDA33PE1	F35	MDA36
A24	HA05#	C14	HD04#	E04	VCCA33PE1	F37	MODTA3
A25	HA10#	C15	HD03#	E06	HD57#	F38	VCC18MEM
A26	NC	C16	GND	E07	GND	F39	MCSA0#
A27	GND	C17	HD08#	E08	HD45#	F40	MCSA1#
A28	NC	C18	SLP#	E09	HD47#	G01	PEGTX1+
A29	HGTLCOMPN	C19	NMI	E10	HD34#	G02	GND
A30	MEMCOMP	C20	GND	E11	GND	G03	PEGRX0+
A31	MDQSA7-	C21	HDEFER#	E12	HD23#	G04	PEGTX0-
A32	GND	C22	HA09#	E13	HD20#	G05	GND
A33	MDA54	C23	HREQ2#	E14	HD12#	G06	GNDA33PE2
A34	MDA46	C24	GND	E15	GND	G07	VCCA33PE2
A35	GND	C25	HA15#	E16	HD06#	G08	VCC33PEX
A36	MDA45	C26	NC	E17	HD00#	G09	HD32#
A37	MDA39	C27	NC	E18	SMI#	G10	HD40#
A38	MDA35	C28	GND	E19	GND	G11	HD28#
A39	GND	C29	VCCA33HCK	E20	HBNR#	G12	GND
A40	MDQSA4+	C30	MDA62	E21	HDBSY#	G13	HD29#
B01	GND	C31	GND	E22	HREQ1#	G14	HD21#
B02	HDBI3#	C32	MDA55	E23	GND	G15	HDBI0#
B03	HDSTB3N#	C33	MDA50	E24	HA08#	G16	GND
B04	HD61#	C34	MDA47	E25	HA12#	G17	THRMTRIP# / GPIO7
B05	GND	C35	MDQSA5-	E26	NC	G18	STPCLK#
B06	HD63#	C36	GND	E27	GND	G19	HDPWR#
B07	HD33#	C37	MDA34	E28	NC	G20	GND
B08	HDSTB2N#	C38	MDA32	E29	HCLK+	G21	HRS2#
B09	GND	C39	MDA37	E30	MDA63	G22	NC
B10	HDBI2#	C40	GND	E31	MDQMA7	G23	HREQ0#
B11	HDSTB1P#	D01	HD59#	E32	MDA49	G24	GND
B12	HD31#	D02	GND	E33	MDQSA6-	G25	HA16#
B13	GND	D03	HD58#	E34	MDA43	G26	HA30#
B14	HD14#	D04	HD52#	E35	GND	G27	NC
B15	HD09#	D05	HD54#	E36	MDA40	G28	GND
B16	HDSTB0N#	D06	GND	E38	MODTA1	G30	MDA57
B17	GND	D07	HD44#	E39	MCSA3#	G31	MDA61
B18	FERR#	D08	HD42#	E40	VCC18MEM	G32	MDA53
B19	INTR	D09	HD36#	F01	PEXCLK-	G33	MDA52
B20	HBPRI#	D10	GND	F02	PEXREXT	G37	MODTA2
B21	GND	D11	HD18#	F03	PEXCOMP	G38	MCSA2#
B22	HHITM#	D12	HD30#	F04	PEGTX0+	G39	VCC18MEM
B23	HA06#	D13	HDBI1#	F05	VCC33PEX	G40	MSWEA#
B24	HA07#	D14	GND	F06	VCC33PEX	H01	PEGTX1-
B25	GND	D15	HD01#	F07	VCC33PEX	H02	PEGTX2+
B26	NC	D16	HD13#	F08	VCC33PEX	H03	PEGRX0-
B27	NC	D17	HD07#	F09	GND	H04	GND
B28	NC	D18	GND	F10	HD43#	H05	GND
B29	HGTLCOMPP	D19	A20M#	F11	HD27#	H06	PEGRX1+
B30	VSUS15MEM	D20	HHIT#	F12	HD16#	H07	VCC33PEX

Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name
H08	VCC33PEX	K03	PE0TX+	N40	MCLKOA4+	T20	GND
H09	HD46#	K04	PEGRX2-	P01	LCD1D0-	T21	VCC15
H10	GND	K05	PEGRX3+	P02	GNDLVDS	T22	GND
H11	HGTLVREF1	K06	GND	P03	VCC33LVDS	T23	VCC15
H12	HD19#	K07	VSUS15PEX	P04	VCC33LVDS	T24	GND
H13	HD17#	K08	VCC33PEX	P05	VCC33LVDS	T25	VCC15
H14	GND	K09	VCC33PEX	P14	GND	T26	GND
H15	HD15#	K20	VTT	P15	VCC33PEX	T27	VCC18MEM
H16	GCLK	K21	VTT	P16	GND	T32	VCC18MEM
H17	DPSLP#	K22	VTT	P17	VTT	T33	MDA28
H18	GND	K32	VCC18MEM	P18	GND	T34	GND
H19	CPURST#	K33	MCKEA0	P19	VTT	T35	MDA22
H20	HLOCK#	K34	VCC18MEM	P20	GND	T36	MDA19
H21	HBREQ0#	K35	MBAA2	P21	VTT	T37	MDA23
H22	GND	K36	MAA02	P22	GND	T38	GND
H23	HADSTB0N#	K37	MAA04	P23	VTT	T39	MDQSA2+
H24	HADSTB0P#	K38	VCC18MEM	P24	GND	T40	MDQSA2-
H25	HGTLVREF0	K39	MAA03	P25	VCC18MEM	U01	LCD1D2+
H26	GND	K40	MAA08	P26	GND	U02	GNDLVDS
H27	NC	L01	PE0RX+	P27	VCC18MEM	U03	LCD1CLK-
H28	VTT	L02	GND	P32	VCC18MEM	U04	VCCA33PLLLVDS2
H29	VTT	L03	PE0TX-	P33	GND	U05	GNDALVDS
H30	MDA59	L04	GND	P34	MDA27	U06	GNDLVDS
H31	GND	L05	PEGRX3-	P35	MDQSA3-	U14	VCC33PEX
H32	MDA60	L06	VCC33PEX	P36	MDQSA3+	U15	GND
H34	GND	L07	VCC33PEX	P37	GND	U16	VCC15
H36	MSRASA#	L08	VCC33PEX	P38	MCLKOA5-	U17	GND
H37	VCC18MEM	L09	VCC33PEX	P39	MCLKOA5+	U18	VCC15
H38	MAA13	L32	VCC18MEM	P40	MCLKOA4-	U19	GND
H39	MODTA0	L33	MCKEA2	R01	LCD1D0+	U20	VCC15
H40	MSCASA#	L34	VCC18MEM	R02	LCD1D1-	U21	GND
J01	PEGTX3+	L35	MCKEA3	R03	GNDLVDS	U22	VCC15
J02	PEGTX2-	L36	MAA09	R04	VCC33LVDS	U23	GND
J03	GND	L37	MAA01	R05	VCC33LVDS	U24	VCC15
J04	PEGRX2+	L38	VCC18MEM	R06	GNDLVDS	U25	GND
J05	GND	L39	MAA05	R14	VCC33PEX	U26	VCC18MEM
J06	PEGRX1-	L40	MAA11	R15	GND	U27	GND
J07	VCC33PEX	M01	PE0RX-	R16	VTT	U32	VCC18MEM
J08	VCC33PEX	M02	PE1TX+	R17	GND	U33	MEMVREF
J09	VCC33PEX	M03	GND	R18	VTT	U34	GND
J10	VTT	M04	VCC33PEX	R19	GND	U36	MDA17
J11	VTT	M05	VCC33PEX	R20	VTT	U37	MDA16
J12	VTT	M06	VCC33PEX	R21	GND	U38	MDA21
J13	VTT	M07	VCC33PEX	R22	VTT	U39	GND
J14	VTT	M08	VCC33PEX	R23	GND	U40	MDA20
J15	VTT	M09	VCC33PEX	R24	VCC18MEM	V01	LCD1D3-
J16	VTT	M32	VCC18MEM	R25	GND	V02	GNDLVDS
J17	VTT	M34	NC	R26	VCC18MEM	V03	LCD1CLK+
J18	VTT	M35	MCKEA1	R27	GND	V04	VCCA33LVDS
J19	VTT	M36	VCC18MEM	R32	VCC18MEM	V05	GNDA33PLLLVDS2
J20	TP1	M38	MAA12	R33	MDA31	V06	GNDLVDS
J21	TP2	M39	MAA07	R34	MDA25	V14	GND
J22	TP3	M40	VCC18MEM	R35	MDA24	V15	VCC33LVDS
J23	VTT	N01	GND	R36	GND	V16	GND
J24	VTT	N02	PE1TX-	R37	MDA29	V17	VCC15
J25	BISTIN	N03	PE1RX+	R38	MDA18	V18	GND
J26	DFTIN	N04	PE1RX-	R39	MDQMA2	V19	VCC15
J27	TESTIN	N05	VCC33PEX	R40	GND	V20	GND
J30	VCC18MEM	N06	VCC33PEX	T01	LCD1D2-	V21	VCC15
J31	VCC18MEM	N07	VCC33PEX	T02	LCD1D1+	V22	GND
J32	VCC18MEM	N08	VCC33PEX	T03	GNDLVDS	V23	VCC15
J34	MBAA0	N09	VCC33PEX	T04	VCCA33PLLLVDS1	V24	GND
J35	MAA06	N32	VCC18MEM	T05	GNDA33PLLLVDS1	V25	VCC15
J36	VCC18MEM	N33	MDA30	T06	GNDLVDS	V26	GND
J37	MBAA1	N34	MDA26	T14	GND	V27	VCC18MEM
J38	MAA00	N35	GND	T15	VCC33PEX	V32	VCC18MEM
J39	MAA10	N36	MDQMA3	T16	GND	V33	MDA15
J40	VCC18MEM	N37	MCLKOA1+	T17	VCC15	V34	MDA10
K01	PEGTX3-	N38	MCLKOA1-	T18	GND	V35	MDA09
K02	GND	N39	GND	T19	VCC15	V36	GND

Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name
V37	GND	AA16	VCC15	AC26	VCC18MEM	AF01	CRTAR
V38	MDQMA1	AA17	GND	AC27	GND	AF02	CRTAG
V39	MCLKOA2-	AA18	VCC15	AC32	VCC18MEM	AF03	GNDA33DAC3
V40	MCLKOA2+	AA19	GND	AC33	MDB07	AF04	VCCA33PLL2
W01	LCD1D3+	AA20	VCC15	AC34	MDB00	AF05	VCCA33PLL1
W02	LCD0D3+	AA21	GND	AC35	MDB05	AF06	GNDA33PLL1
W03	GNDLVDS	AA22	VCC15	AC36	GND	AF07	GNDA33PLL2
W04	GNDLVDS	AA23	GND	AC37	MDB04	AF08	XIN
W05	GNDLVDS	AA24	VCC15	AC38	MDQMB0	AF14	GND
W14	VCC33LVDS	AA25	GND	AC39	MDB03	AF15	VCC33
W15	GND	AA26	VCC18MEM	AC40	GND	AF16	GND
W16	VCC15	AA27	GND	AD01	NC	AF17	VCC33
W17	GND	AA32	VCC18MEM	AD02	LCD0D0-	AF18	GND
W18	VCC15	AA33	MDA03	AD03	DVP1SPCLK	AF19	VCC33
W19	GND	AA34	MDA06	AD04	DVP1SPD	AF20	GND
W20	VCC15	AA35	GND	AD05	CRTHSYNC	AF21	VCC33
W21	GND	AA36	MDA05	AD06	CRTVSYNC	AF22	GND
W22	VCC15	AA37	MCLKOA0+	AD14	GND	AF23	VSUS33USB
W23	GND	AA38	MCLKOA0-	AD15	VCC33	AF24	GNDUSB
W24	VCC15	AA39	GND	AD16	GND	AF25	VCCA15SATA
W25	GND	AA40	MDQMA0	AD17	VCC15	AF26	GNDA15SATA
W26	VCC18MEM	AB01	LCD0D1+	AD18	GND	AF27	VCCCR
W27	GND	AB02	GNDLVDS	AD19	VCC15	AF32	VCC18MEM
W32	VCC18MEM	AB03	LCD0D2-	AD20	GND	AF33	GND
W33	GND	AB04	GNDLVDS	AD21	VCC15	AF34	MDB23
W34	MDA11	AB05	LVDSENVDDA	AD22	GND	AF35	MDB16
W35	MDA13	AB06	NC	AD23	VCC15	AF36	MDB18
W36	MDA12	AB07	LVDSENVBLDB	AD24	GND	AF37	GND
W37	MDA08	AB14	GND	AD25	VCC15	AF38	MDB19
W38	MDQSA1-	AB15	VCC15	AD26	GND	AF39	MDQSB2
W39	MDQSA1+	AB16	GND	AD27	VCC18MEM	AF40	MDQMB2
W40	GND	AB17	VCC15	AD32	VCC18MEM	AG01	VCCA33DAC1
Y01	LCD0CLK+	AB18	GND	AD33	MDB08	AG02	VCCA33DAC2
Y02	LCD0D3-	AB19	VCC15	AD34	GND	AG03	VCCA33PLL3
Y03	GNDLVDS	AB20	GND	AD35	MDB09	AG04	DISPCLKO1 / VIDEO_GPIO5
Y04	GNDLVDS	AB21	VCC15	AD36	MDB15	AG05	DISPCLKI1 / VIDEO_GPIO4
Y05	GNDLVDS	AB22	GND	AD37	MDB13	AG06	DVP1CLK
Y06	NC	AB23	VCC15	AD38	GND	AG07	DVP1VS / IRRX
Y14	GND	AB24	GND	AD39	MDB06	AG08	DVP1D04 / DTR2
Y15	VCC15	AB25	VCC15	AD40	MDB01	AG09	VCC33
Y16	GND	AB26	GND	AE01	CRTAB	AG14	VCC33
Y17	VCC15	AB27	VCC18MEM	AE02	RSET	AG15	GND
Y18	GND	AB32	VCC18MEM	AE03	GNDA33DAC2	AG16	VCC33
Y19	VCC15	AB33	GND	AE04	GNDA33DAC1	AG17	GND
Y20	GND	AB34	MDA00	AE05	CRTSPCLK	AG18	VCC33
Y21	VCC15	AB35	MDA01	AE06	CRTSPD	AG19	GND
Y22	GND	AB36	MDB02	AE07	GNDA33PLL3	AG20	VCC33
Y23	VCC15	AB37	GND	AE14	VCC33	AG21	GND
Y24	GND	AB38	MDQSB0	AE15	GND	AG22	VSUS33USB
Y25	VCC15	AB39	MCLKOB+	AE16	VCC15	AG23	GNDUSB
Y26	GND	AB40	MCLKOB-	AE17	GND	AG24	VCCA15SATA
Y27	VCC18MEM	AC01	LCD0D1-	AE18	VCC15	AG25	GNDA15SATA
Y32	VCC18MEM	AC02	LCD0D0+	AE19	GND	AG26	VSUS15
Y33	MDA14	AC03	GNDLVDS	AE20	VCC15	AG27	GND
Y34	MDA02	AC04	LVDSENVBLDA	AE21	GND	AG32	VCC18MEM
Y35	GND	AC05	GNDLVDS	AE22	VCC15	AG33	MDB21
Y36	MDA07	AC06	GNDLVDS	AE23	GND	AG34	MDB20
Y37	MDA04	AC07	GNDLVDS	AE24	VCC15	AG35	MDB17
Y38	GND	AC14	VCC15	AE25	GND	AG36	GND
Y39	MDQSA0+	AC15	GND	AE26	VCCSD0	AG37	MDB22
Y40	MDQSA0-	AC16	VCC15	AE27	VCCSD1	AG38	MDB26
AA01	LCD0CLK-	AC17	GND	AE32	VCC18MEM	AG39	MDB31
AA02	GNDLVDS	AC18	VCC15	AE33	MDB11	AG40	GND
AA03	LCD0D2+	AC19	GND	AE34	MDB12	AH01	DISPCLKO0 / VIDEO_GPIO3
AA04	GNDLVDS	AC20	VCC15	AE35	GND	AH02	DVP1DE / IRRX2 / ITMOFF
AA05	LVDSENVDDB	AC21	GND	AE36	MDB14	AH03	DVP1D09 / DCD1
AA06	NC	AC22	VCC15	AE37	MDQMB1	AH04	DVP1D10 / SOUT1
AA07	BLTCK	AC23	GND	AE38	MDB10	AH05	DVP1D07 / CTS2
AA14	VCC15	AC24	VCC15	AE39	GND	AH06	DVP1D05 / DSR2
AA15	GND	AC25	GND	AE40	MDQSB1	AH07	DVP1TVCLKR

Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name
AH08	DVP1D02 / SOUT2	AM01	VCPD06 / RTS1 / PTS0D6	AP15	SYSIDLE / GPO10
AH09	VCC33	AM02	VCPD05 / DSR1 / PTS0D5	AP17	VSUS33USB
AH33	VCC18MEM	AM03	VCPCLK / DSR2 / PTS0CLK	AP18	VSUS33USB
AH34	GND	AM04	VCPD03 / SIN1/ PTS0D3	AP19	VSUS33USB
AH35	MDB28	AM05	VCPD08 / SIN2 / PTS0ERR	AP20	VSUS33USB
AH36	MDB25	AM06	VCPD12 / IRTX / STS1ERR	AP21	VSUS33USB
AH37	MDQSB3	AM07	VCPD15 / DTR2 / STS1D	AP22	VSUS33USB
AH38	GND	AM08	VCPD14 / IRRX2 / ITMOFF	AP23	VSUS15USB
AH39	MDB24	AM09	INTC#	AP24	VCCA15SATA
AH40	MDB29	AM10	PDA2	AP25	VCCA15SATA
AJ01	DISPCLKI0 / VIDEO_GPIO2	AM11	GND	AP26	VCCA33SATA
AJ02	IRSCLK	AM12	GND	AP27	VCCA33SATA
AJ03	DVP1D12 / DTR1	AM13	AZBITCLK	AP28	GNDAPLLSATA
AJ04	DVP1D11 / SIN1	AM14	SPIDO / GPO1	AP30	SUSB# / GPO8
AJ05	DVP1D15 / CTS1	AM15	CLKRUN#	AP31	SUSC# / GPO9
AJ06	DVP1D06 / RTS2	AM24	VCCA15SATA	AP32	SDIO0PSEL
AJ07	DVP1D03 / SIN2	AM25	VCCA15SATA	AP33	AZSDIN0
AJ08	DVP1HS / IRTX	AM26	GNDA33SATA	AP36	MAB10
AJ09	VCC33	AM27	GNDA33SATA	AP37	MBAB1
AJ33	VCC18MEM	AM28	SREXT	AP39	MAB01
AJ35	GND	AM33	VCC18MEM	AP40	VCC18MEM
AJ36	MDB27	AM36	MAB03	AR01	REQ1#
AJ37	MDB30	AM37	MAB05	AR02	GNT0#
AJ38	GND	AM38	MAB02	AR03	REQ0#
AJ39	MDQMB3	AM39	VCC18MEM	AR04	AD12
AK01	VCPD02 / SOUT1 / PTS0D2	AM40	MAB04	AR05	AD09
AK02	VCPD00 / RI1 / PTS0D0	AN01	VCPD07 / CTS1 / PTS0D7	AR06	AD03
AK03	DVP1D14 / RTS1	AN02	INTA#	AR07	AD01
AK04	DVP1D13 / DSR1	AN03	PCIDREQ# / GPIO8	AR08	PDD01
AK05	DVP1TVFLD	AN04	PCIDGNT# / GPIO9	AR09	PDD15
AK06	DVP1D08 / RI1	AN05	CBE1#	AR10	PDIOW#
AK07	DVP1D01 / DCD2	AN06	AD14	AR11	IRQ15
AK08	DVP1D00 / RI2	AN07	AD10	AR12	LPCAD3
AK09	TP6	AN08	AD02	AR13	LPCDRQ1#
AK11	VCC33	AN09	PDD13	AR14	C4PSTOP# / GPO6
AK12	VCC33	AN10	PDD14	AR15	SPKR / GPO7 / SATALED1#
AK13	VCC33	AN11	PDA1	AR16	PCICLK
AK14	VCC33	AN12	PDCS1#	AR17	VSUS33USB
AK15	VCC33	AN13	SPISS0# / GPO3	AR18	VCCA33PLLUSB
AK16	VCC33	AN14	SPIDI / GPI0	AR19	VCCA15PLLUSB
AK33	VCC18MEM	AN15	THRM# / GPI9	AR20	VSUS33USB
AK34	MAB12	AN24	VCCA15SATA	AR21	VSUS33USB
AK35	MAB07	AN25	VCCA15SATA	AR22	VSUS33USB
AK36	VCC18MEM	AN26	GNDA33SATA	AR23	USBREXT
AK37	MAB00	AN27	GNDA33SATA	AR24	VCCA15SATA
AK38	MCSB#	AN28	CLKI25M	AR25	VCCA33SATA
AK39	MODTB	AN30	TP8	AR26	VCCA33SATA
AK40	VCC18MEM	AN31	TP7	AR27	SATAR50COMP
AL01	VCPD04 / DTR1 / PTS0D4	AN32	AZSDIN2	AR28	VCCA33PLLSATA
AL02	VCPVS / RTS2 / PTS0SYNC	AN33	AZSDIN1	AR30	EXTSMI# / GPI5
AL03	VCPHS / CTS2 / PTS0VLD	AN35	MAB11	AR31	PWRBTN#
AL04	VCPD01 / DCD1 / PTS0D1	AN36	VCC18MEM	AR32	BATLOW# / GPI4
AL05	VCPD09 / SOUT2 / STSLVLD	AN37	VCC18MEM	AR33	KBDT / KBC_CPURST# / GPIO4
AL06	VCPD11 / RI2 / STS1CLK	AN38	MAB08	AR34	KBCK / A20GATE / GPIO5
AL07	VCPD10 / DCD2 / STS1SYNC	AN39	MAB06	AR38	SDIO0D2
AL08	VCPD13 / IRRX	AN40	MCKEB	AR39	SDIO0D3
AL10	PDIOR#	AP01	INTB#	AR40	SDIO0CMD#
AL11	PDCS3#	AP02	INTD#	AT01	AD30
AL12	TP5	AP03	GNT1#	AT02	AD31
AL13	AZSYNC	AP04	AD21	AT03	AD29
AL14	AZSDOUT	AP05	AD13	AT04	TRDY#
AL15	TP4	AP06	AD11	AT05	DEVSEL#
AL33	VCC18MEM	AP07	AD08	AT06	CBE0#
AL34	VCC18MEM	AP08	AD00	AT07	AD06
AL35	MAB09	AP09	PDD02	AT08	PDDREQ
AL36	MSWEB#	AP10	GND	AT09	GND
AL37	MBAB0	AP11	GND	AT10	GND
AL38	VCC18MEM	AP12	PDA0	AT11	PDIORDY
AL39	MSRASB#	AP13	SPISS1# / GPO2	AT12	TCSEN#
AL40	MSCASB#	AP14	GPIO13	AT13	GPIO10 / PCIERST0#

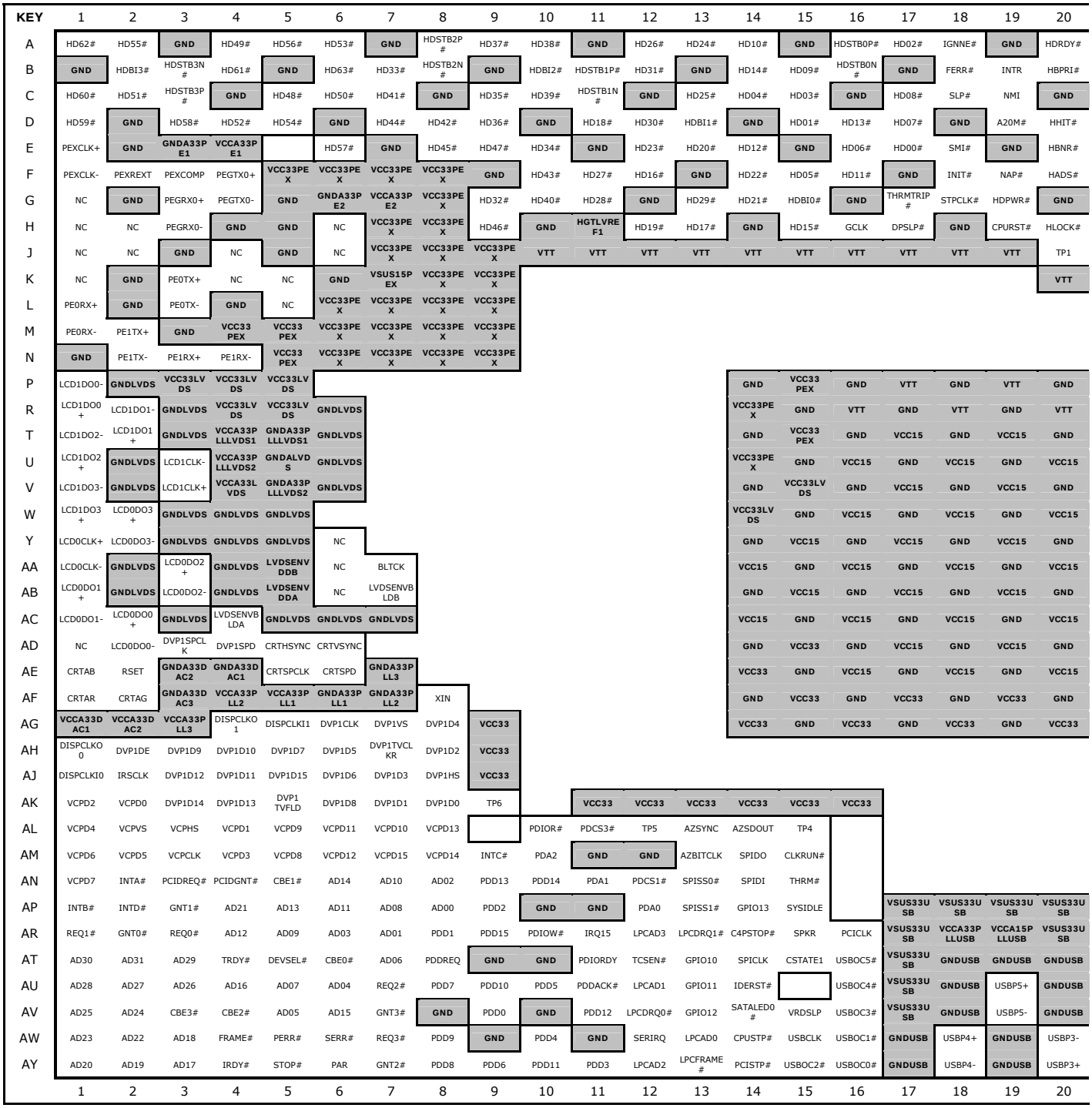
Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name
AT14	SPICLK / GPIO6	AV05	AD05	AW35	SDIO0POFF
AT15	CSTATE1 / GPO5	AV06	AD15	AW36	CR_D4 / SD_D4
AT16	USBOC5#	AV07	GNT3#	AW37	CR_D0 / SD_D0
AT17	VSUS33USB	AV08	GND	AW38	RSVD2
AT18	GNDUSB	AV09	PDD00	AW39	CR_D6 / SD_D6
AT19	GNDUSB	AV10	GND	AW40	SDIO1WPD#
AT20	GNDUSB	AV11	PDD12	AY01	AD20
AT21	GNDUSB	AV12	LPCDRQ0#	AY02	AD19
AT22	VSUS33USB	AV13	GPIO12	AY03	AD17
AT23	GNDUSB	AV14	SATALED0# / GPO4	AY04	IRDY#
AT24	VCCA15SATA	AV15	VRDSLP	AY05	STOP#
AT25	VCCA33SATA	AV16	USBOC3#	AY06	PAR
AT26	GNDA15SATA	AV17	VSUS33USB	AY07	GNT2#
AT27	GNDA15SATA	AV18	GNDUSB	AY08	PDD08
AT28	GNDA15SATA	AV19	USBP5-	AY09	PDD06
AT29	RING# / CRPWREN# / GPI8	AV20	GNDUSB	AY10	PDD11
AT30	PWRGD	AV21	USBP1+	AY11	PDD03
AT31	PME#	AV22	GNDUSB	AY12	LPCAD2
AT32	VSUS33	AV23	USBP0+	AY13	LPCFRAME#
AT33	SMBDT1	AV24	GNDUSB	AY14	PCISTP#
AT34	AZRST#	AV25	GNDA15SATA	AY15	USBOC2#
AT35	CRSD_WPD#	AV26	SRX1+	AY16	USBOC0#
AT36	SDIO0CD#	AV27	GNDA15SATA	AY17	GNDUSB
AT37	SDIO0WPD#	AV28	STX0+	AY18	USBP4-
AT38	SDIO0CLK	AV29	GNDA15SATA	AY19	GNDUSB
AT39	SDIO0D0	AV30	VBAT	AY20	USBP3+
AT40	SDIO0D1	AV31	WAKE# / GPI2	AY21	GNDUSB
AU01	AD28	AV32	VSUS33	AY22	USBP2+
AU02	AD27	AV33	MSCK / IRQ1	AY23	GNDUSB
AU03	AD26	AV34	SMBCK1	AY24	GNDA15SATA
AU04	AD16	AV35	SDIO1POFF	AY25	STX1+
AU05	AD07	AV36	RSVD1	AY26	GNDA15SATA
AU06	AD04	AV37	CRSD_CMD#	AY27	SRX0-
AU07	REQ2#	AV38	SDIO1CD#	AY28	GNDA15SATA
AU08	PDD07	AV39	SDIO1D0	AY29	RTCXI
AU09	PDD10	AV40	SDIO1CLK	AY30	VSUS15
AU10	PDD05	AW01	AD23	AY31	SUSA# / GPO0
AU11	PDDACK#	AW02	AD22	AY32	VSUS33
AU12	LPCAD1	AW03	AD18	AY33	PCIRST0#
AU13	GPIO11 / PCIERST1#	AW04	FRAME#	AY34	SMBCK2 / GPIO1
AU14	IDERST#	AW05	PERR#	AY35	SDIO1PSEL
AU16	USBOC4#	AW06	SERR#	AY36	CR_D5 / SD_D5
AU17	VSUS33USB	AW07	REQ3#	AY37	CR_CLK / SD_CLK
AU18	GNDUSB	AW08	PDD09	AY38	CR_D2 / SD_D2
AU19	USBP5+	AW09	GND	AY39	CR_D3 / SD_D3
AU20	GNDUSB	AW10	PDD04	AY40	CR_D7 / SD_D7
AU21	USBP1-	AW11	GND		
AU22	GNDUSB	AW12	SERIRQ		
AU23	USBP0-	AW13	LPCAD0		
AU24	GNDUSB	AW14	CPUSTP#		
AU25	GNDA15SATA	AW15	USBCLK		
AU26	SRX1-	AW16	USBOC1#		
AU27	GNDA15SATA	AW17	GNDUSB		
AU28	STX0-	AW18	USBP4+		
AU29	GNDA15SATA	AW19	GNDUSB		
AU30	RSMRST#	AW20	USBP3-		
AU31	LID# / GPI7	AW21	GNDUSB		
AU32	VSUS33	AW22	USBP2-		
AU33	MSDT / IRQ12	AW23	GNDUSB		
AU34	SMBALRT#	AW24	GNDA15SATA		
AU35	CRSD_CD#	AW25	STX1-		
AU36	CR_D1 / SD_D1	AW26	GNDA15SATA		
AU37	SDIO1D1	AW27	SRX0+		
AU38	SDIO1CMD#	AW28	GNDA15SATA		
AU39	SDIO1D3	AW29	RTCXO		
AU40	SDIO1D2	AW30	GPI1		
AV01	AD25	AW31	INTRUDER# / GPI6		
AV02	AD24	AW32	VSUS33		
AV03	CBE3#	AW33	PCIRST1#		
AV04	CBE2#	AW34	SMBDT2 / GPIO0		

Table 4. VX800 Power / Ground Ball List

Ball Name	Ball Numbers
GND	A03, A07, A11, A15, A19, A23, A27, A32, A35, A39, B01, B05, B09, B13, B17, B21, B25, B33, B37, C04, C08, C12, C16, C20, C24, C28, C31, C36, C40, D02, D06, D10, D14, D18, D22, D26, D31, D34, D38, E02, E07, E11, E15, E19, E23, E27, E35, F09, F13, F17, F21, F25, F30, F32, F33, G02, G05, G12, G16, G20, G24, G28, H04, H05, H10, H14, H18, H22, H26, H31, H34, J03, J05, K02, K06, L02, L04, M03, N01, N35, N39, P14, P16, P18, P20, P22, P24, P26, P33, P37, R15, R17, R19, R21, R23, R25, R27, R36, R40, T14, T16, T18, T20, T22, T24, T26, T34, T38, U15, U17, U19, U21, U23, U25, U27, U34, U39, V14, V16, V18, V20, V22, V24, V26, V36, V37, W15, W17, W19, W21, W23, W25, W27, W33, W40, Y14, Y16, Y18, Y20, Y22, Y24, Y26, Y35, Y38, AA15, AA17, AA19, AA21, AA23, AA25, AA27, AA35, AA39, AB14, AB16, AB18, AB20, AB22, AB24, AB26, AB33, AB37, AC15, AC17, AC19, AC21, AC23, AC25, AC27, AC36, AC40, AD14, AD16, AD18, AD20, AD22, AD24, AD26, AD34, AD38, AE15, AE17, AE19, AE21, AE23, AE25, AE35, AE39, AF14, AF16, AF18, AF20, AF22, AF33, AF37, AG15, AG17, AG19, AG21, AG27, AG36, AG40, AH34, AH38, AJ35, AJ38, AM11, AM12, AP10, AP11, AT09, AT10, AV08, AV10, AW09, AW11
GNDA33PE[2:1]	G06, E03
GNDA33DAC[3:1]	AF03, AE03, AE04
GNDLVDS	P02, R03, R06, T03, T06, U02, U06, V02, V06, W03, W04, W05, Y03, Y04, Y05, AA02, AA04, AB02, AB04, AC03, AC05, AC06, AC07
GNDALVDS	U05
GNDA33PLLLVDS[2:1]	V05, T05
GNDA15SATA	AF26, AG25, AT26, AT27, AT28, AU25, AU27, AU29, AV25, AV27, AV29, AW24, AW26, AW28, AY24, AY26, AY28
GNDA33SATA	AM26, AM27, AN26, AN27
GNDAPLLSATA	AP28
GNDA33PLL[3:1]	AE07, AF07, AF06
GNDAHCK	D29
GNDUSB	AF24, AG23, AT18, AT19, AT20, AT21, AT23, AU18, AU20, AU22, AU24, AV18, AV20, AV22, AV24, AW17, AW19, AW21, AW23, AY17, AY19, AY21, AY23
VBAT	AV30
VCC15	T17, T19, T21, T23, T25, U16, U18, U20, U22, U24, V17, V19, V21, V23, V25, W16, W18, W20, W22, W24, Y15, Y17, Y19, Y21, Y23, Y25, AA14, AA16, AA18, AA20, AA22, AA24, AB15, AB17, AB19, AB21, AB23, AB25, AC14, AC16, AC18, AC20, AC22, AC24, AD17, AD19, AD21, AD23, AD25, AE16, AE18, AE20, AE22, AE24
VCC33	AD15, AE14, AF15, AF17, AF19, AF21, AG09, AG14, AG16, AG18, AG20, AH09, AJ09, AK11, AK12, AK13, AK14, AK15, AK16
VCC18MEM	E40, F38, G39, H37, J30, J31, J32, J36, J40, K32, K34, K38, L32, L34, L38, M32, M36, M40, N32, P25, P27, P32, R24, R26, R32, T27, T32, U26, U32, V27, V32, W26, W32, Y27, Y32, AA26, AA32, AB27, AB32, AC26, AC32, AD27, AD32, AE32, AF32, AG32, AH33, AJ33, AK33, AK36, AK40, AL33, AL34, AL38, AM33, AM39, AN36, AN37, AP40
VCC33PEX	F05, F06, F07, F08, G08, H07, H08, J07, J08, J09, K08, K09, L06, L07, L08, L09, M04, M05, M06, M07, M08, M09, N05, N06, N07, N08, N09, P15, R14, T15, U14
VCCCR	AF27
VCCSD[1:0]	AE27, AE26
VCC33LVDS	P03, P04, P05, R04, R05, V15, W14
VCCA33PE[2:1]	G07, E04
VCCA33DAC[2:1]	AG02, AG01
VCCA33LVDS	V04
VCCA33PLLLVDS[2:1]	U04, T04
VCCA15SATA	AF25, AG24, AM24, AM25, AN24, AN25, AP24, AP25, AR24, AT24
VCCA33SATA	AP26, AP27, AR25, AR26, AT25
VCCA33PLLSATA	AR28
VCCA15PLLUSB	AR19
VCCA33PLLUSB	AR18
VCCA33HCK	C29
VCCA33PLL[3:1]	AG03, AF04, AF05
VSUS15	AG26, AY30
VSUS15MEM	B30
VSUS15PEX	K07
VSUS15USB	AP23
VSUS33USB	AF23, AG22, AP17, AP18, AP19, AP20, AP21, AP22, AR17, AR20, AR21, AR22, AT17, AT22, AU17, AV17
VSUS33	AT32, AU32, AV32, AW32, AY32
VTT	H28, H29, J10, J11, J12, J13, J14, J15, J16, J17, J18, J19, J23, J24, K20, K21, K22, P17, P19, P21, P23, R16, R18, R20, R22

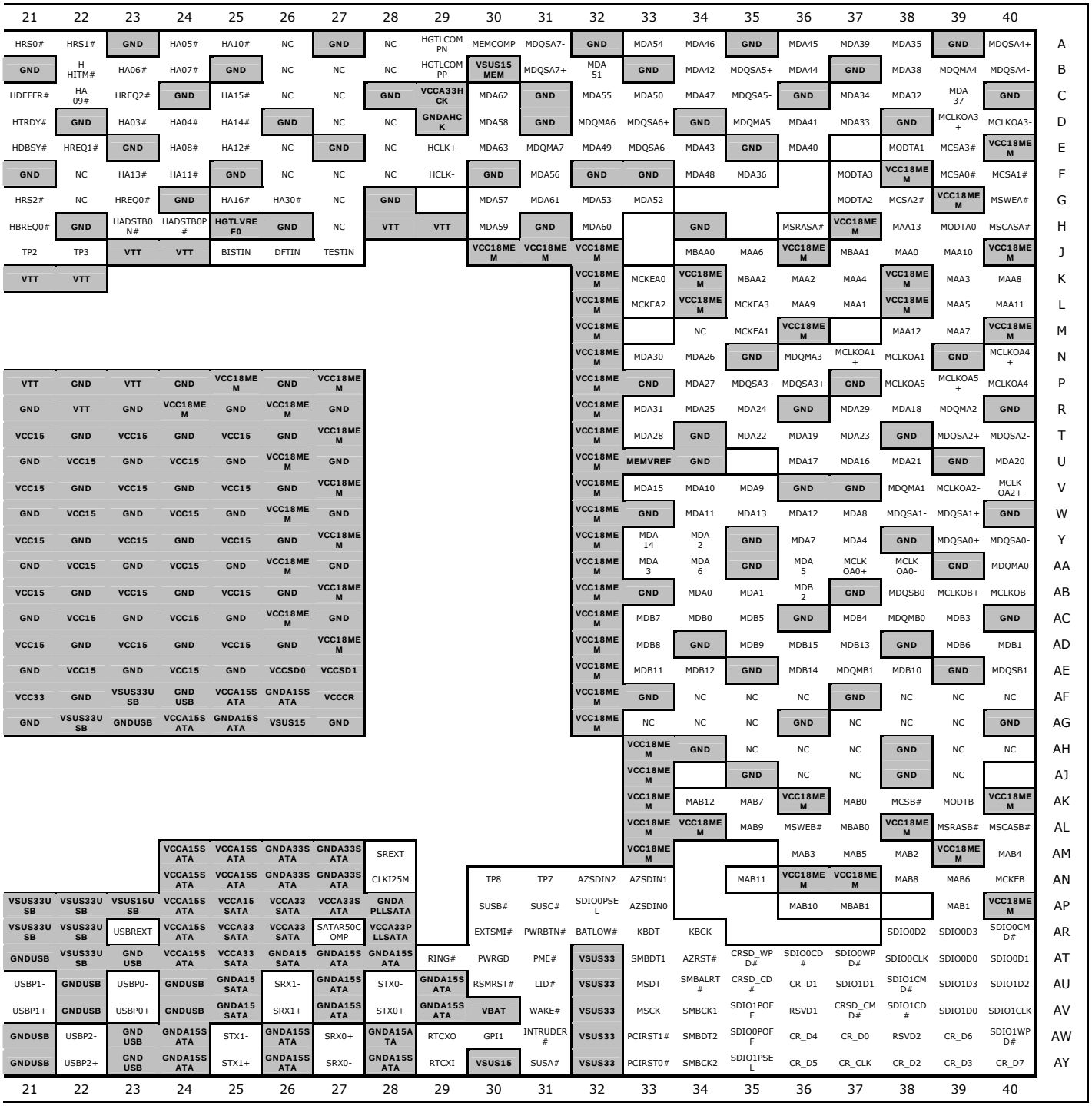
VX800UT Ball Map

Figure 3. VX800UT Ball Map – Left Side Top View



KEY	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	HD62#	HD55#	GND	HD49#	HD56#	HD53#	GND	HDSTB2P#	HD37#	HD38#	GND	HD26#	HD24#	HD10#	GND	HDSTB0P#	HD02#	IGNNE#	GND	HDRDY#
B	GND	HDBI3#	HDSTB3N#	HD61#	GND	HD63#	HD33#	HDSTB2N#	GND	HDBI2#	HDSTB1P#	HD31#	GND	HD14#	HD09#	HDSTB0N#	GND	FERR#	INTR	HBPRI#
C	HD60#	HD51#	HDSTB3P#	GND	HD48#	HD50#	HD41#	GND	HD35#	HD39#	HDSTB1N#	GND	HD25#	HD04#	HD03#	GND	HD08#	SLP#	NMI	GND
D	HD59#	GND	HD58#	HD52#	HD54#	GND	HD44#	HD42#	HD36#	GND	HD18#	HD30#	HDBI1#	GND	HD01#	HD13#	HD07#	GND	A20M#	HHIT#
E	PEXCLK+	GND	GNDA33PE1	VCCA33PE1		HD57#	GND	HD45#	HD47#	HD34#	GND	HD23#	HD20#	HD12#	GND	HD06#	HD00#	SMI#	GND	HBNR#
F	PEXCLK-	PEXREXT	PEXCOMP	PEGTX0+	VCC33PEX	VCC33PEX	VCC33PEX	VCC33PEX	GND	HD43#	HD27#	HD16#	GND	HD22#	HD05#	HD11#	GND	INIT#	NAP#	HADS#
G	NC	GND	PEGRX0+	PEGTX0-	GND	GNDA33PE2	VCCA33PE2	VCC33PEX	HD32#	HD40#	HD28#	GND	HD29#	HD21#	HDBI0#	GND	THRMTRIP#	STPCLK#	HDPWR#	GND
H	NC	NC	PEGRX0-	GND	GND	NC	VCC33PEX	VCC33PEX	HD46#	GND	HGTLVREF1	HD19#	HD17#	GND	HD15#	GCLK	DPSLP#	GND	CPURST#	HLOCK#
J	NC	NC	GND	NC	GND	NC	VCC33PEX	VCC33PEX	VCC33PEX	VTT	VTT	VTT	VTT	VTT	VTT	VTT	VTT	VTT	VTT	TP1
K	NC	GND	PE0TX+	NC	NC	GND	VSUS15PEX	VCC33PEX	VCC33PEX											VTT
L	PE0RX+	GND	PE0TX-	GND	NC	VCC33PEX	VCC33PEX	VCC33PEX	VCC33PEX											
M	PE0RX-	PE1TX+	GND	VCC33PEX	VCC33PEX	VCC33PEX	VCC33PEX	VCC33PEX	VCC33PEX											
N	GND	PE1TX-	PE1RX+	PE1RX-	VCC33PEX	VCC33PEX	VCC33PEX	VCC33PEX	VCC33PEX											
P	LCD1DO0-	GNDLVDS	VCC33LVDS	VCC33LVDS	VCC33LVDS															
R	LCD1DO0+	LCD1DO1-	GNDLVDS	VCC33LVDS	VCC33LVDS	GNDLVDS														
T	LCD1DO2-	LCD1DO1+	GNDLVDS	VCCA33PLLLVDS1	GNDA33PLLLVDS1	GNDLVDS														
U	LCD1DO2+	GNDLVDS	LCD1CLK-	VCCA33PLLLVDS2	GNDALVDS	GNDLVDS														
V	LCD1DO3-	GNDLVDS	LCD1CLK+	VCCA33LVDS	GNDA33PLLLVDS2	GNDLVDS														
W	LCD1DO3+	LCD0DO3+	GNDLVDS	GNDLVDS	GNDLVDS															
Y	LCD0CLK+	LCD0DO3-	GNDLVDS	GNDLVDS	GNDLVDS	NC														
AA	LCD0CLK-	GNDLVDS	LCD0DO2+	GNDLVDS	LVDSENVDDB	NC	BLTCK													
AB	LCD0DO1+	GNDLVDS	LCD0DO2-	GNDLVDS	LVDSENVDDA	NC	LVDSENVBLDB													
AC	LCD0DO1-	LCD0DO0+	GNDLVDS	LVDSENVBLDA	GNDLVDS	GNDLVDS	GNDLVDS													
AD	NC	LCD0DO0-	DVP1SPCLK	DVP1SPD	CRTHSYNC	CRTVSYNC														
AE	CRTAB	RSET	GNDA33DAC2	GNDA33DAC1	CRTSPCLK	CRTSPD	GNDA33PLL3													
AF	CRTAR	CRTAG	GNDA33DAC3	VCCA33PLL2	VCCA33PLL1	GNDA33PLL1	GNDA33PLL2	XIN												
AG	VCCA33DAC1	VCCA33DAC2	VCCA33PLL3	DISPCLKO1	DISPCLKI1	DVP1CLK	DVP1VS	DVP1D4	VCC33											
AH	DISPCLKO0	DVP1DE	DVP1D9	DVP1D10	DVP1D7	DVP1D5	DVP1TVCLKR	DVP1D2	VCC33											
AJ	DISPCLKI0	IRSCLK	DVP1D12	DVP1D11	DVP1D15	DVP1D6	DVP1D3	DVP1HS	VCC33											
AK	VCPD2	VCPD0	DVP1D14	DVP1D13	DVP1TVFLD	DVP1D8	DVP1D1	DVP1D0	TP6		VCC33	VCC33	VCC33	VCC33	VCC33	VCC33				
AL	VCPD4	VCPVS	VCPHS	VCPD1	VCPD9	VCPD11	VCPD10	VCPD13		PDIOR#	PDCS3#	TP5	AZSYNC	AZSDOUT	TP4					
AM	VCPD6	VCPD5	VCPCLK	VCPD3	VCPD8	VCPD12	VCPD15	VCPD14	INTC#	PDA2	GND	GND	AZBITCLK	SPIDO	CLKRUN#					
AN	VCPD7	INTA#	PCIDREQ#	PCIDGNT#	CBE1#	AD14	AD10	AD02	PDD13	PDD14	PDA1	PDCS1#	SPISS0#	SPIDI	THRM#					
AP	INTB#	INTD#	GNT1#	AD21	AD13	AD11	AD08	AD00	PDD2	GND	GND	PDA0	SPISS1#	GPIO13	SYSIDLE		VSUS33USB	VSUS33USB	VSUS33USB	VSUS33USB
AR	REQ1#	GNT0#	REQ0#	AD12	AD09	AD03	AD01	PDD1	PDD15	PDIOW#	IRQ15	LPCAD3	LPCDRQ1#	C4PSTOP#	SPKR	PCICLK	VSUS33USB	VCCA33PLLUSB	VCCA15PLLUSB	VSUS33USB
AT	AD30	AD31	AD29	TRDY#	DEVSEL#	CBE0#	AD06	PDDREQ	GND	GND	PDIORDY	TCSEN#	GPIO10	SPICLK	CSTATE1	USBOC5#	VSUS33USB	GNDUSB	GNDUSB	GNDUSB
AU	AD28	AD27	AD26	AD16	AD07	AD04	REQ2#	PDD7	PDD10	PDD5	PDDACK#	LPCAD1	GPIO11	IDERST#		USBOC4#	VSUS33USB	GNDUSB	USBP5+	GNDUSB
AV	AD25	AD24	CBE3#	CBE2#	AD05	AD15	GNT3#	GND	PDD0	GND	PDD12	LPCDRQ0#	GPIO12	SATALED0#	VRDSLP	USBOC3#	VSUS33USB	GNDUSB	USBP5-	GNDUSB
AW	AD23	AD22	AD18	FRAME#	PERR#	SERR#	REQ3#	PDD9	GND	PDD4	GND	SERIRQ	LPCAD0	CPUSTP#	USBCLK	USBOC1#	GNDUSB	USBP4+	GNDUSB	USBP3-
AY	AD20	AD19	AD17	IRDY#	STOP#	PAR	GNT2#	PDD8	PDD6	PDD11	PDD3	LPCAD2	LPCFRAME#	PCISTP#	USBOC2#	USBOC0#	GNDUSB	USBP4-	GNDUSB	USBP3+
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20

Figure 4. VX800UT Ball Map – Right Side Top View



21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	
HRS0#	HRS1#	GND	HA05#	HA10#	NC	GND	NC	HGTLCOMPN	MEMCOMP	MDQSA7-	GND	MDA54	MDA46	GND	MDA45	MDA39	MDA35	GND	MDQSA4+	A
GND	H HITM#	HA06#	HA07#	GND	NC	NC	NC	HGTLCOMPP	VSUS15MEM	MDQSA7+	MDA 51	GND	MDA42	MDQSA5+	MDA44	GND	MDA38	MDQMA4	MDQSA4-	B
HDEFER#	HA 09#	HREQ2#	GND	HA15#	NC	NC	GND	VCCA33HCK	MDA62	GND	MDA55	MDA50	MDA47	MDQSA5-	GND	MDA34	MDA32	MDA 37	GND	C
HTRDY#	GND	HA03#	HA04#	HA14#	GND	NC	NC	GNDAHCK	MDA58	GND	MDQMA6	MDQSA6+	GND	MDQMA5	MDA41	MDA33	GND	MCLKOA3+	MCLKOA3-	D
HDBSY#	HREQ1#	GND	HA08#	HA12#	NC	GND	NC	HCLK+	MDA63	MDQMA7	MDA49	MDQSA6-	MDA43	GND	MDA40		MODTA1	MCSA3#	VCC18MEM	E
GND	NC	HA13#	HA11#	GND	NC	NC	NC	HCLK-	GND	MDA56	GND	GND	MDA48	MDA36		MODTA3	VCC18MEM	MCSA0#	MCSA1#	F
HRS2#	NC	HREQ0#	GND	HA16#	HA30#	NC	GND		MDA57	MDA61	MDA53	MDA52				MODTA2	MCSA2#	VCC18MEM	MSWEA#	G
HBREQ0#	GND	HADSTB0N#	HADSTB0P#	HGTLVREF0	GND	NC	VTT	VTT	MDA59	GND	MDA60		GND		MSRASA#	VCC18MEM	MAA13	MODTA0	MSCASA#	H
TP2	TP3	VTT	VTT	BISTIN	DFTIN	TESTIN			VCC18MEM	VCC18MEM	VCC18MEM		MBAA0	MAA6	VCC18MEM	MBAA1	MAA0	MAA10	VCC18MEM	J
VTT	VTT										VCC18MEM	MCKEA0	VCC18MEM	MBAA2	MAA2	MAA4	VCC18MEM	MAA3	MAA8	K
											VCC18MEM	MCKEA2	VCC18MEM	MCKEA3	MAA9	MAA1	VCC18MEM	MAA5	MAA11	L
											VCC18MEM		NC	MCKEA1	VCC18MEM		MAA12	MAA7	VCC18MEM	M
											VCC18MEM	MDA30	MDA26	GND	MDQMA3	MCLKOA1+	MCLKOA1-	GND	MCLKOA4+	N
VTT	GND	VTT	GND	VCC18MEM	GND	VCC18MEM					VCC18MEM	GND	MDA27	MDQSA3-	MDQSA3+	GND	MCLKOA5-	MCLKOA5+	MCLKOA4-	P
GND	VTT	GND	VCC18MEM	GND	VCC18MEM	GND					VCC18MEM	MDA31	MDA25	MDA24	GND	MDA29	MDA18	MDQMA2	GND	R
VCC15	GND	VCC15	GND	VCC15	GND	VCC18MEM					VCC18MEM	MDA28	GND	MDA22	MDA19	MDA23	GND	MDQSA2+	MDQSA2-	T
GND	VCC15	GND	VCC15	GND	VCC18MEM	GND					VCC18MEM	MEMVREF	GND		MDA17	MDA16	MDA21	GND	MDA20	U
VCC15	GND	VCC15	GND	VCC15	GND	VCC18MEM					VCC18MEM	MDA15	MDA10	MDA9	GND	GND	MDQMA1	MCLKOA2-	MCLK OA2+	V
GND	VCC15	GND	VCC15	GND	VCC18MEM	GND					VCC18MEM	GND	MDA11	MDA13	MDA12	MDA8	MDQSA1-	MDQSA1+	GND	W
VCC15	GND	VCC15	GND	VCC15	GND	VCC18MEM					VCC18MEM	MDA 14	MDA 2	GND	MDA7	MDA4	GND	MDQSA0+	MDQSA0-	Y
GND	VCC15	GND	VCC15	GND	VCC18MEM	GND					VCC18MEM	MDA 3	MDA 6	GND	MDA 5	MCLK OA0+	MCLK OA0-	GND	MDQMA0	AA
VCC15	GND	VCC15	GND	VCC15	GND	VCC18MEM					VCC18MEM	GND	MDA0	MDA1	MDB 2	GND	MDQSB0	MCLKOB+	MCLKOB-	AB
GND	VCC15	GND	VCC15	GND	VCC18MEM	GND					VCC18MEM	MDB7	MDB0	MDB5	GND	MDB4	MDQMB0	MDB3	GND	AC
VCC15	GND	VCC15	GND	VCC15	GND	VCC18MEM					VCC18MEM	MDB8	GND	MDB9	MDB15	MDB13	GND	MDB6	MDB1	AD
GND	VCC15	GND	VCC15	GND	VCCSD0	VCCSD1					VCC18MEM	MDB11	MDB12	GND	MDB14	MDQMB1	MDB10	GND	MDQSB1	AE
VCC33	GND	VSUS33USB	GNDUSB	VCCA15SATA	GNDA15SATA	VCCCR					VCC18MEM	GND	NC	NC	NC	GND	NC	NC	NC	AF
GND	VSUS33USB	GNDUSB	VCCA15SATA	GNDA15SATA	VSUS15	GND					VCC18MEM	NC	NC	NC	GND	NC	NC	NC	GND	AG
												VCC18MEM	GND	NC	NC	NC	GND	NC	NC	AH
												VCC18MEM		GND	NC	NC	GND	NC		AJ
												VCC18MEM	MAB12	MAB7	VCC18MEM	MAB0	MCSB#	MODTB	VCC18MEM	AK
												VCC18MEM	VCC18MEM	MAB9	MSWEB#	MBAB0	VCC18MEM	MSRASB#	MSCASB#	AL
			VCCA15SATA	VCCA15SATA	GNDA33SATA	GNDA33SATA	SREXT					VCC18MEM			MAB3	MAB5	MAB2	VCC18MEM	MAB4	AM
			VCCA15SATA	VCCA15SATA	GNDA33SATA	GNDA33SATA	CLKI25M		TP8	TP7	AZSDIN2	AZSDIN1		MAB11	VCC18MEM	VCC18MEM	MAB8	MAB6	MCKEB	AN
VSUS33USB	VSUS33USB	VSUS15USB	VCCA15SATA	VCCA15SATA	VCCA33SATA	VCCA33SATA	GNDA PLLSATA		SUSB#	SUSC#	SDIO0PSEL	AZSDIN0			MAB10	MBAB1		MAB1	VCC18MEM	AP
VSUS33USB	VSUS33USB	USBREXT	VCCA15SATA	VCCA33SATA	VCCA33SATA	SATAR50COMP	VCCA33PLLSATA		EXTSMI#	PWRBTN#	BATLOW#	KBDT	KBCK				SDIO0D2	SDIO0D3	SDIO0CMD#	AR
GNDUSB	VSUS33USB	GND USB	VCCA15SATA	VCCA33SATA	GNDA15SATA	GNDA15SATA	GNDA15SATA	RING#	PWRGD	PME#	VSUS33	SMBDT1	AZRST#	CRSD_WPD#	SDIO0CD#	SDIO0WPD#	SDIO0CLK	SDIO0D0	SDIO0D1	AT
USBP1-	GNDUSB	USBP0-	GNDUSB	GNDA15SATA	SRX1-	GNDA15SATA	STX0-	GNDA15SATA	RSMRST#	LID#	VSUS33	MSDT	SMBALRT#	CRSD_CD#	CR_D1	SDIO1D1	SDIO1CMD#	SDIO1D3	SDIO1D2	AU
USBP1+	GNDUSB	USBP0+	GNDUSB	GNDA15SATA	SRX1+	GNDA15SATA	STX0+	GNDA15SATA	VBAT	WAKE#	VSUS33	MSCK	SMBCK1	SDIO1POFF	RSVD1	CRSD_CMD#	SDIO1CD#	SDIO1D0	SDIO1CLK	AV
GNDUSB	USBP2-	GND USB	GNDA15SATA	STX1-	GNDA15SATA	SRX0+	GNDA15ATA	RTCXO	GPI1	INTRUDER#	VSUS33	PCIRST1#	SMBDT2	SDIO0POFF	CR_D4	CR_D0	RSVD2	CR_D6	SDIO1WPD#	AW
GNDUSB	USBP2+	GND USB	GNDA15SATA	STX1+	GNDA15SATA	SRX0-	GNDA15SATA	RTCXI	VSUS15	SUSA#	VSUS33	PCIRST0#	SMBCK2	SDIO1PSEL	CR_D5	CR_CLK	CR_D2	CR_D3	CR_D7	AY
21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	

VX800UT Signal Ball List

Table 5. VX800UT Signal Ball List (Listed by Ball Name)

Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #
A20M#	D19	CRTVSYNC	AD06	GND	AC25	GND	D10
AD00	AP08	CSTATE1 / GPO5	AT15	GND	AC27	GND	D14
AD01	AR07	DEVSEL#	AT05	GND	AC36	GND	D18
AD02	AN08	DFTIN	J26	GND	AC40	GND	D22
AD03	AR06	DISPCLKI0 / VIDEO_GPIO2	AJ01	GND	AD14	GND	D26
AD04	AU06	DISPCLKI1 / VIDEO_GPIO4	AG05	GND	AD16	GND	D31
AD05	AV05	DISPCLKO0 / VIDEO_GPIO3	AH01	GND	AD18	GND	D34
AD06	AT07	DISPCLKO1 / VIDEO_GPIO5	AG04	GND	AD20	GND	D38
AD07	AU05	DPSLP#	H17	GND	AD22	GND	E02
AD08	AP07	DVP1CLK	AG06	GND	AD24	GND	E07
AD09	AR05	DVP1D00 / RI2	AK08	GND	AD26	GND	E11
AD10	AN07	DVP1D01 / DCD2	AK07	GND	AD34	GND	E15
AD11	AP06	DVP1D02 / SOUT2	AH08	GND	AD38	GND	E19
AD12	AR04	DVP1D03 / SIN2	AJ07	GND	AE15	GND	E23
AD13	AP05	DVP1D04 / DTR2	AG08	GND	AE17	GND	E27
AD14	AN06	DVP1D05 / DSR2	AH06	GND	AE19	GND	E35
AD15	AV06	DVP1D06 / RTS2	AJ06	GND	AE21	GND	F09
AD16	AU04	DVP1D07 / CTS2	AH05	GND	AE23	GND	F13
AD17	AY03	DVP1D08 / RI1	AK06	GND	AE25	GND	F17
AD18	AW03	DVP1D09 / DCD1	AH03	GND	AE35	GND	F21
AD19	AY02	DVP1D10 / SOUT1	AH04	GND	AE39	GND	F25
AD20	AY01	DVP1D11 / SIN1	AJ04	GND	AF14	GND	F30
AD21	AP04	DVP1D12 / DTR1	AJ03	GND	AF16	GND	F32
AD22	AW02	DVP1D13 / DSR1	AK04	GND	AF18	GND	F33
AD23	AW01	DVP1D14 / RTS1	AK03	GND	AF20	GND	G02
AD24	AV02	DVP1D15 / CTS1	AJ05	GND	AF22	GND	G05
AD25	AV01	DVP1DE / IRRX2 / ITMOFF	AH02	GND	AF33	GND	G12
AD26	AU03	DVP1HS / IRTX	AJ08	GND	AF37	GND	G16
AD27	AU02	DVP1SPCLK	AD03	GND	AG15	GND	G20
AD28	AU01	DVP1SPD	AD04	GND	AG17	GND	G24
AD29	AT03	DVP1TVCLKR	AH07	GND	AG19	GND	G28
AD30	AT01	DVP1TVFLD	AK05	GND	AG21	GND	H04
AD31	AT02	DVP1VS / IRRX	AG07	GND	AG27	GND	H05
AZBITCLK	AM13	EXTSMI# / GPI5	AR30	GND	AG36	GND	H10
AZRST#	AT34	FERR#	B18	GND	AG40	GND	H14
AZSDIN0	AP33	FRAME#	AW04	GND	AH34	GND	H18
AZSDIN1	AN33	GCLK	H16	GND	AH38	GND	H22
AZSDIN2	AN32	GND	A03	GND	AJ35	GND	H26
AZSDOUT	AL14	GND	A07	GND	AJ38	GND	H31
AZSYNC	AL13	GND	A11	GND	AM11	GND	H34
BATLOW# / GPI4	AR32	GND	A15	GND	AM12	GND	J03
BISTIN	J25	GND	A19	GND	AP10	GND	J05
BLTCK	AA07	GND	A23	GND	AP11	GND	K02
C4PSTOP# / GPO6	AR14	GND	A27	GND	AT09	GND	K06
CBE0#	AT06	GND	A32	GND	AT10	GND	L02
CBE1#	AN05	GND	A35	GND	AV08	GND	L04
CBE2#	AV04	GND	A39	GND	AV10	GND	M03
CBE3#	AV03	GND	AA15	GND	AW09	GND	N01
CLKI25M	AN28	GND	AA17	GND	AW11	GND	N35
CLKRUN#	AM15	GND	AA19	GND	B01	GND	N39
CPURST#	H19	GND	AA21	GND	B05	GND	P14
CPUSTP#	AW14	GND	AA23	GND	B09	GND	P16
CR_CLK / SD_CLK	AY37	GND	AA25	GND	B13	GND	P18
CR_D0 / SD_D0	AW37	GND	AA27	GND	B17	GND	P20
CR_D1 / SD_D1	AU36	GND	AA35	GND	B21	GND	P22
CR_D2 / SD_D2	AY38	GND	AA39	GND	B25	GND	P24
CR_D3 / SD_D3	AY39	GND	AB14	GND	B33	GND	P26
CR_D4 / SD_D4	AW36	GND	AB16	GND	B37	GND	P33
CR_D5 / SD_D5	AY36	GND	AB18	GND	C04	GND	P37
CR_D6 / SD_D6	AW39	GND	AB20	GND	C08	GND	R15
CR_D7 / SD_D7	AY40	GND	AB22	GND	C12	GND	R17
CRSD_CD#	AU35	GND	AB24	GND	C16	GND	R19
CRSD_CMD#	AV37	GND	AB26	GND	C20	GND	R21
CRSD_WPD#	AT35	GND	AB33	GND	C24	GND	R23
CRTAB	AE01	GND	AB37	GND	C28	GND	R25
CRTAG	AF02	GND	AC15	GND	C31	GND	R27
CRTAR	AF01	GND	AC17	GND	C36	GND	R36
CRTHSYNC	AD05	GND	AC19	GND	C40	GND	R40
CRTSPCLK	AE05	GND	AC21	GND	D02	GND	T14
CRTSPD	AE06	GND	AC23	GND	D06	GND	T16

Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #
GND	T18	GNDA33SATA	AM26	HA11#	F24	HD55#	A02
GND	T20	GNDA33SATA	AM27	HA12#	E25	HD56#	A05
GND	T22	GNDA33SATA	AN26	HA13#	F23	HD57#	E06
GND	T24	GNDA33SATA	AN27	HA14#	D25	HD58#	D03
GND	T26	GNDAHCK	D29	HA15#	C25	HD59#	D01
GND	T34	GNDALVDS	U05	HA16#	G25	HD60#	C01
GND	T38	GNDAPLLSATA	AP28	HA30#	G26	HD61#	B04
GND	U15	GNDLVDS	AA02	HADS#	F20	HD62#	A01
GND	U17	GNDLVDS	AA04	HADSTB0N#	H23	HD63#	B06
GND	U19	GNDLVDS	AB02	HADSTB0P#	H24	HDBI0#	G15
GND	U21	GNDLVDS	AB04	HBNR#	E20	HDBI1#	D13
GND	U23	GNDLVDS	AC03	HBPRI#	B20	HDBI2#	B10
GND	U25	GNDLVDS	AC05	HBREQ0#	H21	HDBI3#	B02
GND	U27	GNDLVDS	AC06	HCLK-	F29	HDBSY#	E21
GND	U34	GNDLVDS	AC07	HCLK+	E29	HDEFER#	C21
GND	U39	GNDLVDS	P02	HD00#	E17	HDPWR#	G19
GND	V14	GNDLVDS	R03	HD01#	D15	HDRDY#	A20
GND	V16	GNDLVDS	R06	HD02#	A17	HDSTB0N#	B16
GND	V18	GNDLVDS	T03	HD03#	C15	HDSTB0P#	A16
GND	V20	GNDLVDS	T06	HD04#	C14	HDSTB1N#	C11
GND	V22	GNDLVDS	U02	HD05#	F15	HDSTB1P#	B11
GND	V24	GNDLVDS	U06	HD06#	E16	HDSTB2N#	B08
GND	V26	GNDLVDS	V02	HD07#	D17	HDSTB2P#	A08
GND	V36	GNDLVDS	V06	HD08#	C17	HDSTB3N#	B03
GND	V37	GNDLVDS	W03	HD09#	B15	HDSTB3P#	C03
GND	W15	GNDLVDS	W04	HD10#	A14	HGTLCOMPN	A29
GND	W17	GNDLVDS	W05	HD11#	F16	HGTLCOMPP	B29
GND	W19	GNDLVDS	Y03	HD12#	E14	HGTLVREF0	H25
GND	W21	GNDLVDS	Y04	HD13#	D16	HGTLVREF1	H11
GND	W23	GNDLVDS	Y05	HD14#	B14	HHIT#	D20
GND	W25	GNDUSB	AF24	HD15#	H15	HHITM#	B22
GND	W27	GNDUSB	AG23	HD16#	F12	HLOCK#	H20
GND	W33	GNDUSB	AT18	HD17#	H13	HREQ0#	G23
GND	W40	GNDUSB	AT19	HD18#	D11	HREQ1#	E22
GND	Y14	GNDUSB	AT20	HD19#	H12	HREQ2#	C23
GND	Y16	GNDUSB	AT21	HD20#	E13	HRS0#	A21
GND	Y18	GNDUSB	AT23	HD21#	G14	HRS1#	A22
GND	Y20	GNDUSB	AU18	HD22#	F14	HRS2#	G21
GND	Y22	GNDUSB	AU20	HD23#	E12	HTRDY#	D21
GND	Y24	GNDUSB	AU22	HD24#	A13	IDERST#	AU14
GND	Y26	GNDUSB	AU24	HD25#	C13	IGNNE#	A18
GND	Y35	GNDUSB	AV18	HD26#	A12	INIT#	F18
GND	Y38	GNDUSB	AV20	HD27#	F11	INTA#	AN02
GNDA15SATA	AF26	GNDUSB	AV22	HD28#	G11	INTB#	AP01
GNDA15SATA	AG25	GNDUSB	AV24	HD29#	G13	INTC#	AM09
GNDA15SATA	AT26	GNDUSB	AW17	HD30#	D12	INTD#	AP02
GNDA15SATA	AT27	GNDUSB	AW19	HD31#	B12	INTR	B19
GNDA15SATA	AT28	GNDUSB	AW21	HD32#	G09	INTRUDER# / GPI6	AW31
GNDA15SATA	AU25	GNDUSB	AW23	HD33#	B07	IRDY#	AY04
GNDA15SATA	AU27	GNDUSB	AY17	HD34#	E10	IRQ15	AR11
GNDA15SATA	AU29	GNDUSB	AY19	HD35#	C09	IRSCLK	AJ02
GNDA15SATA	AV25	GNDUSB	AY21	HD36#	D09	KBCK / A20GATE / GPIO5	AR34
GNDA15SATA	AV27	GNDUSB	AY23	HD37#	A09	KBDT / KBC_CPURST# / GPIO4	AR33
GNDA15SATA	AV29	GNT0#	AR02	HD38#	A10	LCD0CLK- / TX2-	AA01
GNDA15SATA	AW24	GNT1#	AP03	HD39#	C10	LCD0CLK+ / TX2+	Y01
GNDA15SATA	AW26	GNT2#	AY07	HD40#	G10	LCD0D0- / TXC-	AD02
GNDA15SATA	AW28	GNT3#	AV07	HD41#	C07	LCD0D0+ / TXC+	AC02
GNDA15SATA	AY24	GPI1	AW30	HD42#	D08	LCD0D1- / TX0-	AC01
GNDA15SATA	AY26	GPIO10 / PCIERST0#	AT13	HD43#	F10	LCD0D1+ / TX0+	AB01
GNDA15SATA	AY28	GPIO11 / PCIERST1#	AU13	HD44#	D07	LCD0D2- / TX1-	AB03
GNDA33DAC1	AE04	GPIO12	AV13	HD45#	E08	LCD0D2+ / TX1+	AA03
GNDA33DAC2	AE03	GPIO13	AP14	HD46#	H09	LCD0D3-	Y02
GNDA33DAC3	AF03	HA03#	D23	HD47#	E09	LCD0D3+	W02
GNDA33PE1	E03	HA04#	D24	HD48#	C05	LCD1CLK-	U03
GNDA33PE2	G06	HA05#	A24	HD49#	A04	LCD1CLK+	V03
GNDA33PLL1	AF06	HA06#	B23	HD50#	C06	LCD1D0-	P01
GNDA33PLL2	AF07	HA07#	B24	HD51#	C02	LCD1D0+	R01
GNDA33PLL3	AE07	HA08#	E24	HD52#	D04	LCD1D1-	R02
GNDA33PLLLVDS1	T05	HA09#	C22	HD53#	A06	LCD1D1+	T02
GNDA33PLLLVDS2	V05	HA10#	A25	HD54#	D05	LCD1D2-	T01

Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #
LCD1D2+	U01	MCSB#	AK38	MDB05	AC35	NC	AG39
LCD1D3-	V01	MDA00	AB34	MDB06	AD39	NC	AF40
LCD1D3+	W01	MDA01	AB35	MDB07	AC33	NC	AJ39
LID# / GPI7	AU31	MDA02	Y34	MDB08	AD33	NC	AF39
LPCAD0	AW13	MDA03	AA33	MDB09	AD35	NC	AH37
LPCAD1	AU12	MDA04	Y37	MDB10	AE38	NC	A26
LPCAD2	AY12	MDA05	AA36	MDB11	AE33	NC	A28
LPCAD3	AR12	MDA06	AA34	MDB12	AE34	NC	AA06
LPCDRQ0#	AV12	MDA07	Y36	MDB13	AD37	NC	AB06
LPCDRQ1#	AR13	MDA08	W37	MDB14	AE36	NC	AD01
LPCFRAME#	AY13	MDA09	V35	MDB15	AD36	NC	B26
LVDSENVBLDA	AC04	MDA10	V34	MDQMA0	AA40	NC	B27
LVDSENVBLDB	AB07	MDA11	W34	MDQMA1	V38	NC	B28
LVDSENVDDA	AB05	MDA12	W36	MDQMA2	R39	NC	C26
LVDSENVDDB	AA05	MDA13	W35	MDQMA3	N36	NC	C27
MAA00	J38	MDA14	Y33	MDQMA4	B39	NC	D27
MAA01	L37	MDA15	V33	MDQMA5	D35	NC	D28
MAA02	K36	MDA16	U37	MDQMA6	D32	NC	E26
MAA03	K39	MDA17	U36	MDQMA7	E31	NC	E28
MAA04	K37	MDA18	R38	MDQMB0	AC38	NC	F22
MAA05	L39	MDA19	T36	MDQMB1	AE37	NC	F26
MAA06	J35	MDA20	U40	MDQSA0-	Y40	NC	F27
MAA07	M39	MDA21	U38	MDQSA0+	Y39	NC	F28
MAA08	K40	MDA22	T35	MDQSA1-	W38	NC	G22
MAA09	L36	MDA23	T37	MDQSA1+	W39	NC	G27
MAA10	J39	MDA24	R35	MDQSA2-	T40	NC	H27
MAA11	L40	MDA25	R34	MDQSA2+	T39	NC	M34
MAA12	M38	MDA26	N34	MDQSA3-	P35	NC	Y06
MAA13	H38	MDA27	P34	MDQSA3+	P36	NC	J06
MAB00	AK37	MDA28	T33	MDQSA4-	B40	NC	H06
MAB01	AP39	MDA29	R37	MDQSA4+	A40	NC	K04
MAB02	AM38	MDA30	N33	MDQSA5-	C35	NC	J04
MAB03	AM36	MDA31	R33	MDQSA5+	B35	NC	L05
MAB04	AM40	MDA32	C38	MDQSA6-	E33	NC	K05
MAB05	AM37	MDA33	D37	MDQSA6+	D33	NC	H01
MAB06	AN39	MDA34	C37	MDQSA7-	A31	NC	G01
MAB07	AK35	MDA35	A38	MDQSA7+	B31	NC	J02
MAB08	AN38	MDA36	F35	MDQSB0	AB38	NC	H02
MAB09	AL35	MDA37	C39	MDQSB1	AE40	NC	K01
MAB10	AP36	MDA38	B38	MEMCOMP	A30	NC	J01
MAB11	AN35	MDA39	A37	MEMVREF	U33	NMI	C19
MAB12	AK34	MDA40	E36	MODTA0	H39	PAR	AY06
MBAA0	J34	MDA41	D36	MODTA1	E38	PCICLK	AR16
MBAA1	J37	MDA42	B34	MODTA2	G37	PCIDGNT# / GPIO9	AN04
MBAA2	K35	MDA43	E34	MODTA3	F37	PCIDREQ# / GPIO8	AN03
MBAB0	AL37	MDA44	B36	MODTB	AK39	PCIRST0#	AY33
MBAB1	AP37	MDA45	A36	MSCASA#	H40	PCIRST1#	AW33
MCKEA0	K33	MDA46	A34	MSCASB#	AL40	PCISTP#	AY14
MCKEA1	M35	MDA47	C34	MSCK / IRQ1	AV33	PDA0	AP12
MCKEA2	L33	MDA48	F34	MSDT / IRQ12	AU33	PDA1	AN11
MCKEA3	L35	MDA49	E32	MSRASA#	H36	PDA2	AM10
MCKEB	AN40	MDA50	C33	MSRASB#	AL39	PDCS1#	AN12
MCLKOA0-	AA38	MDA51	B32	MSWEA#	G40	PDCS3#	AL11
MCLKOA0+	AA37	MDA52	G33	MSWEB#	AL36	PDD00	AV09
MCLKOA1-	N38	MDA53	G32	NAP#	F19	PDD01	AR08
MCLKOA1+	N37	MDA54	A33	NC	AF35	PDD02	AP09
MCLKOA2-	V39	MDA55	C32	NC	AG35	PDD03	AY11
MCLKOA2+	V40	MDA56	F31	NC	AF36	PDD04	AW10
MCLKOA3-	D40	MDA57	G30	NC	AF38	PDD05	AU10
MCLKOA3+	D39	MDA58	D30	NC	AG34	PDD06	AY09
MCLKOA4-	P40	MDA59	H30	NC	AG33	PDD07	AU08
MCLKOA4+	N40	MDA60	H32	NC	AG37	PDD08	AY08
MCLKOA5-	P38	MDA61	G31	NC	AF34	PDD09	AW08
MCLKOA5+	P39	MDA62	C30	NC	AH39	PDD10	AU09
MCLKOB-	AB40	MDA63	E30	NC	AH36	PDD11	AY10
MCLKOB+	AB39	MDB00	AC34	NC	AG38	PDD12	AV11
MCSA0#	F39	MDB01	AD40	NC	AJ36	PDD13	AN09
MCSA1#	F40	MDB02	AB36	NC	AH35	PDD14	AN10
MCSA2#	G38	MDB03	AC39	NC	AH40	PDD15	AR09
MCSA3#	E39	MDB04	AC37	NC	AJ37	PDDACK#	AU11

Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #
PDDREQ	AT08	SPISS1# / GPO2	AP13	VCC15	AD19	VCC18MEM	K38
PDIOR#	AL10	SPKR / GPO7 / SATALED1#	AR15	VCC15	AD21	VCC18MEM	L32
PDIORDY	AT11	SREXT	AM28	VCC15	AD23	VCC18MEM	L34
PDIOW#	AR10	SRX0-	AY27	VCC15	AD25	VCC18MEM	L38
PE0RX-	M01	SRX0+	AW27	VCC15	AE16	VCC18MEM	M32
PE0RX+	L01	SRX1-	AU26	VCC15	AE18	VCC18MEM	M36
PE0TX-	L03	SRX1+	AV26	VCC15	AE20	VCC18MEM	M40
PE0TX+	K03	STOP#	AY05	VCC15	AE22	VCC18MEM	N32
PE1RX-	N04	STPCLK#	G18	VCC15	AE24	VCC18MEM	P25
PE1RX+	N03	STX0-	AU28	VCC15	T17	VCC18MEM	P27
PE1TX-	N02	STX0+	AV28	VCC15	T19	VCC18MEM	P32
PE1TX+	M02	STX1-	AW25	VCC15	T21	VCC18MEM	R24
PEGRX0-	H03	STX1+	AY25	VCC15	T23	VCC18MEM	R26
PEGRX0+	G03	SUSA# / GPO0	AY31	VCC15	T25	VCC18MEM	R32
PEGTX0-	G04	SUSB# / GPO8	AP30	VCC15	U16	VCC18MEM	T27
PEGTX0+	F04	SUSC# / GPO9	AP31	VCC15	U18	VCC18MEM	T32
PERR#	AW05	SYSIDLE / GPO10	AP15	VCC15	U20	VCC18MEM	U26
PEXCLK-	F01	TCSEN#	AT12	VCC15	U22	VCC18MEM	U32
PEXCLK+	E01	TESTIN	J27	VCC15	U24	VCC18MEM	V27
PEXCOMP	F03	THRM# / GPI9	AN15	VCC15	V17	VCC18MEM	V32
PEXREXT	F02	THRMTRIP# / GPIO7	G17	VCC15	V19	VCC18MEM	W26
PME#	AT31	TP1	J20	VCC15	V21	VCC18MEM	W32
PWRBTN#	AR31	TP2	J21	VCC15	V23	VCC18MEM	Y27
PWRGD	AT30	TP3	J22	VCC15	V25	VCC18MEM	Y32
REQ0#	AR03	TP4	AL15	VCC15	W16	VCC33	AD15
REQ1#	AR01	TP5	AL12	VCC15	W18	VCC33	AE14
REQ2#	AU07	TP6	AK09	VCC15	W20	VCC33	AF15
REQ3#	AW07	TP7	AN31	VCC15	W22	VCC33	AF17
RING# / CRPWREN# / GPI8	AT29	TP8	AN30	VCC15	W24	VCC33	AF19
RSET	AE02	TRDY#	AT04	VCC15	Y15	VCC33	AF21
RSMRST#	AU30	USBCLK	AW15	VCC15	Y17	VCC33	AG09
RSVD1	AV36	USBOC0#	AY16	VCC15	Y19	VCC33	AG14
RSVD2	AW38	USBOC1#	AW16	VCC15	Y21	VCC33	AG16
RTCXI	AY29	USBOC2#	AY15	VCC15	Y23	VCC33	AG18
RTCXO	AW29	USBOC3#	AV16	VCC15	Y25	VCC33	AG20
SATALED0# / GPO4	AV14	USBOC4#	AU16	VCC18MEM	AA26	VCC33	AH09
SATAR50COMP	AR27	USBOC5#	AT16	VCC18MEM	AA32	VCC33	AJ09
SDIO0CD#	AT36	USBP0-	AU23	VCC18MEM	AB27	VCC33	AK11
SDIO0CLK	AT38	USBP0+	AV23	VCC18MEM	AB32	VCC33	AK12
SDIO0CMD#	AR40	USBP1-	AU21	VCC18MEM	AC26	VCC33	AK13
SDIO0D0	AT39	USBP1+	AV21	VCC18MEM	AC32	VCC33	AK14
SDIO0D1	AT40	USBP2-	AW22	VCC18MEM	AD27	VCC33	AK15
SDIO0D2	AR38	USBP2+	AY22	VCC18MEM	AD32	VCC33	AK16
SDIO0D3	AR39	USBP3-	AW20	VCC18MEM	AE32	VCC33LVDS	P03
SDIO0POFF	AW35	USBP3+	AY20	VCC18MEM	AF32	VCC33LVDS	P04
SDIO0PSEL	AP32	USBP4-	AY18	VCC18MEM	AG32	VCC33LVDS	P05
SDIO0WPD#	AT37	USBP4+	AW18	VCC18MEM	AH33	VCC33LVDS	R04
SDIO1CD#	AV38	USBP5-	AV19	VCC18MEM	AJ33	VCC33LVDS	R05
SDIO1CLK	AV40	USBP5+	AU19	VCC18MEM	AK33	VCC33LVDS	V15
SDIO1CMD#	AU38	USBREXT	AR23	VCC18MEM	AK36	VCC33LVDS	W14
SDIO1D0	AV39	VBAT	AV30	VCC18MEM	AK40	VCC33PEX	F05
SDIO1D1	AU37	VCC15	AA14	VCC18MEM	AL33	VCC33PEX	F06
SDIO1D2	AU40	VCC15	AA16	VCC18MEM	AL34	VCC33PEX	F07
SDIO1D3	AU39	VCC15	AA18	VCC18MEM	AL38	VCC33PEX	F08
SDIO1POFF	AV35	VCC15	AA20	VCC18MEM	AM33	VCC33PEX	G08
SDIO1PSEL	AY35	VCC15	AA22	VCC18MEM	AM39	VCC33PEX	H07
SDIO1WPD#	AW40	VCC15	AA24	VCC18MEM	AN36	VCC33PEX	H08
SERIRQ	AW12	VCC15	AB15	VCC18MEM	AN37	VCC33PEX	J07
SERR#	AW06	VCC15	AB17	VCC18MEM	AP40	VCC33PEX	J08
SLP#	C18	VCC15	AB19	VCC18MEM	E40	VCC33PEX	J09
SMBALRT#	AU34	VCC15	AB21	VCC18MEM	F38	VCC33PEX	K08
SMBCK1	AV34	VCC15	AB23	VCC18MEM	G39	VCC33PEX	K09
SMBCK2 / GPIO1	AY34	VCC15	AB25	VCC18MEM	H37	VCC33PEX	L06
SMBDT1	AT33	VCC15	AC14	VCC18MEM	J30	VCC33PEX	L07
SMBDT2 / GPIO0	AW34	VCC15	AC16	VCC18MEM	J31	VCC33PEX	L08
SMI#	E18	VCC15	AC18	VCC18MEM	J32	VCC33PEX	L09
SPICLK / GPIO6	AT14	VCC15	AC20	VCC18MEM	J36	VCC33PEX	M04
SPIDI / GPI0	AN14	VCC15	AC22	VCC18MEM	J40	VCC33PEX	M05
SPIDO / GPO1	AM14	VCC15	AC24	VCC18MEM	K32	VCC33PEX	M06
SPISS0# / GPO3	AN13	VCC15	AD17	VCC18MEM	K34	VCC33PEX	M07

Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #
VCC33PEX	M08	VSUS33	AV32				
VCC33PEX	M09	VSUS33	AW32				
VCC33PEX	N05	VSUS33	AY32				
VCC33PEX	N06	VSUS33USB	AF23				
VCC33PEX	N07	VSUS33USB	AG22				
VCC33PEX	N08	VSUS33USB	AP17				
VCC33PEX	N09	VSUS33USB	AP18				
VCC33PEX	P15	VSUS33USB	AP19				
VCC33PEX	R14	VSUS33USB	AP20				
VCC33PEX	T15	VSUS33USB	AP21				
VCC33PEX	U14	VSUS33USB	AP22				
VCCA15PLLUSB	AR19	VSUS33USB	AR17				
VCCA15SATA	AF25	VSUS33USB	AR20				
VCCA15SATA	AG24	VSUS33USB	AR21				
VCCA15SATA	AM24	VSUS33USB	AR22				
VCCA15SATA	AM25	VSUS33USB	AT17				
VCCA15SATA	AN24	VSUS33USB	AT22				
VCCA15SATA	AN25	VSUS33USB	AU17				
VCCA15SATA	AP24	VSUS33USB	AV17				
VCCA15SATA	AP25	VTT	H28				
VCCA15SATA	AR24	VTT	H29				
VCCA15SATA	AT24	VTT	J10				
VCCA33DAC1	AG01	VTT	J11				
VCCA33DAC2	AG02	VTT	J12				
VCCA33HCK	C29	VTT	J13				
VCCA33LVDS	V04	VTT	J14				
VCCA33PE1	E04	VTT	J15				
VCCA33PE2	G07	VTT	J16				
VCCA33PLL1	AF05	VTT	J17				
VCCA33PLL2	AF04	VTT	J18				
VCCA33PLL3	AG03	VTT	J19				
VCCA33PLLLVDS1	T04	VTT	J23				
VCCA33PLLLVDS2	U04	VTT	J24				
VCCA33PLLSATA	AR28	VTT	K20				
VCCA33PLLUSB	AR18	VTT	K21				
VCCA33SATA	AP26	VTT	K22				
VCCA33SATA	AP27	VTT	P17				
VCCA33SATA	AR25	VTT	P19				
VCCA33SATA	AR26	VTT	P21				
VCCA33SATA	AT25	VTT	P23				
VCCCR	AF27	VTT	R16				
VCCSD0	AE26	VTT	R18				
VCCSD1	AE27	VTT	R20				
VCPCLK / DSR2 / PTS0CLK	AM03	VTT	R22				
VCPD00 / RI1 / PTS0D0	AK02	WAKE# / GPI2	AV31				
VCPD01 / DCD1 / PTS0D1	AL04	XIN	AF08				
VCPD02 / SOUT1 / PTS0D2	AK01						
VCPD03 / SIN1/ PTS0D3	AM04						
VCPD04 / DTR1 / PTS0D4	AL01						
VCPD05 / DSR1 / PTS0D5	AM02						
VCPD06 / RTS1 / PTS0D6	AM01						
VCPD07 / CTS1 / PTS0D7	AN01						
VCPD08 / SIN2 / PTS0ERR	AM05						
VCPD09 / SOUT2 / STSLVLD	AL05						
VCPD10 / DCD2 / STS1SYNC	AL07						
VCPD11 / RI2 / STS1CLK	AL06						
VCPD12 / IRTX / STS1ERR	AM06						
VCPD13 / IRRX	AL08						
VCPD14 / IRRX2 / ITMOFF	AM08						
VCPD15 / DTR2 / STS1D	AM07						
VCPHS / CTS2 / PTS0VLD	AL03						
VCPVS / RTS2 / PTS0SYNC	AL02						
VRDSLP	AV15						
VSUS15	AG26						
VSUS15	AY30						
VSUS15MEM	B30						
VSUS15PEX	K07						
VSUS15USB	AP23						
VSUS33	AT32						
VSUS33	AU32						

Table 6. VX800UT Signal Ball List (Listed by Ball Number)

Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name
A01	HD62#	B31	MDQSA7+	D21	HTRDY#	F13	GND
A02	HD55#	B32	MDA51	D22	GND	F14	HD22#
A03	GND	B33	GND	D23	HA03#	F15	HD05#
A04	HD49#	B34	MDA42	D24	HA04#	F16	HD11#
A05	HD56#	B35	MDQSA5+	D25	HA14#	F17	GND
A06	HD53#	B36	MDA44	D26	GND	F18	INIT#
A07	GND	B37	GND	D27	NC	F19	NAP#
A08	HDSTB2P#	B38	MDA38	D28	NC	F20	HADS#
A09	HD37#	B39	MDQMA4	D29	GNDAHCK	F21	GND
A10	HD38#	B40	MDQSA4-	D30	MDA58	F22	NC
A11	GND	C01	HD60#	D31	GND	F23	HA13#
A12	HD26#	C02	HD51#	D32	MDQMA6	F24	HA11#
A13	HD24#	C03	HDSTB3P#	D33	MDQSA6+	F25	GND
A14	HD10#	C04	GND	D34	GND	F26	NC
A15	GND	C05	HD48#	D35	MDQMA5	F27	NC
A16	HDSTB0P#	C06	HD50#	D36	MDA41	F28	NC
A17	HD02#	C07	HD41#	D37	MDA33	F29	HCLK-
A18	IGNNE#	C08	GND	D38	GND	F30	GND
A19	GND	C09	HD35#	D39	MCLKOA3+	F31	MDA56
A20	HDRDY#	C10	HD39#	D40	MCLKOA3-	F32	GND
A21	HRS0#	C11	HDSTB1N#	E01	PEXCLK+	F33	GND
A22	HRS1#	C12	GND	E02	GND	F34	MDA48
A23	GND	C13	HD25#	E03	GNDA33PE1	F35	MDA36
A24	HA05#	C14	HD04#	E04	VCCA33PE1	F37	MODTA3
A25	HA10#	C15	HD03#	E06	HD57#	F38	VCC18MEM
A26	NC	C16	GND	E07	GND	F39	MCSA0#
A27	GND	C17	HD08#	E08	HD45#	F40	MCSA1#
A28	NC	C18	SLP#	E09	HD47#	G01	NC
A29	HGTLCOMPN	C19	NMI	E10	HD34#	G02	GND
A30	MEMCOMP	C20	GND	E11	GND	G03	PEGRX0+
A31	MDQSA7-	C21	HDEFER#	E12	HD23#	G04	PEGTX0-
A32	GND	C22	HA09#	E13	HD20#	G05	GND
A33	MDA54	C23	HREQ2#	E14	HD12#	G06	GNDA33PE2
A34	MDA46	C24	GND	E15	GND	G07	VCCA33PE2
A35	GND	C25	HA15#	E16	HD06#	G08	VCC33PEX
A36	MDA45	C26	NC	E17	HD00#	G09	HD32#
A37	MDA39	C27	NC	E18	SMI#	G10	HD40#
A38	MDA35	C28	GND	E19	GND	G11	HD28#
A39	GND	C29	VCCA33HCK	E20	HBNR#	G12	GND
A40	MDQSA4+	C30	MDA62	E21	HDBSY#	G13	HD29#
B01	GND	C31	GND	E22	HREQ1#	G14	HD21#
B02	HDBI3#	C32	MDA55	E23	GND	G15	HDBI0#
B03	HDSTB3N#	C33	MDA50	E24	HA08#	G16	GND
B04	HD61#	C34	MDA47	E25	HA12#	G17	THRMTRIP# / GPIO7
B05	GND	C35	MDQSA5-	E26	NC	G18	STPCLK#
B06	HD63#	C36	GND	E27	GND	G19	HDPWR#
B07	HD33#	C37	MDA34	E28	NC	G20	GND
B08	HDSTB2N#	C38	MDA32	E29	HCLK+	G21	HRS2#
B09	GND	C39	MDA37	E30	MDA63	G22	NC
B10	HDBI2#	C40	GND	E31	MDQMA7	G23	HREQ0#
B11	HDSTB1P#	D01	HD59#	E32	MDA49	G24	GND
B12	HD31#	D02	GND	E33	MDQSA6-	G25	HA16#
B13	GND	D03	HD58#	E34	MDA43	G26	HA30#
B14	HD14#	D04	HD52#	E35	GND	G27	NC
B15	HD09#	D05	HD54#	E36	MDA40	G28	GND
B16	HDSTB0N#	D06	GND	E38	MODTA1	G30	MDA57
B17	GND	D07	HD44#	E39	MCSA3#	G31	MDA61
B18	FERR#	D08	HD42#	E40	VCC18MEM	G32	MDA53
B19	INTR	D09	HD36#	F01	PEXCLK-	G33	MDA52
B20	HBPRI#	D10	GND	F02	PEXREXT	G37	MODTA2
B21	GND	D11	HD18#	F03	PEXCOMP	G38	MCSA2#
B22	HHITM#	D12	HD30#	F04	PEGTX0+	G39	VCC18MEM
B23	HA06#	D13	HDBI1#	F05	VCC33PEX	G40	MSWEA#
B24	HA07#	D14	GND	F06	VCC33PEX	H01	NC
B25	GND	D15	HD01#	F07	VCC33PEX	H02	NC
B26	NC	D16	HD13#	F08	VCC33PEX	H03	PEGRX0-
B27	NC	D17	HD07#	F09	GND	H04	GND
B28	NC	D18	GND	F10	HD43#	H05	GND
B29	HGTLCOMPP	D19	A20M#	F11	HD27#	H06	NC
B30	VSUS15MEM	D20	HHIT#	F12	HD16#	H07	VCC33PEX

Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name
H08	VCC33PEX	K03	PE0TX+	N40	MCLKOA4+	T20	GND
H09	HD46#	K04	NC	P01	LCD1D0-	T21	VCC15
H10	GND	K05	NC	P02	GNDLVDS	T22	GND
H11	HGTLVREF1	K06	GND	P03	VCC33LVDS	T23	VCC15
H12	HD19#	K07	VSUS15PEX	P04	VCC33LVDS	T24	GND
H13	HD17#	K08	VCC33PEX	P05	VCC33LVDS	T25	VCC15
H14	GND	K09	VCC33PEX	P14	GND	T26	GND
H15	HD15#	K20	VTT	P15	VCC33PEX	T27	VCC18MEM
H16	GCLK	K21	VTT	P16	GND	T32	VCC18MEM
H17	DPSLP#	K22	VTT	P17	VTT	T33	MDA28
H18	GND	K32	VCC18MEM	P18	GND	T34	GND
H19	CPURST#	K33	MCKEA0	P19	VTT	T35	MDA22
H20	HLOCK#	K34	VCC18MEM	P20	GND	T36	MDA19
H21	HBREQ0#	K35	MBAA2	P21	VTT	T37	MDA23
H22	GND	K36	MAA02	P22	GND	T38	GND
H23	HADSTB0N#	K37	MAA04	P23	VTT	T39	MDQSA2+
H24	HADSTB0P#	K38	VCC18MEM	P24	GND	T40	MDQSA2-
H25	HGTLVREF0	K39	MAA03	P25	VCC18MEM	U01	LCD1D2+
H26	GND	K40	MAA08	P26	GND	U02	GNDLVDS
H27	NC	L01	PE0RX+	P27	VCC18MEM	U03	LCD1CLK-
H28	VTT	L02	GND	P32	VCC18MEM	U04	VCCA33PLLLVDS2
H29	VTT	L03	PE0TX-	P33	GND	U05	GNDALVDS
H30	MDA59	L04	GND	P34	MDA27	U06	GNDLVDS
H31	GND	L05	NC	P35	MDQSA3-	U14	VCC33PEX
H32	MDA60	L06	VCC33PEX	P36	MDQSA3+	U15	GND
H34	GND	L07	VCC33PEX	P37	GND	U16	VCC15
H36	MSRASA#	L08	VCC33PEX	P38	MCLKOA5-	U17	GND
H37	VCC18MEM	L09	VCC33PEX	P39	MCLKOA5+	U18	VCC15
H38	MAA13	L32	VCC18MEM	P40	MCLKOA4-	U19	GND
H39	MODTA0	L33	MCKEA2	R01	LCD1D0+	U20	VCC15
H40	MSCASA#	L34	VCC18MEM	R02	LCD1D1-	U21	GND
J01	NC	L35	MCKEA3	R03	GNDLVDS	U22	VCC15
J02	NC	L36	MAA09	R04	VCC33LVDS	U23	GND
J03	GND	L37	MAA01	R05	VCC33LVDS	U24	VCC15
J04	NC	L38	VCC18MEM	R06	GNDLVDS	U25	GND
J05	GND	L39	MAA05	R14	VCC33PEX	U26	VCC18MEM
J06	NC	L40	MAA11	R15	GND	U27	GND
J07	VCC33PEX	M01	PE0RX-	R16	VTT	U32	VCC18MEM
J08	VCC33PEX	M02	PE1TX+	R17	GND	U33	MEMVREF
J09	VCC33PEX	M03	GND	R18	VTT	U34	GND
J10	VTT	M04	VCC33PEX	R19	GND	U36	MDA17
J11	VTT	M05	VCC33PEX	R20	VTT	U37	MDA16
J12	VTT	M06	VCC33PEX	R21	GND	U38	MDA21
J13	VTT	M07	VCC33PEX	R22	VTT	U39	GND
J14	VTT	M08	VCC33PEX	R23	GND	U40	MDA20
J15	VTT	M09	VCC33PEX	R24	VCC18MEM	V01	LCD1D3-
J16	VTT	M32	VCC18MEM	R25	GND	V02	GNDLVDS
J17	VTT	M34	NC	R26	VCC18MEM	V03	LCD1CLK+
J18	VTT	M35	MCKEA1	R27	GND	V04	VCCA33LVDS
J19	VTT	M36	VCC18MEM	R32	VCC18MEM	V05	GNDA33PLLLVDS2
J20	TP1	M38	MAA12	R33	MDA31	V06	GNDLVDS
J21	TP2	M39	MAA07	R34	MDA25	V14	GND
J22	TP3	M40	VCC18MEM	R35	MDA24	V15	VCC33LVDS
J23	VTT	N01	GND	R36	GND	V16	GND
J24	VTT	N02	PE1TX-	R37	MDA29	V17	VCC15
J25	BISTIN	N03	PE1RX+	R38	MDA18	V18	GND
J26	DFTIN	N04	PE1RX-	R39	MDQMA2	V19	VCC15
J27	TESTIN	N05	VCC33PEX	R40	GND	V20	GND
J30	VCC18MEM	N06	VCC33PEX	T01	LCD1D2-	V21	VCC15
J31	VCC18MEM	N07	VCC33PEX	T02	LCD1D1+	V22	GND
J32	VCC18MEM	N08	VCC33PEX	T03	GNDLVDS	V23	VCC15
J34	MBAA0	N09	VCC33PEX	T04	VCCA33PLLLVDS1	V24	GND
J35	MAA06	N32	VCC18MEM	T05	GNDA33PLLLVDS1	V25	VCC15
J36	VCC18MEM	N33	MDA30	T06	GNDLVDS	V26	GND
J37	MBAA1	N34	MDA26	T14	GND	V27	VCC18MEM
J38	MAA00	N35	GND	T15	VCC33PEX	V32	VCC18MEM
J39	MAA10	N36	MDQMA3	T16	GND	V33	MDA15
J40	VCC18MEM	N37	MCLKOA1+	T17	VCC15	V34	MDA10
K01	NC	N38	MCLKOA1-	T18	GND	V35	MDA09
K02	GND	N39	GND	T19	VCC15	V36	GND

Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name
V37	GND	AA16	VCC15	AC26	VCC18MEM	AF01	CRTAR
V38	MDQMA1	AA17	GND	AC27	GND	AF02	CRTAG
V39	MCLKOA2-	AA18	VCC15	AC32	VCC18MEM	AF03	GNDA33DAC3
V40	MCLKOA2+	AA19	GND	AC33	MDB07	AF04	VCCA33PLL2
W01	LCD1D3+	AA20	VCC15	AC34	MDB00	AF05	VCCA33PLL1
W02	LCD0D3+	AA21	GND	AC35	MDB05	AF06	GNDA33PLL1
W03	GNDLVDS	AA22	VCC15	AC36	GND	AF07	GNDA33PLL2
W04	GNDLVDS	AA23	GND	AC37	MDB04	AF08	XIN
W05	GNDLVDS	AA24	VCC15	AC38	MDQMB0	AF14	GND
W14	VCC33LVDS	AA25	GND	AC39	MDB03	AF15	VCC33
W15	GND	AA26	VCC18MEM	AC40	GND	AF16	GND
W16	VCC15	AA27	GND	AD01	NC	AF17	VCC33
W17	GND	AA32	VCC18MEM	AD02	LCD0D0-	AF18	GND
W18	VCC15	AA33	MDA03	AD03	DVP1SPCLK	AF19	VCC33
W19	GND	AA34	MDA06	AD04	DVP1SPD	AF20	GND
W20	VCC15	AA35	GND	AD05	CRTHSYNC	AF21	VCC33
W21	GND	AA36	MDA05	AD06	CRTVSYNC	AF22	GND
W22	VCC15	AA37	MCLKOA0+	AD14	GND	AF23	VSUS33USB
W23	GND	AA38	MCLKOA0-	AD15	VCC33	AF24	GNDUSB
W24	VCC15	AA39	GND	AD16	GND	AF25	VCCA15SATA
W25	GND	AA40	MDQMA0	AD17	VCC15	AF26	GNDA15SATA
W26	VCC18MEM	AB01	LCD0D1+	AD18	GND	AF27	VCCCR
W27	GND	AB02	GNDLVDS	AD19	VCC15	AF32	VCC18MEM
W32	VCC18MEM	AB03	LCD0D2-	AD20	GND	AF33	GND
W33	GND	AB04	GNDLVDS	AD21	VCC15	AF34	NC
W34	MDA11	AB05	LVDSENVDDA	AD22	GND	AF35	NC
W35	MDA13	AB06	NC	AD23	VCC15	AF36	NC
W36	MDA12	AB07	LVDSENVBLDB	AD24	GND	AF37	GND
W37	MDA08	AB14	GND	AD25	VCC15	AF38	NC
W38	MDQSA1-	AB15	VCC15	AD26	GND	AF39	NC
W39	MDQSA1+	AB16	GND	AD27	VCC18MEM	AF40	NC
W40	GND	AB17	VCC15	AD32	VCC18MEM	AG01	VCCA33DAC1
Y01	LCD0CLK+	AB18	GND	AD33	MDB08	AG02	VCCA33DAC2
Y02	LCD0D3-	AB19	VCC15	AD34	GND	AG03	VCCA33PLL3
Y03	GNDLVDS	AB20	GND	AD35	MDB09	AG04	DISPCLKO1 / VIDEO_GPIO5
Y04	GNDLVDS	AB21	VCC15	AD36	MDB15	AG05	DISPCLKI1 / VIDEO_GPIO4
Y05	GNDLVDS	AB22	GND	AD37	MDB13	AG06	DVP1CLK
Y06	NC	AB23	VCC15	AD38	GND	AG07	DVP1VS / IRRX
Y14	GND	AB24	GND	AD39	MDB06	AG08	DVP1D04 / DTR2
Y15	VCC15	AB25	VCC15	AD40	MDB01	AG09	VCC33
Y16	GND	AB26	GND	AE01	CRTAB	AG14	VCC33
Y17	VCC15	AB27	VCC18MEM	AE02	RSET	AG15	GND
Y18	GND	AB32	VCC18MEM	AE03	GNDA33DAC2	AG16	VCC33
Y19	VCC15	AB33	GND	AE04	GNDA33DAC1	AG17	GND
Y20	GND	AB34	MDA00	AE05	CRTSPCLK	AG18	VCC33
Y21	VCC15	AB35	MDA01	AE06	CRTSPD	AG19	GND
Y22	GND	AB36	MDB02	AE07	GNDA33PLL3	AG20	VCC33
Y23	VCC15	AB37	GND	AE14	VCC33	AG21	GND
Y24	GND	AB38	MDQSB0	AE15	GND	AG22	VSUS33USB
Y25	VCC15	AB39	MCLKOB+	AE16	VCC15	AG23	GNDUSB
Y26	GND	AB40	MCLKOB-	AE17	GND	AG24	VCCA15SATA
Y27	VCC18MEM	AC01	LCD0D1-	AE18	VCC15	AG25	GNDA15SATA
Y32	VCC18MEM	AC02	LCD0D0+	AE19	GND	AG26	VSUS15
Y33	MDA14	AC03	GNDLVDS	AE20	VCC15	AG27	GND
Y34	MDA02	AC04	LVDSENVBLDA	AE21	GND	AG32	VCC18MEM
Y35	GND	AC05	GNDLVDS	AE22	VCC15	AG33	NC
Y36	MDA07	AC06	GNDLVDS	AE23	GND	AG34	NC
Y37	MDA04	AC07	GNDLVDS	AE24	VCC15	AG35	NC
Y38	GND	AC14	VCC15	AE25	GND	AG36	GND
Y39	MDQSA0+	AC15	GND	AE26	VCCSD0	AG37	NC
Y40	MDQSA0-	AC16	VCC15	AE27	VCCSD1	AG38	NC
AA01	LCD0CLK-	AC17	GND	AE32	VCC18MEM	AG39	NC
AA02	GNDLVDS	AC18	VCC15	AE33	MDB11	AG40	GND
AA03	LCD0D2+	AC19	GND	AE34	MDB12	AH01	DISPCLKO0 / VIDEO_GPIO3
AA04	GNDLVDS	AC20	VCC15	AE35	GND	AH02	DVP1DE / IRRX2 / ITMOFF
AA05	LVDSENVDDB	AC21	GND	AE36	MDB14	AH03	DVP1D09 / DCD1
AA06	NC	AC22	VCC15	AE37	MDQMB1	AH04	DVP1D10 / SOUT1
AA07	BLTCK	AC23	GND	AE38	MDB10	AH05	DVP1D07 / CTS2
AA14	VCC15	AC24	VCC15	AE39	GND	AH06	DVP1D05 / DSR2
AA15	GND	AC25	GND	AE40	MDQSB1	AH07	DVP1TVCLKR

Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name
AH08	DVP1D02 / SOUT2	AM01	VCPD06 / RTS1 / PTS0D6	AP15	SYSIDLE / GPO10
AH09	VCC33	AM02	VCPD05 / DSR1 / PTS0D5	AP17	VSUS33USB
AH33	VCC18MEM	AM03	VCPCLK / DSR2 / PTS0CLK	AP18	VSUS33USB
AH34	GND	AM04	VCPD03 / SIN1/ PTS0D3	AP19	VSUS33USB
AH35	NC	AM05	VCPD08 / SIN2 / PTS0ERR	AP20	VSUS33USB
AH36	NC	AM06	VCPD12 / IRTX / STS1ERR	AP21	VSUS33USB
AH37	NC	AM07	VCPD15 / DTR2 / STS1D	AP22	VSUS33USB
AH38	GND	AM08	VCPD14 / IRRX2 / ITMOFF	AP23	VSUS15USB
AH39	NC	AM09	INTC#	AP24	VCCA15SATA
AH40	NC	AM10	PDA2	AP25	VCCA15SATA
AJ01	DISPCLKI0 / VIDEO_GPIO2	AM11	GND	AP26	VCCA33SATA
AJ02	IRSCLK	AM12	GND	AP27	VCCA33SATA
AJ03	DVP1D12 / DTR1	AM13	AZBITCLK	AP28	GNDAPLLSATA
AJ04	DVP1D11 / SIN1	AM14	SPIDO / GPO1	AP30	SUSB# / GPO8
AJ05	DVP1D15 / CTS1	AM15	CLKRUN#	AP31	SUSC# / GPO9
AJ06	DVP1D06 / RTS2	AM24	VCCA15SATA	AP32	SDIO0PSEL
AJ07	DVP1D03 / SIN2	AM25	VCCA15SATA	AP33	AZSDIN0
AJ08	DVP1HS / IRTX	AM26	GNDA33SATA	AP36	MAB10
AJ09	VCC33	AM27	GNDA33SATA	AP37	MBAB1
AJ33	VCC18MEM	AM28	SREXT	AP39	MAB01
AJ35	GND	AM33	VCC18MEM	AP40	VCC18MEM
AJ36	NC	AM36	MAB03	AR01	REQ1#
AJ37	NC	AM37	MAB05	AR02	GNT0#
AJ38	GND	AM38	MAB02	AR03	REQ0#
AJ39	NC	AM39	VCC18MEM	AR04	AD12
AK01	VCPD02 / SOUT1 / PTS0D2	AM40	MAB04	AR05	AD09
AK02	VCPD00 / RI1 / PTS0D0	AN01	VCPD07 / CTS1 / PTS0D7	AR06	AD03
AK03	DVP1D14 / RTS1	AN02	INTA#	AR07	AD01
AK04	DVP1D13 / DSR1	AN03	PCIDREQ# / GPIO8	AR08	PDD01
AK05	DVP1TVFLD	AN04	PCIDGNT# / GPIO9	AR09	PDD15
AK06	DVP1D08 / RI1	AN05	CBE1#	AR10	PDIOW#
AK07	DVP1D01 / DCD2	AN06	AD14	AR11	IRQ15
AK08	DVP1D00 / RI2	AN07	AD10	AR12	LPCAD3
AK09	TP6	AN08	AD02	AR13	LPCDRQ1#
AK11	VCC33	AN09	PDD13	AR14	C4PSTOP# / GPO6
AK12	VCC33	AN10	PDD14	AR15	SPKR / GPO7 / SATALED1#
AK13	VCC33	AN11	PDA1	AR16	PCICLK
AK14	VCC33	AN12	PDCS1#	AR17	VSUS33USB
AK15	VCC33	AN13	SPISS0# / GPO3	AR18	VCCA33PLLUSB
AK16	VCC33	AN14	SPIDI / GPI0	AR19	VCCA15PLLUSB
AK33	VCC18MEM	AN15	THRM# / GPI9	AR20	VSUS33USB
AK34	MAB12	AN24	VCCA15SATA	AR21	VSUS33USB
AK35	MAB07	AN25	VCCA15SATA	AR22	VSUS33USB
AK36	VCC18MEM	AN26	GNDA33SATA	AR23	USBREXT
AK37	MAB00	AN27	GNDA33SATA	AR24	VCCA15SATA
AK38	MCSB#	AN28	CLKI25M	AR25	VCCA33SATA
AK39	MODTB	AN30	TP8	AR26	VCCA33SATA
AK40	VCC18MEM	AN31	TP7	AR27	SATAR50COMP
AL01	VCPD04 / DTR1 / PTS0D4	AN32	AZSDIN2	AR28	VCCA33PLLSATA
AL02	VCPVS / RTS2 / PTS0SYNC	AN33	AZSDIN1	AR30	EXTSMI# / GPI5
AL03	VCPHS / CTS2 / PTS0VLD	AN35	MAB11	AR31	PWRBTN#
AL04	VCPD01 / DCD1 / PTS0D1	AN36	VCC18MEM	AR32	BATLOW# / GPI4
AL05	VCPD09 / SOUT2 / STSLVLD	AN37	VCC18MEM	AR33	KBDT / KBC_CPURST# / GPIO4
AL06	VCPD11 / RI2 / STS1CLK	AN38	MAB08	AR34	KBCK / A20GATE / GPIO5
AL07	VCPD10 / DCD2 / STS1SYNC	AN39	MAB06	AR38	SDIO0D2
AL08	VCPD13 / IRRX	AN40	MCKEB	AR39	SDIO0D3
AL10	PDIOR#	AP01	INTB#	AR40	SDIO0CMD#
AL11	PDCS3#	AP02	INTD#	AT01	AD30
AL12	TP5	AP03	GNT1#	AT02	AD31
AL13	AZSYNC	AP04	AD21	AT03	AD29
AL14	AZSDOUT	AP05	AD13	AT04	TRDY#
AL15	TP4	AP06	AD11	AT05	DEVSEL#
AL33	VCC18MEM	AP07	AD08	AT06	CBE0#
AL34	VCC18MEM	AP08	AD00	AT07	AD06
AL35	MAB09	AP09	PDD02	AT08	PDDREQ
AL36	MSWEB#	AP10	GND	AT09	GND
AL37	MBAB0	AP11	GND	AT10	GND
AL38	VCC18MEM	AP12	PDA0	AT11	PDIORDY
AL39	MSRASB#	AP13	SPISS1# / GPO2	AT12	TCSEN#
AL40	MSCASB#	AP14	GPIO13	AT13	GPIO10 / PCIERST0#

Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name
AT14	SPICLK / GPIO6	AV05	AD05	AW35	SDIO0POFF
AT15	CSTATE1 / GPO5	AV06	AD15	AW36	CR_D4 / SD_D4
AT16	USBOC5#	AV07	GNT3#	AW37	CR_D0 / SD_D0
AT17	VSUS33USB	AV08	GND	AW38	RSVD2
AT18	GNDUSB	AV09	PDD00	AW39	CR_D6 / SD_D6
AT19	GNDUSB	AV10	GND	AW40	SDIO1WPD#
AT20	GNDUSB	AV11	PDD12	AY01	AD20
AT21	GNDUSB	AV12	LPCDRQ0#	AY02	AD19
AT22	VSUS33USB	AV13	GPIO12	AY03	AD17
AT23	GNDUSB	AV14	SATALED0# / GPO4	AY04	IRDY#
AT24	VCCA15SATA	AV15	VRDSLP	AY05	STOP#
AT25	VCCA33SATA	AV16	USBOC3#	AY06	PAR
AT26	GNDA15SATA	AV17	VSUS33USB	AY07	GNT2#
AT27	GNDA15SATA	AV18	GNDUSB	AY08	PDD08
AT28	GNDA15SATA	AV19	USBP5-	AY09	PDD06
AT29	RING# / CRPWREN# / GPI8	AV20	GNDUSB	AY10	PDD11
AT30	PWRGD	AV21	USBP1+	AY11	PDD03
AT31	PME#	AV22	GNDUSB	AY12	LPCAD2
AT32	VSUS33	AV23	USBP0+	AY13	LPCFRAME#
AT33	SMBDT1	AV24	GNDUSB	AY14	PCISTP#
AT34	AZRST#	AV25	GNDA15SATA	AY15	USBOC2#
AT35	CRSD_WPD#	AV26	SRX1+	AY16	USBOC0#
AT36	SDIO0CD#	AV27	GNDA15SATA	AY17	GNDUSB
AT37	SDIO0WPD#	AV28	STX0+	AY18	USBP4-
AT38	SDIO0CLK	AV29	GNDA15SATA	AY19	GNDUSB
AT39	SDIO0D0	AV30	VBAT	AY20	USBP3+
AT40	SDIO0D1	AV31	WAKE# / GPI2	AY21	GNDUSB
AU01	AD28	AV32	VSUS33	AY22	USBP2+
AU02	AD27	AV33	MSCK / IRQ1	AY23	GNDUSB
AU03	AD26	AV34	SMBCK1	AY24	GNDA15SATA
AU04	AD16	AV35	SDIO1POFF	AY25	STX1+
AU05	AD07	AV36	RSVD1	AY26	GNDA15SATA
AU06	AD04	AV37	CRSD_CMD#	AY27	SRX0-
AU07	REQ2#	AV38	SDIO1CD#	AY28	GNDA15SATA
AU08	PDD07	AV39	SDIO1D0	AY29	RTCXI
AU09	PDD10	AV40	SDIO1CLK	AY30	VSUS15
AU10	PDD05	AW01	AD23	AY31	SUSA# / GPO0
AU11	PDDACK#	AW02	AD22	AY32	VSUS33
AU12	LPCAD1	AW03	AD18	AY33	PCIRST0#
AU13	GPIO11 / PCIERST1#	AW04	FRAME#	AY34	SMBCK2 / GPIO1
AU14	IDERST#	AW05	PERR#	AY35	SDIO1PSEL
AU16	USBOC4#	AW06	SERR#	AY36	CR_D5 / SD_D5
AU17	VSUS33USB	AW07	REQ3#	AY37	CR_CLK / SD_CLK
AU18	GNDUSB	AW08	PDD09	AY38	CR_D2 / SD_D2
AU19	USBP5+	AW09	GND	AY39	CR_D3 / SD_D3
AU20	GNDUSB	AW10	PDD04	AY40	CR_D7 / SD_D7
AU21	USBP1-	AW11	GND		
AU22	GNDUSB	AW12	SERIRQ		
AU23	USBP0-	AW13	LPCAD0		
AU24	GNDUSB	AW14	CPUSTP#		
AU25	GNDA15SATA	AW15	USBCLK		
AU26	SRX1-	AW16	USBOC1#		
AU27	GNDA15SATA	AW17	GNDUSB		
AU28	STX0-	AW18	USBP4+		
AU29	GNDA15SATA	AW19	GNDUSB		
AU30	RSMRST#	AW20	USBP3-		
AU31	LID# / GPI7	AW21	GNDUSB		
AU32	VSUS33	AW22	USBP2-		
AU33	MSDT / IRQ12	AW23	GNDUSB		
AU34	SMBALRT#	AW24	GNDA15SATA		
AU35	CRSD_CD#	AW25	STX1-		
AU36	CR_D1 / SD_D1	AW26	GNDA15SATA		
AU37	SDIO1D1	AW27	SRX0+		
AU38	SDIO1CMD#	AW28	GNDA15SATA		
AU39	SDIO1D3	AW29	RTCXO		
AU40	SDIO1D2	AW30	GPI1		
AV01	AD25	AW31	INTRUDER# / GPI6		
AV02	AD24	AW32	VSUS33		
AV03	CBE3#	AW33	PCIRST1#		
AV04	CBE2#	AW34	SMBDT2 / GPIO0		

Table 7. VX800UT Power / Ground Ball List

Ball Name	Ball Numbers
GND	A03, A07, A11, A15, A19, A23, A27, A32, A35, A39, B01, B05, B09, B13, B17, B21, B25, B33, B37, C04, C08, C12, C16, C20, C24, C28, C31, C36, C40, D02, D06, D10, D14, D18, D22, D26, D31, D34, D38, E02, E07, E11, E15, E19, E23, E27, E35, F09, F13, F17, F21, F25, F30, F32, F33, G02, G05, G12, G16, G20, G24, G28, H04, H05, H10, H14, H18, H22, H26, H31, H34, J03, J05, K02, K06, L02, L04, M03, N01, N35, N39, P14, P16, P18, P20, P22, P24, P26, P33, P37, R15, R17, R19, R21, R23, R25, R27, R36, R40, T14, T16, T18, T20, T22, T24, T26, T34, T38, U15, U17, U19, U21, U23, U25, U27, U34, U39, V14, V16, V18, V20, V22, V24, V26, V36, V37, W15, W17, W19, W21, W23, W25, W27, W33, W40, Y14, Y16, Y18, Y20, Y22, Y24, Y26, Y35, Y38, AA15, AA17, AA19, AA21, AA23, AA25, AA27, AA35, AA39, AB14, AB16, AB18, AB20, AB22, AB24, AB26, AB33, AB37, AC15, AC17, AC19, AC21, AC23, AC25, AC27, AC36, AC40, AD14, AD16, AD18, AD20, AD22, AD24, AD26, AD34, AD38, AE15, AE17, AE19, AE21, AE23, AE25, AE35, AE39, AF14, AF16, AF18, AF20, AF22, AF33, AF37, AG15, AG17, AG19, AG21, AG27, AG36, AG40, AH34, AH38, AJ35, AJ38, AM11, AM12, AP10, AP11, AT09, AT10, AV08, AV10, AW09, AW11
GNDA33PE[2:1]	G06, E03
GNDA33DAC[3:1]	AF03, AE03, AE04
GNDLVDS	P02, R03, R06, T03, T06, U02, U06, V02, V06, W03, W04, W05, Y03, Y04, Y05, AA02, AA04, AB02, AB04, AC03, AC05, AC06, AC07
GNDALVDS	U05
GNDA33PLLLVDS[2:1]	V05, T05
GNDA15SATA	AF26, AG25, AT26, AT27, AT28, AU25, AU27, AU29, AV25, AV27, AV29, AW24, AW26, AW28, AY24, AY26, AY28
GNDA33SATA	AM26, AM27, AN26, AN27
GNDAPLLSATA	AP28
GNDA33PLL[3:1]	AE07, AF07, AF06
GNDAHCK	D29
GNDUSB	AF24, AG23, AT18, AT19, AT20, AT21, AT23, AU18, AU20, AU22, AU24, AV18, AV20, AV22, AV24, AW17, AW19, AW21, AW23, AY17, AY19, AY21, AY23
VBAT	AV30
VCC15	T17, T19, T21, T23, T25, U16, U18, U20, U22, U24, V17, V19, V21, V23, V25, W16, W18, W20, W22, W24, Y15, Y17, Y19, Y21, Y23, Y25, AA14, AA16, AA18, AA20, AA22, AA24, AB15, AB17, AB19, AB21, AB23, AB25, AC14, AC16, AC18, AC20, AC22, AC24, AD17, AD19, AD21, AD23, AD25, AE16, AE18, AE20, AE22, AE24
VCC33	AD15, AE14, AF15, AF17, AF19, AF21, AG09, AG14, AG16, AG18, AG20, AH09, AJ09, AK11, AK12, AK13, AK14, AK15, AK16
VCC18MEM	E40, F38, G39, H37, J30, J31, J32, J36, J40, K32, K34, K38, L32, L34, L38, M32, M36, M40, N32, P25, P27, P32, R24, R26, R32, T27, T32, U26, U32, V27, V32, W26, W32, Y27, Y32, AA26, AA32, AB27, AB32, AC26, AC32, AD27, AD32, AE32, AF32, AG32, AH33, AJ33, AK33, AK36, AK40, AL33, AL34, AL38, AM33, AM39, AN36, AN37, AP40
VCC33PEX	F05, F06, F07, F08, G08, H07, H08, J07, J08, J09, K08, K09, L06, L07, L08, L09, M04, M05, M06, M07, M08, M09, N05, N06, N07, N08, N09, P15, R14, T15, U14
VCCCR	AF27
VCCSD[1:0]	AE27, AE26
VCC33LVDS	P03, P04, P05, R04, R05, V15, W14
VCCA33PE[2:1]	G07, E04
VCCA33DAC[2:1]	AG02, AG01
VCCA33LVDS	V04
VCCA33PLLLVDS[2:1]	U04, T04
VCCA15SATA	AF25, AG24, AM24, AM25, AN24, AN25, AP24, AP25, AR24, AT24
VCCA33SATA	AP26, AP27, AR25, AR26, AT25
VCCA33PLLSATA	AR28
VCCA15PLLUSB	AR19
VCCA33PLLUSB	AR18
VCCA33HCK	C29
VCCA33PLL[3:1]	AG03, AF04, AF05
VSUS15	AG26, AY30
VSUS15MEM	B30
VSUS15PEX	K07
VSUS15USB	AP23
VSUS33USB	AF23, AG22, AP17, AP18, AP19, AP20, AP21, AP22, AR17, AR20, AR21, AR22, AT17, AT22, AU17, AV17
VSUS33	AT32, AU32, AV32, AW32, AY32
VTT	H28, H29, J10, J11, J12, J13, J14, J15, J16, J17, J18, J19, J23, J24, K20, K21, K22, P17, P19, P21, P23, R16, R18, R20, R22

Signal Descriptions

CPU Interface

CPU Interface				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
HCLK+/–	E29, F29	I	**Host Clock.** ***VX800:*** 200 / 133 / 100 MHz ***VX800UT:*** 133 / 100 MHz	**VTT**
HA[30, 16:03]#	(see ball list)	IO	**Host Data Address.** Signal balls HA[30]# and HA[16:3]# are used. Host data addresses are transferred in 4X rate in V4 host protocol. On beat 0 and 2, address bits HA[30, 16:3]# are transferred. On beat 1 and 3, address bits HA[31, HAP, 29:17]# are transferred.	**VTT**
HD[63:0]#	(see ball list)	IO	**Host Data.** These signals are connected to the CPU data bus.	**VTT**
HADS#	F20	IO	**Address Strobe**. The CPU asserts ADS# in T1 of the CPU bus cycle.	**VTT**
HBNR#	E20	IO	**Block Next Request**. Used to block the current request bus owner from issuing new requests. This signal is used to dynamically control the processor bus pipeline depth.	**VTT**
HBPRI#	B20	IO	**Priority Agent Bus Request**. The owner of this signal will always be the next bus owner. This signal has priority over symmetric bus requests and causes the current symmetric owner to stop issuing new transactions unless the HLOCK# signal is asserted.	**VTT**
HDBSY#	E21	IO	**Data Bus Busy**. Used by the data bus owner to hold the data bus for transfers requiring more than one cycle.	**VTT**
HDEFER#	C21	IO	**Defer**. A dynamic deferring policy is used to optimize system performance. The DEFER# signal is also used to indicate a processor retry response.	**VTT**
HDRDY#	A20	IO	**Data Ready**. Asserted for each cycle that data is transferred.	**VTT**
HHIT#	D20	IO	**Hit**. Indicates that a caching agent holds the requested line. Also driven in conjunction with HITM# by the target to extend the snoop window.	**VTT**
HHITM#	B22	I	**Hit Modified**. Asserted by the CPU to indicate that the address presented with the last assertion of EADS# is modified in the L1 cache and needs to be written back.	**VTT**
HLOCK#	H20	I	**Host Lock**. All CPU cycles sampled with the assertion of HLOCK# and ADS# until the negation of HLOCK# must be atomic.	**VTT**
HREQ[2:0]#	C23 E22 G23	IO	**Host Request Command**. Signal balls HREQ[2:0]# are used. Host request commands are transferred in 4X rate in V4 host protocol. On beat 0 and 2, host request bits HREQ[2:0]# are transferred. On beat 1 and 3, host request bits HREQ[4:3]# are transferred on signal balls HREQ[1:0]#.	**VTT**

CPU Interface – continued				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
HTRDY#	D21	IO	**Host Target Ready**. Indicates that the target of the processor transaction is able to enter the data transfer phase.	**VTT**
HRS[2:0]#	G21 A22 A21	IO	**Response Signals**. Indicates the type of response per the table below: **HRS[2:0]# Response type** 000 Idle State 001 Retry Response 010 Defer Response 011 Reserved 100 Hard Failure 101 Normal Without Data 110 Implicit Writeback 111 Normal With Data	**VTT**
CPURST#	H19	O	**CPU Reset.** Reset output to CPU. External pull-up and filter capacitor to ground should be provided per CPU manufacturer's recommendations.	**VTT**
HBREQ0#	H21	I	**Bus Request 0.** Connect to CPU bus request 0.	**VTT**
HDBI[3:0]#	B02 B10 D13 G15	IO	**Host Dynamic Bus Inversion.** Driven along with HD[63:0]# to indicate if the associated signals are inverted or not. Used to limit the number of simultaneously switching signals to 8 for the associated 16-bit data signal group (HDBI3# for HD[63:48]#, HDBI2# for HD[47:32]#, HDBI1# for HD[31:16]#, and HDBI0# for HD[15:0]#). HDBIn# is asserted to limit the number of switching data signals simultaneously.	**VTT**
HADSTB0N# **HADSTB0P#**	H23 H24	IO	**Host Address Strobe.** HADSTB0P# / HADSTB0N# are negative-edge going data strobes used to latch HA[30, 16:03]# and HREQ[2:0]# on even and odd data beat transfers respectively.	**VTT**
HDSTB[3:0]P# **HDSTB[3:0]N#**	C03 A08 B11 A16 B03 B08 C11 B16	IO	**Host Differential Data Strobes.** Source synchronous strobes used to transfer HD[63:0]# & HDBI[3:0]# at a 4x transfer rate. HDSTB3P# / HDSTB3N# are the strobes for HD[63:48]# & HDBI3#; HDSTB2P# / HDSTB2N# are the strobes for HD[47:32]# & HDBI2#; HDSTB1P# / HDSTB1N# are the strobes for HD[31:16]# & HDBI1#; and HDSTB0P# / HDSTB0N# are the strobes for HD[15:0]# & HDBI0#.	**VTT**
HDPWR#	G19	O	**Data Bus Power Reduction.** Request to reduce power on the mobile CPU data bus input buffer. HIGH will disable the CPU data bus input buffer.	**VTT**

CPU Control Interface – continued				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
A20M#	D19	OD	**A20 Mask.** Connect to A20 mask input of the CPU to control address bit-20 generation. Logical combination of the A20GATE input (from internal or external keyboard controller) and Port92 bit-1 (Fast_A20).	**VTT**
FERR#	B18	I	**Numerical Coprocessor Error.** This signal is tied to the coprocessor error signal on the CPU. Internally generates interrupt 13 if active. This signal has a programmable internal 19.4K ohm pull-up resistor (default enable, D17F0 RxE3[1]). If internal pull-up is used, this signal can be left unconnected.	**VTT**
IGNNE#	A18	OD	**Ignore Numeric Error.** This signal is connected to the CPU "ignore error" signal.	**VTT**
INIT#	F18	OD	**Initialization.** INIT# is asserted if a shut-down special cycle on the PCI bus is detected or if a soft reset is initiated by the register.	**VTT**
INTR	B19	OD	**CPU Interrupt.** INTR is driven by the VX800 Series to signal the CPU that an interrupt request is pending and needs service.	**VTT**
NMI	C19	OD	**Non-Maskable Interrupt.** NMI is used to force a non-maskable interrupt to the CPU. VX800 Series generates an NMI when PCI bus SERR# is asserted.	**VTT**
SMI#	E18	OD	**System Management Interrupt.** SMI# is asserted by VX800 Series to the CPU in response to power management events.	**VTT**
THRMTRIP# / GPIO7	G17	I	**Thermal Detect Power Down.** This signal indicates a thermal trip from the processor.	**VTT**
STPCLK#	G18	O	**Stop Clock.** This signal is asserted by the VX800 Series to throttle the processor clock. This signal has a programmable internal 19.4K ohm pull-up resistor (default enable, D17F0 RxE3[0]).	**VTT**
SLP#	C18	O	**Sleep.** Used to put the CPU into a sleep state.	**VTT**
DPSLP#	H17	O	**CPU Deep Sleep.** Used to put the CPU into a deeper sleep mode.	**VTT**
NAP#	F19	O	**CPU NAP State.** Connected to the NAP# of CPU. The assertion causes the processor to intitiate a minimum P state by sending the VID targeting to the minimum operation voltage in C4 state to CPU voltage regulator. NAP# is the invert of VRDPSLP.	**VTT**

DDR2 SDRAM Memory Interface

System Memory Interface (Channel A)				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
MAA[13:0]	(see ball list)	O	**DRAM Row/Column Address.**	**VCC18MEM**
MBAA[2:0]	K35 J37 J34	O	**DRAM Bank Address.**	**VCC18MEM**
MSRASA#	H36	O	**DRAM Row Address Strobe.**	**VCC18MEM**
MSCASA#	H40	O	**DRAM Column Address Strobe.**	**VCC18MEM**
MSWEA#	G40	O	**DRAM Write Enable.**	**VCC18MEM**
MDA[63:0]	(see ball list)	IO	**Memory Data.** In 32-bit memory interface mode, connect memory data lines to MDA[31:0].	**VCC18MEM**
MDQMA[7:0]	(see ball list)	O	**Memory Data Mask.** In 32-bit memory interface mode, connect to MDQMA[3:0].	**VCC18MEM**
MODTA[3:0]	(see ball list)	O	**Memory On-Die Termination Enable.**	**VCC18MEM**
MDQSA[7:0]+/–	(see ball list)	IO	**Memory Data Strobes.** In 32-bit memory interface mode, connect to MDQSA[3:0]+/–.	**VCC18MEM**
MCSA[3:0]#	(see ball list)	O	**Memory Chip Select.**	**VCC18MEM**
MCKEA[3:0]	(see ball list)	O	**Memory Clock Enable.**	**VCC18MEM**
MCLKOA[5:0]+/–	(see ball list)	O	**Differential Memory Clock Output.**	**VCC18MEM**

SnapShot Memory Interface (Channel C)				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
MAB[12:0]	(see ball list)	O	**DRAM Row/Column Address.**	**VCC18MEM**
MBAB[1:0]	AP37 AL37	O	**DRAM Bank Address.**	**VCC18MEM**
MSRASB#	AL39	O	**DRAM Row Address Strobe.**	**VCC18MEM**
MSCASB#	AL40	O	**DRAM Column Address Strobe.**	**VCC18MEM**
MSWEB#	AL36	O	**DRAM Write Enable.**	**VCC18MEM**
MDB[15:0]	(see ball list)	IO	**Memory Data.** Connect to MDB[15:0]. MDB[31:16] are reserved.	**VCC18MEM**
MDQMB[1:0]	AE37, AC38	O	**Memory Data Mask.** Connect to MDQMB[1:0]. MDQMB[3:2] are reserved.	**VCC18MEM**
MODTB	AK39	O	**Memory On-Die Termination Enable.**	**VCC18MEM**
MDQSB[1:0]	AE40, AB38	IO	**Memory Data Strobes.** Connect to MDQSB[1:0]. MDQSB[3:2] are reserved.	**VCC18MEM**
MCSB#	AK38	O	**Memory Chip Select.**	**VCC18MEM**
MCKEB	AN40	O	**Memory Clock Enable.**	**VCC18MEM**
MCLKOB+/–	AB39, AB40	O	**Differential Memory Clock Output.**	**VCC18MEM**

PCI Express Interface

PCI Express Interface				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
PEXCLK+/–	E01, F01	I	**PCI Express Clock.** These pins receive the 100 MHz clock used by the internal PCI Express logic. Multiplied up to 2.5 GHz on-chip for use by the integrated PCI Express PHY to transmit / receive data.	**VCC33PEX**
PCIERST0# / GPIO10	AT13	O	**PCI Express Reset 0.**	**VCC33**
PCIERST1# / GPIO11	AU13	O	**PCI Express Reset 1.**	**VCC33**
PEXCOMP	F03	AI	**PCI Express Port Compensation.**	**VCC33PEX**
PEXREXT	F02	AI	**PCI Express Port External Resistor.**	**VCC33PEX**
PCI Express Port G				
VX800: **PEGRX[3:0]+/–** ***VX800UT:*** **PEGRX0+/–**	(see ball list)	I	***VX800:*** **PCI Express Port G Differential Receive Data [3:0].** ***VX800UT:*** **PCI Express Port G Differential Receive Data [0].**	**VCC33PEX**
VX800: **PEGTX[3:0]+/–** ***VX800UT:*** **PEGTX0+/–**	(see ball list)	O	***VX800:*** **PCI Express Port G Differential Transmit Data [3:0].** ***VX800UT:*** **PCI Express Port G Differential Transmit Data [0].**	**VCC33PEX**
PCI Express Port 0 (1-Lane)				
PE0RX+/–	L01, M01	I	**PCI Express Port 0 Differential Receive Data.**	**VCC33PEX**
PE0TX+/–	K03, L03	O	**PCI Express Port 0 Differential Transmit Data.**	**VCC33PEX**
PCI Express Port 1 (1-Lane)				
PE1RX+/–	N03, N04	I	**PCI Express Port 1 Differential Receive Data.**	**VCC33PEX**
PE1TX+/–	M02, N02	O	**PCI Express Port 1 Differential Transmit Data.**	**VCC33PEX**

LVDS Interface

LVDS Interface				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
LCD0D0+/–	AC02, AD02	O	**LVDS Single Channel Mode:** LVDS Differential Data 0 for Panel 0. **LVDS Dual Channel Mode:** LVDS Differential Data 0.	**VCC33LVDS**
LCD0D1+/–	AB01, AC01	O	**Single Channel Mode:** LVDS Differential Data 1 for Panel 0. **Dual Channel Mode:** LVDS Differential Data 1.	**VCC33LVDS**
LCD0D2+/–	AA03, AB03	O	**Single Channel Mode:** LVDS Differential Data 2 for Panel 0. **Dual Channel Mode:** LVDS Differential Data 2.	**VCC33LVDS**
LCD0D3+/–	W02, Y02	O	**Single Channel Mode:** LVDS Differential Data 3 for Panel 0. **Dual Channel Mode:** LVDS Differential Data 3.	**VCC33LVDS**
LCD0CLK+/–	Y01, AA01	O	**Single Channel Mode:** LVDS Differential Clock for Panel 0. **Dual Channel Mode:** LVDS Differential Clock for Panel 0.	**VCC33LVDS**
LCD1D0+/–	R01, P01	O	**Single Channel Mode:** LVDS Differential Data 0 for Panel 1. **Dual Channel Mode:** LVDS Differential Data 4.	**VCC33LVDS**
LCD1D1+/–	T02, R02	O	**Single Channel Mode:** LVDS Differential Data 1 for Panel 1. **Dual Channel Mode:** LVDS Differential Data 5.	**VCC33LVDS**
LCD1D2+/–	U01, T01	O	**Single Channel Mode:** LVDS Differential Data 2 for Panel 1 **Dual Channel Mode:** LVDS Differential Data 6.	**VCC33LVDS**
LCD1D3+/–	W01, V01	O	**Single Channel Mode:** LVDS Differential Data 3 for Panel 1 **Dual Channel Mode:** LVDS Differential Data 7.	**VCC33LVDS**
LCD1CLK+/–	V03, U03	O	**Single Channel Mode:** LVDS Differential Clock for Panel 1. **Dual Channel Mode:** LVDS Differential Clock for Panel 1.	**VCC33LVDS**

LCD Panel Power and Brightness Control				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
LVDSENVDD[A:B]	AB05 AA05	O	**Enable Panel VDD Power.** For two panels.	**VCC33**
LVDSENVBLD[A:B]	AC04 AB07	O	**Enable Panel Back Light.** For two panels.	**VCC33**
BLTCK	AA07	O	**LVDS Backlight PWM Clock Control.**	**VCC33**

CRT Interface

CRT Interface				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
CRTAR **CRTAG** **CRTAB**	AF01 AF02 AE01	AO	**Analog Red / Green / Blue.** DAC outputs.	**VCCA33DAC**
CRTHSYNC	AD05	O	**Horizontal Sync.**	**VCC33**
CRTVSYNC	AD06	O	**Vertical Sync.**	**VCC33**
RSET	AE02	AI	**Reference Resistor.** Tie to GNDADAC through an external resistor to control the RAMDAC full-scale current.	**VCCA33DAC**
CRTSPCLK	AE05	IO	**CRT Serial Port (SMBus) Clock.**	**VCC33**
CRTSPD	AE06	IO	**CRT Serial Port (SMBus) Data.**	**VCC33**

Video Capture Port Interface

VCP interface is multiplexed with UART and IR ports.
The VCP interface can be enabled when set 3C5.78[7] = 0.

Video Capture Mode				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
VCPD[7:0]	(see ball list)	I	**Video Capture Port Data [7:0] of 8-bit CCIR-601/656 Port or lower half of 16-bit CCIR-601/656 Port.**	**VCC33**
VCPD8	AM05	I	**Video Capture Port Data 8 of 16-bit CCIR-601/656 Port.**	**VCC33**
VCPD9	AL05	I	**Video Capture Port Data 9 of 16-bit CCIR-601/656 Port.**	**VCC33**
VCPD10	AL07	I	**Video Capture Port Data 10 of 16-bit CCIR-601/656 Port.**	**VCC33**
VCPD11	AL06	I	**Video Capture Port Data 11 of 16-bit CCIR-601/656 Port.**	**VCC33**
VCPD12	AM06	I	**Video Capture Port Data 12 of 16-bit CCIR-601/656 Port.**	**VCC33**
VCPD[14:13]	AM08 AL08	I	**Video Capture Port Data [14:13] of 16-bit CCIR-601/656 Port.**	**VCC33**
VCPD15	AM07	I	**Video Capture Port Data 15 of 16-bit CCIR-601/656 Port.**	**VCC33**
VCPHS	AL03	I	**Video Capture Port Horizontal Sync.**	**VCC33**
VCPVS	AL02	I	**Video Capture Port Vertical Sync.**	**VCC33**
VCPCLK	AM03	I	**Video Capture Port Clock.**	**VCC33**

The transport stream input mode signals are multiplexed with VCP interface signals.

Transport Stream Input Mode				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
PTS0D[7:0]	(see ball list)	I	**Parallel Transport Stream Port 0 Data [7:0].**	**VCC33**
PTS0ERR	AM05	I	**Parallel Transport Stream Port 0 Error.**	**VCC33**
PTS0VLD	AL03	I	**Parallel Transport Stream Port 0 Data Valid.**	**VCC33**
PTS0SYNC	AL02	I	**Parallel Transport Stream Port 0 Data Sync.**	**VCC33**
PTS0CLK	AM03	I	**Parallel Transport Stream Port 0 Clock.**	**VCC33**
STS1VLD	AL05	I	**Serial Transport Stream Port 1 Data Valid.**	**VCC33**
STS1SYNC	AL07	I	**Serial Transport Stream Port 1 Data Sync.**	**VCC33**
STS1CLK	AL06	I	**Serial Transport Stream Port 1 Clock.**	**VCC33**
STS1ERR	AM06	I	**Serial Transport Stream Port 1 Error.**	**VCC33**
STS1D	AM07	I	**Serial Transport Stream Port 1 Data.**	**VCC33**

Digital Video Port 1 (DVP1) Interface

DVP1 interface is multiplexed with UART and IR ports.
The DVP1 interface can be enabled when set 3C5.78[7] = 0.

Digital Video Port 1 (DVP1) Interface				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
DVP1D[15:0]	(see ball list)	O	**12-Bit Digital Video Output Mode:** DVP1D[11:0] is the data for 12-Bit DVO Interface. **18-Bit TTL Panel Interface Mode:** DVP1D[15:0] is the TTL Panel Data [15:0].	**VCC33**
DVP1HS	AJ08	O	**12-Bit Digital Video Output Mode:** DVP1HS is Digital Video Port 1 Horizontal Sync. **18-Bit TTL Panel Interface Mode:** DVP1HS is the TTL Panel Horizontal Sync.	**VCC33**
DVP1VS	AG07	O	**12-Bit Digital Video Output Mode:** DVP1VS is Digital Video Port 1 Vertical Sync. **18-Bit TTL Panel Interface Mode:** DVP1VS is the TTL Panel Vertical Sync.	**VCC33**
DVP1DE	AH02	O	**12-Bit Digital Video Output Mode:** DVP1DE is Digital Video Port 1 Data Enable. **18-Bit TTL Panel Interface Mode:** DVP1DE is the TTL Panel Data Enable.	**VCC33**
DVP1TVFLD	AK05	IO	**12-Bit Digital Video Output Mode:** For external TV encoder: DVP1TVFLD is TV Field Out. **18-Bit TTL Panel Interface Mode:** DVP1TVFLD is the TTL Panel Data 17.	**VCC33**
DVP1CLK	AG06	O	**12-Bit Digital Video Output Mode:** DVP1CLK is Digital Video Port 1 Clock. **18-Bit TTL Panel Interface Mode:** DVP1CLK is the TTL Panel Clock.	**VCC33**
DVP1TVCLKR	AH07	I	**12-Bit Digital Video Output Mode:** For external TV encoder: DVP1TVCLKR is the TV Return Clock. For external DVI transmitter: DVP1TVCLKR is the Display Detect. **18-Bit TTL Panel Interface Mode:** DVP1TVCLKR is the TTL Panel Data 16. Tie to GND if not used.	**VCC33**
DVP1SPD	AD04	IO	**DVP1 SMBus Data.**	**VCC33**
DVP1SPCLK	AD03	IO	**DVP1 SMBus Clock.**	**VCC33**

Functions of Digital Video Port 1					
Ball Name	**Ball #**	**DVO (TV Encoder)**	**DVO (DVI Transmitter)**	**18-bit TTL Panel**	
				Signal	**RGB Color Mapping**
DVP1D15	AJ05	-	-	TTLPD15	R5
DVP1D14	AK03	-	-	TTLPD14	R4
DVP1D13	AK04	-	-	TTLPD13	R3
DVP1D12	AJ03	-	-	TTLPD12	R2
DVP1D11	AJ04	DVO-TVD11	DVO-DVID11	TTLPD11	G7 (MSB)
DVP1D10	AH04	DVO-TVD10	DVO-DVID10	TTLPD10	G6
DVP1D09	AH03	DVO-TVD09	DVO-DVID09	TTLPD09	G5
DVP1D08	AK06	DVO-TVD08	DVO-DVID08	TTLPD08	G4
DVP1D07	AH05	DVO-TVD07	DVO-DVID07	TTLPD07	G3
DVP1D06	AJ06	DVO-TVD06	DVO-DVID06	TTLPD06	G2
DVP1D05	AH06	DVO-TVD05	DVO-DVID05	TTLPD05	B7 (MSB)
DVP1D04	AG08	DVO-TVD04	DVO-DVID04	TTLPD04	B6
DVP1D03	AJ07	DVO-TVD03	DVO-DVID03	TTLPD03	B5
DVP1D02	AH08	DVO-TVD02	DVO-DVID02	TTLPD02	B4
DVP1D01	AK07	DVO-TVD01	DVO-DVID01	TTLPD01	B3
DVP1D00	AK08	DVO-TVD00	DVO-DVID00	TTLPD00	B2
DVP1DE	AH02	DVO-TVDE	DVO-DVIDE	TTLPDE	DE
DVP1TVFLD	AK05	DVO-TVFIELD	-	TTLPD17	R7 (MSB)
DVP1HS	AJ08	DVO-TVHS	DVO-DVIHS	TTLPHS	HSYNC
DVP1VS	AG07	DVO-TVVS	DVO-DVIVS	TTLPVS	VSYNC
DVP1CLK	AG06	DVO-TVCLK	DVO-DVICLK	TTLPCLK	Clock
DVP1TVCLKR	AH07	DVO-TVCLKR	DVO-DVIDET	TTLPD16	R6

PCI Bus Interface

PCI Bus Interface				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
AD[31:0]	(see ball list)	IO	**Address / Data Bus.** Multiplexed address and data. The address is driven with FRAME# assertion and data is driven or received in following cycles.	**VCC33**
CBE[3:0]#	AV03 AV04 AN05 AT06	IO	**Command / Byte Enable.** The command is driven with FRAME# assertion. Byte enables corresponding to supplied or requested data are driven on following clocks.	**VCC33**
DEVSEL#	AT05	IO	**Device Select.** The VX800 Series asserts this signal to claim PCI transactions through positive or subtractive decoding. As an input, DEVSEL# indicates the response to a VX800 Series-initiated transaction and is also sampled when decoding whether to subtractively decode the cycle. This signal has a programmable internal 19.4K ohm pull-up resistor (default enable, D17F7 Rx55[0]).	**VCC33**
FRAME#	AW04	IO	**Frame.** Assertion indicates the address phase of a PCI transfer. Negation indicates that one additional data transfer is desired by the cycle initiator. This signal has a programmable internal 19.4K ohm pull-up resistor (default enable, D17F7 Rx55[0]).	**VCC33**
IRDY#	AY04	IO	**Initiator Ready.** Asserted when the initiator is ready for data transfer. This signal has a programmable internal 19.4K ohm pull-up resistor (default enable, D17F7 Rx55[0]).	**VCC33**
TRDY#	AT04	IO	**Target Ready.** Asserted when the target is ready for data transfer. This signal has a programmable internal 19.4K ohm pull-up resistor (default enable, D17F7 Rx55[0]).	**VCC33**
STOP#	AY05	IO	**Stop.** Asserted by the target to request the master to stop the current transaction. This signal has a programmable internal 19.4K ohm pull-up resistor (default enable, D17F7 Rx55[0]).	**VCC33**
SERR#	AW06	I	**System Error.** SERR# can be pulsed active by any PCI device that detects a system error condition. Upon sampling SERR# active, the VX800 Series can be programmed to generate an NMI to the CPU. This signal has a programmable internal 19.4K ohm pull-up resistor (default enable, D17F7 Rx55[0]). If this signal is not used and the internal pull-up is enabled, then this signal can be left unconnected.	**VCC33**
PERR#	AW05	-	**Parity Error.** PERR#, sustained tri-state, is only for the reporting of data parity errors during all PCI transactions except a Special Cycle. This signal has a programmable internal 19.4K ohm pull-up resistor (default enable, D17F7 Rx55[0]). If this signal is not used and the internal pull-up is enabled, then this signal can be left unconnected.	**VCC33**
PAR	AY06	IO	**Parity.** A single parity bit is provided over AD[31:0] and C/BE[3:0]#.	**VCC33**

PCI Bus Interface - continued				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
INTA# **INTB#** **INTC#** **INTD#**	AN02 AP01 AM09 AP02	I	**PCI Interrupt Request**. The INTA# through INTD# signal balls are typically connected to the PCI bus INTA#-INTD# signals per the table below. BIOS settings must match the physical connection method. INTA# INTB# INTC# INTD# PCI Slot 1 INTA# INTB# INTC# INTD# PCI Slot 2 INTB# INTC# INTD# INTA# PCI Slot 3 INTC# INTD# INTA# INTB# PCI Slot 4 INTD# INTA# INTB# INTC# This signal has a programmable internal 19.4K ohm pull-up resistor (default enable, D17F7 Rx55[1]). If this signal is not used and the internal pull-up is enabled, then this signal can be left unconnected.	**VCC33**
REQ3# **REQ2#** **REQ1#** **REQ0#**	AW07 AU07 AR01 AR03	I	**PCI Request.** These signals connect to the VX800 Series from each PCI slot (or each PCI master) for access request to the PCI bus. This signal has a programmable internal 19.4K ohm pull-up resistor (default enable, D17F7 Rx55[1]). If this signal is not used and the internal pull-up is enabled, then this signal can be left unconnected.	**VCC33**
GNT3# **GNT2#** **GNT1#** **GNT0#**	AV07 AY07 AP03 AR02	O	**PCI Grant.** These signals are driven by the VX800 Series to grant PCI bus access to a specific PCI master. This signal has a programmable internal 19.4K ohm pull-up resistor (default enable, D17F7 Rx55[1]).	**VCC33**
PCIRST[1:0]#	AW33 AY33	O	**PCI Reset.** This signal is used to reset devices attached to the PCI bus. All power-on strap options are sampled by the rising edge of this signal.	**VCC33**
PCICLK	AR16	I	**PCI Clock.** This signal provides timing for all transactions on the PCI Bus. This clock is necessary even if the system does not need PCI interface.	**VCC33**

USB 2.0 Interface

USB 2.0 Interface				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
USBP0+/–	AV23, AU23	IO	**USB Port 0 Differential Data.** This signal has an internal 15K ohm pull-down resistor.	**VSUS33USB**
USBP1+/–	AV21, AU21	IO	**USB Port 1 Differential Data.** This signal has an internal 15K ohm pull-down resistor.	**VSUS33USB**
USBP2+/–	AY22, AW22	IO	**USB Port 2 Differential Data.** This signal has an internal 15K ohm pull-down resistor.	**VSUS33USB**
USBP3+/–	AY20, AW20	IO	**USB Port 3 Differential Data.** This signal has an internal 15K ohm pull-down resistor.	**VSUS33USB**
USBP4+/–	AW18, AY18	IO	**USB Port 4 Differential Data.** This signal has an internal 15K ohm pull-down resistor.	**VSUS33USB**
USBP5+/–	AU19, AV19	IO	**USB Port 5 Differential Data.** This signal has an internal 15K ohm pull-down resistor.	**VSUS33USB**
USBCLK	AW15	I	**USB Clock.** 48 MHz clock input for the USB and HD Audio. If USB and HD Audio interfaces are not used, leave it unconnected.	**VSUS33USB**
USBOC0#	AY16	I	**USB Port 0 Over Current Detect.** Port 0 is disabled if low. If USB interface is not needed, leave it unconnected.	**VSUS33USB**
USBOC1#	AW16	I	**USB Port 1 Over Current Detect.** Port 1 is disabled if low. If USB interface is not needed, leave it unconnected.	**VSUS33USB**
USBOC2#	AY15	I	**USB Port 2 Over Current Detect.** Port 2 is disabled if low. If USB interface is not needed, leave it unconnected.	**VSUS33USB**
USBOC3#	AV16	I	**USB Port 3 Over Current Detect.** Port 3 is disabled if low. If USB interface is not needed, leave it unconnected.	**VSUS33USB**
USBOC4#	AU16	I	**USB Port 4 Over Current Detect.** Port 4 is disabled if low. If USB interface is not needed, leave it unconnected.	**VSUS33USB**
USBOC5#	AT16	I	**USB Port 5 Over Current Detect.** Port 5 is disabled if low. If USB interface is not needed, leave it unconnected.	**VSUS33USB**
USBREXT	AR23	AI	**USB External Resistor** If USB interface is not needed, leave it unconnected.	**VSUS33USB**

SATA Interface

SATA Interface				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
SRX0+/–	AW27, AY27	I	**SATA Port 0 Differential Receiver.**	**VCCA33SATA**
SRX1+/–	AV26, AU26	I	**SATA Port 1 Differential Receiver.**	**VCCA33SATA**
STX0+/–	AV28, AU28	O	**SATA Port 0 Differential Transmitter.**	**VCCA33SATA**
STX1+/–	AY25, AW25	O	**SATA Port 1 Differential Transmitter.**	**VCCA33SATA**
CLKI25M	AN28	I	**SATA 25MHz Input.** 3.3V clock swing. Tie to GND if not used.	**VCCA33SATA**
SREXT	AM28	AI	**SATA External Resistor.** If SATA interface is not needed, leave it unconnected.	**VCCA33SATA**
SATALED0# / GPO4	AV14	O	**SATA LED 0.** This signal can optionally be used as GPO4.	**VCC33**
SATALED1# / SPKR / GPO7	AR15	O	**SATA LED 1.** This signal can optionally be used as SPKR or GPO7.	**VCC33**

Enhanced IDE Interface

Enhanced IDE Interface				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
PDIORDY	AT11	I	EIDE Mode: **PDIORDY:** Device ready indicator UltraDMA Mode: **(Write) PDDMARDY**: Output flow control. The device may assert PDDMARDY to pause output transfers **(Read) PDSTROBE:** Input data strobe (both edges). The device may stop assertion of PDSTROBE to pause input data transfers This signal has a programmable internal 19.4K ohm pull-up resistor (default enable, D17F0 Rx47[1]).	**VCC33**
PDIOR#	AL10	O	EIDE Mode: **PDIOR#:** Device read strobe UltraDMA Mode: **(Write) PHSTROBE:** Output data strobe (both edges). The host may stop assertion of PHSTROBE to pause output data transfers **(Read) PHDMARDY:** Input flow control**.** The host may assert PHDMARDY to pause input transfers This signal has a programmable internal 19.4K ohm pull-up resistor (default enable, D17F7 Rx55[2]).	**VCC33**
PDIOW#	AR10	O	EIDE Mode: **PDIOW#:** Device write strobe UltraDMA Mode: **PSTOP:** Stop transfer. Asserted by the host prior to initiation of an UltraDMA burst; negated by the host before data is transferred in an UltraDMA burst. Assertion of PSTOP by the host during or after data transfer signals the termination of the burst. This signal has a programmable internal 19.4K ohm pull-up resistor (default enable, D17F7 Rx55[2]).	**VCC33**
PDDREQ	AT08	I	**IDE Device DMA Request.** This signal has a programmable internal 10K ohm pull-down resistor (default enable, D17F0 Rx47[0]).	**VCC33**
PDDACK#	AU11	O	**IDE Device DMA Acknowledge.** This signal has a programmable internal 19.4K ohm pull-up resistor (default enable, D17F0 Rx47[1]).	**VCC33**
PDCS1#	AN12	O	**IDE Master Chip Select.** This signal has an internal 19.4K ohm pull-up resistor.	**VCC33**
PDCS3#	AL11	O	**IDE Slave Chip Select.** PDCS3# has a programmable internal 19.4K ohm pull-up resistor (default enable, D17F0 Rx47[1]).	**VCC33**
PDA[2:0]	AM10 AN11 AP12	O	**IDE Disk Address.** PDA[2:0] are used to indicate which byte in either the ATA command block or control block is being accessed.	**VCC33**
PDD[15:0]	(see ball list)	IO	**IDE Data Bus.** PDD[7:0] have programmable internal 10K ohm pull-down resistors (default enable, D17F0 Rx47[0]).	**VCC33**
IRQ15	AR11	I	**IDE Channel Interrupt Request.** This signal has a programmable internal 19.4K ohm pull-up resistor (default enable, D17F7 Rx55[2]). If this signal is not used and the internal pull-up is enabled, then this signal can be left unconnected.	**VCC33**
IDERST#	AU14	OD	**IDE Reset Output.**	**VCC33**

Card Reader Interface

Card Reader Interface				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
CR_D[7:4] / SD_D[7:4]	AY40 AW39 AY36 AW36	IO	**Card Reader Data**	**VCCCR**
CR_D[3:0] / SD_D[3:0]	AY39 AY38 AU36 AW37	IO	**Card Reader Data**	**VCCCR**
CR_CLK / SD_CLK	AY37	O	**Card Reader Clock**	**VCCCR**
CRPWREN# / RING# / GPI8	AT29	O	**Card Reader Pad Power Enable** 0: Power on 1: Power off	**VSUS33**
SecureDigital / Multi Media Card Interface				
SD_D[7:0] / CR_D[7:0]	(see ball list)	IO	**SD/MMC Card Data**. Under SD/MMC mode, these signals have internal 19.4K ohm pull-up resistors.	**VCCCR**
CRSD_CD#	AU35	I	**SD/MMC Card Detection.** This signal has an internal 19.4K ohm pull-up resistor.	**VCCCR**
CRSD_CMD#	AV37	IO	**SD/MMC Card Command/Response.** This signal has an internal 19.4K ohm pull-up resistor.	**VCCCR**
CRSD_WPD#	AT35	I	**SD/MMC Card Write Protect Detection.** This signal has an internal 19.4K ohm pull-up resistor.	**VCCCR**
SD_CLK / CR_CLK	AY37	O	**SD/MMC Card Clock.**	**VCCCR**

Note: For details of Memory Stick / Memory Stick Pro pin confirguations, please contact VIA Technical Support Department.

SDIO Interface

SDIO Interface				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
SDIO0D[3:0]	AR39 AR38 AT40 AT39	IO	**SDIO Port 0 Data**. These signals have internal 19.4K ohm pull-up resistors.	**VCCSD0**
SDIO0CD#	AT36	I	**SDIO Port 0 Card Detection.** This signal has an internal 19.4K ohm pull-up resistor.	**VCCSD0**
SDIO0CMD#	AR40	IO	**SDIO Port 0 Command/Response.** This signal has an internal 19.4K ohm pull-up resistor.	**VCCSD0**
SDIO0WPD#	AT37	I	**SDIO Port 0 Write Protect Detection.** This signal has an internal 19.4K ohm pull-up resistor.	**VCCSD0**
SDIO0CLK	AT38	O	**SDIO Port 0 Card Clock.**	**VCCSD0**
SDIO0PSEL	AP32	O	**SDIO Port 0 Power Select.** 1: 1.8V 0: 3.3V	**VSUS33**
SDIO0POFF	AW35	O	**SDIO Port 0 Power Off.**	**VSUS33**
SDIO1D[3:0]	AU39 AU40 AU37 AV39	IO	**SDIO Port 1 Data**. These signals have internal 19.4K ohm pull-up resistors.	**VCCSD1**
SDIO1CD#	AV38	I	**SDIO Port 1 Card Detection.** This signal has an internal 19.4K ohm pull-up resistor.	**VCCSD1**
SDIO1CMD#	AU38	IO	**SDIO Port 1 Command/Response.** This signal has an internal 19.4K ohm pull-up resistor.	**VCCSD1**
SDIO1WPD#	AW40	I	**SDIO Port 1 Write Protect Detection.** This signal has an internal 19.4K ohm pull-up resistor.	**VCCSD1**
SDIO1CLK	AV40	O	**SDIO Port 1 Card Clock.**	**VCCSD1**
SDIO1PSEL	AY35	O	**SDIO Port 1 Power Select.** 1: 1.8V 0: 3.3V	**VSUS33**
SDIO1POFF	AV35	O	**SDIO Port 1 Power Off.**	**VSUS33**

LPC Bus Interface

LPC Bus Interface				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
LPCAD[3:0]	AR12 AY12 AU12 AW13	IO	**LPC Address / Data.** This signal has an internal 19.4K ohm pull-up resistor.	**VCC33**
LPCFRAME#	AY13	O	**LPC Frame.**	**VCC33**
LPCDRQ0#	AV12	I	**LPC DMA / Bus Master Request 0.** This signal has an internal 19.4K ohm pull-up resistor.	**VCC33**
LPCDRQ1#	AR13	I	**LPC DMA / Bus Master Request 1.** This signal has an internal 19.4K ohm pull-up resistor.	**VCC33**

SMBus Interface

SMBus Interface				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
SMBCK1	AV34	OD	**SMB Channel 1 Clock.** Master Mode. This signal has an internal 19.4K ohm pull-up resistor.	**VSUS33**
SMBDT1	AT33	OD	**SMB Channel 1 Data.** Master Mode. This signal has an internal 19.4K ohm pull-up resistor.	**VSUS33**
SMBCK2 / GPIO1	AY34	OD	**SMB Channel 2 Clock.** Slave Mode. This signal has an internal 19.4K ohm pull-up resistor.	**VSUS33**
SMBDT2 / GPIO0	AW34	OD	**SMB Channel 2 Data.** Slave Mode. This signal has an internal 19.4K ohm pull-up resistor.	**VSUS33**
SMBALRT#	AU34	I	**SMB Alert.** (With optional 19.4K ohm built-in pull-up resistor) Enabled by System Management Bus I/O space. When enabled, SMBALRT# assertion generates an IRQ or SMI interrupt or a power management resume event. This signal has a programmable internal 19.4K ohm pull-up resistor (default enable, D17F0 Rx97[2]). If internal pull-up is used, this signal can be left unconnected.	**VSUS33**

SPI Controller Interface

SPI Controller Interface				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
SPIDO / GPO1	AM14	O	**SPI Data Out.** Transfer data serially from SPI slave device / flash memory to SPI Controller.	**VCC33**
SPIDI / GPI0	AN14	I	**SPI Data In.** Transfer data serially from SPI Controller to SPI slave device / flash memory. This signal has an internal 19.4K ohm pull-up resistor.	**VCC33**
SPISS0# / GPO3	AN13	O	**SPI Slave Chip Select 0.** Select SPI slave device. This signal has an internal 19.4K ohm pull-up resistor.	**VCC33**
SPISS1# / GPO2	AP13	O	**SPI Slave Chip Select 1.** Select SPI slave device. This signal has an internal 19.4K ohm pull-up resistor.	**VCC33**
SPICLK / GPIO6	AT14	O	**SPI Clock.** This signal has an internal 19.4K ohm pull-up resistor.	**VCC33**

UART Interface

Two UART ports are multiplexed with either VCP or DVP1 interface.
To enable UART and disable VCP, set the following registers:
Set 3C5.78[7] = 1 and D17F0 Rx46[7]=0 and D17F0 Rx46[6]=1

UART Interface (When VCP is Disabled)				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
SOUT1 / PTS0D2 / VCPD2	AK01	O	**Transmit Data for UART Port 1.**	**VCC33**
SOUT2 / STS1VLD / VCPD9	AL05	O	**Transmit Data for UART Port 2.**	**VCC33**
SIN1 / PTS0D3 / VCPD3	AM04	I	**Receive Data for UART Port 1.**	**VCC33**
SIN2 / PTS0ERR / VCPD8	AM05	I	**Receive Data for UART Port 2.**	**VCC33**
RTS1 / PTS0D6 / VCPD6	AM01	O	**Request To Send for UART Port 1.**	**VCC33**
RTS2 / PTS0SYNC / VCPVS	AL02	O	**Request To Send for UART Port 2.**	**VCC33**
CTS1 / PTS0D7 / VCPD7	AN01	I	**Clear To Send for UART Port 1.**	**VCC33**
CTS2 / PTS0VLD / VCPHS	AL03	I	**Clear To Send for UART Port 2.**	**VCC33**
DTR1 / PTS0D4 / VCPD4	AL01	O	**Data Terminal Ready for UART Port 1.**	**VCC33**
DTR2 / STS1D / VCPD15	AM07	O	**Data Terminal Ready for UART Port 2.**	**VCC33**
DSR1 / PTS0D5 / VCPD5	AM02	I	**Data Set Ready for UART Port 1.**	**VCC33**
DSR2 / PTS0CLK / VCPCLK	AM03	I	**Data Set Ready for UART Port 2.**	**VCC33**
DCD1 / PTS0D1 / VCPD1	AL04	I	**Data Carrier Detect for UART Port 1.**	**VCC33**
DCD2 / STS1SYNC / VCPD10	AL07	I	**Data Carrier Detect for UART Port 2.**	**VCC33**
RI1 / PTS0D0 / VCPD0	AK02	I	**Ring Indicator for UART Port 1.**	**VCC33**
RI2 / STS1CLK / VCPD11	AL06	I	**Ring Indicator for UART Port 2.**	**VCC33**

To enable UART and disable DVP1, set the following registers:
Set 3C5.78[7] = 1 and D17F0 Rx46[7]=1 and D17F0 Rx46[6]=1

UART Interface (When DVP1 is Disabled)				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
SOUT1 / DVP1D10	AH04	O	**Transmit Data for UART Port 1.**	**VCC33**
SOUT2 / DVP1D2	AH08	O	**Transmit Data for UART Port 2.**	**VCC33**
SIN1 / DVP1D11	AJ04	I	**Receive Data for UART Port 1.**	**VCC33**
SIN2 / DVP1D3	AJ07	I	**Receive Data for UART Port 2.**	**VCC33**
RTS1 / DVP1D14	AK03	O	**Request To Send for UART Port 1.**	**VCC33**
RTS2 / DVP1D6	AJ06	O	**Request To Send for UART Port 2.**	**VCC33**
CTS1 / DVP1D15	AJ05	I	**Clear To Send for UART Port 1.**	**VCC33**
CTS2 / DVP1D7	AH05	I	**Clear To Send for UART Port 2.**	**VCC33**
DTR1 / DVP1D12	AJ03	O	**Data Terminal Ready for UART Port 1.**	**VCC33**
DTR2 / DVP1D4	AG08	O	**Data Terminal Ready for UART Port 2.**	**VCC33**
DSR1 / DVP1D13	AK04	I	**Data Set Ready for UART Port 1.**	**VCC33**
DSR2 / DVP1D5	AH06	I	**Data Set Ready for UART Port 2.**	**VCC33**
DCD1 / DVP1D9	AH03	I	**Data Carrier Detect for UART Port 1.**	**VCC33**
DCD2 / DVP1D1	AK07	I	**Data Carrier Detect for UART Port 2.**	**VCC33**
RI1 / DVP1D8	AK06	I	**Ring Indicator for UART Port 1.**	**VCC33**
RI2 / DVP1D0	AK08	I	**Ring Indicator for UART Port 2.**	**VCC33**

IR Interface

One IR interface is multiplexed with either VCP or DVP1 interface.
To enable IR and disable VCP, set the following registers:
Set 3C5.78[7] = 1 and D17F0 Rx46[7]=0 and D17F0 RxB0[0]=1

IR Interface (When VCP is Disabled)				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
IRTX / STS1ERR / VCPD12	AM06	O	**Infrared Transmit Data.**	**VCC33**
IRRX / VCPD13	AL08	I	**Infrared Receive Data.**	**VCC33**
IRRX2 / **ITMOFF** / VCPD14	AM08	IO	**Input Mode: Infrared Receive Data 2** **Output Mode: Infrared Module Off**	**VCC33**
IRSCLK	AJ02	O	**Infrared Transceiver Clock.**	**VCC33**

To enable IR and disable DVP1, set the following registers:
Set 3C5.78[7] = 1 and D17F0 Rx46[7]=1 and D17F0 RxB0[0]=1

IR Interface (When DVP1 is Disabled)				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
IRTX / DVP1HS	AJ08	O	**Infrared Transmit Data.**	**VCC33**
IRRX / DVP1VS	AG07	I	**Infrared Receive Data.**	**VCC33**
IRRX2 / **ITMOFF** / DVP1DE	AH02	IO	**Input Mode: Infrared Receive Data 2** **Output Mode: Infrared Module Off**	**VCC33**
IRSCLK	AJ02	O	**Infrared Transceiver Clock.**	**VCC33**

High Definition Audio Interface

High Definition Audio Interface				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
AZRST#	AT34	O	**High Definition Audio Reset.**	**VSUS33**
AZBITCLK	AM13	O	**High Definition Audio Bit Clock.** 24.00 MHz.	**VCC33**
AZSYNC	AL13	O	**High Definition Audio Sync.** 48 KHz Frame Sync and outbound tag signal.	**VCC33**
AZSDOUT	AL14	O	**High Definition Audio Serial Data Output.**	**VCC33**
AZSDIN[2:0]	AN32 AN33 AP33	IO	**High Definition Audio Serial Data Input.** These signals have internal 10K ohm pull-down resistor. Tie to GND if not used.	**VSUS33**

Speaker Interface

Speaker Interface				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
SPKR / SATALED1# / GPO7	AR15	O	**Speaker Out.**	**VCC33**

Trusted Platform Module Signal Descriptions

Trusted Platform Module (TPM)				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
TCSEN#	AT12	I	**Trusted Configuration Space Enable.** This signal has an internal 19.4K ohm pull-up resistor. If this signal is not used, leave it unconnected.	**VCC33**

Serial IRQ Interface

Serial IRQ Interface				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
SERIRQ	AW12	IO	**Serial IRQ.** This signal has an internal 19.4K ohm pull-up resistor. If this signal is not used, leave it unconnected.	**VCC33**

PC / PCI DMA Interface

PC / PCI DMA Interface				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
PCIDREQ# / GPIO8	AN03	I	**PC / PCI DMA Request.** This signal has an internal 19.4K ohm pull-up resistor. If this signal is not used, leave it unconnected.	**VCC33**
PCIDGNT# / GPIO9	AN04	O	**PC / PCI DMA Grant.** This signal has an internal 19.4K ohm pull-up resistor.	**VCC33**

Internal Keyboard Controller Interface

Internal Keyboard Controller Interface				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
MSCK / IRQ1	AV33	IO	**Mouse Clock.** From internal mouse controller. This signal has an internal 19.4K ohm pull-up resistor.	**VSUS33**
MSDT / IRQ12	AU33	IO	**Mouse Data.** From internal mouse controller. This signal has an internal 19.4K ohm pull-up resistor.	**VSUS33**
KBCK / A20GATE / GPIO5	AR34	IO	**Keyboard Clock.** From internal keyboard controller. This signal has an internal 19.4K ohm pull-up resistor. This signal is used as A20GATE to connect to external keyboard controller's A20Gate signal if external KBC is used.	**VSUS33**
KBDT / KBC_CPURST# / GPIO4	AR33	IO	**Keyboard Data.** From internal keyboard controller. This signal has an internal 19.4K ohm pull-up resistor. This signal is used as KBC_CPURST# to connect to external keyboard controller's CPURST# signal if external KBC is used.	**VSUS33**

General Purpose Input Interface

General Purpose Input Interface – Signal Attributes										
Signal Name	**Ball #**	**I/O**	**Default Function**	**Signal State**					**Interrupt Triggered by GPI**	**Power Plane**
				Reset	**After Reset**	**POS**	**STR**	**STD**		
GPI0 / SPIDI	AN14	I	SPIDI	SPIDI	SPIDI	SPIDI	Off	Off	SCI/SMI	VCC33
GPI1	AW30	I	GPI	Driven	Driven	Driven	Driven	Driven	SCI/SMI	VSUS33
GPI2 / WAKE#	AV31	I	GPI2	Static	Driven	Driven	Driven	Driven	SCI/SMI	VSUS33
GPI4 / BATLOW#	AR32	I	GPI4	Static	Driven	Driven	Driven	Driven	No	VSUS33
GPI5 / EXTSMI#	AR30	I	GPI5	Static	Driven	Driven	Driven	Driven	No	VSUS33
GPI6 / INTRUDER#	AW31	I	GPI6	Static	Driven	Driven	Driven	Driven	No	VBAT
GPI7 / LID#	AU31	I	GPI7	Static	Driven	Driven	Driven	Driven	No	VSUS33
GPI8 / RING# / CRPWREN#	AT29	I	GPI8	Static	Driven	Driven	Driven	Driven	No	VSUS33
GPI9 / THRM#	AN15	I	GPI9	Static	Driven	Driven	Off	Off	No	VCC33

GPI Signal States:

1. **Static**: The input signal must remain static, either high or low.
2. **Driven**: The input signal is driven from outside. It is allowed to change.
3. **Off**: The power plane of the input signal is off.

System States:

1. **Reset**: During <RSMRST#, PCIRST1#, PCIRST0#> is <0, 0, 0>
2. **After Reset**: Immediately after <RSMRST#, PCIRST1#, PCIRST0#> is <1, 1, 1>

Timing Duration of GPI Pins for SCI/SMI Driven and S3/S4 Wakeup:

	SCI Sample Clock	**Duration for SCI Driven**	**Min. Academic Latency**
GPI0	32KHz	62.5us	125us
GPI1	33MHz	120ns	180ns
GPI2	33MHz	120ns	180ns

	SMI Sample Clock	**Duration for SMI Driven**	**Min. Academic Latency**
GPI0	32KHz	62.5us	125us
GPI1	33MHz	120ns	150ns
GPI2	33MHz	120ns	150ns

	S3/S4 Sample Clock	**Duration for S3/S4 Wakeup**	**Min. Academic Latency**
GPI0	32KHz	62.5us	125us
GPI1	32KHz	62.5us	125us
GPI2	32KHz	62.5us	125us

General Purpose Input Interface – Signal Control Registers				
Signal Name	**Control Register**	**GPI Status Register**	**GPI SCI/SMI Register**	**Status Change Register**
GPI0	D17F0 RxE4[1] = 1	PMIO Rx48[0]	PMIO Rx24[0] = 1, PMIO Rx22[0] = 1	PMIO Rx20[0]
GPI1	N/A	PMIO Rx48[1]	PMIO Rx24[1] = 1, PMIO Rx22[1] = 1	PMIO Rx20[1]
GPI2	D17F0 RxE2[1] = 0	PMIO Rx48[2]	PMIO Rx52[0] = 1, D17F0 RxE0[0], D17F0 RxE1[0]	PMIO Rx50[0]
GPI4	PMIO Rx25[4] = 0, PMIO Rx23[4] = 0	PMIO Rx48[4]	N/A	N/A
GPI5	PMIO Rx24[4] = 0, PMIO Rx22[4] = 0	PMIO Rx48[5]	N/A	N/A
GPI6	PMIO Rx24[6] = 0, PMIO Rx22[6] = 0	PMIO Rx48[6]	N/A	N/A
GPI7	PMIO Rx25[3] = 0, PMIO Rx23[3] = 0	PMIO Rx48[7]	N/A	N/A
GPI8	D17F0 Rx9F[7] = 1, PMIO Rx25[0] = 0, PMIO Rx23[0] = 0	PMIO Rx49[0]	N/A	N/A
GPI9	PMIO Rx25[2] = 0, PMIO Rx23[2] = 0, D17F0 Rx8C[3] = 0	PMIO Rx49[1]	N/A	N/A

General Purpose Output Interface

General Purpose Output Interface – Signal Attributes										
Signal Name	**Ball #**	**I/O**	**Default Function**	**Signal State Before Programming GPO**			**Signal State After Programming GPO**			**Power Plane**
				Resume Reset	**Reset**	**After Reset**	**Before Reset**	**Reset**	**After Reset**	
GPO0 / SUSA#	AY31	O	SUSA#	Floating	1	1	Defined	Defined	Defined	VSUS33
GPO1 / SPIDO	AM14	O	SPIDO	Not fixed	0	0	Defined	0	0	VCC33
GPO2 / SPISS1#	AP13	O	SPISS1#	Not fixed	1	1	Defined	1	1	VCC33
GPO3 / SPISS0#	AN13	O	SPISS0#	Not fixed	1	1	Defined	1	1	VCC33
GPO4 / SATALED0#	AV14	O	SATALED0#	Not fixed	1	1	Defined	1	1	VCC33
GPO5 / CSTATE1	AT15	O	CSTATE1	Not fixed	1	0	Defined	1	0	VCC33
GPO6 / C4PSTOP#	AR14	O	C4PSTOP#	Not fixed	1	1	Defined	1	1	VCC33
GPO7 / SPKR / SATALED1#	AR15	O	SPKR	Not fixed	Floating	0	Defined	Floating	0	VCC33
GPO8 / SUSB#	AP30	O	SUSB#	0	1	1	Defined	Defined	Defined	VSUS33
GPO9 / SUSC#	AP31	O	SUSC#	0	1	1	Defined	Defined	Defined	VSUS33
GPO10 / SYSIDLE	AP15	O	SYSIDLE	Not fixed	1	0	Defined	1	0	VCC33

GPO Signal States:

1. **High-Z**: Tri-State.
2. **High**: The output signal is logic "1".
3. **Low**: The output signal is logic "0".
4. **Defined**: The output signal can be high or low, defined by the GPO function.
5. **Undefined**: The output signal is undetermined.
6. **Off**: The power plane of output signal is off.

System States:

1. **Reset**: During <RSMRST#, PCIRST1#, PCIRST0#> is <0, 0, 0>
2. **After Reset**: Immediately after <RSMRST#, PCIRST1#, PCIRST0#> is <1, 1, 1>

General Purpose Output Interface – Signal Control Registers		
Signal Name	**Control Register**	**GPO Output Register**
GPO0	D17F0 Rx9F[2] = 1	PMIO Rx4C[0]
GPO1	D17F0 RxE4[1] = 1	PMIO Rx4C[1]
GPO2	D17F0 RxE4[1] = 1	PMIO Rx4C[2]
GPO3	D17F0 RxE4[1] = 1	PMIO Rx4C[3]
GPO4	D17F0 RxE4[2] = 1	PMIO Rx4C[4]
GPO5	D17F0 RxE4[5] = 1	PMIO Rx4C[5]
GPO6	D17F0 RxE4[5] = 1	PMIO Rx4C[6]
GPO7	D17F0 RxE4[4] = 1	PMIO Rx4C[7]
GPO8	D17F0 Rx94[2] = 1	PMIO Rx4D[0]
GPO9	D17F0 Rx94[2] = 1	PMIO Rx4D[1]
GPO10	D17F0 RxE4[6] = 1	PMIO Rx4D[2]

General Purpose Input/Output Interface

General Purpose Input/Output Interface – Signal Attributes										
Signal Name	**Ball #**	**I/O**	**Default Function**	**Signal State Before Programming GPO**			**Signal State After Programming GPO**			**Power Plane**
				Resume Reset	**Reset**	**After Reset**	**Before Reset**	**Reset**	**After Reset**	
GPIO0 / SMBDT2	AW34	IO	SMBDT2	1	1	1	Defined	Defined	Defined	VSUS33
GPIO1 / SMBCK2	AY34	IO	SMBCK2	1	1	1	Defined	Defined	Defined	VSUS33
GPIO4 / KBDT / KBC_CPURST#	AR33	IO	KBDT KBC_CPURST#	1	1	1	Defined	Defined	Defined	VSUS33
GPIO5 / KBCK / A20GATE	AR34	IO	KBCK A20GATE	1	1	1	Defined	Defined	Defined	VSUS33
GPIO6 / SPICLK	AT14	IO	SPICLK	Not fixed	0	0	Defined	0	0	VCC33
GPIO7 / THRMTRIP#	G17	IO	THRMTRIP#	Not fixed	1	1	Defined	1	1	VTT
GPIO8 / PCIDREQ#	AN03	IO	PCIDREQ#	Not fixed	1	1	Defined	1	1	VCC33
GPIO9 / PCIDGNT#	AN04	IO	PCIDGNT#	Not fixed	1	1	Defined	1	1	VCC33
GPIO10 / PCIERST0#	AT13	IO	GPIO10	Not fixed	0	1	Defined	0	1	VCC33
GPIO11 / PCIERST1#	AU13	IO	GPIO11	Not fixed	0	1	Defined	0	1	VCC33
GPIO12	AV13	IO	GPIO12	Not fixed	1	1	Defined	1	1	VCC33
GPIO13	AP14	IO	GPIO13	Not fixed	1	1	Defined	1	1	VCC33

Graphics General Purpose Input/Output Signals				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
VIDEO_GPIO2 / DISPCLKI0	AJ01	IO	**Graphics General Purpose I/O.**	VCC33
VIDEO_GPIO3 / DISPCLKO0	AH01	IO	**Graphics General Purpose I/O.**	VCC33
VIDEO_GPIO4 / DISPCLKI1	AG05	IO	**Graphics General Purpose I/O.**	VCC33
VIDEO_GPIO5 / DISPCLKO1	AG04	IO	**Graphics General Purpose I/O.**	VCC33

General Purpose Input/Output Interface – Signal Registers					
Signal Name	**Control Register**	**GPI Status Register**	**GPI SCI/SMI Register**	**GPI Status Change Register**	**GPO Output Register**
GPIO0	D17F0 Rx95[3] = 1, D17F0 Rx95[2] = 1	PMIO Rx49[2]	PMIO Rx52[2] = 1, D17F0 RxE0[2], D17F0 RxE1[2]	PMIO Rx50[2]	PMIO Rx4D[3]
GPIO1	D17F0 Rx95[3] = 1, D17F0 Rx95[2] = 1	PMIO Rx49[3]	PMIO Rx52[3] = 1, D17F0 RxE0[3], D17F0 RxE1[3]	PMIO Rx50[3]	PMIO Rx4D[4]
GPIO4	D17F0 Rx97[0] = 1	PMIO Rx49[6]	N/A	N/A	PMIO Rx4D[7]
GPIO5	D17F0 Rx97[0] = 1	PMIO Rx49[7]	N/A	N/A	PMIO Rx4E[0]
GPIO6	D17F0 RxE4[1] = 1	PMIO Rx4A[0]	N/A	N/A	PMIO Rx4E[1]
GPIO7	PMIO Rx2B[1] = 0	PMIO Rx4A[1]	N/A	N/A	PMIO Rx4E[2]
GPIO8	D17F0 Rx53[7] = 0	PMIO Rx4A[2]	N/A	N/A	PMIO Rx4E[3]
GPIO9	D17F0 Rx53[7] = 0	PMIO Rx4A[3]	N/A	N/A	PMIO Rx4E[4]
GPIO10	D17F0 RxFC[3] = 1	PMIO Rx4A[4]	PMIO Rx52[4] = 1, D17F0 RxE0[4], D17F0 RxE1[4]	PMIO Rx50[4]	PMIO Rx4E[5]
GPIO11	D17F0 RxFC[4] = 1	PMIO Rx4A[5]	PMIO Rx52[5] = 1, D17F0 RxE0[5], D17F0 RxE1[5]	PMIO Rx50[5]	PMIO Rx4E[6]
GPIO12	N/A	PMIO Rx4A[6]	PMIO Rx52[6] = 1, D17F0 RxE0[6], D17F0 RxE1[6]	PMIO Rx50[6]	PMIO Rx4E[7]
GPIO13	N/A	PMIO Rx4A[7]	PMIO Rx52[7] = 1, D17F0 RxE0[7], D17F0 RxE1[7]	PMIO Rx50[7]	PMIO Rx4F[0]

Power Management Control and Event Signals

Power Management Control and Event Signals				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
PWRBTN#	AR31	I	**Power Button.** Used by the Power Management subsystem to monitor an external system on/off button or switch. Internal logic powered by VSUS33. This signal has a programmable internal 19.4K ohm pull-up resistor (default enable, D17F0 Rx97[2]). If internal pull-up is used, this signal can be left unconnected.	**VSUS33**
EXTSMI# / GPI5	AR30	IO	**External System Management Interrupt.** When enabled, a falling edge on this input causes an SMI# to be generated to the CPU to enter SMI mode. This signal has an internal 19.4K ohm pull-up resistor.	**VSUS33**
PME#	AT31	I	**Power Management Event.** This signal has an internal 19.4K ohm pull-up resistor. If this signal is not used, leave it unconnected.	**VSUS33**
LID# / GPI7	AU31	I	**Notebook Computer Display Lid Open / Closed Monitor.** Used by the Power Management subsystem to monitor the opening and closing of the display lid of notebook computers. Can be used to detect either low-to-high or high-to-low transitions to generate an SMI#. This signal has an internal 19.4K ohm pull-up resistor. If this signal is not used, leave it unconnected.	**VSUS33**
WAKE# / GPI2	AV31	I	**Wake.** Indicates that a system wake event has occurred. Used to waken the chip from deep sleep mode (S3 / S4 / S5 states). Wire-OR with PEWAKE# on the PCI Express bus connector. This signal has an internal 19.4K ohm pull-up resistor. If this signal is not used, leave it unconnected.	**VSUS33**
INTRUDER# / GPI6	AW31	I	**Intrusion Indicator.**	**VBAT**
THRM# / GPI9	AN15	I	**Thermal Alarm Monitor.** This signal is to enable the throttling mode of the STPCLK# signal for thermal control. This signal has an internal 19.4K ohm pull-up resistor. If this signal is not used, leave it unconnected.	**VCC33**
RING# / CRPWREN# / GPI8	AT29	I	**Ring Indicator.** May be connected to external modem circuitry to allow the system to be re-activated by a received phone call. This signal has a programmable internal 19.4K ohm pull-up resistor (default enable, D17F0 Rx94[3]). If this signal is not used and the internal pull-up is enabled, leave it unconnected.	**VSUS33**
BATLOW# / GPI4	AR32	I	**Battery Low Indicator.** This signal has an internal 19.4K ohm pull-up resistor. If it is not used, leave it unconnected.	**VSUS33**

Power Management Control and Event Signals - continued				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
CPUSTP#	AW14	O	**CPU Clock Stop.** Signals the system clock generator to disable the CPU clock outputs. This signal has an internal 19.4K ohm pull-up resistor.	**VCC33**
PCISTP#	AY14	O	**PCI Clock Stop.** Signals the system clock generator to disable the PCI clock outputs. This signal has an internal 19.4K ohm pull-up resistor.	**VCC33**
SUSA# / GPO0	AY31	O	**Suspend Plane A Control**. Asserted during power management POS, STR, and STD suspend states. Used to control the primary power plane.	**VSUS33**
SUSB# / GPO8	AP30	O	**Suspend Plane B Control**. Asserted during power management STR and STD suspend states. Used to control the secondary power plane.	**VSUS33**
SUSC# / GPO9	AP31	O	**Suspend Plane C Control.** Asserted during power management STD suspend state. Used to control the tertiary power plane. Also connected to ATX power-on circuitry.	**VSUS33**
CLKRUN#	AM15	IO	**PCI Clock Run.** Suspend PCICLK when CLKRUN# is high. See PCI Specification for CLKRUN# protocol. This signal has an internal 19.4K ohm pull-up resistor.	**VCC33**
SYSIDLE / GPO10	AP15	O	**System Idle.** High indicates system is in idle/S0 state. This signal has an internal 19.4K ohm pull-up resistor.	**VCC33**
CSTATE1 / GPO5	AT15	O	**CState 1.** This signal has an internal 19.4K ohm pull-up resistor.	**VCC33**
C4PSTOP# / GPO6	AR14	O	**C4P Stop.** When the C4P sleep state is entered, the internal PLL is turned off. Connect to clock generator to stop host, graphics (66MHz), USB (48MHz) and SATA (25MHz) clock source. This signal has an internal 19.4K ohm pull-up resistor.	**VCC33**
VRDSLP	AV15	O	**Voltage Regulator Deep Sleep.** Connected to the CPU voltage regulator. High selects the proper voltage for deep sleep mode. This signal has an internal 19.4K ohm pull-up resistor. If it is not used, leave it unconnected.	**VCC33**

Clock, Test and Miscellaneous Signals

Clock, Test and Miscellaneous Signals				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
Clock Signals of Graphics & Video Processors				
DISPCLKI0 / VIDEO_GPIO2	AJ01	I	**SSC Dot Clock 0 (Pixel Clock) In.** DISPCLKI0 can optionally be used as VIDEO_GPIO2 (Graphics GPIO pin). Please refer to the "Graphics General Purpose Input/Output Signals" table for details.	**VCC33**
DISPCLKO0/ VIDEO_GPIO3	AH01	O	**Dot Clock 0 (Pixel Clock) Out.** DISPCLKO0 can optionally be used as VIDEO_GPIO3 (Graphics GPIO pin). Please refer to the "Graphics General Purpose Input/Output Signals" table for details.	**VCC33**
DISPCLKI1 / VIDEO_GPIO4	AG05	I	**SSC Dot Clock 1 (Pixel Clock) In.** DISPCLKI1 can optionally be used as VIDEO_GPIO4 (Graphics GPIO pin). Please refer to the "Graphics General Purpose Input/Output Signals" table for details.	**VCC33**
DISPCLKO1 / VIDEO_GPIO5	AG04	O	**Dot Clock 1 (Pixel Clock) Out.** DISPCLKO1 can optionally be used as VIDEO_GPIO5 (Graphics GPIO pin). Please refer to the "Graphics General Purpose Input/Output Signals" table for details.	**VCC33**
GCLK	H16	I	**Graphics Clock (66Mhz).**	**VTT**
XIN	AF08	I	**14.31818MHz Reference Frequency Input.** External 14.31818 MHz clock source. All internal graphics controller clocks and internal timer are synthesized on chip using this frequency as a reference.	**VCC33**
RTC Crystal Interface				
RTCXI	AY29	I	**RTC Crystal Input**: 32.768 KHz Crystal Input.	**VBAT**
RTCXO	AW29	O	**RTC Crystal Output**: 32.768 KHz Crystal Output.	**VBAT**
Power State and System Reset				
PWRGD	AT30	I	**Power Good.** Connected to the Power Good signal on the Power Supply. Internal logic powered by VBAT.	**VBAT**
RSMRST#	AU30	I	**Resume Reset.** When asserted, this signal resets the VX800 Series and sets all register bits to the default value. The rising edge of this signal is used to sample all power-up strap options	**VBAT**
Test and Miscellaneous Signals				
TESTIN	J27	I	**Test In.** This signal is used for testing. Tie to GND for normal system operation.	**VTT**
DFTIN	J26	I	**DFT In.** This signal is used for testing. Tie to GND for normal system operation.	**VTT**
BISTIN	J25	I	**BIST In.** This signal is used for testing. Tie to GND for normal system operation.	**VTT**
TP[3:1]	J22 J21 J20	-	**Test Pad.**	**VTT**
TP[6:4]	AK09 AL12 AL15	-	**Test Pad.**	**VCC33**
TP7	AN31	-	**Test Pad.**	**VSUS33**
TP8	AN30	-	**Test Pad.**	**VBAT**

Compensation Signals

Compensation				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
HGTLCOMPP	B29	AI	**AGTL P Compensation.**	**VTT**
HGTLCOMPN	A29	AI	**AGTL N Compensation.**	**VTT**
MEMCOMP	A30	AI	**DRAM Compensation.**	**VCC18MEM**
SATAR50COMP	AR27	AI	**Serial ATA Auto Compensation.** If SATA interface is not needed, leave it unconnected.	**VCCA33SATA**

Reference Voltage Signals

Reference Voltages			
Signal Name	**Ball #**	**I/O**	**Signal Description**
HGTLVREF[1:0]	H11, H25	AI	**Host CPU Interface AGTL+ Voltage Reference.** Set it to 2/3 of VTT.
MEMVREF	U33	AI	**Memory Voltage Reference.** Set it to 1/2 of VCC18MEM.

Power / Ground Signals

Digital Power / Ground		
Signal Name	**Ball #**	**Signal Description**
VTT	(see ball list)	**I/O Power for CPU Interface.** 1.05V ±5%
VCC18MEM	(see ball list)	**I/O Power for Memory Interface.** 1.8V (DDR2) ±5%.
VSUS15MEM	B30	**Suspend Power for Memory Module.** ***VX800:*** 1.5V ±5% ***VX800UT:*** 1.25V ±5%
VCC15	(see ball list)	**Core Power.** This supply is turned on only when the mechanical switch on the power supply is turned on and the PWRON signal is conditioned high. ***VX800:*** 1.5V ±5% ***VX800UT:*** 1.25V ±5%
VSUS15	(see ball list)	**Suspend Power.** ***VX800:*** 1.5V ±5% ***VX800UT:*** 1.25V ±5%
VSUS33	(see ball list)	**Suspend Power.** Always available unless the mechanical switch of the power supply is turned off. If the "soft-off" state is not implemented, then these signal balls can be connected to VCC33. 3.3V ±5%.
VSUS15PEX	(see ball list)	**PCI Express Suspend Power.** ***VX800:*** 1.5V ±5%. ***VX800UT:*** 1.25V ±5%.
VCC33PEX	(see ball list)	**Power for PCI Express I/O Interface Logic.** 3.3V ±5%.
VCC33	(see ball list)	**I/O Power.** 3.3V ±5%
VBAT	AV30	**RTC Battery.** Battery input for internal RTC (RTCXI, RTCXO).
GND	(see ball list)	**Ground.** Connect to primary motherboard ground plane.
VSUS15USB	AP23	**Suspend Power for USB.** ***VX800:*** 1.5V ±5%. ***VX800UT:*** 1.25V ±5%.
VSUS33USB	(see ball list)	**Suspend Power for USB Interface.** 3.3V ±5%.
GNDUSB	(see ball list)	**Ground for USB.**
VCC33LVDS	(see ball list)	**Power for LVDS Transmitter.** 3.3V ±5%.
GNDLVDS	(see ball list)	**Ground for LVDS Transmitter.**

Analog Power / Ground		
Signal Name	**Ball #**	**Signal Description**
Host Interface		
VCCA33HCK	C29	**Power for Host CPU Clock PLL.** 3.3V ±5%.
GNDAHCK	D29	**Ground for Host CPU Clock PLL.**
PCI Express Interface		
VCCA33PE1	(see ball list)	**Power for PCI Express PHY PLL.** 3.3V ±5%.
GNDA33PE1	(see ball list)	**Ground for PCI Express PHY PLL.**
VCCA33PE2	(see ball list)	**Power for PCI Express EPLL.** 3.3V ±5%.
GNDA33PE2	(see ball list)	**Ground for PCI Express EPLL.**
Graphics and Video		
VCCA33PLL[3:1]	AG03 AF04 AF05	**Power for Graphics Controller PLL.** 3.3V ±5%.
GNDA33PLL[3:1]	AE07 AF07 AF06	**Ground for Graphics Controller PLL.**
VCCA33DAC[2:1]	AG02 AG01	**Power for DAC.** 3.3V ±5%.
GNDA33DAC[3:1]	AF03 AE03 AE04	**Ground for DAC.**
LVDS Transmitter		
VCCA33PLLLVDS[2:1]	U04 T04	**LVDS PLL Power.** 3.3V ±5%
GNDA33PLLLVDS[2:1]	V05 T05	**LVDS PLL Ground.**
VCCA33LVDS	V04	**LVDS Analog Power.** 3.3V ±5%
GNDALVDS	U05	**LVDS Analog Ground.**
SATA Controller		
VCCA15SATA	(see ball list)	**SATA Analog Power.** 1.5V ±5%.
GNDA15SATA	(see ball list)	**SATA Analog Ground.**
VCCA33SATA	(see ball list)	**SATA Analog Power.** 3.3V ±5%.
GNDA33SATA	(see ball list)	**SATA Analog Ground.**
VCCA33PLLSATA	(see ball list)	**SATA PLL Analog Power.** 3.3V ±5%.
GNDAPLLSATA	(see ball list)	**SATA PLL Analog Ground.**
USB Controller		
VCCA15PLLUSB	AR19	**USB PLL Analog Voltage.** ***VX800:*** 1.5V ±5% ***VX800UT:***1.25V ±5%
VCCA33PLLUSB	AR18	**USB PLL Analog Voltage.** 3.3V ±5%.
SDIO Interface		
VCCSD0	AE26	**I/O Power for SDIO Port 0.** 1.8/3.3V ±5%.
VCCSD1	AE27	**I/O Power for SDIO Port 1.** 1.8/3.3V ±5%.
Card Reader Interface		
VCCCR	AF27	**I/O Power for Card Reader.** 3.3V ±5%.

Multiplexed Interface Tables

VCP Multiplexed Signals				
Ball#	**Video Capture Port**	**Transport Stream Input Mode** (8-bit Parallel + Serial)	**UART Interface**	**IR Interface**
AK02	VCPD0	PTS0D0	RI1	-
AL04	VCPD1	PTS0D1	DCD1	-
AK01	VCPD2	PTS0D2	SOUT1	-
AM04	VCPD3	PTS0D3	SIN1	-
AL01	VCPD4	PTS0D4	DTR1	-
AM02	VCPD5	PTS0D5	DSR1	-
AM01	VCPD6	PTS0D6	RTS1	-
AN01	VCPD7	PTS0D7	CTS1	-
AM05	VCPD8	PTS0ERR	SIN2	-
AL05	VCPD9	STS1VLD	SOUT2	-
AL07	VCPD10	STS1SYNC	DCD2	-
AL06	VCPD11	STS1CLK	RI2	-
AM06	VCPD12	STS1ERR	-	IRTX
AL08	VCPD13	-	-	IRRX
AM08	VCPD14	-	-	IRRX2 / ITMOFF
AM07	VCPD15	STS1D	DTR2	-
AL03	VCPHS	PTS0VLD	CTS2	-
AL02	VCPVS	PTS0SYNC	RTS2	-
AM03	VCPCLK	PTS0CLK	DSR2	-
AJ02	-	-	-	IRSCLK

DVP Multiplexed Signals			
Ball#	Digital Video Port 1	UART Interface	IR Interface
AK08	DVP1D0	RI2	-
AK07	DVP1D1	DCD2	-
AH08	DVP1D2	SOUT2	-
AJ07	DVP1D3	SIN2	-
AG08	DVP1D4	DTR2	-
AH06	DVP1D5	DSR2	-
AJ06	DVP1D6	RTS2	-
AH05	DVP1D7	CTS2	-
AK06	DVP1D8	RI1	-
AH03	DVP1D9	DCD1	-
AH04	DVP1D10	SOUT1	-
AJ04	DVP1D11	SIN1	-
AJ03	DVP1D12	DTR1	-
AK04	DVP1D13	DSR1	-
AK03	DVP1D14	RTS1	-
AJ05	DVP1D15	CTS1	-
AJ08	DVP1HS	-	IRTX
AG07	DVP1VS	-	IRRX
AH02	DVP1DE	-	IRRX2 / ITMOFF
AK05	DVP1TVFLD	-	-
AG06	DVP1CLK	-	-
AH07	DVP1TVCLKR	-	-
AD04	DVP1SPD	-	-
AD03	DVP1SPCLK	-	-
AJ02	-	-	IRSCLK

Card Reader Multiplexed Signals		
Ball#	Card Reader Interface	SD / MMC Interface
AY40	CR_D7	SD_D7
AW39	CR_D6	SD_D6
AY36	CR_D5	SD_D5
AW36	CR_D4	SD_D4
AY39	CR_D3	SD_D3
AY38	CR_D2	SD_D2
AU36	CR_D1	SD_D1
AW37	CR_D0	SD_D0
AY37	CR_CLK	SD_CLK

Strapping Signal Table

Strapping Signal (External pull-up / pulldown straps are required to select "H" / "L". "X" means the strapping is ignored.)			
Signal	**Ball #**	**Function**	**Description**
GPIO12: CSTATE1	AV13: AT15	**FSB Clock**	State (GPIO12:CSTATE1) Mode (MHz) LL 100 MHz LH 133 MHz *(VX800UT)* HL 200 MHz *(VX800)* HH Auto
SYSIDLE	AP15	**IO Queue Depth**	L: 12-level deep H: 1-level deep
GPIO13	AP14	**GTL Pull-up**	L: Enable internal GTL Pull-up H: Disable internal GTL Pull-up
PDA0	AP12	**Reserved**	Always strapped LOW
PDA1	AN11	**Dual Processor Configuration**	L: Single Processor H: Dual Processor
PDA2	AM10	**PLL_OK Source Selection**	L: PLL_OK from PLL H: PLL_OK from logic counter
AZSDOUT	AL14	**Auto Reboot**	L: Enable H: Disable
AZSYNC	AL13	**LPC FWH Command**	L: Enable H: Disable
AZBITCLK	AM13	**SPI / LPC ROM Select**	L: LPC ROM H: SPI ROM
SPISS[1:0]#	AP13 AN13	**IDE Controller**	State (SPISS[1:0]#) Mode LL IDE Others Reserved
TP8	AN30	**Reserved**	Always strapped LOW.
INTRUDER#	AW31	**Reserved**	Always strapped HIGH.
VCPD[10:9,7:6]	AL07 AL05 AN01 AM01	**Reserved**	Always strapped LOW.

Note: Please refer to Figure 14 for detailed strapping timing.

Summary of IO Pads with Integrated Pull-Up/Pull-Down Resistors

The VX800 Series IO pads, as listed below, are integrated with internal 19.4K ohm ± 30% pull-up or 10K / 15 K ohm ± 30% pull-down resistor to reduce component counts on the motherboards.

IO pads with internal pull-up:

- CPU control interface: FERR#, STPCLK#
- PCI interface: FRAME#, TRDY#, IRDY#, STOP#, DEVSEL#, PERR#, SERR#, INT[A, B, C, D]#, REQ[3:0]#, GNT[3:0]#
- LPC interface: LPCAD[3:0], LPCDRQ0#, LPCDRQ1#
- PS/2 interface: MSCK, MSDT, KBCK, KBDT
- Serial IRQ interface: SERIRQ
- SecureDigital / Multi Media Card interface: SD_D[7:0], CRSD_CD#, CRSD_CMD#, CRSD_WPD#
- SDIO interface: SDIO0D[3:0], SDIO0CD#, SDIO0CMD#, SDIO0WPD#, SDIO1D[3:0], SDIO1CD#, SDIO1CMD#, SDIO1WPD#
- SPI Controller interface: SPIDI, SPISS0#, SPISS1#, SPICLK
- Trusted Platform Module interface: TCSEN#
- PC / PCI DMA interface: PCIDREQ#, PCIDGNT#
- EIDE interface: PDIORDY, PDIOR#, PDIOW#, PDDACK#, PDCS1#, PDCS3#, IRQ15
- SMBus interface: SMBCK1, SMBDT1, SMBCK2, SMBDT2, SMBALRT#
- Power management event signals: BATLOW#, THRM#, PME#, RING#, EXTSMI#, LID#, PWRBTN#, WAKE#, CPUSTP#, PCISTP#, CLKRUN#, SYSIDLE, C4PSTOP#, CSTATE1, VRDSLP

IO pads with internal pull-down:

- USB interface: USBP[5:0]+/–
- EIDE interface: PDDREQ, PDD[7:0]
- High Definition Audio interface: AZSDIN[2:0]

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Table 8. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes
T_C	Operating case temperature	0	95	^oC	1
T_S	Storage temperature	–55	125	^oC	1
V_{IN}	Input voltage	0	V_{RAIL} + 10%	Volts	1, 2
V_{OUT}	Output voltage	0	V_{RAIL} + 10%	Volts	1, 2

Note:

1. Stress above the conditions listed may cause permanent damage to the device. Functional operation of this device should be restricted to the conditions described under operating conditions.
2. V_{RAIL} is defined as the V_{CC} level of the respective rail. Memory is 1.8V (DDR2). Graphics / Display is 3.3V.

Electrical Characteristics – Clock

Table 9. Electrical Characteristics - HCLK

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
HCLK Long Accuracy	ppm	See Tperiod min-max values	-300	300	ppm
HCLK Frequency	F_{HCLK}	Freq = 100Mhz	–	100.03	MHz
Clock Period	T_{PERIOD}	Freq = 100Mhz	9.997	–	ns
HCLK Frequency	F_{HCLK}	Freq = 100Mhz, SSC -0.5%	–	100.03	MHz
Clock Period	T_{PERIOD}	Freq = 100Mhz, SSC -0.5%	9.997	–	ns
HCLK Jitter – Cycle to Cycle	TJ_{C2C}	Freq = 100MHz Differential Measurement	–	200	ps
HCLK Frequency	F_{HCLK}	Freq = 200Mhz	–	200.06	MHz
Clock Period	T_{PERIOD}	Freq = 200Mhz	4.998	–	ns
HCLK Frequency	F_{HCLK}	Freq = 200Mhz, SSC -0.5%	–	200.06	MHz
Clock Period	T_{PERIOD}	Freq = 200Mhz, SSC -0.5%	4.998	–	ns
HCLK Jitter – Cycle to Cycle	TJ_{C2C}	Freq = 200MHz Differential Measurement	–	150	ps
Input Voltage High	V_H	Statistical measurement on single ended signal	660	850	mV
Input Voltage Low	V_L	Statistical measurement on single ended signal	-150	–	mV
Maximum Input Voltage	V_{OVS}	Measurement on single ended signal using absolute	–	1150	mV
Minimum Input Voltage	V_{UDV}	Measurement on single ended signal using absolute	-300	–	mV
Crossing Point Voltage	V_{XABS}	Single-ended Measurement	250	550	mV
Crossing Point Variation	ΔV_{CROSS}	Single-ended Measurement	–	140	mV
Ring Back Voltage	V_{RB}	Single-ended Measurement	–	200	mV
Rise Time	T_R	V_L = 0.245V, V_H = 0.455V	175	700	ps
Fall Time	T_F	V_H = 0.455V, V_L = 0.245V	175	700	ps
Duty Cycle	D_{CYC}	Differential Measurement	45	55	%

Table 10. Electrical Characteristics – PCI Express (100MHz)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
PCIECLK Long Accuracy	ppm	See Tperiod min-max values	-300	300	ppm
PCIEX Frequency	F_{PCIE}	None SSC	–	100.03	MHz
Clock Period	T_{PERIOD}	None SSC	9.997	–	ns
Input Voltage	V_H	Statistical measurement on single ended signal	660	850	mV
Input Voltage	V_L	Statistical measurement on single ended signal	-150	–	mV
Maximum Input Voltage	V_{OVS}	Measurement on single ended signal using absolute	–	1150	mV
Minimum Input Voltage	V_{UDV}	Measurement on single ended signal using absolute	-300	–	mV
Crossing Point Voltage	V_{XABS}	Single-ended Measurement	250	550	mV
Crossing Point Variation	ΔV_{CROSS}	Single-ended Measurement	–	140	mV
Rise Time	T_R	V_L = 0.245V, V_H = 0.455V	175	700	ps
Fall Time	T_F	V_H = 0.455V V_L = 0.245V	175	700	ps
Duty Cycle	D_{CYC}	Differential Measurement	45	55	%
PCIEX Jitter – Cycle to Cycle	TJ_{C2C}	Differential Measurement	–	125	ps

Table 11. Electrical Characteristics – GCLK

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Long Accuracy	ppm	See Tperiod min-max values	-300	300	ppm
Frequency	F_{GCLK}		–	66.69	MHz
Clock Period	T_{PERIOD}		14.995	–	ns
Input High Voltage	V_{IH}		2	4	V
Input Low Voltage	V_{IL}		-0.65	0.8	V
High Time	V_{TH}		5	–	ns
Low Time	V_{TL}		5	–	ns
Edge Rate	T_{SR}	Rising/Falling edge rate	0.67	4	V/ns
Rise Time	T_R	V_L =0.4 V, V_H = 2.4 V	0.5	3	ns
Fall Time	T_F	V_H =2.4 V, V_L = 0.4 V	0.5	3	ns
Duty Cycle	D_{CYC}	V_T = 1.5 V	45	55	%
Jitter, Cycle to cycle	TJ_{C2C}	V_T = 1.5 V	–	500	ps

Table 12. Electrical Characteristics – USBCLK

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Long Accuracy	ppm	See Tperiod min-max values	-100	100	ppm
Frequency	F_{48MHZ}		–	48.0048	MHz
Clock Period	T_{PERIOD}	48.00MHz output nominal	20.8313	–	ns
Input High Voltage	V_{IH}		2	4	V
Input Low Voltage	V_{IL}		-0.65	0.8	V
High Time	V_{TH}		7	–	ns
Low Time	V_{TL}		7	–	ns
Edge Rate	T_{SR}	Rising/Falling edge rate	0.67	4	V/ns
Rise Time	T_R	V_L =0.4 V, V_H = 2.4 V	0.5	3	ns
Fall Time	T_F	V_H =2.4 V, V_L = 0.4 V	0.5	3	ns
Duty Cycle	D_{CYC}	V_T = 1.5 V	45	55	%
Jitter – Cycle to cycle	TJ_{C2C}	V_T = 1.5 V	–	250	ps

Table 13. Electrical Characteristics – PCICLK

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Frequency	F_{PCICLK}		30	35	MHz
Clock period	T_{PERIOD}		28.57	33.33	ns
Input High Voltage	V_{IH}		2	4	V
Input Low Voltage	V_{IL}		-0.65	0.8	V
High Time	V_{TH}		12	–	ns
Low Time	V_{TL}		12	–	ns
Edge Rate	T_{SR}	Rising/Falling edge rate	0.5	4	V/ns
Rise Time	T_R	V_L =0.4 V, V_H = 2.4 V	0.5	4	ns
Fall Time	T_F	V_H =2.4 V, V_L = 0.4 V	0.5	4	ns
Duty Cycle	D_{CYC}	V_T = 1.5 V	45	55	%
Jitter – Cycle to cycle	TJ_{C2C}	V_T = 1.5 V	–	500	ps

Table 14. Electrical Characteristics – XIN

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Long Accuracy	ppm	See Tperiod min-max values	-30	30	ppm
Frequency	F_{REF}		14.3175705	14.31842954	MHz
Clock period	T_{PERIOD}		69.84	69.8422	ns
Input High Voltage	V_{IH}		2	4	V
Input Low Voltage	V_{IL}		-0.55	0.8	V
High Time	V_{TH}		24	–	ns
Low Time	V_{TL}		24	–	ns
Edge Rate	T_{SR}	Rising/Falling edge rate	0.5	4	V/ns
Rise Time	T_R	V_L =0.4 V, V_H = 2.4 V	0.5	4	ns
Fall Time	T_F	V_H =2.4 V, V_L = 0.4 V	0.5	4	ns
Duty Cycle	D_{CYC}	V_T = 1.5 V	45	55	%
Jitter – Cycle to cycle	TJ_{C2C}	V_T = 1.5 V	–	500	ps

Table 15. Electrical Characteristics – CLKI25M

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Long Accuracy	ppm	See Tperiod min-max values	-30	30	ppm
Frequency	F_{SATA}		24.9992	25.0007	MHz
Clock Period	T_{PERIOD}		39.9988	40.0012	ns
Input High Voltage	V_{IH}		2	4	V
Input Low Voltage	V_{IL}		-0.55	0.8	V
High Time	V_{TH}		17	–	ns
Low Time	V_{TL}		17	–	ns
Rising Edge Slew Rate	T_{RSR}	Measurement from 0.8 to 2.0 V	1	4	V/ns
Falling Edge Slew Rate	T_{FSR}	Measurement from 2.0 to 0.8 V	1	4	V/ns
Duty Cycle	D_{CYC}	V_T = 1.5V	45	55	%
Jitter, Cycle to Cycle	TJ_{C2C}	V_T = 1.5V	–	150	ps

Table 16. Electrical Characteristics – MCLK Out

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Output Frequency Range	F_{MCLK}	667 Mhz D0F3 Rx[E6]=FF D0F3 Rx[EE]=00	400	667	MHz
Output pk-pk Voltage	$V_{OD(AC)}$	Single Ended Measurement	1	–	V
Output Cross-Point Voltage	$V_{OX(AC)}$	Single Ended Measurement	–	±100	mV
Output Ske MLKO+/MCLKO-	T_{SKEW}	Differential measurement	–	100	ps
Output Slew Rate	T_{SR}	Differential measurement - 20 % to 80%	–	400	ps
Output Duty Cycle	D_{CYC}	Differential measurement	48	52	%
Jitter – Accumulated	TJ_{ACC}	Differential measurement	–	200	ps

Electrical Characteristics - Host Interface

DC Specification

Table 17. Host Interface (1X / 4X)

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input High Voltage	V_{IH}	HGTLVREF +0.1	VTT +0.1	V
Input Low Voltage	V_{IL}	-0.1	HGTLVREF -0.1	V
Output High Voltage	V_{OH}	0.90*VTT	VTT	V
Output Low Voltage	V_{OL}	–	0.3*VTT+.1	V

AC Timing

Figure 5. Common Clock 1x Control Timings

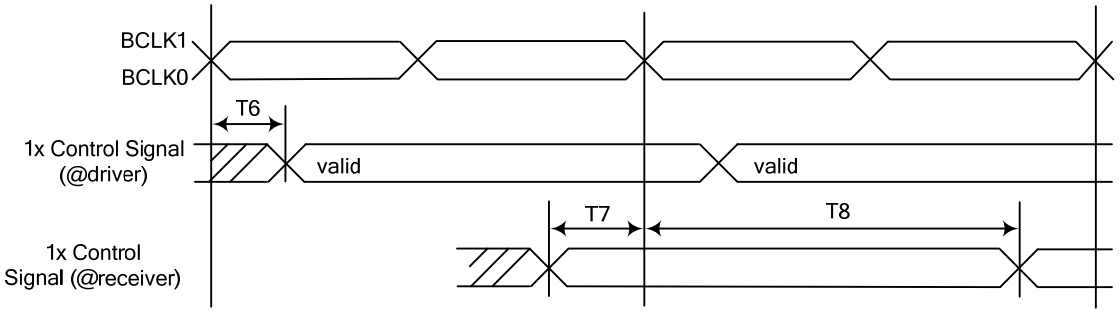


Table 18. Common Clock (1x) AC Specification

PARAMETER	SYMBOL	Product	MIN	MAX	UNITS	NOTES
Valid Output Delay	T6	800MHz – VX800	1.718	2.060	ns	–
		533MHz– VX800UT	1.840	2.450		2
Control Signal Setup Time	T7	800MHz – VX800	1.415	–	ns	–
		533MHz– VX800UT	1.795	–		2
Control Signal Hold Time	T8	800MHz – VX800	0.000	–	ns	–
		533MHz– VX800UT	0.000	–		2

Note:

1. Common Clock 1x control signals including HADS#, HBNR#, HBPRI#, HDBSY#, HDEFER#, HDRDY#, HHIT#, HHITM#, HLOCK#, HTRDY#, HRS[2:0]#, HDPWR#, HBREQ0# and CPURST#.
2. For VX800UT, VCC15 = 1.25V

Figure 6. Source Synchronous 4X Address Timings (System Processor Source)

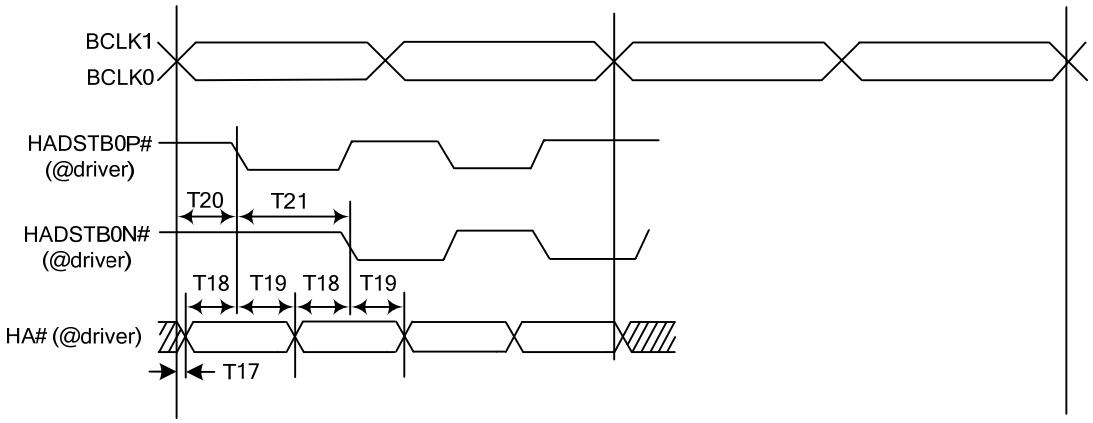


Table 19. Source Synchronous 4X AC Specification (System Processor Source)

PARAMETER	SYMBOL	Product	MIN	MAX	UNITS	NOTES
Address Output Valid Delay	T17	800MHz – VX800	–	2.013	ns	–
		533MHz– VX800UT	–	1.945		2
Address Output Valid Delay Before Address Strobe	T18	800MHz – VX800	0.558	–	ns	–
		533MHz– VX800UT	0.995	–		2
Address Output Valid Delay After Address Strobe	T19	800MHz – VX800	0.556	–	ns	–
		533MHz– VX800UT	0.550	–		2
Address Strobe Output Valid Delay	T20	800MHz – VX800	–	2.694	ns	–
		533MHz– VX800UT	–	3.140		2
First Address Strobe to Subsequent Strobe	T21	800MHz – VX800	–	1.250	ns	–
		533MHz– VX800UT	–	1.875		2

Note:

1. HA# signals including HA[30,16:3]# and HREQ[2:0]#.
2. For VX800UT, VCC15 = 1.25V

Figure 7. Source Synchronous 4X Address Timings (System Processor Target)

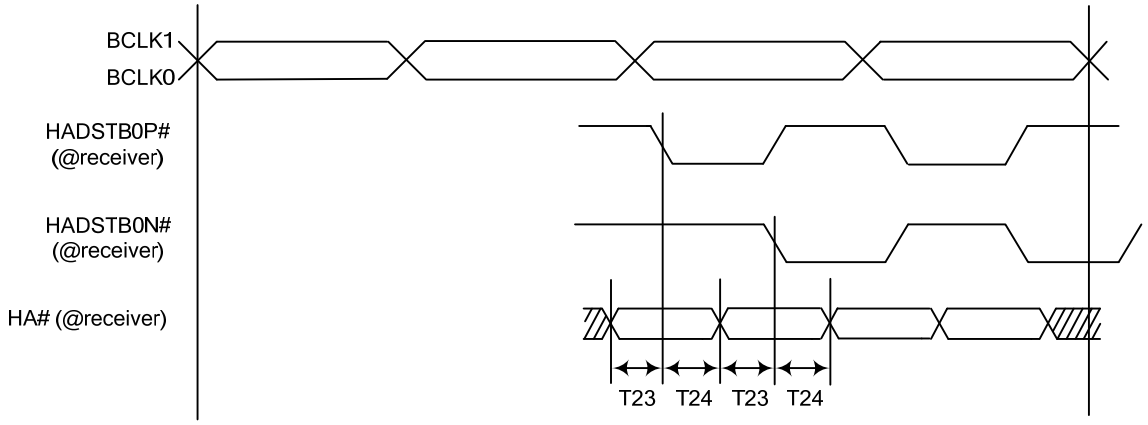


Table 20. Source Synchronous 4X AC Specification (System Processor Target)

PARAMETER	SYMBOL	Product	MIN	UNITS	NOTES
Address Input Setup Time	T23	800MHz – VX800	0.346	ns	–
		533MHz– VX800UT	0.351		2
Address Input Hold Time	T24	800MHz – VX800	0.486	ns	–
		533MHz– VX800UT	0.564		2

Note:

1. HA# signals including HA[30,16:3]# and HREQ[2:0]#.
2. For VX800UT, VCC15 = 1.25V

Figure 8. Source Synchronous 4X Data Timings (System Processor Source)

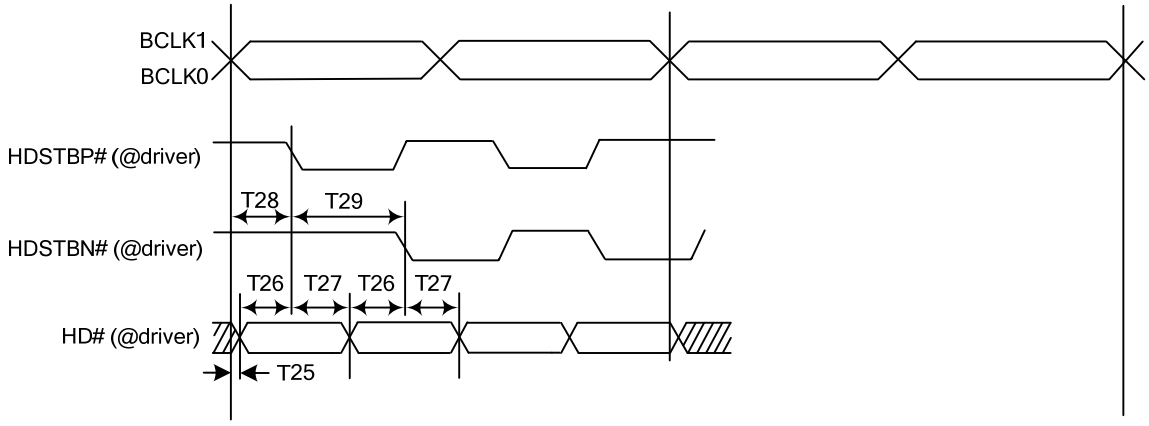


Table 21. Source Synchronous 4X AC Specification (System Processor Source)

PARAMETER	SYMBOL	Product	MIN	MAX	UNITS	NOTES
Data Output Valid Delay	T25	800MHz – VX800	–	2.864 2.210	ns	2
		533MHz– VX800UT	–	2.930 2.080		2, 3
Data Output Valid Delay Before Data Strobe	T26	800MHz – VX800	0.500	–	ns	–
		533MHz VX800UT	0.920	–		3
Data Output Valid Delay After Data Strobe	T27	800MHz – VX800	0.546	–	ns	–
		533MHz– VX800UT	0.680	–		3
Data Strobe Output Valid Delay	T28	800MHz – VX800	–	3.414 2.770	ns	2
		533MHz– VX800UT	–	3.940 3.315		2, 3
First Data Strobe to Subsequent Strobe	T29	800MHz – VX800	–	1.250	ns	–
		533MHz– VX800UT	–	1.875		3

Note:

1. HD# Signals including HD[63:0]# and HDBI[3:0]#.
2. Output Stagger Delay with longer max delay time on HD[63:48]#, HD[31:16]#, HDBI[3,1]#, HDSTB3P#, HDSTB3N#, HDSTB1P#, HDSTB1N# when the output stagger delay register is set .
3. For VX800UT, VCC15 = 1.25V

Figure 9. Source Synchronous 4X Data Timings (System Processor Target)

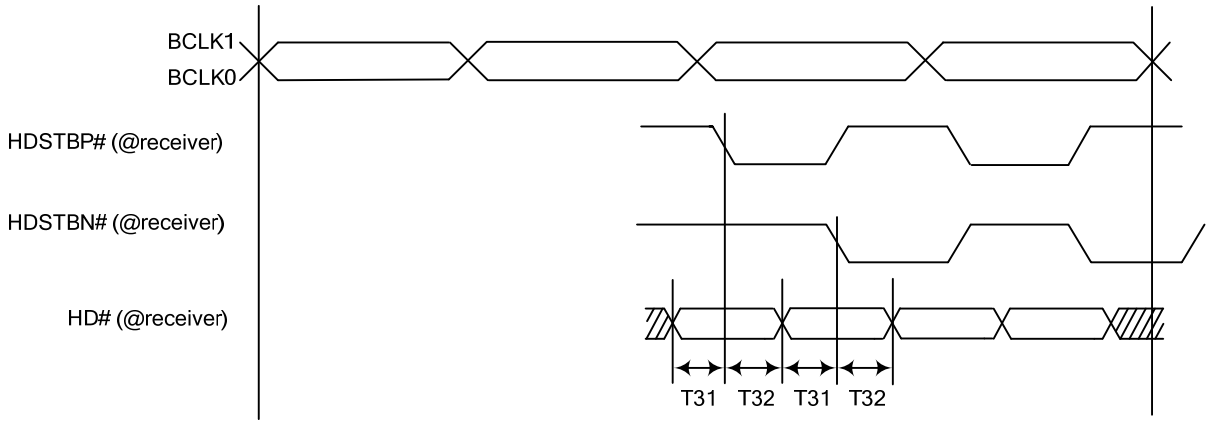


Table 22. Source Synchronous 4X AC Specification (System Processor Target)

PARAMETER	SYMBOL	Product	MIN	UNITS	NOTES
Data Input Setup Time	T31	800MHz – VX800	0.446	ns	–
		533MHz– VX800UT	0.475		2
Data Input Hold Time	T32	800MHz – VX800	0.460	ns	–
		533MHz– VX800UT	0.496		2

Note:

1. HD# Signals including HD[63:0]# and HDBI[3:0]#.
2. For VX800UT, VCC15 = 1.25V

Electrical Characteristics – System Memory

DC / AC Specification

Table 23. System Memory (Channel A) Interface - Input Logic Level

PARAMETER	SYMBOL	MIN	MAX	UNITS
DC Input Logic High	V_{IH}	VREF+0.125	VDDQ+0.3	V
DC Input Logic Low	V_{IL}	–0.3	VREF–0.125	V
DDR2 667				
AC Input Logic High	V_{IH}	VREF+0.20	–	V
AC Input Logic Low	V_{IL}	–	VREF–0.20	V
DDR2 533 / 400				
AC Input Logic High	V_{IH}	VREF+0.25	–	V
AC Input Logic Low	V_{IL}	–	VREF–0.25	V

Table 24. System Memory (Channel A) Interface – Differential Logic Level

PARAMETER	SYMBOL	MIN	MAX	UNITS
Differential Input				
AC Differential Input Voltage	V_{ID}	0.5	VDDQ+0.6	V
AC Differential Cross Point Voltage	V_{IX}	0.5 * VDDQ–0.175	0.5 * VDDQ+0.175	V
Differential Output				
AC Differential Cross Point Voltage	V_{OX}	0.5 * VDDQ–0.125	0.5 * VDDQ + 0.125	V

AC Timing

Figure 10. DDR2 Data and Strobe Timing (System Processor Target)

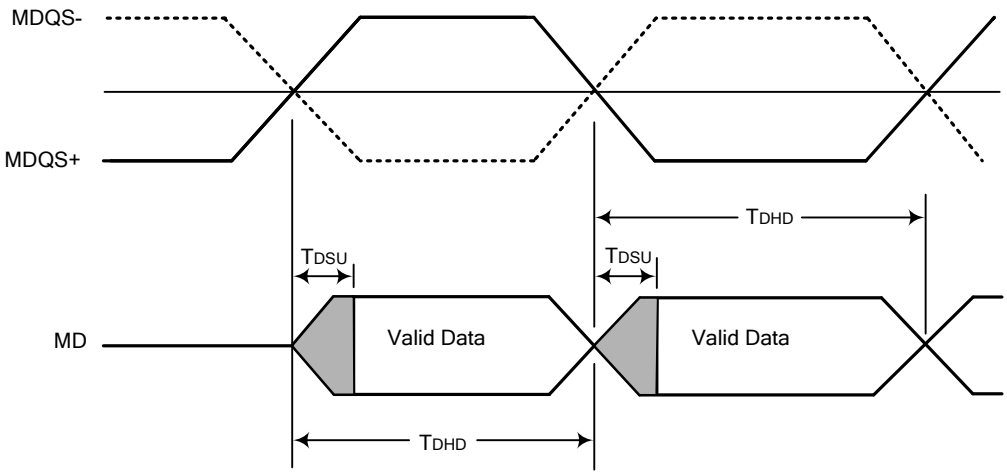


Table 25. DDR2 Data and Strobe AC Specification

PARAMETER	SYMBOL	Product	MIN	UNITS	NOTES
Input Setup Time	T_{DSU}	800MHz – VX800	0	ns	–
		533MHz – VX800UT	0		2
Input Hold Time	T_{DHD}	800MHz – VX800	1.084	ns	–
		533MHz – VX800UT	1.16		2

Note:

1. MD signals including MDA[63:0].
2. For VX800UT, VCC15 = 1.25V

Figure 11. DDR2 Data and Strobe Timing (System Processor Source)

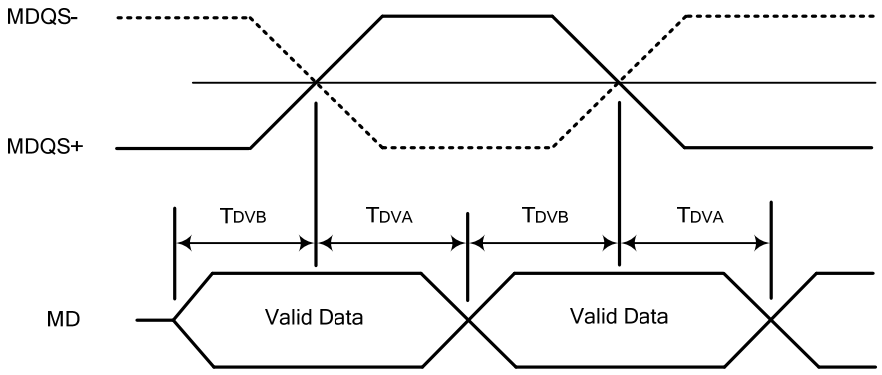


Table 26. DDR2 Data and Strobe AC Specification

PARAMETER	SYMBOL	Product	MIN	UNITS	NOTES
Data Output Valid Delay After Data Strobe	T_{DVA}	800MHz – VX800	0.671	ns	–
		533MHz – VX800UT	0.87		2
Data Output Valid Delay Before Data Strobe	T_{DVB}	800MHz – VX800	0.407	ns	–
		533MHz – VX800UT	0.51		2

Note:

1. MD signals including MDA[63:0], MDQMA[7:0]
2. For VX800UT, VCC15 = 1.25

Figure 12. DDR2 Command Signals Timing

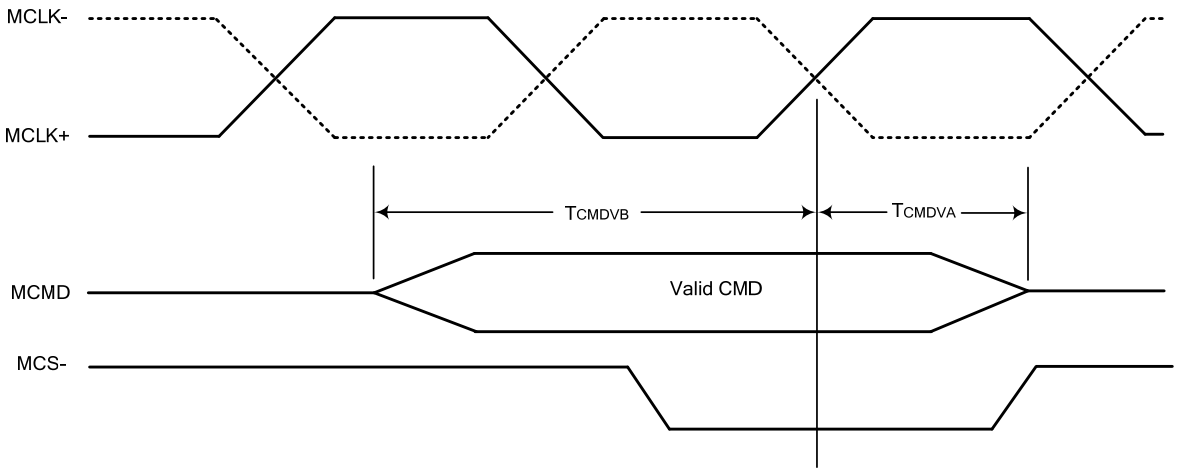


Table 27. DDR2 Command AC Specification

PARAMETER	SYMBOL	Product	MIN	UNITS	NOTES
Command Signals Output Valid Delay After MCLKO	T_{CMDVA}	800MHz – VX800	1.152	ns	–
		533MHz – VX800UT	1.675		2
Command Signals Output Valid Delay Before MCLKO	T_{CMDVB}	800MHz – VX800	1.131	ns	–
		533MHz – VX800UT	1.335		2

Note:

1. MCMD signals including MAA[13:0], MBAA[2:0], MSRASA#, MSCASA# and MSWEA#.
2. For VX800UT, VCC15 = 1.25V

Figure 13. DDR2 Control Signals Timing

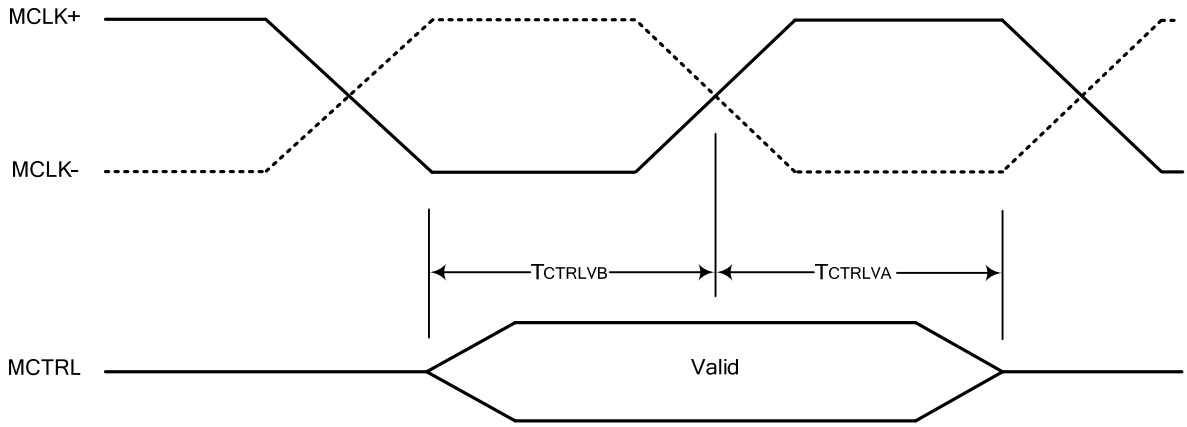


Table 28. DDR2 Control Signal AC Specification

PARAMETER	SYMBOL	Product	MIN	UNITS	NOTES
Control Signals Output Valid Delay After MCLKO	T_{CTRLVA}	800MHz – VX800	1.428	ns	–
		533MHz – VX800UT	1.525		2
Control Signals Output Valid Delay Before MCLKO	T_{CTRLVB}	800MHz – VX800	1.032	ns	–
		533MHz – VX800UT	1.71		2

Note:

1. MCTRL signals including MODTA[3:0], MCSA[3:0]# and MCKEA[3:0].
2. For VX800UT, VCC15 = 1.25V

Electrical Characteristics – PCI Express Interface

Table 29. PCI Express Interface - Differential Transmitter Specifications (TX)

PARAMETER	SYMBOL	MIN	NOM	MAX	UNITS
Unit Interval	UI	399.88	400	400.12	ps
Differential Peak-to-Peak Output Voltage	VTX-DIFFp-p	0.8	–	1.2	V
De-emphasized Differential Output Voltage (ratio)	VTX-DE-RATIO	-3	-3.5	-4	dB
Minimum TX Eye Width	VTX-EYE	0.7	–	–	UI
Maximum Time Between Jitter Median and Maximum Deviation From the Median	VTX-EYEMEDIANTO-MAX-JITTER	–	–	0.15	UI
D+/D- TX Output Rise/Fall Time	VTX-RISE, VTXFALL	0.125	–	–	UI
AC Peak Common Mode Output Voltage	VTX-CM-ACp	–	–	20	mV
Absolute Delta of DC Common Mode Voltage during L0 and Electrical Idle	VTX-CM-DCACIVE-IDLEDELTA	0	–	100	mV
Absolute Delta of DC Common Mode Voltage Between D+ and D-	VTX-CM-DC-LINEDELTA	0	–	25	mV
Electrical Idle Differential Peak Output Voltage	VTX-IDLE-DIFFp	0	–	20	mV
The amount of voltage allowed during Receiver detection	VTX-RCV-DETECT	–	–	600	mV
Minimum Time Specification in Electrical Idle	VTX-IDLE-MIN	50	–	–	UI
Maximum Time Totransition to a Valid Electrical Idle after Sending an Electrical Idle Odered Set	VTX-IDLE-SET-TOIDLE	–	–	20	UI
Maximum Time Spent in Electrical Idle Before Initiating a Rceiver Detect Sequence	VTX-IDLERCVDETECT-MAX	–	–	100	ms
Differential Return Loss	RLTX-DIFF	12	–	–	dB
Common Mode Return Loss	RLTX-CM	6	–	–	dB
DC Differential TX Impedance	ZTX-DIFF-DC	80	100	120	Ohm
Transmitter Common Mode High Impedance State (DC)	ZTX-COM-High-IMP-DC	5	–	20	K
Lane-to-lane Skew	LTX-SKEW	–	–	500	ps
AC Coupling Capacitor	CTX	75	–	200	pF

Table 30. PCI Express Interface - Differential Receiver Specifications

PARAMETER	SYMBOL	MIN	NOM	MAX	UNITS
Unit Interval	UI	399.88	400	400.12	ps
Differential Peak-topeak Input Voltage	VRX-DIFFp-p	0.175	–	1.2	V
Minimum RX Eye Width	VRX-EYE	0.4	–	–	UI
Maximum Time Between Jitter Median and Maximum Deviation From the Median	VRX-EYEMEDIANTO-MAX-JITTER	–	–	0.3	UI
AC Peak Common Mode Input Voltage	VRX-CM-A_{Cp}	–	–	150	mV
Differential Return Loss	RLRX-DIFF	15	–	–	dB
Common Mode Return Loss	RLRX-CM	6	–	–	dB
DC Differential RX Impedance	ZRX-DIFF-DC	80	100	120	Ohm
DC Input Common Mode Input Impedance	ZRX-COM-DC	40	50	60	Ohm
Initial DC Input Common Mode Input Impedance	ZRX-COMINITIAL-DC	5	50	60	Ohm
Powered Down DC Input Common Mode Input Impedance	ZRX-COMHIGH-IMP-DC	200	–	–	K
Electrical Idle Threshold	VRX-IDLEDET-DIFFp-p	65	–	175	mV
Unexpected Electrical Idle Enter Detect Threshold Integration Time	TRX-IDLEDETOFFENTERTIME	–	–	10	ms
Lane-to-lane Skew	LTX-SKEW	–	–	20	ns

Electrical Characteristics – LVDS Interface

Table 31. LVDS Interface – Differential Singal AC Specifications

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Differential output voltage	V_{OD}	247	–	454	mV
Change in VOD magnitude	ΔV_{OD}	–	–	50	mV
Output common-mode voltage	V_{OS}	1.125	–	1.375	mV
Change in VOCM magnitude	ΔV_{OCM}	–	–	50	mV
Short Circuit Output Current	$\|I_{OS}\|$	–	3.5	5	mA
LVDS low to high transition time	L_{LHT}	–	0.75	1.5	ns
LVDS high to low transition time	L_{HLT}	–	0.75	1.5	ns
Output pulse position for bit 0	T_{PPOS0}	-0.2	0	0.2	ns
Output pulse position for bit 1	T_{PPOS1}	1.48	1.68	1.88	ns
Output pulse position for bit 2	T_{PPOS2}	3.16	3.36	3.56	ns
Output pulse position for bit 3	T_{PPOS3}	4.88	5.08	5.28	ns
Output pulse position for bit 4	T_{PPOS4}	6.52	6.72	6.92	ns
Output pulse position for bit 5	T_{PPOS5}	8.2	8.4	8.6	ns
Output pulse position for bit 6	T_{PPOS6}	9.88	10.08	10.28	ns

Electrical Characteristics – CRT Interface

Table 32. CRT Interface – RGB

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS
High-level output voltage	V_{OH}	Max. luminance, white video level voltage	665	–	770	mV
DAC noise at white level	V_{ON}	Max. luminance	–	37.15	–	mV
Low-level output voltage	V_{OL}	Min. luminance white video level voltage	–	0	–	V
Output rising time	T_{OR}	–	–	–	3.08	ns
Output falling time	T_{OF}	–	–	–	3.08	ns
Overshoot	V_{ov}	–	–	–	12	%
Undershoot	V_{us}	–	–	–	12	%
RBG Output skew	T_{SKEW}	–	–	–	1.54	ns

Table 33. CRT Interface – HSYNC and VSYNC

PARAMETER	SYMBOL	MIN	MAX	UNITS
High-level output voltage	V_{OH}	2.4	3.6	V
Low-level output voltage	V_{OL}	-0.3	0.4	V
Output rising time	T_{OR}	–	4.93	ns
Output falling time	T_{OF}	–	4.93	ns
Overshoot	V_{ov}	–	30	%
Undershoot	V_{us}	–	30	%
H-Sync Output jitter	T_{jitter}	–	15	% of Pixel Clock

Electrical Characteristics – USB Interface

Table 34. USB Interface - Signal DC Characteristics

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Impedance	–	80	90	100	Ohm
USB Signals: Input Level for Low-speed and Full-speed Mode					
Input Low Voltage	V_{IL}	–	–	0.8	V
Input High Voltage	V_{IH}	2	–	3.6	V
Differential Input Sensitivity	V_{DI}	0.2	–	–	V
Differential Common Mode Range	V_{CM}	0.8	–	2.5	V
Single-Ended Receiver Threshold	V_{SE1}	0.8	–	–	V
USB Signals: Input Level for High-speed Mode					
HS Squelch Detection Threshold	V_{HSSQ}	100	–	150	mV
HS Disconnect DetectionThreshold	V_{HSDSC}	525	–	625	mV
HS Data Signaling Common Mode Voltage Range	V_{HSCM}	-50	–	500	mV
USB Signals: Output Level for Low-speed and Full-speed Modes					
Output High Voltage	V_{OH}	2.8	–	3.6	V
Output Low Voltage	V_{OL}	0	–	0.3	V
Single-Ended Threshold	V_{OSE1}	0.8	–	–	V
Output Signal Crossover Voltage	V_{CRS}	1.3	–	2	V
USB Signals: Output Level for High-speed Modes					
HS Idle Level	V_{HSOI}	-10	–	10	mV
HS Data Signaling High	V_{HSOH}	360	–	440	mV
HS Data Signaling Low	V_{HSOL}	-10	–	10	mV
Chirp J Level	V_{CHIRPJ}	700	–	1100	mV
Chirp K Level	V_{CHIRPK}	-900	–	-500	mV

Table 35. USB Interface - Signal Electrical Characteristics (Full-speed Source)

PARAMETER	SYMBOL	MIN	MAX	UNITS
Rise Time	T_{FR}	4	20	ns
Fall Time	T_{FF}	4	20	ns
Differential Rise and Fall Time Matching	T_{FRFM}	90	111.1	%
Driver Output Resistance for driver which is not high-speed capable	Z_{DRV}	28	44	Ohm
Full-speed Data Rate for hubs and devices which are high-speed capable	$T_{FDRATHS}$	11.994	12.006	Mbps
Full-speed Data Rate for devices which are not high-speed capable	T_{FDRATE}	11.97	12.03	Mbps
Frame Interval	T_{FRAME}	0.9995	1.0005	ms
Consecutive Frame Interval Jitter	T_{RFI}	–	42	ns
Source Jitter Total (including frequency tolerance)				
To Next Transition	T_{DJ1}	-3.5	3.5	ns
For Paired Transitions	T_{DJ2}	-4	4	ns
Source SE0 Interval of EOP	T_{FEOPT}	160	175	ns
Source Jitter for Differential Transition to SE0 Transition	T_{FDEOP}	-2	5	ns
Receiver Data Jitter Tolerance				
To Next Transition	T_{JR1}	-18.5	18.5	ns
For Paired Transitions	T_{JR2}	-9	9	ns
Receiver SE0 Interval of EOP	T_{FEOPR}	82	–	ns
Width of SE0 Interval during Differential Transition	T_{FST}	–	14	ns

Table 36. USB Interface - Signal Electrical Characteristics (Low-speed Source)

PARAMETER	SYMBOL	MIN	MAX	UNITS
Rise Time	T_{LR}	75	300	ns
Fall Time	T_{LF}	75	300	ns
Differential Rise and Fall Time Matching	T_{LFRFM}	80	125	%
Low-speed Data Rate for hubs and devices which are highspeed capable	$T_{LDRATHS}$	1.49925	1.50075	Mbps
Low-speed Data Rate for devices which are not highspeed capable	T_{LDRATE}	1.4775	1.5225	Mbps
Upstream Facing Port Source Jitter Total (including frequency tolerance)				
To Next Transition	T_{UDJ1}	-95	95	ns
For Paired Transitions	T_{UDJ2}	-150	150	ns
Upstream facing port source Jitter for Differential Transition to SE0 Transition	T_{LDEOP}	-40	100	ns
Upstream Facing Port Differential Receiver Jitter				
To Next Transition	T_{DJR1}	-75	75	ns
For Paired Transitions	T_{DJR2}	-45	45	ns
Downstream Facing Port Source Jitter Total (including frequency tolerance):				
To Next Transition	T_{DDJ1}	-25	25	ns
For Paired Transitions	T_{DDJ2}	-14	14	ns
Downstream Facing Port Differential Receiver Jitter				
To Next Transition	T_{UJR1}	-152	152	ns
For Paired Transitions	T_{UJR2}	-200	200	ns
Source SE0 Interval of EOP	T_{LEOPT}	1.25	1.5	us
Receiver SE0 Interval of EOP	T_{FEOPR}	670	–	ns
Width of SE0 Interval during Differential Transition	T_{LST}	–	210	ns

Table 37. USB Interface - Signal Electrical Characteristics (High-speed Source)

PARAMETER	SYMBOL	MIN	MAX	UNITS
High speed Signal Rate	T_{HSDRAT}	479.76	480.24	Mbps
High speed EOP Width	–	15.625	17.7083	ns
High speed EOP Width (Bits)	–	7.5	8.5	–
Microframe Interval	T_{HSFRAM}	124.9375	125.0625	us
High speed Output Rise Time (10% - 90%)	T_{HSR}	500	–	ps
High speed Output Fall Time (10% - 90%)	T_{HSF}	500	–	ps

Electrical Characteristics – SATA Interface

Table 38. SATA Interface – Differential Signal AC Specifications

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Gen I Operating Data Period	UI	666.43	–	670.23	ps
Gen II Operating Data Period	UI	333.21	–	335.11	ps
Minimum Input Voltage - 1.5 Gb/s, GenI	V_{IMIN}	325.00	–	–	mVdiffp-p
Minimum Input Voltage - 3.0 Gb/s, GenII	V_{IMIN}	275.00	–	–	mVdiffp-p
Maximum Input Voltage - 1.5 Gb/s, GenI	V_{IMAX}	–	–	600.00	mVdiffp-p
Maximum Input Voltage - 3.0 Gb/s, GenII	V_{IMAX}	–	–	750.00	mVdiffp-p
Minimum Output Voltage, GenI	V_{OMIN}	400.00	–	–	mVdiffp-p
Minimum Output Voltage, GenII	V_{OMIN}	400.00	–	–	mVdiffp-p
Maximum Output Voltage, GenI	V_{OMAX}	–	–	600.00	mVdiffp-p
Maximum Output Voltage, GenII	V_{OMAX}	–	–	700.00	mVdiffp-p
Rise Time (20% – 80% at transmitter), GenI	T_R	0.15	–	0.41	UI
Fall Time (80% – 20% at transmitter), Gen I	T_F	0.15	–	0.41	UI
Rise Time (20% – 80% at transmitter), GenII	T_R	0.20	–	0.41	UI
Fall Time (80% – 20% at transmitter), Gen II	T_F	0.20	–	0.41	UI
TX Differential Skew	Tskew-tx	–	–	20.00	ps

Table 39. SATA Interface – OOB Specifications

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
UI During OOB Signaling	U_{IOOB}	646.67	–	686.67	ps
COMINIT/COMRESET/COMWAKE Transmit Burst Length	T_1	101.30	106.70	112.00	ns
COMWAKE Transmit Gap Length	T_1	101.30	106.70	112.00	ns
COMINIT/COMRESET Transmit Gap Length	T_2	304.00	320.00	336.00	ns
OOB Signal Detection Threshold,GenI	Vthresh	50.00	–	200.00	mVppd
OOB Signal Detection Threshold,GenII	Vthresh	75.00	–	200.00	mVppd

Table 40. SATA Interface – Receiver Specification

PARAMETER	SYMBOL	MIN	MAX	UNITS
RX Pair Differential Impedance	Zdiff-rx	85.00	115.00	Ohm
RX Single-Ended Impedance	Zse-rx	40.00	–	Ohm

Table 41. SATA Interface – Receiver Specification (RLDD11-rx)

PARAMETER	MIN	UNITS
Gen II (3Gb/s) Differential Mode Return Loss		
Freq: 150MHz-300MHz	-18.00	dB
Freq: 300MHz-600MHz	-14.00	dB
Freq: 600MHz-1.2GHz	-10.00	dB
Freq: 1.2GHz-2.4GHz	-8.00	dB
Freq: 2.4GHz-3.0GHz	-3.00	dB
Freq: 3.0GHz-5.0GHz	-1.00	dB
Gen II (3Gb/s) Common Mode Return Loss		
Freq: 150MHz-300MHz	-5.00	dB
Freq: 300MHz-600MHz	-5.00	dB
Freq: 600MHz-1.2GHz	-2.00	dB
Freq: 1.2GHz-2.4GHz	-1.00	dB
Freq: 2.4GHz-3.0GHz	-1.00	dB
Freq: 3.0GHz-5.0GHz	-1.00	dB
Gen I (1.5Gb/s) Differential Mode Return Loss		
Freq: 75MHz-150MHz	-18.00	dB
Freq: 150MHz-300MHz	-14.00	dB
Freq: 300MHz-600MHz	-10.00	dB
Freq: 600MHz-1.2GHz	-8.00	dB
Freq: 1.2GHz-2.4GHz	-3.00	dB
Freq: 2.4GHz-3.0GHz	-1.00	dB

Table 42. SATA Interface – Transmitter Specification

PARAMETER	SYMBOL	MIN	MAX	UNITS
TX Pair Differential Impedance	Zdiff-tx	85.00	115.00	Ohm
TX Single-Ended Impedance	Zse-tx	40.00	–	Ohm

Table 43. SATA Interface – Transmitter Specification (RLDD11-TX)

PARAMETER	MIN	UNITS
Gen II (3Gb/s) Differential Mode Return Loss		
Freq: 150MHz-300MHz	-14.00	dB
Freq: 300MHz-600MHz	-8.00	dB
Freq: 600MHz-1.2GHz	-6.00	dB
Freq: 1.2GHz-2.4GHz	-6.00	dB
Freq: 2.4GHz-3.0GHz	-3.00	dB
Freq: 3.0GHz-5.0GHz	-1.00	dB
Gen II (3Gb/s) Common Mode Return Loss		
Freq: 150MHz-300MHz	-8.00	dB
Freq: 300MHz-600MHz	-5.00	dB
Freq: 600MHz-1.2GHz	-2.00	dB
Freq: 1.2GHz-2.4GHz	-1.00	dB
Freq: 2.4GHz-3.0GHz	-1.00	dB
Freq: 3.0GHz-5.0GHz	-1.00	dB
Gen I (1.5Gb/s) Differential Mode Return Loss		
Freq: 75MHz-150MHz	-14.00	dB
Freq: 150MHz-300MHz	-8.00	dB
Freq: 300MHz-600MHz	-6.00	dB
Freq: 600MHz-1.2GHz	-6.00	dB
Freq: 1.2GHz-2.4GHz	-3.00	dB
Freq: 2.4GHz-3.0GHz	-1.00	dB

Electrical Characteristics – Miscellaneous Interfaces

Table 44. Miscellaneous Interfaces

Signal Group	Signals	Reference
1	**SDIO Ports:** SDIO0D[3:0], SDIO0CLK, SDIO0CMD#, SDIO0WPD#, SDIO1D[3:0], SDIO1CLK, SDIO1CMD#, SDIO1WPD# **Card Reader Interface:** CR_D[7:0], CR_CLK, CRSD_CD#, CRSD_WPD#	Refer to Table 46
2	**CPU Control Interface:** A20M#, FERR#, IGNNE#, INIT#, INTR, NMI, SLP#, SMI#, STPCLK#, NAP#, THRMTRIP#, DPSLP# **Test and Miscellaneous Signals:** TESTIN, DFTIN, BISTIN, TP[3:1]	Refer to Table 47
3	**RTC Crystal Interface:** RTCXO, RTCXI **Power State and System Reset:** RSMRST#, PWRGD **Power Management Control and Event Signal:** INTRUDER# **Test and Miscellaneous Signals:** TP8	Refer to Table 48
4	**Clock Signals of Graphics & Video Processors:** DISPCLKI0, DISPCLKO0, DISPCLKI1, DISPCLKO1 **Video Capture Port Interface:** VCPD[15:0], VCPHS, VCPVS, VCPCLK **Digital Video Port 1 (DVP1) Interface:** DVP1D[15:0], DVP1HS, DVP1VS, DVP1DE, DVP1TVCLKR, DVP1CLK, DVP1TVFLD **LCD Panel Power and Brightness Control:** LVDSENVDD[A:B], LVDSENBLD[A:B] **IR Interface:** IRSCLK	Refer to Table 49
5	**Enhanced IDE Interface:** PDD[15:0], PDDACK#, PDIORDY, PDIOR#, PDIOW#	Refer to Table 50
6	**CRT Interface:** CRTSPD, CRTSPCLK, CRTHSYNC, CRTVSYNC **LCD Panel Power and Brightness Control:** BLTCK **Digital Video Port 1 (DVP1) Interface:** DVP1SPD, DVP1SPCLK **Test and Miscellaneous Signals:** TP6	Refer to Table 51
7	**Enhanced IDE Interface:** IRQ15 **SMBus Interface:** SMBDT1, SMBCK1, SMBDT2, SMBCK2 **Internal Mouse / Keyboard Controller Interface:** KBDT, KBCK, MSCK, MSDT **Test and Miscellaneous Signals:** TP7	Refer to Table 52

Table 45. Miscellaneous Interfaces (cont.)

Signal Group	Signals	Reference
8	**Enhanced IDE Interface:** PDCS3#, PDDREQ, PDA[2:0], IDERST# **SATA Interface:** SATALED0# **SDIO Ports:** SDIO0CD#, SDIO0PSEL, SDIO0POFF, SDIO1CD#, SDIO1PSEL, SDIO1POFF **PCI Bus Interface:** PCIRST[1:0]# **High Definition Audio Interface:** AZRST#, AZSDIN[2:0] **Speaker Interface:** SPKR **General Purpose Input/Output Interface:** GPIO[13:10] **Power Management Control and Event Signal:** RING#, SUSA#, SUSB#, SUSC#, C4PSTOP#, VRDSLP, CPUSTP#, CSTATE1, PCISTP#, SYSIDLE **PC / PCI DMA Interface:** PCIDREQ#, PCIDGNT# **Test and Miscellaneous Signals:** TP[5:4]	Refer to Table 53
9	**High Definition Audio Interface:** AZBITCLK, AZSDOUT, AZSYNC **SPI Controller Interface:** SPIDI, SPIDO, SPICLK, SPISS[1:0]#	Refer to Table 54
10	**Enhanced IDE Interface:** PDCS1# **LPC Bus Interface:** LPCFRAME#, LPCAD[3:0] **Serial IRQ Interface:** SERIRQ **Power Management Control and Event Signal:** CLKRUN# **PCI Bus Interface:** DEVSEL#, FRAME#, IRDY#, STOP#, TRDY#, SERR#, PAR, AD[31:00], CBE[3:0]#, GNT[3:0]#, PERR#, CBE[3:0]#	Refer to Table 55
11	**LPC Bus Interface:** LPCDRQ[1:0]# **Power Management Control and Event Signal:** THRM#, WAKE#, BATLOW#, EXTSMI#, LID#, PWRBTN#, PME# **SMBus Interface:** SMBALRT# **PCI Bus Interface:** INTA#, INTB#, INTC#, INTD#, REQ[3:0]# **General Purpose Input Interface:** GPI1 **Trusted Platform Module Interface:** TCSEN# **USB 2.0 Interface:** USBOC[5:0]#	Refer to Table 56

Table 46. Electrical Characteristics of Group 1

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS
DC Supply Voltage	V_{CC}	–	3.135	3.3	3.465	V
Input Low Voltage	V_{IL}	–	-0.3	–	0.25*VCC	V
Input High Voltage	V_{IH}	–	0.625*VCC	–	VCC + 0.5	V
Low-level Output Voltage	V_{OL}	IOL = 0.1 mA	–	–	0.125*VCC	V
High-level Output Voltage	V_{OH}	IOH = -0.1 mA	0.75*VCC	–	–	V
Input Leakage Current	I_{IL}	$0<V_{IN}<V_{CC}$	–	–	±10	uA
Tristate Leakage Current	I_{OZ}	$0<V_{OUT}<V_{CC}$	–	–	±20	uA

Table 47. Electrical Characteristics of Group 2

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS
DC Supply Voltage	V_{TT}	–	0.9975	1.05	1.1025	V
Input Low Voltage	V_{IL}	–	-0.1	–	0.3*VTT	V
Input High Voltage	V_{IH}	–	0.7*VTT	–	VTT+0.1	V
Output Low Voltage	V_{OL}	IOL = 2 mA	-0.1	0	0.15*VTT	V
Output High Voltage	V_{OH}	IOH = - 0.5 mA	0.9*VTT	VTT	VTT+0.1	V

Table 48. Electrical Characteristics of Group 3

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS
DC Supply Voltage	V_{BAT}	–	2.4	3	3.45	V
Input Low Voltage	V_{IL}	–	-0.3	–	0.3*VBAT	V
Input High Voltage	V_{IH}	–	0.7*VBAT	–	VBAT + 0.5	V
Power Supply Current – RTC Battery	I_{BAT}	Battery Mode	–	–	10	uA

Table 49. Electrical Characteristics of Group 4

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS
DC Supply Voltage	V_{CC}	–	3.135	3.3	3.465	V
Input Low Voltage	V_{IL}	–	-0.5	–	0.8	V
Input High Voltage	V_{IH}	–	2	–	VCC + 0.5	V
Low-level Output Voltage	V_{OL}	IOL = 4 mA	–	–	0.55	V
High-level Output Voltage	V_{OH}	IOH = -1 mA	2.4	–	–	V

Table 50. Electrical Characteristics of Group 5

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS
DC Supply Voltage	V_{CC}	–	3.135	3.3	3.465	V
Input Low Voltage	V_{IL}	–	-0.5	–	0.3*VCC	V
Input High Voltage	V_{IH}	–	0.55*VCC	–	VCC5 + 0.5	V
Low-level Output Voltage	V_{OL}	IOL = 6 mA	–	–	0.55	V
High-level Output Voltage	V_{OH}	IOH = - 6 mA	0.85*VCC	–	–	V

Table 51. Electrical Characteristics of Group 6

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS
DC Supply Voltage	V_{CC}	–	3.135	3.3	3.465	V
Input Low Voltage	V_{IL}	–	-0.5	–	0.8	V
Input High Voltage	V_{IH}	–	2	–	VCC + 0.5	V
Low-level Output Voltage	V_{OL}	IOL = 4 mA	–	–	0.55	V
High-level Output Voltage	V_{OH}	IOH = - 1 mA	2.4	–	–	V

Table 52. Electrical Characteristics of Group 7

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS
DC Supply Voltage	V_{CC}	–	3.135	3.3	3.465	V
Input Low Voltage	V_{IL}	–	-0.5	–	0.8	V
Input High Voltage	V_{IH}	–	2.1	–	VCC5 + 0.5	V
Low-level Output Voltage	V_{OL}	IOL = 6 mA	–	–	0.4	V
High-level Output Voltage	V_{OH}	IOH = -1 mA	0.9*VCC	–	–	V
Input Leakage Current	I_{IL}	$0<V_{IN}<V_{CC}$	–	–	±10	uA
Tristate Leakage Current	I_{OZ}	$0<V_{OUT}<V_{CC}$	–	–	±20	uA

Table 53. Electrical Characteristics of Group 8

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS
DC Supply Voltage	V_{CC}	–	3.135	3.3	3.465	V
Input Low Voltage	V_{IL}	–	-0.5	–	0.8	V
Input High Voltage	V_{IH}	–	2	–	VCC + 0.5	V
Low-level Output Voltage	V_{OL}	IOL = 4 mA	–	–	0.55	V
High-level Output Voltage	V_{OH}	IOH = -1 mA	2.4	–	–	V
Input Leakage Current	I_{IL}	$0<V_{IN}<V_{CC}$	–	–	±10	uA
Tristate Leakage Current	I_{OZ}	$0<V_{OUT}<V_{CC}$	–	–	±20	uA

Table 54. Electrical Characteristics of Group 9

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS
DC Supply Voltage	V_{CC}	–	3.135	3.3	3.465	V
Input Low Voltage	V_{IL}	–	-0.3	–	0.35*VCC	V
Input High Voltage	V_{IH}	–	0.65*VCC	–	VCC + 0.5	V
Low-level Output Voltage	V_{OL}	IOL = 1.5 mA	–	–	0.1*VCC	V
High-level Output Voltage	V_{OH}	IOH = - 0.5 mA	0.9*VCC	–	–	V

Table 55. Electrical Characteristics of Group 10

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS
DC Supply Voltage	V_{CC}	–	3.135	3.3	3.465	V
Input Low Voltage	V_{IL}	–	-0.5	–	0.3*VCC	V
Input High Voltage	V_{IH}	–	0.5*VCC	–	VCC + 0.5	V
Low-level Output Voltage	V_{OL}	IOL = 1.5 mA	–	–	0.1*VCC	V
High-level Output Voltage	V_{OH}	IOH = - 0.5 mA	0.9*VCC	–	–	V

Table 56. Electrical Characteristics of Group 11

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS
DC Supply Voltage	V_{CC}	–	3.135	3.3	3.465	V
Input Low Voltage	V_{IL}	–	-0.5	–	0.8	V
Input High Voltage	V_{IH}	–	2	–	VCC + 0.5	V
Input Leakage Current	I_{IL}	$0<V_{IN}<V_{CC}$	–	–	±10	uA
Tristate Leakage Current	I_{OZ}	$0<V_{OUT}<V_{CC}$	–	–	±20	uA

Strapping Timing Requirement

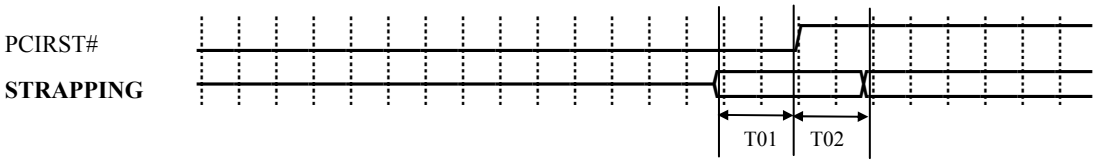


Figure 14. Strapping Timing

Symbol	Parameter	Min	Max	Unit	Note
T01	STRAPPING signals setup time	1	–	us	1
T02	STRAPPING signals hold time	1	–	us	1

Note:

1. VIL (max)=0.8V , VIH (min) = 2.0V.

Power Sequence

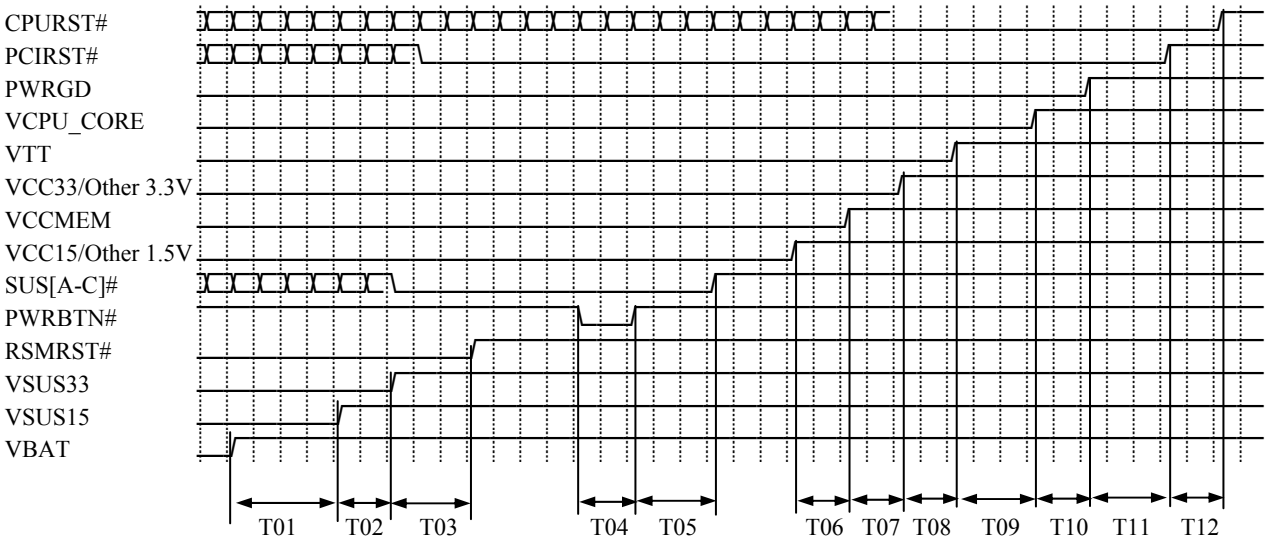


Figure 15. Power On Sequence and Reset Signal Timing

Symbol	Parameter	Min	Max	Unit	Note
T01	VBAT supply active to VSUS15 supply active	0	–	ms	–
T02	VSUS15 supply active to VSUS33 supply active	0	–	ms	1
T03	VSUS33 supply active to RSMRST# inactive	5	–	ms	–
T04	PWRBTN# active width	1	–	RTCCLK	–
T05	PWRBTN# rising to SUS[A-C]# inactive	–	5	RTCCLK	–
T06	VCC15 supply active to VCCMEM supply active	0	–	ms	2
T07	VCCMEM supply active to VCC33 supply active	–	–	ms	3
T08	VCC33 supply active to VTT supply active	0	–	ms	4
T09	VTT supply active to VCPU_CORE supply active	0	–	ms	–
T10	VCPU_CORE supply active to PWRGD active	10	–	ms	–
T11	PWRGD active to PCIRST# inactive	7	–	ms	–
T12	PCIRST# inactive to CPURST# inactive	15	–	us	5

Note:

2. VSUS15 must be powered up before VSUS33 is powered up.
3. VCC15 must be powered up before VCCMEM and VCC33 are powered up.
4. No timing interdependencies between VCCMEM and VCC33.
5. VCC33 and VTT assume to be powered up “together”.
6. CPURST# is de-asserted after the completion of ROMSIP cycles.

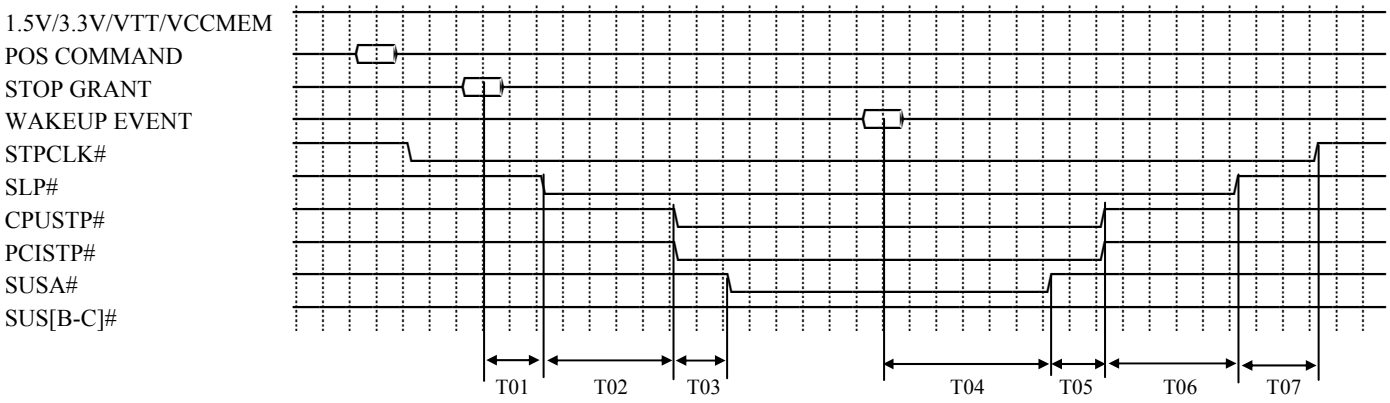


Figure 16. Power On Suspend (S1) and Resume Sequence

Symbol	Parameter	Min	Max	Unit	Note
T01	STOP GRANT to SLP# active	—	1	RTCCLK	—
T02	SLP# active to CPUSTP# and PCISTP# active	—	2	RTCCLK	—
T03	CPUSTP# and PCISTP# active to SUSA# active	—	1	RTCCLK	—
T04	Wakeup Event to SUSA# inactive	—	2	RTCCLK	—
T05	SUSA# inactive to CPUSTP# and PCISTP# inactive	16	32	ms	1
T06	CPUSTP# and PCISTP# inactive to SLP# inactive	1.03	2.03	ms	2
T07	SLP# inactive to STPCLK# inactive	—	1	RTCCLK	—

Note:

1. If D17F0 Rx95[7] = 1, the minimum delay is 1ms and the maximum delay is 2ms.
2. If D17F0 Rx95[7] = 1, the minimum delay is 155us and the maximum delay is 310us.

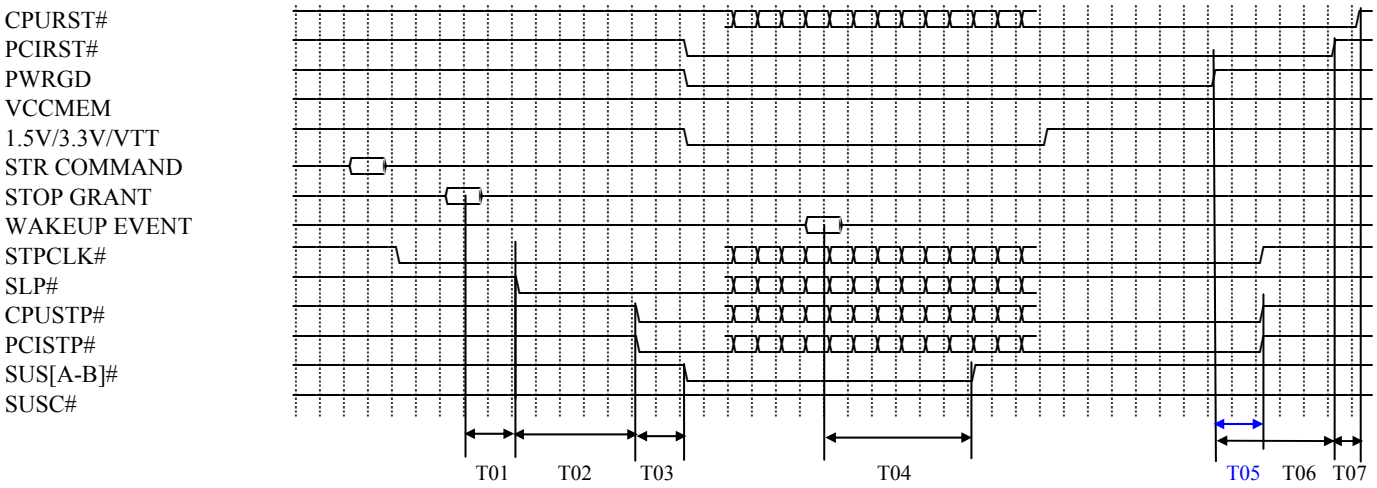


Figure 17. Suspend to RAM (S3) and Resume Sequence

Symbol	Parameter	Min	Max	Unit	Note
T01	STOP GRANT to SLP# active	—	1	RTCCLK	—
T02	SLP# active to CPUSTP# and PCISTP# active	—	2	RTCCLK	—
T03	CPUSTP# and PCISTP# active to SUS[A-B]# active	—	1	RTCCLK	—
T04	Wakeup Event to SUS[A-B]# inactive	—	2	RTCCLK	—
T05	PWRGD active to CPUSTP/PCISTP# inactive	1.03	2.03	ms	1
T06	PWRGD active to PCIRST# inactive	7	—	ms	—
T07	PCIRST# inactive to CPURST# inactive	12	—	us	2

Note:

1. If D17F0Rx95[7]=0, the minimum delay is 16ms and maximum delay is 32ms.
2. CPURST# is de-asserted at the completion of the ROMSIP cycle.

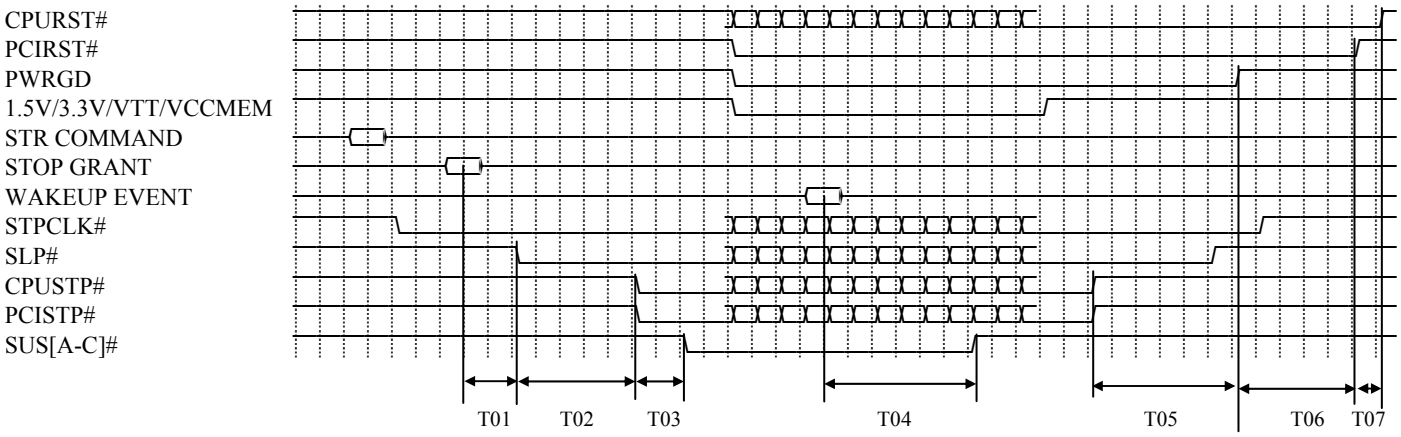


Figure 18. Suspend to DISK (S4) and Resume Sequence

Symbol	Parameter	Min	Max	Unit	Note
T01	STOP GRANT to SLP# active	–	1	RTCCLK	–
T02	SLP# active to CPUSTP# and PCISTP# active	–	2	RTCCLK	–
T03	CPUSTP# and PCISTP# active to SUS[A-C]# active	–	1	RTCCLK	–
T04	Wakeup Event to SUS[A-C]# inactive	–	2	RTCCLK	–
T05	PWRGD active to CPUSTP/PCISTP# inactive	1.03	2.03	ms	1
T06	PWRGD active to PCIRST# inactive	7	–	ms	–
T07	PCIRST# inactive to CPURST# inactive	12	–	us	2

Note:
1. If D17F0 Rx95[7]=0, the minimum delay is 16ms and maximum delay is 32ms.
2. CPURST# is de-asserted at the completion of the ROMSIP cycle.

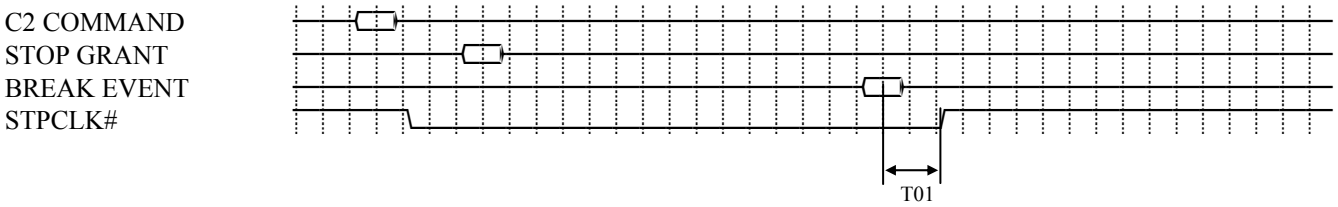


Figure 19. CPU C2 Sequence

Symbol	Parameter	Min	Max	Unit	Note
T01	Break Event to STPCLK# inactive	2	—	PCICLK	—

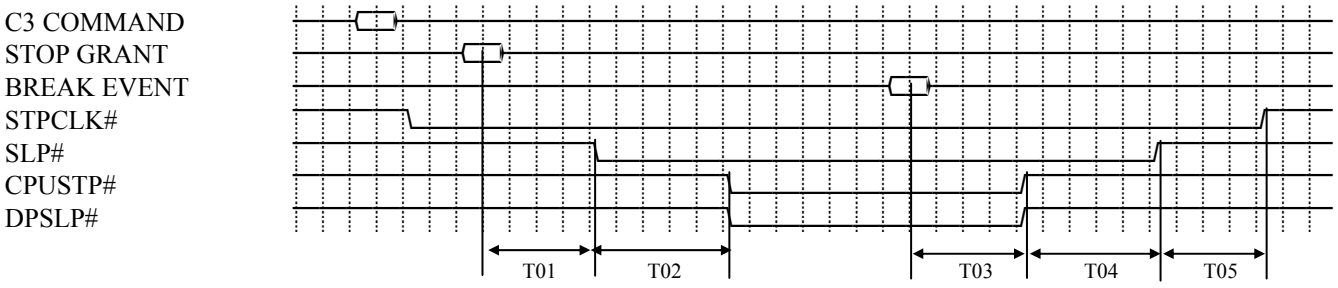


Figure 20. CPU C3 Sequence

Symbol	Parameter	Min	Max	Unit	Note
T01	STOP GRANT to SLP# active	0.83	1.66	us	1, 2
T02	SLP# active to CPUSTP# and DPSLP# active	1	1.25	us	1, 2
T03	Break Event to CPUSTP# and DPSLP# inactive	0.83	1.66	us	1, 2
T04	CPUSTP# and DPSLP# inactive to SLP# inactive	15	23.5	us	1, 3
T05	SLP# inactive to STPCLK# inactive	0.83	0.83	us	1, 2

Note:
1. Refer to BIOS Porting Guide for suggested values and System Programming Manual for register definitions.
2. The time sequence with 2T (1T=0.03us) offset is valid.
3. The time sequence with 2T (1T=0.83us) offset is valid.

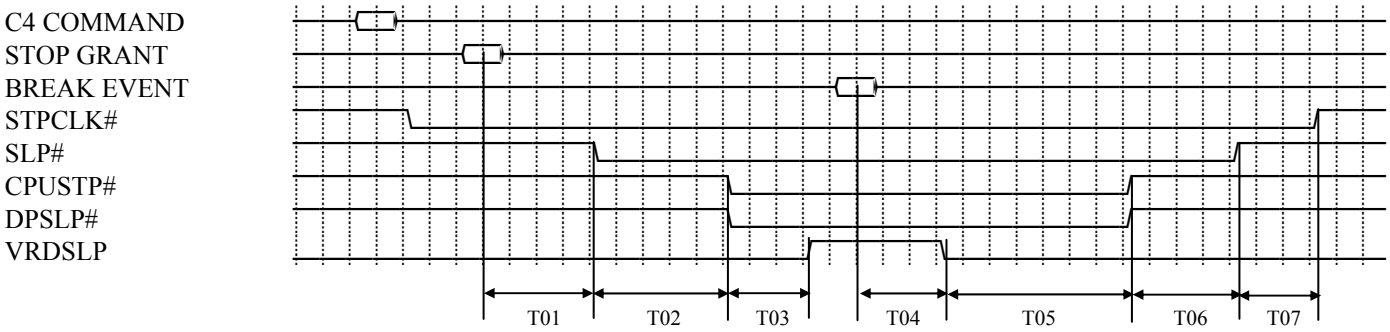


Figure 21. CPU C4 Sequence

Symbol	Parameter	Min	Max	Unit	Note
T01	STOP GRANT to SLP# active	0.83	1.66	us	1, 2
T02	SLP# active to CPUSTP# and DPSLP# active	1	1.25	us	1, 2
T03	CPUSTP# and DPSLP# active to VRDSLP active	0.63	0.83	us	1, 2
T04	Break Event to VRDSLP inactive	0	0.83	us	1, 2
T05	VRDSLP inactive to CPUSTP# and DPSLP# inactive	11.5	13.5	us	1, 3
T06	CPUSTP# and DPSLP# inactive to SLP# inactive	15	23.5	us	1, 3
T07	SLP# inactive to STPCLK# inactive	0.83	0.83	us	1, 2

Note:

1. Refer to BIOS Porting Guide for suggested values and System Programming Manual for register definitions.
2. The time sequence with 2T (1T=0.03us) offset is valid.
3. The time sequence with 2T (1T=0.83us) offset is valid.

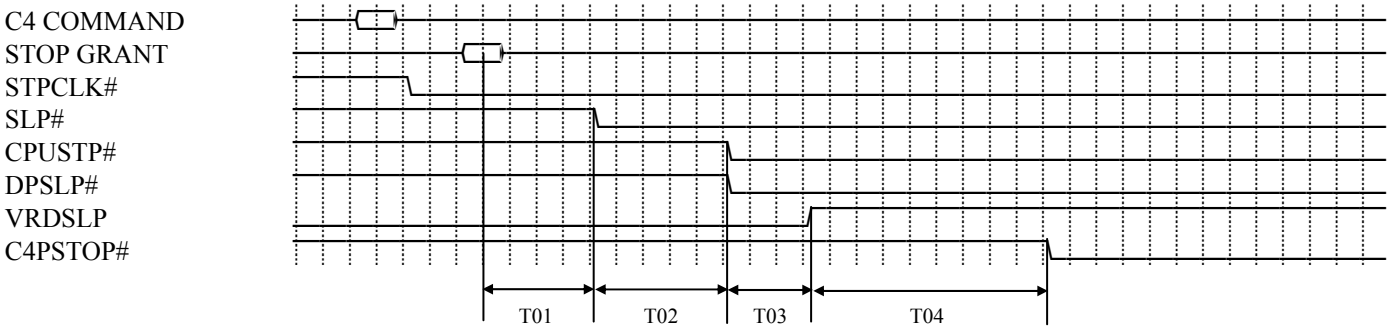


Figure 22. CPU C4P Entrance Sequence

Symbol	Parameter	Min	Max	Unit	Note
T01	STOP GRANT to SLP# active	7.5	–	us	1
T02	SLP# active to CPUSTP# and DPSLP# active	11.25	–	us	1
T03	CPUSTP# and DPSLP# active to VRDSLP active	3.75	–	us	1
T04	VRDSLP active C4PSTOP# active	30.03	–	us	–

Note:

1. Refer to System Programming Manual for detail of configuration settings.

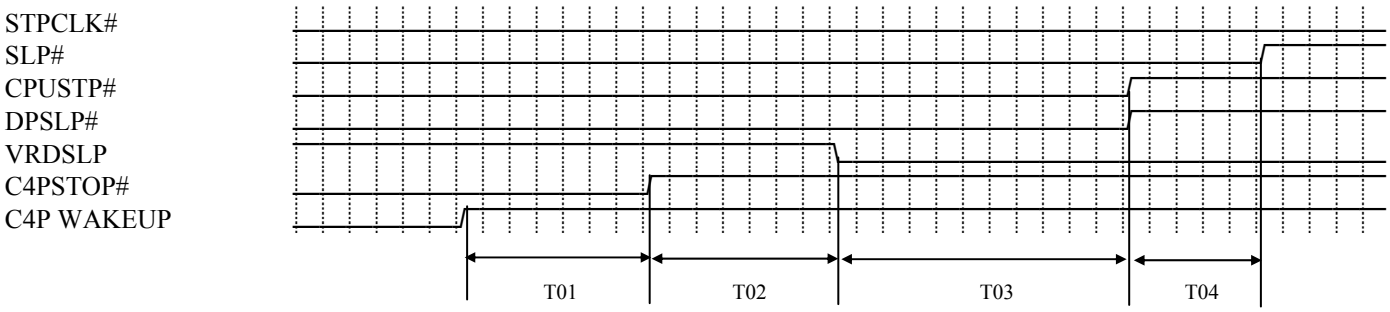


Figure 23. CPU C4P Exit Sequence

Symbol	Parameter	Min	Max	Unit	Note
T01	C4P WAKEUP active to C4PSTOP# inactive	30	—	us	—
T02	C4PSTOP# inactive to VRDSLP inactive	180	—	us	—
T03	VRDSLP inactive to DPSLP# and CPUSTP# inactive	90	110	us	1
T04	CPUSTP# and DPSLP# inactive to SLP# inactive	7.5	—	us	1

Note:

1. Refer to System Programming Manual for detail of configuration settings.

Package Thermal Simulation

Heat sink is required for this chip.
The compression force limit of this chip is 100 psi.

Package Specification	Simulation Result	
	Thermal Characterization (unit: ºC/W)	
	Vflow (m/s)	θja
FCBGA 33 x 33 mm	0.00	13.44
	1.00	9.70
	2.00	8.58
	4.00	7.61
	θjc	0.01
	θjb	6.77

Vflow (m/s): Velocity of external flow passing by the package

T_j (ºC): Junction temperature

T_a (ºC): Ambient temperature

T_cx (ºC): Temperature on whole top surface equal to ambient temperature

θjc (ºC/W): Junction-to-case thermal resistance
θjc = (T_j-T_cx) / Power where Tcase equal to Ta

θja (ºC/W): Junction-to-ambient thermal resistance
θja = (T_j-T_a) / Power

θjb (ºC/W): Junction-to-board thermal resistance

MECHANICAL SPECIFICATIONS

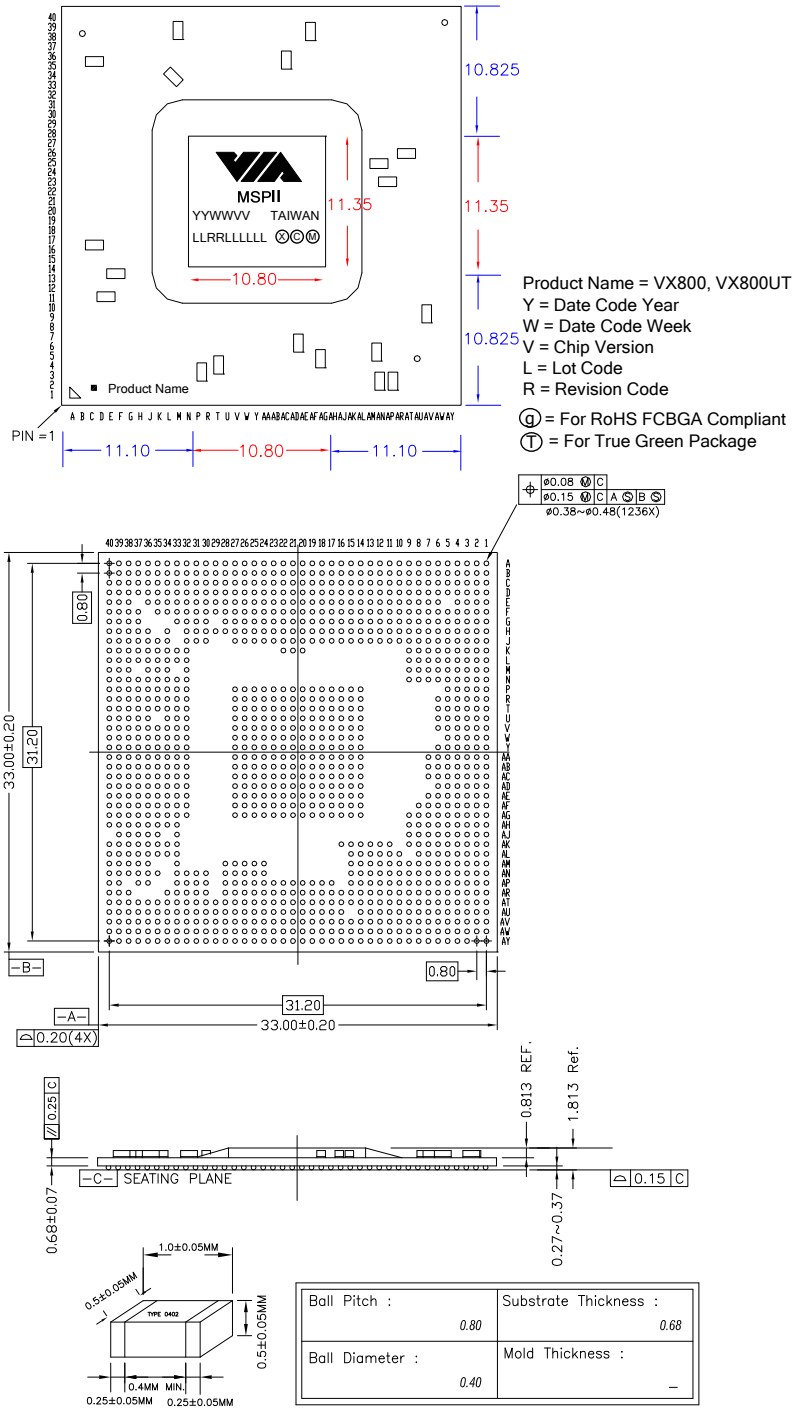


Figure 24. RoHS and True Green Mechanical Specifications – FCBGA-1086 Ball Grid Array Packages