Data Sheet

VX900 Series

All-in-One
System Processor

Preliminary Revision 1.0
September 3, 2010

VIA TECHNOLOGIES, INC.

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Offices:

VIA Technologies Incorporated
USA Office:
940 Mission Court
Fremont, CA 94539
USA
Tel: (510) 683-3300
Fax: (510) 683-3301 or (510) 687-4654
Home Page: http://www.viatech.com

VIA Technologies Incorporated
Taiwan Office:
1st Floor, No. 531
Chung-Cheng Road, Hsin-Tien
Taipei, Taiwan ROC
Tel : (886-2) 2218-5452
Fax : (886-2) 2218-5453
Home page: http://www.via.com.tw

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1.0	9/03/10	Initial public release	DA

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DOCUMENT INTRODUCTION

This document includes specifications of VX900M and VX900 models, please refer to Table 1 for the detailed specifications.

Table 1. VX900M and VX900 Feature Comparison Table

Product Model	VX900M VX900MH *	VX900 VX900H *
FSB Speed (MHz)	400-800	400-800
Memory Type	Single channel DDR2 667 DDR3 800	Single channel DDR2 800 DDR3 1066
PCI Express	3 ports: 3*1 Gen1 (1.1)	4 ports: 1*8 + 3*1 Gen2 (1.1 / 2.0)
Video Interface	LVDS – single channel	
	HDMI – 1 port	
	Display Port – 2 ports	
Video Decoding	HD capable	BD capable
Core Voltage	1.0V	1.2V

Note: VX900H and VX900MH are with HDCP capability supported, while VX900 and VX900M are not.

VX900 SERIES

A LOW POWER ALL-IN-ONE SYSTEM PROCESSOR

400 – 800 MHz FSB VIA C7(M) / Nano Processor
DDR2 800 / DDR3 1066 SDRAM Controller
Integrated Chrome9 HD DX9 3D / 2D Graphics & Video Processor
Blu-Ray Ready *(VX900 Only)*
Unified Video Decoding Accelerator
Integrated LVDS and HDMI Transmitter
DisplayPort™ Support
One 8-Lane PCIe port and Three 1-Lane PCIe ports
Eight USB 2.0 / 1.1 Ports, One USB Device Port
One SDIO Port, Four UART Ports, SPI, RTC, LPC and SMBus
SD / MS Pro / xD Memory Card Controller
High Definition Audio Controller
ACPI and Comprehensive Power Management

PRODUCT FEATURES

- **Process Technology**
  - **VX900M:** 80nm, 1.0V core voltage
  - **VX900:** 80nm, 1.2V core voltage
- **Package**
  - 31 x 31mm FCBGA package (Flip Chip Ball Grid Array) with 1089 balls and 0.8mm ball pitch
- **CPU Support**
  - VIA C7(M) / Nano processor with V4 protocol
  - 800 / 533 / 400 MHz FSB support
- **Memory Sub-system**
  - **VX900M:** Supports DDR3 800 and DDR2 667 MHz SDRAM
  - **VX900:** Supports DDR3 1066 and DDR2 800 MHz SDRAM
  - Supports 64/32-bit data width without ECC
  - Supports 64Mb / 128Mb / 256Mb / 512Mb / 1Gb / 2Gb / 4Gb (x8 / x16) with 8-bank device support
  - Supports CL 4T ~ 11T for DDR3
    Supports CL 2T ~ 9T for DDR2
  - Supports 2 unbuffered double-sided DIMMs
  - Supports up to 8GB physical memory size

- **Advanced High Bandwidth PCI Express Interface**

VX900:

– Compatible with PCI Express 2.0
– Four PCI Express ports supported
  – ***1st port***: a 8-lane port for high-end graphics interface
    – Configurable lane width, 8 / 4 / 1, through hand-shaking for transfer rate up to 4 GB/sec bidirectional
    – Configurable lane combinations: one 8-lane / one 4-lane + one DP port
    – Supports two upstream virtual channels
  – ***2nd - 4th ports***: Three 1-lane ports for peripheral devices
    – Configurable lane combination: 3 x 1-Lane or 1 x 2-Lane + 1 x 1-Lane

VX900M:

– Compatible with PCI Express 1.1
– Three 1-lane PCI Express ports for peripheral devices
  – Configurable lane combinations: 3 x 1-Lane or 1 x 2-Lane + 1 x 1-Lane
– Supports interconnect power management
– Supports polarity reversal
– Supports Hot Plug
– Loop-back testing mode for easy debugging mode for PCI Express

- **Chrome9 HD DX9 Integrated Graphics Processor with 2D / 3D / Video Controllers**

– Optimized Unified Memory Architecture (UMA)
– Supports up to 512 MB frame buffers size
– PCI v2.3 Host Bus compliant

2D Graphics Processor

– 128-bit 2D graphics engine
– Hardware 2D rotation
– Supports ROP3, 256 operations
– Supports 8bpp, 16bpp and 32bpp color depth modes
– BitBLT (Bit Block Transfer) functions including alpha BLTs
– Color expansion, source Color Key and destination Color Key
– Bresenham line drawing / style line function
– Transparency mode
– Window clipping
– Text function

3D Graphics Processor

– 128-bit DX-9 engine with 2PS and 2VS
– DirectX 9.0 programmable graphics engine
– 2x Pixel Shader (SM 2.0)
– 2x Vertex Shader
– Internal full ARGB 2-10-10-10 format for high rendering quality
– 96-bit (4xFP24) Pixel Precision
– Pixel Shader supports 16 concurrent texture map references per rendering pass
– Shadow volume acceleration (2-Sided Stencil)
– Unconditional non-power-of-2 textures
– MIP-Mapped volume/cube maps
– Floating point render target/texture formats
– Vertex cache
– Color buffer with sRGB format supported and blending with color field 1.0
– Supports various texture formats, including 16/32bpp RGB, 32bpp sRGB, YUV422, V410, L16 compressed texture (DXTC) and depth texture
– Video texture supported with programmable de-Gamma
– Multiple render target (MRT) up to 4
– Perspective color, fog, texture

- High quality texture filtering with bi-linear, tri-linear, anisotropy (up to 16x by trilinear), or programmable 4x4 filter (Gaussian filter, HP filter, LP filter)
- Maximum 28.5M polygon/sec and 400M pixels/sec for 2 texture
- 8K texture cache
- Flat and Gouraud shading
- Linear address
- Hardware back-face culling
- 16-bit and 32-bit Z test and 24+8 Z+ stencil test support
- Edge anti-aliasing
- Two texture per pass
- Alpha blending
- Hardware bump-mapping

Hi-Def Video Processing and Display

- Supports Chromotion programmable video engine
- Bob, Weave and Motion-Adaptive de-interlacing modes
- Supports 3:2 / 2:2 / 2:3:3:2 pull-down detection
- Supports all other cadence detection including 2:2:2:4/3:2:3:2:2/5:5/6:4/8:7 format
- Supports color enhanced effects as brightness, contrast, hue and saturation adjustment
- Supports color space conversion
- Hardware DVD sub-picture blending
- High quality video up / down scaling engine supports input up to 1920 pixels wide
- Supports Microsoft VMR through front-end video scaling, color space conversion and blending
- Image sharpening and de-blocking
- True-color hardware cursor (64x64x32bpp) with 256-level blending effect
- Support two Video Display engines for multi-video windows application as picture-in-picture and video conference
- High quality scaling (up or down) in both horizontal and vertical direction on the display pipe

Video Capture Capability

- Supports parallel and serial Transport Stream inputs
- Supports 8-bit or 16-bit CCIR656/601input
- Video capture and playback tear free auto flipping
- External Hsync / Vsync support
- Supports HD capture for resolution up to 1080i60 or 1080p30

- **Unified Video Decoding Accelerator**
  - Blu-Ray ready (***VX900 only***)
  - Hardware video playback is available only in memory 64-bit data width mode

MPEG-2 Decoding Mode

- Fully compatible with ISO/IEC 13818-2 MPEG2 specification in Main Profile
- Supports VLD (Variable Length Decode) level of HW acceleration
- Supports motion compensation level of HW acceleration
- Supports MP@HL

MPEG-4 Decoding Mode

- Supports MPEG4 (ISO/IEC 14496-2)
- Supports MPEG4 ASP (Advanced Simple Profile) Level 5
- Supports I, P, and B VOPs
- Supports interlaced frame decoding
- Supports ¼-pixel MC support
- High video quality and performance

VC1 / WMV Decoding Mode

- Accelerates AP@L3 decoding from VLD or iDCT level
- Supports adaptive macroblock quantization
- Supports variable-sized iDCT Transform
- Supports intensity compensation
- Supports de-blocking filtering
- Supports range remapping
- Supports interlace field and frame coding modes
- VC-1 AP, VC-1 SP/MP (WMV)

H.264 Decoding Mode

- Accelerates HP@L4.1 H.264 stream from VLD level
- Supports multi-mode, multi-reference MC
- Supports interlaced frame / MBAFF decoding
- Supports CAVLC and CABAC
- Supports inter / intra prediction
- Supports inner loop de-block filter
- Supports 4x4 / 8x8 integer transform
- Supports B-frame prediction weighting
- BP / MP / HP (CABAC or CAVLC) up to Level 4.1

- **Display Support for Video Output**

– A dedicated CRT interface
– A single-channel LVDS transmitter
– A digital video output port (DVP1) to external HDMI / LVDS / DVI transmitter and TV Encoder
– A multiplexed display interface for DisplayPort™ / HDMI
– A multiplexed display interface for DisplayPort™ / PCI Express

Display Port Interface

– Two DisplayPort™: DP1 (multiplexed with HDMI) and DP2 (multiplexed with PCIe)
– Industry standard compliance
  – Compatible with DisplayPorts 1.1a, CEA-861-C and HDCP1.3
– Video support
  – VESA DMT and CVT timing standards
  – Output format
    – 24-bpp RGB / YCbCr 4:4:4
    – 18-bpp RGB
    – 30-bpp RGB / YCbCr 4:4:4
    – 16-bpp YCbCr 4:2:2
    – 20-bpp YCbCr 4:2:2
– Audio support
  – Compliant with IEC 60958 standard
  – Supports up to eight channels of LPCM at 192kHz with a 24-bit sample size
– Main link support
  – 1 / 2 / 4 lane
  – 2.7 / 1.62Gbps link rate
  – TU size: 32 – 64
  – Default and enhance framing mode
– Maximum supported resolution
  – **VX900M**: 2048 x 1536 at 60Hz
  – **VX900**: 2048 x 1536 at 75Hz

HDMI (High-Definition Multimedia Interface)

– Supports up to two HDMI output
  – One through integrated HDMI interface (multiplexed with DP1)
  – Another through DVP1 with external HDMI transmitter
– Compatible with HDMI specification version 1.2 and HDCP 1.3
– Video pixel encoded in RGB 4:4:4 / YCbCr 4:4:4 / YCbCr 4:2:2 formats
– 24 bits per pixel transferred
– Pixel rate up to 225MHz
– Supports 1x, 2x, 4x pixel-repetition in CEA-861

Integrated LVDS Transmitter

– Compatible with TIA/EIA-644
– Support pixel clock up to 85Mhz
– Supports panel resolution up to WXGA (1366 x 768)
– Supports one single-channel 18-bit or 24-bit LVDS panel

LVDS Panel Interface (DVP1)

– Supports panel resolution from UXGA (1600 x 1200) through external LVDS transmitter and Digital Video Port.

TTL LCD Panel Interface (DVP1)

– Supports 18-bit TTL LCD panel interface

TV-Out Interface (DVP1)

– 12-bit / 16-bit / 20-bit interface to external TV encoder for NTSC or PAL TV or HDTV display

12-bit DVI Transmitter Interface (DVP1)

- Double-data-rate data transfer with clock rates up to 165 MHz
- Built-in digital phase adjuster to fine-tune signal timing between clock and data bus
- Optional 16-bit ARGB interface (DVP1)
- Video data output to external HDMI (High-Definition Multimedia Interface) transmitter

CRT Display Interface

- Three 10-bit true-color RAMDAC up to 350 MHz pixel rate with gamma correction capability
- Supports CRT resolutions up to 2048 x 1536

• DuoView+™ Dual Image Capability

- Multi-monitor, extended desktop support
- Two independent display engines which can display completely different information at different resolutions, pixel depths, and refresh rates
- CRT and LVDS/DVI panel refresh rates are independently programmable for optimum image quality

• Full Software Support

- Microsoft DirectX 7.0, 8 .0 and 9.0 compatible
- Microsoft DirectX Texture Compression (DXTC / S3TC)
- Supports OpenGL™ 1.4
- Drivers for major WinXP APIs: Direct3D™, DirectDraw™, DirectShow™ and OpenGL™ ICD
- Supports Microsoft Windows 7, Windows Vista, XP and Windows CE
- Supports Linux

• Graphics Power Management Support

- Built-in reference voltage generator and monitor sense circuits
- Automatic panel power sequencing and VESA DPMS (Display Power Management Signaling) CRT power-down
- External I/O signal controls enabling of graphics accelerator into standby / suspend-off state
- Dynamic clock gating for inactive functions to achieve maximum power saving
- Extensive display power management
- I^2C Serial Bus and DDC / E-DDC Monitor Communications for Plug-and-Play configuration

- **High Definition (HD) Audio Controller**
  - High performance audio controller with 192 KHz sample rate, 32-bit per sample and up to 8 channels
  - Microsoft UAA (Universal Audio Architecture) driver support
  - Up to three independent playback streams and audio codecs
  - Multiple recording channels for array microphone
  - Supports jack sensing / retasking
- **Serial ATA 2.0 Controller**
  - Compliant with Serial ATA Specification Revision 2.6
  - Support up to 2 S-ATA devices
  - Integrated S-ATA PHY supports both 1.5 and 3Gbit/s transfer speed
  - Support PCI native and ATA compatibility modes
  - Supports RAID and SATA Port Multiplier
- **Universal Serial Bus Controller**
  - USB 2.0 and Enhanced Host Controller Interface (EHCI) v1.0 compliant
  - USB 1.1 and Universal Host Controller Interface (UHCI) v1.1 compliant
  - Eight USB host ports and one USB device port
  - Legacy keyboard and PS/2 mouse support
  - One USB 2.0 debug port
- **SPI Controller**
  - Supports two SPI master ports
  - Supports SPI ROM
  - Supports to write 256 bytes in one shot
  - Supports external plug programmer to update BIOS data
  - Supports dynamic clock stop
  - Supports 16-byte data buffer
  - Programmable clock rate
- **SDIO Host Controller**
  - Compliant with SD Host Controller Standard Specification ver. 1.00 with both DMA and PIO mode.
  - Compliant with SD Memory Card Specification ver. 2.0.
  - Supports SD 1-bit and 4-bit data transfer modes
  - 1 independent SDIO port multiplexed with card reader interface
  - Supports up to 7 functions in SDIO 1-bit or 4-bit mode with each slot
  - Supports host clock rate from 187.5KHz to 48MHz
  - Supports high-speed SDIO card with up to 192Mbit/sec transfer rate
  - Supports multiple block transaction with stop command
  - Supports wakeup control
  - Support 1.8V and 3.3V SD Bus Voltage
  - Supports both DMA and PIO modes
  - Supports single block or multiple block read / write transaction
  - Supports host controller base clock 33 MHz and 48 MHz

- **MemoryStick™ (MS) / MemoryStick Pro™ (MS Pro) Interfaces**
  - Complies with MemoryStick interface specification
  - Supports 4-bit and 1-bit MS Pro interface
  - Fully supports Memory Stick Pro TPCs
  - Hardware CRC16 generation and verification
  - Supports multi-page access
  - Supports flash command timeout detection
  - Supports over clock rate up to 48MHz
- **Secure Digital™ (SD) / Multi Media Card™ (MMC) Interfaces**
  - Complies with Secure Digital/MMC interfaces specification
  - Supports 4-bit and 1-bit Secure Digital interface
  - Complies with SD Memory Card Specifications rev. 2.0
  - Command transmit and response receive can be enabled separately
  - Hardware CRC7 generation and verification on CMD
  - Hardware CRC16 generation and verification on DAT
  - Optional single byte/bit operation on both CMD and DAT
  - Data processing in block or byte
  - Supports multiple block transaction with stop command
  - Supports different clock rate from 375 KHz to 48 MHz
- **Multi Media Card™ Interface**
  - Compliant with MMC 4.0 standard specification
  - Compliant with eMMC 4.3 standard specification
  - Supports MMC 1/4/8-bit data transfer modes
  - Supports 375KHz~48MHz host clock rate
  - Supports high-speed MMC card with up to 384Mbit/sec transfer rate
  - Supports single and multiple block transaction
- **xD-Picture™ (xD) Card Interface**
  - Built-in hardware 1-bit ECC
  - Supports hardware address mapping
- **Concurrent PCI Bus Controller**
  - PCI 2.3 compliant, 33MHz, 32 bit, 3.3V PCI interface with 5V tolerant inputs
  - Supports two PCI masters
  - Zero wait state PCI master and slave burst transfer rate, with up to 132 MB/sec data transfer rate
  - PCI master snoop ahead and snoop filtering
  - Byte merging in the write buffers to reduce the number of PCI cycles
  - Supports delay transaction
  - Transaction timer for fair arbitration between PCI masters
  - Symmetric arbitration between Host / PCI bus for optimized system performance
  - Complete steerable PCI interrupts
  - Supports PC / PCI DMA
- **System Management Bus Interface**
  - Compliant with System Management Bus (SMBus) Revision 2.0
  - I2C devices compatible
  - Supports SMBus Address Resolution Protocol (ARP) by using host commands through software
  - Supports slave interface for external SMBus masters to control resume events
  - Supports Alarm-On-LAN 2 through a SMBus-interfaced register

- **Plug and Play Functions**
  - Steerable PCI interrupts
  - Steerable interrupts for integrated peripheral controllers
  - Microsoft Windows Plug and Play BIOS compliant
- **Integrated Legacy Functions**
  - Integrated Keyboard Controller with PS2 mouse and password wake-up support
  - Integrated two RS-232 serial ports with DMA support (optional)
  - Integrated DS12885-style Real Time Clock with extended 256 byte CMOS RAM, Day / Month Alarm and century field
  - Integrated DMA, timer, and interrupt controller
  - Fast reset and Gate A20 operation
- **Comprehensive Power Management**
  - ACPI 3.0 and APM v1.2 Compliant
  - Supports CPU clock throttling and clock stop during ACPI C2 / C3 / C4 states
  - Supports normal, doze, sleep, suspend and conserve modes
  - Supports multiple system suspend types: Power-on Suspend (POS) with flexible CPU / PCI bus reset options, Suspend to DRAM (STR), and Suspend to Disk (STD), all with hardware automatic wake-up
  - Integrates an idle timer, a peripheral timer and a general purpose timer, plus a 24/32-bit ACPI compliant timer
  - Supports extensive LCD panel display power management
  - Multiple suspend power plane controls and suspend status indicators
  - Global and local device power control
  - Supports system event monitoring with two event classes
  - Dedicated input pins for power and sleep buttons, and external modem ring indicator
  - Flexible and programmable internal / external SMI sources
  - Thermal alarm on external temperature sensing circuit
  - Dynamic clock gating control on functional blocks
  - Dynamic I/O pad driving control
  - I/O pad leakage control
- **Built-in NAND-tree Pin Scan Test Capability**

BALLOUTS

VX900 Ball Map

Figure 1. VX900 Ball Map – Left Side Top View

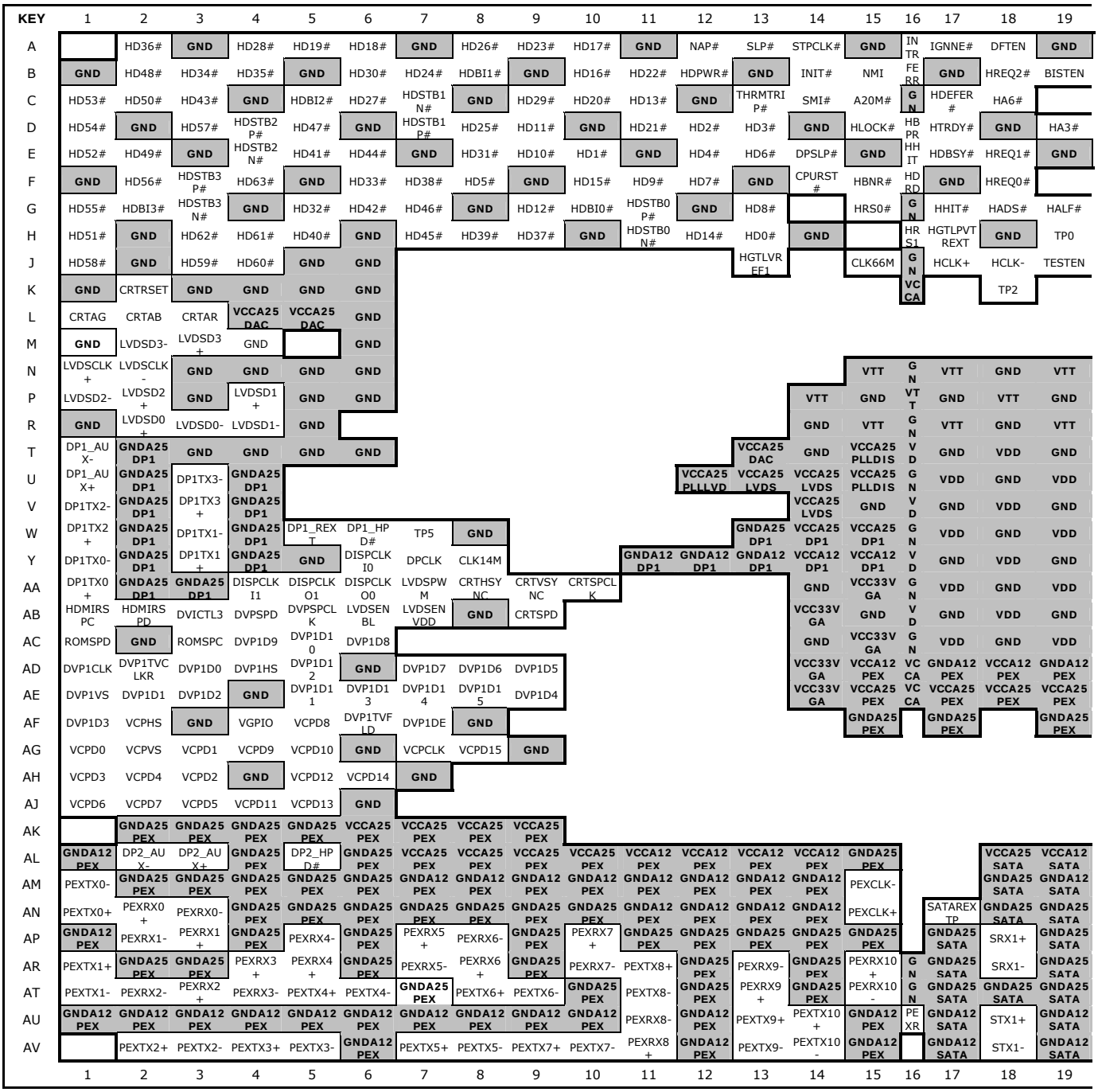
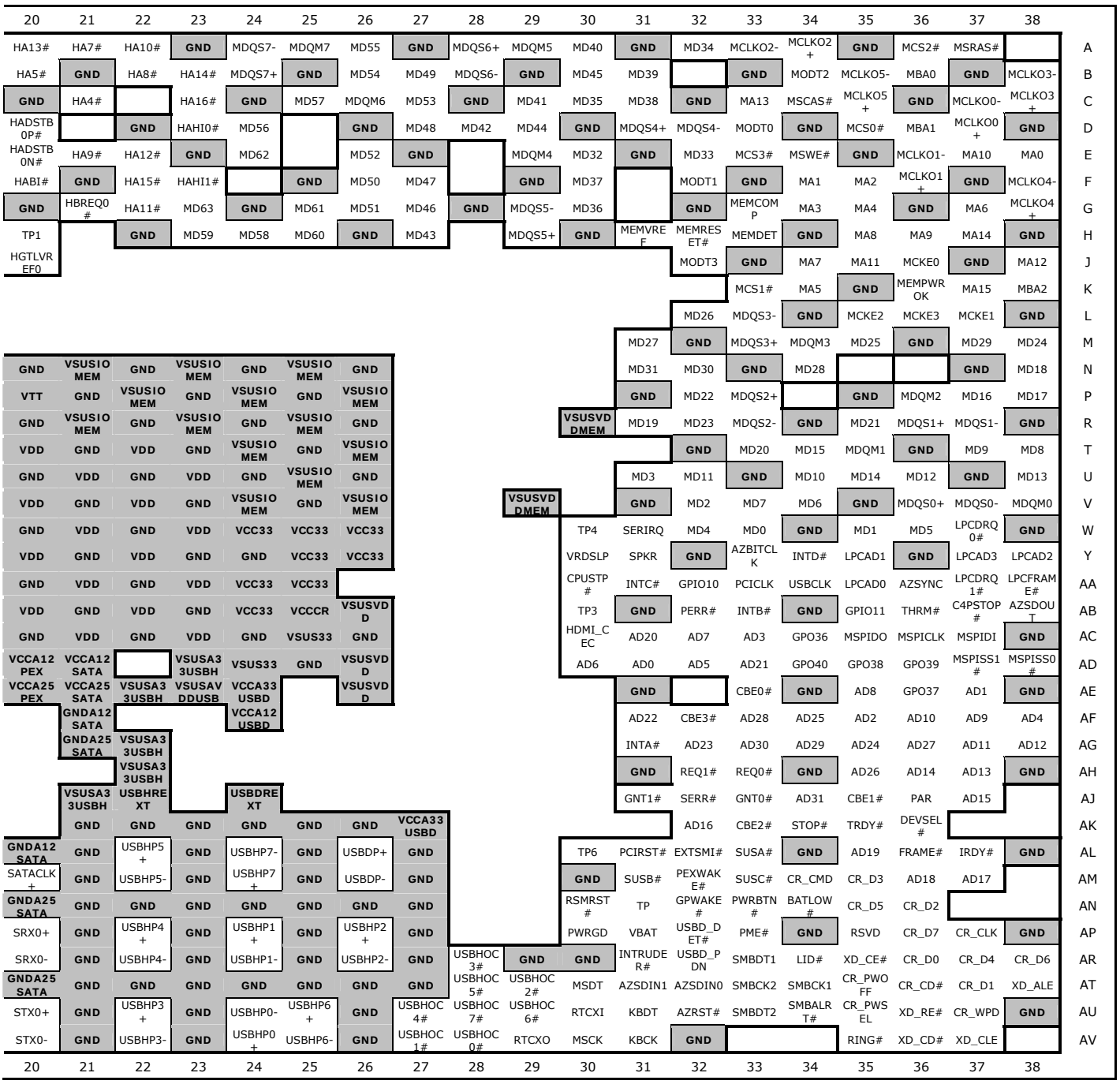


Figure 2. VX900 Ball Map – Right Side Top View



	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	
A	HA13#	HA7#	HA10#	GND	MDQS7-	MDQM7	MD55	GND	MDQS6+	MDQM5	MD40	GND	MD34	MCLKO2-	MCLKO2+	GND	MCS2#	MSRAS#		A
B	HA5#	GND	HA8#	HA14#	MDQS7+	GND	MD54	MD49	MDQS6-	GND	MD45	MD39		GND	MODT2	MCLKO5-	MBA0	GND	MCLKO3-	B
C	GND	HA4#		HA16#	GND	MD57	MDQM6	MD53	GND	MD41	MD35	MD38	GND	MA13	MSCAS#	MCLKO5+	GND	MCLKO0-	MCLKO3+	C
D	HADSTB0P#		GND	HAHI0#	MD56		GND	MD48	MD42	MD44	GND	MDQS4+	MDQS4-	MODT0	GND	MCS0#	MBA1	MCLKO0+	GND	D
E	HADSTB0N#	HA9#	HA12#	GND	MD62		MD52	GND		MDQM4	MD32	GND	MD33	MCS3#	MSWE#	GND	MCLKO1-	MA10	MA0	E
F	HABI#	GND	HA15#	HAHI1#		GND	MD50	MD47		GND	MD37		MODT1	GND	MA1	MA2	MCLKO1+	GND	MCLKO4-	F
G	GND	HBREQ0#	HA11#	MD63	GND	MD61	MD51	MD46	GND	MDQS5-	MD36		GND	MEMCOMP	MA3	MA4	GND	MA6	MCLKO4+	G
H	TP1		GND	MD59	MD58	MD60	GND	MD43		MDQS5+	GND	MEMVREF	MEMRESET#	MEMDET	GND	MA8	MA9	MA14	GND	H
J	HGTLVREF0												MODT3	GND	MA7	MA11	MCKE0	GND	MA12	J
K														MCS1#	MA5	GND	MEMPWROK	MA15	MBA2	K
L													MD26	MDQS3-	GND	MCKE2	MCKE3	MCKE1	GND	L
M												MD27	GND	MDQS3+	MDQM3	MD25	GND	MD29	MD24	M
N												MD31	MD30	GND	MD28			GND	MD18	N
P												GND	MD22	MDQS2+		GND	MDQM2	MD16	MD17	P
R											VSUSVDDMEM	MD19	MD23	MDQS2-	GND	MD21	MDQS1+	MDQS1-	GND	R
T													GND	MD20	MD15	MDQM1	GND	MD9	MD8	T
U												MD3	MD11	GND	MD10	MD14	MD12	GND	MD13	U
V										VSUSVDDMEM		GND	MD2	MD7	MD6	GND	MDQS0+	MDQS0-	MDQM0	V
W												TP4	SERIRQ	MD4	MD0	GND	MD1	MD5	LPCDRQ0#	GND	W
Y												VRDSLP	SPKR	GND	AZBITCLK	INTD#	LPCAD1	GND	LPCAD3	LPCAD2	Y
AA												CPUSTP#	INTC#	GPIO10	PCICLK	USBCLK	LPCAD0	AZSYNC	LPCDRQ1#	LPCFRAME#	AA
AB												TP3	GND	PERR#	INTB#	GND	GPIO11	THRM#	C4PSTOP#	AZSDOUT	AB
AC												HDMI_CEC	AD20	AD7	AD3	GPO36	MSPIDO	MSPICLK	MSPIDI	GND	AC
AD												AD6	AD0	AD5	AD21	GPO40	GPO38	GPO39	MSPISS1#	MSPISS0#	AD
AE													GND		CBE0#	GND	AD8	GPO37	AD1	GND	AE
AF													AD22	CBE3#	AD28	AD25	AD2	AD10	AD9	AD4	AF
AG													INTA#	AD23	AD30	AD29	AD24	AD27	AD11	AD12	AG
AH													GND	REQ1#	REQ0#	GND	AD26	AD14	AD13	GND	AH
AJ													GNT1#	SERR#	GNT0#	AD31	CBE1#	PAR	AD15		AJ
AK														AD16	CBE2#	STOP#	TRDY#	DEVSEL#			AK
AL	GNDA12SATA	GND	USBHP5+	GND	USBHP7-	GND	USBDP+	GND				TP6	PCIRST#	EXTSMI#	SUSA#	GND	AD19	FRAME#	IRDY#	GND	AL
AM	SATACLK+	GND	USBHP5-	GND	USBHP7+	GND	USBDP-	GND				GND	SUSB#	PEXWAKE#	SUSC#	CR_CMD	CR_D3	AD18	AD17		AM
AN	GNDA25SATA	GND	GND	GND	GND	GND	GND	GND				RSMRST#	TP	GPWAKE#	PWRBTN#	BATLOW#	CR_D5	CR_D2			AN
AP	SRX0+	GND	USBHP4+	GND	USBHP1+	GND	USBHP2+	GND				PWRGD	VBAT	USBD_DET#	PME#	GND	RSVD	CR_D7	CR_CLK	GND	AP
AR	SRX0-	GND	USBHP4-	GND	USBHP1-	GND	USBHP2-	GND	USBHOC3#	GND	GND	INTRUDER#	USBD_PDN	SMBDT1	LID#	XD_CE#	CR_D0	CR_D4	CR_D6	AR
AT	GNDA25SATA	GND	GND	GND	GND	GND	GND	GND	USBHOC5#	USBHOC2#	MSDT	AZSDIN1	AZSDIN0	SMBCK2	SMBCK1	CR_PWOFF	CR_CD#	CR_D1	XD_ALE	AT	
AU	STX0+	GND	USBHP3+	GND	USBHP0-	USBHP6+	GND	USBHOC4#	USBHOC7#	USBHOC6#	RTCXI	KBDT	AZRST#	SMBDT2	SMBALRT#	CR_PWSEL	XD_RE#	CR_WPD	GND	AU
AV	STX0-	GND	USBHP3-	GND	USBHP0+	USBHP6-	GND	USBHOC1#	USBHOC0#	RTCXO	MSCK	KBCK	GND			RING#	XD_CD#	XD_CLE		AV
	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	

VX900 Signal Ball List

Table 2. VX900 Signal Ball List (Listed by Ball Name)

Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #
A20M#	C15	CRTSPD	AB09	GND	B33	GND	L06
AD0 / GPI10	AD31	CRTVSYNC	AA09	GND	B37	GND	L34
AD1 / GPI11	AE37	DEVSEL# / SIN2	AK36	GND	C04	GND	L38
AD2	AF35	DFTEN	A18	GND	C08	GND	M01
AD3	AC33	DISPCLKI0 / VGPI0	Y06	GND	C12	GND	M04
AD4 / GPO4	AF38	DISPCLKI1 / VGPI1	AA04	GND	C16	GND	M06
AD5	AD32	DISPCLKO0 / VGPO0	AA06	GND	C20	GND	M32
AD6	AD30	DISPCLKO1 / VGPO1	AA05	GND	C24	GND	M36
AD7	AC32	DP1_AUX-	T01	GND	C28	GND	N03
AD8	AE35	DP1_AUX+	U01	GND	C32	GND	N04
AD9 / GPIO13	AF37	DP1_HPD#	W06	GND	C36	GND	N05
AD10 / GPIO14	AF36	DP1_REXT	W05	GND	D02	GND	N06
AD11 / GPIO15	AG37	DP1TX0- / HDMITX2-	Y01	GND	D06	GND	N16
AD12 / GPIO16	AG38	DP1TX0+ / HDMITX2+	AA01	GND	D10	GND	N18
AD13 / GPIO17	AH37	DP1TX1- / HDMITX1-	W03	GND	D14	GND	N20
AD14 / GPIO18	AH36	DP1TX1+ / HDMITX1+	Y03	GND	D18	GND	N22
AD15 / GPIO19	AJ37	DP1TX2- / HDMITX0-	V01	GND	D22	GND	N24
AD16 / GPIO20	AK32	DP1TX2+ / HDMITX0+	W01	GND	D26	GND	N26
AD17 / GPIO21	AM37	DP1TX3- / HDMICLK-	U03	GND	D30	GND	N33
AD18 / GPIO22	AM36	DP1TX3+ / HDMICLK+	V03	GND	D34	GND	N37
AD19 / GPIO23	AL35	DP2_AUX-	AL02	GND	D38	GND	P03
AD20 / GPIO24	AC31	DP2_AUX+	AL03	GND	E03	GND	P05
AD21 / GPIO25	AD33	DP2_HPD#	AL05	GND	E07	GND	P06
AD22 / GPIO26	AF31	DPCLK	Y07	GND	E11	GND	P15
AD23 / GPIO27	AG32	DPSLP#	E14	GND	E15	GND	P17
AD24 / GPIO28	AG35	DVICTL3	AB03	GND	E19	GND	P19
AD25 / GPIO29	AF34	DVP1CLK	AD01	GND	E23	GND	P21
AD26 / GPIO30	AH35	DVP1D0 / RI1	AD03	GND	E27	GND	P23
AD27 / GPIO31	AG36	DVP1D1 / DCD1	AE02	GND	E31	GND	P25
AD28 / GPIO32	AF33	DVP1D2 / SOUT1	AE03	GND	E35	GND	P31
AD29 / GPIO33	AG34	DVP1D3 / SIN1	AF01	GND	F01	GND	P35
AD30 / GPIO34	AG33	DVP1D4 / DTR1	AE09	GND	F05	GND	R01
AD31 / GPIO35	AJ34	DVP1D5 / DSR1	AD09	GND	F09	GND	R05
AZBITCLK	Y33	DVP1D6 / RTS1	AD08	GND	F13	GND	R14
AZRST#	AU32	DVP1D7 / CTS1	AD07	GND	F17	GND	R16
AZSDIN0	AT32	DVP1D8 / RI0	AC06	GND	F21	GND	R18
AZSDIN1	AT31	DVP1D9 / DCD0	AC04	GND	F25	GND	R20
AZSDOUT	AB38	DVP1D10 / SOUT0	AC05	GND	F29	GND	R22
AZSYNC	AA36	DVP1D11 / SIN0	AE05	GND	F33	GND	R24
BATLOW# / GPI4	AN34	DVP1D12 / DTR0	AD05	GND	F37	GND	R26
BISTEN	B19	DVP1D13 / DSR0	AE06	GND	G04	GND	R34
C4PSTOP# / GPO6	AB37	DVP1D14 / RTS0	AE07	GND	G08	GND	R38
CBE0# / CTS3	AE33	DVP1D15 / CTS0	AE08	GND	G12	GND	T03
CBE1# / RI2	AJ35	DVP1DE	AF07	GND	G16	GND	T04
CBE2# / DCD2	AK33	DVP1HS	AD04	GND	G20	GND	T05
CBE3# / SOUT2	AF32	DVP1TVCLKR	AD02	GND	G24	GND	T06
CLK14M	Y08	DVP1TVFLD	AF06	GND	G28	GND	T14
CLK66M	J15	DVP1VS	AE01	GND	G32	GND	T17
CPURST#	F14	DVPSPCLK	AB05	GND	G36	GND	T19
CPUSTP# / GPO5	AA30	DVPSPD	AB04	GND	H02	GND	T21
CR_CD# / MMC_CD# / SD_CD# / SDIOCD#	AT36	EXTSMI# / GPI5	AL32	GND	H06	GND	T23
CR_CLK / MMC_CLK / XD_WE# / SD_CLK / SDIOCLK	AP37	FERR#	B16	GND	H10	GND	T25
CR_CMD / MMC_CMD# / XD_RB# / SD_CMD / SDIOCMD	AM34	FRAME# / CTS2	AL36	GND	H14	GND	T32
CR_D0 / MMC_D0 / XD_D0 / SD_D0 / SDIOD0	AR36	GND	A03	GND	H18	GND	T36
CR_D1 / MMC_D1 / XD_D1 / SD_D1 / SDIOD1	AT37	GND	A07	GND	H22	GND	U16
CR_D2 / MMC_D2 / XD_D2 / SD_D2 / SDIOD2	AN36	GND	A11	GND	H26	GND	U18
CR_D3 / MMC_D3 / XD_D3 / SD_D3 / SDIOD3	AM35	GND	A15	GND	H30	GND	U20
CR_D4 / MMC_D4 / XD_D4	AR37	GND	A19	GND	H34	GND	U22
CR_D5 / MMC_D5 / XD_D5	AN35	GND	A23	GND	H38	GND	U24
CR_D6 / MMC_D6 / XD_D6	AR38	GND	A27	GND	J02	GND	U26
CR_D7 / MMC_D7 / XD_D7	AP36	GND	A31	GND	J05	GND	U33
CR_PWOFF / SDIOPWOFF / GPO12	AT35	GND	A35	GND	J06	GND	U37
CR_PWSEL / SDIOPWSEL / GPO11	AU35	GND	B01	GND	J33	GND	V15
CR_WPD / XD_WP# / SD_WPD / SDIOWPD	AU37	GND	B05	GND	J37	GND	V17
CRTAB	L02	GND	B09	GND	K01	GND	V19
CRTAG	L01	GND	B13	GND	K03	GND	V21
CRTAR	L03	GND	B17	GND	K04	GND	V23
CRTHSYNC	AA08	GND	B21	GND	K05	GND	V25
CRTRSET	K02	GND	B25	GND	K06	GND	V31
CRTSPCLK	AA10	GND	B29	GND	K35	GND	V35

Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #
GND	W08	GND	AN21	GNDA12SATA	AM19	GNDA25SATA	AT18
GND	W16	GND	AN22	GNDA12SATA	AU17	GNDA25SATA	AT19
GND	W18	GND	AN23	GNDA12SATA	AU19	GNDA25SATA	AT20
GND	W20	GND	AN24	GNDA12SATA	AV17	GNT0# / SOUT3	AJ33
GND	W22	GND	AN25	GNDA12SATA	AV19	GNT1# / RTS3	AJ31
GND	W34	GND	AN26	GNDA25DP1	T02	GPIO10 / SATALED0#	AA32
GND	W38	GND	AN27	GNDA25DP1	U02	GPIO11 / SATALED1#	AB35
GND	Y05	GND	AP21	GNDA25DP1	U04	GPO36 / PCIERST1#	AC34
GND	Y17	GND	AP23	GNDA25DP1	V02	GPO37 / PCIERST2#	AE36
GND	Y19	GND	AP25	GNDA25DP1	V04	GPO38 / PCIERST3#	AD35
GND	Y21	GND	AP27	GNDA25DP1	W02	GPO39	AD36
GND	Y23	GND	AP34	GNDA25DP1	W04	GPO40	AD34
GND	Y24	GND	AP38	GNDA25DP1	W13	GPWAKE# / GPI1	AN32
GND	Y32	GND	AR21	GNDA25DP1	Y02	HA3#	D19
GND	Y36	GND	AR23	GNDA25DP1	Y04	HA4#	C21
GND	AA14	GND	AR25	GNDA25DP1	AA02	HA5#	B20
GND	AA16	GND	AR27	GNDA25DP1	AA03	HA6#	C18
GND	AA18	GND	AR29	GNDA25HCK	J16	HA7#	A21
GND	AA20	GND	AR30	GNDA25PEX	AF15	HA8#	B22
GND	AA22	GND	AT21	GNDA25PEX	AF17	HA9#	E21
GND	AB08	GND	AT22	GNDA25PEX	AF19	HA10#	A22
GND	AB15	GND	AT23	GNDA25PEX	AK02	HA11#	G22
GND	AB17	GND	AT24	GNDA25PEX	AK03	HA12#	E22
GND	AB19	GND	AT25	GNDA25PEX	AK04	HA13#	A20
GND	AB21	GND	AT26	GNDA25PEX	AK05	HA14#	B23
GND	AB23	GND	AT27	GNDA25PEX	AL04	HA15#	F22
GND	AB31	GND	AU21	GNDA25PEX	AL06	HA16#	C23
GND	AB34	GND	AU23	GNDA25PEX	AL15	HABI#	F20
GND	AC02	GND	AU26	GNDA25PEX	AM02	HADS#	G18
GND	AC14	GND	AU38	GNDA25PEX	AM03	HADSTB0N#	E20
GND	AC16	GND	AV21	GNDA25PEX	AM04	HADSTB0P#	D20
GND	AC18	GND	AV23	GNDA25PEX	AM05	HAHI0#	D23
GND	AC20	GND	AV26	GNDA25PEX	AM06	HAHI1#	F23
GND	AC22	GND	AV32	GNDA25PEX	AN04	HALF#	G19
GND	AC24	GNDA12DP1	Y11	GNDA25PEX	AN05	HBNR#	F15
GND	AC26	GNDA12DP1	Y12	GNDA25PEX	AN06	HBPRI#	D16
GND	AC38	GNDA12DP1	Y13	GNDA25PEX	AN07	HBREQ0#	G21
GND	AD06	GNDA12PEX	AD17	GNDA25PEX	AN08	HCLK-	J18
GND	AD25	GNDA12PEX	AD19	GNDA25PEX	AN09	HCLK+	J17
GND	AE04	GNDA12PEX	AL01	GNDA25PEX	AN10	HD0#	H13
GND	AE31	GNDA12PEX	AM07	GNDA25PEX	AP04	HD1#	E10
GND	AE34	GNDA12PEX	AM08	GNDA25PEX	AP06	HD2#	D12
GND	AE38	GNDA12PEX	AM09	GNDA25PEX	AP09	HD3#	D13
GND	AF03	GNDA12PEX	AM10	GNDA25PEX	AP11	HD4#	E12
GND	AF08	GNDA12PEX	AM11	GNDA25PEX	AP12	HD5#	F08
GND	AG06	GNDA12PEX	AM12	GNDA25PEX	AP13	HD6#	E13
GND	AG09	GNDA12PEX	AM13	GNDA25PEX	AP14	HD7#	F12
GND	AH04	GNDA12PEX	AM14	GNDA25PEX	AP15	HD8#	G13
GND	AH07	GNDA12PEX	AN11	GNDA25PEX	AR02	HD9#	F11
GND	AH31	GNDA12PEX	AN12	GNDA25PEX	AR03	HD10#	E09
GND	AH34	GNDA12PEX	AN13	GNDA25PEX	AR06	HD11#	D09
GND	AH38	GNDA12PEX	AN14	GNDA25PEX	AR09	HD12#	G09
GND	AJ06	GNDA12PEX	AP01	GNDA25PEX	AR12	HD13#	C11
GND	AK21	GNDA12PEX	AU01	GNDA25PEX	AR14	HD14#	H12
GND	AK22	GNDA12PEX	AU02	GNDA25PEX	AR16	HD15#	F10
GND	AK23	GNDA12PEX	AU03	GNDA25PEX	AT07	HD16#	B10
GND	AK24	GNDA12PEX	AU04	GNDA25PEX	AT10	HD17#	A10
GND	AK25	GNDA12PEX	AU05	GNDA25PEX	AT12	HD18#	A06
GND	AK26	GNDA12PEX	AU06	GNDA25PEX	AT14	HD19#	A05
GND	AL21	GNDA12PEX	AU07	GNDA25PEX	AT16	HD20#	C10
GND	AL23	GNDA12PEX	AU08	GNDA25SATA	AG21	HD21#	D11
GND	AL25	GNDA12PEX	AU09	GNDA25SATA	AM18	HD22#	B11
GND	AL27	GNDA12PEX	AU10	GNDA25SATA	AN18	HD23#	A09
GND	AL34	GNDA12PEX	AU12	GNDA25SATA	AN19	HD24#	B07
GND	AL38	GNDA12PEX	AU15	GNDA25SATA	AN20	HD25#	D08
GND	AM21	GNDA12PEX	AV06	GNDA25SATA	AP17	HD26#	A08
GND	AM23	GNDA12PEX	AV12	GNDA25SATA	AP19	HD27#	C06
GND	AM25	GNDA12PEX	AV15	GNDA25SATA	AR17	HD28#	A04
GND	AM27	GNDA12SATA	AF21	GNDA25SATA	AR19	HD29#	C09
GND	AM30	GNDA12SATA	AL20	GNDA25SATA	AT17	HD30#	B06

Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #
HD31#	E08	INTR	A16	MD5	W36	MDQS1+	R36
HD32#	G05	INTRUDER# / GPI6	AR31	MD6	V34	MDQS2-	R33
HD33#	F06	IRDY# / DSR2	AL37	MD7	V33	MDQS2+	P33
HD34#	B03	KBCK / GPIO5 / A20GATE	AV31	MD8	T38	MDQS3-	L33
HD35#	B04	KBDT / GPIO4 / KBC_CPURST#	AU31	MD9	T37	MDQS3+	M33
HD36#	A02	LID# / GPI7	AR34	MD10	U34	MDQS4-	D32
HD37#	H09	LPCAD0	AA35	MD11	U32	MDQS4+	D31
HD38#	F07	LPCAD1	Y35	MD12	U36	MDQS5-	G29
HD39#	H08	LPCAD2	Y38	MD13	U38	MDQS5+	H29
HD40#	H05	LPCAD3	Y37	MD14	U35	MDQS6-	B28
HD41#	E05	LPCDRQ0#	W37	MD15	T34	MDQS6+	A28
HD42#	G06	LPCDRQ1#	AA37	MD16	P37	MDQS7-	A24
HD43#	C03	LPCFRAME#	AA38	MD17	P38	MDQS7+	B24
HD44#	E06	LVDSCLK-	N02	MD18	N38	MEMCOMP	G33
HD45#	H07	LVDSCLK+	N01	MD19	R31	MEMDET	H33
HD46#	G07	LVDSD0-	R03	MD20	T33	MEMPWROK	K36
HD47#	D05	LVDSD0+	R02	MD21	R35	MEMRESET#	H32
HD48#	B02	LVDSD1-	R04	MD22	P32	MEMVREF	H31
HD49#	E02	LVDSD1+	P04	MD23	R32	MODT0	D33
HD50#	C02	LVDSD2-	P01	MD24	M38	MODT1	F32
HD51#	H01	LVDSD2+	P02	MD25	M35	MODT2	B34
HD52#	E01	LVDSD3-	M02	MD26	L32	MODT3	J32
HD53#	C01	LVDSD3+	M03	MD27	M31	MSCAS#	C34
HD54#	D01	LVDSENBL	AB06	MD28	N34	MSCK / GPIO3	AV30
HD55#	G01	LVDSENVDD	AB07	MD29	M37	MSDT / GPIO2	AT30
HD56#	F02	LVDSPWM	AA07	MD30	N32	MSPICLK / GPIO6	AC36
HD57#	D03	MA0	E38	MD31	N31	MSPIDI / GPI0	AC37
HD58#	J01	MA1	F34	MD32	E30	MSPIDO / GPO1	AC35
HD59#	J03	MA2	F35	MD33	E32	MSPISS0# / GPO3	AD38
HD60#	J04	MA3	G34	MD34	A32	MSPISS1# / GPO2	AD37
HD61#	H04	MA4	G35	MD35	C30	MSRAS#	A37
HD62#	H03	MA5	K34	MD36	G30	MSWE#	E34
HD63#	F04	MA6	G37	MD37	F30	NAP#	A12
HDBI0#	G10	MA7	J34	MD38	C31	NMI	B15
HDBI1#	B08	MA8	H35	MD39	B31	PAR / DTR3	AJ36
HDBI2#	C05	MA9	H36	MD40	A30	PCICLK	AA33
HDBI3#	G02	MA10	E37	MD41	C29	PCIRST#	AL31
HDBSY#	E17	MA11	J35	MD42	D28	PERR#	AB32
HDEFER#	C17	MA12	J38	MD43	H27	PEXCLK-	AM15
HDMI_CEC	AC30	MA13	C33	MD44	D29	PEXCLK+	AN15
HDMIRSPC	AB01	MA14	H37	MD45	B30	PEXREXTP0	AU16
HDMIRSPD	AB02	MA15	K37	MD46	G27	PEXRX0-	AN03
HDPWR#	B12	MBA0	B36	MD47	F27	PEXRX0+	AN02
HDRDY#	F16	MBA1	D36	MD48	D27	PEXRX1-	AP02
HDSTB0N#	H11	MBA2	K38	MD49	B27	PEXRX1+	AP03
HDSTB0P#	G11	MCKE0	J36	MD50	F26	PEXRX2-	AT02
HDSTB1N#	C07	MCKE1	L37	MD51	G26	PEXRX2+	AT03
HDSTB1P#	D07	MCKE2	L35	MD52	E26	PEXRX3-	AT04
HDSTB2N#	E04	MCKE3	L36	MD53	C27	PEXRX3+	AR04
HDSTB2P#	D04	MCLKO0-	C37	MD54	B26	PEXRX4-	AP05
HDSTB3N#	G03	MCLKO0+	D37	MD55	A26	PEXRX4+	AR05
HDSTB3P#	F03	MCLKO1-	E36	MD56	D24	PEXRX5-	AR07
HGTLPVT_REXT	H17	MCLKO1+	F36	MD57	C25	PEXRX5+	AP07
HGTLVREF0	J20	MCLKO2-	A33	MD58	H24	PEXRX6-	AP08
HGTLVREF1	J13	MCLKO2+	A34	MD59	H23	PEXRX6+	AR08
HHIT#	G17	MCLKO3-	B38	MD60	H25	PEXRX7-	AR10
HHITM#	E16	MCLKO3+	C38	MD61	G25	PEXRX7+	AP10
HLOCK#	D15	MCLKO4-	F38	MD62	E24	PEXRX8-	AU11
HREQ0#	F18	MCLKO4+	G38	MD63	G23	PEXRX8+	AV11
HREQ1#	E18	MCLKO5-	B35	MDQM0	V38	PEXRX9-	AR13
HREQ2#	B18	MCLKO5+	C35	MDQM1	T35	PEXRX9+	AT13
HRS0#	G15	MCS0#	D35	MDQM2	P36	PEXRX10-	AT15
HRS1#	H16	MCS1#	K33	MDQM3	M34	PEXRX10+	AR15
HTRDY#	D17	MCS2#	A36	MDQM4	E29	PEXTX0- / DP2TX3-	AM01
IGNNE#	A17	MCS3#	E33	MDQM5	A29	PEXTX0+ / DP2TX3+	AN01
INIT#	B14	MD0	W33	MDQM6	C26	PEXTX1- / DP2TX2-	AT01
INTA# / DCD3	AG31	MD1	W35	MDQM7	A25	PEXTX1+ / DP2TX2+	AR01
INTB# / GPIO8	AB33	MD2	V32	MDQS0-	V37	PEXTX2- / DP2TX1-	AV03
INTC# / GPIO9	AA31	MD3	U31	MDQS0+	V36	PEXTX2+ / DP2TX1+	AV02
INTD# / GPIO12	Y34	MD4	W32	MDQS1-	R37	PEXTX3- / DP2TX0-	AV05

Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #
PEXTX3+ / DP2TX0+	AV04	USBDREXT	AJ24	VCCA25PEX	AK08	VSUSA33USBH	AE22
PEXTX4-	AT06	USBHOC0#	AV28	VCCA25PEX	AK09	VSUSA33USBH	AG22
PEXTX4+	AT05	USBHOC1#	AV27	VCCA25PEX	AL07	VSUSA33USBH	AH22
PEXTX5-	AV08	USBHOC2#	AT29	VCCA25PEX	AL08	VSUSA33USBH	AJ21
PEXTX5+	AV07	USBHOC3#	AR28	VCCA25PEX	AL09	VSUSAVDDUSBH	AE23
PEXTX6-	AT09	USBHOC4#	AU27	VCCA25PEX	AL10	VSUSIOMEM	N21
PEXTX6+	AT08	USBHOC5#	AT28	VCCA25PLLDISP	T15	VSUSIOMEM	N23
PEXTX7-	AV10	USBHOC6#	AU29	VCCA25PLLDISP	U15	VSUSIOMEM	N25
PEXTX7+	AV09	USBHOC7#	AU28	VCCA25PLLLVDS	U12	VSUSIOMEM	P22
PEXTX8-	AT11	USBHP0-	AU24	VCCA25SATA	AE21	VSUSIOMEM	P24
PEXTX8+	AR11	USBHP0+	AV24	VCCA25SATA	AL18	VSUSIOMEM	P26
PEXTX9-	AV13	USBHP1-	AR24	VCCA33USBD	AE24	VSUSIOMEM	R21
PEXTX9+	AU13	USBHP1+	AP24	VCCA33USBD	AK27	VSUSIOMEM	R23
PEXTX10-	AV14	USBHP2-	AR26	VCCCR	AB25	VSUSIOMEM	R25
PEXTX10+	AU14	USBHP2+	AP26	VCPCLK / PTS0CLK / DSR1	AG07	VSUSIOMEM	T24
PEXWAKE# / GPI14	AM32	USBHP3-	AV22	VCPD0 / PTS0D0 / RI0	AG01	VSUSIOMEM	T26
PME# / GPIO7	AP33	USBHP3+	AU22	VCPD1 / PTS0D1 / DCD0	AG03	VSUSIOMEM	U25
PWRBTN#	AN33	USBHP4-	AR22	VCPD2 / PTS0D2 / SOUT0	AH03	VSUSIOMEM	V24
PWRGD	AP30	USBHP4+	AP22	VCPD3 / PTS0D3 / SIN0	AH01	VSUSIOMEM	V26
REQ0# / SIN3	AH33	USBHP5-	AM22	VCPD4 / PTS0D4 / DTR0	AH02	VSUSVDD	AB26
REQ1# / DSR3	AH32	USBHP5+	AL22	VCPD5 / PTS0D5 / DSR0	AJ03	VSUSVDD	AD26
RING# / GPI8	AV35	USBHP6-	AV25	VCPD6 / PTS0D6 / RTS0	AJ01	VSUSVDD	AE26
ROMSPC	AC03	USBHP6+	AU25	VCPD7 / PTS0D7 / CTS0	AJ02	VSUSVDDMEM	R30
ROMSPD	AC01	USBHP7-	AL24	VCPD8 / PTS0ERR / SIN1	AF05	VSUSVDDMEM	V29
RSMRST#	AN30	USBHP7+	AM24	VCPD9 / STS1VLD / SOUT1	AG04	VTT	N15
RSVD	AP35	USBHREXT	AJ22	VCPD10 / STS1SYNC / DCD1	AG05	VTT	N17
RTCXI	AU30	VBAT	AP31	VCPD11 / STS1CLK / RI1	AJ04	VTT	N19
RTCXO	AV29	VCC33	W24	VCPD12 / STS1ERR	AH05	VTT	P14
SATACLK+	AM20	VCC33	W25	VCPD13	AJ05	VTT	P16
SATAREXTP	AN17	VCC33	W26	VCPD14	AH06	VTT	P18
SERIRQ	W31	VCC33	Y25	VCPD15 / STS1D / DTR1	AG08	VTT	P20
SERR# / RI3	AJ32	VCC33	Y26	VCPHS / PTS0VLD / CTS1	AF02	VTT	R15
SLP#	A13	VCC33	AA24	VCPVS / PTS0SYNC / RTS1	AG02	VTT	R17
SMBALRT#	AU34	VCC33	AA25	VDD	T16	VTT	R19
SMBCK1	AT34	VCC33	AB24	VDD	T18	XD_ALE	AT38
SMBCK2 / GPIO1	AT33	VCC33VGA	AA15	VDD	T20	XD_CD#	AV36
SMBDT1	AR33	VCC33VGA	AB14	VDD	T22	XD_CE#	AR35
SMBDT2 / GPIO0	AU33	VCC33VGA	AC15	VDD	U17	XD_CLE	AV37
SMI#	C14	VCC33VGA	AD14	VDD	U19	XD_RE#	AU36
SPKR / GPO0	Y31	VCC33VGA	AE14	VDD	U21		
SRX0-	AR20	VCCA12DP1	Y14	VDD	U23		
SRX0+	AP20	VCCA12DP1	Y15	VDD	V16		
SRX1-	AR18	VCCA12PEX	AD15	VDD	V18		
SRX1+	AP18	VCCA12PEX	AD16	VDD	V20		
STOP# / DTR2	AK34	VCCA12PEX	AD18	VDD	V22		
STPCLK#	A14	VCCA12PEX	AD20	VDD	W17		
STX0-	AV20	VCCA12PEX	AL11	VDD	W19		
STX0+	AU20	VCCA12PEX	AL12	VDD	W21		
STX1-	AV18	VCCA12PEX	AL13	VDD	W23		
STX1+	AU18	VCCA12PEX	AL14	VDD	Y16		
SUSA# / SLOWCLK / GPO7	AL33	VCCA12SATA	AD21	VDD	Y18		
SUSB# / GPO8	AM31	VCCA12SATA	AL19	VDD	Y20		
SUSC# / GPO9	AM33	VCCA12USBD	AF24	VDD	Y22		
TESTEN	J19	VCCA25DAC	L04	VDD	AA17		
THRM# / GPI9	AB36	VCCA25DAC	L05	VDD	AA19		
THRMTRIP#	C13	VCCA25DAC	T13	VDD	AA21		
TP	AN31	VCCA25DP1	W14	VDD	AA23		
TP0	H19	VCCA25DP1	W15	VDD	AB16		
TP1	H20	VCCA25HCK	K16	VDD	AB18		
TP2	K18	VCCA25LVDS	U13	VDD	AB20		
TP3	AB30	VCCA25LVDS	U14	VDD	AB22		
TP4	W30	VCCA25LVDS	V14	VDD	AC17		
TP5	W07	VCCA25PEX	AE15	VDD	AC19		
TP6	AL30	VCCA25PEX	AE16	VDD	AC21		
TRDY# / RTS2	AK35	VCCA25PEX	AE17	VDD	AC23		
USBCLK	AA34	VCCA25PEX	AE18	VGPIO	AF04		
USBD_DET#	AP32	VCCA25PEX	AE19	VRDSLP	Y30		
USBD_PDN / GPO10	AR32	VCCA25PEX	AE20	VSUS33	AC25		
USBDP-	AM26	VCCA25PEX	AK06	VSUS33	AD24		
USBDP+	AL26	VCCA25PEX	AK07	VSUSA33USBH	AD23		

Table 3. VX900 Signal Ball List (Listed by Ball Number)

Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name
A02	HD36#	B36	MBA0	D34	GND	F34	MA1
A03	GND	B37	GND	D35	MCS0#	F35	MA2
A04	HD28#	B38	MCLKO3-	D36	MBA1	F36	MCLKO1+
A05	HD19#	**C01**	HD53#	D37	MCLKO0+	F37	GND
A06	HD18#	C02	HD50#	D38	GND	F38	MCLKO4-
A07	GND	C03	HD43#	**E01**	HD52#	**G01**	HD55#
A08	HD26#	C04	GND	E02	HD49#	G02	HDBI3#
A09	HD23#	C05	HDBI2#	E03	GND	G03	HDSTB3N#
A10	HD17#	C06	HD27#	E04	HDSTB2N#	G04	GND
A11	GND	C07	HDSTB1N#	E05	HD41#	G05	HD32#
A12	NAP#	C08	GND	E06	HD44#	G06	HD42#
A13	SLP#	C09	HD29#	E07	GND	G07	HD46#
A14	STPCLK#	C10	HD20#	E08	HD31#	G08	GND
A15	GND	C11	HD13#	E09	HD10#	G09	HD12#
A16	INTR	C12	GND	E10	HD1#	G10	HDBI0#
A17	IGNNE#	C13	THRMTRIP#	E11	GND	G11	HDSTB0P#
A18	DFTEN	C14	SMI#	E12	HD4#	G12	GND
A19	GND	C15	A20M#	E13	HD6#	G13	HD8#
A20	HA13#	C16	GND	E14	DPSLP#	G15	HRS0#
A21	HA7#	C17	HDEFER#	E15	GND	G16	GND
A22	HA10#	C18	HA6#	E16	HHITM#	G17	HHIT#
A23	GND	C20	GND	E17	HDBSY#	G18	HADS#
A24	MDQS7-	C21	HA4#	E18	HREQ1#	G19	HALF#
A25	MDQM7	C23	HA16#	E19	GND	G20	GND
A26	MD55	C24	GND	E20	HADSTB0N#	G21	HBREQ0#
A27	GND	C25	MD57	E21	HA9#	G22	HA11#
A28	MDQS6+	C26	MDQM6	E22	HA12#	G23	MD63
A29	MDQM5	C27	MD53	E23	GND	G24	GND
A30	MD40	C28	GND	E24	MD62	G25	MD61
A31	GND	C29	MD41	E26	MD52	G26	MD51
A32	MD34	C30	MD35	E27	GND	G27	MD46
A33	MCLKO2-	C31	MD38	E29	MDQM4	G28	GND
A34	MCLKO2+	C32	GND	E30	MD32	G29	MDQS5-
A35	GND	C33	MA13	E31	GND	G30	MD36
A36	MCS2#	C34	MSCAS#	E32	MD33	G32	GND
A37	MSRAS#	C35	MCLKO5+	E33	MCS3#	G33	MEMCOMP
B01	GND	C36	GND	E34	MSWE#	G34	MA3
B02	HD48#	C37	MCLKO0-	E35	GND	G35	MA4
B03	HD34#	C38	MCLKO3+	E36	MCLKO1-	G36	GND
B04	HD35#	**D01**	HD54#	E37	MA10	G37	MA6
B05	GND	D02	GND	E38	MA0	G38	MCLKO4+
B06	HD30#	D03	HD57#	**F01**	GND	**H01**	HD51#
B07	HD24#	D04	HDSTB2P#	F02	HD56#	H02	GND
B08	HDBI1#	D05	HD47#	F03	HDSTB3P#	H03	HD62#
B09	GND	D06	GND	F04	HD63#	H04	HD61#
B10	HD16#	D07	HDSTB1P#	F05	GND	H05	HD40#
B11	HD22#	D08	HD25#	F06	HD33#	H06	GND
B12	HDPWR#	D09	HD11#	F07	HD38#	H07	HD45#
B13	GND	D10	GND	F08	HD5#	H08	HD39#
B14	INIT#	D11	HD21#	F09	GND	H09	HD37#
B15	NMI	D12	HD2#	F10	HD15#	H10	GND
B16	FERR#	D13	HD3#	F11	HD9#	H11	HDSTB0N#
B17	GND	D14	GND	F12	HD7#	H12	HD14#
B18	HREQ2#	D15	HLOCK#	F13	GND	H13	HD0#
B19	BISTEN	D16	HBPRI#	F14	CPURST#	H14	GND
B20	HA5#	D17	HTRDY#	F15	HBNR#	H16	HRS1#
B21	GND	D18	GND	F16	HDRDY#	H17	HGTLPVT_REXT
B22	HA8#	D19	HA3#	F17	GND	H18	GND
B23	HA14#	D20	HADSTB0P#	F18	HREQ0#	H19	TP0
B24	MDQS7+	D22	GND	F20	HABI#	H20	TP1
B25	GND	D23	HAHI0#	F21	GND	H22	GND
B26	MD54	D24	MD56	F22	HA15#	H23	MD59
B27	MD49	D26	GND	F23	HAHI1#	H24	MD58
B28	MDQS6-	D27	MD48	F25	GND	H25	MD60
B29	GND	D28	MD42	F26	MD50	H26	GND
B30	MD45	D29	MD44	F27	MD47	H27	MD43
B31	MD39	D30	GND	F29	GND	H29	MDQS5+
B33	GND	D31	MDQS4+	F30	MD37	H30	GND
B34	MODT2	D32	MDQS4-	F32	MODT1	H31	MEMVREF
B35	MCLKO5-	D33	MODT0	F33	GND	H32	MEMRESET#

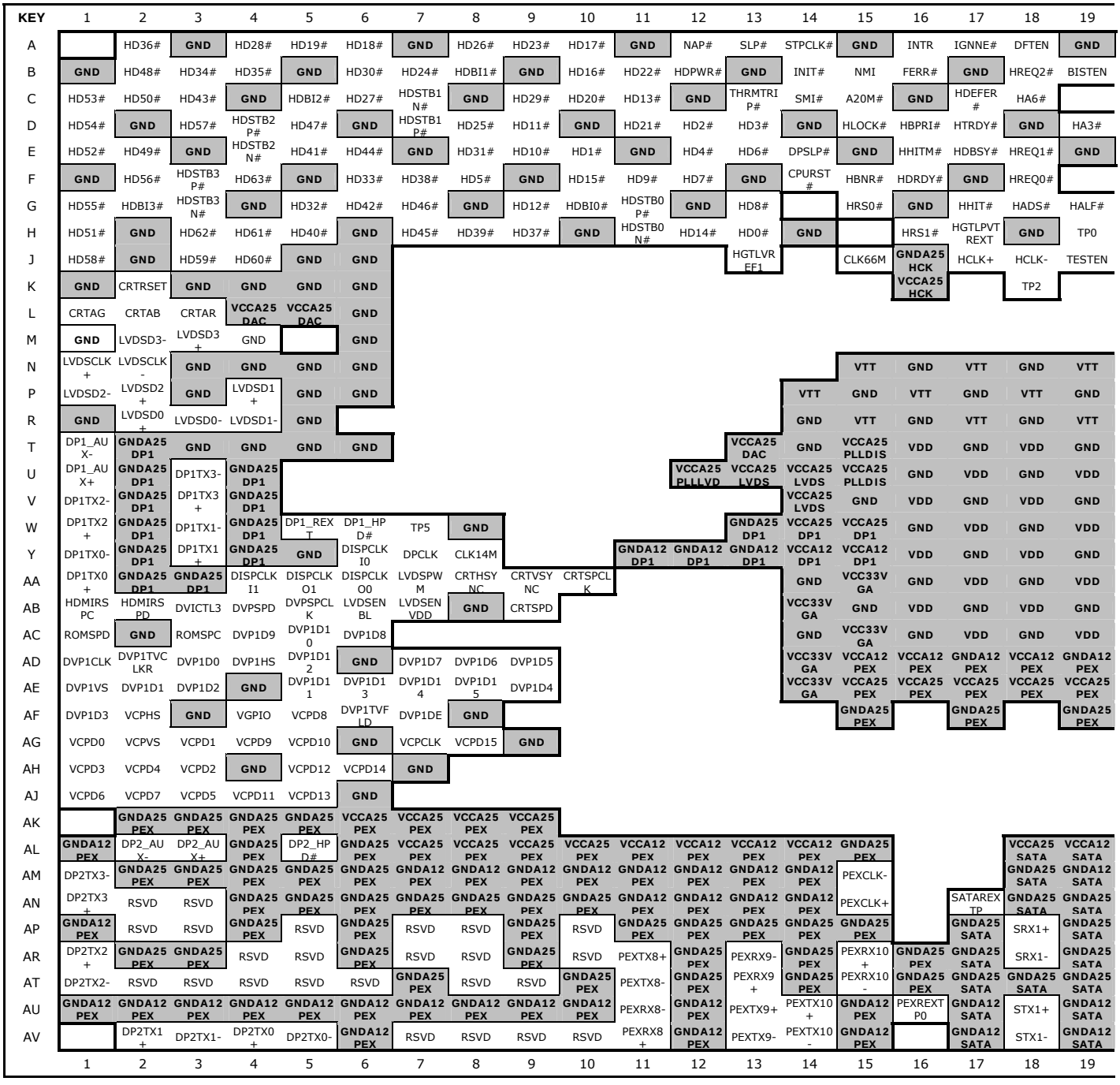
Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name
H33	MEMDET	N05	GND	R36	MDQS1+	V23	GND
H34	GND	N06	GND	R37	MDQS1-	V24	VSUSIOMEM
H35	MA8	N15	VTT	R38	GND	V25	GND
H36	MA9	N16	GND	**T01**	DP1_AUX-	V26	VSUSIOMEM
H37	MA14	N17	VTT	T02	GNDA25DP1	V29	VSUSVDDMEM
H38	GND	N18	GND	T03	GND	V31	GND
J01	HD58#	N19	VTT	T04	GND	V32	MD2
J02	GND	N20	GND	T05	GND	V33	MD7
J03	HD59#	N21	VSUSIOMEM	T06	GND	V34	MD6
J04	HD60#	N22	GND	T13	VCCA25DAC	V35	GND
J05	GND	N23	VSUSIOMEM	T14	GND	V36	MDQS0+
J06	GND	N24	GND	T15	VCCA25PLLDISP	V37	MDQS0-
J13	HGTLVREF1	N25	VSUSIOMEM	T16	VDD	V38	MDQM0
J15	CLK66M	N26	GND	T17	GND	**W01**	DP1TX2+ / HDMITX0+
J16	GNDA25HCK	N31	MD31	T18	VDD	W02	GNDA25DP1
J17	HCLK+	N32	MD30	T19	GND	W03	DP1TX1- / HDMITX1-
J18	HCLK-	N33	GND	T20	VDD	W04	GNDA25DP1
J19	TESTEN	N34	MD28	T21	GND	W05	DP1_REXT
J20	HGTLVREF0	N37	GND	T22	VDD	W06	DP1_HPD#
J32	MODT3	N38	MD18	T23	GND	W07	TP5
J33	GND	**P01**	LVDSD2-	T24	VSUSIOMEM	W08	GND
J34	MA7	P02	LVDSD2+	T25	GND	W13	GNDA25DP1
J35	MA11	P03	GND	T26	VSUSIOMEM	W14	VCCA25DP1
J36	MCKE0	P04	LVDSD1+	T32	GND	W15	VCCA25DP1
J37	GND	P05	GND	T33	MD20	W16	GND
J38	MA12	P06	GND	T34	MD15	W17	VDD
K01	GND	P14	VTT	T35	MDQM1	W18	GND
K02	CRTRSET	P15	GND	T36	GND	W19	VDD
K03	GND	P16	VTT	T37	MD9	W20	GND
K04	GND	P17	GND	T38	MD8	W21	VDD
K05	GND	P18	VTT	**U01**	DP1_AUX+	W22	GND
K06	GND	P19	GND	U02	GNDA25DP1	W23	VDD
K16	VCCA25HCK	P20	VTT	U03	DP1TX3- / HDMICLK-	W24	VCC33
K18	TP2	P21	GND	U04	GNDA25DP1	W25	VCC33
K33	MCS1#	P22	VSUSIOMEM	U12	VCCA25PLLLVDS	W26	VCC33
K34	MA5	P23	GND	U13	VCCA25LVDS	W30	TP4
K35	GND	P24	VSUSIOMEM	U14	VCCA25LVDS	W31	SERIRQ
K36	MEMPWROK	P25	GND	U15	VCCA25PLLDISP	W32	MD4
K37	MA15	P26	VSUSIOMEM	U16	GND	W33	MD0
K38	MBA2	P31	GND	U17	VDD	W34	GND
L01	CRTAG	P32	MD22	U18	GND	W35	MD1
L02	CRTAB	P33	MDQS2+	U19	VDD	W36	MD5
L03	CRTAR	P35	GND	U20	GND	W37	LPCDRQ0#
L04	VCCA25DAC	P36	MDQM2	U21	VDD	W38	GND
L05	VCCA25DAC	P37	MD16	U22	GND	**Y01**	DP1TX0- / HDMITX2-
L06	GND	P38	MD17	U23	VDD	Y02	GNDA25DP1
L32	MD26	**R01**	GND	U24	GND	Y03	DP1TX1+ / HDMITX1+
L33	MDQS3-	R02	LVDSD0+	U25	VSUSIOMEM	Y04	GNDA25DP1
L34	GND	R03	LVDSD0-	U26	GND	Y05	GND
L35	MCKE2	R04	LVDSD1-	U31	MD3	Y06	DISPCLKI0 / VGPI0
L36	MCKE3	R05	GND	U32	MD11	Y07	DPCLK
L37	MCKE1	R14	GND	U33	GND	Y08	CLK14M
L38	GND	R15	VTT	U34	MD10	Y11	GNDA12DP1
M01	GND	R16	GND	U35	MD14	Y12	GNDA12DP1
M02	LVDSD3-	R17	VTT	U36	MD12	Y13	GNDA12DP1
M03	LVDSD3+	R18	GND	U37	GND	Y14	VCCA12DP1
M04	GND	R19	VTT	U38	MD13	Y15	VCCA12DP1
M06	GND	R20	GND	**V01**	DP1TX2- / HDMITX0-	Y16	VDD
M31	MD27	R21	VSUSIOMEM	V02	GNDA25DP1	Y17	GND
M32	GND	R22	GND	V03	DP1TX3+ / HDMICLK+	Y18	VDD
M33	MDQS3+	R23	VSUSIOMEM	V04	GNDA25DP1	Y19	GND
M34	MDQM3	R24	GND	V14	VCCA25LVDS	Y20	VDD
M35	MD25	R25	VSUSIOMEM	V15	GND	Y21	GND
M36	GND	R26	GND	V16	VDD	Y22	VDD
M37	MD29	R30	VSUSVDDMEM	V17	GND	Y23	GND
M38	MD24	R31	MD19	V18	VDD	Y24	GND
N01	LVDSCLK+	R32	MD23	V19	GND	Y25	VCC33
N02	LVDSCLK-	R33	MDQS2-	V20	VDD	Y26	VCC33
N03	GND	R34	GND	V21	GND	Y30	VRDSLP
N04	GND	R35	MD21	V22	VDD	Y31	SPKR / GPO0

Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name
Y32	GND	AC04	DVP1D9 / DCD0	AE22	VSUSA33USBH	AJ06	GND
Y33	AZBITCLK	AC05	DVP1D10 / SOUT0	AE23	VSUSAVDDUSBH	AJ21	VSUSA33USBH
Y34	INTD# / GPIO12	AC06	DVP1D8 / RI0	AE24	VCCA33USBD	AJ22	USBHREXT
Y35	LPCAD1	AC14	GND	AE26	VSUSVDD	AJ24	USBDREXT
Y36	GND	AC15	VCC33VGA	AE31	GND	AJ31	GNT1# / RTS3
Y37	LPCAD3	AC16	GND	AE33	CBE0# / CTS3	AJ32	SERR# / RI3
Y38	LPCAD2	AC17	VDD	AE34	GND	AJ33	GNT0# / SOUT3
AA01	DP1TX0+ / HDMITX2+	AC18	GND	AE35	AD8	AJ34	AD31 / GPIO35
AA02	GNDA25DP1	AC19	VDD	AE36	GPO37 / PCIERST2#	AJ35	CBE1# / RI2
AA03	GNDA25DP1	AC20	GND	AE37	AD1 / GPI11	AJ36	PAR / DTR3
AA04	DISPCLKI1 / VGPI1	AC21	VDD	AE38	GND	AJ37	AD15 / GPIO19
AA05	DISPCLKO1 / VGPO1	AC22	GND	**AF01**	DVP1D3 / SIN1	**AK02**	GNDA25PEX
AA06	DISPCLKO0 / VGPO0	AC23	VDD	AF02	VCPHS / PTS0VLD / CTS1	AK03	GNDA25PEX
AA07	LVDSPWM	AC24	GND	AF03	GND	AK04	GNDA25PEX
AA08	CRTHSYNC	AC25	VSUS33	AF04	VGPIO	AK05	GNDA25PEX
AA09	CRTVSYNC	AC26	GND	AF05	VCPD8 / PTS0ERR / SIN1	AK06	VCCA25PEX
AA10	CRTSPCLK	AC30	HDMI_CEC	AF06	DVP1TVFLD	AK07	VCCA25PEX
AA14	GND	AC31	AD20 / GPIO24	AF07	DVP1DE	AK08	VCCA25PEX
AA15	VCC33VGA	AC32	AD7	AF08	GND	AK09	VCCA25PEX
AA16	GND	AC33	AD3	AF15	GNDA25PEX	AK21	GND
AA17	VDD	AC34	GPO36 / PCIERST1#	AF17	GNDA25PEX	AK22	GND
AA18	GND	AC35	MSPIDO / GPO1	AF19	GNDA25PEX	AK23	GND
AA19	VDD	AC36	MSPICLK / GPIO6	AF21	GNDA12SATA	AK24	GND
AA20	GND	AC37	MSPIDI / GPI0	AF24	VCCA12USBD	AK25	GND
AA21	VDD	AC38	GND	AF31	AD22 / GPIO26	AK26	GND
AA22	GND	**AD01**	DVP1CLK	AF32	CBE3# / SOUT2	AK27	VCCA33USBD
AA23	VDD	AD02	DVP1TVCLKR	AF33	AD28 / GPIO32	AK32	AD16 / GPIO20
AA24	VCC33	AD03	DVP1D0 / RI1	AF34	AD25 / GPIO29	AK33	CBE2# / DCD2
AA25	VCC33	AD04	DVP1HS	AF35	AD2	AK34	STOP# / DTR2
AA30	CPUSTP# / GPO5	AD05	DVP1D12 / DTR0	AF36	AD10 / GPIO14	AK35	TRDY# / RTS2
AA31	INTC# / GPIO9	AD06	GND	AF37	AD9 / GPIO13	AK36	DEVSEL# / SIN2
AA32	GPIO10 / SATALED0#	AD07	DVP1D7 / CTS1	AF38	AD4 / GPO4	**AL01**	GNDA12PEX
AA33	PCICLK	AD08	DVP1D6 / RTS1	**AG01**	VCPD0 / PTS0D0 / RI0	AL02	DP2_AUX-
AA34	USBCLK	AD09	DVP1D5 / DSR1	AG02	VCPVS / PTS0SYNC / RTS1	AL03	DP2_AUX+
AA35	LPCAD0	AD14	VCC33VGA	AG03	VCPD1 / PTS0D1 / DCD0	AL04	GNDA25PEX
AA36	AZSYNC	AD15	VCCA12PEX	AG04	VCPD9 / STS1VLD / SOUT1	AL05	DP2_HPD#
AA37	LPCDRQ1#	AD16	VCCA12PEX	AG05	VCPD10 / STS1SYNC / DCD1	AL06	GNDA25PEX
AA38	LPCFRAME#	AD17	GNDA12PEX	AG06	GND	AL07	VCCA25PEX
AB01	HDMIRSPC	AD18	VCCA12PEX	AG07	VCPCLK / PTS0CLK / DSR1	AL08	VCCA25PEX
AB02	HDMIRSPD	AD19	GNDA12PEX	AG08	VCPD15 / STS1D / DTR1	AL09	VCCA25PEX
AB03	DVICTL3	AD20	VCCA12PEX	AG09	GND	AL10	VCCA25PEX
AB04	DVPSPD	AD21	VCCA12SATA	AG21	GNDA25SATA	AL11	VCCA12PEX
AB05	DVPSPCLK	AD23	VSUSA33USBH	AG22	VSUSA33USBH	AL12	VCCA12PEX
AB06	LVDSENBL	AD24	VSUS33	AG31	INTA# / DCD3	AL13	VCCA12PEX
AB07	LVDSENVDD	AD25	GND	AG32	AD23 / GPIO27	AL14	VCCA12PEX
AB08	GND	AD26	VSUSVDD	AG33	AD30 / GPIO34	AL15	GNDA25PEX
AB09	CRTSPD	AD30	AD6	AG34	AD29 / GPIO33	AL18	VCCA25SATA
AB14	VCC33VGA	AD31	AD0 / GPI10	AG35	AD24 / GPIO28	AL19	VCCA12SATA
AB15	GND	AD32	AD5	AG36	AD27 / GPIO31	AL20	GNDA12SATA
AB16	VDD	AD33	AD21 / GPIO25	AG37	AD11 / GPIO15	AL21	GND
AB17	GND	AD34	GPO40	AG38	AD12 / GPIO16	AL22	USBHP5+
AB18	VDD	AD35	GPO38 / PCIERST3#	**AH01**	VCPD3 / PTS0D3 / SIN0	AL23	GND
AB19	GND	AD36	GPO39	AH02	VCPD4 / PTS0D4 / DTR0	AL24	USBHP7-
AB20	VDD	AD37	MSPISS1# / GPO2	AH03	VCPD2 / PTS0D2 / SOUT0	AL25	GND
AB21	GND	AD38	MSPISS0# / GPO3	AH04	GND	AL26	USBDP+
AB22	VDD	**AE01**	DVP1VS	AH05	VCPD12 / STS1ERR	AL27	GND
AB23	GND	AE02	DVP1D1 / DCD1	AH06	VCPD14	AL30	TP6
AB24	VCC33	AE03	DVP1D2 / SOUT1	AH07	GND	AL31	PCIRST#
AB25	VCCCR	AE04	GND	AH22	VSUSA33USBH	AL32	EXTSMI# / GPI5
AB26	VSUSVDD	AE05	DVP1D11 / SIN0	AH31	GND	AL33	SUSA# / SLOWCLK / GPO7
AB30	TP3	AE06	DVP1D13 / DSR0	AH32	REQ1# / DSR3	AL34	GND
AB31	GND	AE07	DVP1D14 / RTS0	AH33	REQ0# / SIN3	AL35	AD19 / GPIO23
AB32	PERR#	AE08	DVP1D15 / CTS0	AH34	GND	AL36	FRAME# / CTS2
AB33	INTB# / GPIO8	AE09	DVP1D4 / DTR1	AH35	AD26 / GPIO30	AL37	IRDY# / DSR2
AB34	GND	AE14	VCC33VGA	AH36	AD14 / GPIO18	AL38	GND
AB35	GPIO11 / SATALED1#	AE15	VCCA25PEX	AH37	AD13 / GPIO17	**AM01**	PEXTX0- / DP2TX3-
AB36	THRM# / GPI9	AE16	VCCA25PEX	AH38	GND	AM02	GNDA25PEX
AB37	C4PSTOP# / GPO6	AE17	VCCA25PEX	**AJ01**	VCPD6 / PTS0D6 / RTS0	AM03	GNDA25PEX
AB38	AZSDOUT	AE18	VCCA25PEX	AJ02	VCPD7 / PTS0D7 / CTS0	AM04	GNDA25PEX
AC01	ROMSPD	AE19	VCCA25PEX	AJ03	VCPD5 / PTS0D5 / DSR0	AM05	GNDA25PEX
AC02	GND	AE20	VCCA25PEX	AJ04	VCPD11 / STS1CLK / RI1	AM06	GNDA25PEX
AC03	ROMSPC	AE21	VCCA25SATA	AJ05	VCPD13	AM07	GNDA12PEX

Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name
AM08	GNDA12PEX	AP24	USBHP1+	AT31	AZSDIN1
AM09	GNDA12PEX	AP25	GND	AT32	AZSDIN0
AM10	GNDA12PEX	AP26	USBHP2+	AT33	SMBCK2 / GPIO1
AM11	GNDA12PEX	AP27	GND	AT34	SMBCK1
AM12	GNDA12PEX	AP30	PWRGD	AT35	CR_PWOFF / SDIOPWOFF / GPO12
AM13	GNDA12PEX	AP31	VBAT	AT36	CR_CD# / MMC_CD# / SD_CD# / SDIOCD#
AM14	GNDA12PEX	AP32	USBD_DET#	AT37	CR_D1 / MMC_D1 / XD_D1 / SD_D1 / SDIOD1
AM15	PEXCLK-	AP33	PME# / GPIO7	AT38	XD_ALE
AM18	GNDA25SATA	AP34	GND	**AU01**	GNDA12PEX
AM19	GNDA12SATA	AP35	RSVD	AU02	GNDA12PEX
AM20	SATACLK+	AP36	CR_D7 / MMC_D7 / XD_D7	AU03	GNDA12PEX
AM21	GND	AP37	CR_CLK / MMC_CLK / XD_WE# / SD_CLK / SDIOCLK	AU04	GNDA12PEX
AM22	USBHP5-	AP38	GND	AU05	GNDA12PEX
AM23	GND	**AR01**	PEXTX1+ / DP2TX2+	AU06	GNDA12PEX
AM24	USBHP7+	AR02	GNDA25PEX	AU07	GNDA12PEX
AM25	GND	AR03	GNDA25PEX	AU08	GNDA12PEX
AM26	USBDP-	AR04	PEXRX3+	AU09	GNDA12PEX
AM27	GND	AR05	PEXRX4+	AU10	GNDA12PEX
AM30	GND	AR06	GNDA25PEX	AU11	PEXRX8-
AM31	SUSB# / GPO8	AR07	PEXRX5-	AU12	GNDA12PEX
AM32	PEXWAKE# / GPI14	AR08	PEXRX6+	AU13	PEXTX9+
AM33	SUSC# / GPO9	AR09	GNDA25PEX	AU14	PEXTX10+
AM34	CR_CMD / MMC_CMD# / XD_RB# / SD_CMD / SDIOCMD	AR10	PEXRX7-	AU15	GNDA12PEX
AM35	CR_D3 / MMC_D3 / XD_D3 / SD_D3 / SDIOD3	AR11	PEXTX8+	AU16	PEXREXTP0
AM36	AD18 / GPIO22	AR12	GNDA25PEX	AU17	GNDA12SATA
AM37	AD17 / GPIO21	AR13	PEXRX9-	AU18	STX1+
AN01	PEXTX0+ / DP2TX3+	AR14	GNDA25PEX	AU19	GNDA12SATA
AN02	PEXRX0+	AR15	PEXRX10+	AU20	STX0+
AN03	PEXRX0-	AR16	GNDA25PEX	AU21	GND
AN04	GNDA25PEX	AR17	GNDA25SATA	AU22	USBHP3+
AN05	GNDA25PEX	AR18	SRX1-	AU23	GND
AN06	GNDA25PEX	AR19	GNDA25SATA	AU24	USBHP0-
AN07	GNDA25PEX	AR20	SRX0-	AU25	USBHP6+
AN08	GNDA25PEX	AR21	GND	AU26	GND
AN09	GNDA25PEX	AR22	USBHP4-	AU27	USBHOC4#
AN10	GNDA25PEX	AR23	GND	AU28	USBHOC7#
AN11	GNDA12PEX	AR24	USBHP1-	AU29	USBHOC6#
AN12	GNDA12PEX	AR25	GND	AU30	RTCXI
AN13	GNDA12PEX	AR26	USBHP2-	AU31	KBDT / GPIO4 / KBC_CPURST#
AN14	GNDA12PEX	AR27	GND	AU32	AZRST#
AN15	PEXCLK+	AR28	USBHOC3#	AU33	SMBDT2 / GPIO0
AN17	SATAREXTP	AR29	GND	AU34	SMBALRT#
AN18	GNDA25SATA	AR30	GND	AU35	CR_PWSEL / SDIOPWSEL / GPO11
AN19	GNDA25SATA	AR31	INTRUDER# / GPI6	AU36	XD_RE#
AN20	GNDA25SATA	AR32	USBD_PDN / GPO10	AU37	CR_WPD / XD_WP# / SD_WPD / SDIOWPD
AN21	GND	AR33	SMBDT1	AU38	GND
AN22	GND	AR34	LID# / GPI7	**AV02**	PEXTX2+ / DP2TX1+
AN23	GND	AR35	XD_CE#	AV03	PEXTX2- / DP2TX1-
AN24	GND	AR36	CR_D0 / MMC_D0 / XD_D0 / SD_D0 / SDIOD0	AV04	PEXTX3+ / DP2TX0+
AN25	GND	AR37	CR_D4 / MMC_D4 / XD_D4	AV05	PEXTX3- / DP2TX0-
AN26	GND	AR38	CR_D6 / MMC_D6 / XD_D6	AV06	GNDA12PEX
AN27	GND	**AT01**	PEXTX1- / DP2TX2-	AV07	PEXTX5+
AN30	RSMRST#	AT02	PEXRX2-	AV08	PEXTX5-
AN31	TP	AT03	PEXRX2+	AV09	PEXTX7+
AN32	GPWAKE# / GPI1	AT04	PEXRX3-	AV10	PEXTX7-
AN33	PWRBTN#	AT05	PEXTX4+	AV11	PEXRX8+
AN34	BATLOW# / GPI4	AT06	PEXTX4-	AV12	GNDA12PEX
AN35	CR_D5 / MMC_D5 / XD_D5	AT07	GNDA25PEX	AV13	PEXTX9-
AN36	CR_D2 / MMC_D2 / XD_D2 / SD_D2 / SDIOD2	AT08	PEXTX6+	AV14	PEXTX10-
AP01	GNDA12PEX	AT09	PEXTX6-	AV15	GNDA12PEX
AP02	PEXRX1-	AT10	GNDA25PEX	AV17	GNDA12SATA
AP03	PEXRX1+	AT11	PEXTX8-	AV18	STX1-
AP04	GNDA25PEX	AT12	GNDA25PEX	AV19	GNDA12SATA
AP05	PEXRX4-	AT13	PEXRX9+	AV20	STX0-
AP06	GNDA25PEX	AT14	GNDA25PEX	AV21	GND
AP07	PEXRX5+	AT15	PEXRX10-	AV22	USBHP3-
AP08	PEXRX6-	AT16	GNDA25PEX	AV23	GND
AP09	GNDA25PEX	AT17	GNDA25SATA	AV24	USBHP0+
AP10	PEXRX7+	AT18	GNDA25SATA	AV25	USBHP6-
AP11	GNDA25PEX	AT19	GNDA25SATA	AV26	GND
AP12	GNDA25PEX	AT20	GNDA25SATA	AV27	USBHOC1#
AP13	GNDA25PEX	AT21	GND	AV28	USBHOC0#
AP14	GNDA25PEX	AT22	GND	AV29	RTCXO
AP15	GNDA25PEX	AT23	GND	AV30	MSCK / GPIO3
AP17	GNDA25SATA	AT24	GND	AV31	KBCK / GPIO5 / A20GATE
AP18	SRX1+	AT25	GND	AV32	GND
AP19	GNDA25SATA	AT26	GND	AV35	RING# / GPI8
AP20	SRX0+	AT27	GND	AV36	XD_CD#
AP21	GND	AT28	USBHOC5#	AV37	XD_CLE
AP22	USBHP4+	AT29	USBHOC2#		
AP23	GND	AT30	MSDT / GPIO2		

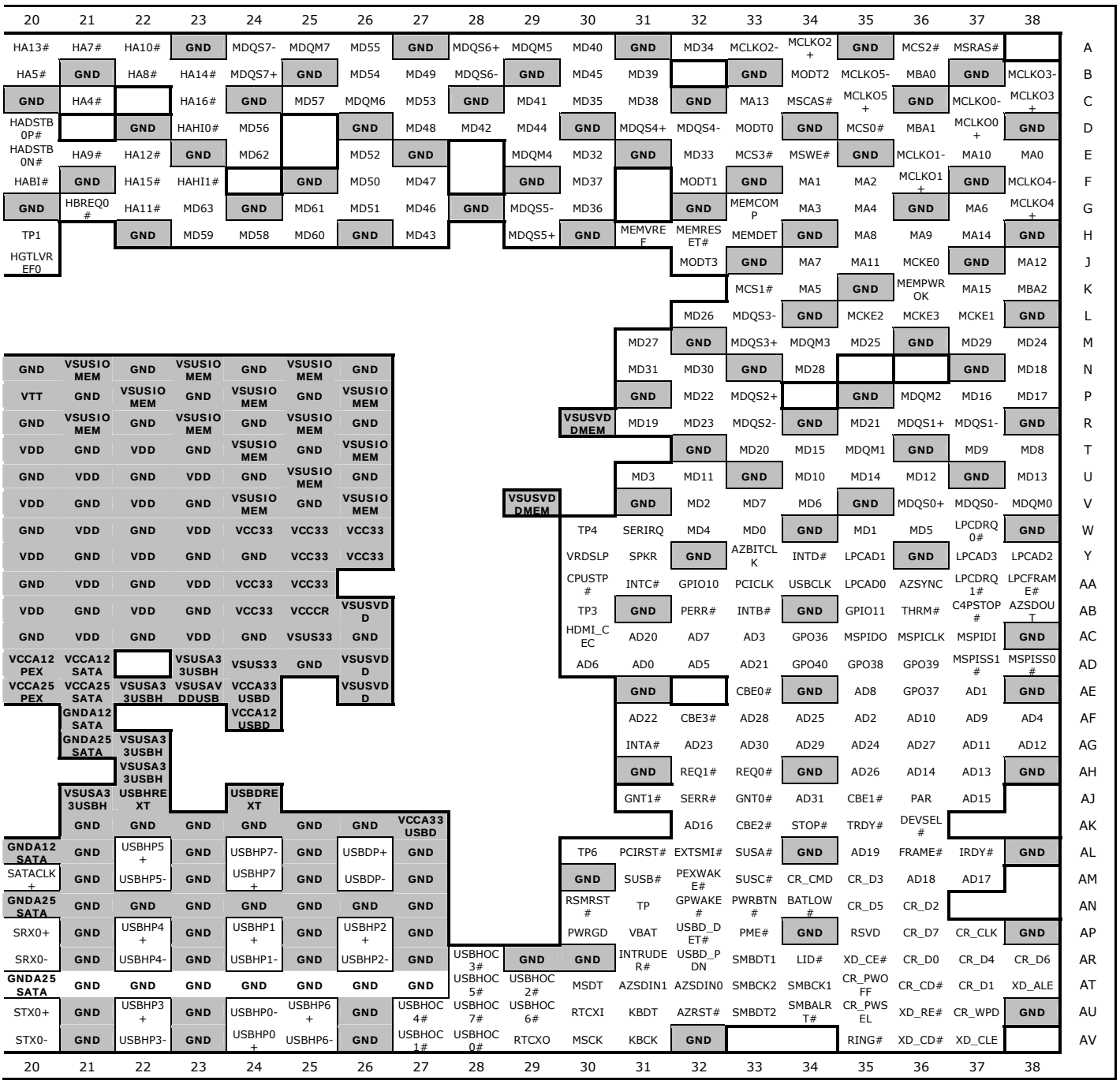
VX900M Ball Map

Figure 3. VX900M Ball Map – Left Side Top View



KEY	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
A		HD36#	GND	HD28#	HD19#	HD18#	GND	HD26#	HD23#	HD17#	GND	NAP#	SLP#	STPCLK#	GND	INTR	IGNNE#	DFTEN	GND
B	GND	HD48#	HD34#	HD35#	GND	HD30#	HD24#	HDBI1#	GND	HD16#	HD22#	HDPWR#	GND	INIT#	NMI	FERR#	GND	HREQ2#	BISTEN
C	HD53#	HD50#	HD43#	GND	HDBI2#	HD27#	HDSTB1N#	GND	HD29#	HD20#	HD13#	GND	THRMTRIP#	SMI#	A20M#	GND	HDEFER#	HA6#	
D	HD54#	GND	HD57#	HDSTB2P#	HD47#	GND	HDSTB1P#	HD25#	HD11#	GND	HD21#	HD2#	HD3#	GND	HLOCK#	HBPRI#	HTRDY#	GND	HA3#
E	HD52#	HD49#	GND	HDSTB2N#	HD41#	HD44#	GND	HD31#	HD10#	HD1#	GND	HD4#	HD6#	DPSLP#	GND	HHITM#	HDBSY#	HREQ1#	GND
F	GND	HD56#	HDSTB3P#	HD63#	GND	HD33#	HD38#	HD5#	GND	HD15#	HD9#	HD7#	GND	CPURST#	HBNR#	HDRDY#	GND	HREQ0#	
G	HD55#	HDBI3#	HDSTB3N#	GND	HD32#	HD42#	HD46#	GND	HD12#	HDBI0#	HDSTB0P#	GND	HD8#		HRS0#	GND	HHIT#	HADS#	HALF#
H	HD51#	GND	HD62#	HD61#	HD40#	GND	HD45#	HD39#	HD37#	GND	HDSTB0N#	HD14#	HD0#	GND		HRS1#	HGTLPVTREXT	GND	TP0
J	HD58#	GND	HD59#	HD60#	GND	GND							HGTLVREF1		CLK66M	GNDA25HCK	HCLK+	HCLK-	TESTEN
K	GND	CRTRSET	GND	GND	GND	GND										VCCA25HCK		TP2	
L	CRTAG	CRTAB	CRTAR	VCCA25DAC	VCCA25DAC	GND													
M	GND	LVDSD3-	LVDSD3+	GND		GND													
N	LVDSCLK+	LVDSCLK-	GND	GND	GND	GND									VTT	GND	VTT	GND	VTT
P	LVDSD2-	LVDSD2+	GND	LVDSD1+	GND	GND								VTT	GND	VTT	GND	VTT	GND
R	GND	LVDSD0+	LVDSD0-	LVDSD1-	GND									GND	VTT	GND	VTT	GND	VTT
T	DP1_AUX-	GNDA25DP1	GND	GND	GND	GND							VCCA25DAC	GND	VCCA25PLLDIS	VDD	GND	VDD	GND
U	DP1_AUX+	GNDA25DP1	DP1TX3-	GNDA25DP1								VCCA25PLLLVD	VCCA25LVDS	VCCA25LVDS	VCCA25PLLDIS	GND	VDD	GND	VDD
V	DP1TX2-	GNDA25DP1	DP1TX3+	GNDA25DP1										VCCA25LVDS	GND	VDD	GND	VDD	GND
W	DP1TX2+	GNDA25DP1	DP1TX1-	GNDA25DP1	DP1_REXT	DP1_HPD#	TP5	GND					GNDA25DP1	VCCA25DP1	VCCA25DP1	GND	VDD	GND	VDD
Y	DP1TX0-	GNDA25DP1	DP1TX1+	GNDA25DP1	GND	DISPCLKI0	DPCLK	CLK14M			GNDA12DP1	GNDA12DP1	GNDA12DP1	VCCA12DP1	VCCA12DP1	VDD	GND	VDD	GND
AA	DP1TX0+	GNDA25DP1	GNDA25DP1	DISPCLKI1	DISPCLKO1	DISPCLKO0	LVDSPWM	CRTHSYNC	CRTVSYNC	CRTSPCLK				GND	VCC33VGA	GND	VDD	GND	VDD
AB	HDMIRSPC	HDMIRSPD	DVICTL3	DVPSPD	DVPSPCLK	LVDSENBL	LVDSENVDD	GND	CRTSPD					VCC33VGA	GND	VDD	GND	VDD	GND
AC	ROMSPD	GND	ROMSPC	DVP1D9	DVP1D10	DVP1D8								GND	VCC33VGA	GND	VDD	GND	VDD
AD	DVP1CLK	DVP1TVCLKR	DVP1D0	DVP1HS	DVP1D12	GND	DVP1D7	DVP1D6	DVP1D5					VCC33VGA	VCCA12PEX	VCCA12PEX	GNDA12PEX	VCCA12PEX	GNDA12PEX
AE	DVP1VS	DVP1D1	DVP1D2	GND	DVP1D11	DVP1D13	DVP1D14	DVP1D15	DVP1D4					VCC33VGA	VCCA25PEX	VCCA25PEX	VCCA25PEX	VCCA25PEX	VCCA25PEX
AF	DVP1D3	VCPHS	GND	VGPIO	VCPD8	DVP1TVFLD	DVP1DE	GND							GNDA25PEX		GNDA25PEX		GNDA25PEX
AG	VCPD0	VCPVS	VCPD1	VCPD9	VCPD10	GND	VCPCLK	VCPD15	GND										
AH	VCPD3	VCPD4	VCPD2	GND	VCPD12	VCPD14	GND												
AJ	VCPD6	VCPD7	VCPD5	VCPD11	VCPD13	GND													
AK		GNDA25PEX	GNDA25PEX	GNDA25PEX	GNDA25PEX	VCCA25PEX	VCCA25PEX	VCCA25PEX	VCCA25PEX										
AL	GNDA12PEX	DP2_AUX-	DP2_AUX+	GNDA25PEX	DP2_HPD#	GNDA25PEX	VCCA25PEX	VCCA25PEX	VCCA25PEX	VCCA25PEX	VCCA12PEX	VCCA12PEX	VCCA12PEX	VCCA12PEX	GNDA25PEX			VCCA25SATA	VCCA12SATA
AM	DP2TX3-	GNDA25PEX	GNDA25PEX	GNDA25PEX	GNDA25PEX	GNDA25PEX	GNDA12PEX	GNDA12PEX	GNDA12PEX	GNDA12PEX	GNDA12PEX	GNDA12PEX	GNDA12PEX	GNDA12PEX	PEXCLK-			GNDA25SATA	GNDA12SATA
AN	DP2TX3+	RSVD	RSVD	GNDA25PEX	GNDA25PEX	GNDA25PEX	GNDA25PEX	GNDA25PEX	GNDA25PEX	GNDA25PEX	GNDA12PEX	GNDA12PEX	GNDA12PEX	GNDA12PEX	PEXCLK+		SATAREXTP	GNDA25SATA	GNDA25SATA
AP	GNDA12PEX	RSVD	RSVD	GNDA25PEX	RSVD	GNDA25PEX	RSVD	RSVD	GNDA25PEX	RSVD	GNDA25PEX	GNDA25PEX	GNDA25PEX	GNDA25PEX	GNDA25PEX		GNDA25SATA	SRX1+	GNDA25SATA
AR	DP2TX2+	GNDA25PEX	GNDA25PEX	RSVD	RSVD	GNDA25PEX	RSVD	RSVD	GNDA25PEX	RSVD	PEXTX8+	GNDA25PEX	PEXRX9-	GNDA25PEX	PEXRX10+	GNDA25PEX	GNDA25SATA	SRX1-	GNDA25SATA
AT	DP2TX2-	RSVD	RSVD	RSVD	RSVD	RSVD	GNDA25PEX	RSVD	RSVD	GNDA25PEX	PEXTX8-	GNDA25PEX	PEXRX9+	GNDA25PEX	PEXRX10-	GNDA25PEX	GNDA25SATA	GNDA25SATA	GNDA25SATA
AU	GNDA12PEX	GNDA12PEX	GNDA12PEX	GNDA12PEX	GNDA12PEX	GNDA12PEX	GNDA12PEX	GNDA12PEX	GNDA12PEX	GNDA12PEX	PEXRX8-	GNDA12PEX	PEXTX9+	PEXTX10+	GNDA12PEX	PEXREXTP0	GNDA12SATA	STX1+	GNDA12SATA
AV		DP2TX1+	DP2TX1-	DP2TX0+	DP2TX0-	GNDA12PEX	RSVD	RSVD	RSVD	RSVD	PEXRX8+	GNDA12PEX	PEXTX9-	PEXTX10-	GNDA12PEX		GNDA12SATA	STX1-	GNDA12SATA
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19

Figure 4. VX900M Ball Map – Right Side Top View



	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	
A	HA13#	HA7#	HA10#	GND	MDQS7-	MDQM7	MD55	GND	MDQS6+	MDQM5	MD40	GND	MD34	MCLKO2-	MCLKO2+	GND	MCS2#	MSRAS#		A
B	HA5#	GND	HA8#	HA14#	MDQS7+	GND	MD54	MD49	MDQS6-	GND	MD45	MD39		GND	MODT2	MCLKO5-	MBA0	GND	MCLKO3-	B
C	GND	HA4#		HA16#	GND	MD57	MDQM6	MD53	GND	MD41	MD35	MD38	GND	MA13	MSCAS#	MCLKO5+	GND	MCLKO0-	MCLKO3+	C
D	HADSTB0P#		GND	HAHI0#	MD56		GND	MD48	MD42	MD44	GND	MDQS4+	MDQS4-	MODT0	GND	MCS0#	MBA1	MCLKO0+	GND	D
E	HADSTB0N#	HA9#	HA12#	GND	MD62		MD52	GND		MDQM4	MD32	GND	MD33	MCS3#	MSWE#	GND	MCLKO1-	MA10	MA0	E
F	HABI#	GND	HA15#	HAHI1#		GND	MD50	MD47		GND	MD37		MODT1	GND	MA1	MA2	MCLKO1+	GND	MCLKO4-	F
G	GND	HBREQ0#	HA11#	MD63	GND	MD61	MD51	MD46	GND	MDQS5-	MD36		GND	MEMCOMP	MA3	MA4	GND	MA6	MCLKO4+	G
H	TP1		GND	MD59	MD58	MD60	GND	MD43		MDQS5+	GND	MEMVREF	MEMRESET#	MEMDET	GND	MA8	MA9	MA14	GND	H
J	HGTLVREF0												MODT3	GND	MA7	MA11	MCKE0	GND	MA12	J
K														MCS1#	MA5	GND	MEMPWROK	MA15	MBA2	K
L													MD26	MDQS3-	GND	MCKE2	MCKE3	MCKE1	GND	L
M												MD27	GND	MDQS3+	MDQM3	MD25	GND	MD29	MD24	M
N												MD31	MD30	GND	MD28			GND	MD18	N
P												GND	MD22	MDQS2+		GND	MDQM2	MD16	MD17	P
R											VSUSVDDMEM	MD19	MD23	MDQS2-	GND	MD21	MDQS1+	MDQS1-	GND	R
T													GND	MD20	MD15	MDQM1	GND	MD9	MD8	T
U												MD3	MD11	GND	MD10	MD14	MD12	GND	MD13	U
V										VSUSVDDMEM		GND	MD2	MD7	MD6	GND	MDQS0+	MDQS0-	MDQM0	V
W											TP4	SERIRQ	MD4	MD0	GND	MD1	MD5	LPCDRQ0#	GND	W
Y											VRDSLP	SPKR	GND	AZBITCLK	INTD#	LPCAD1	GND	LPCAD3	LPCAD2	Y
AA											CPUSTP#	INTC#	GPIO10	PCICLK	USBCLK	LPCAD0	AZSYNC	LPCDRQ1#	LPCFRAME#	AA
AB											TP3	GND	PERR#	INTB#	GND	GPIO11	THRM#	C4PSTOP#	AZSDOUT	AB
AC											HDMI_CEC	AD20	AD7	AD3	GPO36	MSPIDO	MSPICLK	MSPIDI	GND	AC
AD											AD6	AD0	AD5	AD21	GPO40	GPO38	GPO39	MSPISS1#	MSPISS0#	AD
AE												GND		CBE0#	GND	AD8	GPO37	AD1	GND	AE
AF												AD22	CBE3#	AD28	AD25	AD2	AD10	AD9	AD4	AF
AG												INTA#	AD23	AD30	AD29	AD24	AD27	AD11	AD12	AG
AH												GND	REQ1#	REQ0#	GND	AD26	AD14	AD13	GND	AH
AJ												GNT1#	SERR#	GNT0#	AD31	CBE1#	PAR	AD15		AJ
AK													AD16	CBE2#	STOP#	TRDY#	DEVSEL#			AK
AL	GNDA12SATA	GND	USBHP5+	GND	USBHP7-	GND	USBDP+	GND			TP6	PCIRST#	EXTSMI#	SUSA#	GND	AD19	FRAME#	IRDY#	GND	AL
AM	SATACLK+	GND	USBHP5-	GND	USBHP7+	GND	USBDP-	GND			GND	SUSB#	PEXWAKE#	SUSC#	CR_CMD	CR_D3	AD18	AD17		AM
AN	GNDA25SATA	GND	GND	GND	GND	GND	GND	GND			RSMRST#	TP	GPWAKE#	PWRBTN#	BATLOW#	CR_D5	CR_D2			AN
AP	SRX0+	GND	USBHP4+	GND	USBHP1+	GND	USBHP2+	GND			PWRGD	VBAT	USBD_DET#	PME#	GND	RSVD	CR_D7	CR_CLK	GND	AP
AR	SRX0-	GND	USBHP4-	GND	USBHP1-	GND	USBHP2-	GND	USBHOC3#	GND	GND	INTRUDER#	USBD_PDN	SMBDT1	LID#	XD_CE#	CR_D0	CR_D4	CR_D6	AR
AT	GNDA25SATA	GND	GND	GND	GND	GND	GND	GND	USBHOC5#	USBHOC2#	MSDT	AZSDIN1	AZSDIN0	SMBCK2	SMBCK1	CR_PWOFF	CR_CD#	CR_D1	XD_ALE	AT
AU	STX0+	GND	USBHP3+	GND	USBHP0-	USBHP6+	GND	USBHOC4#	USBHOC7#	USBHOC6#	RTCXI	KBDT	AZRST#	SMBDT2	SMBALRT#	CR_PWSEL	XD_RE#	CR_WPD	GND	AU
AV	STX0-	GND	USBHP3-	GND	USBHP0+	USBHP6-	GND	USBHOC1#	USBHOC0#	RTCXO	MSCK	KBCK	GND			RING#	XD_CD#	XD_CLE		AV
	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	

VX900M Signal Ball List

Table 4. VX900M Signal Ball List (Listed by Ball Name)

Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #
A20M#	C15	CRTSPD	AB09	GND	B01	GND	J33
AD0 / GPI10	AD31	CRTVSYNC	AA09	GND	B05	GND	J37
AD1 / GPI11	AE37	DEVSEL# / SIN2	AK36	GND	B09	GND	K01
AD2	AF35	DFTEN	A18	GND	B13	GND	K03
AD3	AC33	DISPCLKI0 / VGPI0	Y06	GND	B17	GND	K04
AD4 / GPO4	AF38	DISPCLKI1 / VGPI1	AA04	GND	B21	GND	K05
AD5	AD32	DISPCLKO0 / VGPO0	AA06	GND	B25	GND	K06
AD6	AD30	DISPCLKO1 / VGPO1	AA05	GND	B29	GND	K35
AD7	AC32	DP1_AUX-	T01	GND	B33	GND	L06
AD8	AE35	DP1_AUX+	U01	GND	B37	GND	L34
AD9 / GPIO13	AF37	DP1_HPD#	W06	GND	C04	GND	L38
AD10 / GPIO14	AF36	DP1_REXT	W05	GND	C08	GND	M01
AD11 / GPIO15	AG37	DP1TX0- / HDMITX2-	Y01	GND	C12	GND	M04
AD12 / GPIO16	AG38	DP1TX0+ / HDMITX2+	AA01	GND	C16	GND	M06
AD13 / GPIO17	AH37	DP1TX1- / HDMITX1-	W03	GND	C20	GND	M32
AD14 / GPIO18	AH36	DP1TX1+ / HDMITX1+	Y03	GND	C24	GND	M36
AD15 / GPIO19	AJ37	DP1TX2- / HDMITX0-	V01	GND	C28	GND	N03
AD16 / GPIO20	AK32	DP1TX2+ / HDMITX0+	W01	GND	C32	GND	N04
AD17 / GPIO21	AM37	DP1TX3- / HDMICLK-	U03	GND	C36	GND	N05
AD18 / GPIO22	AM36	DP1TX3+ / HDMICLK+	V03	GND	D02	GND	N06
AD19 / GPIO23	AL35	DP2_AUX-	AL02	GND	D06	GND	N16
AD20 / GPIO24	AC31	DP2_AUX+	AL03	GND	D10	GND	N18
AD21 / GPIO25	AD33	DP2_HPD#	AL05	GND	D14	GND	N20
AD22 / GPIO26	AF31	DP2TX0-	AV05	GND	D18	GND	N22
AD23 / GPIO27	AG32	DP2TX0+	AV04	GND	D22	GND	N24
AD24 / GPIO28	AG35	DP2TX1-	AV03	GND	D26	GND	N26
AD25 / GPIO29	AF34	DP2TX1+	AV02	GND	D30	GND	N33
AD26 / GPIO30	AH35	DP2TX2-	AT01	GND	D34	GND	N37
AD27 / GPIO31	AG36	DP2TX2+	AR01	GND	D38	GND	P03
AD28 / GPIO32	AF33	DP2TX3-	AM01	GND	E03	GND	P05
AD29 / GPIO33	AG34	DP2TX3+	AN01	GND	E07	GND	P06
AD30 / GPIO34	AG33	DPCLK	Y07	GND	E11	GND	P15
AD31 / GPIO35	AJ34	DPSLP#	E14	GND	E15	GND	P17
AZBITCLK	Y33	DVICTL3	AB03	GND	E19	GND	P19
AZRST#	AU32	DVP1CLK	AD01	GND	E23	GND	P21
AZSDIN0	AT32	DVP1D0 / RI1	AD03	GND	E27	GND	P23
AZSDIN1	AT31	DVP1D1 / DCD1	AE02	GND	E31	GND	P25
AZSDOUT	AB38	DVP1D2 / SOUT1	AE03	GND	E35	GND	P31
AZSYNC	AA36	DVP1D3 / SIN1	AF01	GND	F01	GND	P35
BATLOW# / GPI4	AN34	DVP1D4 / DTR1	AE09	GND	F05	GND	R01
BISTEN	B19	DVP1D5 / DSR1	AD09	GND	F09	GND	R05
C4PSTOP# / GPO6	AB37	DVP1D6 / RTS1	AD08	GND	F13	GND	R14
CBE0# / CTS3	AE33	DVP1D7 / CTS1	AD07	GND	F17	GND	R16
CBE1# / RI2	AJ35	DVP1D8 / RI0	AC06	GND	F21	GND	R18
CBE2# / DCD2	AK33	DVP1D9 / DCD0	AC04	GND	F25	GND	R20
CBE3# / SOUT2	AF32	DVP1D10 / SOUT0	AC05	GND	F29	GND	R22
CLK14M	Y08	DVP1D11 / SIN0	AE05	GND	F33	GND	R24
CLK66M	J15	DVP1D12 / DTR0	AD05	GND	F37	GND	R26
CPURST#	F14	DVP1D13 / DSR0	AE06	GND	G04	GND	R34
CPUSTP# / GPO5	AA30	DVP1D14 / RTS0	AE07	GND	G08	GND	R38
CR_CD# / MMC_CD# / SD_CD# / SDIOCD#	AT36	DVP1D15 / CTS0	AE08	GND	G12	GND	T03
CR_CLK / MMC_CLK / XD_WE# / SD_CLK / SDIOCLK	AP37	DVP1DE	AF07	GND	G16	GND	T04
CR_CMD / MMC_CMD# / XD_RB# / SD_CMD / SDIOCMD	AM34	DVP1HS	AD04	GND	G20	GND	T05
CR_D0 / MMC_D0 / XD_D0 / SD_D0 / SDIOD0	AR36	DVP1TVCLKR	AD02	GND	G24	GND	T06
CR_D1 / MMC_D1 / XD_D1 / SD_D1 / SDIOD1	AT37	DVP1TVFLD	AF06	GND	G28	GND	T14
CR_D2 / MMC_D2 / XD_D2 / SD_D2 / SDIOD2	AN36	DVP1VS	AE01	GND	G32	GND	T17
CR_D3 / MMC_D3 / XD_D3 / SD_D3 / SDIOD3	AM35	DVPSPCLK	AB05	GND	G36	GND	T19
CR_D4 / MMC_D4 / XD_D4	AR37	DVPSPD	AB04	GND	H02	GND	T21
CR_D5 / MMC_D5 / XD_D5	AN35	EXTSMI# / GPI5	AL32	GND	H06	GND	T23
CR_D6 / MMC_D6 / XD_D6	AR38	FERR#	B16	GND	H10	GND	T25
CR_D7 / MMC_D7 / XD_D7	AP36	FRAME# / CTS2	AL36	GND	H14	GND	T32
CR_PWOFF / SDIOPWOFF / GPO12	AT35	GND	A03	GND	H18	GND	T36
CR_PWSEL / SDIOPWSEL / GPO11	AU35	GND	A07	GND	H22	GND	U16
CR_WPD / XD_WP# / SD_WPD / SDIOWPD	AU37	GND	A11	GND	H26	GND	U18
CRTAB	L02	GND	A15	GND	H30	GND	U20
CRTAG	L01	GND	A19	GND	H34	GND	U22
CRTAR	L03	GND	A23	GND	H38	GND	U24
CRTHSYNC	AA08	GND	A27	GND	J02	GND	U26
CRTRSET	K02	GND	A31	GND	J05	GND	U33
CRTSPCLK	AA10	GND	A35	GND	J06	GND	U37

Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #
GND	V15	GND	AL27	GNDA12PEX	AU10	GNDA25SATA	AN18
GND	V17	GND	AL34	GNDA12PEX	AU12	GNDA25SATA	AN19
GND	V19	GND	AL38	GNDA12PEX	AU15	GNDA25SATA	AN20
GND	V21	GND	AM21	GNDA12PEX	AV06	GNDA25SATA	AP17
GND	V23	GND	AM23	GNDA12PEX	AV12	GNDA25SATA	AP19
GND	V25	GND	AM25	GNDA12PEX	AV15	GNDA25SATA	AR17
GND	V31	GND	AM27	GNDA12SATA	AF21	GNDA25SATA	AR19
GND	V35	GND	AM30	GNDA12SATA	AL20	GNDA25SATA	AT17
GND	W08	GND	AN21	GNDA12SATA	AM19	GNDA25SATA	AT18
GND	W16	GND	AN22	GNDA12SATA	AU17	GNDA25SATA	AT19
GND	W18	GND	AN23	GNDA12SATA	AU19	GNDA25SATA	AT20
GND	W20	GND	AN24	GNDA12SATA	AV17	GNT0# / SOUT3	AJ33
GND	W22	GND	AN25	GNDA12SATA	AV19	GNT1# / RTS3	AJ31
GND	W34	GND	AN26	GNDA25DP1	T02	GPIO10 / SATALED0#	AA32
GND	W38	GND	AN27	GNDA25DP1	U02	GPIO11 / SATALED1#	AB35
GND	Y05	GND	AP21	GNDA25DP1	U04	GPO36 / PCIERST1#	AC34
GND	Y17	GND	AP23	GNDA25DP1	V02	GPO37 / PCIERST2#	AE36
GND	Y19	GND	AP25	GNDA25DP1	V04	GPO38 / PCIERST3#	AD35
GND	Y21	GND	AP27	GNDA25DP1	W02	GPO39	AD36
GND	Y23	GND	AP34	GNDA25DP1	W04	GPO40	AD34
GND	Y24	GND	AP38	GNDA25DP1	W13	GPWAKE# / GPI1	AN32
GND	Y32	GND	AR21	GNDA25DP1	Y02	HA3#	D19
GND	Y36	GND	AR23	GNDA25DP1	Y04	HA4#	C21
GND	AA14	GND	AR25	GNDA25DP1	AA02	HA5#	B20
GND	AA16	GND	AR27	GNDA25DP1	AA03	HA6#	C18
GND	AA18	GND	AR29	GNDA25HCK	J16	HA7#	A21
GND	AA20	GND	AR30	GNDA25PEX	AF15	HA8#	B22
GND	AA22	GND	AT21	GNDA25PEX	AF17	HA9#	E21
GND	AB08	GND	AT22	GNDA25PEX	AF19	HA10#	A22
GND	AB15	GND	AT23	GNDA25PEX	AK02	HA11#	G22
GND	AB17	GND	AT24	GNDA25PEX	AK03	HA12#	E22
GND	AB19	GND	AT25	GNDA25PEX	AK04	HA13#	A20
GND	AB21	GND	AT26	GNDA25PEX	AK05	HA14#	B23
GND	AB23	GND	AT27	GNDA25PEX	AL04	HA15#	F22
GND	AB31	GND	AU21	GNDA25PEX	AL06	HA16#	C23
GND	AB34	GND	AU23	GNDA25PEX	AL15	HABI#	F20
GND	AC02	GND	AU26	GNDA25PEX	AM02	HADS#	G18
GND	AC14	GND	AU38	GNDA25PEX	AM03	HADSTB0N#	E20
GND	AC16	GND	AV21	GNDA25PEX	AM04	HADSTB0P#	D20
GND	AC18	GND	AV23	GNDA25PEX	AM05	HAHI0#	D23
GND	AC20	GND	AV26	GNDA25PEX	AM06	HAHI1#	F23
GND	AC22	GND	AV32	GNDA25PEX	AN04	HALF#	G19
GND	AC24	GNDA12DP1	Y11	GNDA25PEX	AN05	HBNR#	F15
GND	AC26	GNDA12DP1	Y12	GNDA25PEX	AN06	HBPRI#	D16
GND	AC38	GNDA12DP1	Y13	GNDA25PEX	AN07	HBREQ0#	G21
GND	AD06	GNDA12PEX	AD17	GNDA25PEX	AN08	HCLK-	J18
GND	AD25	GNDA12PEX	AD19	GNDA25PEX	AN09	HCLK+	J17
GND	AE04	GNDA12PEX	AL01	GNDA25PEX	AN10	HD0#	H13
GND	AE31	GNDA12PEX	AM07	GNDA25PEX	AP04	HD1#	E10
GND	AE34	GNDA12PEX	AM08	GNDA25PEX	AP06	HD2#	D12
GND	AE38	GNDA12PEX	AM09	GNDA25PEX	AP09	HD3#	D13
GND	AF03	GNDA12PEX	AM10	GNDA25PEX	AP11	HD4#	E12
GND	AF08	GNDA12PEX	AM11	GNDA25PEX	AP12	HD5#	F08
GND	AG06	GNDA12PEX	AM12	GNDA25PEX	AP13	HD6#	E13
GND	AG09	GNDA12PEX	AM13	GNDA25PEX	AP14	HD7#	F12
GND	AH04	GNDA12PEX	AM14	GNDA25PEX	AP15	HD8#	G13
GND	AH07	GNDA12PEX	AN11	GNDA25PEX	AR02	HD9#	F11
GND	AH31	GNDA12PEX	AN12	GNDA25PEX	AR03	HD10#	E09
GND	AH34	GNDA12PEX	AN13	GNDA25PEX	AR06	HD11#	D09
GND	AH38	GNDA12PEX	AN14	GNDA25PEX	AR09	HD12#	G09
GND	AJ06	GNDA12PEX	AP01	GNDA25PEX	AR12	HD13#	C11
GND	AK21	GNDA12PEX	AU01	GNDA25PEX	AR14	HD14#	H12
GND	AK22	GNDA12PEX	AU02	GNDA25PEX	AR16	HD15#	F10
GND	AK23	GNDA12PEX	AU03	GNDA25PEX	AT07	HD16#	B10
GND	AK24	GNDA12PEX	AU04	GNDA25PEX	AT10	HD17#	A10
GND	AK25	GNDA12PEX	AU05	GNDA25PEX	AT12	HD18#	A06
GND	AK26	GNDA12PEX	AU06	GNDA25PEX	AT14	HD19#	A05
GND	AL21	GNDA12PEX	AU07	GNDA25PEX	AT16	HD20#	C10
GND	AL23	GNDA12PEX	AU08	GNDA25SATA	AG21	HD21#	D11
GND	AL25	GNDA12PEX	AU09	GNDA25SATA	AM18	HD22#	B11

Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #
HD23#	A09	HRS1#	H16	MCS1#	K33	MDQM3	M34
HD24#	B07	HTRDY#	D17	MCS2#	A36	MDQM4	E29
HD25#	D08	IGNNE#	A17	MCS3#	E33	MDQM5	A29
HD26#	A08	INIT#	B14	MD0	W33	MDQM6	C26
HD27#	C06	INTA#	AG31	MD1	W35	MDQM7	A25
HD28#	A04	INTB# / GPIO8	AB33	MD2	V32	MDQS0-	V37
HD29#	C09	INTC# / GPIO9	AA31	MD3	U31	MDQS0+	V36
HD30#	B06	INTD# / GPIO12	Y34	MD4	W32	MDQS1-	R37
HD31#	E08	INTR	A16	MD5	W36	MDQS1+	R36
HD32#	G05	INTRUDER# / GPI6	AR31	MD6	V34	MDQS2-	R33
HD33#	F06	IRDY# / DSR2	AL37	MD7	V33	MDQS2+	P33
HD34#	B03	KBCK / GPIO5 / A20GATE	AV31	MD8	T38	MDQS3-	L33
HD35#	B04	KBDT / GPIO4 / KBC_CPURST#	AU31	MD9	T37	MDQS3+	M33
HD36#	A02	LID# / GPI7	AR34	MD10	U34	MDQS4-	D32
HD37#	H09	LPCAD0	AA35	MD11	U32	MDQS4+	D31
HD38#	F07	LPCAD1	Y35	MD12	U36	MDQS5-	G29
HD39#	H08	LPCAD2	Y38	MD13	U38	MDQS5+	H29
HD40#	H05	LPCAD3	Y37	MD14	U35	MDQS6-	B28
HD41#	E05	LPCDRQ0#	W37	MD15	T34	MDQS6+	A28
HD42#	G06	LPCDRQ1#	AA37	MD16	P37	MDQS7-	A24
HD43#	C03	LPCFRAME#	AA38	MD17	P38	MDQS7+	B24
HD44#	E06	LVDSCLK-	N02	MD18	N38	MEMCOMP	G33
HD45#	H07	LVDSCLK+	N01	MD19	R31	MEMDET	H33
HD46#	G07	LVDSD0-	R03	MD20	T33	MEMPWROK	K36
HD47#	D05	LVDSD0+	R02	MD21	R35	MEMRESET#	H32
HD48#	B02	LVDSD1-	R04	MD22	P32	MEMVREF	H31
HD49#	E02	LVDSD1+	P04	MD23	R32	MODT0	D33
HD50#	C02	LVDSD2-	P01	MD24	M38	MODT1	F32
HD51#	H01	LVDSD2+	P02	MD25	M35	MODT2	B34
HD52#	E01	LVDSD3-	M02	MD26	L32	MODT3	J32
HD53#	C01	LVDSD3+	M03	MD27	M31	MSCAS#	C34
HD54#	D01	LVDSENBL	AB06	MD28	N34	MSCK / GPIO3	AV30
HD55#	G01	LVDSENVDD	AB07	MD29	M37	MSDT / GPIO2	AT30
HD56#	F02	LVDSPWM	AA07	MD30	N32	MSPICLK / GPIO6	AC36
HD57#	D03	MA0	E38	MD31	N31	MSPIDI / GPI0	AC37
HD58#	J01	MA1	F34	MD32	E30	MSPIDO / GPO1	AC35
HD59#	J03	MA2	F35	MD33	E32	MSPISS0# / GPO3	AD38
HD60#	J04	MA3	G34	MD34	A32	MSPISS1# / GPO2	AD37
HD61#	H04	MA4	G35	MD35	C30	MSRAS#	A37
HD62#	H03	MA5	K34	MD36	G30	MSWE#	E34
HD63#	F04	MA6	G37	MD37	F30	NAP#	A12
HDBI0#	G10	MA7	J34	MD38	C31	NMI	B15
HDBI1#	B08	MA8	H35	MD39	B31	PAR / DTR3	AJ36
HDBI2#	C05	MA9	H36	MD40	A30	PCICLK	AA33
HDBI3#	G02	MA10	E37	MD41	C29	PCIRST#	AL31
HDBSY#	E17	MA11	J35	MD42	D28	PERR#	AB32
HDEFER#	C17	MA12	J38	MD43	H27	PEXCLK-	AM15
HDMI_CEC	AC30	MA13	C33	MD44	D29	PEXCLK+	AN15
HDMIRSPC	AB01	MA14	H37	MD45	B30	PEXREXTP0	AU16
HDMIRSPD	AB02	MA15	K37	MD46	G27	PEXRX8-	AU11
HDPWR#	B12	MBA0	B36	MD47	F27	PEXRX8+	AV11
HDRDY#	F16	MBA1	D36	MD48	D27	PEXRX9-	AR13
HDSTB0N#	H11	MBA2	K38	MD49	B27	PEXRX9+	AT13
HDSTB0P#	G11	MCKE0	J36	MD50	F26	PEXRX10-	AT15
HDSTB1N#	C07	MCKE1	L37	MD51	G26	PEXRX10+	AR15
HDSTB1P#	D07	MCKE2	L35	MD52	E26	PEXTX8-	AT11
HDSTB2N#	E04	MCKE3	L36	MD53	C27	PEXTX8+	AR11
HDSTB2P#	D04	MCLKO0-	C37	MD54	B26	PEXTX9-	AV13
HDSTB3N#	G03	MCLKO0+	D37	MD55	A26	PEXTX9+	AU13
HDSTB3P#	F03	MCLKO1-	E36	MD56	D24	PEXTX10-	AV14
HGTLPVT_REXT	H17	MCLKO1+	F36	MD57	C25	PEXTX10+	AU14
HGTLVREF0	J20	MCLKO2-	A33	MD58	H24	PEXWAKE# / GPI14	AM32
HGTLVREF1	J13	MCLKO2+	A34	MD59	H23	PME# / GPIO7	AP33
HHIT#	G17	MCLKO3-	B38	MD60	H25	PWRBTN#	AN33
HHITM#	E16	MCLKO3+	C38	MD61	G25	PWRGD	AP30
HLOCK#	D15	MCLKO4-	F38	MD62	E24	REQ0# / SIN3	AH33
HREQ0#	F18	MCLKO4+	G38	MD63	G23	REQ1# / DSR3	AH32
HREQ1#	E18	MCLKO5-	B35	MDQM0	V38	RING# / GPI8	AV35
HREQ2#	B18	MCLKO5+	C35	MDQM1	T35	ROMSPC	AC03
HRS0#	G15	MCS0#	D35	MDQM2	P36	ROMSPD	AC01

Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #
RSMRST#	AN30	USBDREXT	AJ24	VCCA25PEX	AK08	VSUSA33USBH	AE22
RSVD	AN03	USBHOC0#	AV28	VCCA25PEX	AK09	VSUSA33USBH	AG22
RSVD	AN02	USBHOC1#	AV27	VCCA25PEX	AL07	VSUSA33USBH	AH22
RSVD	AP02	USBHOC2#	AT29	VCCA25PEX	AL08	VSUSA33USBH	AJ21
RSVD	AP03	USBHOC3#	AR28	VCCA25PEX	AL09	VSUSAVDDUSBH	AE23
RSVD	AT02	USBHOC4#	AU27	VCCA25PEX	AL10	VSUSIOMEM	N21
RSVD	AT03	USBHOC5#	AT28	VCCA25PLLDISP	T15	VSUSIOMEM	N23
RSVD	AT04	USBHOC6#	AU29	VCCA25PLLDISP	U15	VSUSIOMEM	N25
RSVD	AR04	USBHOC7#	AU28	VCCA25PLLLVDS	U12	VSUSIOMEM	P22
RSVD	AP05	USBHP0-	AU24	VCCA25SATA	AE21	VSUSIOMEM	P24
RSVD	AP35	USBHP0+	AV24	VCCA25SATA	AL18	VSUSIOMEM	P26
RSVD	AR05	USBHP1-	AR24	VCCA33USBD	AE24	VSUSIOMEM	R21
RSVD	AR07	USBHP1+	AP24	VCCA33USBD	AK27	VSUSIOMEM	R23
RSVD	AP07	USBHP2-	AR26	VCCCR	AB25	VSUSIOMEM	R25
RSVD	AP08	USBHP2+	AP26	VCPCLK / PTS0CLK / DSR1	AG07	VSUSIOMEM	T24
RSVD	AR08	USBHP3-	AV22	VCPD0 / PTS0D0 / RI0	AG01	VSUSIOMEM	T26
RSVD	AR10	USBHP3+	AU22	VCPD1 / PTS0D1 / DCD0	AG03	VSUSIOMEM	U25
RSVD	AP10	USBHP4-	AR22	VCPD2 / PTS0D2 / SOUT0	AH03	VSUSIOMEM	V24
RSVD	AT06	USBHP4+	AP22	VCPD3 / PTS0D3 / SIN0	AH01	VSUSIOMEM	V26
RSVD	AT05	USBHP5-	AM22	VCPD4 / PTS0D4 / DTR0	AH02	VSUSVDD	AB26
RSVD	AV08	USBHP5+	AL22	VCPD5 / PTS0D5 / DSR0	AJ03	VSUSVDD	AD26
RSVD	AV07	USBHP6-	AV25	VCPD6 / PTS0D6 / RTS0	AJ01	VSUSVDD	AE26
RSVD	AT09	USBHP6+	AU25	VCPD7 / PTS0D7 / CTS0	AJ02	VSUSVDDMEM	R30
RSVD	AT08	USBHP7-	AL24	VCPD8 / PTS0ERR / SIN1	AF05	VSUSVDDMEM	V29
RSVD	AV10	USBHP7+	AM24	VCPD9 / STS1VLD / SOUT1	AG04	VTT	N15
RSVD	AV09	USBHREXT	AJ22	VCPD10 / STS1SYNC / DCD1	AG05	VTT	N17
RTCXI	AU30	VBAT	AP31	VCPD11 / STS1CLK / RI1	AJ04	VTT	N19
RTCXO	AV29	VCC33	W24	VCPD12 / STS1ERR	AH05	VTT	P14
SATACLK+	AM20	VCC33	W25	VCPD13	AJ05	VTT	P16
SATAREXTP	AN17	VCC33	W26	VCPD14	AH06	VTT	P18
SERIRQ	W31	VCC33	Y25	VCPD15 / STS1D / DTR1	AG08	VTT	P20
SERR# / RI3	AJ32	VCC33	Y26	VCPHS / PTS0VLD / CTS1	AF02	VTT	R15
SLP#	A13	VCC33	AA24	VCPVS / PTS0SYNC / RTS1	AG02	VTT	R17
SMBALRT#	AU34	VCC33	AA25	VDD	T16	VTT	R19
SMBCK1	AT34	VCC33	AB24	VDD	T18	XD_ALE	AT38
SMBCK2 / GPIO1	AT33	VCC33VGA	AA15	VDD	T20	XD_CD#	AV36
SMBDT1	AR33	VCC33VGA	AB14	VDD	T22	XD_CE#	AR35
SMBDT2 / GPIO0	AU33	VCC33VGA	AC15	VDD	U17	XD_CLE	AV37
SMI#	C14	VCC33VGA	AD14	VDD	U19	XD_RE#	AU36
SPKR / GPO0	Y31	VCC33VGA	AE14	VDD	U21		
SRX0-	AR20	VCCA12DP1	Y14	VDD	U23		
SRX0+	AP20	VCCA12DP1	Y15	VDD	V16		
SRX1-	AR18	VCCA12PEX	AD15	VDD	V18		
SRX1+	AP18	VCCA12PEX	AD16	VDD	V20		
STOP# / DTR2	AK34	VCCA12PEX	AD18	VDD	V22		
STPCLK#	A14	VCCA12PEX	AD20	VDD	W17		
STX0-	AV20	VCCA12PEX	AL11	VDD	W19		
STX0+	AU20	VCCA12PEX	AL12	VDD	W21		
STX1-	AV18	VCCA12PEX	AL13	VDD	W23		
STX1+	AU18	VCCA12PEX	AL14	VDD	Y16		
SUSA# / SLOWCLK / GPO7	AL33	VCCA12SATA	AD21	VDD	Y18		
SUSB# / GPO8	AM31	VCCA12SATA	AL19	VDD	Y20		
SUSC# / GPO9	AM33	VCCA12USBD	AF24	VDD	Y22		
TESTEN	J19	VCCA25DAC	L04	VDD	AA17		
THRM# / GPI9	AB36	VCCA25DAC	L05	VDD	AA19		
THRMTRIP#	C13	VCCA25DAC	T13	VDD	AA21		
TP	AN31	VCCA25DP1	W14	VDD	AA23		
TP0	H19	VCCA25DP1	W15	VDD	AB16		
TP1	H20	VCCA25HCK	K16	VDD	AB18		
TP2	K18	VCCA25LVDS	U13	VDD	AB20		
TP3	AB30	VCCA25LVDS	U14	VDD	AB22		
TP4	W30	VCCA25LVDS	V14	VDD	AC17		
TP5	W07	VCCA25PEX	AE15	VDD	AC19		
TP6	AL30	VCCA25PEX	AE16	VDD	AC21		
TRDY# / RTS2	AK35	VCCA25PEX	AE17	VDD	AC23		
USBCLK	AA34	VCCA25PEX	AE18	VGPIO	AF04		
USBD_DET#	AP32	VCCA25PEX	AE19	VRDSLP	Y30		
USBD_PDN / GPO10	AR32	VCCA25PEX	AE20	VSUS33	AC25		
USBDP-	AM26	VCCA25PEX	AK06	VSUS33	AD24		
USBDP+	AL26	VCCA25PEX	AK07	VSUSA33USBH	AD23		

Table 5. VX900M Signal Ball List (Listed by Ball Number)

Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name
A02	HD36#	B36	MBA0	D34	GND	F34	MA1
A03	GND	B37	GND	D35	MCS0#	F35	MA2
A04	HD28#	B38	MCLKO3-	D36	MBA1	F36	MCLKO1+
A05	HD19#	**C01**	HD53#	D37	MCLKO0+	F37	GND
A06	HD18#	C02	HD50#	D38	GND	F38	MCLKO4-
A07	GND	C03	HD43#	**E01**	HD52#	**G01**	HD55#
A08	HD26#	C04	GND	E02	HD49#	G02	HDBI3#
A09	HD23#	C05	HDBI2#	E03	GND	G03	HDSTB3N#
A10	HD17#	C06	HD27#	E04	HDSTB2N#	G04	GND
A11	GND	C07	HDSTB1N#	E05	HD41#	G05	HD32#
A12	NAP#	C08	GND	E06	HD44#	G06	HD42#
A13	SLP#	C09	HD29#	E07	GND	G07	HD46#
A14	STPCLK#	C10	HD20#	E08	HD31#	G08	GND
A15	GND	C11	HD13#	E09	HD10#	G09	HD12#
A16	INTR	C12	GND	E10	HD1#	G10	HDBI0#
A17	IGNNE#	C13	THRMTRIP#	E11	GND	G11	HDSTB0P#
A18	DFTEN	C14	SMI#	E12	HD4#	G12	GND
A19	GND	C15	A20M#	E13	HD6#	G13	HD8#
A20	HA13#	C16	GND	E14	DPSLP#	G15	HRS0#
A21	HA7#	C17	HDEFER#	E15	GND	G16	GND
A22	HA10#	C18	HA6#	E16	HHITM#	G17	HHIT#
A23	GND	C20	GND	E17	HDBSY#	G18	HADS#
A24	MDQS7-	C21	HA4#	E18	HREQ1#	G19	HALF#
A25	MDQM7	C23	HA16#	E19	GND	G20	GND
A26	MD55	C24	GND	E20	HADSTB0N#	G21	HBREQ0#
A27	GND	C25	MD57	E21	HA9#	G22	HA11#
A28	MDQS6+	C26	MDQM6	E22	HA12#	G23	MD63
A29	MDQM5	C27	MD53	E23	GND	G24	GND
A30	MD40	C28	GND	E24	MD62	G25	MD61
A31	GND	C29	MD41	E26	MD52	G26	MD51
A32	MD34	C30	MD35	E27	GND	G27	MD46
A33	MCLKO2-	C31	MD38	E29	MDQM4	G28	GND
A34	MCLKO2+	C32	GND	E30	MD32	G29	MDQS5-
A35	GND	C33	MA13	E31	GND	G30	MD36
A36	MCS2#	C34	MSCAS#	E32	MD33	G32	GND
A37	MSRAS#	C35	MCLKO5+	E33	MCS3#	G33	MEMCOMP
B01	GND	C36	GND	E34	MSWE#	G34	MA3
B02	HD48#	C37	MCLKO0-	E35	GND	G35	MA4
B03	HD34#	C38	MCLKO3+	E36	MCLKO1-	G36	GND
B04	HD35#	**D01**	HD54#	E37	MA10	G37	MA6
B05	GND	D02	GND	E38	MA0	G38	MCLKO4+
B06	HD30#	D03	HD57#	**F01**	GND	**H01**	HD51#
B07	HD24#	D04	HDSTB2P#	F02	HD56#	H02	GND
B08	HDBI1#	D05	HD47#	F03	HDSTB3P#	H03	HD62#
B09	GND	D06	GND	F04	HD63#	H04	HD61#
B10	HD16#	D07	HDSTB1P#	F05	GND	H05	HD40#
B11	HD22#	D08	HD25#	F06	HD33#	H06	GND
B12	HDPWR#	D09	HD11#	F07	HD38#	H07	HD45#
B13	GND	D10	GND	F08	HD5#	H08	HD39#
B14	INIT#	D11	HD21#	F09	GND	H09	HD37#
B15	NMI	D12	HD2#	F10	HD15#	H10	GND
B16	FERR#	D13	HD3#	F11	HD9#	H11	HDSTB0N#
B17	GND	D14	GND	F12	HD7#	H12	HD14#
B18	HREQ2#	D15	HLOCK#	F13	GND	H13	HD0#
B19	BISTEN	D16	HBPRI#	F14	CPURST#	H14	GND
B20	HA5#	D17	HTRDY#	F15	HBNR#	H16	HRS1#
B21	GND	D18	GND	F16	HDRDY#	H17	HGTLPVT_REXT
B22	HA8#	D19	HA3#	F17	GND	H18	GND
B23	HA14#	D20	HADSTB0P#	F18	HREQ0#	H19	TP0
B24	MDQS7+	D22	GND	F20	HABI#	H20	TP1
B25	GND	D23	HAHI0#	F21	GND	H22	GND
B26	MD54	D24	MD56	F22	HA15#	H23	MD59
B27	MD49	D26	GND	F23	HAHI1#	H24	MD58
B28	MDQS6-	D27	MD48	F25	GND	H25	MD60
B29	GND	D28	MD42	F26	MD50	H26	GND
B30	MD45	D29	MD44	F27	MD47	H27	MD43
B31	MD39	D30	GND	F29	GND	H29	MDQS5+
B33	GND	D31	MDQS4+	F30	MD37	H30	GND
B34	MODT2	D32	MDQS4-	F32	MODT1	H31	MEMVREF
B35	MCLKO5-	D33	MODT0	F33	GND	H32	MEMRESET#

Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name
H33	MEMDET	N05	GND	R36	MDQS1+	V23	GND
H34	GND	N06	GND	R37	MDQS1-	V24	VSUSIOMEM
H35	MA8	N15	VTT	R38	GND	V25	GND
H36	MA9	N16	GND	**T01**	DP1_AUX-	V26	VSUSIOMEM
H37	MA14	N17	VTT	T02	GNDA25DP1	V29	VSUSVDDMEM
H38	GND	N18	GND	T03	GND	V31	GND
J01	HD58#	N19	VTT	T04	GND	V32	MD2
J02	GND	N20	GND	T05	GND	V33	MD7
J03	HD59#	N21	VSUSIOMEM	T06	GND	V34	MD6
J04	HD60#	N22	GND	T13	VCCA25DAC	V35	GND
J05	GND	N23	VSUSIOMEM	T14	GND	V36	MDQS0+
J06	GND	N24	GND	T15	VCCA25PLLDISP	V37	MDQS0-
J13	HGTLVREF1	N25	VSUSIOMEM	T16	VDD	V38	MDQM0
J15	CLK66M	N26	GND	T17	GND	**W01**	DP1TX2+ / HDMITX0+
J16	GNDA25HCK	N31	MD31	T18	VDD	W02	GNDA25DP1
J17	HCLK+	N32	MD30	T19	GND	W03	DP1TX1- / HDMITX1-
J18	HCLK-	N33	GND	T20	VDD	W04	GNDA25DP1
J19	TESTEN	N34	MD28	T21	GND	W05	DP1_REXT
J20	HGTLVREF0	N37	GND	T22	VDD	W06	DP1_HPD#
J32	MODT3	N38	MD18	T23	GND	W07	TP5
J33	GND	**P01**	LVDSD2-	T24	VSUSIOMEM	W08	GND
J34	MA7	P02	LVDSD2+	T25	GND	W13	GNDA25DP1
J35	MA11	P03	GND	T26	VSUSIOMEM	W14	VCCA25DP1
J36	MCKE0	P04	LVDSD1+	T32	GND	W15	VCCA25DP1
J37	GND	P05	GND	T33	MD20	W16	GND
J38	MA12	P06	GND	T34	MD15	W17	VDD
K01	GND	P14	VTT	T35	MDQM1	W18	GND
K02	CRTRSET	P15	GND	T36	GND	W19	VDD
K03	GND	P16	VTT	T37	MD9	W20	GND
K04	GND	P17	GND	T38	MD8	W21	VDD
K05	GND	P18	VTT	**U01**	DP1_AUX+	W22	GND
K06	GND	P19	GND	U02	GNDA25DP1	W23	VDD
K16	VCCA25HCK	P20	VTT	U03	DP1TX3- / HDMICLK-	W24	VCC33
K18	TP2	P21	GND	U04	GNDA25DP1	W25	VCC33
K33	MCS1#	P22	VSUSIOMEM	U12	VCCA25PLLLVDS	W26	VCC33
K34	MA5	P23	GND	U13	VCCA25LVDS	W30	TP4
K35	GND	P24	VSUSIOMEM	U14	VCCA25LVDS	W31	SERIRQ
K36	MEMPWROK	P25	GND	U15	VCCA25PLLDISP	W32	MD4
K37	MA15	P26	VSUSIOMEM	U16	GND	W33	MD0
K38	MBA2	P31	GND	U17	VDD	W34	GND
L01	CRTAG	P32	MD22	U18	GND	W35	MD1
L02	CRTAB	P33	MDQS2+	U19	VDD	W36	MD5
L03	CRTAR	P35	GND	U20	GND	W37	LPCDRQ0#
L04	VCCA25DAC	P36	MDQM2	U21	VDD	W38	GND
L05	VCCA25DAC	P37	MD16	U22	GND	**Y01**	DP1TX0- / HDMITX2-
L06	GND	P38	MD17	U23	VDD	Y02	GNDA25DP1
L32	MD26	**R01**	GND	U24	GND	Y03	DP1TX1+ / HDMITX1+
L33	MDQS3-	R02	LVDSD0+	U25	VSUSIOMEM	Y04	GNDA25DP1
L34	GND	R03	LVDSD0-	U26	GND	Y05	GND
L35	MCKE2	R04	LVDSD1-	U31	MD3	Y06	DISPCLKI0 / VGPI0
L36	MCKE3	R05	GND	U32	MD11	Y07	DPCLK
L37	MCKE1	R14	GND	U33	GND	Y08	CLK14M
L38	GND	R15	VTT	U34	MD10	Y11	GNDA12DP1
M01	GND	R16	GND	U35	MD14	Y12	GNDA12DP1
M02	LVDSD3-	R17	VTT	U36	MD12	Y13	GNDA12DP1
M03	LVDSD3+	R18	GND	U37	GND	Y14	VCCA12DP1
M04	GND	R19	VTT	U38	MD13	Y15	VCCA12DP1
M06	GND	R20	GND	**V01**	DP1TX2- / HDMITX0-	Y16	VDD
M31	MD27	R21	VSUSIOMEM	V02	GNDA25DP1	Y17	GND
M32	GND	R22	GND	V03	DP1TX3+ / HDMICLK+	Y18	VDD
M33	MDQS3+	R23	VSUSIOMEM	V04	GNDA25DP1	Y19	GND
M34	MDQM3	R24	GND	V14	VCCA25LVDS	Y20	VDD
M35	MD25	R25	VSUSIOMEM	V15	GND	Y21	GND
M36	GND	R26	GND	V16	VDD	Y22	VDD
M37	MD29	R30	VSUSVDDMEM	V17	GND	Y23	GND
M38	MD24	R31	MD19	V18	VDD	Y24	GND
N01	LVDSCLK+	R32	MD23	V19	GND	Y25	VCC33
N02	LVDSCLK-	R33	MDQS2-	V20	VDD	Y26	VCC33
N03	GND	R34	GND	V21	GND	Y30	VRDSLP
N04	GND	R35	MD21	V22	VDD	Y31	SPKR / GPO0

Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name
Y32	GND	AC04	DVP1D9 / DCD0	AE22	VSUSA33USBH	AJ06	GND
Y33	AZBITCLK	AC05	DVP1D10 / SOUT0	AE23	VSUSAVDDUSBH	AJ21	VSUSA33USBH
Y34	INTD# / GPIO12	AC06	DVP1D8 / RI0	AE24	VCCA33USBD	AJ22	USBHREXT
Y35	LPCAD1	AC14	GND	AE26	VSUSVDD	AJ24	USBDREXT
Y36	GND	AC15	VCC33VGA	AE31	GND	AJ31	GNT1# / RTS3
Y37	LPCAD3	AC16	GND	AE33	CBE0# / CTS3	AJ32	SERR# / RI3
Y38	LPCAD2	AC17	VDD	AE34	GND	AJ33	GNT0# / SOUT3
AA01	DP1TX0+ / HDMITX2+	AC18	GND	AE35	AD8	AJ34	AD31 / GPIO35
AA02	GNDA25DP1	AC19	VDD	AE36	GPO37 / PCIERST2#	AJ35	CBE1# / RI2
AA03	GNDA25DP1	AC20	GND	AE37	AD1 / GPI11	AJ36	PAR / DTR3
AA04	DISPCLKI1 / VGPI1	AC21	VDD	AE38	GND	AJ37	AD15 / GPIO19
AA05	DISPCLKO1 / VGPO1	AC22	GND	**AF01**	DVP1D3 / SIN1	**AK02**	GNDA25PEX
AA06	DISPCLKO0 / VGPO0	AC23	VDD	AF02	VCPHS / PTS0VLD / CTS1	AK03	GNDA25PEX
AA07	LVDSPWM	AC24	GND	AF03	GND	AK04	GNDA25PEX
AA08	CRTHSYNC	AC25	VSUS33	AF04	VGPIO	AK05	GNDA25PEX
AA09	CRTVSYNC	AC26	GND	AF05	VCPD8 / PTS0ERR / SIN1	AK06	VCCA25PEX
AA10	CRTSPCLK	AC30	HDMI_CEC	AF06	DVP1TVFLD	AK07	VCCA25PEX
AA14	GND	AC31	AD20 / GPIO24	AF07	DVP1DE	AK08	VCCA25PEX
AA15	VCC33VGA	AC32	AD7	AF08	GND	AK09	VCCA25PEX
AA16	GND	AC33	AD3	AF15	GNDA25PEX	AK21	GND
AA17	VDD	AC34	GPO36 / PCIERST1#	AF17	GNDA25PEX	AK22	GND
AA18	GND	AC35	MSPIDO / GPO1	AF19	GNDA25PEX	AK23	GND
AA19	VDD	AC36	MSPICLK / GPIO6	AF21	GNDA12SATA	AK24	GND
AA20	GND	AC37	MSPIDI / GPI0	AF24	VCCA12USBD	AK25	GND
AA21	VDD	AC38	GND	AF31	AD22 / GPIO26	AK26	GND
AA22	GND	**AD01**	DVP1CLK	AF32	CBE3# / SOUT2	AK27	VCCA33USBD
AA23	VDD	AD02	DVP1TVCLKR	AF33	AD28 / GPIO32	AK32	AD16 / GPIO20
AA24	VCC33	AD03	DVP1D0 / RI1	AF34	AD25 / GPIO29	AK33	CBE2# / DCD2
AA25	VCC33	AD04	DVP1HS	AF35	AD2	AK34	STOP# / DTR2
AA30	CPUSTP# / GPO5	AD05	DVP1D12 / DTR0	AF36	AD10 / GPIO14	AK35	TRDY# / RTS2
AA31	INTC# / GPIO9	AD06	GND	AF37	AD9 / GPIO13	AK36	DEVSEL# / SIN2
AA32	GPIO10 / SATALED0#	AD07	DVP1D7 / CTS1	AF38	AD4 / GPO4	**AL01**	GNDA12PEX
AA33	PCICLK	AD08	DVP1D6 / RTS1	**AG01**	VCPD0 / PTS0D0 / RI0	AL02	DP2_AUX-
AA34	USBCLK	AD09	DVP1D5 / DSR1	AG02	VCPVS / PTS0SYNC / RTS1	AL03	DP2_AUX+
AA35	LPCAD0	AD14	VCC33VGA	AG03	VCPD1 / PTS0D1 / DCD0	AL04	GNDA25PEX
AA36	AZSYNC	AD15	VCCA12PEX	AG04	VCPD9 / STS1VLD / SOUT1	AL05	DP2_HPD#
AA37	LPCDRQ1#	AD16	VCCA12PEX	AG05	VCPD10 / STS1SYNC / DCD1	AL06	GNDA25PEX
AA38	LPCFRAME#	AD17	GNDA12PEX	AG06	GND	AL07	VCCA25PEX
AB01	HDMIRSPC	AD18	VCCA12PEX	AG07	VCPCLK / PTS0CLK / DSR1	AL08	VCCA25PEX
AB02	HDMIRSPD	AD19	GNDA12PEX	AG08	VCPD15 / STS1D / DTR1	AL09	VCCA25PEX
AB03	DVICTL3	AD20	VCCA12PEX	AG09	GND	AL10	VCCA25PEX
AB04	DVPSPD	AD21	VCCA12SATA	AG21	GNDA25SATA	AL11	VCCA12PEX
AB05	DVPSPCLK	AD23	VSUSA33USBH	AG22	VSUSA33USBH	AL12	VCCA12PEX
AB06	LVDSENBL	AD24	VSUS33	AG31	INTA# / DCD3	AL13	VCCA12PEX
AB07	LVDSENVDD	AD25	GND	AG32	AD23 / GPIO27	AL14	VCCA12PEX
AB08	GND	AD26	VSUSVDD	AG33	AD30 / GPIO34	AL15	GNDA25PEX
AB09	CRTSPD	AD30	AD6	AG34	AD29 / GPIO33	AL18	VCCA25SATA
AB14	VCC33VGA	AD31	AD0 / GPI10	AG35	AD24 / GPIO28	AL19	VCCA12SATA
AB15	GND	AD32	AD5	AG36	AD27 / GPIO31	AL20	GNDA12SATA
AB16	VDD	AD33	AD21 / GPIO25	AG37	AD11 / GPIO15	AL21	GND
AB17	GND	AD34	GPO40	AG38	AD12 / GPIO16	AL22	USBHP5+
AB18	VDD	AD35	GPO38 / PCIERST3#	**AH01**	VCPD3 / PTS0D3 / SIN0	AL23	GND
AB19	GND	AD36	GPO39	AH02	VCPD4 / PTS0D4 / DTR0	AL24	USBHP7-
AB20	VDD	AD37	MSPISS1# / GPO2	AH03	VCPD2 / PTS0D2 / SOUT0	AL25	GND
AB21	GND	AD38	MSPISS0# / GPO3	AH04	GND	AL26	USBDP+
AB22	VDD	**AE01**	DVP1VS	AH05	VCPD12 / STS1ERR	AL27	GND
AB23	GND	AE02	DVP1D1 / DCD1	AH06	VCPD14	AL30	TP6
AB24	VCC33	AE03	DVP1D2 / SOUT1	AH07	GND	AL31	PCIRST#
AB25	VCCCR	AE04	GND	AH22	VSUSA33USBH	AL32	EXTSMI# / GPI5
AB26	VSUSVDD	AE05	DVP1D11 / SIN0	AH31	GND	AL33	SUSA# / SLOWCLK / GPO7
AB30	TP3	AE06	DVP1D13 / DSR0	AH32	REQ1# / DSR3	AL34	GND
AB31	GND	AE07	DVP1D14 / RTS0	AH33	REQ0# / SIN3	AL35	AD19 / GPIO23
AB32	PERR#	AE08	DVP1D15 / CTS0	AH34	GND	AL36	FRAME# / CTS2
AB33	INTB# / GPIO8	AE09	DVP1D4 / DTR1	AH35	AD26 / GPIO30	AL37	IRDY# / DSR2
AB34	GND	AE14	VCC33VGA	AH36	AD14 / GPIO18	AL38	GND
AB35	GPIO11 / SATALED1#	AE15	VCCA25PEX	AH37	AD13 / GPIO17	**AM01**	DP2TX3-
AB36	THRM# / GPI9	AE16	VCCA25PEX	AH38	GND	AM02	GNDA25PEX
AB37	C4PSTOP# / GPO6	AE17	VCCA25PEX	**AJ01**	VCPD6 / PTS0D6 / RTS0	AM03	GNDA25PEX
AB38	AZSDOUT	AE18	VCCA25PEX	AJ02	VCPD7 / PTS0D7 / CTS0	AM04	GNDA25PEX
AC01	ROMSPD	AE19	VCCA25PEX	AJ03	VCPD5 / PTS0D5 / DSR0	AM05	GNDA25PEX
AC02	GND	AE20	VCCA25PEX	AJ04	VCPD11 / STS1CLK / RI1	AM06	GNDA25PEX
AC03	ROMSPC	AE21	VCCA25SATA	AJ05	VCPD13	AM07	GNDA12PEX

Ball #	Ball Name	Ball #	Ball Name	Ball #	Ball Name
AM08	GNDA12PEX	AP24	USBHP1+	AT31	AZSDIN1
AM09	GNDA12PEX	AP25	GND	AT32	AZSDIN0
AM10	GNDA12PEX	AP26	USBHP2+	AT33	SMBCK2 / GPIO1
AM11	GNDA12PEX	AP27	GND	AT34	SMBCK1
AM12	GNDA12PEX	AP30	PWRGD	AT35	CR_PWOFF / SDIOPWOFF / GPO12
AM13	GNDA12PEX	AP31	VBAT	AT36	CR_CD# / MMC_CD# / SD_CD# / SDIOCD#
AM14	GNDA12PEX	AP32	USBD_DET#	AT37	CR_D1 / MMC_D1 / XD_D1 / SD_D1 / SDIOD1
AM15	PEXCLK-	AP33	PME# / GPIO7	AT38	XD_ALE
AM18	GNDA25SATA	AP34	GND	**AU01**	GNDA12PEX
AM19	GNDA12SATA	AP35	RSVD	AU02	GNDA12PEX
AM20	SATACLK+	AP36	CR_D7 / MMC_D7 / XD_D7	AU03	GNDA12PEX
AM21	GND	AP37	CR_CLK / MMC_CLK / XD_WE# / SD_CLK / SDIOCLK	AU04	GNDA12PEX
AM22	USBHP5-	AP38	GND	AU05	GNDA12PEX
AM23	GND	**AR01**	DP2TX2+	AU06	GNDA12PEX
AM24	USBHP7+	AR02	GNDA25PEX	AU07	GNDA12PEX
AM25	GND	AR03	GNDA25PEX	AU08	GNDA12PEX
AM26	USBDP-	AR04	RSVD	AU09	GNDA12PEX
AM27	GND	AR05	RSVD	AU10	GNDA12PEX
AM30	GND	AR06	GNDA25PEX	AU11	PEXRX8-
AM31	SUSB# / GPO8	AR07	RSVD	AU12	GNDA12PEX
AM32	PEXWAKE# / GPI14	AR08	RSVD	AU13	PEXTX9+
AM33	SUSC# / GPO9	AR09	GNDA25PEX	AU14	PEXTX10+
AM34	CR_CMD / MMC_CMD# / XD_RB# / SD_CMD / SDIOCMD	AR10	RSVD	AU15	GNDA12PEX
AM35	CR_D3 / MMC_D3 / XD_D3 / SD_D3 / SDIOD3	AR11	PEXTX8+	AU16	PEXREXTP0
AM36	AD18 / GPIO22	AR12	GNDA25PEX	AU17	GNDA12SATA
AM37	AD17 / GPIO21	AR13	PEXRX9-	AU18	STX1+
AN01	DP2TX3+	AR14	GNDA25PEX	AU19	GNDA12SATA
AN02	RSVD	AR15	PEXRX10+	AU20	STX0+
AN03	RSVD	AR16	GNDA25PEX	AU21	GND
AN04	GNDA25PEX	AR17	GNDA25SATA	AU22	USBHP3+
AN05	GNDA25PEX	AR18	SRX1-	AU23	GND
AN06	GNDA25PEX	AR19	GNDA25SATA	AU24	USBHP0-
AN07	GNDA25PEX	AR20	SRX0-	AU25	USBHP6+
AN08	GNDA25PEX	AR21	GND	AU26	GND
AN09	GNDA25PEX	AR22	USBHP4-	AU27	USBHOC4#
AN10	GNDA25PEX	AR23	GND	AU28	USBHOC7#
AN11	GNDA12PEX	AR24	USBHP1-	AU29	USBHOC6#
AN12	GNDA12PEX	AR25	GND	AU30	RTCXI
AN13	GNDA12PEX	AR26	USBHP2-	AU31	KBDT / GPIO4 / KBC_CPURST#
AN14	GNDA12PEX	AR27	GND	AU32	AZRST#
AN15	PEXCLK+	AR28	USBHOC3#	AU33	SMBDT2 / GPIO0
AN17	SATAREXTP	AR29	GND	AU34	SMBALRT#
AN18	GNDA25SATA	AR30	GND	AU35	CR_PWSEL / SDIOPWSEL / GPO11
AN19	GNDA25SATA	AR31	INTRUDER# / GPI6	AU36	XD_RE#
AN20	GNDA25SATA	AR32	USBD_PDN / GPO10	AU37	CR_WPD / XD_WP# / SD_WPD / SDIOWPD
AN21	GND	AR33	SMBDT1	AU38	GND
AN22	GND	AR34	LID# / GPI7	**AV02**	DP2TX1+
AN23	GND	AR35	XD_CE#	AV03	DP2TX1-
AN24	GND	AR36	CR_D0 / MMC_D0 / XD_D0 / SD_D0 / SDIOD0	AV04	DP2TX0+
AN25	GND	AR37	CR_D4 / MMC_D4 / XD_D4	AV05	DP2TX0-
AN26	GND	AR38	CR_D6 / MMC_D6 / XD_D6	AV06	GNDA12PEX
AN27	GND	**AT01**	DP2TX2-	AV07	RSVD
AN30	RSMRST#	AT02	RSVD	AV08	RSVD
AN31	TP	AT03	RSVD	AV09	RSVD
AN32	GPWAKE# / GPI1	AT04	RSVD	AV10	RSVD
AN33	PWRBTN#	AT05	RSVD	AV11	PEXRX8+
AN34	BATLOW# / GPI4	AT06	RSVD	AV12	GNDA12PEX
AN35	CR_D5 / MMC_D5 / XD_D5	AT07	GNDA25PEX	AV13	PEXTX9-
AN36	CR_D2 / MMC_D2 / XD_D2 / SD_D2 / SDIOD2	AT08	RSVD	AV14	PEXTX10-
AP01	GNDA12PEX	AT09	RSVD	AV15	GNDA12PEX
AP02	RSVD	AT10	GNDA25PEX	AV17	GNDA12SATA
AP03	RSVD	AT11	PEXTX8-	AV18	STX1-
AP04	GNDA25PEX	AT12	GNDA25PEX	AV19	GNDA12SATA
AP05	RSVD	AT13	PEXRX9+	AV20	STX0-
AP06	GNDA25PEX	AT14	GNDA25PEX	AV21	GND
AP07	RSVD	AT15	PEXRX10-	AV22	USBHP3-
AP08	RSVD	AT16	GNDA25PEX	AV23	GND
AP09	GNDA25PEX	AT17	GNDA25SATA	AV24	USBHP0+
AP10	RSVD	AT18	GNDA25SATA	AV25	USBHP6-
AP11	GNDA25PEX	AT19	GNDA25SATA	AV26	GND
AP12	GNDA25PEX	AT20	GNDA25SATA	AV27	USBHOC1#
AP13	GNDA25PEX	AT21	GND	AV28	USBHOC0#
AP14	GNDA25PEX	AT22	GND	AV29	RTCXO
AP15	GNDA25PEX	AT23	GND	AV30	MSCK / GPIO3
AP17	GNDA25SATA	AT24	GND	AV31	KBCK / GPIO5 / A20GATE
AP18	SRX1+	AT25	GND	AV32	GND
AP19	GNDA25SATA	AT26	GND	AV35	RING# / GPI8
AP20	SRX0+	AT27	GND	AV36	XD_CD#
AP21	GND	AT28	USBHOC5#	AV37	XD_CLE
AP22	USBHP4+	AT29	USBHOC2#		
AP23	GND	AT30	MSDT / GPIO2		

Table 6. VX900 Series Power / Ground Ball List

Ball Name	Ball Numbers
GND	A03, A07, A11, A15, A19, A23, A27, A31, A35, B01, B05, B09, B13, B17, B21, B25, B29, B33, B37, C04, C08, C12, C16, C20, C24, C28, C32, C36, D02, D06, D10, D14, D18, D22, D26, D30, D34, D38, E03, E07, E11, E15, E19, E23, E27, E31, E35, F01, F05, F09, F13, F17, F21, F25, F29, F33, F37, G04, G08, G12, G16, G20, G24, G28, G32, G36, H02, H06, H10, H14, H18, H22, H26, H30, H34, H38, J02, J05, J06, J33, J37, K01, K03, K04, K05, K06, K35, L06, L34, L38, M01, M04, M06, M32, M36, N03, N04, N05, N06, N16, N18, N20, N22, N24, N26, N33, N37, P03, P05, P06, P15, P17, P19, P21, P23, P25, P31, P35, R01, R05, R14, R16, R18, R20, R22, R24, R26, R34, R38, T03, T04, T05, T06, T14, T17, T19, T21, T23, T25, T32, T36, U16, U18, U20, U22, U24, U26, U33, U37, V15, V17, V19, V21, V23, V25, V31, V35, W08, W16, W18, W20, W22, W34, W38, Y05, Y17, Y19, Y21, Y23, Y24, Y32, Y36, AA14, AA16, AA18, AA20, AA22, AB08, AB15, AB17, AB19, AB21, AB23, AB31, AB34, AC02, AC14, AC16, AC18, AC20, AC22, AC24, AC26, AC38, AD06, AD25, AE04, AE31, AE34, AE38, AF03, AF08, AG06, AG09, AH04, AH07, AH31, AH34, AH38, AJ06, AK21, AK22, AK23, AK24, AK25, AK26, AL21, AL23, AL25, AL27, AL34, AL38, AM21, AM23, AM25, AM27, AM30, AN21, AN22, AN23, AN24, AN25, AN26, AN27, AP21, AP23, AP25, AP27, AP34, AP38, AR21, AR23, AR25, AR27, AR29, AR30, AT21, AT22, AT23, AT24, AT25, AT26, AT27, AU21, AU23, AU26, AU38, AV21, AV23, AV26, AV32
GNDA12DP1	Y11, Y12, Y13
GNDA12PEX	AD17, AD19, AL01, AM07, AM08, AM09, AM10, AM11, AM12, AM13, AM14, AN11, AN12, AN13, AN14, AP01, AU01, AU02, AU03, AU04, AU05, AU06, AU07, AU08, AU09, AU10, AU12, AU15, AV06, AV12, AV15
GNDA12SATA	AF21, AL20, AM19, AU17, AU19, AV17, AV19
GNDA25DP1	T02, U02, U04, V02, V04, W02, W04, W13, Y02, Y04, AA02, AA03
GNDA25HCK	J16
GNDA25PEX	AF15, AF17, AF19, AK02, AK03, AK04, AK05, AL04, AL06, AL15, AM02, AM03, AM04, AM05, AM06, AN04, AN05, AN06, AN07, AN08, AN09, AN10, AP04, AP06, AP09, AP11, AP12, AP13, AP14, AP15, AR02, AR03, AR06, AR09, AR12, AR14, AR16, AT07, AT10, AT12, AT14, AT16
GNDA25SATA	AG21, AM18, AN18, AN19, AN20, AP17, AP19, AR17, AR19, AT17, AT18, AT19, AT20
VCC33	W24, W25, W26, Y25, Y26, AA24, AA25, AB24
VCC33VGA	AA15, AB14, AC15, AD14, AE14
VDD	T16, T18, T20, T22, U17, U19, U21, U23, V16, V18, V20, V22, W17, W19, W21, W23, Y16, Y18, Y20, Y22, AA17, AA19, AA21, AA23, AB16, AB18, AB20, AB22, AC17, AC19, AC21, AC23
VSUS33	AC25, AD24
VSUSVDD	AB26, AD26, AE26
VSUSVDDMEM	R30, V29
VSUSIOMEM	N21, N23, N25, P22, P24, P26, R21, R23, R25, T24, T26, U25, V24, V26
VTT	N15, N17, N19, P14, P16, P18, P20, R15, R17, R19

Signal Descriptions

CPU Interface

CPU Interface				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
HCLK+/–	J17, J18	IO	**Host Clock.** *100 / 133 / 166 / 200 MHz*	**VTT**
HA[16:3]# **HAHI[1:0]#**	(see ball lists)	IO	**Host CPU Address Bus.**	**VTT**
HREQ[2:0]#	B18 E18 F18	IO	**Host Request Command.** Signal balls HREQ[2:0]# are used. Host request commands are transferred in 4X rate in V4 host protocol. On beat 0 and 2, host request bits HREQ[2:0]# are transferred. On beat 1 and 3, host request bits HREQ[4:3]# are transferred on signal balls.	**VTT**
HADSTB0P# **HADSTB0N#**	D20 E20	IO	**Host Address Strobe.** HADSTB0P# / HADSTB0N# are negative-edge going strobes used to latch HAHI[1:0]#, HA[16:3]# and HREQ[2:0]# on even and odd data beat transfers respectively.	**VTT**
HABI#	F20	IO	**Address Bus Inversion.** When this signal is asserted, the address and request signals are of inverted sense.	**VTT**
HD[63:0]#	(see ball lists)	IO	**Host Data.** These signals are connected to the CPU data bus.	**VTT**
HDBI[3:0]#	G02 C05 B08 G10	IO	**Host CPU Dynamic Bus Inversion.** Driven along with HD[63:0]# to indicate if the associated signals are inverted or not. Used to limit the number of simultaneously switching signals to 8 for the associated 16-bit data pin group. HDBI[0]# governs the polarity of HD[15:0]#. HDBI[1]# governs the polarity of HD[31:16]#. HDBI[2]# governs the polarity of HD[47:32]#. HDBI[3]# governs the polarity of HD[63:48]#.	**VTT**
HDSTB[3:0]P# **HDSTB[3:0]N#**	(see ball lists)	IO	**Host Data Strobes.** Source synchronous strobes used to transfer HD[63:0]# & HDBI[3:0]# at a 4x transfer rate. HD[15:0]# are grouped with HDSTB[0]N#, HDSTB[0]P# and HDBI[0]#. HD[31:16]# are grouped with HDSTB[1]N#, HDSTB[1]P# and HDBI[1]#. HD[47:32]# are grouped with HDSTB[2]N#, HDSTBP[2]P# and HDBI[2]#. HD[63:48]# are grouped with HDSTB[3]N#, HDSTBP[3]P# and HDBI[3]#.	**VTT**

CPU Interface (continued)				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
CPURST#	F14	O	**CPU Reset.** Reset output to CPU.	**VTT**
HADS#	G18	IO	**Address Strobe.** The CPU asserts HADS# in T1 of the CPU bus cycle.	**VTT**
HBNR#	F15	IO	**Block Next Request.** Used to block the current request bus owner from issuing new requests. This signal is used to dynamically control the processor bus pipeline depth.	**VTT**
HBPRI#	D16	IO	**Priority Agent Bus Request.** The owner of this signal will always be the next bus owner. This signal has priority over symmetric bus requests and causes the current symmetric owner to stop issuing new transactions unless the HLOCK# signal is asserted.	**VTT**
HDBSY#	E17	IO	**Data Bus Busy.** Used by the data bus owner to hold the data bus for transfers requiring more than one cycle.	**VTT**
HDEFER#	C17	IO	**Defer.** A dynamic deferring policy is used to optimize system performance. The signal is also used to indicate a processor retry response.	**VTT**
HDRDY#	F16	IO	**Data Ready.** Asserted for each cycle that data is transferred.	**VTT**
HHIT#	G17	IO	**Hit.** Indicates that a caching agent holds an unmodified version of the requested line. Also driven in conjunction with HHITM# by the target to extend the snoop window.	**VTT**
HHITM#	E16	IO	**Hit Modified.** Asserted by the CPU to indicate that the address is modified in the L1 cache and needs to be written back.	**VTT**
HLOCK#	D15	I	**Host Lock.** All CPU cycles sampled with the assertion of HLOCK# and ADS# until the negation of HLOCK# must be atomic.	**VTT**
HTRDY#	D17	O	**Host Target Ready.** Indicates that the target of the processor transaction is able to enter the data transfer phase.	**VTT**
HRS[1:0]#	H16 G15	O	**Response Signals.** Indicates the type of response per the table below: **HRS[1:0]#** — **Response type** 00 — Idle State 01 — Retry Response 10 — Defer Response 11 — Normal State	**VTT**
HBREQ0#	G21	IO	**Bus Request 0.** Connect to CPU bus request 0.	**VTT**
HALF#	G19	I	**Dynamic FSB Frequency Switching Mode.** Allows the processor to operate at lower frequencies and provides very fast transitions between full and half speed modes.	**VTT**
HDPWR#	B12	O	**Data Bus Power Reduction.** Request to reduce power on the mobile CPU data bus input buffer. HIGH will disable the CPU data bus input buffer.	**VTT**

CPU Control Interface				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
A20M#	C15	O	**A20 Mask.** Connect to A20 mask input of the CPU to control address bit-20 generation. Logical combination of the A20GATE input (from internal or external keyboard controller) and Port92 bit-1 (Fast_A20).	**VTT**
FERR#	B16	I	**Numerical Coprocessor Error.** This signal is tied to the coprocessor error signal on the CPU. Internally generates interrupt 13 if active.	**VTT**
IGNNE#	A17	O	**Ignore Numeric Error.** This signal is connected to the CPU "ignore error" signal.	**VTT**
INIT#	B14	OD	**Initialization.** INIT# is asserted if a shut-down special cycle on the PCI bus is detected or if a soft reset is initiated by the register.	**VTT**
INTR	A16	OD	**CPU Interrupt.** INTR is driven by the VX900 series to signal the CPU that an interrupt request is pending and needs service.	**VTT**
NMI	B15	OD	**Non-Maskable Interrupt.** NMI is used to force a non-maskable interrupt to the CPU.	**VTT**
SMI#	C14	O	**System Management Interrupt.** SMI# is asserted by VX900 series to the CPU in response to power management events.	**VTT**
THRMTRIP#	C13	I	**Thermal Detect Power Down.** This signal indicates a thermal trip from the processor.	**VTT**
STPCLK#	A14	O	**Stop Clock.** This signal is asserted by the VX900 series to throttle the processor clock.	**VTT**
SLP#	A13	O	**Sleep.** Used to put the CPU into a sleep state.	**VTT**
DPSLP#	E14	O	**CPU Deep Sleep.** Used to put the CPU into a deeper sleep mode.	**VTT**
NAP#	A12	O	**CPU NAP State.** Connected to the NAP# of CPU. The assertion causes the processor to initiate a minimum P state by sending the VID targeting to the minimum operation voltage in C4 state to CPU voltage regulator.	**VTT**

System Memory Interface (DDR2 / DDR3)

System Memory Interface				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
MD[63:0]	(see ball lists)	IO	**Memory Data.** MD[7:0] are grouped with MDQM[0] and MDQS[0]+/–. MD[15:8] are grouped with MDQM[1] and MDQS[1]+/–. MD[23:16] are grouped with MDQM[2] and MDQS[2]+/–. MD[31:24] are grouped with MDQM[3] and MDQS[3]+/–. MD[39:32] are grouped with MDQM[4] and MDQS[4]+/–. MD[47:40] are grouped with MDQM[5] and MDQS[5]+/–. MD[55:48] are grouped with MDQM[6] and MDQS[6]+/–. MD[63:56] are grouped with MDQM[7] and MDQS[7]+/–.	**VSUSIOMEM**
MDQM[7:0]	(see ball lists)	O	**Memory Data Mask.**	**VSUSIOMEM**
MDQS[7:0]+/–	(see ball lists)	IO	**Memory Data Strobes.**	**VSUSIOMEM**
MODT[3:0]	(see ball lists)	O	**Memory On-Die Termination Enable.**	**VSUSIOMEM**
MCKE[3:0]	(see ball lists)	O	**Memory Clock Enable.**	**VSUSIOMEM**
MCS[3:0]#	(see ball lists)	O	**Memory Chip Select.**	**VSUSIOMEM**
MA[15:0]	(see ball lists)	O	**DRAM Row/Column Address.**	**VSUSIOMEM**
MBA[2:0]	K38 D36 B36	O	**DRAM Bank Address.**	**VSUSIOMEM**
MSRAS#	A37	O	**DRAM Row Address Strobe.**	**VSUSIOMEM**
MSCAS#	C34	O	**DRAM Column Address Strobe.**	**VSUSIOMEM**
MSWE#	E34	O	**DRAM Write Enable.**	**VSUSIOMEM**
MCLKO[5:0]+/-	(see ball lists)	O	**Differential Memory Clock Output.**	**VSUSIOMEM**

System Memory Interface – Miscellaneous				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
MEMDET	H33	I	**DDR2 / DDR3 Memory Detect.**	**VSUSIOMEM**
MEMRESET#	H32	O	**DDR3 Reset Signal.**	**VSUSIOMEM**
MEMPWROK	K36	I	**Power OK.**	**VSUSIOMEM**

PCI Express Interface

PCI Express Interface is multiplexed with *Display Port 2 interface.*

PCI Express Interface				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
VX900 Only **PEXTX[7:0]+/-**	(see ball lists)	O	**PCI Express Differential Transmit Pair for Port 0.** Supports link width: x8. *PEXTX[3:0]+/- are multiplexed with* DP2TX[0:3]+/-.	**VCCA25PEX**
VX900 Only **PEXRX[7:0]+/-**	(see ball lists)	I	**PCI Express Differential Receive Pair for Port 0.** Supports link width: x8.	**VCCA25PEX**
PEXTX[10:8]+/-	(see ball lists)	O	**PCI Express Differential Transmit Pair for Port 1-3.** Supports link width: PE1: x2, PE2-PE3: x1**.**	**VCCA25PEX**
PEXRX[10:8]+/-	(see ball lists)	I	**PCI Express Differential Receive Pair for Port 1-3.** Supports link width: PE1: x2, PE2-PE3: x1	**VCCA25PEX**
PEXCLK+/-	AN15, AM15	I	**PCI Express Clock.** These signals receive the 100 MHz clock used by the internal PCI Express logic. Multiplied up to 2.5 GHz on-chip for use by the integrated PCI Express PHY to transmit / receive data.	**VCCA25PEX**
PEXREXTP0	AU16	AI	**PCI Express Port External Resistor.** This signal needs an external 3.09K 1% ohm pull down resistor to GND.	**VCCA25PEX**
PCIERST1# / GPO36	AC34	O	**PCI Express Reset 1** This pin is configured by the GPO36 register. If GPO36 is not used, it can be PCI Express Reset function while strapping function is not affected.	**VCC33**
PCIERST2# / GPO37	AE36	O	**PCI Express Reset 2** This pin is configured by the GPO37 register. If GPO37 is not used, it can be PCI Express Reset function while strapping function is not affected.	**VCC33**
PCIERST3# / GPO38	AD35	O	**PCI Express Reset 3** This pin is configured by the GPO38 register. If GPO38 is not used, it can be PCI Express Reset function while strapping function is not affected.	**VCC33**

Note: The I/O attribute "AI" stands for Analog Input.

CRT Interface

CRT Interface				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
CRTAR **CRTAG** **CRTAB**	L03 L01 L02	AO	**Analog Red / Green / Blue.** DAC outputs.	**VCCA25DAC**
CRTHSYNC	AA08	O	**Horizontal Sync.**	**VCC33VGA**
CRTVSYNC	AA09	O	**Vertical Sync.**	**VCC33VGA**
CRTRSET	K02	AI	**Reference Resistor.** Tie to GND through an external resistor 174 1% ohm to control the RAMDAC full-scale current.	**VCCA25DAC**
CRTSPCLK	AA10	IO	**I^2C Clock to CRT.**	**VCC33VGA**
CRTSPD	AB09	IO	**I^2C Data to CRT.**	**VCC33VGA**

Integrated LVDS Interface

LVDS Interface				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
LVDSD[3:0]+/–	(see ball list)	O	**LVDS Differential Data.** Supports Single Channel Mode.	**VCCA25LVDS**
LVDSCLK+/–	N01, N02	O	**LVDS Differential Clock.**	**VCCA25LVDS**

LCD Panel Power and Brightness Control

LCD Panel Power and Brightness Control				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
LVDSENVDD	AB07	O	**Enable Panel VDD Power.**	**VCC33VGA**
LVDSENBL	AB06	O	**Enable Panel Back Light.**	**VCC33VGA**
LVDSPWM	AA07	O	**LVDS Backlight Strength Control.** PWM output.	**VCC33VGA**

Display Port Interface

Display Port 1 (DP1): This Interface is multiplexed with *HDMI interface*.

Display Port 1				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
DP1TX[2:0]+/- HDMITX[0:2]+/-	(see ball lists)	O	**Display Port 1 Lane 2-0.**	**VCCA25DP1**
DP1TX3+/- HDMICLK+/-	V03, U03	O	**Display Port 1 Lane 3.**	**VCCA25DP1**
DP1_AUX+/-	U01, T01	IO	**Display Port 1 Differential Half-duplex Bi-direction Auxiliary Channel.**	**VCCA25DP1**
DP1_HPD#	W06	I	**Display Port 1 Hot Plug Detect.**	**VCCA25DP1**
DP1_REXT	W05	I	**Display Port External Resistor**. Connect to external resistor. This signal needs an external 6.04K 1% ohm pull down resistor.	**VCCA25DP1**

Display Port 2 (DP2): **VX900** – Multiplexed with *PCI Express interface.*
VX900M – Dedicated DP.

Display Port 2				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
DP2TX[3:0]+/- PEXTX[0:3]+/-	(see ball lists)	O	**Display Port 2 Lane 3-0.**	**VCCA25PEX**
DP2_AUX+/-	AL03, AL02	IO	**Display Port 2 Differential Half-duplex Bi-direction Auxiliary Channel.**	**VCCA25PEX**
DP2_HPD#	AL05	I	**Display Port 2 Hot Plug Detect.**	**VCCA25PEX**

Display Port Clock Signal				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
DPCLK	Y07	I	**Display Port Clock.** 27 MHz.	**VCC33VGA**

Multiplexed Display Interface - HDMI Interface

This HDMI Interface is multiplexed with *Display Port 1 (DP1) interface*.

HDMI Interface				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
HDMITX[2:0]+/- DP1TX[0:2]+/-	(see ball lists)	O	**HDMI Data.**	**VCCA25DP1**
HDMICLK+/- DP1TX3+/-	V03, U03	O	**HDMI Clock.**	**VCCA25DP1**
HDMI I^2C Clock Signals				
HDMIRSPC	AB01	IO	**I^2C Clock to HDMI Receiver.**	**VCC33VGA**
HDMIRSPD	AB02	IO	**I^2C Data to HDMI Receiver.**	**VCC33VGA**
HDMI SEEPROM I^2C Clock Signals				
ROMSPC	AC03	IO	**I^2C Clock to HDCP SEEPROM.**	**VCC33VGA**
ROMSPD	AC01	IO	**I^2C Data to HDCP SEEPROM.**	**VCC33VGA**

Video Capture Port Interface (VCP)

VCP interface is multiplexed with *Transport Stream and PCI UART ports (COM0 and COM1)*. Please refer to the table "Multiplexed Signals of VCP" for detail multiplex pin assignment.

Video Capture Mode				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
VCPD[7:0]	(see ball list)	I	**Video Capture Port Data [7:0] of 8-bit CCIR-601/656 Port or lower half of 16-bit CCIR-601/656 Port.**	**VCC33VGA**
VCPD8	AF05	I	**Video Capture Port Data 8 of 16-bit CCIR-601/656 Port.**	**VCC33VGA**
VCPD9	AG04	I	**Video Capture Port Data 9 of 16-bit CCIR-601/656 Port.**	**VCC33VGA**
VCPD10	AG05	I	**Video Capture Port Data 10 of 16-bit CCIR-601/656 Port.**	**VCC33VGA**
VCPD11	AJ04	I	**Video Capture Port Data 11 of 16-bit CCIR-601/656 Port.**	**VCC33VGA**
VCPD12	AH05	I	**Video Capture Port Data 12 of 16-bit CCIR-601/656 Port.**	**VCC33VGA**
VCPD13	AJ05	I	**Video Capture Port Data 13 of 16-bit CCIR-601/656 Port.**	**VCC33VGA**
VCPD14	AH06	I	**Video Capture Port Data 14 of 16-bit CCIR-601/656 Port.**	**VCC33VGA**
VCPD15	AG08	I	**Video Capture Port Data 15 of 16-bit CCIR-601/656 Port.**	**VCC33VGA**
VCPHS	AF02	I	**Video Capture Port Horizontal Sync.**	**VCC33VGA**
VCPVS	AG02	I	**Video Capture Port Vertical Sync.**	**VCC33VGA**
VCPCLK	AG07	I	**Video Capture Port Clock.**	**VCC33VGA**

Transport Stream Input Mode				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
PTS0D[7:0]	(see ball list)	I	**Parallel Transport Stream Port 0 Data [7:0].**	**VCC33VGA**
PTS0ERR	AF05	I	**Parallel Transport Stream Port 0 Error.**	**VCC33VGA**
PTS0VLD	AF02	I	**Parallel Transport Stream Port 0 Data Valid.**	**VCC33VGA**
PTS0SYNC	AG02	I	**Parallel Transport Stream Port 0 Data Sync.**	**VCC33VGA**
PTS0CLK	AG07	I	**Parallel Transport Stream Port 0 Clock.**	**VCC33VGA**
STS1VLD	AG04	I	**Serial Transport Stream Port 1 Data Valid.**	**VCC33VGA**
STS1SYNC	AG05	I	**Serial Transport Stream Port 1 Data Sync.**	**VCC33VGA**
STS1CLK	AJ04	I	**Serial Transport Stream Port 1 Clock.**	**VCC33VGA**
STS1ERR	AH05	I	**Serial Transport Stream Port 1 Error.**	**VCC33VGA**
STS1D	AG08	I	**Serial Transport Stream Port 1 Data.**	**VCC33VGA**

Digital Video Output Port 1 (DVP1) Interface

DVP1 interface is multiplexed with *PCI UART Interface (COM0 & COM1)*. Please refer to the table "Multiplexed Signals of DVP1" for detail multiplex pin assignment. This DVP port supports video output through LVDS Transmitter / DVI Transmitter / HDMI Transmitter / TV Encoder. Please refer to the "Digital Video Port 1 (DVP1) – Display Interface Configurations" in the following section for detailed pin mapping assignment.

Digital Video Port 1 (DVP1) Interface				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
DVP1D[15:0]	(see ball lists)	O	**12-Bit Digital Video Output Mode:** DVP1D[11:0] is the data for 12-Bit DVO Interface. **18-Bit TTL Panel Interface Mode:** DVP1D[15:0] is the TTL Panel Data [15:0]. **20-Bit TV Output Panel Interface Mode:** DVP1D[15:0] is the first 16 bits of the TV Interface. Multiplexed with COM0 and COM1 ports, refer to multiplexed tables listed later for details.	**VCC33VGA**
DVP1HS DVP1D17	AD04	O	**12-Bit Digital Video Output Mode:** DVP1HS is Digital Video Port 1 Horizontal Sync. **18-Bit TTL Panel Interface Mode:** DVP1HS is the TTL Panel Horizontal Sync. **20-Bit TV Output Panel Interface Mode:** DVP1D[17] is the 18th bit of the TV Interface.	**VCC33VGA**
DVP1VS DVP1D16	AE01	O	**12-Bit Digital Video Output Mode:** DVP1VS is Digital Video Port 1 Vertical Sync. **18-Bit TTL Panel Interface Mode:** DVP1VS is the TTL Panel Vertical Sync. **20-Bit TV Output Panel Interface Mode:** DVP1D[16] is the 17th bit of the TV Interface.	**VCC33VGA**
DVP1DE DVP1D19	AF07	O	**12-Bit Digital Video Output Mode:** DVP1DE is Digital Video Port 1 Data Enable. **18-Bit TTL Panel Interface Mode:** DVP1DE is the TTL Panel Data Enable. **20-Bit TV Output Panel Interface Mode:** DVP1D[19] is the 20th bit of the TV Interface.	**VCC33VGA**
DVP1CLK	AD01	O	**12-Bit Digital Video Output Mode:** DVP1CLK is Digital Video Port 1 Clock. **18-Bit TTL Panel Interface Mode:** DVP1CLK is the TTL Panel Clock. **20-Bit TV Output Panel Interface Mode:** DVP1CLK is the TV Clock of the TV Interface.	**VCC33VGA**

Digital Video Port 1 (DVP1) Interface (continued)				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
DVP1TVCLKR DVP1DET	AD02	I	**12-Bit Digital Video Output Mode:** For external TV encoder: DVP1TVCLKR is the TV Return Clock. For external DVI transmitter: DVP1TVCLKR is the Display Detect. **18-Bit TTL Panel Interface Mode:** DVP1TVCLKR is the TTL Panel Data 16. **20-Bit TV Output Panel Interface Mode:** DVP1DET is the Display Detect signal of the TV Interface.	**VCC33VGA**
DVP1TVFLD DVP1D18	AF06	IO	**12-Bit Digital Video Output Mode:** For external TV encoder: DVP1TVFLD is TV Field Out. **18-Bit TTL Panel Interface Mode:** DVP1TVFLD is the TTL Panel Data 17. **20-Bit TV Output Panel Interface Mode:** DVP1D[18] is the 19th bit of the TV Interface.	**VCC33VGA**
DVPSPCLK	AB05	IO	**I^2C Clock to DVP1.**	**VCC33VGA**
DVPSPD	AB04	IO	**I^2C Data to DVP1.**	**VCC33VGA**
DVI Control Signal				
DVICTL3	AB03	IO	**DVI Control Signal 3 for External TMDS Transmitter.**	**VCC33VGA**

PCI Bus Interface

PCI interface is multiplexed with *PCI UART interface (COM2 & COM3)*.

PCI Bus Interface				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
AD[31:0]	(see ball list)	IO	**Address / Data Bus.** Multiplexed address and data. The address is driven with FRAME# assertion and data is driven or received in following cycles. AD0 is multiplexed with GPI10. AD1 is multiplexed with GPI11. AD4 is multiplexed with GPO4. AD[31:9] is multiplexed with GPIO[35:13].	**VCC33**
CBE3# / SOUT2 **CBE2#** / DCD2 **CBE1#** / RI2 **CBE0#** / CTS3	AF32 AK33 AJ35 AE33	IO	**Command / Byte Enable.** The command is driven with FRAME# assertion. Byte enables corresponding to supplied or requested data are driven on following clocks.	**VCC33**
DEVSEL# / SIN2	AK36	IO	**Device Select.** This signal is asserted claim PCI transactions through positive or subtractive decoding. As an input, DEVSEL# indicates the response to a VX900 series initiated transaction and is also sampled when decoding whether to subtractively decode the cycle. This signal has a programmable internal 3.3K ohm pull-up resistor (default enable, D17F7 Rx55[0]).	**VCC33**
FRAME# / CTS2	AL36	IO	**Frame.** Assertion indicates the address phase of a PCI transfer. Negation indicates that one additional data transfer is desired by the cycle initiator. This signal has a programmable internal 10K ohm pull-up resistor (default enable, D17F7 Rx55[0]).	**VCC33**
IRDY# / DSR2	AL37	IO	**Initiator Ready.** Asserted when the initiator is ready for data transfer. This signal has a programmable internal 10K ohm pull-up resistor (default enable, D17F7 Rx55[0]).	**VCC33**
TRDY# / RTS2	AK35	IO	**Target Ready.** Asserted when the target is ready for data transfer. This signal has a programmable internal 10K ohm pull-up resistor (default enable, D17F7 Rx55[0]).	**VCC33**
STOP# / DTR2	AK34	IO	**Stop.** Asserted by the target to request the master to stop the current transaction. This signal has a programmable internal 10K ohm pull-up resistor (default enable, D17F7 Rx55[0]).	**VCC33**
PAR / DTR3	AJ36	IO	**Parity.** A single parity bit is provided over AD[31:0] and CBE[3:0]#.	**VCC33**
PERR#	AB32	IO	**Parity Error.** PERR#, sustained tri-state, is only for the reporting of data parity errors during all PCI transactions except a Special Cycle. This signal has an internal 10K ohm pull-up resistor.	**VCC33**
SERR# / RI3	AJ32	I	**System Error.** SERR# is for the reporting of address parity errors, data parity errors on a Special Cycle command or any other system error. . This signal has a programmable internal 3.3K ohm pull-up resistor (default enable, D17F7 Rx55[0]).	**VCC33**

PCI Bus Interface (continued)				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
INTA# / DCD3 **INTB#** / GPIO8 **INTC#** / GPIO9 **INTD#** / GPIO12	AG31 AB33 AA31 Y34	I	**PCI Interrupt Request**. BIOS settings must match the physical connection method. Please refer to D17F0 Rx55-57 for details of PCI PnP interrupt routing setting. This signal has an internal 10K ohm pull-up resistor.	**VCC33**
REQ1# / DSR3 **REQ0#** / SIN3	AH32, AH33	I	**PCI Request.** These signals connect to the VX900 series from each PCI slot (or each PCI master) for access request to the PCI bus. These signals have an internal 10K ohm pull-up resistors.	**VCC33**
GNT1# / RTS3 **GNT0#** / SOUT3	AJ31, AJ33	O	**PCI Grant.** These signals are driven by the VX900 series to grant PCI bus access to a specific PCI master.	**VCC33**
PCIRST#	AL31	O	**PCI Reset.** This signal is used to reset devices attached to the PCI bus. The rising edge of this signal and PWRGD are used to sample power-up strap options.	**VSUS33**
PCICLK	AA33	I	**PCI Clock.** This signal provides timing for all transactions on the PCI Bus. This clock is necessary even if the system does not need PCI interface.	**VCC33**

USB Device Mode

One USB Device Port				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
USBDP+/–	AL26, AM26	IO	**USB Device Port Differential Data.**	**VCCA33USBD**
USBDREXT	AJ24	AI	**USB Device External Resistor** This signal needs an external 6.04K 1% ohm pull-down resistor. If the USB device interface is not needed, leave it unconnected.	**VCCA33USBD**
USBD_PDN GPO10	AR32	O	**USB Device Port Power Down Indicator** In USB device mode, this signal will be used to power on USB device PHY power. If the USB device mode is disabled, this pin can be used as GPO10 by register setting.	**VCC33**
USBD_DET#	AP32	I	**USB Device Port Attached to USB Host Detection Signal** This active low signal indicates a detection event while the USB device port of this chip is plugged into other USB host port, which will generate an USB wakeup event in a suspend state (S1/S3/S4/S5).	**VSUS33**

USB Interface

USB Interface				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
USBHP0+/–	AV24, AU24	IO	**USB Host Port 0 Differential Data.** This signal has an internal 15K ohm pull-down resistor.	**VSUSA33USBH**
USBHP1+/–	AP24, AR24	IO	**USB Host Port 1 Differential Data.** This signal has an internal 15K ohm pull-down resistor.	**VSUSA33USBH**
USBHP2+/–	AP26, AR26	IO	**USB Host Port 2 Differential Data.** This signal has an internal 15K ohm pull-down resistor.	**VSUSA33USBH**
USBHP3+/–	AU22, AV22	IO	**USB Host Port 3 Differential Data.** This signal has an internal 15K ohm pull-down resistor.	**VSUSA33USBH**
USBHP4+/–	AP22, AR22	IO	**USB Host Port 4 Differential Data.** This signal has an internal 15K ohm pull-down resistor.	**VSUSA33USBH**
USBHP5+/–	AL22, AM22	IO	**USB Host Port 5 Differential Data.** This signal has an internal 15K ohm pull-down resistor.	**VSUSA33USBH**
USBHP6+/–	AU25, AV25	IO	**USB Host Port 6 Differential Data.** This signal has an internal 15K ohm pull-down resistor.	**VSUSA33USBH**
USBHP7+/–	AM24, AL24	IO	**USB Host Port 7 Differential Data.** This signal has an internal 15K ohm pull-down resistor.	**VSUSA33USBH**
USBCLK	AA34	I	**USB Host Clock.** 48 MHz clock input for the USB and HD Audio. This signal needs an external 22 ohm serial damping resistor. If USB and HD Audio interfaces are not used, leave it unconnected.	**VCC33**
USBHOC0#	AV28	I	**USB Host Port 0 Over Current Detect.** Port 0 is disabled if low.	**VSUSA33USBH**
USBHOC1#	AV27	I	**USB Host Port 1 Over Current Detect.** Port 1 is disabled if low.	**VSUSA33USBH**
USBHOC2#	AT29	I	**USB Host Port 2 Over Current Detect.** Port 2 is disabled if low.	**VSUSA33USBH**
USBHOC3#	AR28	I	**USB Host Port 3 Over Current Detect.** Port 3 is disabled if low.	**VSUSA33USBH**
USBHOC4#	AU27	I	**USB Host Port 4 Over Current Detect.** Port 4 is disabled if low.	**VSUSA33USBH**
USBHOC5#	AT28	I	**USB Host Port 5 Over Current Detect.** Port 5 is disabled if low.	**VSUSA33USBH**
USBHOC6#	AU29	I	**USB Host Port 5 Over Current Detect.** Port 5 is disabled if low.	**VSUSA33USBH**
USBHOC7#	AU28	I	**USB Host Port 5 Over Current Detect.** Port 5 is disabled if low.	**VSUSA33USBH**
USBHREXT	AJ22	AI	**USB External Resistor.** This signal needs an external 6.04K 1% ohm pull-down resistor. If USB interface is not needed, leave it unconnected.	**VSUSA33USBH**

SATA Interface

SATA Interface				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
SRX0+/–	AP20, AR20	I	**SATA Port 0 Differential Receiver.**	**VCCA25SATA**
SRX1+/–	AP18, AR18	I	**SATA Port 1 Differential Receiver.**	**VCCA25SATA**
STX0+/–	AU20, AV20	O	**SATA Port 0 Differential Transmitter.**	**VCCA25SATA**
STX1+/–	AU18, AV18	O	**SATA Port 1 Differential Transmitter.**	**VCCA25SATA**
SATALED0# GPIO10	AA32	O	**SATA LED for Port 0.**	**VCC33**
SATALED1# GPIO11	AB35	O	**SATA LED for Port 1.**	**VCC33**
SATAREXTP	AN17	AI	**External Resistor Positive Terminal.** This signal needs an external 3K ohm 1% pull-down resistor.	**VCCA25SATA**
SATACLK+	AM20	I	**SATA Reference Clock.** 100 MHz.	VCCA25SATA

Card Reader Interface

Card Reader is multiplexed with either: *Multi Media Card, xD Card, Secure Digital and SDIO Interface.*

Card Reader Interface					
Signal Name	**Mux Signal**	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
CR_D[7:4]	MMC_D[7:4] XD_D[7:4]	AP36 AR38 AN35 AR37	IO	**Card Reader Data.**	**VCCCR**
CR_D[3:0]	MMC_D[3:0] XD_D[3:0] SD_D[3:0] SDIOD[3:0]	AM35 AN36 AT37 AR36	IO	**Card Reader Data.**	**VCCCR**
CR_CLK	MMC_CLK XD_WE# SD_CLK SDIOCLK	AP37	O	**Card Reader Clock.**	**VCCCR**
CR_CD#	MMC_CD# SD_CD# SDIOCD#	AT36	I	**Card Detection.** This active low signal indicates a detection event when the card is inserted.	**VSUS33**
CR_CMD	MMC_CMD# XD_RB# SD_CMD SDIOCMD	AM34	IO	**Card Reader Command / Response.**	**VCCCR**
CR_WPD	XD_WP# SD_WPD SDIOWPD	AU37	IO	**SD/MMC Card Write Protect Detection.** This signal will keep at high level if it is not connected. L: Disable write protection. Write operation is allowed. H: Enable write protection	**VCCCR**
CR_PWSEL	SDIOPWSEL GPO11	AU35	O	**Card Reader Power Select.**	**VSUS33**
CR_PWOFF	SDIOPWOFF GPO12	AT35	O	**Card Power Off.** This signal controls the delivery of power to card. L: On H: Off	**VSUS33**

Note: For more information on MS/MS Pro card support, please contact VIA.

Multi Media Card Interface

Multi Media Card Interface is multiplexed with *Card Reade, xD Card and SDIO Interface*.

Multi Media Card Interface				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
MMC_D[7:4] CR_D[7:4]	AP36 AR38 AN35 AR37	IO	**MMC Card Data.**	**VCCCR**
MMC_D[3:0] CR_D[3:0]	AM35 AN36 AT37 AR36	IO	**MMC Card Data.**	**VCCCR**
MMC_CD# CR_CD#	AT36	I	**MMC Card Detection.** This active low signal indicates a detection event when the card is inserted.	**VSUS33**
MMC_CMD# CR_CMD	AM34	IO	**MMC Card Command / Response.**	**VCCCR**
MMC_CLK CR_CLK	AP37	O	**MMC Card Clock.**	**VCCCR**

xD Card Interface

xD Card Interface is multiplexed with *Card Reader, Multi Media Card, Secure Digital and SDIO Interface*.

xD Card Interface				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
XD_D[7:4] CR_D[7:4]	AP36 AR38 AN35 AR37	IO	**xD Card Data.** In xD mode, these signals have internal 15K ohm pull-down resistors.	**VCCCR**
XD_D[3:0] CR_D[3:0]	AM35 AN36 AT37 AR36	IO	**xD Card Data.** In xD mode, these signals have internal 15K ohm pull-down resistors.	**VCCCR**
XD_RB# CR_CMD	AM34	IO	**xD Card Ready / Busy.** In xD mode, this signal has an internal 25K ohm pull-up resistor.	**VCCCR**
XD_WE# CR_CLK	AP37	O	**xD Card Write Enable.** In xD mode, this signal has an internal 15K ohm pull-up resistor.	**VCCCR**
XD_WP# CR_WPD	AU37	I	**xD Card Write Protect Detection.** In xD mode, this signal has an internal 15K ohm pull-down resistor. L: Enable write protection H: Disable write protection. Write operation is allowed.	**VCCCR**
XD_CD#	AV36	I	**xD Card Detection.** This active low signal indicates a detection event when the card is inserted. This signal has an internal 10K ohm pull-up resistor.	**VSUS33**
XD_CE#	AR35	O	**xD Card Chip Enable.** This signal has an internal 15K ohm pull-up resistor.	**VCCCR**
XD_CLE	AV37	O	**xD Card Command Latch Enable.** High level indicates command latch is enabled. This signal has an internal 15K ohm pull-down resistor.	**VCCCR**
XD_RE#	AU36	O	**xD Card Read Enable.** This signal has an internal 15K ohm pull-up resistor.	**VCCCR**
XD_ALE	AT38	O	**xD Card Address Latch Enable.** High level indicates address latch is enabled. In xD mode, this signal has an internal 15K ohm pull-down resistor.	**VCCCR**

Secure Digital Interface

Secure Card Interface is multiplexed with *Card Reader, xD Card and SDIO Interface*.

Secure Digital Interface				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
SD_D[3:0] CR_D[3:0]	AM35 AN36 AT37 AR36	IO	**SD Card Data.** In SD mode, these signals have internal 25K ohm pull-up resistors.	**VCCCR**
SD_CD# CR_CD#	AT36	I	**SD Card Detection.** This active low signal indicates a detection event when the card is inserted.	**VSUS33**
SD_CMD CR_CMD	AM34	IO	**SD Card Command/Response.** In SD mode, this signal has an internal 25K ohm pull-up resistor.	**VCCCR**
SD_CLK CR_CLK	AP37	O	**SD Card Clock.**	**VCCCR**
SD_WPD CR_WPD	AU37	IO	**SD Card Write Protect Detection.** This signal will keep at high level if it is not connected. In SD mode, this signal has an internal 25K ohm pull-up resistor. L: Disable write protection. Write operation is allowed. H: Enable write protection	**VCCCR**

SDIO Interface

SDIO Interface is multiplexed with *Card Reader, Multi Media Card, xD Card, Secure Digital Interface*.

SDIO Interface				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
SDIOD[3:0] CR_D[3:0]	AM35 AN36 AT37 AR36	IO	**SDIO Port Data.** These signals have internal 25K ohm pull-up resistors.	**VCCCR**
SDIOCD# CR_CD#	AT36	I	**SDIO Port Card Detection.** This active low signal indicates a detection event when the card is inserted.	**VSUS33**
SDIOCMD CR_CMD	AM34	IO	**SDIO Port Command/Response.** This signal has an internal 25K ohm pull-up resistor.	**VCCCR**
SDIOWPD CR_WPD	AU37	IO	**SDIO Port Write Protect Detection.** This signal has an internal 25K ohm pull-up resistor. This signal will keep at high level if it is not connected. L: Disable write protection. Write operation is allowed. H: Enable write protection	**VCCCR**
SDIOCLK CR_CLK	AP37	O	**SDIO Port Card Clock.**	**VCCCR**
SDIOPSEL CR_PWSEL	AU35	O	**SDIO Port Power Select.** This signal has an internal 10K ohm pull-up resistor. The internal pull-up resistor can be enabled by setting D17F0 Rx94[3]=1	**VSUS33**
SDIOPOFF CR_PWOFF	AT35	O	**SDIO Port Power Off.** This signal controls the delivery of power to card. This signal has an internal 10K ohm pull-up resistor. The internal pull-up resistor can be enabled by setting D17F0 Rx94[3]=1 L: On H: Off	**VSUS33**

LPC Bus Interface

LPC Bus Interface				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
LPCAD[3:0]	Y37 Y38 Y35 AA35	IO	**LPC Address / Data.** This signal has an internal 22K ohm pull-up resistor.	**VCC33**
LPCFRAME#	AA38	O	**LPC Frame.**	**VCC33**
LPCDRQ0#	W37	I	**LPC DMA / Bus Master Request 0.** This signal has an internal 15K ohm pull-up resistor.	**VCC33**
LPCDRQ1#	AA37	I	**LPC DMA / Bus Master Request 1.** This signal has an internal 15K ohm pull-up resistor.	**VCC33**

SMBus Interface

SMBus Interface				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
SMBCK1	AT34	OD	**SMB Channel 1 Clock.** Master Mode.	**VSUS33**
SMBDT1	AR33	OD	**SMB Channel 1 Data.** Master Mode.	**VSUS33**
SMBCK2 GPIO1	AT33	OD	**SMB Channel 2 Clock.** Slave Mode.	**VSUS33**
SMBDT2 GPIO0	AU33	OD	**SMB Channel 2 Data.** Slave Mode.	**VSUS33**
SMBALRT#	AU34	I	**SMB Alert.** Enabled by System Management Bus I/O space. When enabled, SMBALRT# assertion generates an IRQ or SMI interrupt or a power management resume event. This signal has a programmable internal 4.7K ohm resistor pull up to VSUS33.	**VSUS33**

SPI Controller Interface

SPI Controller Interface				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
MSPIDO GPO1	AC35	O	**SPI Master Device Data Out.** Transfer data serially from SPI Controller to SPI slave device / flash memory.	**VCC33**
MSPIDI GPI0	AC37	I	**SPI Master Device Data In.** Transfer data serially from SPI slave device / flash memory to SPI Controller. This signal has an internal 10K ohm pull-up resistor.	**VCC33**
MSPISS0# GPO3	AD38	O	**SPI Master Device Chip Select 0.** Select SPI slave device. This signal has an internal 10K ohm pull-up resistor.	**VCC33**
MSPISS1# GPO2	AD37	O	**SPI Master Device Chip Select 1.** Select SPI slave device. This signal has an internal 10K ohm pull-up resistor.	**VCC33**
MSPICLK GPIO6	AC36	IO	**SPI Master Device Clock.** This signal has an internal 10K ohm pull-up resistor.	**VCC33**

PCI UART Interface

There are 4 COM ports integrated within this chip. COM0 and COM1 are multiplexed with either VCP or DVP port, while COM2 and COM3 are multiplexed with PCI interface.

To use UART COM0 and COM1 on the multiplexed DVP interface, set D17F0 RxB0[7]=1 and D17F0 Rx46[6]=1.

PCI UART Interface				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
COM Port 0 (When DVP is Disabled)				
SOUT0 DVP1D10	AC05	O	**Transmit Data for PCI UART Port 0.**	**VCC33**
SIN0 DVP1D11	AE05	I	**Receive Data for PCI UART Port 0.**	**VCC33**
RTS0 DVP1D14	AE07	O	**Request To Send for PCI UART Port 0.**	**VCC33**
CTS0 DVP1D15	AE08	I	**Request To Send for PCI UART Port 0.**	**VCC33**
DTR0 DVP1D12	AD05	O	**Data Terminal Ready for PCI UART Port 0.**	**VCC33**
DSR0 DVP1D13	AE06	I	**Data Set Ready for PCI UART Port 0.**	**VCC33**
DCD0 DVP1D9	AC04	I	**Data Carrier Detect for PCI UART Port 0.**	**VCC33**
RI0 DVP1D8	AC06	I	**Ring Indicator for PCI UART Port 0.**	**VCC33**
COM Port 1 (When DVP is Disabled)				
SOUT1 DVP1D2	AE03	O	**Transmit Data for PCI UART Port 1.**	**VCC33**
SIN1 DVP1D3	AF01	I	**Receive Data for PCI UART Port 1.**	**VCC33**
RTS1 DVP1D6	AD08	O	**Request To Send for PCI UART Port 1.**	**VCC33**
CTS1 DVP1D7	AD07	I	**Clear To Send for PCI UART Port 1.**	**VCC33**
DTR1 DVP1D4	AE09	O	**Data Terminal Ready for PCI UART Port 1.**	**VCC33**
DSR1 DVP1D5	AD09	I	**Data Set Ready for PCI UART Port 1.**	**VCC33**
DCD1 DVP1D1	AE02	I	**Data Carrier Detect for PCI UART Port 1.**	**VCC33**
RI1 DVP1D0	AD03	I	**Ring Indicator for PCI UART Port 1.**	**VCC33**

To use UART COM0 and COM1 on the multiplexed VCP interface, set D17F0 RxB0[7]=0 and D17F0 Rx46[6]=1.

PCI UART Interface					
Signal Name	**Mux Signal**	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
COM Port 0 (When VCP is Disabled)					
SOUT0	VCPD2 PTS0D2	AH03	O	**Transmit Data for PCI UART Port 0.**	**VCC33VGA**
SIN0	VCPD3 PTS0D3	AH01	I	**Receive Data for PCI UART Port 0.**	**VCC33VGA**
RTS0	VCPD6 PTS0D6	AJ01	O	**Request To Send for PCI UART Port 0.**	**VCC33VGA**
CTS0	VCPD7 PTS0D7	AJ02	I	**Request To Send for PCI UART Port 0.**	**VCC33VGA**
DTR0	VCPD4 PTS0D4	AH02	O	**Data Terminal Ready for PCI UART Port 0.**	**VCC33VGA**
DSR0	VCPD5 PTS0D5	AJ03	I	**Data Set Ready for PCI UART Port 0.**	**VCC33VGA**
DCD0	VCPD1 PTS0D1	AG03	I	**Data Carrier Detect for PCI UART Port 0.**	**VCC33VGA**
RI0	VCPD0 PTS0D0	AG01	I	**Ring Indicator for PCI UART Port 0.**	**VCC33VGA**
COM Port 1 (When VCP is Disabled)					
SOUT1	VCPD9 STS1VLD	AG04	O	**Transmit Data for PCI UART Port 1.**	**VCC33VGA**
SIN1	VCPD8 PTS0ERR	AF05	I	**Receive Data for PCI UART Port 1.**	**VCC33VGA**
RTS1	VCPVS PTS0SYNC	AG02	O	**Request To Send for PCI UART Port 1.**	**VCC33VGA**
CTS1	VCPHS PTS0VLD	AF02	I	**Clear To Send for PCI UART Port 1.**	**VCC33VGA**
DTR1	VCPD15 STS1D	AG08	O	**Data Terminal Ready for PCI UART Port 1.**	**VCC33VGA**
DSR1	VCPCLK PTS0CLK	AG07	I	**Data Set Ready for PCI UART Port 1.**	**VCC33VGA**
DCD1	VCPD10 STS1SYNC	AG05	I	**Data Carrier Detect for PCI UART Port 1.**	**VCC33VGA**
RI1	VCPD11 STS1CLK	AJ04	I	**Ring Indicator for PCI UART Port 1.**	**VCC33VGA**

PCI UART Interface (continued)				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
COM Port 2				
SOUT2 CBE3#	AF32	O	**Transmit Data for PCI UART Port 2.**	**VCC33**
SIN2 DEVSEL#	AK36	I	**Receive Data for PCI UART Port 2.**	**VCC33**
RTS2 TRDY#	AK35	O	**Request To Send for PCI UART Port 2.**	**VCC33**
CTS2 FRAME#	AL36	I	**Clear To Send for PCI UART Port 2.**	**VCC33**
DTR2 STOP#	AK34	O	**Data Terminal Ready for PCI UART Port 2.**	**VCC33**
DSR2 IRDY#	AL37	I	**Data Set Ready for PCI UART Port 2.**	**VCC33**
DCD2 CBE2#	AK33	I	**Data Carrier Detect for PCI UART Port 2.**	**VCC33**
RI2 CBE1#	AJ35	I	**Ring Indicator for PCI UART Port 2.**	**VCC33**
COM Port 3				
SOUT3 GNT0#	AJ33	O	**Transmit Data for PCI UART Port 3.**	**VCC33**
SIN3 REQ0#	AH33	I	**Receive Data for PCI UART Port 3.**	**VCC33**
RTS3 GNT1#	AJ31	O	**Request To Send for PCI UART Port 3.**	**VCC33**
CTS3 CBE0#	AE33	I	**Clear To Send for PCI UART Port 3.**	**VCC33**
DTR3 PAR	AJ36	O	**Data Terminal Ready for PCI UART Port 3.**	**VCC33**
DSR3 REQ1#	AH32	I	**Data Set Ready for PCI UART Port 3.**	**VCC33**
DCD3 INTA#	AG31	I	**Data Carrier Detect for PCI UART Port 3.**	**VCC33**
RI3 SERR#	AJ32	I	**Ring Indicator for PCI UART Port 3.**	**VCC33**

High Definition Audio Interface

High Definition Audio Interface				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
AZRST#	AU32	O	**High Definition Audio Reset.**	**VSUS33**
AZBITCLK	Y33	O	**High Definition Audio Bit Clock.** 24.00 MHz.	**VCC33**
AZSYNC	AA36	O	**High Definition Audio Sync.** 48 KHz Frame Sync and outbound tag signal.	**VCC33**
AZSDOUT	AB38	O	**High Definition Audio Serial Data Output.**	**VCC33**
AZSDIN[1:0]	AT31 AT32	IO	**High Definition Audio Serial Data Input.** These signals have internal 4.7K ohm pull-down resistor.	**VSUS33**

Speaker Interface

Speaker Interface				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
SPKR GPO0	Y31	OD	**Speaker Out.**	**VCC33**

Serial IRQ Interface

Serial IRQ Interface				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
SERIRQ	W31	IO	**Serial IRQ.** This signal has an internal 22K ohm pull-up resistor. If this signal is not used, leave it unconnected.	**VCC33**

Internal Keyboard Controller Interface

Internal Keyboard Controller Interface				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
MSCK GPIO3	AV30	OD	**Mouse Clock.** From internal mouse controller. This signal has a programmable internal 10K ohm pull-up resistor.	**VSUS33**
MSDT GPIO2	AT30	OD	**Mouse Data.** From internal mouse controller. This signal has a programmable internal 10K ohm pull-up resistor.	**VSUS33**
KBCK GPIO5 A20GATE	AV31	OD	**Keyboard Clock.** From internal keyboard controller. This signal has a programmable internal 10K ohm pull-up resistor. This signal is used as A20GATE to connect to external keyboard controller's A20Gate signal if external KBC is used.	**VSUS33**
KBDT GPIO4 KBC_CPURST#	AU31	OD	**Keyboard Data.** From internal keyboard controller. This signal has a programmable internal 10K ohm pull-up resistor. This signal is used as KBC_CPURST# to connect to external keyboard controller's CPURST# signal if external KBC is used.	**VSUS33**

Note: For the above signals, the pull-up resistor is enabled by setting D17F0 Rx9F[7]=1.

General Purpose Input Interface

General Purpose Input Interface – Signal Attributes											
Signal Name	**Ball #**	**I/O**	**Default Function**	**Signal State**					**Interrupt Triggered by GPI**	**Power Plane**	**Min Pulse Width (no less than)**
				Reset	**After Reset**	**POS**	**STR**	**STD**			
GPI0 MSPIDI	AC37	I	MSPIDI	Off	Off	Static	Off	Off	SCI/SMI	VCC33	30us
GPI1 GPWAKE#	AN32	I	GPWAKE#	Driven	Driven	Driven	Driven	Driven	SCI/SMI	VSUS33	Note 2
GPI4 BATLOW#	AN34	I	BATLOW#	Static	Driven	Driven	Driven	Driven	No	VSUS33	None
GPI5 EXTSMI#	AL32	I	EXTSMI#	Static	Driven	Driven	Driven	Driven	No	VSUS33	None
GPI6 INTRUDER#	AR31	I	INTRUDER#	Static	Driven	Driven	Driven	Driven	No	VBAT	None
GPI7 LID#	AR34	I	LID#	Static	Driven	Driven	Driven	Driven	No	VSUS33	None
GPI8 RING#	AV35	I	RING#	Static	Driven	Driven	Driven	Driven	No	VSUS33	None
GPI9 THRM#	AB36	I	THRM#	Off	Off	Driven	Off	Off	No	VCC33	None
GPI10 AD0	AD31	I	GPI10	Off	Off	Driven	Off	Off	No	VCC33	None
GPI11 AD1	AG37	I	GPI11	Off	Off	Driven	Off	Off	No	VCC33	None
GPI14 PEXWAKE#	AM32	I	PEXWAKE#	Static	Driven	Driven	Driven	Driven	SCI/SMI	VSUS33	Note 3

GPI Signal States:

1. **Static**: The input signal must remain static, either high or low.
2. **Driven**: The input signal is driven from outside. It is allowed to change.
3. **Off**: The power plane of the input signal is off.

System States:

1. **Reset**: During <RSMRST#, PCIRST#> is <0, 0>
2. **After Reset**: Immediately after <RSMRST#, PCIRST#> is <1, 0>
3. **POS / STR / STD:** Stands for S1 / S3 / S4 state.

Note:

1. "None" means the GPI is level active and should be kept in order to be captured by the read cycle towards the status register.
2. Wake up from Cx/Sx state: It is negedge (falling edge) active and minimum pulse width should be no less than 30us.
   Wake up from Cx state: Triggering polarity is controlled by D17F0 RxE0[1] and minimum pulse width should be no less than 120ns.
3. Wake up from Cx/Sx state: It is negedge (falling edge) active and minimum pulse width should be no less than 30us.
   Wake up from Cx state: Triggering polarity is controlled by D17F0 RxE0[0] and minimum pulse width should be no less than 120ns.

General Purpose Input Interface – Signal Control Registers				
Signal Name	**Control Register**	**GPI Status Register**	**GPI SCI/SMI Register**	**Status Change Register**
GPI0	D17F0 RxE4[1] = 1	PMIO Rx48[0]	PMIO Rx24[0] = 1 or PMIO Rx22[0] = 1	PMIO Rx20[0]
GPI1	N/A	PMIO Rx48[1]	1) PMIO Rx24[1] = 1 PMIO Rx22[1] = 1 2) PMIO Rx52[1] = 1 & { D17F0 RxE0[1] D17F0 RxE1[1] }	PMIO Rx20[1] PMIO Rx50[1]
GPI4	N/A	PMIO Rx48[4]	PMIO Rx25[4] = 1 or PMIO Rx23[4] = 1	PMIO Rx21[4]
GPI5	N/A	PMIO Rx48[5]	PMIO Rx24[4] = 1 or PMIO Rx22[4] = 1	PMIO Rx20[4]
GPI6	N/A	PMIO Rx48[6]	PMIO Rx24[6] = 1 or PMIO Rx22[6] = 0	PMIO Rx20[6]
GPI7	N/A	PMIO Rx48[7]	PMIO Rx25[3] = 0 or PMIO Rx23[3] = 0	PMIO Rx21[3]
GPI8	N/A	PMIO Rx49[0]	PMIO Rx25[0] = 1 or PMIO Rx23[0] = 1	PMIO Rx21[0]
GPI9	N/A	PMIO Rx49[1]	{ PMIO Rx25[2] = 1 or PMIO Rx23[2] = 1 } & D17F0 Rx8C[3] = 1	PMIO Rx21[2]
GPI10	N/A	PMIO Rx4B[0]	D17F0 Rx54[4] =0	N/A
GPI11	N/A	PMIO Rx4B[1]	D17F0 Rx54[4] =0	N/A
GPI14	PMIO Rx6F[1] = 1	PMIO Rx4B[5]	PMIO Rx52[0] = 1 & { D17F0 RxE0[0], D17F0 RxE1[0] }	PMIO Rx50[0]

General Purpose Output Interface

General Purpose Output Interface – Signal Attributes										
Signal Name	**Ball #**	**I/O**	**Default Function**	**Signal State Before Programming GPO**			**Signal State After Programming GPO**			**Power Plane**
				Resume Reset	**Reset**	**After Reset**	**Before Reset**	**Reset**	**After Reset**	
GPO0 SPKR	Y31	O	SPKR	Off	Floating	0	Defined	Floating	0	VCC33
GPO1 MSPIDO	AC35	O	MSPIDO	Off	0	0	Defined	0	0	VCC33
GPO2 MSPISS1#	AD37	O	MSPISS1#	Off	1	1	Defined	1	1	VCC33
GPO3 MSPISS0#	AD38	O	MSPISS0#	Off	1	1	Defined	1	1	VCC33
GPO4[1] AD4	AF38	O	Note	Off	1	1	Defined	1	1	VCC33
GPO5 CPUSTP#	AA30	O	CPUSTP#	Off	1	1	Defined	1	1	VCC33
GPO6 C4PSTOP#	AB37	O	C4PSTOP#	Off	1	1	Defined	1	1	VCC33
GPO7 SUSA# SLOWCLK	AL33	O	SUSA#	Floating	1	1	Defined	Defined	Defined	VSUS33
GPO8 SUSB#	AM31	O	SUSB#	0	1	1	Defined	Defined	Defined	VSUS33
GPO9 SUSC#	AM33	O	SUSC#	0	1	1	Defined	Defined	Defined	VSUS33
GPO10 USBD_PDN	AR32	O	USBD_PDN	0	0	0	Defined	Defined	Defined	VCC33
GPO11 CR_PWSEL SDIO2PWSEL	AU35	O	CR_PWSEL	0	0	0	Defined	Defined	Defined	VSUS33
GPO12 CR_PWOFF SDIO2PWOFF	AT35	O	CR_PWOFF	0	1	1	Defined	Defined	Defined	VSUS33
GPO36[2] PCIERST1#	AC34	O	GPO36	0	0	1	Defined	Floating	1	VCC33
GPO37[2] PCIERST2#	AE36	O	GPO37	0	0	1	Defined	Floating	1	VCC33
GPO38[2] PCIERST3#	AD35	O	GPO38	0	0	1	Defined	Floating	1	VCC33
GPO39[2]	AD36	O	GPO39	0	0	1	Defined	Floating	1	VCC33
GPO40[2]	AD34	O	GPO40	0	0	1	Defined	Floating	1	VCC33

Note:

1. If the strapping MSPISS0# for PCI Master Mode is enabled, then the default function is AD4; else the default function is GPO4.
2. Driving the pins when VCC3 power is off will cause a leakage from these pin.

GPO Signal States:

1. **High-Z**: Tri-State.
2. **High**: The output signal is logic “1”.
3. **Low**: The output signal is logic “0”.
4. **Defined**: The output signal can be high or low, defined by the GPO function.
5. **Undefined**: The output signal is undetermined.
6. **Off**: The power plane of output signal is off.
7. **Not fixed**: The pad is in output mode, and its output value is uncertain.
8. **Floating**: The pad is in input mode, and its state depends on the output drive.

System States:

1. **Resume Reset**: RSMRST# = 0
2. **Reset**: During <RSMRST#, PCIRST1#, PCIRST0#> is <0, 0, 0>
3. **After Reset:** Immediately after <RSMRST#, PCIRST1#, PCIRST0#> is <1, 1, 1>
4. **Before Reset**: Current state is <RSMRST#, PCIRST#> = <1, 1> and next state is <RSMRST#, PCIRST#> = <1, 0>

General Purpose Output Interface – Signal Control Registers		
Signal Name	**Control Register**	**GPO Output Register**
GPO0	D17F0 RxE4[4] = 1	PMIO Rx4C[0]
GPO1	D17F0 RxE4[1] = 1	PMIO Rx4C[1]
GPO2	D17F0 RxE4[1] = 1	PMIO Rx4C[2]
GPO3	D17F0 RxE4[1] = 1	PMIO Rx4C[3]
GPO4	D17F0 Rx54[4] = 0	PMIO Rx4C[4]
GPO5	D17F0 RxE4[5] = 1	PMIO Rx4C[5]
GPO6	D17F0 RxE4[5] = 1	PMIO Rx4C[6]
GPO7	D17F0 Rx95[1] = 1 & PMIO Rx6F[0] = 0 & D17F0 Rx94[1:0] = 00	PMIO Rx4C[7]
GPO8	D17F0 Rx94[2] = 1	PMIO Rx4D[0]
GPO9	D17F0 Rx94[2] = 1	PMIO Rx4D[1]
GPO10	D17F0 RxE4[6] = 1	PMIO Rx4D[2]
GPO11	D17F0 Rx9B[0] = 1	PMIO Rx4F[1]
GPO12	D17F0 Rx9B[0] = 1	PMIO Rx4F[2]
GPO36	N/A	PMIO Rx47[3]
GPO37	N/A	PMIO Rx47[4]
GPO38	N/A	PMIO Rx47[5]
GPO39	N/A	PMIO Rx47[6]
GPO40	N/A	PMIO Rx47[7]

General Purpose Input/Output Interface

General Purpose Input/Output Interface – Signal Attributes											
Signal Name	**Ball #**	**I/O**	**Default Function**	**Signal State Before Programming GPO**			**Signal State After Programming GPO**			**Power Plane**	**Min. Pulse Width**
				Resume Reset	**Reset**	**After Reset**	**Before Reset**	**Reset**	**After Reset**		
GPIO0 SMBDT2	AU33	OD	SMBDT2	Floating	1	1	Defined	Defined	Defined	VSUS33	120ns
GPIO1 SMBCK2	AT33	OD	SMBCK2	Floating	1	1	Defined	Defined	Defined	VSUS33	120ns
GPIO2 MSDT	AT30	OD	MSDT	Floating	1	1	Defined	Defined	Defined	VSUS33	None
GPIO3 MSCK	AV30	OD	MSCK	Floating	1	1	Defined	Defined	Defined	VSUS33	None
GPIO4 KBDT KBC_CPURST#	AU31	OD	KBDT	Floating	1	1	Defined	Defined	Defined	VSUS33	None
GPIO5 KBCK A20GATE	AV31	OD	KBCK	Floating	1	1	Defined	Defined	Defined	VSUS33	None
GPIO6 MSPICLK	AC36	OD	MSPICLK	Off	0	0	Defined	0	0	VCC33	None
GPIO7 PME#	AP33	OD	GPIO7	1	1	1	Defined	Defined	Defined	VSUS33	None
GPIO8 INTB#	AB33	OD	INTB#	Off	1	1	Defined	1	1	VCC33	None
GPIO9 INTC#	AA31	OD	GPIO9	Off	1	1	Defined	1	1	VCC33	None
GPIO10 [1] SATALED0#	AA32	OD	GPIO10	Off	1	1	Defined	1	1	VCC33	120ns
GPIO11 [1] SATALED1#	AB35	OD	GPIO11	Off	1	1	Defined	1	1	VCC33	120ns
GPIO12 INTD#	Y34	OD	GPIO12	Off	1	1	Defined	1	1	VCC33	None
GPIO13 AD9	AF37	OD	GPIO13	Off	1	1	Defined	1	1	VCC33	None
GPIO14 AD10	AF36	OD	GPIO14	Off	1	1	Defined	1	1	VCC33	None
GPIO15 ~ GPIO16 AD11~AD12	AG37 AG38	OD	GPIO15~GPIO16	Off	1	1	Defined	1	1	VCC33	None
GPIO17 ~ GPIO32 AD13~AD28	see pin list	OD	GPIO17~GPIO32	Off	1	1	Defined	1	1	VCC33	None
GPIO33 ~ GPIO35 AD29~AD31	AG34 AG33 AJ34	OD	GPIO33~GPIO35	Off	1	1	Defined	1	1	VCC33	None

Note:
1. Driving the pins when VCC3 power is off will cause a leakage from these pin.
2. For signals with OD attribute above, an external resister (10K) pull-high to proper power plan is recommended.
3. "None" means the GPIO is level active and should be kept in order to be captured by the read cycle towards the status register.

GPIO Signal States:

1. **High-Z**: Tri-State.
2. **High**: The output signal is logic “1”.
3. **Low**: The output signal is logic “0”.
4. **Defined**: The output signal can be high or low, defined by the GPO function.
5. **Undefined**: The output signal is undetermined.
6. **Off**: The power plane of output signal is off.
7. **Not fixed**: The pad is in output mode, and its output value is uncertain.
8. **Floating**: The pad is in input mode, and its state depends on the output drive.

System States:

1. **Resume Reset**: RSMRST# = 0
2. **Reset**: During <RSMRST#, PCIRST1#, PCIRST0#> is <0, 0, 0>
3. **After Reset:** Immediately after <RSMRST#, PCIRST1#, PCIRST0#> is <1, 1, 1>
4. **Before Reset**: Current state is <RSMRST#, PCIRST#> = <1, 1> and next state is <RSMRST#, PCIRST#> = <1, 0>

General Purpose Input/Output Interface – Signal Registers					
Signal Name	**Control Register**	**GPI Status Register**	**GPI SCI/SMI Register**	**GPI Status Change Register**	**GPO Output Register**
GPIO0	D17F0 Rx95[3] = 1 D17F0 Rx95[2] = 1	PMIO Rx49[2]	PMIO Rx52[2] = 1 D17F0 RxE0[2] D17F0 RxE1[2]	PMIO Rx50[2]	PMIO Rx4D[3]
GPIO1	D17F0 Rx95[3] = 1 D17F0 Rx95[2] = 1	PMIO Rx49[3]	PMIO Rx52[3] = 1 D17F0 RxE0[3] D17F0 RxE1[3]	PMIO Rx50[3]	PMIO Rx4D[4]
GPIO2	D17F0 Rx97[6] = 1 D17F0 Rx51[2]=1	PMIO Rx49[4]	N/A	N/A	PMIO Rx4D[5]
GPIO3	D17F0 Rx97[6] = 1 D17F0 Rx51[2]=1	PMIO Rx49[5]	N/A	N/A	PMIO Rx4D[6]
GPIO4	D17F0 Rx97[0] = 1 D17F0 Rx51[0]=1	PMIO Rx49[6]	N/A	N/A	PMIO Rx4D[7]
GPIO5	D17F0 Rx97[0] = 1 D17F0 Rx51[0]=1	PMIO Rx49[7]	N/A	N/A	PMIO Rx4E[0]
GPIO6	D17F0 RxE4[1] = 1	PMIO Rx4A[0]	N/A	N/A	PMIO Rx4E[1]
GPIO7	D17F0 Rx9B[4] = 1 D17F0 Rx54[4] = 0	PMIO Rx4A[1]	N/A	N/A	PMIO Rx4E[2]
GPIO8	D17F0 Rx54[4] = 0	PMIO Rx4A[2]	N/A	N/A	PMIO Rx4E[3]
GPIO9	D17F0 Rx54[4] = 0	PMIO Rx4A[3]	N/A	N/A	PMIO Rx4E[4]
GPIO10	D17F0 RxE4[0] = 0	PMIO Rx4A[4]	PMIO Rx52[4] = 1 D17F0 RxE0[4] D17F0 RxE1[4]	PMIO Rx50[4]	PMIO Rx4E[5]
GPIO11	D17F0 RxE4[0] = 0	PMIO Rx4A[5]	PMIO Rx52[5] = 1 D17F0 RxE0[5] D17F0 RxE1[5]	PMIO Rx50[5]	PMIO Rx4E[6]
GPIO12	D17F0 Rx54[4] = 0	PMIO Rx4A[6]	N/A	N/A	PMIO Rx4E[7]
GPIO13	D17F0 Rx54[4] = 0	PMIO Rx4A[7]	N/A	N/A	PMIO Rx4F[0]
GPIO14	D17F0 Rx54[4] = 0	PMIO Rx4B[4]	N/A	N/A	PMIO Rx4F[3]
GPIO15~ GPIO16	D17F0 Rx54[4] = 0	PMIO Rx4B[6:7]	N/A	N/A	PMIO Rx4F[6:7]
GPIO17~ GPIO32	D17F0 Rx54[4] = 0	PMIO Rx3C[0:15]	N/A	N/A	PMIO Rx3C[16:31]
GPIO33~ GPIO35	D17F0 Rx54[4] = 0	PMIO Rx46[0:2]	N/A	N/A	PMIO Rx47[0:2]

Graphics General Purpose Input / Output Interface

Graphics General Purpose Input / Output Interface				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
VGPIO	AF04	IO	**Dedicated Video GPIO**	**VCC33VGA**
VGPI0 DISPCLKI0	Y06	I	**Graphics General Purpose Input**	**VCC33VGA**
VGPO0 DISPCLKO0	AA06	O	**Graphics General Purpose Output**	**VCC33VGA**
VGPI1 DISPCLKI1	AA04	I	**Graphics General Purpose Input**	**VCC33VGA**
VGPO1 DISPCLKO1	AA05	O	**Graphics General Purpose Output**	**VCC33VGA**

Power Management Control and Event Signals

Power Management Control and Event Signals						
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Triggered Polarity**	**Min. Pulse Width** (no less than)	**Power Plane**
PWRBTN#	AN33	I	**Power Button.** This signal could generate SCI/SMI and wake up the system from sleep state. If press PWRBTN# for four consecutive seconds or longer, the system will move to S5 state unconditionally. PWRBTN# has internal de-bounce logic and internal logic powered by VSUS33.	Negative edge	16ms	**VSUS33**
EXTSMI# GPI5	AL32	I	**External System Management Interrupt.** When enabled, a falling edge on this input causes an SMI# to be generated to the CPU to enter SMI mode. This signal has an internal 8K ohm pull-up resistor.	Negative edge	30us	**VSUS33**
PME# GPIO7	AP33	I	**Power Management Event.** This signal has an internal 10K ohm pull-up resistor.	Negative edge	Not required	**VSUS33**
LID# / GPI7	AR34	I	**Notebook Computer Display Lid Open / Closed Monitor.** Used by the Power Management subsystem to monitor the opening and closing of the display lid of notebook computers. Can be used to detect either low-to-high or high-to-low transitions to generate an SMI#. This signal has an internal 8K ohm pull-up resistor.	PMIO Rx2C[7]	Note 1	**VSUS33**
PEXWAKE# GPI14	AM32	I	**PCIe Wake-Up Event.** Indicates that a system wake event has occurred. Used to waken the chip from deep sleep mode (S3 / S4 / S5 states).	Negative edge	30 us	**VSUS33**
GPWAKE# GPI1	AN32	I	**GPI Wake-Up Event.** This signal has an internal 8K ohm pull-up resistor.	Negative edge	30 us	**VSUS33**
INTRUDER# GPI6	AR31	I	**Intrusion Indicator.** This signal needs an external 1M ohm pull-up resister to VBAT to prevent leakage.	Negative edge	Not required	**VBAT**
THRM# GPI9	AB36	I	**Thermal Alarm Monitor.** This signal is to enable the throttling mode of the STPCLK# signal for thermal control. This signal has an internal 8K ohm pull-up resistor.	PMIO Rx2C[6]	60ns	**VCC33**
RING# GPI8	AV35	I	**Ring Indicator.** May be connected to external modem circuitry to allow the system to be re-activated by a received phone call. This signal has an internal 10K ohm pull-up resistor.	Negative edge	30us	**VSUS33**
BATLOW# / GPI4	AN34	I	**Battery Low Indicator.** This signal has an internal 8K ohm pull-up resistor.	Positive edge	60ns	**VSUS33**

Note:

1. If D17F0 Rx80[5]=1, minimum pulse width should be no less than 16ms
   If D17F0 Rx80[5]= 0, minimum pulse width should be no less than 30us

Power Management Control and Event Signals (continued)				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
CPUSTP# GPO5	AA30	O	**CPU Clock Stop.** Signals the system clock generator to disable the CPU clock outputs.	**VCC33**
SUSA# SLOWCLK GPO7	AL33	O	**Suspend Plane A Control**. Asserted during power management POS, STR, and STD suspend states. Used to control the primary power plane.	**VSUS33**
SUSB# GPO8	AM31	O	**Suspend Plane B Control**. Asserted during power management STR and STD suspend states. Used to control the secondary power plane.	**VSUS33**
SUSC# GPO9	AM33	O	**Suspend Plane C Control.** Asserted during power management STD suspend state. Used to control the tertiary power plane. Also connected to ATX power-on circuitry.	**VSUS33**
C4PSTOP# GPO6	AB37	O	**C4P Stop.** When the C4P sleep state is entered, the internal PLL is turned off. This signal has an internal 19.4K ohm pull-up resistor.	**VCC33**
VRDSLP	Y30	O	**Voltage Regulator Deep Sleep.** Connected to the CPU voltage regulator. High selects the proper voltage for deep sleep mode. This signal has an internal 10K ohm pull-up resistor.	**VCC33**
HDMI_CEC	AC30	IO	**HDMI CEC (Consumer Electronics Control) Bus.**	**VCC33**

Clock, Test and Miscellaneous Signals

Clock, Test and Miscellaneous Signals				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
GFX Clock Signals				
DISPCLKI0 VGPI0	Y06	I	**Dot Clock (Pixel Clock) Input.** DISPCLKI0 can optionally be used as VGPI0.	**VCC33VGA**
DISPCLKO0 VGPO0	AA06	O	**Dot Clock (Pixel Clock) Output.** DISPCLKO0 can optionally be used as VGPO0.	**VCC33VGA**
DISPCLKI1 VGPI1	AA04	I	**Dot Clock (Pixel Clock) Input.** DISPCLKI1 can optionally be used as VGPI1.	**VCC33VGA**
DISPCLKO1 VPGO1	AA05	O	**Dot Clock (Pixel Clock) Output.** DISPCLKO1 can optionally be used as VGPO1.	**VCC33VGA**
CLK14M	Y08	I	**Graphic Clock.** 14.318 MHz, shared with OSC.	**VCC33VGA**
RTC Crystal Clock Signal				
RTCXI	AU30	I	**RTC Crystal Input**: 32.768 KHz Crystal Input.	**VBAT**
RTCXO	AV29	O	**RTC Crystal Output**: 32.768 KHz Crystal Output.	**VBAT**
Power State and System Reset				
PWRGD	AP30	I	**Power Good.** Connected to the Power Good signal on the Power Supply indicating all power rails have been stable. The rising edge of this signal and PCIRST# are used to sample power-up strap options. PWRGD is a Schmitt trigger input pin. Internal logic powered by VBAT. Reserve a pull down resister 33K to GND.	**VBAT**
RSMRST#	AN30	I	**Resume Reset.** When asserted, this signal resets VX900 series and sets all register bits to the default value. RSMRST # is a Schmitt trigger input pin.	**VBAT**
Power Management				
CLK66M	J15	I	**66 MHz Clock for Power Management.**	**VTT**

Clock, Test and Miscellaneous Signals (continued)				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
Test and Miscellaneous Signals				
TESTEN	J19	I	**Test In.** This signal is used for testing. Tie to GND for normal system operation.	**VTT**
DFTEN	A18	I	**DFT In.** This signal is used for testing. Tie to GND for normal system operation.	**VTT**
BISTEN	B19	I	**BIST In.** This signal is used for testing. Tie to GND for normal system operation.	**VTT**
TP	AN31	I	**Test Point for Current Adjustment.** Pull down through a 47K Ohm to GND.	**VBAT**
TP[2:0]	K18 H20 H19	I	**Test Pad.** Connect TP2 through 47K Ohm pull down to GND.	**VTT**
TP[4:3]	W30 AB30	I	**Test Pad.** Connect TP3 through 47K Ohm pull down to GND.	**VCC33**
TP5	W07	I	**Test Pad.**	**VCC33VGA**
TP6	AL30	I	**Test Pad.**	**VSUS33**
SLOWCLK SUSA# GPO7	AL33	O	**Slow Clock.** Slow clock is generated from internal 32KHz clock. Refer to D17F0 Rx94[1:0] for detail	**VSUS33**

Compensation Signals

Compensation				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
MEMCOMP	G33	AI	**Memory Compensation.**	**VSUSIOMEM**
HGTLPVT_REXT	H17	AI	**AGTL P Compensation.**	**VTT**

Reference Voltage Signals

Reference Voltages			
Signal Name	**Ball #**	**I/O**	**Signal Description**
MEMVREF	H31	AI	**Memory Voltage Reference.**
HGTLVREF[1:0]	J13, J20	AI	**Host CPU Interface AGTL+ Voltage Reference.** Set it to 2/3 of VTT.

Power / Ground Signals

Digital Power / Ground		
Signal Name	**Ball #**	**Signal Description**
VTT	(see ball list)	**I/O Power for Host Interface.** 1.05V±5%
VSUSIOMEM	(see ball list)	**Suspend Power for Memory Module.** **DDR2:** 1.8V±5% **DDR3:** 1.5V±5%
VSUSVDDMEM	R30, V29	**Suspend Digital Power.** **VX900:** 1.2V±5% **VX900M:** 1.0V±5%
VSUS33	(see ball list)	**Suspend Power.** Always available unless the mechanical switch of the power supply is turned off. If the "soft-off" state is not implemented, then these signal balls can be connected to VCC33. 3.3V ±5%.
VSUSVDD	AB26, AD26, AE26	**Suspend Core Power.** S5 power for USB logic core with VSUS. **VX900:** 1.2V±5% **VX900M:** 1.0V±5%
VDD	(see ball list)	**Core Power.** **VX900:** 1.2V±5% **VX900M:** 1.0V±5%
VCC33	(see ball list)	**I/O Power.** 3.3V ±5%
VCC33VGA	(see ball list)	**3.3V Pad Power of VGA Pads.**
GNDA12PEX	(see ball list)	**Ground for PCI Express.**
GNDA25PEX	(see ball list)	**Ground for PCI Express.**
GNDA12DP1	Y11, Y12, Y13	**Ground for Display Port 1.**
GNDA25DP1	(see ball list)	**Ground for Display Port 1.**
GNDA12SATA	(see ball list)	**SATA Analog Ground.**
GNDA25SATA	(see ball list)	**SATA Analog Ground.**
GNDA25HCK	J16	**Ground for Host CPU Clock PLL.**
VBAT	AP31	**RTC Battery.** Battery input for internal RTC (RTCXI, RTCXO).
GND	(see ball list)	**Ground.** Connect to primary motherboard ground plane.

Analog Power / Ground		
Signal Name	**Ball #**	**Signal Description**
Host Interface		
VCCA25HCK	K16	**Power for Host CPU Clock PLL.** 2.5V ±5%
Graphics and Video		
VCCA25DAC	L04, L05,T13	**Power for DAC.** 2.5V ±5%
VCCA25PLLDISP	T15, U15	**Power for Graphics PLL.** 2.5V ±5%
LVDS Transmitter		
VCCA25LVDS	U13, U14, V14	**Power for LVDS.** 2.5V ±5%
VCCA25PLLLVDS	U12	**Power for LVDS PLL.** 2.5V ±5%
SATA Interface		
VCCA12SATA	AD21, AL19	**Power for SATA Device.** 1.2V ±5%
VCCA25SATA	AE21, AL18	**Power for SATA Device.** 2.5V ±5%
PCIe Interface		
VCCA12PEX	(see ball list)	**Power for PCIe Device.** 1.2V ±5%
VCCA25PEX	(see ball list)	**Power for PCIe Device.** 2.5V ±5%
USB Controller		
VCCA12USBD	AF24	**Power for USB Device.** **VX900:** 1.2V ±5% **VX900M:** 1.0V ±5%
VCCA33USBD	AE24, AK27	**Power for USB Device.** 3.3V ±5%.
VSUSA33USBH	(see ball list)	**Suspend Power (S5) for USB Host.** 3.3V ±5%.
VSUSAVDDUSBH	AE23	**Suspend Analog Power (S5) for USB Host.** **VX900:** 1.2V ±5% **VX900M:** 1.0V ±5%
Display Port Interface		
VCCA12DP1	Y14, Y15	**Power for DP.** 1.1V±5%. **Power for HDMI.** 1.1V-5% ~ 1.2V+5%
VCCA25DP1	W14, W15	**Power for DP/HDMI.** 2.5V±5%.
Card Reader Interface		
VCCCR	AB25	**I/O Power for Card Reader.** 1.8V / 3.3V ±5%.

Multiplexed Interface Tables

This section provides detailed multiplexed signals information for VX900 series.

Digital Video Port 1 (DVP1) – Display Interface Configurations

Functions of Digital Video Port 1						
Ball Name	**Ball #**	**20-bit TV Output Mode**	**DVO (TV Encoder)**	**DVO (DVI Transmitter)**	**18-bit TTL Panel**	
					Signal	**RGB Color Mapping**
DVP1D15	AE08	DVP1D15	–	–	TTLPD15	R5
DVP1D14	AE07	DVP1D14	–	–	TTLPD14	R4
DVP1D13	AE06	DVP1D13	–	–	TTLPD13	R3
DVP1D12	AD05	DVP1D12	–	–	TTLPD12	R2
DVP1D11	AE05	DVP1D11	DVO-TVD11	DVO-DVID11	TTLPD11	G7 (MSB)
DVP1D10	AC05	DVP1D10	DVO-TVD10	DVO-DVID10	TTLPD10	G6
DVP1D9	AC04	DVP1D9	DVO-TVD09	DVO-DVID09	TTLPD09	G5
DVP1D8	AC06	DVP1D8	DVO-TVD08	DVO-DVID08	TTLPD08	G4
DVP1D7	AD07	DVP1D7	DVO-TVD07	DVO-DVID07	TTLPD07	G3
DVP1D6	AD08	DVP1D6	DVO-TVD06	DVO-DVID06	TTLPD06	G2
DVP1D5	AD09	DVP1D5	DVO-TVD05	DVO-DVID05	TTLPD05	B7 (MSB)
DVP1D4	AE09	DVP1D4	DVO-TVD04	DVO-DVID04	TTLPD04	B6
DVP1D3	AF01	DVP1D3	DVO-TVD03	DVO-DVID03	TTLPD03	B5
DVP1D2	AE03	DVP1D2	DVO-TVD02	DVO-DVID02	TTLPD02	B4
DVP1D1	AE02	DVP1D1	DVO-TVD01	DVO-DVID01	TTLPD01	B3
DVP1D0	AD03	DVP1D0	DVO-TVD00	DVO-DVID00	TTLPD00	B2
DVP1DE	AF07	DVP1D19	DVO-TVDE	DVO-DVIDE	TTLPDE	DE
DVP1TVFLD	AF06	DVP1D18	DVO-TVFIELD	–	TTLPD17	R7 (MSB)
DVP1HS	AD04	DVP1D17	DVO-TVHS	DVO-DVIHS	TTLPHS	HSYNC
DVP1VS	AE01	DVP1D16	DVO-TVVS	DVO-DVIVS	TTLPVS	VSYNC
DVP1CLK	AD01	DVP1CLK	DVO-TVCLK	DVO-DVICLK	TTLPCLK	Clock
DVP1TVCLKR	AD02	DVP1DET	DVO-TVCLKR	DVO-DVIDET	TTLPD16	R6

Multiplexed Signals of DVP1

DVP1 and PCI UART Multiplexed Signals		
Ball#	**Digital Video Port 1**	**PCI UART Interface**
AD03	DVP1D0	RI1
AE02	DVP1D1	DCD1
AE03	DVP1D2	SOUT1
AF01	DVP1D3	SIN1
AE09	DVP1D4	DTR1
AD09	DVP1D5	DSR1
AD08	DVP1D6	RTS1
AD07	DVP1D7	CTS1
AC06	DVP1D8	RI0
AC04	DVP1D9	DCD0
AC05	DVP1D10	SOUT0
AE05	DVP1D11	SIN0
AD05	DVP1D12	DTR0
AE06	DVP1D13	DSR0
AE07	DVP1D14	RTS0
AE08	DVP1D15	CTS0
AD04	DVP1HS	–
AE01	DVP1VS	–
AF07	DVP1DE	–
AF06	DVP1TVFLD	–
AD01	DVP1CLK	–
AD02	DVP1TVCLKR	–
AB04	DVPSPD	–
AB05	DVPSPCLK	–

Multiplexed Signals of VCP

VCP Multiplexed Signals			
Ball#	**Video Capture Port**	**Transport Stream Input Mode** (8-bit Parallel + Serial)	**PCI UART Interface**
AG01	VCPD0	PTS0D0	RI0
AG03	VCPD1	PTS0D1	DCD0
AH03	VCPD2	PTS0D2	SOUT0
AH01	VCPD3	PTS0D3	SIN0
AH02	VCPD4	PTS0D4	DTR0
AJ03	VCPD5	PTS0D5	DSR0
AJ01	VCPD6	PTS0D6	RTS0
AJ02	VCPD7	PTS0D7	CTS0
AF05	VCPD8	PTS0ERR	SIN1
AG04	VCPD9	STS1VLD	SOUT1
AG05	VCPD10	STS1SYNC	DCD1
AJ04	VCPD11	STS1CLK	RI1
AH05	VCPD12	STS1ERR	-
AJ05	VCPD13	-	-
AH06	VCPD14	-	-
AG08	VCPD15	STS1D	DTR1
AF02	VCPHS	PTS0VLD	CTS1
AG02	VCPVS	PTS0SYNC	RTS1
AG07	VCPCLK	PTS0CLK	DSR1

Multiplexed Signals of Card Reader

Card Reader Multiplexed Signals					
Ball#	**Ball Name**	**MMC**	**xD**	**SD**	**SDIO**
AR36	CR_D0	MMC_D0	XD_D0	SD_D0	SDIOD0
AT37	CR_D1	MMC_D1	XD_D1	SD_D1	SDIOD1
AN36	CR_D2	MMC_D2	XD_D2	SD_D2	SDIOD2
AM35	CR_D3	MMC_D3	XD_D3	SD_D3	SDIOD3
AR37	CR_D4	MMC_D4	XD_D4	–	–
AN35	CR_D5	MMC_D5	XD_D5	–	–
AR38	CR_D6	MMC_D6	XD_D6	–	–
AP36	CR_D7	MMC_D7	XD_D7	–	–
AT36	CR_CD#	MMC_CD#	–	SD_CD#	SDIOCD#
AP37	CR_CLK	MMC_CLK	XD_WE#	SD_CLK	SDIOCLK
AM34	CR_CMD	MMC_CMD#	XD_RB#	SD_CMD	SDIOCMD
AT35	CR_PWOFF	–	–	–	SDIOPWOFF
AU35	CR_PWSEL	–	–	–	SDIOPWSEL
AU37	CR_WPD	–	XD_WP#	SD_WPD	SDIOWPD
AT38	–	–	XD_ALE	–	–
AV36	–	–	XD_CD#	–	–
AR35	–	–	XD_CE#	–	–
AV37	–	–	XD_CLE	–	–
AU36	–	–	XD_RE#	–	–

Strapping Signal Table

Related strapping signal information is listed below, external pull-up / pull-down straps are required to select "H" / "L". "X" means the strapping is ignored.

Strapping Signal					
Signal		**Ball#**	**Function**	**Description**	**Power**
North Module	**GPO36**	AC34	FSB Clock	Always strapping low with 1K ohm to ground for normal operation.	VCC33
	GPO37	AE36			VCC33
	GPO38	AD35			VCC33
	GPO39	AD36	IOQ Depth Select	L: 12 or 16 Levels H: 1 Level	VCC33
	GPO40	AD34	DP / HDMI Select	L: HDMI Mode H: DP Mode	VCC33
	C4PSTOP#	AB37	PCIe / DP Select	L: PCIe x 4 H: DP x 4	VCC33
	DVP1D7	AD07	Reserved	Always strapping low with 4.7K ohm to ground for normal operation.	VCC33
	DVP1D9	AC04	Reserved	Always strapping low with 4.7K ohm to ground for normal operation.	VCC33
	DVP1D10	AC05	Reserved	Always strapping low with 4.7K ohm to ground for normal operation.	VCC33
	DVP1D14	AE07	Reserved	Always strapping low with 4.7K ohm to ground for normal operation.	VCC33
South Module	**AZBITCLK**	Y33	SPI / LPC ROM Select	L: LPC ROM H: SPI ROM	VCC33
	AZSDOUT	AB38	System Auto Reboot	L: Enable H: Disable	VCC33
	AZSYNC	AA36	LPC FWH Command	L: Enable H: Disable	VCC33
	MSPISS0#	AD38	PCI Master Mode Enable	L: Disable H: Enable	VCC33
	MSPISS1#	AD37	DebugLink Enable	L: xD Mode (For normal operation) H: DebugLink Mode	VCC33

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Table 7. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes
T_C	Operating case temperature	0	95	^oC	1
T_S	Storage temperature	–55	125	^oC	1
V_{IN}	Input voltage	0	V_{RAIL} + 10%	Volts	1, 2
V_{OUT}	Output voltage	0	V_{RAIL} + 10%	Volts	1, 2

Note:

1. Stress above the conditions listed may cause permanent damage to the device. Functional operation of this device should be restricted to the conditions described under operating conditions.
2. V_{RAIL} is defined as the V_{CC} level of the respective rail.

Electrical Characteristics - Clock

Table 8. Electrical Characteristics – HCLK+/-

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Clock Period	T_{PERIOD}	Freq = 100Mhz	9.999	10.001	ns
HCLK Frequency	F_{HCLK}	Freq = 100Mhz, SSC -0.5%	–	100.03	MHz
Clock Period	T_{PERIOD}	Freq = 100Mhz, SSC -0.5%	9.997	–	ns
Clock Period	T_{PERIOD}	Freq = 200Mhz	4.995	5.0005	ns
HCLK Frequency	F_{HCLK}	Freq = 200Mhz, SSC -0.5%	–	200.06	MHz
Clock Period	T_{PERIOD}	Freq = 200Mhz, SSC -0.5%	4.998	–	ns
Jitter – Cycle to Cycle	TJ_{C2C}	Differential Measurement	–	85	ps
Input Voltage	V_H	Statistical measurement on single-ended signal	660	850	mV
Input Voltage	V_L	Statistical measurement on single-ended signal	-150	–	mV
Maximum Input Voltage	V_{OVS}	Measurement on single-ended signal using absolute	–	1150	mV
Minimum Input Voltage	V_{UDV}	Measurement on single-ended signal using absolute	-300	–	mV
Crossing Point Voltage	V_{XABS}	Single-ended Measurement	300	550	mV
Crossing Point Variation	ΔV_{CROSS}	Single-ended Measurement	–	140	mV
Rising Edge Slew Rate	T_{SLR}	Differential Measurement	2.5	8	V/ns
Falling Edge Slew Rate	T_{FLR}	Differential Measurement	2.5	8	V/ns
Duty Cycle	D_{CYC}	Differential Measurement	45	55	%

Table 9. Electrical Characteristics – PEXCLK+/- (100MHz)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Clock Period	T_{PERIOD}	Freq = 100Mhz, None SSC	9.999	10.001	ns
PEXCLK Frequency	F_{PEXCLK}	100Mhz, SSC -0.5%	–	100.03	MHz
Clock Period	T_{PERIOD}	100Mhz, SSC -0.5%	9.997	–	ns
Input High Voltage	V_H	Statistical measurement on Single ended signal	660	850	V
Input Low Voltage	V_L	Statistical measurement on Single ended signal	-150	–	V
Maximum Input Voltage	V_{OVS}	Measurement on Single ended signal using absolute	–	1150	mV
Minimum Input Voltage	V_{UDV}	Measurement on Single ended signal using absolute	-300	–	mV
Crossing Point Voltage	V_{XABS}	Single-ended Measurement	300	550	mV
Crossing Point Variation	ΔV_{CROSS}	Single-ended Measurement	–	140	mV
Rising Edge Slew Rate	T_{SLR}	Differential Measurement	0.6	4	V/ns
Falling Edge Slew Rate	T_{FLR}	Differential Measurement	0.6	4	V/ns
Duty Cycle	D_{CYC}	Differential Measurement	45	55	%
Jitter – Cycle to Cycle	TJ_{C2C}	Differential Measurement	–	125	ps

Table 10. Electrical Characteristics – CLK66M

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Clock Period	T_{PERIOD}	66.666MHz nominal	14.998	15.001	ns
Input High Voltage	V_{IH}		2.4	–	V
Input Low Voltage	V_{IL}		–	0.4	V
Rise Time	T_R	V_L =0.8 V, V_H = 2.0 V	0.3	1.2	ns
Fall Time	T_F	V_H =2.0 V, V_L = 0.8 V	0.3	1.2	ns
Duty Cycle	D_{CYC}	V_T = 1.5 V	45	55	%

Table 11. Electrical Characteristics – USBCLK

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Clock Period	T_{PERIOD}	48.00MHz nominal	20.8313	20.8354	ns
Input High Voltage	V_{IH}		2.4	–	V
Input Low Voltage	V_{IL}		–	0.4	V
Rise Time	T_R	V_L =0.8 V, V_H = 2.0 V	0.6	1.2	ns
Fall Time	T_F	V_H =2.0 V, V_L = 0.8 V	0.6	1.2	ns
Duty Cycle	D_{CYC}	V_T = 1.5 V	45	55	%

Table 12. Electrical Characteristics – PCICLK

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Frequency	F_{PCICLK}		30	35	MHz
Clock Period	T_{PERIOD}	33.333MHz output nominal	28.57	33.33	ns
Input High Voltage	V_{IH}		2.4	4	V
Input Low Voltage	V_{IL}		-0.3	0.4	V
Edge Rate	T_{SR}	Rising/Falling edge rate	0.5	4	V/ns
Rise Time	T_R	V_L =0.8 V, V_H = 2.0 V	0.3	1.2	ns
Fall Time	T_F	V_H =2.0 V, V_L = 0.8 V	0.3	1.2	ns
Duty Cycle	D_{CYC}	V_T = 1.5 V	45	55	%

Table 13. Electrical Characteristics – CLK14M

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Long Accuracy	ppm	See Tperiod min-max values	-30	30	ppm
Frequency	F_{REF}		14.3175705	14.31842954	MHz
Clock Period	T_{PERIOD}		69.84	69.8422	ns
Input High Voltage	V_{IH}		2.4	4	V
Input Low Voltage	V_{IL}		-0.3	0.4	V
Edge Rate	T_{SR}	Rising/Falling edge rate	0.5	4	V/ns
Rise Time	T_R	V_L =0.8 V, V_H = 2.0 V	0.3	1.2	ns
Fall Time	T_F	V_H =2.0 V, V_L = 0.8 V	0.3	1.2	ns
Duty Cycle	D_{CYC}	V_T = 1.5 V	45	55	%

Table 14. Electrical Characteristics - MCLK Out (DDR2)

PARAMETER	SYMBOL	CONDITIONS	MIN	Typ.	MAX	UNITS
Output Frequency Range	F_{MCLK}	DDR2 - 800 Mhz D0F3 Rx[E6]=FF D0F3 Rx[EE]=00*	–	400	–	MHz
Output pk-pk Voltage	$V_{OD(AC)}$	Single Ended Measurement	0.5	–	VDDQ	V
Output Cross-Point Voltage	$V_{OX(AC)}$	Single Ended Measurement	–	–	±175	mV
Output Skew MLKO+/MCLKO-	T_{SKEW}	Differential measurement	–	–	100	ps
Output Duty Cycle	D_{CYC}	Differential measurement	48	–	52	%
Jitter – Cycle to cycle	TJ_{ACC}	Differential measurement DDR2-667	-125	–	125	ps
Jitter – Cycle to cycle	TJ_{ACC}	Differential measurement DDR2-800	-100	–	100	ps

Table 15. Electrical Characteristics - MCLK Out (DDR3)

PARAMETER	SYMBOL	CONDITIONS	MIN	Typ.	MAX	UNITS
Output Frequency Range	F_{MCLK}	DDR3 - 800 Mhz D0F3 Rx[E6]=FF D0F3 Rx[EE]=00		400	–	MHz
Output Cross-Point Voltage	$V_{OX(AC)}$	Single Ended Measurement	–		±150	mV
Output Skew MLKO+/MCLKO-	T_{SKEW}	Differential measurement	–		±100	ps
Output Duty Cycle	D_{CYC}	Differential measurement	47		53	%
Jitter – Cycle to cycle	TJ_{ACC}	Differential measurement DDR3-800	-100		100	ps
Jitter – Cycle to cycle	TJ_{ACC}	Differential measurement DDR3-1066	-90		90	ps

Table 16. Electrical Characteristics – DPCLK

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Clock Period	T_{PERIOD}	27MHz nominal	37.033	37.040	ns
Input High Voltage	V_{IH}		2.4	–	V
Input Low Voltage	V_{IL}		-0.3	0.4	V
Rise Time	T_R	V_L =0.8 V, V_H = 2.0 V	0.3	1.2	ns
Fall Time	T_F	V_H =2.0 V, V_L = 0.8 V	0.3	1.2	ns
Duty Cycle	D_{CYC}	V_T = 1.5 V	45	55	%

Table 17. Electrical Characteristics – SATACLK

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Clock Period	T_{PERIOD}	100MHz nominal	9.999	10.001	ns
Input High Voltage	V_{IH}		2.4	–	V
Input Low Voltage	V_{IL}		–	0.4	V
Rise Time	T_R	V_L =0.8 V, V_H = 2.0 V	0.2	1.2	ns
Fall Time	T_F	V_H =2.0 V, V_L = 0.8 V	0.2	1.2	ns
Duty Cycle	D_{CYC}	V_T = 1.5 V	45	55	%

Electrical Characteristics – Host Interface

Table 18. Host Interface (1X/4X)

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input Low Voltage	V_{IL}	-0.1	HGTLVREF-0.2	V
Input High Voltage	V_{IH}	HGTLVREF+0.2	VTT+0.1	V
Output Low Voltage	V_{OL}	–	0.3*VTT+.1	V
Output High Voltage	V_{OH}	0.9*VTT	VTT	V

Electrical Characteristics – System Memory

Table 19. System Memory Interface (DDR2)- Input Logic Level

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
DC Input Logic High	V_{IH}	VREF+0.125	VDDQ+0.3	V	
DC Input Logic Low	V_{IL}	–0.3	VREF–0.125	V	
DDR2 800 / 667					
AC Input Logic High	V_{IH}	VREF+0.20	–	V	
AC Input Logic Low	V_{IL}	-	VREF–0.20	V	
DDR2 533 / 400					
AC Input Logic High	V_{IH}	VREF+0.250		V	
AC Input Logic Low	V_{IL}	-	VREF–0.250	V	

Table 20. System Memory Interface (DDR2) - Differential Logic Level

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Differential Input					
Differential Input Voltage	V_{ID}	0.5	VDDQ	V	
Differential Cross Point Voltage	V_{IX}	0.5 * VDDQ–0.175	0.5 * VDDQ+0.175	V	

Table 21. System Memory Interface (DDR3)- Input Logic Level

PARAMETER	SYMBOL	MIN	MAX	UNITS
DC Input Logic High	$V_{IH(DC)}$	VREF+0.100	VDD	V
DC Input Logic Low	$V_{IL(DC)}$	0	VREF–0.100	V
AC Input Logic High	$V_{IH(AC)}$	VREF+0.175	–	V
AC Input Logic Low	$V_{IL(AC)}$	–	VREF–0.175	V

Table 22. System Memory Interface (DDR3) - Differential Logic Level

PARAMETER	SYMBOL	MIN	MAX	UNITS
Differential Input				
AC Differential Input High	$V_{IHdiff(AC)}$	$2x(V_{IH(AC)} - V_{ref})$	–	
AC Differential Input Low	$V_{ILdiff(AC)}$	–	$2x(V_{ref} - V_{IL(AC)})$	
Differential Output				
Differential Cross Point Voltage	V_{OX}	0.5 * VDDQ–0.150	0.5 * VDDQ + 0.150	V

Electrical Characteristics – PCI Express Interface

Table 23. PCIe Differential Transmitter (TX) Output Specifications for Gen1

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Unit Interval	UI	399.88	400	400.12	ps
Differential Peak-to-Peak Output Voltage	VTX-DIFFp-p	0.8	–	1.2	V
De-emphasized Differential Output Voltage (ratio)	VTX-DE-RATIO	-3	-3.5	-4	dB
Minimum TX Eye Width	VTX-EYE	0.75	–	–	UI
Maximum Time between Jitter Median and Maximum Deviation from the Median	VTX-EYE-MEDIANTO-MAX-JITTER	–	–	0.125	UI
DC Differential TX Impedance	ZTX-DIFF-DC	80	100	120	Ohm
AC Coupling Capacitor	CTX	75	–	200	pF

Table 24. PCIe Differential Receiver (RX) Output Specifications for Gen1

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Unit Interval	UI	399.88	400	400.12	ps
DC Differential RX Impedance	ZRX-DIFF-DC	80	100	120	Ohm
DC Input Common Mode Input Impedance	ZRX-COM-DC	40	50	60	Ohm
Electrical Idle Threshold	VRX-IDLEDET-DIFFp-p	65	–	175	mV

Table 25. PCIe Differential Transmitter (TX) Output Specifications for Gen2

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Unit Interval	UI	199.94	–	201.06	ps
Differential p-p Tx Voltage Swing	Vtx-diff-pp 3p5dB	0.25	–	1.2	V
Differential p-p Tx Voltage Swing	Vtx-diff-pp 6dB	0.26	–	1.2	V
Tx de-emphasis Level Ratio	Vtx-de-ratio 3.5dB	3	–	4	dB
Tx de-emphasis Level Ratio	Vtx-de-ratio 6dB	5.5	–	6.5	dB
TX Peak-to-Peak Jitter	Ttx-pp-jitter	–	–	105	ps
Tx deterministic jitter > 1.5 MHz	Ttx-HF-dj-dd	–	–	0.15	UI
Transmitter Eye Including all Jitter Sources	Ttx-eye	0.75	–	–	UI
DC Differential Tx Impedance	Ztx-diff-dc	–	–	120	ohm
AC Coupling Capacitor	Ctx	75	–	200	nF

Table 26. PCIe Differential Receiver (RX) Output Specifications for Gen2

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
DC Differential Impedance	Zrx-diff-dc	80	–	120	ohm
Receiver DC Single-Ended Impedance	Zrx-dc	40	–	60	ohm
Electrical Idle Detect Threshold	Vrx-idle-det DIFFp-p	65	–	175	mV

Electrical Characteristics – HDMI

Table 27. HDMI

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
single-ended high-level output voltage	V_{OH}	AVDD = 3.3 V ± 5% RT = 50Ω ± 10%	A_{VDD}−0.01	–	A_{VDD}+0.01	V
single-ended low-level output voltage	V_{OL}		A_{VDD}−0.6	–	A_{VDD}−0.4	V
single-ended output swing voltage	V_{SWING}		400	550	600	MV_{P-P}
single-ended standby/off output voltage	V_{OFF}		A_{VDD}−0.01	–	A_{VDD}+0.01	V

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Input Clock Frequency	$f_{(IDCKP)}$	25	–	165	MHz
Input Clock Period	$T_{(IDCKP)}$	4.44	–	40	ns
Input Clock Duty Cycle	t_{DUTY}	40%	50%	60%	–
TMDS Differential Clock Jitter	$t_{(JIT)}$	–	–	0.25Tbit	ns
Overshoot	V_{os}	–	–	15%	See note
Undershoot	V_{us}	–	–	25%	See note
Output rise time (20%--80%)	t_r	75ps	–	0.4Tbit	ns
Output fall time (20%--80%)	t_f	75ps	–	0.4Tbit	ns
Inter-Pair Skew at Source Connector	$t_{SK(D)}$	–	–	0.2Tpixel	ns
Intra-Pair Skew at Source Connector	$t_{SK(CC)}$	–	–	0.15Tbit	ps

Note: % of full differential amplitude.

Electrical Characteristics – LVDS Interface

Table 28. LVDS Interface - Differential Signal AC Specifications

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Differential Output Voltage	V_{OD}	247	350	454	mV
Change in VOD Magnitude	ΔV_{OD}	–	–	50	mV
Output Common-Mode Voltage	V_{OC}	1.125	–	1.375	mV
Change in VOCM Magnitude	ΔV_{OCM}	–	–	150	mV
LVDS Low to High Transition Time	L_{LHT}	–	0.25	–	ns
LVDS High to Low Transition Time	L_{HLT}	–	0.25	–	ns
Output Pulse Position for bit 0	T_{PPOS0}	-0.2	0	0.2	ns
Output Pulse Position for bit 1	T_{PPOS1}	1.48	1.68	1.88	ns
Output Pulse Position for bit 2	T_{PPOS2}	3.16	3.36	3.56	ns
Output Pulse Position for bit 3	T_{PPOS3}	4.88	5.08	5.28	ns
Output Pulse Position for bit 4	T_{PPOS4}	6.52	6.72	6.92	ns
Output Pulse Position for bit 5	T_{PPOS5}	8.2	8.4	8.6	ns
Output Pulse Position for bit 6	T_{PPOS6}	9.88	10.08	10.28	ns

Note: Clock frequency = 85MHz

Electrical Characteristics – Display Port Interface

Table 29. Display Port Interface

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Unit Interval for High Bit Rate (2.7 Gbps / lane)	UI_High_Rate	–	370	–	ps
Unit Interval for Low Bit Rate (1.62 Gbps / lane)	UI_Low_Rate	–	617	–	ps
Link Clock down Spreading	Down_Spread_Amplitude	0	–	0.5	%
Link Clock down Spreading Frequency	Down_Spread_Frequency	30	–	33	KHz
Differential Peak-to-Peak Output Voltage Level 1	VTX-DIFFp-p-Level1	0.34	0.4	0.46	V
Differential Peak-to-Peak Output Voltage Level 2	VTX-DIFFp-p-Level2	0.51	0.6	0.68	V
Differential Peak-to-Peak Output Voltage Level 3	VTX-DIFFp-p-Level3	0.69	0.8	0.92	V
Differential Peak-to-Peak Output Voltage Level 4	VTX-DIFFp-p-Level4	1.02	1.2	1.38	V
No Pre-emphasis	VTX-PREEMP-RATIO	0.0	0.0	0.0	dB
3.5 dB Pre-emphasis Level		2.8	3.5	4.2	dB
6.0 dB Pre-emphasis Level		4.8	6.0	7.2	dB
9.5 dB Pre-emphasis Level		7.6	9.5	11.4	dB
Lane-to-Lane Output Skew at Tx Package Pins	LTX-SKEWINTER_PAIR	–	–	2	UI

Electrical Characteristics – CRT Interface

Table 30. CRT Interface – RGB

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS
High-Level Output Voltage	V_{OH}	Max. luminance, white video level voltage	665	700	770	mV
Low-Level Output Voltage	V_{OL}	Min. luminance white video level voltage	–	0	–	V
Output Rising Time	T_{OR}	–	–	–	50%	Pixel Clock Period
Output Falling Time	T_{OF}	–	–	–	50%	Pixel Clock Period
Overshoot	V_{os}	–	–	–	12%	Voltage level
Undershoot	V_{us}	–	–	–	12%	Voltage level
RBG Output Skew	T_{SKEW}	–	–	–	25%	Pixel Clock Period

Table 31. CRT Interface – HSYNC and VSYNC

PARAMETER	SYMBOL	MIN	MAX	UNITS
High-Level Output Voltage	V_{OH}	2.4	–	V
Low-Level Output Voltage	V_{OL}	0	0.5	V
Output Rising Time	T_{OR}	–	80%	Pixel Clock Period
Output Falling Time	T_{OF}	–	80%	Pixel Clock Period
Overshoot	V_{os}	–	30%	Voltage level
Undershoot	V_{us}	–	30%	Voltage level
H-Sync Output Jitter	T_{jitter}	–	15%	Pixel Clock Period

Electrical Characteristics – USB Interface

Table 32. USB Interface - Signal DC Characteristics

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Impedance	–	80	90	100	Ohm
USB Signals: Input Level for Low-speed and Full-speed Mode					
Input Low Voltage	V_{IL}	–	–	0.8	V
Input High Voltage	V_{IH}	2	–	3.6	V
Differential Input Sensitivity	V_{DI}	0.2	–	–	V
Differential Common Mode Range	V_{CM}	0.8	–	2.5	V
Single-Ended Receiver Threshold	V_{SE1}	0.8	–	–	V
USB Signals: Input Level for High-speed Mode					
HS Squelch Detection Threshold	V_{HSSQ}	100	–	150	mV
HS Disconnect Detection Threshold	V_{HSDSC}	525	–	625	mV
HS Data Signaling Common Mode Voltage Range	V_{HSCM}	-50	–	500	mV
USB Signals: Output Level for Low-speed and Full-speed Modes					
Output High Voltage	V_{OH}	2.8	–	3.6	V
Output Low Voltage	V_{OL}	0	–	0.3	V
Single-Ended Threshold	V_{OSE1}	0.8	–	–	V
Output Signal Crossover Voltage	V_{CRS}	1.3	–	2	V
USB Signals: Output Level for High-speed Modes					
HS Idle Level	V_{HSOI}	-10	–	10	mV
HS Data Signaling High	V_{HSOH}	360	–	440	mV
HS Data Signaling Low	V_{HSOL}	-10	–	10	mV
Chirp J Level	V_{CHIRPJ}	700	–	1100	mV
Chirp K Level	V_{CHIRPK}	-900	–	-500	mV

Table 33. USB Interface - Signal Electrical Characteristics (Full-speed Source)

PARAMETER	SYMBOL	MIN	MAX	UNITS
Rise Time	T_{FR}	4	20	ns
Fall Time	T_{FF}	4	20	ns
Differential Rise and Fall Time Matching	T_{FRFM}	90	111.1	%
Driver Output Resistance for driver which is not high-speed capable	Z_{DRV}	28	44	Ohm
Full-speed Data Rate for hubs and devices which are high-speed capable	$T_{FDRATHS}$	11.994	12.006	Mbps
Full-speed Data Rate for devices which are not high-speed capable	T_{FDRATE}	11.97	12.03	Mbps
Frame Interval	T_{FRAME}	0.9995	1.0005	ms
Consecutive Frame Interval Jitter	T_{RFI}	–	42	ns
Source Jitter Total (including frequency tolerance)				
To Next Transition	T_{DJ1}	-3.5	3.5	ns
For Paired Transitions	T_{DJ2}	-4	4	ns
Source SE0 Interval of EOP	T_{FEOPT}	160	175	ns
Source Jitter for Differential Transition to SE0 Transition	T_{FDEOP}	-2	5	ns
Receiver Data Jitter Tolerance				
To Next Transition	T_{JR1}	-18.5	18.5	ns
For Paired Transitions	T_{JR2}	-9	9	ns
Receiver SE0 Interval of EOP	T_{FEOPR}	82	–	ns
Width of SE0 Interval during Differential Transition	T_{FST}	–	14	ns

Table 34. USB Interface - Signal Electrical Characteristics (Low-speed Source)

PARAMETER	SYMBOL	MIN	MAX	UNITS
Rise Time	T_{LR}	75	300	ns
Fall Time	T_{LF}	75	300	ns
Differential Rise and Fall Time Matching	T_{LFRFM}	80	125	%
Low-speed Data Rate for hubs and devices which are highspeed capable	$T_{LDRATHS}$	1.49925	1.50075	Mbps
Low-speed Data Rate for devices which are not highspeed capable	T_{LDRATE}	1.4775	1.5225	Mbps
Upstream Facing Port Source Jitter Total (including frequency tolerance)				
To Next Transition	T_{UDJ1}	-95	95	ns
For Paired Transitions	T_{UDJ2}	-150	150	ns
Upstream facing port source Jitter for Differential Transition to SE0 Transition	T_{LDEOP}	-40	100	ns
Upstream Facing Port Differential Receiver Jitter				
To Next Transition	T_{DJR1}	-75	75	ns
For Paired Transitions	T_{DJR2}	-45	45	ns
Downstream Facing Port Source Jitter Total (including frequency tolerance):				
To Next Transition	T_{DDJ1}	-25	25	ns
For Paired Transitions	T_{DDJ2}	-14	14	ns
Downstream Facing Port Differential Receiver Jitter				
To Next Transition	T_{UJR1}	-152	152	ns
For Paired Transitions	T_{UJR2}	-200	200	ns
Source SE0 Interval of EOP	T_{LEOPT}	1.25	1.5	us
Receiver SE0 Interval of EOP	T_{FEOPR}	670	–	ns
Width of SE0 Interval during Differential Transition	T_{LST}	–	210	ns

Table 35. USB Interface - Signal Electrical Characteristics (High-speed Source)

PARAMETER	SYMBOL	MIN	MAX	UNITS
High Speed Signal Rate	T_{HSDRAT}	479.76	480.24	Mbps
High Speed EOP Width	–	15.625	17.7083	ns
High Speed EOP Width (Bits)	–	7.5	8.5	–
Microframe Interval	T_{HSFRAM}	124.9375	125.0625	us
High speed Output Rise Time (10% - 90%)	T_{HSR}	500	–	ps
High speed Output Fall Time (10% - 90%)	T_{HSF}	500	–	ps

Electrical Characteristics – SATA Interface

Table 36. SATA Interface – Differential Signals AC Specifications

PARAMETER	SYMBOL	MIN	MAX	UNITS
Gen I Operating Data Period	UI	666.43	670.23	ps
Gen II Operating Data Period	UI	333.22	335.12	ps
Minimum Output Voltage, GenI	V_{OMIN}	400.00	–	mVdiffp-p
Maximum Output Voltage, GenI	V_{OMAX}	–	600.00	mVdiffp-p
Minimum Output Voltage, GenII	V_{OMIN}	400.00	–	mVdiffp-p
Maximum Output Voltage, GenII	V_{OMAX}	–	700.00	mVdiffp-p
Rise Time (20% – 80% at transmitter), GenI	TR	0.15	0.41	UI
Fall Time (80% – 20% at transmitter), GenI	TF	0.15	0.41	UI
Rise Time (20% – 80% at transmitter), GenII	TR	0.20	0.41	UI
Fall Time (80% – 20% at transmitter), GenII	TF	0.20	0.41	UI
TX Differential Skew	Tskew-tx	–	20.00	ps

Table 37. OOB Specifications

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
OOB Signal Detection Threshold, GenI	Vthresh	50.00	–	200.00	mVppd
OOB Signal Detection Threshold, GenII	–	75.00	–	200.00	mVppd

Electrical Characteristics –Miscellaneous Interfaces

Table 38. Miscellaneous Interfaces

Signal Group	Signals	Reference
1	**SDIO Ports:** SDIOD[3:0], SDIOCLK, SDIOCMD, SDIOWPD **Card Reader Interface:** CR_D[7:0], CR_CLK, CR_CMD, CR_WPD **xD Card Interface:** XD_RE#, XD_CLE, XD_CE#	Refer to Table 40
2	**CPU Control Interface:** A20M#, FERR#, IGNNE#, INIT#, INTR, NMI, SLP#, SMI#, STPCLK#, NAP#, THRMTRIP#, DPSLP# **Test and Miscellaneous Signals:** TESTEN, DFTEN, BISTEN, TP[2:0]	Refer to Table 41
3	**RTC Crystal Interface:** RTCXO, RTCXI **Power State and System Reset:** RSMRST#, PWRGD **Power Management Control and Event Signal:** INTRUDER# **Test and Miscellaneous Signals:** TP	Refer to Table 42
4	**Clock Signals of Graphics & Video Processors:** DISPCLKI0, DISPCLKO0, DISPCLKI1, DISPCLKO1 **Video Capture Port Interface:** VCPD[15:0], VCPHS, VCPVS, VCPCLK **Digital Video Port 1 (DVP1) Interface:** DVP1D[15:0], DVP1HS, DVP1VS, DVP1DE, DVP1TVCLKR, DVP1CLK, DVP1TVFLD, VGPIO **LCD Panel Power and Brightness Control:** LVDSENVDD, LVDSENBL	Refer to Table 43
5	**CRT Interface:** CRTSPD, CRTSPCLK, CRTHSYNC, CRTVSYNC **LCD Panel Power and Brightness Control:** LVDSPWM **Digital Video Port 1 (DVP1) Interface:** DVPSPD, DVPSPCLK **HDMI I^2C Clock Signals :** HDMIRSPC, HDMIRSPD **HDMI SEEPROM I^2C Clock Signals :** ROMSPC, ROMSPD **Test and Miscellaneous Signals:** TP5	Refer to Table 44
6	**SMBus Interface:** SMBDT1, SMBCK1, SMBDT2, SMBCK2 **Internal Mouse / Keyboard Controller Interface:** KBDT, KBCK, MSCK, MSDT **Test and Miscellaneous Signals:** TP6	Refer to Table 45

Table 39. Miscellaneous Interfaces (cont.)

Signal Group	Signals	Reference
7	**SDIO Ports:** SDIOCD#, SDIOPWSEL, SDIOPWOFF **PCI Bus Interface:** INTA#, INTB#, INTC#, INTD#, REQ[1:0]#, PCIRST# **USB Device Mode:** USBD_DET# **USB 2.0 Interface:** USBHOC[7:0]# **Card Reader Interface:** CR_CD#, CR_PWSEL, CR_PWOFF **xD Card Interface:** XD_CD# **LPC Bus Interface:** LPCDRQ[1:0]# **High Definition Audio Interface:** AZRST#, AZSDIN[1:0] **Speaker Interface:** SPKR **General Purpose Input/Output Interface:** GPIO[11:10], GPIO[40:36] **Power Management Control and Event Signal:** RING#, SUSA#, SUSB#, SUSC#, C4PSTOP#, VRDSLP, CPUSTP#, THRM#, BATLOW#, EXTSMI#, PWRBTN#, GPWAKE#, PEXWAKE#, LID#, PME#, HDMI_CEC **Test and Miscellaneous Signals:** TP[4:3]	Refer to Table 46
8	**High Definition Audio Interface:** AZBITCLK, AZSDOUT, AZSYNC **SPI Controller Interface:** MSPIDI, MSPIDO, MSPICLK, MSPISS[1:0]#	Refer to Table 47
9	**PCI Bus Interface:** AD[31:0], CBE[3:0]#, DEVSEL#, FRAME#, IRDY#, TRDY#, STOP#, PAR, PERR#, SERR#, GNT[1:0]# **LPC Bus Interface:** LPCFRAME#, LPCAD[3:0], SERIRQ	Refer to Table 48
10	**System Memory Interface:** MEMPWROK, MEMRESET#	Refer to Table 49
11	**System Memory Interface:** MEMDET	Refer to Table 50
12	**Display Port Interface:** DP2_HPD#	Refer to Table 51
13	**Display Port Interface:** DP1_HPD#	Refer to Table 52

Table 40. Electrical Characteristics of Group 1

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS
DC supply voltage	V_{CC}	–	–	1.8	–	V
Input low voltage	V_{IL}	–	-0.3	–	0.25*VCC	V
Input high voltage	V_{IH}	–	0.625*VCC	–	VCC + 0.5	V
Low-level output voltage	V_{OL}	IOL = 0.1 mA	–	–	0.125*VCC	V
High-level output voltage	V_{OH}	IOH = -0.1 mA	0.75*VCC	–	–	V
Input Leakage current	I_L	0<Vout<VCC	–	–	±20	uA

Table 41. Electrical Characteristics of Group 2

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS
DC supply voltage	V_{TT}	–	0.9975	1.05	1.1025	V
Input low voltage	V_{IL}	–	-0.1	–	0.3*VTT	V
Input high voltage	V_{IH}	–	0.7*VTT	–	VTT+0.1	V
Output low voltage	V_{OL}	IOL = 2 mA	-0.1	0	0.15*VTT	V
Output high voltage	V_{OH}	IOH = - 0.5 mA	0.9*VTT	VTT	VTT+0.1	V

Table 42. Electrical Characteristics of Group 3

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS
DC supply voltage	V_{BAT}	–	2.3	3	3.465	V
Input low voltage	V_{IL}	–	-0.3	–	0.3*VBAT	V
Input high voltage	V_{IH}	–	0.7*VBAT	–	VBAT + 0.5	V
Power Supply Current – RTC Battery	I_{BAT}	Battery Mode	–	–	10	uA

Table 43. Electrical Characteristics of Group 4

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS
DC supply voltage	V_{CC}	–	3.135	3.3	3.465	V
Input low voltage	V_{IL}	–	-0.5	–	0.8	V
Input high voltage	V_{IH}	–	2	–	VCC + 0.5	V
Low-level output voltage	V_{OL}	IOL = 4 mA	–	–	0.55	V
High-level output voltage	V_{OH}	IOH = -1 mA	2.4	–	–	V

Table 44. Electrical Characteristics of Group 5

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS
DC supply voltage	V_{CC}	–	3.135	3.3	3.465	V
Input low voltage	V_{IL}	–	-0.5	–	0.8	V
Input high voltage	V_{IH}	–	2	–	VCC + 0.5	V
Low-level output voltage	V_{OL}	IOL = 4 mA	–	–	0.55	V
High-level output voltage	V_{OH}	IOH = - 1 mA	2.4	–	–	V

Table 45. Electrical Characteristics of Group 6

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS
DC supply voltage	V_{CC}	–	3.135	3.3	3.465	V
Input low voltage	V_{IL}	–	-0.5	–	0.8	V
Input high voltage	V_{IH}	–	2.1	–	VCC5 + 0.5	V
Low-level output voltage	V_{OL}	IOL = 6 mA	–	–	0.4	V
High-level output voltage	VOH	IOH = -1 mA	0.9*VCC	–	–	V
Input Leakage current	I_L	0<Vout<VCC	–	–	±20	uA

Table 46. Electrical Characteristics of Group 7

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS
DC supply voltage	V_{CC}	–	3.135	3.3	3.465	V
Input low voltage	V_{IL}	–	-0.5	–	0.8	V
Input high voltage	V_{IH}	–	2	–	VCC + 0.5	V
Low-level output voltage	V_{OL}	IOL = 4 mA	–	–	0.55	V
High-level output voltage	V_{OH}	IOH = -1 mA	2.4	–	–	V
Input Leakage Current	I_L	0 < Vout < VCC	–	–	±20	uA

Table 47. Electrical Characteristics of Group 8

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS
DC supply voltage	V_{CC}	–	3.135	3.3	3.465	V
Input low voltage	V_{IL}	–	-0.3	–	0.35*VCC	V
Input high voltage	V_{IH}	–	0.65*VCC	–	VCC + 0.5	V
Low-level output voltage	V_{OL}	IOL = 1.5 mA	–	–	0.1*VCC	V
High-level output voltage	V_{OH}	IOH = - 0.5 mA	0.9*VCC	–	–	V

Table 48. Electrical Characteristics of Group 9

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS
DC supply voltage	V_{CC}	–	3.135	3.3	3.465	V
Input low voltage	V_{IL}	–	-0.5	–	0.3*VCC	V
Input high voltage	V_{IH}	–	0.5*VCC	–	VCC + 0.5	V
Low-level output voltage	V_{OL}	IOL = 1.5 mA	–	–	0.1*VCC	V
High-level output voltage	V_{OH}	IOH = - 0.5 mA	0.9*VCC	–	–	V

Table 49. Electrical Characteristics of Group 10

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS
DC supply voltage	V_{CC}	–	1.425	1.5	1.89	V
Low-level output voltage	V_{OL}	IOL = 0.1 mA	–	–	0.125*VCC	V
High-level output voltage	V_{OH}	IOH = - 0.1 mA	0.75*VCC	–	–	V

Table 50. Electrical Characteristics of Group 11

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS
DC supply voltage	V_{CC}	–	1.425	1.5	1.89	V
Input low voltage	V_{IL}	–	-0.3	–	0.25*VCC	V
Input high voltage	V_{IH}	–	0.625*VCC	–	VCC + 0.5	V

Table 51. Electrical Characteristics of Group 12

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS
DC supply voltage	V_{CC}	–	3.315	3.3	3.465	V
Input low voltage	V_{IL}	–	-0.3	–	0.25*VCC	V
Input high voltage	V_{IH}	–	0.625*VCC	–	VCC + 0.5	V

Table 52. Electrical Characteristics of Group 13

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS
DC supply voltage	V_{CC}	–	2.375	2.5	2.625	V
Input low voltage	V_{IL}	–	-0.3	–	0.25*VCC	V
Input high voltage	V_{IH}	–	0.625*VCC	–	VCC + 0.5	V

AC Timing – Host Interface

Figure 5. Common Clock 1x Control Timings

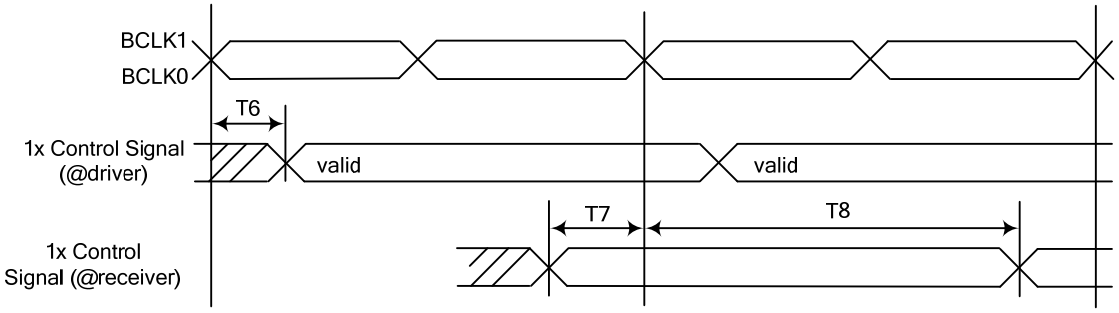


Table 53. Common Clock (1x) AC Specification

PARAMETER	SYMBOL	PRODUCT	MIN	MAX	UNITS
Valid Output Delay	T6	800MHz – VX900(M)	0.237	1.044	ns
Control Signal Setup Time	T7	800MHz – VX900(M)	1.742	–	ns
Control Signal Hold Time	T8	800MHz – VX900(M)	0.000	–	ns

Note: Common Clock 1x control signals including HADS#, HALF#, HBNR#, HBPRI#, HDBSY#, HDEFER#, HDRDY#, HHIT#, HHITM#, HLOCK#, HTRDY#, HRS[2:0]#, HDPWR#, HBREQ0# and CPURST#.

Figure 6. Source Synchronous 4X Address Timings (System Processor Source)

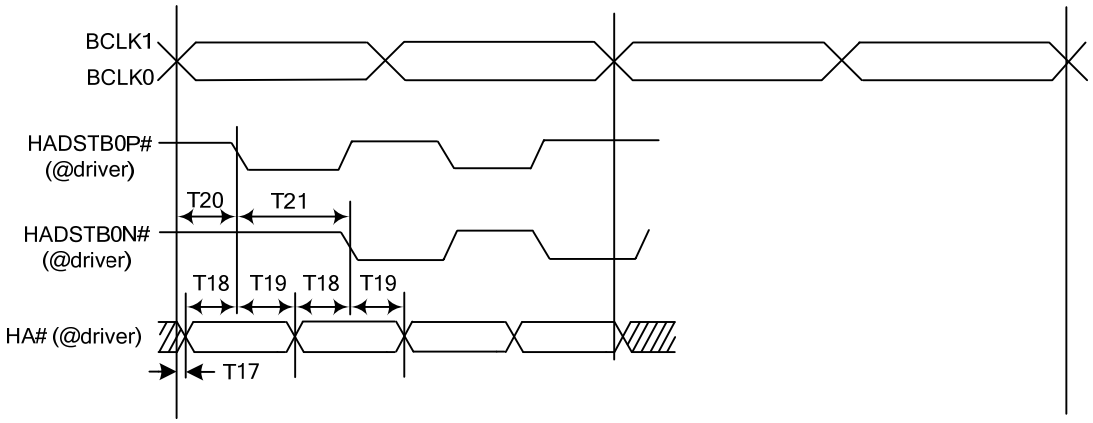


Table 54. Source Synchronous 4X AC Specification (System Processor Source)

PARAMETER	SYMBOL	PRODUCT	MIN	MAX	UNITS
Address Output Valid Delay	T17	800MHz – VX900(M)	–	2.304	ns
Address Output Valid Delay Before Address Strobe	T18	800MHz – VX900(M)	0.486	–	ns
Address Output Valid Delay After Address Strobe	T19	800MHz – VX900(M)	0.425	–	ns
Address Strobe Output Valid Delay	T20	800MHz – VX900(M)	–	2.860	ns
First Address Strobe to Subsequent Strobe	T21	800MHz – VX900(M)	–	1.300	ns

Note: HA# signals including HA[16:3]#, HABI#, HAHI[1:0]# and HREQ[2:0]#.

Figure 7. Source Synchronous 4X Address Timings (System Processor Target)

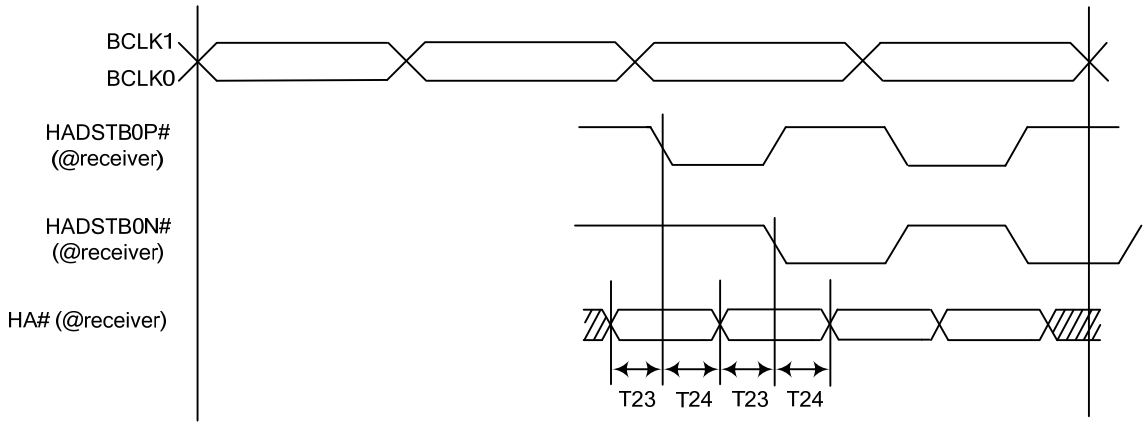


Table 55. Source Synchronous 4X AC Specification (System Processor Target)

PARAMETER	SYMBOL	PRODUCT	MIN	UNITS
Address Input Setup Time	T23	800MHz – VX900(M)	0.467	ns
Address Input Hold Time	T24	800MHz – VX900(M)	0.481	ns

Note: HA# signals including HA[16:3]#, HABI#, HAHI[1:0]# and HREQ[2:0]#.

Figure 8. Source Synchronous 4X Data Timings (System Processor Source)

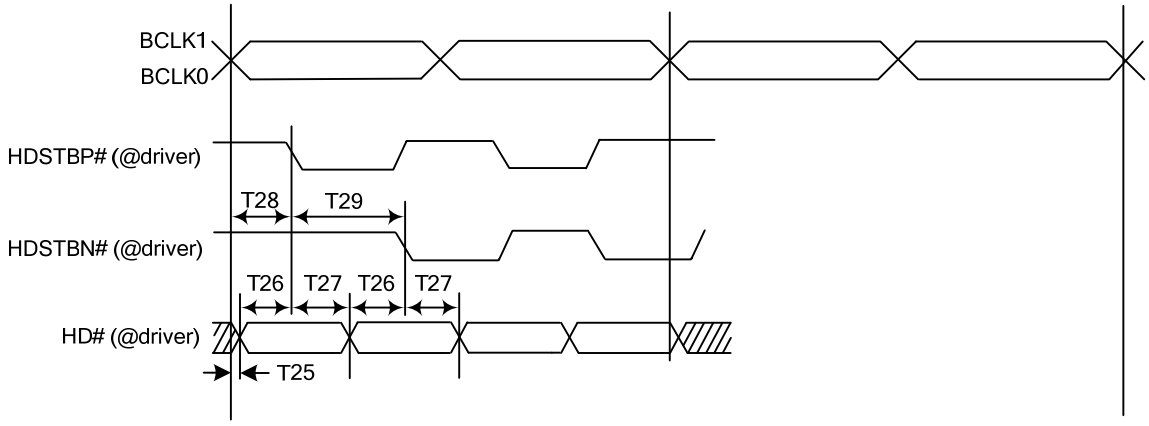


Table 56. Source Synchronous 4X AC Specification (System Processor Source)

PARAMETER	SYMBOL	PRODUCT	MIN	MAX	UNITS	NOTES
Data Output Valid Delay	T25	800MHz – VX900(M)	–	2.217	ns	2
Data Output Valid Delay Before Data Strobe	T26	800MHz – VX900(M)	0.480	–	ns	
Data Output Valid Delay After Data Strobe	T27	800MHz – VX900(M)	0.369	–	ns	
Data Strobe Output Valid Delay	T28	800MHz – VX900(M)	–	2.864	ns	2
First Data Strobe to Subsequent Strobe	T29	800MHz – VX900(M)	–	1.300	ns	

Note: HD# Signals including HD[63:0]# and HDBI[3:0]#.

Figure 9. Source Synchronous 4X Data Timings (System Processor Target)

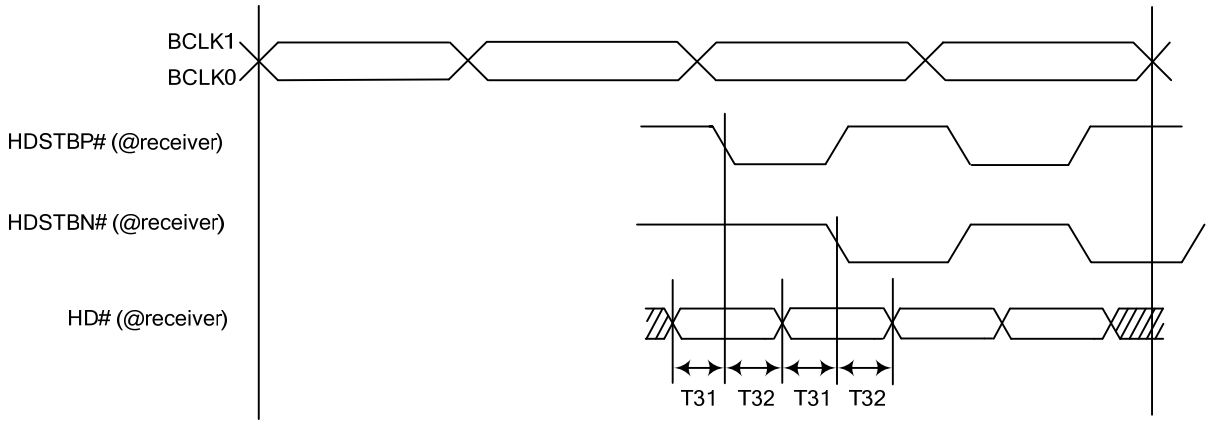


Table 57. Source Synchronous 4X AC Specification (System Processor Target)

PARAMETER	SYMBOL	PRODUCT	MIN	UNITS
Data Input Setup Time	T31	800MHz – VX900(M)	0.471	ns
Data Input Hold Time	T32	800MHz – VX900(M)	0.507	ns

Note: HD# Signals including HD[63:0]# and HDBI[3:0]#.

AC Timing – System Memory Interface

Figure 10. DDR3 Data and Strobe Timing (System Processor Target)

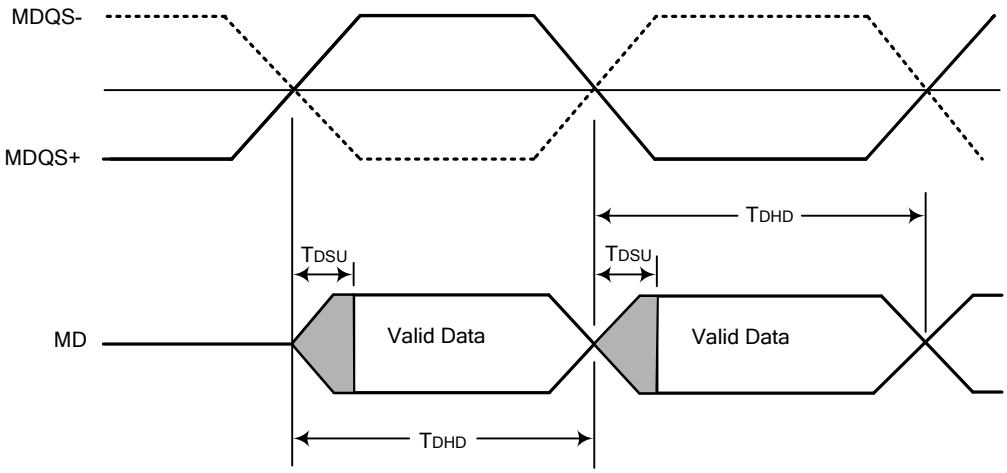


Table 58. DDR3 Data and Strobe AC Specification

PARAMETER	SYMBOL	PRODUCT	MIN	UNITS
Input Setup Time	T_{DSU}	DDR3-800 – VX900M	0	ns
		DDR3-1066 – VX900	0	
Input Hold Time	T_{DHD}	DDR3-800 – VX900M	1.097	ns
		DDR3-1066 – VX900	0.823	

Note: MD signals including MD[63:0], MDQM[7:0].

Figure 11. DDR3 Data and Strobe Timing (System Processor Source)

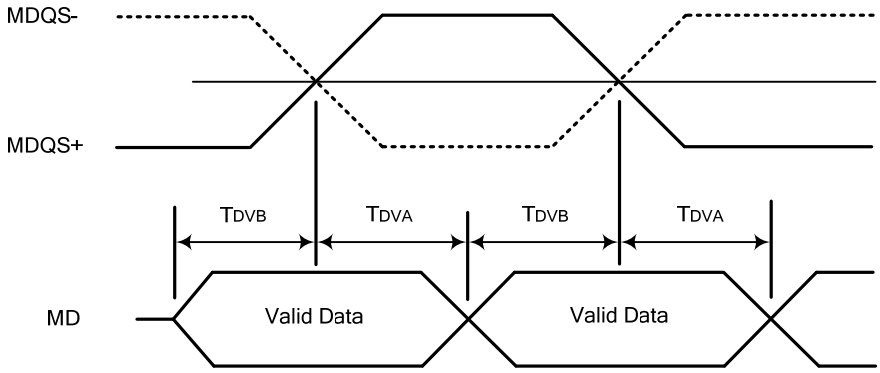


Table 59. DDR3 Data and Strobe AC Specification

PARAMETER	SYMBOL	PRODUCT	MIN	UNITS
Data Output Valid Delay After Data Strobe	T_{DVA}	DDR3-800 – VX900M	0.305	ns
		DDR3-1066 – VX900	0.229	
Data Output Valid Delay Before Data Strobe	T_{DVB}	DDR3-800 – VX900M	0.389	ns
		DDR3-1066 – VX900	0.292	

Note: MD signals including MD[63:0], MDQM[7:0]

Figure 12. DDR3 Command Signals Timing

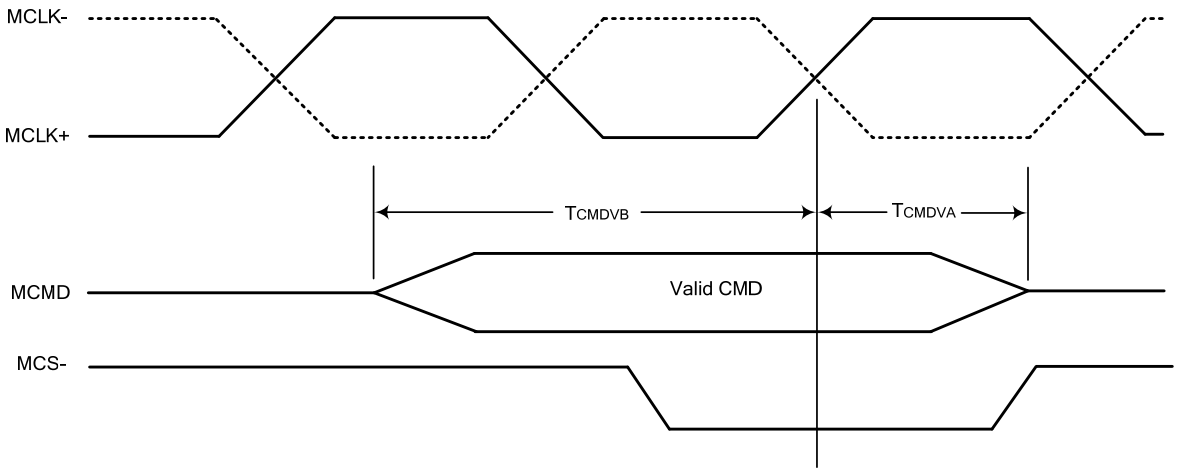


Table 60. DDR3 Command AC Specification

PARAMETER	SYMBOL	PRODUCT	MIN	UNITS
Command Signals Output Valid Delay After MCLKO	T_{CMDVA}	DDR3-800 – VX900M	1.901	ns
		DDR3-1066 – VX900	0.740	
Command Signals Output Valid Delay Before MCLKO	T_{CMDVB}	DDR3-800 – VX900M	2.826	ns
		DDR3-1066 – VX900	2.071	

Note: MCMD signals including MA[13:0], MBA[2:0], MSRAS#, MSCAS# and MSWE#.

Figure 13. DDR3 Control Signals Timing

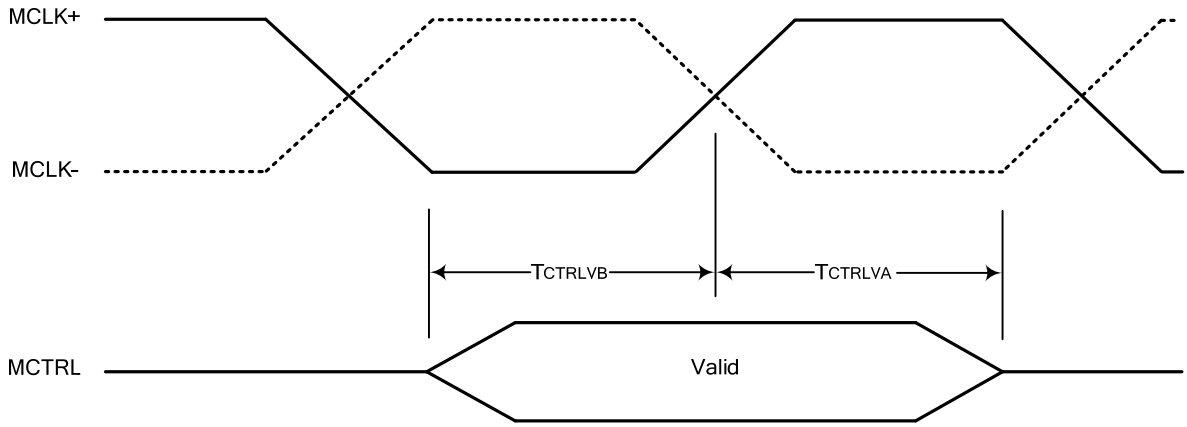


Table 61. DDR3 Control Signal AC Specification

PARAMETER	SYMBOL	PRODUCT	MIN	UNITS
Control Signals Output Valid Delay After MCLKO	T_{CTRLVA}	DDR3-800 – VX900M	1.001	ns
		DDR3-1066 – VX900	0.726	
Control Signals Output Valid Delay Before MCLKO	T_{CTRLVB}	DDR3-800 – VX900M	0.964	ns
		DDR3-1066 – VX900	0.723	

Note: MCTRL signals including MODT[3:0], MCS[3:0]# and MCKE[3:0].

Strapping Timing Requirement

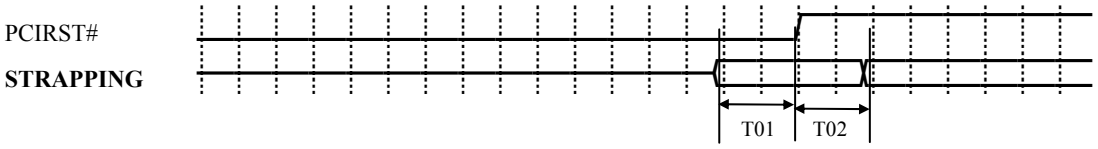


Figure 14. Strapping Timing Requirement

Symbol	Parameter	Min	Max	Unit	Note
T01	STRAPPING signals valid to PCIRST# asserted	0	—	us	1,2
T02	STRAPPING signals valid to PCIRST# de-asserted	1	—	us	1,2

Note:

1. VIL (max)=0.8V, VIH (min) = 2.0V.
2. Keep Strapping signals unchanged between PCIRST# sampling windows.
3. Signals strapped by PCIRST#： GPO39, AZBITCLK, AZSDOUT, AZSYNC and MSPISS1#

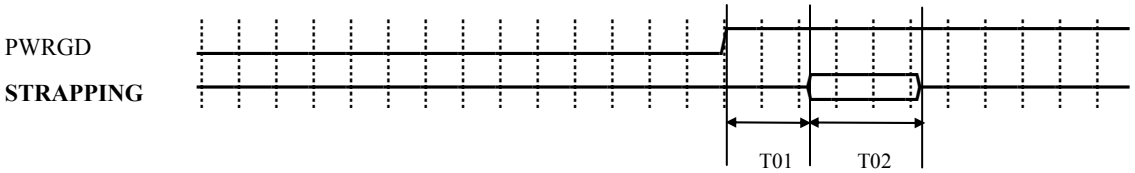


Figure 15. Strapping Timing Requirement

Symbol	Parameter	Min	Max	Unit	Note
T01	STRAPPING signals delay from PWRGD	2	3	RTCCLK	1,2
T02	STRAPPING signals sampling window	3	—	RTCCLK	1,2

Note:

1. VIL (max)=0.8V, VIH (min) = 2.0V.
2. Keep Strapping signals unchanged in sampling windows.
3. Signals strapped by PWRGD: GPO36, GPO37, GPO38, C4PSTOP#, GPO40 and MSPISS0#

Power Sequence

The power rails mentioned in this section are measured at 90% nominal voltage. Signals are measured at 50% swing point.

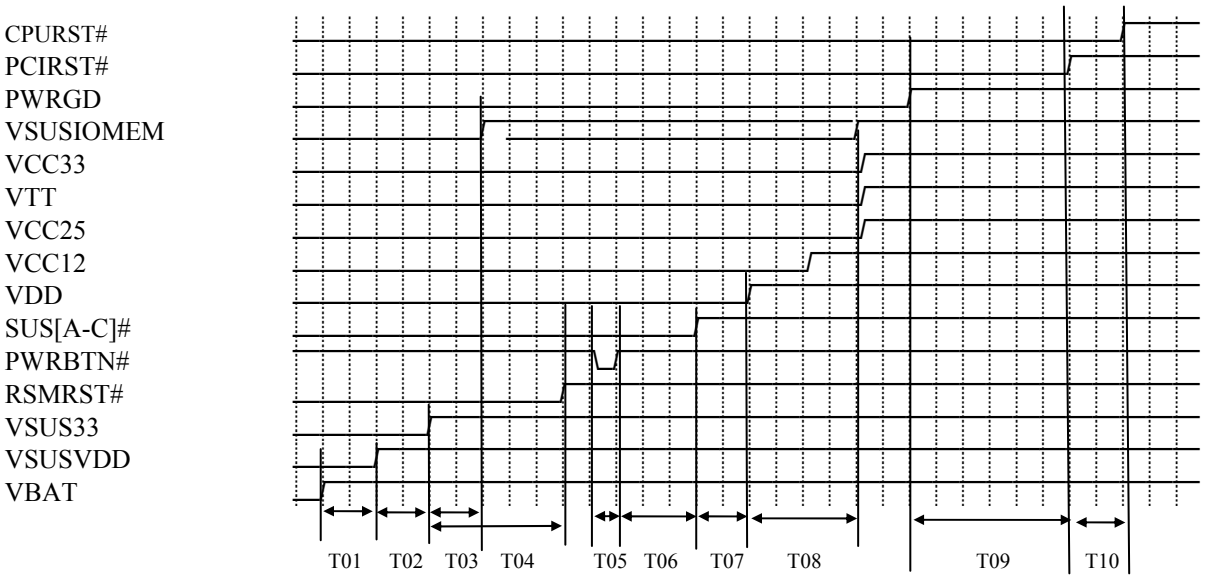


Figure 16. Power On Sequence and Reset Signal Timing

Symbol	Parameter	Min	Max	Unit	Note
T01	VBAT supply active to VSUSVDD supply active	0	—	ms	
T02	VSUSVDD supply active to VSUS33 supply active	0	—	ms	
T03	VSUS33 supply active to VSUS18MEM	0	—	ms	
T04	VSUS33 supply active to RSMRST# supply active	5	—	ms	
T05	PWRBTN# active width	1	—	RTCCLK	
T06	PWRBTN# rising to SUS[A-C]# inactive	—	5	RTCCLK	
T07	SUS[A-C]# rising to VDD supply active	0	—	ms	
T08	VDD supply active to VTT/VCC12/VCC25/VCC33 supply active	1	—	ms	
T09	PWRGD supply active to PCIRST# inactive	7	—	ms	
T10	PCIRST# supply active to CPURST# inactive	12	—	us	

Note:

1. VSUSVDD must be powered up before VSUS33 is powered up.
2. VDD must be powered up before VTT/VCC12/VCC25/VCC33 are powered up.
3. VCC12 must be powered up before VCC25 is powered up.
4. No timing interdependencies between VSUSIOMEM and VTT/VCC12/VCC33/VCC25.
5. CPURST# is de-asserted after the completion of ROMSIP cycles.

6. The power-on sequence is suggested for following connections.

Voltage
VCC12 VCCA12SATA VCCA12PEX VCCA12DP1
VCC25 VCCA25HCK VCCA25DAC VCCA25PLLDISP VCCA25LVDS VCCA25PLLLVDS VCCA25SATA VCCA25DP1 VCCA25PEX
VCC33 VCC33 VCC33VGA
VSUSVDD VSUSVDD VSUSAVDDUSBH VSUSVDDMEM
VSUS33 VSUS33 VSUSA33USBH

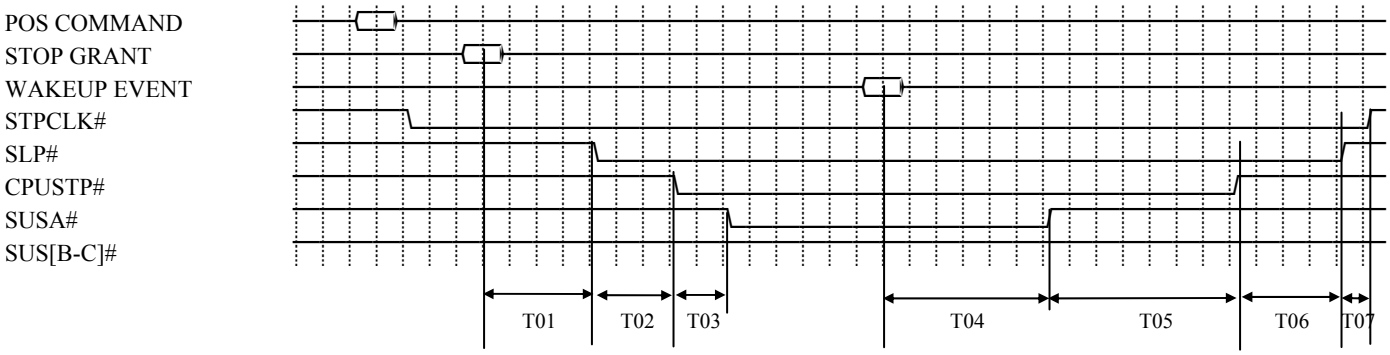


Figure 17. Power On Suspend (S1) and Resume Sequence

Symbol	Parameter	Min	Max	Unit	Note
T01	STOP GRANT to SLP# active	—	3	RTCCLK	
T02	SLP# active to CPUSTP# active	—	2	RTCCLK	
T03	CPUSTP# active to SUSA# active	—	1	RTCCLK	
T04	Wakeup Event to SUSA# inactive	2	5	RTCCLK	
T05	SUSA# inactive to CPUSTP# inactive	1	2	ms	1
T06	CPUSTP# inactive to SLP# inactive	155	310	us	2
T07	SLP# inactive to STPCLK# inactive	—	1	RTCCLK	

Note:

1. If D17F0 Rx95[7] = 0, the minimum delay is 16ms and the maximum delay is 32ms.
2. If D17F0 Rx95[7] = 0, the minimum delay is 1us and the maximum delay is 2ms.

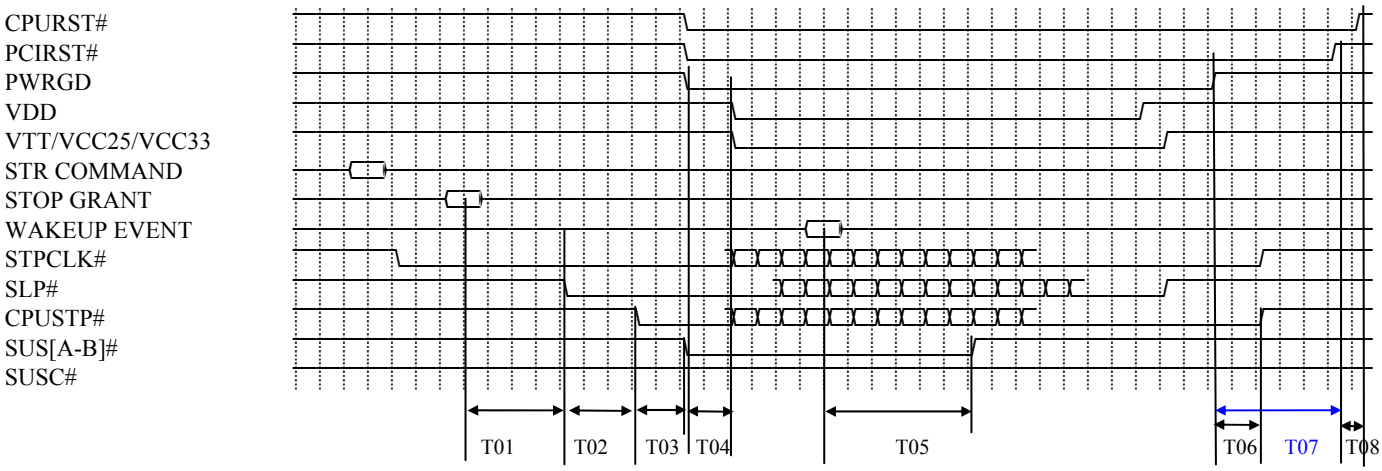


Figure 18. Suspend to RAM (S3) and Resume Sequence

Symbol	Parameter	Min	Max	Unit	Note
T01	STOP GRANT to SLP# active	—	3	RTCCLK	
T02	SLP# active to CPUSTP# and PCISTP# active	—	2	RTCCLK	
T03	CPUSTP# and PCISTP# active to SUS[A-B]# active	—	1	RTCCLK	
T04	PWRGD inactive to VDD supply inactive	0	—	ms	
T05	Wakeup Event to SUS[A-B]# inactive	2	5	RTCCLK	
T06	PWRGD active to CPUSTP/PCISTP# inactive	1.03	2.03	ms	1
T07	PWRGD active to PCIRST# inactive	7	—	ms	
T08	PCIRST# inactive to CPURST# inactive	12	—	us	

Note:

1. If D17F0Rx95[7]=0, the minimum delay is 16ms and maximum delay is 32ms.
2. SLP# and STPCLK# will be de-asserted before de-assertion of CPURST#.
3. PWRGD is asserted minimum 30ms after all system powers are ready.
4. Please note that the detailed ramp up sequence of VTT/VCC12/VCC25/VCC33/VDD conforms to Figure 16.

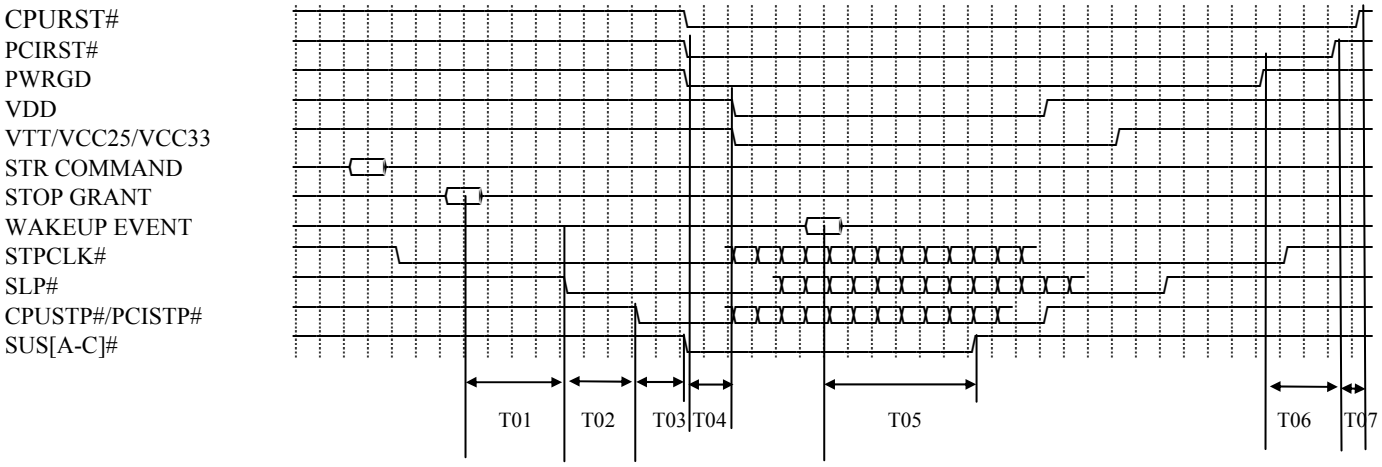


Figure 19. Suspend to DISK (S4) and Resume Sequence

Symbol	Parameter	Min	Max	Unit	Note
T01	STOP GRANT to SLP# active		3	RTCCLK	
T02	SLP# active to CPUSTP# and PCISTP# active		2	RTCCLK	
T03	CPUSTP# and PCISTP# active to SUS[A-C]# active		1	RTCCLK	
T04	PWRGD inactive to VDD supply inactive	0	—	ms	
T05	Wakeup Event to SUS[A-C]# inactive	2	5	RTCCLK	
T06	PWRGD active to PCIRST# inactive	7		ms	
T07	PCIRST# inactive to CPURST# inactive	12		us	1

Note:

1. CPURST# is de-asserted after the completion of ROMSIP cycles.
2. SLP# and STPCLK# will be de-asserted before de-assertion of CPURST#.
3. PWRGD is asserted minimum 30ms after all system powers are ready.
4. Please note that the detailed ramp up sequence of VTT/VCC12/VCC25/VCC33/VDD conforms to Figure 16.

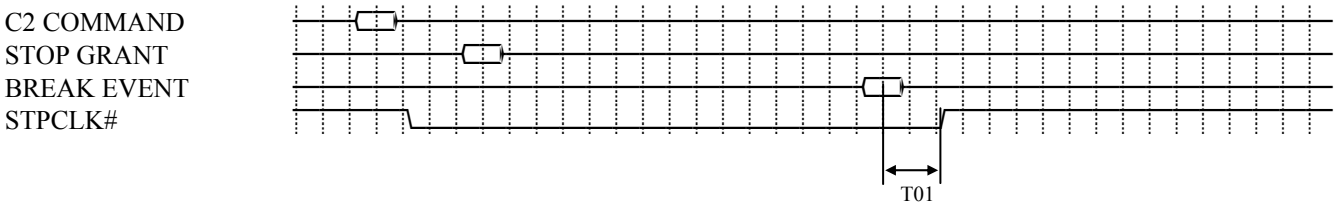


Figure 20. CPU C2 Sequence

Symbol	Parameter	Min	Max	Unit	Note
T01	Break Event to STPCLK# inactive	2	—	PCICLK	

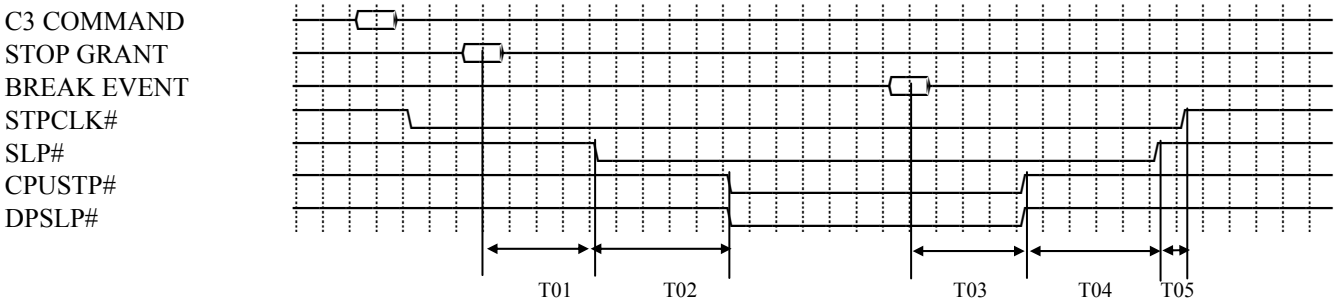


Figure 21. CPU C3 Sequence

Symbol	Parameter	Min	Max	Unit	Note
T01	STOP GRANT to SLP# active	0.83	1.66	us	1, 2
T02	SLP# active to CPUSTP# and DPSLP# active	1	1.25	us	1, 2
T03	Break Event to CPUSTP# and DPSLP# inactive	0.93	1.66	us	1, 2
T04	CPUSTP# and DPSLP# inactive to SLP# inactive	15	23.5	us	1, 3
T05	SLP# inactive to STPCLK# inactive	0.83	0.83	ns	1, 2

Note:

1. Refer to System Programming Manual for detail of configuration settings.
2. The time sequence with 2T (1T=0.03us) offset is valid.
3. The time sequence with 2T (1T=0.83us) offset is valid.

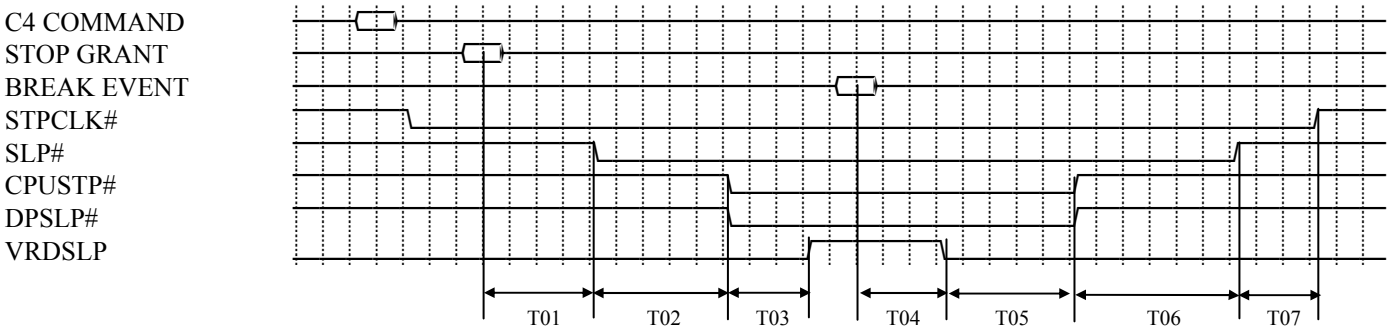


Figure 22. CPU C4 Sequence

Symbol	Parameter	Min	Max	Unit	Note
T01	STOP GRANT to SLP# active	0.83	1.66	us	1, 2
T02	SLP# active to CPUSTP# and DPSLP# active	1	1.25	us	1, 2
T03	CPUSTP# and DPSLP# active to VRDSLP active	0.63	0.83	us	1, 2
T04	Break Event to VRDSLP inactive	0	0.83	us	1, 2
T05	VRDSLP inactive to CPUSTP# and DPSLP#	20	25	us	1, 3, 4
T06	CPUSTP# and DPSLP# inactive to SLP# inactive	15	23.5	us	1, 3
T07	SLP# inactive to STPCLK# inactive	0.83	0.83	us	1, 2

Note:

1. Refer to System Programming Manual for detail of configuration settings.
2. The time sequence with 2T (1T=0.03us) offset is valid.
3. The time sequence with 2T (1T=0.83us) offset is valid.
4. If D17F0 RxE5[7] = 0, the minimum delay is 35us and the maximum delay is 45us.

Power Consumption – by Each Power Rail

Table 62. Power Consumption

Power Rails	Current (mA)			
	Min	Avg.	Max.	EDP
VCC33	26.20	30.80	58.90	64
VSUS33	2.11	2.23	4.80	8
VCC33VGA	0.25	1.43	54.00	108 (Note4)
VCCA33USBD	16.08	18.15	19.28	30
VSUSA33USBH	9.90	43.05	152.60	200
VCCCR	–	14.77	15.87	32
VCCA25HCK	8.87	8.90	11.96	23.92
VCCA25LVDS	–	53.97	54.02	81.03
VCCA25PLLLVDS	–	7.73	8.76	13.14
VCCA25DAC	63.74	63.67	73.40	110.1
VCCA25PLLDISP	42.52	42.85	44.60	89.2
VCCA25DP1	16.20	135.40	144.00	216
VCCA25PEX *(VX900M)*	**30.08**	**185.50**	**185.57**	**222.7**
VCCA25PEX *(VX900: 4 x1-lane PCIe ports)*	**30.08**	**210.16**	**302.62**	**363.1**
VCCA25PEX *(VX900: 3x1-lane ports+1x8-lane port)*	**30.08**	**560**	**561**	**673**
VCCA25SATA	13.40	86.43	86.64	173.3
VCCA12SATA	5.31	34.68	43.31	51.972
VCCA12DP1	5.10	16.81	18.00	27
VCCA12PEX *(VX900M)*	**33.19**	**95.76**	**95.96**	**115.15**
VCCA12PEX *(VX900: 4 x1-lane PCIe ports)*	**33.19**	**116.81**	**132.76**	**159.31**
VCCA12PEX *(VX900: 3x1-lane ports+1x8-lane port)*	**33.19**	**250**	**250**	**300**
VSUSIOMEM *(VX900M)*	**157.02**	**437.17**	**678.00**	**1017**
VSUSIOMEM *(VX900)*	**157.02**	**437.17**	**700.00**	**1050**
VDD (1.0V) *(VX900M)*	**778.71**	**999.80**	**1194.00**	**1791**
VDD (1.2V) *(VX900)*	**1156.00**	**1473.00**	**2062**	**3093**
VSUSVDD VSUSVDDMEM	3.59	3.79	4.04	5
VSUSAVDDUSBH	1.07	1.17	2.22	3
VCCA12USBD	0.80	1.01	1.60	3
VTT	42.77	51.11	85.20	161

Note:

1. If the power rails are not specified, it is for both VX900 and VX900M.
2. The data are resulted from measuring several certain software applications.
3. It is recommended for system power designer to refer to EDP.
4. The maximum value is considered when DVP is enabled.

Package Thermal Simulation

Heat sink is required for this chip.
The compression force limit of this chip is 100 psi.

Package Specification	Simulation Result			
	Thermal Characterization (unit: ºC/W)			
	Vflow (m/s)	Ψjt	Ψjb	Rja
FCBGA 31 x 31 mm	0.00	0.01	8.17	15.12
	1.00	0.01	7.84	11.11
	2.00	0.01	7.52	9.82
	4.00	0.01	7.18	8.75
	JESD-51	Rjc	Rjb	-
		0.01	8.65	-

Boundary Conditions

Vflow (m/s) Velocity of external flow passing by the package

Temperature

T_j (ºC) Junction temperature

T_a (ºC) Ambient temperature

T_b (ºC) PCB reference temperature

T_c (ºC) Case temperature of the package (the top center of the package surface for single-chip device)

Thermal Resistance

Ψjt Thermal characterization parameter from device junction to the top center of the package surface

Ψjt = (T_j-T_c) / Power

Ψjb Thermal characterization parameter from device junction to board

Ψjb = (T_j-T_b) / Power

Rja Thermal characterization parameter from device junction to air

Rja = (T_j-T_a) / Power

Rjb Thermal characterization parameter from device junction to PCB

Rjb = (T_j-T_b) / Power

Rjc Thermal characterization parameter from device junction to the top center of the package surface under infinite heatsink test environment per JESD-51

Rjc = (T_j-T_c) / Power

NAND TREE

This chapter describes the NAND tree test configuration, condition and procedure for VX900 Series.

NAND Trees

There are four NAND trees implemented in VX900 series. The NAND Tree input pin sequences and output pins are listed in tables below.

NAND Tree Test Mode Set Up

TESTEN = 1b

DFTEN = 1b

BISTEN = 1b

TP2 = 0

TP3 = 1b

NAND Tree Test Procedure

Step 1: Set up NAND Tree test mode
Pull the following signals **low**: TP2
Pull the following signals **high**: TESTEN, DFTEN, BISTEN and TP3.

Step 2: Apply power to the chip

Step 3: Set all NAND Tree input pins to high level.

Step 4: Change the voltage level of NAND Tree input pin to **low** following the sequence listed in the NAND Tree table. The voltage level of the NAND Tree output will be toggled accordingly one by one. Through monitoring the output pin state, the unconnected or stuck pins can be located if there is any.

Table 63. NAND Tree Group 0 & 1

Ball#	NAND Tree 0	Output	Note	Ball#	NAND Tree 1	Output	Note
J04	HD60#	= sig0[0];	Start of NAND Tree 0	B12	HDPWR#	= sig1[0];	Start of NAND Tree 1
H04	HD61#	= sig0[2];		E14	DPSLP#	= sig1[2];	
E01	HD52#	= sig0[3];		A12	NAP#	= sig1[3];	
H01	HD51#	= sig0[4];		C13	THRMTRIP#	= sig1[4];	
J01	HD58#	= sig0[5];		A13	SLP#	= sig1[5];	
J03	HD59#	= sig0[6];		J15	CLK66M	= sig1[6];	
H03	HD62#	= sig0[7];		G15	HRS0#	= sig1[7];	
G02	HDBI3#	= sig0[8];		A14	STPCLK#	= sig1[8];	
F03	HDSTB3P#	= sig0[9];		D15	HLOCK#	= sig1[9];	
G03	HDSTB3N#	= sig0[10];		B14	INIT#	=sig1[10];	
C01	HD53#	= sig0[11];		F16	HDRDY#	=sig1[11];	
E02	HD49#	= sig0[12];		F15	HBNR#	=sig1[12];	
B02	HD48#	= sig0[13];		C14	SMI#	=sig1[13];	
D01	HD54#	= sig0[14];		E16	HHITM#	=sig1[14];	
C02	HD50#	= sig0[15];		H16	HRS1#	=sig1[15];	
F04	HD63#	= sig0[16];		C15	A20M#	=sig1[16];	
D03	HD57#	= sig0[17];		J18	HCLK-	=sig1[17];	
G01	HD55#	= sig0[18];		J17	HCLK+	=sig1[18];	
G06	HD42#	= sig0[19];		B16	FERR#	=sig1[19];	
G05	HD32#	= sig0[20];		B15	NMI	=sig1[20];	
E05	HD41#	= sig0[21];		A16	INTR	=sig1[21];	
A02	HD36#	= sig0[22];		G18	HADS#	=sig1[22];	
F06	HD33#	= sig0[23];		D16	HBPRI#	=sig1[23];	
C03	HD43#	= sig0[24];		E17	HDBSY#	=sig1[24];	
D05	HD47#	= sig0[25];		G17	HHIT#	=sig1[25];	
H08	HD39#	= sig0[26];		C17	HDEFER#	=sig1[26];	
C05	HDBI2#	= sig0[27];		D17	HTRDY#	=sig1[27];	
D04	HDSTB2P#	= sig0[28];		A17	IGNNE#	=sig1[28];	
E04	HDSTB2N#	= sig0[29];		G19	HALF#	=sig1[29];	
B03	HD34#	= sig0[30];		G21	HBREQ0#	=sig1[30];	
E06	HD44#	= sig0[31];		C18	HA6#	=sig1[31];	
H09	HD37#	= sig0[32];		D19	HA3#	=sig1[32];	
G07	HD46#	= sig0[33];		E18	HREQ1#	=sig1[33];	
F07	HD38#	= sig0[34];		F18	HREQ0#	=sig1[34];	
B04	HD35#	= sig0[35];		B18	HREQ2#	=sig1[35];	
H05	HD40#	= sig0[36];		A21	HA7#	=sig1[36];	
H07	HD45#	= sig0[37];		A20	HA13#	=sig1[37];	
A04	HD28#	= sig0[38];		B20	HA5#	=sig1[38];	
B06	HD30#	= sig0[39];		C21	HA4#	=sig1[39];	
C06	HD27#	= sig0[40];		F20	HABI#	=sig1[40];	
A05	HD19#	= sig0[41];		D20	HADSTB0P#	=sig1[41];	
E08	HD31#	= sig0[42];		E20	HADSTB0N#	=sig1[42];	
B07	HD24#	= sig0[43];		E21	HA9#	=sig1[43];	
A06	HD18#	= sig0[44];		G22	HA11#	=sig1[44];	
A08	HD26#	= sig0[45];		F23	HAHI1#	=sig1[45];	

(To be continued)

(Continued for Group 0 & 1)

Ball#	NAND Tree 0	Output	Note	Ball#	NAND Tree 1	Output	Note
B08	HDBI1#	= sig0[46];		F22	HA15#	=sig1[46];	
D07	HDSTB1P#	= sig0[47];		D23	HAHI0#	=sig1[47];	
C07	HDSTB1N#	= sig0[48];		A22	HA10#	=sig1[48];	
A10	HD17#	= sig0[49];		C23	HA16#	=sig1[49];	
B10	HD16#	= sig0[50];		B23	HA14#	=sig1[50];	
C09	HD29#	= sig0[51];		B22	HA8#	=sig1[51];	
D08	HD25#	= sig0[52];		E22	HA12#	=sig1[52];	
A09	HD23#	= sig0[53];		F34	MA1		(output)
B11	HD22#	= sig0[54];					
C10	HD20#	= sig0[55];					
D11	HD21#	= sig0[56];					
G09	HD12#	= sig0[57];					
E09	HD10#	= sig0[58];					
F10	HD15#	= sig0[59];					
F08	HD5#	= sig0[60];					
H12	HD14#	= sig0[61];					
D09	HD11#	= sig0[62];					
E10	HD1#	= sig0[63];					
C11	HD13#	= sig0[64];					
G10	HDBI0#	= sig0[65];					
G11	HDSTB0P#	= sig0[66];					
H11	HDSTB0N#	= sig0[67];					
D12	HD2#	= sig0[68];					
F12	HD7#	= sig0[69];					
H13	HD0#	= sig0[70];					
F11	HD9#	= sig0[71];					
G13	HD8#	= sig0[72];					
D13	HD3#	= sig0[73];					
E13	HD6#	= sig0[74];					
E12	HD4#	= sig0[75];					
E38		MA0	(output)				

Table 64. NAND Tree Group 2 & 3

Ball#	NAND Tree 2	Output	Note	Ball#	NAND Tree 3	Output	Note
C25	MD57	= sig2[0];	Start of NAND Tree 2	G27	MD46	= sig3[0];	Start of NAND Tree 3
G25	MD61	= sig2[1];		D29	MD44	= sig3[1];	
H24	MD58	= sig2[2];		D28	MD42	= sig3[2];	
H25	MD60	= sig2[3];		H27	MD43	= sig3[3];	
A25	MDQM7	= sig2[4];		A29	MDQM5	= sig3[4];	
B24	MDQS7+	= sig2[5];		H29	MDQS5+	= sig3[5];	
A24	MDQS7-	= sig2[6];		G29	MDQS5-	= sig3[6];	
H23	MD59	= sig2[7];		C29	MD41	= sig3[7];	
E24	MD62	= sig2[8];		A30	MD40	= sig3[8];	
D24	MD56	= sig2[9];		B30	MD45	= sig3[9];	
G23	MD63	= sig2[10];		F27	MD47	= sig3[10];	
C27	MD53	= sig2[11];		F30	MD37	= sig3[11];	
B27	MD49	= sig2[12];		E32	MD33	= sig3[12];	
E26	MD52	= sig2[13];		E30	MD32	= sig3[13];	
D27	MD48	= sig2[14];		G30	MD36	= sig3[14];	
C26	MDQM6	= sig2[15];		E29	MDQM4	= sig3[15];	
A28	MDQS6+	= sig2[16];		D31	MDQS4+	= sig3[16];	
B28	MDQS6-	= sig2[17];		D32	MDQS4-	= sig3[17];	
B26	MD54	= sig2[18];		C30	MD35	= sig3[18];	
F26	MD50	= sig2[19];		B31	MD39	= sig3[19];	
G26	MD51	= sig2[20];		C31	MD38	= sig3[20];	
A26	MD55	= sig2[21];		A32	MD34	= sig3[21];	
N34	MD28	= sig2[22];		D33	MODT0	= sig3[22];	
M37	MD29	= sig2[23];		B34	MODT2	= sig3[23];	
M35	MD25	= sig2[24];		C34	MSCAS#	= sig3[24];	
M38	MD24	= sig2[25];		C33	MA13	= sig3[25];	
M34	MDQM3	= sig2[26];		A33	MCLKO2-	= sig3[26];	
M33	MDQS3+	= sig2[27];		A34	MCLKO2+	= sig3[27];	
L33	MDQS3-	= sig2[28];		F32	MODT1	= sig3[28];	
M31	MD27	= sig2[29];		H32	MEMRESET#	= sig3[29];	
L32	MD26	= sig2[30];		H33	MEMDET	= sig3[30];	
N32	MD30	= sig2[31];		E33	MCS3#	= sig3[31];	
N31	MD31	= sig2[32];		C35	MCLKO5+	= sig3[32];	
R35	MD21	= sig2[33];		B35	MCLKO5-	= sig3[33];	
R32	MD23	= sig2[34];		J32	MODT3	= sig3[34];	
P37	MD16	= sig2[35];		D37	MCLKO0+	= sig3[35];	
T33	MD20	= sig2[36];		C37	MCLKO0-	= sig3[36];	
P36	MDQM2	= sig2[37];		E34	MSWE#	= sig3[37];	
P33	MDQS2+	= sig2[38];		D35	MCS0#	= sig3[38];	
R33	MDQS2-	= sig2[39];		K33	MCS1#	= sig3[39];	
P38	MD17	= sig2[40];		B36	MBA0	= sig3[40];	
P32	MD22	= sig2[41];		A36	MCS2#	= sig3[41];	
R31	MD19	= sig2[42];		A37	MSRAS#	= sig3[42];	
N38	MD18	= sig2[43];		D36	MBA1	= sig3[43];	
U38	MD13	= sig2[44];		K34	MA5	= sig3[44];	

(To be continued)

(Continued for Group 2 & 3)

Ball#	NAND Tree 2	Output	Note	Ball#	NAND Tree 3	Output	Note
U34	MD10	= sig2[45];		C38	MCLKO3+	= sig3[45];	
U32	MD11	= sig2[46];		B38	MCLKO3-	= sig3[46];	
U36	MD12	= sig2[47];		K36	MEMPWROK	= sig3[47];	
T35	MDQM1	= sig2[48];		K38	MBA2	= sig3[48];	
R36	MDQS1+	= sig2[49];		J38	MA12	= sig3[49];	
R37	MDQS1-	= sig2[50];		H35	MA8	= sig3[50];	
T37	MD9	= sig2[51];		G35	MA4	= sig3[51];	
T38	MD8	= sig2[52];		J34	MA7	= sig3[52];	
U35	MD14	= sig2[53];		J35	MA11	= sig3[53];	
T34	MD15	= sig2[54];		J36	MCKE0	= sig3[54];	
W32	MD4	= sig2[55];		E36	MCLKO1-	= sig3[55];	
W33	MD0	= sig2[56];		F36	MCLKO1+	= sig3[56];	
W35	MD1	= sig2[57];		H36	MA9	= sig3[57];	
W36	MD5	= sig2[58];		G37	MA6	= sig3[58];	
V38	MDQM0	= sig2[59];		F38	MCLKO4-	= sig3[59];	
V36	MDQS0+	= sig2[60];		G38	MCLKO4+	= sig3[60];	
V37	MDQS0-	= sig2[61];		H37	MA14	= sig3[61];	
V34	MD6	= sig2[62];		E37	MA10	= sig3[62];	
V33	MD7	= sig2[63];		L36	MCKE3	= sig3[63];	
V32	MD2	= sig2[64];		L35	MCKE2	= sig3[64];	
U31	MD3	= sig2[65];		L37	MCKE1	= sig3[65];	
F35	MA2		(output)	K37	MA15	= sig3[66];	
				G34	MA3		(output)

Table 65. NAND Tree Group 4 & 5

Ball#	NAND Tree 4	Output	Note	Ball#	NAND Tree 5	Output	Note
Y37	LPCAD3	= sig4[0];	Start of NAND Tree 4	AF32	CBE3#	= sig5[0];	Start of NAND Tree 5
Y35	LPCAD1	= sig4[1];		AF31	AD22	= sig5[1];	
Y34	INTD#	= sig4[2];		AJ35	CBE1#	= sig5[2];	
Y38	LPCAD2	= sig4[3];		AL36	FRAME#	= sig5[3];	
W37	LPCDRQ0#	= sig4[4];		AM37	AD17	= sig5[4];	
AA38	LPCFRAME#	= sig4[5];		AG32	AD23	= sig5[5];	
AA37	LPCDRQ1#	= sig4[6];		AM36	AD18	= sig5[6];	
AA36	AZSYNC	= sig4[7];		AG33	AD30	= sig5[7];	
W31	SERIRQ	= sig4[8];		AK35	TRDY#	= sig5[8];	
AA35	LPCAD0	= sig4[9];		AJ34	AD31	= sig5[9];	
AB38	AZSDOUT	= sig4[10];		AG31	INTA#	= sig5[10];	
AA34	USBCLK	= sig4[11];		AH33	REQ0#	= sig5[11];	
Y31	SPKR	= sig4[12];		AK34	STOP#	= sig5[12];	
AC36	MSPICLK	= sig4[13];		AJ33	GNT0#	= sig5[13];	
AB36	THRM#	= sig4[14];		AL35	AD19	= sig5[14];	
AB37	C4PSTOP#	= sig4[15];		AH32	REQ1#	= sig5[15];	
AC37	MSPIDI	= sig4[16];		AK33	CBE2#	= sig5[16];	
AD38	MSPISS0#	= sig4[17];		AJ32	SERR#	= sig5[17];	
AD37	MSPISS1#	= sig4[18];		AK32	AD16	= sig5[18];	
AB35	GPIO11	= sig4[19];		AJ31	GNT1#	= sig5[19];	
AD36	GPO39	= sig4[20];		AP37	CR_CLK	= sig5[20];	
Y30	VRDSLP	= sig4[21];		AR38	CR_D6	= sig5[21];	
AA30	CPUSTP#	= sig4[22];		AT38	XD_ALE	= sig5[22];	
Y33	AZBITCLK	= sig4[23];		AN36	CR_D2	= sig5[23];	
AC35	MSPIDO	= sig4[24];		AR37	CR_D4	= sig5[24];	
AE36	GPO37	= sig4[25];		AT37	CR_D1	= sig5[25];	
AA31	INTC#	= sig4[26];		AM35	CR_D3	= sig5[26];	
AD35	GPO38	= sig4[27];		AN35	CR_D5	= sig5[27];	
AD34	GPO40	= sig4[28];		AR36	CR_D0	= sig5[28];	
AC34	GPO36	= sig4[29];		AU37	CR_WPD#	= sig5[29];	
AC30	HDMI_CEC	= sig4[30];		AP36	CR_D7	= sig5[30];	
AA32	GPIO10	= sig4[31];		AV37	XD_CLE	= sig5[31];	
AB33	INTB#	= sig4[32];		AR35	XD_CE#	= sig5[32];	
AA33	PCICLK	= sig4[33];		AU36	XD_RE#	= sig5[33];	
AB32	PERR#	= sig4[34];		AM34	CR_CMD	= sig5[34];	
AC31	AD20	= sig4[35];		AP33	PME#	= sig5[35];	
AE37	AD1	= sig4[36];		AN34	BATLOW#	= sig5[36];	
AF38	AD4	= sig4[37];		AT36	CR_CD#	= sig5[37];	
AF37	AD9	= sig4[38];		AP35	RSVD	= sig5[38];	
AC33	AD3	= sig4[39];		AL33	SUSA#	= sig5[39];	
AC32	AD7	= sig4[40];		AT35	CR_PWOFF	= sig5[40];	
AG38	AD12	= sig4[41];		AV36	XD_CD#	= sig5[41];	
AE35	AD8	= sig4[42];		AU35	CR_PWSEL	= sig5[42];	
AF36	AD10	= sig4[43];		AM33	SUSC#	= sig5[43];	
AD31	AD0	= sig4[44];		AL32	EXTSMI#	= sig5[44];	

(To be continued)

(Continued for Group 4 & 5)

Ball#	NAND Tree 4	Output	Note	Ball#	NAND Tree 5	Output	Note
AD30	AD6	= sig4[45];		AR34	LID#	= sig5[45];	
AG37	AD11	= sig4[46];		AV35	RING#	= sig5[46];	
AG36	AD27	= sig4[47];		AN33	PWRBTN#	= sig5[47];	
AH37	AD13	= sig4[48];		AM32	PEXWAKE#	= sig5[48];	
AD33	AD21	= sig4[49];		AU34	SMBALRT#	= sig5[49];	
AH36	AD14	= sig4[50];		AR33	SMBDT1	= sig5[50];	
AJ37	AD15	= sig4[51];		AT34	SMBCK1	= sig5[51];	
AF35	AD2	= sig4[52];		AP32	USBD_DET#	= sig5[52];	
AG35	AD24	= sig4[53];		AL31	PCIRST#	= sig5[53];	
AF34	AD25	= sig4[54];		AU33	SMBDT2	= sig5[54];	
AJ36	PAR	= sig4[55];		AR32	USBD_PDN	= sig5[55];	
AH35	AD26	= sig4[56];		AT32	AZSDIN0	= sig5[56];	
AL37	IRDY#	= sig4[57];		AT33	SMBCK2	= sig5[57];	
AD32	AD5	= sig4[58];		AM31	SUSB#	= sig5[58];	
AE33	CBE0#	= sig4[59];		AU32	AZRST#	= sig5[59];	
AG34	AD29	= sig4[60];		AT31	AZSDIN1	= sig5[60];	
AK36	DEVSEL#	= sig4[61];		AV31	KBCK	= sig5[61];	
AF33	AD28	= sig4[62];		AU31	KBDT	= sig5[62];	
W30	TP4		(output)	AT30	MSDT	= sig5[63];	
				AV30	MSCK	= sig5[64];	
				AN32	GPWAKE#	= sig5[65];	
				AV28	USBHOC0#	= sig5[66];	
				AV27	USBHOC1#	= sig5[67];	
				AT29	USBHOC2#	=sig5[68];	
				AU29	USBHOC6#	=sig5[69];	
				AU27	USBHOC4#	=sig5[70];	
				AT28	USBHOC5#	=sig5[71];	
				AU28	USBHOC7#	=sig5[72];	
				AR28	USBHOC3#	=sig5[73];	
				AL30	TP6		(output)

Table 66. NAND Tree Table Group 6 & 7

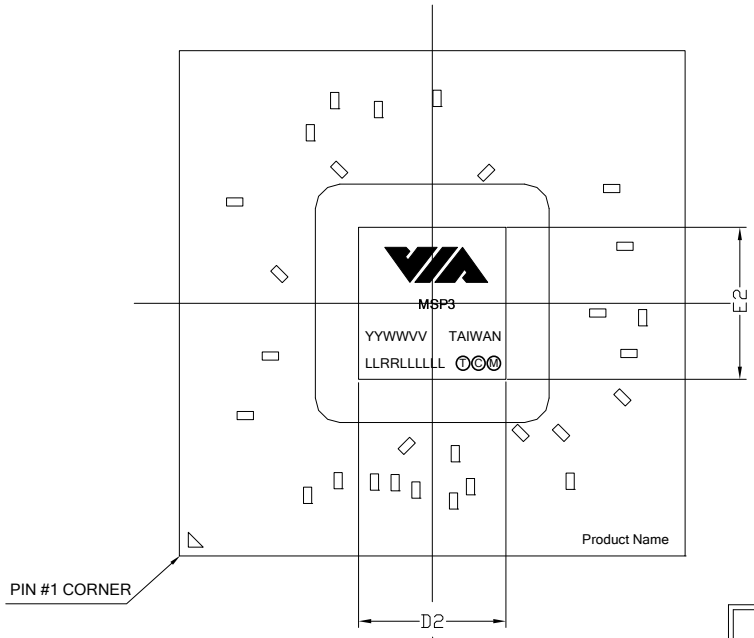
Ball#	NAND Tree 6	Output	Note	Ball#	NAND Tree 7	Output	Note
AJ05	VCPD13	= sig7[0];	Start of NAND Tree 6			= sig7[0];	Start of NAND Tree 7
AH06	VCPD14	= sig7[1];				= sig7[1];	
AJ04	VCPD11	= sig7[2];				= sig7[2];	
AH05	VCPD12	= sig7[3];				= sig7[3];	
AJ03	VCPD5	= sig7[4];				= sig7[4];	
AJ02	VCPD7	= sig7[5];				= sig7[5];	
AG05	VCPD10	= sig7[6];				= sig7[6];	
AH03	VCPD2	= sig7[7];				= sig7[7];	
AH02	VCPD4	= sig7[8];				= sig7[8];	
AH01	VCPD3	= sig7[9];				= sig7[9];	
AJ01	VCPD6	= sig7[10];				= sig7[10];	
AF05	VCPD8	= sig7[11];				= sig7[11];	
AG02	VCPVS	= sig7[12];				= sig7[12];	
AG03	VCPD1	= sig7[13];				= sig7[13];	
AG04	VCPD9	= sig7[14];				= sig7[14];	
AG01	VCPD0	= sig7[15];				= sig7[15];	
AF02	VCPHS	= sig7[16];				= sig7[16];	
AG08	VCPD15	= sig7[17];				= sig7[17];	
AG07	VCPCLK	= sig7[18];				= sig7[18];	
AF06	DVP1TVFLD	= sig7[19];				= sig7[19];	
AF01	DVP1D3	= sig7[20];				= sig7[20];	
AF04	VGPIO	= sig7[21];				= sig7[21];	
AF07	DVP1DE	= sig7[22];				= sig7[22];	
AE05	DVP1D11	= sig7[23];				= sig7[23];	
AE06	DVP1D13	= sig7[24];				= sig7[24];	
AE03	DVP1D2	= sig7[25];				= sig7[25];	
AE09	DVP1D4	= sig7[26];				= sig7[26];	
AE08	DVP1D15	= sig7[27];				= sig7[27];	
AE01	DVP1VS	= sig7[28];				= sig7[28];	
AD05	DVP1D12	= sig7[29];				= sig7[29];	
AD04	DVP1HS	= sig7[30];				= sig7[30];	
AE02	DVP1D1	= sig7[31];				= sig7[31];	
AD09	DVP1D5	= sig7[32];				= sig7[32];	
AD03	DVP1D0	= sig7[33];				= sig7[33];	
AD02	DVP1TVCLKR	= sig7[34];				= sig7[34];	
AD07	DVP1D7	= sig7[35];				= sig7[35];	
AD08	DVP1D6	= sig7[36];				= sig7[36];	
AE07	DVP1D14	= sig7[37];				= sig7[37];	
AD01	DVP1CLK	= sig7[38];				= sig7[38];	
AC05	DVP1D10	= sig7[39];				= sig7[39];	
AC04	DVP1D9	= sig7[40];				= sig7[40];	
AC06	DVP1D8	= sig7[41];				= sig7[41];	
AB02	HDMIRSPD	= sig7[42];				= sig7[42];	
AC01	ROMSPD	= sig7[43];				= sig7[43];	
AC03	ROMSPC	= sig7[44];				= sig7[44];	

(To be continued)

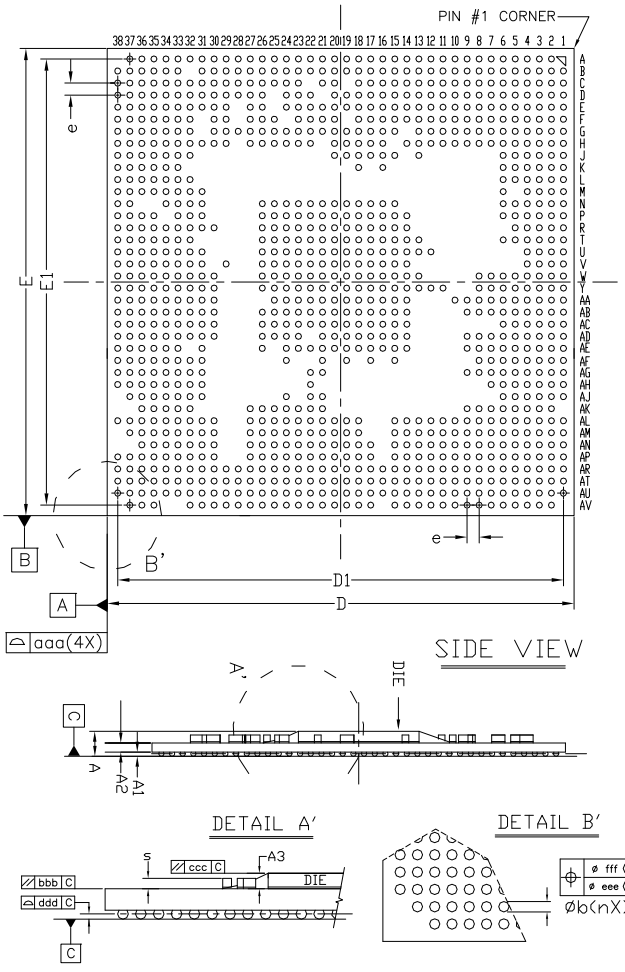
(Continued for Group 6 & 7)

Ball#	NAND Tree 6	Output	Note	Ball#	NAND Tree 7	Output	Note
AB03	DVICTL3	= sig7[45];				= sig7[45];	
AB07	LVDSENVDD	= sig7[46];				= sig7[46];	
AB01	HDMIRSPC	= sig7[47];				= sig7[47];	
AB06	LVDSENBL	= sig7[48];				= sig7[48];	
AA07	LVDSPWM	= sig7[49];				= sig7[49];	
AB04	DVPSPD	= sig7[50];				= sig7[50];	
AB05	DVPSPCLK	= sig7[51];				= sig7[51];	
AA04	DISPCLKI1	= sig7[52];				= sig7[52];	
AA05	DISPCLKO1	= sig7[53];				= sig7[53];	
Y06	DISPCLKI0	= sig7[54];				= sig7[54];	
Y07	DPCLK	= sig7[55];				= sig7[55];	
Y08	CLK14M	= sig7[56];				= sig7[56];	
AA06	DISPCLKO0	= sig7[57];				= sig7[57];	
AA08	CRTHSYNC	= sig7[58];				= sig7[58];	
AB09	CRTSPD	= sig7[59];				= sig7[59];	
AA09	CRTVSYNC	=sig7[60];				=sig7[60];	
AA10	CRTSPCLK	=sig7[61];				=sig7[61];	
		=sig7[62];				=sig7[62];	
		=sig7[63];				=sig7[63];	
		=sig7[64];				=sig7[64];	
		=sig7[65];				=sig7[65];	
B26	MD54		(output)				

MECHANICAL SPECIFICATIONS



Product Name = VX900, VX900H, VX900M, VX900MH
Y = Date Code Year
W = Date Code Week
V = Chip Version
L = Lot Code
R = Revision Code
T = True Green Only



	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOM.	MAX.
TOTAL THICKNESS	A	1.79	1.88	1.97
STAND OFF	A1	0.27	–	0.37
SUBSTRATE THICKNESS	A2	0.61	0.68	0.75
DIE THICKNESS	A3	0.85	0.88	0.90
BODY SIZE	D		31.00	BSC
	E		31.00	BSC
BALL DIAMETER			0.40	
BALL WIDTH (BALL MOUNTED)	b	0.38	–	0.48
BALL PITCH	e		0.80	BSC
BALL COUNT	n		1089	
EDGE BALL CENTER TO CENTER	D1		29.60	BSC
	E1		29.60	BSC
EXPOSE DIE SIZE	D2		9.05	BSC
	E2		9.32	BSC
PACKAGE EDGE TOLERANCE	aaa		0.10	
SUBSTRATE FLATNESS	bbb		0.10	
TOP FLATNESS	ccc		0.20	
COPLANARLTY	ddd		0.20	
BALL OFFSET (PACKAGE)	eee		0.15	
BALL OFFSET (BALL)	fff		0.10	
COMPONENT HEIGHT(MAX.)	s	–	–	0.65

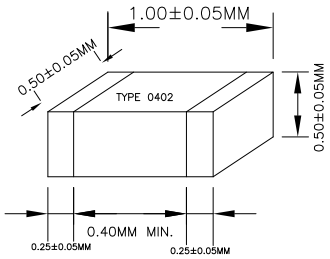


Figure 23. Mechanical Specifications – FCBGA-1089 Ball Grid Array Package