



# Data Sheet

## VT8237S South Bridge

Revision 1.02  
August 1, 2007

VIA TECHNOLOGIES, INC.

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## REVISION HISTORY

Document Release	Date	Revision	Initials
1.0	7/11/07	Initial external release	SV
1.01	7/17/07	Updated DC characteristics	SV
1.02	8/1/07	Updated signal description: Internal Keyboard Controller <b><u>B0D15F0</u></b> Added register Rx83[5:3]	SV

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# VT8237S SOUTH BRIDGE

High Definition Audio  
1 GB/Sec Ultra V-Link Interface  
Eight USB 2.0 / USB 1.1 Ports  
Dual Channel Serial ATA 2.5 / RAID Controller  
UltraDMA-133 Master Mode EIDE Controller  
10 / 100 MAC with MII Interface  
Keyboard / Mouse Controller  
LPC, SMBus, Serial IRQ, PnP, ACPI / SPI  
PC2001 Compliant Enhanced Power Management

## PRODUCT FEATURES

- **Inter-Operable with a Wide Variety of VIA North Bridges**
  - Combines with P4M800 CE / P4M800 Pro / P4M890 / P4M900 / PT890 CE for high performance Pentium 4 based server / workstation / desktop designs
  - Combines with K8M890 CE / K8T890 CF / K8T900 for high performance Athlon 64 (Opteron) based server / workstation / desktop designs
  - Combines with VN800 / VN890 for complete Pentium 4 based mobile designs
  - Combines with KN400A / K8N890 CE for complete Athlon / Athlon 64 (Opteron) based mobile designs
  - Combines with CN700 / CN800 for complete featured, power efficient VIA C7 based desktop / mobile / embedded designs
- **High Bandwidth 1 GB/Sec Ultra V-Link Controller**
  - Supports 8-bit / 16-bit, 66 MHz, 2x, 4x and 8x transfer modes, Ultra V-Link Client interface with 1 GB/Sec maximum bandwidth
  - Full duplex commands with separate Strobe / Command Request / Data split transaction
  - Auto Client Retry to eliminates V-Link Host-Client Retry cycles
  - Intelligent V-Link transaction protocol to minimize data wait-state, throttle transfer latency to avoid data overflow
  - Highly efficient V-Link arbitration with minimum overhead; all V-Link transactions have predictable cycle length with known Command / Data duration
  - Auto connect / reconnect capability and dynamic stop for minimum power consumption
  - Parity checking to insure correct data transfers
- **Ultra DMA-133 / 100 / 66 Bus Master EIDE Controller**
  - Dual channel hard disk controller supporting up to four Enhanced IDE devices
  - Data transfer rate up to 133 MB/sec to cover PIO mode 4, multi-word DMA mode 2 and UltraDMA-133 interface
  - Dual DMA engines for concurrent dual channel operation
  - Full scatter gather capability
  - Supports ATAPI compliant devices including DVD devices
  - Supports PCI native and ATA compatibility modes
  - Bus master programming interface for SFF-8038i rev.1.0 and Windows-95 compliant
  - Complete software driver support

- **Dual Channel Serial ATA 2.5 / RAID Controller**

- Complies with Serial ATA Specification Revision 2.5
- Dual Channel master mode
- On-chip two-channel Serial ATA (S-ATA) PHY for support of up to two S-ATA devices directly
- S-ATA devices can be configured in multiple RAID configurations – supports RAID Level 0, RAID Level 1 and JBOD
- S-ATA drive transfer rate is capable of up to 300 MB/s per channel (serial speed of 3 Gbit/s)
- External Crystal input for Serial ATA port operation
- Supports defer spin up and port multiplier

- **Fast Ethernet Controller**

- High performance PCI master interface with scatter / gather and bursting capability
- Standard MII interface to external PHY receiver
- 1 / 10 / 100 MHz full and half duplex operation
- Independent 2K byte FIFOs for receive and transmit
- Flexible dynamically loadable EEPROM algorithm
- Physical, Broadcast, and Multicast address filtering using hashing function
- Magic packet and wake-on-address filtering
- Software controllable power down

- **SPI Controller**

- Support SPI flash memory control (reference specification of M25P20 of ST)
- Without a preceding write enable command
- Support to write 256 bytes in one shot
- Support external plug programmer to update BIOS data
- Support one SPI flash memory
- Support Dynamic clock stop
- Provide data buffers of 16 bytes

- **APIC Controller**

- Integrated APIC controller with 24 interrupt channels
- FSB delivery function (Index 03 –Boot Configuration: FSB/APIC Bus Delivery Select)
- Compatible with Novell OS

- **Universal Serial Bus Controller**

- Eight USB 2.0 ports with integrated PHY
- One USB 2.0 root hub and four USB 1.1 root hubs
- USB 2.0 and Enhanced Host Controller Interface (EHCI) v1.0 compliant
- USB 1.1 and Universal Host Controller Interface (UHCI) v1.1 compatible
- Integrated physical layer transceivers with optional over-current detection status on USB inputs
- Eighteen level (doublewords) data FIFO with full scatter and gather capability
- Legacy keyboard and PS/2 mouse support
- One USB 2.0 High-Speed debug port

- **High Definition (HD) Audio Controller**

- High definition audio controller with 192 KHz sample rate, 32-bit per sample and up to 8 channels
- Microsoft UAA (Universal Audio Architecture) driver support
- Up to four independent playback streams and audio codecs
- Multiple recording channels for array microphone
- Supports jack sensing / retasking

- **System Management Bus Interface**

- Compliant with System Management Bus (SMBus) Revision 2.0
- I<sup>2</sup>C devices compatible
- Supports SMBus Address Resolution Protocol (ARP) by using host commands through software
- Supports slave interface for external SMBus masters to control resume events
- Supports Alert On LAN II through a SMBus-interfaced register

- **Concurrent PCI Bus Controller**

- 33 MHz operation
- Supports up to six PCI masters
- Peer concurrency
- Concurrent multiple PCI master transactions; i.e., allow PCI masters from both PCI buses active at the same time
- Zero wait state PCI master and slave burst transfer rate
- PCI to system memory data streaming up to 132Mbyte/sec (north bridge data transfer via high speed Ultra V-Link)
- PCI master snoop ahead and snoop filtering
- Eight DW of CPU to PCI posted write buffers
- Byte merging in the write buffers to reduce the number of PCI cycles and to create further PCI bursting possibilities
- Enhanced PCI command optimization (MRL, MRM, MWI, etc.)
- Four lines of post write buffers from PCI masters to DRAM
- Sixteen levels (double-words) of prefetch buffers from DRAM for access by PCI masters
- Delay transaction from PCI master accessing DRAM
- Transaction timer for fair arbitration between PCI masters (granularity of two PCI clocks)
- Symmetric arbitration between Host/PCI bus for optimized system performance
- Complete steerable PCI interrupts
- PCI-2.3 compliant, 32 bit 3.3V PCI interface with 5V tolerant inputs

- **Sophisticated Mobile Power Management**

- ACPI 3.0 and APM v1.2 Compliant
- Supports OnNow power management
- Supports Intel Enhanced SpeedStep™ with dedicated pins
- Supports PCI Express WAKE suspend resume event
- Supports CPU clock throttling and clock stop during ACPI C0 / C1 / C2 / C3 states
- Supports PCI clock run, Power Management Enable (PME) control, and PCI / CPU clock generator stop control
- Supports multiple system suspend types: power-on suspends (POS) with flexible CPU / PCI bus reset options, suspend to DRAM (STR), and suspend to disk (soft-off), all with hardware automatic wake-up
- Multiple suspend power plane controls and suspend status indicators
- Integrates an idle timer, a peripheral timer and a general purpose timer, plus a 24/32-bit ACPI compliant timer
- Supports normal, doze, sleep, suspend and conserve modes
- Global and local device power control
- Supports system event monitoring with two event classes
- Primary and secondary interrupt differentiation for individual channels
- Dedicated input pins for power and sleep buttons, external modem ring indicator, and notebook lid open/close for system wake-up
- 32 general purpose input ports and 28 output ports
- Multiple internal and external SMI sources for flexible power management models
- Enhanced integrated real time clock (RTC) with date alarm, month alarm, and century field
- Thermal alarm on external temperature sensing circuit
- I/O pad leakage control

- **Plug and Play Functions**

- Steerable PCI interrupts
- Steerable interrupts for integrated peripheral controllers
- Microsoft Windows Vista™, Windows XPTM, Windows NTTM, Windows 2000™, Windows 98™ and plug and play BIOS compliant

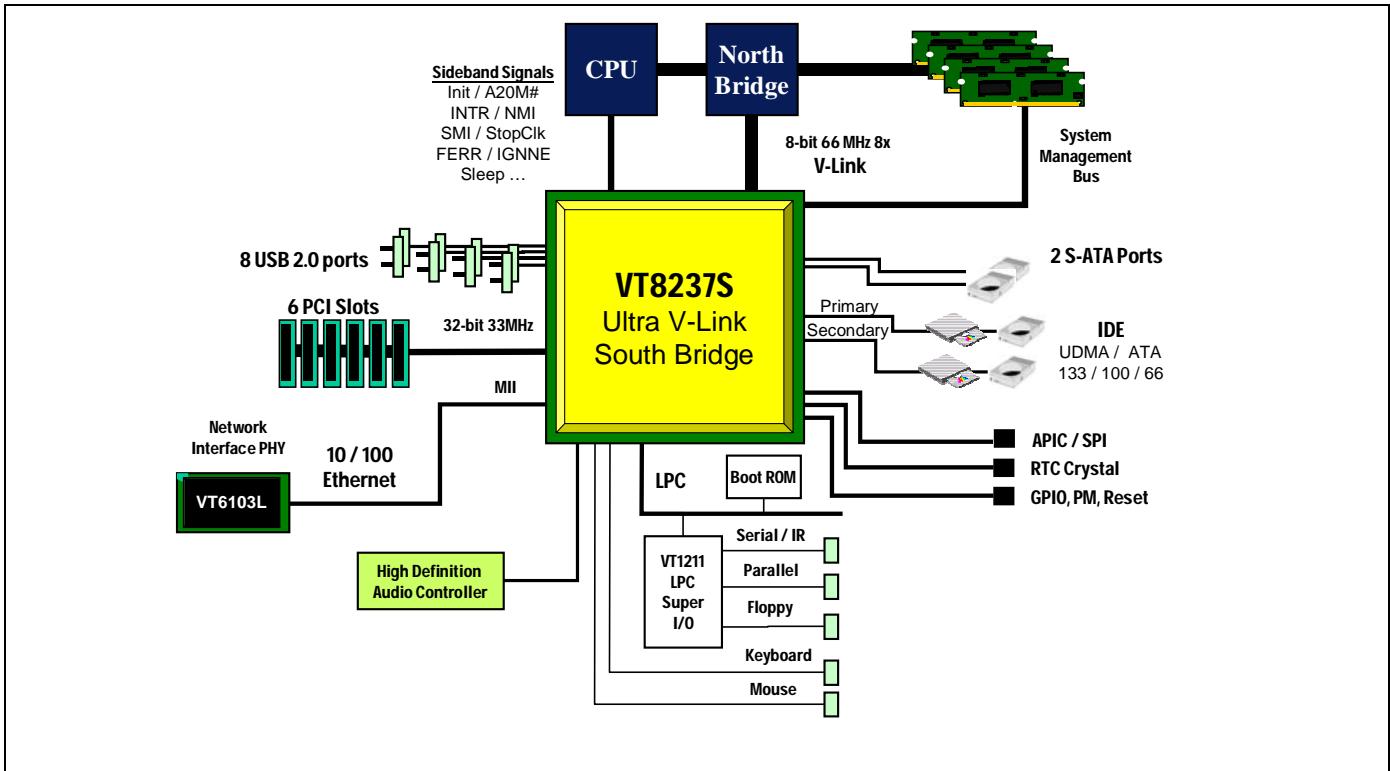
- **Integrated Legacy Functions**

- Integrated Keyboard Controller with PS2 mouse support
- Integrated DS12885-style Real Time Clock with extended 256 byte CMOS RAM and Day/Month Alarm for ACPI
- Integrated DMA, timer, and interrupt controller
- Serial IRQ for docking and non-docking applications
- Fast reset and Gate A20 operation

- **Built-in NAND-tree pin scan test capability**

- **0.15um, 1.5V, low power CMOS process**
- **Single chip 27 x 27 mm, 1.0 mm ball pitch, 542 ball PBGA**

## VT8237S SYSTEM OVERVIEW



**Figure 1. VT8237S System Block Diagram**

The VT8237S South Bridge is a high integration, high performance, power-efficient and high compatibility device that supports Intel and non-Intel based processor to Ultra V-Link bus bridge functionality to make a complete Microsoft PC2001-compliant PCI/LPC system. The VT8237S includes standard intelligent peripheral controllers:

- **Dual-Channel Serial ATA 2.5 / RAID Controller**  
The Serial ATA / RAID controller supports RAID Level 0, RAID Level 1 and JBOD, and complies with Serial ATA Specification Revision 2.5 with 3 Gbits/sec data transfer rates.
- **Dual-Channel Enhanced IDE Controller**  
In addition to standard PIO and DMA mode operation, the VT8237S also supports the UltraDMA-133, 100 and 66 standards, allows reliable data transfer rates up to 133 MB/sec. The IDE controller is SFF-8038i v1.0 and Microsoft Windows-family compliant.
- **IEEE 802.3 compliant 10 / 100 Mbps Ethernet MAC with MII interface to VIA VT6103L external PHYceiver**
- **Universal Serial Bus Controller with eight USB 2.0 ports**  
The VT8237S USB controller includes four USB 1.1 root hubs, one USB 2.0 root hub and eight USB 2.0 ports with integrated physical layer transceivers. Hot plug and isochronous peripherals are supported. Support of legacy keyboard and mouse is implemented so that legacy software could run transparently.
- **SPI Controller**  
The SPI Controller supports SPI flash memory control, Dynamic clock stop and is capable to write 256 bytes in one shot. External plug programmer is also supported when BIOS data needs to be updated.

- Full System Management Bus (SMBus) interface
- Keyboard controller with PS/2 mouse support
- Real Time Clock with 256 bytes extended CMOS

The integrated RTC includes the date alarm, century field and other enhancements for compatibility with the ACPI standard.

- Notebook-class, sophisticated Power Management Unit compliant with ACPI and legacy APM requirements

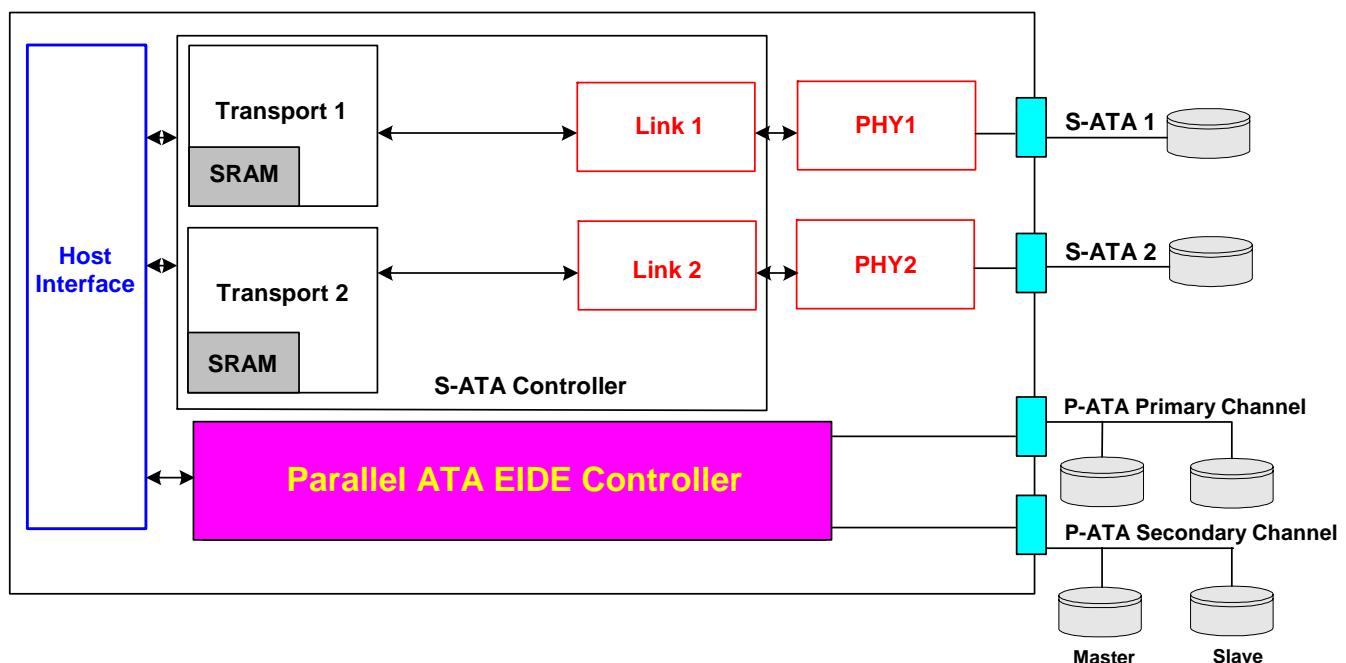
Multiple sleep states (POS, STR and STD) are supported with hardware automatic wake-up. Additional functionality includes event monitoring, CPU clock throttling and stop, PCI bus clock stop control, modular power, clock and leakage control, hardware-based and software-based event handling, general purpose I/O, chip select and external SMI.

- Plug and Play functions with steerable PCI interrupts

The PnP function allows complete steerability of PCI interrupts and integrated peripheral interrupts to system interrupt channel. One additional steerable interrupt channel is provided to allow plug and play and re-configurability of on-board peripherals for Windows family compliance.

The VT8237S also enhances the functionality of standard integrated peripherals. The integrated interrupt controller supports both edge and level triggered interrupts channel by channel. The integrated DMA controller supports type-F DMA. Special circuitry is built in to allow concurrent operation without causing deadlock in a PCI-to-PCI bridge environment.

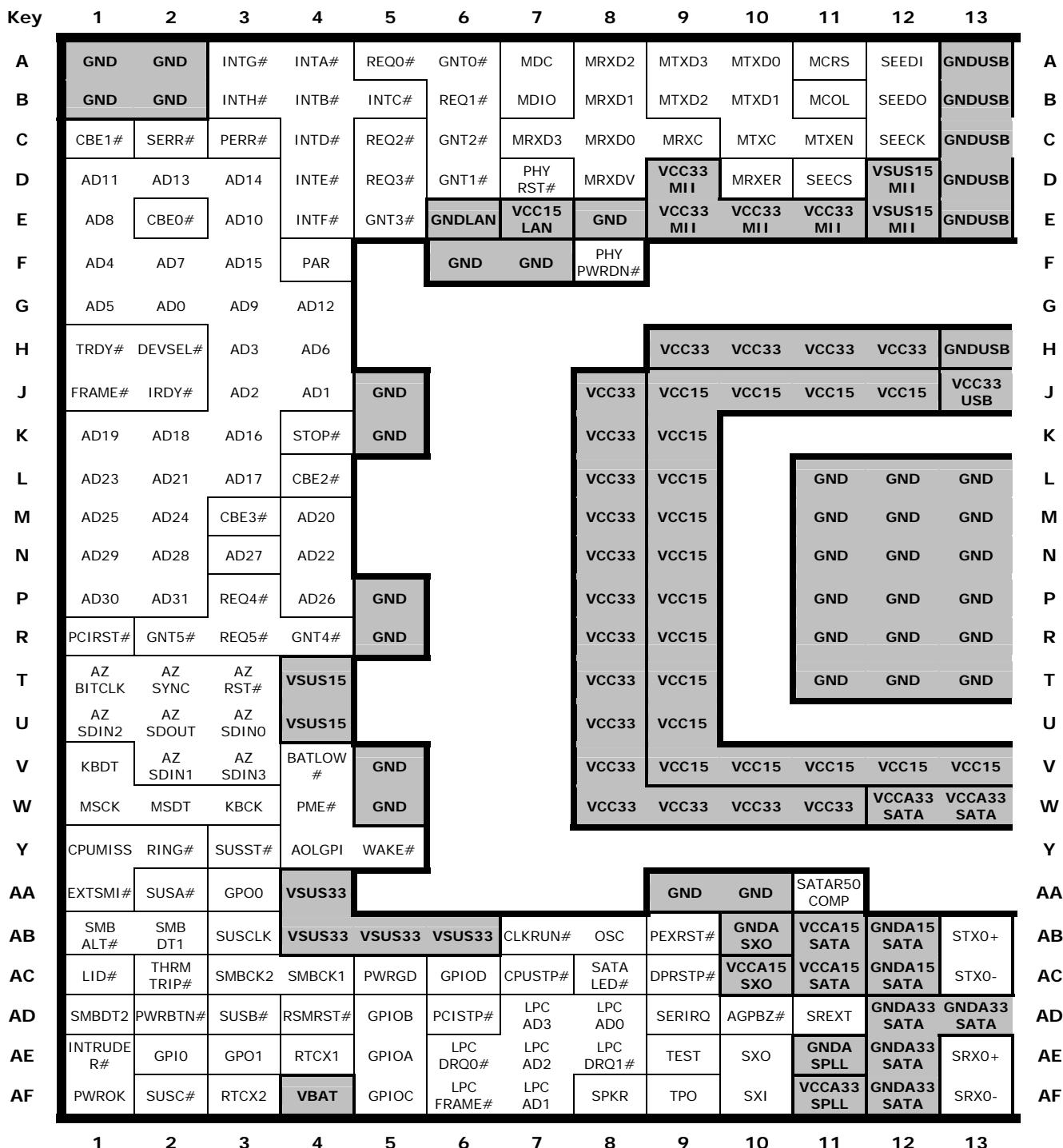
The high performance Serial ATA RAID Controller in the VT8237S supports RAID Level 0, RAID Level 1 and JBOD. The internal PCI interface of the Serial ATA controller complies with PCI Specification Revision 2.3. The chip also complies with revision 1.0 of the scatter / gather host DMA mechanism of “Programming Interface for Bus Master IDE Controller”. The VT8237S complies with Serial ATA Specification Revision 2.5 and includes two internal Serial ATA direct interfaces (i.e., a two-channel S-ATA PHY is provided on-chip) plus two Parallel ATA channels (primary and secondary).



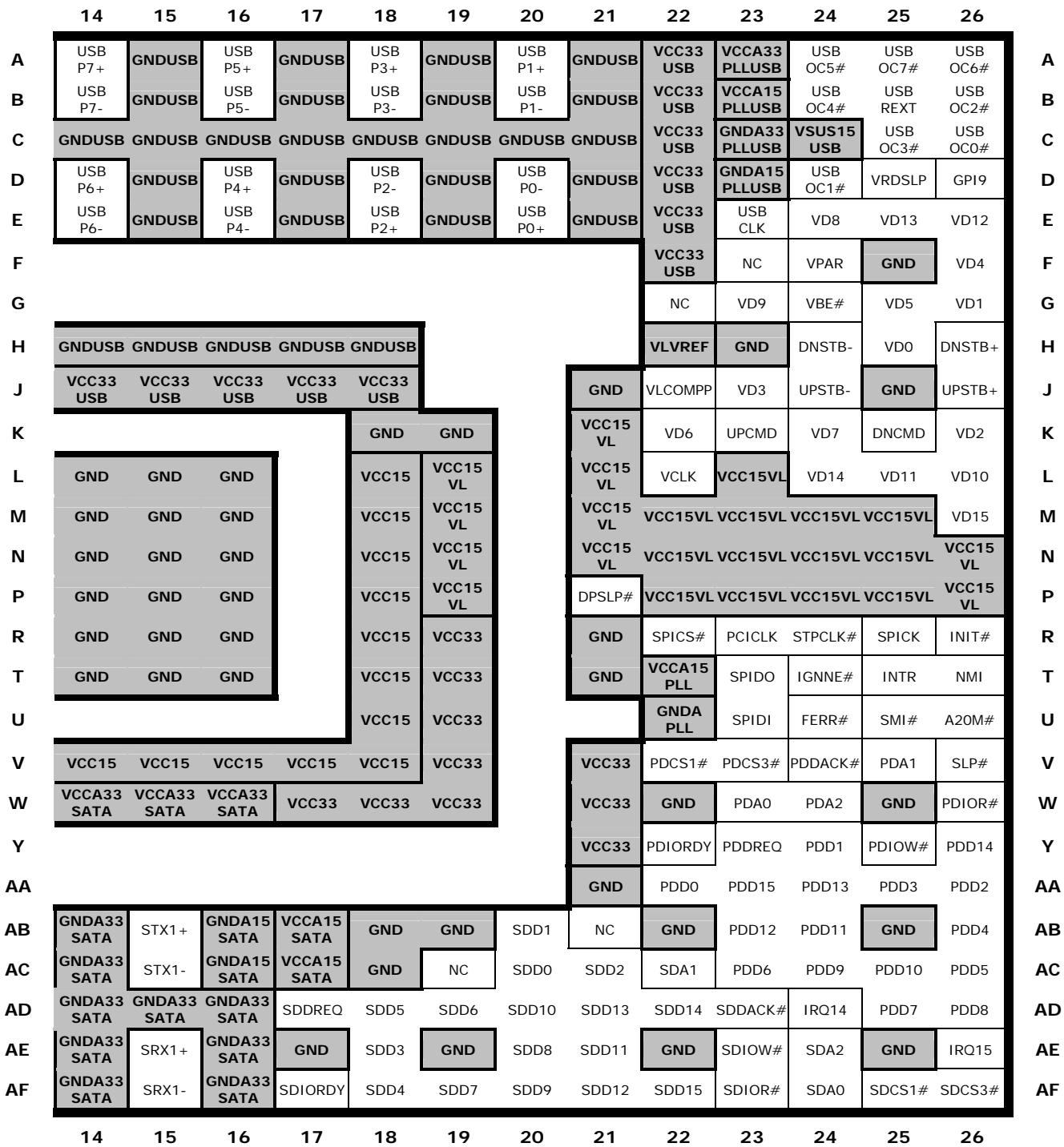
**Figure 2. VT8237S Block Diagram with 2 Serial ATA Devices**

# BALLOUTS

**Figure 3. VT8237S Ball Diagram (Left Side Top View)**



1      2      3      4      5      6      7      8      9      10     11     12     13

**Figure 4. VT8237S Ball Diagram (Right Side Top View)**


## Signal Ball List

**Table 1. Ball List (Listed by Ball Number)**

Ball#	Ball Name	Ball#	Ball Name						
A03	INTG#	D16	USBP4+	K26	VD2	W23	PDAO	AD06	PCISTP#
A04	INTA#	D18	USBP2-	L01	AD23	W24	PDA2	AD07	LPCAD3
A05	REQ0#	D20	USBPO-	L02	AD21	W26	PDIOR#	AD08	LPCAD0
A06	GNT0#	D24	USBOC1#	L03	AD17	Y01	CPUMISS	AD09	SERIRQ
A07	MDC	D25	VRDSLSP	L04	CBE2#	Y02	RING#	AD10	AGPBZ#
A08	MRXD2	D26	GPI9	L22	VCLK	Y03	SUSST#	AD11	SREXT
A09	MTXD3	E01	AD8	L24	VD14	Y04	AOLGPI	AD17	SDDREQ
A10	MTXD0	E02	CBE0#	L25	VD11	Y05	WAKE#	AD18	SDD5
A11	MCRS	E03	AD10	L26	VD10	Y22	PDIORDY	AD19	SDD6
A12	SEEDI	E04	INTF#	M01	AD25	Y23	PDDREQ	AD20	SDD10
A14	USBP7+	E05	GNT3#	M02	AD24	Y24	PDD1	AD21	SDD13
A16	USBP5+	E14	USBP6-	M03	CBE3#	Y25	PDIOW#	AD22	SDD14
A18	USBP3+	E16	USBP4-	M04	AD20	Y26	PDD14	AD23	SDDACK#
A20	USBP1+	E18	USBP2+	M26	VD15	AA01	EXTSMI#	AD24	IRO14
A24	USBOC5#	E20	USBP0+	N01	AD29	AA02	SUSA#	AD25	PDD7
A25	USBOC7#	E23	USBCLK	N02	AD28	AA03	GPO0	AD26	PDD8
A26	USBOC6#	E24	VD8	N03	AD27	AA11	SATAR50COMP		
B03	INTH#	E25	VD13	N04	AD22	AA22	PDD0	AE01	INTRUDER#
B04	INTB#	E26	VD12	P01	AD30	AA23	PDD15	AE02	GPIO
B05	INTC#	F01	AD4	P02	AD31	AA24	PDD13	AE03	GPO1
B06	REQ1#	F02	AD7	P03	REQ4#	AA25	PDD3	AE04	RTCX1
B07	MDIO	F03	AD15	P04	AD26	AA26	PDD2	AE05	GPIOA
B08	MRXD1	F04	PAR	P21	DPSLP#	AB01	SMBALT#	AE06	LPCDRQ0#
B09	MTXD2	F08	PHYPWRDN#	R01	PCIRST#	AB02	SMBDT1	AE07	LPCAD2
B10	MTXD1	F23	NC	R02	GNT5#	AB03	SUSCLK	AE08	LPCDRQ1#
B11	MCOL	F24	VPAR	R03	REQ5#	AB07	CLKRUN#	AE09	TEST
B12	SEEDO	F26	VD4	R04	GNT4#	AB08	OSC	AE10	SXO
B14	USBP7-	G01	AD5	R22	SPICS#	AB09	PEXRST#	AE13	SRX0+
B16	USBP5-	G02	AD0	R23	PCICLK	AB13	STX0+	AE15	SRX1+
B18	USBP3-	G03	AD9	R24	STPCLK#	AB15	STX1+	AE18	SDD3
B20	USBP1-	G04	AD12	R25	SPICK	AB20	SDD1	AE20	SDD8
B24	USBOC4#	G22	NC	R26	INIT#	AB21	NC	AE21	SDD11
B25	USBREXT	G23	VD9	T01	AZBITCLK	AB23	PDD12	AE23	SDIOW#
B26	USBOC2#	G24	VBE#	T02	AZSYNC	AB24	PDD11	AE24	SDA2
C01	CBE1#	G25	VD5	T03	AZRST#	AB26	PDD4	AE26	IRO15
C02	SERR#	G26	VD1	T23	SPIDO				
C03	PERR#	H01	TRDY#	T24	IGNNE#	AC01	LID#	AF01	PWROK
C04	INTD#	H02	DEVSEL#	T25	INTR	AC02	THRMTTRIP#	AF02	SUSC#
C05	REQ2#	H03	AD3	T26	NMI	AC03	SMBCK2	AF03	RTCX2
C06	GNT2#	H04	AD6	U01	AZSDIN2	AC04	SMBCK1	AF05	GPIOC
C07	MRXD3	H24	DNSTB-	U02	AZSDOUT	AC05	PWRGD	AF06	LPCFRAME#
C08	MRXD0	H25	VDO	U03	AZSDINO	AC06	GPIOD	AF07	LPCAD1
C09	MRXC	H26	DNSTB+	U23	SPIDI	AC07	CPUSTP#	AF08	SPKR
C10	MTXC	J01	FRAME#	U24	FERR#	AC08	SATALED#	AF09	TPO
C11	MTXEN	J02	IRDY#	U25	SMI#	AC09	DPRSTP#	AF10	SXI
C12	SEECK	J03	AD2	U26	A20M#	AC13	STX0-	AF13	SRX0-
C25	USBOC3#	J04	AD1	V01	KBDT	AC15	STX1-	AF15	SRX1-
C26	USBOC0#	J22	VLCOMPP	V02	AZSDIN1	AC19	NC	AF17	SDIORDY
D01	AD11	J23	VD3	V03	AZSDIN3	AC20	SDD0	AF18	SDD4
D02	AD13	J24	UPSTB-	V04	BATLOW#	AC21	SDD2	AF20	SDD9
D03	AD14	J26	UPSTB+	V22	PDCS1#	AC22	SDA1	AF21	SDD12
D04	INTE#	K01	AD19	V23	PDCS3#	AC23	PDD6	AF22	SDD15
D05	REQ3#	K02	AD18	V24	PDDACK#	AC24	PDD9	AF23	SDIOR#
D06	GNT1#	K03	AD16	V25	PDA1	AC25	PDD10	AF24	SDAO
D07	PHYRST#	K04	STOP#	V26	SLP#	AC26	PDD5	AF25	SDCS1#
D08	MRXDV	K22	VD6	W01	MSCK	AD01	SMBDT2	AF26	SDCS3#
D10	MRXER	K23	UPCMD	W02	MSDT	AD02	PWRBTN#		
D11	SEECS	K24	VD7	W03	KBCK	AD03	SUSB#		
D14	USBP6+	K25	DNCMD	W04	PME#	AD04	RSMRST#		
						AD05	GPIOB		

Note: For ground and power balls, please refer to Table 3.

**Table 2. Ball List (Listed by Ball Name)**

Ball#	Ball Name	Ball#	Ball Name	Ball#	Ball Name	Ball#	Ball Name	Ball#	Ball Name
U26	A20M#	J01	FRAME#	F23	NC	AF25	SDCS1#	AE09	TEST
G02	AD0	A06	GNT0#	G22	NC	AF26	SDCS3#	AC01	THRMTTRIP#
JO4	AD1	D06	GNT1#	AB21	NC	AC20	SDD0	AF09	TPO
JO3	AD2	C06	GNT2#	AC19	NC	AB20	SDD1	H01	TRDY#
H03	AD3	E05	GNT3#	T26	NMI	AC21	SDD2	K23	UPCMD
F01	AD4	R04	GNT4#	AB08	OSC	AE18	SDD3	J24	UPSTB-
G01	AD5	R02	GNT5#	F04	PAR	AF18	SDD4	J26	UPSTB+
H04	AD6	AE02	GPIO	R23	PCICLK	AD18	SDD5	E23	USCLK
F02	AD7	D26	GPIO	R01	PCIRST#	AD19	SDD6	C26	USBOC0#
E01	AD8	AE05	GPIOA	AD06	PCISTP#	AF19	SDD7	D24	USBOC1#
G03	AD9	AD05	GPIOB	W23	PDA0	AE20	SDD8	B26	USBOC2#
E03	AD10	AF05	GPIOC	V25	PDA1	AF20	SDD9	C25	USBOC3#
D01	AD11	AC06	GPIOD	W24	PDA2	AD20	SDD10	B24	USBOC4#
G04	AD12	AA03	GPO0	V22	PDCS1#	AE21	SDD11	A24	USBOC5#
D02	AD13	AE03	GPO1	V23	PDCS3#	AF21	SDD12	A26	USBOC6#
D03	AD14	T24	IGNNE#	AA22	PDD0	AD21	SDD13	A25	USBOC7#
F03	AD15	R26	INIT#	Y24	PDD1	AD22	SDD14	D20	USBPO-
K03	AD16	A04	INTA#	AA26	PDD2	AF22	SDD15	E20	USBPO+
L03	AD17	B04	INTB#	AA25	PDD3	AD23	SDDACK#	B20	USBP1-
K02	AD18	B05	INTC#	AB26	PDD4	AD17	SDDREQ	A20	USBP1+
K01	AD19	C04	INTD#	AC26	PDD5	AF23	SDIOR#	D18	USBP2-
M04	AD20	D04	INTE#	AC23	PDD6	AF17	SDIORDY	E18	USBP2+
L02	AD21	E04	INTF#	AD25	PDD7	AE23	SDIOW#	B18	USBP3-
N04	AD22	A03	INTG#	AD26	PDD8	C12	SEECK	A18	USBP3+
L01	AD23	B03	INTH#	AC24	PDD9	D11	SEECS	E16	USBP4-
M02	AD24	T25	INTR	AC25	PDD10	A12	SEEDI	D16	USBP4+
M01	AD25	AE01	INTRUDER#	AB24	PDD11	B12	SEEDO	B16	USBP5-
P04	AD26	J02	IRDY#	AB23	PDD12	AD09	SERIRQ	A16	USBP5+
N03	AD27	AD24	IRO14	AA24	PDD13	C02	SERR#	E14	USBP6-
N02	AD28	AE26	IRO15	Y26	PDD14	V26	SLP#	D14	USBP6+
N01	AD29	W03	KBCK	AA23	PDD15	AB01	SMBALT#	B14	USBP7-
P01	AD30	V01	KBDT	V24	PDDACK#	AC04	SMBCK1	A14	USBP7+
P02	AD31	AC01	LID#	Y23	PDDREQ	AC03	SMBCK2	B25	USBREXT
AD10	AGPBZ#	AD08	LPCADO	W26	PDIOR#	AB02	SMBDT1	G24	VBE#
Y04	AOLGPI	AF07	LPCAD1	Y22	PDIORDY	AD01	SMBDT2	L22	VCLK
T01	AZBITCLK	AE07	LPCAD2	Y25	PDIOW#	U25	SMI#	H25	VDO
T03	AZRST#	AD07	LPCAD3	C03	PERR#	R25	SPICK	G26	VD1
U03	AZSDINO	AE06	LPCDRQ0#	AB09	PEXRST#	R22	SPICS#	K26	VD2
V02	AZSDIN1	AE08	LPCDRQ1#	F08	PHYPWRDN#	U23	SPIDI	J23	VD3
U01	AZSDIN2	AF06	LPCFRAME#	D07	PHYRST#	T23	SPIDO	F26	VD4
V03	AZSDIN3	B11	MCOL	W04	PME#	AF08	SPKR	G25	VD5
U02	AZSDOUT	A11	MCRS	AD02	PWRBTN#	AD11	SREXT	K22	VD6
T02	AZSYNC	A07	MDC	AC05	PWRGD	AF13	SRX0-	K24	VD7
VO4	BATLOW#	B07	MDIO	AF01	PWROK	AE13	SRX0+	E24	VD8
E02	CBE0#	C09	MRXC	A05	REQ0#	AF15	SRX1-	G23	VD9
C01	CBE1#	C08	MRXD0	B06	REQ1#	AE15	SRX1+	L26	VD10
L04	CBE2#	B08	MRXD1	C05	REQ2#	K04	STOP#	L25	VD11
M03	CBE3#	A08	MRXD2	D05	REQ3#	R24	STPCLK#	E26	VD12
AB07	CLKRUN#	C07	MRXD3	P03	REQ4#	AC13	STX0-	E25	VD13
Y01	CPUMISS	D08	MRXdV	R03	REQ5#	AB13	STX0+	L24	VD14
AC07	CPUSTP#	D10	MRXER	Y02	RING#	AC15	STX1-	M26	VD15
H02	DEVSEL#	W01	MSCK	AD04	RSMRST#	AB15	STX1+	J22	VLCOMPP
K25	DNCMD	W02	MSDT	AE04	RTCX1	AA02	SUSA#	F24	VPAR
H24	DNSTB-	C10	MTXC	AF03	RTCX2	AD03	SUSB#	D25	VRDSL
H26	DNSTB+	A10	MTXD0	AC08	SATALED#	AF02	SUSC#	Y05	WAKE#
AC09	DPRSTP#	B10	MTXD1	AA11	SATAR50COMP	AB03	SUSCLK		
P21	DPSLP#	B09	MTXD2	AF24	SDAO	Y03	SUSST#		
AA01	EXTSMI#	A09	MTXD3	AC22	SDA1	AF10	SXI		
U24	FERR#	C11	MTXEN	AE24	SDA2	AE10	SXO		

Note: For ground and power balls, please refer to Table 3.

**Table 3. Power / Ground Ball List**

Ball#	Ball Name	Ball#	Ball Name	Ball#	Ball Name	Ball#	Ball Name	Ball#	Ball Name
A01	GND	T14	GND	B19	GNDUSB	V13	VCC15	W10	VCC33
A02	GND	T15	GND	B21	GNDUSB	V14	VCC15	W11	VCC33
B01	GND	T16	GND	C13	GNDUSB	V15	VCC15	W17	VCC33
B02	GND	T21	GND	C14	GNDUSB	V16	VCC15	W18	VCC33
E08	GND	V05	GND	C15	GNDUSB	V17	VCC15	W19	VCC33
F06	GND	W05	GND	C16	GNDUSB	V18	VCC15	W21	VCC33
F07	GND	W22	GND	C17	GNDUSB	E07 VCC15LAN		Y21	VCC33
F25	GND	W25	GND	C18	GNDUSB	K21	VCC15VL	D09	VCC33MII
H23	GND	AA09	GND	C19	GNDUSB	L19	VCC15VL	E09	VCC33MII
J05	GND	AA10	GND	C20	GNDUSB	L21	VCC15VL	E10	VCC33MII
J21	GND	AA21	GND	C21	GNDUSB	L23	VCC15VL	E11	VCC33MII
J25	GND	AB18	GND	D13	GNDUSB	M19	VCC15VL	A22	VCC33USB
K05	GND	AB19	GND	D15	GNDUSB	M21	VCC15VL	B22	VCC33USB
K18	GND	AB22	GND	D17	GNDUSB	M22	VCC15VL	C22	VCC33USB
K19	GND	AB25	GND	D19	GNDUSB	M23	VCC15VL	D22	VCC33USB
L11	GND	AC18	GND	D21	GNDUSB	M24	VCC15VL	E22	VCC33USB
L12	GND	AE17	GND	E13	GNDUSB	M25	VCC15VL	F22	VCC33USB
L13	GND	AE19	GND	E15	GNDUSB	N19	VCC15VL	J13	VCC33USB
L14	GND	AE22	GND	E17	GNDUSB	N21	VCC15VL	J14	VCC33USB
L15	GND	AE25	GND	E19	GNDUSB	N22	VCC15VL	J15	VCC33USB
L16	GND	D23	GNDA15PLLUSB	E21	GNDUSB	N23	VCC15VL	J16	VCC33USB
M11	GND	AB12	GNDA15SATA	H13	GNDUSB	N24	VCC15VL	J17	VCC33USB
M12	GND	AB16	GNDA15SATA	H14	GNDUSB	N25	VCC15VL	J18	VCC33USB
M13	GND	AC12	GNDA15SATA	H15	GNDUSB	N26	VCC15VL	T22	VCCA15PLL
M14	GND	AC16	GNDA15SATA	H16	GNDUSB	P19	VCC15VL	B23	VCCA15PLLUSB
M15	GND	C23	GNDA33PLLUSB	H17	GNDUSB	P22	VCC15VL	AB11	VCCA15SATA
M16	GND	AB14	GNDA33SATA	H18	GNDUSB	P23	VCC15VL	AB17	VCCA15SATA
N11	GND	AC14	GNDA33SATA	AF04	VBAT	P24	VCC15VL	AC11	VCCA15SATA
N12	GND	AD12	GNDA33SATA	J09	VCC15	P25	VCC15VL	AC17	VCCA15SATA
N13	GND	AD13	GNDA33SATA	J10	VCC15	P26	VCC15VL	AC10	VCCA15SXO
N14	GND	AD14	GNDA33SATA	J11	VCC15	H09 VCC33		A23	VCCA33PLLUSB
N15	GND	AD15	GNDA33SATA	J12	VCC15	H10	VCC33	W12	VCCA33SATA
N16	GND	AD16	GNDA33SATA	K09	VCC15	H11	VCC33	W13	VCCA33SATA
P05	GND	AE12	GNDA33SATA	L09	VCC15	H12	VCC33	W14	VCCA33SATA
P11	GND	AE14	GNDA33SATA	L18	VCC15	J08	VCC33	W15	VCCA33SATA
P12	GND	AE16	GNDA33SATA	M09	VCC15	K08	VCC33	W16	VCCA33SATA
P13	GND	AF12	GNDA33SATA	M18	VCC15	L08	VCC33	AF11	VCCA33SPLL
P14	GND	AF14	GNDA33SATA	N09	VCC15	M08	VCC33	H22	VLVREF
P15	GND	AF16	GNDA33SATA	N18	VCC15	N08	VCC33	T04	VSUS15
P16	GND	U22	GNDAPLL	P09	VCC15	P08	VCC33	U04	VSUS15
R05	GND	AE11	GNDASPLL	P18	VCC15	R08	VCC33	D12	VSUS15MII
R11	GND	AB10	GNDASXO	R09	VCC15	R19	VCC33	E12	VSUS15MII
R12	GND	E06	GNDLAN	R18	VCC15	T08	VCC33	C24	VSUS15USB
R13	GND	A13	GNDUSB	T09	VCC15	T19	VCC33	AA04	VSUS33
R14	GND	A15	GNDUSB	T18	VCC15	U08	VCC33	AB04	VSUS33
R15	GND	A17	GNDUSB	U09	VCC15	U19	VCC33	AB05	VSUS33
R16	GND	A19	GNDUSB	U18	VCC15	V08	VCC33	AB06	VSUS33
R21	GND	A21	GNDUSB	V09	VCC15	V19	VCC33		
T11	GND	B13	GNDUSB	V10	VCC15	V21	VCC33		
T12	GND	B15	GNDUSB	V11	VCC15	W08	VCC33		
T13	GND	B17	GNDUSB	V12	VCC15	W09	VCC33		

## Signal Descriptions

### Ultra V-Link Interface

Ultra V-Link Interface				
Signal Name	Ball #	I/O	Signal Description	Power Plane
<b>DNCMD</b>	K25	I	<b>Command from Host-to-Client.</b> Connect to ball VDNCMD on north bridge.	<b>VCC15VL</b>
<b>DNSTB+</b>	H26	I	<b>Strobe from Host-to-Client.</b> Connect to ball VDNSTB+ on north bridge.	<b>VCC15VL</b>
<b>DNSTB-</b>	H24	I	<b>Complement Strobe from Host-to-Client.</b> Connect to ball VDNSTB- on north bridge.	<b>VCC15VL</b>
<b>UPCMD</b>	K23	O	<b>Command from Client-to-Host.</b> Connect to ball VUPCMD on north bridge.	<b>VCC15VL</b>
<b>UPSTB+</b>	J26	O	<b>Strobe from Client-to-Host.</b> Connect to ball VUPSTB+ on north bridge.	<b>VCC15VL</b>
<b>UPSTB-</b>	J24	O	<b>Complement Strobe from Client-to-Host.</b> Connect to ball VUPSTB- on north bridge.	<b>VCC15VL</b>
<b>VBE#</b>	G24	IO	<b>Byte Enable.</b> Connect to same named pin on north bridge.	<b>VCC15VL</b>
<b>VCLK</b>	L22	I	<b>V-Link Clock.</b> 66 MHz. Supplied by clock generator.	<b>VCC33</b>
<b>VD[15:0]</b>	(see ball list)	IO	<b>Data Bus.</b> All bits 15-0 are implemented for use with VIA north bridge chips which support this capability (if not, only bits 7-0 are used). VD[7:0] are also used to send strap information to the chipset north bridge (see strap table below for details). The specific interpretation of these straps is north bridge chip design dependent.	<b>VCC15VL</b>
<b>VPAR</b>	F24	IO	<b>Parity.</b> If the VPAR function is implemented in a compatible manner on the north bridge, this pin should be connected to the north bridge VPAR. If VPAR is not implemented in the north bridge chip or is incompatible with the VT8237S (4x V-Link north bridges) connect this signal to an 8.2K pullup to 2.5V.	<b>VCC15VL</b>

**CPU Interface**

CPU Interface				
Signal Name	Ball #	I/O	Signal Description	Power Plane
A20M#	U26	OD	<b>A20 Mask.</b> Connect to A20 mask input of the CPU to control address bit-20 generation. Logical combination of the A20GATE input (from internal or external keyboard controller) and Port 92 bit-1 (Fast A20).	VCC33
FERR#	U24	I	<b>Numerical Coprocessor Error.</b> This signal is tied to the coprocessor error signal on the CPU. Internally generates interrupt 13 if active.	VCC33
IGNNE#	T24	OD	<b>Ignore Numeric Error.</b> This signal is connected to the CPU "ignore error" pin.	VCC33
INIT#	R26	OD	<b>Initialization.</b> The VT8237S asserts INIT# if it detects a shut-down special cycle on the PCI bus or if a soft reset is initiated by the register.	VCC33
INTR	T25	OD	<b>CPU Interrupt.</b> INTR is driven by the VT8237S to signal the CPU that an interrupt request is pending and needs service.	VCC33
NMI	T26	OD	<b>Non-Maskable Interrupt.</b> NMI is used to force a non-maskable interrupt to the CPU. The VT8237S generates an NMI when PCI bus SERR# is asserted.	VCC33
SLP#	V26	OD	<b>Sleep.</b> Used to put the CPU to sleep.	VCC33
SMI#	U25	OD	<b>System Management Interrupt.</b> SMI# is asserted by the VT8237S to the CPU in response to different Power-Management events.	VCC33
STPCLK#	R24	OD	<b>Stop Clock.</b> STPCLK# is asserted by the VT8237S to the CPU to throttle the processor clock.	VCC33

Note: Connect each of the above signals to 150 Ω pullup resistors to VCC\_CMOS (see Design Guide).

**CPU Speed Control Interface**

CPU Speed Control Interface				
Signal Name	Ball #	I/O	Signal Description	Power Plane
DPRSTP#	AC09	I	<b>Deeper Sleep.</b>	VCC33
VRDSLP / GPI29 / GPO9	D25	OD	<b>Voltage Regulator Deep Sleep.</b> Connected to the CPU voltage regulator. High selects the proper voltage for deep sleep mode.	VCC33
DPSLP# / GPI23 / GPO23 / LDTSTP#	P21	OD	<b>CPU Deep Sleep.</b> Used to put the CPU into a deeper sleep mode.	VCC33
AGPBZ# / GPI6	AD10	I	<b>AGP Busy.</b> Low indicates that an AGP master cycle is in progress (CPU speed transitions will be postponed if this input is asserted low). Connected to the AGP Bus AGPBZ# pin.	VCC33

### SPI Controller Interface

SPI Controller Interface				
Signal Name	Ball #	I/O	Signal Description	Power Plane
<b>SPIDO / GPIO11 / GPO11</b>	T23	O	<b>SPI Data Out.</b> Transfer data serially from SPI flash memory to SPI Controller.	<b>VCC33</b>
<b>SPIDI / GPI19 / GPO19</b>	U23	I	<b>SPI Data In.</b> Transfer data serially from SPI Controller to SPI flash memory.	<b>VCC33</b>
<b>SPICS#</b>	R22	O	<b>SPI Bus Chip Select.</b> Used to select SPI flash memory, active low.	<b>VCC33</b>
<b>SPICK / GPIO10 / GPO10</b>	R25	O	<b>SPI Clock.</b>	<b>VCC33</b>

### Serial ATA Interface

Serial ATA Interface				
Signal Name	Ball #	I/O	Signal Description	Power Plane
<b>SREXT</b>	AD11	AI	<b>SATA External Resistor.</b>	<b>VCCA33SATA</b>
<b>SRX0+-</b>	AE13, AF13	I	<b>SATA Port 0 Differential Receiver.</b>	<b>VCCA33SATA</b>
<b>SRX1+-</b>	AE15, AF15	I	<b>SATA Port 1 Differential Receiver.</b>	<b>VCCA33SATA</b>
<b>STX0+-</b>	AB13, AC13	O	<b>SATA Port 0 Differential Transmitter.</b>	<b>VCCA33SATA</b>
<b>STX1+-</b>	AB15, AC15	O	<b>SATA Port 1 Differential Transmitter.</b>	<b>VCCA33SATA</b>
<b>SXI</b>	AF10	I	<b>SATA Crystal In.</b>	<b>VCCA15SXO</b>
<b>SXO</b>	AE10	O	<b>SATA Crystal Out.</b>	<b>VCCA15SXO</b>
<b>SATALED#</b>	AC08	O	<b>SATA LED.</b>	<b>VCC33</b>

### PCI Bus Interface

PCI Bus Interface				
Signal Name	Ball #	I/O	Signal Description	Power Plane
<b>AD[31:0]</b>	(see ball list)	IO	<b>Address / Data Bus.</b> Multiplexed address and data. The address is driven with FRAME# assertion and data is driven or received in following cycles.	<b>VCC33</b>
<b>CBE[3:0]#</b>	M03, L04 C01, E02	IO	<b>Command / Byte Enable.</b> The command is driven with FRAME# assertion. Byte enables corresponding to supplied or requested data are driven on following clocks.	<b>VCC33</b>
<b>DEVSEL#</b>	H02	IO	<b>Device Select.</b> The VT8237S asserts this signal to claim PCI transactions through positive or subtractive decoding. As an input, DEVSEL# indicates the response to a VT8237S-initiated transaction and is also sampled when decoding whether to subtractively decode the cycle.	<b>VCC33</b>
<b>FRAME#</b>	J01	IO	<b>Frame.</b> Assertion indicates the address phase of a PCI transfer. Negation indicates that one more data transfer is desired by the cycle initiator.	<b>VCC33</b>
<b>GNT5# / GPO7</b> <b>GNT4#, R04</b> <b>GNT3#, E05</b> <b>GNT2#, C06</b> <b>GNT1#, D06</b> <b>GNT0#, A06</b>	R02 R04 E05 C06 D06 A06	O	<b>PCI Grant.</b> These signals are driven by the VT8237S to grant PCI access to a specific PCI master.	<b>VCC33</b>

PCI Bus Interface (continued)							
Signal Name	Ball #	I/O	Signal Description			Power Plane	
<b>INTA#</b>	A04	I	<b>PCI Interrupt Request.</b> The INTA# through INTD# pins are typically connected to the PCI bus INTA#-INTD# pins per the table below. INTE-H# are enabled by setting. BIOS settings must match the physical connection method.			<b>VCC33</b>	
<b>INTB#</b>	B04		<b>INTA#</b> <b>INTB#</b> <b>INTC#</b> <b>INTD#</b>				
<b>INTC#</b>	B05		PCI Slot 1    INTA#    INTB#    INTC#    INTD#				
<b>INTD#</b>	C04		PCI Slot 2    INTB#    INTC#    INTD#    INTE#				
<b>INTE#/GPI12, /GPO12,</b>	D04		PCI Slot 3    INTC#    INTD#    INTE#    INTF#				
<b>INTF#/GPI13, /GPO13,</b>	E04		PCI Slot 4    INTD#    INTE#    INTF#    INTG#				
<b>INTG#/GPI14, /GPO14,</b>	A03		PCI Slot 5    INTE#    INTF#    INTG#    INTH#				
<b>INTH#/GPI15, /GPO15</b>	B03		PCI Slot 6    INTF#    INTG#    INTH#    INTA#				
<b>IRDY#</b>	J02	IO	<b>Initiator Ready.</b> Asserted when the initiator is ready for data transfer.			<b>VCC33</b>	
<b>PAR</b>	F04	IO	<b>Parity.</b> A single parity bit is provided over AD[31:0] and C/BE[3:0]#.			<b>VCC33</b>	
<b>PCIRST#</b>	R01	O	<b>PCI Reset.</b> This signal is used to reset devices attached to the PCI bus.			<b>VSUS33</b>	
<b>PCICLK</b>	R23	I	<b>PCI Clock.</b> This signal provides timing for all transactions on the PCI Bus.			<b>VCC33</b>	
<b>PERR#</b>	C03	—	<b>Parity Error.</b> PERR#, sustained tri-state, is only for the reporting of data parity errors during all PCI transactions except for a Special Cycle.			<b>VCC33</b>	
<b>REQ5#/GPI7, REQ4#, REQ3#, REQ2#, REQ1#, REQ0#</b>	R03 P03 D05 C05 B06 A05	I	<b>PCI Request.</b> These signals connect to the VT8237S from each PCI slot (or each PCI master) to request the PCI bus.			<b>VCC33</b>	
<b>SERR#</b>	C02	I	<b>System Error.</b> SERR# can be pulsed active by any PCI device that detects a system error condition. Upon sampling SERR# active, the VT8237S can be programmed to generate an NMI to the CPU.			<b>VCC33</b>	
<b>STOP#</b>	K04	IO	<b>Stop.</b> Asserted by the target to request the master to stop the current transaction.			<b>VCC33</b>	
<b>TRDY#</b>	H01	IO	<b>Target Ready.</b> Asserted when the target is ready for data transfer.			<b>VCC33</b>	
<b>CLKRUN#</b>	AB07	IO	<b>PCI Bus Clock Run.</b> This signal indicates whether the PCI clock is or will be stopped (high) or running (low). The VT8237S drives this signal low when the PCI clock is running (default on reset) and releases it when it stops the PCI clock. External devices may assert this signal low to request that the PCI clock be restarted or prevent it from stopping.			<b>VCC33</b>	

MII Interface

LAN Controller - Media Independent Interface (MII)				
Signal Name	Ball #	I/O	Signal Description	Power Plane
<b>MCOL</b>	B11	I	<b>MII Collision Detect.</b> From the external PHY.	<b>VCC33MII</b>
<b>MCRS</b>	A11	I	<b>MII Carrier Sense.</b> Asserted by the external PHY when the media is active.	<b>VCC33MII</b>
<b>MDC</b>	A07	O	<b>MII Management Data Clock.</b> Sent to the external PHY as a timing reference for MDIO	<b>VCC33MII</b>
<b>MDIO</b>	B07	IO	<b>MII Management Data I/O.</b> Read from the MDI bit or written to the MDO bit.	<b>VCC33MII</b>
<b>MRXC</b>	C09	I	<b>MII Receive Clock.</b> 2.5 or 25 MHz clock recovered by the PHY.	<b>VCC33MII</b>
<b>MRXD[3:0]</b>	C07, A08, B08, C08	I	<b>MII Receive Data.</b> Parallel receive data lines driven by the external PHY synchronous with MRXC.	<b>VCC33MII</b>
<b>MRXDV</b>	D08	I	<b>MII Receive Data Valid.</b>	<b>VCC33MII</b>
<b>MRXER</b>	D10	I	<b>MII Receive Error.</b> Asserted by the PHY when it detects a data decoding error.	<b>VCC33MII</b>
<b>MTXC</b>	C10	I	<b>MII Transmit Clock.</b> Always active 2.5 or 25 MHz clock supplied by the PHY.	<b>VCC33MII</b>
<b>MTXD[3:0]</b>	A09, B09, B10, A10	O	<b>MII Transmit Data.</b> Parallel transmit data lines synchronized to MTXC.	<b>VCC33MII</b>
<b>MTXEN</b>	C11	O	<b>MII Transmit Enable.</b> Signals that transmit is active from the MII port to the PHY.	<b>VCC33MII</b>
<b>PHYPWRDN#</b>	F08	O	<b>PHY Power Down.</b> Output when PHY is in power state as D1 hot, D2 hot or D3 hot with no PME and WOL enable.	<b>VCC33MII</b>
<b>PHYRST#</b>	D07	O	<b>External PHY Reset.</b>	<b>VCC33MII</b>

Serial EEPROM Interface

Serial EEPROM Interface				
Signal Name	Ball #	I/O	Signal Description	Power Plane
<b>SEECK</b>	C12	O	<b>Serial EEPROM Clock.</b>	<b>VCC33</b>
<b>SEECS</b>	D11	O	<b>Serial EEPROM Chip Select.</b>	<b>VCC33</b>
<b>SEEDI</b>	A12	O	<b>Serial EEPROM Data Input.</b> Connect to EEPROM Data In pin.	<b>VCC33</b>
<b>SEEDO</b>	B12	I	<b>Serial EEPROM Data Output.</b> Connect to EEPROM Data Out pin.	<b>VCC33</b>

Note: The serial EEPROM Interface signals are disabled if the SEEDI signal is strapped high.

### USB 2.0 Interface

Universal Serial Bus 2.0 Interface				
Signal Name	Ball #	I/O	Signal Description	Power Plane
<b>USBCLK</b>	E23	I	<b>USB Clock.</b> 48 MHz clock input for the USB interface	VCC33USB
<b>USBOC0#</b>	C26	I	<b>USB Port 0 Over Current Detect.</b> Port 0 is disabled if low.	VCC33USB
<b>USBOC1#</b>	D24	I	<b>USB Port 1 Over Current Detect.</b> Port 1 is disabled if low.	VCC33USB
<b>USBOC2#</b>	B26	I	<b>USB Port 2 Over Current Detect.</b> Port 2 is disabled if low.	VCC33USB
<b>USBOC3#</b>	C25	I	<b>USB Port 3 Over Current Detect.</b> Port 3 is disabled if low.	VCC33USB
<b>USBOC4#</b>	B24	I	<b>USB Port 4 Over Current Detect.</b> Port 4 is disabled if low.	VCC33USB
<b>USBOC5#</b>	A24	I	<b>USB Port 5 Over Current Detect.</b> Port 5 is disabled if low.	VCC33USB
<b>USBOC6#</b>	A26	I	<b>USB Port 6 Over Current Detect.</b> Port 6 is disabled if low.	VCC33USB
<b>USBOC7#</b>	A25	I	<b>USB Port 7 Over Current Detect.</b> Port 7 is disabled if low.	VCC33USB
<b>USBP0+-</b>	E20, D20	IO	<b>USB Port 0 Differential Data.</b>	VCC33USB
<b>USBP1+-</b>	A20, B20	IO	<b>USB Port 1 Differential Data</b>	VCC33USB
<b>USBP2+-</b>	E18, D18	IO	<b>USB Port 2 Differential Data</b>	VCC33USB
<b>USBP3+-</b>	A18, B18	IO	<b>USB Port 3 Differential Data</b>	VCC33USB
<b>USBP4+-</b>	D16, E16	IO	<b>USB Port 4 Differential Data</b>	VCC33USB
<b>USBP5+-</b>	A16, B16	IO	<b>USB Port 5 Differential Data</b>	VCC33USB
<b>USBP6+-</b>	D14, E14	IO	<b>USB Port 6 Differential Data</b>	VCC33USB
<b>USBP7+-</b>	A14, B14	IO	<b>USB Port 7 Differential Data</b>	VCC33USB
<b>USBREXT</b>	B25	AI	<b>USB External Resistor.</b>	VCC33USB

### SMBus Interface

System Management Bus (SMB) Interface ( $I^2C$ Bus)				
Signal Name	Ball #	I/O	Signal Description	Power Plane
<b>SMBALT#</b>	AB01	I	<b>SMB Alert.</b> Enabled by System Management Bus I/O space. When the chip is enabled to allow it, assertion generates an IRQ or SMI interrupt or a power management resume event.	VSUS33
<b>SMBCK1</b>	AC04	OD	<b>SMB / <math>I^2C</math> Channel 1 Clock.</b> Mater Mode.	VSUS33
<b>SMBCK2 / GPIO27 / GPO27</b>	AC03	OD	<b>SMB / <math>I^2C</math> Channel 2 Clock.</b> Slave Mode.	VSUS33
<b>SMBDT1</b>	AB02	OD	<b>SMB / <math>I^2C</math> Channel 1 Data.</b> Mater Mode.	VSUS33
<b>SMBDT2 / GPIO26 / GPO26</b>	AD01	OD	<b>SMB / <math>I^2C</math> Channel 2 Data.</b> Slave Mode.	VSUS33

### Low Pin Count Interface

Low Pin Count (LPC) Interface				
Signal Name	Ball #	I/O	Signal Description	Power Plane
<b>LPCAD[3:0]</b>	AD07, AE07, AF07, AD08	IO	<b>LPC Address / Data.</b>	VCC33
<b>LPCDRQ[1:0]#</b>	AE08, AE06	I	<b>LPC DMA / Bus Master Request 0 and 1.</b>	VCC33
<b>LPCFRAME#</b>	AF06	O	<b>LPC Frame.</b>	VCC33

Note: Connect the LPC interface LPCRST# (LPC Reset) signal to PCIRST#

**Enhanced IDE Interface**

UltraDMA-133 / 100 / 66 / 33 Enhanced IDE Interface				
Signal Name	Ball #	I/O	Signal Description	Power Plane
<b>IRQ14</b>	AD24	I	<b>Primary Channel Interrupt Request.</b>	VCC33
<b>IRQ15</b>	AE26	I	<b>Secondary Channel Interrupt Request.</b>	VCC33
<b>PDA[2:0]</b>	W24, V25, W23	O	<b>Primary Disk Address.</b> PDA[2:0] are used to indicate which byte in either the ATA command block or control block is being accessed. Strap information is communicated to the north bridge via VD[6:4].	VCC33
<b>PDCS1#</b>	V22	O	<b>Primary Master Chip Select.</b> This signal corresponds to CS1FX# on the primary IDE connector.	VCC33
<b>PDCS3#</b>	V23	O	<b>Primary Slave Chip Select.</b> This signal corresponds to CS3FX# on the primary IDE connector.	VCC33
<b>PDD[15:0]</b>	(see ball list)	IO	<b>Primary Disk Data.</b>	VCC33
<b>PDDACK#</b>	V24	O	<b>Primary Device DMA Acknowledge.</b> <u>Primary</u> channel DMA acknowledge	VCC33
<b>PDDREQ</b>	Y23	I	<b>Primary Device DMA Request.</b> <u>Primary</u> channel DMA request	VCC33
<b>PDIOR#/</b> <b>PHDMARDY /</b> <b>PHSTROBE</b>	W26	O	EIDE Mode: <b>Primary Device I/O Read.</b> Device read strobe UltraDMA Mode: <b>Primary Host DMA Ready.</b> <u>Primary</u> channel input flow control. The host may assert PHDMARDY to pause input transfers <b>Primary Host Strobe.</b> Output data strobe (both edges). The host may stop PHSTROBE to pause output data transfers	VCC33
<b>PDIORDY /</b> <b>PDDMARDY /</b> <b>PDSTROBE</b>	Y22	I	EIDE Mode: <b>Primary I/O Channel Ready.</b> Device ready indicator UltraDMA Mode: <b>Primary Device DMA Ready.</b> Output flow control. The device may assert PDDMARDY to pause output transfers <b>Primary Device Strobe.</b> Input data strobe (both edges). The device may stop PDSTROBE to pause input data transfers	VCC33
<b>PDIOW#/</b> <b>PSTOP</b>	Y25	O	EIDE Mode: <b>Primary Device I/O Write.</b> Device write strobe UltraDMA Mode: <b>Primary Stop.</b> Stop transfer: Asserted by the host prior to initiation of an UltraDMA burst; negated by the host before data is transferred in an UltraDMA burst. Assertion of STOP by the host during or after data transfer in UltraDMA mode signals the termination of the burst.	VCC33
<b>SDA[2:0]</b>	AE24, AC22, AF24	O	<b>Secondary Disk Address.</b> SDA[2:0] are used to indicate which byte in either the ATA command block or control block is being accessed.	VCC33
<b>SDCS1#</b>	AF25	O	<b>Secondary Master Chip Select.</b> This signal corresponds to CS17X# on the secondary IDE connector.	VCC33
<b>SDCS3#</b>	AF26	O	<b>Secondary Slave Chip Select.</b> This signal corresponds to CS37X# on the secondary IDE connector.	VCC33
<b>SDD[15:0]</b>	(see ball list)	IO	<b>Secondary Disk Data.</b>	VCC33
<b>SDDACK#</b>	AD23	O	<b>Secondary Device DMA Acknowledge.</b> <u>Secondary</u> channel DMA acknowledge	VCC33
<b>SDDREQ</b>	AD17	I	<b>Secondary Device DMA Request.</b> <u>Secondary</u> channel DMA request	VCC33

UltraDMA-133 / 100 / 66 / 33 Enhanced IDE Interface (continued)						
Signal Name	Ball #	I/O	Signal Description		Power Plane	
<b>SDIOR# / SHDMARDY / SHSTROBE</b>	AF23	O	EIDE Mode: <b>Secondary Device I/O Read.</b> Device read strobe UltraDMA Mode: <b>Secondary Host DMA Ready.</b> Input flow control. The host may assert SHDMARDY to pause input transfers <b>Second Host Strobe.</b> Output strobe (both edges). The host may stop SHSTROBE to pause output data transfers			<b>VCC33</b>
<b>SDIORDY / SDDMARDY / SDSTROBE</b>	AF17	I	EIDE Mode: <b>Secondary I/O Channel Ready.</b> Device ready indicator UltraDMA Mode: <b>Secondary Device DMA Ready.</b> Output flow control. The device may assert SDDMARDY to pause output transfers <b>Secondary Device Strobe.</b> Input data strobe (both edges). The device may stop SDSTROBE to pause input data transfers			<b>VCC33</b>
<b>SDIOW# / SSTOP</b>	AE23	O	EIDE Mode: <b>Secondary Device I/O Write.</b> Device write strobe UltraDMA Mode: <b>Secondary Stop.</b> Stop transfer: Asserted by the host prior to initiation of an UltraDMA burst; negated by the host before data is transferred in an UltraDMA burst. Assertion of STOP by the host during or after data transfer in UltraDMA mode signals the termination of the burst.			<b>VCC33</b>

High Definition Audio Interface

High Definition Audio				
Signal Name	Ball #	I/O	Signal Description	Power Plane
AZBITCLK	T01	O	<b>High Definition Audio Bit Clock.</b> 24.00 MHz.	VCC33
AZRST#	T03	O	<b>High Definition Audio Reset.</b>	VSUS33
AZSDIN0	U03	I	<b>High Definition Audio Serial Data Input 0.</b> Point-to-point serial data input signal 0.	VSUS33
AZSDIN1	V02	I	<b>High Definition Audio Serial Data Input 1.</b> Point-to-point serial data input signal 1.	VSUS33
AZSDIN2 / PCS0# / GPIO20	U01	I	<b>High Definition Audio Serial Data Input 2.</b> Point-to-point serial data input signal 2.  AZSDIN2 is multiplexed with PCS0#. AZSDIN2 can optionally be used as GPIO20.	VSUS33
AZSDIN3 / PCS1# / GPIO21	V03	I	<b>High Definition Audio Serial Data Input 3</b> Point-to-point serial data input signal 3.  AZSDIN3 is multiplexed with this pin PCS1#. AZSDIN3 can optionally be used as GPIO21.	VSUS33
AZSDOUT	U02	O	<b>High Definition Audio Serial Data Output.</b> Bussed serial data output signal 0.	VCC33
AZSYNC	T02	O	<b>High Definition Audio Sync.</b> 48 KHz Frame Sync and outbound tag signal.	VCC33

Serial IRQ Interface

Serial IRQ				
Signal Name	Ball #	I/O	Signal Description	Power Plane
SERIRQ	AD09	IO	<b>Serial IRQ.</b> This signal has an internal pull-up resistor.	VCC33

PC / PCI DMA Interface

PC / PCI DMA				
Signal Name	Ball #	I/O	Signal Description	Power Plane
PCREQA / GPIO24 / GPO24 (GPIOA)	AE05	I	<b>PC / PCI Request A.</b>	VCC33
PCREQB / GPIO25 / GPO25 (GPIOB)	AD05	I	<b>PC / PCI Request B.</b>	VCC33
PCGNTA / GPIO30 / GPO30 (GPIOC)	AF05	O	<b>PC / PCI Grant A.</b>	VCC33
PCGNTB / GPIO31 / GPO31 (GPIOD)	AC06	O	<b>PC / PCI Grant B.</b>	VCC33

### Internal Keyboard Controller Interface

Internal Keyboard Controller				
Signal Name	Ball #	I/O	Signal Description	Power Plane
<b>MSCK / IRQ1</b>	W01	IO	<b>MultiFunction Pin</b> Internal mouse controller enabled by B0D17F0 Rx51[1]. B0D17F0 Rx51[2]=1 <b>Mouse Clock.</b> From internal mouse controller. B0D17F0 Rx51[2]=0 <b>Interrupt Request 1.</b> Interrupt input 1.	<b>VSUS33</b>
<b>MSDT / IRQ12</b>	W02	IO	<b>MultiFunction Pin</b> Internal mouse controller enabled by B0D17F0 Rx51[1]. B0D17F0 Rx51[2]=1 <b>Mouse Data.</b> From internal mouse controller. B0D17F0 Rx51[2]=0 <b>Interrupt Request 12.</b> Interrupt input 12.	<b>VSUS33</b>
<b>KBCK / KA20G</b>	W03	IO	<b>MultiFunction Pin</b> Internal keyboard controller enabled by B0D17F0 Rx51[0]. B0D17F0 Rx51[0]=1 <b>Keyboard Clock.</b> From internal keyboard controller B0D17F0 Rx51[0]=0 <b>Gate A20.</b> Input from external keyboard controller.	<b>VSUS33</b>
<b>KBDT / KBRC#</b>	V01	IO	<b>MultiFunction Pin</b> Internal keyboard controller enabled by B0D17F0 Rx51[0]. B0D17F0 Rx51[0]=1 <b>Keyboard Data.</b> From internal keyboard controller. B0D17F0 Rx51[0]=0 <b>KBDT / KBRC#.</b> From external keyboard controller (KBC) for CPURST# generation	<b>VSUS33</b>

### Speaker Interface

Speaker Interface				
Signal Name	Ball #	I/O	Signal Description	Power Plane
<b>SPKR</b>	AF08	O	<b>Speaker.</b> Strap low to enable (high to disable) CPU frequency strapping.	<b>VCC33</b>

### Programming Chip Selects Signals

Programming Chip Selects Signals				
Signal Name	Ball #	I/O	Signal Description	Power Plane
<b>PCS0# / AZSDIN2 / GPIO20</b>	U01	O	<b>Programmable Chip Select 0.</b> AZSDIN2 is multiplexed with this pin. PCS0# can optionally be used as GPIO20.	<b>VSUS33</b>
<b>PCS1# / AZSDIN3 / GPIO21</b>	V03	O	<b>Programmable Chip Select 1.</b> AZSDIN3 is multiplexed with this pin. PCS1# can optionally be used as GPIO21.	<b>VSUS33</b>

**General Purpose Input Interface**

General Purpose Input				
Signal Name	Ball #	I/O	Signal Description	Power Plane
<b>GPI0</b>	AE02	I	<b>General Purpose Input 0.</b>	<b>VBAT</b>
<b>GPI1 / THRMTRIP#</b>	AC02	I	<b>General Purpose Input 1.</b>	<b>VSUS33</b>
<b>GPI2 / EXTSMI#</b>	AA01	I	<b>General Purpose Input 2.</b>	<b>VSUS33</b>
<b>GPI3 / RING#</b>	Y02	I	<b>General Purpose Input 3.</b>	<b>VSUS33</b>
<b>GPI4 / LID#</b>	AC01	I	<b>General Purpose Input 4.</b>	<b>VSUS33</b>
<b>GPI5 / BATLOW#</b>	V04	I	<b>General Purpose Input 5.</b>	<b>VSUS33</b>
<b>GPI6 / AGPBZ#</b>	AD10	I	<b>General Purpose Input 6.</b>	<b>VCC33</b>
<b>GPI7 / REQ5#</b>	R03	I	<b>General Purpose Input 7.</b>	<b>VCC33</b>
<b>GPI9 / UDPWR</b>	D26	I	<b>General Purpose Input 9.</b>	<b>VCC33USB</b>
<b>GPI16 / INTRUDER#</b>	AE01	I	<b>General Purpose Input 16.</b>	<b>VBAT</b>
<b>GPI17 / CPUMISS</b>	Y01	I	<b>General Purpose Input 17.</b>	<b>VSUS33</b>
<b>GPI18 / THRM# / AOLGPI</b>	Y04	I	<b>General Purpose Input 18.</b>	<b>VSUS33</b>
<b>GPI29 / VRDSLP</b>	D25	I	<b>General Purpose Input 29.</b>	<b>VCC33</b>

**General Purpose Output Interface**

General Purpose Output				
Signal Name	Ball #	I/O	Signal Description	Power Plane
<b>GPO0</b>	AA03	O	<b>General Purpose Output 0.</b>	<b>VSUS33</b>
<b>GPO1</b>	AE03	O	<b>General Purpose Output 1.</b>	<b>VSUS33</b>
<b>GPO2 / SUSA#</b>	AA02	O	<b>General Purpose Output 2.</b>	<b>VSUS33</b>
<b>GPO3 / SUSST#</b>	Y03	O	<b>General Purpose Output 3.</b>	<b>VSUS33</b>
<b>GPO4 / SUSCLK</b>	AB03	O	<b>General Purpose Output 4.</b>	<b>VSUS33</b>
<b>GPO5 / CPUSTP#</b>	AC07	O	<b>General Purpose Output 5.</b>	<b>VCC33</b>
<b>GPO6 / PCISTP#</b>	AD06	O	<b>General Purpose Output 6.</b>	<b>VCC33</b>
<b>GPO7 / GNT5#</b>	R02	O	<b>General Purpose Output 7.</b>	<b>VCC33</b>
<b>GPO9 / VRDSLP</b>	D25	O	<b>General Purpose Output 9.</b>	<b>VCC33USB</b>
<b>GPO22 / SPICS#</b>	R22	O	<b>General Purpose Output 22.</b>	<b>VCC33</b>
<b>GPO29 / PEXRST#</b>	AB09	O	<b>General Purpose Output 29.</b>	<b>VCC33</b>

General Purpose Input / Output Interface

General Purpose Input / Output				
Signal Name	Ball #	I/O	Signal Description	Power Plane
GPIO10 / SPICK	R25	IO	General Purpose I/O 10.	VCC33
GPIO11 / SPIDO	T23	IO	General Purpose I/O 11.	VCC33
GPIO12 / INTE#	D04	IO	General Purpose I/O 12.	VCC33
GPIO13 / INTF#	E04	IO	General Purpose I/O 13.	VCC33
GPIO14 / INTG#	A03	IO	General Purpose I/O 14.	VCC33
GPIO15 / INTH#	B03	IO	General Purpose I/O 15.	VCC33
GPIO19 / SPIDI	U23	IO	General Purpose I/O 19.	VCC33
GPIO20 / AZSDIN2 / PCS0#	U01	IO	General Purpose I/O 20.	VSUS33
GPIO21 / AZSDIN3 / PCS1#	V03	IO	General Purpose I/O 21.	VSUS33
GPIO23 / DPSLP# / LDTSTP#	P21	IO	General Purpose I/O 23.	VCC33
GPIO24 / GPIOA / PCREQA	AE05	IO	General Purpose I/O A / 24.	VCC33
GPIO25 / GPIOB / PCREQB	AD05	IO	General Purpose I/O B / 25.	VCC33
GPIO26 / SMBDT2	AD01	IO	General Purpose I/O 26.	VSUS33
GPIO27 / SMBCK2	AC03	IO	General Purpose I/O 27.	VSUS33
GPIO28 / DPRSTP#	AC09	IO	General Purpose I/O 28.	VCC33
GPIO30 / GPIOC / PCGNTA	AF05	IO	General Purpose I/O C / 30.	VCC33
GPIO31 / GPIOD / PCGNTB	AC06	IO	General Purpose I/O D / 31.	VCC33

Power Management and Event Signals

Power Management and Event Detection				
Signal Name	Ball #	I/O	Signal Description	Power Plane
BATLOW# / GPI5	V04	I	<b>Battery Low Indicator.</b> BATLOW# can optionally be used as GPI5.	VSUS33
CPUMISS / GPI17	Y01	I	<b>CPU Missing.</b> Used to detect the physical presence of the CPU chip in its socket. High indicates no CPU present. Connect to the CPUMISS pin of the CPU socket. The state of this pin may be read in the SMBus 2 registers. This signal may be used as CPUMISS and GPI17 at the same time.	VSUS33
CPUSTP# / GPO5	AC07	O	<b>CPU Clock Stop.</b> Signals the system clock generator to disable the CPU clock outputs. Not connected if not used.	VCC33
EXTSMI# / GPI2	AA01	IO	<b>External System Management Interrupt.</b> When enabled to allow it, a falling edge on this input causes an SMI# to be generated to the CPU to enter SMI mode. EXTSMI# can optionally be used as GPI2	VSUS33
INTRUDER# / GPI16	AE01	I	<b>Intrusion Indicator.</b> INTRUDER# can optionally be used as GPI16.	VBAT
LID# / GPI4	AC01	I	<b>Notebook Computer Display Lid Open / Closed Monitor.</b> Used by the Power Management subsystem to monitor the opening and closing of the display lid of notebook computers. Can be used to detect either low-to-high or high-to-low transitions to generate an SMI#. LID# can optionally be used as GPI4.	VSUS33
PCISTP# / GPO6	AD06	O	<b>PCI Clock Stop.</b> Signals the system clock generator to disable the PCI clock outputs. Not connected if not used.	VCC33
PEXRST# / GPO29	AB09	O	<b>PCIe Bus Reset Signal.</b>	VSUS33
PME#	W04	I	<b>Power Management Event.</b>	VSUS33
PWRBTN#	AD02	I	<b>Power Button.</b> Used by the Power Management subsystem to monitor an external system on/off button or switch. Internal logic powered by VSUS33.	VSUS33
RING# / GPI3	Y02	I	<b>Ring Indicator.</b> May be connected to external modem circuitry to allow the system to be re-activated by a received phone call. RING# can optionally be used as GPI3.	VSUS33
SMBALT#	AB01	I	<b>SMB Alert.</b> When programmed to allow it, assertion generates an IRQ, SMI, or power management event.	VSUS33
SUSA# / GPO2	AA02	O	<b>Suspend Plane A Control.</b> Asserted during power management POS, STR, and STD suspend states. Used to control the primary power plane.	VSUS33
SUSB#	AD03	O	<b>Suspend Plane B Control.</b> Asserted during power management STR and STD suspend states. Used to control the secondary power plane.	VSUS33
SUSC#	AF02	O	<b>Suspend Plane C Control.</b> Asserted during power management STD suspend state. Used to control the tertiary power plane. Also connected to ATX power-on circuitry.	VSUS33
SUSCLK / GPO4	AB03	O	<b>Suspend Clock.</b> It is an output clock of the RTC generator circuit to use by other chips for refresh clock.	VSUS33
SUSST# / GPO3	Y03	O	<b>Suspend Status 1.</b> Typically connected to the North Bridge to provide information on host clock status. Asserted when the system may stop the host clock, such as Stop Clock or during POS, STR, or STD suspend states.	VSUS33

Power Management and Event Detection (continued)				
Signal Name	Ball #	I/O	Signal Description	Power Plane
AOLGPI / GPI18 / THRM#	Y04	I	<b>Alert On LAN.</b> The state of this pin may be read in the SMBus 2 registers. This signal may be used as AOLGPI, GPI18 and THRM# all at the same time.	<b>VSUS33</b>
RSMRST#	AD04	I	<b>Resume Reset.</b> Resets the internal logic connected to the VSUS33 power plane and also resets portions of the internal RTC logic. Internal logic powered by VBAT.	<b>VBAT</b>
THRM# / GPI18 / AOLGPI	Y04	I	<b>Thermal Alarm Monitor.</b> This signal is to enable the throttling mode for the duty cycle control of stop clock. AOLGPI is multiplexed with this pin. THRM# can optionally be used as GPI18.	<b>VSUS33</b>
WAKE#	Y05	I	<b>For a Wake-up Event.</b> Connect to PCI Express PEWAKE# signal.	<b>VSUS33</b>
THRMTrip# / GPI1	AC02	I	<b>Thermal Detect Power Down.</b> This signal is to indicate a thermal trip from the processor.	<b>VSUS33</b>

#### Resets, Clocks and Power Status Interfaces

Resets, Clocks and Power Status				
Signal Name	Ball #	I/O	Signal Description	Power Plane
PWRGD	AC05	I	<b>Power Good.</b> Connected to the Power Good signal on the Power Supply.	<b>VBAT</b>
PWROK	AF01	O	<b>Power OK.</b> Internal logic powered by VSUS33.	<b>VSUS33</b>
PCIRST#	R01	O	<b>PCI Reset.</b> Active low reset signal for the PCI bus. The VT8237S will assert this pin during power-up or from the control register.	<b>VSUS33</b>
OSC	AB08	I	<b>Oscillator.</b> 14.31818 MHz clock signal used by the internal Timer.	<b>VCC33</b>
RTCX1	AE04	I	<b>RTC Crystal Input:</b> 32.768 KHz crystal or oscillator input.	<b>VBAT</b>
RTCX2	AF03	O	<b>RTC Crystal Output:</b> 32.768 KHz crystal output.	<b>VBAT</b>
TEST	AE09	I	Test.	<b>VCC33</b>
TPO	AF09	O	<b>Test Pin Output.</b> Output pin for test mode.	<b>VCC33</b>

#### Compensation and Reference Voltage Signal Descriptions

Compensation and Reference Voltage				
Signal Name	Ball #	I/O	Signal Description	Power Plane
VLCOMP	J22	AI	<b>V-Link Compensation.</b>	<b>VCC15VL</b>
VLVREF	H22	P	<b>V-Link Voltage Reference.</b>	<b>VCC15VL</b>

**Power / Ground Signals**

<b>Analog Power and Ground</b>			
<b>Signal Name</b>	<b>Ball #</b>	<b>I/O</b>	<b>Signal Description</b>
<b>SATA Controller</b>			
<b>GNDA15SATA</b>	(see ball list)	P	<b>SATA Analog Ground.</b>
<b>GNDA33SATA</b>	(see ball list)	P	<b>SATA Analog Ground.</b>
<b>GNDASXO</b>	AB10	P	<b>SATA Oscillator Ground.</b>
<b>VCCA15SATA</b>	AB11, AB17, AC11, AC17	P	<b>SATA Analog Power.</b> 1.5V ±5%.
<b>VCCA15SXO</b>	AC10	P	<b>SATA Oscillator Power.</b> 1.5V ±5%.
<b>VCCA33SATA</b>	(see ball list)	P	<b>SATA Analog Power.</b> 3.3V ±5%.
<b>PLL Analog</b>			
<b>GNDAPLL</b>	U22	P	<b>PLL Analog Ground.</b> Connect to GND through a ferrite bead.
<b>GNDASPLL</b>	AE11	P	<b>Serial ATA PLL Analog Ground.</b>
<b>VCCA15PLL</b>	T22	P	<b>PLL Analog Power.</b> 1.5V ±5%. Connect to VCC through a ferrite bead.
<b>VCCA33SPLL</b>	AF11	P	<b>Serial ATA PLL Analog Power.</b> 3.3V ±5%.
<b>USB Controller</b>			
<b>GNDA15PLLUSB</b>	D23	P	<b>USB PLL Analog Ground.</b> Connect to GND through a ferrite bead.
<b>GNDA33PLLUSB</b>	C23	P	<b>USB PLL Analog Ground.</b> Connect to GND through a ferrite bead.
<b>VCCA15PLLUSB</b>	B23	P	<b>USB PLL Analog Voltage.</b> Connect to VCC through a ferrite bead. 1.5V ±5%.
<b>VCCA33PLLUSB</b>	A23	P	<b>USB PLL Analog Voltage.</b> Connect to VCC through a ferrite bead. 3.3V ±5%.
<b>VCC33USB</b>	(see ball list)	P	<b>USB 2.0 Differential Output Power.</b> 3.3V ±5%. Power for USB differential outputs (USBP0+, P0-, P1+, P1-, P2+, P2-, P3+, P3-, P4+, P4-, P5+, P5-, P6+, P6-, P7+, P7-). Connect to VSUS33 through a ferrite bead if suspend wake-up is required.
<b>GNDUSB</b>	(see ball list)	P	<b>USB Ground.</b>

<b>Digital Power and Ground</b>			
<b>Signal Name</b>	<b>Ball #</b>	<b>I/O</b>	<b>Signal Description</b>
<b>GND</b>	(see ball list)	P	<b>Ground.</b> Connect to primary motherboard ground plane.
<b>GNDLAN</b>	E06	P	<b>LAN Ground.</b> Connect to GND through a ferrite bead.
<b>VBAT</b>	AF04	P	<b>RTC Battery.</b> Battery input for internal RTC (RTCX1, RTCX2).
<b>VCC15</b>	(see ball list)	P	<b>Core Power.</b> 1.5V ±5%. This supply is turned on only when the mechanical switch on the power supply is turned on and the PWRON signal is conditioned high.
<b>VCC15LAN</b>	E07	P	<b>LAN Power.</b> 1.5V ±5%. Power for LAN. Connect to VCC through a ferrite bead.
<b>VCC15VL</b>	(see ball list)	P	<b>V-Link Compensation Circuit Voltage.</b> 1.5V ±5%
<b>VCC33</b>	(see ball list)	P	<b>I/O Power.</b> 3.3V ±5%
<b>VCC33MII</b>	D09, E09 E10, E11	P	<b>MII I/O Power.</b> 3.3V ±5% I/O Power for LAN Media Independent Interface (interface to external PHY). Connect to VSUS33 suspend power.
<b>VSUS15</b>	T04, U04	P	<b>Suspend Power.</b> 1.5V ±5%.
<b>VSUS15MII</b>	D12, E12	P	<b>MII Suspend Power.</b> 1.5V ±5%.
<b>VSUS15USB</b>	C24	P	<b>USB Suspend Power.</b> 1.5V ±5%.
<b>VSUS33</b>	AA04, AB04, AB05, AB06	P	<b>Suspend Power.</b> 3.3V ±5%. Always available unless the mechanical switch of the power supply is turned off. If the “soft-off” state is not implemented, then these signal balls can be connected to VCC33.

Strapping Signal Table

<b>Strapping Signal</b> (External pullup / pulldown straps are required to select "H" / "L")				
Strap Pins for VT8237S Configuration				
Signal	Ball#	Function	Description	Note
AZSDOUT	U02	Auto Reboot	L: Enable Auto Reboot H: Disable Auto Reboot Default setting: Disable	
AZSYNC	T02	LPC FWH Command	L: Enable LPC FWH Command H: Disable LPC FWH Command Default setting: Disable	
SPKR	AF8	CPU Frequency Strapping	L: Enable CPU Frequency Strapping H: Disable CPU Frequency Strapping Default setting: Disable	
SEEDI	A12	External LAN EEPROM	L: Enable external EEPROM H: Disable external EEPROM Default setting: Enable	
SUSA#	AA02	Integrated LAN Reset Method	L: For Notebook (without wake on LAN feature from S4 / S5) H: For Desktop	
Strap Pins for North Bridge ("NB") Configuration				
PDCS3#	V23	NB Configuration	PDCS3# signal state is reflected on signal VD7 during power up for North Bridge configuration.	Check the North Bridge DS for details
PDA2	W24	NB Configuration	PDA2 signal state is reflected on signal VD6 during power up for North Bridge configuration.	Check the North Bridge DS for details
PDA1	V25	NB Configuration	PDA1 signal state is reflected on signal VD5 during power up for North Bridge configuration.	Check the North Bridge DS for details
GPIOD / PCGNTB	AC06	NB Configuration	GPIOD/PCGNTB signal state is reflected on signal VD3 during power up for North Bridge configuration.	Check the North Bridge DS for details
GPIOB / PCREQB	AD05	NB Configuration	GPIOB/PCREQB signal state is reflected on signal VD2 during power up for North Bridge configuration.	Check the North Bridge DS for details
PDA0, GPIOA / PCREQA, GPIOC / PCGNTA	W23 AE05 AF05	NB Configuration	PDA0, GPIOA/PCREQA and GPIOC/PCGNTA signal states are reflected on signals VD4, VD1 and VD0 during power up for North Bridge configuration.	Check the North Bridge DS for details

Summary of Internal Pull-Up / Pull-Down Resistor Implementation

Internal Pullups are present on signals SERIRQ and LAD[3:0]

Internal Pulldowns are present on all LAN signals except MDIO. MDIO is an internal pull-up signal.

## REGISTER OVERVIEW

In the register descriptions, column “Default” indicates the default value of register bit. While column “Attribute” indicates access type of register bit.

### Abbreviation

#### Attribute Definitions:

**Read / Write Attributes:** read / write attributes may be used together to specify combined attributes

- RO:** Read Only.
- RZ:** Read as Zero.
- R1:** Read as 1.
- IW:** Ignore Write.
- MW:** Must Write back what is read.
- XW:** Backdoor Write.
- W:** Write Only. (register value can not be read by the software)
- RW:** Read / Write.
- RW1:** Write Once then Read Only after that.
- RW1C:** Read / Write of “1” clears bit to zero.
- RsvdP:** Reserved. Must do a read-modify-write to preserve the bit values.
- RsvdZ:** Reserved. Must write 0’s.
- RSM:** Bits are in resume-well.

**Sticky Attributes:** adding a “S” in tail to indicate a sticky register, which means that register will not be set or altered by hot reset.

Ex. **RWS:** Sticky-Read/Write. **ROS:** Sticky-Read Only. **RW1CS:** Sticky-Write-1-to-Clear.

#### Default Value Definitions

- Dip:** Means the default value is set by dip switch or strapping.
- HwInit:** Hardware initialized; bit default value is set by hardware to reflect related status.

#### PCI Device & Function Definitions

There are six PCI devices and up to 13 PCI functions are implemented in this chip. To specifically identify a PCI function, the following abbreviations will be applied in subsequent sections.

- B0D15F0:** Bus 0, Device 15, Function 0 – Serial ATA Controller
- B0D15F1:** Bus 0, Device 15, Function 1 – Parallel ATA Controller
- B0D16F0:** Bus 0, Device 16, Function 0 – USB 1.1 UHCI Ports 0-1
- B0D16F1:** Bus 0, Device 16, Function 1 – USB 1.1 UHCI Ports 2-3
- B0D16F2:** Bus 0, Device 16, Function 2 – USB 1.1 UHCI Ports 4-5
- B0D16F3:** Bus 0, Device 16, Function 3 – USB 1.1 UHCI Ports 6-7
- B0D16F4:** Bus 0, Device 16, Function 4 – USB 2.0 EHCI Ports 0-7
- B0D17F0:** Bus 0, Device 17, Function 0 – Bus Controller and Power Management
- B0D17F7:** Bus 0, Device 17, Function 7 – Ultra V-Link Control
- B0D18F0:** Bus 0, Device 18, Function 0 – VIA LAN Controller
- B0D19F0:** Bus 0, Device 19, Function 0 – PCI-to-PCIe Bridge
- B0D19F1:** Bus 0, Device 19, Function 1 – PCI-to-PCI Bridge
- BnD1F0:** Bus n, Device 1, Function 0 – High Definition Audio Controller

**Power Management Register Space Definitions**

The following abbreviations are used to identify the register spaces used in Power Management Unit (**B0D17F0**).

**PMIO:** ACPI I/O space

**PM-MMIO:** Power Management Memory Mapped I/O space

**SMIO:** System Management Bus I/O space

**Other Abbreviations**

The following abbreviations are also implemented in this document.

**HDAC:** High Definition Audio Controller (*Implemented in BnD1F0*)

**HDAC-MMIO :** HDAC Memory-Mapped I/O space

**SPI-MMIO :** SPI Memory-Mapped I/O space

## REGISTER DESCRIPTIONS

### Legacy I/O Ports

This group of registers includes the DMA Controllers, Interrupt Controllers, and Timer/Counters as well as a number of miscellaneous ports originally implemented using discrete logic on original PC/AT motherboards. All of the registers listed are integrated on-chip. These registers are implemented in a precise manner for backwards compatibility with previous generations of PC hardware. These registers are listed for information purposes only. Detailed descriptions of the actions and programming of these registers are included in numerous industry publications (duplication of that information here is beyond the scope of this document). All of these registers reside in I/O space.

**Table 4. System I/O Map**

Port	Function	Actual Port Decoding
00-1F	<b>Master DMA Controller</b>	0000 0000 000x xxxx
20-3F	<b>Master Interrupt Controller</b>	0000 0000 001x xxxx
40-5F	<b>Timer / Counter</b>	0000 0000 010x xxxx
60-6F	<b>Keyboard Controller</b>	0000 0000 0110 xxxx
(60h)	<b>KBC Data</b>	0000 0000 0110 x0x0
(61h)	<b>Misc Functions &amp; Speaker Control</b>	0000 0000 0110 xxx1
(64h)	<b>KBC Command / Status</b>	0000 0000 0110 x1x0
70-77	<b>RTC/CMOS/NMI-Disable</b>	0000 0000 0111 0xxx
78-7F	<b>-available for system use</b>	0000 0000 0111 1xxx
80	<b>-reserved- (debug port)</b>	0000 0000 1000 0000
81-8F	<b>DMA Page Registers</b>	0000 0000 1000 xxxx
90-91	<b>-available for system use-</b>	0000 0000 1001 000x
92	<b>System Control</b>	0000 0000 1001 0010
93-9F	<b>-available for system use</b>	0000 0000 1001 xxxx
A0-BF	<b>Slave Interrupt Controller</b>	0000 0000 101x xxxx
C0-DF	<b>Slave DMA Controller</b>	0000 0000 110x xxxx
E0-FF	<b>-available for system use</b>	0000 0000 111x xxxx
100-CF7	<b>-available for system use</b>	
CF8-CFB	<b>PCI Configuration Address</b>	0000 1100 1111 10xx
CFC-CFF	<b>PCI Configuration Data</b>	0000 1100 1111 11xx
D00-FFFF	<b>-available for system use-</b>	

## Miscellaneous Functions and System Control

### I/O Port Address: 61h

#### Miscellaneous Functions & Speaker Control

**Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	<b>SERR# Status</b> 0: SERR# has not been asserted Note: This bit is set when the PCI bus SERR# signal is asserted. Once set, this bit may be cleared by setting bit-2 of this register. Bit-2 should be cleared to enable recording of the next SERR# (i.e., bit-2 must be set to 0 to enable this bit to be set).
6	RO	0	<b>IOCHK# Status</b> 0: IOCHK# has not been asserted Note: This bit is set when the ISA bus IOCHCK# signal is asserted. Once set, this bit may be cleared by setting bit-3 of this register. Bit-3 should be cleared to enable recording of the next IOCHCK# (i.e., bit-3 must be set to 0 to enable this bit to be set). IOCHCK# generates NMI to the CPU if NMI is enabled.
5	RO	0	<b>Timer/Counter 2 Output</b> This bit reflects the output of Timer/Counter 2 without any synchronization.
4	RO	0	<b>Refresh Detected</b> This bit toggles on every rising edge of the ISA bus REFRESH# signal.
3	RW	0	<b>IOCHK# Enable</b> 0: Enable (see bit-6 above) 1: Disable (force IOCHCK# inactive and clear any "IOCHCK# Active" condition in bit-6)
2	RW	0	<b>SERR# Enable</b> 0: Enable (see bit-7 above) 1: Disable (force SERR# inactive and clear any "SERR# Active" condition in bit-7)
1	RW	0	<b>Speaker Enable</b> 0: Disable 1: Enable Timer/Counter 2 output to drive SPKR pin
0	RW	0	<b>Timer/Counter 2 Enable</b> 0: Disable 1: Enable Timer/Counter 2

### I/O Port Address: 92h

#### System Control

**Default Value: 00h**

Bit	Attribute	Default	Description
7:2	RO	0	<b>Reserved</b>
1	RW	0	<b>A20 Address Line Enable</b> 0: A20 disabled / forced 0 (real mode) 1: A20 address line enabled
0	RW	0	<b>High Speed Reset</b> 0: Normal 1: Briefly pulse system reset to switch from protected mode to real mode

### **Keyboard Controller I/O Registers**

The keyboard controller handles the keyboard and mouse interfaces. Two ports are used: port 60h and port 64h. Reads from port 64h returns a status byte. Writes to port 64h are command codes (see command code list following the register descriptions). Input and output data is transferred via port 60h.

A “Control” register is also available. It is accessible by writing commands 20h / 60h to the command port (port 64h); the control byte is written by first sending 60h to the command port, then sending the control byte value. The control register may be read by sending a command of 20h to port 64h, waiting for “Output Buffer Full” status = 1, then reading the control byte value from port 60h.

Traditional (non-integrated) keyboard controllers have an “Input Port” and an “Output Port” that control pins dedicated to specific functions. In the integrated version, connections are hard wired as listed below. Outputs are “open-collector” so to allow input on one of these pins, the output value for that pin would be set high (non-driving) and the desired input value read on the input port. These ports are defined as follows:

<b>Bit</b>	<b>Input Port</b>
0	Keyboard Data In
1	Mouse Data In
<b>Bit</b>	<b>Output Port</b>
0	System Reset (1 = Execute Reset)
1	Gate A20 (1 = A20 Enabled)
2	Mouse Data Out
3	Mouse Clock Out
6	Keyboard Clock Out
7	Keyboard Data Out
<b>Bit</b>	<b>Test Port</b>
0	Keyboard Clock In
1	Mouse Clock In

### **Hardwired Internal Connections**

Keyboard Data Out (Open Collector) <=> Keyboard Data In

Keyboard Clock Out (Open Collector) <=> Keyboard Clock In

Mouse Data Out (Open Collector) <=> Mouse Data In

Mouse Clock Out (Open Collector) <=> Mouse Clock In

Keyboard OBF Interrupt => IRQ1

Mouse OBF Interrupt => IRQ12

### **Input / Output / Test Port Command Codes**

C0h transfers input port data to the output buffer.

D0h copies output port values to the output buffer.

E0h transfers test input port data to the output buffer.

The above definitions are provided for reference only as actual keyboard and mouse control is no longer performed bit-by bit using the above ports but controlled directly by keyboard / mouse controller internal logic. Data is sent and received using the command codes listed on the following page.

### **I/O Port Address: 60h**

#### **Keyboard Controller Input / Output Buffer**

<b>Bit</b>	<b>Attribute</b>	<b>Description</b>
7:0	WO	<b>Keyboard Controller Input Buffer</b> Only write to port 60h if port 64h bit-1 = 0 (1=full).
7:0	RO	<b>Keyboard Controller Output Buffer</b> Only read from port 60h if port 64h bit-0 = 1 (0=empty).

**I/O Port Address: 64h**
**Keyboard / Mouse Status**
**Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	<b>Parity Error</b> 0: No parity error (odd parity received) 1: Even parity occurred on last byte received from keyboard / mouse
6	RO	0	<b>General Receive / Transmit Timeout</b> 0: No Error 1: Error
5	RO	0	<b>Mouse Output Buffer Full</b> 0: Mouse output buffer empty 1: Mouse output buffer holds mouse data
4	RO	0	<b>Keylock Status</b> 0: Locked 1: Free
3	RO	0	<b>Command / Data</b> 0: Last write was data write 1: Last write was command write
2	RO	0	<b>System Flag</b> 0: Power-On Default 1 Self Test Successful
1	RO	0	<b>Input Buffer Full</b> 0: Input Buffer Empty 1: Input Buffer Full
0	RO	0	<b>Keyboard Output Buffer Full</b> 0: Keyboard Output Buffer Empty 1: Keyboard Output Buffer Full

**KBC Control Register (R/W via Commands 20h/60h)**

Bit	Attribute	Default	Description
7	RO	0	<b>Reserved</b>
6	RW	1b	<b>PC Compatibility</b> 0: Disable scan conversion 1: Convert scan codes to PC format; convert 2-byte break sequences to 1-byte PC-compatible break codes
5	RW	0	<b>Mouse Interface</b> 0: Enable 1: Disable
4	RW	0	<b>Keyboard Interface</b> 0: Enable 1: Disable
3	RO	0	<b>Reserved</b>
2	RO	0	<b>System Flag</b> This bit may be read back as status register bit-2
1	RW	0	<b>Mouse Interrupts</b> 0: Disable 1: Enable - Generate interrupt on IRQ12 when mouse data comes into output buffer
0	RW	0	<b>Keyboard Interrupts</b> 0: Disable 1: Enable - Generate interrupt on IRQ1 when output buffer has been written.

**I/O Port Address: 64h**
**Keyboard / Mouse Command**

This port is used to send commands to the keyboard / mouse controller. The command codes recognized by the VT8237S South Bridge are listed in the table below.

**Table 5. Keyboard Controller Command Codes**

<b>Code</b>	<b>Keyboard Command Code Description</b>
20h	Read Control Byte (next byte is Control Byte)
21-3Fh	Read SRAM Data (next byte is Data Byte)
60h	Write Control Byte (next byte is Control Byte)
61-7Fh	Write SRAM Data (next byte is Data Byte)
A1h	Output Keyboard Controller Version #
A4h	Test if Password is installed (always returns F1h to indicate not installed)
A7h	Disable Mouse Interface
A8h	Enable Mouse Interface
A9h	Mouse Interface Test (puts test results in port 60h) Value: 0=OK, 1=clk stuck low, 2=clk stuck high, 3=data stuck lo, 4=data stuck hi, FF=general error
AAh	KBC self test (returns 55h if OK, FCh if not)
ABh	Keyboard Interface Test (see A9h Mouse Test)
ADh	Disable Keyboard Interface
AEh	Enable Keyboard Interface
AFh	Return Version #
C0h	Read Input Port (read input data to output buffer)
C1h	Poll Input Port (read Mouse Data In continuously to status bit 5)
C8h	Unblock Mouse Output (use before D1 to change active mode)
C9h	Reblock Mouse Output (protection mechanism for D1)
Cah	Read Mode (output KBC mode info to port 60 output buffer: bit-0=0 if ISA, 1 if PS/2)
D0h	Read Output Port (copy output port values to port 60)
D1h	Write Output Port (data byte following is written to keyboard output port as if it came from keyboard)
D2h	Write Keyboard Output Buffer & clear status bit-5 (write following byte to keyboard)
D3h	Write Mouse Output Buffer & set status bit-5 (write following byte to mouse; put value in mouse input buffer so it appears to have come from the mouse)
D4h	Write Mouse (write following byte to mouse)
E0h	Read Keyboard Clock In and Mouse Clock In (return in bits 0-1 respectively of response byte)
Exh	Set Mouse Clock Out per command bit 3 Set Mouse Data Out per command bit 2 Set Gate A20 per command bit 1
Fxh	Pulse Mouse Clock Out low for 6usec per cmd bit 3 Pulse Mouse Data Out low for 6usec per cmd bit 2 Pulse Gate A20 low for 6usec per command bit 1 Pulse System Reset low for 6usec per cmd bit 0

Note: All other codes not listed are undefined.

### **DMA Controller I/O Registers**

Channels 0-3 of the Master DMA Controller control System DMA Channels 0-3. There are 16 Master DMA Controller registers. Channels 0-3 of the Slave DMA Controller control System DMA Channels 4-7. There are 16 Slave DMA Controller registers.

The Master and Slave DMA Controllers are compatible with the Intel 8237 DMA Controller chip. Detailed description of 8237 DMA controller operations can be obtained from the Intel Peripheral Components Data Book and numerous other industry publications.

**Table 6. DMA Controller I/O Registers Map**

I/O Port Address	Description
<b>Master DMA Controller</b>	
00h	Ch 0 Base / Current Address
01h	Ch 0 Base / Current Count
02h	Ch 1 Base / Current Address
03h	Ch 1 Base / Current Count
04h	Ch 2 Base / Current Address
05h	Ch 2 Base / Current Count
06h	Ch 3 Base / Current Address
07h	Ch 3 Base / Current Count
08h	Status / Command
09h	Write Request
0Ah	Write Single Mask
0Bh	Write Mode
0Ch	Clear Byte Pointer F/F
0Dh	Master Clear
0Eh	Clear Mask
0Fh	R/W All Mask Bits
<b>Slave DMA Controller</b>	
C0h	Ch 4 Base / Current Address
C2h	Ch 4 Base / Current Count
C4h	Ch 5 Base / Current Address
C6h	Ch 5 Base / Current Count
C8h	Ch 6 Base / Current Address
CAh	Ch 6 Base / Current Count
CCh	Ch 7 Base / Current Address
CEh	Ch 7 Base / Current Count
D0h	Status / Command
D2h	Write Request
D4h	Write Single Mask
D6h	Write Mode
D8h	Clear Byte Pointer F/F
DAh	Master Clear
DCh	Clear Mask
DEh	Read/Write All Mask Bits
<b>DMA Page Registers</b>	
81h	Channel 2 DMA Page (M-2)
82h	Channel 3 DMA Page (M-3)
83h	Channel 1 DMA Page (M-1)
87h	Channel 0 DMA Page (M-0)
89h	Channel 6 DMA Page (S-2)
8Ah	Channel 7 DMA Page (S-3)
8Bh	Channel 5 DMA Page (S-1)
8Fh	Channel 4 DMA Page (S-0)

Note: Not all bits of the address are decoded.

**I/O Port Address: 00h**
**Ch 0 Base / Current Address**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	<b>Ch 0 Base / Current Address</b>

**I/O Port Address: 01h**
**Ch 0 Base / Current Count**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	<b>Ch 0 Base / Current Count</b>

**I/O Port Address: 02h**
**Ch 1 Base / Current Address**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	<b>Ch 1 Base / Current Address</b>

**I/O Port Address: 03h**
**Ch 1 Base / Current Count**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	<b>Ch 1 Base / Current Count</b>

**I/O Port Address: 04h**
**Ch 2 Base / Current Address**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	<b>Ch 2 Base / Current Address</b>

**I/O Port Address: 05h**
**Ch 2 Base / Current Count**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	<b>Ch 2 Base / Current Count</b>

**I/O Port Address: 06h**
**Ch 3 Base / Current Address**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	<b>Ch 3 Base / Current Address</b>

**I/O Port Address: 07h**
**Ch 3 Base / Current Count**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	<b>Ch 3 Base / Current Count</b>

**I/O Port Address: 08h**
**Status / Command**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	Status / Command

**I/O Port Address: 09h**
**Write Request**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	WO	0	Write Request

**I/O Port Address: 0Ah**
**Write Single Mask**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	WO	0	Write Single Mask

**I/O Port Address: 0Bh**
**Write Mode**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	WO	0	Write Mode

**I/O Port Address: 0Ch**
**Clear Byte Pointer F/F**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	WO	0	Clear Byte Pointer F/F

**I/O Port Address: 0Dh**
**Master Clear**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	WO	0	Master Clear

**I/O Port Address: 0Eh**
**Clear Mask**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	WO	0	Clear Mask

**I/O Port Address: 0Fh**
**R/W All Mask Bits**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	R/W All Mask Bits

**I/O Port Address: C0h**
**Ch 4 Base / Current Address**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	<b>Ch 4 Base / Current Address</b>

**I/O Port Address: C2h**
**Ch 4 Base / Current Count**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	<b>Ch 4 Base / Current Count</b>

**I/O Port Address: C4h**
**Ch 5 Base / Current Address**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	<b>Ch 5 Base / Current Address</b>

**I/O Port Address: C6h**
**Ch 5 Base / Current Count**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	<b>Ch 5 Base / Current Count</b>

**I/O Port Address: C8h**
**Ch 6 Base / Current Address**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	<b>Ch 6 Base / Current Address</b>

**I/O Port Address: CAh**
**Ch 6 Base / Current Count**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	<b>Ch 6 Base / Current Count</b>

**I/O Port Address: CCh**
**Ch 7 Base / Current Address**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	<b>Ch 7 Base / Current Address</b>

**I/O Port Address: CEh**
**Ch 7 Base / Current Count**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	<b>Ch 7 Base / Current Count</b>

**I/O Port Address: D0h**
**Status / Command**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	Status / Command

**I/O Port Address: D2h**
**Write Request**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	WO	0	Write Request

**I/O Port Address: D4h**
**Write Single Mask**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	WO	0	Write Single Mask

**I/O Port Address: D6h**
**Write Mode**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	WO	0	Write Mode

**I/O Port Address: D8h**
**Clear Byte Pointer F/F**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	WO	0	Clear Byte Pointer F/F

**I/O Port Address: DAh**
**Master Clear**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	WO	0	Master Clear

**I/O Port Address: DCh**
**Clear Mask**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	WO	0	Clear Mask

**I/O Port Address: DEh**
**Read/Write All Mask Bits**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	WO	0	Read/Write All Mask Bits

There are eight DMA Page Registers, one for each DMA channel. These registers provide bits 16-23 of the 24-bit address for each DMA channel (bits 0-15 are stored in registers in the Master and Slave DMA Controllers). They are located at the following I/O Port addresses.

**I/O Port Address: 81h**
**Channel 2 DMA Page (M-2)**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	Channel 2 DMA Page (M-2)

**I/O Port Address: 82h**
**Channel 3 DMA Page (M-3)**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	Channel 3 DMA Page (M-3)

**I/O Port Address: 83h**
**Channel 1 DMA Page (M-1)**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	Channel 1 DMA Page (M-1)

**I/O Port Address: 87h**
**Channel 0 DMA Page (M-0)**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	Channel 0 DMA Page (M-0)

**I/O Port Address: 89h**
**Channel 6 DMA Page (S-2)**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	Channel 6 DMA Page (S-2)

**I/O Port Address: 8Ah**
**Channel 7 DMA Page (S-3)**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	Channel 7 DMA Page (S-3)

**I/O Port Address: 8Bh**
**Channel 5 DMA Page (S-1)**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	Channel 5 DMA Page (S-1)

**I/O Port Address: 8Fh**
**Channel 4 DMA Page (S-0)**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	Channel 4 DMA Page (S-0)

### DMA Controller Shadow Registers

The DMA Controller shadow registers are enabled by setting B0D17F0 Rx40 [1]. If the shadow registers are enabled, they are read back at the indicated I/O port instead of the standard DMA controller registers (writes are unchanged).

Port Address	Attribute	Description
Port 0	RO	Channel 0 Base Address
Port 1	RO	Channel 0 Byte Count
Port 2	RO	Channel 1 Base Address
Port 3	RO	Channel 1 Byte Count
Port 4	RO	Channel 2 Base Address
Port 5	RO	Channel 2 Byte Count
Port 6	RO	Channel 3 Base Address
Port 7	RO	Channel 3 Byte Count
Port 8	RO	1st Read Channel 0-3 Command Register
Port 8	RO	2nd Read Channel 0-3 Request Register
Port 8	RO	3rd Read Channel 0 Mode Register
Port 8	RO	4th Read Channel 1 Mode Register
Port 8	RO	5th Read Channel 2 Mode Register
Port 8	RO	6th Read Channel 3 Mode Register
Port F	RO	Channel 0-3 Read All Mask
Port C4	RO	Channel 5 Base Address
Port C6	RO	Channel 5 Byte Count
Port C8	RO	Channel 6 Base Address
Port CA	RO	Channel 6 Byte Count
Port CC	RO	Channel 7 Base Address
Port CE	RO	Channel 7 Byte Count
Port D0	RO	1st Read Channel 4-7 Command Register
Port D0	RO	2nd Read Channel 4-7 Request Register
Port D0	RO	3rd Read Channel 4 Mode Register
Port D0	RO	4th Read Channel 5 Mode Register
Port D0	RO	5th Read Channel 6 Mode Register
Port D0	RO	6th Read Channel 7 Mode Register
Port DE	RO	Channel 4-7 Read All Mask

### Interrupt Controller I/O Registers

The Master and Slave Interrupt Controllers are compatible with the Intel 8259 Interrupt Controller chip. The Slave Interrupt Controller controls system interrupt channels 8-15. Detailed descriptions of 8259 Interrupt Controller operations can be obtained from the Intel Peripheral Components Data Book and numerous other industry publications.

**Table 7. Interrupt Controller I/O Registers Map**

I/O Port Address	Description
20h	Master Interrupt Control
21h	Master Interrupt Mask
A0h	Slave Interrupt Control
A1h	Slave Interrupt Mask

Not all bits of the address are decoded.

#### I/O Port Address: 20h

##### Master Interrupt Control

**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	Master Interrupt Control

#### I/O Port Address: 21h

##### Master Interrupt Mask

**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	Master Interrupt Mask

#### I/O Port Address: A0h

##### Slave Interrupt Control

**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	Slave Interrupt Control

#### I/O Port Address: A1h

##### Slave Interrupt Mask

**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	Slave Interrupt Mask

### Interrupt Controller Shadow Registers

The following shadow registers are enabled by setting B0D17F0 Rx40[1]. If the shadow registers are enabled, they are read back at the indicated I/O port instead of the standard interrupt controller registers (writes are unchanged).

#### I/O Port Address: 20h

##### Master Interrupt Control Shadow

#### I/O Port Address: A0h

##### Slave Interrupt Control Shadow

Bit	Attribute	Description
7	RO	<b>Reserved</b>
6	RO	<b>OCW3 bit 2 (POLL)</b>
5	RO	<b>OCW3 bit 0 (RIS)</b>
4	RO	<b>OCW3 bit 5 (SMM)</b>
3	RO	<b>OCW2 bit 7 (R)</b>
2	RO	<b>ICW4 bit 4 (SFNM)</b>
1	RO	<b>ICW4 bit 1 (AEOI)</b>
0	RO	<b>ICW1 bit 3 (LTIM)</b>

#### I/O Port Address: 21h

##### Master Interrupt Mask Shadow

#### I/O Port Address: A1h

##### Slave Interrupt Mask Shadow

Bit	Attribute	Default	Description
7:5	RO	0	<b>Reserved</b>
4:0	RO	—	<b>T7-T3 of Interrupt Vector Address</b>

Timer / Counter Registers
**Table 8. Timer / Counter I/O Registers Map**

I/O Port Address	Description
40h	Timer / Counter 0 Count
41h	Timer / Counter 1 Count
42h	Timer / Counter 2 Count
43h	Timer / Counter Cmd Mode

Note:

- 1) Not all bits of the address are decoded.
- 2) The Timer / Counters are compatible with the Intel 8254 Timer / Counter chip. Detailed descriptions of 8254 Timer / Counter operation can be obtained from the Intel Peripheral Components Data Book and numerous other industry publications.

I/O Port Address: 40h
Timer / Counter 0 Count
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	Timer / Counter 0 Count

I/O Port Address: 41h
Timer / Counter 1 Count
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	Timer / Counter 1 Count

I/O Port Address: 42h
Timer / Counter 2 Count
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	Timer / Counter 2 Count

I/O Port Address: 43h
Timer / Counter Cmd Mode
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	WO	0	Timer / Counter Cmd Mode

Timer / Counter Shadow Registers

The following shadow registers are enabled for readback by setting B0D17F0 Rx40[1]. If the shadow registers are enabled, they are read back at the indicated I/O port instead of the standard timer / counter registers (writes are unchanged).

Port Address	Attribute	Description
Port 40	RO	Counter 0 Base Count Value (LSB 1st MSB 2nd)
Port 41	RO	Counter 1 Base Count Value (LSB 1st MSB 2nd)
Port 42	RO	Counter 2 Base Count Value (LSB 1st MSB 2nd)

## CMOS / RTC I/O Registers

### I/O Port Address: 70h

#### CMOS Address

Bit	Attribute	Default	Description
7	RW	1b	<b>NMI Disable</b> 0: Enable NMI Generation. NMI is asserted on encountering SERR# on the PCI bus. 1: Disable NMI Generation
6:0	RW	—	<b>CMOS Address</b> (lower 128 bytes)

### I/O Port Address: 71h

#### CMOS Data

Bit	Attribute	Default	Description
7:0	RW	0	<b>CMOS Data</b> (128 bytes)

Note: Ports 70-71 may be accessed if B0D17F0 Rx51[3] is set to one to select the internal RTC. If Rx51[3] is set to zero, accesses to ports 70-71 will be directed to an external RTC.

### I/O Port Address: 74h

#### CMOS Address

Bit	Attribute	Default	Description
7:0	RW	0	<b>CMOS Address</b> (256 bytes)

### I/O Port Address: 75h

#### CMOS Data

Bit	Attribute	Default	Description
7:0	RW	0	<b>CMOS Data</b> (256 bytes)

Note: Ports 74-75 may be accessed only if B0D17F0 Rx4E[3] (Port 74/75 Access Enable) is set to one to enable port 74/75 access.

Note: Ports 70-71 are compatible with PC industry-standards and may be used to access the lower 128 bytes of the 256-byte on-chip CMOS RAM. Ports 74-75 may be used to access the full on-chip extended 256-byte space in cases where the on-chip RTC is disabled.

Note: The system Real Time Clock (RTC) is part of the “CMOS” block. The RTC control registers are located at specific offsets in the CMOS data area (0-0Dh and 7D-7Fh). Detailed descriptions of CMOS / RTC operation and programming can be obtained from the VIA VT82887 Data Book or numerous other industry publications. For reference, the definition of the RTC register locations and bits are summarized in the following table:

**Table 9. CMOS Register Summary**

Offset	Description		
	Register Function	Binary Range	BCD Range
00	Seconds	00-3Bh	00-59h
01	Seconds Alarm	00-3Bh	00-59h
02	Minutes	00-3Bh	00-59h
03	Minutes Alarm	00-3Bh	00-59h
04	Hours	am 12hr 01-1Ch	01-12h
		pm 12hr 81-8Ch	81-92h
		24hr: 00-17h	00-23h
05	Hours Alarm	am 12hr: 01-1Ch	01-12h
		pm 12hr: 81-8Ch	81-92h
		24hr: 00-17h	00-23h
06	Day of the Week	Mon=1: 01-07h	01-07h
07	Day of the Month	01-1Fh	01-31h
08	Month	01-0Ch	01-12h
09	Year	00-63h	00-99h
	Register Function	Bit Description	
0A	Register A	7:	UIP Update In Progress
		6:4:	DV2-0 Divide (010=ena osc & keep time)
		3:0:	RS3-0 Rate Select for Periodic Interrupt
0B	Register B	7:	SET Inhibit Update Transfers
		6:	PIE Periodic Interrupt Enable
		5:	AIE Alarm Interrupt Enable
		4:	UIE Update Ended Interrupt Enable
		3:	SQWE No function (read/write bit)
		2:	DM Data Mode (0=BCD; 1=Binary)
		1:	24/12 Hours Byte Format
		0:	DSE Daylight Savings Enable
0C	Register C	7:	IRQF Interrupt Request Flag
		6:	PF Periodic Interrupt Flag
		5:	AF Alarm Interrupt Flag
		4:	UF Update Ended Flag
		3:0	Unused (always read 0)
0D	Register D	7:	VRT Reads 1 if VBAT voltage is OK
		6:0	Unused (always read 0)
<b>0E-7C Software-Defined Storage Registers</b>			
Offset	Extended Function	Binary Range	BCD Range
7D	Date Alarm	01	01-31h
7E	Month Alarm	01	01-12h
7F	Century Field	13	19-20h

### **Keyboard / Mouse Wakeup Index / Data Registers**

The Keyboard / Mouse Wakeup registers are accessed by performing I/O operations to / from an index / data pair of registers in system I/O space at port addresses 2Eh and 2Fh. The registers accessed using this mechanism are used to initialize Keyboard / Mouse Wakeup functions at index values in the range of E0-EF.

Keyboard / Mouse Wakeup initialization is accomplished in three steps:

- 1) Enter initialization mode (set B0D17F0 Rx51[1] = 1)
- 2) Initialize the chip
  - a) Write index to port 2Eh
  - b) Read / write data from / to port 2Fh
  - c) Repeat a and b for all desired registers

Exit initialization mode (set B0D17F0 Rx51[1] = 0)

#### **I/O Port Address: 2Eh**

##### **Keyboard Wakeup Index**

Bit	Attribute	Default	Description
7:0	RW	0	<b>Index Value</b> B0D17F0 PCI configuration space register Rx51[1] must be set to 1 to enable access to the configuration registers.

#### **I/O Port Address: 2Fh**

##### **Keyboard Wakeup Data**

Bit	Attribute	Default	Description
7:0	RW	0	<b>Data Value</b>

### **Keyboard / Mouse Wakeup Registers**

These registers are accessed via the port 2E / 2F index / data register pair with B0D17F0 Rx51[1] = 1 using the indicated index values below.

#### **Offset Address: E0h**

##### **Keyboard / Mouse Wakeup Enable**

**Default Value: 08h**

Bit	Attribute	Default	Description
7:4	RO	0	<b>Reserved</b>
3	RW	1b	<b>Win98 Keyboard Power Key Wake-up</b> 0: Disable 1: Enable
2	RW	0	<b>Password Wake-up</b> 0: Disable 1: Enable
1	RW	0	<b>PS/2 Mouse Wake-up</b> 0: Disable 1: Enable
0	RW	0	<b>Keyboard Wake-up</b> 0: Disable 1: Enable

#### **Offset Address: E1h**

##### **Keyboard Wakeup Scan Code Set 0**

**Default Value: F0h**

Bit	Attribute	Default	Description
7:0	RW	F0h	<b>Keyboard Wakeup First Reference Scan Code</b> Write 00h means that Keyboard supports any key wake up.

#### **Offset Address: E2h**

##### **Keyboard Wakeup Scan Code Set 1**

**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	<b>Keyboard Wakeup Second Reference Scan Code</b> Write 00h means that PS/2 mouse supports any key wakeup.

#### **Offset Address: E3h**

##### **Keyboard Wakeup Scan Code Set 2**

**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	<b>Keyboard Wakeup Third Reference Scan Code</b>

#### **Offset Address: E4h**

##### **Keyboard Wakeup Scan Code Set 3**

**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	<b>Keyboard Wakeup Fourth Reference Scan Code</b>

#### **Offset Address: E5h**

##### **Keyboard Wakeup Scan Code Set 4**

**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	<b>Keyboard Wakeup Fifth Reference Scan Code</b>

**Offset Address: E6h**
**Keyboard Wakeup Scan Code Set 5**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	Keyboard Wakeup Sixth Reference Scan Code

**Offset Address: E7h**
**Keyboard Wakeup Scan Code Set 6**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	Keyboard Wakeup Seventh Reference Scan Code

**Offset Address: E8h**
**Keyboard Wakeup Scan Code Set 7**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	Keyboard Wakeup Eighth Reference Scan Code

**Offset Address: E9h**
**Mouse Wakeup Scan Code Set 1**
**Default Value: 09h**

Bit	Attribute	Default	Description
7:0	RW	09h	Mouse Wakeup Scan Code Set 1

**Offset Address: EAh**
**Mouse Wakeup Scan Code Set 2**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	Mouse Wakeup Scan Code Set 2

**Offset Address: EBh**
**Mouse Wakeup Scan Code Mask**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	Mouse Wakeup Scan Code Mask

## Memory Mapped I/O APIC Registers

The IO APIC registers are accessed by an indirect addressing scheme using Index Registers and Data Registers that are mapped into memory space.

**Table 10. Memory Mapped I/O APIC Registers Summary Table**

Memory Address	Function	Size
FEC00000	<b>APIC Index</b>	8 bit
FEC00010	<b>APIC Data</b>	32 bit
FEC00020	<b>APIC IRQ Pin Assertion</b>	8 bit
FEC00040	<b>APIC EOI</b>	8 bit

### Memory Address: FEC00000h

#### APIC Index

**Default Value:** 0000 0000h

Bit	Attribute	Default	Description
31:8	RO	0	<b>Reserved</b>
7:0	RW	0	<b>I/O APIC Index</b> 8-bit pointer to the I/O APIC register

### Memory Address: FEC00010h

#### APIC Data

**Default Value:** 0000 0000h

Bit	Attribute	Default	Description
31:0	RW	0	<b>I/O APIC Data</b> This is a 32-bit register for the data to be read or written to the I/O APIC indirect register pointed by the Index Register.

### Memory Address: FEC00020h

#### APIC IRQ Pin Assertion

**Default Value:** nnh

Bit	Attribute	Default	Description
7:5	RO	—	<b>Reserved</b>
4:0	WO	nnh	<b>IRQ Number</b> Bits 4:0 written to this register contain the IRQ number for this interrupt. The only valid values are 0-23.

### Memory Address: FEC00040h

#### APIC EOI

**Default Value:** nnh

Bit	Attribute	Default	Description
7:0	WO	nnh	<b>Redirection Entry Clear</b> When a write is issued to this register, the I/O APIC will check this field and compare it with the vector field for each entry in the I/O Redirection Table. When a match is found, the “RemoteIRR” (Indexed I/O APIC Rx10-3F[14]) registers bit for that I/O Redirection Entry will be cleared.

## Indexed I/O APIC Registers

### Index: 0h

#### I/O APIC Identification

**Default Value:** 0000 0000h

Bit	Attribute	Default	Description
31:28	RO	0	<b>Reserved</b>
27:24	RW	0	<b>I/O APIC Identification</b> Software must program this value before using the I/O APIC.
23:0	RO	0	<b>Reserved</b>

### Index: 1h

#### I/O APIC Version

**Default Value:** 0017 8003h

Bit	Attribute	Default	Description
31:24	RO	0	<b>Reserved</b>
23:16	RO	17h	<b>Maximum Redirection Entry</b> This value is equal to the number of interrupt input pins for the I/O APIC minus one. For this I/O APIC, the value is 17h.
15	RO	1b	<b>PCI IRQ</b> This bit is set to 1 to indicate that this version of the I/O APIC implements the IRQ Assertion register and that PCI devices are allowed to write to it to cause interrupt.
14:8	RO	0	<b>Reserved</b>
7:0	RO	03h	<b>APIC Version</b> The implementation version for this I/O APIC is 03h.

### Index: 2h

#### I/O APIC Arbitration

**Default Value:** 0000 0000h

Bit	Attribute	Default	Description
31:28	RO	0	<b>Reserved</b>
27:24	RO	0	<b>I/O APIC Arbitration ID</b>
23:0	RO	0	<b>Reserved</b>

### Index: 3h

#### Boot Configuration

**Default Value:** 0000 0000h

Bit	Attribute	Default	Description
31:1	RO	0	<b>Reserved</b>
0	RW	0	<b>Delivery Type</b> 0: Interrupt Delivery Mechanism is via the APIC Serial Bus 1: Interrupt Delivery Mechanism is a Front-side Bus Message

**Index: 3F-10h**
**I/O Redirection Table**
**Default Value: nnn1 nnnn nnnn nnnnh**

There are 16 64-bit I/O Redirection Table entry registers. Each register is a dedicated entry for each interrupt input signal.

**Table 11. I/O Redirection Table**

Index	Function
11-10h	I/O APIC Redirection – APIC IRQ0
13-12h	I/O APIC Redirection – APIC IRQ1
15-14h	I/O APIC Redirection – APIC IRQ2
17-16h	I/O APIC Redirection – APIC IRQ3
19-18h	I/O APIC Redirection – APIC IRQ4
1B-1Ah	I/O APIC Redirection – APIC IRQ5
1C-1Dh	I/O APIC Redirection – APIC IRQ6
1E-1Fh	I/O APIC Redirection – APIC IRQ7
21-20h	I/O APIC Redirection – APIC IRQ8
23-22h	I/O APIC Redirection – APIC IRQ9
25-24h	I/O APIC Redirection – APIC IRQ10
27-26h	I/O APIC Redirection – APIC IRQ11
29-28h	I/O APIC Redirection – APIC IRQ12
2B-2Ah	I/O APIC Redirection – APIC IRQ13
2D-2Ch	I/O APIC Redirection – APIC IRQ14
2F-2Eh	I/O APIC Redirection – APIC IRQ15
31-30h	I/O APIC Redirection – APIC IRQ16
33-32h	I/O APIC Redirection – APIC IRQ17
35-34h	I/O APIC Redirection – APIC IRQ18
37-36h	I/O APIC Redirection – APIC IRQ19
39-38h	I/O APIC Redirection – APIC IRQ20
3B-3Ah	I/O APIC Redirection – APIC IRQ21
3D-3Ch	I/O APIC Redirection – APIC IRQ22
3F-3Eh	I/O APIC Redirection – APIC IRQ23



## Configuration Space I/O

Configuration space accesses for all functions use PCI configuration mechanism 1 (see PCI specification revision 2.2 for more details). The ports respond only to double-word accesses. Byte or word accesses will be passed on unchanged.

### I/O Port Address: CFB-CF8h

#### PCI Configuration Address

**Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RW	0	<b>Configuration Space Enable</b> 0: Disabled 1: Convert configuration data port writes to configuration cycles on the PCI bus
30:24	RO	0	<b>Reserved.</b> Always reads 0
23:16	RW	0	<b>PCI Bus Number</b> Used to choose a specific PCI bus in the system.
15:11	RW	0	<b>Device Number</b> Used to choose a specific device in the system (devices 0 and 1 are defined).
10:8	RW	0	<b>Function Number</b> Used to choose a specific function if the selected device supports multiple functions.
7:2	RW	0	<b>Register Number (also called the "Offset")</b> Used to select a specific DWORD in the configuration space.
1:0	RW	0	<b>Fixed</b> (always reads 0)

### I/O Port Address: CFF-CFCCh

#### PCI Configuration Data

**Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	<b>PCI Configuration Data</b>

Note: Refer to PCI Bus Specification Version 2.2 for further details on operation of the above configuration registers.

## Bus 0 Device 15 Function 0 (B0D15F0): Serial ATA Controller

There are 2 ports defined for SATA:

- Port 0: Primary Master port.
- Port 1: Secondary Master port.

### Header Registers (0-4Fh)

#### Offset Address: 1-0h (B0D15F0)

**Vendor ID**

**Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	<b>Vendor ID</b>

#### Offset Address: 3-2h (B0D15F0)

**Device ID**

**Default Value: 5372h**

Bit	Attribute	Default	Description
15:0	RO	5372h	<b>Device ID</b> Note: The value of this field will change dependent on Sub Class Code (0Ah) , If Rx0A = 04h (RAID), Device ID = 7372h If Rx0A = 01h (IDE), Device ID = 5372h

#### Offset Address: 5-4h (B0D15F0)

**PCI Command**

**Default Value: 0000h**

Bit	Attribute	Default	Description
15:11	RO	0	<b>Reserved</b>
10	RW	0	<b>Interrupt Disable</b>
9	RW	0	<b>Enable Fast Back-to-Back</b>
8:7	RO	0	<b>Reserved</b>
6	RO	0	<b>Parity Error Response</b>
5	RO	0	<b>VGA Palette Snooping (Reserved)</b>
4	RO	0	<b>Memory Write and Invalidate</b>
3	RO	0	<b>Respond to Special Cycle</b>
2	RW	0	<b>Bus Master</b>
1	RW	0	<b>Memory Space Access</b>
0	RW	0	<b>I/O Space Access</b> When the “I/O Space” bit is disabled, the device will not respond to I/O addresses.

**Offset Address: 7-6h (B0D15F0)**
**Status Register**
**Default Value: 0290h**

Bit	Attribute	Default	Description
15	RO	0	<b>Detect Parity Error</b>
14	RO	0	<b>Signaled System Error (SERR#)</b>
13	RW1C	0	<b>Received Master Abort</b>
12	RW1C	0	<b>Received Target Abort</b>
11	RO	0	<b>Signaled Target Abort</b>
10:9	RO	01b	<b>DEVSEL# Timing</b> 01b: Medium (default)
8	RO	0	<b>Master Data Parity Detected</b>
7	RO	1b	<b>Fast Back-to-Back Capability</b>
6	RO	0	<b>Reserved</b>
5	RO	0	<b>66 MHz Capable</b>
4	RO	1b	<b>Power Management Capability List</b>
3	RO	0	<b>Interrupt Status</b>
2:0	RO	0	<b>Reserved</b>

**Offset Address: 8h (B0D15F0)**
**Revision ID**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	<b>Revision ID</b>

**Offset Address: 9h (B0D15F0)**
**Programming Interface**
**Default Value: 8Fh**

<b>Configuration 1(When Rx0A = 04h)</b>			
Bit	Attribute	Default	Description
7:0	RO	01h	<b>Programming Interface</b> If Rx0A is 04h, this register will be read as 00h. If Rx0A is 01h, this register will be read as 8Fh.

**Offset Address: 0Ah (B0D15F0)**
**Sub Class Code**
**Default Value: 01h**

Bit	Attribute	Default	Description
7:0	RO	01h	<b>Sub Class</b> 01h: IDE Controller 04h: RAID Controller

**Offset Address: 0Bh (B0D15F0)**
**Base Class Code**
**Default Value: 01h**

Bit	Attribute	Default	Description
7:0	RO	01h	<b>Base Class</b> 01h: Mass Storage Controller

**Offset Address: 0Ch (B0D15F0)**
**Cache Line Size**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	<b>Cache Line Size</b> Fixed at 0

**Offset Address: 0Dh (B0D15F0)**
**Latency Timer**
**Default Value: 20h**

Bit	Attribute	Default	Description
7:4	RW	2h	<b>Latency Timer</b>
3:0	RO	0	<b>Fixed at 0</b>

**Offset Address: 0Eh (B0D15F0)**
**Header Type**
**Default Value: 80h**

Bit	Attribute	Default	Description
7	RO	1b	<b>Multiple Function Device</b>
6:0	RO	0	<b>Fixed at 0</b>

**Offset Address: 0Fh (B0D15F0)**
**Header Type**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	<b>Fixed at 0</b>

**Offset Address: 13-10h (B0D15F0)**
**SATA I Primary Data / Command Base Address**
**Default Value: 0000 0001h**

Specifies an 8 bytes I/O address space.

Bit	Attribute	Default	Description
31:16	RO	0	<b>Reserved</b> (Must be set to 0)
15:3	RW	0	<b>Port Address</b>
2:0	RO	001b	Bit 2:0 fixed at 001b

**Offset Address: 17-14h (B0D15F0)**
**SATA I Primary Control / Status Base Address**
**Default Value: 0000 0001h**

Specifies a 4 bytes I/O address space of which only the third byte is active.

Bit	Attribute	Default	Description
31:16	RO	0	<b>Reserved</b> (Must be set to 0)
15:2	RW	0	<b>Port Address</b>
1:0	RO	01b	Bit 1:0 fix at 01b

**Offset Address: 1B-18h (B0D15F0)**
**SATA I Secondary Data / Command Base Address**
**Default Value: 0000 0001h**

Specifies an 8 bytes I/O address space.

Bit	Attribute	Default	Description
31:16	RO	0	<b>Reserved</b> (Must be set to 0)
15:3	RW	0	<b>Port Address</b>
2:0	RO	001b	Bit 2:0 fixed at 001b

**Offset Address: 1F-1Ch (B0D15F0)**
**SATA I Secondary Control / Status Base Address**
**Default Value: 0000 0001h**

Specifies a 4 bytes I/O address space of which only the third byte is active.

Bit	Attribute	Default	Description
31:16	RO	0	<b>Reserved</b> (Must be set to 0)
15:2	RW	0	<b>Port Address</b>
1:0	RO	01b	Bit 1:0 fix at 01b

**Offset Address: 23-20h (B0D15F0)**
**SATA I Bus Master Control Register Base Address**
**Default Value: 0000 0001h**

Specifies a 16 bytes I/O address space.

Bit	Attribute	Default	Description
31:16	RO	0	<b>Reserved</b> (Must be set to 0)
15:4	RW	0	<b>Port Address</b>
3:0	RO	1h	Bit 3:0 fix at 0001b

**Offset Address: 27-24h (B0D15F0)**
**SATA Control/Status Base Address**
**Default Value: 0000 0001h**

A 128 bytes (2 SATA ports) IO address space

Bit	Attribute	Default	Description
31:16	RO	0	<b>Reserved</b> (Must be set to 0)
15:8	RW	0	<b>Port Address</b>
7:6	RO	0	<b>Port Address</b> 00: Primary master 01: Primary slave 10: Secondary master 11: Reserved
5:0	RO	01h	<b>Fix at 01h</b>

**Offset Address: 2B-28h (B0D15F0) - Reserved**
**Offset Address: 2D-2Ch (B0D15F0)**
**Subsystem Vendor ID**
**Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	<b>Subsystem Vendor ID</b> The read back value can be changed by writing to RxD4-D5.

**Offset Address: 2F-2Eh (B0D15F0)**
**Subsystem ID**
**Default Value: 5372h**

Bit	Attribute	Default	Description
15:0	RO	5372h	<b>Subsystem ID</b> The read back value can be changed by writing to RxD6-D7.

**Offset Address: 33-30h (B0D15F0) - Reserved**
**Offset Address: 34h (B0D15F0)**
**Power Management Capabilities Pointer**
**Default Value: C0h**

Bit	Attribute	Default	Description
7:0	RO	C0h	<b>Power Management Capabilities Pointer</b>

**Offset Address: 3B-35h (B0D15F0) - Reserved**

**Offset Address: 3Ch (B0D15F0)**
**Interrupt Line**
**Default Value: 00h**

Bit	Attribut	Default	Description
7:4	RO	0	<b>Reserved</b>
3:0	RW	0	<b>IDE Interrupt Routing</b> If [7:4] is set to Fh, route to IRQ0. Others are decoded to IRQ0~IRQ15.

**Offset Address: 3Dh (B0D15F0)**
**Interrupt Pin**
**Default Value: 02h**

Bit	Attribute	Default	Description
7:0	RO	02h	<b>Interrupt Routing Mode (INTB# used)</b> Interrupt Routing

**Offset Address: 3F-3Eh (B0D15F0) - Reserved**
**Offset Address: 40h (B0D15F0)**
**SATA Channel Enable**
**Default Value: 03h**

Bit	Attribute	Default	Description
7:4	RO	0	<b>Chip ID</b>
3:2	RO	0	<b>Reserved</b>
1	RW	1b	<b>SATA Primary Channel Enable</b> 0: Disable 1: Enable
0	RW	1b	<b>SATA Secondary Channel Enable</b> 0: Disable 1: Enable

**Offset Address: 41h (B0D15F0)**
**SATA Interrupt Gating**
**Default Value: 13h**

Bit	Attribute	Default	Description
7:2	RO	04h	<b>Reserved</b>
1	RW	1b	<b>SATA I Primary Channel Interrupt Gating</b> Interrupt will be asserted when data are all flushed. 0: Disable 1: Enable
0	RW	1b	<b>SATA I Secondary Channel Interrupt Gating</b> Interrupt will be asserted when data are all flushed. 0: Disable 1: Enable

**Offset Address: 42h (B0D15F0) – Reserved**
**Offset Address: 43h (B0D15F0)**
**FIFO Threshold Control**
**Default Value: 44h**

Bit	Attribute	Default	Description
7	RO	0	<b>Reserved</b>
6:4	RW	100b	<b>Primary Channel Threshold Control</b>
3	RO	0	<b>Reserved</b>
2:0	RW	100b	<b>Secondary Channel Threshold Control</b> <b>FIFO size: 128 DW</b> 000: Zero Threshold 001: 1/8 010: 1/4 011: 3/8 100: 1/2 101: 5/8 110: 3/4 111: 7/8

**Offset Address: 44h (B0D15F0)**
**Miscellaneous Control 1**
**Default Value: 07h**

Bit	Attribute	Default	Description
7	RO	0	<b>Reserved</b>
6	RW	0	<b>Master Read Cycle IRDY# Wait States</b>
5	RW	0	<b>Master Write Cycle IRDY# Wait States</b>
4	RW	0	<b>Wait PHY Ready if Device Detect = 1 When Execute SW Reset</b> 0: Pass this port 1: Wait PHY ready
3	RW	0	<b>Bus Master IDE Status Register Read Retry</b> 0: Disable 1: Enable
2	RW	1b	<b>Change Drive to Clear all FIFO Internal States</b> 0: Disable 1: Enable
1	RW	1b	<b>Split 2 Channel Request</b> 0: Disable 1: Enable
0	RW	1b	<b>Enable / Disable TP Layer Back to Idle When LINK Layer Is Idle</b> 0: Disable 1: Enable

**Offset Address: 45h (B0D15F0)**
**Miscellaneous Control 2**
**Default Value: AFh**

Bit	Attribute	Default	Description
7	RW	1b	<b>Sub Class (Rx0A) Write Protect</b> 0: Rx0A Write Enable 1: Rx0A Write Disable
6	RW	0	<b>Host Clock (33/66) Dynamic Clock Gating</b> 0: Enable 1: Disable
5	RW	1b	<b>Latency Timer</b> 0: Disable 1: Enable Set to 1 only when GNT is deasserted for better performance.
4	RW	0	<b>Interrupt Line (Rx3C) Write Protect</b> 0: Rx3C Write Enable 1: Rx3C Write Disable
3:2	RO	11b	<b>Reserved</b>
1	RW	1b	<b>Primary Channel Read DMA Flush Data After Interrupt</b> 0: Disable 1: Enable
0	RW	1b	<b>Secondary Channel Read DMA Flush Data After Interrupt</b> 0: Disable 1: Enable

**Offset Address: 46h (B0D15F0)**
**Miscellaneous Control 3**
**Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	<b>Reserved</b>
6	RW	0	<b>Transport Dynamic Clock Gating</b> 0: Enable 1: Disable
5:2	RO	0	<b>Reserved</b>
1	RW	0	<b>Improve SATA I PIO Performance</b> 0: On 1: Off
0	RW	0	<b>Mask PCI Bus Input Floating Signal (Vector Mode and Test Only)</b> 0: Disable 1: Enable

**Offset Address: 48h (B0D15F0)**
**PHY Wakeup Request Control**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RO	0	<b>Reserved</b>
5	RW	0	<b>Internal PHY Port 1 Listen Mode</b> 0: Disable 1: Enable
4	RW	0	<b>Internal PHY Port 0 Listen Mode</b> 0: Disable 1: Enable
3	RO	0	<b>Reserved</b>
2	RW	0	<b>Internal PHY Secondary Master Port Wakeup Request</b> It is triggered by the rising edge of each bit written.
1	RO	0	<b>Reserved</b>
0	RW	0	<b>Internal PHY Primary Master Port Wakeup Request</b> It is triggered by the rising edge of each bit written.

**Offset Address: 49h (B0D15F0)**
**Miscellaneous Registers**
**Default Value: 80h**

Bit	Attribute	Default	Description
7	RW	1b	<b>PATA Function</b> 0: Disable (Rx0E[7] will be 0) 1: Enable
6:2	RO	0	<b>Reserved</b>
1	RW	0	<b>Support Port Multiplier Function</b> 0: Disable 1: Enable
0	RO	0	<b>Reserved</b>

**Offset Address: 4B-4Ah (B0D15F0) - Reserved**
**Offset Address: 4Ch (B0D15F0)**
**Step Bus Master Control**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RO	0	<b>Reserved</b>
5	RO	0	<b>Secondary Channel Step Bus Master Busy</b>
4:2	RO	0	<b>Reserved</b>
1	RW	0	<b>Trigger Secondary Channel Start Bus Master Cycle</b> When it change from 0 to 1 and Rx4C[3] = 1, bus master will issue N bus master cycles to VLINK N: Rx4D[7:5]
0	RW	0	<b>Trigger Primary Channel Start Bus Master Cycle</b> When it change from 0 to 1 and Rx4C[3] = 1, bus master will issue N bus master cycles to VLINK N: Rx4D[7:5]

**Offset Address: 4Dh (B0D15F0)**
**Bus Master Control**
**Default Value: 80h**

Bit	Attribute	Default	Description
7:5	RW	100b	<b>Pipeline Level</b> Bus master cycle pipeline level, value 1 ~ 4 can be programmed, other are reserved When step mode enable, it is trigger amounts for each trigger.
4:3	RO	0	<b>Reserved</b>
2	RW	0	<b>ADS Merge</b> 0: Issue ADS if FIFO ready 1: Merge 2 ADS if FIFO ready
1	RW	0	<b>Only 4 QW Requirement</b> 0: Bus Master cycle will be 4QW or 8QW length for each ADS 1: Bus Master cycle only be 4QW length for each ADS
0	RW	0	<b>Aggressive Bus Master Cycle Request</b> 0: Start bus master cycle when FIFO threshold (Rx43) hit 1: Start bus master cycle when Data ready

**Offset Address: 4Eh (B0D15F0)**
**SATA I Debugging Signals Output Control 1**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RO	0	<b>Reserved</b>
5	RW	0	<b>Enable Secondary Master Port PHY Error Status (2) Output to PDDREQ Pin</b>
4	RW	0	<b>Enable Secondary Master Port PHY Error Status (1) Output to PDDREQ Pin</b>
3:2	RO	0	<b>Reserved</b>
1	RW	0	<b>Enable Primary Master Port PHY Error Status (2) Output to PDDREQ Pin</b>
0	RW	0	<b>Enable Primary Master Port PHY Error Status (1) Output to PDDREQ Pin</b>

Error status (1): (a) 10 bit to 8 bit error or (b) crc error or (c) disparity error or (d) handshake error

Error status (2): (a) link sequence error or (b) FIS type error or (c) transport port state transmission error

**Offset Address: 4Fh (B0D15F0)**
**SATA I Debugging Signals Output Control 2**
**Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	<b>Output BIST Error Signal to PDDREQ Pin</b>
6	RW	0	<b>Output Device Mode Error Signal to Output Pin (PDDREQ, Test Only)</b>
5:1	RO	0	<b>Reserved</b>
0	RW	0	<b>Enable Error Signal Output to PDDREQ Pin</b>

SATA Transport Control Registers (50-53h)
Offset Address: 50h (B0D15F0)
Software Controllable Power Mode Request
**Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RO	0	<b>Reserved</b>
5	RW	0	<b>Internal PHY Secondary Master Port SLUMBER Request</b>
4	RW	0	<b>Internal PHY Secondary Master Port PARTIAL Request</b>
3:2	RO	0	<b>Reserved</b>
1	RW	0	<b>Internal PHY Primary Master Port SLUMBER Request</b>
0	RW	0	<b>Internal PHY Primary Master Port PARTIAL Request</b>

Note: The internal request is triggered by the rising edge of each bit.

Offset Address: 51h (B0D15F0)
Hardware Controllable Power Mode
**Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	<b>Change Drive &amp; Let Idle Device Enter Power Mode</b> 0: Disable 1: Enable
6	RW	0	<b>Change Drive Power Mode Selection for Idle Device</b> 0: Partial 1: Slumber
5	RO	0	<b>Reserved</b>
4	RW	0	<b>Enter to Partial Process (Item1) Disabled</b> 0: Enable 1: Disable
3	RW	0	<b>Enter to Slumber Process (Item2) Disabled</b> 0: Enable 1: Disable
2:0	RW	0	<b>Power Clock Select</b> 000 T = 1t 001 T = 2t ..... 1.Power Mode Control Process: Partial will be requested if transport idle for at least 2T. 2.Slumber will be requested if transport layer idle for at least 10 T. (t = 0.425s) 3. 111 only for test, it shouldn't be programmed

Offset Address: 52h (B0D15F0)
Transport Miscellaneous Control
**Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	<b>Reserved</b>
6	RW	0	<b>Transport Issues Early Request to Link for Better Performance</b>
5	RO	0	<b>Reserved</b>
4	RW	0	<b>Signal Data FIS (Frame Information Structure) Transmission</b> Allow over 8K bytes.
3	RW	0	<b>BIST FIS</b> Controller can accept BIST FIS when behaves as a device (Rx53[1:0] are set). This bit is set only for controller to control BIST FIS self-test.
2	RW	0	<b>SATA Flow Control Water Flag</b> 0: 52DW 1: 40DW
1:0	RO	0	<b>Reserved</b>

**Offset Address: 53h (B0D15F0)**
**Device Mode Testing Register**
**Default Value: 00h**

Bit	Attribute	Default	Description
7	WO/RO	0	<b>Trigger Secondary Channel Device Mode</b> Write “1” to trigger device mode memory read based on the address specified in Rx93 - 90 Read value indicates memory read cycle is busy now
6	WO/RO	0	<b>Trigger Primary Channel Device Mode</b> Write “1” to trigger device mode memory read based on the address specified in Rx93 - 90 Read value indicates memory read cycle is busy now
5	RO	0	<b>Secondary Channel CRC Error Status</b>
4	RO	0	<b>Primary Channel CRC Error Status</b>
3	RW	0	<b>Secondary Channel Device Mode Simulation Continues When Handshake Error Occurs</b> (but always stop at CRC error)
2	RW	0	<b>Primary Channel Device Mode Simulation Continues When Handshake Error Occurs</b> (but always stop at CRC error)
1	RW	0	<b>Set Secondary Channel as Device Controller</b>
0	RW	0	<b>Set Primary Channel as Device Controller</b>

**SATA Link Control Registers (54-56h)**
**Offset Address: 55-54h (B0D15F0) - Reserved**
**Offset Address: 56h (B0D15F0)**
**SATA Link Control 3**
**Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	<b>Waiting Device SYNC Primitive After Wake Up from Power Mode</b> 0: Disable 1: Enable
6	RO	0	<b>Reserved</b>
5	RW	0	<b>Receive Scrambler</b> 0: Enable 1: Disable
4	RW	0	<b>Transmit Scrambler</b> 0: Enable 1: Disable
3	RW	0	<b>Align Primitive Transmission</b> 0: Enable 1: Disable
2	RW	0	<b>Continue Primitive Transmission</b> 0: Enable 1: Disable
1	RW	0	<b>Continue Primitive After Align</b> 0: Enable 1: Disable
0	RW	0	<b>SATA Link Dynamic Clock Gating</b> 0: Enable 1: Disable

### SATA PHY Control Registers (57-63h)

#### Offset Address: 57h (B0D15F0)

##### PHY Control Register 1

Default Value: 00h

Bit	Attribute	Default	Description
7:2	RO	0	<b>Reserved</b>
1:0	RW	0	<b>Data Pattern Select</b> PHY test mode data pattern select

#### Offset Address: 58h (B0D15F0)

##### PHY Test Mode Control

Default Value: 00h

Bit	Attribute	Default	Description
7	RW	0	<b>Test Gen2 or Gen1 Select</b> 0: Gen1 1: Gen2
6	RO	0	<b>Reserved</b>
5	RW	0	<b>Test Port Select</b>
4	RW	0	<b>PHY Test Mode Enable</b>
3:0	RW	0	<b>PHY Test Mode Type Select</b>

#### Offset Address: 5Ah (B0D15F0)

##### PHY Test Mode

Default Value: 80h

Bit	Attribute	Default	Description
7	RW	1b	<b>Support Asynchronous Recovery Function</b>
6	RW	0	<b>Testing Autocor for 50ohm Termination Resistance</b> 0: Disable 1: Enable
5	RW	0	<b>Extend OOB Burst Length</b> 0: Disable 1: Enable
4	RO	0	<b>Reserved</b>
3	RW	0	<b>Enable PLL Test (Output 300MHz Clock)</b>
2	RW	0	<b>Test Data Output to Pin Enable</b>
1	RW	0	<b>Data Output to Pin Selection</b> 0: 10 bit 1: 8 bit
0	RW	0	<b>Test 8b Data Output Direction</b> 0: RX 1: TX

#### Offset Address: 5Bh (B0D15F0)

##### PHY Test Mode Status

Default Value: 00h

Bit	Attribute	Default	Description
7:4	RO	0	<b>Reserved</b>
3	RO	0	<b>PHY Detect Squelch</b>
2	RO	0	<b>PHY Receive COMWAKE</b>
1	RO	0	<b>PHY Receive COMINIT</b>
0	RO	0	<b>PHY Direct Access Check Error</b>

**Offset Address: 5Ch (B0D15F0)**
**PHY Control Register 1**
**Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	<b>Bypass Oscillator</b>
6	RW	0	<b>OSC Latch Up Test Control</b>
5	RW	0	<b>SATA PHY Dynamic Cock Gating</b> 0: Enable                    1: Disable
4	RW	0	<b>Double (6 to 12) OOB Burst Number</b> 1: Double
3:2	RO	0	<b>Reserved</b>
1:0	RW	0	<b>Disable Port {1,0}</b>

**Offset Address: 5Eh (B0D15F0)**
**PHY Control Register 3**
**Default Value: 20h**

Bit	Attribute	Default	Description
7	RW	0	<b>SATA PHY 150MHz Dynamic Clock Gating</b> 0: Enable                    1: Disable
6	RW	0	<b>Select CDR Regulator Reset Source</b>
5	RW	1b	<b>When Cdr Disperses, Re-assign Phase-mode and Cdr Reset Signals</b> 0: Disable                    1: Enable
4	RW	0	<b>Ixx,fix in GenII Retry 3<sup>rd</sup> Times Before Reduce Speed</b>
3	RO	0	<b>Reserved</b>
2	RW	0	<b>Ignore the Squelch Signal After PHYRDY</b> 0: Disable                    1: Enable
1	RW	0	<b>Reduce Speed When Unsolicited COMINIT</b> 0: Reduce to Gen I            1: Keep at Gen II
0	RW	0	<b>Force Host Always in Gen2 Speed</b> 0: Disable                    1: Enable

**Offset Address: 5Fh (B0D15F0)**
**Hot Plug Status**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW1C	0	<b>Reserved</b>
5	RW1C	0	<b>Secondary Channel Master Plug Out Status</b>
4	RW1C	0	<b>Secondary Channel Master Plug In Status</b>
3:2	RW1C	0	<b>Reserved</b>
1	RW1C	0	<b>Primary Channel Master Plug Out Status</b>
0	RW1C	0	<b>Primary Channel Master Plug In Status</b>

**Offset Address: 60h (B0D15F0)**
**SATA I RAM BIST**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RO	0	<b>Reserved</b>
5	RO	0	<b>Secondary RAM BIST Error Status</b>
4	WO/RO	0	<b>Trigger Secondary RAM BIST / Busy Status of RAM BIST</b>
3:2	RO	0	<b>Reserved</b>
1	RO	0	<b>Primary RAM BIST Error Status</b>
0	WO/RO	0	<b>Trigger Primary RAM BIST / Busy Status of RAM BIST</b>

**Offset Address: 63-61h (B0D15F0) - Reserved**

### Analog PHY Control (64-77h)

#### Offset Address: 64h (B0D15F0)

##### Analog PHY (AFE) Control Register 1

Default Value: 0Ch

Bit	Attribute	Default	Description
7	RW	0	Serial Data Loopback from PISO to CDR
6	RW	0	CDR Bandwidth Select Bit 1 – Gen1
5	RW	0	CDR Bandwidth Select Bit 0 – Gen1
4	RW	0	Squelch Window Select Bit 1 – Gen1
3	RW	1b	Squelch Window Select Bit 0 – Gen1
2	RW	1b	Options for CDR Charge Pump Bit 2 – Gen1
1	RW	0	Options for CDR Charge Pump Bit 1 – Gen1
0	RW	0	Options for CDR Charge pump Bit 0 – Gen1

#### Offset Address: 65h (B0D15F0)

##### AFE Control Register 2

Default Value: CBh

Bit	Attribute	Default	Description
7:4	RO	Ch	Reserved (Do Not Program)
3	RW	1b	Port 0,1 Control for Driver Current Source Bit 3 – Gen1
2	RW	0	Port 0,1 Control for Driver Current Source Bit 2 – Gen1
1	RW	1b	Port 0,1 Control for Driver Current Source Bit 1 – Gen1
0	RW	1b	Port 0,1 Control for Driver Current Source Bit 0 – Gen1

#### Offset Address: 66h (B0D15F0) - Reserved

#### Offset Address: 67h (B0D15F0)

##### AFE Control Register 4

Default Value: 60h

Bit	Attribute	Default	Description
7:4	RO	6h	Reserved (Do Not Program)
3	RW	0	Port 0,1 Control for Pre / De-emphasis Level Bit 3 – Gen1
2	RW	0	Port 0,1 Control for Pre / De-emphasis Level Bit 2 – Gen1
1	RW	0	Port 0,1 Control for Pre / De-emphasis Level Bit 1 – Gen1
0	RW	0	Port 0,1 Control for Pre / De-emphasis Level Bit 0 – Gen1

#### Offset Address: 68h (B0D15F0) - Reserved

#### Offset Address: 69h (B0D15F0)

##### AFE Control Register 6

Default Value: 00h

Bit	Attribute	Default	Description
7	RW	0	Supports External Interconnect Box-to-Box / Long-Haul (Gen1x or Gen2x Support) 0: Disable 1: Enable
6:4	RO	0	Reserved
3	RW	0	Gen1 Port 0 Enable Pre / De-emphasis
2	RW	0	Gen1 Port 1 Enable Pre / De-emphasis
1:0	RO	0	Reserved

**Offset Address: 6Ah (B0D15F0)**
**AFE Control Register 7**
**Default Value: 02h**

Bit	Attribute	Default	Description
7:4	RO	0	<b>Reserved</b>
3	RW	0	<b>Mode Select</b> 0: Auto Mode 1: Manual Mode
2	RW	0	<b>Manual Setting – 50-ohm Termination Bit 2</b>
1	RW	1b	<b>Manual Setting – 50-ohm Termination Bit 1</b>
0	RW	0	<b>Manual Setting – 50-ohm Termination Bit 0</b>

**Offset Address: 6Bh (B0D15F0)**
**AFE Control Register 8**
**Default Value: 0Ah**

Bit	Attribute	Default	Description
7:4	RO	0	<b>Reserved</b>
3	RO	1b	<b>Autocomp Value</b>
2	RO	0	<b>Autocomp Values of Termination Bit 2</b>
1	RO	1b	<b>Autocomp Values of Termination Bit 1</b>
0	RO	0	<b>Autocomp Values of Termination Bit 0</b>

**Offset Address: 6Ch (B0D15F0)**
**AFE Control Register 9**
**Default Value: 44h**

Bit	Attribute	Default	Description
7	RW	0	<b>Duty-Balance Control Rising Time for Serial Data Port 0 Bit 1</b>
6	RW	1b	<b>Duty-Balance Control Rising Time for Serial Data Port 0 Bit 0</b>
5	RW	0	<b>Duty-Balance Control Falling Time for Serial Data Port 0 Bit 1</b>
4	RW	0	<b>Duty-Balance Control Falling Time for Serial Data Port 0 Bit 0</b>
3	RW	0	<b>Duty-Balance Control Rising Time for Serial Data Port 1 Bit 1</b>
2	RW	1b	<b>Duty-Balance Control Rising Time for Serial Data Port 1 Bit 0</b>
1	RW	0	<b>Duty-Balance Control Falling Time for Serial Data Port 1 Bit 1</b>
0	RW	0	<b>Duty-Balance Control Falling Time for Serial Data Port 1 Bit 0</b>

**Offset Address: 6Dh (B0D15F0) - Reserved**
**Offset Address: 6Eh (B0D15F0)**
**AFE Control Register 11**
**Default Value: 51h**

Bit	Attribute	Default	Description
7	RW	0	<b>Port Control for Driver Current Source Bit 3 – Gen2</b>
6	RW	1b	<b>Port Control for Driver Current Source Bit 2 – Gen2</b>
5	RW	0	<b>Port Control for Driver Current Source Bit 1 – Gen2</b>
4	RW	1b	<b>Port Control for Driver Current Source Bit 0 – Gen2</b>
3	RW	0	<b>Port Control for Pre / De-emphasis Level Bit 1 - Gen2</b>
2	RW	0	<b>Port Control for Pre / De-emphasis Level Bit 0 - Gen2</b>
1	RW	0	<b>Squelch Window Select Bit 1 – Gen2</b>
0	RW	1b	<b>Squelch Window Select Bit 0 – Gen2</b>

**Offset Address: 6Fh (B0D15F0)**
**AFE Control Register 12**
**Default Value: 04h**

Bit	Attribute	Default	Description
7	RW	0	<b>Port Control for Pre / De-emphasis Level Bit 3 - Gen2</b>
6	RW	0	<b>Port Control for Pre / De-emphasis Level Bit 2 - Gen2</b>
5	RW	0	<b>CDR Bandwidth Select Bit 1 - Gen2</b>
4	RW	0	<b>CDR Bandwidth Select Bit 0 - Gen2</b>
3	RO	0	<b>Reserved</b>
2	RW	1b	<b>Options for CDR Charge Pump Bit 2 - Gen2</b>
1	RW	0	<b>Options for CDR Charge Pump Bit 1 - Gen2</b>
0	RW	0	<b>Options for CDR Charge Pump Bit 0 - Gen2</b>

**Offset Address: 70h (B0D15F0)**
**AFE Control Register 13**
**Default Value: 46h**

Bit	Attribute	Default	Description
7	RW	0	<b>NO SATA</b> 0: SATA used 1: SATA no used Set this bit when SATA doesn't used, it will assert all reset for SATA PHY but configuration cycle still can be accessed.
6	RW	1b	<b>COMRESET Fix 6 Burst</b> 0: COMRESET burst terminated when receive COMINIT 1: COMRESET keep 6 burst
5:4	RO	0	<b>Reserved</b>
3	RW	0	<b>Squelch Detect Test Circuit Reset</b> 0: Assert reset for Detect Test Circuit 1: De-assert reset for Detect Test Circuit (start detect)
2	RW	1b	<b>Enable Asynchronous Recovery Time Out Counter</b> 0: Asynchronous Recovery continue even though no Device 1: Asynchronous Recovery stop when repeat 5 times and no Device
1	RO	1b	<b>Reserved (Do Not Program)</b>
0	RW	0	<b>Enable Reset SATA OSC</b> 0: Not reset SATA OSC 1: Reset SATA OSC with current source reset

**Offset Address: 71h (B0D15F0) - Reserved**

**Offset Address: 72h (B0D15F0)**
**AFE Control Register 14**
**Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	<b>Function Test Mode (Test Only)</b> 0: Normal operation mode 1: Function test mode
6:2	RO	0	<b>Reserved</b>
1	RW	0	<b>Change Testing Disparity</b> 0: Rd- 1: Rd+
0	RW	0	<b>Test Long or Short Pattern in Composite Mode</b> 0: Short pattern 1: Long pattern

**Offset Address: 73h (B0D15F0)**
**AFE Control Register 15**
**Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	<b>SATA Receiver Sensitivity and Jitter Mode (Test Only)</b> 0: Disable 1: Enable
6	RW	0	<b>Start to Test Receiver Sensitivity and Jitter Mode (Test Only)</b>
5	RW	0	<b>Select 10-bit Data to Test Output Pins from SIPO or WALIGN</b> 0: WALIGN 1: SIPO
4	RO	0	<b>Check Error Status</b>
3:0	RO	0	<b>Error Times Report</b>

**Offset Address: 74h (B0D15F0)**
**AFE Control Register 16**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:2	RO	0	<b>Reserved</b>
1:0	RO	0	<b>CDR Disperse Status of Port {1, 0 }</b>

**Offset Address: 75h (B0D15F0)**
**AFE Control Register 17**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RO	0	<b>Reserved</b>
2:0	RO	0	<b>Select Debug Signals to IDE PAD (16 Bits)</b> 0h: Disable output 1h: TRxLocked, TAfePhase, TSquelch, TGen2_en, TCdrReset, TpinData 2h: LK_CurrState, PHY_CurrState 3h: LK_StopClk, StopClk150M 4h: TSquelch for ATE test squelch window Others: Reserved

**Offset Address: 76h (B0D15F0)**
**AFE Control Register 18**
**Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	Select Align Primitive have 2 or 4 than phyrdy Asserted in GenII Mode (test) 0: 4-primitive
6	RW	0	Select Retry Cdr Method 0: Select 750DW(GenII) or 940DW(GenI) retry    1: Frequency detect retry
5:2	RO	0	<b>Reserved</b>
1:0	RW	0	<b>Retry When Cdr Disperse</b> 00: Not retry Cdr in GenII and GenI 01: Retry Cdr in GenI 10: Retry Cdr in GenII 11: Retry Cdr in GenII and GenI

**Offset Address: 77h (B0D15F0) - Reserved**
**Misc. Registers (78-8Fh)**
**Offset Address: 78h (B0D15F0)**
**SATA I Primary Channel Transport Status 1**
**Default Value: 01h**

Bit	Attribute	Default	Description
7:5	RO	0	<b>Reserved</b>
4	RO	0	<b>Primary Channel DMA Read Device Cycle Active</b>
3	RO	0	<b>Primary Channel DMA Write Device Cycle Active</b>
2	RO	0	<b>Primary Channel SG Operation Active</b>
1	RO	0	<b>Primary Channel Interrupt Status</b>
0	RO	1b	<b>Primary Channel FIFO Empty Status</b>

**Offset Address: 79h (B0D15F0)**
**SATA I Primary Channel Transport Status 2**
**Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	<b>Primary Channel PMP Error Status</b>
6:5	RO	0	<b>Reserved</b>
4	RO	0	<b>Primary Channel Slave Drive Select</b>
3	RO	0	<b>Transmit PIO Data Cycle Active</b>
2	RO	0	<b>Receive PIO Data Cycle Active</b>
1	RO	0	<b>Transmit DMA Data Cycle Active</b>
0	RO	0	<b>Receive DMA Data Cycle Active</b>

**Offset Address: 7Ah (B0D15F0)**
**SATA I Secondary Channel Transport Status 1**
**Default Value: 01h**

Bit	Attribute	Default	Description
7:5	RO	0	<b>Reserved</b>
4	RO	0	<b>Secondary Channel DMA Read Device Cycle Active</b>
3	RO	0	<b>Secondary Channel DMA Write Device Cycle Active</b>
2	RO	0	<b>Secondary Channel SG Operation Active</b>
1	RO	0	<b>Secondary Channel Interrupt Status</b>
0	RO	1b	<b>Secondary Channel FIFO Empty Status</b>

**Offset Address: 7Bh (B0D15F0)**
**SATA I Secondary Channel Transport Status 2**
**Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	Secondary Channel PMP Error Status
6:5	RO	0	Reserved
4	RO	0	Primary Channel Slave Drive Select
3	RO	0	Transmit PIO Data Cycle Active
2	RO	0	Receive PIO Data Cycle Active
1	RO	0	Transmit DMA Data Cycle Active
0	RO	0	Receive DMA Data Cycle Active

**Offset Address: 7F-7Ch (B0D15F0) - Reserved**
**Offset Address: 80h (B0D15F0)**
**Port Select**
**Default Value: 40h**

Bit	Attribute	Default	Description
7:1	RO	20h	Reserved
0	RW	0	Port Select for (1) Parsing FIS Number When in Device Mode 0: Port 0                                   1: Port 1

**Offset Address: 82-81h (B0D15F0) – Reserved**
**Offset Address: 83h (B0D15F0)**
**Other Control**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RO	0	Reserved
5	RW	0	Staggered Spin-Up Port 1 if Rx83[3] is 0. 0: Wait state                                   1: Start OOB sequence
4	RW	0	Staggered Spin-Up Port 0 if Rx83[3] is 0. 0: Wait state                                   1: Start OOB sequence
3	RO	0	Staggered Spin-Up Support Status 0: Support                                   1: No support
2:0	RO	0	Reserved

**Offset Address: 87-84h (B0D15F0) - Reserved**
**Offset Address: 88h (B0D15F0)**
**Primary Channel PMP field**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	Reserved
3:0	RW	0	Primary Channel Master PMP Field It only valid when Rx80[6] = 1

**Offset Address: 89h (B0D15F0)**
**Secondary Channel PMP field**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	Reserved
3:0	RW	0	Secondary Channel Master PMP Field It only valid when Rx80[6] = 1

**Offset Address: 9F-8Ah (B0D15F0) – Reserved**

**SATA I SCR Registers (A0-BFh)**
**Offset Address: A0h (B0D15F0)**

Primary Channel Master Device Status (Sstatus)

Default Value: 00h

Bit	Attribute	Default	Description
7:5	RO	0	<b>Reserved</b>
4	RO	0	<b>SATA Generation II (3G) Status</b>
3	RO	0	<b>SLUMBER Interface Power Management State</b>
2	RO	0	<b>PARTIAL Interface Power Management State</b>
1	RO	0	<b>PHY Ready Status</b>
0	RO	0	<b>Device Detection Status</b>

**Offset Address: A1h (B0D15F0) - Reserved**
**Offset Address: A2h (B0D15F0)**

Secondary Channel Master Device Status (Sstatus)

Default Value: 00h

Bit	Attribute	Default	Description
7:5	RO	0	<b>Reserved</b>
4	RO	0	<b>SATA Generation II (3G) Status</b>
3	RO	0	<b>SLUMBER Interface Power Management State</b>
2	RO	0	<b>PARTIAL Interface Power Management State</b>
1	RO	0	<b>PHY Ready Status</b>
0	RO	0	<b>Device Detection Status</b>

**Offset Address: A3h (B0D15F0) - Reserved**
**Offset Address: A4h (B0D15F0)**

Primary Channel Master Device Control (Scontrol)

Default Value: 0Ch

Bit	Attribute	Default	Description
7:4	RO	0	<b>Reserved</b>
3	RW	1b	<b>Transition to SLUMBER Power Management State Disabled</b>
2	RW	1b	<b>Transition to PARTIAL Power Management State Disabled</b>
1	RW	0	<b>Disable SATA Interface And Put PHY In Offline Mode</b>
0	RW	0	<b>Perform SATA Interface Communication Initialization Sequence to Establish Communication</b>

Note: This register is only valid when Rx80[6] = 1

**Offset Address: A5h (B0D15F0) - Reserved**
**Offset Address: A6h (B0D15F0)**

Secondary Channel Master Device Control (Scontrol)

Default Value: 0Ch

Bit	Attribute	Default	Description
7:4	RO	0	<b>Reserved</b>
3	RW	1b	<b>Transition to SLUMBER Power Management State Disabled</b>
2	RW	1b	<b>Transition to PARTIAL Power Management State Disabled</b>
1	RW	0	<b>Disable SATA Interface And Put PHY In Offline Mode</b>
0	RW	0	<b>Perform SATA Interface Communication Initialization Sequence to Establish Communication</b>

Note: This register is only valid when Rx80[6] = 1

**Offset Address: AF-A7h (B0D15F0) - Reserved**
**Offset Address: B3-B0h (B0D15F0)**
**Primary Channel Master SCR Error**
**Default Value: 0002 0000h**

Bit	Attribute	Default	Description
31:28	RO	0	<b>Reserved</b>
27	RW1C	0	<b>Port Selector Presence Detected</b>
26	RW1C	0	<b>Exchanged</b>
25	RW1C	0	<b>Unrecognized FIS Type</b>
24	RW1C	0	<b>Transport State Transition Error</b>
23	RW1C	0	<b>Link Sequence Error</b>
22	RW1C	0	<b>Handshake Error</b>
21	RW1C	0	<b>CRC Error</b>
20	RW1C	0	<b>Disparity Error</b>
19	RW1C	0	<b>10B to 8B Decode Error</b>
18	RW1C	0	<b>COMWAKE Detected</b>
17	RW1C	1b	<b>PHY Internal Error</b>
16	RW1C	0	<b>PhyRdy Change</b> ERR: Contains error information for use by host software in determining the appropriate response to the error condition.
15:12	RO	0	<b>Reserved</b>
11	RW1C	0	<b>Internal Error</b>
10	RW1C	0	<b>Protocol Error</b>
9	RW1C	0	<b>Non-recovered Persistent Communication or Data Integrity Error</b>
8	RW1C	0	<b>Non-recovered Transient Data Integrity Error</b>
7:2	RO	0	<b>Reserved</b>
1	RW1C	0	<b>Recovered Communications Error</b>
0	RW1C	0	<b>Recovered Data Integrity Error</b>

**Offset Address: B7-B4h (B0D15F0) - Reserved**
**Offset Address: BB-B8h (B0D15F0)**
**Secondary Channel Master SCR Error**
**Default Value: 0002 0000h**

Bit	Attribute	Default	Description
31:28	RO	0	<b>Reserved</b>
27	RW1C	0	<b>Port Selector Presence Detected</b>
26	RW1C	0	<b>Exchanged</b>
25	RW1C	0	<b>Unrecognized FIS Type</b>
24	RW1C	0	<b>Transport State Transition Error</b>
23	RW1C	0	<b>Link Sequence Error</b>
22	RW1C	0	<b>Handshake Error</b>
21	RW1C	0	<b>CRC Error</b>
20	RW1C	0	<b>Disparity Error</b>
19	RW1C	0	<b>10B to 8B Decode Error</b>
18	RW1C	0	<b>COMWAKE Detected</b>
17	RW1C	1b	<b>PHY Internal Error</b>
16	RW1C	0	<b>PhyRdy Change</b> ERR: Contains error information for use by host software in determining the appropriate response to the error condition.
15:12	RO	0	<b>Reserved</b>
11	RW1C	0	<b>Internal Error</b>
10	RW1C	0	<b>Protocol Error</b>
9	RW1C	0	<b>Non-recovered Persistent Communication or Data Integrity Error</b>
8	RW1C	0	<b>Non-recovered Transient Data Integrity Error</b>
7:2	RO	0	<b>Reserved</b>
1	RW1C	0	<b>Recovered Communications Error</b>
0	RW1C	0	<b>Recovered Data Integrity Error</b>

**Offset Address: BF-BCh (B0D15F0) - Reserved**

**Legacy Registers (C0-EBh)**
**Offset Address: C3-C0h (B0D15F0)**
**PCI Power Management Control and Status**
**Default Value: 0001 0002h**

Bit	Attribute	Default	Description
31:16	RO	0001h	<b>PCI Power Management Indication</b> Indicates that this pointer is a PCI power management.
15:0	RO	0002h	<b>PCI Power Management Interface Specification</b> Version.02 indicates that this function compiles with Revision 1.1 of PCI Power Management Interface Spec.

**Offset Address: C5-C4h (B0D15F0)**
**Power State**
**Default Value: 0000h**

Bit	Attribute	Default	Description
15:2	RO	0	<b>Reserved</b>
1:0	RW	00b	<b>Power State</b> 00b: D0 11b: D3 hot

**Offset Address: D0-C6h (B0D15F0) - Reserved**
**Offset Address: D1h (B0D15F0)**
**PATA Enable Method**
**Default Value: 02h**

Bit	Attribute	Default	Description
7:4	RO	0	<b>Reserved</b>
3	RW	0	<b>PATA Enable Method</b> 0: PATA will be enabled with Rx49[7] = 1 1: PATA will be enabled with Rx49[7] = 1 and SATA function enabled
2:0	RO	010b	<b>Reserved</b> (Do Not Program)

**Offset Address: D3-D2h (B0D15F0)**
**IDE Mode Device ID**
**Default Value: 5372h**

Bit	Attribute	Default	Description
15:0	RW	5372h	<b>IDE Mode Device ID Back Door Register</b>

**Offset Address: D5-D4h (B0D15F0)**
**Subsystem Vendor ID Back Door Registers**
**Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RW	1106h	<b>Back Door of Sub-vender ID</b>

**Offset Address: D7-D6h (B0D15F0)**
**Subsystem ID Back Door Registers**
**Default Value: 5372h**

Bit	Attribute	Default	Description
15:0	RW	5372h	<b>Back Door of Sub-system ID</b>

**Offset Address: D9-D8h (B0D15F0) - Reserved**
**Offset Address: DB-DAh (B0D15F0)**
**RAID Mode Device ID**
**Default Value: 7372h**

Bit	Attribute	Default	Description
15:0	RW	7372h	<b>RAID Mode Device ID Back Door Register</b>

**Offset Address: EB-DCh (B0D15F0) - Reserved**

### SATA Status, Error and Control Registers (0-8Bh)

#### SATA Status

**Default Value: 0000 0000h**

**SCR Offset Address 3-0h: Primary Master**

**SCR Offset Address 83-80h: Secondary Master**

Bit	Attribute	Default	Description
31:12	RO	0	<b>Fixed at 0</b>
11:8	RO	0	<b>IPM Status</b> IPM indicates current Interface Power Management 0000: Device is not present or communication is not established 0001: Interface is in active state 0010: Interface is in PARTIAL power management state 0110: Interface is in SLUMBER power management state All other values reserved
7:4	RO	0	<b>SPD Status</b> SPD indicates the Negotiated Interface Communication Speed Established 0000: No negotiated speed (device is not present or communication is not established) 0001: Negotiate in Generation 1 communication rate All other values reserved
3:0	RO	0	<b>Interface Device Detection and PHY State</b> 0000: No device is detected and PHY communication is not established 0001: Device presence detected but PHY communication is not established 0011: Device presence detected and PHY communication is established 0100: PHY in offline mode as a result of the interface is disabled or running in a BIST loopback mode All other values reserved

#### SATA Error

**Default Value: 0000 0000h**

**SCR Offset Address 7-4h: Primary Master**

**SCR Offset Address 87-84h: Secondary Master**

Conveys supplemental interface error information to complement the error information available in the Shadow Register Block Error register.

Bit	Attribute	Default	Description
31:28	RO	0	<b>Reserved</b>
27	RW1C	0	<b>Port Selector Presence Detected</b>
26	RW1C	0	<b>Exchanged</b>
25	RW1C	0	<b>Unrecognized FIS Type</b>
24	RW1C	0	<b>Transport State Transition Error</b>
23	RW1C	0	<b>Link Sequence Error</b>
22	RW1C	0	<b>Hand Shake Error</b>
21	RW1C	0	<b>CRC Error</b>
20	RW1C	0	<b>Disparity Error</b>
19	RW1C	0	<b>10B to 8B Decode Error</b>
18	RW1C	0	<b>Comm Wake Detected</b>
17	RW1C	0	<b>PHY Internal Error</b>
16	RW1C	0	<b>PhyRdy Change</b>
15:12	RO	0	<b>Reserved</b>
11	RW1C	0	<b>Internal Error</b>
10	RW1C	0	<b>Protocol Error</b>
9	RW1C	0	<b>Non-recovered Persistent Communication or Data Integrity Error</b>
8	RW1C	0	<b>Non-recovered Transient Data Integrity Error</b>
7:2	RO	0	<b>Reserved</b>
1	RW1C	0	<b>Recovered Communications Error</b>
0	RW1C	0	<b>Recovered Data Integrity Error</b>

**SATA Control**
**Default Value: 0000 0320h**
**SCR Offset Address 0B-8h: Primary Master**
**SCR Offset Address 8B-88h: Secondary Master**

Bit	Attribute	Default	Description
31:20	RO	0	<b>Fixed at 0</b>
19:16	RW	0	<b>PMP Control</b> The Port Multiplier Port (PMP) field represents the 4-bits value to be placed in the PMP field of all transmitted FISes. This field is “0000” upon power-up. This field is optional and an HBA implementation may choose to ignore this field if the FIS to be transmitted is constructed via an alternative method.
15:12	W1	0	<b>SPM Control</b> The SPM field represent is used to select a power management state 0001b: transition to the Partial power management state initiated. 0010b: transition to the Slumber power management state initiated. 0100b: transition to the Active power management state initiated. This field be read as 0000b
11:8	RW	0011b	<b>IPM Control</b> The IPM field represents the enabled interface power management states that can be invoked via the Serial ATA interface power management capabilities 0000b: No interface power management state restrictions. 0001b: Transitions to the PARTIAL power management state is disabled. 0010b: Transitions to the SLUMBER power management state is disabled. 0011b: Transitions to both the PARTIAL and SLUMBER power management states are disabled. All other values reserved
7:4	RW	0010b	<b>SPD Control</b> The SPD field represents the highest communication speed that the interface is permitted to negotiate when interface communication speed is established 0000b: No speed negotiation restrictions 0001b: Limit speed negotiation to a rate not greater than Generation 1 communication rate 0010b: Limit speed negotiation to a rate not greater than Generation II communication rate All other values reserved
3:0	RW	0	<b>DET Control</b> The DET field controls the host after device detection and interface initialization. 0000b: No device detection or initialization action requested 0001b: Performs interface communication initialization sequence to establish communication 0100: Disable the Serial ATA interface and put PHY in offline mode All other values reserved

Note: This register is only valid when Rx80[6] = 0

**SATA Notification**
**Default Value: 0000 0000h**
**SCR Offset Address 13-10h: Primary Master**
**SCR Offset Address 93-90h: Secondary Master**

Bit	Attribute	Default	Description
31:16	RO	0	<b>Fixed at 0</b>
15:0	W1C	0	<b>Notify</b> It indicate which port after Port Multiplier need be serviced when related bit = 1. Bit 0 – Port 0 after Port Multiplier need be serviced Bit 1 – Port 1 after Port Multiplier need be serviced .. Bit 15 – Port 15 after Port Multiplier need be serviced Related bit can be clear by writing ‘1’

## **Bus 0 Device 15 Function 1 (B0D15F1) – Enhanced IDE Controller**

The Enhanced IDE (Parallel ATA) Controller interface is fully compatible with the SFF 8038i v1.0 specification. There are two sets of software accessible registers -- PCI configuration registers and Bus Master IDE I/O registers. The PCI configuration registers are located in the Bus 0 Device 15 Function 1 PCI configuration space of the VT8237S. The Bus Master IDE I/O registers are defined in the SFF8038i v1.0 specification.

### **Header Registers (0-3Fh)**

#### **Offset Address: 1-0h (B0D15F1)**

**Vendor ID**
**Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	VIA Technology ID Code

#### **Offset Address: 3-2h (B0D15F1)**

**Vendor ID**
**Default Value: 0571h**

Bit	Attribute	Default	Description
15:0	RO	0571h	Device ID Code

#### **Offset Address: 5-4h (B0D15F1)**

**PCI Command**
**Default Value: 0000h**

Bit	Attribute	Default	Description
15:11	RO	0	<b>Reserved</b>
10	RW	0	<b>Interrupt Disable</b>
9:3	RO	0	<b>Reserved</b>
2	RW	0	<b>Bus Master</b> S/G Operation can be issued only when the “Bus Master” bit is enabled. 0: Disable 1: Enable
1	RO	0	<b>Reserved</b>
0	RW	0	<b>I/O Space</b> When the “I/O Space” bit is disabled, the device will not respond to any I/O address for both compatible and native mode. 0: Disable 1: Enable

#### **Offset Address: 7-6h (B0D15F1)**

**Status**
**Default Value: 0290h**

Bit	Attribute	Default	Description
15:14	RO	0	<b>Reserved</b>
13	RWC	0	<b>Received Master Abort</b>
12	RWC	0	<b>Received Target Abort</b>
11	RO	0	<b>Reserved</b>
10:9	RO	01b	<b>DEVSEL# Timing</b> Fixed at 01b
8	RO	0	<b>Reserved</b>
7	RO	1b	<b>Fast Back to Back Capable</b> Fixed at 1b
6:5	RO	0	<b>Reserved</b>
4	RO	1b	<b>Capability List.</b> Fixed at 1b
3	RO	0	<b>Interrupt Status</b>
2:0	RO	0	<b>Reserved</b>

**Offset Address: 8h (B0D15F1)**
**Revision ID**
**Default Value: 07h**

Bit	Attribute	Default	Description
7:0	RO	07h	<b>Revision ID</b>

**Offset Address: 9h (B0D15F1)**
**Programming Interface**
**Default Value: 8Ah**

Bit	Attribute	Default	Description
7	RO	1b	<b>Master IDE Capability Supported</b> Fixed at 1b
6:4	RO	0	<b>Reserved</b>
3	RO	1b	<b>Secondary Channel Native Mode Capability Supported</b>
2	RW	0	<b>Channel Operating Mode – Secondary</b> 0: Compatibility Mode 1: Native PCI Mode
1	RO	1b	<b>Primary Channel Native Mode Capability Supported</b>
0	RW	0	<b>Channel Operating Mode – Primary</b> 0: Compatibility Mode 1: Native PCI Mode Note: [7:0] will be RO when Rx0A (Sub Class Code) is RAID Controller (default = 04h).

**Offset Address: 0Ah (B0D15F1)**
**Sub Class Code**
**Default Value: 01h**

Bit	Attribute	Default	Description
7:0	RO	01h	<b>Sub Class Code</b> 01h: IDE Controller 04h: RAID controller

Note: 1. Switch to RAID controller will enter native mode automatically.

**Offset Address: 0Bh (B0D15F1)**
**Base Class Code**
**Default Value: 01h**

Bit	Attribute	Default	Description
7:0	RO	01h	<b>Base Class Code</b> Fixed at 01h (mass storage controller).

**Offset Address: 0Ch (B0D15F1)**
**Cache Line Size**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	<b>Cache Line Size</b>

**Offset Address: 0Dh (B0D15F1)**
**Latency Timer**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	<b>Latency Timer</b>
3:0	RO	0	Fixed at 0

**Offset Address: 0Eh (B0D15F1)**
**Header Type**
**Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	<b>Multiple Function Device</b>
6:0	RO	0	Fixed at 0

**Offset Address: 0Fh (B0D15F1) - Reserved**

**Offset Address: 13-10h (B0D15F1)**
**Primary Data / Command Base Address**
**Default Value: 0000 0000h**

Specifies an 8 byte I/O address space.

Bit	Attribute	Default	Description
31:16	RO	0	<b>Reserved</b> . Must be 0.
15:3	RW	0	<b>Port Address</b>
2	RO	0	<b>Fixed at 0</b>
1:0	RO	0	<b>I/O Cycle</b>

Note:

1. RO when during Compatibility Mode and its value is always 0000 0000h.
2. Default is 1F1h when during Native Mode.
3. Reset to default (1F1h) when changing from native to compatible if Rx72[5] is set. If Rx72[5] is cleared, this field will be kept when changing from native to compatible.

**Offset Address: 17-14h (B0D15F1)**
**Primary Control / Status Base Address**
**Default Value: 0000 0000h**

Specifies a 4 byte I/O address space.

Bit	Attribute	Default	Description
31:16	RO	0	<b>Reserved</b> . Must be 0.
15:2	RW	0	<b>Port Address</b>
1:0	RO	0	<b>I/O Cycle</b>

Note:

1. RO when during Compatibility Mode and its value is always 0000 0000h.
2. Default is 3F5h when during Native Mode.
3. Only the third byte is active.
4. Reset to default (3F5h) when changing from native to compatible if Rx72[5] is set. If Rx72[5] is cleared, this field will be kept when changing from native to compatible.

**Offset Address: 1B-18h (B0D15F1)**
**Secondary Data / Command Base Address**
**Default Value: 0000 0000h**

Specifies an 8 byte I/O address space.

Bit	Attribute	Default	Description
31:16	RO	0	<b>Reserved</b> . Must be 0.
15:3	RW	0	<b>Port Address</b>
2	RO	0	<b>Fixed at 0</b>
1:0	RO	0	<b>I/O Cycle</b>

Note:

1. RO when during Compatibility Mode and its value is always 0000 0000h.
2. Default is 171h when during Native Mode.
3. Reset to default (171h) when changing from native to compatible if Rx72[5] is set. If Rx72[5] is cleared, this field will be kept when changing from native to compatible.

**Offset Address: 1F-1Ch (B0D15F1)**
**Secondary Control / Status Base Address**
**Default Value: 0000 0000h**

Specifies a 4 byte I/O address space.

Bit	Attribute	Default	Description
31:16	RO	0	<b>Reserved</b> . Must be 0.
15:2	RW	0	<b>Port Address</b>
1:0	RO	0	<b>I/O Cycle</b>

Note:

1. RO when during Compatibility Mode and its value is always 0000 0000h.
2. Default is 375h when during Native Mode.
3. Only the third byte is active.
4. Reset to default (375h) when changing from native to compatible if Rx72[5] is set. If Rx72[5] is cleared, this field will be kept when changing from native to compatible.

**Offset Address: 23-20h (B0D15F1)**
**But Master Control Registers Base Address**
**Default Value: 0000 0001h**

Specifies a 16 byte I/O address space and detailed information in the next section.

Bit	Attribute	Default	Description
31:16	RO	0	<b>Reserved</b> . Must be 0.
15:4	RW	0	<b>Port Address</b>
3:2	RO	0	<b>Fixed at 0</b>
1:0	RO	01b	<b>I/O Cycle</b>

**Offset Address: 2B-24h (B0D15F1) - Reserved**
**Offset Address: 2D-2Ch (B0D15F1)**
**Subsystem Vendor**
**Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	<b>Subsystem Vendor ID</b> The read back value can be changed by writing to RxD4-D5.

**Offset Address: 2F-2Eh (B0D15F1)**
**Subsystem ID**
**Default Value: 0571h**

Bit	Attribute	Default	Description
15:0	RO	0571h	<b>Subsystem ID</b> The read back value can be changed by writing to RxD6-D7.

**Offset Address: 33-30h (B0D15F1) - Reserved**
**Offset Address: 34h (B0D15F1)**
**PCI Power Management Capability Pointer**
**Default Value: C0h**

Bit	Attribute	Default	Description
7:0	RO	C0h	<b>Capability Pointer</b>

**Offset Address: 3B-35h (B0D15F1) - Reserved**
**Offset Address: 3Ch (B0D15F1)**
**Interrupt Line**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	<b>Reserved</b>
3:0	RW	0	<b>IDE Interrupt Line Routing (native mode only)</b> If modify bit [7:4] to 1111b, route to IRQ0. Others are decoded to IRQ0 ~ IRQ15.

**Offset Address: 3Dh (B0D15F1)**
**Interrupt Pin**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	<b>Interrupt Pin Routing Mode</b> 01h: Native mode interrupt pin routing 00h: Compatibility mode interrupt pin routing

**Offset Address: 3F-3Eh (B0D15F1)**
**Minimum Grant and Maximum Latency**
**Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RO	0	<b>Minimum Grant and Maximum Latency</b>

**IDE-Controller-Specific Configuration Registers (40-BFh)**
**Offset Address: 40h (B0D15F1)**
**Chip Enable**
**Default Value: 08h**

Bit	Attribute	Default	Description
7:2	RO	02h	<b>Reserved</b> (Do Not Program)
1	RW	0	<b>IDE Primary Channel Enable</b> 0: Disable 1: Enable
0	RW	0	<b>IDE Secondary Channel Enable</b> 0: Disable 1: Enable

**Offset Address: 41h (B0D15F1)**
**IDE Configuration**
**Default Value: 02h**

Bit	Attribute	Default	Description
7	RW	0	<b>Primary IDE PIO Read Prefetch Enable</b> 0: Disable 1: Enable
6	RW	0	<b>Primary IDE PIO Post Write Enable</b> 0: Disable 1: Enable
5	RW	0	<b>Secondary IDE PIO Read Prefetch Enable</b> 0: Disable 1: Enable
4	RW	0	<b>Secondary IDE PIO Post Write Enable</b> 0: Disable 1: Enable
3:0	RO	2h	<b>Reserved</b> (Do Not Program)

**Offset Address: 42h (B0D15F1)**
**Miscellaneous Control**
**Default Value: 09h**

Bit	Attribute	Default	Description
7	RW	0	<b>PIO Operating Mode – Primary Channel</b> Selects the mode used in the primary channel for the I/O Base Address (not IRQ routing or sharing). 0: Compatibility Mode (fixed addressing) 1: Native PCI Mode (flexible addressing)
6	RW	0	<b>PIO Operating Mode – Secondary Channel</b> Selects the mode used in the secondary channel for the I/O Base Address (not IRQ routing or sharing). 0: Compatibility Mode (fixed addressing) 1: Native PCI Mode (fixed addressing)
5	RW	0	<b>Interrupt Operation Mode – Primary</b> 0: Compatibility mode (fixed interrupt) 1: Native mode (flexible interrupt)
4	RW	0	<b>Interrupt Operation Mode – Secondary</b> 0: Compatibility mode (fixed interrupt) 1: Native mode (flexible interrupt)
3:0	RO	9h	<b>Reserved</b> (Do Not Program)

Note:

1. Bit [7:4] are read only when Rx0A (Sub Class Code) = 04h (RAID mode).
2. Do not program Rx42[7:4].

**Offset Address: 43h (B0D15F1)**
**FIFO Configuration**
**Default Value: 05h**

Bit	Attribute	Default	Description
7:4	RO	0	<b>Reserved</b>
3:2	RW	01b	<b>Primary Channel FIFO Threshold</b> Determines the threshold required before the primary channel FIFO is flushed. 00: FIFO flushed when 1/4 full 01: FIFO flushed when 1/2 full 10: FIFO flushed when 3/4 full 11: FIFO flushed when completed full (Can not be used when UDMA is read)
1:0	RW	01b	<b>Secondary Channel FIFO Threshold</b> Determines the threshold required before the secondary channel FIFO is flushed. 00: FIFO flushed when 1/4 full 01: FIFO flushed when 1/2 full 10: FIFO flushed when 3/4 full 11: FIFO flushed when completed full (Can not be used when UDMA is read)

Note:

1. If Rx72[4] = 1, bit 3-0 is only threshold for device to memory transfer.
2. If Rx72[4] = 0, bit 3-0 is threshold for both device to memory and memory to device transfer. (default)

**Offset Address: 44h (B0D15F1)**
**Miscellaneous Control**
**Default Value: 08h**

Bit	Attribute	Default	Description
7:5	RO	0	<b>Reserved</b>
4	RW	0	<b>PIO Read Pre-Fetch Byte Counter</b> Determines whether the amount of data prefetched under PIO read is limited. 0: Disable (no limit) 1: Enable. The maximum number of bytes that can be prefetched is determined by Rx61-60[11:0] for the Primary channel and Rx69-68[11:0] for the secondary channel.
3	RW	1b	<b>Bus Master IDE Status Register Read Retry</b> Determines whether a read to the bus master IDE status register is retried when DMA operation is not complete. 0: Disable. Reads will return status even if DMA operation is not complete. 1: Enable. Reads of the status register are automatically retried while DMA operation is not complete.
2	RW	0	<b>Packet Command Prefetching</b> Determines whether prefetching is enabled for packet commands. Packet commands are commands for ATAPI, which is used for operating devices such as CD-ROM drives. 0: Disable default 1: Enable
1	RO	0	<b>Reserved</b>
0	RW	0	<b>UltraDMA Host Must Wait for First Transfer Before Termination</b> 0: Enable. The UltraDMA host must wait until at least the first transfer is completed before it can terminate a transaction. 1: Disable

**Offset Address: 45h (B0D15F1)**
**Miscellaneous Control**
**Default Value: 80h**

Bit	Attribute	Default	Description
7	RW	1b	<b>Rx0A (Sub Class Code) Write Protect</b> 0: Disable (writes to Rx0A are allowed) 1: Enable (writes to Rx0A are ignored)
6	RW	0	<b>Interrupt Steering Swap</b> Controls whether primary and secondary channel interrupts are swapped. 0: Primary channel interrupt is steered to IRQ14, Secondary channel is steered to IRQ15 1: Primary channel interrupt is steered to IRQ15, Secondary channel interrupt is steered to IRQ14
5	RO	0	<b>Reserved</b>
4	RW	0	<b>Rx3C (Interrupt Line) Write Protect</b> 0: Disable (writes to Rx3C are allowed) 1: Enable (writes to Rx3C are ignored)
3	RW	0	<b>“Memory-Read-Multiple” Command</b> 0: Disable 1: Enable
2	RW	0	<b>“Memory-Write-and-Invalidate” Command</b> 0: Disable 1: Enable
1	RW	0	<b>Force Internal Clock as 100MHz Clock Source</b> 0: Disable 1: Enable
0	RO	0	<b>Reserved</b>

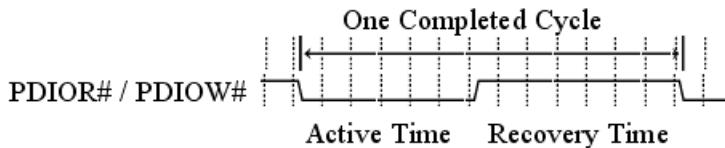
**Offset Address: 46h (B0D15F1)**
**Miscellaneous Control**
**Default Value: C0h**

Bit	Attribute	Default	Description
7	RW	1b	<b>Primary Channel Read DMA FIFO Flush</b> 0: Disable 1: Enable. The primary channel DMA FIFO is flushed when an interrupt request is generated.
6	RW	1b	<b>Secondary Channel Read DMA FIFO Flush</b> 0: Disable 1: Enable. The secondary channel DMA FIFO is flushed when an interrupt request is generated.
5:3	RO	0	<b>Reserved</b>
2	RW	0	<b>Scatter / Gather Descriptor Pre-Fetch Cache Feature Enable</b>
1:0	RO	0	<b>Reserved</b>

**Offset Address: 47h (B0D15F1) - Reserved**

**Offset Address: 4B-48h (B0D15F1)**
**IDE Drive Timing Control**
**Default Value: A8A8 A8A8h**

The following fields define the Active Pulse Width and Recovery Time for the IDE PDIOR# and PDIOW# signals when accessing the data ports (1F0 and 170):



The actual value for each field is the encoded value in the field plus one and indicates the number of PCI clocks. For example, if the value in the field is 1010b (10 decimal), the active pulse width or recovery time is 11 PCI clocks.

Bit	Attribute	Default	Description
31:28	RW	1010b	<b>Primary Drive 0 Active Pulse Width</b>
27:24	RW	1000b	<b>Primary Drive 0 Recovery Time</b>
23:20	RW	1010b	<b>Primary Drive 1 Active Pulse Width</b>
19:16	RW	1000b	<b>Primary Drive 1 Recovery Time</b>
15:12	RW	1010b	<b>Secondary Drive 0 Active Pulse Width</b>
11:8	RW	1000b	<b>Secondary Drive 0 Recovery Time</b>
7:4	RW	1010b	<b>Secondary Drive 1 Active Pulse Width</b>
3:0	RW	1000b	<b>Secondary Drive 1 Recovery Time</b>

Note: PIO Data Port (1F0 and 170h) access timing control and Multi-Word DMA cycle timing control, timing = (Program Value + 1) \* 30 ns.

**Offset Address: 4Ch (B0D15F1)**
**Address Setup Time**
**Default Value: FFh**

The following fields define the Address Setup Time. The Address Setup Time is measured from the point when address signals are stable to the point when PDIOR# and PDIOW# are asserted. The IDE specification requires the setup time to not exceed 1T. However, the VT8237S provides flexibility for devices that may not be able to meet the 1T requirement.

Bit	Attribute	Default	Description
7:6	RW	11b	<b>Primary Drive 0 Address Setup Time</b> 00: 1T 01: 2T 10: 3T 11: 4T
5:4	RW	11b	<b>Primary Drive 1 Address Setup Time (Slave)</b> 00: 1T 01: 2T 10: 3T 11: 4T
3:2	RW	11b	<b>Secondary Drive 0 Address Setup Time (Master)</b> 00: 1T 01: 2T 10: 3T 11: 4T
1:0	RW	11b	<b>Secondary Drive 1 Address Setup Time (Slave)</b> 00: 1T 01: 2T 10: 3T 11: 4T

Note: Timing = (Program Value + 1) \* 30 ns, 1T = 30ns.

**Offset Address: 4Dh (B0D15F1) - Reserved**
**Offset Address: 4Eh (B0D15F1)**
**Secondary IDE Drive Non-Data Port Access Timing**
**Default Value: B6h**

Bit	Attribute	Default	Description
7:4	RW	Bh	<b>PDIOR# / PDIOW# Active Pulse Width</b>
3:0	RW	6h	<b>PDIOR# / PDIOW# Recovery Time</b>

Note: Secondary IDE Non-Data Port (171h ~ 177h) access timing control, timing = (Program Value + 1) \* 30ns.

**Offset Address: 4Fh (B0D15F1)**
**Primary IDE Drive Non-Data Port Access Timing**
**Default Value: B6h**

Bit	Attribute	Default	Description
7:4	RW	Bh	<b>PDIOR# / PDIOW# Active Pulse Width</b>
3:0	RW	6h	<b>PDIOR# / PDIOW# Recovery Time</b>

Note: Secondary IDE Non-Data Port (1F1h ~ 1F7h) access timing control, timing = (Program Value + 1) \* 30ns.

**Offset Address: 50h (B0D15F1)**
**Secondary IDE Drive 1 (Slave) Ultra DMA Mode Control**
**Default Value: 07h**

Bit	Attribute	Default	Description
7	RW	0	<b>Ultra DMA Source Mode Enable</b> 0: Set feature command 1: Register feature command
6	RW	0	<b>Ultra DMA Mode Enable</b> 0: Disable 1: Enable
5	RO	0	<b>Current Transfer Mode</b> 0: PIO or DMA Mode 1: Ultra DMA Mode
4	RW	0	<b>Cable Type Reporting</b> 0: 40-pin cable is being used 1: 80-pin cable is being used
3:0	RW	7h	<b>Ultra DMA Write Strobe Timing Control</b> 0: (Program Value + 2) * 7.5ns 1: (Program Value + 2) * 10ns (Ultra DMA 100 Using) 2-15: (Program Value + 2) * 7.5ns

**Offset Address: 51h (B0D15F1)**
**Secondary IDE Drive 0 (Master) Ultra DMA Mode Control**
**Default Value: 07h**

Bit	Attribute	Default	Description
7	RW	0	<b>Ultra DMA Source Mode Enable</b> 0: Set feature command 1: Register feature command
6	RW	0	<b>Ultra DMA Mode Enable</b> 0: Disable 1: Enable
5	RO	0	<b>Current Transfer Mode</b> 0: PIO or DMA Mode 1: Ultra DMA Mode
4	RW	0	<b>Cable Type Reporting</b> 0: 40-pin cable is being used 1: 80-pin cable is being used
3:0	RW	7h	<b>Ultra DMA Write Strobe Timing Control</b> 0: (Program Value + 2) * 7.5ns 1: (Program Value + 2) * 10ns (Ultra DMA 100 Using) 2-15: (Program Value + 2) * 7.5ns

**Offset Address: 52h (B0D15F1)**
**Primary IDE Drive 1 (Slave) Ultra DMA Mode Control**
**Default Value: 07h**

Bit	Attribute	Default	Description
7	RW	0	<b>Ultra DMA Source Mode Enable</b> 0: Set Feature Command 1: Register Feature Command
6	RW	0	<b>Ultra DMA Mode Enable</b> 0: Disable 1: Enable
5	RO	0	<b>Current Transfer Mode</b> 0: PIO or DMA Mode 1: Ultra DMA Mode
4	RW	0	<b>Cable Type Reporting</b> 0: 40-pin cable is being used 1: 80-pin cable is being used
3:0	RW	7h	<b>Ultra DMA Write Strobe Timing Control</b> 0: (Program Value + 2) * 7.5ns 1: (Program Value + 2) * 10ns (Ultra DMA 100 Using) 2-15: (Program Value + 2) * 7.5ns

**Offset Address: 53h (B0D15F1)**
**Primary IDE Drive 0 (Master) Ultra DMA Mode Control**
**Default Value: 07h**

Bit	Attribute	Default	Description
7	RW	0	<b>Ultra DMA Source Mode Enable</b> 0: Set Feature Command 1: Register Feature Command
6	RW	0	<b>Ultra DMA Mode Enable</b> 0: Disable 1: Enable
5	RO	0	<b>Current Transfer Mode</b> 0: PIO or DMA Mode 1: UltraDMA Mode
4	RW	0	<b>Cable Type Reporting</b> 0: 40-pin cable is being used 1: 80-pin cable is being used
3:0	RW	7h	<b>Ultra DMA Write Strobe Timing Control</b> 0: (Program Value + 2) * 7.5ns 1: (Program Value + 2) * 10ns (Ultra DMA 100 Using) 2-15: (Program Value + 2) * 7.5ns

**Offset Address: 54h (B0D15F1)**
**Revision**
**Default Value: 0Ch**

Bit	Attribute	Default	Description
7	RW	0	<b>Enable Legacy IRQ14 or IRQ15 Usage when IDE Channel is Disabled</b> 0: Enable. Release IRQ14 when Rx40[1] is cleared, release IRQ15 when Rx40[0] is cleared. 1: Disable
6	RO	0	<b>Reserved</b>
5	RW	0	<b>Clear Native Mode Interrupt on Falling Edge of Gated Interrupt</b> 0: Disable 1: Enable. The interrupt will be automatically cleared on the falling edge of the gated interrupt.
4	RW	0	<b>Improve PIO Prefetch and Post-Write Performance</b> 0: Enable. PIO prefetch and post write performance is increased by being given higher throughput. 1: Disable
3	RW	1b	<b>Memory Prefetch Size</b> This bit determines how many lines are prefetched from memory for IDE transactions. 0: Prefetch 1 line 1: Prefetch 2 lines (16 DoubleWords). This setting improves ATA100 throughput.
2	RW	1b	<b>Change Drive Clears All FIFO &amp; Internal States</b> 0: Disable 1: Command switch from one drive to another drive in the same channel terminates all previous outstanding transactions involving the previous drive.
1:0	RO	0	<b>Reserved</b>

**Offset Address: 55h (B0D15F1)**
**IDE Clock Gating**
**Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	<b>Primary Channel Hot Swap Enable</b> 0: Disable 1: Enable When set 1, primary channel bus will tri-state and read status will be 7fh
6	RW	0	<b>Secondary Channel Hot Swap Enable</b> 0: Disable 1: Enable When set 1, secondary channel bus will tri-state and read status will be 7fh
5:4	RO	0	<b>Reserved</b>
3	RW	0	<b>FIFO Dynamic 100/133MHz Clock Gating</b> 0: Enable 1: Disable
2	RO	0	<b>Reserved</b>
1	RW	0	<b>Dynamic 100/133 MHz Clock Gating</b> 0: Enable 1: Disable
0	RW	0	<b>Dynamic 66 MHz Clock Gating</b> 0: Enable 1: Disable

**Offset Address: 5F-56h (B0D15F1) - Reserved**
**Offset Address: 61-60h (B0D15F1)**
**Primary IDE Sector Size**
**Default Value: 0200h**

Bit	Attribute	Default	Description
15:12	RO	0	<b>Reserved</b>
11:0	RW	200h	<b>Prefetch Sector Size</b>

**Offset Address: 67-62h (B0D15F1) - Reserved**
**Offset Address: 69-68h (B0D15F1)**
**Secondary IDE Sector Size**
**Default Value: 0200h**

Bit	Attribute	Default	Description
15:12	RO	0	<b>Reserved</b>
11:0	RW	200h	<b>Prefetch Sector Size</b>

**Offset Address: 70h (B0D15F1)**
**Primary IDE Status**
**Default Value: 02h**

Bit	Attribute	Default	Description
7	RO	0	<b>Interrupt Status</b> 1: Primary channel interrupt request pending
6	RO	0	<b>PIO Prefetch Status</b> 1: PIO Prefetch transaction in progress
5	RO	0	<b>PIO Post Write Status</b> 1: PIO Post Write transaction in progress
4	RO	0	<b>DMA Read Operation Status</b> 1: DMA Read Prefetch transaction in progress
3	RO	0	<b>DMA Write Operation Status</b> 1: DMA Write transaction in progress
2	RO	0	<b>Bus Master Operation Complete</b> 1: Bus Master transaction in progress
1	RO	1b	<b>FIFO Empty Status</b> 1: Primary Channel FIFO empty
0	RO	0	<b>Response to External DMA Request</b> 1: External primary channel DMA request pending

**Offset Address: 71h (B0D15F1)**
**Primary Interrupt Gating**
**Default Value: 01h**

Bit	Attribute	Default	Description
7:1	RO	0	<b>Reserved</b>
0	RW	1b	<b>Interrupt Gating</b> 0: Disable 1: Enable (IRQ output gated until FIFO empty)

**Offset Address: 72h (B0D15F1)**
**Miscellaneous Control**
**Default Value: 25h**

Bit	Attribute	Default	Description
7:6	RO	0	<b>Reserved</b>
5	RW	1b	<b>Enable Reset I/O Base Address When Changing from Native Mode to Compatible Mode</b> 0: Disable 1: Enable
4	RW	0	<b>Separate FIFO Threshold Usage Enable</b> 0: Disable 1: Enable
3:2	RW	01b	<b>Primary Channel FIFO Threshold (Memory to Device)</b>
1:0	RW	01b	<b>Secondary Channel FIFO Threshold (Memory to Device)</b> 00: 1/4 01: 1/2 10: 3/4 11: 1

**Offset Address: 77-73h (B0D15F1) - Reserved**
**Offset Address: 78h (B0D15F1)**
**Secondary IDE Status**
**Default Value: 02h**

Bit	Attribute	Default	Description
7	RO	0	<b>Interrupt Status</b> 1: Secondary channel interrupt request pending
6	RO	0	<b>PIO Prefetch Status</b> 1: PIO Prefetch transaction in progress
5	RO	0	<b>PIO Post Write Status</b> 1: PIO Post Write transaction in progress
4	RO	0	<b>DMA Read Operation Status</b> 1: DMA Read Prefetch transaction in progress
3	RO	0	<b>DMA Write Operation Status</b> 1: DMA Write transaction in progress
2	RO	0	<b>Bus Master Operation Complete</b> 1: Bus Master transaction in progress
1	RO	1b	<b>FIFO Empty Status</b> 1: Primary Channel FIFO empty
0	RO	0	<b>Response to External DMA Request</b> 1: External primary channel DMA request pending

**Offset Address: 79h (B0D15F1)**
**Secondary Interrupt Gating**
**Default Value: 01h**

Bit	Attribute	Default	Description
7:1	RO	0	<b>Reserved</b>
0	RW	1b	<b>Interrupt Gating</b> 0: Disable 1: Enable (IRQ output gated until FIFO empty)

**Offset Address: 83-80h (B0D15F1)**
**Primary Channel Scatter / Gather Descriptor Address**
**Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:2	RW	0	Primary Channel Scatter / Gather Descriptor Address [31:2]
1:0	RO	0	Primary Channel Scatter / Gather Descriptor Address[1:0]. Fix at 0.

**Offset Address: 87-84h (B0D15F1) - Reserved**
**Offset Address: 8B-88h (B0D15F1)**
**Secondary Channel Scatter / Gather Descriptor Address**
**Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:2	RW	0	Secondary Channel Scatter / Gather Descriptor Address [31:2]
1:0	RO	0	Secondary Channel Scatter / Gather Descriptor Address[1:0]. Fix at 0.

Note: Rx83-80 and Rx8B-88 are used for debugging purposes only.

**Offset Address: BF-8Ch (B0D15F1) - Reserved**

**IDE Power Management Registers (C0-CFh)**
**Offset Address: C3-C0h (B0D15F1)**
**PCI Power Management Capability**
**Default Value: 0002 0001h**

Bit	Attribute	Default	Description
31:19	RO	0	<b>PM Capabilities</b>
18:16	RO	010b	<b>Version – Indicates PCI PM Spec Rev 1.1 Support</b>
15:8	RO	0	<b>Next Capability</b>
7:0	RO	01h	<b>Cap ID</b>

Note: This field reports support details for Power Management Capabilities according to the PCI Power Management specification.

**Offset Address: C5-C4h (B0D15F1)**
**Power Management Control / Status**
**Default Value: 0000h**

Bit	Attribute	Default	Description	
15:2	RO	0	<b>Reserved</b>	
1:0	RW	00b	<b>Power State</b> 00: D0 10: Reserved	01: Reserved 11: D3 Hot

**Offset Address: D3-C6h (B0D15F1) - Reserved**
**Offset Address: D5-D4h (B0D15F1)**
**Subsystem Vender ID Back Door Registers**
**Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RW	1106h	<b>Subsystem-Vendor ID (Rx2C-2D) Back Door</b>

**Offset Address: D7-D6h (B0D15F1)**
**Subsystem ID Back Door Registers**
**Default Value: 0571h**

Bit	Attribute	Default	Description
15:0	RW	0571h	<b>Subsystem ID (Rx2E-2F) Back Door</b>

**Offset Address: F5-D8h (B0D15F1) – Reserved**

### Bus Master IDE I/O Registers (0-0Fh)

These registers are compliant with the SFF 8038I v1.0 standard. Refer to the SFF 8038I v1.0 specification for further details. Rx23-20h is Bus Master IDE I/O Registers base address.

#### I/O Offset Address: 0h

##### Primary Channel Bus Master IDE Command

**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	Primary Channel Bus Master IDE Command

#### I/O Offset Address: 1h – Reserved

#### I/O Offset Address: 2h

##### Primary Channel Bus Master Status

**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW1C	0	Primary Channel Bus Master Status

#### I/O Offset Address: 3h – Reserved

#### I/O Offset Address: 7-4h

##### Primary Channel Bus Master IDE Descriptor Table Pointer

**Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	Primary Channel Bus Master IDE Descriptor Table Pointer

#### I/O Offset Address: 8h

##### Secondary Channel Bus Master IDE Command

**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	Secondary Channel Bus Master IDE Command

#### I/O Offset Address: 9h – Reserved

#### I/O Offset Address: 0Ah

##### Secondary Channel Bus Master Status

**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW1C	0	Secondary Channel Bus Master Status

#### I/O Offset Address: 0Bh – Reserved

#### I/O Offset Address: 0F-0Ch

##### Secondary Channel Bus Master IDE Descriptor Table Pointer

**Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	Secondary Channel Bus Master IDE Descriptor Table Pointer

## Bus 0 Device 16 Function 0-3 (D16F0-F3) – USB 1.1 UHCI Ports 0-7

This Universal Serial Bus host controller interface is fully compatible with UHCI specification v1.1. There are two sets of software accessible registers: PCI configuration registers and USB I/O registers. The PCI configuration registers are located in the Bus 0 Device 16 Function 0-3 PCI configuration space of the VT8237S. The USB I/O registers are defined in UHCI specification v1.1. The registers are identical in the Bus 0 Device 16 Functions 0-3 where each function controls different USB ports (function 0 for ports 0-1, function 1 for ports 2-3, function 2 for ports 4-5, and function 3 for ports 6-7).

### PCI Configuration Space Header (0-3Fh)

#### Offset Address: 1-0h (B0D16F0-F3)

**Vendor ID**
**Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	VIA Technology ID Code

#### Offset Address: 3-2h (B0D16F0-F3)

**Device ID**
**Default Value: 3038h**

Bit	Attribute	Default	Description
15:0	RO	3038h	Device ID Code

#### Offset Address: 5-4h (B0D16F0-F3)

**Command**
**Default Value: 0000h**

Bit	Attribute	Default	Description
15:11	RO	0	<b>Reserved</b>
10	RW	0	<b>Interrupt Disable</b>
9:5	RO	0	<b>Reserved</b>
4	RW	0	<b>Memory Write and Invalidate</b>
3	RO	0	<b>Respond To Special Cycle</b> Hardwired to 0 (Does not monitor special cycles)
2	RW	0	<b>Bus Master</b>
1	RW	0	<b>Memory Space</b>
0	RW	0	<b>I/O Space</b>

#### Offset Address: 7-6h (B0D16F0-F3)

**Status**
**Default Value: 0210h**

Bit	Attribute	Default	Description
15:14	RO	0	<b>Reserved</b>
13	RW1C	0	<b>Received Master Abort</b>
12	RW1C	0	<b>Received Target Abort</b>
11	RO	0	<b>Reserved</b>
10:9	RO	01b	<b>DEVSEL# Timing</b> Fixed at 01b 00: Fast 10: Slow 01: Medium 11: Reserved
8:4	RO	01h	<b>Fixed at 01h</b> (for PCI PMI)
3	RW1C	0	<b>Interrupt Status</b>
2:0	RO	0	<b>Fixed at 0</b> (for PCI PMI)

**Offset Address: 8h (B0D16F0-F3)**
**Revision ID**
**Default Value:** nnh

Bit	Attribute	Default	Description
7:0	RO	nnh	<b>Revision ID</b>

**Offset Address: 0B-9h (B0D16F0-F3)**
**Class Code**
**Default Value:** 0C 0300h

Bit	Attribute	Default	Description
23:0	RO	0C 0300h	<b>Class Code</b> To indicate the USB1.1 Host Controller

**Offset Address: 0Ch (B0D16F0-F3)**
**Cache Line Size**
**Default Value:** 00h

Bit	Attribute	Default	Description
7:0	RW	0	<b>Cache Line Size</b>

**Offset Address: 0Dh (B0D16F0-F3)**
**Latency Timer**
**Default Value:** 16h

Bit	Attribute	Default	Description
7:0	RW	16h	<b>Latency Timer</b>

**Offset Address: 0Eh (B0D16F0-F3)**
**Header Type Default**
**Value:** 80h

Bit	Attribute	Default	Description
7:0	RO	80h	<b>Header Type</b>

**Offset Address: 0Fh (B0D16F0-F3)**
**BIST**
**Default Value:** 00h

Bit	Attribute	Default	Description
7:0	RO	0	<b>BIST (Build In Self Test)</b> Fixed at 0

**Offset Address: 1F-10h (B0D16F0-F3) - Reserved**
**Offset Address: 23-20h (B0D16F0-F3)**
**USB I/O Register Base Address**
**Default Value:** 0000 FCE1h

Bit	Attribute	Default	Description
31:16	RO	0	<b>Reserved</b>
15:5	RW	07E7h	<b>USB I/O Register Base Address</b> Port Address for the base of the 32-byte USB I/O Register block, corresponding to AD[15:5]
4:0	RO	01h	<b>32 Byte Aligned IO Space</b>

**Offset Address: 2D-2Ch (B0D16F0-F3)**
**Subsystem Vendor ID**
**Default Value:** 1106h

Bit	Attribute	Default	Description
15:0	RO	1106h	<b>Subsystem Vendor ID</b> RW if Rx42[4] = 1

**Offset Address: 2F-2Eh (B0D16F0-F3)**
**Subsystem ID**
**Default Value: 3038h**

Bit	Attribute	Default	Description
15:0	RO	3038h	<b>Subsystem ID</b> RW if Rx42[4] = 1

**Offset Address: 33-30h (B0D16F0-F3) - Reserved**
**Offset Address: 34h (B0D16F0-F3)**
**Power Management Capabilities**
**Default Value: 80h**

Bit	Attribute	Default	Description
7:0	RO	80h	<b>Power Management Capabilities</b> Fixed at 80h

**Offset Address: 3B-35h (B0D16F0-F3) - Reserved**
**Offset Address: 3Ch (B0D16F0-F3)**
**Interrupt Line**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	<b>Reserved</b>
3:0	RW	0000b	<b>USB Interrupt Routing</b> 0000: Disabled 0010: Reserved 0100: IRQ4 0110: IRQ6 1000: IRQ8 1010: IRQ10 1100: IRQ12 1110: IRQ14 0001: IRQ1 0011: IRQ3 0101: IRQ5 0111: IRQ7 1001: IRQ9 1011: IRQ11 1101: IRQ13 1111: Disabled

**Offset Address: 3Dh (B0D16F0)**
**Interrupt Pin**
**Default Value: 01h**

Bit	Attribute	Default	Description
7:0	RO	01h	<b>Interrupt Pin</b> Fixed at 01h (INTA#)

**Offset Address: 3Dh (B0D16F1)**
**Interrupt Pin**
**Default Value: 02h**

Bit	Attribute	Default	Description
7:0	RO	02h	<b>Interrupt Pin</b> Fixed at 02h (INTB#)

**Offset Address: 3Dh (B0D16F2)**
**Interrupt Pin**
**Default Value: 03h**

Bit	Attribute	Default	Description
7:0	RO	03h	<b>Interrupt Pin</b> Fixed at 03h (INTC#)

### **Offset Address: 3Dh (B0D16F3)**

## **Interrupt Pin**

**Default Value: 04h**

Bit	Attribute	Default	Description
7:0	RO	04h	<b>Interrupt Pin</b> Fixed at 04h (INTD#)

## **Offset Address: 3F-3Eh (B0D16F3) - Reserved**

## **USB 1.1-Specific Configuration Registers (40-C1h)**

Offset Address: 41-40h (B0D16F0-F3) – Reserved

## **Offset Address: 42h (B0D16F0-F3)**

## Miscellaneous Control 3

**Default Value: 03h**

Bit	Attribute	Default	Description
7:5	RO	0	<b>Reserved</b>
4	RW	0	<b>Subsystem ID / Subsystem Vender ID Back Door Enable</b> Specifies whether Rx2C~2F are RO or RW 0: Read Only   1: Read / Write
3:0	<b>RO</b>	11b	<b>Reserved</b>

#### **Offset Address: 47-43h (B0D16F0-F3) – Reserved**

## Offset Address: 48h (B0D16F0-F3)

## Miscellaneous Control 5

**Default Value: 00h**

## **Offset Address: 49h (B0D16F0-F3)**

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## Miscellaneous Control 6

**Default Value: 0Bh**

Bit	Attribute	Default	Description
7:2	<b>RO</b>	0	<b>Reserved</b>
1	RW	1b	<b>EHCI Supports PME Assertion in D3 Cold State</b> 0: Not Supported      1: Supported
0	RW	1b	<b>UHCI Supports PME Assertion in D3 Cold State</b> 0: Not Supported      1: Supported

Note: Rx49[2:0] can only be written from function 0. Rx49[2:0] is RO for function 1~3.

## **Offset Address: 4Ah (B0D16F0-F3)**

## Miscellaneous Control 7

**Default Value:** A0h

Bit	Attribute	Default	Description
7:3	RW	14h	<b>USB 1.1 Bus Timeout Parameter</b>
2:1	<b>RO</b>	0	<b>Reserved</b>
0	RW	0	<b>Use External 60 MHz Clock</b> Set this bit to use external 60 MHz input clock 0: Disable                            1: Enable

## Offset Address: 4Bh (B0D16F0-F3)

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## Miscellaneous Control 8

**Default Value: 0Bh**

Bit	Attribute	Default	Description
7:4	<b>RO</b>	0	<b>Reserved</b>
3:1	RO	101b	<b>Reserved (Do Not Program)</b>
0	RW	1b	<b>Clock Auto Stop Enable</b> 0: Disable. No Stop                    1: Enable. Auto Stop

**Offset Address: 5F-4Ch (B0D16F0-F3) - Reserved**

**Offset Address: 60h (B0D16F0-F3)**

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## **Serial Bus Release Number**

**Default Value:** 10h

Bit	Attribute	Default	Description
7:0	RO	10h	<b>Release Number</b> Fixed at 10h

## **Offset Address: 7F-61h (B0D16F0-F3) - Reserved**

**Offset Address: 83-80h (B0D16F0-F3)**
**Power Management Capability**
**Default Value: FFC2 0001h**

Bit	Attribute	Default	Description
31:0	RO	FFC2 0001h	<b>Power Management Capability</b> If Rx49[0] = 1, this register is fixed at FFC20001h. If Rx49[0] = 0, this register is fixed at 7E0A0001h.

**Offset Address: 85-84h (B0D16F0-F3)**
**Power Management Capability Status**
**Default Value: 0000h**

Bit	Attribute	Default	Description
15	RWC	0	<b>PME Status</b> 0: Not active 1: Active
14:9	RO	0	<b>Reserved</b>
8	RW	0	<b>PME Enable</b> 0: Disable 1: Enable
7:2	RO	0	<b>Reserved</b>
1:0	RW	00b	<b>Power Management Capability Status</b> 00: D0 01: Reserved 10: Reserved 11: D3 Hot

**Offset Address: BF-86h (B0D16F0-F3) - Reserved**
**Offset Address: C1-C0h (B0D16F0-F3)**
**Legacy Support (for UHCI v1.1 Compliant)**
**Default Value: 2000h**

Bit	Attribute	Default	Description
15	RW1C	0	<b>End Of A20GATE Pass Through Status (A20PTS)</b>
14	RO	0	<b>Reserved</b> Fixed to 0.
13	RW	1	<b>USB PIRQ Enable (USBPIRQDEN)</b>
12	RO	0	<b>USB IRQ Status (USBIRQS)</b>
11	RW1C	0	<b>Trap By 64h Write Status (TBY64W)</b>
10	RW1C	0	<b>Trap By 64h Read Status (TBY64R)</b>
9	RW1C	0	<b>Trap By 60h Write Status (TBY60W)</b>
8	RW1C	0	<b>Trap By 60h Read Status (TBY60R)</b>
7	RW	0	<b>SMI At End Of Pass Through Enable (SMIEPTE)</b>
6	RO	0	<b>Pass Through Status (PSS)</b>
5	RW	0	<b>A20Gate Pass Through Enable (A20PTEN)</b>
4	RW	0	<b>Trap/SMI On IRQ Enable (USBSMIEN)</b>
3	RW	0	<b>Trap/SMI On 64h Write Enable (64WEN)</b>
2	RW	0	<b>Trap/SMI On 64h Read Enable (64REN)</b>
1	RW	0	<b>Trap/SMI On 60h Write Enable (60WEN)</b>
0	RW	0	<b>Trap/SMI On 60h Read Enable (60REN)</b>

Note: This register provides control and status capability for the legacy keyboard and mouse functions. Please refer to UHCI Spec. for further details.

### I/O Offset Address: 0-13h

These registers are compliant with the UHCI v1.1 standard. Refer to the UHCI v1.1 specification for further details.

#### I/O Offset Address: 1-0h

##### USB Command

**Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW	0	USB Command

#### I/O Offset Address: 3-2h

##### USB Status

**Default Value: 0020h**

Bit	Attribute	Default	Description
15:0	RW1C	0020h	USB Status

#### I/O Offset Address: 5-4h

##### USB Interrupt Enable

**Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW	0	USB Interrupt Enable

#### I/O Offset Address: 7-6h

##### Frame Number

**Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW	0	Frame Number

#### I/O Offset Address: 0B-8h

##### Frame List Base Address

**Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	Frame List Base Address

#### I/O Offset Address: 0Ch

##### Start of Frame Modify

**Default Value: 40h**

Bit	Attribute	Default	Description
7:0	RW	40h	Start of Frame Modify

#### I/O Offset Address: 0F-0Dh – Reserved

#### I/O Offset Address: 11-10h

##### Port 0 Status / Control

**Default Value: 0480h**

Bit	Attribute	Default	Description
15:0	RO/RW/ RW1C	0480h	Port 0 Status / Control Refer to UHCI Spec. for detail.

#### I/O Offset Address: 13-12h

##### Port 1 Status / Control

**Default Value: 0480h**

Bit	Attribute	Default	Description
15:0	RO/RW/ RW1C	0480h	Port 1 Status / Control Refer to UHCI Spec. for detail.

## **Bus 0 Device 16 Function 4 (D16F4) - USB 2.0 EHCI**

This Enhanced Serial Bus host controller interface is fully compatible with EHCI specification v1.0. There are two sets of software accessible registers: PCI configuration registers and EHCI Memory I/O registers. The PCI configuration registers are located in the Bus 0 Device 16 Function 4 PCI configuration space of the VT8237S. The EHCI Memory I/O registers are defined in EHCI specification v1.0. The registers in this function control USB 2.0 functions.

## **PCI Configuration Space Header (0-3Fh)**

**Offset Address: 1-0h (B0D16F4)**

Vendor ID			Default Value: 1106h
Bit	Attribute	Default	Description
15:0	RO	1106h	VIA Technology ID Code

Offset Address: 3-2h (B0D16F4)

Device ID				Default Value: 3104h
Bit	Attribute	Default	Description	
15:0	PO	3104h	Device ID Code	

Offset Address: 5-4h (B0D16F4)

Command				Default Value: 0000h
Bit	Attribute	Default	Description	
15:11	RO	0	<b>Reserved</b>	
10	RW	0	<b>Interrupt Disable</b>	
9:5	RO	0	<b>Reserved</b>	
4	RW	0	<b>Memory Write and Invalidate</b>	
3	RO	0	<b>Reserved</b> (special cycle monitoring) Fixed at 0	
2	RW	0	<b>Bus Master</b>	
1	RW	0	<b>Memory Space</b>	
0	RW	0	<b>I/O Space</b>	

**Offset Address: 7-6h (B0D16F4)**

**Offset Address: 8h (B0D16F4)**
**Revision ID**
**Default Value:** mnh

Bit	Attribute	Default	Description
7:0	RO	nnh	<b>Revision ID</b>

**Offset Address: 0B-9h (B0D16F4)**
**Class Code**
**Default Value:** 0C 0320h

Bit	Attribute	Default	Description
23:0	RO	0C 0320h	<b>Class Code for USB2.0 EHCI Host Controller</b>

**Offset Address: 0Ch (B0D16F4)**
**Cache Line Size**
**Default Value:** 00h

Bit	Attribute	Default	Description
7:0	RW	0	<b>Cache Line Size</b>

**Offset Address: 0Dh (B0D16F4)**
**Latency Timer**
**Default Value:** 16h

Bit	Attribute	Default	Description
7:0	RW	16h	<b>Latency Timer</b>

**Offset Address: 0Eh (B0D16F4)**
**Header Type**
**Default Value:** 00h

Bit	Attribute	Default	Description
7:0	RO	0	<b>Header Type</b>

**Offset Address: 0Fh (B0D16F4)**
**BIST**
**Default Value:** 00h

Bit	Attribute	Default	Description
7:0	RO	0	<b>BIST (Built In Self Test).</b> Fixed at 00h

**Offset Address: 13-10h (B0D16F4)**
**EHCI Memory Mapped I/O Base Address**
**Default Value:** 0000 0000h

Bit	Attribute	Default	Description
31:8	RW	0	<b>EHCI Memory Mapped I/O Registers Base Address</b> Memory Address for the base of the USB 2.0 EHCI I/O Register block, corresponding to AD[31:8]
7:3	RO	0	<b>Reserved</b>
2:1	RO	0	<b>Memory Mapping</b> Reads 00b for 32-bit addressing
0	RO	0	<b>Reserved</b>

**Offset Address: 2B-14h (B0D16F4) - Reserved**

**Offset Address: 2D-2Ch (B0D16F4)**
**Subsystem Vendor ID**
**Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	<b>Subsystem Vendor ID</b> RW if Rx42[4] = 1

**Offset Address: 2F-2Eh (B0D16F4)**
**Subsystem ID**
**Default Value: 3104h**

Bit	Attribute	Default	Description
15:0	RO	3104h	<b>Subsystem ID</b> RW if Rx42[4] = 1

**Offset Address: 33-30h (B0D16F4) - Reserved**
**Offset Address: 34h (B0D16F4)**
**Power Management Capabilities**
**Default Value: 80h**

Bit	Attribute	Default	Description
7:0	RO	80h	<b>Power Management Capabilities.</b> Fixed at 80h

**Offset Address: 3B-35h (B0D16F4) - Reserved**
**Offset Address: 3Ch (B0D16F4)**
**Interrupt Line**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	<b>Reserved</b>
3:0	RW	0000b	<b>USB Interrupt Routing</b> 0000: Disabled 0001: IRQ1 0010: Reserved 0011: IRQ3 0100: IRQ4 0101: IRQ5 0110: IRQ6 0111: IRQ7 1000: IRQ8 1001: IRQ9 1010: IRQ10 1011: IRQ11 1100: IRQ12 1101: IRQ13 1110: IRQ14 1111: Disabled

**Offset Address: 3Dh (B0D16F4)**
**Interrupt Pin**
**Default Value: 04h**

Bit	Attribute	Default	Description
7:0	RO	04h	<b>Interrupt Pin.</b> Fixed at 04h

**Offset Address: 3F-3Eh (B0D16F4) - Reserved**

## USB 2.0-Specific Configuration Registers (40-FCh)

Offset Address: 41-40h (B0D16F4) – Reserved

**Offset Address: 42h (B0D16F4)**

## Miscellaneous Control 3

**Default Value: 03h**

**Offset Address: 43h (B0D16F4)**

## Miscellaneous Control 4

**Default Value: 00h**

<b>Bit</b>	<b>Attribute</b>	<b>Default</b>	<b>Description</b>
7	RW	0	<b>DIS_TERM_ON_H</b> Disable port 8 internal termination resistor in high-speed mode for system test.
6	RW	0	<b>DIS_TERM_ON_G</b> Disable port 7 internal termination resistor in high-speed mode for system test.
5	RW	0	<b>DIS_TERM_ON_F</b> Disable port 6 internal termination resistor in high-speed mode for system test.
4	RW	0	<b>DIS_TERM_ON_E</b> Disable port 5 internal termination resistor in high-speed mode for system test.
3	RW	0	<b>DIS_TERM_ON_D</b> Disable port 4 internal termination resistor in high-speed mode for system test.
2	RW	0	<b>DIS_TERM_ON_C</b> Disable port 3 internal termination resistor in high-speed mode for system test.
1	RW	0	<b>DIS_TERM_ON_B</b> Disable port 2 internal termination resistor in high-speed mode for system test.
0	RW	0	<b>DIS_TERM_ON_A</b> Disable port 1 internal termination resistor in high-speed mode for system test.

## **Offset Address: 48-44h (B0D16F4) – Reserved**

**Offset Address: 49h (B0D16F4)**

## Miscellaneous Control 6

**Default Value: 60h**

Bit	Attribute	Default	Description
7	RW	0	<b>Enable MAC Provides More Delay between Transactions</b> The delay parameter is in D16F4 Rx4A 0: Disable 1: Enable
6	RW	1b	<b>Enable MAC Provides Timeout to Device When Receiver Detects Error</b> The delay parameter is in D16F4 Rx51 0: Disable 1: Enable
5	RW	1b	<b>Clock Auto Stop</b> 0: Disable. No stop 1: Enable. Auto stop
4	RW	0	<b>Disable Auto Power Down Receiver Squelch Detector</b> 0: Auto power down 1: Always power up
3:0	RO	0	<b>Reserved</b>

**Offset Address: 4Ah (B0D16F4)**
**MAC Inter-Transaction Delay Parameter**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	<b>MAC Inter-Transaction Delay Parameter</b>

**Offset Address: 4Bh (B0D16F4)**
**Miscellaneous Control 7**
**Default Value: 09h**

Bit	Attribute	Default	Description
7:4	RO	0	<b>Reserved</b>
3:0	RW	9h	<b>USB 2.0 MAC Transmit Turn Around Time Parameter</b>

**Offset Address: 4Ch (B0D16F4)**
**Miscellaneous Control 8**
**Default Value: 12h**

Bit	Attribute	Default	Description
7:5	RO	0	<b>Reserved</b>
4	RW	1	<b>USB2.0 EHCI Debug Port Support</b> 0: Disable 1: Enable
3:2	RO	0	<b>Reserved</b>
1:0	RW	10b	<b>Squelch Detector Fine Tune</b>

**Offset Address: 4Dh (B0D16F4)**
**USB2.0 Pre-SOF Time Period Select**
**Default Value: 00h**

Bit	Attribute	Default	Description
4:3	RW	00h	<b>USB2.0 Pre-SOF Time Period Select</b> <b>There are 7500 T totally in one frame.</b> 00: Time period to next SOF is (150 T + MAXLEN) 01: Time period to next SOF is (300 T + MAXLEN) 10: Time period to next SOF is (500 T + MAXLEN) 11: Time period to next SOF is (800 T + MAXLEN)

**Offset Address: 50-4Eh (B0D16F4) - Reserved**
**Offset Address: 51h (B0D16F4)**
**USB 2.0 MAC Timeout Parameter**
**Default Value: 60h**

Bit	Attribute	Default	Description
7:0	RW	60h	<b>USB 2.0 Receive Timeout Parameter</b> The unit is byte time. According to the core spec, the host controller or a device expecting a response to a transmission must not timeout the transaction if the inter-packet delays in 736 and 816 bit times. The worst round trip delay is 721 bit times.

**Offset Address: 57-52h (B0D16F4) - Reserved**
**Offset Address: 58h (B0D16F4)**
**PHY Control 1**
**Default Value: 04h**

Bit	Attribute	Default	Description
7:2	RO	01h	<b>Reserved (Do Not Program)</b>
1:0	RW	0	<b>XCVR1.1 Slew Rate Control</b>

**Offset Address: 59h (B0D16F4) – Reserved**
**Offset Address: 5B-5Ah (B0D16F4)**
**High-Speed Port Pad Termination Resistor Fine Tune**
**Default Value: 8888h**

Bit	Attribute	Default	Description
15:8	RW	88h	<b>High-Speed Port Pad Termination Resistor Fine Tune (Port A &amp; B)</b>
7:0	RW	88h	<b>High-Speed Port Pad Termination Resistor Fine Tune (Port C &amp; D)</b>

**Offset Address: 5Ch (B0D16F4)**
**PHY Control 3**
**Default Value: 53h**

Bit	Attribute	Default	Description
7	RW	0	<b>DPLL Zero Phase Start Select</b> 0: ZPS takes 8-bit times to start 1: ZPS takes 4-bit times to start
6:4	RW	101b	<b>Delay DPLL Input Data Control</b>
3:2	RW	0	<b>DPLL Track Speed Select</b>
1:0	RW	11b	<b>DPLL Lock Speed Select</b>

**Offset Address: 5E-5Dh (B0D16F4)**
**High-Speed Port Pad Termination Resistor Fine Tune**
**Default Value: 8888h**

Bit	Attribute	Default	Description
15:8	RW	88h	<b>High-Speed Port Pad Termination Resistor Fine Tune (Port G &amp; H)</b>
1:0	RW	88h	<b>High-Speed Port Pad Termination Resistor Fine Tune (Port E &amp; F)</b>

**Offset Address: 5Fh (B0D16F4) – Reserved**
**Offset Address: 60h (B0D16F4)**
**Serial Bus Release Number**
**Default Value: 20h**

Bit	Attribute	Default	Description
7:0	RO	20h	<b>Serial Bus Release Number</b> Fixed at 20h for USB2.0

**Offset Address: 61h (B0D16F4)**
**Frame Length Adjustment**
**Default Value: 20h**

Bit	Attribute	Default	Description
7:6	RO	0	<b>Reserved</b>
5:0	RW	20h	<b>Frame Length Adjustment</b>

**Offset Address: 63-62h (B0D16F4)**
**Port Wake Capability**
**Default Value: 0001h**

Bit	Attribute	Default	Description
15:1	RW	00h	<b>Port Wake Capability</b> To support 8 Ports, [8:1] is RW and [15:9] is RO
0	RO	1b	<b>Port Wake Capability Implement</b> 0: Port Wake Capability is not Implemented 1: Port Wake Capability is Implemented

**Offset Address: 67-64h (B0D16F4) - Reserved**

**Offset Address: 6B-68h (B0D16F4)**

### **USB Legacy Support Extended Capability**

**Default Value:** 0000 0001h

Bit	Attribute	Default	Description
31:25	RO	0	<b>Reserved</b>
24	RW	0	<b>HC OS Owned Semaphore</b>
23:17	RO	0	<b>Reserved</b>
16	RW	0	<b>HC BIOS Owned Semaphore</b>
15:8	RO	0	<b>Next EHCI Extended Capability Pointer</b>
7:0	RO	01h	<b>Capability ID</b>

**Offset Address: 6F-6Ch (B0D16F4)**

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## **USB Legacy Support Control / Status**

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**Default Value:** 0000 0000h

Bit	Attribute	Default	Description
31:0	RO/RW/RW1C	0	<b>USB Legacy Support Control / Status</b> Reference EHCI Spec. for detail.

**Offset Address: 71-70h (B0D16F4)**

## **SRAM Direct Access Address**

**Default Value:** 0000h

Bit	Attribute	Default	Description
15:9	RO	0	<b>Reserved</b>
8:0	RW	0	<b>SRAM Direct Access Address</b> The valid address range of SRAM 0 and 1 is from 0h to 100h, SRAM 2 and 3 is from 0h to 80h.

### **Offset Address: 72h (B0D16F4) - Reserved**

**Offset Address: 73h (B0D16F4)**

## **SRAM Direct Access Control**

**Default Value:** 00h

**Offset Address: 77-74h (B0D16F4)**

SRAM Data

**Default Value:** 0000 0000h

<b>Bit</b>	<b>Attribute</b>	<b>Default</b>	<b>Description</b>
31:0	RW	0	<p><b>SRAM Data</b></p> <p>This 32 bit register stores read data from SRAM, or data to write. This register is also used by SRAM BIST logic as test pattern. It accesses all the three SRAMs with the specified pattern and its complement.</p>

**Offset Address: 7F-78h (B0D16F4) - Reserved**

**Offset Address: 80h (B0D16F4)**

## **Power Management Capability ID**

**Default Value:** 01h

Bit	Attribute	Default	Description
7:0	RO	01h	<b>Power Management Capability ID</b>

**Offset Address: 81h (B0D16F4)**
**Next Item Pointer**
**Default Value: 88h**

Bit	Attribute	Default	Description
7:0	RO	88h	<b>Next Item Pointer</b> If Rx4D[0] = 1, this register is fixed at 88h. If Rx4D[0] = 0, this register is fixed at 00h.

**Offset Address: 83-82h (B0D16F4)**
**Power Management Capability**
**Default Value: FFC2h**

Bit	Attribute	Default	Description
15:0	RO	FFC2h	<b>Power Management Capability</b> If D16F0 Rx49[1]= 1, this register is fixed at FFC2h. If D16F0 Rx49[1]= 0, this register is fixed at 7E0Ah.

**Offset Address: 85-84h (B0D16F4)**
**Power Management Capability Control / Status**
**Default Value: 0000h**

Bit	Attribute	Default	Description
15	RWC	0	<b>PME Status</b> 0: Not active 1: Active
14:9	RO	0	<b>Reserved</b>
8	RW	0	<b>PME Enable</b> 0: Disable 1: Enable
7:2	RO	0	<b>Reserved</b>
1:0	RW	00b	<b>Power State</b> 00: D0 01: D1 10: D2 11: D3 Hot

**Offset Address: 87-86h (B0D16F4) - Reserved**
**Offset Address: 88h (B0D16F4)**
**Next Item Pointer**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	<b>Next Item Pointer</b>

**Offset Address: 89h (B0D16F4)**
**Next Item Pointer 2**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	<b>Next Item Pointer 2</b>

**Offset Address: 8B-8Ah (B0D16F4)**
**Debug Port Base Offset**
**Default Value: 20A0h**

Bit	Attribute	Default	Description
15:0	RO	20A0h	<b>Debug Port Base Offset</b> If Rx4C[4] = 1, this register is fixed at 20A0h. If Rx4C[4] = 0, this register is fixed at 0000h.

**Offset Address: F4-8Ch (B0D16F4) – Reserved**

### EHCI USB 2.0 Memory I/O Registers

These registers are compliant with the EHCI v1.0 standard. Refer to the EHCI v1.0 specification for further details.

#### EHCI Capabilities (0-0Bh)

**Offset Address: 0h**

**Capability Register Length**

**Default Value: 10h**

Bit	Attribute	Default	Description
7:0	RO	10h	Capability Register Length

**Offset Address: 1h – Reserved**

**Offset Address: 3-2h**

**Interface Version Number**

**Default Value: 0100h**

Bit	Attribute	Default	Description
15:0	RO	0100h	Interface Version Number

**Offset Address: 7-4h**

**Structure Parameters**

**Default Value: 0010 4208h**

Bit	Attribute	Default	Description
31:0	RO	0010 4208h	<b>Structure Parameters</b> If D16F4 Rx4C[4] = 1, fixed at 0010 4208h. If D16F4 Rx4C[4] = 0, fixed at 0000 4208h.

**Offset Address: 0B-8h**

**Capability Parameters**

**Default Value: 0000 6872h**

Bit	Attribute	Default	Description
31:0	RO	0000 6872h	<b>Capability Parameters</b>

**Host Controller Operations (10-73h)**
**Offset Address: 13-10h**
**USB Command**
**Default Value: 0008 0000h**

Bit	Attribute	Default	Description
31:0	RW	0008 0000h	<b>USB Command</b>

**Offset Address: 17-14h**
**USB Status**
**Default Value: 0000 1000h**

Bit	Attribute	Default	Description
31:0	RW1C	0000 1000h	<b>USB Status</b>

**Offset Address: 1B-18h**
**USB Interrupt Enable**
**Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	<b>USB Interrupt Enable</b>

**Offset Address: 1F-1Ch**
**USB Frame Index**
**Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	<b>USB Frame Index</b>

**Offset Address: 23-20h**
**4G Segment Selector**
**Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	<b>4G Segment Selector</b>

**Offset Address: 27-24h**
**Frame List Base Address**
**Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	<b>Frame List Base Address</b>

**Offset Address: 2B-28h**
**Next Asynchronous List Address**
**Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	<b>Next Asynchronous List Address</b>

**Offset Address: 4F-2Ch – Reserved**
**Offset Address: 53-50h**
**Configured Flag Registers**
**Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	<b>Configured Flag Registers</b>

**Offset Address: 57-54h**
**Port 1 Status / Control**
**Default Value: 0000 3000h**

Bit	Attribute	Default	Description
31:0	RW1C	0000 3000h	Port 1 Status / Control

**Offset Address: 5B-58h**
**Port 2 Status / Control**
**Default Value: 0000 3000h**

Bit	Attribute	Default	Description
31:0	RW1C	0000 3000h	Port 2 Status / Control

**Offset Address: 5F-5Ch**
**Port 3 Status / Control**
**Default Value: 0000 3000h**

Bit	Attribute	Default	Description
31:0	RW1C	0000 3000h	Port 3 Status / Control

**Offset Address: 63-60h**
**Port 4 Status / Control**
**Default Value: 0000 3000h**

Bit	Attribute	Default	Description
31:0	RW1C	0000 3000h	Port 4 Status / Control

**Offset Address: 67-64h**
**Port 5 Status / Control**
**Default Value: 0000 3000h**

Bit	Attribute	Default	Description
31:0	RW1C	0000 3000h	Port 5 Status / Control

**Offset Address: 6B-68h**
**Port 6 Status / Control**
**Default Value: 0000 3000h**

Bit	Attribute	Default	Description
31:0	RW1C	0000 3000h	Port 6 Status / Control

**Offset Address: 6F-6Ch**
**Port 7 Status / Control**
**Default Value: 0000 3000h**

Bit	Attribute	Default	Description
31:0	RW1C	0000 3000h	Port 7 Status / Control

**Offset Address: 73-70h**
**Port 8 Status / Control**
**Default Value: 0000 3000h**

Bit	Attribute	Default	Description
31:0	RW1C	0000 3000h	Port 8 Status / Control

## Bus 0 Device 17 Function 0 (B0D17F0) - Bus Control and Power Management

All registers are located in the device 17 function 0 configuration space of the VT8237S South Bridge. These registers are accessed through PCI configuration mechanism #1 via I/O address 0CF8h / 0CFCh.

### PCI Configuration Space Header (0-3Fh)

#### Offset Address: 1-0h (B0D17F0)

**Vendor ID**

**Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	<b>Vendor ID</b>

#### Offset Address: 3-2h (B0D17F0)

**Device ID**

**Default Value: 3372h**

Bit	Attribute	Default	Description
15:0	RO	3372h	<b>Device ID</b>

#### Offset Address: 5-4h (B0D17F0)

**Command**

**Default Value: 0003h**

Bit	Attribute	Default	Description
15:7	RO	0	<b>Reserved</b>
6	RW	0	<b>Parity Error response</b> 0: Ignore parity error 1: Normal response
5:4	RO	0	<b>Reserved</b>
3	RO	0	<b>Special Cycle Enable</b> 0: Disable 1: Enable
2	RO	0	<b>Bus Master</b>
1	RW	1b	<b>Memory Space</b>
0	RW	1b	<b>I/O Space</b>

#### Offset Address: 7-6h (B0D17F0)

**Status**

**Default Value: 0210h**

Bit	Attribute	Default	Description
15	RO	0	<b>Detected Parity Error</b> Set only by the master when it detects a parity error.
14	RO	0	<b>Signaled System Error</b> Always reads 0.
13	RO	0	<b>Signaled Master Abort</b> Note: Set by master when it receives a target abort reset when writing 1.
12	RO	0	<b>Received Target Abort</b> Note: Set by master when it receives a target abort reset when writing 1.
11	RO	0	<b>Signaled Target Abort</b> Note: Set by target when it terminates a transaction with target abort reset when writing 1.
10:9	RO	01b	<b>DEVSEL# Timing</b> 00: Fast 01: Medium 10: Slow 11: Reserved Note: For target device only.
8	RO	0	<b>Data Parity Detected</b> Reads 1 if PERR# is asserted (driven or observed) or a bus master data parity error occurred.
7	RO	0	<b>Fast Back-to-Back Capable</b>
6:0	RO	10h	<b>Reserved (Do Not Program)</b>

Note: 1. These signals come from internal logic.

2. For these bits not supported or static, please hardwire to 0/1.

**Offset Address: 8h (B0D17F0)**
**Revision ID**
**Default Value:** nnh

Bit	Attribute	Default	Description
7:0	RO	nnh	<b>Revision ID</b>

**Offset Address: 0B-9h (B0D17F0)**
**Class Code**
**Default Value:** 06 0100h

Bit	Attribute	Default	Description
23:0	RO	06 0100h	<b>Class Code</b>

**Offset Address: 0Eh (B0D17F0)**
**Header Type**
**Default Value:** 80h

Bit	Attribute	Default	Description
7:0	RO	80h	<b>Header Type</b> Multifunction Device

**Offset Address: 2F-2Ch (B0D17F0)**
**Subsystem ID and Subsystem Vendor ID**
**Default Value:** 0000 0000h

Bit	Attribute	Default	Description
31:16	RO	0	<b>Subsystem ID</b> The read back value can be changed by writing to backdoor Rx72-73.
15:0	RO	0	<b>Subsystem Vendor ID</b> The read back value can be changed by writing to backdoor Rx70-71.

**Offset Address: 73-70h (B0D17F0)**
**Subsystem ID and Subsystem Vendor ID Back Door Registers**
**Default Value:** 0000 0000h

Bit	Attribute	Default	Description
31:16	RW	0	<b>Subsystem ID (Rx2E-2F) Back Door</b>
15:0	RW	0	<b>Subsystem Vendor ID (Rx2C-2D) Back Door</b>

**ISA Bus Control (40-49h)**
**Offset Address: 40h (B0D17F0)**
**ISA Bus Control**
**Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	<b>Extra / Normal ISA Command Delay</b> 0: Normal 1: External
6	RW	0	<b>I/O Recovery Time</b> 0: Disable 1: Enable
5	RO	0	<b>Reserved</b>
4	RW	0	<b>ROM Write</b> 0: Disable 1: Enable
3	RW	0	<b>Double DMA Clock</b> 0: Disable 1: Enable
2	RW	0	<b>4D0 / 4D1 Support</b> 0: Disable 1: Enable
1	RW	0	<b>DMA / Interrupt / Timer Shadow Register Read</b> 0: Disable 1: Enable
0	RW	0	<b>BCLK = PCLK/2</b> 0: Disable 1: Enable

**Offset Address: 41h (B0D17F0)**
**ROM Decode Control**
**Default Value: 80h**

Setting these bits to 1 enables the indicated address range to be included in the LPC BIOS ROM address decode:

Bit	Attribute	Default	Description
7	RW	1b	<b>000E0000 - 000FFFFF</b>
6	RW	0	<b>FFF0000h - FFF7FFFFh</b> <b>FFB0000h - FFB7FFFFh</b>
5	RW	0	<b>FFE8000h - FFEFFFFFFh</b> <b>FFA8000h - FFAFFFFFFh</b>
4	RW	0	<b>FFE0000h - FFE7FFFFh</b> <b>FFA0000h - FFA7FFFFh</b>
3	RW	0	<b>FFD8000h - FFDFFFFFh</b> <b>FF98000h - FF9FFFFh</b>
2	RW	0	<b>FFD0000h - FFD7FFFFh</b> <b>FF90000h - FF97FFFFh</b>
1	RW	0	<b>FFC8000h - FFCFFFFFFh</b> <b>FF88000h - FF87FFFFh</b>
0	RW	0	<b>FFC0000h - FFC7FFFFh</b> <b>FF80000h - FF87FFFFh</b>

Note: The following memory address range for ROM FFF80000-FFFFFFFFFF, FFB80000-FFBFFFFFF and 000F0000-000FFFFFF are decoded.

**Offset Address: 42h (B0D17F0)**
**Line Buffer Control**
**Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	<b>DMA Line Buffer</b> Controls whether the DMA line buffer is used. 0: Disable 1: Enable (Master DMA waits until the line buffer is full (8 DWords) before transmitting data (bit-6 must also be enabled to insure that there are no coherency issues).
6	RW	0	<b>Gate Interrupt Until Line Buffer Flush Complete</b> This bit should be enabled if bit-7 is enabled. 0: Disable 1: Enable INTR is gated until the line buffer is flushed to insure that there are no coherency issues.
5	RW	0	<b>Flush Line Buffer for Interrupt when DMA is not Granted</b> 0: Disable 1: Enable
4	RW	0	<b>Uninterruptible Burst Read</b> 0: Disable 1: Enable The PCI bus is not granted to DMA until burst read transactions from the north bridge are completed.
3	RW	0	<b>Gate IRQ Until Line Buffer Flush Completed</b> 0: Disable 1: Enable
2	RW	0	<b>IRQ Flush Line Buffer When Grant to DMA</b> Even if DMA is granted with Rx42[5]=1 0: Disable 1: Enable
1:0	RO	0	<b>Reserved</b>

**Offset Address: 43h (B0D17F0)**
**Delay Transaction Control**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	<b>Reserved</b>
3	RW	0	<b>Delayed Transactions (PCI Spec Rev 2.1)</b> This bit controls whether delayed transactions (delayed read / write and posted write) are enabled. 0: Disable 1: Enable
2	RW	0	<b>Only Posted Write</b> This bit controls whether posted write is enabled, as opposed to bit-3 which controls whether delayed read / write as well as posted write are enabled. 0: Disable 1: Enable
1	RW	0	<b>Write Delay Transaction Timeout Timer</b> When enabled, if a delayed transaction (write cycle only) is not retried after $2^{15}$ PCI clocks, the transaction is terminated. 0: Disable 1: Enable
0	RW	0	<b>Read Delay Transaction Timeout Timer</b> When enabled, if a delayed transaction (read cycle only) is not retried after $2^{15}$ PCI clocks, the transaction is terminated. 0: Disable 1: Enable

**Offset Address: 44h (B0D17F0)**
**PCI PNP Interrupt Routing INTE/F#**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	<b>PCI INTF# Routing (Refer to PnP IRQ Routing Table)</b>
3:0	RW	0	<b>PCI INTE# Routing (Refer to PnP IRQ Routing Table)</b>

**Offset Address: 45h (B0D17F0)**

## **PCI PNP Interrupt Routing INTG/H#**

**Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	PCI INTH# Routing (Refer to PnP IRQ Routing Table)
3:0	RW	0	PCI INTG# Routing (Refer to PnP IRQ Routing Table)

**Offset Address: 46h (B0D17F0)**

## **PCI INTE-F# Interrupt Control**

**Default Value: 00h**

Note: For routing control of PCI INTA#-INTD#, see Device 17 Function 0 Rx54-57 and Table 1 PnP IRQ Routing Table for reference

**Offset Address: 48h (B0D17F0)**
**Read Pass Write Control**
**Default Value: 0Ch**

Bit	Attribute	Default	Description
7	RW	0	<b>FSB Fixed at Low DW</b> 0: Disable (Address Bit-2 not masked) 1: Enable (force A2 from APIC FSB to low) Address bit A2 controls whether data is in the lower (0) or upper (1) doubleword of a quadword sent to the CPU. When this bit is enabled, A2 is masked which means it is always 0 to select the lower doubleword.
6:4	RO	0	<b>Reserved</b>
3	RW	1b	<b>LPC Read Pass Write</b> 0: Disable (a read cannot be performed before a preceding write has been completed) 1: Enable (internal LPC devices are allowed to perform a read before a preceding write)
2	RW	1b	<b>IDE Read Pass Write</b> 0: Disable (a read cannot be performed before a preceding write has been completed) 1: Enable (the internal IDE controller is allowed to perform a read before a preceding write)
1	RW	0	<b>USB Read Pass Write</b> 0: Disable (a read cannot be performed before a preceding write has been completed) 1: Enable (the internal USB controllers are allowed to perform a read before a preceding write)
0	RW	0	<b>NIC Read Pass Write</b> 0: Disable (a read cannot be performed before a preceding write has been completed) 1: Enable (the internal LAN controller is allowed to perform a read before a preceding write)

**Offset Address: 49h (B0D17F0)**
**SB Peripheral Device Control**
**Default Value: 20h**

Bit	Attribute	Default	Description
7	RW	0	<b>SERR on V-Link Bus Directed to PMU (SMI, SCI)</b> 0: Disable 1: Enable
6	RW	0	<b>South Bridge Internal Master Devices Priority Higher Than External PCI Master</b> 0: Disable 1: Enable Normally priority is the same for internal and external PCI master devices, but when this bit is enabled, internal master devices are given higher priority than external PCI masters (3/4 : 1/4).
5	RW	1b	<b>SB Peripheral Device clean to Mask Off IRQ</b> Controls whether interrupt requests are gated until data is written to memory. 0: Disable 1: Enable
4	RW	0	<b>PCIM Address Stepping</b> 0: Disable 1: Enable
3	RW	0	<b>PCIM Wait State</b> 0: Disable 1: Enable
2	RW	0	<b>WSC Mask Off INTR</b> Controls whether INTR is masked until write snoop is complete. 0: Disable 1: Enable
1:0	RO	0	<b>Reserved</b>

LPC Firmware Memory Control (4A-4Bh)
Offset Address: 4Ah (B0D17F0)
**LPC Firmware Memory Control 1**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RW	0	<b>LPC Firmware Memory Base Address A[23:17]</b>
0	RW	0	<b>LPC Firmware Memory Programmable IDSEL</b> 0: Disable 1: Enable

Offset Address: 4Bh (B0D17F0)
**LPC Firmware Memory Control 2**
**Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	<b>Reserved</b>
6:4	RW	000b	<b>LPC Firmware Memory Base Address Mask</b> Bit-6 = 1 to mask A19 decoding (Support 1024K FWH ROM size) Bit-5 = 1 to mask A18 decoding (Support 512K FWH ROM size) Bit-4 = 1 to mask A17 decoding (Support 256K FWH ROM size)
3:0	RW	0000b	<b>LPC Firmware Memory IDSEL Value</b> 0000: Address range decoded as ID select 0 0001: Address range decoded as ID select 1 1111: Address range decoded as ID select F

### Miscellaneous Control (4C-4Fh)

#### Offset Address: 4Ch (B0D17F0)

##### IDE Interrupt Select

**Default Value: 04h**

Bit	Attribute	Default	Description
7:6	RW	00b	<b>I/O Recovery Time Select</b> When D17F0 Rx40[6] is enabled, this field determines the I/O recovery time. 00: 1 Bus Clock 01: 2 Bus Clock 10: 4 Bus Clock 11: 8 Bus Clock
5:4	RO	0	<b>Reserved</b>
3:2	RW	01b	<b>IDE Secondary Channel IRQ Routing</b> 00: IRQ14 01: IRQ15 10: IRQ10 11: IRQ11
1:0	RW	00b	<b>IDE Primary Channel IRQ Routing</b> 00: IRQ14 01: IRQ15 10: IRQ10 11: IRQ11

Note: When the internal APIC is enabled, internal IRQ routing to the APIC is fixed as follows:

INTA# => IRQ16

INTB# and HD audio IRQ => IRQ17

INTC# => IRQ18

INTD# => IRQ19

IDE, USB0 IRQ and INTE# => IRQ20

SATA, USB2, EHCI IRQ and INTF# => IRQ21

USB1 IRQ and INTG# => IRQ22

USB3, LAN IRQ and INTH# => IRQ23

#### Offset Address: 4Dh (B0D17F0)

##### Miscellaneous Control

**Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	<b>LPC Firmware Memory 16 Bytes Burst Read</b> 0: Disable 1: Enable
6	RW	0	<b>LPC Firmware Memory 4 Bytes Burst Read / Write Access</b> 0: Disable 1: Enable
5	RW1	0	<b>Firmware Memory Burst Detection</b> Write 1 to start to detect the Firmware memory burst ability 0: Complete 1: Incomplete If the LPC Firmware memory support 16 byte burst, the Rx4D[7] will be set to 1 after burst detection complete. If the LPC Firmware memory support 4 byte burst, the Rx4D[6] will be set 1 after burst detection complete.
4	RW	0	<b>LPC Firmware Memory IDSEL Value</b> Firmware Memory IDSEL[3:0] is AD[31:28] when this register's bit 1=1 0: Disable 1: Enable
3	RW	0	<b>Enable Fixed Path of External Interrupt Delivery Mode Only in APIC Ch0 When Interrupt Controller Has Not Been Masked Yet</b> 0: Disable 1: Enable
2	RW	0	<b>Serial IRQs Always be Shared in APIC Mode</b> 0: Disable 1: Enable
1	RW	0	<b>LPC Memory Cycle Goes to LPC Firmware Memory Cycle</b> 0: Only ROM Cycle will be transferred to LPC firmware memory cycle 1: All memory cycle will be transferred to LPC firmware cycle
0	RW	0	<b>LPC TPM Function</b> 0: Disable 1: Enable

**Offset Address: 4Eh (B0D17F0)**
**Internal RTC Test Mode and Extra Feature Control**
**Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	<b>RTC High Bank Rx38-3F R/W Protect</b> 0: Disable (allow R/W) 1: Enable (Protect)
6	RW	0	<b>RTC Low Bank Rx38-3F R/W Protect</b> 0: Disable (allow R/W) 1: Enable (Protect)
5	RO	0	<b>Reserved</b>
4	RO	0	<b>Last Port 70/74 Written Status</b> 0: Last write was to port 70 1: Last write was to port 74
3	RW	0	<b>Extra RTC Port 74/75</b> The RTC is normally accessed through ports 70/74. This bit controls whether two extra ports (74 / 75) can be used to access the RTC. 0: Disable 1: Enable
2:0	RO	0	<b>Reserved</b>

**Offset Address: 4Fh (B0D17F0)**
**PCI Bus and CPU Interface Control**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:2	RO	0	<b>Reserved</b>
1	RW	0	<b>Reset External PCI Device Only</b> 0: All the devices will be reset. 1: USB controller in South Bridge will not be reset by software PCI Reset.
0	RW	0	<b>Software PCI Reset</b> Write 1 to generate PCI reset. Software reset also can be produced by writing I/O port CF9. Write 1 to I/O port CF9 bit2 to produce software reset. If CF9 bit 1 is 0, INIT will be produced. If I/O port CF9 bit 1 is 1, PCIRST will be produced. I/O port CF9 bit 1 default value is 1. 0: Disable 1: Enable

**Function Control (50-51h)**
**Offset Address: 50h (B0D17F0)**
**Function Control 1**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RO	0	<b>Reserved</b>
5	RW	0	<b>Device 16 Function 1 USB 2</b> 0: Enable 1: Disable
4	RW	0	<b>Device 16 Function 0 USB 1</b> 0: Enable 1: Disable
3	RW	0	<b>Device 15 Function 0 Serial ATA</b> 0: Enable 1: Disable
2	RW	0	<b>Device 16 Function 2 USB 3</b> 0: Enable 1: Disable
1	RW	0	<b>Device 16 Function 4 USB 5</b> 0: Enable 1: Disable
0	RW	0	<b>Device 16 Function 3 USB 4</b> 0: Enable 1: Disable

**Offset Address: 51h (B0D17F0)**
**Function Control 2**
**Default Value: 1Dh**

Bit	Attribute	Default	Description
7:6	RO	0	<b>Reserved</b>
5	RW	0	<b>Internal LAN Controller Clock Gating</b> When bit-4 of this register is disabled, the LAN function is disabled but the LAN controller clock is not gated automatically. This bit controls whether the clock is actually gated. 0: Disable 1: Enable
4	RW	1b	<b>Internal LAN Controller</b> 0: Disable 1: Enable
3	RW	1b	<b>Internal RTC</b> 0: Disable 1: Enable
2	RW	1b	<b>Internal PS2 Mouse</b> 0: Disable 1: Enable
1	RW	0	<b>Internal KBC Configuration</b> 0: Disable 1: Enable
0	RW	1b	<b>Internal Keyboard Controller</b> 0: Disable 1: Enable

Note:

Pin	External KBC	Internal KBC
V01	KBRC#	KBDT
W03	KA20G	KBCK
W02	IRQ12	MSDT
W01	IRQ1	MSCK

**Serial IRQ, LPC and PC / PCI DMA Control (52-53h)**
**Offset Address: 52h (B0D17F0)**
**Serial IRQ, PCI / DMA Control and LPC Control**
**Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	<b>Reserved</b>
6	RW	0	<b>LPC Short Wait Abort</b> 0: Disable 1: Enable. During a short wait, the cycle is aborted after 8Ts.
5	RW	0	<b>LPC Frame Wait State</b> 0: Disable 1: Enable
4	RW	0	<b>LPC Stop to Start Frame Wait State</b> 0: Disable. One idle state is inserted between Stop and Start. 1: Enable. Stop is followed immediately by Start.
3	RW	0	<b>Serial IRQ</b> 0: Disable. 1: Enable. (IRQ asserted via signal SERIRQ)
2	RW	0	<b>Serial IRQ Quiet Mode</b> 0: Continuous Mode 1: Quiet Mode
1:0	RW	00b	<b>Serial IRQ Start-Frame Width</b> 00: 4 PCI Clocks 10: 8 PCI Clocks 01: 6 PCI Clocks 11: 10 PCI Clocks

**Offset Address: 53h (B0D17F0)**
**PC / PCI DMA Control**
**Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	<b>Multiplexed Pin Selection for GPIO or PCI Request A</b> 0: AE05=GPIO24, AF05=GPIO30 1: AE05=PCREQA, AF05=PCGNTA
6	RW	0	<b>PCI DMA Channel 7</b> 0: Disable 1: Enable
5	RW	0	<b>PCI DMA Channel 6</b> 0: Disable 1: Enable
4	RW	0	<b>PCI DMA Channel 5</b> 0: Disable 1: Enable
3	RW	0	<b>PCI DMA Channel 3</b> 0: Disable 1: Enable
2	RW	0	<b>PCI DMA Channel 2</b> 0: Disable 1: Enable
1	RW	0	<b>PCI DMA Channel 1</b> 0: Disable 1: Enable
0	RW	0	<b>PCI DMA Channel 0</b> 0: Disable 1: Enable

**Plug and Play Control – PCI (54-57h)**
**Offset Address: 54h (B0D17F0)**
**PCI Bus and CPU Interface Control**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	<b>Reserved</b> The following bits all default to “Non-Invert” triggered (0).
3	RW	0	<b>PCI INTA# Invert / Non-Invert Trigger</b> 0: Non-Invert                           1: Invert
2	RW	0	<b>PCI INTB# Invert / Non-Invert Trigger</b> 0: Non-Invert                           1: Invert
1	RW	0	<b>PCI INTC# Invert / Non-Invert Trigger</b> 0: Non-Invert                           1: Invert
0	RW	0	<b>PCI INTD# Invert / Non-Invert Trigger</b> 0: Non-Invert                           1: Invert

Note: PCI INTA-D# normally connect to PCI interrupt pins INTA-D# (see pin definitions for more information).

**Offset Address: 55h (B0D17F0)**
**PCI PNP Interrupt Routing 1**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	<b>PCI INTA# Routing</b> (see “PnP IRQ Routing” table)
3:0	RO	0	<b>Reserved</b> Always reads 0.

**Offset Address: 56h (B0D17F0)**
**PCI PNP Interrupt Routing 2**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	<b>PCI INTC# Routing</b> (see “PnP IRQ Routing” table)
3:0	RW	0	<b>PCI INTB# Routing</b> (see “PnP IRQ Routing” table)

**Offset Address: 57h (B0D17F0)**
**PCI PNP Interrupt Routing 3**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	<b>PCI INTD# Routing</b> (see “PnP IRQ Routing” table)
3:0	RO	0	<b>Reserved</b> Always reads 0.

**Table 12. PnP IRQ Routing Table**

0000	Reserved
0001	IRQ1
0010	Reserved
0011	IRQ3
0100	IRQ4
0101	IRQ5
0110	IRQ6
0111	IRQ7
1000	Reserved
1001	IRQ9
1010	IRQ10
1011	IRQ11
1100	IRQ12
1101	Reserved
1110	IRQ14
1111	IRQ15

Note: When enable internal APIC, PCI devices and internal function IRQ routing as below:

INTA#	IRQ16
INTB# and HD audio IRQ	IRQ17
INTC#	IRQ18
INTD#	IRQ19
IDE, USB0 IRQ and INTE#	IRQ20
SATA, USB2, EHCI IRQ and INTF#	IRQ21
USB1 IRQ and INTG#	IRQ22
USB3, LAN IRQ and INTH#	IRQ23

**GPIO and Miscellaneous Control (58-5Bh)**
**Offset Address: 58h (B0D17F0)**
**Miscellaneous Control 1**
**Default Value: 20h**

Bit	Attribute	Default	Description
7	RW	0	<b>Multiplexed Pin Selection for GPIO or PCI Request B</b> 0: AD05 = GPIO25, AC06 = GPIO31      1: AD05 = PCREQB, AC06 = PCGNTB
6	RW	0	<b>Internal APIC</b> 0: Disable      1: Enable
5	RW	1b	<b>South Bridge Interrupt Cycles Run at 33 MHz</b> 0: Disable      1: Enable
4	RW	0	<b>South Bridge Decode</b> 0: Subtractive      1: Positive
3	RW	0	<b>RTC High Bank Access</b> 0: Disable      1: Enable
2	RW	0	<b>RTC Rx32 Write Protect</b> 0: Disable (not protected)      1: Enable (write protected)
1	RW	0	<b>RTC Rx0D Write Protect</b> 0: Disable (not protected)      1: Enable (write protected)
0	RW	0	<b>RTC Rx32 Map to Century Byte</b> Controls whether RTC Rx32 is mapped to the century byte. 0: Disable      1: Enable

**Offset Address: 59h (B0D17F0)**
**Miscellaneous Control 2**
**Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	<b>ROM Memory Cycles Go To LPC</b> 0: Disable (all memory cycles go to LPC) 1: Enable (only ROM memory cycles go to LPC)
6	RO	0	<b>Reserved</b>
5	RW	0	<b>LPC RTC</b> 0: Disable      1: Enable
4	RW	0	<b>LPC Keyboard</b> 0: Disable (ISA Keyboard)      1: Enable (LPC Keyboard)
3	RW	0	<b>Port 62h / 66h (MCCS#) to LPC</b> 0: Disable      1: Enable
2	RW	0	<b>Port 62h / 66h (MCCS#) Decoding</b> 0: Disable      1: Enable
1	RW	0	<b>Mask A20M# Active</b> 0: Disable (A20M# act normally)      1: Enable (A20M# signal de-asserted)
0	RW	0	<b>NMI on PCI Parity Error</b> 0: Disable 1: Enable (to generate NMI, Port 61bit [3] and Port 70 bit [7] must also be set)

Note: To produce NMI correctly, port 61 [3] must be set to 0 and port 70 bit [7] must be set to 0 since Data parity error report is combined with IOCHK.

**Offset Address: 5Ah (B0D17F0)**
**DMA Bandwidth Control**
**Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	<b>DMA Channel 7 Bandwidth</b> 0: Normal 1:Improved
6	RW	0	<b>DMA Channel 6 Bandwidth</b> 0: Normal 1:Improved
5	RW	0	<b>DMA Channel 5 Bandwidth</b> 0: Normal 1:Improved
4	RW	0	<b>DMA Single Transfer Mode Bandwidth</b> 0: Normal 1:Improved
3	RW	0	<b>DMA Channel 3 Bandwidth</b> 0: Normal 1:Improved
2	RW	0	<b>DMA Channel 2 Bandwidth</b> 0: Normal 1:Improved
1	RW	0	<b>DMA Channel 1 Bandwidth</b> 0: Normal 1:Improved
0	RW	0	<b>DMA Channel 0 Bandwidth</b> 0: Normal 1:Improved

Note: The above bits determine if DMA bandwidth is improved for the specified channel. If enabled, bandwidth improvement is accomplished by reducing the transaction latency between the DMA Controller and the LPC Bus Controller.

**Offset Address: 5Bh (B0D17F0)**
**Miscellaneous Control 3**
**Default Value: 01h**

Bit	Attribute	Default	Description
7	RW	0	<b>LPC Firmware Memory Read TRDY 1 Wait State</b> 0: Disable 1: Enable
6	RW	0	<b>Destination Control for IO Port 0x80</b> 0: IO Port 0x80 goes to ISA Bus 1: IO Port 0x80 goes to LPC Bus
5	RW	0	<b>PCI/DMA Memory Cycles Output to PCI Bus</b> 0: Disable 1: Enable
4	RO	0	<b>Reserved</b>
3	RW	0	<b>Bypass APIC De-Assert Message</b> 0: Disable 1: Enable
2	RW	0	<b>APIC LDT Mode</b> 0: Disable 1: Enable
1	RW	0	<b>Multiplexed Pin Selection for INTE# -INTH# or GPI12-15</b> 0: GPI12-15 1: INTE#-INTH#
0	RW	1b	<b>Dynamic Clock Stop</b> 0: Disable 1: Enable

**Programmable Chip Select Control (5D-66h)**
**Offset Address: 5D-5Ch (B0D17F0)**
**PCS 0 I/O Port Address**
**Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW	0	<b>PCS 0 I/O Port Address</b>

**Offset Address: 5F-5Eh (B0D17F0)**
**PCS 1 I/O Port Address**
**Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW	0	<b>PCS 1 I/O Port Address</b>

**Offset Address: 61-60h (B0D17F0)**
**PCS 2 I/O Port Address**
**Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW	0	<b>PCS 2 I/O Port Address</b>

**Offset Address: 63-62h (B0D17F0)**
**PCS 3 I/O Port Address**
**Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW	0	<b>PCS 3 I/O Port Address</b>

**Offset Address: 65-64h (B0D17F0)**
**PCS I/O Port Address Mask**
**Default Value: 0000h**

Bit	Attribute	Default	Description
15:12	RW	0000b	<b>PCS 3 I/O Port Address Mask 3-0</b> 0000: Decode range is 1 byte 0011: Decode range is 4 bytes 1111: Decode range is 16 bytes 0001: Decode range is 2 bytes 0111: Decode range is 8 bytes
11:8	RW	0000b	<b>PCS 2 I/O Port Address Mask 3-0</b> 0000: Decode range is 1 byte 0011: Decode range is 4 bytes 1111: Decode range is 16 bytes 0001: Decode range is 2 bytes 0111: Decode range is 8 bytes
7:4	RW	0000b	<b>PCS 1 I/O Port Address Mask 3-0</b> 0000: Decode range is 1 byte 0011: Decode range is 4 bytes 1111: Decode range is 16 bytes 0001: Decode range is 2 bytes 0111: Decode range is 8 bytes
3:0	RW	0000b	<b>PCS 0 I/O Port Address Mask 3-0</b> 0000: Decode range is 1 byte 0011: Decode range is 4 bytes 1111: Decode range is 16 bytes 0001: Decode range is 2 bytes 0111: Decode range is 8 bytes

**Offset Address: 66h (B0D17F0)**
**PCS Control**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	<b>Reserved</b>
3	RW	0	<b>PCS 3</b> 0: Disable 1: Enable
2	RW	0	<b>PCS 2</b> 0: Disable 1: Enable
1	RW	0	<b>PCS 1</b> 0: Disable 1: Enable
0	RW	0	<b>PCS 0</b> 0: Disable 1: Enable

**Output Control (67h)**
**Offset Address: 67h (B0D17F0)**
**Output Control**
**Default Value: 04h**

Bit	Attribute	Default	Description
7	RW	0	<b>LPC PCS3</b> 0: Disable 1: Enable (PCS3 is on LPC bus)
6	RW	0	<b>LPC PCS2</b> 0: Disable 1: Enable (PCS2 is on LPC bus)
5	RW	0	<b>LPC PCS1</b> 0: Disable 1: Enable (PCS1 is on LPC bus)
4	RW	0	<b>LPC PCS0</b> 0: Disable 1: Enable (PCS0 is on LPC bus)
3	RO	0	<b>Reserved</b>
2	RW	1b	<b>FERR Voltage</b> 0: 2.5V 1: 1.5V
1:0	RW	0	<b>IDE Pad Driving Select</b>

**High Precision Event Timers (HPET) (68-6Bh)**
**Offset Address: 68h (B0D17F0)**
**HPET Control**
**Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	<b>High Precision Event Timers</b> 0: Disable 1: Enable
6:0	RO	0	<b>Reserved</b> Always reads 0.

**Offset Address: 6B-69h (B0D17F0)**
**HPET Control**
**Default Value: 00 0000h**

Bit	Attribute	Default	Description
23:2	RW	0	<b>HPET Memory Base Address [31:10]</b>
1:0	RO	0	<b>Reserved</b>

**ISA Decoding Control (6C-6Fh)**
**Offset Address: 6Ch (B0D17F0)**
**ISA Positive Decoding Control 1**
**Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	<b>On-Board I/O (Ports 00-FFh) Positive Decoding</b> 0: Disable 1: Enable
6	RW	0	<b>Microsoft-Sound System I/O Port Positive Decoding</b> 0: Disable 1: Enable (bits 5-4 determine the decode range)
5:4	RW	00b	<b>Microsoft Sound System I/O Decode Range</b> 00: 0530h-0537h 01: 0604h-060Bh 10: 0E80-0E87h 11: 0F40h-0F47h
3	RW	0	<b>APIC Positive Decoding</b> 0: Disable 1: Enable
2	RW	0	<b>ROM Positive Decoding</b> 0: Disable 1: Enable
1	RW	0	<b>PCS1# Positive Decoding</b> 0: Disable 1: Enable
0	RW	0	<b>PCS0# Positive Decoding</b> 0: Disable 1: Enable

**Offset Address: 6Dh (B0D17F0)**
**ISA Positive Decoding Control 2**
**Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	<b>FDC Positive Decoding</b> 0: Disable 1: Enable
6	RW	0	<b>LPT Positive Decoding</b> 0: Disable 1: Enable
5:4	RW	00b	<b>LPT Decode Range</b> 00: 3BCh-3BFh, 7BCh-7Beh 01: 378h-37Fh, 778h-77Ah 10: 278h-27Fh, 678h-67Ah 11: Reserved
3	RW	0	<b>Game Port Positive Decoding</b> 0: Disable 1: Enable
2	RW	0	<b>MIDI Positive Decoding</b> 0: Disable 1: Enable
1:0	RW	00b	<b>MIDI Decode Range</b> 00: 300-303h 01: 310-313h 10: 320-323h 11: 330-333h

**Offset Address: 6Eh (B0D17F0)**
**ISA Positive Decoding Control 3**
**Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	<b>COM Port B Positive Decoding</b> 0: Disable 1: Enable
6:4	RW	000b	<b>COM-Port B Decode Range</b> 000: 3F8h-3FFh (COM1) 010: 220h-227h 100: 238h-23Fh 110: 338h-33Fh 001: 2F8h-2FFh (COM2) 011: 228h-22Fh 101: 2E8h-2EFh (COM4) 111: 3E8h-3EFh (COM3)
3	RW	0	<b>COM Port A Positive Decoding</b> 0: Disable 1: Enable
2:0	RW	000b	<b>COM-Port A Decode Range</b> 000: 3F8h-3FFh (COM1) 010: 220h-227h 100: 238h-23Fh 110: 338h-33Fh 001: 2F8h-2FFh (COM2) 011: 228h-22Fh 101: 2E8h-2EFh (COM4) 111: 3E8h-3EfH (COM3)

**Offset Address: 6Fh (B0D17F0)**
**ISA Positive Decoding Control 4**
**Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	<b>Reserved</b>
6	RW	0	<b>LPC TPM Positive Decoding</b> 0: Disable 1: Enable
5	RW	0	<b>PCS2# and PCS3# Positive Decoding</b> 0: Disable 1: Enable
4	RW	0	<b>I/O Port CF9h Positive Decoding</b> 0: Disable 1: Enable
3	RW	0	<b>FDC Decoding Range</b> 0: Primary 1: Secondary
2	RW	0	<b>Sound Blaster Positive Decoding</b> 0: Disable 1: Enable
1:0	RW	00b	<b>Sound Blaster Decode Range</b> 00: 220-22F, 230-233h 10: 260-26F, 270-273h, 01: 240-24F, 250-253h 11: 280-28F, 290-293h

**PCI I/O Cycle Control (70h-7Fh)**
**Offset Address: 70-74h (B0D17F0) – Reserved**
**Offset Address: 75h (B0D17F0)**
**ROM Memory Address Range**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	<b>Programmable Firmware Memory IDSEL for All Memory Range When Rx4D[1] = 1</b>
3	RW	0	<b>ROM Memory Address Range</b> FF700000-FF7FFFFF FF300000-FF3FFFFF
2	RW	0	<b>ROM Memory Address Range</b> FF600000-FF6FFFFF FF200000-FF2FFFFF
1	RW	0	<b>ROM Memory Address Range</b> FF500000-FF5FFFFF FF100000-FF1FFFFF
0	RW	0	<b>ROM Memory Address Range</b> FF400000-FF4FFFFF FF000000-FF0FFFFF

**Offset Address: 76h (B0D17F0)**
**ROM Memory Address Range**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	<b>Programmable Firmware Memory IDSEL for the Following two 1MB Memory Range</b> FF500000-FF5FFFFF FF100000-FF1FFFFF
3:0	RW	0	<b>Programmable Firmware Memory IDSEL for the Following two 1MB Memory Range</b> FF400000-FF4FFFFF FF000000-FF0FFFFF

**Offset Address: 77h (B0D17F0)**
**ROM Memory Address Range**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	<b>Programmable Firmware Memory IDSEL for the Following two 1MB Memory Range</b> FF700000-FF7FFFFF FF300000-FF3FFFFF
3:0	RW	0	<b>Programmable Firmware Memory IDSEL for the Following two 1MB Memory Range</b> FF600000-FF6FFFFF FF200000-FF2FFFFF

**Offset Address: 78-7B (B0D17F0) - Reserved**

**Offset Address: 7Ch (B0D17F0)**
**ROM Memory Address Range 1**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	<b>Programmable Firmware Memory IDSEL for the Following Two 512K Memory Range</b> FFC80000-FFCFFFFF FF880000-FF8FFFFFF
3:0	RW	0	<b>Programmable Firmware Memory IDSEL for the Following Two 512K Memory Range</b> FFC00000-FFC7FFFF FF800000-FF87FFFF

**Offset Address: 7Dh (B0D17F0)**
**ROM Memory Address Range 2**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	<b>Programmable Firmware Memory IDSEL for the Following Two 512K Memory Range</b> FFD80000-FFDFFFFFF FF980000-FF9FFFFFF
3:0	RW	0	<b>Programmable Firmware Memory IDSEL for the Following Two 512K Memory Range</b> FFD00000-FFD7FFFF FF900000-FF97FFFF

**Offset Address: 7Eh (B0D17F0)**
**ROM Memory Address Range 3**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	<b>Programmable Firmware Memory IDSEL for the Following Two 512K Memory Range</b> FFE80000-FFEFFFFFF FFA80000-FFAFFFFFF
3:0	RW	0	<b>Programmable Firmware Memory IDSEL for the Following Two 512K Memory Range</b> FFE00000-FFE7FFFF FFA00000-FFA7FFFF

**Offset Address: 7Fh (B0D17F0)**
**ROM Memory Address Range 4**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	<b>Programmable Firmware Memory IDSEL for the Following Two 512K Memory Range</b> FFF80000-FFFFFFFFFF FFB80000-FFBFFFFFF 000E0000-000FFFFF
3:0	RW	0	<b>Programmable Firmware Memory IDSEL for the Following Two 512K Memory Range</b> FFF00000-FFF7FFFF FFB00000-FFB7FFFF

**Power Management-Specific Configuration Registers (80-C7h)**
**Offset Address: 80h (B0D17F0)**
**General Configuration 1**
**Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	<b>Reserved</b> Always reads 0.
6	RW	0	<b>GP19 (UDPWR) as SLPBTN#</b> 0: Disable 1: Enable
5	RW	0	<b>Debounce</b> 0: Disable 1: Enable
4	RO	0	<b>Reserved</b> Always reads 0.
3	RW	0	<b>Microsoft Sound Monitor in Audio Access</b> This bit controls whether an I/O access to the sound port sets PMIO Rx33-30[10] = 1. 0: Disable 1: Enable
2	RW	0	<b>Game Port Monitor in Audio Access</b> This bit controls whether an I/O access to the game port sets PMIO Rx33-30[10] = 1. 0: Disable 1: Enable
1	RW	0	<b>Sound Blaster Monitor in Audio Access</b> This bit controls whether an I/O access to the sound blaster port sets PMIO Rx33-30[10] = 1. 0: Disable 1: Enable
0	RW	0	<b>MIDI Monitor in Audio Access</b> This bit controls whether an I/O access to the MIDI port sets PMIO Rx33-30[10] = 1. 0: Disable 1: Enable

**Offset Address: 81h (B0D17F0)**
**General Configuration 1**
**Default Value: 04h**

Bit	Attribute	Default	Description
7	RW	0	<b>ACPI I/O Enable</b> 0: Disable access to ACPI I/O block 1: Allow access to Power Management I/O Register Block (see offset 4B-48 to set the base address for this register block). The definitions of the registers in the Power Management I/O Register Block are included later in this document, following the Power Management Subsystem overview.
6:4	RO	0	<b>Reserved</b>
3	RW	0	<b>ACPI Timer with 32 Bit Width</b>
2	RW	1b	<b>RTC Enable Signal Gated with PSON (SUSC#) in Soft-Off Mode</b> This bit controls whether RTC control signals are gated during system suspend state. This is to prevent CMOS and Power-Well register data from being corrupted during system on/off when the control signals (PWRGD) may not be stable. 0: Disable 1: Enable
1	RW	0	<b>Clock Throttling Clock Select (STPCLK#)</b> This bit controls the timer tick base for the throttle timer. 0: 30 usec (480 usec cycle time when using a 4-bit timer) 1: 1 msec (16 msec cycle time when using a 4-bit timer)  The timer tick base can be further lowered to 7.5 usec (120 usec cycle time when using a 4-bit timer) by setting Rx8D[4] = 1. When Rx8D[4] = 1, the setting of this bit is ignored.
0	RO	0	<b>Reserved</b>

**Offset Address: 82h (B0D17F0)**
**ACPI Interrupt Select**
**Default Value: 40h**

Bit	Attribute	Default	Description
7	RO	0	<b>ATX / AT Power Indicator</b> 0: ATX 1: AT
6	RO	1b	<b>PSON (SUSC#) Current State</b> During system on/off, this status bit reports whether PSON gating state has been completed. 0 means that gating is active now and 1 means that gating is complete. Software should not access any CMOS or Power-Well registers until this bit becomes 1 if Rx81[2] = 1 (see register description on previous page). 0: PSON Gating Active 1: PSON Gating Complete
5	RO	0	<b>Reserved</b> Always reads 0.
4	RO	0	<b>SUSC# AC-Power-On Default Value</b> This bit is written at RTC Index 0D bit-7. If this bit is 0, the system is configured to “default on” when power is connected.
3:0	RW	0000b	<b>ACPI IRQ Select</b> This field determines the routing of the ACPI IRQ. 0000: Disabled 0001: IRQ1 0010: Reserved 0011: IRQ3 0100: IRQ4 0101: IRQ5 0110: IRQ6 0111: IRQ7 1000: IRQ8 1001: IRQ9 1010: IRQ10 1011: IRQ11 1100: IRQ12 1101: IRQ13 1110: IRQ14 1111: IRQ15

**Offset Address: 83h (B0D17F0) - Reserved**

**Offset Address: 85-84h (B0D17F0)**
**IRQn as Primary Interrupt**
**Default Value: 0000h**

If a device IRQ is enabled as a Primary IRQ, that device's IRQ can be used to generate wake events. The bits in this register are used in conjunction with:

D17F0 PMIO Rx28[7] – Primary Resume Status

D17F0 PMIO Rx2A[7] – Primary Resume Enable

If a device on one of the IRQ's is set to enable the Primary Interrupt, once the device generates an IRQ, the D17F0 PMIO Rx28[7] status bit will become 1 to report the occurrence of the Primary IRQ. If PMIO Rx2A[7] is set to 1 to enable Resume-on-Primary-IRQ, the IRQ then becomes a wake event.

Bit	Attribute	Default	Description
15	RW	0	<b>IRQ15 as Primary Interrupt Channel</b> 0: Disable 1: Enable
14	RW	0	<b>IRQ14 as Primary Interrupt Channel</b> 0: Disable 1: Enable
13	RW	0	<b>IRQ13 as Primary Interrupt Channel</b> 0: Disable 1: Enable
12	RW	0	<b>IRQ12 as Primary Interrupt Channel</b> 0: Disable 1: Enable
11	RW	0	<b>IRQ11 as Primary Interrupt Channel</b> 0: Disable 1: Enable
10	RW	0	<b>IRQ10 as Primary Interrupt Channel</b> 0: Disable 1: Enable
9	RW	0	<b>IRQ9 as Primary Interrupt Channel</b> 0: Disable 1: Enable
8	RW	0	<b>IRQ8 as Primary Interrupt Channel</b> 0: Disable 1: Enable
7	RW	0	<b>IRQ7 as Primary Interrupt Channel</b> 0: Disable 1: Enable
6	RW	0	<b>IRQ6 as Primary Interrupt Channel</b> 0: Disable 1: Enable
5	RW	0	<b>IRQ5 as Primary Interrupt Channel</b> 0: Disable 1: Enable
4	RW	0	<b>IRQ4 as Primary Interrupt Channel</b> 0: Disable 1: Enable
3	RW	0	<b>IRQ3 as Primary Interrupt Channel</b> 0: Disable 1: Enable
2	RO	0	<b>Reserved</b> Always reads 0.
1	RW	0	<b>IRQ1 as Primary Interrupt Channel</b> 0: Disable 1: Enable
0	RW	0	<b>IRQ0 as Primary Interrupt Channel</b> 0: Disable 1: Enable

**Offset Address: 87-86h (B0D17F0)**
**IRQn as Secondary Interrupt**
**Default Value: 0000h**

For legacy PMU, the bits in this register are used in conjunction with:  
 D17F0 PMIO Rx28[1] – Secondary Event Timer Timeout Status  
 D17F0 PMIO Rx2A[1] – SMI on Secondary Event Timer Timeout

Secondary IRQ's are different from Primary IRQ's in that systems that resume due to a Secondary IRQ can return directly to suspend state after the secondary event timer times out. For this to work, D17F0 PMIO Rx2A[1] needs to be set to one to enable SMI-on-Secondary-Event-Timer-Timeout (when PMIO Rx28[1] = 1). The timer's count value can be set via Rx93-90[27-26].

Bit	Attribute	Default	Description
15	RW	0	<b>IRQ15 as Secondary Interrupt Channel</b> 0: Disable 1:Enable
14	RW	0	<b>IRQ14 as Secondary Interrupt Channel</b> 0: Disable 1:Enable
13	RW	0	<b>IRQ13 as Secondary Interrupt Channel</b> 0: Disable 1:Enable
12	RW	0	<b>IRQ12 as Secondary Interrupt Channel</b> 0: Disable 1:Enable
11	RW	0	<b>IRQ11 as Secondary Interrupt Channel</b> 0: Disable 1:Enable
10	RW	0	<b>IRQ10 as Secondary Interrupt Channel</b> 0: Disable 1:Enable
9	RW	0	<b>IRQ9 as Secondary Interrupt Channel</b> 0: Disable 1:Enable
8	RW	0	<b>IRQ8 as Secondary Interrupt Channel</b> 0: Disable 1:Enable
7	RW	0	<b>IRQ7 as Secondary Interrupt Channel</b> 0: Disable 1:Enable
6	RW	0	<b>IRQ6 as Secondary Interrupt Channel</b> 0: Disable 1:Enable
5	RW	0	<b>IRQ5 as Secondary Interrupt Channel</b> 0: Disable 1:Enable
4	RW	0	<b>IRQ4 as Secondary Interrupt Channel</b> 0: Disable 1:Enable
3	RW	0	<b>IRQ3 as Secondary Interrupt Channel</b> 0: Disable 1:Enable
2	RO	0	<b>Reserved</b> Always reads 0.
1	RW	0	<b>IRQ1 as Secondary Interrupt Channel</b> 0: Disable 1:Enable
0	RW	0	<b>IRQ0 as Secondary Interrupt Channel</b> 0: Disable 1:Enable

**Offset Address: 89-88h (B0D17F0)**
**Power Management I/O Base**
**Default Value: 0001h**

Bit	Attribute	Default	Description
15:7	RW	00h	<b>ACPI IO Base Register</b>
6:0	RO	01h	<b>Hardwire to 01h.</b>

**Offset Address: 8Ah (B0D17F0)**
**Dynamically Switching Processor Power State**
**Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	<b>Reserved</b>
6	RW	0	Enable K8 New C3
5	RW	0	Extend Arbiter Enable during Popup / Popdown Mode
4	RW	0	<b>Down C3 or C4 Mode Enable (C2 to C3/C4)</b> This bit is used in conjunction with bit 3. If bit 3 is 0, this bit must be 0. 0: Will not attempt to automatically return to a previous C3 or C4 state. 1: Observes that there are no bus master activities, it can return to a previous C3 or C4 state.
3	RW	0	<b>Up C2 Mode Enable (C3/C4 to C2)</b> 0: Will treat Bus Master traffic as a break event and will return from C3/C4 to C0 based on a break event. 1: Observes a bus master request; it will take the system from a C3 or C4 state to a C2 state and auto enable Bus Masters. This will let snoops and memory access occurs.
2	RW	0	<b>Bus Master Status Report</b> 0: Sets D17F0 PMIO Rx0[4] if there is bus master activity. 1: Will not set the PMIO Rx0[4] if there is bus master activity. Note: 1. It is expected that if bit 3 is set, bit 2 should also be set. 2. PMIO Rx0[4] will be set by LPC DMA or LPC masters even if this bit is set.
1:0	RO	0	<b>Reserved</b> Always reads 0.

**Offset Address: 8Ch (B0D17F0)**
**Host Bus Power Management Control**
**Default Value: 07h**

Bit	Attribute	Default	Description																																																																				
7:4	RW	0	<b>Thermal Duty Cycle</b> This field determines the duty cycle of STPCLK# when the THRM# pin is asserted. The STPCLK# duty cycle when THRM# is NOT asserted is controlled by D17F0 PMIO Rx10[3:0]. The duty cycle indicates the percentage of performance (the lower the percentage, the lower the performance and the higher the power savings). If the Throttling Timer Width (D17F0 Rx8D[6:5]) is set to 3-bit width, bit-0 of this field should be set to 0 (and the performance increment will be 12.5%). If the Throttling Timer Width is set to 2-bit width, bits 1-0 of this field should be set to 0 (and the performance increment will be 25%).																																																																				
			<b>Throttling Timer Width</b> <table border="1"> <thead> <tr> <th></th> <th>4-Bit</th> <th>3-Bit</th> <th>2-Bit</th> </tr> </thead> <tbody> <tr><td>0000</td><td>Reserved</td><td>Reserved</td><td>Reserved</td></tr> <tr><td>0001</td><td>6.25%</td><td>Reserved</td><td>Reserved</td></tr> <tr><td>0010</td><td>12.50%</td><td>12.50%</td><td>Reserved</td></tr> <tr><td>0011</td><td>18.75%</td><td>Reserved</td><td>Reserved</td></tr> <tr><td>0100</td><td>25.00%</td><td>25.00%</td><td>25.00%</td></tr> <tr><td>0101</td><td>31.25%</td><td>Reserved</td><td>Reserved</td></tr> <tr><td>0110</td><td>37.50%</td><td>37.50%</td><td>Reserved</td></tr> <tr><td>0111</td><td>43.75%</td><td>Reserved</td><td>Reserved</td></tr> <tr><td>1000</td><td>50.00%</td><td>50.00%</td><td>50.00%</td></tr> <tr><td>1001</td><td>56.25%</td><td>Reserved</td><td>Reserved</td></tr> <tr><td>1010</td><td>62.50%</td><td>62.50%</td><td>Reserved</td></tr> <tr><td>1011</td><td>68.75%</td><td>Reserved</td><td>Reserved</td></tr> <tr><td>1100</td><td>75.00%</td><td>75.00%</td><td>75.00%</td></tr> <tr><td>1101</td><td>81.25%</td><td>Reserved</td><td>Reserved</td></tr> <tr><td>1110</td><td>87.50%</td><td>87.50%</td><td>Reserved</td></tr> <tr><td>1111</td><td>93.75%</td><td>Reserved</td><td>Reserved</td></tr> </tbody> </table>		4-Bit	3-Bit	2-Bit	0000	Reserved	Reserved	Reserved	0001	6.25%	Reserved	Reserved	0010	12.50%	12.50%	Reserved	0011	18.75%	Reserved	Reserved	0100	25.00%	25.00%	25.00%	0101	31.25%	Reserved	Reserved	0110	37.50%	37.50%	Reserved	0111	43.75%	Reserved	Reserved	1000	50.00%	50.00%	50.00%	1001	56.25%	Reserved	Reserved	1010	62.50%	62.50%	Reserved	1011	68.75%	Reserved	Reserved	1100	75.00%	75.00%	75.00%	1101	81.25%	Reserved	Reserved	1110	87.50%	87.50%	Reserved	1111	93.75%	Reserved	Reserved
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3	RW	0	<b>THRM# Enable</b> 0: Disable 1: Enable																																																																				
2	RW	1b	<b>Processor Break Event</b> 0: Disable 1: Enable																																																																				
1	RW	1b	<b>Disable C3 Auto Master Gating</b>																																																																				
0	RW	1b	<b>Enable VID/FID Change as a Break Event</b>																																																																				

### **Offset Address: 8Dh (B0D17F0)**

## **Throttle / Clock Stop Control**

**Default Value: 00h**

**Offset Address: 93-90h (B0D17F0)**
**GP Timer Control**
**Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:30	RW	00b	<b>Conserve Mode Timer Count Value</b> 00: 1/16 second 10: 1 second 01: 1/8 second 11: 1 minute
29	W1C	0	<b>Conserve Mode Status</b> This bit reads 1 when in Conserve Mode
28	RW	0	<b>Conserve Mode</b> This bit controls whether conserve mode (throttling) is enabled. When this bit is set, the system can enter conserve mode when primary activity is not detected within a given time period (determined by bits 31-30 of this register). Primary activity is defined in D17F0 PMIO Rx33-30. 0: Disable 1: Enable
27:26	RW	00b	<b>Secondary Event Timer Count Value</b> 00: 2 milliseconds 10: ½ second 01: 64 milliseconds 11: by EOI + 0.25 milliseconds
25	W1C	0	<b>Secondary Event Occurred Status</b> This bit reads 1 to indicate that a secondary event has occurred (to resume the system from suspend) and the secondary event timer is counting down.
24	RW	0	<b>Secondary Event Timer Enable</b> 0: Disable 1: Enable
23:16	RO/WO	0	<b>GP1 Timer Count Value</b> (base defined by bits 5-4) Write to load count value; Read to get current count
15:8	RO/WO	0	<b>GP0 Timer Count Value</b> (base defined by bits 1-0) Write to load count value; Read to get current count
7	RW	0	<b>GP1 Timer Start</b> On setting this bit to 1, the GP1 timer loads the value defined by bits 23-16 of this register and starts counting down. The GP1 timer is reloaded at the occurrence of certain peripheral events enabled in the GP Timer Reload Enable Register (D17F0 PMIO Rx38). If no such event occurs and the GP1 timer counts down to zero, then the GP1 Timer Timeout Status bit PMIO Rx28[3] is set to one. Additionally, if the GP1 Timer Timeout Enable bit PMIO Rx2A[3] is set, then an SMI is generated.
6	RW	0	<b>GP1 Timer Automatic Reload</b> 0: GP1 Timer stops at 0 1: Reload GP1 timer automatically after counting down to 0
5:4	RW	00b	<b>GP1 Timer Tick Select</b> 00: Disable 10: 1 second 01: 1/16 second 11: 1 minute
3	RW	0	<b>GP0 Timer Start</b> On setting this bit to 1, the GP0 timer loads the value defined by bits 15-8 of this register and starts counting down. The GP0 timer is reloaded at the occurrence of certain peripheral events enabled in the GP Timer Reload Enable Register (D17F0 PMIO Rx38). If no such event occurs and the GP0 timer counts down to zero, then the GP0 Timer Timeout Status bit in PMIO Rx28[2] is set to one. Additionally, if the GP0 Timer Timeout Enable bit PMIO Rx2A[2] is set, then an SMI is generated.
2	RW	0	<b>GP0 Timer Automatic Reload</b> 0: GP0 Timer stops at 0 1: Reload GP0 timer automatically after counting down to 0
1:0	RW	00b	<b>GP0 Timer Tick Select</b> 00: Disable 10: 1 second 01: 1/16 second 11: 1 minute

**Offset Address: 94h (B0D17F0)**
**Miscellaneous Power Well**
**Default Value: 80h**

Bit	Attribute	Default	Description
7	RW	1	<b>SMBus Clock Select</b> 0: SMBus from divider of 14.318 Mhz Note: If set, SMBus always uses RTC clock. If not set, SMBus uses RTC clock in suspend mode, use 128K when D17F0 RxD2[2] is set. 1: SMBus from RTC clock
6	RW	0	<b>Check Power Button Enable for STR / STD Wake-Up by PWRBTN#</b> 0: Disable 1: Enable
5	RW	0	<b>Internal PLL Reset During Suspend</b> 0: Enable 1: Disable
4	RW	0	<b>Multiplexed Pins Selection for SUSST# or GPO3</b> 0: Select SUSST# 1: Select GPO3
3	RO	0	<b>Reserved</b>
2	RW	0	<b>Multiplexed Pins Selection for SUSA# or GPO2</b> 0: Select SUSA# 1: Select GPO2
1:0	RW	00b	<b>GPO0 Output Select</b> This field controls the GPO0 output signal for Pulse Width Modulation. 00: GPO0 Fixed Output Level (defined by D17F0 PMIO Rx4C[0]) 01: GPO0 output is 1 Hz "SLOWCLK" 10: GPO0 output is 4 Hz "SLOWCLK" 11: GPO0 output is 16 Hz "SLOWCLK"

**Offset Address: 95h (B0D17F0)**
**Miscellaneous Power Well Control**
**Default Value: 40h**

Bit	Attribute	Default	Description
7	RW	0	<b>CPUSTRP# to SUSST# Delay Select</b> This bit controls the delay between the deassertion of CPUSTRP# and the deassertion of SUSST# during a resume. 0: 1 msec minimum 1: 125 usec minimum
6	RW	1b	<b>SUSST# Deasserted Before PWRGD for STD</b> 0: Disable 1: Enable (SUST# is deasserted before PWRGD when resuming from STD)
5	RW	0	<b>Keyboard / Mouse Port Swap</b> This bit determines whether the keyboard and mouse ports can be swapped. 0: Disable 1: Enable
4	RW	0	<b>PWRGD Reset</b>
3	RW	0	<b>Multiplexed Pin Selection for SMB Channel 2 or GPO</b> 0: Select (GPI26/SMBDT2, GPI27/SMBCK2) 1: Select (GPO26, GPO27)
2	RW	0	<b>AOL 2 SMB Slave</b> This bit controls whether external SMB masters can access internal SMB registers (for Alert-On-LAN). 0: Enable 1: Disable
1	RW	0	<b>Multiplexed Pins Selection for SUSCLK or GPO4</b> 0: SUSCLK 1: GPO4
0	RW	0	<b>USB Wakeup for POS / STR / STD / Soft</b> This bit controls whether USB Wakeup is enabled when D17F0 PMIO Rx21-20[14] = 1. This allows wakeup from STR, STD, Soft Off, and POS. 0: Disable 1: Enable

**Offset Address: 96h (B0D17F0)**
**BATWell**
**Default Value: 0Fh**

Bit	Attribute	Default	Description
7:6	RO	0	<b>Reserved</b> Always reads 0.
5	RW	0	<b>Reserved</b> Always reads 0
4	RW	0	1. SMB GPOUT6 and GPOUT7 as PWRGD and PWRBTN 2. Enable ASF remote control: Power Up, Power Down, Power Cycle, System Reset via decoded GPOUT2, GPOUT1, GPOUT0
3:0	RW	Fh	<b>CPU Frequency Strapping Value Output to NMI, INTR, IGNNE#, and A20M# during RESET#</b> The value written to this field is strapped through NMI, INTR, IGNNE#, and A20M# during RESET# to determine the multiplier for setting the CPU's internal frequency. If the CPU hangs due to inappropriate settings written here, the GP3 timer (second timeout) can be used to initiate a system reboot (D17F0 PMIO Rx42[2] = 1). Refer to the BIOS Porting Guide for additional details.

**Offset Address: 97h (B0D17F0)**
**PWRWELL**
**Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	<b>Enable S3/S4/S5 fully wake up after core power stable</b>
6	RW	0	<b>Enable KBDC D2 command interrupt gating</b>
5	RW	0	<b>Enable PCIe PME S1 State Wake Event</b>
4	RW	0	<b>Enable SATA Spin Up Device 1</b>
3	RW	0	<b>Enable SATA Spin Up Device 0</b>
2	RW	0	<b>Support SATA Spin Up Device Feature</b>
1	RW	0	<b>PCIe Wake Enable (ACPI IO Rx03[6]) Attribution Option</b> 0: Disable 1: Enable
0	RO	0	<b>Reserved</b> Always reads 0.

**Offset Address: 98h (B0D17F0)**
**GPI2 / GPI3 Timer Control**
**Default Value: 10h**

Bit	Attribute	Default	Description
7	RW	0	<b>GPI3 Timer Start</b> On setting this bit to 1, the GPI3 timer loads the value defined by Rx9A and starts counting down. The GPI3 timer is reloaded at the occurrence of certain events enabled in the GP Timer Reload Enable Register (D17F0 PMIO Rx38). If no such event occurs and the GPI3 timer counts down to zero, then the GPI3 Timer Timeout Status bit PMIO Rx29-28[13] is set to one. Additionally, if the GP3 Timer Timeout Enable bit PMIO Rx2B-2A[13] is set, then an SMI is generated.
6	RW	0	<b>GPI3 Timer Automatic Reload</b> 0: GP3 Timer stops at 0. 1: Reload GP3 timer automatically after counting down to 0.
5:4	RW	01b	<b>GPI3 Timer Tick Select</b> 00: Disable 10: 1 second 01: 1/16 second 11: 1 minute
3	RW	0	<b>GP2 Timer Start</b> On setting this bit to 1, the GP2 timer loads the value defined by D17F0 Rx99 and starts counting down. The GP2 timer is reloaded at the occurrence of certain events enabled in the GP Timer Reload Enable Register (PMIO Rx 38). If no such event occurs and the GP2 timer counts down to zero, then the GP2 Timer Timeout Status bit PMIO Rx29-28[12] is set to one. Additionally, if the GP2 Timer Timeout Enable bit PMIO Rx2B-2A[12] is set, then an SMI is generated.
2	RW	0	<b>GPI2 Timer Automatic Reload</b> 0: GP2 Timer stops at 0. 1: Reload GP2 timer automatically after counting down to 0.
1:0	RW	00b	<b>GPI2 Timer Tick Select</b> 00: Disable 10: 1 second 01: 1 ms 11: 1 minute

**Offset Address: 99h (B0D17F0)**
**GPI2 Timer**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO/WO	0	<b>Write: GPI2 Timer Load Value</b> <b>Read: GPI2 Timer Current Count</b>

**Offset Address: 9Ah (B0D17F0)**
**GPI3 Timer**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO/WO	0	<b>Write: GPI3 Timer Load Value</b> <b>Read: GPI3 Timer Current Count</b>

**Offset Address: 9Bh (B0D17F0)**
**ASF Lock Registers**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	0	<b>Reserved</b>
5	RW	0	<b>Lock Keyboard Access</b>
4:3	RW	0	<b>Reserved</b>
2	RW	0	<b>Lock Reset Button</b>
1	RW	0	<b>Lock Power Button</b>
0	RW	0	<b>Reserved</b>

**Offset Address: 9Ch (B0D17F0)**
**ASF Command (ASF Index = 0 & Byte Write)**
**Default Value: 00h**

Bit	Attribute	Default	Description	
7:3	RO	0	<b>Reserved</b>	
2:0	RO	000b	<b>ASF Command</b> 000: Reserved 010: Unconditional power down 100: Hard reset system 110: Watch dog timer reload	001: WAKE / SMI 011: Hard reset without cycling 101: Reserved 111: Reserved

**Offset Address: 9Dh (B0D17F0)**
**ASF Data Message 1 (ASF Index = 4 & Byte Write)**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	ASF Data Message 1

**Offset Address: 9Eh (B0D17F0)**
**ASF Data Message 2 (ASF Index = 5 & Byte Write)**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	ASF Data Message 2

**Offset Address: A3-9Fh (B0D17F0) - Reserved**
**Offset Address: BE-BCh (B0D17F0)**
**SPI IO Base Address**
**Default Value: 00 0000h**

Bit	Attribute	Default	Description
23:0	RW	0	SPI IO Base Address [31:8] SPI IO Base Address = (RxBE-BC) <<8

**Offset Address: C3-C0h (B0D17F0)**
**Power Management Capability**
**Default Value: 0002 0001h**

Bit	Attribute	Default	Description
31:16	RO	0002h	<b>Power Management Capability</b>
15:8	RO	0	Next Pointer
7:0	RO	01h	Capability ID

**Offset Address: C7-C4h (B0D17F0)**
**Power Management Capability**
**Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:16	RO	0	<b>Power Management Capability Data</b>
15:8	RO	0	PM CSR P2P Support Extensions
7:0	RO	0	PM Control / Status (D0/D3 Only) Bits[7:2] are RO. Bit[2:0] are RW.

## **System Management Bus-Specific Configuration Registers (D0-E6h)**

## **Offset Address: D1-D0h (B0D17F0)**

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## SMBus I/O Base

**Default Value:** 0001h

Bit	Attribute	Default	Description
15:4	RW	0	<b>I/O Base (16-byte I/O space)</b>
3:0	RO	01h	<b>Hardwire to 01h.</b>

### **Offset Address: D2h (B0D17F0)**

## SMBus Host Configuration

**Default Value: 00h**

**Offset Address: D3h (B0D17F0)**

## **SMBus Host Slave Command**

**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	SMBus Host Slave Command

**Offset Address: D4h (B0D17F0)**

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### SMBus Slave Address for Port 1

**Default Value:** 00h

<b>Bit</b>	<b>Attribute</b>	<b>Default</b>	<b>Description</b>
7:1	RW	0	<b>SMBus Slave Address for Port 1</b>
0	RW	0	<b>Read / Write for Shadow Port 1</b>

**Offset Address: D5h (B0D17F0)**

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## SMBus Slave Address for Port 2

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**Default Value:** 00h

Bit	Attribute	Default	Description
7:1	RW	0	<b>SMBus Slave Address for Port 2</b>
0	RW	0	<b>Read / Write for Shadow Port 2</b>

**Offset Address: D6h (B0D17F0)**
**SMBus Revision ID**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	SMBus Revision ID

**Offset Address: E0h (B0D17F0)**
**GPI Trigger Level for SCI/SMI Generation**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	<b>GPI[27:24] , GPI[19:16] Trigger Level for SCI/SMI Generation</b> 0: Falling edge active 1: Rising edge active

**Offset Address: E1h (B0D17F0)**
**Reserved**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	<b>Reserved</b>

**Offset Address: E2h (B0D17F0)**
**Internal PCIe and NB PLL Control**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RO	0	<b>Reserved</b>
2	RW	0	<b>Enable Internal Hot Plug to Generate SCI/SMI</b> Note: GPI19 SCI/SMI and related bits must be programmed.
1	RW	0	<b>Enable Internal PM_PME to Generate SCI/SMI</b> Note: GPI18 SCI/SMI and related bits must be programmed.
0	RO	0	<b>Reserved</b>

**Offset Address: E4h (B0D17F0)**
**Multi Function Select 1**
**Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	<b>Fast VR Change Timer</b> D17F0 RxE5[7] controls the time select 10/20 us. 0: Disable 1: Enable
6	RW	0	<b>Multiplexed Pin Selection for (AZSDIN2, AZSDIN3) or (GPIO20, GPIO21) Select</b> 0: AZSDIN2, AZSDIN3 1: GPIO20, GPIO21
5	RW	0	<b>Disable C4 During USB Isochronous Cycle</b> 0: Enable 1: Disable
4	RW	0	<b>Multiplexed Pin Selection for GPI[12:15] / INT[E:H] or GPO[12:15]</b> 0: GPI[12:15] or INT[E:H] (D17F0 Rx5B[1] should also be set.) 1: GPO[12:15]
3	RW	0	<b>Multiplexed Pin Selection for SPICS# or GPO22</b> 0: SPICS# 1: GPO22
2	RW	0	<b>Multiplexed Pin Selection for PCI Request or GPIO</b> 0: GPI7, GPO7 1: REQ5#, GNT5#
1	RW	0	<b>Multiplexed Pins Selection for PCISTP# or GPO6</b> 0: PCISTP# 1: GPO6
0	RW	0	<b>Multiplexed Pins Selection for CPUSTP# or GPO5</b> 0: CPUSTP# 1: GPO5

**Offset Address: E5h (B0D17F0)**
**Multi Function Select 2**
**Default Value: 40h**

Bit	Attribute	Default	Description
7	RW	0	<b>VR Change Timer Select</b> 0: 100 us 1: 200us
6	RW	1	<b>AGPBZ# as Source of Bus Master Status</b> 0: Disable 1: Enable
5	RW	0	<b>EXT APIC Wake-up from PINTH</b> 0: Disable 1: Enable
4	RW	0	<b>Reserved</b>
3	RW	0	<b>CPU Deep Sleep and Speed Selection</b> 0: DPSLP# / DPRSTP# / VRDSLP 1: GPO23 / GPO28 / GPO9
2	RW	0	<b>Multiplexed Pin Selection for AZSDIN3 or PCS1#</b> 0: Select AZSDIN3 1: Select PCS1#
1	RW	0	<b>Multiplexed Pin Selection for AZSDIN2 or PCS0#</b> 0: Select AZSDIN2 1: Select PCS0#
0	RW	0	<b>Reserved</b>

**Offset Address: E6h (B0D17F0)**
**Cx State Break Event Enable**
**Default Value: 08h**

Bit	Attribute	Default	Description
7	RW	0	<b>Parallel IDE or SATA Bus Master break event enable</b> 0: Disable 1: Enable
6	RO	0	<b>Reserved</b>
5	RW	0	<b>PCI Bus Master Break Event Enable</b> 0: Disable 1: Enable
4	RW	0	<b>LAN Bus Master Break Event Enable</b> 0: Disable 1: Enable
3	RW	1	<b>AGPBZ# Bus Master Break Event Enable</b> 0: Disable 1: Enable
2	RW	0	<b>EHCI Bus Master Break Event Enable</b> 0: Disable 1: Enable
1	RW	0	<b>UHCI Bus Master Break Event Enable</b> 0: Disable 1: Enable
0	RW	0	<b>HDAC Bus Master Break Event Enable</b> 0: Disable 1: Enable

**Offset Address: E7h (B0D17F0)**
**C3/C4 Pop-Up/Pop-Down Power Management Extend Register**
**Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	<b>Enable APIC Cycle as a Bus Master Cycle during C3/C4 Pop-Up/Pop-Down Mode</b> 0: Disable 1: Enable
6	RW	0	<b>Enable HD Audio Recording FIFO Non-Empty Flag as a Bus Master Cycle</b> 0: Disable 1: Enable
5	RW	0	<b>Enable HD Audio RIRB/CORB Window Flag as a Bus Master Status</b> 0: Disable 1: Enable
4	RW	0	<b>Enable HD Audio Recording RUN as a Bus Master Status</b> 0: Disable 1: Enable
3	RW	0	<b>Enable HD Audio Recording RUN as a Bus Master Cycle</b> 0: Disable 1: Enable
2	RW	0	<b>Enable HD Audio Play RUN as a Bus Master Cycle</b> 0: Disable 1: Enable
1:0	RW	00b	<b>DPSLP# Inactive to SLP Inactive Latency Selection during C3 and C4 State in P4 Platform</b> 00: 7.5 us 01: 15 us 10: 22.5 us 11: 30 us

### Watchdog Timer Registers (E8-ECh)

#### Offset Address: EB-E8h (B0D17F0)

Watchdog Timer Memory Base

Default Value: 0000 0000h

Bit	Attribute	Default	Description
31:8	RW	0	<b>Watchdog Timer Memory Base</b>
7:0	RO	0	<b>Hardwire to 00h</b>

#### Offset Address: ECh (B0D17F0)

Watchdog Timer Control & C3 Latency Control

Default Value: 00h

Bit	Attribute	Default	Description
7:4	RO	0	<b>Reserved</b>
3	RW	0	<b>Extend C3 SLP De-assert to STPCLK# De-assert Time</b> If D17F0 PMIO Rx10[6] is set, extends to 30us. If not, extends to 15us.
2	RW	0	<b>C3 VID / FID Latency Reduce to 5 us</b>
1	RW	0	<b>Watch Dog Timer Enable</b> If set, can be reset only by PCIRST#. 0: Disable 1: Enable
0	RW	0	<b>Watchdog Timer Memory</b> 0: Disable 1: Enable

## ACPI IO Space Register (0-0Bh)

### Offset Address: 1-0h (PMIO)

#### **Power Management Status**

**Default Value: 0000h**

The bits in this register are set only by hardware and can be reset by software by writing a one to the desired bit position.

Bit	Attribute	Default	Description
15	RW1C	0	<b>Wakeup Status</b> This bit is set when the system is in the suspend state and an enabled resume event occurs. Upon setting this bit, the system automatically transitions from the suspend state to the normal working state (from C3 to C0 for the processor).
14	RW1C	0	<b>PCIe Wake Status</b>
13:12	RO	0	<b>Reserved</b>
11	RW1C	0	<b>Power Status</b> 0: Disable 1: Abnormal power off
10	RW1C	0	<b>RTC Alarm Status</b> This bit is set when the RTC generates an alarm (on assertion of the RTC IRQ signal).
9	RW1C	0	<b>Sleep Button Status (GP18)</b> This bit is set when the sleep button is pressed (SLPBTN# signal asserted low).
8	RW1C	0	<b>Power Button Status</b> This bit is set when the PWRBTN# signal is asserted low. If the PWRBTN# signal is held low for more than four seconds, this bit is cleared, the Power Button Status bit is set, and the system will transition into the soft off state.
7:6	RO	0	<b>Reserved</b>
5	RW1C	0	<b>Global Status</b> This bit is set by hardware when the BIOS Release bit is set (typically by an SMI routine to release control of the SCI lock). When this bit is cleared by software (by writing a one to this bit position) the BIOS Release bit is also cleared at the same time by hardware.
4	RW1C	0	<b>Bus Master Status</b> This bit is set when a system bus master requests the system bus. All PCI master, ISA master and ISA DMA devices are included.
3:1	RO	0	<b>Reserved</b>
0	RW1C	0	<b>ACPI Timer Carry Status</b> The bit is set when the 23rd (31st) bit of the 24 (32) bit ACPI power management timer changes.

### Offset Address: 3-2h (PMIO)

#### **Power Management Enable**

**Default Value: 0100h**

The bits in this register correspond to the bits in the Power Management Status Register at offset 1-0.

Bit	Attribute	Default	Description
15	RO	0	<b>Reserved</b>
14	RW	0	<b>PCIe Wake</b> 0: Disable 1: Enable
13:11	RO	0	<b>Reserved</b>
10	RW	0	<b>RTC Alarm Enable</b> This bit may be set to trigger either an SCI or an SMI (depending on the setting of the SCI Enable bit) to be generated when the RTC Status bit is set.
9	RW	0	<b>Sleep Button Enable</b> This bit may be set to trigger either an SCI or an SMI when the Sleep Button Status bit is set.
8	RW	1b	<b>Power Button</b> This bit may be set to trigger either an SCI or an SMI (depending on the setting of the SCI Enable bit) to be generated when the Power Button Status bit is set.
7:6	RO	0	<b>Reserved</b>
5	RW	0	<b>Global Enable</b> This bit may be set to trigger either an SCI or an SMI (depending on the setting of the SCI Enable bit) to be generated when the Global Status bit is set.
4:1	RO	0	<b>Reserved</b>
0	RW	0	<b>ACPI Timer Enable</b> This bit may be set to trigger either an SCI or an SMI (depending on the setting of the SCI Enable bit) to be generated when the Timer Status bit is set.

**Offset Address: 5-4h (PMIO)**  
**Power Management Control**
**Default Value: 0000h**

The bits in this register correspond to the bits in the Power Management Status Register at offset 1-0.

Bit	Attribute	Default	Description
15	RW	0	<b>Soft Resume</b> This bit is used to allow a system using an AT power supply to operate as if an ATX power supply were being used. Refer to the BIOS Porting Guide for implementation details. 0: Disable 1: Enable
14	RO	0	<b>Reserved</b>
13	WO	—	<b>Sleep Enable</b> This is a write-only bit; reads from this bit always return zero. Writing a one to this bit causes the system to sequence into the sleep (suspend) state defined by the Sleep Type field.
12:10	RW	000b	<b>Sleep Type</b> 000: Normal On 001: Suspend to RAM (STR) 010: Suspend to Disk (STD) (also called Soft Off). The VCC power plane is turned off while the VSUS33 and VBAT planes remain on. 011: Reserved 100: Power On Suspend without Reset 101: Power On Suspend with CPU/PCI Reset 11x: Reserved In any sleep state, there is minimal interface between powered and non-powered planes so that the effort for hardware design may be well managed.
9	RO	0	<b>Reserved</b>
8	RW	0	<b>STD Command Generates System Reset Only</b> 0: Disable 1: Enable (STD command generates a system reset and not STD)
7:3	RO	0	<b>Reserved</b>
2	WO	—	<b>Global Release</b> This bit is set by ACPI software to indicate the release of the SCI lock. Upon setting of this bit, the hardware automatically sets the BIOS Status bit. The bit is cleared by hardware when the BIOS Status bit is cleared by software. Note that the setting of this bit will cause an SMI to be generated if the BIOS Enable bit D17F0 PMIO Rx2A[5] is set.
1	RW	0	<b>Bus Master Reload</b> This bit controls whether bus master requests (D17F0 PMIO Rx1-0[4] = 1) transition the processor from C3 to C0 state. 0: Bus master requests are ignored by power management logic 1: Bus master requests transition the processor from the C3 state to the C0 state
0	RW	0	<b>SCI / SMI Select</b> This bit controls whether SCI or SMI is generated for power management events triggered by the Power Button, Sleep Button, and RTC (when D17F0 PMIO Rx1-0[ 8], [9], or [10] equals one). 0: Generate SMI 1: Generate SCI Note that certain power management events can be programmed individually to generate an SCI or SMI independent of the setting of this bit (refer to the General Purpose SCI Enable and General Purpose SMI Enable registers at PMIO Rx22 and 24). Also, Timer Status & Global Status always generate SCI and BIOS Status always generates SMI.

**Offset Address: 0B-8h (PMIO)**
**ACPI Timer**
**Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RO	0	<b>Extended Timer Value</b> This field reads back 0 if the 24-bit timer option is selected (D17F0 Rx81[3] ).
23:0	RO	0	<b>Timer Value</b> This read-only field returns the running count of the power management timer. This is a 24/32-bit counter that runs off a 3.579545 MHz clock, and counts while in the S0 (working) system state. The timer is reset to an initial value of zero during a reset, and then continues counting until the 14.31818 MHz input to the chip is stopped. If the clock is restarted without a reset, then the counter will continue counting from where it stopped.

**Processor Power Management Registers (10-16h)**
**Offset Address: 13-10h (PMIO)**
**Processor Control**
**Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:12	RO	0	<b>Reserved</b>
11	RW	0	<b>Disable PCISTP# When CLKRUN# is Deasserted</b> 0: Disable 1: Enable
10	RW	0	<b>PCI Bus Clock Run Without Stop</b> 0: CLKRUN# is always asserted 1: CLKRUN# will be de-activated after the PCI bus is idle for 26 clocks
9	RW	0	<b>Host Clock Stop (CPUSTP#)</b> This bit controls whether CPUSTP# is asserted in C3 and S1 states. Normally CPUSTP# is not asserted in C3 and S1 states, only STPCLK# is asserted. 0: CPUSTP# will not be asserted in C3 and S1 states (only STPCLK# is asserted) 1: CPUSTP# will be asserted in C3 and S1 states
8	RW	0	<b>Assert SLP# for Processor Level 3 Read</b> This bit controls whether SLP# is asserted in C3 state. 0: SLP# is not asserted in C3 state 1: SLP# is asserted in C3 state Used with Intel CPUs only.
7	RW	0	<b>Lower CPU Voltage (VRDSLP Active) During C3 / S1</b> This bit controls whether the CPU voltage is lowered when in C3/S1 state. The voltage is lowered using the VRDSLP signal to the voltage regulator. D17F0 PMIO RxE5[3] must be 0 to enable the voltage change function. Bits 8 and 9 of this register must also be set to 1. 0: Disable (normal voltage during C3/S1) 1: Enable (lower voltage during C3/S1) Note: 1. Enable to enter a C4 state in C3 command read and set Rx50[2] and Rx50[3] is a suggestion. 2. Reading LVL4 (Rx16) is the same behavior as reading LVL3 and set this bit. 3. VRDSLP will be active in either this bit set in C3 or LVL4 register read.
6	RW	0	<b>SUSST# Assertion for C3 / C4 State</b>
5	RO	0	<b>Reserved</b>
4	RW	0	<b>Throttling Enable</b> Setting this bit starts clock throttling (modulating the STPCLK# signal) regardless of the CPU state. The throttling duty cycle is determined by bits 3-0 of this register.
3:0	RW	0	<b>Throttling Duty Cycle</b>

**Offset Address: 14h (PMIO)**
**Processor Level 2**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	<b>Processor Level 2</b>

**Offset Address: 15h (PMIO)**
**Processor Level 3**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	<b>Processor Level 3</b>

**Offset Address: 16h (PMIO)**
**Processor Level 4**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	<b>Processor Level 4</b>

**General Purpose Power Management Registers (20-52h)**
**Offset Address: 21-20h (PMIO)**
**General Purpose Status**
**Default Value: 0000h**

Bit	Attribute	Default	Description
15	RW1C	0	<b>NB SERR Status</b>
14	RW1C	0	<b>USB Wake-Up in Suspend</b> For STR / STD / Soff
13	RW1C	0	<b>HDAC Wake-Up Status</b> Can be set only in suspend mode.
12	RW1C	0	<b>Battery Low Status</b> Set when the BATLOW# input is asserted low.
11	RW1C	0	<b>LID# Status</b> Set when the LID# input detects the edge selected by Rx2C [7] 0: Rising                    1: Falling
10	RW1C	0	<b>Thermal Detect Status</b> Set when the THRM# input detects the edge selected by Rx2C[6] 0: Rising                    1: Falling
9	RW1C	0	<b>Mouse Controller PME Status</b>
8	RW1C	0	<b>Ring Status</b> Set when the RING# input is asserted low.
7	RW1C	0	<b>GP3 Timer Timeout Status</b>
6	RW1C	0	<b>INTRUDER# Status</b> Set when the INTRUDER# pin is asserted low.
5	RW1C	0	<b>PME# Status</b> Set when the PME# pin is asserted low.
4	RW1C	0	<b>EXTSMI# Status</b> Set when the EXTSMI# pin is asserted low.
3	RW1C	0	<b>Internal LAN PME Status</b> Set when the internal LAN PME signal is asserted.
2	RW1C	0	<b>Internal Keyboard Controller PME Status</b> Set when the internal KBC PME signal is asserted.
1	RW1C	0	<b>GPI1 Status</b> Set when the GPI1 pin is asserted low.
0	RW1C	0	<b>GPI0 Status</b> Set when the GPIO pin is asserted low.

Note that the above bits correspond one for one with the bits of the General Purpose SCI Enable and General Purpose SMI Enable registers at offsets 22 and 24: An SCI or SMI is generated if the corresponding bit of the General Purpose SCI or SMI Enable registers, respectively, is set to one. The above bits are set by hardware only and can only be cleared by writing a one to the desired bit.

**Offset Address: 23-22h (PMIO)**
**General Purpose SCI / RESUME Enable**
**Default Value: 0000h**

Bit	Attribute	Default	Description
15	RW	0	Enable SCI on NB SERR
14	RW	0	Enable SCI on USB Wake Up
13	RW	0	Enable SCI on HDAC Wake Up
12	RW	0	Enable SCI on BATLOW#
11	RW	0	Enable SCI on LID#
10	RW	0	Enable SCI on THRM Status
9	RW	0	Enable SCI on Mouse PME Status
8	RW	0	Enable SCI on RING#
7	RW	0	Enable SCI on GP3 Timer Timeout
6	RW	0	Enable SCI on INTRUDER# Asserted
5	RW	0	Enable SCI on PME#
4	RW	0	Enable SCI on EXTSMI#
3	RW	0	Enable SCI on Internal LAN PME
2	RW	0	Enable SCI on Internal KBC PME
1	RW	0	Enable SCI on GPIO1#
0	RW	0	Enable SCI on GPIO0#

**Offset Address: 25-24h (PMIO)**
**General Purpose SMI / RESUME Enable**
**Default Value: 0000h**

Bit	Attribute	Default	Description
15	RW	0	Enable SMI on NB SERR
14	RW	0	Enable SMI on USB Wake Up
13	RW	0	Enable SMI on HDAC Wake Up
12	RW	0	Enable SMI on BATLOW#
11	RW	0	Enable SMI on LID#
10	RW	0	Enable SMI on THRM Status
9	RW	0	Enable SMI on Mouse PME Status
8	RW	0	Enable SMI on RING#
7	RO	0	Reserved
6	RW	0	Enable SMI on INTRUDER# Asserted
5	RW	0	Enable SMI on PME#
4	RW	0	Enable SMI on EXTSMI#
3	RW	0	Enable SMI on Internal LAN PME
2	RWC	0	Enable SMI on Internal KBC PME
1	RWC	0	Enable SMI on GPIO1#
0	RWC	0	Enable SMI on GPIO0#

**Offset Address: 29-28h (PMIO)**
**Global Status**
**Default Value: 0000h**

Bit	Attribute	Default	Description
15	RW1C	0	<b>GPIO Range 1 Access Status</b>
14	RW1C	0	<b>GPIO Range 0 Access Status</b>
13	RW1C	0	<b>GP3 Timer Timeout Status</b>
12	RW1C	0	<b>GP2 Timer Timeout Status</b>
11	RW1C	0	<b>SERIRQ SMI Status</b>
10	RW1C	0	<b>PMIO Rx5[6] Write SMI Status</b> This bit reports whether PMIO Rx5[6] is written. If Rx2B[3] is set to enable SMI, an SMI is generated when this bit = 1.
9	RW1C	0	<b>THRMTRIP# Activity Status</b>
8	RW1C	0	<b>CLKRUN# Resume Status</b> This bit is set when PCI bus peripherals wake up the system by asserting CLKRUN#.
7	RW1C	0	<b>Primary IRQ/INIT/NMI/SMI Resume Status</b> This bit is set at the occurrence of primary IRQs as defined in Rx85-84 of PCI configuration space.
6	RW1C	0	<b>Software SMI Status</b> This bit is set when the SMI Command port (Rx2F) is written.
5	RW1C	0	<b>BIOS Status</b> This bit is set when the Global Release bit is set to one (typically by the ACPI software to release control of the SCI lock). When this bit is reset (by writing a one to this bit position) the Global Release bit is reset at the same time by hardware.
4	RW1C	0	<b>Legacy USB Status</b> This bit is set when a legacy USB event occurs. This is normally used for USB keyboards.
3	RW1C	0	<b>GP1 Timer Time Out Status</b> This bit is set when the GP1 timer times out.
2	RW1C	0	<b>GP0 Timer Time Out Status</b> This bit is set when the GP0 timer times out.
1	RW1C	0	<b>Secondary Event Timer Time Out Status</b> This bit is set when the secondary event timer times out.
0	RO	0	<b>Primary Activity Status</b>

Note that SMI can be generated based on the setting of any of the above bits (see the Rx2A Global Enable register bit descriptions).

The bits in this register are set by hardware only and can only be cleared by writing a one to the desired bit position.  
The bits in this register are for SMI's only while the bits in Rx21-20 are for SMI's and SCI's.

**Offset Address: 2B-2Ah (PMIO)**
**Global Enable**
**Default Value: 0200h**

Bit	Attribute	Default	Description
15	RW	0	<b>SMI Enable on GPIO Range 1 Access</b>
14	RW	0	<b>SMI Enable on GPIO Range 0 Access</b>
13	RW	0	<b>SMI Enable on GP3 Timer Timeout</b>
12	RW	0	<b>SMI Enable on GP2 Timer Timeout</b>
11	RW	0	<b>SMI Enable on SERIRQ SMI</b>
10	RW	0	<b>SMI Enable on Rx5[6] (SLP_EN) Write</b>
9	RW	1b	<b>THRMTRIP# Activity Power Off Enable</b>
8	RW	0	<b>CLKRUN# Resume Enable</b> This bit may be set to trigger an SMI to be generated when the CLKRUN# Resume Status bit is set.
7	RW	0	<b>Primary IRQ/INIT/NMI/SMI resume enable in POS state</b> This bit may be set to trigger an SMI to be generated when the Primary IRQ / INIT / NMI / SMI Resume Status bit is set.
6	RW	0	<b>SMI Enable on Software SMI</b> This bit may be set to trigger an SMI to be generated when the Software SMI Status bit is set.
5	RW	0	<b>SMI Enable on BIOS</b> This bit may be set to trigger an SMI to be generated when the BIOS Status bit is set.
4	RW	0	<b>SMI Enable on Legacy USB</b> This bit may be set to trigger an SMI to be generated when the Legacy USB Status bit is set.
3	RW	0	<b>SMI Enable on GP1 Timer Timeout</b> This bit may be set to trigger an SMI to be generated when the GP1 Timer Timeout Status bit is set.
2	RW	0	<b>SMI Enable on GP0 Timer Timeout</b> This bit may be set to trigger an SMI to be generated when the GP0 Timer Timeout Status bit is set.
1	RW	0	<b>SMI Enable on Secondary Event Timeout</b> This bit may be set to trigger an SMI to be generated when the Secondary Event Timer Timeout Status bit is set.
0	RW	0	<b>SMI Enable on Primary Activity</b> This bit may be set to trigger an SMI to be generated when the Primary Activity Status bit is set.

**Offset Address: 2D-2Ch (PMIO)**
**Global Control**
**Default Value: 0000h**

Bit	Attribute	Default	Description
15	RO	0	<b>Reserved</b>
14	RW	0	<b>GPI19 SCI/SMI Enable</b>
13	RW	0	<b>GPI18 SCI/SMI Enable</b>
12	RO	0	<b>Reserved</b>
11	RW	0	<b>IDE Secondary Bus Power-Off</b> 0: Disable 1: Enable
10	RW	0	<b>IDE Primary Bus Power-Off</b> 0: Disable 1: Enable
9	RO	0	<b>Reserved</b>
8	RW1C	0	<b>SMI Active Status</b> 0: SMI Inactive 1: SMI Active
7	RW	0	<b>LID# Triggering Polarity</b> 0: Rising Edge 1: Falling Edge
6	RW	0	<b>THRM# Triggering Polarity</b> 0: Rising Edge 1: Falling Edge
5	RW	0	<b>Battery Low Resume Disable</b> 0: Enable resume 1: Disable resume from suspend when BATLOW# is asserted
4:3	RO	0	<b>Reserved</b>
2	RW	0	<b>Power Button Triggering Select</b> 0: SCI/SMI generated by PWRBTN# rising edge 1: SCI/SMI generated by PWRBTN# falling edge Set to zero to avoid the situation where the Power Button Status bit is set to wake up the system then reset again by PBOR Status to switch the system into the soft-off state.
1	RW	0	<b>BIOS Release</b> This bit is set by legacy software to indicate release of the SCI lock. Upon setting of this bit, hardware automatically sets the Global Status bit. This bit is cleared by hardware when the Global Status bit cleared by software.  Note that if the Global Enable bit is set (Power Management Enable register Rx2[5]), then setting this bit causes an SCI to be generated (because setting this bit causes the Global Status bit to be set).
0	RW	0	<b>SMI Enable</b> 0: Disable all SMI generation 1: Enable SMI generation

**Offset Address: 2Fh (PMIO)**
**SMI Command**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	<b>SMI Command</b> Writing to this port generates SMI.

**Offset Address: 33-30h (PMIO)**
**Primary Activity Detect Status**
**Default Value: 0000 0000h**

These bits correspond to the Primary Activity Detect Enable bits in Rx37-34. If the corresponding bit is set in that register, setting of a bit below will cause the Primary Activity Status bit to be set (Global Status register Rx28[0]). All bits in this register default to 0, are set by hardware only, and may only be cleared by writing 1s to the desired bit.

Bit	Attribute	Default	Description
31:11	RO	0	<b>Reserved</b>
10	RW1C	0	<b>Audio Status</b> Set if Audio is accessed.
9	RW1C	0	<b>Keyboard Controller Access Status</b> Set if the KBC is accessed via I/O port 60h.
8	RW1C	0	<b>VGA Access Status</b> Set if the VGA port is accessed via I/O ports 3B0-3DFh or memory space A0000-BFFFFh.
7	RW1C	0	<b>LPT Port Status</b> Set if the parallel port is accessed via I/O ports 278-27Fh or 378-37Fh (LPT2 or LPT1).
6	RW1C	0	<b>Serial Port B Access Status</b> Set if the serial port is accessed via I/O ports 2F8-2FFh or 2E8-2EfH (COM2 and COM4 respectively).
5	RW1C	0	<b>Serial Port A Access Status</b> Set if the serial port is accessed via I/O ports 3F8-3FFFh or 3E8-3EFh (COM1 and COM3, respectively).
4	RW1C	0	<b>Floppy Access Status</b> Set if the floppy controller is accessed via I/O ports 3F0-3F5h or 3F7h.
3	RW1C	0	<b>Secondary IDE Access Status</b> Set if the IDE controller is accessed via I/O ports 170-177h or 376h.
2	RW1C	0	<b>Primary IDE Access Status</b> Set if the IDE controller is accessed via I/O ports 1F0-1F7h or 3F6h.
1	RW1C	0	<b>Primary Interrupt Activity Status</b> Set on the occurrence of a primary interrupt (enabled via the "Primary Interrupt Channel" register at Device 17 Function 0 PCI configuration register offset 84h).
0	RW1C	0	<b>PCI Master Access Status</b> Set on the occurrence of PCI master activity.

Note: Setting of Primary Activity Status may be done to enable a "Primary Activity Event": An SMI will be generated if the Primary Activity Enable bit is set (PMIO Rx2A[0]) and/or the GP0 timer will be reloaded if the "GP0 Timer Reload on Primary Activity" bit is set (PMIO Rx38[0]).

Note: Bits 2-9 above also correspond to bits of GP Timer Reload Enable register Rx38: If bits are set in that register, setting a corresponding bit in this register will cause the GP1 timer to be reloaded.

**Offset Address: 37-34h (PMIO)**
**Primary Activity Detect Enable**
**Default Value: 0000 0000h**

These bits correspond to the Primary Activity Detect Status bits in Rx33-30. Setting of any of these bits also sets the Primary Activity Status bit (PMIO Rx28[0]) which causes the GP0 timer to be reloaded (if the Primary Activity GP0 Enable bit is set) or generates an SMI (if Primary Activity Enable is set).

Bit	Attribute	Default	Description
31:11	RO	0	<b>Reserved</b>
10	RW	0	<b>SMI on Audio Status</b> 0: Do not set PMIO Rx28[0] if Rx30[10] is set 1: Set PMIO Rx28[0] if Rx30[10] is set
9	RW	0	<b>SMI on Keyboard Controller Status</b> 0: Do not set PMIO Rx28[0] if Rx30[9] is set 1: Set PMIO Rx28[0] if Rx30[9] is set
8	RW	0	<b>SMI on VGA Status</b> 0: Do not set PMIO Rx28[0] if Rx30[8] is set 1: Set PMIO Rx28[0] if Rx30[8] is set
7	RW	0	<b>SMI on LPT Status</b>
6	RW	0	<b>SMI on Serial Port B Status</b> 0: Do not set PMIO Rx28[0] if Rx30[6] is set 1: Set PMIO Rx28[0] if Rx30[6] is set
5	RW	0	<b>SMI on Serial Port A Status</b> 0: Do not set PMIO Rx28[0] if Rx30[5] is set 1: Set PMIO Rx28[0] if Rx30[5] is set
4	RW	0	<b>SMI on Floppy Status</b> 0: Do not set PMIO Rx28[0] if Rx30[4] is set 1: Set PMIO Rx28[0] if Rx30[4] is set
3	RW	0	<b>SMI on Secondary IDE Status</b> 0: Do not set PMIO Rx28[0] if Rx30[3] is set 1: Set PMIO Rx28[0] if Rx30[3] is set
2	RW	0	<b>SMI on Primary IDE Status</b> 0: Do not set PMIO Rx28[0] if Rx30[2] is set 1: Set PMIO Rx28[0] if Rx30[2] is set
1	RW	0	<b>SMI on Primary IRQ Status</b> 0: Do not set PMIO Rx28[0] if Rx30[1] is set 1: Set PMIO Rx28[0] if Rx30[1] is set
0	RW	0	<b>SMI on PCI Master Status</b> 0: Do not set PMIO Rx28[0] if Rx30[0] is set 1: Set PMIO Rx28[0] if Rx30[0] is set

**Offset Address: 38h (PMIO)**
**GP Timer Reload Enable**
**Default Value: 00h**

All bits in this register default to 0 on power up.

Bit	Attribute	Default	Description
7	RW	0	<b>GP1 Timer Reload on KBC Access</b> 0: Normal GP1 Timer Operation 1: Setting of PMIO Rx30[9] causes the GP1 timer to reload
6	RW	0	<b>GP1 Timer Reload on Serial Port Access</b> 0: Normal GP1 Timer Operation 1: Setting of PMIO Rx30[5] or Rx30[6] causes the GP1 timer to reload
5	RO	0	<b>Reserved</b>
4	RW	0	<b>GP1 Timer Reload on VGA Access</b> 0: Normal GP1 Timer Operation 1: Setting of PMIO Rx30[8] causes the GP1 timer to reload
3	RW	0	<b>GP1 Timer Reload on Drive Access</b> 0: Normal GP1 Timer Operation 1: Setting of PMIO Rx30[4], Rx30[3], or Rx30[2] causes the GP1 timer to reload
2	RW	0	<b>GP3 Timer Reload on GPIO Range 1 Access</b> 0: Normal GP3 Timer Operation 1: Setting of Rx28[15] causes the GP3 timer to reload
1	RW	0	<b>GP2 Timer Reload on GPIO Range 0 Access</b> 0: Normal GP2 Timer Operation 1: Setting of Rx29-28[14] causes the GP2 timer to reload
0	RW	0	<b>GP0 Timer Reload on Primary Activity</b> 0: Normal GP0 Timer Operation 1: Setting of Rx28[0] causes the GP0 timer to reload. Primary activities are enabled via the Primary Activity Detect Enable register (offset 37-34) with status recorded in the Primary Activity Detect Status register (offset 33-30).

**Offset Address: 39h (PMIO)**
**ASF Status**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RO	0	<b>Reserved</b>
0	RW1C	0	<b>ASF Wake Up Status</b>

**Offset Address: 3Ah (PMIO)**
**ASF SCI Enable**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RO	0	<b>Reserved</b>
0	RW	0	<b>SCI Enable on ASF Wake</b>

**Offset Address: 3Bh (PMIO)**
**ASF SMI Enable**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RO	0	<b>Reserved</b>
0	RW	0	<b>SMI Enable on ASF Wake</b>

**Offset Address: 40h (PMIO)**
**Extend SMI/IO Trap Status**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	<b>Reserved</b>
4	RW1C	0	<b>BIOS Write Access Status</b>
3	RW1C	0	<b>GP3 Timer Second Timeout With No Cycles</b> 0: Disable 1: Enable (GP3 timer timed out twice with no cycles in between)
2	RW1C	0	<b>GP3 Timer Second Timeout Status</b>
1	RW1C	0	<b>GPIO Range 3 Access Status</b>
0	RW1C	0	<b>GPIO Range 2 Access Status</b>

**Offset Address: 42h (PMIO)**
**Extend SMI/IO Trap Enable**
**Default Value: 04h**

Bit	Attribute	Default	Description
7:5	RO	0	<b>Reserved</b>
4	RW	0	<b>SMI on BIOS Write Access</b> This bit controls whether SMI is generated when BIOS Write Access Status (PMIO Rx40[4] ) = 1. 0: Disable 1: Enable (can be reset only by PCIRST#)
3	RW	0	<b>GP3 Timer Second Timeout Override Enable</b> 0: Enable GP3 timer second timeout reset, only when PMIO Rx42[2] set and SDOUT0 strapping to 0 1: Enable GP3 timer second timeout reset anyway, (override PMIO Rx42[2] and strapping)
2	RW	1b	<b>GP3 Timer Second Timeout Reboot</b> This bit controls whether the system is rebooted when the GP3 timer times out twice (PMIO Rx40[2] = 1). 0: Disable 1: Enable
1	RW	0	<b>SMI on GPIO Range 3 Access</b> This bit controls whether SMI is generated when GPIO range 3 is accessed (PMIO Rx40[1] = 1) 0: Disable 1: Enable
0	RW	0	<b>SMI on GPIO Range 2 Access</b> This bit controls whether SMI is generated when GPIO range 2 is accessed (PMIO Rx40[0] = 1) 0: Disable 1: Enable

**Offset Address: 45-44h (PMIO)**
**EXTSMI# and Miscellaneous Input Value**
**Default Value: 0000h**

Bit	Attribute	Default	Description
15:13	RO	0	<b>Reserved</b>
12	RO	0	<b>Latest PCSn by IOR/IOW Status</b> 0: IOR 1: IOW
11	RO	0	<b>FM SMI or Serial SMI Status</b>
10	RO	0	<b>Reserved</b>
9	RO	0	<b>SMBUS IRQ Status</b>
8	RO	0	<b>SMBUS Resume Status</b>
7:6	RO	0	<b>Reserved</b>
5	RW1C	0	<b>PWRGD Signal Toggle Status</b>
4:0	RO	0	<b>Reserved</b>

**Offset Address: 47-46h (PMIO) - Reserved**

**Offset Address: 4B-48 (PMIO)**
**General Purpose Input**
**Default Value:** —

Bit	Attribute	Default	Description
31:0	RO	—	General Purpose Input

**Offset Address: 4F-4C (PMIO)**
**General Purpose Output**
**Default Value:** 3FFF FFFFh

Reads from this register return the last value written (held on chip). Some GPIO pins can be used as both input and output. The output type of these pins is OD (open drain) so to use one of these pins as an input pin, a one must be written to the corresponding bit of this register.

Bit	Attribute	Default	Description
31:0	RW	3FFF FFFFh	General Purpose Output

**Offset Address: 51-50h (PMIO) - Reserved**
**Offset Address: 52h (PMIO)**
**GPI Change SCI/SMI Enable**
**Default Value:** 00h

Bit	Attribute	Default	Description
7:0	RW	0	<b>GPI [27:24], GPI[19:16] Pin Change SCI / SMI</b> 0: Disable      1: SCI/SMI Enable

**IO Trap Registers (54-5Dh)**
**Offset Address: 57-54h (PMIO)**
**I/O Trap PCI Data**
**Default Value: nnnn nnnnh**

Bit	Attribute	Default	Description
31:0	RO	nnnn nnnnh	PCI Data During I/O Trap SMI

**Offset Address: 59-58h (PMIO)**
**I/O Trap PCI I/O Address**
**Default Value: nnnnh**

Bit	Attribute	Default	Description
15:0	RO	nnnnh	PCI Address During I/O Trap SMI

**Offset Address: 5Ah (PMIO)**
**I/O Trap PCI Command / Byte Enable**
**Default Value: nh**

Bit	Attribute	Default	Description
7:4	RO	nh	PCI Command Type During I/O Trap SMI
3:0	RO	nh	PCI Byte Enable During I/O Trap SMI

**Offset Address: 5Ch (PMIO)**
**CPU Performance**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RO	0	Reserved
0	RW	0	CPU Frequency Select 0: High                    1: Low

**Offset Address: 5Dh (PMIO)**
**Scratch Register**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	Scratch Register

**Offset Address: 63-60h (PMIO)**
**GPI Change Status**
**Default Value:0000 0000h**

Bit	Attribute	Default	Description
31:8	RW1C	0	<b>Reserved</b>
7:0	RW1C	0	<b>GPI [27:24], GPI[19:16] Pin Change Status</b> 0: Falling triggered 1: Rising triggered

Note: 1. GPI18 / PM\_PME:

If ACPI IO Rx2D[5] set, GPI18 status reflects in GPI18\_STS, PM\_PME status reflects in GPI18\_STS also.

2. GPI19 / HotPlug:

If ACPI IO Rx2D[5] set, GPI19 status reflects in GPI19\_STS, Hot Plug status reflects in GPI19\_STS also.

**Offset Address: 67-64h (PMIO)**
**GPI Change SCI Enable**
**Default Value: 00h**

Bit	Attribute	Default	Description
31:8	RW	0	<b>Reserved</b>
7:0	RW	0	<b>SCI on GPI [27:24], GPI[19:16] Pin Change</b>

**Offset Address: 6B-68h (PMIO)**
**GPI Change SMI Enable**
**Default Value: 00h**

Bit	Attribute	Default	Description
31:8	RW	0	<b>Reserved</b>
7:0	RW	0	<b>SMI on GPI [27:24], GPI[19:16] Pin Change</b>

**Watchdog Timer Memory Base (0-7h)**
**Offset Address: 3-0h (PM-MMIO)**
**Watchdog Control / Status**
**Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:8	RO	0	<b>Reserved</b>
7	WO	0	<b>Watchdog Trigger</b>
6:4	RO	0	<b>Reserved</b>
3	RO	0	<b>Watchdog Disable</b>
2	RW	0	<b>Watchdog Action</b> 0: Reset 1: Power off
1	RW1C	0	<b>Watchdog Fired</b>
0	RW	0	<b>Watchdog Enable</b> 0: Stop Watchdog 1: Run Watchdog

**Offset Address: 7-4h (PM-MMIO)**
**Count**
**Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:10	RO	0	<b>Reserved</b>
9:0	WO	0	<b>Count Register</b>

### **System Management Bus I/O Space Registers (0-Fh)**

The base address for these registers is defined in RxD1-D0 of the Device 17 Function 0 PCI configuration registers. The System Management Bus I/O space is enabled for access by the system if Device 17 Function 0 RxD2[0] = 1.

#### **Offset Address: 0h (SMIO)**

##### **SMBus Host Status**

**Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	<b>SMBus Host PEC Error</b> 0: SMBus Host PEC calculation is correct 1: SMBus Host PEC calculation error occurs. This bit is set by hardware only and can be cleared by writing 1 to it.
6	RW1C	0	<b>SMB Semaphore</b> This bit is used as a semaphore among various independent software threads that may need to use the Host SMBus logic and has no effect on hardware. After reset, this bit reads 0.  Writing 1 to this bit causes the next read to return 0; then all reads after that return 1. Writing 0 to this bit has no effect. Software can therefore write 1 to request control and if readback is 0 then it will own usage of the host controller.
5	RO	0	<b>Reserved</b>
4	RW1C	0	<b>Failed Bus Transaction</b> 0: SMBus interrupt not caused by failed bus transaction 1: SMBus interrupt caused by failed bus transaction This bit may be set when SMIO Rx2[1] is set and can be cleared by writing a 1 to this bit position.
3	RW1C	0	<b>Bus Collision</b> 0: SMBus interrupt not caused by transaction collision 1: SMBus interrupt caused by transaction collision. This bit is only set by hardware and can be cleared by writing a 1 to this bit position.
2	RW1C	0	<b>Device Error</b> 0: SMBus interrupt not caused by generation of an SMBus transaction error 1: SMBus interrupt caused by generation of an SMBus transaction error (illegal command field, unclaimed host-initiated cycle, or host device timeout). This bit is only set by hardware and can be cleared by writing a 1 to this bit position.
1	RW1C	0	<b>SMBus Interrupt</b> 0: SMBus interrupt not caused by host command completion 1: SMBus interrupt caused by host command completion. This bit is only set by hardware and can be cleared by writing a 1 to this bit position.
0	RO	0	<b>Host Busy</b> 0: SMBus controller host interface is not processing a command 1: SMBus host controller is busy processing a command None of the other SMBus registers should be accessed if this bit is set.

**Offset Address: 1h (SMIO)**
**SMBus Slave Status**
**Default Value: 00h**

Bit	Attribute	Default	Description
7	RW1C	0	<b>SMB GPIO Slave PEC Error</b> 0: SMBus GPIO Slave PEC calculation is correct. 1: SMBus GPIO Slave PEC calculation error occurs. This bit is set by hardware only and can be cleared by writing 1 to it.
6	RW1C	0	<b>SMB Host Slave PEC Error</b> 0: SMBus Host Slave PEC calculation is correct. 1: SMBus Host Slave PEC calculation error occurs. This bit is set by hardware only and can be cleared by writing 1 to it.
5	RW1C	0	<b>Alert Status</b> 0: SMBus interrupt not caused by SMBALRT# signal 1: SMBus interrupt caused by SMBALRT# signal. This bit will be set only if the Alert Enable bit in SMIO Rx8[3] is set. This bit is only set by hardware and can be cleared by writing a 1 to this bit position.
4	RW1C	0	<b>Shadow 2 Status</b> 0: SMBus interrupt not caused by address match to SMBus Shadow Address Port 2 1: SMBus interrupt or resume event caused by slave cycle address match to SMBus Shadow Address Port 2. This bit is only set by hardware and can be cleared by writing a 1 to this bit position.
3	RW1C	0	<b>Shadow 1 Status</b> 0: SMBus interrupt not caused by address match to SMBus Shadow Address Port 1 1: SMBus interrupt or resume event caused by slave cycle address match to SMBus Shadow Address Port 1. This bit is only set by hardware and can be cleared by writing a 1 to this bit position.
2	RW1C	0	<b>Slave Status</b> 0: SMBus interrupt not caused by slave event match 1: SMBus interrupt or resume event caused by slave cycle event match of the SMBus Slave Command Register at SMIO RxD3 (command match) and the SMBus Slave Event Register at SMIO Rx0A (data event match). This bit is only set by hardware and can be cleared by writing a 1 to this bit position.
1	RO	0	<b>Reserved</b>
0	RO	0	<b>Slave Busy</b> 0: SMBus controller slave interface is not processing data 1: SMBus controller slave interface is busy receiving data None of the other SMBus registers should be accessed if this bit is set.

**Offset Address: 2h (SMIO)**
**SMBus Host Control**
**Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	<b>PEC Enable</b> 0: Disable 1: Enable SMBus Host to support PEC calculation.
6	RW	0	<b>Start</b> 0: Writing 0 has no effect 1: Start Execution of Command Writing a 1 to this bit causes the SMBus controller host interface to initiate execution of the command programmed in the SMBus Command Protocol field (bits 4-2). All necessary registers should be programmed prior to writing a 1 to this bit. The Host Busy bit SMIO Rx0[0] can be used to identify when the SMBus controller has completed command execution.
5:2	RW	0	<b>SMBus Command Protocol</b> Selects the type of command the SMBus host controller will execute. Reads or Writes are determined by Rx4[0]. <b>Protocol</b> 0000: Quick 0001: Byte 0010: Byte Data 0011: Word Data 0100: Process Call 0101: Block 0110: I2C with 10-bit Address 0111: Reserved 10xx: Reserved 1100: I2C Process Call 1101: I2C Block 1110: I2C with 7-bit Address 1111: Universal
1	RW	0	<b>Kill Transaction in Progress</b> 0: Normal host controller operation 1: Stop host transaction currently in progress Setting this bit also sets the status bit SMIO Rx0[4] and asserts the interrupt selected by the SMB Interrupt Select bit SMIO Rx2D2[3].
0	RW	0	<b>Interrupt Enable</b> 0: Disable interrupt generation 1: Enable generation of interrupts on completion of the current host transaction.

**Offset Address: 3h (SMIO)**
**SMBus Host Command**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	<b>SMBus Host Command</b> This field contains the data transmitted in the command field of the SMBus host transaction.

**Offset Address: 4h (SMIO)**
**SMBus Host Address**
**Default Value: 00h**

The contents of this register are transmitted in the address field of the SMBus host transaction.

Bit	Attribute	Default	Description
7:1	RW	0	<b>SMBus Address</b> This field contains the 7-bit address of the targeted slave device.
0	RW	0	<b>SMBus Read or Write</b> 0: Execute a WRITE command 1: Execute a READ command

**Offset Address: 5h (SMIO)**
**SMBus Host Data 0**
**Default Value: 00h**

The contents of this register are transmitted in the Data 0 field of SMBus host transaction writes. On reads, Data 0 bytes are stored here.

Bit	Attribute	Default	Description
7:0	RW	0	<b>SMBus Data 0</b> For Block Write commands, this field is programmed with the block transfer count (a value between 1 and 32). Counts of 0 or greater than 32 are undefined. For Block Read commands, the count received from the SMBus device is stored here.

**Offset Address: 6h (SMIO)**
**SMBus Host Data 1**
**Default Value: 00h**

The contents of this register are transmitted in the Data 1 field of SMBus host transaction writes. On reads, Data 1 bytes are stored here.

Bit	Attribute	Default	Description
7:0	RW	0	<b>SMBus Data 1</b> This register should be programmed with the value to be transmitted in the Data 1 field of an SMBus host interface transaction.

**Offset Address: 7h (SMIO)**
**SMBus Block Data**
**Default Value: 00h**

Reads and writes to this register are used to access the 32-byte block data storage array. An internal index pointer is used to address the array. It is reset to 0 by reads of the SMIO Rx2 and incremented automatically by each access to this register. The transfer of block data into (read) or out of (write) this storage array during an SMBus transaction always starts at index address 0.

Bit	Attribute	Default	Description
7:0	RW	0	<b>SMBus Block Data</b>

**Offset Address: 8h (SMIO)**
**SMBus Slave Control**
**Default Value: 00h**

Reads and writes to this register are used to access the 32-byte block data storage array. An internal index pointer is used to address the array. It is reset to 0 by reads of the SMIO Rx2 and incremented automatically by each access to this register. The transfer of block data into (read) or out of (write) this storage array during an SMBus transaction always starts at index address 0.

Bit	Attribute	Default	Description
7	RW	0	<b>SMBus GPIO Slave PEC Enable</b> 0: Disable. 1: Enable SMBus GPIO Slave to support PEC calculation.
6	RW	0	<b>SMBus Host Slave PEC Enable</b> 0: Disable 1: Enable SMBus Host Slave to support PEC calculation.
5	RW	0	<b>PEC Abort</b> 0: Disable 1: Enable SMBus to abort PEC calculation error
4	RW	0	<b>SMBus GPIO Slave Enable</b> 0: Disable 1: Enable the generation of a resume event when an external SMBus master generates a transaction with an address that matches the GPIO Slave Address register (SMIO Rx0F).
3	RW	0	<b>SMBus Alert Enable</b> 0: Disable 1: Enable generation of an interrupt or resume event on the assertion of the SMBALRT# signal
2	RW	0	<b>SMBus Shadow Port 2 Enable</b> 0: Disable 1: Enable generation of an interrupt or resume event on external SMBus master generation of a transaction with an address that matches the SMBus Slave Shadow Port 2 register (SMIO RxD5).
1	RW	0	<b>SMBus Shadow Port 1 Enable</b> 0: Disable 1: Enable generation of an interrupt or resume event on external SMBus master generation of a transaction with an address that matches the SMBus Slave Shadow Port 1 register (SMIO RxD4).
0	RW	0	<b>SMBus Slave Enable</b> 0: Disable 1: Enable generation of an interrupt or resume event on external SMBus master generation of a transaction with an address that matches the SMBus host controller slave port of 10h, a command field which matches the SMBus Slave Command register (SMIO RxD3), and a match of one of the corresponding enabled events in the SMBus Slave Event Register (SMIO Rx0Ah).

**Offset Address: 9h (SMIO)**
**SMBus Shadow Command**
**Default Value: 00h**

This register is used to store command values for external SMBus master accesses to the host slave and slave shadow ports.

Bit	Attribute	Default	Description
7:0	RO	0	<b>Shadow Command</b> This field contains the command value which was received during an external SMBus master access whose address field matched the host slave address (10h) or one of the slave shadow port addresses.

**Offset Address: 0B-0Ah (SMIO)**
**SMBus Slave Event**
**Default Value: 0000h**

This register is used to enable generation of interrupt or resume events for accesses to the host controller's slave port.

Bit	Attribute	Default	Description
15:0	RW	0	<b>SMBus Slave Event</b> This field contains data bits used to compare against incoming data to the SMBus Slave Data Register (SMIO Rx0Ch). When a bit in this register is set and the corresponding bit the Slave Data register is also set, an interrupt or resume event will be generated if the command value matches the value in the SMBus Slave Command register and the access was to SMBus host address 10h.

**Offset Address: 0D-0Ch (SMIO)**
**SMBus Slave Data**
**Default Value: 0000h**

This register is used to store data values for external SMBus master accesses to the shadow ports or the SMBus host controller's slave port.

Bit	Attribute	Default	Description
15:0	RO	0	<b>SMBus Slave Data</b> This field contains the data value which was transmitted during an external SMBus master access whose address field matched one of the slave shadow port addresses or the SMBus host controller slave port address of 10h.

**Offset Address: 0Fh (SMIO)**
**SMBus GPIO Slave Address**
**Default Value: 30h**

Bit	Attribute	Default	Description
7:1	RW	30h	<b>SMBus GPIO Slave Address</b> Specifies the address used to match against the incoming SMBus.
0	RO	0	<b>Reserved</b>

**Related PCI Space Registers for System Management Bus:**

Refer to D17F0 Rx94 for SMBus Clock Select register information

Refer to D17F0 RxD1-D0 for SMBus I/O Base Address register information

Refer to D17F0 RxD2 for SMBus Host Configuration register information

Refer to D17F0 RxD3 for SMBus Slave Command register information

Refer to D17F0 RxD4 for SMBus Slave Shadow Port 1 register information

Refer to D17F0 RxD5 for SMBus Slave Shadow Port 2 register information

Refer to D17F0 RxD6 for SMBus Revision Identification register information

## SPI Controller

SPI controller is connected to the LPC controller. All registers are memory-mapped and the base address are located in B0D17F0 RxBEh~RxBCh of the LPC controller.

Let SPIBAR = RxBEh~RxBCh [23:0] → SPI Memory-Mapped Base Address = SPIBAR <<8

### Offset Address: 1-0h (SPI-MMIO)

#### SPI Status

**Default Value: 0002h**

Bit	Attribute	Default	Description
15	R/WLO (note)	0	<b>SPI Configuration Lock-Down</b> 0: No Lock-Down 1: SPI Static Configuration information from Rx50h to Rx6Fh cannot be overwritten. Once set to 1, this bit can only be cleared through hardware reset.
14:4	RO	0	<b>Reserved</b>
3	RW1C	0	<b>Blocked Access Status</b> 0: Not blocked 1: Hardware sets this bit to 1 when an access is blocked from running on the SPI interface. Prohibition from running the SPI interface might happen because one of the protection policies, or when any one of the programmed cycle registers is written while a programmed access is already in progress. This bit is set when both programmed accesses and direct memory reads are blocked.
2	RW1C	0	<b>Cycle Done Status</b> 0: Not done 1: Sets this bit to 1 when the SPI Cycle completes after software sets the Rx2[1] SCGO bit
1	RO	1b	<b>SPI Access Grant</b> 0: Default 1: It is set by hardware in response to software setting the SPI Access Request bit and completing the Future Pending handshake with the LAN component
0	RO	0	<b>SPI Cycle Progress</b> 0: Cycle Not in Progress 1: Hardware sets this bit when software sets the Rx2[1] SCGO bit in the Command register. This bit remains set until the cycle completes on the SPI interface. Hardware automatically sets and clears this bit so that software can determine when read data is valid and/or when it is safe to begin programming the next command.

Note: **R/WLO** means **Read/Write Lock-Once**. A register bit can be written to the non-locked value multiple times, but to the locked value only once. After the locked value has been written, the bit becomes read only.

**Offset Address: 3-2h (SPI-MMIO)**
**SPI Control**
**Default Value: 4009h**

Bit	Attribute	Default	Description
15	RW	0	<b>SPI SMI# Enable</b> 0: Disable 1: Enable The SPI asserts an SMI# request whenever Rx1-0[2] Cycle Done Status bit is 1.
14	RW	1b	<b>DATA Cycle</b> 0: No data is delivered for this cycle, and the DBC and data fields themselves are ignored. 1: There is data that corresponds to this transaction.
13	RW	0	<b>Fast Read Enable (FREN)</b> 0: Disable 1: Enable
12	RW	0	<b>Port Select</b> 0: Select CS0 1: Select CS1
11:8	RW	0	<b>Data Byte Count</b> This field specifies the number of bytes to shift in or out during the data portion of the SPI cycle. The valid setting is any value from 0 to 15. The number of bytes transferred is the value of this field plus 1.
7	RW	0	<b>Data Atomic Cycle Sequence</b> 0: No data atomic cycle sequence 1: When set to 1 along with the SCGO assertion, the chip will execute a sequence of data on the SPI interface without allowing the LAN component to arbitrate and interleave cycles.
6:4	RW	0	<b>Cycle Opcode Pointer</b> The field selects one of the programmed opcodes in the Opcode Menu and uses it as the SPI command/Opcde. In the case of an Atomic Cycle Sequence, this determines the second command.
3	RW	1b	<b>Sequence Prefix Opcode Pointer</b> This field selects one of the two programmed prefix opcodes for use when performing an Atomic Cycle Sequence. By making this programmable, this chip supports flash devices that have different opcodes for enabling writes to the data space vs. status register 0: A value of 0 points to the opcode in the least significant byte of the Prefix Opcodes register 1: A value of 1 points to the opcode in the <b>maximum</b> significant byte of the Prefix Opcodes register.
2	RW	0	<b>Atomic Cycle Sequence</b> 0: No atomic cycle sequence. 1: When set to 1 along with the SCGO assertion, the chip will execute a sequence of commands on the SPI interface without allowing the LAN component to arbitrate and interleave cycles.
1	RW	0	<b>SPI Cycle Go &lt;SCGO&gt;</b> 0: SPI Cycle Not Started 1: A write to this register with a 1 in this bit starts the SPI cycle defined by the other bits in this register. The "SPI Cycle in Progress" bit gets set through this action.
0	RW	1b	<b>SPI Access Request</b> This bit is used by software to request that the other SPI master stop initiating long transactions on the SPI bus. 0: No request 1: Request that the other SPI master stop initiating long transactions on the SPI bus

**Offset Address: 7-4h (SPI-MMIO)**
**SPI Control**
**Default Value: 0000h**

Bit	Attribute	Default	Description
31:24	RO	0	<b>Reserved</b>
23:0	RW	0	<b>SPI Cycle Address</b> This field shifted out as the SPI Address

**Offset Address: 47-08h (SPI-MMIO)**
**SPI Data N Register**
**Default Value: 0000h**

Bit	Attribute	Default	Description									
63:0	RW	0	<p><b>SPI Cycle Data[N] &lt;SCD[N]&gt;</b>            This field is shifted out as the SPI Data on the Master-Out Slave-in Data pin during the data portion of the SPI cycle. The SCD[N] register does not begin shift until SPID[N-1] has completely shifted in/out.</p> <p>The register also shifts in the data from the Master-in Slave-Out pin into this register during the data portion of the SPI cycle.</p> <table style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 30%;">Memory Address : SPI Data[0]:</td> <td style="width: 30%;">SPIBAR + 08h</td> <td style="width: 30%;">Size:64bits</td> </tr> <tr> <td>SPI Data[1]:</td> <td>SPIBAR + 10h</td> <td>Size:64bits</td> </tr> <tr> <td>SPIBAR + (18h~47h)</td> <td>Reserved</td> <td>SPI Data[2..7]:</td> </tr> </table>	Memory Address : SPI Data[0]:	SPIBAR + 08h	Size:64bits	SPI Data[1]:	SPIBAR + 10h	Size:64bits	SPIBAR + (18h~47h)	Reserved	SPI Data[2..7]:
Memory Address : SPI Data[0]:	SPIBAR + 08h	Size:64bits										
SPI Data[1]:	SPIBAR + 10h	Size:64bits										
SPIBAR + (18h~47h)	Reserved	SPI Data[2..7]:										

**Offset Address: 4F-48h (SPI-MMIO) - Reserved**
**Offset Address: 53-50h (SPI-MMIO)**
**BIOS Base Address**
**Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RO	0	<b>Reserved</b>
23:8	RW	0	<b>Bottom of System Flash</b> This field determines the bottom of the System BIOS. The chip will not run programmed commands nor memory reads whose address field is less than this value. This field corresponds to bits 23:8 of the 3-Bytes address; bits 7:0 are assumed to be 00h for this vector when comparing to a potential SPI address.
7:0	RO	0	<b>Reserved</b>

**Offset Address: 55-54h (SPI-MMIO)**
**Prefix Opcode Configuration**
**Default Value: 0000h**

Bit	Attribute	Default	Description
15:8	RW	0	<b>Prefix Opcode 1</b> Software programs an SPI pcode into this field that is permitted to run as the first command in an atomic cycle sequence.
7:0	RW	0	<b>Prefix Opcode 0</b> Software programs an SPI pcode into this field that is permitted to run as the first command in an atomic cycle sequence.

**Offset Address: 57-56h (SPI-MMIO)**
**Opcode Type Configuration**
**Default Value: 0000h**

Bit	Attribute	Default	Description
15:14	RW	0	<b>Opcode Type7</b> Refer to the description in bits 1:0
13:12	RW	0	<b>Opcode Type6</b> Refer to the description in bits 1:0
11:10	RW	0	<b>Opcode Type5</b> Refer to the description in bits 1:0
9:8	RW	0	<b>Opcode Type4</b> Refer to the description in bits 1:0
7:6	RW	0	<b>Opcode Type3</b> Refer to the description in bits 1:0
5:4	RW	0	<b>Opcode Type2</b> Refer to the description in bits 1:0
3:2	RW	0	<b>Opcode Type1</b> Refer to the description in bits 1:0
1:0	RW	0	<b>Opcode Type0</b> This field specifies information about the corresponding Opcode 0. This information allow the hardware to: 1) Decides whether to use the address field and 2) Provides BIOS and Shared Flash protection capabilities. The encoding of the two bits is: 00: No address associated with this opcode; Read cycle type 01: No address associated with this opcode; Write cycle type 10: Address required; Read cycle type 11: Address required; Write cycle type

**Offset Address: 5F-58h (SPI-MMIO)**
**Opcode Menu Configuration**
**Default Value: 0000h**

Bit	Attribute	Default	Description
63:56	RW	0	<b>Opcode 7</b> See the description for bits 7:0
55:48	RW	0	<b>Opcode 6</b> See the description for bits 7:0
47:40	RW	0	<b>Opcode 5</b> See the description for bits 7:0
39:32	RW	0	<b>Opcode 4</b> See the description for bits 7:0
31:24	RW	0	<b>Opcode 3</b> See the description for bits 7:0
23:16	RW	0	<b>Opcode 2</b> See the description for bits 7:0
15:8	RW	0	<b>Opcode 1</b> See the description for bits 7:0
7:0	RW	0	<b>Opcode 0</b> Software programs an SPI opcode into this field for use when initiating SPI commands through the Control Register.

**Offset Address: 63-60h (SPI-MMIO)**
**Protected BIOS Range[0] (PBR[0])**
**Default Value: 0000h**

Bit	Attribute	Default	Description
31	RW	0	<b>Write Protection Enable</b> 0: Disable. The base and limit field are ignored when this bit is cleared. 1: Enable. The base and limit fields in this register are valid.
30:24	RO	0	<b>Reserved</b>
23:12	RW	0	<b>Protected Range Limit</b> This field corresponds to SPI address bits 23:12 and specifies the upper limit of the protected range.
11:0	RW	0	<b>Protected Range Base</b> This field corresponds to SPI address 23:12 and specifies the lower base of the protected range.

**Offset Address: 67-64h (SPI-MMIO)**
**Protected BIOS Range[1]**

Register description is same as PBR[0].

**Offset Address: 6B-68h (SPI-MMIO)**
**Protected BIOS Range[2]**

Register description is same as PBR[0].

**Offset Address: 6D-6Ch (SPI-MMIO)**
**Clock Divider & Debug Mode**
**Default Value: 0001h**

Bit	Attribute	Default	Description
15:12	RO	0	<b>Reserved</b>
11	RW	0	<b>DNCLKON</b> 0: Free clock 1: Dynamic clock
10:9	RW	0	<b>Debug Mode</b> 00: Sstate 01: DDBC 10: {block0,block1,data_cycle,SPIGNT,WIP1} 11: {SPICFGHIT,SPIDEVCYC,ROMHIT,2'b0}
8	RO	0	<b>Reserved</b>
7:0	RW	01h	<b>Clock Divider</b> When this field is 1, it is divided by 2 and the default value is 1

## Bus 0 Device 17 Function 7 (B0D17F7): Ultra V-Link Control

This configuration is provided to facilitate the configuration of the South Bridge V-Link controller without requiring new enumeration code. This function is represented as bus number 0, device number 17, and function 7.

### Header Registers (0-3Fh)

#### Offset Address: 1-0h (B0D17F7)

**Vendor ID**

**Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	<b>Vendor ID</b>

#### Offset Address: 3-2h (B0D17F7)

**Device ID**

**Default Value: 287Eh**

Bit	Attribute	Default	Description
15:0	RO	287Eh	<b>Device ID</b>

#### Offset Address: 5-4h (B0D17F7)

**PCI Command**

**Default Value: 0000h**

Bit	Attribute	Default	Description
15:10	RO	0	<b>Reserved</b>
9	RO	0	<b>Fast Back-to-Back Cycle Enable</b> Hardwired to 0.
8	RW	0	<b>SERR# Enable</b> Hardwired to 0.
7	RO	0	<b>Reserved</b>
6	RW	0	<b>Parity Error Response</b> 0: Ignore parity errors 1: Perform parity check and take normal action on detected parity errors
5	RO	0	<b>VGA Palette Snooping</b> Hardwired to 0
4	RO	0	<b>Memory Write and Invalidate</b> Hardwired to 0
3	RO	0	<b>Respond To Special Cycle</b> Hardwired to 0
2	RW	0	<b>Bus Master</b> 0: Never behaves as a bus master 1: Enable to operate as a bus master on the secondary interface
1	RW	0	<b>Memory Space Access</b> 0: Does not respond to memory space access 1: Responds to memory space access
0	RO	0	<b>I/O Space Access</b> 0: Does not respond to I/O space access 1: Responds to I/O space access

**Offset Address: 7-6h (B0D17F7)**
**PCI Status**
**Default Value: 2210h**

Bit	Attribute	Default	Description
15	RW1C	0	<b>Parity Error Detected</b> Set by PERRS, reset by writing 1.
14	RW1C	0	<b>SERR# Detected</b> Note. Set if ECC error
13	RW1C	1b	<b>Set When Terminated with Master-Abort, Except Special Cycle</b> 0: No abort received 1: Transaction aborted by the master
12	RW1C	0	<b>Set When Received a Target-Abort</b> 0: No abort received 1: Transaction aborted by the target
11	RO	0	<b>Set When Signaled a Target-Abort</b>
10:9	RO	01b	<b>DEVSEL# Timing</b> 00: Fast 01: Medium (default) 10: Slow 11: Reserved
8	RW1C	0	<b>Set When Set or Observed SERR# and Parity Error</b> Reserved
7	RO	0	<b>Capable of Accepting Fast Back-to-Back as a Target</b> Reserved
6	RO	0	<b>Reserved</b>
5	RO	0	<b>66 MHz Capable</b>
4	RO	1b	<b>Support New Capability List</b>
3:0	RO	0	<b>Reserved</b>

**Offset Address: 8h (B0D17F7)**
**Revision ID**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	<b>Revision ID</b>

**Offset Address: 0B-9h (B0D17F7)**
**PCI Header Registers**
**Default Value: 06 0000h**

Bit	Attribute	Default	Description
23:0	RO	06 0000h	<b>Class Code</b>

**Offset Address: 0Ch (B0D17F7) - Reserved**
**Offset Address: 0Dh (B0D17F7)**
**Latency Timer**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RW	0	<b>Latency Timer</b>
2:0	RO	0	<b>Latency Timer</b> Bit [2:0] (MLT[2:0]): reserved (RO), guarantee time slice for CPU master

**Offset Address: 0Eh (B0D17F7)**
**Header Type**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	<b>Header Type</b> It adheres to the Type 0 PCI Configuration

**Offset Address: 0Fh (B0D17F7)**
**Built In Self Test (BIST)**
**Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	<b>BIST Support</b>
6:0	RO	0	<b>Reserved</b>

**Offset Address: 2B-10h (B0D17F7) - Reserved**
**Offset Address: 2D-2Ch (B0D17F7)**
**Subsystem Vendor ID**
**Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	<b>Subsystem Vendor ID</b>

**Offset Address: 2F-2Eh (B0D17F7)**
**Subsystem ID**
**Default Value: 337Eh**

Bit	Attribute	Default	Description
15:0	RO	337Eh	<b>Subsystem ID</b>

**Offset Address: 33-30h (B0D17F7) - Reserved**
**Offset Address: 34h (B0D17F7)**
**Capability Pointer**
**Default Value: 58h**

Bit	Attribute	Default	Description
7:0	RO	58h	<b>Capability Pointer</b> Byte offset into configuration space to capability list

**Offset Address: 3F-35h (B0D17F7) - Reserved**

**V-Link Control Interface (40–55h)**
**Offset Address: 40h (B0D17F7)**
**V-Link Specification ID**
**Default Value: F4h**

Bit	Attribute	Default	Description
7:4	RO	Fh	<b>Reserved</b>
3:0	RO	4h	<b>South Bridge Revision ID</b> 0 & F: Means the old version of 8 bits, the operating mode is determined by Rx48[0] (R8XVK) 1: means the support of V-Link capability is up to mode 1. 2: the support of V-Link capability is up to mode 2. 3: the support of V-Link capability is up to mode 3. 4: the support of V-Link capability is up to mode 4.

**Table 13. V-Link Modes Supported**

	X: Multiples of 66MHz cycle	Bus Width	R8XVK (B0D17F7 Rx48[0])	RX16VK (B0D17F7 Rx48[5])	RVKSP (B0D17F7 Rx48[1])
<b>Mode 0</b>	4X	8-bit 	0	0	-
<b>Mode 1</b>	8X	4-bit 	1	0	1
<b>Mode 2</b>	8X	8-bit 	1	0	0
<b>Mode 3</b>	4X	16-bit 	0	1	0
<b>Mode 4</b>	8X	8-bit 	1	1	1

Note:  : half duplex,  : full duplex

**Offset Address: 47-41h (B0D17F7)**

**Offset Address: 48h (B0D17F7)**
**V-Link Configuration -SB**
**Default Value: 1Ah**

This register is used to configure V-Link bus controller on South Bridge chips.

Bit	Attribute	Default	Description
7	RW	0	<b>Parity Check</b> 0: Disable 1: Enable
6	RO	0	<b>Reserved</b>
5	RW	0	<b>16-Bit Width</b> 0: Disable 1: Enable
4	RW	1b	<b>8-Bit Width</b> 0: Disable 1: Enable
3	RW	1b	<b>4X Rate</b> 0: Disable 1: Enable
2	RW	0	<b>2X Rate</b> 0: Disable 1: Enable
1	RW	1b	<b>V-Link Split Bus</b> 0: Disable 1: Enable
0	RW	0	<b>8X Rate</b> 0: Disable 1: Enable

**Offset Address: 49h (B0D17F7)**
**V-Link Capability - SB**
**Default Value: BBh**

Bit	Attribute	Default	Description
7	RW1C	1b	<b>V-Link Parity Error Detected</b>
6	RO	0	<b>Reserved</b>
5	RO	1b	<b>16-Bit Bus Width</b> 0: Not Support 1: Support
4	RO	1b	<b>8-Bit Bus Width</b> 0: Not Support 1: Support
3	RO	1b	<b>4X Rate</b> 0: Not Support 1: Support
2	RO	0	<b>2X Rate</b> 0: Not Support 1: Support
1	RO	1b	<b>V-Link Split Bus</b> Native 8X Mode Support 0: Not Support 1: Support
0	RO	1b	<b>8X Rate</b> 0: Not Support 1: Support

**Offset Address: 4Ah (B0D17F7)**
**SB Downlink (C2P) Status**
**Default Value: 88h**

Bit	Attribute	Default	Description
7:4	RO	1000b	<b>CPU to PCI Request Depth</b> Max # of DNCMD (CPU to PCI) requests 0000 - depth of 1 ... 1111 - depth of 16
3:0	RO	8h	<b>CPU to PCI Write Buffer Size</b> Max # of DW, depth from 1 to 16

**Offset Address: 4Bh (B0D17F7)**
**SB Uplink PCI to CPU (P2C) Configuration 1**
**Default Value: 80h**

Bit	Attribute	Default	Description
7:4	RW	1000b	<b>PCI to CPU Request Depth</b> Max # of outstanding UPCMD (PCI to CPU) requests 0000: 16 level 0001: 1 level 0010: 2 level 0011: 3 level 0100: 4 level 0101: 5 level 0110: 6 level 0111: 7 level 1000: 8 level 1111: 15 level
3:2	RO	0	<b>Reserved</b>
1:0	RW	00b	<b>High Priority PCI to CPU Request Depth</b> 00: 1 levels 01: 4 levels 10: 8 levels 11: 16 levels

**Offset Address: 4Ch (B0D17F7)**
**SB Uplink (P2C) Configuration 2**
**Default Value: 82h**

Bit	Attribute	Default	Description
7:4	RW	8h	<b>PCI to CPU Write Buffer Size</b> (max # of lines)
3:0	RW	2h	<b>PCI to PCI Write Buffer Size</b> (max # of lines)

**Offset Address: 4Dh (B0D17F7)**
**SB V-Link Bus Timer**
**Default Value: 44h**

Bit	Attribute	Default	Description
7:4	RW	0100b	<b>V-Link Bus Timer Used by SB When NB Normal Priority Request Arrived</b> 0000: 0 VCLK 0001: 1*4 VCLK 0010: 2*4 VCLK 0011: 3*4 VCLK 0100: 4*4 VCLK ... 1000: 8*4 VCLK 1001: 16*4 VCLK 1010: 32*4 VCLK 1011: 64*4 VCLK 11--: SB holds the bus as long as there is pending upstream request
3:0	RW	0100b	<b>V-Link Bus Timer Used by SB When NB High Priority Request Arrived</b> 0000: 0 VCLK 0001: 1*2 VCLK 0010: 2*2 VCLK 0011: 3*2 VCLK 0100: 4*2 VCLK ... 1000: 8*2 VCLK 1001: 16*2 VCLK 1010: 32*2 VCLK 1011: 64*2 VCLK 11--: SB holds the bus as long as there is pending upstream request

**Table 14. SB V-Link Bus Timer Operation**

RSNTM[3:0] (Rx4D[7:4])	RSHTM[3:0] (Rx4D[3:0])	NB Request Priority	SB When to Relinquish V-Link Bus
0000	xxxx	Normal / high	Immediately
0001,0010,...	0000	High	Immediately
0001,0010,...	0001,0010,...	High	Wait for either Normal or high timer expired
0001,0010,...	00xx	Normal	Wait for Normal timer expired
0001,0010,...	11xx	Normal / high	Wait for Normal timer expired
11xx	0000	High	Immediately
11xx	0000	Normal	Wait until there is no more pending upstream request
11xx	0001,0010,...	High	Wait for High timer expired
11xx	0001,0010,...	Normal	Wait until there is no more pending upstream request
11xx	11xx	Normal / high	Wait until there is no more pending upstream request

**Offset Address: 4Eh (B0D17F7)**
**V-Link Feature Control**
**Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	<b>Downstream DAC Cycle Supported</b> 0: Disable 1: Enable
6:1	RO	0	<b>Reserved</b>
0	RW	0	<b>Hand Shake V-Link Re-connection Scheme</b>

**Offset Address: 4Fh (B0D17F7)**
**SB V-Link Miscellaneous Control**
**Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	<b>Up Stream High Priority Command</b> 0: Disable 1: Enable high priority up command
6	RW	0	<b>Enable PCI to PCI Bridge Header for External PCI Bus</b> 1: Enable PCI-to-PCI Bridge 0: Disable PCI-to-PCI Bridge
5:4	RO	0	<b>Reserved</b>
3	RW	0	<b>Dynamic STOP on Up Strobe</b> 0: Disable 1: Enable
2	RW	0	<b>Hide C2P Cycle for Internal Devices on PCI BUS.</b> When set to 1, only cycles which act with external PCI devices will appear on PCI Bus.
1	RW	0	<b>Support Extended Configuration Space Up to 4096 bytes</b>
0	RW	0	<b>CPU to PCI Cycle Wait Till PCI to CPU Write Flushed (except CPU to PCI Post-Write)</b> 0: Disable. CPU to PCI Read Access (C2PRA) is not blocked. 1: Enable. C2PRA wait for SB PCI bus (PCI1) P2C write FIFO empty.

**Offset Address: 50h (B0D17F7)**
**SB Peripheral Device's Bus Priority**
**Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	<b>Reserved</b>
6	RW	0	<b>NIC Priority</b> 0: Low Priority 1: High Priority
5	RW	0	<b>SATA Priority</b> 0: Low Priority 1: High Priority
4	RW	0	<b>USB Priority</b> 0: Low Priority 1: High Priority
3	RO	0	<b>Reserved</b>
2	RW	0	<b>IDE Priority</b> 0: Low Priority 1: High Priority
1	RO	0	<b>Reserved</b>
0	RW	0	<b>PCI1</b> 0: Low Priority 1: High Priority

**Offset Address: 51h (B0D17F7)**
**PCI to PCI (P2P) Bridge Related Control 1**
**Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	<b>Enable Subtract Decode for P2P Cycle</b>
6:4	RO	0	<b>Reserved</b>
3:0	RW	0	<b>Promotion Timer for HDAC in CCA</b>

**Offset Address: 52h (B0D17F7)**
**PCI to PCI Bridge Related Control 2**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	Promotion Timer for PCI1 in CCA
3:0	RW	0	Promotion Timer for IDEV in CCA

**Offset Address: 53h (B0D17F7)**
**PCI to PCI Bridge Related Control 3**
**Default Value: 01h**

Bit	Attribute	Default	Description
7:1	RO	0	Reserved
0	RW	1b	Enable B0D19F1 Rx9 read as 01h

**Offset Address: 54h (B0D17F7)**
**PCI to PCI Bridge Related Control 4**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	Reserved
3:0	RW	0	Promotion Timer for SATA in CCA

**Offset Address: 55h (B0D17F7) – Reserved**

**DRAM Configuration (56-57h)**
**Offset Address: 56h (B0D17F7)**
**DRAM Ending for Bank 6**
**Default Value: 01h**

Bit	Attribute	Default	Description
7:0	RW	01h	<b>DRAM Bank 6 Ending Address (HA[31:24])</b>

**Offset Address: 57h (B0D17F7)**
**DRAM Ending for Bank 7**
**Default Value: 01h**

Bit	Attribute	Default	Description
7:0	RW	01h	<b>DRAM Bank 7 Ending Address (HA[31:24])</b>

**Interrupt Discovery and Configuration Capability Block (58-60h)**
**Offset Address: 58h (B0D17F7)**
**Capability ID**
**Default Value: 08h**

Bit	Attribute	Default	Description
7:0	RO	08h	<b>Capability ID</b>

**Offset Address: 59h (B0D17F7)**
**Next Pointer**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	00h	<b>Next Pointer. Null</b>

**Offset Address: 5Ah (B0D17F7)**
**Interrupt Register Index**
**Default Value: 01h**

Bit	Attribute	Default	Description
7:0	RW	01h	<b>Interrupt Register Index</b>

**Offset Address: 5Bh (B0D17F7)**
**Capability Type**
**Default Value: 80h**

Bit	Attribute	Default	Description
7:0	RO	80h	<b>Capability Type</b>

**Offset Address: 5F-5Ch (B0D17F7)**
**Interrupt Register Data Port**
**Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	<b>Interrupt Register Data Port</b>

**Offset Address: 60h (B0D17F7) - Reserved**

**Shadow RAM Control (61-6Fh)**
**Offset Address: 61h (B0D17F7)**
**Page-C ROM Shadow Control**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00b	<b>CC000-CFFFFh Memory Space Access Control</b> 00: Read / Write Disable      01: Write Enable 10: Read Enable      11: Read / Write Enable
5:4	RW	0	<b>C8000-CBFFFh Memory Space Access Control</b>
3:2	RW	0	<b>C4000-C7FFFh Memory Space Access Control</b>
1:0	RW	0	<b>C0000-C3FFFh Memory Space Access Control</b>

**Offset Address: 62h (B0D17F7)**
**Page-D ROM Shadow Control**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00b	<b>DC000-DFFFFFFh Memory Space Access Control</b> 00: Read / Write Disable      01: Write Enable 10: Read Enable      11: Read / Write Enable
5:4	RW	0	<b>D8000-DBFFFh Memory Space Access Control</b>
3:2	RW	0	<b>D4000-D7FFFh Memory Space Access Control</b>
1:0	RW	0	<b>D0000-D3FFFh Memory Space Access Control</b>

**Offset Address: 63h (B0D17F7)**
**Page-E/F ROM, Memory Hole and SMI Decoding**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RO	0	<b>Reserved</b>
5:4	RW	0	<b>F0000-FFFFFh Memory Space Access Control</b>
3:2	RW	00b	<b>Memory Hole</b> 00: None      01: 512K – 640K 10: 15M – 16M (1M)      11: 14M – 16M (2M)
1	RW	0	<b>Disable Data Access on SMRAM (Page A, B) in SM Mode</b> 0: In SM mode, page A, B CPU Data R/W cycles are forwarded to the memory controller. 1: In SM mode, page A, B CPU Data R/W cycles are forwarded to the PCI bus  Notes: 1. This bit is effective when Rx83[0] is set to 0. 2. SMRAM page A, B Code R/W cycles are always forwarded to the memory controller in SM mode.
0	RW	0	<b>Enable Page A, B DRAM Access in Normal Mode</b> 0: Page A, B CPU R/W cycles could be forwarded to memory controller or PCI bus depends on the setting of bit 1 (RABKDOFF), the CPU operating mode (Normal or SM mode) as well as the type (Code or Data) of the CPU cycle. 1: Page A, B CPU R/W cycles (Code and Data) are always (in either Normal or SM mode) forwarded to the memory controller.

**Offset Address: 64h (B0D17F7)**
**Page-E ROM Shadow Control**
**Default Value: E4h**

Bit	Attribute	Default	Description
7:6	RW	11b	<b>EC000-EFFFFh Memory Space Access Control</b> 00: Read / Write Disable      01: Write Enable 10: Read Enable      11: Read / Write Enable
5:4	RW	10b	<b>E8000-EBFFFh Memory Space Access Control</b>
3:2	RW	01b	<b>E4000-E7FFFh Memory Space Access Control</b>
1:0	RW	00b	<b>E0000-E3FFFh Memory Space Access Control</b>

**Offset Address: 6F-65h (B0D17F7) - Reserved**

**Host PCI Bridge Control (70-7Fh)**
**Offset Address: 70h (B0D17F7)**
**CPU to PCI Flow Control 1**
**Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	<b>CPU to PCI Post-Write</b> 0: Disable 1: Enable C2P posted cycle could be delayed by PCI master cycles (i.e. PCI master access is allowed even if C2P buffer is not flushed).
6	RW	0	<b>Back Off PCI Master PCI to CPU Read (P2CR) While Data not return and PCI time-out</b> PCI timer is at Rx75[2:0] (RPTMS[2:0])
5:4	RW	00b	<b>PCI Master to DRAM Prefetch Control</b> x0: Always prefetch x1: Disable prefetch
3	RW	0	<b>PCI Short Latency for Read</b> Back off PCI master once the read data not return.
2	RW	0	<b>PCI to CPU Write Merge into 8QW for CCA</b>
1	RW	0	<b>Delay Transaction</b> 0: Disable 1: Enable
0	RW	0	<b>Cacheline Size</b> 0: 4QW 1: 8QW

**Offset Address: 71h (B0D17F7)**
**CPU to PCI Flow Control 2**
**Default Value: 48h**

Bit	Attribute	Default	Description
7	RW1C	0	<b>Retry Status</b> 0: No retry occurred 1: Retry occurred
6	RW	1b	<b>Action When Retry Timeout</b> 0: Retry forever (record status only) 1: Flush buffer (write) or return 0xFFFFFFFFh (read)
5:4	RW	00b	<b>Retry Count and Retry Back off</b> 00: Retry 2 times, back off CPU 01: Retry 16 times, back off CPU 10: Retry 4 times, back off CPU 11: Retry 64 times, back off CPU
3	RW	1b	<b>PCI Burst Timeout Enable</b> 0: Disable 1: Enable
2	RW	0	<b>SB IDSEL Control</b> SB device number = 17 or 5 0: AD26, AD27, AD28, AD29 (SB dev# = 17) 1: AD18, AD15, AD16, AD17 (SB dev# = 5)
1	RW	0	<b>Compatible TYPE#1 Configuration Cycle AD31</b> 0: Fix AD31 1: Support Type1 configuration cycle
0	RO	0	<b>Reserved</b>

**Offset Address: 72h (B0D17F7)**
**PCI P2C Read Caching and Prefetch Control**
**Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	<b>No Arbitration on PCI Bus During PCI-DMA</b>
6	RW	0	<b>V-Link Downstream Command / Data 1T Faster</b> 0: Decode V-Link down command after 1T sync. 1: Decode V-Link down command in 1T
5	RW	0	<b>Conservative Read Caching</b> Flush previously pre-fetched data when PCI master changes or starting address not being consecutive.
4	RW	0	<b>P2C Write Merge for PCI1</b>
3	RW	0	<b>P2CR Residue Data Flushed by the Next P2CR FRAME</b> 0: Prefetch data invalidate if FRAME de-assert without STOP 1: Prefetch data invalidate if C2P cycles
2	RW	0	<b>PCI Master Read Prefetch Data Residual</b>
1:0	RW	00b	<b>P2CR FIFO Prefetch Depth</b> 00: Prefetch if outstanding read <= 1 line 01: Prefetch if outstanding read <= 2 line: RPF2LN 10: Prefetch if outstanding read <= 3 line: RPF3LN 11: Prefetch if outstanding read <= 5 line: RPF5LN

**Offset Address: 73h (B0D17F7)**
**PCI Master Control**
**Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	<b>Reserved</b>
6	RW	0	<b>PCI Master 1-Wait State Write</b> 0: OWS 1: 1WS
5	RW	0	<b>PCI Master 1-Wait State Read</b> 0: OWS 1: 1WS
4	RW	0	<b>Disable Wait Flush Request Blocking PCI to CPU Write (P2CW) Cycle</b>
3	RW	0	<b>P2CR Caching Flush by NB SPCYC</b>
2:1	RO	0	<b>Reserved</b>
0	RW	0	<b>PCI Master Broken Timer Enable</b> 0: Disable 1: Enabled. Force into arbitration when there is no FRAME# 16 PCICLK after GNT

**Offset Address: 74h (B0D17F7)**
**South Bridge V-Link Registers**
**Default Value: 01h**

Bit	Attribute	Default	Description
7	RW	0	<b>Disable Dynamic CCA Clock Stop</b>
6	RW	0	<b>Disable Dynamic PCI1 Clock Stop (include VKCKG)</b>
5	RW	0	<b>Dynamic SVCTL Clock Stop</b>
4	RW	0	<b>LOCKCYC Flush P2C Cycles Before C2P</b>
3	RW	0	<b>LOCKCYC Block P2C Cycles</b>
2	RW	0	<b>APIC FSB Directly up to V-Link, not on PCI</b> 0: APIC FSB directly up to PCI Bus 1: APIC FSB directly up to V-Link
1	RW	0	<b>V-Link Pad Dynamic Turn Off IE Port</b>
0	RW	1b	<b>V-Link P2C Write Data Queue Full Bug Fix</b>

**Offset Address: 75h (B0D17F7)**
**PCI Arbitration 1**
**Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	<b>Arbitration Mode</b> 0: REQ-based (arbitrate at end of REQ#) 1: Frame-based (arbitrate at FRAME# asserts)
6:4	RW	0	<b>CPU Latency MLT2, MLT1, MLT0</b>
3	RW	0	<b>Disable PCI Master Time-out / Enable New Grant Mechanism</b> 0: Disable PCI master time-out 1: Enable new grant mechanism
2:0	RW	000b	<b>PCI Master Bus Timeout</b> 000: Disable 010: 2x16 PCLK 111: 7 x 16 PCLK
			001: 1x16 PCLK 011: 3x16 PCLK

**Offset Address: 76h (B0D17F7)**
**PCI Arbitration 2**
**Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	<b>IO Port 22 Enable (SB)</b> 0: CPU access to IO address 22 is passed on to the PCI bus 1: CPU access to IO address 22 is processed internally IO
6	RW	0	<b>PCI Bus Parking at the Last PCI Master</b>
5:4	RW	00b	<b>Master Priority Rotation Control</b> 00: Disable 01: Grant to CPU after every PCI master grant 10: Grant to CPU after every 2 PCI master grant 11: Grant to CPU after every 3 PCI master grant
3:2	RW	00b	<b>Select REQ as RQ4</b> 00: REQ4 01: REQ0 10: REQ1 11: REQ2
1	RO	0	<b>Reserved</b>
0	RW	0	<b>Enable RQ4 as High Priority Master</b> 0: Disable 1: Enable

**Offset Address: 77h (B0D17F7)**
**PCI Traffic Control**
**Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	<b>Reserved</b>
6	RW	0	<b>C2PRA Blocked by PCI1 FIFO Empty Instead of PCI to CPU Write Ack (P2CWA) if Bit 6 = 1</b> C2PRA is blocked by P2CWA when Rx4F[0] = 1 Note: it needs to work with Rx4F[0] (RP2CFLSH) assert.
5	RW	0	<b>Put APIC Address Bit 2 to Bit 0 for Information Lost Due to QW-based Address.</b>
4:3	RW	00b	<b>Read FIFO Timer</b> 00: No timer 10: Timeout after 4ms 01: Timeout after 1ms 11: Timeout after 16ms
2	RW	0	<b>GART Table 3.0, else 2.0 Format</b> 0: 2.0 1: 3.0
1	RW	0	<b>GART Table Enable for South Bridge</b>
0	RO	0	<b>Reserved</b>

**Offset Address: 78h (B0D17F7)**
**PCI PAD Control**
**Default Value: 01h**

Bit	Attribute	Default	Description
7	RW	0	<b>Data Pad (AD, PAR) Driving Control</b>
6	RW	0	<b>Data Pad (AD, PAR) Slew Rate Control</b>
5	RW	0	<b>Strobe Pad (GNT) Driving Control</b>
4	RW	0	<b>Strobe Pad (GNT) Slew Rate Control</b>
3:2	RW	0	<b>Data in Delay</b>
1	RO	0	<b>Reserved</b>
0	RO	1b	<b>Bridge is V2X Capable</b> Always reads 1

**Offset Address: 79h (B0D17F7)**
**PCI V2X Data / Strobe Out Delay Control**
**Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	<b>Data Out Change Based Clock</b> 0: Data out changed by internal clock 1: Data out changed by external PCICLK
6:4	RW	000b	<b>Data Out Delay</b> 000: No delay 001: Delay 0.7ns 010: Delay 1.3ns 011: Delay 2.0ns 100: Delay 3.1ns 101: Delay 3.8ns 110: Delay 4.4ns 111: Delay 5.1ns
3	RW	0	<b>Strobe Out Source Clock</b> 0: Strobe out from internal clock 1: Strobe out from external PCICLK
2:0	RW	000b	<b>Strobe Out Delay</b> 000: No delay 001: Delay 0.7ns 010: Delay 1.3ns 011: Delay 2.0ns 100: Delay 3.1ns 101: Delay 3.8ns 110: Delay 4.4ns 111: Delay 5.1ns

**Offset Address: 7Ah (B0D17F7)**
**PCI V2X Device Capability**
**Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	<b>PREQ's Device is V2X Capability</b>
6	RW	0	<b>REQ6's Device is V2X Capability</b>
5	RW	0	<b>REQ5's Device is V2X Capability</b>
4	RW	0	<b>REQ4's Device is V2X Capability</b>
3	RW	0	<b>REQ3's Device is V2X Capability</b>
2	RW	0	<b>REQ2's Device is V2X Capability</b>
1	RW	0	<b>REQ1's Device is V2X Capability</b>
0	RW	0	<b>REQ0's Device is V2X Capability</b> 0: No capability of V2X 1: With capability of V2X

**Offset Address: 7Bh (B0D17F7)**
**REQ Status**
**Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	<b>PREQ Status</b>
6	RO	0	<b>REQ6 Status</b>
5	RO	0	<b>REQ5 Status</b>
4	RO	0	<b>REQ4 Status</b>
3	RO	0	<b>REQ3 Status</b>
2	RO	0	<b>REQ2 Status</b>
1	RO	0	<b>REQ1 Status</b>
0	RO	0	<b>REQ0 Status</b> 0: Inactive 1: Active

**Offset Address: 7Ch (B0D17F7)**
**LDT Related Control**
**Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	<b>Reserved</b>
6	RW	0	<b>Enable Warm Reset When Host Bus Error Occurs</b> 0: V3_HOST_SERR not result to warm reset 1: V3_HOST_SERR result to warm reset. Allow system back from LDT sync flood error.
5	RW	0	<b>Enable Clear CFGCS for Each Configuration Cycle</b> 0: CFC IO cycle not clears CFGCS 1: CFC IO cycle always clears CFGCS. Allow CPU issue CF8/CFC IO cycles without confused with configuration cycles.
4	RW	0	<b>Enable LDT STPGNT Block C2P Response</b> 0: C2P response not blocked by STPCLK/SMI message 1: C2P response blocked by STPCLK/SMI message. Avoid CPU from execution the next instruction when entering suspend mode or system management mode.
3	RW	0	<b>Enable LDT APIC Mode</b> 0: Cfg of 59~5F not remapping to I/O APIC cycle 1: Cfg of 59~5F mapping to I/O APIC cycle
2	RW	0	<b>Enable NMI / SMI / INIT for FSB</b> 0: NMI / SMI / INIT to CPU through external pins 1: NMI / SMI / INIT to CPU through front side bus delivery
1	RW	0	<b>Enable Upstream Message</b> 0: STPCLK/A20G/IGNNE to CPU through external pins 1: STPCLK/A20G/IGNNE to CPU through up message
0	RW	0	<b>Enable LDT Mode</b> 0: FERR from external pin. 1: FERR from downstream message

**Offset Address: 7Dh (B0D17F7) - Reserved**
**Offset Address: 7Eh (B0D17F7)**
**Virtual Channel 0 Arbitration Promoting Timer**
**Default Value: 12h**

Bit	Attribute	Default	Description
7:5	RW	000b	<b>Normal Priority REQ Promote Timer</b> 000: Disable                    001: 120ns 010: 240ns                    011: 360ns ...                              111: 840ns
4:0	RO	12h	<b>Reserved</b>

**Offset Address: 7Fh (B0D17F7)**
**Virtual Channel 1 Arbitration Promoting Timer**
**Default Value: 12h**

Bit	Attribute	Default	Description
7:5	RW	000b	<b>High Priority REQ Promote Timer</b> 000: Disable                    001: 120ns 010: 240ns                    011: 360ns ...                              111: 840ns
4:0	RO	12h	<b>Reserved</b>

**GART Operation (80-B6h)**
**Offset Address: 83-80h (B0D17F7)**
**Graphic Aperture Base Configuration**
**Default Value: 0000 0008h**

Bit	Attribute	Default	Description
31:28	RW	0	<b>Upper Programmable Base Address</b>
27:20	RW	0	<b>Lower Programmable Base Address</b> The aperture base address bit acts as if hardwired to 0 if Rx84[7:0] bit is 0.
19:0	RO	0008h	<b>Reserved</b> (Do Not Program) Indicate that Graphic Aperture range alignment in 1M Bytes Bit 3 indicates that Graphic Aperture range is pre-fetchable.

**Table 15. Graphics Aperture Base Address Table**

Aperture Base Rx80[7:0]	27	26	25	24	23	22	21	20	
Aperture Size Rx84[7:0]	7	6	5	4	3	2	1	0	Aperture Size
	RW	<b>1M</b>							
	RW	0	<b>2M</b>						
	RW	RW	RW	RW	RW	RW	0	0	<b>4M</b>
	RW	RW	RW	RW	RW	0	0	0	<b>8M</b>
	RW	RW	RW	RW	0	0	0	0	<b>16M</b>
	RW	RW	RW	0	0	0	0	0	<b>32M</b>
	RW	RW	0	0	0	0	0	0	<b>64M</b>
	RW	0	0	0	0	0	0	0	<b>128M</b>
	0	0	0	0	0	0	0	0	<b>256M</b>

Note: This range is defined prefetchable.

**Offset Address: 84h (B0D17F7)**
**Graphic Aperture Size**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0000 0000b	<b>Graphic Aperture Size</b> 1111 1111: 1M 1111 1100: 4M 1111 0000: 16M 1100 0000: 64M 0000 0000: 256M 1111 1110: 2M 1111 1000: 8M 1110 0000: 32M 1000 0000: 128M

**Offset Address: 87-85h (B0D17F7) - Reserved**

**Offset Address: 8B-88h (B0D17F7)**
**Graphic Aperture Translation Look-Aside Table Base Address**
**Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:12	RW	0	<b>Pointer to the Base of the Translation Table Used to Map Addresses in Aperture Range</b>
11:2	RO	0	<b>Reserved</b>
1	RW	0	<b>Enable Graphic Aperture Address A[31:28]</b>
0	RO	0	<b>Reserved</b>

**Offset Address: 93-8Ch (B0D17F7) - Reserved**
**Offset Address: 95-94h (B0D17F7)**
**Graphic Aperture Size for AGP3.0**
**Default Value: 0000h**

Bit	Attribute	Default	Description
15:12	RO	0	<b>Reserved</b>
11:0	RW	0000 0000 0000b	<b>Graphic Aperture Size for AGP3.0</b> 1111 0011 1111: 4M                            1111 0011 1110: 8M 1111 0011 1100: 16M                          1111 0011 1000: 32M 1111 0011 0000: 64M                          1111 0010 0000: 128M 1111 0000 0000: 256M                         1110 0000 0000: 512M 1100 0000 0000: 1G                              1000 0000 0000: 2G <= Max 0000 0000 0000: 4G

**Offset Address: B6-96h (B0D17F7) - Reserved**

**V-Link 8X Compensation Circuit (B7-E3h)**
**Offset Address: B7h (B0D17F7)**
**VKCKG Output Duty Cycle Setting**
**Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	SB V-Link Output Strobe Rise Time Control [1]
6	RW	0	SB V-Link Output Strobe Rise Time Control [0]
5	RW	0	SB V-Link Output Strobe Fall Time Control [1]
4	RW	0	SB V-Link Output Strobe Fall Time Control [0]
3	RW	0	SB V-Link Output R-port Rise Time Control [1]
2	RW	0	SB V-Link Output R-port Rise Time Control [0]
1	RW	0	SB V-Link Output R-port Fall Time Control [1]
0	RW	0	SB V-Link Output R-port Fall Time Control [0]

**Offset Address: B8h (B0D17F7)**
**SB V-Link Compensation Control**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	V-Link Auto-Compensation PMOS Output Value
4	RO	0	Reserved
3:1	RO	0	V-Link Auto-Compensation NMOS Output Value
0	RO	0	Reserved

**Offset Address: B9h (B0D17F7)**
**SB V-Link Manual Driving Control - Strobe**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RW	0	Manual Setting - SB V-Link Strobe Pull-up (PMOS)
4	RO	0	Reserved
3:1	RW	0	Manual Setting - SB V-Link Strobe Pull down (NMOS)
0	RO	0	Reserved

**Offset Address: BAh (B0D17F7)**
**SB V-Link Manual Driving Control - Data**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RW	0	Manual Setting - SB V-Link Data Pull-up (PMOS)
4	RO	0	Reserved
3:1	RW	0	Manual Setting - SB V-Link Data Pull-down (NMOS)
0	RO	0	Reserved

**Offset Address: BBh (B0D17F7)**
**V-Link PAD Related Register**
**Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	<b>Compensation Selection</b> 0: Auto compensation (values in Rx B8[7:5]) 1: Manual setting (use the values in Rx B9-BA)
6	RW	0	SB V-Link Output Data Rising Time Control [1]
5	RW	0	SB V-Link Output Data Rising Time Control [0]
4	RW	0	SB V-Link Output Data Falling Time Control [1]
3	RW	0	SB V-Link Output Data Falling Time Control [0]
2	RW	0	SB V-Link Input Reference Voltage Select in 4X If Bit 2 (VREF4XSEL) = 1, VREF4X=0.9V If Bit 2 (VREF4XSEL) = 0, VREF4X=0.75V
1:0	RW	00b	<b>SB V-Link VKCKG Delay Control</b> Bits[1:0] Input strobe (DNSTB) delay 00 0.3ns 01 0.4ns 10 0.5ns 11 0.6ns

**Offset Address: BCh (B0D17F7)**
**V-Link Auto Compensation Termination Resistor Status**
**Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	<b>N Resistor Check Flag for the SB Termination Resistor</b> 0: Abnormal condition occurred 1: Normal operation
6	RO	0	<b>P Resistor Check Flag for the SB Termination Resistor</b> 0: Abnormal condition occurred 1: Normal operation
5	RO	0	<b>N Pull Down Driving Check Flag for the SB Termination Resistor</b> 0: Abnormal condition occurred 1: Normal operation.
4	RO	0	<b>P Pull Down Driving Check Flag for the SB Termination Resistor</b> 0: Abnormal condition occurred 1: Normal operation.
3	RO	0	<b>Reserved</b>
2:0	RO	000b	<b>SB V-Link Auto comp Termination Resistor Value</b> 000: Largest Resistor ... 111: Smallest Resistor

**Offset Address: BDh (B0D17F7)**
**V-Link Manual Termination Resistor Value**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RO	0	<b>Reserved</b>
2:0	RW	000b	<b>V-Link Manual Termination Resistor Value</b> 000: Largest Resistor ... 111: Smallest Resistor

**Offset Address: C8-BEh (B0D17F7) – Reserved**
**Offset Address: C9h (B0D17F7)**
**CPU to PCI Flow Control III**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	<b>Reserved</b>
4:2	RW	0	<b>PCI Master TRDY Timeout</b> 0: Reserved (which cause immediately retry) 1: 1*8 PCICLK 2: 2*8 PCICLK 3: 3*8 PCICLK 4: 4*8 PCICLK 5: 5*8 PCICLK 6: 6*8 PCICLK 7: 7*8 PCICLK
1	RW	0	<b>Back off PCI Master while can't get TRDY and PCI time out (PCI timer is at RXC9[4:2])</b>
0	RO	0	<b>Reserved</b>

**Offset Address: E3-CAh (B0D17F7) - Reserved**

### **DRAM Above 4G Support (E4-FFh)**

**Offset Address: E4h (B0D17F7)**

### **Low Top Address - Low**

**Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	<b>Low Top Address – Low</b>
3:0	RW	0	<b>DRAM Granularity - (Powell)</b>
			<b>Total DRAM</b> <b>RMEMUNIT</b> <b>less than</b> <b>Granularity</b> 0                  4G                  16M 1                  8G                  32M 2                  16G                64M 3                  32G                128M 4                  64G                256M
			<b>RANK Ending Address Formula:</b> $ENDxA[35:24] = RENDxA \ll RMEMUNIT; (x = 0,1,2,3,4,5,6,7)$

**Offset Address: E5h (B0D17F7)**

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## Low Top Address - High

**Default Value:** 00h

Bit	Attribute	Default	Description
7:0	RW	0	<b>Low Top Address – High</b>

**Offset Address: E6h (B0D17F7)**

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## SMM and APIC Decoding

**Default Value:** 01h

Bit	Attribute	Default	Description
7:4	RO	0	<b>Reserved</b>
3	RW	0	<b>MSI Support (Processor Message Enable)</b> 0: Cycles accessing FEE <sub>x</sub> _xxxx from masters are passed to PCI1 (PCIC will not claim) 1: Cycles accessing FEE <sub>x</sub> _xxxx from masters are passed to the Host side for snooping
2	RO	0	<b>Top SMM Enable</b> 0: Disable 1: Enable
1	RW	0	<b>High SMM Enable</b>
0	RW	lb	<b>Compatible SMM Enable</b> 0: Disable 1: Enable

**Offset Address: FB-E7h (B0D17F7) – Reserved**

**Offset Address: FCh (B0D17F7)**

## V-Link Backdoor Control

**Default Value:** 00h

Bit	Attribute	Default	Description
7:3	RO	0	<b>Reserved</b>
2	RW	0	<b>PCI-to-PCIe Bridge Control</b> 0: PCI-to-PCIe Bridge as P2P Bridge 1: PCI-to-PCIe Bridge as host Bridge
1:0	RO	0	<b>Reserved</b>

#### **Offset Address: FF-FDh (B0D17F7) – Reserved**

## Bus 0 Device 18 Function 0 (B0D18F0): LAN

All registers are located in the Device 18 Function 0 PCI configuration space of the VT8237S. These registers are accessed through PCI configuration mechanism #1 via I/O address CF8 / CFC.

### PCI Configuration Space Header Registers (0-3Fh)

#### Offset Address: 1-0h (B0D18F0)

**Vendor ID**

**Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	<b>Vendor ID</b>

#### Offset Address: 3-2h (B0D18F0)

**Device ID**

**Default Value: 3065h**

Bit	Attribute	Default	Description
15:0	RO	3065h	<b>Device ID</b>

#### Offset Address: 5-4h (B0D18F0)

**Command**

**Default Value: 0000h**

Bit	Attribute	Default	Description
15:11	RO	0	<b>Reserved.</b> Always reads 0.
10	RW	0	<b>Interrupt Disable</b>
9:3	RO	0	<b>Reserved.</b> Always reads 0.
2	RW	0	<b>Bus Master.</b> Always reads 0.
1	RW	0	<b>Memory Space.</b> Always reads 0.
0	RW	0	<b>I/O Space</b>

#### Offset Address: 7-6h (B0D18F0)

**Status**

**Default Value: 0210h**

Bit	Attribute	Default	Description
15	RO	0	<b>Detected Parity Error</b> Always reads 0
14	RO	0	<b>Signaled System Error</b> Always reads 0
13	RO	0	<b>Received Master Abort</b> Always reads 0
12	RO	0	<b>Received Target Abort</b> Always reads 0
11	RO	0	<b>Signaled Target Abort</b> Always reads 0
10:9	RO	01b	<b>DEVSEL# Timing</b> Fixed at 01b (Medium)
8	RO	0	<b>Data Parity Detected</b>
7	RO	0	<b>Fast Back-to-Back Capable</b>
6	RO	0	<b>Reserved</b>
5	RO	0	<b>66 MHz Capable</b>
4	RO	1b	<b>Capabilities (e.g. PCI Power Management)</b>
3	RO	0	<b>Interrupt Status</b>
2:0	RO	0	<b>Reserved</b>

**Offset Address: 8h (B0D18F0)**
**Revision ID**
**Default Value: 7Ch**

Bit	Attribute	Default	Description
7:0	RO	7Ch	<b>Revision ID</b>

**Offset Address: 9h (B0D18F0)**
**Program Interface**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	<b>Program Interface</b>

**Offset Address: 0Ah (B0D18F0)**
**Sub Class Code**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	<b>Sub Class Code</b>

**Offset Address: 0Bh (B0D18F0)**
**Class Code**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	<b>Class Code</b>

**Offset Address: 0Ch (B0D18F0)**
**Cache Line Size**
**Default Value: 00h**

This register must be implemented by master devices that can generate the memory-write-and-invalidate command.

Bit	Attribute	Default	Description
7:0	RW	0	<b>Cache Line Size</b>

**Offset Address: 0Dh (B0D18F0)**
**Latency Timer**
**Default Value: 00h**

This register must be implemented as writable by any master that can burst more than two data phases.

Bit	Attribute	Default	Description
7:0	RW	0	<b>Latency Timer</b>

**Offset Address: 0Eh (B0D18F0)**
**Header Type**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	<b>Header Type</b>

**Offset Address: 0Fh (B0D18F0)**
**BIST**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	<b>BIST</b>

**Offset Address: 13-10h (B0D18F0)**
**I/O Base Address**
**Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	<b>I/O Base Address</b>

**Offset Address: 17-14h (B0D18F0)**
**Memory Base Address**
**Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	Memory Base Address

**Offset Address: 27-18h (B0D18F0) - Reserved**
**Offset Address: 2B-28h (B0D18F0)**
**Card Bus CIS Pointer**
**Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	Card Bus CIS Pointer

**Offset Address: 2F-2Ch (B0D18F0) - Reserved**
**Offset Address: 33-30h (B0D18F0)**
**Expansion ROM Base**
**Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	Expansion ROM Base

**Offset Address: 34h (B0D18F0)**
**Capabilities Offset**
**Default Value: 40h**

Bit	Attribute	Default	Description
7:0	RO	40h	<b>Capabilities Offset</b> Offset into the LAN function PCI space pointing to the location of the first item in the function's capability list.

**Offset Address: 3B-35h (B0D18F0) - Reserved**
**Offset Address: 3Ch (B0D18F0)**
**Interrupt Line**
**Default Value: 00h**

Bit	Attribute	Default	Description	
7:4	RO	0	<b>Reserved</b> Always reads 0	
3:0	RO	0000b	<b>LAN Interrupt Routing</b> 0000: Disabled 0010: Reserved 0100: IRQ4 0110: IRQ6 1000: IRQ8 1010: IRQ10 1100: IRQ12 1110: IRQ14 APIC (See Device 17 Function 0 Rx58[6]) x001: IRQ17	0001: IRQ1 0011: IRQ3 0101: IRQ5 0111: IRQ7 1001: IRQ9 1011: IRQ11 1101: IRQ13 1111: Disabled x000: IRQ16 x010: IRQ18

**Offset Address: 3Dh (B0D18F0)**
**Interrupt Pin**
**Default Value: 01h**

Bit	Attribute	Default	Description
7:0	RO	01h	<b>Interrupt Routing Mode</b> 00h: Legacy mode interrupt routing 01h: Native mode interrupt routing

**Offset Address: 3F-3Eh (B0D18F0) – Reserved**

## LAN-Specific PCI Configuration Registers (40-47h)

**Offset Address: 40h (B0D18F0)**

## **Capability ID**

**Default Value: 01h**

Bit	Attribute	Default	Description
7:0	RO	01h	<b>Capability ID</b> Identifies the linked list item as being PCI power management registers Always reads 01h

**Offset Address: 41h (B0D18F0)**

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### **Next Item Pointer**

**Default Value:** 00h

Bit	Attribute	Default	Description
7:0	RO	00h	<b>Next Item Pointer</b> Always reads 00h Offset into the LAN function PCI space pointing to the location of the next item in the function's capability list.

**Offset Address: 43-42h (B0D18F0)**

## **Power Management Configuration**

**Default Value:** 3C02h

**Offset Address: 47-44h (B0D18F0)**

## **Power Management Control / Status**

**Default Value:** 0000 0000h

Bit	Attribute	Default	Description
31:0	RWC	0	<b>Control / Status</b> See Power Management Specification 1.0

## LAN I/O Registers (0-FFh)

### I/O Offset Address: 5-0h

#### Ethernet Address

**Default Value:** nnh

Unless the EEPROM is disabled, the Ethernet Address is loaded to this register from the EEPROM every time the system starts up.

Bit	Attribute	Default	Description
63:0	RW	nnh	<b>Ethernet Address</b>

### I/O Offset Address: 6h

#### Receive Control

**Default Value:** 00h

Bit	Attribute	Default	Description
7:5	RW	0	<b>Reserved</b> Do not program
4	RW	0	<b>Physical Address Packets Accepted</b> 0: Packets with a physical destination address are not accepted 1: All packets with a physical destination address are accepted
3	RW	0	<b>Broadcast Packets Accepted</b> 0: Broadcast packets are rejected 1: Broadcast packets are accepted
2	RW	0	<b>Multicast Packets Accepted</b> 0: Multicast packets are rejected 1: Multicast packets are accepted
1	RW	0	<b>Small Packets Accepted</b> 0: Packets smaller than 64 bytes are rejected 1: Packets smaller than 64 bytes are accepted
0	RW	0	<b>Error Packets Accepted</b> 0: Packets with receive errors are rejected 1: Packets with receive errors are accepted

### I/O Offset Address: 7h

#### Transmit Control

**Default Value:** 00h

Bit	Attribute	Default	Description
7:3	RO	0	<b>Reserved</b>
2:1	RW	00b	<b>Transmit Loopback Mode</b> 00: Normal 01: Internal loopback (signal is looped back to the host from the MAC) 10: MII loopback (signal is looped back to the host from the PHY) 11: Reserved- (Do Not Program)
0	RO	0	<b>Reserved</b>

### I/O Offset Address: 8h

#### Command 0

**Default Value:** 00h

Bit	Attribute	Default	Description
7	RO	0	<b>Reserved</b>
6	RW	0	<b>Receive Poll Demand</b> If this bit is set to 1, the Receive Descriptor (RD) will be polled once (this bit will be cleared by hardware after the polling is complete)
5	RW	0	<b>Transmit Poll Demand</b> If this bit is set to 1, the Transmit Descriptor (TD) will be polled once (this bit will be cleared by hardware after the polling is complete)
4	RW	0	<b>Transmit Process</b> 0: Transmit engine disabled      1: Transmit engine enabled (transmit may occur)
3	RW	0	<b>Receive Process</b> 0: Receive disabled      1: Receive enabled
2	RW	0	<b>Stop NIC</b> 0: NIC enabled      1: NIC disabled (transmit/receive cannot occur)
1	RW	0	<b>Start NIC</b> 0: No command entered      1: Start the NIC
0	RO	0	<b>Reserved</b> (Do Not Program)

I/O Offset Address: 9h
**Command 1**
**Default Value: 08h**

Bit	Attribute	Default	Description
7	RW	0	<b>Software Reset</b> 0: No reset 1: Reset the MAC
6	RW	0	<b>Receive Poll Demand 1</b> This bit functions the same as Rx8[6]. The function can be enabled by setting either bit (for backward compatibility).
5	RW	0	<b>Transmit Poll Demand 1</b> This bit functions the same as Rx8[5]. The function can be enabled by setting either bit (for backward compatibility).
4	RO	0	<b>Reserved</b>
3	RW	1b	<b>TD / RD Auto Polling</b> 0: Enable (polling interval is determined by Rx6F[2:0] ) 1: Disable
2	RW	0	<b>Full Duplex</b> 0: Set MAC to half duplex mode 1: Set MAC to full duplex mode
1:0	RO	0	<b>Reserved</b> (Do Not Program)

I/O Offset Address: 0Ch
**Interrupt Status 0**
**Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	<b>CRC or Miss Packet Tally Counter Overflow</b> Set if either counter overflows (both counters are 16 bits)
6	RW	0	<b>PCI Bus Error</b> Set if PCI bus error occurred.
5	RW	0	<b>Receive Buffer Link Error</b> Set when there is not enough buffer space for a packet requiring multiple buffers.
4	RO	0	<b>Reserved</b> (Do Not Program)
3	RW	0	<b>Transmit Error (Packet Transmit Aborted)</b> Set due to excessive collisions (more than 16), transmit underflow, or transmit data linking error
2	RW	0	<b>Receive Error</b> Set due to CRC error, frame alignment error, FIFO overflow, or received data linking error
1	RW	0	<b>Packet Transmitted Successfully</b>
0	RW	0	<b>Packet Received Successfully</b>

I/O Offset Address: 0Dh
**Interrupt Status 1**
**Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	<b>General Purpose Interrupt</b> This bit is set when there is a general purpose interrupt event (Rx84). This bit is set when any bit in Rx84 equals one and when its corresponding mask bit in Rx86 also equals one.
6	RW	0	<b>Port State Change (PHY)</b>
5	RW	0	<b>Transmit Abort Due to Excessive Collisions</b> Set when there is a transmit error that is due to excessive collisions. Alternatively, Rx0C[3] is set for all transmit errors.
4	RO	0	<b>Receive Buffer Full</b> Set when there is no more buffer space available in system memory.
3	RW	0	<b>Receive Packet Race</b> Set when there is not enough room in the FIFO to receive an additional packet.
2	RW	0	<b>Receive FIFO Overflow</b>
1:0	RO	0	<b>Reserved</b>

**I/O Offset Address: 0Eh**
**Interrupt Mask 0**
**Default Value: 00h**

Bits correspond to the bits in Interrupt Status Register 0. An interrupt is generated when corresponding bits in both registers equal 1.

Bit	Attribute	Default	Description
7:0	RW	0	<b>Interrupt Mask 0</b>

**I/O Offset Address: 0Fh**
**Interrupt Mask 1**
**Default Value: 00h**

Bits correspond to the bits in Interrupt Status Register 1. An interrupt is generated when corresponding bits in both registers equal 1.

Bit	Attribute	Default	Description
7:0	RW	0	<b>Interrupt Mask 1</b>

**I/O Offset Address: 17-10h**
**Multicast Address**
**Default Value: 0000 0000 0000 0000h**

The value in this register determines which Multicast addresses are received.

Bit	Attribute	Default	Description
63:0	RW	0	<b>Multicast Address</b>

**I/O Offset Address: 1B-18Fh**
**RX Address**
**Default Value: 0000 0000h**

This register reports the transmit transcriptor address that is being accessed.

Bit	Attribute	Default	Description
31:0	RW	0	<b>RX Address</b>

**I/O Offset Address: 1F-1CFh**
**TX Address**
**Default Value: 0000 0000h**

This register reports the transmit transcriptor address that is being accessed.

Bit	Attribute	Default	Description
31:0	RW	0	<b>TX Address</b>

**I/O Offset Address: 23-20h**
**Receive Status**
**Default Value: 0000 0400h**

Bit	Attribute	Default	Description
31	RW	0	<b>Descriptor Owner</b> 0: Descriptor Owned By Host (NIC cannot access descriptor) 1: Descriptor Owned by NIC (NIC can access descriptor) Note: This bit has no default so must be set by the driver at initialization.
30:27	RO	0	<b>Reserved</b>
26:16	RO	0	<b>Received Packet Length</b>
15	RO	0	<b>Received Packet Successfully</b>
14	RO	0	<b>Reserved</b>
13	RO	0	<b>NIC Accepted Multicast Packet</b>
12	RO	0	<b>NIC Accepted Broadcast Packet</b>
11	RO	0	<b>NIC Accepted Physical Address Packet</b>
10	RO	1b	<b>Chain Buffer</b> Set if packet too large to occupy a single receive descriptor.
9:8	RO	0	<b>Buffer Descriptor Start / End</b> For packets too large to fit into a single receive descriptor and thus occupy multiple RD's, this field reports whether this RD is the start, middle or end. 00: Chain Buffer Middle Descriptor 01: Chain Buffer End Descriptor 10: Chain Buffer Start Descriptor 11: Single Buffer Descriptor (packet occupies only one descriptor)
7	RO	0	<b>Reserved</b>
6	RO	0	<b>System Error</b>
5	RO	0	<b>Runt Packet (&lt; 64 bytes)</b>
4	RO	0	<b>Long Packet (&gt; 2500 bytes)</b>
3	RO	0	<b>FIFO Overflow Error</b>
2	RO	0	<b>Frame Alignment Error</b>
1	RO	0	<b>CRC Error</b>
0	RO	0	<b>Receiver Error</b>

**I/O Offset Address: 27-24h**
**Rx Data Buffer Control**
**Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:11	RO	0	<b>Reserved</b>
10:0	RO	0	<b>Rx Data Buffer Size</b> The receive data buffer size for this descriptor. The total byte count of the entire frame will be stored in the last descriptor.

**I/O Offset Address: 2B-28h**
**Rx Data Buffer Start Address**
**Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	<b>Rx Data Buffer Start Address</b>

**I/O Offset Address: 2F-2Ch**
**Rx Data Buffer Branch Address**
**Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	<b>Rx Data Buffer Branch Address</b>

Note: Rx20-2F reflect values from the RD being accessed.

I/O Offset Address: 43-40h
**Transmit Status**
**Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RW	0	<b>Descriptor Owner</b> 0: Descriptor Owned By Host (NIC cannot access descriptor) 1: Descriptor Owned by NIC (NIC can access descriptor) This bit has no default so must be set by the driver at initialization.
30:16	RO	0	<b>Reserved</b>
15	RO	0	<b>Transmit Error</b> 0: Transmit Successful      1: Excessive Collisions During Transmit Attempt
14	RO	0	<b>Reserved</b>
13	RO	0	<b>System Error</b>
12	RO	0	<b>Invalid TD Format or Structure or TD Overflow</b>
11	RO	0	<b>Reserved</b>
10	RO	0	<b>Carrier Sense Lost During Transmit</b>
9	RO	0	<b>Out of Window Collision (collision outside initial 64 bytes)</b>
8	RO	0	<b>Transmit Abort (Excessive Collisions)</b>
7	RO	0	<b>CD Heartbeat Issued (10BaseT Only)</b>
6:5	RO	0	<b>Reserved</b>
4	RO	0	<b>Collision Detected During Transmit</b>
3:0	RO	0	<b>Collision Retry Count</b>

I/O Offset Address: 47-44h
**Tx Data Buffer Control**
**Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RO	0	<b>Reserved</b>
23	RO	0	<b>Send-Complete Interrupt</b> 0: Interrupt not generated      1: Interrupt generated after send complete
22	RO	0	<b>End of Transmit Packet</b> For packets too large to fit into a single transmit descriptor and thus occupy multiple TD's, this bit reports whether this TD is the End TD. 0: This TD is not the End TD      1: This TD is the End TD
21	RO	0	<b>Start of Transmit Packet</b> For packets too large to fit into a single transmit descriptor and thus occupy multiple TD's, this bit reports whether this TD is the Start TD. 0: This TD is not the Start TD      1: This TD is the Start TD
20:17	RO	0	<b>Reserved</b>
16	RO	0	<b>Disable CRC Generation</b>
15	RO	0	<b>Chain Buffer</b>
14:11	RO	0	<b>Reserved</b>
10:0	RO	0	<b>Tx Data Buffer Size</b> The transmit data buffer size for this descriptor. The total byte count of the entire frame will be stored in the last descriptor

I/O Offset Address: 4B-48h
**Tx Data Buffer Start Address**
**Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	<b>Tx Data Buffer Start Address</b>

I/O Offset Address: 4F-4Ch
**Tx Data Buffer Branch Address**
**Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:4	RO	0	<b>Tx Data Buffer Branch Address</b>
3:1	RO	0	<b>Reserved</b>
0	RO	0	<b>Tx Interrupt Enable</b> 0: Issue interrupt for this packet      1: No interrupt generated

### **I/O Offset Address: 6Ch**

## **PHY Address**

**Default Value:** 01h

Bit	Attribute	Default	Description
7:6	RW	00b	<b>MII Management Polling Timer Interval (Polling PHY)</b> 00: 1024 MDC Clock Cycles 01: 512 MDC Clock Cycles 10: 128 MDC Clock Cycles 11: 64 MDC Clock Cycles MDC is an internal clock with a 960 ns cycle time.
5	RW	0	<b>Accelerate MDC Speed</b> 0: Normal 1: 4x Accelerated
4:0	RW	01h	<b>Extended PHY Device Address</b> Stored from EEPROM during power-up or EEPROM auto-reload but can be programmed by software

#### I/O Offset Address: 6Dh

## MII Status

**Default Value:** 13h

Bit	Attribute	Default	Description	
7	RW	0	<b>PHY Reset</b> 0: PHY reset not asserted	1: PHY reset asserted
6:5	RO	0	<b>Reserved</b>	
4	RW	1b	<b>PHY Option</b> 0: PHY address updated from EEPROM	1: Use default PHY address of 0001h
3	RW	0	<b>PHY Device Received Error</b> 0: No MII error	1: MII Error
2	RO	0	<b>Reserved</b>	
1	RW	1b	<b>Link Failure</b> 0: Link successful	1: Link unsuccessful (no connection)
0	RW	1b	<b>PHY Speed</b> 0: 100 Mb	1: 10 Mb

### **I/O Offset Address: 6Eh**

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## Buffer Control 0

**Default Value:** 00h

Bit	Attribute	Default	Description			
7:3	RO	0	<b>Reserved.</b> Always reads 0			
2:0	RW	000b	<b>DMA Length</b>			
			000:32 bytes	8 DW	001:64 bytes	16 DW
			010:128 bytes	32 DW	011:256 bytes	64 DW
			100:512 bytes	128 DW	101:1024 bytes	256 DW
			11x:Store & Forward			

**I/O Offset Address: 6Fh**

## **Buffer Control 1**

**Default Value: 00h**

Bit	Attribute	Default	Description								
7:3	RO	0	<b>Reserved</b>								
2:0	RW	000b	<p><b>Polling Interval Timer</b></p> <p>This field determines the polling interval when TX / RX Auto-Polling is enabled (LAN I/O Rx09[3]=0).</p> <table> <tr> <td>000: <math>2^{15}</math> V-Link Clocks</td> <td>001: <math>2^{17}</math> V-Link Clocks</td> </tr> <tr> <td>010: <math>2^{16}</math> V-Link Clocks</td> <td>011: <math>2^{14}</math> V-Link Clocks</td> </tr> <tr> <td>100: <math>2^{13}</math> V-Link Clocks</td> <td>101: <math>2^{12}</math> V-Link Clocks</td> </tr> <tr> <td>110: <math>2^{11}</math> V-Link Clocks</td> <td>111: <math>2^{10}</math> V-Link Clocks</td> </tr> </table>	000: $2^{15}$ V-Link Clocks	001: $2^{17}$ V-Link Clocks	010: $2^{16}$ V-Link Clocks	011: $2^{14}$ V-Link Clocks	100: $2^{13}$ V-Link Clocks	101: $2^{12}$ V-Link Clocks	110: $2^{11}$ V-Link Clocks	111: $2^{10}$ V-Link Clocks
000: $2^{15}$ V-Link Clocks	001: $2^{17}$ V-Link Clocks										
010: $2^{16}$ V-Link Clocks	011: $2^{14}$ V-Link Clocks										
100: $2^{13}$ V-Link Clocks	101: $2^{12}$ V-Link Clocks										
110: $2^{11}$ V-Link Clocks	111: $2^{10}$ V-Link Clocks										

**I/O Offset Address: 70h**
**MII Management Port Command**
**Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	<b>MII (PHY) Auto Polling</b> 0: Disable 1: Enable (polling interval determined by Rx6C[7:6] )
6	RW	0	<b>PHY Read</b> Every time this bit is set to one, the PHY is read once. The address read is determined by Rx71[4:0] and the data is stored in Rx73-72. 0: Disable 1: Enable
5	RW	0	<b>PHY Write</b> Every time this bit is set to one, the PHY is written once. The address written is determined by Rx71[4:0] and the value in Rx73-72 will be written to the PHY. 0: Disable 1: Enable
4	RW	0	<b>PHY Direct Programming Mode</b> 0: Disable (bits 3-0 are ignored, see bits 6-5) 1: Enable (bits 6-5 are ignored, see bits 2-0)
3	RW	0	<b>MDIO Output Enable Indicator</b>
2	RW	0	<b>PHY Direct Programming Write Data Out</b> During direct programming (write), the value in this bit is written to the PHY every time bit-0 of this register (the “clock”) toggles.
1	RO	0	<b>PHY Direct Programming Read Data In</b> During direct programming (read), every time the “clock” (bit-0) toggles, the value from the PHY is stored in this bit.
0	RW	0	<b>PHY Direct Programming Clock</b> This bit acts as the clock during direct reads from and direct writes to the PHY.

**I/O Offset Address: 71h**
**MII Management Port Address**
**Default Value: 81h**

Bit	Attribute	Default	Description
7	RW	1b	<b>Polling Status</b> 0: Polling mechanism is busy (polling can't be initiated) 1: Polling mechanism is idle (polling can be initiated)
6	RO	0	<b>Polling Type</b> 0: Poll One Cycle 1: Auto polling – close the pause function at bit-5
5	RW	0	<b>Polling Complete</b> 0: Polling not complete 1: Polling complete (auto polling data ready)
4:0	RW	01h	<b>MII Management Port Address Bits 4-0</b> This field contains the address of the PHY register to be read or written.

**I/O Offset Address: 73-72h**
**MII Management Port Data**
**Default Value: 81h**

After a PHY read, the data read from the PHY is stored in this register. For writes to the PHY, the data to be written is placed in this register.

Bit	Attribute	Default	Description
15:0	RW	81h	<b>MII Management Port Data</b>

**I/O Offset Address: 74h**
**EEPROM Command / Status**
**Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	<b>EEPROM Program Complete</b> Set when EEPROM loading is complete.
6	RW	0	<b>EEPROM Embedded Program Enable</b> When this bit is set, configuration data (in Rx6E, 6F, 74, 78, 79, 7A, and 7B) will start to be programmed into the EEPROM.
5	RW	0	<b>Dynamically Reload EEPROM Content</b> When this bit toggles, the Ethernet ID (Rx5-0) is reloaded from EEPROM.
4	RW	0	<b>EEPROM Direct Program Mode</b> 0: Disable 1: Enable
3	RW	0	<b>EEPROM Direct Programming Chip Select</b> This bit must be set to allow programming of the EEPROM using bits 2-0
2	RW	0	<b>EEPROM Direct Programming Clock</b> This bit acts as the clock for direct programming of the EEPROM.
1	RW	0	<b>EEPROM Direct Programming Write Data</b> During direct programming (write), the value in this bit is presented to the EEPROM Data In pin and written to the EEPROM every time bit-2 of this register (the "clock") toggles.
0	RO	0	<b>EEPROM Direct Programming Read Data</b> During direct programming (read), every time bit-2 of this register (the "clock") toggles, the value on the EEPROM Data Out pin is stored in this bit.

**I/O Offset Address: 78h**
**EEPROM Control**
**Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	<b>EEPROM Embedded &amp; Direct Programming</b> 0: Disable (EEPROM cannot be programmed) 1: Enable (allow EEPROM to be programmed)
6	RO	0	<b>Extension Clock</b> 0: Disable 1: Enable (the clock to the EEPROM is sent prior to the start of data to allow more time for the EEPROM to return to the ready state)
5:0	RO	0	<b>Reserved</b>

**I/O Offset Address: 79h**
**Configuration 1**
**Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	<b>Transmit Frame Queueing</b> 0: Enable (frames from the PCI bus can be queued in the transmit FIFO – a maximum of 2 packets may be queued) 1: Disable
6	RW	0	<b>Data Parity Generation and Checking</b> This bit controls whether PCI parity is enabled. 0: Disable 1: Enable
5	RW	0	<b>Memory-Read-Line Supported</b> This bit controls whether PCI Memory-Read-Line is supported. 0: Disable 1: Enable
4	RW	0	<b>Transmit FIFO DMA Interleaved to Receiving FIFO DMA After 32 DW Transaction</b> This bit controls whether during a transmit, priority can be given to a receive transaction. 0: Disable 1: Enable (during a transmit, if a receive request is seen, the transmit is paused after 32 DW's and priority is given to the receive)
3	RW	0	<b>Receive FIFO DMA Interleaved to Transmitting FIFO DMA After 32 DW Transaction</b> This bit controls whether during a receive, priority can be given to a transmit transaction. 0: Disable 1: Enable (during a receive, if a transmit request is seen, the receive is paused after 32 DW's and priority is given to the transmit)
2	RW	0	<b>Memory Read Wait States (for ISA only)</b> 0: None 1: Insert one wait state 2222
1	RW	0	<b>Memory Write Wait States (for ISA only)</b> 0: None 1: Insert one wait state 2222
0	RW	0	<b>Latency Timer</b> This bit controls whether PCI Delayed Transactions are enabled. 0: Disable 1: Enable

**I/O Offset Address: 7Ah**
**Configuration 2**
**Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	<b>Reserved</b> Always reads 0
6	RW	0	<b>Unused BootROM Address MA</b> This bit controls whether unused BootROM memory address bits are tied high. 0: Not tied high 1: Tied high
5	RW	0	<b>Delayed Transactions for BootROM Memory Read</b> This bit controls whether PCI delayed transactions are enabled. 0: Disable 1: Enable
4:0	RO	0	<b>Reserved</b> . Always reads 0

**I/O Offset Address: 7Bh**
**Configuration 3**
**Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	<b>Memory Mapped I/O Access</b> 0: Disable 1: Enable
6:4	RO	0	<b>Reserved</b> (Do Not Program)
3	RW	0	<b>Backoff Algorithm</b> 0: Fixed 1: Random
2:1	RO	0	<b>Reserved</b> (Do Not Program)
0	—	0	<b>Backoff Algorithm Optional</b> 0: Disable 1: Enable

**I/O Offset Address: 80h**
**Miscellaneous 1**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	<b>Reserved.</b> Always reads 0
3	RW	0	<b>Full Duplex Flow Control</b> 0: Disable 1: Enable
2	RW	0	<b>Half Duplex Flow Control</b> 0: Disable 1: Enable
1	RW	0	<b>Soft Timer 0 Status / Start</b> 0: Timer Counting (write 0 after time out to start timer counting) 1: Timer Timed Out
0	RW	0	<b>Soft Timer 0 Enable</b> 0: Disable 1: Enable timer to count

**I/O Offset Address: 81h**
**Miscellaneous 2**
**Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	<b>Reserved</b>
6	RW	0	<b>Force Software Reset</b> Setting this bit resets the MAC. This bit functions differently from Rx09[7] in that when Rx09[7] is set, the MAC will reset only after all state machines are in idle mode (all on-going transactions have been completed). When this bit is set, the MAC will be reset regardless of the status of the state machines. This bit is used when Rx09[7] cannot force a reset due to issues with the state machines. 0: Normal 1: Force Reset
5	RO	0	<b>Reserved (Do Not Program)</b>
4:1	RO	0	<b>Reserved</b> Always reads 0
0	RW	0	<b>Soft Timer 1 Enable</b> 0: Disable 1: Enable timer to count

**I/O Offset Address: 83h**
**Sticky Hardware Control**
**Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	<b>Legacy WOL Status (for software reference)</b> This bit reports whether legacy WOL is supported. 0: Disable 1: Enable timer to count
6:4	RO	0	<b>Reserved</b>
3	RO	0	<b>Legacy WOL Status</b> This bit is set when there is a legacy WOL event. 0: No legacy WOL event occurred 1: Legacy WOL event occurred
2	—	0	<b>Legacy WOL Enable</b> This bit controls whether legacy WOL is a wake event. 0: Disable (if a wake event is detected (bit-3 = 1), PME# will not be asserted) 1: Enable (if a wake event is detected (bit-3 = 1), PME# will be asserted)
1:0	RW	0	<b>Sticky DS Shadow</b> This field reports the current power management state of the device. 00: D0 State 01: D1 State 10: D2 State 11: D3 State

**I/O Offset Address: 84h**
**MII Interrupt Status**
**Default Value: 00h**

The bits in this register correspond to bits in the MII Interrupt Mask register (Rx86). An interrupt is generated when corresponding bits in both registers equal one.

Bit	Attribute	Default	Description
7	RW1C	0	<b>Power Event Report in Test Mode</b>
6	RW	0	<b>User Defined Host Driven Interrupt</b>
5	RO	0	<b>Reserved</b> Always reads 0
4	RW1C	0	<b>Suspend Mode MII Polling Status Change</b>
3	RW1C	0	<b>Transmit Data Write Buffer Queue Race</b> Will be set by transmit shutdown
2	RO	0	<b>Reserved</b> Always reads 0
1	RW1C	0	<b>Soft Timer 1 Timeout</b>
0	RW1C	0	<b>Soft Timer 0 Timeout</b> All bits above: write 0 to clear the interrupt

**I/O Offset Address: 86h**
**MII Interrupt Mask**
**Default Value: 00h**

The bits in this register correspond to bits in the MII Interrupt Status register (Rx84). An interrupt is generated when corresponding bits in both registers equal one.

Bit	Attribute	Default	Description
7	RW	0	<b>Interrupt on MII Interrupt Status (Rx84) Bit-7</b>
6	RW	0	<b>Interrupt on MII Interrupt Status (Rx84) Bit-6</b>
5	RO	0	<b>Reserved</b> Always reads 0
4	RW	0	<b>Interrupt on MII Interrupt Status (Rx84) Bit-4</b>
3	RW	0	<b>Interrupt on MII Interrupt Status (Rx84) Bit-3</b>
2	RO	0	<b>Reserved</b> Always reads 0
1	RW	0	<b>Interrupt on MII Interrupt Status (Rx84) Bit-1</b>
0	RW	0	<b>Interrupt on MII Interrupt Status (Rx84) Bit-0</b> 0: Disable 1: Enable

**I/O Offset Address: 93h**
**Flash Checksum**
**Default Value: 55h**

This register stores the checksum from the EEPROM after programming.

Bit	Attribute	Default	Description
7:0	RW	55h	<b>EEPROM Checksum</b>

**I/O Offset Address: 95-94h**
**Suspend Mode MII Address**
**Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW	0	<b>MII Address During Suspend</b> Functionally, this field is the same as Rx71[4:0]. However, during suspend state this field is used because Rx71[4:0] cannot be accessed.

I/O Offset Address: 99-98h
**Pause Timer**
**Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW	0	<b>Pause Timer Value</b> This field is used for full duplex flow control. When the Receive FIFO is nearly full, The transmitter can send a pause frame to the transmitting side (generally a switch) to request a pause. The length of pause time is determined by this field.

I/O Offset Address: 9Ah
**Pause Status**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RO	0	<b>Reserved</b>
0	RW	0	<b>Pause Status</b> 0: Not paused 1:Paused

I/O Offset Address: 9D-9Ch
**Soft Timer 0**
**Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW	0	<b>Soft Timer 0 Count Value</b> This field reports the count value of soft timer 0.

I/O Offset Address: 9F-9Eh
**Soft Timer 1**
**Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW	0	<b>Soft Timer 1 Count Value</b> This field reports the count value of soft timer 1.

I/O Offset Address: A0h
**Wake On LAN Control Set**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	<b>Wake On LAN Control Set</b>

I/O Offset Address: A1h
**Power Configuration Set**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	<b>Power Configuration Set</b>

I/O Offset Address: A3h
**Wake On LAN Configuration Set**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	<b>Wake On LAN Configuration Set</b>

**I/O Offset Address: A4h**
**Wake On LAN Control Clear**
**Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	<b>Link Off Detected</b> (determines whether the system wakes up from link off detection)
6	RW	0	<b>Link On Detected</b> (determines whether the system wakes up from link on detection)
5	RO	0	<b>Magic Packet Filter</b> (determines whether the system wakes up when a Magic Packet is detected)
4	RW	0	<b>Unicast Filter</b> (determines whether the system wakes up when a Unicast Packet is detected)
3	RW	0	<b>CRC3 Pattern Match Filtering</b> (determines whether the system wakes up when packet matching CRC3 pattern is detected)
2	RO	0	<b>CRC2 Pattern Match Filtering</b> (determines whether the system wakes up when packet matching CRC2 pattern is detected)
1	RW	0	<b>CRC1 Pattern Match Filtering</b> (determines whether the system wakes up when packet matching CRC1 pattern is detected)
0	RW	0	<b>CRC0 Pattern Match Filtering</b> (determines whether the system wakes up when packet matching CRC0 pattern is detected) All bits above: 0: Disable 1: Enable

**I/O Offset Address: A5h**
**Power Configuration Clear**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RO	0	<b>Reserved</b>
5	RW	0	<b>WOL Type</b> 0: Driven by Level 1: Driven By Pulse
4	RW	0	<b>Legacy WOL</b> 0: Disable 1: Enable
3:0	RO	0	<b>Reserved</b> (Do Not Program)

**I/O Offset Address: A7h**
**Wake On LAN Configuration Clear**
**Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	<b>Force Power Management Enable over PME Enable Bit (Legacy Use Only)</b>
6	RW	0	<b>Full Duplex During Suspend</b>
5	RW	0	<b>Accept Multicast During Suspend</b> This bit controls whether multicast packets are accepted during suspend state. Whether a multicast packet will actually wake up the system depends on whether the packet is a type of packet set to wake up the system, as determined by RxA0[5:0].
4	RW	0	<b>Accept Broadcast During Suspend</b> This bit controls whether broadcast packets are accepted during suspend state. Whether a broadcast packet will actually wake up the system depends on whether the packet is a type of packet set to wake up the system, as determined by RxA0[5:0].
3	RW	0	<b>MDC Acceleration</b>
2	RW	0	<b>Extend Clock During Suspend</b> When enabled, the clock to the PHY is sent prior to the start of data to allow more time for the PHY to return to ready state.
1:0	RO	0	<b>Reserved</b> (Do Not Program)

**I/O Offset Address: B3-B0h**
**Pattern CRC0**
**Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	<b>CRC0 Pattern</b>

**I/O Offset Address: B7-B4h**
**Pattern CRC1**
**Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	<b>CRC1 Pattern</b>

**I/O Offset Address: BB-B8h**
**Pattern CRC2**
**Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	<b>CRC2 Pattern</b>

**I/O Offset Address: BF-BCh**
**Pattern CRC3**
**Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	<b>CRC3 Pattern</b>

**I/O Offset Address: CF-C0h**
**Byte Mask 0**
**Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	<b>Byte Mask 0</b>

**I/O Offset Address: DF-D0h**
**Byte Mask 1**
**Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	<b>Byte Mask 1</b>

**I/O Offset Address: EF-E0h**
**Byte Mask 2**
**Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	<b>Byte Mask 2</b>

**I/O Offset Address: FF-F0h**
**Byte Mask 3**
**Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	<b>Byte Mask 3</b>

## Bus 0 Device 19 Function 0 (B0D19F0): PCI to PCIe Bridge

### Header Registers (0–3Fh)

#### Offset Address: 1-0h (B0D19F0)

**Vendor ID**

**Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	<b>Vendor ID</b>

#### Offset Address: 3-2h (B0D19F0)

**Device ID**

**Default Value: 337Bh**

Bit	Attribute	Default	Description
15:0	RO	337Bh	<b>Device ID</b>

#### Offset Address: 5-4h (B0D19F0)

**PCI Command**

**Default Value: 0001h**

Bit	Attribute	Default	Description
15:10	RO	0	<b>Reserved</b>
9	RO	0	<b>Fast Back-to-Back Cycle Enable</b> Hardwired to 0.
8	RW	0	<b>SERR# Enable</b> 0: Disable the SERR# driver on the primary interface 1: Enable the SERR# driver on the primary interface
7	RO	0	<b>Reserved</b>
6	RW	0	<b>Parity Checking</b> 0: Ignore parity errors 1: Perform parity check and take normal action on detected parity errors
5:4	RO	0	<b>Reserved</b>
3	RO	0	<b>Respond To Special Cycle</b> Hardwired to 0.
2	RW	0	<b>Bus Master</b> 0: Never behaves as a bus master 1: Enable to operate as a bus master on the secondary interface
1	RW	0	<b>Memory Space Access</b> 0: Does not respond to memory space access 1: Responds to memory space access
0	RW	1b	<b>I/O Space Access</b> 0: Does not respond to I/O space access 1: Responds to I/O space access

**Offset Address: 7-6h (B0D19F0)**
**PCI Status**
**Default Value: 2010h**

Bit	Attribute	Default	Description
15	RW1C	0	<b>Parity Error Detected</b> Set by PERRS, reset by writing 1.
14	RW1C	0	<b>SERR# Detected</b>
13	RW1C	1b	<b>Set When Terminated with Master-Abort, Except Special Cycle</b> 0: No abort received 1: Transaction aborted by the master
12	RW1C	0	<b>Set When Received a Target-Abort</b> 0: No abort received 1: Transaction aborted by the target
11	RO	0	<b>Set When Signaled a Target-Abort</b>
10:9	RO	00b	<b>DEVSEL# Timing</b> 00: Fast 01: Medium (default) 10: Slow 11: Reserved
8	RW1C	0	<b>Set When Set or Observed SERR# and Parity Error</b> Reserved
7	RO	0	<b>Capable of Accepting Fast Back-to-Back as a Target</b> Reserved
6:5	RO	0	<b>Reserved</b>
4	RO	1b	<b>Capabilities List.</b> This bridge supports Capability List.
3:0	RO	0	<b>Reserved</b>

**Offset Address: 8h (B0D19F0)**
**Revision ID**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	00h	<b>Revision ID</b>

**Offset Address: 0B-9h (B0D19F0)**
**Class Code**
**Default Value: 06 0400h**

Bit	Attribute	Default	Description
23:0	RO	06 0400h	<b>Class Code</b>

**Offset Address: 0Ch (B0D19F0) - Reserved**
**Offset Address: 0Dh (B0D19F0)**
**Latency Timer**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	00h	<b>Latency Timer</b> Hardwired to 0.

**Offset Address: 0Eh (B0D19F0)**
**Header Type**
**Default Value: 81h**

Bit	Attribute	Default	Description
7:0	RO	81h	<b>Header Type</b>

**Offset Address: 0Fh (B0D19F0)**
**Built In Self Test (BIST)**
**Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	<b>BIST Support</b>
6:0	RO	0	<b>Reserved</b>

**Offset Address: 17-10h (B0D19F0) - Reserved**
**Offset Address: 18h (B0D19F0)**
**Primary Bus Number**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	<b>Primary Bus Number</b>

**Offset Address: 19h (B0D19F0)**
**Secondary Bus Number**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	<b>Secondary Bus Number</b>

**Offset Address: 1Ah (B0D19F0)**
**Subordinate Bus Number**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	<b>Subordinate Bus Number</b>

**Offset Address: 1Bh (B0D19F0)**
**Master Latency Timer**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	<b>Master Latency Timer</b>

**Offset Address: 1Ch (B0D19F0)**
**IO Base Address**
**Default Value: F0h**

Bit	Attribute	Default	Description
7:4	RW	Fh	<b>IO Base Address</b>
3:0	RO	0	<b>IO Addressing Capability</b>

**Offset Address: 1Dh (B0D19F0)**
**IO Limit Address**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	<b>IO Limit Address</b>
3:0	RO	0	<b>IO Addressing Capability</b>

**Offset Address: 1Eh (B0D19F0)**
**Secondary Status 1**
**Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	<b>Fast Back to Back Cycle</b>
6	RO	0	<b>Reserved</b>
5	RO	0	<b>66MHz Capability</b>
4:0	RO	0	<b>Reserved</b>

**Offset Address: 1Fh (B0D19F0)**
**Secondary Status 2**
**Default Value: 02h**

Bit	Attribute	Default	Description
7	RW1C	0	<b>Detected Parity Error</b>
6	RW1C	0	<b>Received System Error</b>
5	RW1C	0	<b>Received Master Abort</b>
4	RW1C	0	<b>Received Target Abort</b>
3	RO	0	<b>Signaled Target Abort</b>
2:1	RO	01b	<b>DEVSEL# Timing Status</b>
0	RW1C	0	<b>Master Data Parity Error Detected</b>

**Offset Address: 23-20h (B0D19F0)**
**Memory Limit and Base**
**Default Value: 0000 FFF0h**

Bit	Attribute	Default	Description
31:20	RW	0	<b>Memory Limit</b>
19:16	RO	0	<b>Reserved</b>
15:4	RW	FFFh	<b>Memory Base</b>
3:0	RO	0	<b>Reserved</b>

**Offset Address: 27-24h (B0D19F0)**
**Prefetchable Memory Limit and Base**
**Default Value: 0001 FFF1h**

Bit	Attribute	Default	Description
31:20	RW	0	<b>Prefetchable Memory Limit</b>
19:16	RO	1h	<b>Reserved</b>
15:4	RW	FFFh	<b>Pre-fetch able Memory Base</b>
3:0	RO	1h	<b>Reserved</b>

**Offset Address: 2F-28h (B0D19F0)**
**Prefetch able Upper Limit and Base**
**Default Value: 0000 0000 0000 0000h**

Bit	Attribute	Default	Description
63:32	RW	0	<b>Prefetchable Limit Upper 32 Bits [31:0]</b>
31:0	RW	0	<b>Prefetchable Base Upper 32 Bits [31:0]</b>

**Offset Address: 33-30h (B0D19F0)**
**IO Limit/Base Upper 16 Bit**
**Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:16	RO	0	<b>IO Limit Upper 16 Bits</b>
15:0	RO	0	<b>IO Base Upper 16 Bits</b>

**Offset Address: 34h (B0D19F0)**
**Capability Pointer**
**Default Value: 60h**

Bit	Attribute	Default	Description
7:0	RO	60h	<b>Capability Pointer</b>

**Offset Address: 3D-35h (B0D19F0) - Reserved**

**Offset Address: 3F-3Eh (B0D19F0)**
**Bridge Control**
**Default Value: 0000h**

Bit	Attribute	Default	Description
15:12	RO	0	<b>Reserved</b>
11	RW	0	<b>Discard Timer SERR# Enable</b>
10	RW1C	0	<b>Discard Timer Status</b>
9	RW	0	<b>Secondary Discard Timer</b>
8	RW	0	<b>Primary Discard Timer</b>
7	RO	0	<b>Fast Back-to-Back Enable</b>
6	RW	0	<b>Secondary Bus Reset</b>
5	RW	0	<b>Master Abort Mode</b>
4	RW	0	<b>VGA 16-bit Decode</b>
3	RW	0	<b>VGA Enable</b>
2	RW	0	<b>ISA Enable</b>
1	RW	0	<b>SERR# Enable</b>
0	RW	0	<b>Parity Error Response Enable</b>

**Device-Specific Control (Rx40-FFh)**
**Offset Address: 40h (B0D19F0)**
**PCIe Related Control**
**Default Value: 02h**

Bit	Attribute	Default	Description
7:6	RW	00b	<b>Extended CFG Mode</b> 00: Extended CFG mode is off. 01: FF_0xxx_xxxx and FF_1xxx_xxxx from K8 side to support extended CFG. 10: Capability header for extended configuration address support. 11: Memory mapped extended CFG address supported, Rx41[7:0] (RXCFG[35:28]) should also be programmed.
5	RW	0	<b>Enable the Capability / Status Write of the PCI to PCIe Bridge &amp; PCI to PCI Bridge Configuration Capability</b>
4:0	RO	02h	<b>Reserved (Do Not Program)</b>

**Offset Address: 41h (B0D19F0)**
**Memory Mapped Extended CFG Address**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	<b>Extended Configuration Address for A[35:28]</b> 00: No extended configuration address Else: Extended configuration address A[35:28] from host side

**Offset Address: 42h (B0D19F0)**
**PCIe Device Enable and Power Management**
**Default Value: 06h**

Bit	Attribute	Default	Description
7:4	RO	0	<b>Reserved</b>
3	RW	0	<b>Disable High Definition Audio Controller</b>
2:0	RO	110b	<b>Reserved (Do Not Program)</b>

**Offset Address: 5F-43h (B0D19F0) – Reserved**
**Offset Address: 63-60h (B0D19F0)**
**MSI Mapping Capability Register**
**Default Value: A802 7008h**

Bit	Attribute	Default	Description
31:27	RO	15h	<b>Capability Type</b>
26:18	RO	0	<b>Reserved</b>
17	RO-	1b	<b>Fixed.</b> The HT MSI address is only 0000_0000_fexxxx
16	RW	0	<b>MSI Mapping Enable</b> 0: Disable                    1: Enable
15:8	RO	70h	<b>Capability Pointer</b>
7:0	RO	08h	<b>Capability ID</b>

**Offset Address: 6F-64h (B0D19F0) - Reserved**

**Offset Address: 77-70h (B0D19F0)**
**Subsystem ID and Subsystem Vendor ID Capability Structure**
**Default Value: 337B 1106 0000 000Dh**

Bit	Attribute	Default	Description
63:48	RO/RW	337Bh	<b>Subsystem ID</b> RW if D19F0 Rx40[5] = 1
47:32	RO/RW	1106h	<b>Subsystem Vendor ID</b> RW if D19F0 Rx40[5] = 1
31:16	RO	0	<b>Reserved</b>
15:8	RO	0	<b>Capability Pointer</b>
7:0	RO	0Dh	<b>Capability ID</b>

**Offset Address: FF-78h (B0D19F0) - Reserved**

## Bus 0 Device 19 Function 1 (B0D19F1): PCI to PCI Bridge

### Header Registers (0–3Fh)

#### Offset Address: 1-0h (B0D19F1)

**Vendor ID**

**Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	<b>Vendor ID</b>

#### Offset Address: 3-2h (B0D19F1)

**Device ID**

**Default Value: 337Ah**

Bit	Attribute	Default	Description
15:0	RO	337Ah	<b>Device ID</b>

#### Offset Address: 5-4h (B0D19F1)

**PCI Command**

**Default Value: 0001h**

Bit	Attribute	Default	Description
15:10	RO	0	<b>Reserved</b>
9	RO	0	<b>Fast Back-to-Back Cycle Enable</b> Hardwired to 0.
8	RW	0	<b>SERR# Enable</b>
7	RO	0	<b>Reserved</b>
6	RW	0	<b>Parity Checking</b> 0: Ignore parity errors 1: Perform parity check and take normal action on detected parity errors
5:4	RO	0	<b>Reserved</b>
3	RO	0	<b>Respond To Special Cycle</b> Hardwired to 0.
2	RW	0	<b>Bus Master</b> 0: Never behaves as a bus master 1: Enable to operate as a bus master on the secondary interface
1	RW	0	<b>Memory Space Access</b> 0: Does not respond to memory space access 1: Responds to memory space access
0	RW	1b	<b>I/O Space Access</b> 0: Does not respond to I/O space access 1: Responds to I/O space access

**Offset Address: 7-6h (B0D19F1)**
**PCI Status**
**Default Value: 2010h**

Bit	Attribute	Default	Description
15	RW1C	0	<b>Parity Error Detected</b> Set by PERRS, reset by writing 1.
14	RW1C	0	<b>SERR# Detected</b>
13	RW1C	1b	<b>Set When Terminated with Master-Abort, Except Special Cycle</b> 0: No abort received 1: Transaction aborted by the master
12	RW1C	0	<b>Set When Received a Target-Abort</b> 0: No abort received 1: Transaction aborted by the target
11	RO	0	<b>Set When Signaled a Target-Abort</b> NB never signals Target Abort
10:9	RO	00b	<b>DEVSEL# Timing</b> 00: Fast 01: Medium (default) 10: Slow 11: Reserved
8	RW1C	0	<b>Set When Set or Observed SERR# and Parity Error</b> Reserved
7	RO	0	<b>Capable of Accepting Fast Back-to-Back as a Target</b> Reserved
6:5	RO	0	<b>Reserved</b>
4	RO	1b	<b>Capabilities List</b> This bridge supports Capability List.
3:0	RO	0	<b>Reserved</b>

**Offset Address: 8h (B0D19F1)**
**Revision ID**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	<b>Revision ID</b>

**Offset Address: 0B-9h (B0D19F1)**
**Class Code**
**Default Value: 06 0401h**

Bit	Attribute	Default	Description
23:0	RO	06 0401h	<b>Class Code</b> 060400h when backdoor B0D17F7 Rx53[0] is enabled.

**Offset Address: 0Ch (B0D19F1) - Reserved**
**Offset Address: 0Dh (B0D19F1)**
**Latency Timer**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	00h	<b>Latency Timer</b> Hardwired to 0.

**Offset Address: 0Eh (B0D19F1)**
**Header Type**
**Default Value: 01h**

Bit	Attribute	Default	Description
7:0	RO	01h	<b>Header Type</b>

**Offset Address: 0Fh (B0D19F1)**
**Built In Self Test (BIST)**
**Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	<b>BIST Support</b>
6:0	RO	0	<b>Reserved</b>

**Offset Address: 17-10h (B0D19F1) – Reserved**
**Offset Address: 18h (B0D19F1)**
**Primary Bus Number**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	Primary Bus Number

**Offset Address: 19h (B0D19F1)**
**Secondary Bus Number**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	Secondary Bus Number

**Offset Address: 1Ah (B0D19F1)**
**Subordinate Bus Number**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	Subordinate Bus Number

**Offset Address: 1Bh (B0D19F1)**
**Master Latency Timer**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	Master Latency Timer Hardwired to 0.

**Offset Address: 1Ch (B0D19F1)**
**IO Base Address**
**Default Value: F0h**

Bit	Attribute	Default	Description
7:4	RW	Fh	IO Base Address
3:0	RO	0	IO Addressing Capability

**Offset Address: 1Dh (B0D19F1)**
**IO Limit Address**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	IO Limit Address
3:0	RO	0	IO Addressing Capability

**Offset Address: 1Eh (B0D19F1)**
**Secondary Status 1**
**Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	Fast Back to Back Cycle
6	RO	0	Reserved
5	RO	0	66MHz Capability
4:0	RO	0	Reserved

**Offset Address: 1Fh (B0D19F1)**
**Secondary Status 2**
**Default Value: 02h**

Bit	Attribute	Default	Description
7	RW1C	0	<b>Detected Parity Error</b>
6	RW1C	0	<b>Received System Error</b>
5	RW1C	0	<b>Received Master Abort</b>
4	RW1C	0	<b>Received Target Abort</b>
3	RO	0	<b>Signaled Target Abort</b>
2:1	RO	01b	<b>DEVSEL# Timing Status</b>
0	RW1C	0	<b>Master Data Parity Error Detected</b>

**Offset Address: 23-20h (B0D19F1)**
**Memory Limit and Base**
**Default Value: 0000 FFF0h**

Bit	Attribute	Default	Description
31:20	RW	0	<b>Memory Limit</b>
19:16	RO	0	<b>Reserved</b>
15:4	RW	FFFh	<b>Memory Base</b>
3:0	RO	0	<b>Reserved</b>

**Offset Address: 27-24h (B0D19F1)**
**Prefetchable Memory Limit and Base**
**Default Value: 0001 FFF1h**

Bit	Attribute	Default	Description
31:20	RW	0	<b>Prefetchable Memory Limit</b>
19:16	RO	1h	<b>Reserved</b>
15:4	RW	FFFh	<b>Prefetchable Memory Base</b>
3:0	RO	1h	<b>Reserved</b>

**Offset Address: 2F-28h (B0D19F1)**
**Prefetchable Upper Limit and Base**
**Default Value: 0000 0000 0000 0000h**

Bit	Attribute	Default	Description
63:32	RW	0	<b>Prefetchable Limit Upper 32 Bits [31:0]</b>
31:0	RW	0	<b>Prefetchable Base Upper 32 Bits [31:0]</b>

**Offset Address: 33-30h (B0D19F1)**
**IO Limit/Base Upper 16 Bit**
**Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:16	RO	0	<b>IO Limit Upper 16 Bits</b>
15:0	RO	0	<b>IO Base Upper 16 Bits</b>

**Offset Address: 34h (B0D19F0)**
**Capability Pointer**
**Default Value: 60h**

Bit	Attribute	Default	Description
7:0	RO	60h	<b>Capability Pointer</b>

**Offset Address: 3D-35h (B0D19F1) - Reserved**

**Offset Address: 3F-3Eh (B0D19F1)**
**Bridge Control Register**
**Default Value: 0000h**

Bit	Attribute	Default	Description
15:12	RO	0	<b>Reserved</b>
11	RW	0	<b>Discard Timer SERR# Enable</b>
10	RW1C	0	<b>Discard Timer Status</b>
9	RW	0	<b>Secondary Discard Timer</b>
8	RW	0	<b>Primary Discard Timer</b>
7	RO	0	<b>Fast Back-to-Back Enable</b>
6	RW	0	<b>Secondary Bus Reset</b>
5	RW	0	<b>Master Abort Mode</b>
4	RW	0	<b>VGA 16-bit Decode</b>
3	RW	0	<b>VGA Enable</b>
2	RW	0	<b>ISA Enable</b>
1	RW	0	<b>SERR# Enable</b>
0	RW	0	<b>Parity Error Response Enable</b>

**Device-Specific Control (Rx40-FFh)**
**Offset Address: 40h (B0D19F1)**
**External PCI Device Enable Control**
**Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	<b>Reserved</b>
6	RW	0	<b>Hide AD25 on External PCI Bus When Assert</b>
5	RW	0	<b>Hide AD24 on External PCI Bus When Assert</b>
4	RW	0	<b>Hide AD23 on External PCI Bus When Assert</b>
3	RW	0	<b>Hide AD22 on External PCI Bus When Assert</b>
2	RW	0	<b>Hide AD21 on External PCI Bus When Assert</b>
1	RW	0	<b>Hide AD20 on External PCI Bus When Assert</b>
0	RW	0	<b>Hide AD19 on External PCI Bus When Assert</b>

**Offset Address: 5F-41h (B0D19F1) - Reserved**
**Offset Address: 63-60h (B0D19F1)**
**MSI Mapping Capability**
**Default Value: A802 7008h**

Bit	Attribute	Default	Description
31:27	RO	15h	<b>Capability Type</b>
26:18	RO	0	<b>Reserved</b>
17	RO	1b	<b>Fixed.</b> The HT_MSI address is only 0000_0000_fexxxx.
16	RW	0	<b>MSI Mapping Enable.</b> 0: Disable                    1: Enable
15:8	RO	70h	<b>Capability Pointer</b>
7:0	RO	08h	<b>Capability ID</b>

**Offset Address: 77-70h (B0D19F1)**
**Subsystem ID and Subsystem Vendor ID Capability Structure**
**Default Value: 337A 1106 0000 000Dh**

Bit	Attribute	Default	Description
63:48	RO/RW	337Ah	<b>Subsystem ID</b> RW if B0D19F0 Rx40[5] = 1
47:32	RO/RW	1106h	<b>Subsystem Vendor ID</b> RW if B0D19F0 Rx40[5] = 1
31:16	RO	0	<b>Reserved</b>
15:8	RO	0	<b>Capability Pointer</b>
7:0	RO	0Dh	<b>Capability ID</b>

**Offset Address: FF-78h (B0D19F1) - Reserved**

## HDAC: High Definition Audio Controller PCIe Configuration Space

### Header Registers (0-3Fh)

#### Offset Address: 1-0h (HDAC)

Vendor ID

Default Value: 1106h

Bit	Attribute	Default	Description
15:0	RO	1106h	<b>Vendor ID</b>

#### Offset Address: 3-2h (HDAC)

Device ID

Default Value: 3288h

Bit	Attribute	Default	Description
15:0	RO	3288h	<b>Device ID</b>

#### Offset Address: 5-4h (HDAC)

PCI Command

Default Value: 0000h

Bit	Attribute	Default	Description
15:11	RO	0	<b>Reserved</b>
10	RW	0	<b>Interrupt Disable</b>
9	RO	0	<b>Fast Back to Back</b>
8	RO	0	<b>SERR# Enable</b>
7	RO	0	<b>Address Stepping</b>
6	RO	0	<b>Parity Error Response</b>
5	RO	0	<b>VGA Palette Snooping</b>
4	RO	0	<b>Memory Write and Invalidate</b>
3	RO	0	<b>Respond to Special Cycle</b>
2	RW	0	<b>Bus Master</b>
1	RW	0	<b>Memory Space Access</b>
0	RO	0	<b>I/O Space Access</b>

#### Offset Address: 7-6h (HDAC)

PCI Status

Default Value: 0010h

Bit	Attribute	Default	Description
15	RO	0	<b>Detect Parity Error</b>
14	RO	0	<b>Signaled System Error (SERR#)</b>
13	RO	0	<b>Received Master Abort</b>
12	RO	0	<b>Received Target Abort</b>
11	RO	0	<b>Signaled Target Abort</b>
10:9	RO	0	<b>DEVSEL# Timing</b>
8	RO	0	<b>Data Parity Detected</b>
7	RO	0	<b>Fast Back-to-Back Capability</b>
6:5	RO	0	<b>Reserved</b>
4	RO	1b	<b>Capability List</b>
3	RO	0	<b>Interrupt Status</b>
2:0	RO	0	<b>Reserved</b>

**Offset Address: 8h (HDAC)**
**Revision ID**
**Default Value: 10h**

Bit	Attribute	Default	Description
7:0	RO	10h	<b>Revision ID</b>

**Offset Address: 0B-9h (HDAC)**
**Class Code**
**Default Value: 04 0300h**

Bit	Attribute	Default	Description
23:0	RO	04 0300h	<b>Class Code</b>

**Offset Address: 0Ch (HDAC)**
**Cache Line Size**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	<b>Cache Line Size</b>

**Offset Address: 0Dh (HDAC)**
**Latency Timer**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	<b>Latency Timer</b>

**Offset Address: 0Eh (HDAC)**
**Header Type**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	<b>Header Type</b>

**Offset Address: 0Fh (HDAC)**
**Built In Self Test**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	<b>Built In Self Test</b>

**Offset Address: 13-10h (HDAC)**
**HDAC Lower Base Address**
**Default Value: 0000 0004h**

Bit	Attribute	Default	Description
31:14	RW	0	<b>Lower Base Address</b> 16 KB are requested by hardwaring [13:4] to 0s
13:4	RO	0	<b>Hardwired to 0</b>
3	RO	0	<b>Not Prefetchable</b>
2:1	RO	10b	<b>Address Range</b>
0	RO	0	<b>Space Type: Memory Space</b>

**Offset Address: 17-14h (HDAC)**
**HDAC Upper Base Address**
**Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	<b>HDAC Upper Base Address</b>

**Offset Address: 2B-18h (HDAC) – Reserved**
**Offset Address: 2D-2Ch (HDAC)**
**Subsystem Vendor ID**
**Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RW1	1106h	<b>Subsystem Vendor ID</b> RW if Rx40[0] = 1

**Offset Address: 2F-2Eh (HDAC)**
**Subsystem ID**
**Default Value: 3288h**

Bit	Attribute	Default	Description
15:0	RW1	3288h	<b>Subsystem ID</b> RW if Rx40[0] = 1

**Offset Address: 33-30h (HDAC)**
**Expansion ROM**
**Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	<b>Expansion ROM</b>

**Offset Address: 34h (HDAC)**
**Capabilities Pointer**
**Default Value: 50h**

Bit	Attribute	Default	Description
7:0	RO	50h	<b>Capabilities Pointer</b> Points to the power management capability.

**Offset Address: 3B-35h (HDAC) – Reserved**
**Offset Address: 3Ch (HDAC)**
**Interrupt Line**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	<b>Interrupt Line</b>

**Offset Address: 3Dh (HDAC)**
**Interrupt Pin**
**Default Value: 01h**

Bit	Attribute	Default	Description
7:0	RO	01h	<b>Interrupt Pin</b>

**Offset Address: 3F-3Eh (HDAC) – Reserved**

## HDAC PCIe Extended Configuration Space (40-260h)

## Offset Address: 40h (HDAC)

## Back Door Enable

**Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RO	0	<b>Reserved</b>
0	RW	0	<b>Subsystem ID / Subsystem Vender ID Back Door Enable</b> Specifies whether Rx2C~2F are RO or RW 0: Read Only                                    1: Read / Write

### Offset Address: 41h (HDAC)

## **HDAC Control**

**Default Value:** 00h

Bit	Attribute	Default	Description	
7:1	RO	0	<b>Reserved</b>	
0	RW	0	<b>Dynamic Stop</b> 1:Dynamic stop clock	0: Free running

#### **Offset Address: 43-42h (HDAC) – Reserved**

#### Offset Address: 44h (HDAC)

## Traffic Class Select

**Default Value:** 00h

Bit	Attribute	Default	Description
7:3	RO	0	<b>Reserved</b>
2:0	RO	0	<b>HDAC Traffic Class Assignment</b> 000: TC0 Others: Reserved

#### **Offset Address: 4F-45h (HDAC) – Reserved**

### **Offset Address: 51-50h (HDAC)**

## **PCI Power Management Capabilities ID**

**Default Value:** 6001h

Bit	Attribute	Default	Description
15:8	RO	60h	<b>Point to the Next Capability Structure (MSI)</b>
7:0	RO	01h	<b>PCI Power Management Capability</b>

**Offset Address: 53-52h (HDAC)**

## **PCI Power Management Capabilities**

**Default Value:** C842h

Bit	Attribute	Default	Description
15:11	RO	19h	PME Can Be Generated from D3 and D0 State
10	RO	0	D2 State is not Supported
9	RO	0	D1 State is not Supported
8:6	RO	001b	Report D3 Max Suspend Current
5	RO	0	No Device-Specific Initialization is Required
4	RO	0	Reserved
3	RO	0	Hardwired to 0
2:0	RO	010b	Support PCI Power 1.1 Specific

**Offset Address: 57-54h (HDAC)**
**Power Management Control and Status**
**Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:22	RO	0	<b>Hardwired to 0</b>
21:16	RO	0	<b>Reserved</b>
15	RW1C RWM	0	<b>PMES</b> This bit is set when the HDAC controller would normally assert the PME# independent of the state of the PMEE. This bit is in resume well.
14:9	RO	0	<b>Reserved</b>
8	RWS RSM	0	<b>PMEE</b> Enable PME wake up, if PMES is set. This bit is in resume well
7:2	RO	0	<b>Reserved</b>
1:0	RW	00b	<b>Power State</b> This field is used both to determinate the current power state and to set a new power state. 00b: D0 11b: D3 If software attempts to write a value of 10b or 01b into this field, the write operation must complete normally; however, no state change will occur.

**Offset Address: 5F-58h (HDAC) – Reserved**
**Offset Address: 61-60h (HDAC)**
**Message Signal Interrupt (MSI) Capability ID**
**Default Value: 7005h**

Bit	Attribute	Default	Description
15:8	RO	70h	<b>Point to the Next Capability Structure (PCIe)</b>
7:0	RO	05h	<b>MSI Capability</b>

**Offset Address: 63-62h (HDAC)**
**Message Signal Interrupt (MSI) Message Control**
**Default Value: 0080h**

Bit	Attribute	Default	Description
15:8	RO	0	<b>Reserved</b>
7	RO	1b	<b>64 Bit Address Capability</b>
6:4	RO	000b	<b>Multiple Message Enable</b> Normally this is a RW register, but software will always read 000b to indicate only 1 message is supported.
3:1	RO	0	<b>Hardwired to 0 Indicating Request for 1 Message</b>
0	RW	0	<b>MSI Enable</b> 0: A MSI will be generated instead of an INTx 1: A MSI will not be generated.

**Offset Address: 67-64h (HDAC)**
**MSI Message Lower Address**
**Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:2	RW	0	<b>Message Lower Address</b>
1:0	RO	0	<b>Reserved</b>

**Offset Address: 6B-68h (HDAC)**
**MSI Message Upper Address**
**Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	<b>Message Upper Address</b>

**Offset Address: 6D-6Ch (HDAC)**
**MSI Data**
**Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW	0	Data Used for MSI Message

**Offset Address: 6F-6Eh (HDAC) – Reserved**
**Offset Address: 71-70h (HDAC)**
**PCI Express Capability ID**
**Default Value: 0010h**

Bit	Attribute	Default	Description
15:8	RO	0	The Last Capability Structure in the List
7:0	RO	10h	PCI Express Capability

**Offset Address: 73-72h (HDAC)**
**PCI Express Capability**
**Default Value: 0091h**

Bit	Attribute	Default	Description
15:8	RO	0	Hardwired to 0
7:4	RO	1001b	Device/Port Type Hardwired to 1001b
3:0	RO	1h	Capability Version #1

**Offset Address: 77-74h (HDAC)**
**Device Capabilities**
**Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	Device Capabilities Hardwired to 0

**Offset Address: 79-78h (HDAC)**
**Device Control**
**Default Value: 0000h**

Bit	Attribute	Default	Description
15	RO	0	Reserved
14:12	RO	0	Hardwired to 0
11	RO	0	Snoop
10:0	RO	0	Hardwired to 0

**Offset Address: 7B-7Ah (HDAC)**
**Device Status**
**Default Value: 0010h**

Bit	Attribute	Default	Description
15:6	RO	0	Reserved
5	RO	0	Transaction Pending 0: All non-posted requests have been executed 1: Some non-posted request have not been completed
4	RO	1b	Hardwired to 1
3:0	RO	0	Hardwired to 0

**Offset Address: 9F-7Ch (HDAC) – Reserved**

**Offset Address: 103-100h (HDAC)**
**Virtual Channel Enhanced Capability**
**Default Value:** 0001 0002h

Bit	Attribute	Default	Description
31:20	RO	000h	<b>Next Capability Pointer</b> Hardwired to 000h.
19:16	RO	1h	<b>Hardwired to 1</b>
15:0	RO	0002h	<b>Hardwired to 2</b>

**Offset Address: 107-104h (HDAC)**
**Port VC Capability 1**
**Default Value:** 0000 0000h

Bit	Attribute	Default	Description
31:12	RO	0	<b>Reserved</b>
11:3	RO	0	<b>Hardwired to 0</b>
2:0	RO	0	<b>Indicates that one extended VC is supported by the controller</b>

**Offset Address: 10B-108h (HDAC)**
**Port VC Capability 2**
**Default Value:** 0000 0000h

Bit	Attribute	Default	Description
31:24	RO	0	<b>Hardwired to 0.</b> Indicates that a VC arbitration table is not present
23:8	RO	0	<b>Reserved</b>
7:0	RO	0	<b>Hardwired to 0</b>

**Offset Address: 10D-10Ch (HDAC)**
**Port VC Control**
**Default Value:** 0000h

Bit	Attribute	Default	Description
15:0	RO	0	<b>Reserved</b>

**Offset Address: 10F-10Eh (HDAC)**
**Port VC Status**
**Default Value:** 0000h

Bit	Attribute	Default	Description
15:1	RO	0	<b>Reserved</b>
0	RO	0	<b>Hardwired to 0.</b> VC arbitration table is not present

**Offset Address: 113-110h (HDAC)**
**VC0 Resource Capability**
**Default Value:** 0000 0000h

Bit	Attribute	Default	Description
31:0	RO	0	<b>Hardwired to 0.</b> This field is not valid for endpoint devices.

**Offset Address: 117-114h (HDAC)**
**VC0 Resource Control**
**Default Value:** 8000 00FFh

Bit	Attribute	Default	Description
31	RO	1b	<b>VC0 Enable.</b> Hardwired to 1 for VC0
30:27	RO	0	<b>Reserved</b>
26:24	RO	0	<b>VC0 ID.</b> Hardwired to 0 since this field is assigned to VC0.
23:20	RO	0	<b>Reserved</b>
19:16	RO	0	<b>Hardwired to 0</b>
15:8	RO	0	<b>Reserved</b>
7:1	RW	7Fh	<b>TC/VC0 Map</b> Bit 0 is Hardwired to 1 since TC0 is always mapped to VC0. Bit[7:1] are implemented as RW bits
0	RO	1b	<b>TC/VC0 Map</b> Bit 0 is Hardwired to 1 since TC0 is always mapped to VC0.

**Offset Address: 119-118h (HDAC) – Reserved**
**Offset Address: 11B-11Ah (HDAC)**
**VC0 Resource Status**
**Default Value: 0000h**

Bit	Attribute	Default	Description
15:2	RO	0	<b>Reserved</b>
1	RO	0	<b>Hardwired to 0.</b> This bit is not applied to integrated device.
0	RO	0	<b>Hardwired to 0.</b> This bit is not valid for endpoint devices.

**Offset Address: 11F-11Ch (HDAC)**
**VC1 Resource Capability**
**Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	<b>Hardwired to 0.</b> This bit is not valid for endpoint devices

**Offset Address: 123-120h (HDAC)**
**VC1 Resource Control**
**Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RO	0	<b>VC1 Enable.</b> When set to 1, VC1 is enabled.
30:27	RO	0	<b>Reserved</b>
26:24	RO	001b	<b>VC1 ID</b>
23:20	RO	0	<b>Reserved</b>
19:16	RO	0	<b>Hardwired to 0.</b> This bit is not valid for endpoint devices.
15:8	RO	0	<b>Reserved</b>
7:0	RO	0	<b>TC/VC1 Map</b>

**Offset Address: 125-124h (HDAC) – Reserved**
**Offset Address: 127-126h (HDAC)**
**VC1 Resource Status**
**Default Value: 0000h**

Bit	Attribute	Default	Description
15:2	RO	0	<b>Reserved</b>
1:0	RO	0	<b>Hardwired to 0.</b> This bit is not valid for endpoint devices.

**Offset Address: 19F-128h (HDAC) – Reserved**
**Offset Address: 200h (HDAC)**
**BIST Control**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RO	0	<b>Reserved</b>
2	RW	0	<b>BIST Clock Switch.</b> Must be done before enabling playback / recoding run bit.
1	RW	0	<b>Playback BIST Run Bit.</b> Software can only write 1 to enable BIST process, read back as 0 indicates BIST process has completed
0	RW	0	<b>Recoding BIST Run Bit</b> Software can only write 1 to enable BIST process, read back as 0 indicates BIST process has completed

**Offset Address: 20F-201h (HDAC) – Reserved**

**Offset Address: 214-210h (HDAC)**
**BIST Playback Pattern**
**Default Value: 00 0000 0000h**

Bit	Attribute	Default	Description
39:34	RO	0	<b>Reserved</b>
33:0	RW	0	<b>Playback BIST Pattern.</b>

**Offset Address: 21F-215h (HDAC) – Reserved**
**Offset Address: 224-220h (HDAC)**
**BIST Recording Pattern**
**Default Value: 00 0000 0000h**

Bit	Attribute	Default	Description
39:34	RO	0	<b>Reserved</b>
33:0	RW	0	<b>Recording BIST Pattern.</b>

**Offset Address: 22F-225h (HDAC) – Reserved**
**Offset Address: 231-230h (HDAC)**
**SRAMs (Playback Related Only) Direct Read/Write Access**
**Default Value: 0000h**

Bit	Attribute	Default	Description
15:12	RO	0	<b>Reserved</b>
11	RW	0	<b>SRAM BIST Run Bit</b> Enable the direct access operation.
10	RW	0	<b>SRAM BIST Write Enable</b> 1: Indicates a write                    0: Indicates a read
9:8	RW	0	<b>SRAM BIST Extension Selection</b> Indicates the selected SRAM among the four SRAMs 00: SRAM 0                            01: SRAM 1 10: SRAM 2                            11: SRAM 4
7:6	RO	0	<b>Reserved</b>
5:0	RW	0	<b>SRAM BIST Address</b> Indicates the accessing address of the selected SRAM.

**Offset Address: 233-232h (HDAC)**
**SRAMs (Record Related Only) Direct Read/Write Access**
**Default Value: 0000h**

Bit	Attribute	Default	Description
15:12	RO	0	<b>Reserved</b>
11	RW	0	<b>SRAM BIST Run Bit</b> Enable the direct access operation
10	RW	0	<b>SRAM BIST Write Enable</b> 1: Indicates a write                    0: Indicates a read
9:8	RW	0	<b>SRAM BIST Select</b> Indicates the selected SRAM among the four SRAMs 00: SRAM 0                            01: SRAM 1 10: SRAM 2                            11: SRAM 4
7:5	RO	0	<b>Reserved</b>
4:0	RW	0	<b>SRAM BIST Address</b> Indicates the accessing address of the selected SRAM

**Offset Address: 23F-234h (HDAC) – Reserved**

**Offset Address: 244-240h (HDAC)**
**BIST Playback Data Check**
**Default Value: 00 0000 0000h**

Bit	Attribute	Default	Description
39:34	RO	0	<b>Reserved</b>
33:0	RO	0	<b>Playback Data Read from SRAM</b>

**Offset Address: 24F-245h (HDAC) – Reserved**
**Offset Address: 254-250h (HDAC)**
**BIST Recording Data Check**
**Default Value: 00 0000 0000h**

Bit	Attribute	Default	Description
39:34	RO	0	<b>Reserved</b>
33:0	RO	0	<b>Recording Data Read from SRAM</b>

**Offset Address: 25F-255h (HDAC) – Reserved**
**Offset Address: 260h (HDAC)**
**BIST Error Status**
**Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	<b>SRAM3_PLAY BIST Error Status</b>
6	RO	0	<b>SRAM2_PLAY BIST Error Status</b>
5	RO	0	<b>SRAM1_PLAY BIST Error Status</b>
4	RO	0	<b>SRAM0_PLAY BIST Error Status</b>
3	RO	0	<b>SRAM3_REC BIST Error Status</b>
2	RO	0	<b>SRAM2_REC BIST Error Status</b>
1	RO	0	<b>SRAM1_REC BIST Error Status</b>
0	RO	0	<b>SRAM0_REC BIST Error Status</b>

## High Definition Audio Controller Memory Mapped I/O Registers (HDAC-MMIO)

This section describes the memory mapped High Definition Audio Controller register interface. Please refer to High Definition Audio Specification 1.0 for details.

### Global Capabilities and Control (0-1Bh)

#### Offset Address: 1-0h (HDAC-MMIO)

##### Global Capabilities – GCAP

**Default Value: 4401h**

Bit	Attribute	Default	Description
15:12	RO	0100b	<b>Number of Output Streams Supported</b> 0100b: 4 output streams supported
11:8	RO	0100b	<b>Number of Input Streams Supported</b> 0100b: 4 input streams supported
7:3	RO	00000b	<b>Number of Bidirectional Streams Supported</b> 00000b: No bidirectional stream supported
2:1	RO	00b	<b>Number of Serial Data Out Signals</b> 00: 1 SDO 01: 2 SDOS 10: 4 SDOS 11: Reserved
0	RO	1b	<b>64 Bit Address Supported</b> 0: Only 32-bit addressing is available. 1: 64 bit addressing is supported.

#### Offset Address: 3-2h (HDAC-MMIO)

##### Version Number

**Default Value: 0100h**

Bit	Attribute	Default	Description
15:8	RO	01h	<b>Major Version</b>
7:0	RO	00h	<b>Minor Version</b>

The version number “0100h” indicates this chip complies with High Definition Audio Specification Rev 1.0.

#### Offset Address: 7-4h (HDAC-MMIO)

##### Payload Capability

**Default Value: 001D 003Ch**

Bit	Attribute	Default	Description
31:16	RO	001Dh	<b>Input Payload Capability</b> 1Dh: 29-word payload (464 bits) Note: this does not include bandwidth used for command and control.
15:0	RO	003Ch	<b>Output Payload Capability</b> 003Ch: 60-word payload (960 bits)

#### Offset Address: 0B-8h (HDAC-MMIO)

##### Global Control – GCTL

**Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:9	RsvdP	0	<b>Reserved</b>
8	RW	0	<b>Accept Unsolicited Response Enable</b> 0: Unsolicited response from codec are not accepted 1: Unsolicited response from codec are accepted by the controller
7:2	RsvdP	0	<b>Reserved</b>
1	RW	0	<b>Flush Control</b> Writing a 1 to this bit initiates a flush.
0	RWS	HwInit	<b>Controller Reset</b> For read: 0: In reset state For write: 0: Reset the controller 1: Controller is ready for operations. 1: Exit the reset state

**Offset Address: 0D-0Ch (HDAC-MMIO)**
**Wake Enable – WAKEEN**
**Default Value: 0000h**

Bit	Attribute	Default	Description
15:4	RsvdP	0	<b>Reserved</b>
3:0	RW, RSM	0	<b>SDIN Wake Enable Flags</b> 0: Disable 1: Allow the associated SDIN signal to generate a wake or processor interrupt The bit[i] corresponds to SDIN[i] signal.

**Offset Address: 0F-0Eh (HDAC-MMIO)**
**State Change Status – STATESTS**
**Default Value: 0000h**

Bit	Attribute	Default	Description
15:4	RsvdZ	0	<b>Reserved</b>
3:0	RW1CS, RSM	0	<b>SDIN State Change Status Flags</b> 0: No state change 1: The associated SDIN signal received a “State Change” event. The bit[i] corresponds to SDIN[i] signal.

**Offset Address: 11-10h (HDAC-MMIO)**
**Global Status – GSTS**
**Default Value: 0000h**

Bit	Attribute	Default	Description
15:2	RsvdZ	0	<b>Reserved</b>
1	RW1C	0	<b>Flush Status</b> 0: No flush cycle completed                    1: Flush cycle completed This bit is set to 1 by the hardware to indicate that the flush cycle initiated when the Rx8[1] was has completed. Software must write 1 to clear this bit before the next time Rx8[1] is set to clear the bit.
0	RsvdZ	0	<b>Reserved</b>

**Offset Address: 17-12h (HDAC-MMIO) – Reserved**
**Offset Address: 1B-18h (HDAC-MMIO)**
**Stream Payload Capability**
**Default Value: 001D 003Ch**

Bit	Attribute	Default	Description
31:16	RO	001Dh	<b>Input Stream Payload Capability</b> 1Dh: 29-word payload
15:0	RO	003Ch	<b>Output Stream Payload Capability</b> 3Ch: 60-word payload

**Offset Address: 1F-1Ch (HDAC-MMIO) – Reserved**

**Interrupt Control (20-2Fh)**
**Offset Address: 23-20h (HDAC-MMIO)**
**Interrupt Control – INTCTL**
**Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RW	0	<b>Global Interrupt Enable</b> 0: Disable 1: Enable device interrupt generation
30	RW	0	<b>Controller Interrupt Enable</b> 0: Disable 1: Enable controller general interrupts
29:8	RsvdP	0	<b>Reserved</b>
7:4	RW	0	<b>Stream Interrupt Enable – for Output Stream [3:0]</b> 0: Disable 1: Enable
3:0	RW	0	<b>Stream Interrupt Enable – for Input Stream [3:0]</b> 0: Disable 1: Enable

**Offset Address: 27-24h (HDAC-MMIO)**
**Interrupt Status – INTSTS**
**Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RO	0	<b>Global Interrupt Status</b> This bit is an OR of all the interrupt status bit in this register. 0: No interrupt occurred 1: Some interrupt(s) occurred
30	RW1C	0	<b>Controller Interrupt Status</b> 0: No interrupt occurred 1: Some interrupt(s) occurred
29:8	RsvdP	0	<b>Reserved</b>
7:4	RW1C	0	<b>Stream Interrupt Status – for Output Stream [3:0]</b> 0: No interrupt occurred 1: Interrupt occurred
3:0	RW1C	0	<b>Stream Interrupt Status – for Input Stream [3:0]</b> 0: No interrupt occurred 1: Interrupt occurred

**Offset Address: 2F-28h (HDAC-MMIO) – Reserved**
**Synchronization Control (30-3Fh)**
**Offset Address: 33-30h (HDAC-MMIO)**
**Wall Clock Counter**
**Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	<b>Wall Clock Counter</b> 32 bits counter that is incremented at the link bitclk rate and rolls over from FFFF_FFFFh to 0000_0000h. This counter will roll over to zero with a period of approximately 179 seconds.

**Offset Address: 37-34h (HDAC-MMIO) – Reserved**
**Offset Address: 3B-38h (HDAC-MMIO)**
**Stream Synchronization – SSYNC**
**Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:8	RsvdP	0	<b>Reserved</b>
7:4	RW	0	<b>Stream Synchronization Bits – for Input Stream [3:0]</b> 0: Do not block data 1: Blocks data from sending on or receiving from the link
3:0	RW	0	<b>Stream Synchronization Bits – for Output Stream [3:0]</b> 0: Do not block data 1: Blocks data from sending on or receiving from the link

**Offset Address: 3F-3Ch (HDAC-MMIO) – Reserved**

**CORB (Command Output Ring Buffer) Control (40-4Fh)**
**Offset Address: 43-40h (HDAC-MMIO)**
**CORB Lower Base Address – CORBLBBASE**
**Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:7	RW	0	<b>CORB (Command Output Ring Buffer) Lower Base Address</b> Lower address of the Command Output Ring Buffer
6:0	RO	0	<b>Reserved</b> Hardwired to 0. 128 byte alignment

**Offset Address: 47-44h (HDAC-MMIO)**
**CORB Upper Base Address – CORBUBASE**
**Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	<b>CORB Upper Base Address</b> Upper 32 bits of address of the Command Output Ring Buffer

**Offset Address: 49-48h (HDAC-MMIO)**
**CORB Write Pointer**
**Default Value: 0000h**

Bit	Attribute	Default	Description
15:8	RsvdP	0	<b>Reserved</b>
7:0	RW	0	<b>CORB Write Pointer</b> Software write the last valid CORB entry offset into this field in Dword granularity. The DMA engine fetches commands from the CORB until the read point matches the write pointer. The field may be written while the DMA engine is running

**Offset Address: 4B-4Ah (HDAC-MMIO)**
**CORB Read Pointer**
**Default Value: 0000h**

Bit	Attribute	Default	Description
15	WO	0	<b>CORB Read Pointer Reset</b> Writes a 1 to reset the CORB Read Pointer to 0. DMA engine must be stopped prior to resetting the read pointer or else DMA transfer may be corrupted. This bit will always be read 0.
14:8	RsvdP	0	<b>Reserved</b>
7:0	RO	0	<b>CORB Read Pointer</b> Software read this field to determine how many commands it can write to the CORB without over-running. The value read indicates the CORB read pointer offset in Dword granularity. The offset entry read from this field has been successfully fetched by the DMA controller and may be over-written by software. Supports up to 256 CORB entries (256*4B = 1KB) in the cyclic buffer.

**Offset Address: 4Ch (HDAC-MMIO)**
**CORB Control – CORBCTL**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:2	RsvdP	0	<b>Reserved</b>
1	RW	0	<b>Enable CORB DMA Engine</b> 0: DMA Stop 1: DMA Run (when read pointer lags write pointer). Software must read the value back.
0	RW	0	<b>CORB Memory Error Interrupt Enable</b> 0: Disable 1: Enable

**Offset Address: 4Dh (HDAC-MMIO)**
**CORB Status – CORBSTS**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RsvdP	0	<b>Reserved</b>
0	RW1C	0	<b>CORB Memory Error Indication</b> 0: No error 1: Error detected. The controller has detected an error in the pathway between the controller and memory.

**Offset Address: 4Eh (HDAC-MMIO)**
**CORB Size – CORBSIZE**
**Default Value: 42h**

Bit	Attribute	Default	Description
7:4	RO	0100	<b>CORB Size Capability</b> 0100b: 256 entries (1024B)
3:2	RsvdP	0	<b>Reserved</b>
1:0	RO	10b	<b>CORB Size</b> 00: 2 entries (8 bytes)                            01: 16 entries (64 bytes) 10: 256 entries (1 KB)                            11: Reserved

**Offset Address: 4Fh (HDAC-MMIO) – Reserved**

**RIRB (Response Input Ring Buffer) Control (50-5Fh)**
Offset Address: 53-50h (HDAC-MMIO)
**RIRB Lower Base Address – RIRBLBASE**
**Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:7	RW	0	<b>RIRB (Response Input Ring Buffer) Lower Base Address</b> Lower address of the Response Input Ring Buffer
6:0	RO	0	<b>Reserved</b> Hardwired to 0. 128 byte alignment

Offset Address: 57-54h (HDAC-MMIO)
**RIRB Upper Base Address – RIRBUBASE**
**Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	<b>RIRB Upper Base Address</b> Upper 32 bits of the Response Input Output Ring Buffer.

Offset Address: 59-58h (HDAC-MMIO)
**RIRB Write Pointer – RIRBWP**
**Default Value: 0000h**

Bit	Attribute	Default	Description
15	WO	0	<b>RIRB Write Pointer Reset</b> Writes a 1 to reset the RIRB Write Pointer to 0. The DMA engine must be stopped prior to resetting the write pointer or else DMA transfer may be corrupted. This bit always read as 0.
14:8	RsvdP	0	<b>Reserved</b>
7:0	RO	0	<b>RIRB Write Pointer</b> Indicates the last valid RIRB entry written by the DMA controller. Software reads this field to determine how many responses it can read from the RIRB. The value read indicates the RIRB write pointer offset in 2 Dword units. Supports up to 256 RIRB entries in the cyclic buffer.

**Offset Address: 5B-5Ah (HDAC-MMIO)**
**Response Interrupt Count – RINTCNT**
**Default Value: 0000h**

Bit	Attribute	Default	Description
15:8	RsvdP	0	<b>Reserved</b>
7:0	RW	0	<b>N Response Interrupt Count</b> 00h: 256 responses 01h .. FFh: 1 .. 255 responses The DMA engine should be stopped when changing this field or else an interrupt may be lost.

**Offset Address: 5Ch (HDAC-MMIO)**
**RIRB Control – RIRBCTL**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RsvdP	0	<b>Reserved</b>
2	RW	0	<b>Response Overrun Interrupt Control</b> 0: Disable 1: Enable
1	RW	0	<b>Enable RIRB DMA Engine</b> 0: DMA Stop 1: DMA Run (when response queue not empty)
0	RW	0	<b>Response Interrupt Control</b> 0: Disable 1: Enable. Generate an interrupt after N number of response are sent to the RIRB buffer or when an empty response slot is encountered on all SDINx input after a frame which returned a response. The N counter is reset when the interrupt is generated.

**Offset Address: 5Dh (HDAC-MMIO)**
**RIRBSTS – RIRB Status**
**Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RsvdZ	0	<b>Reserved</b>
2	RW1C	0	<b>Response Overrun Interrupt Status</b> Hardware sets this bit to 1 when an overrun occurs in the RIRB. An interrupt may be generated if the response overrun interrupt control bit is set. 0: No overrun 1: Overrun occurred
1	RsvdZ	0	<b>Reserved</b>
0	RW1C	0	<b>Response Interrupt</b> Hardware sets this bit to 1 when an interrupt has been generated after N number of response are sent to the RIRB buffer or when an empty response slot is encountered on all SDINx inputs. 0: No response interrupt 1: Response interrupt occurred

**Offset Address: 5Eh (HDAC-MMIO)**
**RIRBSIZE – RIRBSIZE**
**Default Value: 42h**

Bit	Attribute	Default	Description
7:4	RO	0100	<b>RIRB Size Capability</b> 0100b: 256 entries (2048B)
3:2	RsvdP	0	<b>Reserved</b>
1:0	RO	10b	<b>RIRB Size</b> 00: 2 entries (16 bytes) 01: 16 entries (128 bytes) 10: 256 entries (2 KB) 11: Reserved

**Offset Address: 5Fh (HDAC-MMIO) – Reserved**

**Immediate Command Control (60-6Fh)**
**Offset Address: 63-60h (HDAC-MMIO)**
**Immediate Command Input / Output Interface**
**Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	WO	0	<b>Immediate Command Write</b> The written value will be sent out over the link in the next available frame. Reads always return 0's. Software must ensure that the ICB bit in the immediate command status register is cleared before writing a value into this register or undefined behavior will result.

**Offset Address: 67-64h (HDAC-MMIO)**
**Immediate Response Input Interface**
**Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	<b>Immediate Response Read</b> Reads return the last response came over the link.

**Offset Address: 69-68h (HDAC-MMIO)**
**Immediate Command Status**
**Default Value: 0000h**

Bit	Attribute	Default	Description
15:8	RsvdZ	0	<b>Reserved</b>
7:4	RO	0	<b>Immediate Response Result Address</b> The latched codec address
3	RO	0	<b>Immediate Response Result Unsolicited</b> 0: A solicited response latched                    1: An unsolicited response latched
2	RsvdZ	0	<b>Reserved</b>
1	RW1C	0	<b>Immediate Result Valid</b> 0: No new response 1: A new response arrived. This bit is set to 1 by hardware when a new response has been received.
0	RO	0	<b>Immediate Command Busy</b> 0: Ready for accepting an immediate command            1: Not ready Software must wait until this bit becomes 0 before writing a value in Rx63-60 (ICW).

**Offset Address: 6F-6Ah (HDAC-MMIO) – Reserved**
**DMA Position Base Address (70-7Fh)**
**Offset Address: 73-70h (HDAC-MMIO)**
**DMA Position Lower Base Address – DPLBASE**
**Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:7	RW	0	<b>DMA Position Lower Base Address</b>
6:1	RO	0	<b>DMA Position Lower Base Unimplemented Bits</b> Hardwired to 0
0	RW	0	<b>DMA Position Buffer Enable</b> 0: Disable                    1: Enable

**Offset Address: 77-74h (HDAC-MMIO)**
**DMA Position Upper Base Address – DPUBASE**
**Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	<b>DMA Position Upper Base Address</b> Upper 32 bits of the DMA Position Buffer Base Address

**Offset Address: 7F-78h (HDAC-MMIO) – Reserved**

## Stream Descriptors (80-17Fh)

### Stream Descriptor Control

**Default Value: 00 0000h**

- Offset Address 82-80h: Input Stream 0**
- Offset Address A2-A0h: Input Stream 1**
- Offset Address C2-C0h: Input Stream 2**
- Offset Address E2-E0h: Input Stream 3**
- Offset Address 102-100h: Output Stream 0**
- Offset Address 122-120h: Output Stream 1**
- Offset Address 143-140h: Output Stream 2**
- Offset Address 163-160h: Output Stream 3**

Bit	Attribute	Default	Description
23:20	RW	0	<b>Stream ID</b> A tag corresponds to the transferred data on the link 0: Unused 1 .. 0Fh: Stream 1 .. 15
19	RO	0	<b>Bidirectional Direction Control</b> Hardwired to 0. Bidirectional engine is not supported. 0: Configures as input engine 1: Configures as output engine (Read Only for non-bidirectional engines)
18	RW	0	<b>Traffic Priority</b> Hardwired to 0. The traffic will be handled on a best effort basis. 0: Handles on a “best effort” basis 1: Handles as preferred traffic
17:16	RO	0	<b>Stripe Control</b> Hardwired to 0 indicating that the controller supports 1 SDO line. 00: 1 SDO 01: 2 SDOs 10: 4 SDOs 11: Reserved (Read Only for input streams)
15:5	RsvdP	0	<b>Reserved</b>
4	RW	0	<b>Descriptor Error Interrupt Enable</b> Controls whether an interrupt is generated when the descriptor error status bit is set. 0: Disable 1: Enable
3	RW	0	<b>FIFO Error Interrupt Enable</b> Controls whether the occurrence of a FIFO error (underrun/overrun) will cause an interrupt or not. 0: Disable 1: Enable
2	RW	0	<b>Interrupt On Completion Enable</b> Controls whether an interrupt occurs when a buffer completion with the IOC bit set in its descriptor. 0: Disable 1: Enable.
1	RW	0	<b>Stream Run</b> 0: DMA disable. The DMA engine associated with this input stream will be disabled. If the corresponding Rx38 (SSYNC) bit is 0, input stream data will be taken from the link and moved to the FIFO and an overrun may occur. 1: DMA enable. The DMA engine associated with this input stream will be enabled to transfer data in the FIFO to main memory.
0	RW	0	<b>Stream Reset</b> For read: 0: Ready (not in reset state) 1: In reset state For write: 0: Exit reset 1: Reset the steam

## **Stream Descriptor Status**

**Default Value: 00h**

**Offset Address 83h: Input Stream 0**  
**Offset Address A3h: Input Stream 1**  
**Offset Address C3h: Input Stream 2**  
**Offset Address E3h: Input Stream 3**  
**Offset Address 103h: Output Stream 0**  
**Offset Address 123h: Output Stream 1**  
**Offset Address 143h: Output Stream 2**  
**Offset Address 163h: Output Stream 3**

## **Stream Descriptor Link Position in Buffer**

**Default Value:** 0000 0000h

Offset Address 87-84h: Input Stream 0  
Offset Address A7-A4h: Input Stream 1  
Offset Address C7-C4h: Input Stream 2  
Offset Address E7-E4h: Input Stream 3  
Offset Address 107-104h: Output Stream 0  
Offset Address 127-124h: Output Stream 1  
Offset Address 147-144h: Output Stream 2  
Offset Address 167-164h: Output Stream 3

Bit	Attribute	Default	Description
31:0	RO	0	<b>Link Position in Buffer</b> Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the cyclic buffer length register and then wrap to 0.

## Stream Descriptor Cyclic Buffer Length

**Default Value:** 0000 0000h

**Offset Address 8B-88h: Input Stream 0**  
**Offset Address AB-A8h: Input Stream 1**  
**Offset Address CB-C8h: Input Stream 2**  
**Offset Address EB-E8h: Input Stream 3**  
**Offset Address 10B-108h: Output Stream 0**  
**Offset Address 12B-128h: Output Stream 1**  
**Offset Address 14B-148h: Output Stream 2**  
**Offset Address 16B-168h: Output Stream 3**

Bit	Attribute	Default	Description
31:0	RW	0	<p><b>Cyclic Buffer Length</b>            Indicates the number of bytes in the completed cyclic buffer. Link position in buffer will be reset when it reaches this value.</p>

Stream Descriptor Last Valid Index
**Default Value: 0000h**

**Offset Address 8D-8Ch:** Input Stream 0  
**Offset Address AD-ACh:** Input Stream 1  
**Offset Address CD-CCh:** Input Stream 2  
**Offset Address ED-ECh:** Input Stream 3  
**Offset Address 10D-10Ch:** Output Stream 0  
**Offset Address 12D-12Ch:** Output Stream 1  
**Offset Address 14D-14Ch:** Output Stream 2  
**Offset Address 16D-16Ch:** Output Stream 3

Bit	Attribute	Default	Description
15:8	RsvdP	0	<b>Reserved</b>
7:0	RW	0	<b>Last Valid Index</b>

Stream Descriptor FIFO Size

**Offset Address 91-90h:** Input Stream 0      **Default Value: 0060h**  
**Offset Address B1-B0h:** Input Stream 1      **Default Value: 0060h**  
**Offset Address D1-D0h:** Input Stream 2      **Default Value: 0060h**  
**Offset Address F1-F0h:** Input Stream 3      **Default Value: 0060h**  
**Offset Address 111-110h:** Output Stream 0      **Default Value: 00C0h**  
**Offset Address 131-130h:** Output Stream 1      **Default Value: 00C0h**  
**Offset Address 151-150h:** Output Stream 2      **Default Value: 00C0h**  
**Offset Address 171-170h:** Output Stream 3      **Default Value: 00C0h**

Bit	Attribute	Default	Description
Input Stream			
15:8	RO	0	<b>Reserved</b>
7:0	RO	60h	<b>FIFO Size</b> The max number of bytes that can be fetched by the controller at one time
Output Stream			
15:9	RO	0	<b>Reserved</b>
8:0	RO	C0h	<b>FIFO Size</b> The max number of bytes that can be fetched by the controller at one time

## **Stream Descriptor Format**

**Default Value:** 0000h

Offset Address 93-92h: Input Stream 0  
Offset Address B3-B2h: Input Stream 1  
Offset Address D3-D2h: Input Stream 2  
Offset Address F3-F2h: Input Stream 3  
Offset Address 113-112h: Output Stream 0  
Offset Address 133-132h: Output Stream 1  
Offset Address 153-152h: Output Stream 2  
Offset Address 173-172h: Output Stream 3

Bit	Attribute	Default	Description
15	RO	0	<b>Reserved</b>
14	RW	0	<b>Sample Base Rate</b> 0: 48 KHz                    1: 44.1 KHz
13:11	RW	000b	<b>Sample Base Rate Multiple</b> 000: x1                    001: x2                    010: x3                    011: x4 Others (100 .. 111) : Reserved
10:8	RW	0	<b>Sample Base Rate Divisor</b> 0nh: Divided by (n+1), where 0<=n <=7
7	RsvdP	0	<b>Reserved</b>
6:4	RW	000b	<b>Bits per Sample</b> 000: 8 bits                    001: 16 bits                    010: 20 bits                    011: 24 bits 100: 32 bits                    Others (101 .. 111): Reserved
3:0	RW	0	<b>Number of Channels</b> 0nh: (n+1) channels, where 0<=n <=15

## **Stream Descriptor BDL Pointer Lower Base Address**

**Default Value:** 0000 0000h

Offset Address 9B-98h: Input Stream 0  
Offset Address BB-B8h: Input Stream 1  
Offset Address DB-D8h: Input Stream 2  
Offset Address FB-F8h: Input Stream 3  
Offset Address 11B-118h: Output Stream 0  
Offset Address 13B-138h: Output Stream 1  
Offset Address 15B-158h: Output Stream 2  
Offset Address 17B-178h: Output Stream 3

Bit	Attribute	Default	Description
31:7	RW	0	<b>Buffer Descriptor List Lower Base Address</b>
6:0	RO	0	<b>Unimplemented Bits</b> Hardwired to 0 for 128 bytes alignment.

**Stream Descriptor BDL Pointer Upper Base Address**
**Default Value: 0000 0000h**

Offset Address 9F-9Ch: Input Stream 0  
 Offset Address BF-BCh: Input Stream 1  
 Offset Address DF-DCh: Input Stream 2  
 Offset Address FF-FCh: Input Stream 3  
 Offset Address 11F-11Ch: Output Stream 0  
 Offset Address 13F-13Ch: Output Stream 1  
 Offset Address 15F-15Ch: Output Stream 2  
 Offset Address 17F-17Ch: Output Stream 3

Bit	Attribute	Default	Description
31:0	RW	0	Buffer Descriptor List Upper Base Address

**Alias Registers (2030-2167h)**
**Offset Address: 2033-2030h (HDAC)**
**Wall Clock Counter Alias – WALCLKA**
**Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	Wall Clock Counter Alias

**Stream Descriptor Link Position in Buffer Alias**
**Default Value: 0000 0000h**

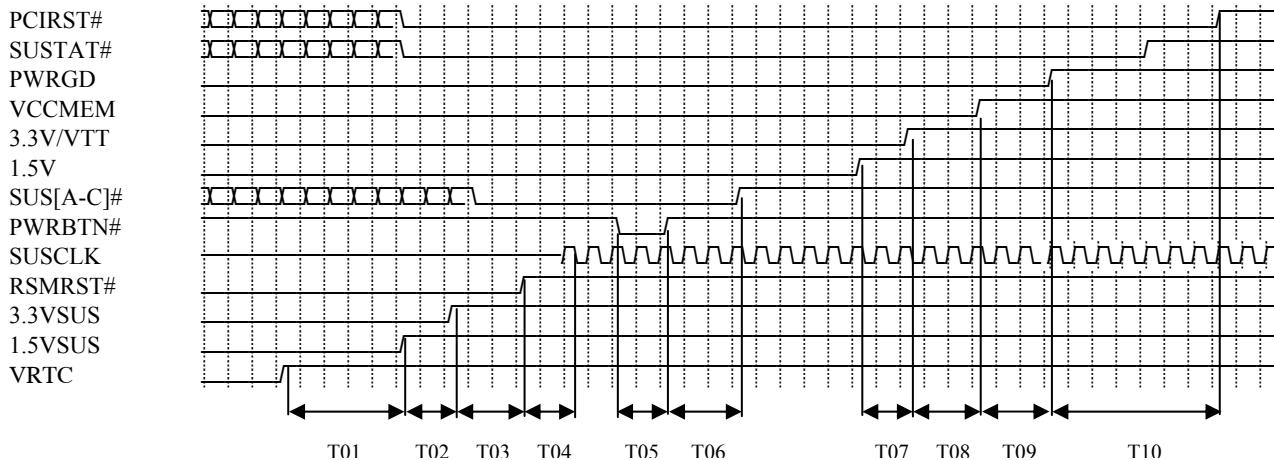
Offset Address 2087-2084h: Input Stream 0  
 Offset Address 20A7-20A4h: Input Stream 1  
 Offset Address 20C7-20C4h: Input Stream 2  
 Offset Address 20E7-20E4h: Input Stream 3  
 Offset Address 2107-2104h: Output Stream 0  
 Offset Address 2127-2124h: Output Stream 1  
 Offset Address 2147-2144h: Output Stream 2  
 Offset Address 2167-2164h: Output Stream 3

Bit	Attribute	Default	Description
31:0	RO	0	Link Position in Buffer n Alias An alias of the link position in buffer register for each stream descriptor

## ELECTRICAL SPECIFICATIONS

### Power Sequence

**Figure 5. Power On Sequence and Reset Signal Timing**



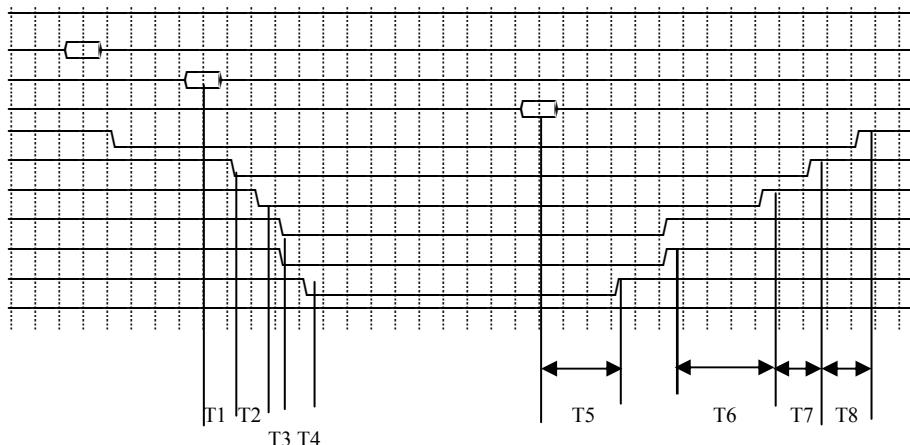
Symbol	Parameter	Min	Max	Unit	Note
T01	VRRTC supply active to 1.5VSUS supply active	0	—	ms	1
T02	1.5VSUS supply active to 3.3VSUS supply active	0.5	—	ms	
T03	3.3VSUS supply active to RSMRST # inactive	5	—	ms	
T04	RSMRST# inactive to SUSCLK running	—	—	ms	
T05	PWRBTN# active width	1	—	RTCCLK	2
T06	PWRBTN# rising to SUS[A-C]# inactive	4	5	RTCCLK	
T07	1.5V supply active to 3.3V supply active	0.5	—	ms	
T08	3.3V/VTT supply active to VCCMEM supply active	—	20	ms	
T09	VCCMEM supply active to PWRGD active	99	—	ms	
T10	PWRGD inactive to PCIRST# inactive	7	—	ms	

Note:

1. The VSUS supply should never be active while the VRTC supply is inactive. Likewise, the VCC supply should never be active while the VSUS supply is inactive.
2. If PWRBTN# debounce circuit enables B0D17F0 Rx80[5], the minimum active time is 16 ms to filter out the mechanical switch bounce.

**Figure 6. Power On Suspend Sequence without RESET**

VCC  
 POS COMMAND  
 STOP GRANT  
 WAKEUP EVENT  
 STPCLK#  
 SLP#  
 SUSTAT#  
 CPUSTP#  
 PCISTP#  
 SUSA#  
 SUS[B-C]#

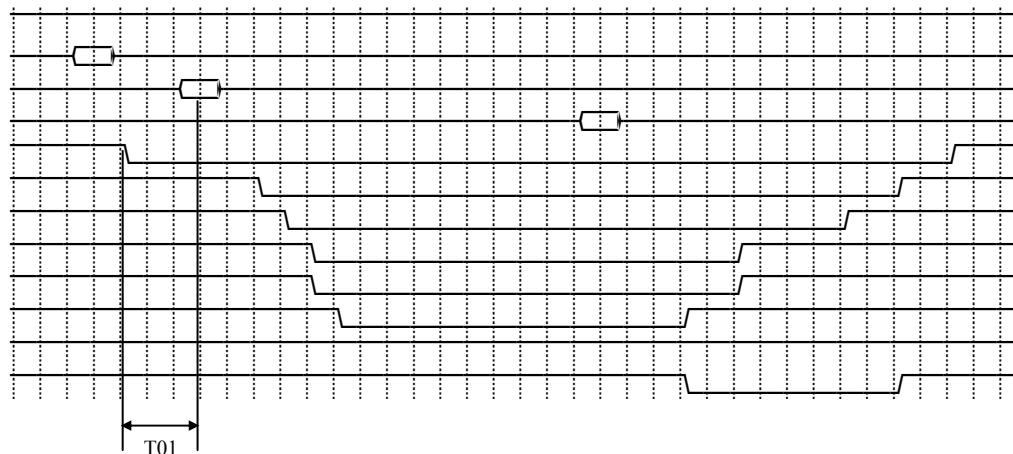


Symbol	Parameter	Min	Max	Unit	Note
T01	STOP GRANT to SLP# active	—	1	RTCCLK	
T02	SLP# active to SUSST# active	—	1	RTCCLK	
T03	SUSTAT# active to CPU/PCISTP# active	—	1	RTCCLK	
T04	CPUSTP#/PCISTP# active to SUS[A-C]# active	—	1	RTCCLK	
T05	WAKEUP event to SUS[A-C]# inactive	—	2	RTCCLK	
T06	CPUSTP#/PCISTP# inactive to SUSTAT# inactive	1	2	ms	1
T07	SUSTAT# inactive to SLP# inactive	—	1	RTCCLK	2
T08	SLP# inactive to STPCLK# inactive	—	1	RTCCLK	3

- Note:
1. If B0D17F0 Rx95[7] is set, the minimum delay is 125 us and the maximum delay is 250 us.
  2. SLP# is de-asserted if SUSTAT# is inactive or reset when PWRGD is inactive.
  3. STPCLK# is de-asserted if SLP# is inactive or reset when PWRGD is inactive.

**Figure 7. Power On Suspend Sequence with RESET**

VCC  
 POS COMMAND  
 STOP GRANT  
 WAKEUP EVENT  
 STPCLK#  
 SLP#  
 SUSTAT#  
 CPUSTP#  
 PCISTP#  
 SUSA#  
 SUS[B-C]#  
 PCIRST

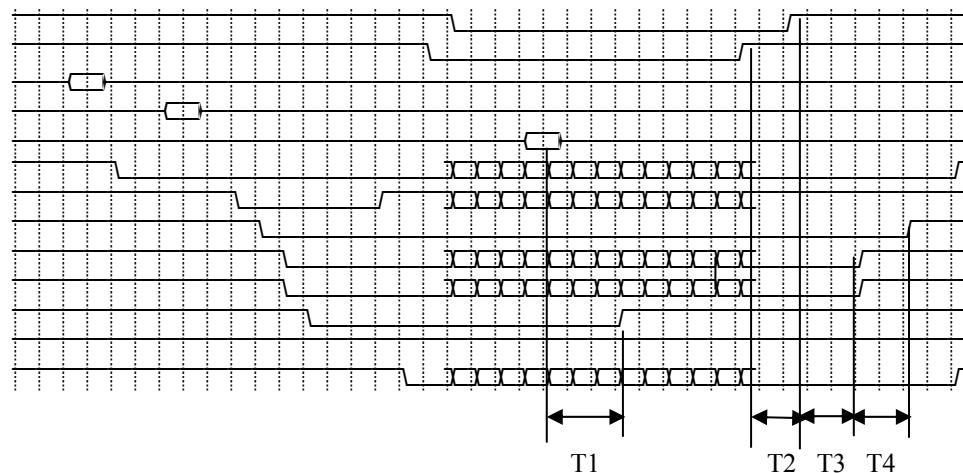


Symbol	Parameter	Min	Max	Unit	Note
T01	STPCLK# active to STOP GRANT command	—	—	—	1

Note: 1. The STPCLK# assertion will trigger the processor to send a stop grant acknowledge cycle. The timing for this cycle is dependent on the processor and the memory controller.

**Figure 8. Suspend to RAM Sequence**

PWRGD  
VCC  
STD COMMAND  
STOP GRANT  
WAKEUP EVENT  
STPCLK#  
SLP#  
SUSTAT#  
CPUSTP#  
CISTP#  
SUS[A-B]#  
SUSC#  
PCIRST

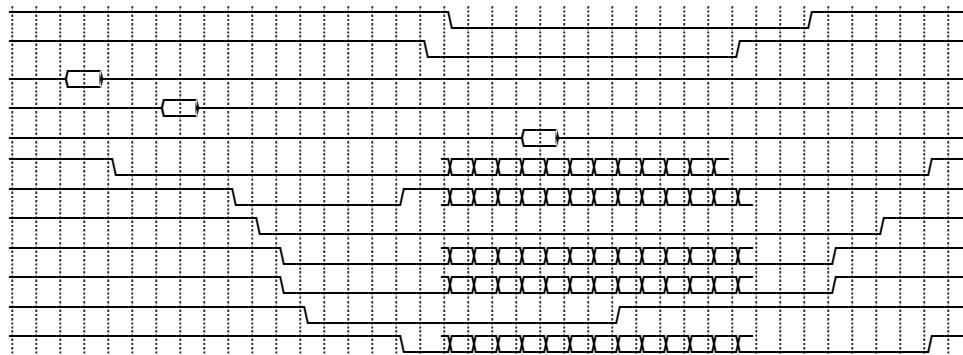


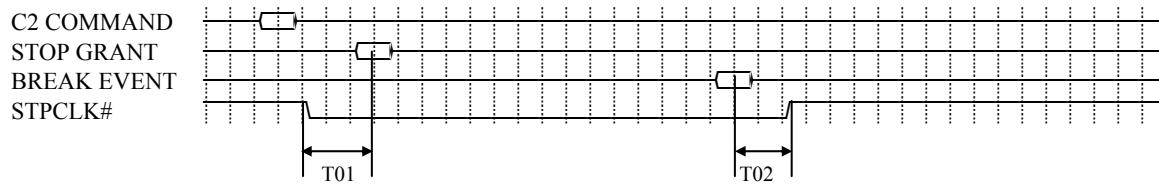
Symbol	Parameter	Min	Max	Unit	Note
T01	WAKEUP event to SUS[A-C]# inactive	—	2	RTCCLK	
T02	VCC supply active to PWRGD active	99	—	ms	
T03	PWRGD to CPUSTP#/PCISTP# inactive	16	32	ms	1
T04	CPUSTP#/PCISTP# inactive to SUSTAT# inactive	1	2	ms	2

- Note: 1. If B0D17F0 Rx95[7] is set, the minimum delay is 1 ms and the maximum delay is 2 ms.  
2. If B0D17F0 Rx95[7] is set, the minimum delay is 125 us and the maximum delay is 250 us.

**Figure 9. Suspend to DISK Sequence**

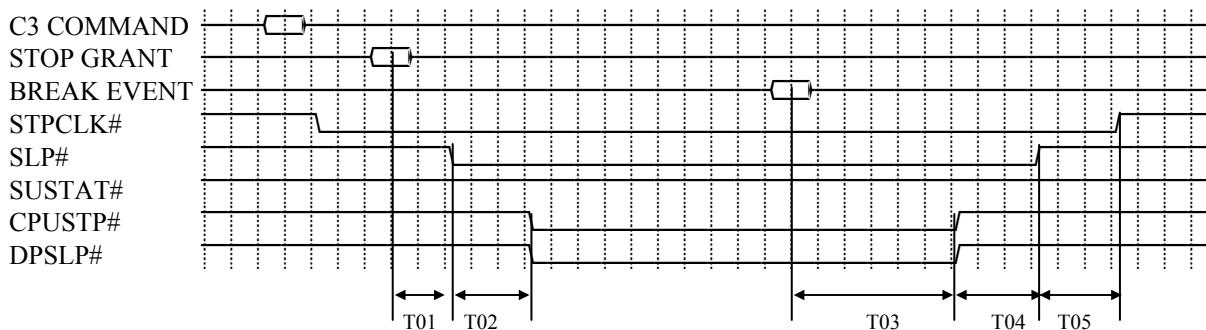
PWRGD  
VCC  
STD COMMAND  
STOP GRANT  
WAKEUP EVENT  
STPCLK#  
SLP#  
SUSTAT#  
CPUSTP#  
CISTP#  
SUS[A-C]#  
PCIRST



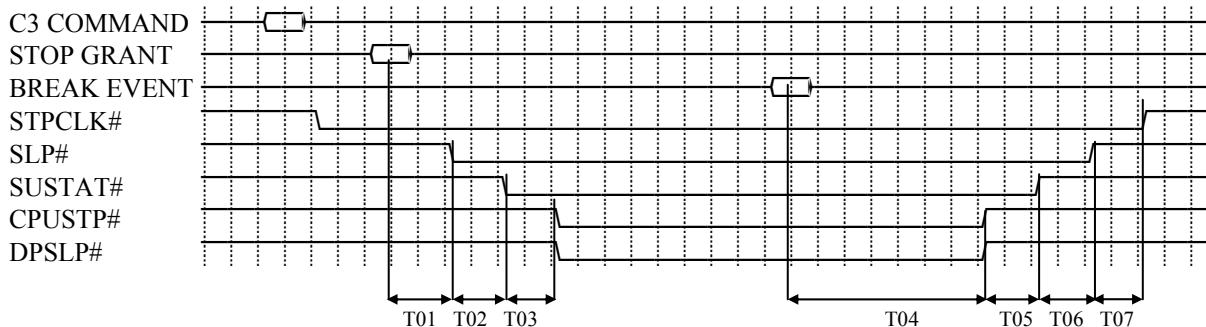
**Figure 10. CPU C2 Sequence**


Symbol	Parameter	Min	Max	Unit	Note
T01	STPCLK# active to STOP GRANT command	—	—		1
T02	Break event to STPCLK# inactive	2	—	PCICLK	

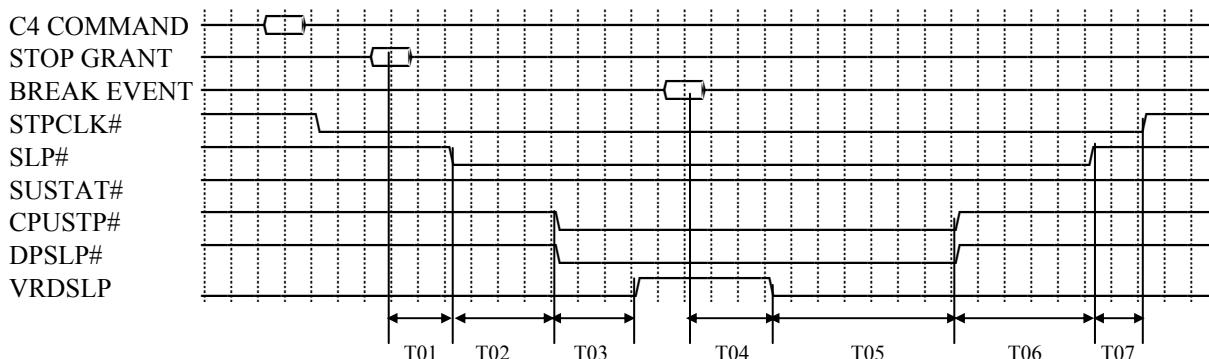
Note: 1. The STPCLK# assertion will trigger the processor to send a stop grant acknowledge cycle. The timing for this cycle is dependent on the processor and the memory controller.

**Figure 11. CPU C3 Sequence without SUSTAT#**


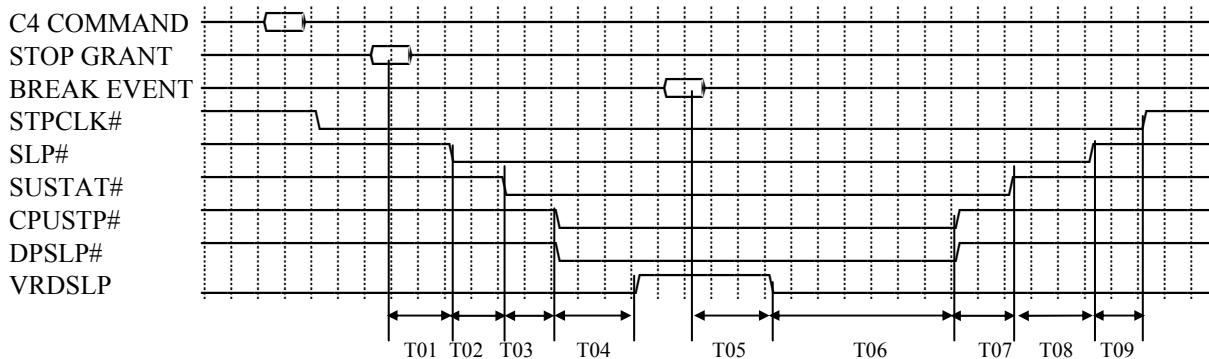
Symbol	Parameter	Min	Max	Unit	Table
T01	STOP GRANT to SLP# active	7.5	—	us	Refer to Table 16, Table 17, Table 18
T02	SLP# active to CPUSTP# active	11.25	—	us	
T03	Break Event to CPUSTP# inactive	7.5	—	us	
T04	CPUSTP# inactive to SLP# inactive	7.5	—	us	
T05	SLP# inactive to STPCLK# inactive	7.5	—	us	

**Figure 12. CPU C3 Sequence with SUSTAT#**


Symbol	Parameter	Min	Max	Unit	Table
T01	STOP GRANT to SLP# active	15	—	us	Refer to Table 16, Table 17, Table 18
T02	SLP# active to SUSTAT# active	15	—	us	
T03	SUSTAT# active to CPUSTP# active	22.5	—	us	
T04	Break Event to CPUSTP# inactive	15	—	us	
T05	CPUSTP# inactive to SUSTAT# inactive	15	—	us	
T06	SUSTAT# inactive to SLP# inactive	15	—	us	
T07	SLP# inactive to STPCLK# inactive	15	—	us	

**Figure 13. CPU C4 Sequence without SUSTAT#**


Symbol	Parameter	Min	Max	Unit	Table
T01	STOP GRANT to SLP# active	7.5	—	us	Refer to Table 16, Table 17, Table 18
T02	SLP# active to CPUSTP# active	11.25	—	us	
T03	CPUSTP# active to VRDSLP active	3.75	—	us	
T04	Break Event to VRDSLP inactive	—	7.5	us	
T05	VRDSLP inactive to CPUSTP# inactive	100	—	us	
T06	CPUSTP# inactive to SLP# inactive	7.5	—	us	
T07	SLP# inactive to STPCLK# inactive	7.5	—	us	

**Figure 14. CPU C4 Sequence with SUSTAT#**


Symbol	Parameter	Min	Max	Unit	Table
T01	STOP GRANT to SLP# active	15	—	us	Refer to Table 16, Table 17, Table 18
T02	SLP# active to SUSTAT# active	15	—	us	
T03	SUSTAT# active to CPUSTP# active	22.5	—	us	
T04	CPUSTP# active to VRDSLP active	7.5	—	us	
T05	Break Event to VRDSLP inactive	—	15	us	
T06	VRDSLP inactive to CPUSTP# inactive	100	—	us	
T07	CPUSTP# inactive to SUSTAT# inactive	15	—	us	
T08	SUSTAT# inactive to SLP# inactive	15	—	us	
T09	SLP# inactive to STPCLK# inactive	15	—	us	

**Table 16. C3 / C4 with and without SUSST#**

C3 without SUSST#

B0D17F0 RxEC[2]	B0D17F0 RxEC[7]	STPGNT to SLP# 1→0	SLP# 1→0 to CPUSTP# 1→0	Break Event to CPUSTP# 0→1	CPUSTP# 0→1 to SLP# 0→1	SLP# 0→1 to STPCLK# 0→1
0	0	7.5 us	11.25 us	7.5 us	Note 2	7.5 us
0	1	0.83 us	1.25 us	0.83 us	Note 3	0.83 us
1	X	0.56 us	0.84 us	0.56 us	0.56 us	0.56 us

C3 with SUSST#

B0D17F0 RxEC[2]	B0D17F0 RxEC[7]	STPGNT to SLP# 1→0	SLP# 1→0 to SUSST# 1→0	SUSST# 1→0 to CPUSTP# 1→0	Break Event to CPUSTP# 0→1	CPUSTP# 0→1 to SUSST# 0→1	SUSST# 0→1 to SLP# 0→1	SLP# 0→1 to STPCLK# 0→1
0	0	15 us	15 us	22.5 us	15 us	15 us	Note 2	15 us
0	1	0.83 us	0.83 us	1.25 us	0.83 us	0.83 us	Note 3	0.83 us
1	X	0.56 us	0.56 us	0.84 us	0.56 us	0.56 us	0.56 us	0.56 us

C4 without SUSST#

B0D17F0 RxEC[2]	B0D17F0 RxEC[7]	STPGNT to SLP# 1→0	SLP# 1→0 to CPUSTP# 1→0	CPUSTP# 1→0 to VRDSLP 0→1	Break Event to VRDSLP 1→0	VRDSLP 1→0 to CPUSTP# 0→1	CPUSTP# 0→1 to SLP# 0→1	SLP# 0→1 to STPCLK# 0→1
0	0	7.5 us	11.25 us	7.5 us	7.5 us	100 us	Note 2	7.5 us
0	1	0.83 us	1.25 us	0.83 us	0.83 us	10 us	Note 3	0.83 us
1	X	X	X	X	X	X	X	X

C4 with SUSST#

B0D17F0 RxEC[2]	B0D17F0 RxEC[7]	STPGNT to SLP# 1→0	SUSST# 1→0 to CPUSTP# 1→0	CPUSTP# 1→0 to VRDSLP 0→1	Break Event to VRDSLP 1→0	VRDSLP 1→0 to CPUSTP# 0→1	CPUSTP# 0→1 to SUSST# 0→1	SLP# 0→1 to STPCLK# 0→1
0	0	15 us	22.5 us	15 us	15 us	100 us	15 us	15 us
0	1	0.83 us	1.25 us	0.83 us	0.83 us	10 us	Note 3	0.83 us
1	X	X	X	X	X	X	X	X

**Table 17. CPUSTP# or DPSLP# Inactive to SLP# Inactive Latency**

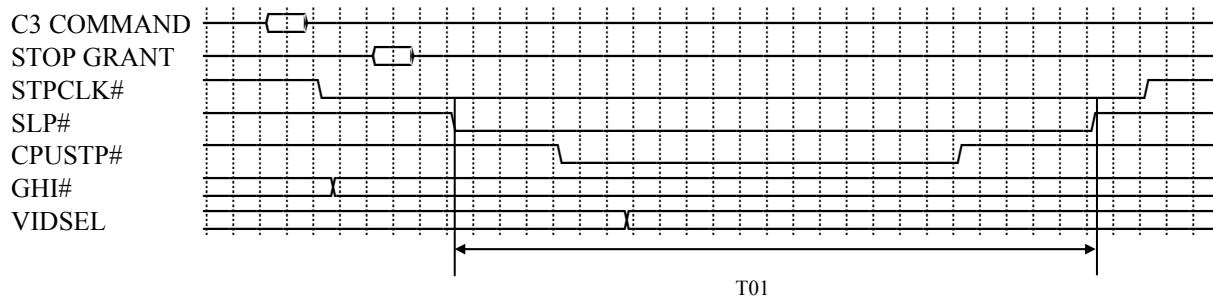
Table 1 When B0D17F0 RxE4[7]=0

B0D17F0 RxEC7[0]	B0D17F0 RxEC7[1]	DPSLP# 0→1 to SLP# 0→1
0	0	7.5 us
1	0	15 us
0	1	22.5 us
1	1	30 us

**Table 18. CPUSTP# or DPSLP# Inactive to SLP# Inactive Latency**

When B0D17F0 RxE4[7]=1

B0D17F0 RxEC7[0]	B0D17F0 RxEC7[1]	DPSLP# 0→1 to SLP# 0→1
0	0	0.83 us
1	0	1.5 ~ 7.5 us
0	1	7.5 ~ 15 us
1	1	10 ~ 22.5 us

**Figure 15. CPU Speedstep Sequence**


Symbol	Parameter	Min	Max	Unit	Note
T01	SLP# asserted time	min	max		1

Note: 1. {B0D17F0 RxE5[7], RxE4[7], RxEC[2]}= {0,0,0}, min= 120 us, max=160 us  
     {B0D17F0 RxE5[7], RxE4[7], RxEC[2]}= {0,0,1}, min= 2.7 us, max=3.4 us  
     {B0D17F0 RxE5[7], RxE4[7], RxEC[2]}= {0,1,0}, min= 13 us, max=18 us  
     {B0D17F0 RxE5[7], RxE4[7], RxEC[2]}= {1,0,0}, min= 240 us, max=290 us  
     {B0D17F0 RxE5[7], RxE4[7], RxEC[2]}= {1,1,0}, min= 26 us, max=31 us

## DC Characteristics

$T_C = 0 \sim 85^\circ\text{C}$ ,  $V_{RAIL} = V_{CC} \pm 10\%$ ,  $V_{CORE} = 1.5\text{V} \pm 10\%$ ,  $GND = 0\text{V}$

**Table 19. DC Characteristics**

Symbol	Parameter	Min	Max	Unit	Condition
$V_{IL}$	Input Low Voltage	-0.5	0.7	V	
$V_{IH}$	Input High Voltage	2.3	$V_{CC} + 0.5$	V	
$V_{OL}$	Output Low Voltage	-	0.87	V	
$V_{OH}$	Output High Voltage	2.4	-	V	
$I_{IL}$	Input Leakage Current	-	$\pm 10$	$\mu\text{A}$	$0 < V_{IN} < V_{CC}$
$I_{OZ}$	Tristate Leakage Current	-	$\pm 20$	$\mu\text{A}$	$0.55 < V_{OUT} < V_{CC}$

## MECHANICAL SPECIFICATIONS

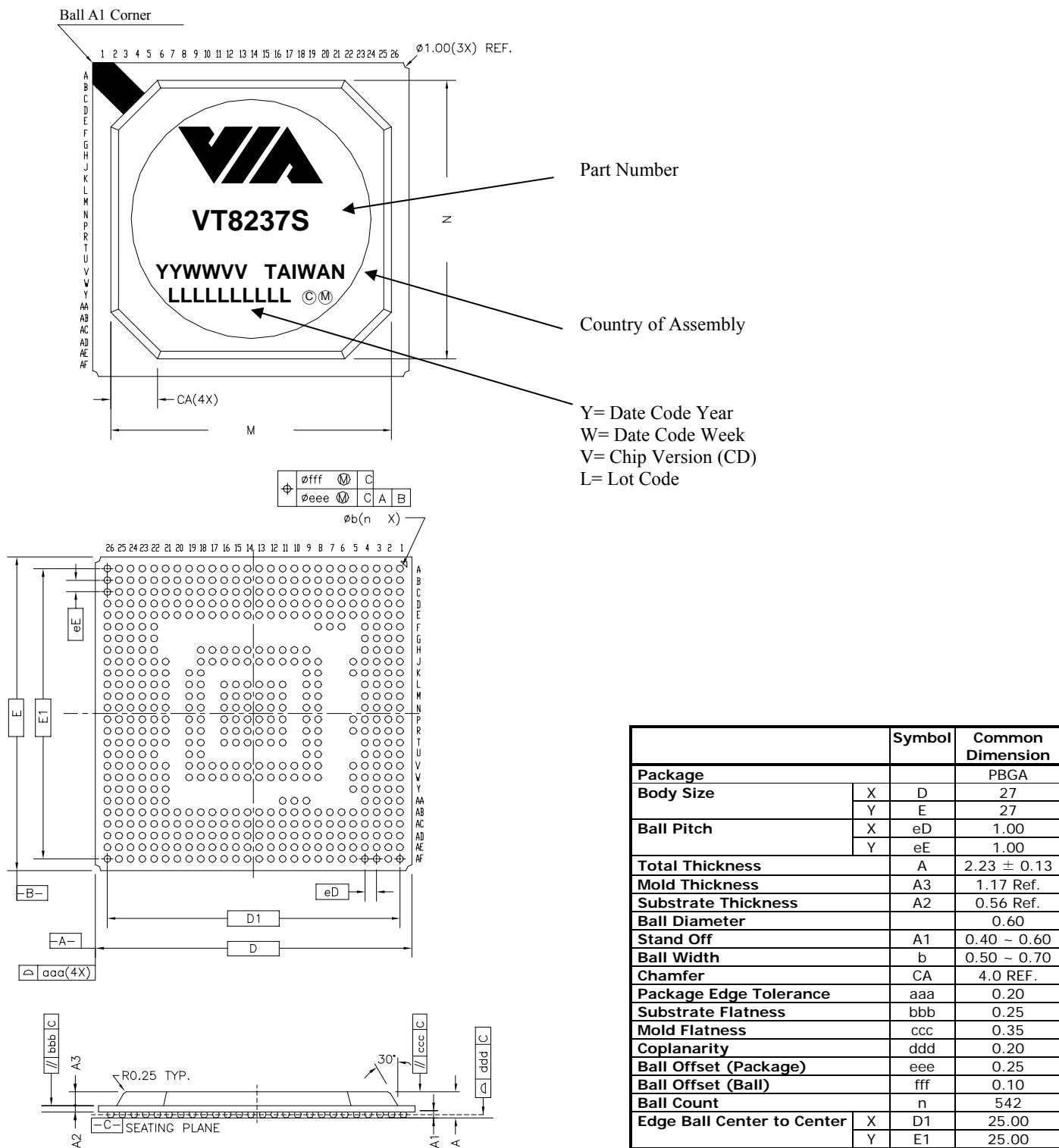
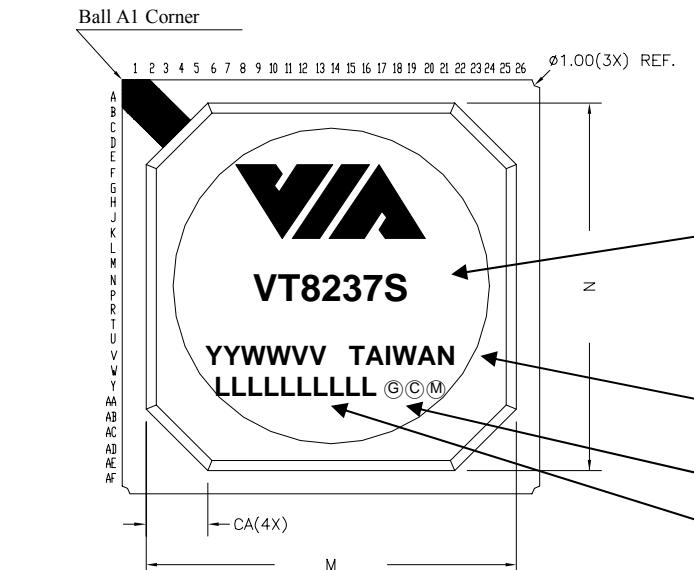


Figure 16. Mechanical Specifications – PBGA-542 Ball Grid Array Package



Part Number

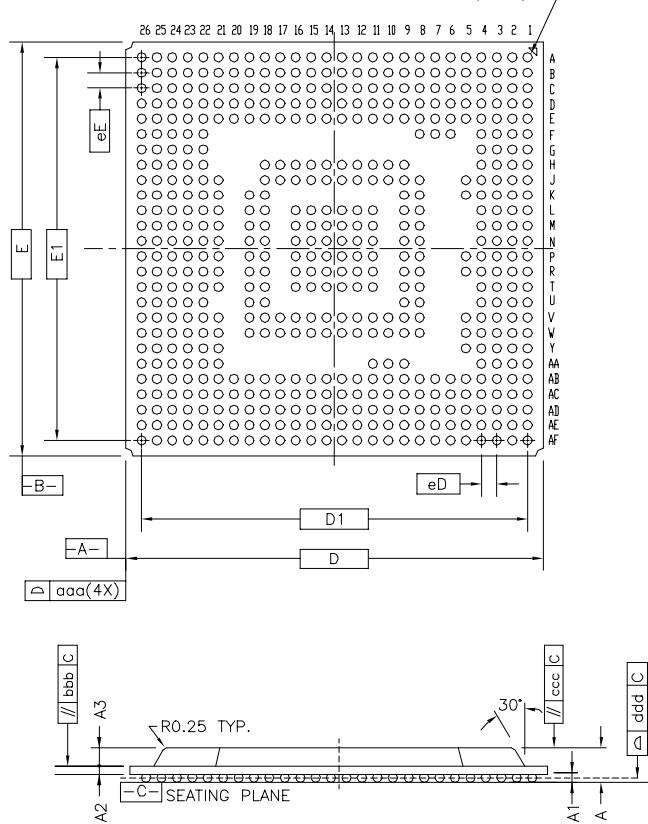
Country of Assembly

Lead-Free

Y= Date Code Year  
 W= Date Code Week  
 V= Chip Version (CD)  
 L= Lot Code

$\oplus$	$\varnothing ffff$	$\ominus$	C
	$\varnothing eee$	$\ominus$	C A B

$\varnothing b(n X)$



	Symbol	Common Dimension
<b>Package</b>		PBGA
<b>Body Size</b>	X	D 27
	Y	E 27
<b>Ball Pitch</b>	X	eD 1.00
	Y	eE 1.00
<b>Total Thickness</b>	A	$2.23 \pm 0.13$
<b>Mold Thickness</b>	A3	1.17 Ref.
<b>Substrate Thickness</b>	A2	0.56 Ref.
<b>Ball Diameter</b>		0.60
<b>Stand Off</b>	A1	$0.40 \sim 0.60$
<b>Ball Width</b>	b	$0.50 \sim 0.70$
<b>Chamfer</b>	CA	4.0 REF.
<b>Package Edge Tolerance</b>	aaa	0.20
<b>Substrate Flatness</b>	bbb	0.25
<b>Mold Flatness</b>	ccc	0.35
<b>Coplanarity</b>	ddd	0.20
<b>Ball Offset (Package)</b>	eee	0.25
<b>Ball Offset (Ball)</b>	fff	0.10
<b>Ball Count</b>	n	542
<b>Edge Ball Center to Center</b>	X	D1 25.00
	Y	E1 25.00

**Figure 17. Lead-Free Mechanical Specifications – PBGA-542 Ball Grid Array Package**