Apollo Pro266T North Bridge

Socket-370 North Bridge with 133 / 100 / 66 MHz Front Side Bus for VIA C3 and Intel Celeron, Pentium III and Pentium III-M (Tualatin) CPUs with AGP 4x and V-Link plus Advanced ECC Memory Controller supporting DDR266 / DDR200 (PC2100 / PC1600) DDR SDRAM and PC133 / PC100 SDR SDRAM for Desktop and Mobile PC Systems

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VIA TECHNOLOGIES, INC.

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REVISION HISTORY

Document Release	Date	Revision	Initials
1.0	1/7/02	Initial external release (same as internal revision 0.4 except for package type update to HSBGA and VIA logo on cover page updated to current style)	DH
1.01	1/31/02	Updated company address; fixed marking spec to remove “Apollo”	DH
1.1	5/6/03	Updated legal page formatting, VIA USA street address, and VIA logos Changed chipset name to be north bridge chip name & removed VT# Fixed V-Link feature bullets; Fixed incorrect JEDEC-spec reference in mech diagram	DH

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

Apollo Pro266T North Bridge

Socket-370 North Bridge
with 133 / 100 / 66 MHz Front Side Bus
for VIA C3 and Intel Celeron,
Pentium III, and Pentium III-M (Tualatin) CPUs
with AGP 4x and V-Link
plus Advanced ECC Memory Controller
supporting DDR266 / DDR200 (PC2100 / PC1600) DDR SDRAM
and PC133 / PC100 SDR SDRAM
for Desktop and Mobile PC Systems

PRODUCT FEATURES

- **AGP / PCI / ISA Mobile and Deep Green PC Ready**
  - GTL+ compliant host bus supports write-combine cycles
  - Supports separately powered 3.3V LVTTL (5V tolerant) and 2.5V SSTL-2 interface to system memory
  - Modular power management and clock control for power conscious system applications
  - Combine with VIA VT8233 highly integrated south bridge chip for state-of-the-art system power management
- **High Integration**
  - Single chip implementation for 64-bit Socket-370 CPU, 64-bit SDR/DDR system memory, 266MB/S high bandwidth V-Link NB/SB, and 32-bit AGP interfaces
  - Chipset: **Apollo Pro266T** V-Link Host system controller and **VT8233** V-Link to PCI/LPC bridge
  - Chipset includes UltraDMA-100 / 66 / 33 EIDE, Six USB ports, AC-97 audio and HSP modem, Networking, PCI / LPC buses, SMBus, and Keyboard / PS2-Mouse Interfaces plus RTC / CMOS on chip
- **High Performance CPU Interface**
  - Supports Socket-370 VIA C3™ and Intel Celeron™, Pentium III™ and Pentium III-M™ (Tualatin) processors
  - 133 / 100 / 66 MHz CPU Front Side Bus (FSB)
  - Built-in PLL (Phase Lock Loop) circuitry for optimal skew control within and between clocking regions
  - Eight outstanding transactions (eight-level In-Order Queue)
  - Supports WC (Write Combining) cycles
  - Dynamic deferred transaction support
  - Sleep mode support
  - System management interrupt, memory remap and STPCLK mechanism

- **Full Featured Accelerated Graphics Port (AGP) Controller**
  - Synchronous and pseudo-synchronous with the host CPU bus with optimal skew control

V-Link	AGP	CPU	Mode
66 MHz	66 MHz	133 MHz	4x synchronous
66 MHz	66 MHz	100 MHz	3x synchronous
66 MHz	66 MHz	66 MHz	2x synchronous

  - AGP v2.0 compliant
  - Supports SideBand Addressing (SBA) mode (non-multiplexed address / data)
  - Supports 266 MHz 4x mode for AD and SBA signaling
  - Pipelined split-transaction long-burst transfers up to 1GB/sec
  - Eight level read request queue
  - Four level posted-write request queue
  - Thirty-two level (quadwords) read data FIFO (256 bytes)
  - Sixteen level (quadwords) write data FIFO (128 bytes)
  - Intelligent request reordering for maximum AGP bus utilization
  - Supports Flush/Fence commands
  - Graphics Address Relocation Table (GART)
    - One level TLB structure
    - Sixteen entry fully associative page table
    - LRU replacement scheme
    - Independent GART lookup control for host / AGP / PCI master accesses
  - Windows 95 OSR-2 VXD and integrated Windows 98 / NT5 miniport driver support
- **High Bandwidth 266 MB/Sec 8-bit V-Link Host Controller**
  - Supports 66MHz V-Link Host interface with total bandwidth of 266MB/S
  - V-Link operates at 4x or 2x modes
  - Full duplex commands with separate STB / CMD
  - Request/Data split transaction
  - Configurable outstanding transaction queue for Host to V-Link Client accesses
  - Supports Defer/Defer-Reply transaction
  - Transaction assurance for V-Link Host to Client access. Eliminate V-Link Host-Client Retry cycles
  - Intelligent V-Link transaction protocol to eliminate data wait-state/throttle transfer latency. All V-Link transaction both Host and Client have consistent view of transaction data depth and buffer size to avoid data overflow.
  - High efficient V-Link arbitration with minimum overhead. All V-Link transaction with predictable cycle length with known CMD/Date duration.

- **Advanced High-Performance DDR / SDR DRAM Controller**
  - DRAM interface synchronous with host CPU (133 / 100 / 66 MHz) for most flexible configuration
  - DRAM interface may be faster than CPU by 33 MHz to allow use of PC100 / DDR200 memory modules with 66MHz Celeron or use of PC133 / DDR266 with 100MHz Pentium II or Pentium III
  - DRAM interface may be slower than CPU by 33 MHz to allow use of older memory modules with newer CPUs (e.g., PC66 memory modules with 100 MHz Pentium II or Pentium III)
  - Concurrent CPU, AGP, and PCI access
  - Supports DDR and SDR SDRAM memory types
  - Dynamic Clock Enable (CKE) control for SDRAM power reduction in high speed systems
  - Mixed 1M / 2M / 4M / 8M / 16M / 32M /64MxN DRAMs
  - Supports 8 banks up to 4 GB DRAMs (512Mb x8 / x16 DRAM technology) for registered DDR / SDR modules
  - Supports 6 banks up to 3 GB DRAMs (512Mb x8 / x16 DRAM technology) for unbuffered DDR / SDR modules
  - Flexible row and column addresses. 64-bit data width only
  - LVTTL 3.3V DRAM interface with 5V-tolerant inputs for SDR SDRAM and 2.5V SSTL-2 DRAM interface for DDR SDRAM
  - Programmable I/O drive capability for MA, command, and MD signals
  - Dual copies of MA and control signals for improved drive
  - Optional ECC (single-bit error correction and multi-bit error detection) or EC (error checking only) for DRAM integrity
  - Two-bank interleaving for 16Mbit SDRAM support
  - Two-bank and four bank interleaving for 64Mbit SDRAM support
  - Supports maximum 16-bank interleave (i.e., 16 pages open simultaneously); banks are allocated based on LRU
  - Seamless DRAM command scheduling for maximum DRAM bus utilization (e.g., precharge other banks while accessing the current bank)
  - Four cache lines (16 quadwords) of CPU to DRAM write buffers
  - Four cache lines of CPU to DRAM read prefetch buffers
  - Read around write capability for non-stalled CPU read
  - Speculative DRAM read before snoop result
  - Burst read and write operation
  - x-1-1-1-1-1-1-1 back-to-back accesses for SDR SDRAM
  - x-1/2-1/2-1/2-1-1/2-1/2-1/2 back-to-back accesses for DDR SDRAM
  - Supports DDR SDRAM CL 2/2.5/3 and 1T per command
  - Decoupled and burst DRAM refresh with staggered RAS timing (CAS before RAS or self refresh)
- **Advanced System Power Management Support**
  - Dynamic power down of SDRAM (CKE)
  - V-Link and AGP bus clock run and clock generator control
  - VTT suspend power plane preserves memory data
  - Suspend-to-DRAM and Self-Refresh operation
  - SDRAM self-refresh power down
  - 8 bytes of BIOS scratch registers
  - Low-leakage I/O pads
- **Built-in NAND-tree pin scan test capability**
- **2.5V, 0.22um, high speed / low power CMOS process**
- **35 x 35 mm, 560 pin HSBGA Package (Ball Grid Array with Heat Spreader)**

OVERVIEW

Apollo Pro266T is a high performance, cost-effective and energy efficient chip set for the implementation of AGP / V-Link / PCI / LPC desktop personal computer systems with 133, 100 and 66 MHz front side bus frequencies based on 64-bit Socket-370 VIA C3 and Intel Celeron, Pentium-III, and Pentium II-M (Tualatin) super-scalar processors.

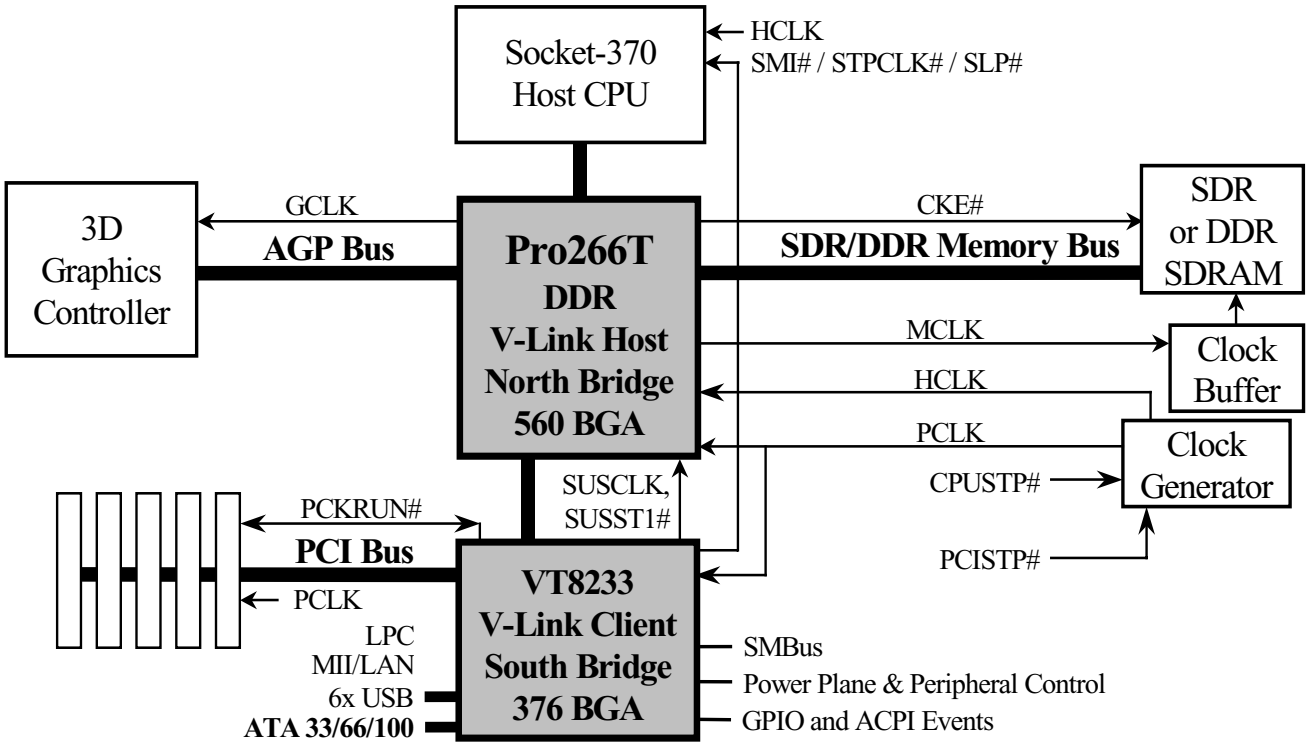


Figure 1. Apollo Pro266T System Block Diagram

The complete chip set consists of the Apollo Pro266T V-Link DDR Host system controller (560 pin BGA) and the VT8233 highly integrated V-Link Client PCI/LPC controller (376 pin BGA). The Host system controller provides superior performance between the CPU, DRAM, AGP bus, and V-Link interface with pipelined, burst, and concurrent operation. The VT8233 V-Link Client controller is a highly integrated PCI / LPC controller. Its internal bus structure is based on 66 MHz PCI bus that provides 2x bandwidth compare to previous generation PCI/ISA bridge chips. The VT8233 integrated Client V-Link controller with 266MB/S bandwidth between Host/Client V-Link interface, provides a V-Link-PCI and V-Link-LPC controller. It supports five PCI slots of arbitration and decoding for all integrated functions and LPC bus.

The Apollo Pro266T supports eight banks of DDR / SDR SDRAMs up to 4 GB for "registered" SDRAM modules (six banks up to 3GB for "unbuffered" modules). The DRAM controller supports Double-Data-Rate (DDR) SDRAM or can be configured to support standard Synchronous DRAM (SDR SDRAM). The DDR / SDR DRAM interface allows zero wait state bursting between the DRAM and the data buffers at 133 / 100 / 66 MHz. The eight banks of DRAM can be composed of an arbitrary mixture of 1M / 2M / 4M / 8M / 16M / 32M / 64M xN DRAMs. The DRAM controller also supports optional ECC (single-bit error correction and multi-bit detection) or EC (error checking) capability. The DRAM controller can run in either synchronous or pseudo-synchronous mode relative to the host CPU bus frequency (133 / 100 / 66 MHz).

The Apollo Pro266T Host system controller also supports full AGP v2.0 capability for maximum bus utilization including 2x and 4x mode transfers, SBA (SideBand Addressing), Flush/Fence commands, and pipelined grants. An eight level request queue plus a four level post-write request queue with thirty-two and sixteen quadwords of read and write data FIFO's respectively are included for deep pipelined and split AGP transactions. A single-level GART TLB with 16 full associative entries and flexible CPU / AGP / PCI remapping control is also provided for operation under protected mode operating environments. Both Windows-95 VXD and Windows-98 / NT5 miniport drivers are supported for interoperability with major AGP-based 3D and DVD-capable multimedia accelerators.

The Apollo Pro266T host system controller supports a high speed 8-bit 66 MHz Quad Data Transfer interconnect (V-Link) to the VT8233 South Bridge. The chip also contains a built-in bus-to-bus bridge to allow simultaneous concurrent operations on each bus. Five levels (doublewords) of post write buffers are included to allow for concurrent CPU and V-Link operation. For V-Link Host operation, forty-eight levels (doublewords) of post write buffers and sixteen levels (doublewords) of prefetch buffers are included for concurrent V-Link bus and DRAM / cache accesses. When combined the V-Link Host/Client controllers, it realizes a complete PCI sub-system and supports enhanced PCI bus commands such as Memory-Read-Line, Memory-Read-Multiple and Memory-Write-Invalid commands to minimize snoop overhead. In addition, advanced features are supported such as snoop ahead, snoop filtering, L1 write-back forward to PCI master, and L1 write-back merged with PCI post write buffers to minimize PCI master read latency and DRAM utilization. Delay transaction and read caching mechanisms are also implemented for further improvement of overall system performance.

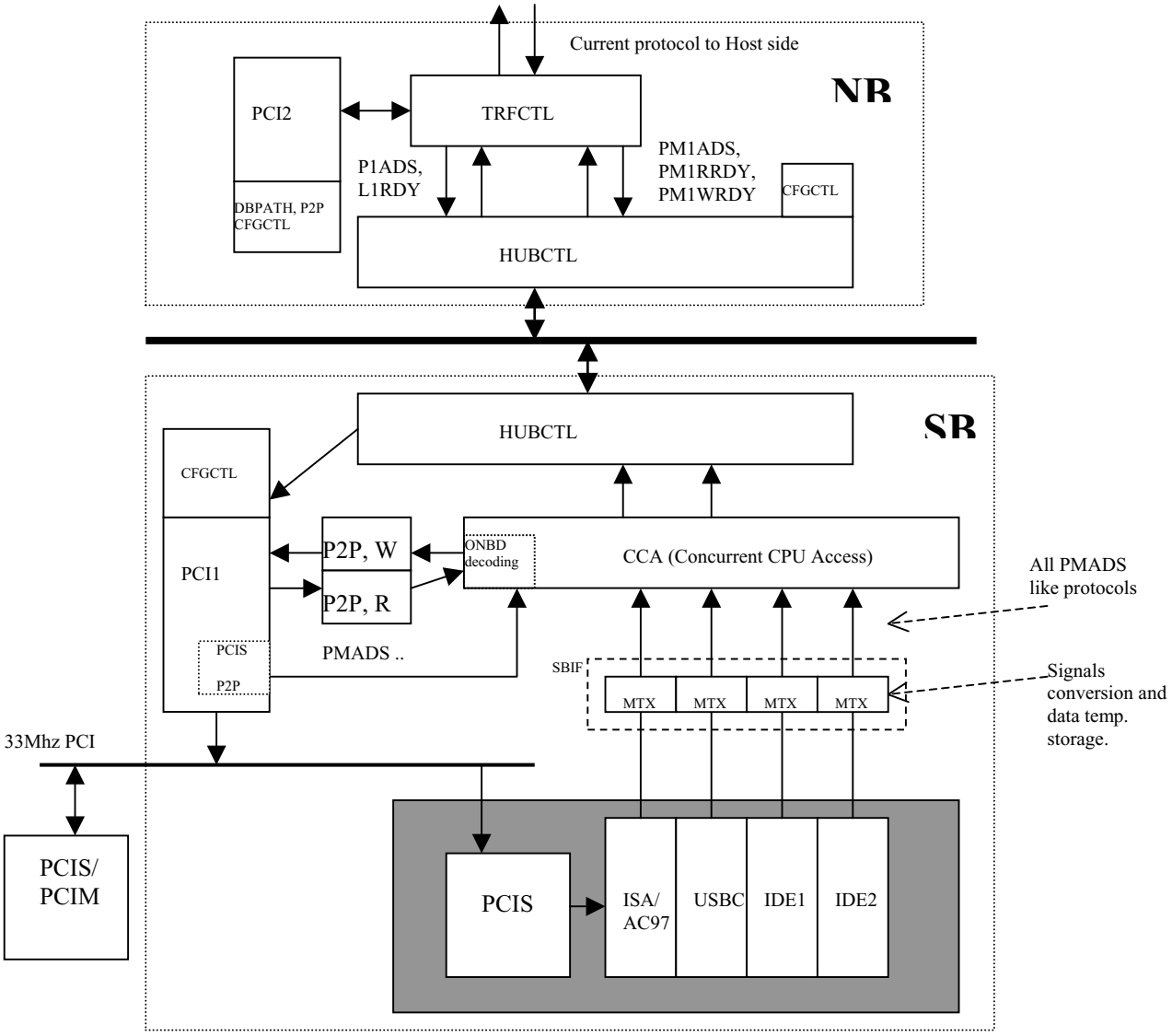
The 376-pin Ball Grid Array VT8233 Client V-Link PCI / LPC controller supports four levels (doublewords) of line buffers, type F DMA transfers and delay transaction to allow efficient PCI bus utilization and (PCI-2.2 compliant). The VT8233 integrated PCI controller and PCI arbitration for up to five PCI slots. One of the PCI REQ / GNT pair can be configured as high-priority to better support a low latency PCI bus master device. The VT8233 integrated networking MAC controller with standard MII interface to an external PHY for 10 / 100Mb base-T Ethernet or 1 / 10Mb PNA home networking.

The VT8233 also includes an integrated keyboard controller with PS2 mouse support, integrated DS12885 style real time clock with extended 256 byte CMOS RAM, integrated master mode enhanced IDE controller with full scatter / gather capability and extension to UltraDMA-100 / 66 / 33 for 100 / 66 / 33 MB/sec transfer rate, integrated USB interface with root hubs and six function ports with built-in physical layer transceivers, Distributed DMA support, and OnNow / ACPI compliant advanced configuration and power management interface.

For sophisticated power management, the Apollo Pro266T chipset provides independent clock stop control for the CPU / SDRAM, PCI, and AGP buses and Dynamic CKE control for powering down of the SDRAM. A separate suspend-well plane is implemented for the SDRAM control signals for Suspend-to-DRAM operation. Coupled with the VT8233 south bridge chip, a complete power conscious PC main board can be implemented with no external TTLs.

The Apollo Pro266T chipset is ideal for high performance, high quality, high energy efficient and high integration desktop and notebook AGP / PCI / LPC computer systems.

Figure 2. Apollo Pro266T V-Link Chipset Block Diagram



PINOUTS

Figure 3. Ball Diagram (Top View)

Key	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
A	VCC AGP	VCC AGP	GD16	GD17	AGP VREF	VCC AGP	GD23	GD24	GD28	VCC AGP	SBA7	SBS#	SBA0	VCC AGP	HD62	HD54	HD59	HD49	HD45	HD37	HD34	HD35	HD25	HD24	HD16	VTT
B	GD15	GBE1#	GBE2#	GND	GD21	VCC AGP	GBE3#	GD27	GD30	VCC AGP	SBA4	SBS	SBA1	VCC AGP	HD50	HD46	HD52	HD51	HD42	HD39	HD22	HD19	HD26	HD23	HD30	HD7
C	GD11	GD12	GD13	GD14	GD19	GD20	GD22	GD26	GD31	GRBF#	SBA5	GND	GGNT#	HD56	HD60	HD58	HD57	HD47	GND	HD36	HD31	HD32	GND	HD21	HD20	HD13
D	GD8	GND	GBE0#	GND	GD18	GND	GDEV SEL#	GD25	ST0	ST2	GPIPE#	SBA3	SBA2	GREQ#	HD61	HD53	HD48	HD41	HD27	HD38	HD28	HD33	HD3	HD11	HD14	HD2
E	VCC AGP	VCC AGP	GDS0#	GD10	G STOP#	GT RDY#	G FRM#	GDS1	GWBF#	GND	SBA6	VCC AGP	ST1	CPU RSTD	VCC	HD55	HD63	GND	HD44	HD43	HD29	HD9	HD18	HD12	HD10	HD17
F	GD7	GD4	GD6	GDS0	GD9	GND	GND	GDS1#	GD29	GND	GI RDY#	VCC AGP	GND	GND	VCC	GTL VREF	HD40	GND	VTT	GND	GND	HD5	HD8	HD1	HD4	HD15
G	GD5	GND	GCLK	GND	GPAR	VCC AGP	G7	8	9	10	11	12	13	14	VTT	16	17	VCC	VTT	VTT	GND	HD0	HD6	CPU RST#	HA26	HA29
H	GD1	GD3	GD0	GD2	VCC QQ	VCC AGP	H	AGP Pins							15			18	19	H20	VTT	HA27	HA30	GND	HA18	HA24
J	VCC AGP	G COMP	GND QQ	VAD0 strap	GND	GND	J		VCC AGP	VCC AGP	VCC	VCC	VCC AGP	VCC	VCC	VCC	VCC	VTT		J	GND	HA20	HA23	HA31	HA22	HA17
K	UP STB	UP STB#	UP CMD	VBE#	VL VREF	VAD1 strap	K	Vlink	VCC AGP	K10	11	12	13	14	15	16	K17	VTT	K	VTT	VTT	HCLK	HA25	HA19	HA10	HA21
L	DN CMD	DN STB	DN STB#	VPAR	VAD4	VAD2 strap	L	Pins	VCC	L	GND	GND	GND	GND	GND	GND	L	VCC	CPU Pins	L	AVCC HCK	AGND HCK	TEST IN#	HA28	HA5	HA12
M	VCC VL	VCC VL	GND	GND	VCC VL	VCC VL	M		VCC	M	GND	GND	GND	GND	GND	GND	M	VCC		M	HA6	HA15	HA13	HA16	HA3	HA9
N	VCC VK	VAD6	VAD7	VAD5	VAD3 strap	VCC VL	N		VCC VL	N	GND	GND	GND	GND	GND	GND	N	VTT		N	HREQ 4#	HA8	HA11	HA14	BNR#	HA4
P	VL COMP	GND	PWR OK	RE SET#	GND	GND	P		VCC M	P	GND	GND	GND	GND	GND	GND	P	VTT	P	VTT	GND	GND	HREQ 0#	GND	HREQ 2#	BPRI#
R	MD58	MD63	MD59	VSUS 25	SUST#	VCCM	R		VCC	R	GND	GND	GND	GND	GND	GND	R	VCC	R	VTT	VTT	HA7	HREQ 1#	H LOCK#	DE FER#	HREQ 3#
T	VCCM	VCCM	GND	GND	MD62	VCCM	T		VCC	T	GND	GND	GND	GND	GND	GND	T	VCC	T	VTT	GTL VREF	GND	RS1#	HITM#	HIT#	RS0#
U	MD57	DQM7 CKE7	DQS7# CKE7	MD61	MD56	MD60	U		VCC M	U10	11	12	13	14	15	16	U17	VCC M		U	AVCC MCK	AGND MCK	HT RDY#	DBSY#	RS2#	DRDY#
V	MD51	MD55	MD50	MD54	MD53	M VREF	V		VCC M	VCC M	VCC	VCC	VCC M	VCC M	VCC	VCC	VCC M	VCC M		V	GND	MCLK F	MCLK	GND	BREQ 0#	GND
W	DQS6# CKE6	DQM6 CKE6	MD52	AGND DL2	AVCC DL2	GND	W						DDR Pins							W	VCCM	VCCM	MD0	ADS#	VCCM	VCCM
Y	VCCM	VCCM	GND	GND	CS7#	VCCM	Y7	8	9	10	11	12	13	14	15	16	17	18	19	Y20	GND	MAB 14	MAA 14	GND	MD5	MD4
AA	MD49	MD48	MD47	MD46	CS6#	GND	VCCM	GND	VCCM	AVCC DL1	GND	VCCM	GND	VCCM	VCCM	GND	VCCM	MD18	M VREF	VCCM	GND	MAA 8	MD2	DQM0 CKE0	MD1	DQS0# CKE0
AB	MD43	DQM5 CKE5	MD42	MAA 11	MAB 11	MAA 12	MD39	MAB 10	VCCM	AGND DL1	MECC6 CKE6	VCCM	MAB 1	MAB 2	MAB 4	MAA 4	VCCM	MD22	MD16	VCCM	MAA 5	MAB 8	GND	MAA 13	GND	MD6
AC	MD41	GND	DQS5# CKE5	MAB 12	GND	SRAS A#	MD38	GND	MAB 0	NC	GND	MECC5 CKE5	GND	MAA 1	MAB 3	GND	MAA 3	MD28	MD17	MAA 6	MAB 5	DQM1 CKE1	MAB 7	MAA 9	MAB 13	MD7
AD	MD45	MD44	MD40	CS1#	CS5#	SWE B#	MAA 10	DQS4# CKE4	MD36	MD32	MECC2 CKE2	MECC0 CKE0	MAA 0	MD27	MAA 2	DQM3 CKE3	DQS3# CKE3	MD24	DQS2# CKE2	GND	GND	MD14	MD13	MAA 7	MAB 9	MD3
AE	CS3#	CS2#	SCAS A#	CS4#	GND	SRAS B#	DQM4 CKE4	GND	MD33	MECC3 CKE3	GND	MECC1 CKE1	GND	MD31	MD30	GND	MD29	MD23	DQM2 CKE2	MAB 6	MD11	MD10	GND	MD9	GND	VCCM
AF	VCCM	VCCM	CS0#	SCAS B#	SWE A#	MD35	VCCM	MD34	MD37	MECC7 CKE7	DQM8	DQS8#	VCCM	MECC4 CKE4	MD26	VCCM	MD25	MD19	MD21	VCCM	MD20	MD15	DQS1# CKE1	MD12	MD8	VCCM

Table 1. Pin List (Numerical Order)

Pin #		Pin Name	Pin #		Pin Name	Pin #		Pin Name	Pin #		Pin Name	Pin #		Pin Names	Pin #		Pin Name
A01	**P**	**VCCAGP**	D03	IO	GBE0#	G05	IO	GPAR	P01	I	VLCOMP	Y23	O	MAA14	AC25	O	MAB13
A02	**P**	**VCCAGP**	**D04**	**P**	**GND**	**G06**	**P**	**VCCAGP**	**P02**	**P**	**GND**	**Y24**	**P**	**GND**	AC26	IO	MD07
A03	IO	GD16	D05	IO	GD18	**G21**	**P**	**GND**	P03	I	PWROK	Y25	IO	MD05	AD01	IO	MD45
A04	IO	GD17	**D06**	**P**	**GND**	G22	IO	HD00	P04	I	RESET#	Y26	IO	MD04	AD02	IO	MD44
A05	**P**	**AGPVREF**	D07	IO	GDEVSEL#	G23	IO	HD06	**P05**	**P**	**GND**	AA01	IO	MD49	AD03	IO	MD40
A06	**P**	**VCCAGP**	D08	IO	GD25	G24	O	CPURST#	**P06**	**P**	**GND**	AA02	IO	MD48	AD04	O	CS1#
A07	IO	GD23	D09	O	ST0	G25	IO	HA26	**P21**	**P**	**GND**	AA03	IO	MD47	AD05	O	CS5#
A08	IO	GD24	D10	O	ST2	G26	IO	HA29	**P22**	**P**	**GND**	AA04	IO	MD46	AD06	O	SWEB#
A09	IO	GD28	D11	I	GPIPE#	H01	IO	GD1	P23	IO	HREQ0#	AA05	O	CS6#	AD07	O	MAA10
A10	**P**	**VCCAGP**	D12	I	SBA3	H02	IO	GD3	**P24**	**P**	**GND**	**AA06**	**P**	**GND**	AD08	IO	DQS4# / CKE4
A11	I	SBA7	D13	I	SBA2	H03	IO	GD0	P25	IO	HREQ2#	**AA07**	**P**	**VCCM**	AD09	IO	MD36
A12	I	SBS#	D14	I	GREQ#	H04	IO	GD2	P26	IO	BPRI#	**AA08**	**P**	**GND**	AD10	IO	MD32
A13	I	SBA0	D15	IO	HD61	**H05**	**P**	**VCCQQ**	R01	IO	MD58	**AA09**	**P**	**VCCM**	AD11	IO	MECC2 / CKE2
A14	**P**	**VCCAGP**	D16	IO	HD53	**H06**	**P**	**VCCAGP**	R02	IO	MD63	**AA10**	**P**	**AVCCDL1**	AD12	IO	MECC0 / CKE0
A15	IO	HD62	D17	IO	HD48	**H21**	**P**	**VTT**	R03	IO	MD59	**AA11**	**P**	**GND**	AD13	O	MAA00
A16	IO	HD54	D18	IO	HD41	H22	IO	HA27	**R04**	**P**	**VSUS25**	**AA12**	**P**	**VCCM**	AD14	IO	MD27
A17	IO	HD59	D19	IO	HD27	H23	IO	HA30	R05	I	SUST#	**AA13**	**P**	**GND**	AD15	O	MAA02
A18	IO	HD49	D20	IO	HD38	**H24**	**P**	**GND**	**R06**	**P**	**VCCM**	**AA14**	**P**	**VCCM**	AD16	O	DQM3 / CKE3
A19	IO	HD45	D21	IO	HD28	H25	IO	HA18	**R21**	**P**	**VTT**	**AA15**	**P**	**VCCM**	AD17	IO	DQS3# / CKE3
A20	IO	HD37	D22	IO	HD33	H26	IO	HA24	R22	IO	HA07	**AA16**	**P**	**GND**	AD18	IO	MD24
A21	IO	HD34	D23	IO	HD03	J01	**P**	**VCCAGP**	R23	IO	HREQ1#	**AA17**	**P**	**VCCM**	AD19	IO	DQS2# / CKE2
A22	IO	HD35	D24	IO	HD11	J02	I	GCOMP	R24	I	HLOCK#	AA18	IO	MD18	**AD20**	**P**	**GND**
A23	IO	HD25	D25	IO	HD14	**J03**	**P**	**GNDQQ**	R25	IO	DEFER#	**AA19**	**P**	**MVREF**	**AD21**	**P**	**GND**
A24	IO	HD24	D26	IO	HD02	J04	IO	VAD0 / strap	R26	IO	HREQ3#	**AA20**	**P**	**VCCM**	AD22	IO	MD14
A25	IO	HD16	**E01**	**P**	**VCCAGP**	**J05**	**P**	**GND**	**T01**	**P**	**VCCM**	**AA21**	**P**	**GND**	AD23	IO	MD13
A26	**P**	**VTT**	**E02**	**P**	**VCCAGP**	**J06**	**P**	**GND**	**T02**	**P**	**VCCM**	AA22	O	MAA08	AD24	O	MAA07
B01	IO	GD15	E03	IO	GDS0#	**J21**	**P**	**GND**	**T03**	**P**	**GND**	AA23	IO	MD02	AD25	O	MAB09
B02	IO	GBE1#	E04	IO	GD10	J22	IO	HA20	**T04**	**P**	**GND**	AA24	O	DQM0 / CKE0	AD26	IO	MD03
B03	IO	GBE2#	E05	IO	GSTOP#	J23	IO	HA23	T05	IO	MD62	AA25	IO	MD01	AE01	O	CS3#
B04	**P**	**GND**	E06	IO	GTRDY#	J24	IO	HA31	**T06**	**P**	**VCCM**	AA26	IO	DQS0# / CKE0	AE02	O	CS2#
B05	IO	GD21	E07	IO	GFRM#	J25	IO	HA22	**T21**	**P**	**GTLVREF**	AB01	IO	MD43	AE03	O	SCASA#
B06	**P**	**VCCAGP**	E08	IO	GDS1	J26	IO	HA17	**T22**	**P**	**GND**	AB02	O	DQM5 / CKE5	AE04	O	CS4#
B07	IO	GBE3#	E09	I	GWBF#	K01	I	UPSTB	T23	IO	RS1#	AB03	IO	MD42	**AE05**	**P**	**GND**
B08	IO	GD27	**E10**	**P**	**GND**	K02	I	UPSTB#	T24	I	HITM#	AB04	O	MAA11	AE06	O	SRASB#
B09	IO	GD30	E11	I	SBA6	K03	I	UPCMD	T25	IO	HIT#	AB05	O	MAB11	AE07	O	DQM4 / CKE4
B10	**P**	**VCCAGP**	**E12**	**P**	**VCCAGP**	K04	IO	VBE#	T26	IO	RS0#	AB06	O	MAA12	**AE08**	**P**	**GND**
B11	I	SBA4	E13	O	ST1	**K05**	**P**	**VLVREF**	U01	IO	MD57	AB07	IO	MD39	AE09	IO	MD33
B12	I	SBS	E14	O	CPURSTD#	K06	IO	VAD1 / strap	U02	O	DQM7 / CKE7	AB08	O	MAB10	AE10	IO	MECC3 / CKE3
B13	I	SBA1	**E15**	**P**	**VCC**	**K21**	**P**	**VCCGTL**	U03	IO	DQS7# / CKE7	**AB09**	**P**	**VCCM**	**AE11**	**P**	**GND**
B14	**P**	**VCCAGP**	E16	IO	HD55	K22	I	HCLK	U04	IO	MD61	**AB10**	**P**	**AGNDDL1**	AE12	IO	MECC1 / CKE1
B15	IO	HD50	E17	IO	HD63	K23	IO	HA25	U05	IO	MD56	AB11	IO	MECC6 / CKE6	**AE13**	**P**	**GND**
B16	IO	HD46	**E18**	**P**	**GND**	K24	IO	HA19	U06	IO	MD60	**AB12**	**P**	**VCCM**	AE14	IO	MD31
B17	IO	HD52	E19	IO	HD44	K25	IO	HA10	**U21**	**P**	**AVCCMCK**	AB13	O	MAB01	AE15	IO	MD30
B18	IO	HD51	E20	IO	HD43	K26	IO	HA21	**U22**	**P**	**AGNDMCK**	AB14	O	MAB02	**AE16**	**P**	**GND**
B19	IO	HD42	E21	IO	HD29	L01	O	DNCMD	U23	IO	HTRDY#	AB15	O	MAB04	AE17	IO	MD29
B20	IO	HD39	E22	IO	HD09	L02	O	DNSTB	U24	IO	DBSY#	AB16	O	MAA04	AE18	IO	MD23
B21	IO	HD22	E23	IO	HD18	L03	O	DNSTB#	U25	IO	RS2#	**AB17**	**P**	**VCCM**	AE19	O	DQM2 / CKE2
B22	IO	HD19	E24	IO	HD12	L04	IO	VPAR	U26	IO	DRDY#	AB18	IO	MD22	AE20	O	MAB06
B23	IO	HD26	E25	IO	HD10	L05	IO	VAD4	V01	IO	MD51	AB19	IO	MD16	AE21	IO	MD11
B24	IO	HD23	E26	IO	HD17	L06	IO	VAD2 / strap	V02	IO	MD55	**AB20**	**P**	**VCCM**	AE22	IO	MD10
B25	IO	HD30	F01	IO	GD7	**L21**	**P**	**AVCCHCK**	V03	IO	MD50	AB21	O	MAA05	**AE23**	**P**	**GND**
B26	IO	HD07	F02	IO	GD4	**L22**	**P**	**AGNDHCK**	V04	IO	MD54	AB22	O	MAB08	AE24	IO	MD09
C01	IO	GD11	F03	IO	GD6	L23	I	TESTIN#	V05	IO	MD53	**AB23**	**P**	**GND**	**AE25**	**P**	**GND**
C02	IO	GD12	F04	IO	GDS0	L24	IO	HA28	**V06**	**P**	**MVREF**	AB24	O	MAA13	**AE26**	**P**	**VCCM**
C03	IO	GD13	F05	IO	GD9	L25	IO	HA05	**V21**	**P**	**GND**	**AB25**	**P**	**GND**	**AF01**	**P**	**VCCM**
C04	IO	GD14	**F06**	**P**	**GND**	L26	IO	HA12	V22	I	MCLKF	AB26	IO	MD06	**AF02**	**P**	**VCCM**
C05	IO	GD19	**F07**	**P**	**GND**	**M01**	**P**	**VCCVL**	V23	O	MCLK	AC01	IO	MD41	AF03	O	CS0#
C06	IO	GD20	F08	IO	GDS1#	**M02**	**P**	**VCCVL**	**V24**	**P**	**GND**	**AC02**	**P**	**GND**	AF04	O	SCASB#
C07	IO	GD22	F09	IO	GD29	**M03**	**P**	**GND**	V25	O	BREQ0#	AC03	IO	DQS5# / CKE5	AF05	O	SWEA#
C08	IO	GD26	**F10**	**P**	**GND**	**M04**	**P**	**GND**	**V26**	**P**	**GND**	AC04	O	MAB12	AF06	IO	MD35
C09	IO	GD31	F11	IO	GIRDY#	**M05**	**P**	**VCCVL**	W01	IO	DQS6# / CKE6	**AC05**	**P**	**GND**	**AF07**	**P**	**VCCM**
C10	I	GRBF#	**F12**	**P**	**VCCAGP**	**M06**	**P**	**VCCVL**	W02	O	DQM6 / CKE6	AC06	O	SRASA#	AF08	IO	MD34
C11	I	SBA5	**F13**	**P**	**GND**	M21	IO	HA06	W03	IO	MD52	AC07	IO	MD38	AF09	IO	MD37
C12	**P**	**GND**	**F14**	**P**	**GND**	M22	IO	HA15	**W04**	**P**	**AGNDDL2**	**AC08**	**P**	**GND**	AF10	IO	MECC7 / CKE7
C13	O	GGNT#	**F15**	**P**	**VCC**	M23	IO	HA13	W05	P	**AVCCDL2**	AC09	O	MAB00	AF11	O	DQM8
C14	IO	HD56	**F16**	**P**	**GTLVREF**	M24	IO	HA16	**W06**	**P**	**GND**	AC10	-	NC	AF12	IO	DQS8#
C15	IO	HD60	F17	IO	HD40	M25	IO	HA03	**W21**	**P**	**VCCM**	**AC11**	**P**	**GND**	**AF13**	**P**	**VCCM**
C16	IO	HD58	**F18**	**P**	**GND**	M26	IO	HA09	**W22**	**P**	**VCCM**	AC12	IO	MECC5 / CKE5	AF14	IO	MECC4 / CKE4
C17	IO	HD57	**F19**	**P**	**VTT**	N01	I	VCCVK	W23	IO	MD00	**AC13**	**P**	**GND**	AF15	IO	MD26
C18	IO	HD47	**F20**	**P**	**GND**	N02	IO	VAD6	W24	IO	ADS#	AC14	O	MAA01	**AF16**	**P**	**VCCM**
C19	**P**	**GND**	**F21**	**P**	**GND**	N03	IO	VAD7	**W25**	**P**	**VCCM**	AC15	O	MAB03	AF17	IO	MD25
C20	IO	HD36	F22	IO	HD05	N04	IO	VAD5	**W26**	**P**	**VCCM**	**AC16**	**P**	**GND**	AF18	IO	MD19
C21	IO	HD31	F23	IO	HD08	N05	IO	VAD3 / strap	**Y01**	**P**	**VCCM**	AC17	O	MAA03	AF19	IO	MD21
C22	IO	HD32	F24	IO	HD01	**N06**	**P**	**VCCVL**	**Y02**	**P**	**VCCM**	AC18	IO	MD28	**AF20**	**P**	**VCCM**
C23	**P**	**GND**	F25	IO	HD04	N21	IO	HREQ4#	**Y03**	**P**	**GND**	AC19	IO	MD17	AF21	IO	MD20
C24	IO	HD21	F26	IO	HD15	N22	IO	HA08	**Y04**	**P**	**GND**	AC20	O	MAA06	AF22	IO	MD15
C25	IO	HD20	G01	IO	GD5	N23	IO	HA11	Y05	O	CS7#	AC21	O	MAB05	AF23	IO	DQS1# / CKE1
C26	IO	HD13	**G02**	**P**	**GND**	N24	IO	HA14	**Y06**	**P**	**VCCM**	AC22	O	DQM1 / CKE1	AF24	IO	MD12
D01	IO	GD8	G03	I	GCLK	N25	IO	BNR#	**Y21**	**P**	**GND**	AC23	O	MAB07	AF25	IO	MD08
D02	**P**	**GND**	**G04**	**P**	**GND**	N26	IO	HA04	Y22	O	MAB14	AC24	O	MAA09	**AF26**	**P**	**VCCM**

Center **VCC** Pins (19 pins): **G18,J11-12,14-17,L9,18,M9,18,R9,18,T9,18,V11-12,15-16** **VCCM** (9 pins): **P9,U9,18,V9-10,13-14,17-18** **VCCAGP** (4 pins): **J9-10,13,K9**
Center **GND** Pins (36 pins): **L11-16, M11-16, N11-16, P11-16, R11-16, T11-16** **VTT** (11 pins): **G15,19-20,J18,K18,20,N18,P18,20,R20,T20** **VCCVL** (1 pin): **N9**

Table 2. Pin List (Alphabetical Order)

Pin #		Pin Name	Pin #		Pin Name	Pin #		Pin Name	Pin #		Pin Name	Pin #		Pin Names	Pin #		Pin Name
W24	IO	ADS#	B08	IO	GD27	G05	IO	GPAR	D18	IO	HD41	AB19	IO	MD16	D10	O	ST2
AB10	**P**	**AGNDDL1**	A09	IO	GD28	D11	I	GPIPE#	B19	IO	HD42	AC19	IO	MD17	R05	I	SUST#
W04	**P**	**AGNDDL2**	F09	IO	GD29	C10	I	GRBF#	E20	IO	HD43	AA18	IO	MD18	AF05	O	SWEA#
L22	**P**	**AGNDHCK**	B09	IO	GD30	D14	I	GREQ#	E19	IO	HD44	AF18	IO	MD19	AD06	O	SWEB#
U22	**P**	**AGNDMCK**	C09	IO	GD31	E05	IO	GSTOP#	A19	IO	HD45	AF21	IO	MD20	L23	I	TESTIN#
A05	**P**	**AGPVREF**	F04	IO	GDS0	**F16**	**P**	**GTLVREF**	B16	IO	HD46	AF19	IO	MD21	K03	I	UPCMD
AA10	**P**	**AVCCDL1**	E03	IO	GDS0#	**T21**	**P**	**GTLVREF**	C18	IO	HD47	AB18	IO	MD22	K01	I	UPSTB
W05	**P**	**AVCCDL2**	E08	IO	GDS1	E06	IO	GTRDY#	D17	IO	HD48	AE18	IO	MD23	K02	I	UPSTB#
L21	**P**	**AVCCHCK**	F08	IO	GDS1#	E09	I	GWBF#	A18	IO	HD49	AD18	IO	MD24	J04	IO	VAD0 / strap
U21	**P**	**AVCCMCK**	D07	IO	GDEVSEL#	M25	IO	HA03	B15	IO	HD50	AF17	IO	MD25	K06	IO	VAD1 / strap
N25	IO	BNR#	E07	IO	GFRM#	N26	IO	HA04	B18	IO	HD51	AF15	IO	MD26	L06	IO	VAD2 / strap
P26	IO	BPRI#	C13	O	GGNT#	L25	IO	HA05	B17	IO	HD52	AD14	IO	MD27	N05	IO	VAD3 / strap
V25	O	BREQ0#	F11	IO	GIRDY#	M21	IO	HA06	D16	IO	HD53	AC18	IO	MD28	L05	IO	VAD4
G24	O	CPURST#	**B04**	**P**	**GND**	R22	IO	HA07	A16	IO	HD54	AE17	IO	MD29	N04	IO	VAD5
E14	O	CPURSTD#	**C12**	**P**	**GND**	N22	IO	HA08	E16	IO	HD55	AE15	IO	MD30	N02	IO	VAD6
AF03	O	CS0#	**C19**	**P**	**GND**	M26	IO	HA09	C14	IO	HD56	AE14	IO	MD31	N03	IO	VAD7
AD04	O	CS1#	**C23**	**P**	**GND**	K25	IO	HA10	C17	IO	HD57	AD10	IO	MD32	K04	IO	VBE#
AE02	O	CS2#	**D02**	**P**	**GND**	N23	IO	HA11	C16	IO	HD58	AE09	IO	MD33	**E15**	**P**	**VCC**
AE01	O	CS3#	**D04**	**P**	**GND**	L26	IO	HA12	A17	IO	HD59	AF08	IO	MD34	**F15**	**P**	**VCC**
AE04	O	CS4#	**D06**	**P**	**GND**	M23	IO	HA13	C15	IO	HD60	AF06	IO	MD35	**A01**	**P**	**VCCAGP**
AD05	O	CS5#	**E10**	**P**	**GND**	N24	IO	HA14	D15	IO	HD61	AD09	IO	MD36	**A02**	**P**	**VCCAGP**
AA05	O	CS6#	**E18**	**P**	**GND**	M22	IO	HA15	A15	IO	HD62	AF09	IO	MD37	**A06**	**P**	**VCCAGP**
Y05	O	CS7#	**F06**	**P**	**GND**	M24	IO	HA16	E17	IO	HD63	AC07	IO	MD38	**A10**	**P**	**VCCAGP**
U24	IO	DBSY#	**F07**	**P**	**GND**	J26	IO	HA17	T25	IO	HIT#	AB07	IO	MD39	**A14**	**P**	**VCCAGP**
R25	IO	DEFER#	**F10**	**P**	**GND**	H25	IO	HA18	T24	I	HITM#	AD03	IO	MD40	**B06**	**P**	**VCCAGP**
L01	O	DNCMD	**F13**	**P**	**GND**	K24	IO	HA19	R24	I	HLOCK#	AC01	IO	MD41	**B10**	**P**	**VCCAGP**
L02	O	DNSTB	**F14**	**P**	**GND**	J22	IO	HA20	P23	IO	HREQ0#	AB03	IO	MD42	**B14**	**P**	**VCCAGP**
L03	O	DNSTB#	**F18**	**P**	**GND**	K26	IO	HA21	R23	IO	HREQ1#	AB01	IO	MD43	**E01**	**P**	**VCCAGP**
AA24	O	DQM0 / CKE0	**F20**	**P**	**GND**	J25	IO	HA22	P25	IO	HREQ2#	AD02	IO	MD44	**E02**	**P**	**VCCAGP**
AC22	O	DQM1 / CKE1	**F21**	**P**	**GND**	J23	IO	HA23	R26	IO	HREQ3#	AD01	IO	MD45	**E12**	**P**	**VCCAGP**
AE19	O	DQM2 / CKE2	**G02**	**P**	**GND**	H26	IO	HA24	N21	IO	HREQ4#	AA04	IO	MD46	**F12**	**P**	**VCCAGP**
AD16	O	DQM3 / CKE3	**G04**	**P**	**GND**	K23	IO	HA25	U23	IO	HTRDY#	AA03	IO	MD47	**G06**	**P**	**VCCAGP**
AE07	O	DQM4 / CKE4	**G21**	**P**	**GND**	G25	IO	HA26	AD13	O	MAA00	AA02	IO	MD48	**H06**	**P**	**VCCAGP**
AB02	O	DQM5 / CKE5	**H24**	**P**	**GND**	H22	IO	HA27	AC14	O	MAA01	AA01	IO	MD49	**J01**	**P**	**VCCAGP**
W02	O	DQM6 / CKE6	**J05**	**P**	**GND**	L24	IO	HA28	AD15	O	MAA02	V03	IO	MD50	**R06**	**P**	**VCCM**
U02	O	DQM7 / CKE7	**J06**	**P**	**GND**	G26	IO	HA29	AC17	O	MAA03	V01	IO	MD51	**T01**	**P**	**VCCM**
AF11	O	DQM8	**J21**	**P**	**GND**	H23	IO	HA30	AB16	O	MAA04	W03	IO	MD52	**T02**	**P**	**VCCM**
AA26	IO	DQS0# / CKE0	**M03**	**P**	**GND**	J24	IO	HA31	AB21	O	MAA05	V05	IO	MD53	**T06**	**P**	**VCCM**
AF23	IO	DQS1# / CKE1	**M04**	**P**	**GND**	K22	I	HCLK	AC20	O	MAA06	V04	IO	MD54	**W21**	**P**	**VCCM**
AD19	IO	DQS2# / CKE2	**P02**	**P**	**GND**	G22	IO	HD00	AD24	O	MAA07	V02	IO	MD55	**W22**	**P**	**VCCM**
AD17	IO	DQS3# / CKE3	**P05**	**P**	**GND**	F24	IO	HD01	AA22	O	MAA08	U05	IO	MD56	**W25**	**P**	**VCCM**
AD08	IO	DQS4# / CKE4	**P06**	**P**	**GND**	D26	IO	HD02	AC24	O	MAA09	U01	IO	MD57	**W26**	**P**	**VCCM**
AC03	IO	DQS5# / CKE5	**P21**	**P**	**GND**	D23	IO	HD03	AD07	O	MAA10	R01	IO	MD58	**Y01**	**P**	**VCCM**
W01	IO	DQS6# / CKE6	**P22**	**P**	**GND**	F25	IO	HD04	AB04	O	MAA11	R03	IO	MD59	**Y02**	**P**	**VCCM**
U03	IO	DQS7# / CKE7	**P24**	**P**	**GND**	F22	IO	HD05	AB06	O	MAA12	U06	IO	MD60	**Y06**	**P**	**VCCM**
AF12	IO	DQS8#	**T03**	**P**	**GND**	G23	IO	HD06	AB24	O	MAA13	U04	IO	MD61	**AA07**	**P**	**VCCM**
U26	IO	DRDY#	**T04**	**P**	**GND**	B26	IO	HD07	Y23	O	MAA14	T05	IO	MD62	**AA09**	**P**	**VCCM**
D03	IO	GBE0#	**T22**	**P**	**GND**	F23	IO	HD08	AC09	O	MAB00	R02	IO	MD63	**AA12**	**P**	**VCCM**
B02	IO	GBE1#	**V21**	**P**	**GND**	E22	IO	HD09	AB13	O	MAB01	AD12	IO	MECC0 / CKE0	**AA14**	**P**	**VCCM**
B03	IO	GBE2#	**V24**	**P**	**GND**	E25	IO	HD10	AB14	O	MAB02	AE12	IO	MECC1 / CKE1	**AA15**	**P**	**VCCM**
B07	IO	GBE3#	**V26**	**P**	**GND**	D24	IO	HD11	AC15	O	MAB03	AD11	IO	MECC2 / CKE2	**AA17**	**P**	**VCCM**
G03	I	GCLK	**W06**	**P**	**GND**	E24	IO	HD12	AB15	O	MAB04	AE10	IO	MECC3 / CKE3	**AA20**	**P**	**VCCM**
J02	I	GCOMP	**Y03**	**P**	**GND**	C26	IO	HD13	AC21	O	MAB05	AF14	IO	MECC4 / CKE4	**AB09**	**P**	**VCCM**
H03	IO	GD0	**Y04**	**P**	**GND**	D25	IO	HD14	AE20	O	MAB06	AC12	IO	MECC5 / CKE5	**AB12**	**P**	**VCCM**
H01	IO	GD1	**Y21**	**P**	**GND**	F26	IO	HD15	AC23	O	MAB07	AB11	IO	MECC6 / CKE6	**AB17**	**P**	**VCCM**
H04	IO	GD2	**Y24**	**P**	**GND**	A25	IO	HD16	AB22	O	MAB08	AF10	IO	MECC7 / CKE7	**AB20**	**P**	**VCCM**
H02	IO	GD3	**AA06**	**P**	**GND**	E26	IO	HD17	AD25	O	MAB09	**V06**	**P**	**MVREF**	**AE26**	**P**	**VCCM**
F02	IO	GD4	**AA08**	**P**	**GND**	E23	IO	HD18	AB08	O	MAB10	**AA19**	**P**	**MVREF**	**AF01**	**P**	**VCCM**
G01	IO	GD5	**AA11**	**P**	**GND**	B22	IO	HD19	AB05	O	MAB11	AC10	-	NC	**AF02**	**P**	**VCCM**
F03	IO	GD6	**AA13**	**P**	**GND**	C25	IO	HD20	AC04	O	MAB12	P03	I	PWROK	**AF07**	**P**	**VCCM**
F01	IO	GD7	**AA16**	**P**	**GND**	C24	IO	HD21	AC25	O	MAB13	P04	I	RESET#	**AF13**	**P**	**VCCM**
D01	IO	GD8	**AA21**	**P**	**GND**	B21	IO	HD22	Y22	O	MAB14	T26	IO	RS0#	**AF16**	**P**	**VCCM**
F05	IO	GD9	**AB23**	**P**	**GND**	B24	IO	HD23	V22	I	MCLKF	T23	IO	RS1#	**AF20**	**P**	**VCCM**
E04	IO	GD10	**AB25**	**P**	**GND**	A24	IO	HD24	V23	O	MCLK	U25	IO	RS2#	**AF26**	**P**	**VCCM**
C01	IO	GD11	**AC02**	**P**	**GND**	A23	IO	HD25	W23	IO	MD00	A13	I	SBA0	**H05**	**P**	**VCCQQ**
C02	IO	GD12	**AC05**	**P**	**GND**	B23	IO	HD26	AA25	IO	MD01	B13	I	SBA1	**N01**	**P**	**VCCVK**
C03	IO	GD13	**AC08**	**P**	**GND**	D19	IO	HD27	AA23	IO	MD02	D13	I	SBA2	**M01**	**P**	**VCCVL**
C04	IO	GD14	**AC11**	**P**	**GND**	D21	IO	HD28	AD26	IO	MD03	D12	I	SBA3	**M02**	**P**	**VCCVL**
B01	IO	GD15	**AC13**	**P**	**GND**	E21	IO	HD29	Y26	IO	MD04	B11	I	SBA4	**M05**	**P**	**VCCVL**
A03	IO	GD16	**AC16**	**P**	**GND**	B25	IO	HD30	Y25	IO	MD05	C11	I	SBA5	**M06**	**P**	**VCCVL**
A04	IO	GD17	**AD20**	**P**	**GND**	C21	IO	HD31	AB26	IO	MD06	E11	I	SBA6	**N06**	**P**	**VCCVL**
D05	IO	GD18	**AD21**	**P**	**GND**	C22	IO	HD32	AC26	IO	MD07	A11	I	SBA7	P01	I	VLCOMP
C05	IO	GD19	**AE05**	**P**	**GND**	D22	IO	HD33	AF25	IO	MD08	B12	I	SBS	**K05**	**P**	**VLVREF**
C06	IO	GD20	**AE08**	**P**	**GND**	A21	IO	HD34	AE24	IO	MD09	A12	I	SBS#	L04	IO	VPAR
B05	IO	GD21	**AE11**	**P**	**GND**	A22	IO	HD35	AE22	IO	MD10	AE03	O	SCASA#	**R04**	**P**	**VSUS25**
C07	IO	GD22	**AE13**	**P**	**GND**	C20	IO	HD36	AE21	IO	MD11	AF04	O	SCASB#	**A26**	**P**	**VTT**
A07	IO	GD23	**AE16**	**P**	**GND**	A20	IO	HD37	AF24	IO	MD12	AC06	O	SRASA#	**F19**	**P**	**VTT**
A08	IO	GD24	**AE23**	**P**	**GND**	D20	IO	HD38	AD23	IO	MD13	AE06	O	SRASB#	**H21**	**P**	**VTT**
D08	IO	GD25	**AE25**	**P**	**GND**	B20	IO	HD39	AD22	IO	MD14	D09	O	ST0	**K21**	**P**	**VTT**
C08	IO	GD26	**J03**	**P**	**GNDQQ**	F17	IO	HD40	AF22	IO	MD15	E13	O	ST1	**R21**	**P**	**VTT**

Center **VCC** Pins (19 pins): **G18,J11-12,14-17,L9,18,M9,18,R9,18,T9,18,V11-12,15-16** **VCCM** (9 pins): **P9,U9,18,V9-10,13-14,17-18** **VCCAGP** (4 pins): **J9-10,13,K9**
Center **GND** Pins (36 pins): **L11-16, M11-16, N11-16, P11-16, R11-16, T11-16** **VTT** (11 pins): **G15,19-20,J18,K18,20,N18,P18,20,R20,T20** **VCCVL** (1 pin): **N9**

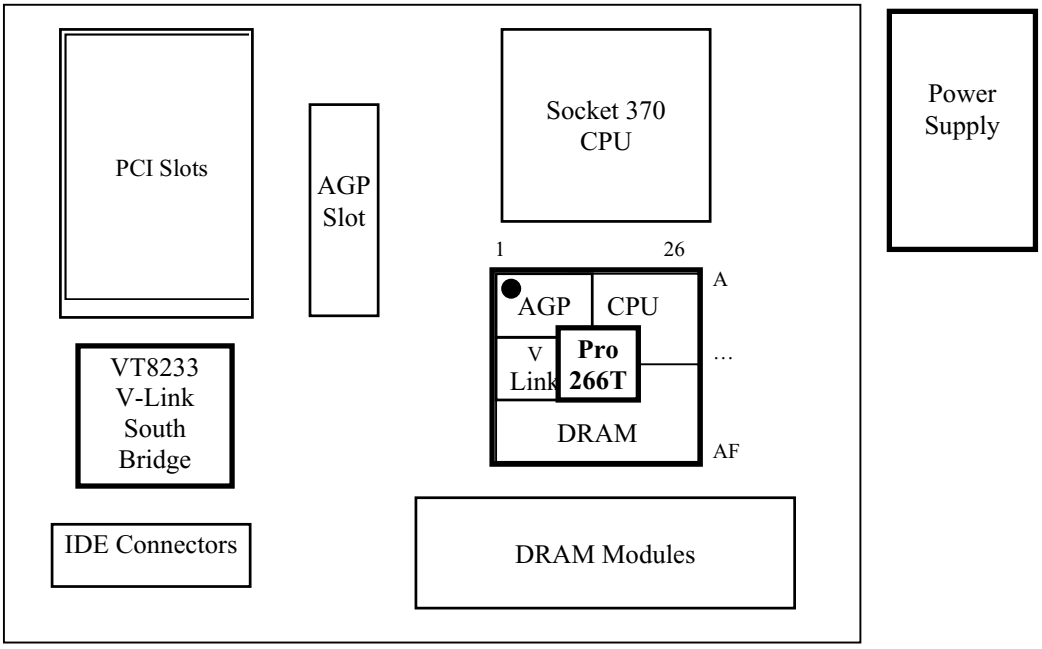
Pin Descriptions

Table 3. Pin Descriptions

CPU Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
HA[31:3]#	(See Pin List)	IO	**Host Address Bus.** HA[31:3] connect to the address bus of the host CPU. During CPU cycles HA[31:3] are inputs. These signals are driven by the Pro266T during cache snooping operations.
HD[63:0]#	(See Pin List)	IO	**Host CPU Data.** These signals are connected to the CPU data bus.
ADS#	W24	IO	**Address Strobe**. The CPU asserts ADS# in T1 of the CPU bus cycle.
BNR#	N25	IO	**Block Next Request**. Used to block the current request bus owner from issuing new requests. This signal is used to dynamically control the processor bus pipeline depth.
BPRI#	P26	IO	**Priority Agent Bus Request**. The owner of this signal will always be the next bus owner. This signal has priority over symmetric bus requests and causes the current symmetric owner to stop issuing new transactions unless the HLOCK# signal is asserted. The Pro266T drives this signal to gain control of the processor bus.
DBSY#	U24	IO	**Data Bus Busy**. Used by the data bus owner to hold the data bus for transfers requiring more than one cycle.
DEFER#	R25	IO	**Defer**. The Pro266T uses a dynamic deferring policy to optimize system performance. The Pro266T also uses the DEFER# signal to indicate a processor retry response.
DRDY#	U26	IO	**Data Ready**. Asserted for each cycle that data is transferred.
HIT#	T25	IO	**Hit**. Indicates that a cacheing agent holds an unmodified version of the requested line. Also driven in conjunction with HITM# by the target to extend the snoop window.
HITM#	T24	I	**Hit Modified**. Asserted by the CPU to indicate that the address presented with the last snoop cycle is modified in the L1 cache and needs to be written back.
HLOCK#	R24	I	**Host Lock**. All CPU cycles sampled with the assertion of HLOCK# and ADS# until the negation of HLOCK# must be atomic.
HREQ[4:0]#	N21, R26, P25, R23, P23	IO	**Request Command**. Asserted during both clocks of the request phase. In the first clock, the signals define the transaction type to a level of detail that is sufficient to begin a snoop request. In the second clock, the signals carry additional information to define the complete transaction type.
HTRDY#	U23	IO	**Host Target Ready**. Indicates that the target of the processor transaction is able to enter the data transfer phase.
RS[2:0]#	U25, T23, T26	IO	**Response Signals**. Indicates the type of response per the table below: **RS[2:0]#** — **Response type** 000 — Idle State 001 — Retry Response 010 — Defer Response 011 — Reserved 100 — Hard Failure 101 — Normal Without Data 110 — Implicit Writeback 111 — Normal With Data
CPURST#	G24	O	**CPU Reset.** Reset output to CPU
BREQ0#	V25	O	**Bus Request 0.** Bus request output to CPU.

Note: Clocking of the CPU interface is performed with HCLK. See the clock pin group at the end of the pin descriptions section for descriptions of the clock pins.

The Pro266T pinouts were defined assuming the ATX PCB layout model shown below (and general pin layout shown) as a guide for PCB component placement. Other PCB layouts (AT, LPX, and NLX) were also considered and can typically follow the same general component placement.



Apollo Pro266Tis an upgrade of Apollo Pro266 but the ballouts are slightly different. The Pro266T has 8 more balls than the Pro266. Seven of the eight new balls are VTT power signals for enhancing the Pentium III-M (Tualatin) CPU termination power supply to the Pro266T. The other ball is used as a VCC power signal. 9 of 13 VCCGTL power signals in the Pro266 used as AGTL+ IO power from a 2.5V power source are replaced by VTT power signals in Pro266T for AGTL(+) IO power. The remaining VCCGTL power signals are replaced by VCC power signals in Pro266T for its own core power. Except for VTT, VCC and VCCGTL power signals and two signals at J1 and AC10, ball assignment for all the remaining signals between both chips is exactly the same. Refer to the table below for more detail on ballout differences between the Pro266T and Pro266 chips. Also refer to the Pro266T Design Guide for details on designing motherboards to accommodate either chip.

Table 4. Ballout Differences Between Pro266T and Pro266

Signal Group	Pro266T	Pro266	Ballout assignment
Power	VTT	VCCGTL	A26, F19, H21, J18, K18, K21, N18, P18, R21
	VTT	-	G15, G19, G20, K20, P20, R20, T20
	VCC	VCCGTL	E15, F15, J14, J17
	VCC	-	G18
Signal	VCCAGP	GCOMPP	J1
	NC	DQSFB	AC10

DRAM Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
MD[63:0]	(See Pin List)	IO	**Memory Data.** These signals are connected to the DRAM data bus.
MECC[7:0] / CKE[7:0]	AF10, AB11, AC12, AF14, AE10, AD11, AE12, AD12	IO	**DRAM ECC or EC Data:** when ECC is enabled. **Clock Enables:** For each DRAM bank for powering down the SDRAMs in notebook applications. Also used in desktop systems for clock control to reduce power usage and for reducing heat/temperature in high-speed memory systems.
MAA[14:0]	Y23, AB24, AB6, AB4, AD7, AC24, AA22, AD24, AC20, AB21, AB16, AC17, AD15, AC14, AD13	O	**Memory Address A.** DRAM address lines (two sets for better drive)
MAB[14:0]	Y22, AC25, AC4, AB5, AB8, AD25, AB22, AC23, AE20, AC21, AB15, AC15, AB14, AB13, AC9	O	**Memory Address B.** DRAM address lines (two sets for better drive).
CS[7:0]#	Y5, AA5, AD5, AE4, AE1, AE2, AD4, AF3	O	**Memory Chip Select.** Chip select of each bank.
DQM8, **DQM7** / CKE7, **DQM6** / CKE6, **DQM5** / CKE5, **DQM4** / CKE4, **DQM3** / CKE3, **DQM2** / CKE2, **DQM1** / CKE1, **DQM0** / CKE0	AF11, U2, W2, AB2, AE7, AD16, AE19, AC22, AA24	O	**Memory Data Mask.** Data mask of each data byte lane (DQM[0-7] and ECC byte (DQM8).
SRASA#, SRASB#	AC6, AE6	O	**Row Address Command Indicator.** (2 pins for better drive)
SCASA#, **SCASB#**	AE3, AF4	O	**Column Address Command Indicator.** (2 pins for better drive)
SWEA#, **SWEB#**	AF5, AD6	O	**Write Enable Command Indicator.** (2 pins for better drive)
DQS[8]#, **DQS[7:0]**# / CKE[7:0]	AF12, U3, W1, AC3, AD8, AD17, AD19, AF23, AA26	IO	**DDR Data Strobe.** DQS[8]# for ECC bit.

V-Link Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
VAD7, **VAD6,** **VAD5,** **VAD4,** **VAD3** / strap, **VAD2** / strap, **VAD1** / strap, **VAD0** / strap	N3, N2, N4, L5, N5, L6, K6, J4	IO	**V-Link Address/Data Bus.**
VPAR	L4	IO	**Parity.**
VBE#	K4	IO	**Byte Enable.**
UPCMD	K3	I	**Command from Client-to-Host.**
UPSTB	K1	I	**Strobe from Client-to-Host.**
UPSTB#	K2	I	**Complement strobe from Client-to-Host.**
DNCMD	L1	O	**Command from Host-to-Client.**
DNSTB	L2	O	**Strobe from Host-to-Client.**
DNSTB#	L3	O	**Complement strobe from Host-to-Client.**

AGP Bus Interface

Signal Name	Pin #	I/O	Signal Description
GD[31:0]	(See Pin List)	IO	**Address/Data Bus.** The standard AGP/PCI address and data lines. The address is driven with GDS0# and GDS1# assertion for AGP transfers and is driven with GFRM# assertion for PCI transfers.
GBE[3:0]#	B7, B3, B2, D3	IO	**Command/Byte Enable.** **AGP:** These pins provide command information (different commands than for PCI) driven by the master (graphics controller) when requests are being enqueued using PIPE#. These pins provide valid byte information during AGP write transactions and are driven by the master. The target (this chip) drives these lines to "0000" during the return of AGP read data, but the state of these pins is ignored by the AGP master. **PCI:** Commands are driven with GFRM# assertion. Byte enables corresponding to supplied or requested data are driven on following clocks.
GPAR	G5	IO	**AGP Parity.** A single parity bit is provided over GD[31:0] and GBE[3:0].
GDS0	F4	IO	**Bus Strobe 0 (AGP transactions only).** Provides timing for 2x data transfer mode on AD[15:0]. The agent that is providing the data drives this signal.
GDS0#	E3	IO	**Bus Strobe 0 compliment and Bus Strobe 0 (AGP transactions only).** Provides timing for 4x data transfer mode on AD[15:0]. The agent that is providing the data drives this signal.
GDS1	E8	IO	**Bus Strobe 1 (AGP transactions only).** Provides timing for 2x data transfer mode on AD[31:16]. The agent that is providing the data drives this signal.
GDS1#	F8	IO	**Bus Strobe 1 compliment and Bus Strobe 1 (AGP transactions only).** Provides timing for 4x data transfer mode on AD[31:16]. The agent that is providing the data drives this signal.
GFRM#	E7	IO	**Frame (PCI transactions only).** Assertion indicates the address phase of a PCI transfer. Negation indicates that one more data transfer is desired by the cycle initiator.
GIRDY#	F11	IO	**Initiator Ready** **AGP:** For write operations, the assertion of this pin indicates that the master is ready to provide *all* write data for the current transaction. Once this pin is asserted, the master is not allowed to insert wait states. For read operations, the assertion of this pin indicates that the master is ready to transfer a subsequent block of read data. The master is *never* allowed to insert a wait state during the initial block of a read transaction. However, it may insert wait states after each block transfers. **PCI:** Asserted when the initiator is ready for data transfer.
GTRDY#	E6	IO	**Target Ready:** **AGP:** Indicates that the target is ready to provide read data for the entire transaction (when the transaction can complete within four clocks) or is ready to transfer a (initial or subsequent) block of data when the transfer requires more than four clocks to complete. The target is allowed to insert wait states after each block transfers on both read and write transactions. **PCI:** Asserted when the target is ready for data transfer.
GSTOP#	E5	IO	**Stop (PCI transactions only).** Asserted by the target to request the master to stop the current transaction.
GDEVSEL#	D7	IO	**Device Select (PCI transactions only).** This signal is driven by the Pro266T when a PCI initiator is attempting to access main memory. It is an input when the Pro266T is acting as PCI initiator. Not used for AGP cycles.
GPIPE#	D11	I	**Pipelined Request.** Asserted by the master (graphics controller) to indicate that a full-width request is to be enqueued by the target Pro266T. The master enqueues one request each rising edge of GCLK while GPIPE# is asserted. When GPIPE# is deasserted no new requests are enqueued across the AD bus.
GRBF#	C10	I	**Read Buffer Full.** Indicates if the master (graphics controller) is ready to accept previously requested low priority read data. When GRBF# is asserted, the Pro266T will not return low priority read data to the master.
GWBF#	E9	I	**Write Buffer Full.**

AGP Bus Interface (continued)			
Signal Name	**Pin #**	**I/O**	**Signal Description**
SBA[7:0]	A11, E11, C11, B11, D12, D13, B13, A13	I	**SideBand Address.** Provides an additional bus to pass address and command information from the master (graphics controller) to the target (the Pro266T, these pins are ignored until enabled.
SBS	B12	I	**Sideband Strobe.** Provides timing for SBA[7:0] (driven by the master)
SBS#	A12	I	**Sideband Strobe compliment and SBS .** Provides timing for SBA[7:0] (driven by the master) when 4x timing is supported.
ST[2:0]	D10, E13, D9	O	**Status (AGP only).** Provides information from the arbiter to a master to indicate what it may do. Only valid while GGNT# is asserted. 000 Indicates that previously requested low priority read or flush data is being returned to the master (graphics controller). 001 Indicates that previously requested high priority read data is being returned to the master. 010 Indicates that the master is to provide low priority write data for a previously enqueued write command. 011 Indicates that the master is to provide high priority write data for a previously enqueued write command. 100 Reserved. (arbiter must not issue, may be defined in the future). 101 Reserved. (arbiter must not issue, may be defined in the future). 110 Reserved. (arbiter must not issue, may be defined in the future). 111 Indicates that the master (graphics controller) has been given permission to start a bus transaction. The master may enqueue AGP requests by asserting PIPE# or start a PCI transaction by asserting GFRM#. ST[2:0] are always outputs from the Pro266T and inputs to the master.
GREQ#	D14	I	**Request.** Master request for AGP.
GGNT#	C13	O	**Grant.** Permission is given to the master to use AGP.

Note: For PCI operation on the AGP bus, the following pins are not required:
- PERR# (parity and error reporting not required on transient data devices such as graphics controllers)
- LOCK# (no lock requirement on AGP)
- IDSEL (internally connected to AD16 on AGP-compliant masters)

Note: Separate system interrupts are not provided for AGP. The AGP connector provides interrupts via PCI bus INTA-B#.

Note: The AGP bus supports only one master directly (REQ[3:0]# and GNT[3:0]# are not provided). External logic is required to implement additional master capability. Note that the arbitration mechanism on the AGP bus is different from the PCI bus.

Note: A separate reset is not required for the AGP bus (RESET# resets both PCI and AGP buses)

Note: Two mechanisms are provided by the AGP bus to enqueue master requests: GPIPE# (to send addresses multiplexed on the AD lines) and the SBA port (to send addresses unmultiplexed). AGP masters implement one or the other or select one at initialization time (they are not allowed to change during runtime). Therefore only one of the two will be used and the signals associated with the other will not be used. Therefore the Pro266T has an internal pullup on GRBF# to maintain it in the de-asserted state in case it is not implemented on the master device.

Clock / Reset Control			
Signal Name	**Pin #**	**I/O**	**Signal Description**
HCLK	K22	I	**Host Clock.** This pin receives the host CPU clock (66 / 100 / 133 MHz). This clock is used by all Pro266T logic that is in the host CPU domain.
GCLK	G3	I	**AGP Clock.** This pin receives the AGP bus clock (66 MHz). This clock is used by all Pro266T logic that is in the AGP clock domain. The AGP clock must be synchronous / pseudo-synchronous to the host CPU clock (selectable as shown in the table above).
MCLK	V23	O	**DRAM Clock.** Output from internal clock generator to the external clock buffer.
MCLKF	V22	I	**DRAM Clock Feedback Input.**
RESET#	P4	I	**Reset.** Input from south bridge chip. When asserted, this signal resets the Pro266T and sets all register bits to the default value. The same signal that connects to this pin may also be used (connected through an external inverter) to reset the ISA bus (if implemented). The rising edge of this signal is used to sample all power-up strap options.
PWROK	P3	I	**Power OK.**
CPURST#	G24	O	**CPU Reset.** CPU Reset output to the CPU.
CPURSTD#	E14	O	**CPU Reset Delayed.** CPU Reset output to the CPU, 2T delayed from CPURST#.
SUST#	R5	I	**Suspend Status.** For implementation of the Suspend-to-DRAM feature. Connect to an external pullup to disable.

Power, Ground, Analog, and Test			
Signal Name	**Pin #**	**I/O**	**Signal Description**
VCC	(See Pin List)	P	**Core Power.** 2.5V ± 5%.
GND	(See Pin List)	P	**Ground**
VTT	A26, F19, G15, G19-20, H21, J18, K18, K20-K21, N18, P18, P20, R20-R21, T20	P	**CPU Interface Termination Power.** 1.2V ± 5% for Pentium III-M (Tualatin) CPUs, 1.5V ± 5% for all other Pentium / Celeron / VIA-C3 CPUs (see CPU specs for specific voltage)
VCCVL	M1-M2, M5-M6, N6, N9	P	**V-Link Power.** 2.5V ± 5%.
VCCM	P9, R6, T1-T2, T6, U9, U18, V9-V10, V13-V14, V17-V18, W21-W22, W25-W26, Y1-Y2, Y6, AA7, AA9, AA12, AA14, AA15, AA17, AA20, AB9, AB12, AB17, AB20, AE26, AF1, AF2, AF7, AF13, AF16, AF20, AF26	P	**DRAM Power.** Connect to 2.5V ± 5% power source for DDR SDRAM or to 3.3V ± 5% for SDR SDRAM (see Design Guide for details).
VCCAGP	A1-A2, A6, A10, A14, B6, B10, B14, E1-E2, E12, F12, G6, H6, J1, J9-J10, J13, K9	P	**AGP Power.** 1.5V (AGP 4x) / 3.3V (AGP 2x and 1x) ± 5%.
VCCQQ	H5	P	**AGP Quiet Power.** 1.5V (AGP 4x) / 3.3V (AGP 2x and 1x) ± 5%.
GNDQQ	J3	P	**AGP Quiet Ground.**
VSUS25	R4	P	**Suspend Power.** 2.5V ±5%.
AVCCHCK	L21	P	**PLL Power.** Clock generator/deskew. 2.5V ±5%.
AGNDHCK	L22	P	**PLL Analog Ground.** Clock generator/deskew ground. Connect to main ground plane through ferrite bead.
AVCCMCK	U21	P	**DRAM Deskew Power.** 2.5V ±5%.
AGNDMCK	U22	P	**DRAM Deskew Analog Ground.** Connect to main ground plane through ferrite bead.
AVCCDL1	AA10	P	**DLL1 Power.** 2.5V ±5%.
AGNDDL1	AB10	P	**DLL1 Analog ground**
AVCCDL2	W5	P	**DLL2 Power.** 2.5V ±5%.
AGNDDL2	W4	P	**DLL2 Analog ground**
MVREF	V6, AA19	P	**DDR SDRAM Memory Voltage Reference.** 1.25V
GTLVREF	F16, T21	P	**CPU Interface GTL+ Voltage Reference.** 2/3 VTT ±2%
AGPVREF	A5	P	**AGP Voltage Reference.** ½ VCCQQ.
VLVREF	K5	P	**V-Link Voltage Reference.** 0.9V.
VCCVK	N1	I	**V-Link Compensation Circuit Power.** 2.5V ±5%.
VLCOMP	P1	I	**P Channel Compensation for V-Link**
GCOMP	J2	I	**P Channel Compensation for AGP**
TESTIN#	L23	I	**Test Input.** NAND tree / tristate mode test select.

REGISTERS

Register Overview

The following tables summarize the configuration and I/O registers of the Pro266T. These tables also document the power-on default value ("Default") and access type ("Acc") for each register. Access type definitions used are RW (Read/Write), RO (Read/Only), "—" for reserved / used (essentially the same as RO), and RWC (or just WC) (Read / Write 1's to Clear individual bits). Registers indicated as RW may have some read/only bits that always read back a fixed value (usually 0 if unused); registers designated as RWC or WC may have some read-only or read write bits (see individual register descriptions following these tables for details). All offset and default values are shown in hexadecimal unless otherwise indicated.

Table 5. Registers

I/O Ports

Port #	I/O Port	Default	Acc
22	PCI / AGP Arbiter Disable	00	RW
CFB-8	Configuration Address	0000 0000	RW
CFF-C	Configuration Data	0000 0000	RW

Pro266T Device 0 Registers - Host Bridge

Header Registers

Offset	Configuration Space Header	Default	Acc
1-0	Vendor ID	**1106**	RO
3-2	Device ID	**3101**	RO
5-4	Command	**0006**	**RW**
7-6	Status	**0210**	**WC**
8	Revision ID	**0n**	RO
9	Program Interface	00	RO
A	Sub Class Code	00	RO
B	Base Class Code	**06**	RO
C	Reserved	00	—
D	Latency Timer	00	**RW**
E	Header Type	00	RO
F	Built In Self Test (BIST)	00	RO
13-10	Graphics Aperture Base	**0000 0008**	**RW**
14-2B	Reserved	00	—
2D-2C	Subsystem Vendor ID	0000	**RW**
2F-2E	Subsystem ID	0000	**RW**
33-30	Reserved	00	—
37-34	Capability Pointer	**0000 00A0**	RO
3F-38	Reserved	00	—

Device-Specific Registers

Offset	V-Link Control	Default	Acc
40	V-Link Revision ID	00	RW
41	V-Link NB Capability	**18**	RW
42	V-Link NB Downlink Command	**88**	RW
44-43	V-Link NB Uplink Status	**8280**	RW
45	V-Link NB Bus Timer	**44**	RW
46	V-Link Misc NB Control	00	RW
47	V-Link Control	00	RW
48	V-Link NB/SB Configuration	**18**	RW
49	V-Link SB Capability	**18**	RW
4A	V-Link SB Downlink Status	**88**	**RO**
4C-4B	V-Link SB Uplink Command	**8280**	**RO**
4D	V-Link SB Bus Timer	**44**	RW
4E	CCA Master High Priority	00	RW
4F	V-Link SB Miscellaneous Control	00	RW

Offset	Host CPU Protocol Control	Default	Acc
50	CPU Interface Request Phase Control	00	RW
51	CPU Interface Basic Control	00	RW
52	CPU Interface Advanced Control	00	RW
53	CPU Interface Arbitration Control	**03**	RW
54	Miscellaneous	00	RW

Device-Specific Registers (continued)

Offset	DRAM Control	Default	Acc
55	DRAM Control	00	RW
56-57	(see below)		
59-58	MA Map Type	**2222**	RW
5F-5A	DRAM Row Ending Address:		
5A	Bank 0 Ending (HA[31:24])	**01**	RW
5B	Bank 1 Ending (HA[31:24])	**01**	RW
5C	Bank 2 Ending (HA[31:24])	**01**	RW
5D	Bank 3 Ending (HA[31:24])	**01**	RW
5E	Bank 4 Ending (HA[31:24])	**01**	RW
5F	Bank 5 Ending (HA[31:24])	**01**	RW
56	Bank 6 Ending (HA[31:24])	**01**	RW
57	Bank 7 Ending (HA[31:24])	**01**	RW
60	DRAM Type	00	RW
61	ROM Shadow Control C0000-CFFFF	00	RW
62	ROM Shadow Control D0000-DFFFF	00	RW
63	ROM Shadow Control E0000-FFFFF	00	RW
64	DRAM Timing for All Banks	**E4**	RW
65	DRAM Arbitration Timer	00	RW
66	DRAM Arbitration Control	00	RW
67	DRAM DQS/SDR/MD Read Delay	00	RW
68	DRAM DDR Control	00	RW
69	Extended SMRAM Control	00	RW
6A	DRAM Refresh Counter	00	RW
6B	DRAM Arbitration Control	**10**	RW
6C	SDRAM Control	00	RW
6D	DRAM Control Drive Strength	00	RW
6E	ECC Control	00	RW
6F	ECC Status	00	**RO**

Offset	PCI Bus Control	Default	Acc
70	PCI Buffer Control	00	RW
71	CPU to PCI Flow Control	**48**	RW
72	-reserved-	00	—
73	PCI Master Control	00	RW
74	-reserved-	00	—
75	PCI Arbitration 1	00	RW
76	PCI Arbitration 2	00	RW
77-7F	-reserved-	00	—

Offset	GART/TLB Control	Default	Acc
83-80	GART/TLB Control	0000 0000	RW
84	Graphics Aperture Size	00	RW
85-87	-reserved-	00	—
8B-88	Gr. Aperture TLB Base Register Base	0000 0000	RW
8C-9F	-reserved-	00	—

Device 0 Device-Specific Registers (continued)

Offset	AGP Control	Default	Acc
A0	AGP ID	**02**	**RO**
A1	AGP Next Item Pointer	**C0**	**RO**
A2	AGP Specification Revision	**20**	**RO**
A3	-reserved-	00	—
A7-A4	AGP Status	**1F00 0201**	**RO**
AB-A8	AGP Command	0000 0000	RW
AC	AGP Control	00	RW
AD	AGP Latency Timer	**02**	RW
AE	AGP Miscellaneous Control	00	RW
AF	-reserved-	00	—
B0	AGP Compensation Control / Status	**xx**	RW
B1	AGP Compensation Drive Strength	**63**	RW
B2	AGP Drive / Delay Control	**08**	RW
B3	AGP Strobe Drive Strength		RW

Offset	V-Link Control	Default	Acc
B4	V-Link NB Compensation Control	00	RW
B5	V-Link NB Drive Control	00	RW
B6-B7	-reserved-	00	—
B8	V-Link SB Compensation Control	00	RW
B9	V-Link SB Drive Control	00	RW
BA-BD	-reserved-	00	—

Offset	DRAM Interface Control	Default	Acc
BE	MECC Drive Strength	00	RW
BF	MA / SCMD Pad Toggle Reduction	00	RW

Offset	Extended Power Management	Default	Acc
C0	Capability ID	**01**	**RO**
C1	Next Pointer	00	**RO**
C2	Power Management Capabilities 1	**02**	**RO**
C3	Power Management Capabilities 2	00	**RO**
C4	Power Management Control / Status	00	RW
C5	Power Management Status	00	RW
C6	PCI-to-PCI Bridge Support Extension	00	RW
C7	Power Management Data	00	RW
C8-CF	-reserved-	00	—

Offset	ECC Error Control	Default	Acc
D3-D0	ECC Error Address	xx	**RO**
D4	ECC Error Syndrome Bit	xx	**RO**
D5-DF	-reserved-	00	—

Offset	UMA Control (Reserved)	Default	Acc
E0-E3	-reserved-	00	—

Offset	DRAM Above 4G Control	Default	Acc
E4	Low Top Address Low	00	RW
E5	Low Top Address High	**FF**	RW
E6	SMM / APIC Decoding	**01**	RW
E7-EF	-reserved-	00	—

Offset	Test	Default	Acc
F0	PLL Test Mode (do not program)	00	RW
F1	PLL Test Mode Select	00	RW
F2	Chip Test Mode (do not program)	00	RW

Offset	BIOS Scratch & Foundry ID	Default	Acc
F3-F7	BIOS Scratch Registers	00	RW
F8	Foundry ID	00	RW

Offset	Back Door Control	Default	Acc
F9	Back Door Control	00	RW
FA	Back-Door Max # of AGP Requests	00	RW
FB	Back-Door Revision ID	00	RW
FD-FC	Back-Door Device ID	0000	RW
FE-FF	-reserved-	00	—

Pro266T Device 1 - PCI-to-PCI Bridge

Header Registers

Offset	Configuration Space Header	Default	Acc
1-0	Vendor ID	**1106**	RO
3-2	Device ID	**B101**	RO
5-4	Command	**0007**	**RW**
7-6	Status	**0230**	**WC**
8	Revision ID (R/W if Rx44[7]=1)	**0n**	RO
9	Program Interface	00	RO
A	Sub Class Code	**04**	RO
B	Base Class Code	**06**	RO
C	-reserved-	00	—
D	Latency Timer	00	**RW**
E	Header Type	**01**	RO
F	Built In Self Test (BIST)	00	RO
17-10	-reserved-	00	—
18	Primary Bus Number	00	**RW**
19	Secondary Bus Number	00	**RW**
1A	Subordinate Bus Number	00	**RW**
1B	Secondary Latency Timer	00	RO
1C	I/O Base	**F0**	**RW**
1D	I/O Limit	00	**RW**
1F-1E	Secondary Status	0000	RO
21-20	Memory Base	**FFF0**	**RW**
23-22	Memory Limit (Inclusive)	0000	**RW**
25-24	Prefetchable Memory Base	**FFF0**	**RW**
27-26	Prefetchable Memory Limit	0000	**RW**
28-33	-reserved-	00	—
34	Capability Pointer	**80**	RO
35-3D	-reserved-	00	—
3F-3E	PCI-to-PCI Bridge Control	00	**RW**

Device-Specific Registers

Offset	AGP Bus Control	Default	Acc
40	CPU-to-AGP Flow Control 1	00	RW
41	CPU-to-AGP Flow Control 2	**08**	RW
42	AGP Master Control	00	RW
43	AGP Master Latency Timer	**22**	RW
44	Back-Door Register Control	**20**	RW
45	Fast Write Control	**72**	RW
47-46	PCI-to-PCI Bridge Device ID	0000	RW
48-7F	-reserved-	00	—
80	Capability ID	**01**	**RO**
81	Next Pointer	00	**RO**
82	Power Management Capabilities 1	**02**	**RO**
83	Power Management Capabilities 2	00	**RO**
84	Power Management Control / Status	00	RW
85	Power Management Status	00	**RO**
86	PCI-PCI Bridge Support Extensions	00	**RO**
87	Power Management Data	00	**RO**
88-FF	-reserved-	00	—

Miscellaneous I/O

One I/O port is defined in the Pro266T: Port 22.

Port 22 – PCI / AGP Arbiter Disable .....RW

7-2 Reserved ..... always reads 0

1 AGP Arbiter Disable
- 0 Respond to GREQ# signal .....default
- 1 Do not respond to GREQ# signal

0 PCI Arbiter Disable
- 0 Respond to all REQ# signals .....default
- 1 Do not respond to any REQ# signals, including PREQ#

This port can be enabled for read/write access by setting bit-7 of Device 0 Configuration Register 76.

Configuration Space I/O

All registers in the Pro266T (listed above) are addressed via the following configuration mechanism:

Mechanism #1

These ports respond only to double-word accesses. Byte or word accesses will be passed on unchanged.

Port CFB-CF8 - Configuration Address..... RW

31 Configuration Space Enable
- 0 Disabled..... default
- 1 Convert configuration data port writes to configuration cycles on the PCI bus

30-24 Reserved .....always reads 0

23-16 PCI Bus Number
Used to choose a specific PCI bus in the system

15-11 Device Number
Used to choose a specific device in the system (devices 0 and 1 are defined for the Pro266T)

10-8 Function Number
Used to choose a specific function if the selected device supports multiple functions (only function 0 is defined for the Pro266T).

7-2 Register Number (also called the "Offset")
Used to select a specific DWORD in the Pro266T configuration space

1-0 Fixed .....always reads 0

Port CFF-CFC - Configuration Data..... RW

Refer to PCI Bus Specification Version 2.1 for further details on operation of the above configuration registers.

Register Descriptions

Device 0 Header Registers - Host Bridge

All registers are located in PCI configuration space. They should be programmed using PCI configuration mechanism 1 through CF8 / CFC with bus number, function number, and device number equal to zero.

Device 0 Offset 1-0 - Vendor ID (1106h) .....RO

15-0 ID Code (reads 1106h to identify VIA Technologies)

Device 0 Offset 3-2 - Device ID (3101h).....RO

15-0 ID Code (reads 3101h to identify the Pro266T)

Device 0 Offset 5-4 –Command (0006h).....RW

15-10 Reserved ..... always reads 0

9 Fast Back-to-Back Cycle Enable ..... RO
- 0 Fast back-to-back transactions only allowed to the same agent.....default
- 1 Fast back-to-back transactions allowed to different agents

8 SERR# Enable..... RO
- 0 SERR# driver disabled.....default
- 1 SERR# driver enabled

(SERR# is used to report parity errors if bit-6 is set).

7 Address / Data Stepping..... RO
- 0 Device never does stepping.....default
- 1 Device always does stepping

6 Parity Error Response.....**RW**
- 0 Ignore parity errors & continue.....default
- 1 Take normal action on detected parity errors

5 VGA Palette Snoop..... RO
- 0 Treat palette accesses normally.....default
- 1 Don't respond to palette accesses on PCI bus

4 Memory Write and Invalidate Command ..... RO
- 0 Bus masters must use Mem Write.....default
- 1 Bus masters may generate Mem Write & Inval

3 Special Cycle Monitoring..... RO
- 0 Does not monitor special cycles.....default
- 1 Monitors special cycles

2 Bus Master ..... RO
- 0 Never behaves as a bus master
- 1 Can behave as a bus master.....default

1 Memory Space..... RO
- 0 Does not respond to memory space
- 1 Responds to memory space.....default

0 I/O Space ..... RO
- 0 Does not respond to I/O space .....default
- 1 Responds to I/O space

Device 0 Offset 7-6 – Status (0210h).....RWC

15 Detected Parity Error
- 0 No parity error detected..... default
- 1 Error detected in either address or data phase. This bit is set even if error response is disabled (command register bit-6). .....write one to clear

14 Signaled System Error (SERR# Asserted)
..... always reads 0

13 Signaled Master Abort
- 0 No abort received ..... default
- 1 Transaction aborted by the master .....
.....write one to clear

12 Received Target Abort
- 0 No abort received ..... default
- 1 Transaction aborted by the target .....
.....write one to clear

11 Signaled Target Abort ..... always reads 0
- 0 Target Abort never signaled

10-9 DEVSEL# Timing
- 00 Fast
- 01 Medium ..... always reads 01
- 10 Slow
- 11 Reserved

8 Data Parity Error Detected
- 0 No data parity error detected ..... default
- 1 Error detected in data phase. Set only if error response enabled via command bit-6 = 1 and Pro266T was initiator of the operation in which the error occurred.....write one to clear

7 Fast Back-to-Back Capable..... always reads 0

6 User Definable Features ..... always reads 0

5 66MHz Capable..... always reads 0

4 Supports New Capability list..... always reads 1

3-0 Reserved ..... always reads 0

Device 0 Offset 8 - Revision ID (0nh)..... RO

7-0 Chip Revision Code..... always reads 0nh
..... (n = revision code)

Device 0 Offset 9 - Programming Interface (00h)..... RO

7-0 Interface Identifier..... always reads 00

Device 0 Offset A - Sub Class Code (00h)..... RO

7-0 Sub Class Code..... reads 00 to indicate Host Bridge

Device 0 Offset B - Base Class Code (06h)..... RO

7-0 Base Class Code.. reads 06 to indicate Bridge Device

Device 0 Offset D - Latency Timer (00h)..... RW

Specifies the latency timer value in PCI bus clocks.

7-3 Reserved ..... always read 0

2-0 Guaranteed Time Slice for CPU (fixed granularity of 8 clks) ..... always read 0

Bits 2-1 are writeable but read 0 for PCI specification compatibility. The programmed value may be read back in Offset 75 bits 5-4 (PCI Arbitration 1).

Device 0 Host Bridge Header Registers (continued)

Device 0 Offset E - Header Type (00h).....RO

7-0 Header Type Code ..... reads 00: single function

Device 0 Offset F - Built In Self Test (BIST) (00h).....RO

7 BIST Supported .....reads 0: no supported functions

6-0 Reserved ..... always reads 0

Device 0 Offset 13-10 - Graphics Aperture Base (00000008h) .....RW

31-28 Upper Programmable Base Address Bits ..... def=0

27-20 Lower Programmable Base Address Bits ..... def=0

These bits behave as if hardwired to 0 if the corresponding Graphics Aperture Size register bit (Device 0 Offset 84h) is 0.

27	26	25	24	23	22	21	20	(This Register)
7	6	5	4	3	2	1	0	(Gr Aper Size)
RW	RW	RW	RW	RW	RW	RW	RW	1M
RW	RW	RW	RW	RW	RW	RW	0	2M
RW	RW	RW	RW	RW	RW	0	0	4M
RW	RW	RW	RW	RW	0	0	0	8M
RW	RW	RW	RW	0	0	0	0	16M
RW	RW	RW	0	0	0	0	0	32M
RW	RW	0	0	0	0	0	0	64M
RW	0	0	0	0	0	0	0	128M
0	0	0	0	0	0	0	0	256M

19-0 Reserved ..... always reads 00008

Note: The locations in the address range defined by this register are prefetchable.

Device 0 Offset 2D-2C – Subsystem Vendor ID (0000h) RW

15-0 Subsystem Vendor ID ..... default = 0

This register may be written once and is then read only.

Device 0 Offset 2F-2E – Subsystem ID (0000h)..... RW

15-0 Subsystem ID ..... default = 0

This register may be written once and is then read only.

Device 0 Offset 37-34 - Capability Pointer (000000A0h) RO

Contains an offset from the start of configuration space.

31-0 AGP Capability List Pointer ..... always reads A0h

Device 0 Configuration Registers - Host Bridge

These registers are normally programmed once at system initialization time.

V-Link Control

Device 0 Offset 40 – V-Link Specification ID (00h) .....RO

7-0 Specification Revision..... always reads 00

Device 0 Offset 41 – NB V-Link Capability (18h) .....RO

7-6 Reserved ..... always reads 0
5 16-bit Bus Width Supported .....RO
0 Not Supported .....default
1 Supported
4 8-Bit Bus Width Supported.....RO
0 Not Supported
1 Supported .....default
3 4x Rate Supported .....RO
0 Not Supported
1 Supported .....default
2 2x Rate Supported .....RO
0 Not Supported .....default
1 Supported
1-0 Reserved ..... always reads 0

Device 0 Offset 42 – NB Downlink Command (88h) .....RW

7-4 DnCmd Max Request Depth (0=1 DnCmd) . def = 8
3-0 DnCmd Write Buffer Size (doublewords)..... def = 8

Device 0 Offset 44-43 – NB Uplink Status (8280h).....RO

15-12 UpCmd P2C Write Buffer Size (max lines).. def = 8
11-8 UpCmd P2P Write Buffer Size (max lines).. def = 2
7-4 UpCmd Max Request Depth (0=1 UpCmd) . def = 8
3-0 Reserved ..... always reads 0

Device 0 Offset 45 –NB V-Link Bus Timer (44h) .....RW

7-4 Timer for Normal Priority Requests from SB
3-0 Timer for High Priority Requests from SB
0000 Immediate
0001 1*4 VCLKs
0010 2*4 VCLKs
0011 3*4 VCLKs
0100 4*4 VCLKs..... default (both timers)
0101 5*4 VCLKs
0110 6*4 VCLKs
0111 7*4 VCLKs
1000 8*4 VCLKs
1001 16*4 VCLKs
1010 32*4 VCLKs
1011 64*4 VCLKs
11xx Own the bus for as long as there is a request

Device 0 Offset 46 – NB V-Link Misc Control (00h) ..... RW

7 Downstream High Priority
0 Disable High Priority Down Commands..... def
1 Enable High Priority Down Commands
6 Downlink Priority
0 Treat Downlink Cycles as Normal Priority def
1 Treat Downlink Cycles as High Priority
5-4 Combine Multiple STPGNT Cycles into V-Link Command
00 Compatible, 1 command per V-Link cmd ... def
01 2 commands per V-Link command
10 3 commands per V-Link command
11 1 commands per V-Link command
3-2 V-Link Master Access Ordering Rules
00 High priority read, pass normal read (not pass write) ..... default
01 Read (high/normal) pass write (HR>LR>W)
1x Read / write in order
1-0 Reserved .....always reads 0

Device 0 Offset 47 – V-Link Control (00h)..... RW

7-3 Reserved .....always reads 0
2 Auto-Disconnect
0 Disable..... default
1 Enable
1 V-Link Disconnect Cycle for HALT cycle
0 Disable..... default
1 Enable
0 V-Link Disconnect Cycle for STPGNT Cycle
0 Disable..... default
1 Enable

Device 0 Offset 48 – NB/SB V-Link Configuration (18h)RW

7 Reserved .....always reads 0
6 Rest Bus Width Supported
0 Not Supported ..... default
1 Supported
5 16-bit Bus Width Supported
0 Not Supported ..... default
1 Supported
4 8-Bit Bus Width Supported
0 Not Supported
1 Supported ..... default
3 4x Rate Supported
0 Not Supported
1 Supported ..... default
2 2x Rate Supported
0 Not Supported ..... default
1 Supported
1-0 Reserved .....always reads 0

Device 0 Offset 49 – SB V-Link Capability (18h) ..... RO

7-6 Reserved ..... always reads 0
5 16-bit Bus Width Supported ..... RO
0 Not Supported ..... default
1 Supported
4 8-Bit Bus Width Supported ..... RO
0 Not Supported
1 Supported ..... default
3 4x Rate Supported ..... RO
0 Not Supported
1 Supported ..... default
2 2x Rate Supported ..... RO
0 Not Supported ..... default
1 Supported
1-0 Reserved ..... always reads 0

Device 0 Offset 4A – SB Downlink Status (88h) ..... RO

7-4 DnCmd Max Request Depth (0=1 DnCmd) . def = 8
3-0 DnCmd Write Buffer Size (doublewords)..... def = 8

Device 0 Offset 4C-4B – SB Uplink Command (8280h). RW

15-12 UpCmd P2C Write Buffer Size (max lines).. def = 8
11-8 UpCmd P2P Write Buffer Size (max lines).. def = 2
7-4 UpCmd Max Request Depth (0=1 UpCmd) . def = 8
3-0 Reserved ..... always reads 0

Device 0 Offset 4D – SB V-Link Bus Timer (44h) ..... RW

7-4 Timer for Normal Priority Requests from SB
3-0 Timer for High Priority Requests from SB
0000 Immediate
0001 1*4 VCLKs
0010 2*4 VCLKs
0011 3*4 VCLKs
0100 4*4 VCLKs ..... default (both timers)
0101 5*4 VCLKs
0110 6*4 VCLKs
0111 7*4 VCLKs
1000 8*4 VCLKs
1001 16*4 VCLKs
1010 32*4 VCLKs
1011 64*4 VCLKs
11xx Own the bus for as long as there is a request

Device 0 Offset 4E – CCA Master Priority (00h)..... RW

7 Packet Bus High Priority
0 Low priority ..... default
1 High priority
6 LAN / NIC High Priority
0 Low priority ..... default
1 High priority
5 Reserved ..... always reads 0
4 USB High Priority
0 Low priority ..... default
1 High priority
3 Reserved ..... always reads 0
2 IDE High Priority
0 Low priority ..... default
1 High priority
1 AC97-ISA High Priority
0 Low priority ..... default
1 High priority
0 PCI High Priority
0 Low priority ..... default
1 High priority

Device 0 Offset 4F – SB V-Link Misc Control (00h) ..... RW

7 Upstream Command High Priority
0 Disable high priority up commands..... default
1 Enable high priority up commands
6-1 Reserved ..... always reads 0
0 Down Cycle Wait for Up Cycle Write Flush (Except Down Cycle Post Write)
0 Disable ..... default
1 Enable

Host CPU Control

Device 0 Offset 50 – Request Phase Control (00h) .....RW

7 CPU Hardwired IOQ (In Order Queue) Size
Default set from the strap on South Bridge LA18 (communicated to the Pro266T via VAD2). This register can be written 0 to restrict the chip to one level of IOQ.
0 1-Level
1 8-Level

6 GTL Pullup
Default set from the inverse of the strap on South Bridge LA19 (communicated to the Pro266T via VAD3).
0 Disable .....default
1 Enable

5 Reserved ..... always reads 0

4-0 Dynamic Defer Snoop Stall Count

Device 0 Offset 51 – CPU Interface Basic Control (00h)RW

7 Reserved ..... always reads 0

6 Read Around Write
0 Disable .....default
1 Enable

5 DRQ Control
0 Non pipelined similar to Pro266).....default
1 Pipelined

4 CPU to PCI Read Defer
0 Disable .....default
1 Enable

3 Two Defer / Retry Entries
0 Disable .....default
1 Enable

2 Two Defer / Retry Entries Shared
0 Each entry is dedicated to 1 CPU.....default
1 Each entry is shared by 2 CPUs

1 PCI Master Pipelined Access
0 Disable .....default
1 Enable

0 Reserved ..... always reads 0

Device 0 Offset 52 – CPU Interface Advanced Ctrl (00h)RW

7 CPU RW DRAM 0WS for Back-to-Back Pipeline Access
0 Disable..... default
1 Enable

6 HREQ / HPRI
0 Disable..... default
1 Enable

5 GTL POS
0 Disable (Pro266 Compatible) ..... default
1 Enable

4 Dynamic Snoop Stall for CPU FIFO Full
0 Disable..... default
1 Enable

3 Write Retire Policy After 2 Writes
0 Disable..... default
1 Enable

2 133 / 100 DADS Fast Conversion
0 Disable..... default
1 Enable

1 Consecutive Speculative Read
0 Disable..... default
1 Enable

0 Speculative Read
0 Disable..... default
1 Enable

Device 0 Offset 53 – CPU Arbitration Control (03h) .... RW

7-4 Host Timer ..... default = 0

3-0 BPRI Timer (units of 4 HCLKs) ..... default = 3

Device 0 Offset 54 – CPU Frequency (00h) ..... RW

7-6 CPU Frequency (VAD1-0 strap from SB SA[16-17])
00 66
01 100
1x 133

5-2 Reserved .....always reads 0

1 AGP Capability Header Support
0 Disable..... default
1 Enable

0 VPX Mode
0 Disable (AGP Mode)..... default
1 Enable (VPX Mode)

DRAM Control

These registers are normally set at system initialization time and not accessed after that during normal system operation. Some of these registers, however, may need to be programmed using specific sequences during power-up initialization to properly detect the type and size of installed memory (refer to the VIA Technologies Pro266T BIOS porting guide for details).

Table 6. System Memory Map

Space	Start	Size	Address Range	Comment
DOS	0	640K	00000000-0009FFFF	Cacheable
VGA	640K	128K	000A0000-000BFFFF	Used for SMM
BIOS	768K	16K	000C0000-000C3FFF	Shadow Ctrl 1
BIOS	784K	16K	000C4000-000C7FFF	Shadow Ctrl 1
BIOS	800K	16K	000C8000-000CBFFF	Shadow Ctrl 1
BIOS	816K	16K	000CC000-000CFFFF	Shadow Ctrl 1
BIOS	832K	16K	000D0000-000D3FFF	Shadow Ctrl 2
BIOS	848K	16K	000D4000-000D7FFF	Shadow Ctrl 2
BIOS	864K	16K	000D8000-000DBFFF	Shadow Ctrl 2
BIOS	880K	16K	000DC000-000DFFFF	Shadow Ctrl 2
BIOS	896K	64K	000E0000-000EFFFF	Shadow Ctrl 3
BIOS	960K	64K	000F0000-000FFFFF	Shadow Ctrl 3
Sys Bus Init	1MB D Top 4G-64K	— 64K	00100000-DRAM Top DRAM Top-FFFEFFFF FFFEFFFF-FFFFFFFF	Can have hole 000Fxxxx alias

Device 0 Offset 55 – DRAM Control (00h)..... RW

7 0WS Back-to-Back Write to Different DDR Bank
- 0 Disable..... default
- 1 Enable

6 Reserved .....always reads 0

5 DQS Input DLL Adjustment
- 0 Disable..... default
- 1 Enable

4 DQS Output DLL Adjustment
- 0 Disable..... default
- 1 Enable

3 DQM Removal (Always Perform 4-Burst RW)
- 0 Disable..... default
- 1 Enable

2 DQS Output
- 0 Disable..... default
- 1 Enable

1 Auto Precharge for TLB Read or CPU WriteBack
- 0 Disable..... default
- 1 Enable

0 Write Recovery Time
- 0 1T ..... default
- 1 2T

Device 0 Offset 59-58 - DRAM MA Map Type (2222h). RW

15-13 Bank 5/4 MA Map Type (see table below)
12 Bank 5/4 1T Command Rate
0 2T Command .....default
1 1T Command
11-9 Bank 7/6 MA Map Type (see table below)
8 Bank 7/6 1T Command Rate
0 2T Command .....default
1 1T Command
7-5 Bank 1/0 MA Map Type (see table below)
4 Bank 1/0 1T Command Rate
0 2T Command .....default
1 1T Command
3-1 Bank 3/2 MA Map Type (see table below)
0 Bank 3/2 1T Command Rate
0 2T Command .....default
1 1T Command

Table 7. MA Map Type Encoding

000	16Mb	8-bit, 9-bit, 10-bit Column Address
001	64/128Mb	8-bit Column Address .....default
010	64/128Mb	9-bit Column Address
011	64/128Mb	10/11-bit Column Address
100		-reserved-
101	256Mb	8-bit Column Address
110	256Mb	9-bit Column Address
111	256Mb	10/11-bit Column Address

Device 0 Offset 5F-5A – DRAM Row Ending Address:

Offset 5A – Bank 0 Ending (HA[31:24]) (01h)..... RW
Offset 5B – Bank 1 Ending (HA[31:24]) (01h)..... RW
Offset 5C – Bank 2 Ending (HA[31:24]) (01h)..... RW
Offset 5D – Bank 3 Ending (HA[31:24]) (01h)..... RW
Offset 5E – Bank 4 Ending (HA[31:24]) (01h)..... RW
Offset 5F – Bank 5 Ending (HA[31:24]) (01h)..... RW
Offset 56 – Bank 6 Ending (HA[31:24]) (01h)..... RW
Offset 57 – Bank 7 Ending (HA[31:24]) (01h)..... RW

Note : BIOS is required to fill the ending address registers for all banks even if no memory is populated. The endings have to be in incremental order.

Device 0 Offset 60 – DRAM Type (00h)..... RW

7-6 DRAM Type for Bank 7/6
5-4 DRAM Type for Bank 5/4
3-2 DRAM Type for Bank 3/2
1-0 DRAM Type for Bank 1/0
00 SDR SDRAM..... default
01 -reserved- (do not program)
10 DDR SDRAM
11 -reserved-

Table 8. Memory Address Mapping Table

SDR / DDR SDRAM (x4 DRAMs supported by SDR only)

MA:	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
16Mb		24		13	12	11	14	22	21	20	19	18	17	16	15	12 row
(000)				13	PC	24	23	10	9	8	7	6	5	4	3	10,9,8 col
64/128Mb																x16 (14,8)
2K page	14	24	14	13	12	11	23	22	21	20	19	18	17	16	15	x32 (14,8)
001		27	14	13	PC	26	25	10	9	8	7	6	5	4	3	x8 (14,9)
4K page	14	25	14	13	12	24	23	22	21	20	19	18	17	16	15	x16 (14,9)
010		27	14	13	PC	26	11	10	9	8	7	6	5	4	3	x4 (14,10)
8K page	14	26	14	13	25	24	23	22	21	20	19	18	17	16	15	x8 (14,10)
011		27	14	13	PC	12	11	10	9	8	7	6	5	4	3	x4 (14,11)
256Mb																
2K page	25	24	14	13	12	11	23	22	21	20	19	18	17	16	15	x32 (15,8)
101		27	14	13	PC	26	25	10	9	8	7	6	5	4	3	
4K page	26	25	14	13	12	24	23	22	21	20	19	18	17	16	15	x16 (15,9)
110		27	14	13	PC	26	11	10	9	8	7	6	5	4	3	
8K page	27	26	14	13	25	24	23	22	21	20	19	18	17	16	15	x8 (15,10)
111		28	14	13	PC	12	11	10	9	8	7	6	5	4	3	x4 (15,11)

Device 0 Offset 61 - Shadow RAM Control 1 (00h).....RW

7-6 CC000h-CFFFFh
- 00 Read/write disable.....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

5-4 C8000h-CBFFFh
- 00 Read/write disable.....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

3-2 C4000h-C7FFFh
- 00 Read/write disable.....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

1-0 C0000h-C3FFFh
- 00 Read/write disable.....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

Device 0 Offset 62 - Shadow RAM Control 2 (00h).....RW

7-6 DC000h-DFFFFh
- 00 Read/write disable.....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

5-4 D8000h-DBFFFh
- 00 Read/write disable.....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

3-2 D4000h-D7FFFh
- 00 Read/write disable.....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

1-0 D0000h-D3FFFh
- 00 Read/write disable.....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

Device 0 Offset 63 - Shadow RAM Control 3 (00h)..... RW

7-6 E0000h-EFFFFh
- 00 Read/write disable ..... default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

5-4 F0000h-FFFFFh
- 00 Read/write disable ..... default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

3-2 Memory Hole
- 00 None ..... default
- 01 512K-640K
- 10 15M-16M (1M)
- 11 14M-16M (2M)

1-0 SMI Mapping Control

	SMM		Non-SMM	
	Code	Data	Code	Data
00	DRAM	DRAM	PCI	PCI
01	DRAM	DRAM	DRAM	DRAM
10	DRAM	PCI	PCI	PCI
11	DRAM	DRAM	DRAM	DRAM

Device 0 Offset 64 - DRAM Timing for All Banks (E4h)RW

7 Precharge Command to Active Command Period
- 0 TRP = 2T
- 1 TRP = 3T.....default

6 Active Command to Precharge Command Period
- 0 TRAS = 5T
- 1 TRAS = 6T.....def

5-4 CAS Latency

	SDR	DDR
00	1T	-
01	2T	2T
10	3T	2.5T.....default
11	-	3T

3 Reserved ..... always reads 0

2 ACTIVE to CMD
- 0 2T
- 1 3T .....default

1-0 Bank Interleave
- 00 No Interleave.....default
- 01 2-way
- 10 4-way
- 11 Reserved

For 16Mb SDRAMs bank interleave is always 2-way

Device 0 Offset 65 - DRAM Arbitration Timer (00h) ....RW

7-4 AGP Timer (units of 4 MCLKs) ..... default = 0
3-0 CPU Timer (units of 4 MCLKs)..... default = 0

Device 0 Offset 66 - DRAM Arbitration Control (00h)..RW

7 SDR – Feedback Clock Select
DDR - DQS Input Delay Setting
- 0 Auto (Rx67 reads DLL calibration result) ...def
- 1 Manual (Rx67 reads DQS input delay)

6 DDR - DQS Output Delay Setting
- 0 Auto .....default
- 1 Manual

5-4 Arbitration Parking Policy
- 00 Park at last bus owner .....default
- 01 Park at CPU
- 10 Park at AGP
- 11 -reserved-

3-0 AGP / CPU Priority (units of 4 MCLKs)

Device 0 Offset 67 – DDR Strobe Input Delay (00h) ..... RW

SDR:
7-5 Reserved .....always reads 0
4 MD Latch Clock Select
- 0 Internal clock..... default
- 1 External feedback clock

3 Reserved .....always reads 0
2-0 MD Latch Delay

DDR:
7-6 CS Early Clock Select ..... default = 0
5-0 DQS Input Delay ..... default = 0
(if Rx66[7]=0, read DLL calibration result)

Device 0 Offset 68 – DDR Strobe Output Delay (00h)... RW

7-0 DDR DQS Output Delay ..... default = 0

Device 0 Offset 69 – DRAM Clock Select (00h).....RW

7 CPU Operating Frequency Faster Than DRAM
- 0 CPU Same As or Equal to DRAM.....default
- 1 CPU Faster Than DRAM by 33 MHz

6 DRAM Operating Frequency Faster Than CPU
- 0 DRAM Same As or Equal to CPU.....default
- 1 DRAM Faster Than CPU by 33 MHz

Rx68[1-0]	Rx69[7-6]	CPU / DRAM
00	00	66 / 66 (def)
00	01	66 / 100†
01	10	100 / 66
01	00	100 / 100
01	01	100 / 133†
1x	10	133 / 100
1x	00	133 / 133

†Rx53[6] must also be set to 1 for DRAM > CPU

5 Dynamic CKE
- 0 Disable .....default
- 1 Enable

4 Reserved ..... always reads 0

3 DRAM 8K Page Enable
- 0 Disable .....default
- 1 Enable

2 DRAM 4K Page Enable
- 0 Disable .....default
- 1 Enable

1 DIMM Type
- 0 Unbuffered.....default
- 1 Registered

0 Multiple Page Mode
- 0 Disable .....default
- 1 Enable

Device 0 Offset 6A - Refresh Counter (00h)..... RW

7-0 Refresh Counter (in units of 16 MCLKs)
- 00 DRAM Refresh Disabled ..... default
- 01 32 MCLKs
- 02 48 MCLKs
- 03 64 MCLKs
- 04 80 MCLKs
- 05 96 MCLKs
- … …

The programmed value is the desired number of 16-MCLK units minus one.

Device 0 Offset 6B - DRAM Arbitration Control (10h).RW

7 Fast Read to Write turn-around
- 0 Disable .....default
- 1 Enable

6 Page Kept Active When Cross Bank
- 0 Disable .....default
- 1 Enable

5 Burst Refresh
- 0 Disable .....default
- 1 Enable

4 CKE Function
- 0 Disable
- 1 Enable .....default

3 Swap HA14 and HA22
- 0 Normal .....default
- 1 Swap to Improve Performance

2-0 SDRAM Operation Mode Select
- 000 Normal SDRAM Mode.....default
- 001 NOP Command Enable
- 010 All-Banks-Precharge Command Enable (CPU-to-DRAM cycles are converted to All-Banks-Precharge commands).
- 011 MSR Enable CPU-to-DRAM cycles are converted to commands and the commands are driven on MA[14:0]. The BIOS selects an appropriate host address for each row of memory such that the right commands are generated on MA[14:0].
- 100 CBR Cycle Enable (if this code is selected, CAS-before-RAS refresh is used; if it is not selected, RAS-Only refresh is used)
- 101 Reserved
- 11x Reserved

Device 0 Offset 6C - Drive Control 1 (00h)..... RW

7-6 SDRAM A Drive – SRASA/SCASA/SWEA, MAA
- 00 ..... default
- 01
- 10
- 11

5-4 SDRAM B Drive – SRASB/SCASB/SWEB, MAB
- 00 ..... default
- 01
- 10
- 11

3-2 DDR DQS Drive
- 00 ..... default
- 01
- 10
- 11

1-0 MD/MECC/CAS/CKE Early Clock Select
- 00 ..... default
- 01
- 10
- 11

Device 0 Offset 6D - Drive Control 2 (00h)..... RW

7-6 Early Clock Select for SCMD, MA Output (for 1T Command)
- 00 ..... default
- 01
- 10
- 11

5-4 DQM Drive
- 00 ..... default
- 01
- 10
- 11

3-2 RAS# Drive
- 00 ..... default
- 01
- 10
- 11

1-0 Memory Data Drive (MD, MECC)
- 00 ..... default
- 01
- 10
- 11

Device 0 Offset 6E - ECC Control (00h) .....RW

7 ECC / EC Mode Select
- 0 ECC Checking and Reporting.....default
- 1 ECC Checking, Reporting, and Correcting

6 Perform Read-Modify-Write for Partial Write
- 0 Disable .....default
- 1 Enable

5 Enable SERR# on ECC / EC Multi-Bit Error
- 0 Don't assert SERR# for multi-bit errors .....def
- 1 Assert SERR# for multi-bit errors

4 Enable SERR# on ECC / EC Single-Bit Error
- 0 Don't assert SERR# for single-bit errors .....def
- 1 Assert SERR# for single-bit errors

3 ECC / EC Enable - Bank 7/6 (DIMM 3)
- 0 Disable (no ECC or EC for banks 7/6)...default
- 1 Enable (ECC or EC per bit-7)

2 ECC / EC Enable - Bank 5/4 (DIMM 2)
- 0 Disable (no ECC or EC for banks 5/4)...default
- 1 Enable (ECC or EC per bit-7)

1 ECC / EC Enable - Bank 3/2 (DIMM 1)
- 0 Disable (no ECC or EC for banks 3/2)...default
- 1 Enable (ECC or EC per bit-7)

0 ECC / EC Enable - Bank 1/0 (DIMM 0)
- 0 Disable (no ECC or EC for banks 1/0)...default
- 1 Enable (ECC or EC per bit-7)

Error checking / correction may be enabled bank-pair by bank-pair (DIMM by DIMM) by using bits 0-2 above. Bank pairs must be populated with 72-bit memory to enable for EC or ECC since the additional data bits must be present in either case. For this reason, if 64-bit memory is populated in a particular bank pair, the corresponding bit 0-2 should be set to 0 to disable both EC and ECC for that bank pair. For those bank pairs that have 72-bit memory available (and have the corresponding bit 0-2 set), either EC or ECC may be selected via bit-7 above (i.e., all enabled bank pairs will use EC or all will use ECC).

If error checking / reporting only (EC) is selected, all read and write cycles will use normal timing. Partial writes (with EC or ECC enabled) will use read-modify-write cycles to maintain correct error correction codes in the additional 8 data bits. If EC and ECC are disabled for a particular bank pair, partial writes to that bank pair will use the byte enables to write only the selected bytes (using normal write cycles and cycle timing). If error correction (ECC) is selected, the first read of a transaction will always have one additional cycle of latency.

Bit-7	Bits 2-0	RMW	Error Checking	Error Correction
0/1	0	No	No	No
0	1	Yes	Yes	No
1	1	Yes	Yes	Yes

Device 0 Offset 6F - ECC Status (00h).....RWC

7 Multi-bit Error Detected ..... write of '1' resets

6-4 Multi-bit Error DRAM Bank..... default=0
Encoded value of the bank with the multi-bit error.

3 Single-bit Error Detected ..... write of '1' resets

2-0 Single-bit Error DRAM Bank ..... default=0
Encoded value of the bank with the single-bit error.

Table 9. DIMM Module Configuration

Rx6B [4] CKE Ena	Rx6E [3-0] ECC Ena	Rx6E [6] RMW Ena	Rx55 [3] No DQM	DIMM Module Configuration	MECC [7-0] Pins	DQM [8-0] Pins	DQS# [8-0] Pins
1	1	0	1	DDR Only x8 with ECC	MECC[7-0]	CKE[7-0]	DQS[8-0]#
1	0	0	0	DDR Only x8 no ECC	CKE[7-0]	DQM[7-0]	DQS[7-0]#
0	0	0	0	184-Pin DDR/SDR Mix	CKE[7-0]	DQM[8-0]	DQS[8-0]#
1	1	x	0	168-Pin SDR Only	MECC[7-0]	DQM[8-0]	CKE[7-0]
1	0	0	1	2 DDR + 2 SDR (SDR Installed)	CKE[7-0]	-	DQS[7-0]#
1	0	0	0	2 DDR + 2 SDR (DDR Installed)	CKE[7-0]	DQM[7-0]	DQS[7-0]#

PCI Bus Control

These registers are normally programmed once at system initialization time.

Device 0 Offset 70 - PCI Buffer Control (00h).....RW

7 CPU to PCI Post-Write
- 0 Disable .....default
- 1 Enable

6 Reserved ..... always reads 0

5-4 PCI Master to DRAM Prefetch
- 00 Always prefetch .....default
- x1 Prefetch disabled
- 10 Prefetch only for enhance command

3-2 Reserved ..... always reads 0

1 Delay Transaction
- 0 Disable .....default
- 1 Enable

0 Reserved ..... always reads 0

Device 0 Offset 71 - CPU to PCI Flow Control 1 (48h)RWC

7 Retry Status
- 0 No retry occurred .....default
- 1 Retry occurred..... **write 1 to clear**

6 Retry Timeout Action
- 0 Retry Forever (record status only)
- 1 Flush buffer for write
  or return all 1s for read**.....default**

5-4 Retry Count and Retry Backoff
- 00 Retry 2 times, backoff CPU .....default
- 01 Retry 16 times
- 10 Retry 4 times
- 11 Retry 64 times

3 PCI Burst
- 0 Disable
- 1 Enable **.....default**

2 Reserved ..... always reads 0

1 Compatible Type 1 Configuration Cycle AD31
- 0 Fix AD31 .....default
- 1

0 IDSEL Control
- 0 AD11, AD12 .....default
- 1 AD30, AD31

Device 0 Offset 73 - PCI Master Control 1 (00h) .....RWC

7 Reserved .....always reads 0

6 PCI Master 1-Wait-State Write
- 0 Zero wait state TRDY# response..... default
- 1 One wait state TRDY# response

5 PCI Master 1-Wait-State Read
- 0 Zero wait state TRDY# response..... default
- 1 One wait state TRDY# response

4 WSC# (Write Snoop Complete)
- 0 Disable..... default
- 1 Enable

3-1 Reserved .....always reads 0

0 PCI Master Broken Timer Enable
- 0 Disable..... default
- 1 Enable. Force into arbitration when there is no FRAME# 16 PCICLK's after the grant.

Device 0 Offset 75 - PCI Arbitration 1 (00h) ..... RW

7 Arbitration Mode
- 0 REQ-based (arbitrate at end of REQ#) ..default
- 1 Frame-based (arbitrate at FRAME# assertion)

6-4 CPU Latency ..... read only, reads Rx0D bits 2:1

3 Reserved ..... always reads 0

2-0 PCI Master Bus Time-Out

(force into arbitration after a period of time)
- 000 Disable .....default
- 001 1x16 PCICLKs
- 010 2x16 PCICLKs
- 011 3x16 PCICLKs
- 100 4x16 PCICLKs
- ... ...
- 111 7x16 PCICLKs

Device 0 Offset 76 - PCI Arbitration 2 (00h)..... RW

7 I/O Port 22 Enable (South Bridge)
- 0 CPU access to I/O address 22 is passed on to the PCI bus ..... default
- 1 CPU access to I/O address 22 is processed internally

6 Reserved .....always reads 0

5-4 Master Priority Rotation Control
- 00 Disable..... default
- 01 Grant to CPU after every PCI master grant
- 10 Grant to CPU after every 2 PCI master grants
- 11 Grant to CPU after every 3 PCI master grants

With setting 01, the CPU will always be granted access after the current bus master completes, no matter how many PCI masters are requesting. With setting 10, if other PCI masters are requesting during the current PCI master grant, the highest priority master will get the bus after the current master completes, but the CPU will be guaranteed to get the bus after that master completes. With setting 11, if other PCI masters are requesting, the highest priority will get the bus next, then the next highest priority will get the bus, then the CPU will get the bus. In other words, with the above settings, even if multiple PCI masters are continuously requesting the bus, the CPU is guaranteed to get access after every master grant (01), after every other master grant (10) or after every third master grant (11).

3-2 REQn# to REQ4# Mapping
- 00 REQ4#..... default
- 01 REQ0#
- 10 REQ1#
- 11 REQ2#

1 Reserved .....always reads 0

0 REQ4# is High Priority Master
- 0 Disable..... default
- 1 Enable

GART / Graphics Aperture Control

The function of the Graphics Address Relocation Table (GART) is to translate virtual 32-bit addresses issued by an AGP device into 4K-page based physical addresses for system memory access. In this translation, the upper 20 bits (A31-A12) are remapped, while the lower 12 address bits (A11-A0) are used unchanged.

A one-level fully associative lookup scheme is used to implement the address translation. In this scheme, the upper 20 bits of the virtual address are used to point to an entry in a page table located in system memory. Each page table entry contains the upper 20 bits of a physical address (a "physical page" address). For simplicity, each page table entry is 4 bytes. The total size of the page table depends on the GART range (called the "aperture size") which is programmable in the Pro266T.

This scheme is shown in the figure below.

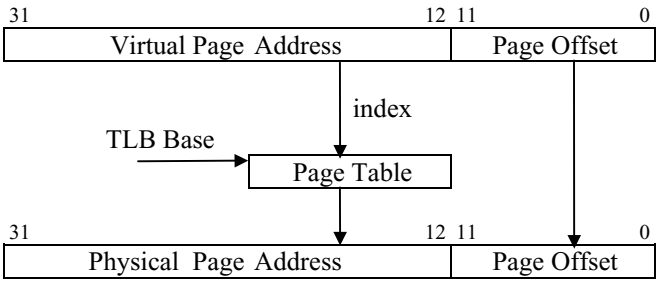


Figure 4. Graphics Aperture Address Translation

Since address translation using the above scheme requires an access to system memory, an on-chip cache (called a "Translation Lookaside Buffer" or TLB) is utilized to enhance performance. The TLB in the Pro266T contains 16 entries. Address "misses" in the TLB require an access of system memory to retrieve translation data. Entries in the TLB are replaced using an LRU (Least Recently Used) algorithm.

Addresses are translated only for accesses within the "Graphics Aperture" (GA). The Graphics Aperture can be any power of two in size from 1MB to 256MB (i.e., 1MB, 2MB, 4MB, 8MB, etc). The base of the Graphics Aperture can be anywhere in the system virtual address space on an address boundary determined by the aperture size (e.g., if the aperture size is 4MB, the base must be on a 4MB address boundary). The Graphics Aperture Base is defined in register offset 10 of device 0. The Graphics Aperture Size and TLB Table Base are defined in the following register group (offsets 84 and 88 respectively) along with various control bits.

Device 0 Offset 83-80 - GART/TLB Control (00000000h) RW

31-16 Reserved ..... always reads 0

15-8 Reserved (test mode status) ..... RO

7 Flush Page TLB
- 0 Disable..... default
- 1 Enable

6-0 Reserved (always program to 0) ..... RW

Note: For any master access to the Graphics Aperture range, snoop will not be performed.

Device 0 Offset 84 - Graphics Aperture Size (00h) ..... RW

7-0 Graphics Aperture Size

11111111	1M
11111110	2M
11111100	4M
11111000	8M
11110000	16M
11100000	32M
11000000	64M
10000000	128M
00000000	256M

Offset 8B-88 - GA Translation Table Base (00000000h) RW

31-12 Graphics Aperture Translation Table Base. Pointer to the base of the translation table in system memory used to map addresses in the aperture range (the pointer to the base of the "Directory" table).

11-2 Reserved ..... always reads 0

1 Graphics Aperture Enable
- 0 Disable..... default
- 1 Enable

Note: To disable the Graphics Aperture, set this bit to 0 and set all bits of the Graphics Aperture Size to 0. To enable the Graphics Aperture, set this bit to 1 and program the Graphics Aperture Size to the desired aperture size.

0 Reserved ..... always reads 0

AGP Control

Device 0 Offset A3-A0 - AGP Capability Identifier (0020C002h) .....RO

31-24 Reserved ..... always reads 00h
23-20 Major Specification Revision ..... always reads 2h
Major rev of AGP spec that device conforms to (2.x)
19-16 Minor Specification Revision ..... always reads 0h
Minor rev # of AGP spec that device conforms to
15-8 Pointer to Next Item ..... always reads C0 (last item)
7-0 AGP ID .. (always reads 02 to indicate it is AGP)

Device 0 Offset A7-A4 - AGP Status (1F000201h) .....RO

31-24 Maximum AGP Requests..... always reads 1F†
Max # of AGP requests the device can manage (32)
† See also RxFC[1] and RxFD[4-0]
23-10 Reserved .....always reads 0s
9 Supports SideBand Addressing ..... always reads 1
8-6 Reserved .....always reads 0s
5 4G Supported (can be written at RxAE[5]..... def=0
4 Fast Wr Supported (can be written at AE[4]... def=0
3 Reserved .....always reads 0s
2 4X Rate Supported (can be written at AE[2]).. def=0
1 2X Rate Supported (can be written at AC[3]) . def=0
0 1X Rate Supported ..... always reads 1

Device 0 Offset AB-A8 - AGP Command (00000000h) . RW

31-24 Request Depth (reserved for target).. always reads 0s
23-10 Reserved ..... always reads 0s
9 SideBand Addressing Enable
0 Disable..... default
1 Enable
8 AGP Enable
0 Disable..... default
1 Enable
7-6 Reserved ..... always reads 0s
5 4G Enable
0 Disable..... default
1 Enable
4 Fast Write Enable
0 Disable..... default
1 Enable
3 Reserved ..... always reads 0s
2 4X Mode Enable
0 Disable..... default
1 Enable
1 2X Mode Enable
0 Disable..... default
1 Enable
0 1X Mode Enable
0 Disable..... default
1 Enable

Device 0 Offset AC - AGP Control (08h) .....RW

7 AGP Disable
- 0 Enable .....default
- 1 Disable

6 AGP Read Synchronization
- 0 Disable .....default
- 1 Enable

5 AGP Read Snoop DRAM Post-Write Buffer
- 0 Disable .....default
- 1 Enable

4 GREQ# Priority Becomes Higher When Arbiter is Parked at AGP Master
- 0 Disable .....default
- 1 Enable

3 2X Rate Supported (read also at RxA4[1])
- 0 Not supported
- 1 Supported .....default

2 LPR In-Order Access (Force Fence)
- 0 Fence/Flush functions not guaranteed. AGP read requests (low/normal priority and high priority) may be executed before previously issued write requests. .....default
- 1 Force all requests to be executed in order (automatically enables Fence/Flush functions). Low (i.e., normal) priority AGP read requests will never be executed before previously issued writes. High priority AGP read requests may still be executed prior to previously issued write requests as required.

1 AGP Arbitration Parking
- 0 Disable .....default
- 1 Enable (GGNT# remains asserted until either GREQ# de-asserts or data phase ready)

0 AGP to PCI Master or CPU to PCI Turnaround Cycle
- 0 2T or 3T Timing.....default
- 1 1T Timing

Device 0 Offset AD – AGP Latency Timer (02h) ..... RW

7-6 Reserved .....always reads 0

5 Input on AGP GD / GBE Pads
- 0 Disable Input ..... default
- 1 Enable Input

4 Choose First or Last Ready of DRAM
- 0 Last ready chosen ..... default
- 1 First ready chosen

3-0 AGP Data Phase Latency Timer..... default = 02h

Device 0 Offset AE – AGP Miscellaneous Control (00h)RW

7-6 Reserved .....always reads 0

5 4G Supported
- 0 4G not supported ..... default
- 1 4G supported

4 Fast Write Supported
- 0 Fast Write not supported ..... default
- 1 Fast Write supported

3 Reserved .....always reads 0

2 4x Rate Supported
- 0 4x Rate not supported..... default
- 1 4x Rate supported

1-0 Reserved .....always reads 0

Device 0 Offset B0 – AGP Pad Control / Status (xxh) ...RW

7 AGP 4x Strobe VREF Control
- 0 STB VREF is STB# and vice versa
- 1 STB VREF is AGPREF **.....default**

6 AGP 4x Strobe & GD Pad Drive Strength
- 0 Drive strength set to compensation circuit default .....default
- 1 Drive strength controlled by RxB1[7-0]

5-3 AGP Compensation Circuit N Control Output. RO

2-0 AGP Compensation Circuit P Control Output . RO

Device 0 Offset B1 – AGP Compensation Drive Strength (63h).....RW

7-4 AGP Output Buffer Drive Strength N Ctrl ... def=6

3-0 AGP Output Buffer Drive Strength P Ctrl.... def=3

Device 0 Offset B2 – AGP Pad Drive / Delay Ctrl (08h) RW

7 GD/GBE/GDS, SBA/SBS Control

1.5V (Bit-1 = 0)
- 0 SBA/SBS = no cap ..... default
  GD/GBE/GDS = no cap
- 1 SBA/SBS = no cap
  GD/GBE/GDS = **cap**

3.3V (Bit-1 = 1)
- 0 SBA/SBS = **cap** ..... default
  GD/GBE/GDS = no cap
- 1 SBA/SBS = **cap**
  GD/GBE/GDS = **cap**

6-5 Reserved .....always reads 0

4 GD[31-16] Staggered Delay
- 0 None ..... default
- 1 GD[31:16] delayed by 1 ns

3 GD / GDS / GDS# Slew Rate Control
- 0 Disable
- 1 Enable**..... default**

2 GDS / GDS# Preamble Control
- 0 Disable..... default
- 1 Enable

1 AGP Bus Voltage
- 0 1.5V ..... default
- 1 3.3V

0 GDS Output Delay
- 0 None ..... default
- 1 GDS[1-0] & GDS[1-0]# delayed by 0.4 ns

Note: GDS1 & GDS1# will be delayed an additional 1ns if bit-4 = 1

Device 0 Offset B3 – AGP Strobe Drive Strength..... RW

7-4 AGP Strobe Output Buffer Drive Strength N Ctrl

3-0 AGP Strobe Output Buffer Drive Strength P Ctrl

V-Link Control

Device 0 Offset B4 – V-Link NB Compensation Ctrl (00h)RW

7-6 **V-Link Autocomp Output Value**..... always reads 0
5 **Pullup Compensation Selection**
0 Auto Comp (use values in bits 7-6).....default
1 Manual Comp (use values in bits 3-2)
4 **Pulldown Compensation Selection**
0 Auto Comp (use values in bits 7-6).....default
1 Manual Comp (use values in bits 1-0)
3-2 **Pullup Compensation Manual Setting** ..... def = 0
1-0 **Pulldown Compensation Manual Setting** .... def = 0

Device 0 Offset B5 – V-Link NB Drive Control (00h)....RW

7-6 **NB V-Link Strobe Pullup Manual Setting**
5-4 **NB V-Link Strobe Pulldown Manual Setting**
3-1 **Reserved** ..... always reads 0
0 **NB V-Link Slew Rate Control**
0 Disable .....default
1 Enable

Device 0 Offset B8 – V-Link SB Compensation Ctrl (00h)RW

7-6 **V-Link Autocomp Output Value**..... always reads 0
5 **Pullup Compensation Selection**
0 Auto Comp (use values in bits 7-6).....default
1 Manual Comp (use values in bits 3-2)
4 **Pulldown Compensation Selection**
0 Auto Comp (use values in bits 7-6).....default
1 Manual Comp (use values in bits 1-0)
3-2 **Pullup Compensation Manual Setting** ..... def = 0
1-0 **Pulldown Compensation Manual Setting** .... def = 0

Device 0 Offset B9 – V-Link SB Drive Control (00h) ....RW

7-6 **SB V-Link Strobe Pullup Manual Setting**
5-4 **SB V-Link Strobe Pulldown Manual Setting**
3-1 **Reserved** ..... always reads 0
0 **SB V-Link Slew Rate Control**
0 Disable .....default
1 Enable

DRAM Interface Control

Device 0 Offset BE – MECC Drive Strength (00h)..... RW

7-6 **MECC Drive Strength** ..... default = 0
5-0 **Reserved** .....always reads 0

Device 0 Offset BF – DRAM Pad Toggle Reduction (00h)RW

7 **MA / SCMD Pin Toggle Reduction**
0 Disable..... default
1 Enable (MA and S command pins won't toggle if not accessed)
6 **Slew Rate Control for MA / SCMD Group B**
0 Disable..... default
1 Enable
5 **Slew Rate Control for MA / SCMD Group A**
0 Disable..... default
1 Enable
4 **Reserved** .....always reads 0
3 **DIMM #3 MAA / MAB Select**
0 MAA ..... default
1 MAB
2 **DIMM #2 MAA / MAB Select**
0 MAA ..... default
1 MAB
1 **DIMM #1 MAA / MAB Select**
0 MAA ..... default
1 MAB
0 **DIMM #0 MAA / MAB Select**
0 MAA ..... default
1 MAB

Extended Power Management Control

Device 0 Offset C0 – Capability ID (01h).....RO

Device 0 Offset C1 – Next Pointer (00h).....RO

Device 0 Offset C2 – Power Mgmt Capabilities 1 (02h)..RO

Device 0 Offset C3 – Power Mgmt Capabilities 2 (00h)..RO

Device 0 Offset C4 – Power Mgmt Control/Status (00h)RW

7-2 Reserved ..... always reads 0

1-0 Power State

00 D0 .....default

11 D3 hot

Device 0 Offset C5 – Power Management Status (00h) .RW

Device 0 Offset C6 – PCI to PCI Bridge Support Extensions (00h) .....RW

Device 0 Offset C7 – Power Management Data (00h)....RW

ECC Error Control

Device 0 Offset D3-D0 – ECC Error Address (xxh) ..... RO

Device 0 Offset D4 – ECC Error Syndrome (xxh)..... RO

DRAM Above 4G Control

Device 0 Offset E4 – Low Top Address Low (00h).....RW

7-4 Low Top Address Low ..... default = 0

3-0 DRAM Granularity

0 16M Total DRAM less than 4G.....default
1 32M Total DRAM less than 8G
2 64M Total DRAM less than 16G
3 128M Total DRAM less than 32G
4 256M Total DRAM less than 64G
5-7 -reserved-

Device 0 Offset E5 – Low Top Address High (FFh).....RW

7-0 Low Top Address High ..... default = FFh

Device 0 Offset E6 – SMM / APIC Decoding (01h).....RW

7-6 Reserved ..... always reads 0

5 Reserved (Do Not Program)..... default = 0

4 I/O APIC Decoding

0 FECxxxxx accesses go to PCI .....default
1 FEC00000 to FEC7FFFF accesses go to PCI
FEC80000 to FECFFFFF accesses go to AGP

3 MSI (Processor Message) Support

0 Disable (master access to FEExxxxx will go to PCI) .....default
1 Enable (master access to FEExxxxx will be passed to host side to do snoop)

2 Top SMM

0 Disable .....default
1 Enable

1 High SMM

0 Disable .....default
1 Enable

0 Compatible SMM

0 Disable .....default
1 Enable

Test Registers

Device 0 Offset F0-F2 – Test (Do Not Program).....RW

BIOS Scratch Registers

Device 0 Offset F7-F3 – BIOS Scratch Registers.....RW

7-0 No hardware function..... default = 0

Back Door Registers

Device 0 Offset F9 – Back Door Control ..... RW

Device 0 Offset FA – Back Door Max AGP Requests ... RW

Device 0 Offset FB – Back Door Revision ..... RW

Device 0 Offset FD-FC – Back Door Device ID..... RW

Device 1 Header Registers - PCI-to-PCI Bridge

All registers are located in PCI configuration space. They should be programmed using PCI configuration mechanism 1 through CF8 / CFC with bus number of 0 and function number equal to 0 and device number equal to one.

Device 1 Offset 1-0 - Vendor ID (1106h) .....RO

15-0 ID Code (reads 1106h to identify VIA Technologies)

Device 1 Offset 3-2 - Device ID (B101h) .....RO

15-0 ID Code (reads B101h to identify the Pro266T PCI-to-PCI Bridge device)

Device 1 Offset 5-4 – Command (0007h).....RW

15-10 Reserved ..... always reads 0

9 Fast Back-to-Back Cycle Enable ..... RO
- 0 Fast back-to-back transactions only allowed to the same agent.....default
- 1 Fast back-to-back transactions allowed to different agents

8 SERR# Enable..... RO
- 0 SERR# driver disabled.....default
- 1 SERR# driver enabled

(SERR# is used to report parity errors if bit-6 is set).

7 Address / Data Stepping..... RO
- 0 Device never does stepping.....default
- 1 Device always does stepping

6 Parity Error Response.....RW
- 0 Ignore parity errors & continue.....default
- 1 Take normal action on detected parity errors

5 VGA Palette Snoop (Not Supported) ..... RO
- 0 Treat palette accesses normally.....default
- 1 Don't respond to palette writes on PCI bus (10-bit decode of I/O addresses 3C6-3C9 hex)

4 Memory Write and Invalidate Command ..... RO
- 0 Bus masters must use Mem Write.....default
- 1 Bus masters may generate Mem Write & Inval

3 Special Cycle Monitoring..... RO
- 0 Does not monitor special cycles.....default
- 1 Monitors special cycles

2 Bus Master .....RW
- 0 Never behaves as a bus master
- 1 Enable to operate as a bus master on the primary interface on behalf of a master on the secondary interface .....default

1 Memory Space.....RW
- 0 Does not respond to memory space
- 1 Enable memory space access .....default

0 I/O Space .....RW
- 0 Does not respond to I/O space
- 1 Enable I/O space access .....default

Device 1 Offset 7-6 - Status (Primary Bus) (0230h).....RWC

15 Detected Parity Error .....always reads 0

14 Signaled System Error (SERR#).....always reads 0

13 Signaled Master Abort
- 0 No abort received ..... default
- 1 Transaction aborted by the master with Master-Abort (except Special Cycles)..... ..... write 1 to clear

12 Received Target Abort
- 0 No abort received ..... default
- 1 Transaction aborted by the target with Target-Abort ..... write 1 to clear

11 Signaled Target Abort .....always reads 0

10-9 DEVSEL# Timing
- 00 Fast
- 01 Medium .....always reads 01
- 10 Slow
- 11 Reserved

8 Data Parity Error Detected.....always reads 0

7 Fast Back-to-Back Capable.....always reads 0

6 User Definable Features .....always reads 0

5 66MHz Capable.....always reads 1

4 Supports New Capability list.....always reads 0

3-0 Reserved .....always reads 0

Device 1 Offset 8 - Revision ID (00h)RO (RW if Rx44[7]=1)

7-0 Pro266T Chip Revision Code (00=First Silicon)

Device 1 Offset 9 - Programming Interface (00h)..... RO

This register is defined in different ways for each Base/Sub-Class Code value and is undefined for this type of device.

7-0 Interface Identifier.....always reads 00

Device 1 Offset A - Sub Class Code (04h)..... RO

7-0 Sub Class Code .reads 04 to indicate PCI-PCI Bridge

Device 1 Offset B - Base Class Code (06h)..... RO

7-0 Base Class Code.. reads 06 to indicate Bridge Device

Device 1 Offset D - Latency Timer (00h)..... RO

7-0 Reserved .....always reads 0

Device 1 Offset E - Header Type (01h) ..... RO

7-0 Header Type Code..... reads 01: PCI-PCI Bridge

Device 1 Offset F - Built In Self Test (BIST) (00h) ..... RO

7 BIST Supported..... reads 0: no supported functions

6 Start Test ..... write 1 to start but writes ignored

5-4 Reserved .....always reads 0

3-0 Response Code.....0 = test completed successfully

Device 1 Offset 18 - Primary Bus Number (00h).....RW

7-0 Primary Bus Number ..... default = 0

This register is read write, but internally the chip always uses bus 0 as the primary.

Device 1 Offset 19 - Secondary Bus Number (00h) .....RW

7-0 Secondary Bus Number..... default = 0

Note: AGP must use these bits to convert Type 1 to Type 0.

Device 1 Offset 1A - Subordinate Bus Number (00h) ....RW

7-0 Primary Bus Number ..... default = 0

Note: AGP must use these bits to decide if Type 1 to Type 1 command passing is allowed.

Device 1 Offset 1B – Secondary Latency Timer (00h) ....RO

7-0 Reserved ..... always reads 0

Device 1 Offset 1C - I/O Base (f0h).....RW

7-4 I/O Base AD[15:12]..... default = 1111b

3-0 I/O Addressing Capability ..... default = 0

Device 1 Offset 1D - I/O Limit (00h).....RW

7-4 I/O Limit AD[15:12] ..... default = 0

3-0 I/O Addressing Capability ..... default = 0

Device 1 Offset 1F-1E - Secondary Status (0000h).....RO

15-0 Reserved ..... always reads 0

Device 1 Offset 21-20 - Memory Base (fff0h).....RW

15-4 Memory Base AD[31:20].....default = FFFh

3-0 Reserved ..... always reads 0

Device 1 Offset 23-22 - Memory Limit (Inclusive) (0000h) RW

15-4 Memory Limit AD[31:20] ..... default = 0

3-0 Reserved ..... always reads 0

Device 1 Offset 25-24 - Prefetchable Memory Base (fff0h) RW

15-4 Prefetchable Memory Base AD[31:20]default = FFFh

3-0 Reserved ..... always reads 0

Device 1 Offset 27-26 - Prefetchable Memory Limit (0000h) .....RW

15-4 Prefetchable Memory Limit AD[31:20] .....
..... default = 0

3-0 Reserved ..... always reads 0

Device 1 Offset 37-34 - Capability Pointer (00000080h). RO

Contains an offset from the start of configuration space.

31-0 AGP Capability List Pointer.....always reads 80h

Device 1 Offset 3F-3E – PCI-to-PCI Bridge Control (0000h) ..... RW

15-4 Reserved .....always reads 0

3 VGA-Present on AGP

0 Forward VGA accesses to PCI Bus..... default

1 Forward VGA accesses to AGP Bus

Note: VGA addresses are memory A0000-BFFFFh and I/O addresses 3B0-3BBh, 3C0-3CFh and 3D0-3DFh (10-bit decode). "Mono" text mode uses B0000-B7FFFh and "Color" Text Mode uses B8000-BFFFFh. Graphics modes use Axxxxh. Mono VGA uses I/O addresses 3Bx-3Cxh and Color VGA uses 3Cx-3Dxh. If an MDA is present, a VGA will not use the 3Bxh I/O addresses and B0000-B7FFFh memory space; if not, the VGA will use those addresses to emulate MDA modes.

2 Block / Forward ISA I/O Addresses

0 Forward all I/O accesses to the AGP bus if they are in the range defined by the I/O Base and I/O Limit registers (device 1 offset 1C-1D)
..... default

1 Do not forward I/O accesses to the AGP bus that are in the 100-3FFh address range even if they are in the range defined by the I/O Base and I/O Limit registers.

1-0 Reserved .....always reads 0

Device 1 Configuration Registers - PCI-to-PCI Bridge

AGP Bus Control

Device 1 Offset 40 - CPU-to-AGP Flow Control 1 (00h) RW

7 CPU-AGP Post Write
- 0 Disable .....default
- 1 Enable

6 Reserved ..... always reads 0

5 CPU-to-AGP One Wait State Burst Write
- 0 Disable .....default
- 1 Enable

4 AGP to DRAM Prefetch
- 0 Disable .....default
- 1 Enable

3 CPU to AGP Post Write Halt
- 0 Disable .....default
- 1 Enable

2 MDA Present on AGP
- 0 Forward MDA accesses to AGP .....default
- 1 Forward MDA accesses to PCI

Note: Forward despite IO / Memory Base / Limit

Note: MDA (Monochrome Display Adapter) addresses are memory addresses B0000h-B7FFFh and I/O addresses 3B4-3B5h, 3B8-3BAh, and 3BFh (10-bit decode). 3BC-3BE are reserved for printers.

Note: If Rx3E bit-3 is 0, this bit is a don't care (MDA accesses are forwarded to the PCI bus).

1 AGP Master Read Caching
- 0 Disable .....default
- 1 Enable

0 AGP Delay Transaction
- 0 Disable .....default
- 1 Enable

Table 10. VGA / MDA Memory / IO Redirection

3E[3] VGA Pres.	40[2] MDA Pres.	VGA is on	MDA is on	Axxxx, B8xxx Access	B0000 -B7FFF Access	3Cx, 3Dx I/O	3Bx I/O
0	-	PCI	PCI	PCI	PCI	PCI	PCI
1	0	AGP	AGP	AGP	AGP	AGP	AGP
1	1	AGP	PCI	AGP	PCI	AGP	PCI

Device 1 Offset 41 - CPU-to-AGP Flow Control 2 (08h) RW

7 Retry Status
- 0 No retry occurred..... default
- 1 Retry Occurred .....**write 1 to clear**

6 Retry Timeout Action
- 0 No action taken except to record status ..... def
- 1 Flush buffer for write or return all 1s for read

5-4 Retry Count
- 00 Retry 2, backoff CPU ..... default
- 01 Retry 4, backoff CPU
- 10 Retry 16, backoff CPU
- 11 Retry 64, backoff CPU

3 CPU to PCI Bursting Timeout
- 0 Disable
- 1 Enable ..... default

2 Reserved .....always reads 0

1 Invalidate PCI/AGP Read Buffered Data (Read Caching Data) on CPU-to-PCI/AGP Cycle
- 0 Disable..... default
- 1 Enable

0 Reserved .....always reads 0

Device 1 Offset 42 - AGP Master Control (00h) ..... RW

7 Reserved .....always reads 0

6 AGP Master One Wait State Write
- 0 Disable..... default
- 1 Enable

5 AGP Master One Wait State Read
- 0 Disable..... default
- 1 Enable

4 Break Consecutive PCI Master Accesses
- 0 Disable..... default
- 1 Enable

3 Reserved .....always reads 0

2 Claim I/O RW and Memory Read Cycles
- 0 Disable..... default
- 1 Enable

1 Claim Local APIC FEEx xxxx Cycles
- 0 Disable..... default
- 1 Enable

0 Host Side Snoop Cycles 2T Rate
- 0 Disable..... default
- 1 Enable

Device 1 Offset 43 - AGP Master Latency Timer (22h) RW

7-4 Host to AGP Time slot
- 0 Disable (no timer)
- 1 16 GCLKs
- 2 32 GCLKs .....default
- … …
- F 128 GCLKs

3-0 AGP Master Time Slot
- 0 Disable (no timer)
- 1 16 GCLKs
- 2 32 GCLKs .....default
- … …
- F 128 GCLKs

Device 1 Offset 44 – Backdoor Register Control (20h) .RW

7 Rx8 Revision ID Writable
- 0 Disable (Device 1 Rx8 is RO).....default
- 1 Enable (Device 1 Rx8 is RW)

6 Reserved ..... always reads 0

5 Power Management Capability Support
- 0 Read Rx34 as 00
- 1 Read Rx34 as 80 **.....default**

4 Rx1F-1E Reflect Status in Rx7-6
- 0 Rx1F-1E always read 0.....default
- 1 Rx1F-1E read same as Rx7-6

3 Back Door Register for Rx83[2], D2 Support
- 0 Disable .....default
- 1 Enable

2 Back Door Register for Rx83[1], D1 Support
- 0 Disable .....default
- 1 Enable

1 Back Door Register for Rx82[5], Device Specific Initialization
- 0 Disable .....default
- 1 Enable

0 Back Door Register for AGP Device ID
- 0 Disable .....default
- 1 Enable

Device 1 Offset 45 – Fast Write Control (72h)..... RW

7 Force Fast Write Cycle to be QW Aligned (if Rx45[6] = 0)
- 0 Disable..... default
- 1 Enable

6 Merge Multiple CPU Transactions Into One Fast Write Burst Transaction
- 0 Disable
- 1 Enable**..... default**

5 Merge Multiple CPU Write Cycles To Memory Offset 23-20 Into Fast Write Burst Cycles (if Rx45[6] = 0)
- 0 Disable
- 1 Enable**..... default**

4 Merge Multiple CPU Write Cycles To Prefetchable Memory Offset 27-24 Into Fast Write Burst Cycles (if Rx45[6] = 0)
- 0 Disable
- 1 Enable**..... default**

3 Reserved .....always reads 0

2 Fast Write Burst 4T Max (No Slave Flow Control)
- 0 Disable..... default
- 1 Enable

1 Fast Write Fast Back to Back
- 0 Disable
- 1 Enable**..... default**

0 Fast Write Initial Block 1 Wait State
- 0 Disable..... default
- 1 Enable

Rx45 Bits 7-4	CPU Write Address in Mem1	CPU Write Address in Mem2	Fast Write Cycle Alignment
x1xx	-	-	QW aligned, burstable
0000	-	-	DW aligned, nonburstable
x010	0	0	n/a
0010	0	1	DW aligned, non-burstable
x010	1	-	QW aligned, burstable
x001	0	0	n/a
x001	-	1	QW aligned, burstable
0001	1	0	DW aligned, non-burstable
x011	0	0	n/a
x011	1	-	QW aligned, burstable
x011	0	1	QW aligned, burstable
1000	-	-	QW aligned, non-burstable
1010	0	1	QW aligned, non-burstable
1001	1	0	QW aligned, non-burstable

Device 1 Offset 47-46 – PCI-to-PCI Bridge Device ID... RW

15-0 PCI-to-PCI Bridge Device ID ..... default = 0000

Device 1 Offset 80 – Capability ID (01h) ..... RO

7-0 Capability ID ..... always reads 01h

Device 1 Offset 81 – Next Pointer (00h) ..... RO

7-0 Next Pointer: Null ..... always reads 00h

Device 1 Offset 82 – Power Mgmt Capabilities 1 (02h) .. RO

7-0 Power Mgmt Capabilities ..... always reads 02h

Device 1 Offset 83 – Power Mgmt Capabilities 2 (00h) .. RO

7-0 Power Mgmt Capabilities ..... always reads 00h

Device 1 Offset 84 – Power Mgmt Ctrl/Status (00h)..... RW

7-2 Reserved ..... always reads 0

1-0 Power State

00 D0 ..... default
01 -reserved-
10 -reserved-
11 D3 Hot

Device 1 Offset 85 – Power Mgmt Status (00h)..... RO

7-0 Power Mgmt Status ..... default = 00

Device 1 Offset 86 – P2P Br. Support Extensions (00h) . RO

7-0 P2P Bridge Support Extensions ..... default = 00

Device 1 Offset 87 – Power Management Data (00h) ..... RO

7-0 Power Management Data ..... default = 00

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Min	Max	Unit
Case operating temperature (T_C)	0	85	^oC
Storage temperature (T_S)	-55	125	^oC
Input voltage (V_{IN})	-0.5	V_{RAIL} + 10%	Volts
Output voltage (V_{OUT})	-0.5	V_{RAIL} + 10%	Volts

Note: Stress above the conditions listed may cause permanent damage to the device. Functional operation of this device should be restricted to the conditions described under operating conditions.

DC Characteristics

T_C = 0-85^{o}C, V_{RAIL}= V_{CC} +/-5%, V_{CORE} =2.5V+/-5%, GND=0V

Symbol	Parameter	Min	Max	Unit	Condition
V_{IL}	Input low voltage	-0.50	0.8	V	
V_{IH}	Input high voltage	2.0	V_{CC}+0.5	V	
V_{OL}	Output low voltage	-	0.45	V	I_{OL}=4.0mA
V_{OH}	Output high voltage	2.4	-	V	I_{OH}=-1.0mA
I_{IL}	Input leakage current	-	+/-10	uA	$0<V_{IN}<V_{CC}$
I_{OZ}	Tristate leakage current	-	+/-20	uA	$0.45<V_{OUT}<V_{CC}$

Power Characteristics

T_C = 0-85°C, V_{RAIL}= V_{CC} +/-5%, V_{CORE} =2.5V+/-5%, GND=0V

Symbol	Parameter	Typ	Max	Unit	Condition
I_{CC}	Power supply current – VCC			mA	Max operation frequency
I_{CCGTL}	Power supply current – VCCGTL			mA	Max operation frequency
I_{CCVL}	Power supply current – VCCVL			mA	Max operation frequency
I_{CCM}	Power supply current – VCCM			mA	Max operation frequency
I_{CCAGP}	Power supply current – VCCAGP			mA	Max operation frequency
I_{CCQQ}	Power supply current – VCCQQ			mA	Max operation frequency
I_{SUS25}	Power supply current – VSUS25			mA	Max operation frequency
I_{CCAHCK}	Power supply current – AVCCHCK			uA	Max operation frequency
I_{CCAMCK}	Power supply current – AVCCMCK			uA	Max operation frequency
I_{CCADL1}	Power supply current – AVCCDL1			uA	Max operation frequency
I_{CCADL2}	Power supply current – AVCCDL2			uA	Max operation frequency
I_{MVREF}	Reference current – MVREF			uA	Max operation frequency
I_{GTLREF}	Reference current – GTLREF			uA	Max operation frequency
I_{AGPREF}	Reference current – AGPREF			mA	Max operation frequency
I_{VLREF}	Reference current – VLREF			uA	Max operation frequency
P_D	Power dissipation			W	Max operation frequency

AC Timing Specifications

AC timing specifications provided are based on external zero-pf capacitance load. Min/max cases are based on the following table:

Table 11. AC Timing Min / Max Conditions

Parameter	Min	Max	Unit
2.5V Power	2.375	2.625	Volts
3.3V Power	3.135	3.465	Volts
5V Reference	4.75	5.25	Volts
Case Temperature	0	85	^oC

Drive strength for each output pin is programmable. See (Device 0 Rx??) for details.

MECHANICAL SPECIFICATIONS

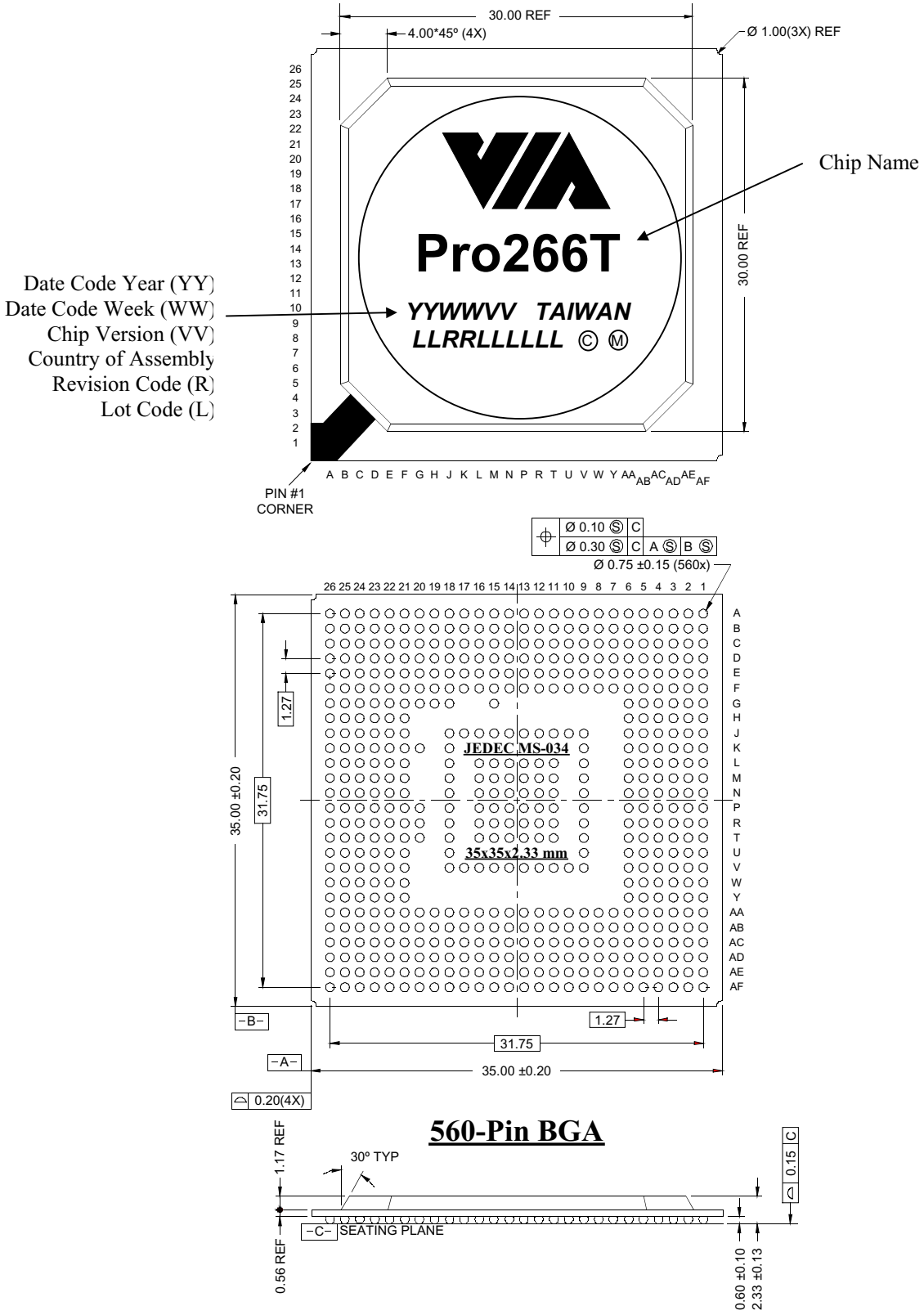


Figure 5. Mechanical Specifications - 560-Pin HSBGA Ball Grid Array Package with Heat Spreader