



P4X266E Chipset

VT8753E

**Single-Chip North Bridge
for Pentium 4 CPUs with 533 / 400 MHz FSB
and 4x AGP Bus
plus Advanced ECC Memory Controller
supporting PC2100 / PC1600 DDR SDRAM
and PC133 / PC100 SDR SDRAM
for Desktop PC Systems**

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VIA TECHNOLOGIES, INC.

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1.03	9/3/02	Fixed VIA USA street address on legal page; updated V-Link feature bullets Corrected miscellaneous document formatting errors and inconsistencies	DH
1.04	1/14/03	Removed misleading “strap” labels on VAD pins Added note to VAD pin descriptions; fixed VAD strap definitions and Rx50[7-6]	DH

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P4X266E CHIPSET

VT8753E

Single-Chip North Bridge
for Pentium 4 CPUs with 533 /400 MHz Front Side Bus
and 4x AGP Bus
plus Advanced ECC Memory Controller
supporting PC2100 / PC1600 DDR SDRAM
and PC133 / PC100 SDR SDRAM
for Desktop PC Systems

PRODUCT FEATURES

- **Defines Integrated Solutions for Value PC Desktop Designs**
 - High performance North Bridge with 533 MHz Front Side Bus for Pentium™ 4 plus AGP 4x external bus
 - 64-bit Advanced ECC Memory controller supporting PC2100/PC1600 DDR and PC100/PC133 SDR SDRAM
 - Combines with VIA VT8233 V-Link South Bridge for integrated LAN, Audio, ATA100 IDE, and 6 USB ports
 - 2.5V Core and AGTL+ I/O
 - 37.5 x 37.5mm PBGA package with 664 balls
- **High Performance CPU Interface**
 - Support for Intel™ Pentium 4 processors with 533 MHz (133 MHz QDR) CPU Front Side Bus (FSB)
 - Built-in Phase Lock Loop circuitry for optimal skew control within and between clocking regions
 - Thirteen outstanding transactions (twelve In-Order Queue (IOQ) plus one output latch)
 - Dynamic deferred transaction support
- **Full Featured Accelerated Graphics Port (AGP) Controller**
 - Supports 266 MHz 4x and 133 MHz 2x transfer modes for AD and SBA signaling
 - AGP specification v2.0 compliant
 - Pseudo-synchronous with the host CPU bus with optimal skew control
 - Supports SideBand Addressing (SBA) mode (non-multiplexed address / data)
 - AGP pipelined split-transaction long-burst transfers up to 1GB/sec
 - Eight level read request queue
 - Four level posted-write request queue
 - Thirty-two level (quadwords) read data FIFO (256 bytes)
 - Sixteen level (quadwords) write data FIFO (128 bytes)
 - Intelligent request reordering for maximum AGP bus utilization
 - Supports Flush/Fence commands
 - Graphics Address Relocation Table (GART)
 - One level TLB structure
 - Sixteen entry fully associative page table
 - LRU replacement scheme
 - Independent GART lookup control for host / AGP / PCI master accesses
 - Windows 95 OSR-2 VXD and integrated Windows 98 / Windows 2000 miniport driver support

- **Advanced High-Performance DDR / SDR DRAM Controller**

- DRAM interface pseudo-synchronous with host CPU (133/100 MHz) for most flexible configuration
- DRAM interface may be faster than CPU by 33 MHz to allow use of 133 MHz memory with 100 MHz FSB clock
- Concurrent CPU, AGP, and V-Link access
- Supports SDR and DDR SDRAM memory types
- Clock Enable (CKE) control for SDRAM power reduction in high speed systems
- Mixed 16M / 32M / 64M x 8/16/32 DRAMs
- Supports 8 banks up to 4 GB DRAMs (512Mb x8/x16 DRAM technology)
- Flexible row and column addresses. 64-bit data width only
- LVTTTL 3.3V DRAM interface with 5V-tolerant inputs for SDR SDRAM and 2.5V SSTL-2 DRAM interface for DDR SDRAM
- Programmable I/O drive capability for MA, MD, and command signals
- Dual copies of MA and control signals for improved drive
- Optional ECC (single-bit error correction and multi-bit error detection) or EC (error checking only) for DRAM integrity
- Two-bank interleaving for 16Mbit SDRAM support
- Two-bank and four bank interleaving for 64Mb, 128Mb, 256Mb and 512Mb SDRAM support
- Supports maximum 16-bank interleave (i.e., 16 pages open simultaneously); banks are allocated based on LRU
- Seamless DRAM command scheduling for maximum DRAM bus utilization
 - (e.g., precharge other banks while accessing the current bank)
- Four cache lines (16 quadwords) of CPU to DRAM write buffers
- Four cache lines of CPU to DRAM read prefetch buffers
- Read around write capability for non-stalled CPU read
- Speculative DRAM read before snoop result
- Burst read and write operation
- Burst length 4 and 8 for SDR and DDR
- Supports DDR SDRAM CL 2/2.5/3 and 1T per command
- 1T and 2T command rate for SDR and DDR which can be specified bank by bank
- Decoupled and burst DRAM refresh with staggered RAS timing (CAS before RAS or self refresh)

- **High Bandwidth 266 MB/Sec 8-bit V-Link Host Controller**

- Supports 66 MHz V-Link Host interface with total bandwidth of 266 MB/sec
- Operates at 2x or 4x modes
- Full duplex commands with separate command / strobe
- Request / Data split transaction
- Configurable outstanding transaction queue for Host to V-Link Client accesses
- Supports Defer / Defer-Reply transactions
- Transaction assurance for V-Link Host to Client access eliminates V-Link Host-Client Retry cycles
- Intelligent V-Link transaction protocol to eliminate data wait-state / throttle transfer latency
- All V-Link transactions for both Host and Client have a consistent view of transaction data depth and buffer size to avoid data overflow
- Highly efficient V-Link arbitration with minimum overhead
- All V-Link transactions have predictable cycle length with known command / data duration

- **Advanced System Power Management Support**

- Power down of SDRAM (CKE)
- VTT suspend power plane preserves memory data
- Suspend-to-DRAM and self-refresh power down
- Low-leakage I/O pads
- ACPI 1.0B and PCI Bus Power Management 1.1 compliant

OVERVIEW

The P4X266E (VT8753E North Bridge plus VT8233 South Bridge) is a high performance, cost-effective and energy efficient chip set for the implementation of desktop personal computer systems with 533 MHz (133 MHz QDR) CPU host bus (“Front Side Bus”) based on 64-bit Intel Pentium-4 super-scalar processors. The chipset VT8753E north bridge (described in this document) supports both 533 MHz and 400 MHz FSB speeds and is pin compatible with the VT8753 north bridge which supports 400 MHz FSB Pentium-4 CPUs.

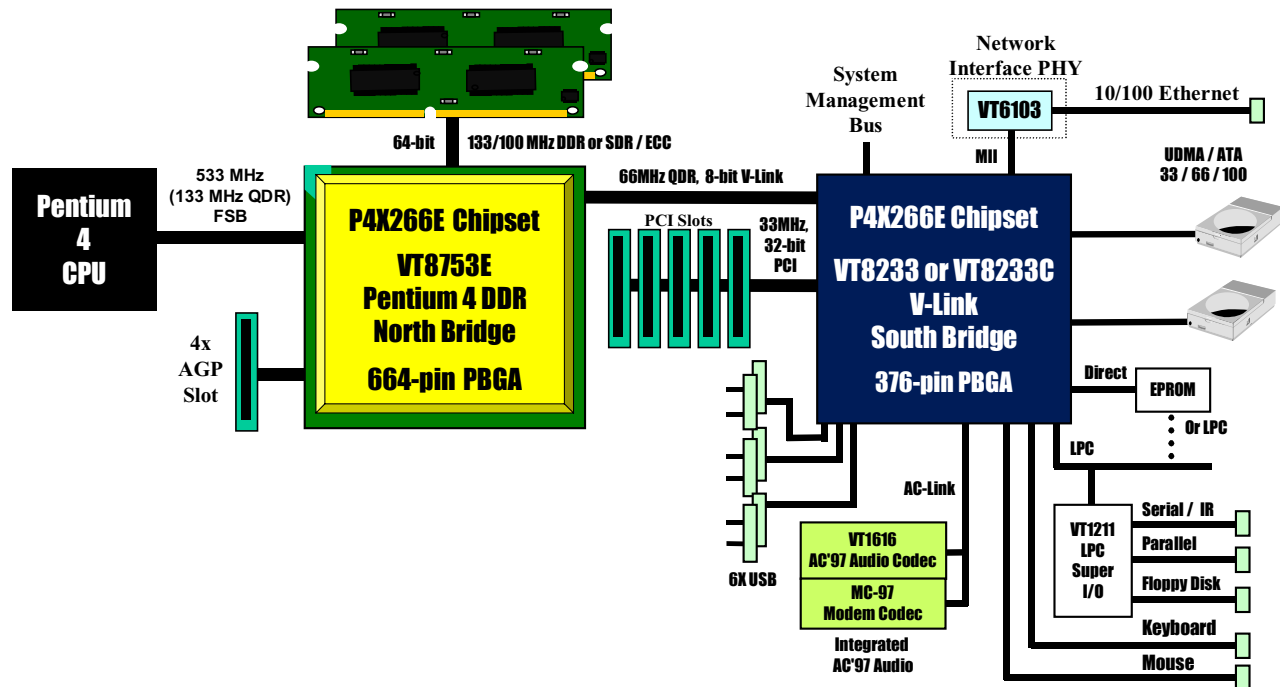


Figure 1. P4X266E Chipset System Block Diagram

The P4X266E chip set consists of the VT8753E North Bridge (664 pin BGA) and the VT8233 V-Link South Bridge (376 pin BGA). The VT8753 and VT8753E (sometimes also called “Host System Controllers”) are updates of VIA’s VT8653 Apollo Pro266T system controller that adds CPU bus extensions to support Pentium 4 CPUs. The VT8753E provides superior performance between the CPU, DRAM, V-Link bus and AGP 4x graphics controller bus with pipelined, burst, and concurrent operation. The VT8233 (which may also be referred to as a “V-Link Client Controller”) is a highly integrated PCI / LPC controller. Its internal bus structure is based on a 66 MHz PCI bus that provides 2x bandwidth compared to previous generation PCI bridge chips. The VT8233 also provides a 266MB/sec bandwidth Host / Client V-Link interface with V-Link-PCI and V-Link-LPC controllers. It supports five PCI slots of arbitration and decoding for all integrated functions and LPC bus.

The VT8753E supports eight banks of SDR / DDR SDRAMs up to 4 GB. The DRAM controller supports PC2100 / PC1600 Double-Data-Rated (DDR) SDRAM but can also support standard PC133 / PC100 Synchronous DRAM (SDR SDRAM). The DDR / SDR DRAM interface allows zero wait state bursting between the DRAM and the data buffers at 133 / 100 MHz. The different banks of DRAM can be composed of an arbitrary mixture of 1M / 2M / 4M / 8M / 16M / 32M / 64M x 8/16/32 DRAMs. The DRAM controller also supports optional ECC (single-bit error correction and multi-bit detection) or EC (error checking) capability. The DRAM controller can run either synchronous or pseudo-synchronous with the host CPU bus.

The VT8753E supports a high speed 8-bit 66 MHz Quad Data Transfer interconnect (V-Link) to the VT8233 South Bridge. The chip also contains a built-in bus-to-bus bridge to allow simultaneous concurrent operations on each bus. Five levels (doublewords) of post write buffers are included to allow for concurrent CPU and V-Link operation. For V-Link Host operation, forty-eight levels (doublewords) of post write buffers and sixteen levels (doublewords) of prefetch buffers are included for concurrent V-Link bus and DRAM/cache accesses. When combined the V-Link Host / Client controllers, it realizes a complete PCI sub-system and

supports enhanced PCI bus commands such as “Memory-Read-Line”, “Memory-Read-Multiple” and “Memory-Write-Invalid” commands to minimize snoop overhead. In addition, advanced features are supported such as snoop ahead, snoop filtering, L1 write-back forward to PCI master, and L1 write-back merged with PCI post write buffers to minimize PCI master read latency and DRAM utilization. Delay transaction and read caching mechanisms are also implemented for further improvement of overall system performance.

The 376-pin Ball Grid Array VT8233 Client V-Link PCI / LPC controller supports four levels (doublewords) of line buffers, type F DMA transfers and delay transaction to allow efficient PCI bus utilization and (PCI-2.1 compliant). The VT8233 integrated PCI controller and PCI arbitration for up to five PCI slots. One of the PCI REQ / GNT pair can be configured as high-priority to better support a low latency PCI bus master device. The VT8233 integrated networking MAC controller with standard MII interface to an external PHY for 10/100Mb base-T Ethernet or 1/10Mb PNA home networking.

The VT8233 also includes an integrated keyboard controller with PS2 mouse support, integrated DS12885 style real time clock with extended 256 byte CMOS RAM, integrated master mode enhanced IDE controller with full scatter / gather capability and extension to UltraDMA-33/66/100 for 33/66/100 MB/sec transfer rate, integrated USB interface with root hubs and six functional ports with built-in physical layer transceivers, Distributed DMA support, and OnNow / ACPI compliant advanced configuration and power management interface.

For sophisticated power management, the P4X266E chipset provides independent clock stop controls for the CPU / SDRAM and AGP bus plus Dynamic CKE control for powerdown of the SDRAM. A separate suspend-well plane is implemented for the SDRAM control signals for Suspend-to-DRAM operation. Coupled with the VT8233 south bridge chip, a complete power conscious PC main board can be implemented with no external TTLs.

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PINOUTS

Figure 2. Ball Diagram (Top View)

Key	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29			
A	NC	GCMP N0	GND QQ	VCC QQ	NC	NC	NC	NC	NC	NC	NC	NC	NC	HD61	HD58	HD56	HD62	HD48	HD47	HD44	HD35	HD40	HD32	HD36	HD16	HD18	HDS 1	HD22	HD27			
B	G GNT#	GND	GCMP N1	GND	NC	NC	NC	NC	NC	NC	NC	NC	NC	HD63	HD55	GND	HDS 3#	HD49	HD46	HD45	HD43	HDBI 2#	HD39	HD33	HD19	HD29	HDS 1#	GND	HD23			
C	G REQ#	SBA 1	SBA 0	GND	NC	NC	NC	NC	NC	NC	GND	NC	NC	GND	HD59	GND	HDS 3	HD51	HD50	HD41	GND	GND	HD38	HD28	HDBI 1#	HD26	HD25	HD20	HD31			
D	SBS#	SBS	SBA 4	SBA 3	GND	NC	NC	NC	NC	NC	NC	NC	NC	HD 60	GND	HDBI 3#	HD54	GND	GND	HDS 2	GND	HD37	HD30	GND	HD21	GND	HD17	HD24	HD13			
E	SBA 5	GND	SBA 6	SBA 2	ST0	NC	NC	NC	NC	NC	NC	NC	NC	CPU RST#	HD57	VTT	HD53	HD52	GND TT	HDS 2#	HD42	HD34	VTT	GND	GND	GND	HD12	HD4	HD7			
F	GD31	NC	SBA 7	GND	ST1	GND	GND	GND	VCC 25	VCC 25	VCC 25	GND	GND	VCC 25	VCC 25	HD VREF	VTT	VTT	HD VREF	VCC 25	VCC 25	HD VREF	VTT	HD VREF	HR COMP	HD3	HD9	HD11	HD1			
G	GD26	GD27	GD29	GD30	G PIPE#	AGP VREF	F7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 G23																	HCMP VREF	HD14	GND	HDBI 0#	HDS 0	HDS 0#			
H	GD24	GND	GD25	GD28	G RBF#	VCC 25	H CRT Pins																	VCC 25	HD5	HD15	GND	GND	HD10			
J	GD23	GDS 1#	GDS 1	GND	ST2	VCC 25	J CPU Pins																	VCC 25	HITM#	HD6	HD2	HD0	HD8			
K	GD21	GD19	GD20	GD22	GBE 3#	VCC AGP	K VCC AGP GND NC NC NC VTT VTT VTT VTT VTT VTT VTT																	VTT	D BSY#	GND	RS2#	RS0#	RS1#			
L	GD18	GND	GD17	G FRM#	G WBF#	VCC AGP	L AGP Pins																	GTL VREF	H LOCK#	B REQ#	HIT#	GND	B PRI#			
M	GI RDY#	GBE 2#	GD16	GND	NC	VCC AGP	M VCC AGP VCC AGP M GND GND GND GND GND GND GND GND GND GND GND GND GND																	VTT	GND HCK	H CLK#	HT RDY#	DE FER#	D RDY#	BNR#		
N	GD14	GD15	GBE 1#	G DSEL#	GD13	VCC 25	N VCC AGP VCC AGP N GND GND GND GND GND GND GND GND GND GND GND GND GND																		VTT	VCC HCK	H CLK	GND	HREQ 2#	HA7	HA3	
P	GD10	GND	GD11	GD12	GT RDY#	VCC 25	P VCC AGP VCC AGP P GND GND GND GND GND GND GND GND GND GND GND GND GND																		VTT	GND TT	ADS#	HREQ 4#	HREQ 1#	GND	HREQ 3#	
R	GBE 0#	GD9	GD8	GND	G STOP#	AGP VREF	R VCC AGP VCC AGP R GND GND GND GND GND GND GND GND GND GND GND GND GND																		VTT	HA VREF	HREQ 0#	HA5	HA4	HA11	HA6	
T	GD6	GD7	GD4	GDS 0	GDS 0#	VCC AGP	T VCC AGP VCC AGP T GND GND GND GND GND GND GND GND GND GND GND GND GND																		VTT	VTT	HAS 0#	GND	HA9	HA15	HA8	
U	GD2	GND	GD5	G PAR	G CLK	VCC AGP	U VCC VL VCC VL U GND GND GND GND GND GND GND GND GND GND GND GND GND																		VTT	VTT	GND	HA16	GND	HA12	HA13	
V	GD3	GD0	GD1	GND	VBE#	VCC AGP	V VCC VL VCC VL V GND GND GND GND GND GND GND GND GND GND GND GND GND																			VCC MEM	HA VREF	HA10	HA14	HA19	HA18	HA17
W	VAD 3	VAD 5	VAD 1	GND	VAD 0	VCC 25	W VCC VL VCC MEM W11 12 13 14 15 16 17 18 W19																	VCC MEM	VCC 25	TEST IN#	GND	HA25	HA22	HA24		
Y	UP CMD	GND	UP STB#	GND	VL VREF	VCC 25	Y VCC VL VCC MEM VCC MEM VCC MEM VCC MEM VCC MEM VCC MEM VCC MEM VCC MEM VCC MEM																	VCC MEM	VCC 25	VTT	HA30	HAS 1#	GND	HA29		
AA	DN STB	DN CMD	DN STB#	UP STB	VAD 4	VCC 25	AA VCC MEM VCC MEM VCC MEM VCC MEM VCC MEM VCC MEM VCC MEM VCC MEM VCC MEM																	VCC MEM	VTT	HA23	HA26	HA21	HA20	HA28		
AB	VAD 6	VAD 7	VAD 2	VL COMP	VSUS 25	GND	AB Mem Pins																	VTT	GND	GND	HA33	HA31	HA27			
AC	PWR OK	GND	RE SET#	SUS ST#	MD59	GND	AC7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 AC23																	GND MCK	MCLK	GND	HA32	GND	MD0			
AD	MD58	MD62	DQS 7#	DQM 7	MD63	GND	MEM VREF	NC	VCC 25	VCC 25	VCC 25	MEM VREF	VCC 25	VCC 25	GND MDLL	SCAS B#	SWE B#	MEM VREF	SRAS B#	VCC 25	VCC 25	VCC 25	MEM VREF	VCC MCK	MCLK F	MD2	MD1	MD5	MD4			
AE	MD57	MD61	MD56	GND	CS6#	CS7#	MD41	NC	CS0#	SCAS A#	MAB 10	CS4#	MECC 7	SWE A#	GND MDLL	MAA 1	GND	GND	GND	MAA 6	MAA 5	MAA 7	MAB 8	MAB 7	MAA 13	MAB 13	MD6	DQM 0	DQS 0#			
AF	MD51	GND	MD60	MD54	MD43	MD45	GND	CS1#	MD38	GND	CS5#	MAA 0	GND	MECC 1	MECC 0	GND	MAA 4	MD30	GND	MD25	MAA 5	GND	MD18	MD17	GND	MAA 9	MAB 9	GND	MD7			
AG	MD55	MD50	MD52	MD49	MD42	MD40	CS3#	MD39	MD34	MD33	MD36	MAA 12	MECC 3	DQS 8#	MAB 1	SRAS A#	MAA 3	MD27	MAB 6	MD29	MAB 14	MAA 8	MD22	MD21	MD10	MD15	MD9	MD8	MD3			
AH	DQS 6#	GND	MD48	GND	DQM 5	CS2#	GND	MAB 11	DQS 4#	GND	MD32	MAA 10	GND	MECC 2	MECC 4	GND	MAB 3	MD31	GND	DQS 3#	MD24	GND	MD19	DQS 2#	GND	MD11	DQM 1	GND	MD12			
AJ	DQM 6	MD53	MD47	MD46	DQS 5#	MD44	MAA 11	MD35	DQM 4	MD37	MAB 12	MAB 0	MECC 6	DQM 8	MECC 5	MAB 2	MAA 2	MAB 4	MD26	DQM 3	MD28	MAA 14	MD23	DQM 2	MD16	MD20	MD14	DQS 1#	MD13			

Table 1. Pin List (Numerical Order)

Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name
A01	– NC	C25	IO HDB11#	G28	IO HDS0	R26	IO HA05	AD02	IO MD62	AG09	IO MD34
A02	AI GCOMPNO	C26	IO HD26	G29	IO HDS0#	R27	IO HA04	AD03	IO DQS7# / CKE7	AG10	IO MD33
A03	P GNDQ	C27	IO HD25	H01	IO GD24	R28	IO HA11	AD04	O DQM7 / CKE7	AG11	IO MD36
A04	P VCCQ	C28	IO HD20	H03	IO GD25	R29	IO HA06	AD05	IO MD63	AG12	O MAA12
A05	– NC	C29	IO HD31	H04	IO GD28	T01	IO GD6	AD07 P MEMVREF		AG13	IO MECC3 / CKE3
A06	– NC	D01	I SBS#	H05	I GRBF#	T02	IO GD7	AD08	– NC	AG14	IO DQS8#
A07	– NC	D02	I SBS	H25	IO HD05	T03	IO GD4	AD12 P MEMVREF		AG15	O MAB01
A08	– NC	D03	I SBA4	H26	IO HD15	T04	IO GDS0	AD15 P GNDMDLL		AG16	O SRASA#
A09	– NC	D04	I SBA3	H29	IO HD10	T05	IO GDS0#	AD16	O SCASB#	AG17	O MAA03
A10	– NC	D06	– NC	J01	IO GD23	T25	IO HAS0#	AD17	O SWEB#	AG18	IO MD27
A11	– NC	D07	– NC	J02	IO GDS1#	T27	IO HA09	AD18 P MEMVREF		AG19	O MAB06
A12	– NC	D08	– NC	J03	IO GDS1	T28	IO HA15	AD19	O SRASB#	AG20	IO MD29
A13	– NC	D09	– NC	J05	O ST2	T29	IO HA08	AD23 P MEMVREF		AG21	O MAB14
A14	IO HD61	D10	– NC	J25	I HITM#	U01	IO GD2	AD24 P VCCMCK		AG22	O MAA08
A15	IO HD58	D11	– NC	J26	IO HD06	U03	IO GD5	AD25	I MCLKF	AG23	IO MD22
A16	IO HD56	D12	– NC	J27	IO HD02	U04	IO GPAR	AD26	IO MD02	AG24	IO MD21
A17	IO HD62	D13	– NC	J28	IO HD00	U05	I GCLK	AD27	IO MD01	AG25	IO MD10
A18	IO HD48	D14	IO HD60	J29	IO HD08	U26	IO HA16	AD28 IO MD05		AG26	IO MD15
A19	IO HD47	D16	IO HDB13#	K01	IO GD21	U28	IO HA12	AD29 IO MD04		AG27	IO MD09
A20	IO HD44	D17	IO HD54	K02	IO GD19	U29	IO HA13	AE01	IO MD57	AG28	IO MD08
A21	IO HD35	D20	IO HD52	K03	IO GD20	V01	IO GD3	AE02	IO MD61	AG29	IO MD03
A22	IO HD40	D22	IO HD37	K04	IO GD22	V02	IO GD0	AE03	IO MD56	AH01	IO DQS6# / CKE6
A23	IO HD32	D23	IO HD30	K05	IO GBE3#	V03	IO GD1	AE05	O CS6#	AH03	IO MD48
A24	IO HD36	D25	IO HD21	K25	IO DBSY#	V05	IO VBE#	AE06	O CS7#	AH05	O DQM5 / CKE5
A25	IO HD16	D27	IO HD17	K27	IO RS2#	V24 P HAVREF		AE07	IO MD41	AH06	O CS2#
A26	IO HD18	D28	IO HD24	K28	IO RS0#	V25	IO HA10	AE08	– NC	AH08	O MAB11
A27	IO HDS1	D29	IO HD13	K29	IO RS1#	V26	IO HA14	AE09	O CS0#	AH09	IO DQS4# / CKE4
A28	IO HD22	E01	I SBA5	L01	IO GD18	V27	IO HA19	AE10	O SCASA#	AH11	IO MD32
A29	IO HD27	E03	I SBA6	L03	IO GD17	V28	IO HA18	AE11	O MAB10	AH12	O MAA10
B01	O GGNT#	E04	I SBA2	L04	IO GFRM#	V29	IO HA17	AE12	O CS4#	AH14	IO MECC2 / CKE2
B03	AI GCOMPNI	E05	O ST0	L05	I GWBF#	W01	IO VAD3	AE13	IO MECC7 / CKE7	AH15	IO MECC4 / CKE4
B05	– NC	E06	– NC	L24 P GTLVREF		W02	IO VAD5	AE14	O SWEA#	AH17	O MAB03
B06	– NC	E07	– NC	L25	I HLOCK#	W03	IO VAD1	AE15 P VCCMDLL		AH18	IO MD31
B07	– NC	E08	– NC	L26	O BREQ#	W05	IO VAD0	AE16	O MAA01	AH20	IO DQS3# / CKE3
B08	– NC	E09	– NC	L27	IO HIT#	W06 P VCCAGP		AE20	O MAA06	AH21	IO MD24
B09	– NC	E10	– NC	L29	IO BPRI#	W25	I TESTIN#	AE21	O MAA05	AH23	IO MD19
B10	– NC	E11	– NC	M01	IO GIRDY#	W27	IO HA25	AE22	O MAA07	AH24	IO DQS2# / CKE2
B11	– NC	E12	– NC	M02	IO GBE2#	W28	IO HA22	AE23	O MAB08	AH26	IO MD11
B12	– NC	E13	– NC	M03	IO GD16	W29	IO HA24	AE24	O MAB07	AH27	O DQM1 / CKE1
B13	– NC	E14	O CPURST#	M05	– NC	Y01	I UPCMD	AE25	O MAA13	AH29	IO MD12
B14	IO HD63	E15	IO HD57	M24 P GNDHCK		Y03	I UPSTB#	AE26	O MAB13	AJ01	O DQM6 / CKE6
B15	IO HD55	E17	IO HD53	M25	I HCLK#	Y05 P VLVREF		AE27	IO MD06	AJ02	IO MD53
B17	IO HDS3#	E18	IO HD52	M26	IO HTRDY#	Y26	IO HA30	AE28	O DQM0 / CKE0	AJ03	IO MD47
B18	IO HD49	E19 P GNDTT		M27	IO DEFER#	Y27	IO HAS1#	AE29	IO DQS0# / CKE0	AJ04	IO MD46
B19	IO HD46	E20	IO HDS2#	M28	IO DRDY#	Y29	IO HA29	AF01	IO MD51	AJ05	IO DQS5# / CKE5
B20	IO HD45	E21	IO HD42	M29	IO BNR#	AA01	O DNSTB	AF03	IO MD60	AJ06	IO MD44
B21	IO HD43	E22	IO HD34	N01	IO GD14	AA02	O DNCMD	AF04	IO MD54	AJ07	O MAA11
B22	IO HDB12#	E27	IO HD12	N02	IO GD15	AA03	O DNSTB#	AF05	IO MD43	AJ08	IO MD35
B23	IO HD39	E28	IO HD04	N03	IO GBE1#	AA04	I UPSTB	AF06	IO MD45	AJ09	O DQM4 / CKE4
B24	IO HD33	E29	IO HD07	N04	IO GDEVSEL#	AA05	IO VAD4	AF08	O CS1#	AJ10	IO MD37
B25	IO HD19	F01	IO GD31	N05	IO GD13	AA25	IO HA23	AF09	IO MD38	AJ11	O MAB12
B26	IO HD29	F02	– NC	N24 P VCCHCK		AA26	IO HA26	AF11	O CS5#	AJ12	O MAB00
B27	IO HDS1#	F03	I SBA7	N25	I HCLK	AA27	IO HA21	AF12	O MAA00	AJ13	IO MECC6 / CKE6
B29	IO HD23	F05	O ST1	N27	IO HREQ#	AA28	IO HA20	AF14	IO MECC1 / CKE1	AJ14	O DQM8
C01	I GREQ#	F16 P HDVREF		N28	IO HA07	AA29	IO HA28	AF15	IO MECC0 / CKE0	AJ15	IO MECC5 / CKE5
C02	I SBA1	F19 P HDVREF		N29	IO HA03	AB01	IO VAD6	AF17	O MAA04	AJ16	O MAB02
C03	I SBA0	F22 P HDVREF		P01	IO GD10	AB02	IO VAD7	AF18	IO MD30	AJ17	O MAA02
C05	– NC	F24 P HDVREF		P03	IO GD11	AB03	IO VAD2	AF20	IO MD25	AJ18	O MAB04
C06	– NC	F25	AI HRCOMP	P04	IO GD12	AB04	AI VDCOMP	AF21	O MAB05	AJ19	IO MD26
C07	– NC	F26	IO HD03	P05	IO GTRDY#	AB05 P VSUS25		AF23	IO MD18	AJ20	O DQM3 / CKE3
C08	– NC	F27	IO HD09	P24 P GNDTT		AB27	IO HA33	AF24	IO MD17	AJ21	IO MD28
C09	– NC	F28	IO HD11	P25	IO ADS#	AB28	IO HA31	AF26	O MAA09	AJ22	O MAA14
C10	– NC	F29	IO HD01	P26	IO HREQ4#	AB29	IO HA27	AF27	O MAB09	AJ23	IO MD23
C12	– NC	G01	IO GD26	P27	IO HREQ1#	AC01	I PWROK	AF29	IO MD07	AJ24	O DQM2 / CKE2
C13	– NC	G02	IO GD27	P29	IO HREQ3#	AC03	I RESET#	AG01	IO MD55	AJ25	IO MD16
C15	IO HD59	G03	IO GD29	R01	IO GBE0#	AC04	I SUSST#	AG02	IO MD50	AJ26	IO MD20
C17	IO HDS3	G04	IO GD30	R02	IO GD9	AC05	IO MD59	AG03	IO MD52	AJ27	IO MD14
C18	IO HD51	G05	I GPIPE#	R03	IO GD8	AC24 P GNDMCK		AG04	IO MD49	AJ28	IO DQS1# / CKE1
C19	IO HD50	G06 P AGPVREF		R05	IO GSTOP#	AC25	O MCLK	AG05	IO MD42	AJ29	IO MD13
C20	IO HD41	G24 P HCMPVREF		R06 P AGPVREF		AC27	IO HA32	AG06	IO MD40		
C23	IO HD38	G25	IO HD14	R24 P HAVREF		AC29	IO MD00	AG07	O CS3#		
C24	IO HD28	G27	IO HDB10#	R25	IO HREQ0#	AD01	IO MD58	AG08	IO MD39		

VCC25 Pins (26 pins): F9-11,14-15,20-21, H6,24, J6,24, N6, P6, W6,24, Y6,24, AA6, AD9-11,13-14,20-22

VCCMEM Pins (26 pins): V20, W10,20, Y10-20, AA9-20

VCCAGP Pins (19 pins): K6,9, L6,9-10, M6,9-10, N9-10, P9-10, R9-10, T6,9-10, U6, V6

VCCVL (4 pins): U9-10, V9-10, W9, Y9

VTT Pins (25 pins): E16, E23, F17-18,23, K14-20,24, L20, M20, N20, P20, R20,T20,24, U20,24, Y25, AA24, AB24

GND Pins (133 pins): B2,4,16,28, C4,11,14,16,21-22, D5,15,18-19,21,24,26, E2,24-26, F4,6-8,12-13, G26, H2,27-28, J4, K10,26, L2,28, M4,12-18, N12-18,26, P2,12-18,28, R4,12-18, T12-18,26, U2,12-18,25,27, V4,12-18, W4,26, Y2,4,28, AB6,25-26, AC2,6,26,28, AD6, AE4,17-19, AF2,7,10,13,16,19,22,25,28, AH2,4,7,10,13,16,19,22,25,28

Table 2. Pin List (Alphabetical Order)

Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name
P25	IO ADS#	G01	IO GD26	J26	IO HD06	F22	P HDVREF	AJ21	IO MD28	C10	– NC
G06	P AGPVREF	G02	IO GD27	E29	IO HD07	F24	P HDVREF	AG20	IO MD29	C12	– NC
R06	P AGPVREF	H04	IO GD28	J29	IO HD08	L27	IO HIT#	AF18	IO MD30	C13	– NC
M29	IO BNR#	G03	IO GD29	F27	IO HD09	J25	I HITM#	AH18	IO MD31	D06	– NC
L29	IO BPRI#	G04	IO GD30	H29	IO HD10	L25	I HLOCK#	AH11	IO MD32	D07	– NC
L26	IO BREQ#	F01	IO GD31	F28	IO HD11	F25	AI HRCOMP	AG10	IO MD33	D08	– NC
E14	O CPURST#	T04	IO GDS0	E27	IO HD12	R25	IO HREQ0#	AG09	IO MD34	D09	– NC
AE09	O CS0#	T05	IO GDS0#	D29	IO HD13	P27	IO HREQ1#	AJ08	IO MD35	D10	– NC
AF08	O CS1#	J03	IO GDS1	G25	IO HD14	N27	IO HREQ2#	AG11	IO MD36	D11	– NC
AH06	O CS2#	J02	IO GDS1#	H26	IO HD15	P29	IO HREQ3#	AJ10	IO MD37	D12	– NC
AG07	O CS3#	N04	IO GDEVSEL#	A25	IO HD16	P26	IO HREQ4#	AF09	IO MD38	D13	– NC
AE12	O CS4#	L04	IO GFRM#	D27	IO HD17	M26	IO HTRDY#	AG08	IO MD39	E06	– NC
AF11	O CS5#	B01	O GGNT#	A26	IO HD18	AF12	O MAA00	AG06	IO MD40	E07	– NC
AE05	O CS6#	M01	IO GIRDY#	B25	IO HD19	AE16	O MAA01	AE07	IO MD41	E08	– NC
AE06	O CS7#	M24	P GNDHCK	C28	IO HD20	AJ17	O MAA02	AG05	IO MD42	E09	– NC
K25	IO DBSY#	AC24	P GNDMCK	D25	IO HD21	AG17	O MAA03	AF05	IO MD43	E10	– NC
M27	IO DEFER#	AD15	P GNDMDLL	A28	IO HD22	AF17	O MAA04	AJ06	IO MD44	E11	– NC
AA02	O DNCMD	A03	P GNDQQ	B29	IO HD23	AE21	O MAA05	AF06	IO MD45	E12	– NC
AA01	O DNSTB	E19	P GNDTT	D28	IO HD24	AE20	O MAA06	AJ04	IO MD46	E13	– NC
AA03	O DNSTB#	P24	P GNDTT	C27	IO HD25	AE22	O MAA07	AJ03	IO MD47	F02	– NC
AE28	O DQM0 / CKE0	U04	IO GPAR	C26	IO HD26	AG22	O MAA08	AH03	IO MD48	M05	– NC
AH27	O DQM1 / CKE1	G05	I GRPPE#	A29	IO HD27	AF26	O MAA09	AG04	IO MD49	AD08	– NC
AJ24	O DQM2 / CKE2	H05	I GRBF#	C24	IO HD28	AH12	O MAA10	AG02	IO MD50	AE08	– NC
AJ20	O DQM3 / CKE3	C01	I GREQ#	B26	IO HD29	AJ07	O MAA11	AF01	IO MD51	AC01	I PWROK
AJ09	O DQM4 / CKE4	R05	IO GSTOP#	D23	IO HD30	AG12	O MAA12	AG03	IO MD52	AC03	I RESET#
AH05	O DQM5 / CKE5	L24	P GTLVREF	C29	IO HD31	AE25	O MAA13	AJ02	IO MD53	K28	IO RS0#
AJ01	O DQM6 / CKE6	P05	IO GTRDY#	A23	IO HD32	AJ22	O MAA14	AF04	IO MD54	K29	IO RS1#
AD04	O DQM7 / CKE7	L05	I GWBF#	B24	IO HD33	AJ12	O MAB00	AG01	IO MD55	K27	IO RS2#
AJ14	O DQM8	N29	IO HA03	E22	IO HD34	AG15	O MAB01	AE03	IO MD56	C03	I SBA0
AE29	IO DQS0# / CKE0	R27	IO HA04	A21	IO HD35	AJ16	O MAB02	AE01	IO MD57	C02	I SBA1
AJ28	IO DQS1# / CKE1	R26	IO HA05	A24	IO HD36	AH17	O MAB03	AD01	IO MD58	E04	I SBA2
AH24	IO DQS2# / CKE2	R29	IO HA06	D22	IO HD37	AJ18	O MAB04	AC05	IO MD59	D04	I SBA3
AH20	IO DQS3# / CKE3	N28	IO HA07	C23	IO HD38	AF21	O MAB05	AF03	IO MD60	D03	I SBA4
AH09	IO DQS4# / CKE4	T29	IO HA08	B23	IO HD39	AG19	O MAB06	AE02	IO MD61	E01	I SBA5
AJ05	IO DQS5# / CKE5	T27	IO HA09	A22	IO HD40	AE24	O MAB07	AD02	IO MD62	E03	I SBA6
AH01	IO DQS6# / CKE6	V25	IO HA10	C20	IO HD41	AE23	O MAB08	AD05	IO MD63	F03	I SBA7
AD03	IO DQS7# / CKE7	R28	IO HA11	E21	IO HD42	AF27	O MAB09	AF15	IO MECC0 / CKE0	D02	I SBS
AG14	IO DQS8#	U28	IO HA12	B21	IO HD43	AE11	O MAB10	AF14	IO MECC1 / CKE1	D01	I SBS#
M28	IO DRDY#	U29	IO HA13	A20	IO HD44	AH08	O MAB11	AH14	IO MECC2 / CKE2	AE10	O SCASA#
R01	IO GBE0#	V26	IO HA14	B20	IO HD45	AJ11	O MAB12	AG13	IO MECC3 / CKE3	AD16	O SCASB#
N03	IO GBE1#	T28	IO HA15	B19	IO HD46	AE26	O MAB13	AH15	IO MECC4 / CKE4	AG16	O SRASA#
M02	IO GBE2#	U26	IO HA16	A19	IO HD47	AG21	O MAB14	AJ15	IO MECC5 / CKE5	AD19	O SRASB#
K05	IO GBE3#	V29	IO HA17	A18	IO HD48	AC25	O MCLK	AJ13	IO MECC6 / CKE6	E05	O ST0
U05	I GCLK	V28	IO HA18	B18	IO HD49	AD25	I MCLKF	AE13	IO MECC7 / CKE7	F05	O ST1
A02	AI GCOMPNO	V27	IO HA19	C19	IO HD50	AC29	IO MD00	AD07	P MEMVREF	J05	O ST2
B03	AI GCOMPNI	AA28	IO HA20	C18	IO HD51	AD27	IO MD01	AD12	P MEMVREF	AC04	I SUSST#
V02	IO GD0	AA27	IO HA21	E18	IO HD52	AD26	IO MD02	AD18	P MEMVREF	AE14	O SWEA#
V03	IO GD1	W28	IO HA22	E17	IO HD53	AG29	IO MD03	AD23	P MEMVREF	AD17	O SWEB#
U01	IO GD2	AA25	IO HA23	D17	IO HD54	AD29	IO MD04	A01	– NC	W25	I TESTIN#
V01	IO GD3	W29	IO HA24	B15	IO HD55	AD28	IO MD05	A05	– NC	Y01	I UPICMD
T03	IO GD4	W27	IO HA25	A16	IO HD56	AE27	IO MD06	A06	– NC	AA04	I UPSTB
U03	IO GD5	AA26	IO HA26	E15	IO HD57	AF29	IO MD07	A07	– NC	Y03	I UPSTB#
T01	IO GD6	AB29	IO HA27	A15	IO HD58	AG28	IO MD08	A08	– NC	W05	IO VAD0
TA02	IO GD7	AA29	IO HA28	C15	IO HD59	AG27	IO MD09	A09	– NC	W03	IO VAD1
R03	IO GD8	Y29	IO HA29	D14	IO HD60	AG25	IO MD10	A10	– NC	AB03	IO VAD2
R02	IO GD9	Y26	IO HA30	A14	IO HD61	AH26	IO MD11	A11	– NC	W01	IO VAD3
P01	IO GD10	AB28	IO HA31	A17	IO HD62	AH29	IO MD12	A12	– NC	AA05	IO VAD4
P03	IO GD11	AC27	IO HA32	B14	IO HD63	AJ29	IO MD13	A13	– NC	W02	IO VAD5
P04	IO GD12	AB27	IO HA33	G27	IO HDBI0#	AJ27	IO MD14	B05	– NC	AB01	IO VAD6
N05	IO GD13	T25	IO HAS0#	C25	IO HDBI1#	AG26	IO MD15	B06	– NC	AB02	IO VAD7
N01	IO GD14	Y27	IO HAS1#	B22	IO HDBI2#	AJ25	IO MD16	B07	– NC	V05	IO VBE#
N02	IO GD15	R24	P HAVREF	D16	IO HDBI3#	AF24	IO MD17	B08	– NC	N24	P VCCHCK
M03	IO GD16	V24	P HAVREF	G28	IO HDS0	AF23	IO MD18	B09	– NC	AD24	P VCCMCK
L03	IO GD17	N25	I HCLK	G29	IO HDS0#	AH23	IO MD19	B10	– NC	AE15	P VCCMDLL
L01	IO GD18	M25	I HCLK#	A27	IO HDS1	AJ26	IO MD20	B11	– NC	A04	P VCCQQ
K02	IO GD19	G24	P HCMPVREF	B27	IO HDS1#	AG24	IO MD21	B12	– NC	AB04	AI VLCOMP
K03	IO GD20	J28	IO HD00	D20	IO HDS2	AG23	IO MD22	B13	– NC	Y05	P VLVREF
K01	IO GD21	F29	IO HD01	E20	IO HDS2#	AJ23	IO MD23	C05	– NC	AB05	P VSUS25
K04	IO GD22	J27	IO HD02	C17	IO HDS3	AH21	IO MD24	C06	– NC		
J01	IO GD23	F26	IO HD03	F17	IO HDS3#	AF20	IO MD25	C07	– NC		
H01	IO GD24	E28	IO HD04	F16	P HDVREF	AJ19	IO MD26	C08	– NC		
H03	IO GD25	H25	IO HD05	F19	P HDVREF	AG18	IO MD27	C09	– NC		

VCC25 Pins (26 pins): F9-11,14-15,20-21, H6,24, J6,24, N6, P6, W6,24, Y6,24, AA6, AD9-11,13-14,20-22

VCCMEM Pins (26 pins): V20, W10,20, Y10-20, AA9-20

VCCAGP Pins (19 pins): K6,9, L6,9-10, M6,9-10, N9-10, P9-10, R9-10, T6,9-10, U6, V6

VCCVL (4 pins): U9-10, V9-10, W9, Y9

VTT Pins (25 pins): E16, E23, F17-18,23, K14-20,24, L20, M20, N20, P20, R20,T20,24, U20,24, Y25, AA24, AB24

GND Pins (133 pins): B2,4,16,28, C4,11,14,16,21-22, D5,15,18-19,21,24,26, E2,24-26, F4,6-8,12-13, G26, H2,27-28, J4, K10,26, L2,28, M4,12-18, N12-18,26, P2,12-18,28, R4,12-18, T12-18,26, U2,12-18,25,27, V4,12-18, W4,26, Y2,4,28, AB6,25-26, AC2,6,26,28, AD6, AE4,17-19, AF2,7,10,13,16,19,22,25,28, AH2,4,7,10,13,16,19,22,25,28

PIN DESCRIPTIONS

Table 3. Pin Descriptions

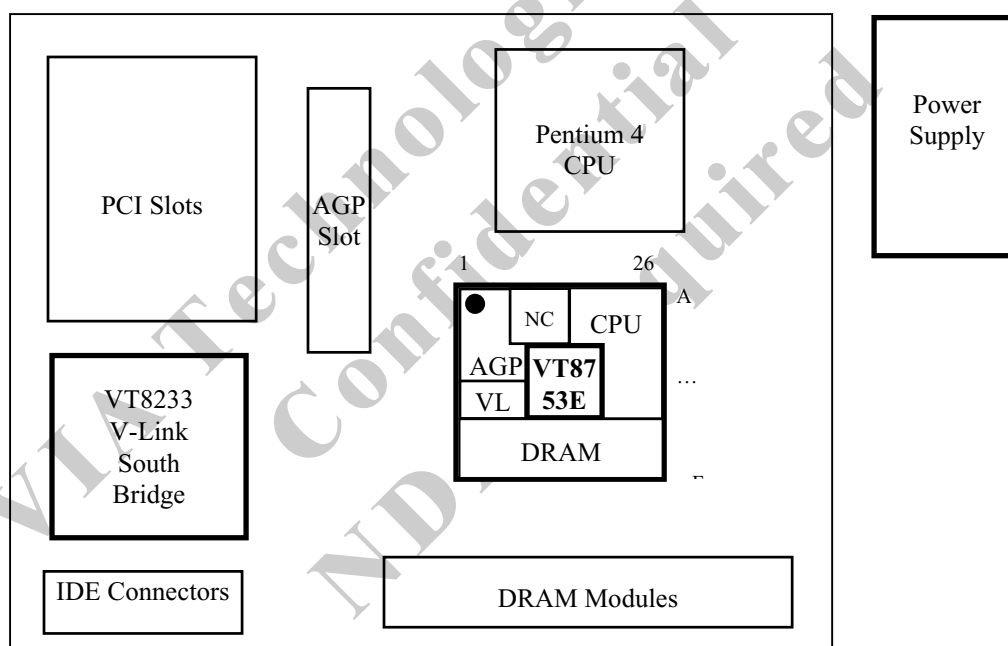
CPU Interface																							
<u>Signal Name</u>	<u>Pin #</u>	<u>I/O</u>	<u>Signal Description</u>																				
HA[33:3]#	(see pinout tables)	IO	Host CPU Address Bus. Connect to the address bus of the host CPU. Inputs during CPU cycles and driven by the VT8753E during cache snooping operations. HA[33:32] are reserved for future use in supporting up to 16 Gbytes of real memory.																				
HAS[1:0]#	Y27, T25	IO	Host CPU Address Strobe. Source synchronous strobes used to transfer HA[31:3]# and HREQ[4:0]# at a 2x transfer rate. HAS1# is the strobe for HA[31:17]# and HAS0# is the strobe for HA[16:3] and HREQ[4:0]#.																				
HD[63:0]#	(see pinout tables)	IO	Host CPU Data. These signals are connected to the CPU data bus.																				
HDBI[3:0]#	D16, B22, C25, G27	IO	Host CPU Dynamic Bus Inversion. Driven along with HD[63:0]# to indicate if the associated signals are inverted or not. Used to limit the number of simultaneously switching signals to 8 for the associated 16-bit data pin group (HDBI3# for HD[63:48]#, HDBI2# for HD[47:32]#, HDBI1# for HD[31:16]#, and HDBI0# for HD[15:0]#). HDBIn# is asserted such that the number of data bits driven low for the corresponding group does not exceed 8.																				
HDS[3:0] HDS[3:0]#	C17, D20, A27, G28 B17, E20, B27, G29	IO	Host CPU Differential Data Strobes. Source synchronous strobes used to transfer HD[63:0]# and HDBI[3:0]# at a 4x transfer rate. HDS3 / HDS3# are the strobes for HD[63:48]# and HDBI3#; HDS2 / HDS2# are the strobes for HD[47:32]# and HDBI2#; HDS1 / HDS1# are the strobes for HD[31:16]# and HDBI1#; and HDS0 / HDS0# are the strobes for HD[15:0]# and HDBI0#.																				
ADS#	P25	IO	Address Strobe. The CPU asserts ADS# in T1 of the CPU bus cycle.																				
DBSY#	K25	IO	Data Bus Busy. Used by the data bus owner to hold the data bus for transfers requiring more than one cycle.																				
DRDY#	M28	IO	Data Ready. Asserted for each cycle that data is transferred.																				
HIT#	L27	IO	Hit. Indicates that a caching agent holds an unmodified version of the requested line. Also driven in conjunction with HITM# by the target to extend the snoop window.																				
HITM#	J25	I	Hit Modified. Asserted by the CPU to indicate that the address is modified in the L1 cache and needs to be written back.																				
HLOCK#	L25	I	Host Lock. All CPU cycles sampled with the assertion of HLOCK# and ADS# until the negation of HLOCK# must be atomic.																				
HREQ[4:0]#	P26, P29, N27, P27, R25	IO	Request Command. Asserted during both clocks of the request phase. In the first clock, the signals define the transaction type to a level of detail that is sufficient to begin a snoop request. In the second clock, the signals carry additional information to define the complete transaction type.																				
HTRDY#	M26	IO	Host Target Ready. Indicates that the target of the processor transaction is able to enter the data transfer phase.																				
RS[2:0]#	K27, K29, K28	IO	Response Signals. Indicates the type of response per the table below: <table> <tr> <th><u>RS[2:0]#</u></th><th><u>Response type</u></th><th><u>RS[2:0]#</u></th><th><u>Response type</u></th></tr> <tr> <td>000</td><td>Idle State</td><td>100</td><td>Hard Failure</td></tr> <tr> <td>001</td><td>Retry Response</td><td>101</td><td>Normal Without Data</td></tr> <tr> <td>010</td><td>Defer Response</td><td>110</td><td>Implicit Writeback</td></tr> <tr> <td>011</td><td>Reserved</td><td>111</td><td>Normal With Data</td></tr> </table>	<u>RS[2:0]#</u>	<u>Response type</u>	<u>RS[2:0]#</u>	<u>Response type</u>	000	Idle State	100	Hard Failure	001	Retry Response	101	Normal Without Data	010	Defer Response	110	Implicit Writeback	011	Reserved	111	Normal With Data
<u>RS[2:0]#</u>	<u>Response type</u>	<u>RS[2:0]#</u>	<u>Response type</u>																				
000	Idle State	100	Hard Failure																				
001	Retry Response	101	Normal Without Data																				
010	Defer Response	110	Implicit Writeback																				
011	Reserved	111	Normal With Data																				

Note: Clocking of the CPU interface is performed with HCLK and HCLK#.

Note: Internal pullup resistors are provided on all AGTL+ interface pins. If the CPU does not have internal pullups, these north bridge internal pullups may be enabled to allow the interface to meet AGTL+ bus interface specifications (see VAD3 strap).

CPU Interface (continued)			
Signal Name	Pin #	I/O	Signal Description
BREQ#	L26	O	Bus Request. Bus request output to CPU.
BPRI#	L29	IO	Priority Agent Bus Request. The owner of this signal will always be the next bus owner. This signal has priority over symmetric bus requests and causes the current symmetric owner to stop issuing new transactions unless the HLOCK# signal is asserted. The VT8753E drives this signal to gain control of the processor bus.
BNR#	M29	IO	Block Next Request. Used to block the current request bus owner from issuing new requests. This signal is used to dynamically control the processor bus pipeline depth.
DEFER#	M27	IO	Defer. The VT8753E uses a dynamic deferring policy to optimize system performance. The VT8753E also uses the DEFER# signal to indicate a processor retry response.
CPURST#	E14	O	CPU Reset. Reset output to CPU. External pullup and filter capacitor to ground should be provided per CPU manufacturer's recommendations.

The pinouts were defined assuming the ATX PCB layout model shown below (and general pin layout shown) as a guide for PCB component placement. Other PCB layouts (AT, LPX, and NLX) were also considered and can typically follow the same general component placement.



DRAM Interface			
<u>Signal Name</u>	<u>Pin #</u>	<u>I/O</u>	<u>Signal Description</u>
MD[63:0]	(see pin lists)	IO	Memory Data. These signals are connected to the DRAM data bus. Output drive strength may be set by Device 0 Rx6D[1-0].
MECC[7:0] / CKE[7:0]	AE13, AJ13, AJ15, AH15, AG13, AH14, AF14, AF15	IO	DRAM ECC or EC Data: when ECC is enabled. Clock Enables: For each DRAM bank for powering down the SDRAMs in notebook applications. Also used in desktop systems for clock control to reduce power usage and for reducing heat/temperature in high-speed memory systems.
MAA[14:0]	AJ22, AE25, AG12, AJ7, AH12, AF26, AG22, AE22, AE20, AE21, AF17, AG17, AJ17, AE16, AF12	O	Memory Address A. DRAM address lines (two sets for better drive). Output drive strength may be set by Device 0 Rx6C[7-6].
MAB[14:0]	AG21, AE26, AJ11, AH8, AE11, AF27, AE23, AE24, AG19, AF21, AJ18, AH17, AJ16, AG15, AJ12	O	Memory Address B. DRAM address lines (two sets for better drive). Output drive strength may be set by Device 0 Rx6C[5-4].
SRASA#, SCASA#, SWEA#	AG16, AE10, AE14	O	Row Address, Column Address and Write Enable Command Indicator Set A. (two sets for better drive). Output drive strength may be set by Device 0 Rx6C[7-6].
SRASB#, SCASB#, SWEB#	AD19, AD16, AD17	O	Row Address, Column Address and Write Enable Command Indicator Set B. (two sets for better drive). Output drive strength may be set by Device 0 Rx6C[5-4].
CS[7:0]#	AE6, AE5, AF11, AE12, AG7, AH6, AF8, AE9	O	Chip Select. Chip select of each bank. Output drive strength may be set by Device 0 Rx6D[3-2].
DQM[8], DQM[7:0] / CKE[7:0]	AJ14, AD4, AJ1, AH5, AJ9, AJ20, AJ24, AH27, AE28	O	Data Mask. Data mask of each byte lane plus DQM8 for ECC byte. Output drive strength may be set by Device 0 Rx6D[5-4].
DQS[8], DQS[7:0]# / CKE[7:0]	AG14, AD3, AH1, AJ5, AH9, AH20, AH24, AJ28, AE29	IO	DDR Data Strobe. Data strobe of each byte lane plus DQS8# for ECC byte. Output drive strength may be set by Device 0 Rx6C[3-2].
CKE[7:0] / MECC[7:0] -or- CKE[7:0] / DQM[7:0] -or- CKE[7:0] / DQS[7:0]#	(see above)	O	Clock Enables. Clock enables for each DRAM bank for powering down the SDRAM or clock control for reducing power usage and for reducing heat / temperature in high-speed memory systems. See Device 0 Rx78[0] for CKE function enable.

AGP Bus Interface			
Signal Name	Pin #	I/O	Signal Description
GD[31:0]	(see pin list)	IO	Address / Data Bus. Address is driven with GDS assertion for AGP-style transfers and with GFRM# assertion for PCI-style transfers.
GBE[3:0]#	K5, M2, N3, R1	IO	Command / Byte Enable. AGP: These pins provide command information (different commands than for PCI) driven by the master (graphics controller) when requests are being enqueued using GPIPE#. These pins provide valid byte information during AGP write transactions and are driven by the master. The target (this chip) drives these lines to “0000” during the return of AGP read data. PCI: Commands are driven with GFRM# assertion. Byte enables corresponding to supplied or requested data are driven on following clocks.
GPAR	U4	IO	AGP Parity. A single parity bit is provided over GD[31:0] and GBE[3:0].
GDS0, GDS0#	T4, T5	IO	Bus Strobe 0. Source synchronous strobes for GD[15:0] (the agent that is providing the data drives these signals). GDS0 provides timing for 2x data transfer mode; GDS0 and GDS0# provide timing for 4x transfer mode.
GDS1, GDS1#	J3, J2	IO	Bus Strobe 1. Source synchronous strobes for GD[31:16] (i.e., the agent that is providing the data drives these signals). GDS1 provides timing for 2x data transfer mode; GDS1 and GDS1# provide timing for 4x transfer mode.
GFRM#	L4	IO	Frame. Assertion indicates the address phase of a PCI transfer. Negation indicates that one more data transfer is desired by the cycle initiator.
GIRDY#	M1	IO	Initiator Ready. AGP: For write operations, the assertion of this pin indicates that the master is ready to provide all write data for the current transaction. Once this pin is asserted, the master is not allowed to insert wait states. For read operations, the assertion of this pin indicates that the master is ready to transfer a subsequent block of read data. The master is never allowed to insert a wait state during the initial block of a read transaction. However, it may insert wait states after each block transfers. PCI: Asserted when the initiator is ready for data transfer.
GTRDY#	P5	IO	Target Ready. AGP: Indicates that the target is ready to provide read data for the entire transaction (when the transaction can complete within four clocks) or is ready to transfer a (initial or subsequent) block of data when the transfer requires more than four clocks to complete. The target is allowed to insert wait states after each block transfer for both read and write transactions. PCI: Asserted when the target is ready for data transfer.
GSTOP#	R5	IO	Stop (PCI transactions only). Asserted by the target to request the master to stop the current transaction.
GDEVSEL#	N4	IO	Device Select (PCI transactions only). This signal is driven by the VT8753E when a PCI initiator is attempting to access main memory. It is an input when the VT8753E is acting as PCI initiator. Not used for AGP cycles.
GPIPE#	G5	I	Pipelined Request. Asserted by the master (the external graphics controller) to indicate that a full-width request is to be enqueued by the target VT8753E. The master enqueues one request each rising edge of GCLK while GPIPE# is asserted. When GPIPE# is deasserted no new requests are enqueued across the AD bus.

AGP Bus Interface (continued)			
<u>Signal Name</u>	<u>Pin #</u>	<u>I/O</u>	<u>Signal Description</u>
GRBF#	H5	I	Read Buffer Full. Indicates if the master (graphics controller) is ready to accept previously requested low priority read data. When GRBF# is asserted, the VT8753E will not return low priority read data to the graphics controller.
GWBF#	L5	I	Write Buffer Full.
SBA[7:0]	F3, E3, E1, D3, D4, E4, C2, C3	I	SideBand Address. Provides an additional bus to pass address and command information from the master (graphics controller) to the target (VT8753E north bridge logic). These pins are ignored until enabled.
SBS, SBS#	D2, D1	I	Sideband Strobe. Driven by the master to provide timing for SBA[7:0]. SBS is used for AGP 2x while SBS and SBS# are used together for AGP 4x.
ST[2:0]	J5, F5, E5	O	Status (AGP only). Provides information from the arbiter to a master to indicate what it may do. Only valid while GGNT# is asserted. 000 Indicates that previously requested low priority read or flush data is being returned to the master (graphics controller). 001 Indicates that previously requested high priority read data is being returned to the master. 010 Indicates that the master is to provide low priority write data for a previously enqueued write command. 011 Indicates that the master is to provide high priority write data for a previously enqueued write command. 100 Reserved. (arbiter must not issue, may be defined in the future). 101 Reserved. (arbiter must not issue, may be defined in the future). 110 Reserved. (arbiter must not issue, may be defined in the future). 111 Indicates that the master (graphics controller) has been given permission to start a bus transaction. The master may enqueue AGP requests by asserting PIPE# or start a PCI transaction by asserting GFRM#. ST[2:0] are always outputs from the target (north bridge logic) and inputs to the master (graphics controller).
GREQ#	C1	I	Request. Master (graphics controller) request for use of the AGP bus.
GGNT#	B1	O	Grant. Permission is given to the master (graphics controller) to use the AGP bus.

Note: For PCI operation on the AGP bus, the following pins are not required:

- PERR# (parity and error reporting not required on transient data devices such as graphics controllers)
- LOCK# (no lock requirement on AGP)
- IDSEL (internally connected to AD16 on AGP-compliant masters)

Note: Separate system interrupts are not provided for AGP. The AGP connector provides interrupts via PCI bus INTA-B#.

Note: The AGP bus supports only one master directly (REQ[3:0]# and GNT[3:0]# are not provided). External logic is required to implement additional master capability. Note that the arbitration mechanism on the AGP bus is different from the PCI bus.

Note: A separate reset is not required for the AGP bus (RESET# resets both PCI and AGP buses)

Note: Two mechanisms are provided by the AGP bus to enqueue master requests: GPIPE# (to send addresses multiplexed on the AD lines) and the SBA port (to send addresses unmultiplexed). AGP masters implement one or the other or select one at initialization time (they are not allowed to change during runtime). Therefore only one of the two will be used and the signals associated with the other will not be used. Therefore the VT8753E has an internal pullup on GRBF# to maintain it in the de-asserted state in case it is not implemented on the master device.

V-Link Interface																																							
Signal Name	Pin #	I/O	Signal Description																																				
VAD7, VAD6, VAD5, VAD4, VAD3, VAD2, VAD1, VAD0	AB2 AB1 W2 AA5 W1 AB3 W3 W5	IO IO IO IO IO IO IO IO	Address / Data Bus. Also used to pass strap information from the south bridge to the north bridge (the straps are not on the north bridge VAD pins but on the indicated south bridge pin and the information passed to the north bridge at reset time on the VAD pins). <table><thead><tr><th></th><th>Connection</th><th>Register</th><th>SB Pin</th></tr></thead><tbody><tr><td>VAD7 – reserved</td><td>n/a</td><td>n/a</td><td>–</td></tr><tr><td>VAD6 – Auto-Configure</td><td>L=Disable, H=Enable</td><td>Rx54[5]</td><td>SDA2</td></tr><tr><td>VAD5 – AGTL+ Drive Strength 4x</td><td>L=1x, H=4x</td><td></td><td>SDA1</td></tr><tr><td>VAD4 – AGTL+ Drive Strength 2x</td><td>L=1x, H=2x</td><td></td><td>SDA0</td></tr><tr><td>VAD3 – Internal AGTL+ Pullups</td><td>L=Enable, H=Disable</td><td>Rx52[5]</td><td>SA19</td></tr><tr><td>VAD2 – IOQ Depth Msb</td><td>LL=LH=HL=reserved,</td><td>Rx50[7]</td><td>SA18</td></tr><tr><td>VAD1 – IOQ Depth Lsb</td><td>HH=12-level</td><td>Rx50[6]</td><td>SA17</td></tr><tr><td>VAD0 – CPU FSB Frequency</td><td>L=100 MHz, H=133 MHz</td><td>Rx54[6]</td><td>SA16</td></tr></tbody></table>		Connection	Register	SB Pin	VAD7 – reserved	n/a	n/a	–	VAD6 – Auto-Configure	L=Disable, H=Enable	Rx54[5]	SDA2	VAD5 – AGTL+ Drive Strength 4x	L=1x, H=4x		SDA1	VAD4 – AGTL+ Drive Strength 2x	L=1x, H=2x		SDA0	VAD3 – Internal AGTL+ Pullups	L=Enable, H=Disable	Rx52[5]	SA19	VAD2 – IOQ Depth Msb	LL=LH=HL=reserved,	Rx50[7]	SA18	VAD1 – IOQ Depth Lsb	HH=12-level	Rx50[6]	SA17	VAD0 – CPU FSB Frequency	L=100 MHz, H=133 MHz	Rx54[6]	SA16
	Connection	Register	SB Pin																																				
VAD7 – reserved	n/a	n/a	–																																				
VAD6 – Auto-Configure	L=Disable, H=Enable	Rx54[5]	SDA2																																				
VAD5 – AGTL+ Drive Strength 4x	L=1x, H=4x		SDA1																																				
VAD4 – AGTL+ Drive Strength 2x	L=1x, H=2x		SDA0																																				
VAD3 – Internal AGTL+ Pullups	L=Enable, H=Disable	Rx52[5]	SA19																																				
VAD2 – IOQ Depth Msb	LL=LH=HL=reserved,	Rx50[7]	SA18																																				
VAD1 – IOQ Depth Lsb	HH=12-level	Rx50[6]	SA17																																				
VAD0 – CPU FSB Frequency	L=100 MHz, H=133 MHz	Rx54[6]	SA16																																				
VBE#	V5	IO	Byte Enable.																																				
UPCMD	Y1	I	Command from Client-to-Host.																																				
UPSTB	AA4	I	Strobe from Client-to-Host.																																				
UPSTB#	Y3	I	Complement Strobe from Client-to-Host.																																				
DNCMD	AA2	O	Command from Host-to-Client.																																				
DNSTB	AA1	O	Strobe from Host-to-Client.																																				
DNSTB#	AA3	O	Complement Strobe from Host-to-Client.																																				

Clocks, Resets, Power Control, General Purpose I/O, Interrupts and Test			
<u>Signal Name</u>	<u>Pin #</u>	<u>I/O</u>	<u>Signal Description</u>
HCLK	N25	I	Host Clock. This pin receives the host CPU clock (100 / 133 MHz). This clock is used by all P4X266E logic that is in the host CPU domain.
HCLK#	M25	I	Host Clock Complement. Used for Quad Data Transfer on host CPU bus.
MCLK	AC25	O	Memory (SDRAM) Clock. Output from internal clock generator to the external clock buffer.
MCLKF	AD25	I	Memory (SDRAM) Clock Feedback. Input from the external clock buffer.
GCLK	U5	I	Graphics Clock. Clock for AGP bus interface.
RESET#	AC3	I	Reset. Input from the South Bridge chip. When asserted, this signal resets P4X266E and sets all register bits to the default value. The rising edge of this signal is used to sample all power-up strap options
PWROK	AC1	I	Power OK. Connect to South Bridge and Power Good circuitry.
SUSST#	AC4	I	Suspend Status. For implementation of the Suspend-to-DRAM feature. Connect to an external pullup to disable.
TESTIN#	W25	I	Test In. This pin is used for testing and must be left unconnected or tied high on all board designs.
NC	(see pin list)	–	No Connect.

Reference Voltages			
<u>Signal Name</u>	<u>Pin #</u>	<u>I/O</u>	<u>Signal Description</u>
GTLVREF	L24	P	Host CPU Interface AGTL+ Voltage Reference. 2/3 VTT $\pm 2\%$ typically derived using a resistive voltage divider. See P4X266 Design Guide.
HDVREF	F16, F19, F22, F24	P	Host CPU Data Voltage Reference. 2/3 VTT $\pm 2\%$ typically derived using a resistive voltage divider. See P4X266 Design Guide.
HAVREF	R24, V24	P	Host CPU Address Voltage Reference. 2/3 VTT $\pm 2\%$ typically derived using a resistive voltage divider. See P4X266 Design Guide.
HCMPVREF	G24	P	Host CPU Compensation Voltage Reference. 1/3 VTT $\pm 2\%$ typically derived using a resistive voltage divider. See P4X266 Design Guide.
MEMVREF	AD7, AD12, AD18, AD23	P	Memory Voltage Reference. 1/2 VCC25 $\pm 2\%$ typically derived using a resistive voltage divider. See P4X266 Design Guide.
VLVREF	Y5	P	V-Link Voltage Reference. 0.9V derived using a resistive voltage divider consisting of 2K Ω 1% to VCC25 and 1.13K Ω 1% to ground.
AGPVREF	G6, R6	P	AGP Voltage Reference. 0.4 VCCQQ (1.32V) when VCCQQ is 3.3V and 0.5 VCCQQ (0.75V) when VCCQQ is 1.5V. Check the VT8753E Design Guide for additional information.

Compensation			
<u>Signal Name</u>	<u>Pin #</u>	<u>I/O</u>	<u>Signal Description</u>
HRCOMP	F25	AI	Host CPU Compensation. Connect 20.5 Ω 1% resistor to ground. Used for Host CPU interface I/O buffer calibration.
VLCOMP	AB4	AI	Vlink P-Channel Compensation. Connect 70 Ω 1% resistor to ground.
GCOMPNO	A2	AI	AGP N-Channel Compensation 0.
GCOMPNI	B3	AI	AGP N-Channel Compensation 1.

Analog Power / Ground			
<u>Signal Name</u>	<u>Pin #</u>	<u>I/O</u>	<u>Signal Description</u>
VCCHCK	N24	P	Power for Host CPU Clock PLL (2.5V $\pm 5\%$)
GNDHCK	M24	P	Ground for Host CPU Clock Circuitry. Connect to main ground plane through a ferrite bead.
VCCMCK	AD24	P	Power for Memory Clock PLL (2.5V $\pm 5\%$)
GNDMCK	AC24	P	Ground for Memory Clock Circuitry. Connect to main ground plane through a ferrite bead.
VCCMDLL	AE15	P	Power for Memory Strobe DLL (2.5V $\pm 5\%$)
GNDMDLL	AD15	P	Ground for Memory Strobe DLL Circuitry. Connect to main ground plane through a ferrite bead.

Digital Power / Ground			
Signal Name	Pin #	I/O	Signal Description
VTT	E16,23, F17-18,23, K14-20,24, L20, M20, N20, P20, R20, T20,24, U20,24, Y25, AA24, AB24	P	Power for CPU I/O Interface Logic (25 Pins). Voltage is CPU dependent.
GNDTT	E19, P24	P	Ground for CPU I/O Interface Logic (2 Pins).
VCCMEM	V20, W10,20, Y10-20, AA9-20	P	Power for Memory I/O Interface Logic (26 Pins). 2.5 / 3.3V $\pm 5\%$.
VCCVL	U9-10, V9-10, W9, Y9	P	Power for V-Link I/O Interface Logic (6 Pins). 2.5V $\pm 5\%$
VCCAGP	K6,9, L6,9-10, M6,9-10, N9-10, P9-10, R9-10, T6,9-10, U6, V6	P	Power for AGP Bus I/O Interface Logic (19 Pins). 1/5 / 3.3V $\pm 5\%$ (Device 0 RxB2[1] should be set to indicate the voltage).
VCCQQ	A4	P	AGP Quiet Power. Connect to main AGP power (VCCAGP) through a ferrite bead.
GNDQQ	A3	P	Ground for AGP Quiet Power. Connect to main ground plane.
VCC25	F9-11,14-15,20-21, H6,24, J6,24, N6, P6, W6,24, Y6,24, AA6, AD9-11,13-14,20-22	P	Power for Internal Logic (26 Pins). 2.5V $\pm 5\%$
VSUS25	AB5	P	Suspend Power. 2.5V $\pm 5\%$
GND	B2,4,16,28, C4,11,14,16,21-22, D5,15,18-19,21,24,26, E2,24-26, F4,6-8,12-13, G26, H2,27-28, J4, K10,26, L2,28, M4,12-18, N12-18,26, P2,12-18,28, R4,12-18, T12-18,26, U2,12-18,25,27, V4,12-18, W4,26, Y2,4,28, AB6,25-26, AC2,6,26,28, AD6, AE4,17-19, AF2,7,10,13,16,19,22,25,28, AH2,4,7,10,13,16,19,22,25,28	P	Digital Ground (133 Pins)

REGISTERS

Register Overview

The following tables summarize the configuration and I/O registers of the P4X266E. These tables also document the power-on default value (“Default”) and access type (“Acc”) for each register. Access type definitions used are RW (Read/Write), RO (Read/Only), “—” for reserved / used (essentially the same as RO), RWC (or just WC) (Read / Write 1’s to Clear individual bits), and W1 (Write Once then Read / Only after that). Registers indicated as RW may have some read-only bits that always read back a fixed value (usually 0 if unused); registers designated as RWC or WC may have some read-only or read write bits (see individual register descriptions following these tables for details). All offset and default values are shown in hexadecimal unless otherwise indicated.

The graphics registers are described in a separate document.

Table 4. Registers

I/O Ports

Port #	I/O Port	Default	Acc
22	PCI / AGP Arbiter Disable	00	RW
CFB-8	Configuration Address	0000 0000	RW
CFF-C	Configuration Data	0000 0000	RW

P4X266E Device 0 Registers - Host Bridge
Header Registers

Offset	Configuration Space Header	Default	Acc
1-0	Vendor ID	1106	RO
3-2	Device ID	3128	RO
5-4	Command	0006	RW
7-6	Status	0210	WC
8	Revision ID	0n	RO
9	Program Interface	00	RO
A	Sub Class Code	00	RO
B	Base Class Code	06	RO
C	-reserved-	00	—
D	Latency Timer	00	RW
E	Header Type	00	RO
F	Built In Self Test (BIST)	00	RO
13-10	Graphics Aperture Base	0000 0008	RW
14-2B	-reserved-	00	—
2D-2C	Subsystem Vendor ID	0000	W1
2F-2E	Subsystem ID	0000	W1
30-33	-reserved-	00	—
37-34	Capability Pointer	0000 00A0	RO
38-3F	-reserved-	00	—

Device-Specific Registers

Offset	V-Link Control	Default	Acc
40	V-Link Revision ID	00	RO
41	V-Link NB Capability	18	RO
42	V-Link NB Downlink Command	88	RW
44-43	V-Link NB Uplink Status	8280	RW
45	V-Link NB Bus Timer	44	RW
46	V-Link Misc NB Control	00	RW
47	V-Link Control	00	RW
48	V-Link NB/SB Configuration	18	RW
49	V-Link SB Capability	18	RO
4A	V-Link SB Downlink Status	88	RO
4C-4B	V-Link SB Uplink Command	8280	RW
4D	V-Link SB Bus Timer	44	RW
4E	CCA Master High Priority	00	RW
4F	V-Link SB Miscellaneous Control	00	RW

Offset	Host CPU Protocol Control	Default	Acc
50	CPU Interface Request Phase Control	00	RW
51	CPU Interface Basic Control	00	RW
52	CPU Interface Advanced Control	00	RW
53	CPU Interface Arbitration Control	03	RW
54	CPU Frequency	40	RW

Device-Specific Registers (continued)

Offset	DRAM Control	Default	Acc
55	DRAM Control	00	RW
56-57	(see below)		
59-58	MA Map Type	2222	RW
5F-5A	DRAM Row Ending Address:		
5A	Bank 0 Ending (HA[31:24])	01	RW
5B	Bank 1 Ending (HA[31:24])	01	RW
5C	Bank 2 Ending (HA[31:24])	01	RW
5D	Bank 3 Ending (HA[31:24])	01	RW
5E	Bank 4 Ending (HA[31:24])	01	RW
5F	Bank 5 Ending (HA[31:24])	01	RW
56	Bank 6 Ending (HA[31:24])	01	RW
57	Bank 7 Ending (HA[31:24])	01	RW
60	DRAM Type	00	RW
61	ROM Shadow Control C0000-CFFFF	00	RW
62	ROM Shadow Control D0000-DFFFF	00	RW
63	ROM Shadow Control E0000-FFFFF	00	RW
64	DRAM Timing for All Banks	E4	RW
65	DRAM Arbitration Timer	00	RW
66	DRAM Arbitration Control	00	RW
67	DRAM DQS/SDR/MD Read Delay	00	RW
68	DRAM DDR Control	00	RW
69	DRAM Clock Select	00	RW
6A	DRAM Refresh Counter	00	RW
6B	DRAM Arbitration Control	00	RW
6C	DRAM Drive Control 1	00	RW
6D	DRAM Drive Control 2	00	RW
6E	ECC Control	00	RW
6F	ECC Status	00	WC

Offset	PCI Bus Control	Default	Acc
70	PCI Buffer Control	00	RW
71	CPU to PCI Flow Control	48	WC
72	-reserved-	00	—
73	PCI Master Control	00	RW
74	-reserved-	00	—
75	PCI Arbitration 1	00	RW
76	PCI Arbitration 2	00	RW
77-7F	-reserved-	00	—

Device 0 Device-Specific Registers (continued)

Offset	GART/TLB Control	Default	Acc
83-80	GART/TLB Control	0000 0000	RW
84	Graphics Aperture Size	00	RW
85	CPU-to-Memory Write Policy	00	RW
86	CPU-to-Memory Bandwidth Timer	00	RW
87	CPU-to-Memory Bandwidth Limit	00	RW
8B-88	Gr. Aperture TLB Base Register Base	0000 0000	RW
8C-9F	-reserved-	00	—

Offset	AGP Control	Default	Acc
A0	AGP ID	02	RO
A1	AGP Next Item Pointer	C0	RO
A2	AGP Specification Revision	20	RO
A3	-reserved-	00	—
A7-A4	AGP Status	1F00 0201	RO
AB-A8	AGP Command	0000 0000	RW
AC	AGP Control	00	RW
AD	AGP Miscellaneous Control	02	RW
AE	AGP Miscellaneous Control	00	RW
AF	-reserved-	00	—
B0	AGP Compensation Control / Status	8x	RW
B1	AGP Output Drive Strength	63	RW
B2	AGP Pad Drive & Delay Control	08	RW
B3	AGP Strobe Drive Strength	63	RW

Offset	V-Link Control	Default	Acc
B4	V-Link NB Compensation Control	00	RW
B5	V-Link NB Drive Control	00	RW
B6-B7	-reserved-	00	—
B8	V-Link SB Compensation Control	00	RW
B9	V-Link SB Drive Control	00	RW
BA-BD	-reserved-	00	—

Offset	DRAM Interface Control	Default	Acc
BE	MECC Drive Strength	00	RW
BF	MA / SCMD Pad Toggle Reduction	00	RW

Offset	Power Mgt. & Misc. Control	Default	Acc
C0	Power Management Capability	01	RO
C1	Power Management Next Pointer	00	RO
C2	Power Management Capabilities I	02	RO
C3	Power Management Capabilities II	00	RO
C4	Power Management Control/Status	00	RW
C5	Power Management Status	00	RO
C6	PCI-to-PCI Bridge Support Extension	00	RO
C7	Power Management Data	00	RO
C8-CF	-reserved-	00	—

Device 0 Device-Specific Registers (continued)

Offset	ECC Error Control	Default	Acc
D3-D0	ECC Error Address	xx	RO
D4	ECC Error Syndrome Bit	xx	RO
D5-D7	-reserved-	00	—

Offset	AGTL+ I/O Control	Default	Acc
D8	Host Address (2x) Pullup Drive	00	RW
D9	Host Address (2x) Pulldown Drive	00	RW
DA	Host Data (4x) Pullup Drive	00	RW
DB	Host Data (4x) Pulldown Drive	00	RW
DC	AGTL+ Output Delay / Stagger Ctrl	00	RW
DD	AGTL+ I/O Control	00	RW
DE	AGTL+ Compensation Status	00	RW
DF	AGTL+ AutoCompensation Offset	00	RW

Offset	UMA Control	Default	Acc
E0	CPU Direct Access FB Base	00	RW
E1	CPU Direct Access FB Size	00	RW
E2	VGA Arbitration Timer 1	00	RW
E3	VGA Arbitration Timer 2	00	RW

Offset	DRAM Above 4G Control	Default	Acc
E4	Low Top Address Low	00	RW
E5	Low Top Address High	FF	RW
E6	SMM / APIC Decoding	01	RW
E7-EF	-reserved-	00	—

Offset	Test, BIOS Scratch, Miscellaneous	Default	Acc
F0-F2	Reserved (Do Not Program)	00	RW
F3-F4	BIOS Scratch Registers	00	RW
F5-FF	Reserved (Do Not Program)	00	RW

P4X266E Device 1 Registers - PCI-to-PCI Bridge
Header Registers

Offset	Configuration Space Header	Default	Acc
1-0	Vendor ID	1106	RO
3-2	Device ID	B091	RO
5-4	Command	0007	RW
7-6	Status	0230	WC
8	Revision ID	nn	RO
9	Program Interface	00	RO
A	Sub Class Code	04	RO
B	Base Class Code	06	RO
C	-reserved-	00	—
D	Latency Timer	00	RO
E	Header Type	01	RO
F	Built In Self Test (BIST)	00	RO
10-17	-reserved-	00	—
18	Primary Bus Number	00	RW
19	Secondary Bus Number	00	RW
1A	Subordinate Bus Number	00	RW
1B	Secondary Latency Timer	00	RO
1C	I/O Base	F0	RW
1D	I/O Limit	00	RW
1F-1E	Secondary Status	0000	RO
21-20	Memory Base	FFF0	RW
23-22	Memory Limit (Inclusive)	0000	RW
25-24	Prefetchable Memory Base	FFF0	RW
27-26	Prefetchable Memory Limit	0000	RW
28-33	-reserved-	00	—
34	Capability Pointer	80	RO
35-3D	-reserved-	00	—
3F-3E	PCI-to-PCI Bridge Control	00	RW

Device-Specific Registers

Offset	AGP Bus Control	Default	Acc
40	CPU-to-AGP Flow Control 1	00	RW
41	CPU-to-AGP Flow Control 2	08	RW
42	AGP Master Control	00	RW
43	AGP Master Latency Timer	22	RW
44	Reserved (Do Not Program)	00	RW
45	Fast Write Control	72	RW
47-46	PCI-to-PCI Bridge Device ID	0000	RW
48-7F	-reserved-	00	—
80	Capability ID	01	RO
81	Next Pointer	00	RO
82	Power Management Capabilities 1	02	RO
83	Power Management Capabilities 2	00	RO
84	Power Management Control / Status	00	RW
85	Power Management Status	00	RO
86	PCI-PCI Bridge Support Extensions	00	RO
87	Power Management Data	00	RO
88-FF	-reserved-	00	—

Miscellaneous I/O

One I/O port is defined in the P4X266E: Port 22.

Port 22 – PCI / AGP Arbiter DisableRW

- 7-2 Reserved** always reads 0
- 1 AGP Arbiter Disable**
 - 0 Respond to GREQ# signaldefault
 - 1 Do not respond to GREQ# signal
- 0 PCI Arbiter Disable**
 - 0 Respond to all REQ# signalsdefault
 - 1 Do not respond to any REQ# signals, including PREQ#

This port can be enabled for read/write access by setting bit-7 of Device 0 Configuration Register 78.

Configuration Space I/O

All registers in the P4X266E (listed above) are addressed via the following configuration mechanism:

Mechanism #1

These ports respond only to double-word accesses. Byte or word accesses will be passed on unchanged.

Port CFB-CF8 - Configuration Address..... RW

31 Configuration Space Enable

- 0 Disabled..... default
- 1 Convert configuration data port writes to configuration cycles on the PCI bus

30-24 Reservedalways reads 0

23-16 PCI Bus Number

Used to choose a specific PCI bus in the system

15-11 Device Number

Used to choose a specific device in the system (devices 0 and 1 are defined for the P4X266E)

10-8 Function Number

Used to choose a specific function if the selected device supports multiple functions (only function 0 is defined for the P4X266E).

7-2 Register Number (also called the "Offset")

Used to select a specific DWORD in the P4X266E configuration space

1-0 Fixedalways reads 0

Port CFE-CFC - Configuration Data..... RW

Refer to PCI Bus Specification Version 2.2 for further details on operation of the above configuration registers.

Device 0 Register Descriptions

Device 0 Host Bridge Header Registers

All registers are located in PCI configuration space. They should be programmed using PCI configuration mechanism 1 through CF8 / CFC with bus number, function number, and device number equal to zero.

Device 0 Offset 1-0 - Vendor ID (1106h).....RO

15-0 ID Code (reads 1106h to identify VIA Technologies)

Device 0 Offset 3-2 - Device ID (3128h).....RO

15-0 ID Code (reads 3128h to identify the P4X266E)

Device 0 Offset 5-4 –Command (0006h).....RW

15-10 Reserved always reads 0

9 Fast Back-to-Back Cycle Enable RO

- 0 Fast back-to-back transactions only allowed to the same agent.....default
- 1 Fast back-to-back transactions allowed to different agents

8 SERR# Enable..... RO

- 0 SERR# driver disabled.....default
 - 1 SERR# driver enabled
- (SERR# is used to report ECC errors).

7 Address / Data Stepping..... RO

- 0 Device never does stepping.....default
- 1 Device always does stepping

6 Parity Error Response.....RW

- 0 Ignore parity errors & continue.....default
- 1 Take normal action on detected parity errors

5 VGA Palette Snoop..... RO

- 0 Treat palette accesses normally.....default
- 1 Don't respond to palette accesses on PCI bus

4 Memory Write and Invalidate Command..... RO

- 0 Bus masters must use Mem Write.....default
- 1 Bus masters may generate Mem Write & Inval

3 Special Cycle Monitoring..... RO

- 0 Does not monitor special cycles.....default
- 1 Monitors special cycles

2 PCI Bus Master..... RO

- 0 Never behaves as a bus master
- 1 Can behave as a bus master.....default

1 Memory Space..... RO

- 0 Does not respond to memory space
- 1 Responds to memory space.....default

0 I/O Space RO

- 0 Does not respond to I/O spacedefault
- 1 Responds to I/O space

Device 0 Offset 7-6 – Status (0210h).....RWC

15 Detected Parity Error

- 0 No parity error detected..... default
- 1 Error detected in either address or data phase.
This bit is set even if error response is disabled (command register bit-6).write one to clear

14 Signaled System Error (SERR# Asserted)

.....always reads 0

13 Signaled Master Abort

- 0 No abort received default
- 1 Transaction aborted by the master
.....write one to clear

12 Received Target Abort

- 0 No abort received default
- 1 Transaction aborted by the target
.....write one to clear

11 Signaled Target Abortalways reads 0

- 0 Target Abort never signaled

10-9 DEVSEL# Timing

- 00 Fast
- 01 Mediumalways reads 01
- 10 Slow
- 11 Reserved

8 Data Parity Error Detected

- 0 No data parity error detected..... default
- 1 Error detected in data phase. Set only if error response enabled via command bit-6 = 1 and P4X266E was initiator of the operation in which the error occurred.....write one to clear

7 Fast Back-to-Back Capable.....always reads 0

6 User Definable Featuresalways reads 0

5 66MHz Capable.....always reads 0

4 Supports New Capability list.....always reads 1

3-0 Reservedalways reads 0

Device 0 Offset 8 - Revision ID (0nh)..... RO

7-0 Chip Revision Code.....always reads 0nh

Device 0 Offset 9 - Programming Interface (00h)..... RO

7-0 Interface Identifieralways reads 00h

Device 0 Offset A - Sub Class Code (00h)..... RO

7-0 Sub Class Codereads 00 to indicate Host Bridge

Device 0 Offset B - Base Class Code (06h)..... RO

7-0 Base Class Code.. reads 06 to indicate Bridge Device

Device 0 Offset D - Latency Timer (00h)..... RW

Specifies the latency timer value in PCI bus clocks.

7-3 Guaranteed Time Slice for CPU default=0

2-0 Reserved (fixed granularity of 8 clks) .. always read 0
These bits are writeable but read 0 for PCI specification compatibility. The programmed value may be read back in Rx75[6-4] (PCI Arbitration 1).

Device 0 Host Bridge Header Registers (continued)
Device 0 Offset E - Header Type (00h).....RO

7-0 Header Type Code reads 00: single function

Device 0 Offset F - Built In Self Test (BIST) (00h).....RO

7 BIST Supportedreads 0: no supported functions

6-0 Reserved always reads 0

Device 0 Offset 13-10 - Graphics Aperture Base
(00000008h)RW

31-28 Upper Programmable Base Address Bits def=0

27-20 Lower Programmable Base Address Bits def=0

These bits behave as if hardwired to 0 if the corresponding Graphics Aperture Size register bit (Device 0 Offset 84h) is 0.

27	26	25	24	23	22	21	20	(This Register)
7	6	5	4	3	2	1	0	(Gr Aper Size)
RW	RW	RW	RW	RW	RW	RW	RW	1M
RW	RW	RW	RW	RW	RW	RW	0	2M
RW	RW	RW	RW	RW	RW	0	0	4M
RW	RW	RW	RW	RW	0	0	0	8M
RW	RW	RW	RW	0	0	0	0	16M
RW	RW	RW	0	0	0	0	0	32M
RW	RW	0	0	0	0	0	0	64M
RW	0	0	0	0	0	0	0	128M
0	0	0	0	0	0	0	0	256M

19-0 Reserved always reads 00008

Note: The locations in the address range defined by this register are prefetchable.

Device 0 Offset 2D-2C – Subsystem Vendor ID (0000h)R/W1

15-0 Subsystem Vendor ID default = 0

This register may be written once and is then read only.

Device 0 Offset 2F-2E – Subsystem ID (0000h)..... R/W1

15-0 Subsystem ID default = 0

This register may be written once and is then read only.

Device 0 Offset 37-34 - Capability Pointer (000000A0h) RO

Contains an offset from the start of configuration space.

31-0 AGP Capability List Pointeralways reads A0h

Device 0 Host Bridge Device-Specific Registers

These registers are normally programmed once at system initialization time.

V-Link Control

Device 0 Offset 40 – V-Link Specification ID (00h)RO

7-0 Specification Revision always reads 00

Device 0 Offset 41 – NB V-Link Capability (18h)RO

7-6 Reserved always reads 0

5 16-bit Bus Width SupportedRO

0 Not Supporteddefault

1 Supported

4 8-Bit Bus Width Supported.....RO

0 Not Supported

1 Supporteddefault

3 4x Rate SupportedRO

0 Not Supported

1 Supporteddefault

2 2x Rate SupportedRO

0 Not Supporteddefault

1 Supported

1-0 Reserved always reads 0

Device 0 Offset 42 – NB Downlink Command (88h).....RW

7-4 DnCmd Max Request Depth (0=1 DnCmd) . def = 8

3-0 DnCmd Write Buffer Size (doublewords)..... def = 8

Device 0 Offset 44-43 – NB Uplink Status (8280h).....RO

15-12 UpCmd P2C Write Buffer Size (max lines).. def = 8

11-8 UpCmd P2P Write Buffer Size (max lines).. def = 2

7-4 UpCmd Max Request Depth (0=1 UpCmd) . def = 8

3-0 Reserved always reads 0

Device 0 Offset 45 –NB V-Link Bus Timer (44h)..... RW

7-4 Timer for Normal Priority Requests from SB

0000 Immediate

0001 1*4 VCLKs

0010 2*4 VCLKs

0011 3*4 VCLKs

0100 4*4 VCLKs default

0101 5*4 VCLKs

0110 6*4 VCLKs

0111 7*4 VCLKs

1000 8*4 VCLKs

1001 16*4 VCLKs

1010 32*4 VCLKs

1011 64*4 VCLKs

11xx Own the bus for as long as there is a request

3-0 Timer for High Priority Requests from SB

0000 Immediate

0001 1*2 VCLKs

0010 2*2 VCLKs

0011 3*2 VCLKs

0100 4*2 VCLKs default

0101 5*2 VCLKs

0110 6*2 VCLKs

0111 7*2 VCLKs

1000 8*2 VCLKs

1001 16*2 VCLKs

1010 32*2 VCLKs

1011 64*2 VCLKs

11xx Own the bus for as long as there is a request

Device 0 Offset 46 – NB V-Link Misc Control (00h).....RW

- 7 Downstream High Priority**
 - 0 Disable High Priority Down Commandsdef
 - 1 Enable High Priority Down Commands
- 6 Downlink Priority**
 - 0 Treat Downlink Cycles as Normal Priority.def
 - 1 Treat Downlink Cycles as High Priority
- 5-4 Combine Multiple STPGNT Cycles Into One V-Link Command**
 - 00 Compatible, 1 command per V-Link cmd....def
 - 01 2 commands per V-Link command
 - 10 3 commands per V-Link command
 - 11 4 commands per V-Link command
- 3-2 V-Link Master Access Ordering Rules**
 - 00 High priority read, pass normal read (not pass write)default
 - 01 Read (high/normal) pass write (HR>LR>W)
 - 1x Read / write in order
- 1-0 Reserved** always reads 0

Device 0 Offset 47 – V-Link Control (00h)RW

- 7-3 Reserved** always reads 0
- 2 Auto-Disconnect**
 - 0 Disabledefault
 - 1 Enable
- 1 V-Link Disconnect Cycle for HALT cycle**
 - 0 Disabledefault
 - 1 Enable
- 0 V-Link Disconnect Cycle for STPGNT Cycle**
 - 0 Disabledefault
 - 1 Enable

Device 0 Offset 48 – NB/SB V-Link Configuration (18h)RW

- 7 Reserved**always reads 0
- 6 Rest Bus Width Supported**
 - 0 Not Supported default
 - 1 Supported
- 5 16-bit Bus Width Supported**
 - 0 Not Supported default
 - 1 Supported
- 4 8-Bit Bus Width Supported**
 - 0 Not Supported
 - 1 Supported default
- 3 4x Rate Supported**
 - 0 Not Supported
 - 1 Supported default
- 2 2x Rate Supported**
 - 0 Not Supported default
 - 1 Supported
- 1-0 Reserved**always reads 0

Device 0 Offset 49 – SB V-Link Capability (18h) RO

- 7-6 Reserved**always reads 0
- 5 16-bit Bus Width Supported RO**
 - 0 Not Supported default
 - 1 Supported
- 4 8-Bit Bus Width Supported RO**
 - 0 Not Supported
 - 1 Supported default
- 3 4x Rate Supported..... RO**
 - 0 Not Supported
 - 1 Supported default
- 2 2x Rate Supported..... RO**
 - 0 Not Supported default
 - 1 Supported
- 1-0 Reserved**always reads 0

Device 0 Offset 4A – SB Downlink Status (88h).....RO

- 7-4 **DnCmd Max Request Depth** (0=1 DnCmd) . def = 8
3-0 **DnCmd Write Buffer Size** (doublewords)..... def = 8

Device 0 Offset 4C-4B – SB Uplink Command (8280h).RW

- 15-12 **UpCmd P2C Write Buffer Size** (max lines).. def = 8
11-8 **UpCmd P2P Write Buffer Size** (max lines) .. def = 2
7-4 **UpCmd Max Request Depth** (0=1 UpCmd) . def = 8
3-0 **Reserved** always reads 0

Device 0 Offset 4D – SB V-Link Bus Timer (44h).....RW

- 7-4 **Timer for Normal Priority Requests from SB**
0000 Immediate
0001 1*4 VCLKs
0010 2*4 VCLKs
0011 3*4 VCLKs
0100 4*4 VCLKsdefault
0101 5*4 VCLKs
0110 6*4 VCLKs
0111 7*4 VCLKs
1000 8*4 VCLKs
1001 16*4 VCLKs
1010 32*4 VCLKs
1011 64*4 VCLKs
11xx Own the bus for as long as there is a request
- 3-0 **Timer for High Priority Requests from SB**
0000 Immediate
0001 1*2 VCLKs
0010 2*2 VCLKs
0011 3*2 VCLKs
0100 4*2 VCLKsdefault
0101 5*2 VCLKs
0110 6*2 VCLKs
0111 7*2 VCLKs
1000 8*2 VCLKs
1001 16*2 VCLKs
1010 32*2 VCLKs
1011 64*2 VCLKs
11xx Own the bus for as long as there is a request

Device 0 Offset 4E – CCA Master Priority (00h)..... RW

- 7 **1394 High Priority**
0 Low priority..... default
1 High priority
- 6 **LAN / NIC High Priority**
0 Low priority..... default
1 High priority
- 5 **Reserved**always reads 0
- 4 **USB High Priority**
0 Low priority..... default
1 High priority
- 3 **Reserved**always reads 0
- 2 **IDE High Priority**
0 Low priority..... default
1 High priority
- 1 **AC97-ISA High Priority**
0 Low priority..... default
1 High priority
- 0 **PCI High Priority**
0 Low priority..... default
1 High priority

Device 0 Offset 4F – SB V-Link Misc Control (00h) RW

- 7 **Upstream Command High Priority**
0 Disable high priority up commands..... default
1 Enable high priority up commands
- 6-1 **Reserved**always reads 0
- 0 **Down Cycle Wait for Up Cycle Write Flush (Except Down Cycle Post Write)**
0 Disable..... default
1 Enable

Host CPU Control
Device 0 Offset 50 – Request Phase Control (00h)RW

- 7-6 CPU Hardwired IOQ (In Order Queue) Size**
Default set from the inverse of the strap information passed from the south bridge via VAD2 and VAD1.
00 -reserved- (both straps pulled high)
01 -reserved-
10 -reserved-
11 12-Level (both straps pulled low)
- 5 Fast DRAM Access**
0 Disabledefault
1 Enable
- 4-0 Dynamic Defer Snoop Stall Count**
(granularity = 2T, normally set to 01000b)

Device 0 Offset 51 – CPU Interface Basic Control (00h)RW

- 7 CPU Read DRAM Fast Ready**
0 Medium / Slow Ready (see bit 0) default
1 Fast Ready (bit-0 of this register is ignored)
- 6 Read Around Write**
0 Disable default
1 Enable
- 5 DRQ Control**
0 Non pipelined similar to VT8633 default
1 Pipelined
- 4 CPU to PCI Read Defer**
0 Disable default
1 Enable
- 3 Two Defer / Retry Entries**
0 Disable default
1 Enable
- 2 Two Defer / Retry Entries Shared**
0 Each entry is dedicated to 1 CPU default
1 Each entry is shared by 2 CPUs
- 1 PCI Master Pipelined Access**
0 Disable default
1 Enable
- 0 CPU Read DRAM Medium Ready**
(this bit is ignored if bit-7 = 1)
0 Slow Ready default
1 Medium Ready

Device 0 Offset 52 – CPU Interface Advanced Ctrl (00h).....RW

- 7 **CPU RW DRAM 0WS for Back-to-Back Pipeline Access**
0 Disabledefault
1 Enable
- 6 **HREQ High Priority**
0 Disabledefault
1 Enable
- 5 **AGTL+ Pullups (VT8753E Only)**
Default set from the inverse of the VAD3 strap.
Bit-5 of this register was reserved in the VT8753 (the function of this bit was performed by Rx50[6])
0 Disable (strap pulled high)
1 Enable (strap pulled low)
- 4 **Dynamic Snoop Stall for CPU FIFO Full**
0 Disabledefault
1 Enable
- 3 **Write Retire Policy After 2 Writes**
0 Disabledefault
1 Enable
- 2 **Reserved** always reads 0
- 1 **Consecutive Speculative Read**
0 Disabledefault
1 Enable
- 0 **Speculative Read**
0 Disabledefault
1 Enable

Device 0 Offset 53 – CPU Arbitration Control (03h).....RW

- 7-4 **Host Timer** default = 0
- 3-0 **BPRI Timer** (units of 4 HCLKs)..... default = 3

Device 0 Offset 54 – CPU Frequency (40h) RW

- 7 **Reserved**always reads 0
- 6 **CPU FSB Frequency Set from VAD0 Strap**
0 100 MHz (strap pulled low)
1 133 MHz (strap pulled high) default
(The 8753 was fixed to 100 MHz FSB)
- 5 **Auto Configure Set from VAD6 Strap**
0 Disable (strap pulled low)
1 Enable (strap pulled high). AGTL+ Drive settings and other chip configuration settings are stored in ROM, transferred from the south bridge (via the V-Link bus), and loaded into the VT8753E automatically after system reset. Refer to the VT8753E BIOS Porting Guide for layout of the AutoConfigure settings in ROM and for recommended bit settings.
- 4 **SDRAM Burst Length of 8**
0 Disable..... default
1 Enable
- 3 **Rx85, 86, and 87 Writable (VT8753E Only)**
0 Disable..... default
1 Enable
- 2 **PCI Master 8QW Operation**
0 Disable..... default
1 Enable
- 1 **AGP Capability Header Support**
0 Disable..... default
1 Enable
- 0 **VPX Mode**
0 Disable (AGP Mode)..... default
1 Enable (VPX Mode)

DRAM Control

These registers are normally set at system initialization time and not accessed after that during normal system operation. Some of these registers, however, may need to be programmed using specific sequences during power-up initialization to properly detect the type and size of installed memory (refer to the VIA Technologies VT8753E BIOS porting guide for details).

Table 5. System Memory Map

<u>Space</u>	<u>Start</u>	<u>Size</u>	<u>Address Range</u>	<u>Comment</u>
DOS	0	640K	00000000-0009FFFF	Cacheable
VGA	640K	128K	000A0000-000BFFFF	Used for SMM
BIOS	768K	16K	000C0000-000C3FFF	Shadow Ctrl 1
BIOS	784K	16K	000C4000-000C7FFF	Shadow Ctrl 1
BIOS	800K	16K	000C8000-000CBFFF	Shadow Ctrl 1
BIOS	816K	16K	000CC000-000CFFFF	Shadow Ctrl 1
BIOS	832K	16K	000D0000-000D3FFF	Shadow Ctrl 2
BIOS	848K	16K	000D4000-000D7FFF	Shadow Ctrl 2
BIOS	864K	16K	000D8000-000DBFFF	Shadow Ctrl 2
BIOS	880K	16K	000DC000-000DFFFF	Shadow Ctrl 2
BIOS	896K	64K	000E0000-000EFFFF	Shadow Ctrl 3
BIOS	960K	64K	000F0000-000FFFFF	Shadow Ctrl 3
Sys	1MB	—	00100000-DRAM Top	Can have hole
Bus	D Top		DRAM Top-FFFFFFF	
Init	4G-64K	64K	FFFEFFFF-FFFFFFFF	000Fxxxx alias

Device 0 Offset 55 – DRAM Control (00h)..... RW

- 7 0WS Back-to-Back Write to Different DDR Bank**
0 Disable..... default
1 Enable
- 6 Reserved**always reads 0
- 5 DQS Input DLL Adjustment**
0 Disable..... default
1 Enable
- 4 DQS Output DLL Adjustment**
0 Disable..... default
1 Enable
- 3 DQM Removal (Always Perform 4-Burst RW)**
0 Disable..... default
1 Enable
- 2 DQS Output**
0 Disable..... default
1 Enable
- 1 Auto Precharge for TLB Read or CPU WriteBack**
0 Disable..... default
1 Enable
- 0 Write Recovery Time**
0 1T default
1 2T

Device 0 Offset 59-58 - DRAM MA Map Type (2222h).RW

- 15-13 **Bank 5/4 MA Map Type** (see Table 6 below)
- 12 **Bank 5/4 1T Command Rate**
- 0 2T Commanddefault
- 1 1T Command
- 11-9 **Bank 7/6 MA Map Type** (see Table 6 below)
- 8 **Bank 7/6 1T Command Rate**
- 0 2T Commanddefault
- 1 1T Command
- 7-5 **Bank 1/0 MA Map Type** (see Table 6 below)
- 4 **Bank 1/0 1T Command Rate**
- 0 2T Commanddefault
- 1 1T Command
- 3-1 **Bank 3/2 MA Map Type** (see Table 6 below)
- 0 **Bank 3/2 1T Command Rate**
- 0 2T Commanddefault
- 1 1T Command

Table 6. MA Map Type Encoding

000	<u>16Mb</u>	8-bit, 9-bit, 10-bit Column Address
001	<u>64/128Mb</u>	8-bit Column Addressdefault
010	<u>64/128Mb</u>	9-bit Column Address
011	<u>64/128Mb</u>	10/11-bit Column Address
100		-reserved-
101	<u>256Mb</u>	8-bit Column Address
110	<u>256Mb</u>	9-bit Column Address
111	<u>256Mb</u>	10/11-bit Column Address

Device 0 Offset 5F-5A – DRAM Row Ending Address:

- Offset 5A – Bank 0 Ending (HA[31:24]) (01h)..... RW**
- Offset 5B – Bank 1 Ending (HA[31:24]) (01h)..... RW**
- Offset 5C – Bank 2 Ending (HA[31:24]) (01h)..... RW**
- Offset 5D – Bank 3 Ending (HA[31:24]) (01h)..... RW**
- Offset 5E – Bank 4 Ending (HA[31:24]) (01h)..... RW**
- Offset 5F – Bank 5 Ending (HA[31:24]) (01h)..... RW**
- Offset 56 – Bank 6 Ending (HA[31:24]) (01h)..... RW**
- Offset 57 – Bank 7 Ending (HA[31:24]) (01h)..... RW**

Note : BIOS is required to fill the ending address registers for all banks even if no memory is populated. The endings have to be in incremental order.

Device 0 Offset 60 – DRAM Type (00h)..... RW

- 7-6 **DRAM Type for Bank 7/6**
- 5-4 **DRAM Type for Bank 5/4**
- 3-2 **DRAM Type for Bank 3/2**
- 1-0 **DRAM Type for Bank 1/0**
- 00 SDR SDRAM..... default
- 01 -reserved- (do not program)
- 10 DDR SDRAM
- 11 -reserved-

Table 7. Memory Address Mapping Table

SDR / DDR SDRAM (x4 DRAMs supported by SDR only)

MA:	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
<u>16Mb</u> (000)		24		13	12	11	14	22	21	20	19	18	17	16	15	12 row 10,9,8 col
				13	PC	24	23	10	9	8	7	6	5	4	3	
<u>64/128Mb</u> 2K page 001	14	24	14	13	12	11	23	22	21	20	19	18	17	16	15	x16 (14,8) x32 (14,8) x8 (14,9)
		27	14	13	PC	26	25	10	9	8	7	6	5	4	3	
4K page 010	14	25	14	13	12	24	23	22	21	20	19	18	17	16	15	x16 (14,9) x4 (14,10)
		27	14	13	PC	26	11	10	9	8	7	6	5	4	3	
8K page 011	14	26	14	13	25	24	23	22	21	20	19	18	17	16	15	x8 (14,10) x4 (14,11)
		27	14	13	PC	12	11	10	9	8	7	6	5	4	3	
<u>256Mb</u> 2K page 101	25	24	14	13	12	11	23	22	21	20	19	18	17	16	15	x32 (15,8) x16 (15,9)
		27	14	13	PC	26	25	10	9	8	7	6	5	4	3	
4K page 110	26	25	14	13	12	24	23	22	21	20	19	18	17	16	15	x16 (15,9) x8 (15,10)
		27	14	13	PC	26	11	10	9	8	7	6	5	4	3	
8K page 111	27	26	14	13	25	24	23	22	21	20	19	18	17	16	15	x8 (15,10) x4 (15,11)
		28	14	13	PC	12	11	10	9	8	7	6	5	4	3	

Device 0 Offset 61 - Shadow RAM Control 1 (00h).....RW

7-6	CC000h-CFFFFh
00	Read/write disable.....default
01	Write enable
10	Read enable
11	Read/write enable
5-4	C8000h-CBFFFh
00	Read/write disable.....default
01	Write enable
10	Read enable
11	Read/write enable
3-2	C4000h-C7FFFh
00	Read/write disable.....default
01	Write enable
10	Read enable
11	Read/write enable
1-0	C0000h-C3FFFh
00	Read/write disable.....default
01	Write enable
10	Read enable
11	Read/write enable

Device 0 Offset 62 - Shadow RAM Control 2 (00h).....RW

7-6	DC000h-DFFFFh
00	Read/write disable.....default
01	Write enable
10	Read enable
11	Read/write enable
5-4	D8000h-DBFFFh
00	Read/write disable.....default
01	Write enable
10	Read enable
11	Read/write enable
3-2	D4000h-D7FFFh
00	Read/write disable.....default
01	Write enable
10	Read enable
11	Read/write enable
1-0	D0000h-D3FFFh
00	Read/write disable.....default
01	Write enable
10	Read enable
11	Read/write enable

Device 0 Offset 63 - Shadow RAM Control 3 (00h).....RW

7-6	E0000h-EFFFFh
00	Read/write disable default
01	Write enable
10	Read enable
11	Read/write enable
5-4	F0000h-FFFFFFh
00	Read/write disable default
01	Write enable
10	Read enable
11	Read/write enable
3-2	Memory Hole
00	None default
01	512K-640K
10	15M-16M (1M)
11	14M-16M (2M)
1-0	SMI Mapping Control
	SMM
	Non-SMM
	Code Data Code Data
00	DRAM DRAM PCI PCI
01	DRAM DRAM DRAM DRAM
10	DRAM PCI PCI PCI
11	DRAM DRAM DRAM DRAM

Device 0 Offset 64 - DRAM Timing for All Banks (E4h) RW

- 7 Precharge Command to Active Command Period**
0 TRP = 2T
1 TRP = 3Tdefault
- 6 Active Command to Precharge Command Period**
0 TRAS = 5T
1 TRAS = 6Tdefault
- 5-4 CAS Latency**

	SDR	DDR
00	1T	-
01	2T	2T
10	3T	2.5Tdefault
11	-	3T
- 3 Reserved** always reads 0
- 2 ACTIVE to CMD**
0 2T
1 3Tdefault
- 1-0 Bank Interleave**
00 No Interleavedefault
01 2-way
10 4-way
11 Reserved
For 16Mb SDRAMs bank interleave is always 2-way

Device 0 Offset 65 - DRAM Arbitration Timer (00h) RW

- 7-4 AGP Timer** (units of 4 MCLKs) default = 0
- 3-0 CPU Timer** (units of 4 MCLKs) default = 0

Device 0 Offset 66 - DRAM Arbitration Control (00h).. RW

- 7 SDR – Feedback Clock Select**
DDR - DQS Input Delay Setting
0 Auto (Rx67 reads DLL calibration result) ...def
1 Manual (Rx67 reads DQS input delay)
- 6 VT8753: DDR - DQS Output Delay Setting**
0 Autodefault
1 Manual
- 6 VT8753E: DRAM Access Timing**
0 2Tdefault
1 3T (set this bit for 133 MHz DRAM clock)
- 5-4 Arbitration Parking Policy**
00 Park at last bus ownerdefault
01 Park at CPU
10 Park at AGP
11 -reserved-
- 3-0 AGP / CPU Priority** (units of 4 MCLKs)

Device 0 Offset 67 – DDR Strobe Input Delay (00h) RW
DDR:

- 7-6 CS Early Clock Select** default = 0
- 5-0 DQS Input Delay** default = 0
(if Rx66[7]=0, read DLL calibration result)

SDR:

- 7-5 Reserved**always reads 0
- 4 MD Latch Clock Select**
0 Internal clock default
1 External feedback clock
- 3 Reserved**always reads 0
- 2-0 MD Latch Delay**

Device 0 Offset 68 – DDR Strobe Output Delay (00h)... RW

- 7-0 DDR DQS Output Delay** default = 0

Device 0 Offset 69 – DRAM Clock Select (00h).....RW

- 7 **Reserved (Do Not Program) (VT8753E)** default = 0
- 6 **DRAM Operating Frequency Faster Than CPU**
- 0 DRAM Same As or Equal to CPU.....default
 - 1 DRAM Faster Than CPU by 33 MHz

CPU / DRAM	Rx54[6]
0 100 / 100	0.....default
1 100 / 133	0
0 133 / 133	1

All other combinations are reserved.

5 **Dynamic CKE (VT8753)**

- 0 Disabledefault
- 1 Enable

4 **Reserved (VT8753)** always reads 0

5 **DRAM Ctrlr Queue Greater Than 2 (VT8753E)**

- 0 Disabledefault
- 1 Enable

4 **DRAM Ctrlr Queue Not Equal To 4 (VT8753E)**

- 0 Disabledefault
- 1 Enable

3 **DRAM 8K Page Enable**

- 0 Disabledefault
- 1 Enable

2 **DRAM 4K Page Enable**

- 0 Disabledefault
- 1 Enable

1 **DIMM Type**

- 0 Unbuffered.....default
- 1 Registered

0 **Multiple Page Mode**

- 0 Disabledefault
- 1 Enable

Device 0 Offset 6A - Refresh Counter (00h)..... RW

7-0 **Refresh Counter** (in units of 16 MCLKs)

- 00 DRAM Refresh Disabled default
- 01 32 MCLKs
- 02 48 MCLKs
- 03 64 MCLKs
- 04 80 MCLKs
- 05 96 MCLKs
-

The programmed value is the desired number of 16-MCLK units minus one.

Device 0 Offset 6B - DRAM Arbitration Control (00h) RW

7 **Fast Read to Write Turn-around**

- 0 Disable..... default
- 1 Enable

6 **Page Kept Active When Cross Bank**

- 0 Disable..... default
- 1 Enable

5 **Burst Refresh**

- 0 Disable..... default
- 1 Enable

4 **CKE Function**

- 0 Disable..... default
- 1 Enable

3 **HA14 / HA22 Swap**

- 0 Normal..... default
- 1 Swap to improve performance

2-0 **SDRAM Operation Mode Select**

- 000 Normal SDRAM Mode default
- 001 NOP Command Enable
- 010 All-Banks-Precharge Command Enable
(CPU-to-DRAM cycles are converted to All-Banks-Precharge commands).
- 011 MSR Enable
CPU-to-DRAM cycles are converted to commands and the commands are driven on MA[14:0]. The BIOS selects an appropriate host address for each row of memory such that the right commands are generated on MA[14:0].
- 100 CBR Cycle Enable (if this code is selected, CAS-before-RAS refresh is used; if it is not selected, RAS-Only refresh is used)
- 101 Reserved
- 11x Reserved

Device 0 Offset 6C – DRAM Drive Control 1 (00h) RW

- 7-6 SDRAM A Drive – SRASA/SCASA/SWEA, MAA**
00 Lowest.....default
01
10
11 Highest
- 5-4 SDRAM B Drive – SRASB/SCASB/SWEB, MAB**
00 Lowest.....default
01
10
11 Highest
- 3-2 DDR DQS Drive**
00 Lowest.....default
01
10
11 Highest
- 1-0 MD/MECC/DQM/CKE Early Clock Select**
00 Latestdefault
01
10
11 Earliest

Note: Refer to the VT8753E BIOS Porting Guide for SDRAM configuration algorithms and recommended settings for these bits for typical memory system configurations.

Device 0 Offset 6D – DRAM Drive Control 2 (00h)..... RW

- 7-6 Early Clock Select for SCMD, MA Output (for 1T Command)**
00 Latest default
01
10
11 Earliest
- 5-4 DQM Drive**
00 Lowest default
01
10
11 Highest
- 3-2 CS# Drive**
00 Lowest..... default
01
10
11 Highest
- 1-0 Memory Data Drive (MD, MECC)**
00 Lowest default
01
10
11 Highest

Note: Refer to the VT8753E BIOS Porting Guide for SDRAM configuration algorithms and recommended settings for these bits for typical memory system configurations.

Device 0 Offset 6E – ECC Control (00h)RW

- 7 ECC / EC Mode Select**
0 ECC Checking and Reportingdefault
1 ECC Checking, Reporting, and Correcting
- 6 Perform Read-Modify-Write for Partial Write**
0 Disabledefault
1 Enable
- 5 Enable SERR# on ECC / EC Multi-Bit Error**
0 Don't assert SERR# for multi-bit errorsdef
1 Assert SERR# for multi-bit errors
- 4 Enable SERR# on ECC / EC Single-Bit Error**
0 Don't assert SERR# for single-bit errorsdef
1 Assert SERR# for single-bit errors
- 3 ECC / EC Enable - Bank 7/6 (DIMM 3)**
0 Disable (no ECC or EC for banks 7/6)....default
1 Enable (ECC or EC per bit-7)
- 2 ECC / EC Enable - Bank 5/4 (DIMM 2)**
0 Disable (no ECC or EC for banks 5/4)....default
1 Enable (ECC or EC per bit-7)
- 1 ECC / EC Enable - Bank 3/2 (DIMM 1)**
0 Disable (no ECC or EC for banks 3/2)....default
1 Enable (ECC or EC per bit-7)
- 0 ECC / EC Enable - Bank 1/0 (DIMM 0)**
0 Disable (no ECC or EC for banks 1/0)....default
1 Enable (ECC or EC per bit-7)

Error checking / correction may be enabled bank-pair by bank-pair (DIMM by DIMM) by using bits 0-3 above. Bank pairs must be populated with 72-bit memory to enable for EC or ECC since the additional data bits must be present in either case. For this reason, if 64-bit memory is populated in a particular bank pair, the corresponding bit 0-3 should be set to 0 to disable both EC and ECC for that bank pair. For those bank pairs that have 72-bit memory available (and have the corresponding bit 0-3 set), either EC or ECC may be selected via bit-7 above (i.e., all enabled bank pairs will use EC or all will use ECC).

If error checking / reporting only (EC) is selected, all read and write cycles will use normal timing. Partial writes (with EC or ECC enabled) will use read-modify-write cycles to maintain correct error correction codes in the additional 8 data bits. If EC and ECC are disabled for a particular bank pair, partial writes to that bank pair will use the byte enables to write only the selected bytes (using normal write cycles and cycle timing). If error correction (ECC) is selected, the first read of a transaction will always have one additional cycle of latency.

Bit-7	Bits 3-0	RMW	Error Checking	Error Correction
0/1	0	No	No	No
0	1	Yes	Yes	No
1	1	Yes	Yes	Yes

Device 0 Offset 6F – ECC Status (00h).....RWC

- 7 Multi-bit Error Detected** write of '1' resets
- 6-4 Multi-bit Error DRAM Bank**..... default=0
Encoded value of the bank with the multi-bit error.
- 3 Single-bit Error Detected** write of '1' resets
- 2-0 Single-bit Error DRAM Bank** default=0
Encoded value of the bank with the single-bit error.

(see RxD0-4 for ECC Error Address and Error Syndrome)

Table 8. DIMM Module Configuration

Rx6B [4] CKE <u>Ena</u>	Rx6E [3-0] ECC <u>Ena</u>	Rx6E [6] RMW <u>Ena</u>	Rx55 [3] No <u>DQM</u>	DIMM Module Configuration	MECC [7-0] Pins	DQM [8-0] Pins	DQS# [8-0] Pins
1	1	0	1	DDR Only x8 with ECC	MECC[7-0]	CKE[7-0]	DQS[8-0]#
1	0	0	0	DDR Only x8 no ECC	CKE[7-0]	DQM[7-0]	DQS[7-0]#
0	0	0	0	184-Pin DDR/SDR Mix	CKE[7-0]	DQM[8-0]	DQS[8-0]#
1	1	x	0	168-Pin SDR Only	MECC[7-0]	DQM[8-0]	CKE[7-0]
1	0	0	1	2 DDR + 2 SDR (SDR Installed)	CKE[7-0]	-	DQS[7-0]#
1	0	0	0	2 DDR + 2 SDR (DDR Installed)	CKE[7-0]	DQM[7-0]	DQS[7-0]#

PCI Bus Control

These registers are normally programmed once at system initialization time.

Device 0 Offset 70 - PCI Buffer Control (00h)..... RW

- 7 CPU to PCI Post-Write**
 - 0 Disabledefault
 - 1 Enable
- 6 Reserved** always reads 0
- 5-4 PCI Master to DRAM Prefetch**
 - 00 Always prefetchdefault
 - x1 Never prefetch
 - 10 Prefetch only for Enhance command
- 3-2 Reserved** always reads 0
- 1 Delay Transaction**
 - 0 Disabledefault
 - 1 Enable
- 0 Reserved** always reads 0

Device 0 Offset 71 - CPU to PCI Flow Control (48h).. RWC

- 7 Retry Status..... RWC**
 - 0 No retry occurreddefault
 - 1 Retry occurred
- 6 Retry Timeout Action**
 - 0 Retry forever (record status only)
 - 1 Flush buffer or return FFFFFFFFh for reads
.....default
- 5-4 Retry Count and Retry Backoff**
 - 00 Retry 2 times, backoff CPUdefault
 - 01 Retry 16 times
 - 10 Retry 4 times
 - 11 Retry 64 times
- 3 PCI Burst**
 - 0 Disable
 - 1 Enabledefault
- 2 Reserved** always reads 0
- 1 Compatible Type#1 Configuration Cycles**
 - 0 Disable (fixed AD31).....default
 - 1 Enable
- 0 IDSEL Control**
 - 0 AD11, AD12default
 - 1 AD30, AD31

Device 0 Offset 73 - PCI Master Control (00h)..... RW

- 7 Reserved**always reads 0
- 6 PCI Master 1-Wait-State Write**
 - 0 Zero wait state TRDY# response..... default
 - 1 One wait state TRDY# response
- 5 PCI Master 1-Wait-State Read**
 - 0 Zero wait state TRDY# response..... default
 - 1 One wait state TRDY# response
- 4 WSC#**
 - 0 Disable..... default
 - 1 Enable
- 3-1 Reserved**always reads 0
- 0 PCI Master Broken Timer Enable**
 - 0 Disable..... default
 - 1 Enable. Force into arbitration when there is no FRAME# 16 PCICLK's after the grant.

Device 0 Offset 75 - PCI Arbitration 1 (00h).....RW

- 7 Arbitration Mode**
0 REQ-based (arbitrate at end of REQ#) ..default
1 Frame-based (arbitrate at FRAME# assertion)
6-4 Latency Timer read only, reads Rx0D bits 2:0
3 Reserved always reads 0
2-0 PCI Master Bus Time-Out
(force into arbitration after a period of time)
000 Disabledefault
001 1x16 PCICLKs
010 2x16 PCICLKs
011 3x16 PCICLKs
100 4x16 PCICLKs
... ..
111 7x16 PCICLKs

Device 0 Offset 76 - PCI Arbitration 2 (00h)..... RW

- 7 I/O Port 22 Access**
0 CPU access to I/O address 22h is passed on to the PCI bus default
1 CPU access to I/O address 22h is processed internally
6 Reservedalways reads 0
5-4 Master Priority Rotation Control
00 Disable..... default
01 Grant to CPU after every PCI master grant
10 Grant to CPU after every 2 PCI master grants
11 Grant to CPU after every 3 PCI master grants
Setting 01: the CPU will always be granted access after the current bus master completes, no matter how many PCI masters are requesting.
Setting 10: if other PCI masters are requesting during the current PCI master grant, the highest priority master will get the bus after the current master completes, but the CPU will be guaranteed to get the bus after that master completes.
Setting 11: if other PCI masters are requesting, the highest priority will get the bus next, then the next highest priority will get the bus, then the CPU will get the bus.
In other words, with the above settings, even if multiple PCI masters are continuously requesting the bus, the CPU is guaranteed to get access after every master grant (01), after every other master grant (10) or after every third master grant (11).
3-2 Select REQn# to REQ4# mapping
00 REQ4#..... default
01 REQ0#
10 REQ1#
11 REQ2#
1 Reservedalways reads 0
0 REQ4# is High Priority Master
0 Disable..... default
1 Enable

GART / Graphics Aperture Control

The function of the Graphics Address Relocation Table (GART) is to translate virtual 32-bit addresses issued by an AGP device into 4K-page based physical addresses for system memory access. In this translation, the upper 20 bits (A31-A12) are remapped, while the lower 12 address bits (A11-A0) are used unchanged.

A one-level fully associative lookup scheme is used to implement the address translation. In this scheme, the upper 20 bits of the virtual address are used to point to an entry in a page table located in system memory. Each page table entry contains the upper 20 bits of a physical address (a "physical page" address). For simplicity, each page table entry is 4 bytes. The total size of the page table depends on the GART range (called the "aperture size") which is programmable in the P4X266E.

This scheme is shown in the figure below.

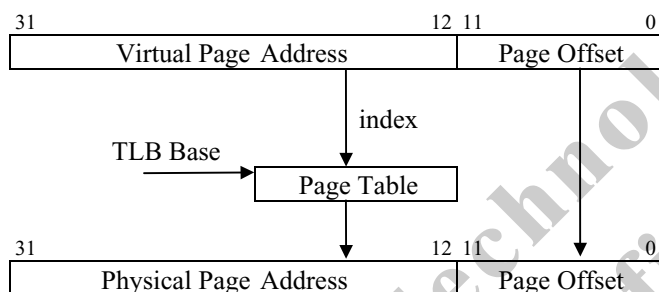


Figure 3. Graphics Aperture Address Translation

Since address translation using the above scheme requires an access to system memory, an on-chip cache (called a "Translation Lookaside Buffer" or TLB) is utilized to enhance performance. The TLB in the P4X266E contains 16 entries. Address "misses" in the TLB require an access of system memory to retrieve translation data. Entries in the TLB are replaced using an LRU (Least Recently Used) algorithm.

Addresses are translated only for accesses within the "Graphics Aperture" (GA). The Graphics Aperture can be any power of two in size from 1MB to 256MB (i.e., 1MB, 2MB, 4MB, 8MB, etc). The base of the Graphics Aperture can be anywhere in the system virtual address space on an address boundary determined by the aperture size (e.g., if the aperture size is 4MB, the base must be on a 4MB address boundary). The Graphics Aperture Base is defined in register offset 10 of device 0. The Graphics Aperture Size and TLB Table Base are defined in the following register group (offsets 84 and 88 respectively) along with various control bits.

Device 0 Offset 83-80 - GART/TLB Control (00000000h) RW

31-16	Reservedalways reads 0
15-8	Reserved (test mode status)RO
7	Flush Page TLB	
	0	Disable..... default
	1	Enable
6-0	Reservedalways reads 0

Note: For any master access to the Graphics Aperture range, snoop will not be performed.

Device 0 Offset 84 - Graphics Aperture Size (00h)..... RW

7-0	Graphics Aperture Size	
11111111	1M	1111000 16M
11111110	2M	1110000 32M
11111100	4M	11000000 64M
11111000	8M	10000000 128M
		00000000 256M

(See Next Page for Rx85-87)

Offset 8B-88 - GA Translation Table Base (00000000h) RW

31-12	Graphics Aperture Translation Table Base.	Pointer to the base of the translation table in system memory used to map addresses in the aperture range (the pointer to the base of the "Directory" table).
11-2	Reservedalways reads 0
1	Graphics Aperture Enable	
	0	Disable..... default
	1	Enable
0	Reservedalways reads 0

Note: To disable the Graphics Aperture, set this bit to 0 and set all bits of the Graphics Aperture Size to 0. To enable the Graphics Aperture, set this bit to 1 and program the Graphics Aperture Size to the desired aperture size.

CPU-to-Memory Access Control

Offset 85 – CPU-to-Memory Write PolicyRO / RW†

Bits 7 and 3 of this register are only available in the VT8753E

7-4 Write Request Limit default = 0

3-0 Write Request Base default = 0

When the number of outstanding write requests is equal to the “limit”, the P4X266E will put a priority on decreasing write requests until the number pending is equal to the “base”.

Offset 86 – CPU-to-Memory Bandwidth Timer ..RO / RW†

This register is only available in the VT8753E

7-4 Host Bandwidth Timer default = 0

3-0 DRAM Bandwidth Timer default = 0

Offset 87 – CPU-to-Memory Bandwidth Limit ...RO / RW†

This register is only available in the VT8753E

7-3 Reserved always reads 0

2-1 Bandwidth Limit

00 Disable (same operation as VT8753)default

01 Fixed DRAM bandwidth limit

10 Fixed CPU bandwidth limit

11 Dynamically toggle between two CPU /
DRAM bandwidth limits (two timers Rx86[7-
4] and Rx86[3-0] are used)

0 CPU Access DRAM Read After Write

0 Normaldefault

1 Improved

Rx85, 86 and 87 should be programmed to optimum values recommended by VIA to increase system performance.

† Rx85, 86 and 87 are Write Enabled via Rx54[3]

AGP Control

Device 0 Offset A3-A0 - AGP Capability Identifier

(0020C002h)	RO
31-24 Reserved always reads 00	
23-20 Major Specification Revision always reads 0010	
	Major rev # of AGP spec to which device conforms	
19-16 Minor Specification Revision always reads 0000	
	Minor rev # of AGP spec to which device conforms	
15-8 Pointer to Next Item always reads C0h (last item)	
7-0 AGP ID	.. (always reads 02 to indicate it is AGP)	

Device 0 Offset A7-A4 - AGP Status (1F000201h)RO

31-24 Maximum AGP Requests always reads 1F	
	Max # of AGP requests the device can manage (32)	
23-10 Reserved always reads 0	
9 Supports SideBand Addressing always reads 1	
8-6 Reserved always reads 0	
5 4G Supported (can be written at RxAE[5])	
4 Fast Write Supported (can be written at RxAE[4])	
3 Reserved always reads 0	
2 4X Rate Supported always reads 0	
1 2X Rate Supported always reads 0	
0 1X Rate Supported always reads 1	

Device 0 Offset AB-A8 - AGP Command (00000000h)..RW

31-24 Request Depth (reserved for target)	..always reads 0s	
23-10 Reservedalways reads 0s	
9 SideBand Addressing Enable		
	0 Disabledefault	
	1 Enable	
8 AGP Enable		
	0 Disabledefault	
	1 Enable	
7-6 Reservedalways reads 0s	
5 4G Enable		
	0 Disabledefault	
	1 Enable	
4 Fast Write Enable		
	0 Disabledefault	
	1 Enable	
3 Reservedalways reads 0s	
2 4X Mode Enable		
	0 Disabledefault	
	1 Enable	
1 2X Mode Enable always reads 0 (disable)	
0 1X Mode Enable always reads 0 (disable)	

Device 0 Offset AC - AGP Control (00h)..... RW

7 AGP DisableRO	
	0 Disable..... default	
	1 Enable	
	This bit is latched from MA9 at the rising edge of RESET#.	
6 AGP Read Synchronization		
	0 Disable..... default	
	1 Enable	
5 AGP Read Snoop DRAM Post-Write Buffer		
	0 Disable..... default	
	1 Enable	
4 GREQ# Priority Becomes Higher When Arbiter is Parked at AGP Master		
	0 Disable..... default	
	1 Enable	
3 2X Rate Supported		
	0 Disable..... default	
	1 Enable	
2 Fence / Flush		
	0 Disable — low priority requests may be executed out of order. default	
	1 Enable — all normal priority AGP operations will be executed in order	
1 AGP Grant Parking Policy		
	0 Non-Parking Grant — if GFRM# or GPIPE# is asserted, GGNT# is deasserted..... default	
	1 Parking Grant — if GFRM# or GPIPE# is asserted, GGNT# is not de-asserted until GREQ# is deasserted or timeout	
0 AGP to PCI Master or CPU to PCI Turnaround Cycle		
	0 2T or 3T Timing..... default	
	1 1T Timing	

AGP Control (continued)
Device 0 Offset AD – AGP Miscellaneous Control (02h)RW

- 7-6 **Reserved** always reads 0
- 5 **Input on AGP GD / GBE Pads**
- 0 Disable default
- 1 Enable
- 4 **Choose First or Last Ready of DRAM**
- 0 Last ready chosen default
- 1 First ready chosen
- 3-0 **AGP Data Phase Latency Timer** default = 02h

Device 0 Offset AE – AGP Miscellaneous Control (00h)RW

- 7-6 **Reserved** always reads 0
- 5 **4G Supported**
- 0 4G not supported default
- 1 4G supported
- 4 **Fast Write Supported**
- 0 Fast Write not supported default
- 1 Fast Write supported
- 3 **Reserved** always reads 0
- 2 **4X Rate Supported**
- 0 Disable default
- 1 Enable
- 1-0 **Reserved** always reads 0

Device 0 Offset B0 – AGP Pad Control / Status (8xh) ...RW

- 7 **AGP 4x Strobe VREF Control**
- This bit is valid only when RxAS[2] = 1 (4x transfer mode enabled), otherwise, STB VREF is AGPVREF.
- 0 STB VREF is STB# and vice versa
- 1 STB VREF is AGPVREF default
- The reference voltage is also determined by setting of RxBS[1] (AGP Bus Voltage):
- | AGP Voltage | This Bit | Strobe Reference Voltage |
|-------------|------------|--------------------------|
| 3.3V | don't care | AGPVREF = 0.4 x 3.3V |
| 1.5V | 1 | AGPVREF = 0.5 x 1.5V |
| 1.5V | 0 | STB / STB# |
- 6 **AGP 4x Strobe & GD Pad Drive Strength**
- 0 Drive strength set to compensation circuit default default
- 1 Drive strength controlled by RxBS[7-0]
- 5-3 **AGP Compensation Circuit N Control Output.RO**
- 2-0 **AGP Compensation Circuit P Control Output.RO**

Device 0 Offset B1 – AGP Drive Strength (63h) RW

- 7-4 **AGP Output Buffer Drive Strength N Ctrl....def=6**
- 3-0 **AGP Output Buffer Drive Strength P Ctrl....def=3**

Device 0 Offset B2 – AGP Pad Drive & Delay Ctrl (08h)RW

- 7 **GD/GDS/GDS#/GBE Pad Control** default = 0
- | | SA / SBS | GD / GBE / GDS |
|--------------|----------|----------------|
| 0 VDDQ=1.5V: | Normal | Normal |
| VDDQ=3.3V: | Delayed | Normal |
| 1 VDDQ=1.5V: | Normal | Delayed |
| VDDQ=3.3V | Delayed | Delayed |
- 6-5 **Reserved** always reads 0
- 4 **GD[31:16] Output Stagger Delay**
- 0 No delay default
- 1 Delay GD[31:16] by 1 ns
- 3 **GD, GDS, GDS# Slew Rate Control**
- 0 Disable
- 1 Enable default
- 2 **GD, GDS, GDS# Preamble Control**
- 0 Disable default
- 1 Enable
- 1 **AGP Bus Voltage**
- 0 1.5V default
- 1 3.3V
- 0 **GDS Output Delay**
- 0 No delay default
- 1 Delay GDS by 400 ps
(GDS & GDS# will be delayed 1 ns more if bit-4 = 1)

Device 0 Offset B3 – AGP Strobe Drive Strength (63h) RW

- 7-4 **AGP Strobe Output Drive Strength N Ctrl ...def=6**
- 3-0 **AGP Strobe Output Drive Strength P Ctrl....def=3**

V-Link Control
Device 0 Offset B4 – V-Link NB Compensation Ctrl (00h)RW

- 7-6 V-Link Autocomp Output Value**..... always reads 0
- 5 Pullup Compensation Selection**
 - 0 Auto Comp (use values in bits 7-6).....default
 - 1 Manual Comp (use values in bits 3-2)
- 4 Pulldown Compensation Selection**
 - 0 Auto Comp (use values in bits 7-6).....default
 - 1 Manual Comp (use values in bits 1-0)
- 3-2 Pullup Compensation Manual Setting** def = 0
- 1-0 Pulldown Compensation Manual Setting** def = 0

Device 0 Offset B5 – V-Link NB Drive Control (00h).... RW

- 7-6 NB V-Link Strobe Pullup Manual Setting**
- 5-4 NB V-Link Strobe Pulldown Manual Setting**
- 3-1 Reserved** always reads 0
- 0 NB V-Link Slew Rate Control**
 - 0 Disabledefault
 - 1 Enable

Device 0 Offset B8 – V-Link SB Compensation Ctrl (00h)RW

- 7-6 V-Link Autocomp Output Value**always reads 0
- 5 Pullup Compensation Selection**
 - 0 Auto Comp (use values in bits 7-6)..... default
 - 1 Manual Comp (use values in bits 3-2)
- 4 Pulldown Compensation Selection**
 - 0 Auto Comp (use values in bits 7-6)..... default
 - 1 Manual Comp (use values in bits 1-0)
- 3-2 Pullup Compensation Manual Setting**.....def = 0
- 1-0 Pulldown Compensation Manual Setting**.....def = 0

Device 0 Offset B9 – V-Link SB Drive Control (00h).... RW

- 7-6 SB V-Link Strobe Pullup Manual Setting**
- 5-4 SB V-Link Strobe Pulldown Manual Setting**
- 3-1 Reserved**always reads 0
- 0 SB V-Link Slew Rate Control**
 - 0 Disable..... default
 - 1 Enable

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DRAM Interface Control

Device 0 Offset BE – MECC Drive Strength (00h) RW

- 7-6 MECC Drive Strength default = 0
5-0 Reserved always reads 0

Device 0 Offset BF – DRAM Pad Toggle Reduction (00h) RW

- 7 MA / SCMD Pin Toggle Reduction
0 Disable default
1 Enable (MA and S command pins won't toggle if not accessed)
6 Slew Rate Control for MA / SCMD Group A
0 Disable default
1 Enable
5 Slew Rate Control for MA / SCMD Group B
0 Disable default
1 Enable
4 Reserved always reads 0
3 DIMM #3 MAA / MAB Select
0 MAA default
1 MAB
2 DIMM #2 MAA / MAB Select
0 MAA default
1 MAB
1 DIMM #1 MAA / MAB Select
0 MAA default
1 MAB
0 DIMM #0 MAA / MAB Select
0 MAA default
1 MAB

Power Management

Device 0 Offset C0 – Power Management Capability ID RO

- 7-0 Capability ID always reads 01h

Device 0 Offset C1 – Power Management Next Pointer. RO

- 7-0 Next Pointer always reads 00h (“Null” Pointer)

Device 0 Offset C2 – Power Mgmt Capabilities I RO

- 7-0 Power Management Capabilities .. always reads 02h

Device 0 Offset C3 – Power Mgmt Capabilities II RO

- 7-0 Power Management Capabilities .. always reads 00h

Device 0 Offset C4 – Power Mgmt Control / Status RW

- 7-2 Reserved always reads 0
1-0 Power State
00 D0 default
01 -reserved-
10 -reserved-
11 D3 Hot

Device 0 Offset C5 – Power Management Status RO

- 7-0 Power Management Status always reads 00h

Device 0 Offset C6 – PCI-to-PCI Bridge Support Ext.... RO

- 7-0 P2P Bridge Support Extensions always reads 00h

Device 0 Offset C7 – Power Management Data RO

- 7-0 Power Management Data always reads 00h

ECC Error Control

Device 0 Offset D3-D0 – ECC Error Address (xxh) RO

Device 0 Offset D4 – ECC Error Syndrome (xxh) RO

AGTL+ I/O Control

Device 0 Offset D8 – Host Address (2x) Pullup Drive....RW

- 7 Reserved always reads 0
- 6-4 Strobe Pullup Drive (HAS#) default = 0
- 3 Reserved always reads 0
- 2-0 Address Pullup Drive (HA,HREQ#) default = 0

Device 0 Offset D9 – Host Address (2x) Pulldown DriveRW

- 7 Reserved always reads 0
- 6-4 Strobe Pulldown Drive (HAS#) default = 0
- 3 Reserved always reads 0
- 2-0 Address Pulldown Drive (HA,HREQ#) . default = 0

Device 0 Offset DA – Host Data (4x) Pullup Drive.....RW

- 7 Reserved always reads 0
- 6-4 Strobe Pullup Drive (HDS,HDS#) default = 0
- 3 Reserved always reads 0
- 2-0 Address Pullup Drive (HD,HDBI#)..... default = 0

Device 0 Offset DB – Host Data (4x) Pulldown Drive....RW

- 7 Reserved always reads 0
- 6-4 Strobe Pulldown Drive (HDS,HDS#) default = 0
- 3 Reserved always reads 0
- 2-0 Address Pulldown Drive (HD,HDBI#) ... default = 0

Note: Refer to the VT8753E BIOS Porting Guide for recommended settings for these bits for typical system configurations.

Device 0 Offset DC – Output Delay / Stagger Control... RW

- 7-6 Data / Strobe Relative Delay
 - 00 Data delay = strobe delay + 150 psec.....default
 - 01 Data delay = strobe delay
 - 10 Data delay = strobe delay – 150 psec
 - 11 Data delay = strobe delay – 300 psec
- 5 HD[63:48, 31:16], HDBI[3,1]# Output Stagger
 - 0 No delaydefault
 - 1 1 nsec delay
- 4 HA[31:17] Output Stagger
 - 0 No delaydefault
 - 1 1 nsec delay
- 3-2 HDS / HDS# Output Extra Delay
 - 00 No delaydefault
 - 01 150 psec delay
 - 10 300 psec delay
 - 11 450 psec delay
- 1-0 HAS # Output Extra Delay
 - 00 No delaydefault
 - 01 150 psec delay
 - 10 300 psec delay
 - 11 450 psec delay

Device 0 Offset DD – AGTL+ I/O Control (00h) RW

- 7 AGTL+ 4x Input Increase Delay to Filter Noise
 - 0 Disable..... default
 - 1 Enable
- 6 AGTL+ 2x Input Increase Delay to Filter Noise
 - 0 Disable..... default
 - 1 Enable
- 5 AGTL+ Slew Rate Control
 - 0 Disable..... default
 - 1 Enable
- 4 Reservedalways reads 0
- 3 Input Pullup
 - 0 Disable..... default
 - 1 Enable
- 2 AGTL+ Strobe Internal Termination Pullups
 - 0 Disable..... default
 - 1 Enable
- 1 AGTL+ Data Internal Termination Pullups
 - 0 Disable..... default
 - 1 Enable
- 0 AGTL+ Dynamic Compensation
 - 0 Disable..... default
 - 1 Enable

Device 0 Offset DE – AGTL+ Comp Status (00h) RW

- 7 Select AutoCompensation Drive
 - 0 Disable..... default
 - 1 Enable (RxD8-DB set automatically on-chip based on auto compensation results)
- 6-4 AGTL+ Compensation Result default = 0
- 3 AGTL+ POS Function
 - 0 Inputs always powered default
 - 1 Inputs powered down when not in input mode
- 2 DBI Double Check
 - 0 Disable..... default
 - 1 Enable (bit-1 must also be 1)
- 1 DBI (Dynamic Bus Inversion) Function
 - 0 Enable..... default
 - 1 Disable (DBI always high)
- 0 Reservedalways reads 0

Device 0 Offset DF – AGTL+ Auto Comp Offset (00h). RW

- 7-4 AGTL+ Drive Offset to Comp Result for 2x Pad
 - default = 0
- 3-0 AGTL+ Drive Offset to Comp Result for 4x Pad
 - default = 0

Frame Buffer Control
Device 0 Offset E0 – CPU Direct Access FB Base (00h) RW

- 7-1 CPU Direct Access FB Base Address[27:21] . def=0
0 CPU Direct Access Frame Buffer
0 Disabledefault
1 Enable

Device 0 Offset E1 – CPU Direct Access FB Size (00h)..RW

- 7 Internal VGA
0 Disabledefault
1 Enable
- 6-4 Frame Buffer Size
000 Nonedefault
001 Reserved
010 Reserved
011 8MB
100 16MB
101 32MB
11x -reserved-

- 3-0 CPU Direct Access FB Base Address[31:28] . def=0

Device 0 Offset E2 – VGA Arbitration Timer 1 (00h) ...RW

- 7-4 VGA High Priority Timer (units of 16 MCLKs)def=0
3-0 VGA Timer (units of 16 MCLKs) default = 0

Device 0 Offset E3 – VGA Arbitration Timer 2 (00h) ...RW

- 7-4 Timer to Promote Graphics Priority
(units of 16 MCLKs) default = 0
3-2 Reserved always reads 0
1-0 Probing Signal Select default = 0

DRAM Above 4G Control
Device 0 Offset E4 – Low Top Address Low (00h) RW

- 7-4 Low Top Address Low default = 0
3-0 DRAM Granularity
0 16M Total DRAM less than 4G default
1 32M Total DRAM less than 8G
2 64M Total DRAM less than 16G
3 128M Total DRAM less than 32G
4 256M Total DRAM less than 64G
5-7 -reserved-

Device 0 Offset E5 – Low Top Address High (FFh) RW

- 7-0 Low Top Address Highdefault = FFh

Device 0 Offset E6 – SMM / APIC Decoding (01h) RW

- 7-6 Reservedalways reads 0
5 Reserved (Do Not Program) default = 0
4 I/O APIC Decoding
0 FECxxxxx accesses go to PCI default
1 FEC00000 to FEC7FFFF accesses go to PCI
FEC80000 to FECFFFFFF accesses go to AGP
- 3 MSI (Processor Message) Support
0 Disable (master access to FEExxxxx will go to PCI) default
1 Enable (master access to FEExxxxx will be passed to host side to do snoop)
- 2 Top SMM
0 Disable default
1 Enable
- 1 High SMM
0 Disable default
1 Enable
- 0 Compatible SMM
0 Disable
1 Enable default

BIOS Scratch
Device 0 Offset F3-F4 – BIOS Scratch Registers RW

- 7-0 No hardware function default = 0

Device 1 Register Descriptions

Device 1 PCI-to-PCI Bridge Header Registers

All registers are located in PCI configuration space. They should be programmed using PCI configuration mechanism 1 through CF8 / CFC with bus number of 0 and function number equal to 0 and device number equal to one.

Device 1 Offset 1-0 - Vendor ID (1106h).....RO

15-0 ID Code (reads 1106h to identify VIA Technologies)

Device 1 Offset 3-2 - Device ID (B091h).....RO

15-0 ID Code (reads B091h to identify the P4X266E PCI-to-PCI Bridge device)

Device 1 Offset 5-4 – Command (0007h).....RW

- 15-10 Reserved** always reads 0
- 9 Fast Back-to-Back Cycle Enable** RO
- 0 Fast back-to-back transactions only allowed to the same agent.....default
- 1 Fast back-to-back transactions allowed to different agents
- 8 SERR# Enable**..... RO
- 0 SERR# driver disabled.....default
- 1 SERR# driver enabled
(SERR# is used to report ECC errors).
- 7 Address / Data Stepping**..... RO
- 0 Device never does stepping.....default
- 1 Device always does stepping
- 6 Parity Error Response**..... RW
- 0 Ignore parity errors & continue.....default
- 1 Take normal action on detected parity errors
- 5 Reserved** always reads 0
- 4 Memory Write and Invalidate Command** RO
- 0 Bus masters must use Mem Write.....default
- 1 Bus masters may generate Mem Write & Inval
- 3 Special Cycle Monitoring**..... RO
- 0 Does not monitor special cycles.....default
- 1 Monitors special cycles
- 2 Bus Master** RW
- 0 Never behaves as a bus master
- 1 Enable to operate as a bus master on the primary interface on behalf of a master on the secondary interfacedefault
- 1 Memory Space**..... RW
- 0 Does not respond to memory space
- 1 Enable memory space accessdefault
- 0 I/O Space** RW
- 0 Does not respond to I/O space
- 1 Enable I/O space accessdefault

Device 1 Offset 7-6 - Status (Primary Bus) (0230h).....RWC

- 15 Detected Parity Error**always reads 0
- 14 Signaled System Error (SERR#)**.....always reads 0
- 13 Signaled Master Abort**
- 0 No abort received default
- 1 Transaction aborted by the master with Master-Abort (except Special Cycles)..... write 1 to clear
- 12 Received Target Abort**
- 0 No abort received default
- 1 Transaction aborted by the target with Target-Abort write 1 to clear
- 11 Signaled Target Abort**always reads 0
- 10-9 DEVSEL# Timing**
- 00 Fast
- 01 Mediumalways reads 01
- 10 Slow
- 11 Reserved
- 8 Data Parity Error Detected**always reads 0
- 7 Fast Back-to-Back Capable**.....always reads 0
- 6 User Definable Features**always reads 0
- 5 66MHz Capable**.....always reads 1
- 4 Supports New Capability list**.....always reads 1
- 3-0 Reserved**always reads 0

Device 1 Offset 8 - Revision ID (00h)..... RO

7-0 P4X266E Chip Revision Code (00=First Silicon)

Device 1 Offset 9 - Programming Interface (00h)..... RO

This register is defined in different ways for each Base/Sub-Class Code value and is undefined for this type of device.

7-0 Interface Identifieralways reads 00

Device 1 Offset A - Sub Class Code (04h)..... RO

7-0 Sub Class Code..reads 04 to indicate PCI-PCI Bridge

Device 1 Offset B - Base Class Code (06h)..... RO

7-0 Base Class Code.. reads 06 to indicate Bridge Device

Device 1 Offset D - Latency Timer (00h)..... RO

7-0 Reservedalways reads 0

Device 1 Offset E - Header Type (01h)..... RO

7-0 Header Type Code..... reads 01: PCI-PCI Bridge

Device 1 Offset F - Built In Self Test (BIST) (00h)..... RO

- 7 BIST Supported**..... reads 0: no supported functions
- 6 Start Test** write 1 to start but writes ignored
- 5-4 Reserved**always reads 0
- 3-0 Response Code**.....0 = test completed successfully

Device 1 Offset 18 - Primary Bus Number (00h).....RW
7-0 Primary Bus Number default = 0

This register is read write, but internally the chip always uses bus 0 as the primary.

Device 1 Offset 19 - Secondary Bus Number (00h).....RW
7-0 Secondary Bus Number default = 0

Note: AGP must use these bits to convert Type 1 to Type 0.

Device 1 Offset 1A - Subordinate Bus Number (00h)RW
7-0 Primary Bus Number default = 0

Note: AGP must use these bits to decide if Type 1 to Type 1 command passing is allowed.

Device 1 Offset 1B – Secondary Latency Timer (00h)RO
7-0 Reserved always reads 0

Device 1 Offset 1C - I/O Base (f0h).....RW
7-4 I/O Base AD[15:12] default = 1111b

3-0 I/O Addressing Capability default = 0

Device 1 Offset 1D - I/O Limit (00h).....RW
7-4 I/O Limit AD[15:12] default = 0

3-0 I/O Addressing Capability default = 0

Device 1 Offset 1F-1E - Secondary Status.....RO
15-0 Secondary Status

Rx44[4] = 0: these bits read back 0000h

Rx44[4] = 1: these bits read back same as Rx7-6

Device 1 Offset 21-20 - Memory Base (fff0h).....RW
15-4 Memory Base AD[31:20] default = FFFh

3-0 Reserved always reads 0

Device 1 Offset 23-22 - Memory Limit (Inclusive) (0000h) RW
15-4 Memory Limit AD[31:20] default = 0

3-0 Reserved always reads 0

Device 1 Offset 25-24 - Prefetchable Memory Base (fff0h) RW
15-4 Prefetchable Memory Base AD[31:20] default = FFFh

3-0 Reserved always reads 0

Device 1 Offset 27-26 - Prefetchable Memory Limit
(0000h) RW
15-4 Prefetchable Memory Limit AD[31:20] . default = 0

3-0 Reserved always reads 0

Device 1 Offset 34 - Capability Pointer (80h)RO

Contains an offset from the start of configuration space.

7-0 AGP Capability List Pointer always reads 80h

Device 1 Offset 3F-3E – PCI-to-PCI Bridge Control
(0000h) RW
15-4 Reservedalways reads 0

3 VGA-Present on AGP

0 Forward VGA accesses to PCI Bus default

1 Forward VGA accesses to AGP Bus

Note: VGA addresses are memory A0000-BFFFFh and I/O addresses 3B0-3BBh, 3C0-3CFh and 3D0-3DFh (10-bit decode). "Mono" text mode uses B0000-B7FFFh and "Color" Text Mode uses B8000-BFFFFh. Graphics modes use Axxxxh. Mono VGA uses I/O addresses 3Bx-3Cxh and Color VGA uses 3Cx-3Dxh. If an MDA is present, a VGA will not use the 3Bxh I/O addresses and B0000-B7FFFh memory space; if not, the VGA will use those addresses to emulate MDA modes.

2 Block / Forward ISA I/O Addresses

0 Forward all I/O accesses to the AGP bus if they are in the range defined by the I/O Base and I/O Limit registers (device 1 offset 1C-1D)

..... default

1 Do not forward I/O accesses to the AGP bus that are in the 100-3FFh address range even if they are in the range defined by the I/O Base and I/O Limit registers.

1-0 Reservedalways reads 0

Device 1 PCI-to-PCI Bridge Device-Specific Registers

AGP Bus Control

Device 1 Offset 40 - CPU-to-AGP Flow Control 1 (00h) RW

- 7 CPU-AGP Post Write**
0 Disabledefault
1 Enable
- 6 Reserved** always reads 0
- 5 CPU-AGP One Wait State Burst Write**
0 Disabledefault
1 Enable
- 4-3 Read Prefetch Control**
00 Always prefetchdefault
x1 Never prefetch
10 Prefetch only for Enhance command
- 2 MDA Present on AGP**
0 Forward MDA accesses to AGPdefault
1 Forward MDA accesses to PCI
Note: Forward despite IO / Memory Base / Limit
Note: MDA (Monochrome Display Adapter) addresses are memory addresses B0000h-B7FFFh and I/O addresses 3B4-3B5h, 3B8-3BAh, and 3BFh (10-bit decode). 3BC-3BE are reserved for printers.
Note: If Rx3E bit-3 is 0, this bit is a don't care (MDA accesses are forwarded to the PCI bus).
- 1 AGP Master Read Caching**
0 Disabledefault
1 Enable
- 0 AGP Delay Transaction**
0 Disabledefault
1 Enable

Table 9. VGA/MDA Memory/IO Redirection

3E[3]	40[2]	VGA	MDA	Axxxx,	B0000	3Cx,	
VGA	MDA	is	is	B8xxx	-B7FFF	3Dx	3Bx
Pres.	Pres.	on	on	Access	Access	I/O	I/O
0	-	PCI	PCI	PCI	PCI	PCI	PCI
1	0	AGP	AGP	AGP	AGP	AGP	AGP
1	1	AGP	PCI	AGP	PCI	AGP	PCI

Device 1 Offset 41 - CPU-to-AGP Flow Control 2 (08h) RW

- 7 Retry Status**
0 No retry occurred..... default
1 Retry Occurred**write 1 to clear**
- 6 Retry Timeout Action**
0 No action taken except to record status def
1 Flush buffer for write or return all 1s for read
- 5-4 Retry Count**
00 Retry 2, backoff CPU default
01 Retry 4, backoff CPU
10 Retry 16, backoff CPU
11 Retry 64, backoff CPU
- 3 CPU-to-AGP Bursting Timeout**
0 Disable
1 Enable..... **default**
- 2 Reserved**always reads 0
- 1 CPU-to-PCI/AGP Cycles Invalidate PCI/AGP Buffered Read Data**
0 Disable..... default
1 Enable
- 0 Reserved**always reads 0

Device 1 Offset 42 - AGP Master Control (00h) RW

- 7 Reserved (Must Be Programmed to 1)** def = 0
When this bit is set, the P4X266E will automatically resolve the problem of AGP master cycles being blocked by PCI Master Cycles.
- 6 AGP Master One Wait State Write**
0 Disable..... default
1 Enable
- 5 AGP Master One Wait State Read**
0 Disable..... default
1 Enable
- 4 Break Consecutive PCI Master Accesses**
0 Disable..... default
1 Enable
- 3 Reserved**always reads 0
- 2 Claim I/O R/W and Memory Read Cycles**
0 Disable..... default
1 Enable
- 1 Claim Local APIC FEEEx xxxx Cycles**
0 Disable..... default
1 Enable
- 0 Snoop Write Enable 2T Rate, Support Host Side Snoop Cycles at 2T Rate**
0 Disable..... default
1 Enable

Device 1 Offset 43 - AGP Master Latency Timer (22h) RW

7-4	Host to AGP Time slot
0	Disable (no timer)
1	16 GCLKs
2	32 GCLKsdefault
...	...
F	128 GCLKs
3-0	AGP Master Time Slot
0	Disable (no timer)
1	16 GCLKs
2	32 GCLKsdefault
...	...
F	128 GCLKs

Device 1 Offset 45 – Fast Write Control (72h)..... RW

7	Force Fast Write Cycle to be QW Aligned (if Rx45[6] = 0)
0	Disable..... default
1	Enable
6	Merge Multiple CPU Transactions Into One Fast Write Burst Transaction
0	Disable
1	Enable..... default
5	Merge Multiple CPU Write Cycles To Memory Offset 23-20 Into Fast Write Burst Cycles (if Rx45[6] = 0)
0	Disable
1	Enable..... default
4	Merge Multiple CPU Write Cycles To Prefetchable Memory Offset 27-24 Into Fast Write Burst Cycles (if Rx45[6] = 0)
0	Disable
1	Enable..... default
3	Reservedalways reads 0
2	Fast Write Burst 4T Max (No Slave Flow Control)
0	Disable..... default
1	Enable
1	Fast Write Fast Back to Back
0	Disable
1	Enable..... default
0	Fast Write Initial Block 1 Wait State
0	Disable..... default
1	Enable

	Rx45	CPU Write	CPU Write	
Bits	Address	Address		
<u>7-4</u>	<u>in Mem1</u>	<u>in Mem2</u>		<u>Fast Write Cycle Alignment</u>
x1xx	-	-		QW aligned, burstable
0000	-	-		DW aligned, nonburstable
x010	0	0		n/a
0010	0	1		DW aligned, non-burstable
x010	1	-		QW aligned, burstable
x001	0	0		n/a
x001	-	1		QW aligned, burstable
0001	1	0		DW aligned, non-burstable
x011	0	0		n/a
x011	1	-		QW aligned, burstable
x011	0	1		QW aligned, burstable
1000	-	-		QW aligned, non-burstable
1010	0	1		QW aligned, non-burstable
1001	1	0		QW aligned, non-burstable

Device 1 Offset 47-46 – PCI-to-PCI Bridge Device ID...RW

15-0 PCI-to-PCI Bridge Device ID default = 0000

Device 1 Offset 80 – Capability ID (01h).....RO

7-0 Capability ID always reads 01h

Device 1 Offset 81 – Next Pointer (00h).....RO

7-0 Next Pointer: Null always reads 00h

Device 1 Offset 82 – Power Mgmt Capabilities 1 (02h)...RO

7-0 Power Mgmt Capabilities always reads 02h

Device 1 Offset 83 – Power Mgmt Capabilities 2 (00h)...RO

7-0 Power Mgmt Capabilities always reads 00h

Device 1 Offset 84 – Power Mgmt Ctrl/Status (00h)..... RW

7-2 Reserved always reads 0

1-0 Power State

00 D0 default
 01 -reserved-
 10 -reserved-
 11 D3 Hot

Device 1 Offset 85 – Power Mgmt Status (00h)..... RO

7-0 Power Mgmt Status default = 00

Device 1 Offset 86 – P2P Br. Support Extensions (00h). RO

7-0 P2P Bridge Support Extensions default = 00

Device 1 Offset 87 – Power Management Data (00h) RO

7-0 Power Management Data default = 00

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FUNCTIONAL DESCRIPTION

Configuration Strapping

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ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Table 10. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes
T_C	Case operating temperature	0	85	$^{\circ}\text{C}$	1
T_S	Storage temperature	-55	125	$^{\circ}\text{C}$	1
V_{IN}	Input voltage	-0.5	$V_{RAIL} + 10\%$	Volts	1, 2
V_{OUT}	Output voltage	-0.5	$V_{RAIL} + 10\%$	Volts	1, 2

Note 1. Stress above the conditions listed may cause permanent damage to the device. Functional operation of this device should be restricted to the conditions described under operating conditions.

Note 2. V_{RAIL} is defined as the V_{CC} level of the respective rail. The CPU interface can be 3.3V or 2.5V. Memory can be 3.3V only. PCI can be 3.3V or 5.0V. Video can be 3.3V or 5.0V. Flat Panel can be 3.3V only. AGP can be 1.5V (4x transfer mode) or 3.3V (2x transfer mode).

DC Characteristics

$T_C = 0-85^{\circ}\text{C}$, $V_{RAIL} = V_{CC} \pm 5\%$, $V_{CORE} = 2.5\text{V} \pm 5\%$, $\text{GND}=0\text{V}$

Table 11. DC Characteristics

Symbol	Parameter	Min	Max	Unit	Condition
V_{IL}	Input Low Voltage	-0.50	0.8	V	
V_{IH}	Input High Voltage	2.0	$V_{CC}+0.5$	V	
V_{OL}	Output Low Voltage	-	0.55	V	$I_{OL}=4.0\text{mA}$
V_{OH}	Output High Voltage	2.4	-	V	$I_{OH}=-1.0\text{mA}$
I_{IL}	Input Leakage Current	-	± 10	μA	$0 < V_{IN} < V_{CC}$
I_{OZ}	Tristate Leakage Current	-	± 20	μA	$0.55 < V_{OUT} < V_{CC}$

Drive strength for selected output pins is programmable. See Device 0 Rx6D, B0[6], B1, B3, BE[7-6] and straps VAD4-5 for details.

Power Characteristics

$T_C = 0-85^{\circ}\text{C}$, $V_{\text{RAIL}} = V_{\text{CC}} \pm 5\%$, $V_{\text{CORE}} = 2.5\text{V} \pm 5\%$, $\text{GND}=0\text{V}$

Table 12. Power Characteristics – Internal and Interface Digital Logic

Symbol	Parameter	Typ	Max	Unit	Condition
I_{TT}	Power Supply Current – VTT			mA	Full-On Operation
I_{TTPOS}	Power Supply Current – VTT			mA	POS
I_{TTSTR}	Power Supply Current – VTT			mA	STR
I_{TTSOF}	Power Supply Current – VTT			mA	Soft-Off
I_{CCG}	Power Supply Current – VCCAGP			mA	Full-On Operation
I_{CCGPOS}	Power Supply Current – VCCAGP			mA	POS
I_{CCGSTR}	Power Supply Current – VCCAGP			mA	STR
I_{CCGSOF}	Power Supply Current – VCCAGP			mA	Soft-Off
I_{CCV}	Power Supply Current – VCCVL			mA	Full-On Operation
I_{CCVPOS}	Power Supply Current – VCCVL			mA	POS
I_{CCVSTR}	Power Supply Current – VCCVL			mA	STR
I_{CCVSOF}	Power Supply Current – VCCVL			mA	Soft-Off
I_{CCM}	Power Supply Current – VCCMEM			mA	Full-On Operation
I_{CCMPOS}	Power Supply Current – VCCMEM			mA	POS
I_{CCMSTR}	Power Supply Current – VCCMEM			mA	STR
I_{CCMSOF}	Power Supply Current – VCCMEM			mA	Soft-Off
I_{CC25}	Power Supply Current – VCC25			mA	Full-On Operation
I_{CC25POS}	Power Supply Current – VCC25			mA	POS
I_{CC25STR}	Power Supply Current – VCC25			mA	STR
I_{CC25SOF}	Power Supply Current – VCC25			mA	Soft-Off
I_{SUS25}	Power Supply Current – VSUS25			mA	Full-On Operation
I_{SUS25POS}	Power Supply Current – VSUS25			mA	POS
I_{SUS25STR}	Power Supply Current – VSUS25			mA	STR
I_{SUS25SOF}	Power Supply Current – VSUS25			mA	Soft-Off
I_{CCQQ}	Power Supply Current – VCCQQ			mA	Max operating frequency
P_D	Power Dissipation			W	Max operating frequency

Table 13. Power Characteristics – Analog and Reference Voltages

Symbol	Parameter	Typ	Max	Unit	Condition
I _{CCGTL}	Power Supply Current – GTLVREF			mA	Max operating frequency
I _{CCHAREF}	Power Supply Current – HAVREF			mA	Max operating frequency
I _{CCHDREF}	Power Supply Current – HDVREF			mA	Max operating frequency
I _{CCCHREF}	Power Supply Current – HCMPVREF			mA	Max operating frequency
I _{CCMREF}	Power Supply Current – MEMVREF			mA	Max operating frequency
I _{CCGREF}	Power Supply Current – AGPVREF			mA	Max operating frequency
I _{CCVLREF}	Power Supply Current – VLVREF			mA	Max operating frequency
I _{CCHCK}	Power Supply Current – VCCHCK			mA	Max operating frequency
I _{CCMCK}	Power Supply Current – VCCMCK			mA	Max operating frequency
I _{CCMDLL}	Power Supply Current – VCCMDLL			mA	Max operating frequency

AC Timing Specifications

AC timing specifications provided are based on external zero-pf capacitance load. Min/max cases are based on the following table:

Table 14. AC Timing Min / Max Conditions

Parameter	Min	Max	Unit
3.3V Power (I/O Pads, VCCQ for 2x transfer mode)	3.135	3.465	Volts
2.5V Power (Internal Logic)	2.375	2.625	Volts
1.5V Power (VCCQ for 4x transfer mode)	1.425	1.575	Volts
Case Temperature	0	85	°C

Drive strength for selected output pins is programmable and may effect AC timing specifications. See Device 0 Rx6D, B0[6], B1, B3, BE[7-6] and straps VAD4-5 for details.

[illegible]

Figure 4. Mechanical Specifications - 664-Pin Ball Grid Array Package