



Data Sheet

KM400A Desktop North Bridge

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VIA TECHNOLOGIES, INC.

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TABLE OF CONTENTS

REVISION HISTORY	I
TABLE OF CONTENTS.....	II
LIST OF FIGURES	IV
LIST OF TABLES	IV
PRODUCT FEATURES	1
OVERVIEW	6
KM400A OVERVIEW	6
SYSTEM POWER MANAGEMENT	7
3D GRAPHICS ENGINE.....	7
2D GRAPHICS ENGINE.....	7
MPEG VIDEO PLAYBACK.....	7
DVI MONITOR AND TV OUTPUT DISPLAY SUPPORT.....	7
HIGH SCREEN RESOLUTION DISPLAY SUPPORT	8
PINOUTS.....	9
PIN DESCRIPTIONS.....	13
REGISTERS.....	25
REGISTER OVERVIEW	25
MISCELLANEOUS I/O.....	29
CONFIGURATION SPACE I/O	29
REGISTER DESCRIPTIONS	30
Device 0 Header Registers - Host Bridge.....	30
Device 0 Configuration Registers - Host Bridge	32
V-Link Control	32
CPU Interface Control.....	35
DRAM Control.....	35
PCI Bus Control	41
GART / Graphics Aperture.....	43
AGP 2.0 Registers	44
AGP 3.0 Registers	45
AGP 2.0 / 3.0 Registers	47
V-Link Drive Control Registers	49
Power Management Registers	50
Extended Power Management	51
Host CPU Interface Control Registers.....	52
Frame Buffer Control	54
DRAM Above 4G Control	54
DRAM Drive Control Registers	55
BIOS Scratch.....	55
Miscellaneous.....	55
Device 1 Header Registers - PCI-to-PCI Bridge	56
Device 1 Configuration Registers - PCI-to-PCI Bridge.....	58
AGP Bus Control.....	58

FUNCTIONAL DESCRIPTION - INTEGRATED GRAPHICS	61
CONFIGURATION STRAPPING.....	61
PCI CONFIGURATION AND INTEGRATED AGP	61
PCI Configuration	61
PCI Subsystem ID.....	61
DISPLAY MEMORY	62
DISPLAY OUTPUT.....	63
SINGLE CRT OR PANEL DISPLAY	63
MULTIPLE DISPLAYS – CRT + 640x480 (VGA) PANEL.....	64
MULTIPLE DISPLAYS – CRT + 800x600 (SVGA) PANEL	65
MULTIPLE DISPLAYS – CRT + 1024x768 (XGA) PANEL.....	66
TV DISPLAY.....	67
ELECTRICAL SPECIFICATIONS	68
ABSOLUTE MAXIMUM RATINGS	68
DC CHARACTERISTICS.....	68
AC TIMING SPECIFICATIONS.....	68
MECHANICAL SPECIFICATIONS.....	69

LIST OF FIGURES

FIGURE 1. SYSTEM BLOCK DIAGRAM.....	6
FIGURE 2. BALL DIAGRAM (TOP VIEW).....	9
FIGURE 3. BALL DIAGRAM (TOP VIEW) – DIGITAL VIDEO OUTPUT ENABLED ON AGP PINS	10
FIGURE 4. GRAPHICS APERTURE ADDRESS TRANSLATION.....	43
FIGURE 5. MECHANICAL SPECIFICATIONS - 552-PIN HSBGA BALL GRID ARRAY PACKAGE WITH HEAT SPREADER.....	69

LIST OF TABLES

TABLE 1. SUPPORTED CRT AND PANEL SCREEN RESOLUTIONS.....	8
TABLE 2. PIN LIST (<u>NUMERICAL ORDER</u>).....	11
TABLE 3. PIN LIST (<u>ALPHABETICAL ORDER</u>)	12
TABLE 4. PIN DESCRIPTIONS	13
TABLE 5. REGISTERS	25
TABLE 6. SYSTEM MEMORY MAP.....	35
TABLE 7. MA MAP TYPE ENCODING	36
TABLE 8. MEMORY ADDRESS MAPPING TABLE	36
TABLE 9. VGA / MDA MEMORY / IO REDIRECTION	58
TABLE 10. DEFINITION OF STRAPPING BITS AT THE RISING EDGE OF THE RESET SIGNAL	61
TABLE 11. PCI SUBSYSTEM ID AND SUBSYSTEM VENDOR ID REGISTERS.....	61
TABLE 12. SUPPORTED FRAME BUFFER MEMORY CONFIGURATIONS.....	62
TABLE 13. SINGLE CRT / PANEL DISPLAY RESOLUTIONS	63
TABLE 14. SUPPORTED RESOLUTIONS – CRT + 640X480 (VGA) PANEL	64
TABLE 15. SUPPORTED RESOLUTIONS – CRT + 800X600 (SVGA) PANEL	65
TABLE 16. SUPPORTED RESOLUTIONS – CRT + 1024X768 (XGA) PANEL	66
TABLE 17. SUPPORTED RESOLUTIONS – TV DISPLAY	67
TABLE 18. ABSOLUTE MAXIMUM RATINGS	68
TABLE 19. DC CHARACTERISTICS.....	68
TABLE 20. AC TIMING MIN / MAX CONDITIONS.....	68

KM400A

NORTH BRIDGE

400 / 333 / 266 / 200 MHz AMD Athlon™ Front Side Bus
Integrated UniChrome 3D / 2D Graphics & Video Controller
Advanced DDR400 SDRAM Controller
533 MB/Sec V-Link Interface
External 8x / 4x AGP Bus

PRODUCT FEATURES

- **Defines Highly Integrated Solutions for Performance Desktop PC Designs**

- High performance UMA North Bridge: Integrated VIA KT600 and UniChrome 3D / 2D Graphics & Video Controllers in a single chip
- Advanced 64-bits DDR SDRAM controller supporting DDR400 / 333 / 266 SDRAM
- Multiple CRT, DVI monitor and TV-Out interfaces
- Combines with VIA VT8235 / VT8237 V-Link South Bridge for integrated 10 / 100 LAN, Audio, ATA133 IDE, LPC, USB 2.0 and Serial ATA (VT8237)
- 2.5V Core power
- 35 x 35mm HSBGA package (Ball Grid Array with Heat Spreader) with 552 balls
- Pin-compatible with VIA KM400 North Bridge

- **High Performance CPU Interface**

- Supports Socket-A (Socket-462) AMD Athlon / Duron processors
- Supports dynamically adjustable HSTL-like transceiver signal levels within a range from 1.1V to 1.7V
- Supports 400 / 333 / 266 / 200 MHz host address and data transfer rate
- Four-entry command queue for optimal CPU throughput
- Four-entry probe queue for probes from the system to the processor
- Eight-entry deep data and control queue separately for CPU-Memory-Read, CPU- Memory-Write and CPU-to-PCI operations
- Integrated CPU-to-DRAM write buffers and CPU-to-DRAM read prefetch buffers
- Supports WC (Write Combining) cycles
- Built-in Phase Lock Loop circuitry for optimal skew control within and between clocking regions

- **Full Featured Accelerated Graphics Port (AGP) Controller**

- AGP v3.0 compliant 8x / 4x transfer mode with Fast Write support
- 1.5V AGP I/O interface
- Pipelined split-transaction long-burst transfers up to 2.1 GB/sec
- Supports Side Band Addressing (SBA) mode
- Supports Flush / Fence commands
- Supports DBI (Dynamic Bus Inversion)
- Pseudo-synchronous AGP and CPU interfaces with optimal skew control
- Thirty-two level request queue for read and write
- Thirty-two level (quadwords) of read and write data FIFO separately
- Graphics Address Relocation Table (GART)
 - One level TLB structure
 - Sixteen entry fully associative page table
 - LRU replacement scheme

- **Advanced High-Performance 64-bit DDR SDRAM Controller**

- Supports DDR400 / 333 / 266 memory types with 2.5V SSTL-2 DRAM interface
- Supports mixed 64 / 128 / 256 / 512 / 1024 Mb SDRAM in x8 or x16 configurations
- Supports CL 2 / 2.5 for DDR266 / 333 and CL 2.5 / 3 for DDR400
- Supports 3 unbuffered double-sided DIMMs and up to 6 GB of physical memory
- Programmable I/O drive capability for memory address, data and control signals
- DRAM interface pseudo-synchronous with host CPU for optimal memory performance
- Concurrent CPU, AGP, internal graphics controller and V-Link access for minimum memory access latency
- Rank interleave, and up to 16-bank page interleave (i.e., 16 pages open simultaneously) based on LRU to effectively reduce memory access latency
- Seamless DRAM command scheduling for maximum DRAM bus utilization (e.g., precharge other banks while accessing the current bank)
- CPU Read-Around-Write capability for non-stalled operation
- Speculative memory read before snoop result to reduce PCI master memory read latency
- Supports burst read and write operations with burst length of 4 or 8
- Optional dynamic Clock Enable (CKE) control for DRAM power reduction during normal system state (S0)
- Supports self-refresh and CAS-before-RAS DRAM refresh with staggered RAS timing

- **High Bandwidth 533 MB/Sec 8-bit V-Link Host Controller**

- Supports 66 MHz, 4x and 8x transfer modes, V-Link Host interface with 533 MB/sec total bandwidth
- Half duplex transfers with separate command / strobe for 4x8 bit mode and full duplex for 8x4 bit mode
- Request / Data split transaction
- Transaction assurance for V-Link Host-to-Client access eliminates V-Link Host-Client Retry cycles
- Intelligent V-Link transaction protocol to minimize data wait-state and throttle transfer latency to avoid data overflow
- Highly efficient V-Link arbitration with minimum overhead

- **Advanced System Power Management Support**

- ACPI 2.0 and PCI Bus Power Management 1.1 compliant
- Supports Suspend-to-DRAM (STR) and DRAM self refresh
- Supports dynamic Clock Enable (CKE) control for DRAM power reduction during normal system state (S0)
- Supports SMI, SMM and STPCLK mechanisms
- Supports AMD PowerNow! Technology
- Low-leakage I/O pads

- **Integrated Graphics with 2D / 3D / Video Controllers**

- Optimized Unified Memory Architecture (UMA)
- Supports 16 / 32 / 64 MB Frame Buffers sizes
- 133 MHz Graphics Engine Clock
- Internal AGP 8x performance
- Two independent 128-bit data paths between North Bridge and graphics core to improve video performance, one for frame buffer access and one for texture / command access
- PCI v2.2 Host Bus compliant
- AGP v3.0 compliant

2D Acceleration Features

- Hardware 2D rotation
- 128-bit 2D graphics engine
- Supports ROP3, 256 operations
- Supports 8bpp, 15/16bpp and 32bpp color depth modes
- BitBLT (Bit Block Transfer) functions including alpha BLTs
- High-color hardware cursor (64x64x16bpp)
- Color expansion, source Color Key and destination Color Key
- Bresenham line drawing / style line function
- Transparency mode
- Window clipping
- Text function

3D Acceleration Features

3D Graphics Processor

- 128-bit 3D graphics engine
- Dual pixel rendering pipes
- Dual texture units
- Floating-point setup engine
- Internal full 32-bit ARGB format for high rendering quality
- 4K Texture Cache

Capability

- Supports ROP2
- Supports various texture formats, including: 16 / 32bbp ARGB, 8bbp Palletized (ARGB) and YUV 422 / 420
- Texture sizes up to 2048x2048
- High quality texture filter for Nearest, Linear, Bi-linear, Tri-linear and Anisotropic modes
- Flat and Gouraud shading
- Vertex Fog and Fog Table
- Z-Bias, LOD-Bias, Edge Anti-aliasing and Alpha Blending
- Hardware Back-Face culling
- Specular Lighting

Performance

- Two textures per pass
- Triangle rate up to 3 million triangles per second
- Pixel rate up to 133 million pixels per second for 2 textures each
- Texel bilinear fill rate up to 266 million texels per second
- High quality dithering

Video Acceleration Features

High Quality Video Processor

- High quality scaler (up or down) for both horizontal and vertical scaling (linear interpolation for horizontal and vertical p-scaling and filtering for horizontal and vertical down-scaling)
- 1 set of Color and Chroma key support
- Color enhancement for contrast, hue, saturation and brightness
- YUV-to-RGB color space conversion
- Bob, weave de-interlacing mode and advanced de-interlacing to improve video quality
- Supports video window overlay
- Hardware sub-picture blending

MPEG Video Playback

- MPEG-2 hardware VLD (Variable Length Decode), iDCT and motion compensation for full speed DVD and MPEG-2 playback at full D1 resolution
- High quality DVD and streaming video playback
- DVD playback auto-flipping
- DVD sub-picture playback overlay

Dual View™ Capability

- WinXP, WinME and Win98 multi-monitor, extended desktop support
- Provides two independent display engines, each of which can display completely different information at different resolutions, pixel depth and refresh rates
- Improved display flexibility with simultaneous CRT / DVI, CRT / TV, DVI / TV and other combined operations

Full Software Support

- Microsoft DirectX 7.0, 8.0 and 9.0 compatible
- Supports OpenGL™
- Drivers for major operating systems and APIs: Windows® 9x/ME, Windows 2000, Windows XP, Direct3D™, DirectDraw™ and DirectShow™ and OpenGL™ ICD for Windows 9x/ME and XP

- **Extensive Display Support for External Video Output**

- CRT display interface
- Digital Video Port supporting TV-Out interface to TV encoder
- 12-bit interface to external TMDS transmitter for driving a DVI monitor
- 12-bit TV-Out interface to TV encoder

CRT Display

- CRT display interface with 24-bit true-color RAMDAC up to 250 MHz pixel rate with gamma correction capability
- Supports CRT resolutions up to 1600x1200

12-bit TMDS Transmitter Interface

- 12-bit, 1.5V low-swing, DVO interface for connecting DVI Monitor through TMDS transmitter
- 12-bit DDR and clock rate up to 165 MHz
- Built-in digital phase adjuster to fine tune signal timing between clock and data bus

TV-Out interface

- 12-bit DVO interface to external TV encoder for NTSC or PAL TV display
- 1.5V signaling on GDVP0 port or 3.3V signaling on DVP0 port

- **Advanced Graphics Power Management Support**

- Built-in reference voltage generator and monitor sense circuits
- Automatic panel power sequencing and VESA DPMS (Display Power Management Signaling) CRT power-down
- External I/O signal controls enabling of graphics controller into standby / suspend-off state
- Dynamic clock gating for inactive functions to achieve maximum power savings
- I²C Serial Bus and DDC Monitor Communications for Plug-and-Play configuration

OVERVIEW

The KM400A is a high performance, cost-effective and energy efficient UMA North Bridge with integrated UniChrome graphics / video controller used for the implementation of desktop personal computer systems based on 400 / 333 / 266 / 200 CPU host bus ("Front Side Bus") for Socket-A AMD Athlon™ and AMD Duron™ processors.

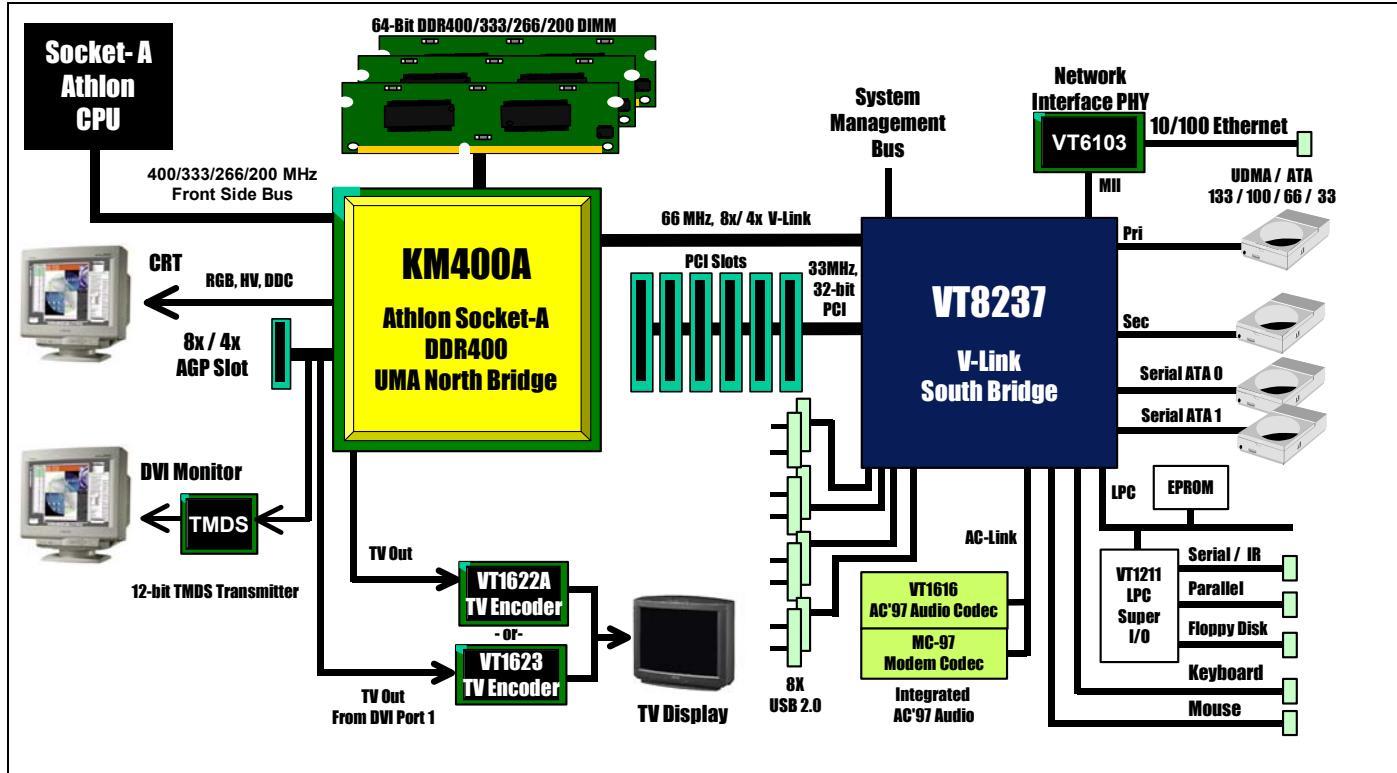


Figure 1. System Block Diagram

The complete desktop chipset consists of the KM400A North Bridge and the VT8237 V-Link South Bridge. The KM400A integrates VIA's most advanced system controller with high-performance UniChrome 3D / 2D graphics and video controller, LCD panel, DVI monitor and TV-Out interfaces. The KM400A provides superior performance between the CPU, DRAM, V-Link and internal or external AGP 8x graphics controller with pipelined, burst and concurrent operation. The VT8237 is a highly integrated peripheral controller which includes V-Link-to-PCI / V-Link-to-LPC controllers, Ultra DMA IDE controllers, Serial ATA controller, USB2.0 host controller, 10/100Mb networking MAC, AC97, and system power management controllers.

KM400A Overview

The KM400A supports 400 / 333 / 266 / 200 MHz FSB AMD Athlon XP and Duron processors; it implements a deep command (4-level), probe (4-level) and memory read/write/PCI command (8-level each) queues for optimal system performance. AMD PowerNow! technology is supported to reduce system power consumption while sustaining CPU's processing power.

The AGP controller is AGP v3.0 compliant with up to 2.1GB/second data transfer rate capability. It supports pseudo-synchronous AGP and CPU interface to maximize system performance. Deep read and write (256 bytes each) FIFO are integrated for optimal bus utilization and minimum data transfer latency.

The KM400A supports dual 64-bit memory channel and up to 3 double-sided DDR400 / 333 / 266 SDRAM DIMMs for 6 GB maximum physical memory. The DDR SDRAM interface allows zero wait-state data transfer bursting between the DRAM and memory controller's data buffers. The different banks of DRAM can be composed of an arbitrary mixture of 64 / 128 / 256 / 512 / 1024 Mb SDRAM in x8 or x16 configurations. The DRAM controller can run either synchronous or pseudo-synchronous with the host CPU bus.

The KM400A North Bridge interfaces to the South Bridge through a high speed (up to 533 MB/sec) 8x 66 MHz Data Transfer interconnect bus called V-Link interface. Deep pre-fetch and post-write buffers are included to allow for concurrent CPU and V-

Link operation. The combined KM400A North Bridge and VT8237 South Bridge system supports enhanced PCI bus commands such as “Memory-Read-Line”, “Memory-Read-Multiple” and “Memory-Write-Invalid” commands to minimize snoop overhead. In addition, advanced features are supported such as CPU write-back forward to PCI master and CPU write-back merged with PCI post-write buffers to minimize PCI master read latency and DRAM utilization. Delay transaction and read caching mechanisms are also implemented for further improvement of overall system performance.

The KM400A North Bridge also integrates a 128-bit graphics controller into the chip. This brings mainstream graphics performance to the Value PC with leading-edge 2D, 3D and DVD video acceleration into a cost effective package. Based on its capabilities, the KM400A is an ideal solution for the consumer, corporate desktop users and entry-level professionals.

System Power Management

For sophisticated power management, the KM400A supports dynamic CKE control to minimize DDR SDRAM power consumption during normal system state (S0). A separate suspend power plane is implemented for the memory control logic for Suspend-to-DRAM state. AMD PowerNow! Technology enables minimization of CPU power consumption while sustaining processing power. The KM400A graphics controller implements dynamic clock gating for inactive functions to achieve maximum power saving. The system can be switched to standby or suspend states to further reduce power consumption when idle. Automatic panel power sequencing and VESA DPMS (Display Power Management Signaling) CRT power-down are supported. Coupled with the VT8237 south bridge chip, a complete power conscious PC main board can be implemented with no external glue logic.

3D Graphics Engine

Featuring an integrated 128-bit 3D graphics engine, the KM400A North Bridge utilizes a highly pipelined architecture that provides high performance along with superior image quality. Several new features enhance the 3D architecture, including two pixel rendering pipes, single-pass multitexturing, bump and cubic mapping, texture compression, edge anti-aliasing, vertex fog and fog table, hardware back-face culling, specular lighting, anisotropic filtering, and an 8-bit stencil buffer. The chip also offers the industry's only simultaneous usage of single-pass multitexturing and single-cycle trilinear filtering – enabling stunning image quality without performance loss. Image quality is further enhanced with true 32-bit color rendering throughout the 3D pipeline to produce more vivid and realistic images. The advanced triangle setup engine provides industry leading 3D performance for a realistic user experience in games and other interactive 3D applications.

2D Graphics Engine

The KM400A North Bridge's advanced 128-bit 2D graphics engine delivers high-speed 2D acceleration for productivity applications. The enhanced 2D architecture with direct access frame buffer capability optimizes UMA performance and provides acceleration of all color depths.

MPEG Video Playback

The KM400A North Bridge provides the ideal architecture for high quality MPEG-2 based video applications. For MPEG video playback, the integrated video engine offloads the CPU by performing planar-to-packed format conversion and motion video compensation tasks, while its enhanced scaling algorithm delivers incredible full-screen video playback.

DVI Monitor and TV Output Display Support

Two 12-bit “Display Port” interfaces are provided (with functions multiplexed with AGP interface functions) plus a dedicated 12-bit display port interface. Multiplexing display functions with AGP bus allows desktop systems to support an external AGP connector for future performance upgrade through external graphics controller. It also allows add-in cards to be designed with an AGP-compatible connector for implementation of the display interface logic to reduce cost in the base (CRT-only) configuration. In value system configurations, external AGP upgrade capability is not normally required by the system, allowing all the AGP pins to be used for implementation of very flexible display functions.

One of the two AGP-multiplexed “Display Ports” implements 12-bit TMDS transmitter interface, and is normally connected to external TMDS transmitter (such as VIA VT1632) to drive external DVI monitor via DVI interface connector, while the other AGP-multiplexed “Display Port” provides 12-bit interface to external TV encoder chip (such as VIA VT1623 and VT1623M) for display of video on a TV display. The dedicated 12-bit interface may optionally be configured for support of external TV encoder (such as VIA VT1622A and VT1622AM) as well.

The flexible display configurations of the KM400A allow support of a DVI monitor (TMDS interface), TV display and CRT display at the same time. Internally the KM400A North Bridge provides two separate display engines; if two display devices are connected, each can display completely different information at different resolution, pixel depth and refresh rate. The maximum display resolutions supported for one display device are listed in the table below. If more than one display is implemented (i.e., if both display engines are functioning at the same time), then available memory bandwidth may limit the display resolutions supported on one or both displays. This will be dependent on many factors including primarily clock rates and memory speeds (contact VIA for additional information).

High Screen Resolution Display Support

Resolutions Supported	Resolution Name	Pixel Depths Supported	System Memory Frame Buffer Size		
			16 MB	32 MB	64 MB
640x480 (4:3)	VGA	8 / 16 / 32	√	√	√
800x600 (4:3)	SVGA	8 / 16 / 32	√	√	√
1024x768 (4:3)	XGA	8 / 16 / 32	√	√	√
1280x1024 (5:4)	SXGA	8 / 16 / 32	√	√	√
1400x1050 (4:3)	SXGA+	8 / 16 / 32	√	√	√
1600x1200 (4:3)	UXGA	8 / 16 / 32	√	√	√

Table 1. Supported CRT and Panel Screen Resolutions

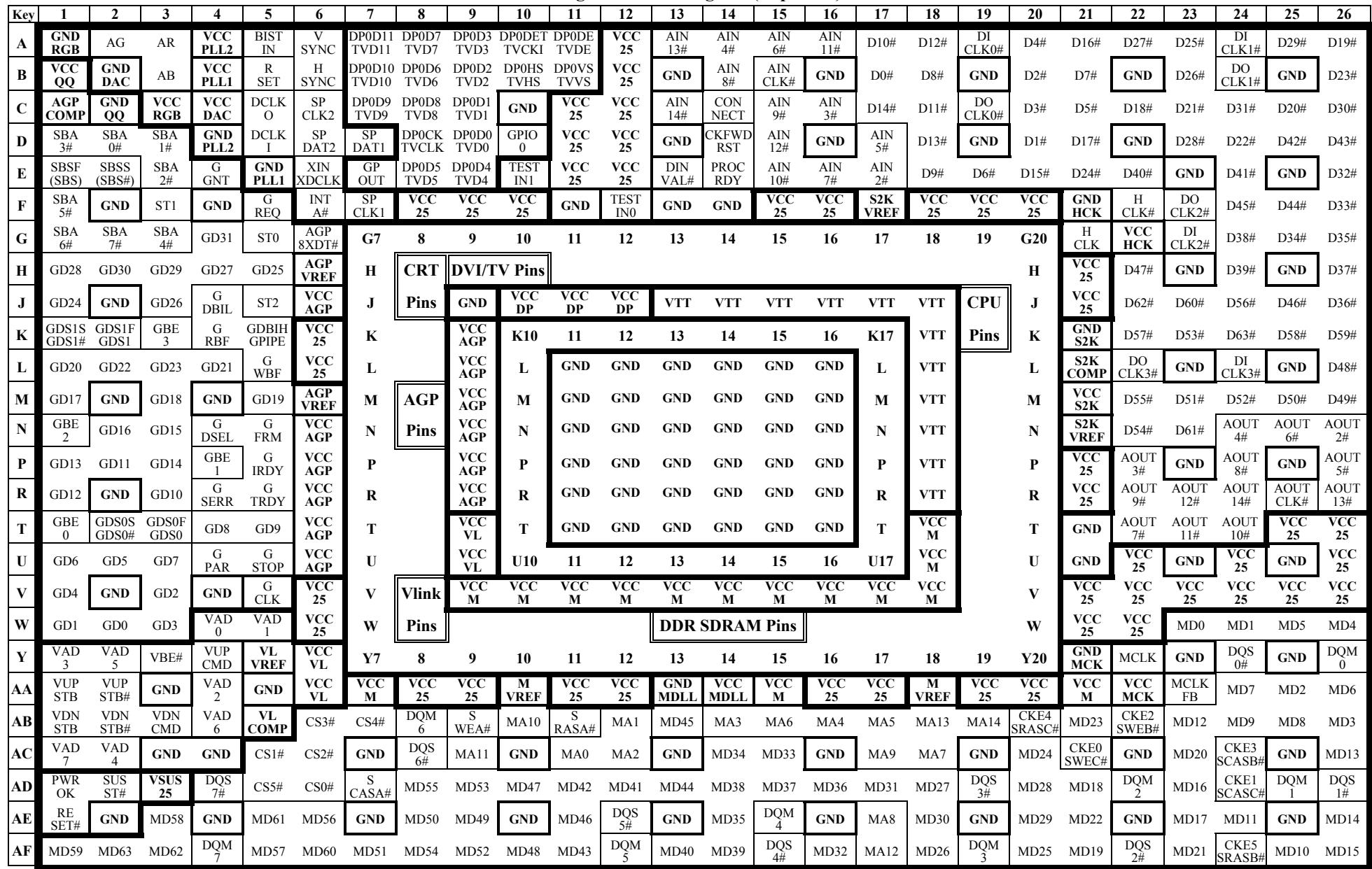
PINOUTS
Figure 2. Ball Diagram (Top View)


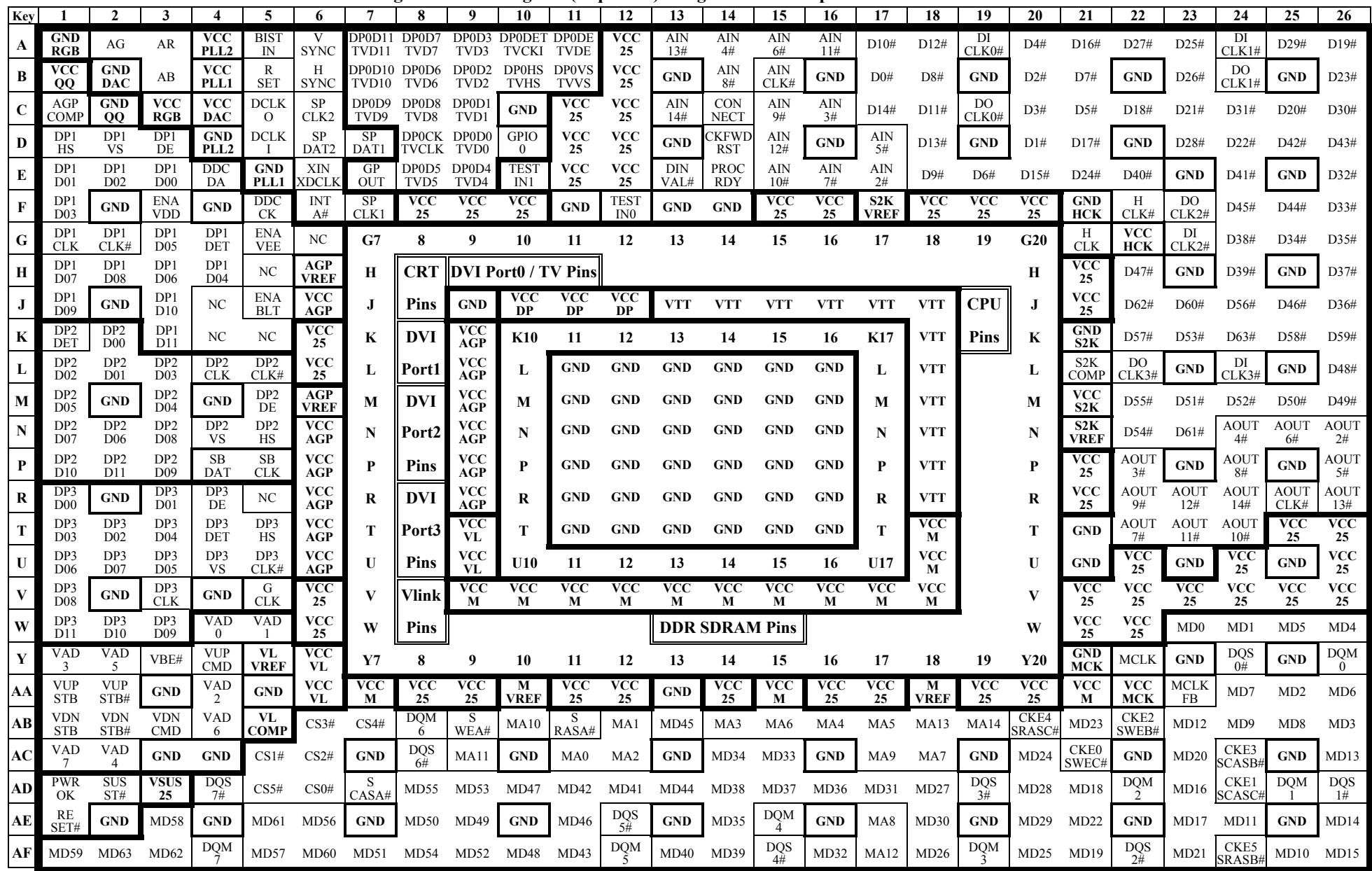
Figure 3. Ball Diagram (Top View) – Digital Video Output Enabled on AGP Pins


Table 2. Pin List (Numerical Order)

Pin #	Pin Name	Pin #	Pin Names	Pin #	Pin Name						
A01	P GNDRGB	D03	I SBA1#/ DP1DE	G05	O ST0 / ENAVEE	P01	IO GD13 / DP2D10	Y23	P GND	AC25	P GND
A02	O AG	D04	P GNDPLL2	G06	I AGP8XDT#	P02	IO GD11 / DP2D11	Y24	O DQS0#	AC26	IO MD13
A03	O AR	D05	I DCLKI	G21	I HCLK	P03	IO GD14 / DP2D09	Y25	P GND	AD01	I PWROK
A04	P VCCPLL2	D06	IO SPDAT2	G22	P VCCHCK	P04	IO GBE1 / SBDA	Y26	O DQM0	AD02	I SUSST#
A05	I BISTIN	D07	IO SPDAT1	G23	O DICLK2#	P05	IO GIRDY / SBCK	AA01	I VUPSTB	AD03	P VSUS25
A06	O VSYNC	D08	O DP0CLK/TVCK	G24	IO D38#	P06	P VCCAGP	AA02	I VUPSTB#	AD04	O DQS7#
A07	O DP0D11 / TVD11	D09	O DP0D00 / TVD0	G25	IO D34#			AA03	P GND	AD05	O CSS#
A08	O DP0D07 / TVD7	D10	IO GPIO0	G26	IO D35#			AA04	IO VAD2	AD06	O CS0#
A09	O DP0D03 / TVD3	D11	P VCC25	H01	IO GD28 / DP1D7			AA05	P GND	AD07	O SCASAS# / strap
A10	O DP0DET/TVCK1	D12	P VCC25	H02	IO GD30 / DP1D8			AA06	P VCCVL	AD08	IO MD55
A11	IO DP0DE / TVDE	D13	P GND	H03	IO GD29 / DP1D6			AA07	P VCCM	AD09	IO MD53
A12	P VCC25	D14	O CFWRDST	H04	IO GD27 / DP1D4			AA08	P VCC25	AD10	IO MD47
A13	O AIN13#	D15	O AIN12#	H05	IO GD25			AA09	P VCC25	AD11	IO MD42
A14	O AIN04#	D16	P GND	H06	P AGPVREF			AA10	P MEMVREF	AD12	IO MD41
A15	O AIN06#	D17	O AIN05#	H21	P VCC25			AA11	P VCC25	AD13	IO MD44
A16	O AIN11#	D18	IO D13#	H22	IO D47#			AA12	P VCC25	AD14	IO MD38
A17	IO D10#	D19	P GND	H23	P GND			AA13	P GND	AD15	IO MD37
A18	IO D12#	D20	IO D01#	H24	IO D39#			AA14	P VCC25	AD16	IO MD36
A19	O DICLK0#	D21	IO D17#	H25	P GND			AA15	P VCCM	AD17	IO MD31
A20	IO D04#	D22	P GND	H26	IO D37#			AA16	P VCC25	AD18	IO MD27
A21	IO D16#	D23	IO D28#	J01	IO GD24 / DP1D9			AA17	P VCC25	AD19	O DOS3#
A22	IO D27#	D24	IO D22#	J02	P GND			AA18	P MEMVREF	AD20	IO MD28
A23	IO D25#	D25	IO D42#	J03	IO GD26 / DP1D10			AA19	P VCC25	AD21	IO MD18
A24	O DICLK1#	D26	IO D43#	J04	IO GDBIL			AA20	P VCC25	AD22	O DQM2
A25	IO D29#	E01	I SBSF / DP1D01	J05	O ST2 / ENABL T			AA21	P VCCM	AD23	IO MD16
A26	IO D19#	E02	I SBSS / DP1D02	J06	P VCCAGP			AA22	P VCCMCK	AD24	O CKE1 / SCASC#
B01	P VCCOO	J21	P VCC25								
B02	P GNDDAC	J22	IO D62#								
B03	O AB	J23	IO D60#								
B04	P VCCPL1	J24	IO D56#								
B05	A RSET	J25	IO D46#								
B06	O HSYNC	J26	IO D36#								
B07	O DP0D10 / TVD10	K01	O GDS15/DP2D2ET								
B08	O DP0D06 / TVD6	K02	IO GDS1F/DP2D00								
B09	O DP0D02 / TVD2	K03	IO GBE3 / DP1D11								
B10	O DP0HS / TVHS	K04	I GRBF								
B11	O DP0VS / TVVS	K05	I GDBIH / GPIPE								
B12	P VCC25	K06	P VCC25								
B13	P GND	K21	P GNDS2K								
B14	O AIN08#	K22	IO D57#								
B15	O AINCLK#	K23	IO D53#								
B16	P GND	K24	IO D63#								
B17	IO D00#	K25	IO D58#								
B18	IO D08#	K26	IO D59#								
B19	P GND	L01	IO GD20 / DP2D02								
B20	IO D02#	L02	IO GD22 / DP2D01								
B21	IO D07#	L03	IO GD23 / DP2D03								
B22	P GND	L04	IO GD21 / DP2CK								
B23	IO D26#	L05	I GWBF/DP2CK#								
B24	I DOCLK1#	L06	P VCC25								
B25	P GND	F01	I SBA5#/ DP1D3								
B26	IO D23#	F02	P GND								
C01	AI AGCOMP	F03	O ST1 / ENAVDD								
C02	P GNDQQ	F04	P GND								
C03	P VCCRGB	F05	I GREO / DDCCK								
C04	P VCCDAC	F06	O INTA#								
C05	O DCLK0	F07	IO SPCLK1								
C06	IO SPCLK2	F08	P VCC25								
C07	O DP0D09 / TVD9	F09	P VCC25								
C08	O DP0D08 / TVD8	F10	P VCC25								
C09	O DP0D01 / TVD1	F11	P GND								
C10	P GND	F12	I TESTIN0								
C11	P VCC25	F13	P GND								
C12	P VCC25	F14	P GND								
C13	O AIN14#	F15	P VCC25								
C14	O CONNECT	F16	P VCC25								
C15	O AIN09#	F17	P S2KVREF								
C16	O AIN03#	F18	P VCC25								
C17	IO D14#	F19	P VCC25								
C18	IO D11#	F20	P VCC25								
C19	I DOCLK0#	F21	P GNDHCK								
C20	IO D03#	F22	I HCLK#								
C21	IO D05#	F23	I DOCLK2#								
C22	IO D18#	F24	IO D45#								
C23	IO D21#	F25	IO D44#								
C24	IO D31#	F26	IO D33#								
C25	IO D20#	G01	I SBA6#/ DP1CK								
C26	IO D30#	G02	I SBA7#/ DP1CK#								
D01	I SBA3#/ DP1HS	G03	I SBA4#/ DP1VS								
D02	I SBA0#/ DP1VS	G04	IO GD31 / DP1DET								
		N21	P S2KVREF								
		N22	IO D54#								
		N23	IO D61#								
		N24	I AOUT04#								
		N25	I AOUT06#								
		N26	I AOUT02#								
		Y21	P GNDMCK								
		Y22	O MCLK								

Center VTT Pins (12 pins): J13-18, K18, L18, M18, N18, P18, R18

Center VCCVL Pin (2 pins) T9, U9

Center VCCAGP pins (6 pins): K9, L9, M9, N9, P9, R9

Center GND Pins (37 pins): J9, L11-16, M11-16, N11-16, P11-16, R11-16, T11-16

Center VCCDP Pins (3 pins): J10-12

Center VCCM Pins (12 pins): T18, U18, V9-18

Table 3. Pin List (Alphabetical Order)

Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Names	Pin #	Pin Name
B03	O AB	C26	IO D30#	N01	IO GBE2 / DP2D07	AA03	P GND	AF23	IO MD21	Y02	IO VAD5
A02	O AG	C24	IO D31#	K03	IO GBE3 / DP1D11	AA05	P GND	AE21	IO MD22	AB04	IO VAD6
G06	I AGP8XDT#	E26	IO D32#	V05	I GCLK	AA13	P GND	AB21	IO MD23	AC01	IO VAD7
C01	AI AGPCOMP	F26	IO D33#	W02	IO GD00 / DP3D10	AC03	P GND	AC20	IO MD24	Y03	IO VBE#
H06	P AGPVREF	G25	IO D34#	W01	IO GD01 / DP3D11	AC04	P GND	AF20	IO MD25	A12	P VCC25
M06	P AGPVREF	G26	IO D35#	V03	IO GD02 / DP3CK	AC07	P GND	AF18	IO MD26	B12	P VCC25
E17	O AIN02#	J26	IO D36#	W03	IO GD03 / DP3D09	AC10	P GND	AD18	IO MD27	C11	P VCC25
C16	O AIN03#	H26	IO D37#	V01	IO GD04 / DP3D08	AC13	P GND	AD20	IO MD28	C12	P VCC25
A14	O AIN04#	G24	IO D38#	U02	IO GD05 / DP3D07	AC16	P GND	AE20	IO MD29	D11	P VCC25
D17	O AIN05#	H24	IO D39#	U01	IO GD06 / DP3D06	AC19	P GND	AE18	IO MD30	D12	P VCC25
A15	O AIN06#	E22	IO D40#	U03	IO GD07 / DP3D05	AC22	P GND	AD17	IO MD31	E11	P VCC25
E16	O AIN07#	E24	IO D41#	T04	IO GD08 / DP3DET	AC25	P GND	AF16	IO MD32	E12	P VCC25
B14	O AIN08#	D25	IO D42#	T05	IO GD09 / DP3HS	AE02	P GND	AC15	IO MD33	F08	P VCC25
C15	O AIN09#	D26	IO D43#	R03	IO GD10 / DP3D01	AE04	P GND	AC14	IO MD34	F09	P VCC25
E15	O AIN10#	F25	IO D44#	P02	IO GD11 / DP2D11	AE07	P GND	AE14	IO MD35	F10	P VCC25
A16	O AIN11#	F24	IO D45#	R01	IO GD12 / DP3D00	AE10	P GND	AD16	IO MD36	F15	P VCC25
D15	O AIN12#	J25	IO D46#	P01	IO GD13 / DP2D10	AE13	P GND	AD15	IO MD37	F16	P VCC25
A13	O AIN13#	H22	IO D47#	P03	IO GD14 / DP2D09	AE16	P GND	AD14	IO MD38	F18	P VCC25
C13	O AIN14#	L26	IO D48#	N03	IO GD15 / DP2D08	AE19	P GND	AF14	IO MD39	F19	P VCC25
B15	O AINCLK#	M26	IO D49#	N02	IO GD16 / DP2D06	AE22	P GND	AF13	IO MD40	F20	P VCC25
N26	I AOUT02#	M25	IO D50#	M01	IO GD17 / DP2D05	AE25	P GND	AD12	IO MD41	H21	P VCC25
P22	I AOUT03#	M23	IO D51#	M03	IO GD18 / DP2D04	B02	P GNDDAC	AD11	IO MD42	J21	P VCC25
N24	I AOUT04#	M24	IO D52#	M05	IO GD19 / DP2DDE	F21	P GNDHCK	AF11	IO MD43	K06	P VCC25
P26	I AOUT05#	K23	IO D53#	L01	IO GD20 / DP2D02	Y21	P GNDMCK	AD13	IO MD44	L06	P VCC25
N25	I AOUT06#	N22	IO D54#	L04	IO GD21 / DP2CK	E05	P GNDPLL1	AB13	IO MD45	P21	P VCC25
T22	I AOUT07#	M22	IO D55#	L02	IO GD22 / DP2D01	D04	P GNDPLL2	AE11	IO MD46	R21	P VCC25
P24	I AOUT08#	J24	IO D56#	L03	IO GD23 / DP2D03	C02	P GNDQQ	AD10	IO MD47	T25	P VCC25
R22	I AOUT09#	K22	IO D57#	J01	IO GD24 / DP1D9	A01	P GNDRGB	AF10	IO MD48	T26	P VCC25
T24	I AOUT10#	K25	IO D58#	H05	IO GD25	K21	P GNDRS2K	AE09	IO MD49	U22	P VCC25
T23	I AOUT11#	K26	IO D59#	J03	IO GD26 / DP1D10	U04	IO GPAR / DP3VS	AE08	IO MD50	U24	P VCC25
R23	I AOUT12#	J23	IO D60#	H04	IO GD27 / DP1D04	D10	IO GPIOI	AF07	IO MD51	U26	P VCC25
R26	I AOUT13#	N23	IO D61#	H01	IO GD28 / DP1D7	E07	IO GPOUT	AF09	IO MD52	V06	P VCC25
R24	I AOUT14#	J22	IO D62#	H03	IO GD29 / DP1D6	K04	I GRBF	AD09	IO MD53	V21	P VCC25
R25	I AOUTCLK#	K24	IO D63#	H02	IO GD30 / DP1D8	F05	I GREQ / DDCCK	AF08	IO MD54	V22	P VCC25
A03	O AR	D05	I DCLKI	G04	IO GD31 / DP1DET	R04	IO GSERR / DP3DE	AD08	IO MD55	V23	P VCC25
A05	I BISTIN	C05	O DCLKO	K05	I GDBIH / GPIPE	U05	IO GSTOP/DP3CK#	AE06	IO MD56	V24	P VCC25
D14	O CFWRDST	A19	O DICLK0#	J04	I GDBIL	R05	I GTRDY	AF05	IO MD57	V25	P VCC25
AC21	O CKE0 / SWEC#	A24	O DICLK1#	T03	IO GDS0F / DP3D04	L05	I GWBF / DP2CK#	AE03	IO MD58	V26	P VCC25
AD24	O CKE1 / SCASC#	G23	O DICLK2#	T02	IO GDS0S / DP3D02	G21	I HCLK	AF01	IO MD59	W06	P VCC25
AB22	O CKE2 / SWEB#	L24	O DICLK3#	K02	IO GDS1F / DP2D00	F22	I HCLK#	AF06	IO MD60	W21	P VCC25
AC24	O CKE3 / SCASB#	E13	O DINVAL#	K01	IO GDS1S / DP2DET	B06	O HSYNC	AE05	IO MD61	W22	P VCC25
AB20	O CKE4 / SRASC#	C19	I DOCLK0#	N04	IO GDS1L / DP2VS	F06	O INTA#	AF03	IO MD62	AA08	P VCC25
AF24	O CKE5 / SRASB#	B24	I DOCLK1#	N05	IO GFRM / DP2HS	AC11	O MA00 / strap	AF02	IO MD63	AA09	P VCC25
C14	O CONNECT	F23	I DOCLK2#	E04	IO GGNT / DDCCA	AB12	O MA01 / strap	AA10	P MEMVREF	AA11	P VCC25
AD06	O CS0#	L22	I DOCLK3#	P05	IO GIRDY / SBCK	AC12	O MA02 / strap	AA18	P MEMVREF	AA12	P VCC25
AC05	O CS1#	D08	IO DP0CLK / TVCLK	B13	P GND	AB14	O MA03 / strap	E14	I PROCRDY	AA14	P VCC25
AC06	O CS2#	D09	IO DP0D00 / TVD0	B16	P GND	AB16	O MA04 / strap	AD01	I PWROK	AA16	P VCC25
AB06	O CS3#	C09	IO DP0D01 / TVD1	B19	P GND	AB17	O MA05 / strap	AE01	I RESET#	AA17	P VCC25
AB07	O CS4#	B09	IO DP0D02 / TVD2	B22	P GND	AB15	O MA06 / strap	B05	A RESET	AA19	P VCC25
AD05	O CS5#	A09	IO DP0D03 / TVD3	B25	P GND	AC18	O MA07 / strap	L21	A S2KCOMP	AA20	P VCC25
B17	IO D00#	E09	IO DP0D04 / TVD4	C10	P GND	AE17	O MA08 / strap	F17	P S2KVREF	J06	P VCCAGP
D20	IO D01#	E08	IO DP0D05 / TVD5	D13	P GND	AC17	O MA09 / strap	N21	P S2KVREF	N06	P VCCAGP
B20	IO D02#	B08	IO DP0D06 / TVD6	D16	P GND	AB10	O MA10 / strap	D02	I SBA0# / DP1VS	P06	P VCCAGP
C20	IO D03#	A08	IO DP0D07 / TVD7	D19	P GND	AC09	O MA11 / strap	D03	I SBA1# / DP1DE	R06	P VCCAGP
A20	IO D04#	C08	IO DP0D08 / TVD8	D22	P GND	AF17	O MA12 / strap	E03	I SBA2# / DP1D00	T06	P VCCAGP
C21	IO D05#	C07	IO DP0D09 / TVD9	E23	P GND	AB18	O MA13 / strap	D01	I SBA3# / DP1HS	U06	P VCCAGP
E19	IO D06#	B07	IO DP0D10 / TVD10	E25	P GND	AB19	O MA14 / strap	G03	I SBA4# / DP1VS	C04	P VCCDAC
B21	IO D07#	A07	IO DP0D11 / TVD11	F02	P GND	Y22	O MCLK	F01	I SBA5# / DP1D3	G22	P VCCCHCK
B18	IO D08#	A11	IO DP0DE / TVDE	F04	P GND	AA23	I MCLKFB	G01	I SBA6# / DP1CK	AA07	P VCCM
E18	IO D09#	A10	IO DP0DET / TVCKI	F11	P GND	W23	IO MD00	G02	I SBA7# / DP1CK#	AA15	P VCCM
A17	IO D10#	B10	IO DP0HS / TVHS	F13	P GND	W24	IO MD01	E01	I SBSF / DP1D01	AA21	P VCCM
C18	IO D11#	B11	IO DP0VS / TVVS	F14	P GND	AA25	IO MD02	E02	I SBSS / DP1D02	AA22	P VCCMCK
A18	IO D12#	Y26	O DQM0	H23	P GND	AB26	IO MD03	AD07	O SCASA# / strap	B04	P VCCPLL1
D18	IO D13#	AD25	O DQM1	H25	P GND	W26	IO MD04	F07	IO SPCLK1	A04	P VCCPLL2
C17	IO D14#	AD22	O DQM2	J02	P GND	W25	IO MD05	C06	IO SPCLK2	B01	P VCCQQ
E20	IO D15#	AF19	O DQM3	L23	P GND	AA26	IO MD06	D07	IO SPDAT1	C03	P VCCRGB
A21	IO D16#	AE15	O DQM4	L25	P GND	AA24	IO MD07	D06	IO SPDAT2	M21	P VCCS2K
D21	IO D17#	AF12	O DQM5	M02	P GND	AB25	IO MD08	AB11	O SRASA# / strap	Y06	P VCCVL
C22	IO D18#	AB08	O DQM6	M04	P GND	AB24	IO MD09	G05	O ST0 / ENAVEE	AA06	P VCCVL
A26	IO D19#	AF04	O DQM7	P23	P GND	AF25	IO MD10	F03	O ST1 / ENAVDD	AB03	O VDNCMD
C25	IO D20#	Y24	O DQS0#	P25	P GND	AE24	IO MD11	J05	O ST2 / ENABL	AB01	O VDNSTB
C23	IO D21#	AD26	O DQS1#	R02	P GND	AB23	IO MD12	AD02	I SUSST#	AB05	A VLCOMP
D24	IO D22#	AF22	O DQS2#	T21	P GND	AC26	IO MD13	AB09	O SWEA# / strap	Y05	P VLVREF
B26	IO D23#	AD19	O DQS3#	U21	P GND	AE26	IO MD14	F12	I TESTINO	AD03	P VSUS25
E21	IO D24#	AF15	O DQS4#	U23	P GND	AF26	IO MD15	E10	I TESTIN1	A06	O VSYNC
A23	IO D25#	AE12	O DQS5#	U25	P GND	AD23	IO MD16	W04	IO VAD0	Y04	I VUPCMD
B23	IO D26#	AC08	O DQS6#	V02	P GND	AE23	IO MD17	W05	IO VAD1	AA01	I VUPSTB
A22	IO D27#	AD04	O DQS7#	V04	P GND	AD21	IO MD18	AA04	IO VAD2	AA02	I VUPSTB#
D23	IO D28#	T01	IO GBE0 / DP3D03	Y23	P GND	AF21	IO MD19	Y01	IO VAD3	E06	I XIN
A25	IO D29#	P04	IO GBE1 / SBDA	Y25	P GND	AC23	IO MD20	AC02	IO VAD4		

Center VTT Pins (12 pins): J13-18, K18, L18, M18, N18, P18, R18

Center VCCVL Pin (2 pins) T9, U9

Center VCCAGP pins (6 pins): K9, L9, M9, N9, P9, R9

Center GND Pins (37 pins): J9, L11-16, M11-16, N11-16, P11-16, R11-16, T11-16

Center VCCDP Pins (3 pins): J10-12

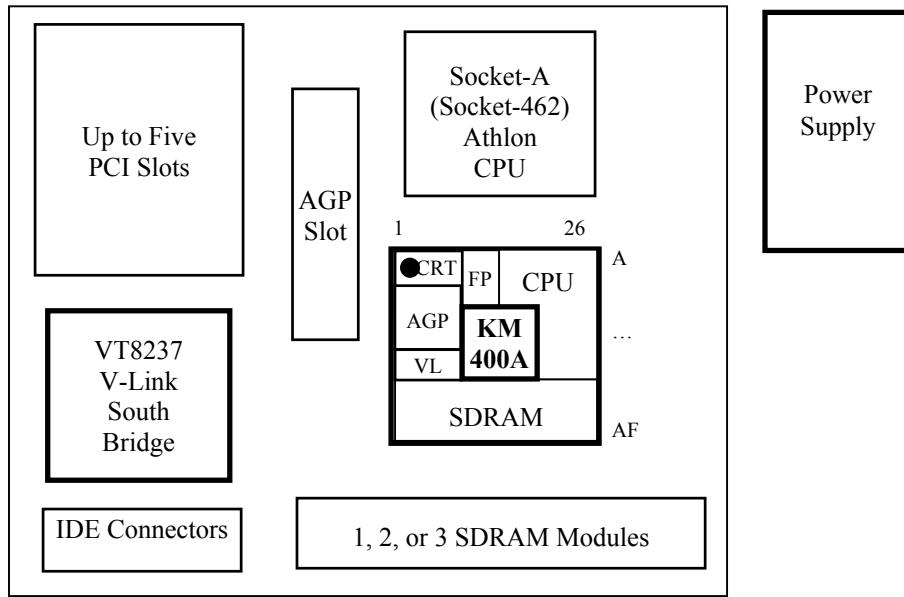
Center VCCM Pins (12 pins): T18, U18, V9-18

PIN DESCRIPTIONS

Table 4. Pin Descriptions

CPU Interface			
Signal Name	Pin #	I/O	Signal Description
CFWDRST	D14	O	CLK Forward Reset. Reset the clock forward circuitry for the Athlon™ interface.
CONNECT	C14	O	Connect. Used for power management and CLK-forward initialization at reset.
PROCRDY	E14	I	Processor Ready. Used for power management and clock-forward initialization at reset.
AIN[14-2]#	(see pin list)	O	Host CPU Address / Command Output. Unidirectional system address / command interface to the processor from the system controller. It is used to transfer probes or data movement commands into the processor during PCI-to-DRAM cycles to snoop the CPU internal Cache. AIN[14:2]# is skew-aligned with the forward clock, AINCLK#
AINCLK#	B15	O	Host CPU Address Output Clock. Single-ended forwarded clock for the AIN[14:2]# bus that is driven by the system controller. Both rising and falling edges are used to transfer addresses or commands to the processor.
AOUT[14-2]#	(see pin list)	I	Host CPU Address Input. Unidirectional system address / command interface from the processor to the system controller. It is used to transfer processor commands or probes responses to the system controller. AOUT[14:2]# is skew-aligned with the forward clock, AOUTCLK#
AOUTCLK#	R25	I	Host CPU Address Input Clock. Single-ended forwarded clock for the AOUT[14:2]# bus that is driven by the processor. Both rising and falling edges are used to transfer commands or probe responses.
D[63-0]#	(see pin list)	IO	Host CPU Data. Bi-directional interface between the processor and the system controller for data movement. D[63:0]# bus is skew-aligned with either the DICLK[3:0]# or DOCLK[3:0]# forward clocks.
DICLK[3-0]#	L24, G23, A24, A19	O	Host CPU Data Input Clock. Single-ended forwarded clocks for the D[63:0]# bus, driven by the system controller to the processor. Each 16-bit data word is skew-aligned with one of these clocks. Both rising and falling edges are used to transfer data to the processor.
DOCLK[3-0]#	L22, F23, B24, C19	I	Host CPU Data Output Clock. Single-ended forwarded clocks for the D[63:0]# bus, driven by the processor to the system controller. Each 16-bit data word is skew-aligned with one of these clocks. Both rising and falling edges are used to transfer data to the system controller.
DINVAL#	E13	O	Host CPU Data Read In Valid. Driven by the system controller to control the flow of data into the processor. DINVAL# can be used to introduce an arbitrary number of cycles between octawords into the processor.

The pinouts were defined assuming the ATX PCB layout model shown below (and general pin layout shown) as a guide for PCB component placement. Other PCB layouts (AT, LPX, and NLX) were also considered and can typically follow the same general component placement.



V-Link Interface

Signal Name	Pin #	I/O	Signal Description
VAD7,	AC1	IO	Address/Data Bus. Also used to transmit strap information from the south bridge (the straps are not on the VAD pins but are on the indicated pins of the south bridge chip).
VAD6,	AB4	IO	
VAD5,	Y2	IO	
VAD4,	AC2	IO	
VAD3,	Y1	IO	
VAD2,	AA4	IO	
VAD1,	W5	IO	
VAD0	W4	IO	
VBE#	Y3	IO	Byte Enable.
VUPCMD	Y4	I	Command from Client-to-Host.
VUPSTB	AA1	I	Strobe from Client-to-Host.
VUPSTB#	AA2	I	Complement Strobe from Client-to-Host.
VDNCMD	AB3	O	Command from Host-to-Client.
VDNSTB	AB1	O	Strobe from Host-to-Client.
VDNSTB#	AB2	O	Complement Strobe from Host-to-Client.

AGP 8x / 4x Bus Interface			
Signal Name	Pin #	I/O	Signal Description
GD[31:0]	(see pin list)	IO	Address / Data Bus. Address is driven with GDS assertion for AGP-style transfers and with GFRM# assertion for PCI-style transfers.
GBE[3:0] (GBE[3:0#] for 4x mode)	K3 N1 P4 T1	IO	Command / Byte Enable. (Interpreted as C/BE# for AGP 2x/4x and C#/BE for 8x). For AGP cycles these pins provide command information (different commands than for PCI) driven by the master (graphics controller) when requests are being enqueued using GPIPE# (2x/4x only as GPIPE# isn't used in 8x mode). These pins provide valid byte information during AGP write transactions and are driven by the master. The target (this chip) drives these lines to "0000" during the return of AGP read data. For PCI cycles, commands are driven with GFRM# assertion. Byte enables corresponding to supplied or requested data are driven on following clocks.
GPAR	U4	IO	AGP Parity. A single parity bit is provided over GD[31:0] and GBE[3:0].
GDBIH / GPIPE# GDBIL	K5 J4	IO	Dynamic Bus Inversion High / Low. AGP 8x transfer mode only. Driven by the source to indicate whether the corresponding data bit group (GDBIH for GD[31:16] and GDBIL for GD[15:0]) needs to be inverted on the receiving end (1 on GDBIx indicates that the corresponding data bit group should be inverted). Used to limit the number of simultaneously switching outputs to 8 for each 16-pin group. Pipelined Request. Not used by AGP 8x. Asserted by the master (external graphics controller) to indicate that a full-width request is to be enqueued by the target (north bridge). The master enqueues one request each rising edge of GCLK while GPIPE# is asserted. When GPIPE# is deasserted no new requests are enqueued across the AD bus. Note: See RxAE[1] for GPIPE# / GDBIH pin function selection.
GDS0F (GDS0 for 4x), GDS0S (GDS0# for 4x)	T3 T2	IO	Bus Strobe 0. Source synchronous strobes for GD[15:0] (the agent that is providing the data drives these signals). GDS0 provides timing for 2x data transfer mode; GDS0 and GDS0# provide timing for 4x mode. For 8x transfer mode, GDS0 is interpreted as GDS0F ("First" strobe) and GDS0# as GDS0S ("Second" strobe).
GDS1F (GDS1 for 4x), GDS1S (GDS1# for 4x)	K2 K1	IO	Bus Strobe 1. Source synchronous strobes for GD[31:16] (i.e., the agent that is providing the data drives these signals). GDS1 provides timing for 2x data transfer mode; GDS1 and GDS1# provide timing for 4x transfer mode. For 8x transfer mode, GDS1 is interpreted as GDS1F ("First" strobe) and GDS1# as GDS1S ("Second" strobe).
GFRM (GFRM# for 4x)	N5	IO	Frame. Assertion indicates the address phase of a PCI transfer. Negation indicates that one more data transfer is desired by the cycle initiator. Interpreted as active high for 8x.
GIRDY (GIRDY# for 4x)	P5	IO	Initiator Ready. (Interpreted as active low for PCI/AGP2x/4x and high for AGP 8x). For AGP write cycles, the assertion of this pin indicates that the master is ready to provide <i>all</i> write data for the current transaction. Once this pin is asserted, the master is not allowed to insert wait states. For AGP read cycles, the assertion of this pin indicates that the master is ready to transfer a subsequent block of read data. The master is <i>never</i> allowed to insert a wait state during the initial block of a read transaction. However, it may insert wait states after each block transfers. For PCI cycles, asserted when the initiator is ready for data transfer.
GTRDY (GTRDY# for 4x)	R5	IO	Target Ready. (Interpreted as active low for PCI/AGP2x/4x and high for AGP 8x). For AGP cycles, indicates that the target is ready to provide read data for the entire transaction (when the transaction can complete within four clocks) or is ready to transfer a (initial or subsequent) block of data when the transfer requires more than four clocks to complete. The target is allowed to insert wait states after each block transfer for both read and write transactions. For PCI cycles, asserted when the target is ready for data transfer.
GDSEL (GDSEL# for 4x mode)	N4	IO	Device Select (PCI transactions only). This signal is driven by the north bridge when a PCI initiator is attempting to access main memory. It is an input when the chip is acting as PCI initiator. Not used for AGP cycles. Interpreted as active high for AGP 8x.

Note: The AGP interface pins can be optionally configured as additional interfaces for connecting to external display devices. For simplification of the AGP pin description tables above and on the next page, that multiplexing is not shown here (see "Additional I2C Interfaces" and "Digital Display" pin description tables later in this document for more information).

AGP 8x / 4x Bus Interface (continued)			
Signal Name	Pin #	I/O	Signal Description
GSTOP (GSTOP# for 4x)	U5	IO	Stop (PCI transactions only). Asserted by the target to request the master to stop the current transaction. Interpreted as active high for AGP 8x.
AGP8XDT#	G6	I	AGP 8x Transfer Mode Detect. Low indicates that the external graphics card can support 8x transfer mode
GRBF (GRBF# for 4x)	K4	I	Read Buffer Full. Indicates if the master (graphics controller) is ready to accept previously requested low priority read data. When GRBF# is asserted, the north bridge will not return low priority read data to the graphics controller.
GWBF (GWBF# for 4x)	L5	I	Write Buffer Full.
SBA[7:0]# (SBA[7:0] for 4x)	(see pin list)	I	SideBand Address. Provides an additional bus to pass address and command information from the master (graphics controller) to the target (north bridge). These pins are ignored until enabled.
SBSF (SBS for 4x), SBSS (SBS# for 4x)	E1 E2	I	Sideband Strobe. Driven by the master to provide timing for SBA[7:0]. SBS is used for AGP 2x while SBS and SBS# are used together for AGP 4x. For 8x mode, the strobe mechanism works differently with SBS interpreted as SBSF ("First" strobe) and SBS# as SBSS ("Second" strobe).
ST[2:0]	J5, F3, G5	O	Status (AGP only). Provides information from the arbiter to a master to indicate what it may do. Only valid while GGNT# is asserted. 000 Indicates that previously requested low priority read or flush data is being returned to the master (graphics controller). 001 Indicates that previously requested high priority read data is being returned to the master. 010 Indicates that the master is to provide low priority write data for a previously enqueued write command. 011 Indicates that the master is to provide high priority write data for a previously enqueued write command. 100 Reserved. (arbiter must not issue, may be defined in the future). 101 Reserved. (arbiter must not issue, may be defined in the future). 110 Reserved. (arbiter must not issue, may be defined in the future). 111 Indicates that the master (graphics controller) has been given permission to start a bus transaction. The master may enqueue AGP requests by asserting PIPE# or start a PCI transaction by asserting GFRM#. ST[2:0] are always outputs from the target (north bridge logic) and inputs to the master (graphics controller).
GREQ (GREQ# for 4x)	F5	I	Request. Master (graphics controller) request for use of the AGP bus.
GGNT (GGNT# for 4x)	E4	O	Grant. Permission is given to the master (graphics controller) to use the AGP bus.
GSERR (GSERR# for 4x)	R4	IO	AGP System Error.

Note: The AGP interface pins can be optionally configured as additional interfaces for connecting to external display devices. For simplification of the AGP pin description tables above and on the next page, that multiplexing is not shown here (see "Additional I2C Interfaces" and "Digital Display" pin description tables later in this document for more information).

Note: Separate system interrupts are not provided for AGP. The AGP connector provides interrupts via PCI bus INTA-B#.

Note: A separate reset is not required for the AGP bus (RESET# resets both PCI and AGP buses)

Note: Two mechanisms are provided by the AGP bus to enqueue master requests: GPIPE# (to send addresses multiplexed on the AD lines) and the SBA port (to send addresses unmultiplexed). AGP masters implement one or the other or select one at initialization time (they are not allowed to change during runtime). Only one of the two will be used; the signals associated with the other will not be used. GRBF# has an internal pullup to maintain it in the deasserted state in case it is not implemented on the master device. AGP 8x mode allows only SBA (GPIPE# isn't used in 8x mode).

Note: AGP 8x signal levels are 0V and 0.8V. AGP 8x mode maintains most signals at a low level when inactive resulting in no current flow.

DDR Synchronous DRAM Interface			
Signal Name	Pin #	I/O	Signal Description
MD[63:0]	(see pinout tables)	IO	Memory Data. These signals are connected to the DRAM data bus. Output drive strength may be set by Device 0 Rx6D[1-0].
MA[14:0]	AB19, AB18, AF17, AC9, AB10, AC17, AE17, AC18, AB15, AB17, AB16, AB14, AC12, AB12, AC11	O	Memory Address. DRAM address lines. Output drive strength may be set by Device 0 Rx6C[7-6].
CS[5:0]#	AD5, AB7, AB6, AC6, AC5, AD6	O	Chip Select. Chip select of each bank. Output drive strength may be set by Device 0 Rx6D[3-2].
DQM[7:0]	AF4, AB8, AF12, AE15, AF19, AD22, AD25, Y26	O	Data Mask. Data mask of each byte lane. Output drive strength may be set by Device 0 Rx6D[5-4].
DQS[7:0]#	AD4, AC8, AE12, AF15, AD19, AF22, AD26, Y24	IO	DDR Data Strobe. Data strobe of each byte lane. Output drive strength may be set by Device 0 Rx6C[3-2].
SRASA#, SRASB# / CKE5, SRASC# / CKE4	AB11 AF24 AB20	O	Row Address Command Indicator. Output drive strength may be set by Device 0 Rx6C[7-4].
SCASA#, SCASB# / CKE3, SCASC# / CKE1	AD7 AC24 AD24	O	Column Address Command Indicator. Output drive strength may be set by Device 0 Rx6C[7-4].
SWEA# SWEB# / CKE2, SWEC# / CKE0	AB9 AB22 AC21	O	Write Enable Command Indicator. Output drive strength may be set by Device 0 Rx6C[7-4].
CKE5 / SRASB#, CKE4 / SRASC#, CKE3 / SCASB#, CKE2 / SWEB#, CKE1 / SCASC#, CKE0 / SWEC#	AF24 AB20 AC24 AB22 AD24 AC21	O	Clock Enables. Clock enables for each DRAM bank for powering down the SDRAM or clock control for reducing power usage and for reducing heat / temperature in high-speed memory systems. See Device 0 Rx78[0] and RxE0[4].

Serial Bus / I2C Interfaces				
Signal Name	AGP Name	Pin #	I/O	Signal Description
SBCK	GIRDY	P5	IO	I2C Serial Bus Clock for Panel (Muxed on AGP Bus Pins).
SBDA	GBE1	P4	IO	I2C Serial Bus Data for Panel (Muxed on AGP Bus Pins).
DDCCK	GREQ	F5	IO	I2C Serial Bus Clock for CRT DDC (Muxed on AGP Bus Pins).
DDCDA	GGNT	E4	IO	I2C Serial Bus Data for CRT DDC (Muxed on AGP Bus Pins).
SPCLK1	n/a	F7	IO	I2C Serial Bus Clock for Display Port 1. As an output, it is programmed via Rx3C5.31[5]. As an input, its status is read via Rx3C5.31[3]. In either case the serial port must be enabled by Rx3C5.31[0] = 1.
SPDAT1	n/a	D7	IO	I2C Serial Bus Data for Display Port 1. As an output, it is programmed via Rx3C5.31[4]. As an input, its status is read via Rx3C5.31[2]. In either case the serial port must be enabled by Rx3C5.31[0] = 1.
SPCLK2	n/a	C6	IO	I2C Serial Bus Clock for Display Port 2 (or DDC if AGP Enabled). As an output, it is programmed via Rx3C5.26[5]. As an input, its status is read via Rx3C5.26[3]. In either case the serial port must be enabled by Rx3C5.26[0] = 1.
SPDAT2	n/a	D6	IO	I2C Serial Bus Data for Display Port 2 (or DDC if AGP Enabled). As an output, it is programmed via Rx3C5.26[4]. As an input, its status is read via Rx3C5.26[2]. In either case the serial port must be enabled by Rx3C5.26[0] = 1.

"Display Ports 1-2" above refer to the 12-bit "DVI" interfaces typically connected to external TMDS transmitters for driving flat panel monitors. One option possible as a result of multiplexing display functions on the AGP port pins is that if AGP is not enabled, an add-in card can be designed to fit in the AGP slot to bring out panel display pins. In this case, the first two sets of serial ports defined above (SBxx and DDCxx) can be used.

Panel Power Control (Muxed with AGP)				
Signal Name	AGP Name	Pin #	I/O	Signal Description
ENAVDD	ST1	F3	IO	Enable Panel VDD Power.
ENAVEE	ST0	G5	IO	Enable Panel VEE Power.
ENABLT	ST2	J5	IO	Enable Panel Back Light.

CRT Display Interface				
Signal Name	Pin #	I/O	Signal Description	
AR	A3	A	Analog Red. Analog red output to the CRT monitor.	
AB	B3	A	Analog Blue. Analog blue output to the CRT monitor.	
AG	A2	A	Analog Green. Analog green output to the CRT monitor.	
HSYNC	B6	O	Horizontal Sync. Output to CRT.	
VSYNC	A6	O	Vertical Sync. Output to CRT.	
RSET	B5	A	Reference Resistor. Tie to GNDRGB through an external $90.9\ \Omega \pm 1\% \Omega$ resistor to control the RAMDAC full-scale current value.	

Dedicated Digital Display Interface Port 0 (Muxed with TV Out)			
Signal Name	Pin #	I/O	Signal Description
DP0D11 / TVD11,	A7	O	Digital Display Port 0 Data. Default output drive is 8 mA. 16 mA may be selected via SR3D[6]=1. TV Encoder outputs are muxed on the DP0D[11:0] pins (see the TV Encoder Interface pin list for details).
DP0D10 / TVD10 / strap,	B7		
DP0D9 / TVD9,	C7		
DP0D8 / TVD8,	C8		
DP0D7 / TVD7 / strap,	A8		
DP0D6 / TVD6 / strap,	B8		
DP0D5 / TVD5 / strap,	E8		
DP0D4 / TVD4 / strap,	E9		
DP0D3 / TVD3 / strap,	A9		
DP0D2 / TVD2 / strap,	B9		
DP0D1 / TVD1 / strap,	C9		
DP0D0 / TVD0 / strap	D9		
DP0HS / TVHS	B10	O	Digital Display Port 0 Horizontal Sync. Internally pulled down.
DP0VS / TVVS	B11	O	Digital Display Port 0 Vertical Sync. Internally pulled down.
DP0DE / TVDE	A11	O	Digital Display Port 0 Data Enable. Internally pulled down.
DP0DET / TVCLKI	A10	I	Digital Display Port 0 Display Detect. If VGA register 3C5.12[5]=0, 3C5.1A[5] will read 1 if a Flat Panel is connected.
DP0CLK / TVCLK	D8	O	Digital Display Port 0 Clock. Internally pulled down during reset. 8mA is the default. 16mA may also be selected.

The above pins are designed to connect to an external TMDS transmitter for driving a DVI connector to a flat panel monitor. The terminology “3C5.nn” above refers to the VGA “Sequencer” registers at I/O port 3C5 index “nn”

Dedicated TV Encoder Interface (Muxed with Digital Display Port 0)			
Signal Name	Pin #	I/O	Signal Description
TVD11 / DP0D11,	A7	O	TV Encoder Data.
TVD10 / DP0D10 / strap,	B7		
TVD9 / DP0D9,	C7		
TVD8 / DP0D8,	C8		
TVD7 / DP0D7 / strap,	A8		
TVD6 / DP0D6 / strap,	B8		
TVD5 / DP0D5 / strap,	E8		
TVD4 / DP0D4 / strap,	E9		
TVD3 / DP0D3 / strap,	A9		
TVD2 / DP0D2 / strap,	B9		
TVD1 / DP0D1 / strap,	C9		
TVD0 / DP0D0 / strap	D9		
TVHS / DP0HS	B10	O	TV Encoder Horizontal Sync. Internally pulled down during reset
TVVS / DP0VS	B11	O	TV Encoder Vertical Sync. Internally pulled down during reset
TVDE / DP0DE	A11	O	TV Encoder Display Enable. Internally pulled down during reset
TVCLKI / DP0DET	A10	I	TV Encoder Clock In. Input clock from TV encoder. Internally pulled down.
TVCLK / DP0CLK	D8	O	TV Encoder Clock Out. Output clock to TV encoder. Internally pulled down.

The above pins are designed to connect to an external TV Encoder chip such as the VIA VT1621 or VT1622 for driving a TV set.

Digital Display Interface Port 1 (Muxed with AGP)				
Signal Name	AGP Name	Pin #	I/O	Signal Description
DP1D11,	GBE3	K3	O	Digital Display Port 1 Data.
DP1D10,	GD26	J3		
DP1D9,	GD24	J1		
DP1D8,	GD30	H2		
DP1D7,	GD28	H1		
DP1D6,	GD29	H3		
DP1D5,	SBA4#	G3		
DP1D4,	GD27	H4		
DP1D3,	SBA5#	F1		
DP1D2,	SBSS	E2		
DP1D1,	SBSF	E1		
DP1D0	SBA2#	E3		
DP1HS	SBA3#	D1	O	Digital Display Port 1 Horizontal Sync.
DP1VS	SBA0#	D2	O	Digital Display Port 1 Vertical Sync.
DP1DE	SBA1#	D3	O	Digital Display Port 1 Data Enable.
DP1DET	GD31	G4	I	Digital Display Port 1 Display Detect. If VGA register 3C5.3E[0] = 1, 3C5.1A[4] will read 1 if a panel is connected. Must be tied to GND if not used.
DP1CLK	SBA6#	G1	O	Digital Display Port 1 Clock.
DP1CLK#	SBA7#	G2	O	Digital Display Port 1 Clock Complement.

The above pins are designed to connect to an external TMDS transmitter for driving a DVI connector to a flat panel monitor.

Digital Display Port 2 Interface (Muxed with AGP)				
Signal Name	AGP Name	Pin #	I/O	Signal Description
DP2D11,	GD11	P2	O	Display Port 2 Data. 3C5.12[4] must be set to 0. Used for driving an external flat panel monitor via external TMDS transmitters.
DP2D10,	GD13	P1		
DP2D09,	GD14	P3		
DP2D08,	GD15	N3		
DP2D07,	GBE2	N1		
DP2D06,	GD16	N2		
DP2D05,	GD17	M1		
DP2D04,	GD18	M3		
DP2D03,	GD23	L3		
DP2D02,	GD20	L1		
DP2D01,	GD22	L2		
DP2D00	GDS1F	K2		
DP2HS	GFRAME	N5	O	Display Port 2 Horizontal Sync.
DP2VS	GDEVSEL	N4	O	Display Port 2 Vertical Sync.
DP2DE	GD19	M5	O	Display Port 2 Data Enable.
DP2DET	GDS1S	K1	I	Display Port 2 Detect. If Rx??[?]=0, Rx??[?] will read 1 if a Flat Panel Monitor is properly connected. Must be tied to GND if not used.
DP2CLK	GD21	L4	O	Display Port 2 Clock.
DP2CLK#	GWBF	L5	O	Display Port 2 Clock Complement.

The above pins are designed to connect to an external TMDS transmitter for driving a DVI connector to a flat panel monitor.

Digital Display Port 3 Interface (Muxed with AGP)				
Signal Name	AGP Name	Pin #	I/O	Signal Description
DP3D11,	GD1	W1	O	Display Port 3 Data. 3C5.12[4] must be set to 0. Used for driving an external flat panel monitor via external TMDS transmitters.
DP3D10,	GD0	W2		
DP3D09,	GD3	W3		
DP3D08,	GD4	V1		
DP3D07,	GD5	U2		
DP3D06,	GD6	U1		
DP3D05,	GD7	U3		
DP3D04,	GDS0F	T3		
DP3D03,	GBE0	T1		
DP3D02,	GDS0S	T2		
DP3D01,	GD10	R3		
DP3D00	GD12	R1		
DP3HS	GD9	T5	O	Display Port 3 Horizontal Sync.
DP3VS	GPAR	U4	O	Display Port 3 Vertical Sync.
DP3DE	GSERR	R4	O	Display Port 3 Data Enable.
DP3DET	GD8	T4	I	Display Port 3 Detect. If Rx??[?]=0, Rx??[?] will read 1 if a Flat Panel Monitor is properly connected. Must be tied to GND if not used.
DP3CLK	GD2	V3	O	Display Port 3 Clock.
DP3CLK#	GSTOP	U5	O	Display Port 3 Clock Complement.

The above pins are designed to connect to an external TMDS transmitter for driving a DVI connector to a flat panel monitor.

Clocks, Resets, Power Control, General Purpose I/O, Interrupts and Test			
Signal Name	Pin #	I/O	Signal Description
HCLK	G21	I	Host Clock. This pin receives the host CPU clock (100 / 133 MHz). This clock is used by all KM400A logic that is in the host CPU domain.
HCLK#	F22	I	Host Clock Complement. HCLK inverted. Used for Quad Data Transfer on host CPU bus.
MCLK	Y22	O	Memory (SDRAM) Clock. Output from internal clock generator to the external clock buffer.
MCLKFB	AA23	I	Memory (SDRAM) Clock Feedback. Input from the external clock buffer.
DCLKI	D5	I	Dot Clock (Pixel Clock) In. Used for external EMI reduction circuit if used. Loop back from DCLKO if external EMI reduction circuit not implemented.
DCLKO	C5	O	Dot Clock (Pixel Clock) Out. Used for external EMI reduction circuit if used. Loop back to DCLKI if external EMI reduction circuit not implemented.
GCLK	V5	I	Graphics Clock.
XIN	E6	I	Reference Frequency Input. An external 14.31818 MHz clock source is normally connected to this pin. All internal graphics controller clocks are synthesized on chip using this frequency as a reference.
RESET#	AE1	I	Reset. Input from the South Bridge chip. When asserted, this signal resets the KM400A and sets all register bits to the default value. The rising edge of this signal is used to sample all power-up strap options
PWROK	AD1	I	Power OK. Connect to South Bridge and Power Good circuitry.
SUSST#	AD2	I	Suspend Status. For implementation of the Suspend-to-DRAM feature. Connect to an external pullup to disable.
GPIO0	D10	O	General Purpose I/O 0. For programming, see VGA register 3C5.25
GPOUT	E7	O	General Purpose Output. For programming, see VGA register 3C5.25
INTA#	F6	O	Interrupt. PCI interrupt output (handled by the interrupt controller in the South Bridge)
BISTIN	A5	I	BIST In. This pin is used for testing and must be left unconnected or tied to GND on all board designs.
TESTIN0	F12	I	Test In 0. This pin is used for testing and must be left unconnected or tied high on all board designs.
TESTIN1	E10	I	Test In 1. This pin is used for testing and must be left unconnected or tied high on all board designs.

Reference Voltages			
Signal Name	Pin #	I/O	Signal Description
S2KVREF	F17, N21	P	S2K Bus Voltage Reference. 0.5 VTT derived using resistive voltage divider. See KM400A Design Guide.
AGPVREF	H6, M6	P	AGP Voltage Reference. 0.4 VCCQQ (1.32V) when VCCQQ is 3.3V and 0.5 VCCQQ (0.75V) when VCCQQ is 1.5V. See KM400A Design Guide.
MEMVREF	AA10, AA18	P	Memory Voltage Reference. 0.5 VCCM derived using resistive voltage divider. See KM400A Design Guide.
VLVREF	Y5	P	V-Link Voltage Reference. 0.625V derived using a resistive voltage divider. See KM400A Design Guide.

Compensation

Signal Name	Pin #	I/O	Signal Description
S2KCOMP	L21	I	S2K Bus Compensation. Connect to 49.9 Ω 1% resistor to ground.
AGPCOMP	C1	AI	AGP Compensation.
VLCOMP	AB5	I	Vlink P-Channel Compensation. Connect 360 Ω 1% resistor to ground.

Analog & Quiet Power and Ground

Signal Name	Pin #	I/O	Signal Description
VCCS2K	M21	P	Power for S2K Bus Circuitry. (2.5V ±5%)
VCCQQ	B1	P	AGP Quiet Power. Connect to main AGP power (VCCAGP = 1.5 / 3.3V ±5%) through a ferrite bead.
VCCHCK	G22	P	Power for Host CPU Clock DLL (2.5V ±5%)
VCCMCK	AA22	P	Power for Memory Clock DLL (2.5V ±5%)
VCCRGB	C3	P	Power for CRT RGB Outputs (2.5V ±5%).
VCCDAC	C4	P	Power for DAC Digital Logic (2.5V ±5%)
VCCPLL1	B4	P	Power for Graphics Controller PLL1 (2.5V ±5%).
VCCPLL2	A4	P	Power for Graphics Controller PLL2 (2.5V ±5%).
GNDS2K	K21	P	Ground for S2K Bus Circuitry. Connect to main ground plane.
GNDQQ	C2	P	Ground for AGP Quiet Power. Connect to main ground plane.
GNDHCK	F21	P	Ground for Host CPU Clock Circuitry. Connect to main ground plane through a ferrite bead.
GNDMCK	Y21	P	Ground for Memory Clock Circuitry. Connect to main ground plane through a ferrite bead.
GNDRGB	A1	P	Connection Point for RGB Load Resistors.
GNDDAC	B2	P	Ground for DAC Analog Circuitry.
GNDPLL1	E5	P	Ground for Graphics Controller PLL1.
GNDPLL2	D4	P	Ground for Graphics Controller PLL2.

Digital Power and Ground

Signal Name	Pin #	I/O	Signal Description
VCC25	(see pin list)	P	Power for Internal Logic (2.5V ±5%).
VSUS25	AD3	P	Suspend Power (2.5V ±5%).
VTT	J13-J18, K18, L18, M18, N18, P18, R18	P	Power for CPU I/O Interface Logic. Voltage is CPU dependent. See also VID (Voltage ID) pin.
VCCAGP	J6, K9, L9, M9, N6, N9, P6, P9, R6, R9, T6, U6	P	Power for AGP Bus I/O Interface Logic. 1.5V±5%
VCCM	T18, U18, V9-V18, AA7, AA15, AA21	P	Power for Memory I/O Interface Logic (2.5 / 3.3V ±5%).
VCCVL	T9, U9, Y6, AA6	P	Power for V-Link I/O Interface Logic (2.5V ±5%).
VCCDP	J10-J12	P	Power for Digital Display Interface (3.3V ±5%).
GND	(see pin table)	P	Ground. Connect to main ground plane.

Strap Pins (External pullup / pulldown straps are required to select "H" / "L")				
Signal	Actual Strap Pin	Function	Description	Status Bit
DP0D[10,7]	DP0D[10,7]	-reserved-	Must be pulled low	-
DP0D[6]	DP0D[6]	DP0 Port Enable	L: Disable H: Enable	3C5.12[6]
DP0D[5]	DP0D[5]	DP0 Port Configuration	L: Display H: TV out	3C5.12[5]
DP0D[4]	DP0D[4]	FP Port Configuration	L: 2 x 12-bit FP interface H: 24-bit FP interface	3C5.12[4]
DP0D[3:0]	DP0D[3:0]	OEM Panel Type	Reserved for customer configuration	3C5.12[3:0]
VAD7	VT8235-CD: SDCS3# VT8235-CE: SDCS3# VT8237: PDCS3#	-reserved-	-	-
VAD5	VT8235-CD: SDA1 VT8235-CE: SDA1 VT8237: PDA1	Auto-Configure	L: Disable (used on-chip defaults) H: Enable (get from ROM) VAD5 is sampled during system initialization; The actual strapping pin is located on the South Bridge chip.	Rx54[5]
VAD[6,4]	VT8235-CD: SDA[2, 0] VT8235-CE: SDA[2, 0] VT8237: PDA[2, 0]	FSB Frequency Select	LL: 100Mhz LH: 133MHz Hx: 166MHz VAD6 and VAD4 are sampled during system initialization; The actual strapping pins are located on the South Bridge chip.	Rx54[7:6]
VAD[3:0]	VT8235-CD: SA[19:16] VT8235-CE: Strap_VAD[3:0] VT8237: GPIO[D, B, A, C]	CPU Clock Divider	LLLL: 11 LLLH: 11.5 LLHL: 12 LLHH: 12 LHLL: 5 LHLH: 5.5 LHHL: 6 LHHH: 6.5 HLLL: 7 HLLH: 7.5 HLHL: 8 HLHH: 8.5 HHLL: 9 HHLH: 9.5 HHHL: 10 HHHH: 10.5 VAD[3:0] are sampled during system initialization; The actual strapping pins are located on the South Bridge chip.	RxD7[6:3]

REGISTERS

Register Overview

The following tables summarize the configuration and I/O registers of the KM400A north bridge. These tables also document the power-on default value (“Default”) and access type (“Acc”) for each register. Access type definitions used are RW (Read/Write), RO (Read/Only), “—” for reserved / used (essentially the same as RO), and RWC (or just WC) (Read / Write 1’s to Clear individual bits). Registers indicated as RW may have some read/only bits that always read back a fixed value (usually 0 if unused); registers designated as RWC or WC may have some read-only or read write bits (see individual register descriptions following these tables for details). All offset and default values are shown in hexadecimal unless otherwise indicated.

The graphics registers are described in a separate document.

Table 5. Registers

I/O Ports

Port #	I/O Port	Default	Acc
22	PCI / AGP Arbiter Disable	00	RW
CFB-8	Configuration Address	0000 0000	RW
CFF-C	Configuration Data	0000 0000	RW

Device 0 Registers - Host Bridge
Header Registers

Offset	Configuration Space Header	Default	Acc
1-0	Vendor ID	1106	RO
3-2	Device ID	3205	RO
5-4	Command	0006	RW
7-6	Status	0210	WC
8	Revision ID	0n	RO
9	Program Interface	00	RO
A	Sub Class Code	00	RO
B	Base Class Code	06	RO
C	-reserved-	00	—
D	Latency Timer	00	RW
E	Header Type	00	RO
F	Built In Self Test (BIST)	00	RO
13-10	Graphics Aperture Base	0000 0008	RW
14-2B	-reserved-	00	—
2D-2C	Subsystem Vendor ID	0000	W1
2F-2E	Subsystem ID	0000	W1
30-33	-reserved-	00	—
37-34	Capability Pointer	0000 00A0	RO
38-3F	-reserved-	00	—

Device-Specific Registers

Offset	V-Link Control	Default	Acc
40	V-Link Revision ID	00	RW
41	V-Link NB Capability	19	RW
42	V-Link NB Downlink Command	88	RW
44-43	V-Link NB Uplink Status	8280	RO
45	V-Link NB Bus Timer	44	RW
46	V-Link Misc NB Control	00	RW
47	V-Link Control	00	RW
48	V-Link NB/SB Configuration	00	RW
49	V-Link SB Capability	19	RW
4A	V-Link SB Downlink Status	88	RO
4C-4B	V-Link SB Uplink Command	8280	RW
4D	V-Link SB Bus Timer	44	RW
4E	CCA Master High Priority	00	RW
4F	V-Link SB Miscellaneous Control	00	RW

Offset	CPU Interface Control	Default	Acc
50-53	-reserved-	00	—
54	CPU FSB Frequency	00	RW

Offset	DRAM Control	Default	Acc
55	DRAM Control	00	RW
56-57	-reserved-	00	—
59-58	MA Map Type	2222	RW
5F-5A	DRAM Row Ending Address:		
5A	Bank 0 Ending (HA[31:24])	01	RW
5B	Bank 1 Ending (HA[31:24])	01	RW
5C	Bank 2 Ending (HA[31:24])	01	RW
5D	Bank 3 Ending (HA[31:24])	01	RW
5E	Bank 4 Ending (HA[31:24])	01	RW
5F	Bank 5 Ending (HA[31:24])	01	RW
60	-reserved-	00	—
61	ROM Shadow Control C0000-CFFFF	00	RW
62	ROM Shadow Control D0000-DFFFF	00	RW
63	ROM Shadow Control E0000-FFFFF	00	RW
64	DRAM Timing for All Banks	E4	RW
65	DRAM Arbitration Timer	00	RW
66	DRAM Arbitration Control	00	RW
67	DDR Strobe Input Delay	00	RW
68	DDR Strobe Output Delay	00	RW
69	DRAM Clock Select	00	RW
6A	DRAM Refresh Counter	00	RW
6B	DRAM Arbitration Control	00	RW
6C	DRAM Early Clock Select	00	RW
6D	DRAM MD Output Delay	00	RW
6E-6F	-reserved-	00	—

Offset	PCI Bus Control	Default	Acc
70	PCI Buffer Control	00	RW
71	CPU to PCI Flow Control	48	RW
72	-reserved-	00	—
73	PCI Master Control	00	RW
74	-reserved-	00	—
75	PCI Arbitration 1	00	RW
76	PCI Arbitration 2	00	RW
77	Chip Test (do not program)	00	RW
78-7F	-reserved-	00	—

Device-Specific Registers (continued)

Offset	AGP 2.0 Control (RxFD[1]=1)	Default	Acc
83-80	AGP 2.0 GART/TLB Control	0000 0000	RW
84	AGP 2.0 Graphics Aperture Size	00	RW
85-87	Reserved (Do Not Program)	00	RW
8B-88	AGP 2.0 GART Table Base	0000 0000	RW
8C-9F	-reserved-	00	—
A3-A0	AGP 2.0 Capabilities	0020 C002	RO
A7-A4	AGP 2.0 Status	1F00 0201	RO
AB-A8	AGP 2.0 Command	0000 0000	RW

Registers A0-AB in the AGP 2.0 register group in the table above are actually offsets from CAPPTR (Rx34) which (with Rx34 = A0h for AGP 2.0) result in the offsets listed above.

Offset	AGP 3.0 Control (RxFD[1]=0)	Default	Acc
83-80	AGP 3.0 Capabilities	0030 C002	RO
87-84	AGP 3.0 Status	1F00 0A03	RO
8B-88	AGP 3.0 Command	1F00 0000	RW
8F-8C	-reserved-	0000 0000	—
93-90	AGP 3.0 GART / TLB Control	0000 0000	RW
97-94	AGP 3.0 Graphics Aperture Size	0001 0F00	RW
9B-98	AGP 3.0 GART Table Base	0000 0000	RW
9C-AB	-reserved-	00	—

Registers 80-AB in the AGP 3.0 register group in the table above are actually offsets from CAPPTR (Rx34) which (with Rx34 = 80h for AGP 3.0) result in the offsets listed above.

Offset	AGP 2.0 / 3.0 Control	Default	Acc
AC	AGP Control	00	RW
AD	AGP Latency Timer	02	RW
AE	AGP Miscellaneous Control	00	RW
AF	AGP 3.0 Control	00	RW
B0	AGP Pad Control / Status	8x	RW
B1	AGP Drive Strength	63	RW
B2	AGP Pad Drive / Delay Control	08	RW
B3	AGP Strobe Output Drive Control	00	RW

Offset	V-Link Control	Default	Acc
B4	V-Link NB Compensation Control	00	RW
B5	V-Link NB Strobe Drive Control	00	RW
B6	V-Link NB Data Drive Control	00	RW
B7	-reserved-	00	—
B8	V-Link SB Compensation Control	00	RW
B9	V-Link SB Strobe Drive Control	00	RW
BA	V-Link SB Data Drive Control	00	RW
BB	-reserved-	00	—

Offset	Power Control	Default	Acc
BC	Power Management Mode	00	RW
BD	DRAM Power Management Control	00	RW
BE	Dynamic Clock Stop Control	00	RW
BF	MA / SCMD Pad Toggle Reduction	00	RW

Offset	Extended Power Management	Default	Acc
C0	Power Management Capability ID	01	RO
C1	Power Management New Pointer	00	RO
C2	Power Management Capabilities I	02	RO
C3	Power Management Capabilities II	00	RO
C4	Power Management Control / Status	00	RW
C5	Power Management Status	00	RW
C6	PCI-to-PCI Bridge Support Extension	00	RW
C7	Power Management Data	00	RW
C8-CF	-reserved-	00	—

Offset	Host CPU Control	Default	Acc
D0-D1	-reserved-	00	—
D2	S2K Timing Control	78	RW
D3	BIU Arbitration Control	00	RW
D4	BIU Control 1	00	RW
D5	BIU Control 2	00	RW
D6	BIU Control 3	00	RW
D7	CPU Strapping		strapping RO
D8	S2K Compensation Strapping	00	RW
D9	S2K Compensation Result 1	00	RO
DA	S2K Compensation Result 2	00	RW
DB	S2K Compensation Result 3	00	RO
DC	S2K Compensation Result 4	07	RW
DD	S2K Compensation Result 5	00	RW
DE	BIU Control 4	00	RW
DF	BIU Control 5	00	RW

Offset	UMA Control	Default	Acc
E0	CPU Direct Access FB Base	00	RW
E1	CPU Direct Access FB Size	00	RW
E2	VGA Arbitration Timer	00	RW
E3	Graphics Arbitration Timer	00	RW

Offset	DRAM Above 4G Control	Default	Acc
E4	Low Top Address Low	00	RW
E5	Low Top Address High	FF	RW
E6	SMM / APIC Decoding	01	RW
E7	-reserved-	00	—

Offset	DRAM Drive	Default	Acc
E8	DRAM DQ Drive	00	RW
E9	DRAM CS# Drive	00	RW
EA	DRAM MAA Drive	00	RW
EB	-reserved-	00	—
EC	DRAM S-Port Control	00	RW
ED	DRAM DQS Drive Control	00	RW
EE	DRAM DQS/MD Duty Cycle Control	00	RW
EF	-reserved-	00	—

Offset	Test, BIOS Scratch, Miscellaneous	Default	Acc
F0-F2	Reserved (Do Not Program)	00	RW
F3-F4	BIOS Scratch Registers	00	RW
F5-FC	Reserved (Do Not Program)	00	RW
FD	AGP 2.0 / 3.0 Select	00	RW
FE-FF	Reserved (Do Not Program)	00	RW

Device 1 – PCI-to-PCI Bridge
Header Registers

Offset	Configuration Space Header	Default	Acc
1-0	Vendor ID	1106	RO
3-2	Device ID	B168	RO
5-4	Command	0007	RW
7-6	Status	0230	WC
8	Revision ID	0n	RO
9	Program Interface	00	RO
A	Sub Class Code	04	RO
B	Base Class Code	06	RO
C	-reserved-	00	—
D	Latency Timer	00	RW
E	Header Type	01	RO
F	Built In Self Test (BIST)	00	RO
10-17	-reserved-	00	—
18	Primary Bus Number	00	RW
19	Secondary Bus Number	00	RW
1A	Subordinate Bus Number	00	RW
1B	Secondary Latency Timer	00	RO
1C	I/O Base	F0	RW
1D	I/O Limit	00	RW
1F-1E	Secondary Status	0000	RO
21-20	Memory Base	FFF0	RW
23-22	Memory Limit (Inclusive)	0000	RW
25-24	Prefetchable Memory Base	FFF0	RW
27-26	Prefetchable Memory Limit	0000	RW
28-2B	-reserved-	00	—
2D-2C	Subsystem Vendor ID	0000	W1
2F-2E	Subsystem ID	0000	W1
30-33	-reserved-	00	—
34	Capability Pointer	80	RO
35-3D	-reserved-	00	—
3F-3E	PCI-to-PCI Bridge Control	00	RW

Device-Specific Registers

Offset	AGP Bus Control	Default	Acc
40	CPU-to-AGP Flow Control 1	00	RW
41	CPU-to-AGP Flow Control 2	00	RW
42	AGP Master Control	00	RW
43	AGP Master Latency Timer	22	RW
44	Back-Door Register Control	00	RW
45	Fast Write Control	72	RW
47-46	PCI-to-PCI Bridge Device ID	0000	RW
48	AGP Parity Error Control	00	RW
49-7F	-reserved-	00	—
80	Capability ID	01	RO
81	Next Pointer	00	RO
82	Power Management Capabilities 1	02	RO
83	Power Management Capabilities 2	00	RO
84	Power Management Control / Status	00	RW
85	Power Management Status	00	RO
86	PCI-PCI Bridge Support Extensions	00	RO
87	Power Management Data	00	RO
88-FF	-reserved-	00	—

Miscellaneous I/O

One I/O port is defined in the KM400A: Port 22.

Port 22 – PCI / AGP Arbiter DisableRW

- 7-1 Reserved** always reads 0
0 PCI / AGP Arbiter Disable
 0 Respond to all REQ# signals.....default
 1 Do not respond to any REQ# signals

This port can be enabled for read/write access by setting bit-7 of Device 0 Configuration Register 78.

Configuration Space I/O

All registers in the KM400A (listed above) are addressed via the following configuration mechanism:

Mechanism #1

These ports respond only to double-word accesses. Byte or word accesses will be passed on unchanged.

Port CFB-CF8 - Configuration Address.....RW

- 31 Configuration Space Enable**
 0 Disabled..... default
 1 Convert configuration data port writes to configuration cycles on the PCI bus
30-24 Reserved always reads 0
23-16 PCI Bus Number
 Used to choose a specific PCI bus in the system
15-11 Device Number
 Used to choose a specific device in the system (devices 0 and 1 are defined for the KM400A)
10-8 Function Number
 Used to choose a specific function if the selected device supports multiple functions (only function 0 is defined for the KM400A).
7-2 Register Number (also called the "Offset")
 Used to select a specific DWORD in the KM400A configuration space
1-0 Fixed always reads 0

Port CFF-CFC - Configuration Data.....RW

Refer to PCI Bus Specification Version 2.1 for further details on operation of the above configuration registers.

Register Descriptions

Device 0 Header Registers - Host Bridge

All registers are located in PCI configuration space. They should be programmed using PCI configuration mechanism 1 through CF8 / CFC with bus number, function number, and device number equal to zero.

Device 0 Offset 1-0 - Vendor ID (1106h)**RO**

15-0 **ID Code** (reads 1106h to identify VIA Technologies)

Device 0 Offset 3-2 - Device ID (3205h).....**RO**

15-0 **ID Code** (reads 3205h to identify the KM400A)

Device 0 Offset 5-4 –Command (0006h).....**RW**

15-10 **Reserved** always reads 0

9 **Fast Back-to-Back Cycle Enable** RO
 0 Fast back-to-back transactions only allowed to the same agent..... default
 1 Fast back-to-back transactions allowed to different agents

8 **SERR# Enable**..... RO
 0 SERR# driver disabled..... default
 1 SERR# driver enabled
 (SERR# is used to report parity errors if bit-6 is set).

7 **Address / Data Stepping** RO
 0 Device never does stepping..... default
 1 Device always does stepping

6 **Parity Error Response**..... **RW**
 0 Ignore parity errors & continue..... default
 1 Take normal action on detected parity errors

5 **VGA Palette Snoop** RO
 0 Treat palette accesses normally..... default
 1 Don't respond to palette accesses on PCI bus

4 **Memory Write and Invalidate Command** RO
 0 Bus masters must use Mem Write..... default
 1 Bus masters may generate Mem Write & Inval

3 **Special Cycle Monitoring** RO
 0 Does not monitor special cycles..... default
 1 Monitors special cycles

2 **PCI Bus Master** RO
 0 Never behaves as a bus master
 1 Can behave as a bus master..... default

1 **Memory Space** RO
 0 Does not respond to memory space
 1 Responds to memory space..... default

0 **I/O Space** RO
 0 Does not respond to I/O space default
 1 Responds to I/O space

Device 0 Offset 7-6 – Status (0210h).....**RWC**

15 Detected Parity Error

0 No parity error detected..... default
 1 Error detected in either address or data phase.
 This bit is set even if error response is disabled (command register bit-6). write one to clear

14 Signaled System Error (SERR# Asserted)

..... always reads 0

13 Signaled Master Abort

0 No abort received default
 1 Transaction aborted by the master
 write one to clear

12 Received Target Abort

0 No abort received default
 1 Transaction aborted by the target
 write one to clear

11 Signaled Target Abort**always reads 0**

0 Target Abort never signaled

10-9 DEVSEL# Timing

00 Fast
 01 Medium always reads 01
 10 Slow
 11 Reserved

8 Data Parity Error Detected

0 No data parity error detected default
 1 Error detected in data phase. Set only if error response enabled via command bit-6 = 1 and KM400A was initiator of the operation in which the error occurred..... write one to clear

7 Fast Back-to-Back Capable**always reads 0**

6 User Definable Features..... **always reads 0**

5 66MHz Capable**always reads 0**

4 Supports New Capability list**always reads 1**

3-0 Reserved**always reads 0**

Device 0 Offset 8 - Revision ID (0nh)**RO**

0-7 **Chip Revision Code**..... default to 0nh (n=rev code)

Device 0 Offset 9 - Programming Interface (00h).....**RO**

7-0 **Interface Identifier****always reads 00**

Device 0 Offset A - Sub Class Code (00h).....**RO**

7-0 **Sub Class Code****reads 00 to indicate Host Bridge**

Device 0 Offset B - Base Class Code (06h).....**RO**

7-0 **Base Class Code**.. reads 06 to indicate Bridge Device

Device 0 Offset D - Latency Timer (00h).....**RW**

Specifies the latency timer value in PCI bus clocks.

7-3 **Guaranteed Time Slice for CPU****default=0**

2-0 **Reserved** (fixed granularity of 8 clks).. always read 0
 Bits 2-1 are writeable but read 0 for PCI specification compatibility. The programmed value may be read back in Offset 75 bits 5-4 (PCI Arbitration 1).

Device 0 Host Bridge Header Registers (continued)Device 0 Offset E - Header Type (00h).....RO7-0 **Header Type Code**reads 00: single functionDevice 0 Offset F - Built In Self Test (BIST) (00h).....RO7 **BIST Supported**reads 0: no supported functions
6-0 **Reserved**always reads 0Device 0 Offset 13-10 - Graphics Aperture Base
(00000008h)RW31-28 **Upper Programmable Base Address Bits**def=027-20 **Lower Programmable Base Address Bits**def=0

These bits behave as if hardwired to 0 if the corresponding Graphics Aperture Size register bit (Device 0 Offset 84h) is 0.

27	26	25	24	23	22	21	20	(This Register)
7	6	5	4	3	2	1	0	(Gr Aper Size)
RW	1M							
RW	0	2M						
RW	RW	RW	RW	RW	RW	0	0	4M
RW	RW	RW	RW	RW	0	0	0	8M
RW	RW	RW	RW	0	0	0	0	16M
RW	RW	RW	0	0	0	0	0	32M
RW	RW	0	0	0	0	0	0	64M
RW	0	0	0	0	0	0	0	128M
0	0	0	0	0	0	0	0	256M

19-0 **Reserved**always reads 00008

Note: The locations in the address range defined by this register are prefetchable.

Device 0 Offset 2D-2C – Subsystem Vendor ID (0000h)R/W115-0 **Subsystem Vendor ID**default = 0
This register may be written once and is then read only.Device 0 Offset 2F-2E – Subsystem ID (0000h)..... R/W115-0 **Subsystem ID**default = 0
This register may be written once and is then read only.Device 0 Offset 37-34 - Capability Pointer (000000A0h) RO

Contains an offset from the start of configuration space.

31-0 **AGP Capability List Pointer**always reads A0h

Device 0 Configuration Registers - Host Bridge

These registers are normally programmed once at system initialization time.

V-Link Control

Device 0 Offset 40 – V-Link Specification ID (00h).....RO

7-0 **Specification Revision** always reads 00

Device 0 Offset 41 – NB V-Link Capability (19h)RO

7-6 **Reserved** always reads 0

5 **16-bit Bus Width Supported** RO

0 Not Supported default

1 Supported

4 **8-Bit Bus Width Supported** RO

0 Not Supported

1 Supported default

3 **4x Rate Supported** RO

0 Not Supported

1 Supported default

2 **2x Rate Supported** RO

0 Not Supported default

1 Supported

1 **Reserved** always reads 0

0 **8x Rate Supported** RO

0 Not Supported

1 Supported default

Device 0 Offset 42 – NB Downlink Command (88h) RW

7-4 **DnCmd Max Request Depth** (0=1 DnCmd).. def = 8

3-0 **DnCmd Write Buffer Size** (doublewords).... def = 8

Device 0 Offset 44-43 – NB Uplink Status (8280h).....RO

15-12 **UpCmd P2C Write Buffer Size** (max lines).. def = 8

11-8 **UpCmd P2P Write Buffer Size** (max lines).. def = 2

7-4 **UpCmd Max Request Depth** (0=1 UpCmd).. def = 8

3-0 **Reserved** always reads 0

Device 0 Offset 45 –NB V-Link Bus Timer (44h)..... RW

7-4 **Timer for Normal Priority Requests from SB**

0000 Immediate

0001 1*4 VCLKs

0010 2*4 VCLKs

0011 3*4 VCLKs

0100 4*4 VCLKs..... default

0101 5*4 VCLKs

0110 6*4 VCLKs

0111 7*4 VCLKs

1000 8*4 VCLKs

1001 16*4 VCLKs

1010 32*4 VCLKs

1011 64*4 VCLKs

11xx Own the bus for as long as there is a request

3-0 **Timer for High Priority Requests from SB**

0000 Immediate

0001 1*2 VCLKs

0010 2*2 VCLKs

0011 3*2 VCLKs

0100 4*2 VCLKs..... default

0101 5*2 VCLKs

0110 6*2 VCLKs

0111 7*2 VCLKs

1000 8*2 VCLKs

1001 16*2 VCLKs

1010 32*2 VCLKs

1011 64*2 VCLKs

11xx Own the bus for as long as there is a request

Device 0 Offset 46 – NB V-Link Misc Control (00h).....RW

7	Downstream High Priority	
0	Disable High Priority Down Commandsdef	
1	Enable High Priority Down Commands	
6	Downlink (C2P) Priority	
0	Treat Downlink Cycles as Normal Priority..def	
1	Treat Downlink Cycles as High Priority	
5-4	Combine Multiple STPGNT Cycles into V-Link Command	
00	Compatible, 1 command per V-Link cmd....def	
01	2 commands per V-Link command	
10	3 commands per V-Link command	
11	4 commands per V-Link command	
3-2	V-Link Master Access Ordering Rules	
00	High priority read, pass normal read (not pass write) ..default	
01	Read (high/normal) pass write (HR>LR>W)	
1x	Read / write in order	
1-0	Reserved	always reads 0

Device 0 Offset 47 – V-Link Control (00h).....RW

7-6	Reserved	always reads 0
5	C2P Read Return Timing	
0	Right after read ack command ..default	
1	Wait until P2C write data flushed	
4-3	Reserved	always reads 0
2	Auto-Disconnect	
0	Disable ..default	
1	Enable	
1	V-Link Disconnect Cycle for HALT cycle	
0	Disable ..default	
1	Enable	
0	V-Link Disconnect Cycle for STPGNT Cycle	
0	Disable ..default	
1	Enable	

Device 0 Offset 48 – NB/SB V-Link Configuration (00h)RW

7	Reservedalways reads 0
6	Rest Bus Width	
0	Disable.....	default
1	Enable	
5	16-bit Bus Width	
0	Disable.....	default
1	Enable	
4	8-Bit Bus Width	
0	Disable.....	default
1	Enable	
3	4x Rate	
0	Disable.....	default
1	Enable	
2	2x Rate	
0	Disable.....	default
1	Enable	
1	Reservedalways reads 0
0	8x Rate	
0	Disable.....	default
1	Enable	

Device 0 Offset 49 – SB V-Link Capability (19h).....RO

7-6	Reserved always reads 0
5	16-bit Bus Width Supported RO
	0 Not Supported default
	1 Supported	
4	8-Bit Bus Width Supported RO
	0 Not Supported	
	1 Supported default
3	4x Rate Supported RO
	0 Not Supported	
	1 Supported default
2	2x Rate Supported RO
	0 Not Supported default
	1 Supported	
1	Reserved always reads 0
0	8x Rate Supported RO
	0 Not Supported	
	1 Supported default

Device 0 Offset 4A – SB Downlink Status (88h).....RO

7-4	DnCmd Max Request Depth (0=1 DnCmd).. def = 8
3-0	DnCmd Write Buffer Size (doublewords).... def = 8

Device 0 Offset 4C-4B – SB Uplink Command (8280h).RW

15-12	UpCmd P2C Write Buffer Size (max lines).. def = 8
11-8	UpCmd P2P Write Buffer Size (max lines).. def = 2
7-4	UpCmd Max Request Depth (0=1 UpCmd).. def = 8
3-0	Reserved always reads 0

Device 0 Offset 4D – SB V-Link Bus Timer (44h).RW

7-4	Timer for Normal Priority Requests from NB
	0000 Immediate
	0001 1*4 VCLKs
	0010 2*4 VCLKs
	0011 3*4 VCLKs
	0100 4*4 VCLKs default
	0101 5*4 VCLKs
	0110 6*4 VCLKs
	0111 7*4 VCLKs
	1000 8*4 VCLKs
	1001 16*4 VCLKs
	1010 32*4 VCLKs
	1011 64*4 VCLKs
	11xx Own the bus for as long as there is a request
3-0	Timer for High Priority Requests from NB
	0000 Immediate
	0001 1*2 VCLKs
	0010 2*2 VCLKs
	0011 3*2 VCLKs
	0100 4*2 VCLKs default
	0101 5*2 VCLKs
	0110 6*2 VCLKs
	0111 7*2 VCLKs
	1000 8*2 VCLKs
	1001 16*2 VCLKs
	1010 32*2 VCLKs
	1011 64*2 VCLKs
	11xx Own the bus for as long as there is a request

Device 0 Offset 4E – CCA Master Priority (00h)..... RW

7	1394 High Priority
	0 Low priority..... default
	1 High priority
6	NIC High Priority
	0 Low priority..... default
	1 High priority
5	Reserved always reads 0
4	USB High Priority
	0 Low priority..... default
	1 High priority
3	Reserved always reads 0
2	IDE High Priority
	0 Low priority..... default
	1 High priority
1	AC97-ISA High Priority
	0 Low priority..... default
	1 High priority
0	PCI High Priority
	0 Low priority..... default
	1 High priority

Device 0 Offset 4F – SB V-Link Misc Control (00h).RW

7	Upstream Command High Priority
	0 Disable high priority up commands..... default
	1 Enable high priority up commands
6-1	Reserved always reads 0
0	Down Cycle Wait for Up Cycle Write Flush (Except Down Cycle Post Write)
	0 Disable..... default
	1 Enable

CPU Interface Control

Device 0 Offset 54 – CPU FSB Frequency (00h).....RW

- 7-6 CPU FSB Frequency.....RO**
 - 00 100 MHz default set from VAD[6,4]
 - 01 133 MHz
 - 10 200 MHz
 - 11 166 MHz
- 5 ROMSIP****RO**
 - 0 Disable default set from VAD[5]
 - 1 Enable
- 4 SDRAM Burst Length 8**
 - 0 Disable default
 - 1 Enable
- 3 Reserved** always reads 0
- 2 PCI Master 8QW Operation**
 - 0 Disable default
 - 1 Enable
- 1-0 Reserved** always reads 0

DRAM Control

These registers are normally set at system initialization time and not accessed after that during normal system operation. Some of these registers, however, may need to be programmed using specific sequences during power-up initialization to properly detect the type and size of installed memory (refer to the VIA Technologies VT8633 BIOS porting guide for details).

Table 6. System Memory Map

<u>Space</u>	<u>Start</u>	<u>Size</u>	<u>Address Range</u>	<u>Comment</u>
DOS	0	640K	00000000-0009FFFF	Cacheable
VGA	640K	128K	000A0000-000BFFFF	Used for SMM
BIOS	768K	16K	000C0000-000C3FFF	Shadow Ctrl 1
BIOS	784K	16K	000C4000-000C7FFF	Shadow Ctrl 1
BIOS	800K	16K	000C8000-000CBFFF	Shadow Ctrl 1
BIOS	816K	16K	000CC000-000CFFFF	Shadow Ctrl 1
BIOS	832K	16K	000D0000-000D3FFF	Shadow Ctrl 2
BIOS	848K	16K	000D4000-000D7FFF	Shadow Ctrl 2
BIOS	864K	16K	000D8000-000DBFFF	Shadow Ctrl 2
BIOS	880K	16K	000DC000-000DFFFF	Shadow Ctrl 2
BIOS	896K	64K	000E0000-000EFFFF	Shadow Ctrl 3
BIOS	960K	64K	000F0000-000FFFFFF	Shadow Ctrl 3
Sys	1MB	—	00100000-DRAM Top	Can have hole
Bus	D Top		DRAM Top-FFFEFFFF	
Init	4G-64K	64K	FFFEFFFF-FFFFFFFFFF	000Fxxxx alias

Device 0 Offset 55 – DRAM Control (00h).....RW

- 7 0WS Back-to-Back Write to Different DDR Bank**
 - 0 Disable default
 - 1 Enable
- 6 Reserved** always reads 0
- 5 DQS Input DLL Adjustment**
 - 0 Disable default
 - 1 Enable
- 4 DQS Output DLL Adjustment**
 - 0 Disable default
 - 1 Enable
- 3 DQM Removal (Always Perform 4-Burst RW)**
 - 0 Disable default
 - 1 Enable
- 2 DQS Output**
 - 0 Disable default
 - 1 Enable
- 1 Auto Precharge for TLB Read or CPU WriteBack**
 - 0 Disable default
 - 1 Enable
- 0 Write Recovery Time**
 - 0 1T (DDR333/266/200) 3T (DDR400) . default
 - 1 2T (DDR333/266/200) 4T (DDR400)

Device 0 Offset 59-58 - DRAM MA Map Type (2222h).RW

15-13 Bank 5/4 MA Map Type (see Table 7 below)

12 Bank 5/4 1T Command Rate

- 0 2T Command default
- 1 1T Command

11-9 Bank 7/6 MA Map Type (see Table 7 below)

8 Bank 7/6 1T Command Rate

- 0 2T Command default
- 1 1T Command

7-5 Bank 1/0 MA Map Type (see Table 7 below)

4 Bank 1/0 1T Command Rate

- 0 2T Command default
- 1 1T Command

3-1 Bank 3/2 MA Map Type (see Table 7 below)

0 Bank 3/2 1T Command Rate

- 0 2T Command default
- 1 1T Command

Table 7. MA Map Type Encoding

000	<u>16Mb</u>	8-bit, 9-bit, 10-bit Column Address
001	<u>64/128Mb</u>	8-bit Column Address default
010	<u>64/128Mb</u>	9-bit Column Address
011	<u>64/128Mb</u>	10/11-bit Column Address
100		-reserved-
101	<u>256Mb</u>	8-bit Column Address
110	<u>256Mb</u>	9-bit Column Address
111	<u>256Mb</u>	10/11-bit Column Address

Table 8. Memory Address Mapping Table

MA:	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
<u>16Mb</u> (000)		24		13	12	11	14	22	21	20	19	18	17	16	15	12 row 10,9,8 col
<u>64/128Mb</u>																x16 (14,8)
2K page	14	24	14	13	12	11	23	22	21	20	19	18	17	16	15	x32 (14,8)
001	27	14	13	PC	24	23	10	9	8	7	6	5	4	3		x8 (14,9)
4K page	14	25	14	13	12	24	23	22	21	20	19	18	17	16	15	x16 (14,9)
010	27	14	13	PC	26	11	10	9	8	7	6	5	4	3		
8K page	14	26	14	13	25	24	23	22	21	20	19	18	17	16	15	x8 (14,10)
011	27	14	13	PC	12	11	10	9	8	7	6	5	4	3		
<u>256Mb</u>																
2K page	25	24	14	13	12	11	23	22	21	20	19	18	17	16	15	x32 (15,8)
101	27	14	13	PC	26	25	10	9	8	7	6	5	4	3		
4K page	26	25	14	13	12	24	23	22	21	20	19	18	17	16	15	x16 (15,9)
110	27	14	13	PC	26	11	10	9	8	7	6	5	4	3		
8K page	27	26	14	13	25	24	23	22	21	20	19	18	17	16	15	x8 (15,10)
111	28	14	13	PC	12	11	10	9	8	7	6	5	4	3		

Device 0 Offset 5F-5A – DRAM Row Ending Address:

<u>Offset 5A – Bank 0 Ending (HA[31:24]) (01h).....</u>	<u>RW</u>
<u>Offset 5B – Bank 1 Ending (HA[31:24]) (01h)</u>	<u>RW</u>
<u>Offset 5C – Bank 2 Ending (HA[31:24]) (01h)</u>	<u>RW</u>
<u>Offset 5D – Bank 3 Ending (HA[31:24]) (01h)</u>	<u>RW</u>
<u>Offset 5E – Bank 4 Ending (HA[31:24]) (01h)</u>	<u>RW</u>
<u>Offset 5F – Bank 5 Ending (HA[31:24]) (01h)</u>	<u>RW</u>
<u>Offset 56 – Bank 6 Ending (HA[31:24]) (01h)</u>	<u>RW</u>
<u>Offset 57 – Bank 7 Ending (HA[31:24]) (01h)</u>	<u>RW</u>

Note : BIOS is required to fill the ending address registers for all banks even if no memory is populated. The endings have to be in incremental order.

Device 0 Offset 61 - Shadow RAM Control 1 (00h).....RW

7-6	CC000h-CFFFFh
00	Read/write disable.....default
01	Write enable
10	Read enable
11	Read/write enable
5-4	C8000h-CBFFFh
00	Read/write disable.....default
01	Write enable
10	Read enable
11	Read/write enable
3-2	C4000h-C7FFFh
00	Read/write disable.....default
01	Write enable
10	Read enable
11	Read/write enable
1-0	C0000h-C3FFFh
00	Read/write disable.....default
01	Write enable
10	Read enable
11	Read/write enable

Device 0 Offset 62 - Shadow RAM Control 2 (00h).....RW

7-6	DC000h-DFFFFh
00	Read/write disable.....default
01	Write enable
10	Read enable
11	Read/write enable
5-4	D8000h-DBFFFh
00	Read/write disable.....default
01	Write enable
10	Read enable
11	Read/write enable
3-2	D4000h-D7FFFh
00	Read/write disable.....default
01	Write enable
10	Read enable
11	Read/write enable
1-0	D0000h-D3FFFh
00	Read/write disable.....default
01	Write enable
10	Read enable
11	Read/write enable

Device 0 Offset 63 - Shadow RAM Control 3 (00h).....RW

7-6	E0000h-EFFFFh
00	Read/write disable default
01	Write enable
10	Read enable
11	Read/write enable
5-4	F0000h-FFFFFh
00	Read/write disable default
01	Write enable
10	Read enable
11	Read/write enable
3-2	Memory Hole
00	None default
01	512K-640K
10	15M-16M (1M)
11	14M-16M (2M)
1-0	SMI Mapping Control (Bit-1 = A,BK Direct Access SMRAM Disable) (Bit-0 = A,BK DRAM Access Enable)

	<u>SMM</u>		<u>Non-SMM</u>	
	<u>Code</u>	<u>Data</u>	<u>Code</u>	<u>Data</u>
00	DRAM	DRAM	PCI	PCI
01	DRAM	DRAM	DRAM	DRAM
10	DRAM	PCI	PCI	PCI
11	DRAM	DRAM	DRAM	DRAM

Device 0 Offset 64 - DRAM Timing for All Banks (E4h)....RW

- 7** Precharge Command to Active Command Period
 - 0 TRP = 2T
 - 1 TRP = 3T (DDR333/266/200), 4T (400). default
- 6** Active Command to Precharge Command Period
 - 0 TRAS = 6T (DDR333/266/200), 8T (400)
 - 1 TRAS = 7T (DDR333/266/200), 10T (400)...def
- 5-4** CAS Latency
 - 00 1.5T
 - 01 2T
 - 10 2.5Tdefault
 - 11 3T
- 3** Reserved always reads 0
- 2** ACTIVE to CMD
 - 0 2T
 - 1 3T (DDR333/266/200), 4T (DDR400)...default
- 1-0** Bank Interleave
 - 00 No Interleave.....default
 - 01 2-way
 - 10 4-way
 - 11 Reserved

For 16Mb SDRAMs, bank interleave is always 2-way

Device 0 Offset 65 - DRAM Arbitration Timer (00h)....RW

- 7-4** AGP Timer (units of 4 MCLKs)..... default = 0
- 3-0** CPU Timer (units of 4 MCLKs)..... default = 0

Device 0 Offset 66 - DRAM Arbitration Control (00h)..RW

- 7** DQS Input Delay Setting
 - 0 Auto (Rx67 reads DLL calibration result) ...def
 - 1 Manual (Rx67 reads DQS input delay)
- 6** DRAM Access Timing
 - 0 2Tdefault
 - 1 3T (Set for 133 MHz DRAM clock)
- 5-4** Arbitration Parking Policy
 - 00 Park at last bus ownerdefault
 - 01 Park at CPU
 - 10 Park at AGP
 - 11 -reserved-
- 3-0** AGP / CPU Priority (units of 4 MCLKs)

Device 0 Offset 67 – DDR Strobe Input Delay (00h)..... RW

- 7-6** Reservedalways reads 0
- 5-0** DQS# Input Delay default = 0
(if Rx66[7]=0, read DLL calibration result)

Device 0 Offset 68 – DDR Strobe Output Delay (00h)... RW

- 7-0** DDR DQS Output Delay default = 0

Device 0 Offset 69 – DRAM Clock Select (00h).....RW

- 7 CPU Operating Frequency Faster Than DRAM**
- 0 CPU Same As or Equal to DRAMdefault
 - 1 CPU Faster Than DRAM by 33 MHz
- 6 DRAM Operating Frequency Faster Than CPU**
- 0 DRAM Same As or Equal to CPUdefault
 - 1 DRAM Faster Than CPU by 33 MHz

<u>Bits 7-6</u>	<u>CPU FSB Freq</u>	<u>DDR DRAM Freq</u>
00	100	100 (DDR200)
	133	133 (DDR266)
	166	166 (DDR333)
01	100	133 (DDR266)
	133	166 (DDR333)
10	–	200 (DDR400)
11	100	166 (DDR333)

Note: The strap information sent from the South Bridge on VAD6,4 determines the CPU FSB frequency, then Rx69[7-6] determines the DRAM frequency and type per the table above. All other combinations are reserved.

- 5 DRAM Queue More Than 2**
- 0 Disabledefault
 - 1 Enable
- 4 DRAM Controller Queue Not Equal To 4**
- 0 Disabledefault
 - 1 Enable
- 3 DRAM 8K Page Enable**
- 0 Disabledefault
 - 1 Enable
- 2 DRAM 4K Page Enable**
- 0 Disabledefault
 - 1 Enable
- 1 Reserved (Do Not Program)..... default = 0**
- 0 Multiple Page Mode**
- 0 Disabledefault
 - 1 Enable

Device 0 Offset 6A - Refresh Counter (00h).....RW

- 7-0 Refresh Counter (in units of 16 DRAM Clocks)**
- 00 DRAM Refresh Disableddefault
 - 01 32 DRAM Clocks
 - 02 48 DRAM Clocks
 - 03 64 DRAM Clocks
 - 04 80 DRAM Clocks
 - 05 96 DRAM Clocks
 -

The programmed value is the desired number of 16-DRAM-Clock units minus one.

Device 0 Offset 6B - DRAM Arbitration Control (00h).RW

7	Fast Read to Write Turn-Around	
0	Disable	default
1	Enable	
6	Page Kept Active When Cross Bank	
0	Disable	default
1	Enable	
5	Burst Refresh	
0	Disable	default
1	Enable	
4	Reserved	always reads 0
3	Swap CA22 / CA14	
0	Enable	default
1	Disable	
2-0	SDRAM Operation Mode Select	
000	Normal SDRAM Mode	default
001	NOP Command Enable	
010	All-Banks-Precache Command Enable (CPU-to-DRAM cycles are converted to All-Banks-Precache commands).	
011	MSR Enable CPU-to-DRAM cycles are converted to commands and the commands are driven on MA[14:0]. The BIOS selects an appropriate host address for each row of memory such that the right commands are generated on MA[14:0].	
100	CBR Cycle Enable (if this code is selected, CAS-before-RAS refresh is used; if it is not selected, RAS-Only refresh is used)	
101	Reserved	
11x	Reserved	

Device 0 Offset 6C – DRAM Early Clock Select (00h).. RW

7-6	CS / CKE Early Clock Select	
00	Latest	default
01		
10		
11	Earliest	
5-4	Early Clock Select for SCMD, MA Output (for 1T Command)	
00	Latest	default
01		
10		
11	Earliest	
3-1	Reserved	always reads 0
0	Reserved (Do Not Program)	default = 0

Device 0 Offset 6D – DRAM MD Output Delay (00h)... RW

7-0	MD Output Delay	default = 0
------------	------------------------------	-------------

Note: Refer to the BIOS Developers Guide for recommended memory configuration detection algorithms and recommended settings for the bits of the above two registers.

PCI Bus Control

These registers are normally programmed once at system initialization time.

Device 0 Offset 70 - PCI Buffer Control (00h).....RW

7	CPU to PCI Post-Write	
0	Disable	default
1	Enable	
6	Reserved	always reads 0
5-4	PCI Master to DRAM Prefetch	
00	Always prefetch	default
x1	Never prefetch	
10	Prefetch only for Enhance command	
3	Reserved	always reads 0
2	PCI Master Read Buffering	
0	Disable	default
1	Enable	
1	Delay Transaction	
0	Disable	default
1	Enable	
0	Reserved	always reads 0

Device 0 Offset 71 - CPU to PCI Flow Control (48h)..RWC

7	Retry Status.....RWC	
0	No retry occurred	default
1	Retry occurred	
6	Retry Timeout Action	
0	Retry forever (record status only)	
1	Flush buffer or return FFFFFFFFh for reads	default
5-4	Retry Count and Retry Backoff	
00	Retry 2 times, backoff CPU	default
01	Retry 16 times	
10	Retry 4 times	
11	Retry 64 times	
3	PCI Burst	
0	Disable	
1	Enable	default
2	Reserved	always reads 0
1	Compatible Type#1 Configuration Cycles	
0	Disable (fixed AD31).....default	
1	Enable	
0	IDSEL Control	
0	AD11, AD12.....default	
1	AD30, AD31	

Device 0 Offset 73 - PCI Master Control (00h).....RW

7	Reserved	always reads 0
6	PCI Master 1-Wait-State Write	
0	Zero wait state TRDY# response.....default	
1	One wait state TRDY# response	
5	PCI Master 1-Wait-State Read	
0	Zero wait state TRDY# response.....default	
1	One wait state TRDY# response	
4	WSC# Enable	
0	Disable.....default	
1	Enable	
3-1	Reserved	always reads 0
0	PCI Master Broken Timer Enable	
0	Disable.....default	
1	Enable. Force into arbitration when there is no FRAME# 16 PCICLK's after the grant.	

Device 0 Offset 75 - PCI Arbitration 1 (00h)RW

7	Arbitration Mode
0	REQ-based (arbitrate at end of REQ#) ..default
1	Frame-based (arbitrate at FRAME# assertion)
6-4	Latency Timer read only, reads Rx0D bits 2:0
3	Reserved always reads 0
2-0	PCI Master Bus Time-Out (force into arbitration after a period of time)
000	Disable default
001	1x16 PCICLKs
010	2x16 PCICLKs
011	3x16 PCICLKs
100	4x16 PCICLKs
...	...
111	7x16 PCICLKs

Device 0 Offset 76 - PCI Arbitration 2 (00h)RW

7	I/O Port 22 Access
0	CPU access to I/O address 22h is passed on to the PCI bus default
1	CPU access to I/O address 22h is processed internally
6	Reserved always reads 0
5-4	Master Priority Rotation Control
00	Disable default
01	Grant to CPU after every PCI master grant
10	Grant to CPU after every 2 PCI master grants
11	Grant to CPU after every 3 PCI master grants
With setting 01, the CPU will always be granted access after the current bus master completes, no matter how many PCI masters are requesting. With setting 10, if other PCI masters are requesting during the current PCI master grant, the highest priority master will get the bus after the current master completes, but the CPU will be guaranteed to get the bus after that master completes. With setting 11, if other PCI masters are requesting, the highest priority will get the bus next, then the next highest priority will get the bus, then the CPU will get the bus. In other words, with the above settings, even if multiple PCI masters are continuously requesting the bus, the CPU is guaranteed to get access after every master grant (01), after every other master grant (10) or after every third master grant (11).	
3-2	REQn# to REQ4# Mapping
00	REQ4# default
01	REQ0#
10	REQ1#
11	REQ2#
1	Reserved always reads 0
0	REQ4# Is High Priority Master
0	Disable default
1	Enable

GART / Graphics Aperture

The function of the Graphics Address Relocation Table (GART) is to translate virtual 32-bit addresses issued by an AGP device into 4K-page based physical addresses for system memory access. In this translation, the upper 20 bits (A31-A12) are remapped, while the lower 12 address bits (A11-A0) are used unchanged.

A one-level fully associative lookup scheme is used to implement the address translation. In this scheme, the upper 20 bits of the virtual address are used to point to an entry in a page table located in system memory. Each page table entry contains the upper 20 bits of a physical address (a “physical page” address). For simplicity, each page table entry is 4 bytes. The total size of the page table depends on the GART range (called the “aperture size”) which is programmable in the VT8377.

This scheme is shown in the figure below.

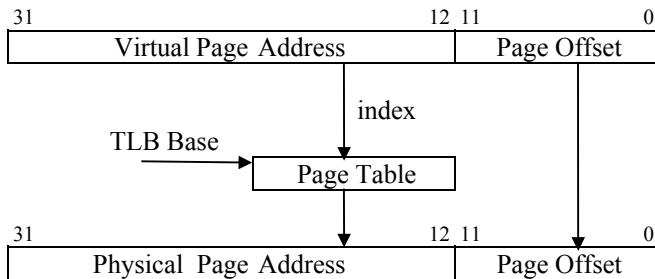


Figure 4. Graphics Aperture Address Translation

Since address translation using the above scheme requires an access to system memory, an on-chip cache (called a “Translation Lookaside Buffer” or TLB) is utilized to enhance performance. The TLB in the VT8377 contains 16 entries. Address “misses” in the TLB require an access of system memory to retrieve translation data. Entries in the TLB are replaced using an LRU (Least Recently Used) algorithm.

Addresses are translated only for accesses within the “Graphics Aperture” (GA). The Graphics Aperture can be any power of two in size from 1MB to 256MB (i.e., 1MB, 2MB, 4MB, 8MB, etc) for AGP 2.0 and 4MB to 2GB for AGP 3.0. The base of the Graphics Aperture can be anywhere in the system virtual address space on an address boundary determined by the aperture size (e.g., if the aperture size is 4MB, the base must be on a 4MB address boundary). The Graphics Aperture Base is defined in register offset 10 of device 0. The Graphics Aperture Size and TLB Table Base are defined in the following register groups (Rx84 and 88 respectively for AGP 2.0 and Rx94 and 98 for AGP 3.0) along with various control bits.

AGP 2.0 Registers

AGP 2.0 registers Rx80-AB are enabled if RxFD[1] = 1 and AGP 3.0 registers Rx80-AB are enabled if RxFD[1] = 0.

Device 0 Offset 83-80 – AGP 2.0 GART/TLB Control...RW

31-16 Reserved	always reads 0
15-8 Reserved (test mode status)	RO
7 Flush Page TLB		
0 Disable	default
1 Enable	
6-0 Reserved (always program to 0)	RW

Note: For any master access to the Graphics Aperture range, snoop will not be performed.

Device 0 Offset 84 – AGP 2.0 Graphics Aperture Size ..RW

7-0 Graphics Aperture Size		
1111111 -reserved-		
11111110 -reserved-		
11111100 4M		
11111000 8M		
11110000 16M		
11000000 32M		
10000000 64M		
00000000 128M		
00000000 256M		

Offset 8B-88 – AGP 2.0 GART Table Base.....RW

31-12 Graphics Aperture Translation Table Base.	RW
Pointer to the base of the translation table in system memory used to map addresses in the aperture range (the pointer to the base of the “Directory” table).		
11-2 Reserved	always reads 0
1 Graphics Aperture		
0 Disable	default
1 Enable	
Note: To disable the Graphics Aperture, set this bit to 0 and set all bits of the Graphics Aperture Size to 0. To enable the Graphics Aperture, set this bit to 1 and program the Graphics Aperture Size to the desired aperture size.		
0 Reserved	always reads 0

Device 0 Offset A3-A0 - AGP 2.0 Capabilities (0020C002h) ..RO

31-24 Reserved	always reads 00
23-20 Major Specification Revision	always reads 0010b
Major rev # of AGP spec that device conforms to		
19-16 Minor Specification Revision	always reads 0000b
Minor rev # of AGP spec that device conforms to		
15-8 Pointer to Next Item	always reads C0 (last item)
7-0 AGP Capability ID	(always reads 02 to indicate it is AGP)

Device 0 Offset A7-A4 - AGP 2.0 Status (1F000201h).... RO

31-24 Maximum AGP Requests	always reads 1Fh Max # of AGP requests the device can manage (32)
23-10 Reserved	always reads 0s
9 Supports SideBand Addressing	always reads 1
8-6 Reserved	always reads 0s
5 Addresses Above 4G Supported	always reads 0†
4 Fast Write Supported	always reads 0†
3 Reserved	always reads 0s
2 4X Rate Supported	always reads 0†
1 2X Rate Supported	always reads 0†
0 1X Rate Supported	always reads 1

†Writable if RxFD[0] = 1.

Device 0 Offset AB-A8 - AGP 2.0 CommandRW

31-24 Request Depth (reserved for target)..	always reads 0s
23-10 Reserved	always reads 0s
9 SideBand Addressing Enable		
0 Disable	default
1 Enable	
8 AGP Enable		
0 Disable	default
1 Enable	
7-6 Reserved	always reads 0s
5 4G Enable		
0 Disable	default
1 Enable	
4 Fast Write Enable		
0 Disable	default
1 Enable	
3 Reserved	always reads 0s
2 4X Mode Enable		
0 Disable	default
1 Enable	
1 2X Mode Enable		
0 Disable	default
1 Enable	
0 1X Mode Enable		
0 Disable	default
1 Enable	

AGP 3.0 Registers

AGP 3.0 registers Rx80-AB are enabled if RxFD[1] = 0 and AGP 2.0 registers Rx80-AB are enabled if RxFD[1] = 1.

Device 0 Offset 83-80 - AGP 3.0 Capabilities (0030C002h).....RO

31-24	Reserved always reads 00
23-20	Major Specification Revision always reads 0011b Major rev # of AGP spec that device conforms to
19-16	Minor Specification Revision always reads 0000b Minor rev # of AGP spec that device conforms to
15-8	Pointer to Next Item always reads C0 (last item)
7-0	AGP Capability ID	(always reads 02 to indicate it is AGP)

Device 0 Offset 87-84 - AGP 3.0 Status (1F000201h).....RO		
31-24	Maximum AGP Requests always reads 1Fh Max # of AGP requests the device can manage (32)
23-16	Reserved always reads 0s†
15-13	Optimum Async Request Size always reads 0s† Suggested setting is 010b or $2^{(2+4)}=64$ Bytes for 8QW access
12-10	Calibration Cycle Setting	
000	4 ms	
001	16 ms	
010	64 ms default†
011	256 ms	
9	Supports SideBand Addressing always reads 1
8	Reserved always reads 0†
7	64-Bit GART Entries always reads 0
6	CPU GART Translation Supported always reads 0
5	Addresses Above 4G Supported always reads 0
4	Fast Write Supported always reads 0
3	AGP 8x Detected Set from AGP8XDT# pin
2	4X Rate Supported Reads 0 if bit-3 = 1 Reads 1 if bit-3 = 0
1	2X Rate Supported always reads 1
0	1X Rate Supported always reads 1

†Writable if RxFD[0] = 1.

Device 0 Offset 8B-88 - AGP 3.0 Command.....RW

31-24	Request Depth	(reserved for target).. always reads 0s
23-13	Reserved always reads 0s
12-10	Calibration Cycle Select default = 0
9	SideBand Addressing	
0	Disable default
1	Enable	
8	AGP	
0	Disable default
1	Enable	
7-6	Reserved always reads 0s
5	Addresses Over 4G	
0	Disable default
1	Enable	
4	Fast Write	
0	Disable default
1	Enable	
3	Reserved always reads 0s
2-0	Transfer Mode Select default = 000b <u>Rx84[3] = 0 (8x mode not detected via AGP8XDT#)</u>
001	1x data transfer rate	
010	2x data transfer rate	
100	4x data transfer rate	
Rx84[3] = 1 (8x mode detected via AGP8XDT#)		
000	-reserved default
001	4x data transfer rate	
010	8x data transfer rate	

Device 0 Offset 93-90 - AGP 3.0 GART / TLB Control.RW

31-10 Reserved always reads 0s
9 Calibration Cycle
 0 Disable default
 1 Enable
8 Graphics Aperture Base Register (Rx13-10) Read
 0 Disable default
 1 Enable
7 GART TLB
 0 Disable (TLB entries are invalidated) default
 1 Enable
6-0 Reserved always reads 0s

Device 0 Offset 97-94 - AGP 3.0 Graphics Aperture SizeRW

31-28 Aperture Page Size Select default = 0000b
 Only 4K pages are allowed
27 Reserved always reads 0s
26-16 Page Size Supported.....**default = 001h**
 If bit-n of this field is 1, indicates support of
 $2^{(n+12)}$ page size. Must be set to 001h (field bit-0
 set) to indicate only 4K pages allowed.
15-12 Reserved always reads 0s
11-0 Aperture Size default = 0

111100111111	4MB
111100111110	8MB
111100111100	16MB
111100111000	32MB
111100110000	64MB
111100100000	128MB
111100000000	256MB
111000000000	512MB
110000000000	1GB
100000000000	2GB <= Max supported
000000000000	4GB <= Do not program

Device 0 Offset 9B-98 - AGP 3.0 GART Table Base.....RW

31-12 GART Base Address [31:12] default = 0
11-0 Reserved always reads 0s

AGP 2.0 / 3.0 Registers

<u>Device 0 Offset AC - AGP Control (00h)RW</u>		
7	AGPRO per strap on MAB9
0	Disabledefault
1	Enable	
6	AGP Read Synchronization	
0	Disabledefault
1	Enable	
5	AGP Read Snoop DRAM Post-Write Buffer	
0	Disabledefault
1	Enable	
4	GREQ# Priority Becomes Higher When Arbiter is Parked at AGP Master	
0	Disabledefault
1	Enable	
3-2	Reservedalways reads 0s
1	AGP Arbitration Parking	
0	Disabledefault
1	Enable (GGNT# remains asserted until either GREQ# de-asserts or data phase ready)	
0	AGP to PCI Master or CPU to PCI Turnaround Cycle	
0	2T or 3T Timingdefault
1	1T Timing	

<u>Device 0 Offset AD – AGP Latency Timer (02h).....RW</u>		
7	AGP Performance Improvement	
0	Disabledefault
1	Enable	
6	Pipe Mode Performance Improvement	
0	Disabledefault
1	Enable	
5	AGP Data Input Enable (for Power Saving)	
0	AGP data input always enableddefault
1	AGP data input only enabled when necessary to avoid redundant transitions	
4	AGP Performance Improvement	
0	Disabledefault
1	Enable	
3-0	AGP Data Phase Latency Timer default = 02h

Device 0 Offset AE – AGP Misc Control (00h)RW

7-3	Reservedalways reads 0
2	AGP Performance Improvement	
0	Disabledefault
1	Enable	
1	DBI / PIPE Mux Function	
0	From DBIH (0.95)default
1	From PIPE (0.9)	
0	CPU GART Read, AGP GART Write Coherency	
0	Disabledefault
1	Enable	

Device 0 Offset AF – AGP 3.0 Control (00h).....RW

7	CPU / PCI Master GART Access	
0	Disabledefault
1	Enable	
6	AGP Calibration	
0	Disabledefault
1	Enable	
5	Mix Coherent / Non-coherent Accesses	
0	Disabledefault
1	Enable	
4	Reservedalways reads 0
3	DBI Function	
0	Disable (DBI input masked and all outputs assume DBI=0)default
1	Enable	
2	DBI Output for AGP Transactions	
0	Disabledefault
1	Enable	
1	DBI Output for Frame Transactions Including Fast-Write	
0	Disabledefault
1	Enable	
0	DBI Output from Frame Transactions	
0	Disabledefault
1	Enable	

Device 0 Offset B0 – AGP Pad Control / Status (8xh)....RW

- 7 AGP 4x Strobe VREF Control**
 0 STB VREF is STB# and vice versa
 1 STB VREF is AGPREF**default**
- 6 AGP 4x Strobe & GD Pad Drive Strength**
 0 Drive strength set to compensation circuit default**default**
 1 Drive strength controlled by RxB1[7-0]
- 5-3 AGP Compensation Circuit N Control Output.RO**
2-0 AGP Compensation Circuit P Control Output.RO
- Note: N = low drive, P = high drive

Device 0 Offset B1 – AGP Drive Strength (63h).....RW

- 7-4 AGP Output Buffer Low Drive Strength..... def=6**
3-0 AGP Output Buffer High Drive Strength..... def=3

Device 0 Offset B2 – AGP Pad Drive / Delay (08h)..... RW

- 7 GD/GBE/GDS, SBA/SBS Control**
 0 SBA/SBS = no cap**default**
 GD/GBE/GDS = no cap
 1 SBA/SBS = **cap**
 GD/GBE/GDS = **cap**
- 6-5 GD / GBE Receive Strobe Delay**
 00 None**default**
 01 Delay by 0.15 ns
 10 Delay by 0.30 ns
 11 Delay by 0.45 ns
- 4 GD[31-16] Staggered Delay**
 0 None**default**
 1 GD[31:16] delayed by 1 ns
- 3 AGP Slew Rate Control**
 0 Disable
 1 Enable.....**default**
- 2 SBA Receive Strobe Delay**
 0 None**default**
 1 Delay by 0.15 ns
- 1-0 GDS Output Delay**
 00 None**default**
 01 Delay by 0.15 ns
 10 Delay by 0.30 ns
 11 Delay by 0.45 ns
 (GDS1 & GDS1# will be delayed an additional 1ns if bit-4 = 1)

Device 0 Offset B3 – AGP Strobe Drive Strength..... RW

- 7-4 AGP Strobe Output Low Drive Strength def=0**
3-0 AGP Strobe Output High Drive Strength def=0

V-Link Drive Control RegistersDevice 0 Offset B4 – V-Link NB Compensation Ctrl (00h)RW

7-5 **V-Link Autocomp High Output Value** ... def=0, RO
4 **Reserved** always reads 0
3-1 **V-Link Autocomp Low Output Value** def=0, RO
0 **Compensation Selection**
 0 Auto Comp (use values in bits 7-1)..... default
 1 Manual Comp (use values in RxB5-B6)

Device 0 Offset B5 – V-Link NB Strobe Drive Ctrl (00h)RW

7-5 **Strobe High Drive Manual Setting** default = 0
4 **Reserved** always reads 0
3-1 **Strobe Low Drive Manual Setting** def = 0
0 **Reserved** always reads 0

Device 0 Offset B6 – V-Link NB Data Drive Ctrl (00h).RW

7-5 **Data High Drive Manual Setting** default = 0
4 **Reserved** always reads 0
3-1 **Data Low Drive Manual Setting** default = 0
0 **Reserved** always reads 0

Device 0 Offset B8 – V-Link SB Compensation Ctrl (00h)RW

7-5 **V-Link Autocomp High Output Value** ... def=0, RO
4 **Reserved** always reads 0
3-1 **V-Link Autocomp Low Output Value** def=0, RO
0 **Compensation Selection**
 0 Auto Comp (use values in bits 7-1)..... default
 1 Manual Comp (use values in RxB9-BA)

Device 0 Offset B9 – V-Link SB Strobe Drive Ctrl (00h)RW

7-5 **Strobe High Drive Manual Setting** default = 0
4 **Reserved** always reads 0
3-1 **Strobe Low Drive Manual Setting** def = 0
0 **Reserved** always reads 0

Device 0 Offset BA – V-Link SB Data Drive Ctrl (00h) RW

7-5 **Data High Drive Manual Setting** default = 0
4 **Reserved** always reads 0
3-1 **Data Low Drive Manual Setting** default = 0
0 **Reserved** always reads 0

Power Management Registers**Device 0 Offset BC – Power Management Mode (00h)..RW**

7	Dynamic Power Management	
0	Disable	default
1	Enable	
6	Halt / Shutdown Enables Power Management	
0	Disable	default
1	Enable	
5	Stop Clock Enables Power Management	
0	Disable	default
1	Enable	
4	Suspend Status Enables Power Management	
0	Disable	default
1	Enable	
3-0	Reserved always reads 0

Device 0 Offset BD – DRAM Power Mgmt Mode (00h) RW

7	DRAM Self-Refresh in Power Management Mode	
0	Disable	default
1	Enable	
6	Dynamic CKE When DRAM Is Idle	
0	Disable	default
1	Enable	
5	Dynamic DRAM I/O Pad Power-Down (Float)	
0	Disable	default
1	Enable	
4-0	Reserved always reads 0

Device 0 Offset BE – Dynamic Clock Stop Control (00h)RW

7	Host CPU Interface Power Management	
0	Disable	default
1	Enable	
6	DRAM Interface Power Management	
0	Disable	default
1	Enable	
5	V-Link Interface Power Management	
0	Disable	default
1	Enable	
4	AGP Interface Power Management	
0	Disable	default
1	Enable	
3	PCI#2 Interface Power Management	
0	Disable	default
1	Enable	
2	Graphics Interface Power Management	
0	Disable	default
1	Enable	
1	Reserved always reads 0
0	Host CPU Fast Power Management (DADS Fast Timing)	
0	Disable	default
1	Enable	

Device 0 Offset BF – DRAM Pad Toggle Reduction (00h)RW

7	MA / SCMD Pin Toggle Reduction	
0	Disable	default
1	Enable (MA and S command pins won't toggle if not accessed)	
6-0	Reserved always reads 0

Extended Power ManagementDevice 0 Offset C0 – Power Management Capability ID RO

7-0 Capability ID always reads 01h

Device 0 Offset C1 – Power Management New Pointer..RO

7-0 New Pointer always reads 00h ("Null" Pointer)

Device 0 Offset C2 – Power Mgmt Capabilities I.....RO

7-0 Power Management Capabilities .. always reads 02h

Device 0 Offset C3 – Power Mgmt Capabilities II RO

7-0 Power Management Capabilities .. always reads 00h

Device 0 Offset C4 – Power Mgmt Control / Status RW

7-2 Reserved always reads 0

1-0 Power State

00 D0 default

01 -reserved-

10 -reserved-

11 D3 Hot

Device 0 Offset C5 – Power Management Status..... RW

7-0 Power Management Status default = 0

Device 0 Offset C6 – PCI-to-PCI Bridge Support Ext... RW

7-0 P2P Bridge Support Extensions default = 0

Device 0 Offset C7 – Power Management Data RW

7-0 Power Management Data default = 0

Host CPU Interface Control Registers

Device 0 Offset D2 – S2K Timing Control III (78h).....RW

The contents of this register are preserved during suspend.
Bits 2-0 have no default value.

7	Disconnect Enable When STPGNT Detected	
6	Write to Read Delay default = 1	
5-4	Read to Write Delay default = 11b	
3	Reserved (Do Not Program) default = 1	
2-0	Write Data Delay from SysDC to CPU Data Output (WrDataDly)	

Device 0 Offset D3 – BIU Arbitration Control.....RW

7-6	Max of Contiguous <u>Probe</u> SysDC Before Switch to Other Type of SysDC	
5-3	Max of Contiguous <u>Read</u> SysDC Before Switch to Other Type of SysDC	
2-0	Max of Contiguous <u>Write</u> SysDC Before Switch to Other Type of SysDC	

Device 0 Offset D4 – BIU Control 1.....RW

7	DRAM Self-Refresh When Disconnected	
0	Disable default	
1	Enable	
6	Probe Next Tag State T1 When PCI Master Read Caching Enabled	
0	Disable default	
1	Enable	
5	64 HCLK Wait Time	
0	Disable default	
1	Enable	
4	Master Request Full Protocol	
0	Enhanced default	
1	Backwards compatible	
VIA recommends setting this bit to 0		
3	DRAM Speculative Read for PCI Master Read (Before Probe Result is Known)	
0	Disable default	
1	Enable	
2	PCI Master Pipeline Request	
0	Disable default	
1	Enable	
1	PCI-to-CPU / CPU-to-PCI (P2C / C2P) Concurrency	
0	Disable default	
1	Enable	
0	Fast Write-to-Read Turnaround	
0	Disable default	
1	Enable	

Device 0 Offset D5 – BIU Control 2RW

7	FWDVLD / PSQH PTR Concurrency	
0	Backwards Compatible default	
1		
6	RHOCTW	
0 default	
1		
5	PMW Address Compare	
0	Backward compatible default	
1	Compare address qualified with PMW	
4	Write Policy for CPU Write to DRAM	
0	Issue DRAM write when FIFO holds more than two requests or DRAM controller idle def	
1	Disable Write Policy	
3	PMR Cycle Control	
0	Stall PMR cycle if MWQ is full default	
1	Execute PMR cycles normally whether MWQ is full or not	
2	FID Command Detect	
0	Disable (command will not have new FID). def	
1	Enable	
1	HALT Command Detect	
0	Disable (command will not do self refresh) def	
1	Enable	
0	Reserved always reads 0	

Device 0 Offset D6 – BIU Control 3RW

7	Memory Write Queue Timer Function	
0	Disable default	
1	Enable	
6	Memory Write Queue Timer Function Trigger	
0	Trigger by data ready for C2M Wr Req def	
1	Trigger by command FIFO utilization	
5-3	Memory Write Queue Timer High Bound def=0	
2-0	Memory Write Queue Timer Low Bound def=0	
Bits 5-0 are defined in units of 4QW / request number		

Device 0 Offset D7 – CPU Strapping Control.....RO

- 7-3 CPU Clock Divideset from VAD[3-0] straps
 00000 11no strap default
 00001 11.5
 00010 12
 00011 12.5
 00100 5
 00101 5.5
 00110 6
 00111 6.5
 01000 7
 01001 7.5
 01010 8
 01011 8.5
 01100 9
 01101 9.5
 01110 10
 01111 10.5
 10000 3
 10001 3.5
 10010 4
 10011 4.5
 101xx -reserved-
2 S2K Drive Strength
 0 Determined by register settings.....default
 1 Determined by auto compensation
1 Fast Address Out Decodeset from ROMSIP#
 0 Normalno strap default
 1 Fast
0 S2K Compensation Circuit
 0 Always Enabledefault
 1 Enable on Disconnect

Device 0 Offset D8 – S2K Compensation Strapping (00h)RW

- 7-4 S2K Pullup Drive Strength default = 0
 3-0 S2K Pulldown Drive Strength default = 0

Device 0 Offset D9 – S2K Compensation Result 1 (00h).RO

- 7-4 Pullup Auto Compensation Result default = 0
 3-0 Pulldown Auto Compensation Result ... default = 0

Device 0 Offset DA – S2K Compensation Result 2.....RW

- 7 S2K Edge DQ Mode..... RO, set from MA11 strap
 0 Central DQdefault
 1 Edge DQ
6-0 S2K Strobe Delay (EdgeDQ).....
set from MA[8-4] straps
 0 Auto Modeno-strap default
 ~0 Strapping Mode

Device 0 Offset DB – S2K Compensation Result 3.....RO

- 7-0 S2K Strobe DLL Delay Counter (Auto)..... def = 0

Device 0 Offset DC – S2K Compensation Result 4 (07h)RW

- 7 S2K Compensation Circuit Trigger
 6 DLL Autodetect..... RO
 5 Delay Compensation Counter Control
 4-3 S2K Pad AC Coupling to VREF Signal in Address / Data Output Clock
2-0 S2K Pad Slew Rate Ctrl (7h is strongest).... def=7h

Device 0 Offset DD – S2K Compensation Result 5 RW

- 7-4 S2K Strobe Output Drive Strength P Control
 3-0 S2K Strobe Output Drive Strength N Control

Device 0 Offset DE – BIU Control 4.....RW

- 7 Pending Memory Read
 0 Read not pending..... default
 1 Read pending
6 Issue Memory Write Queue Ready When Command FIFO is Empty Enough (>24)
 0 Disable..... default
 1 Enable
5 Issue Memory Write Queue If More Than 4 CPU Requests Are Pending
 0 Disable..... default
 1 Enable
4 Fast Write Performance Improvement
 0 Backwards Compatible..... default
 1 Enable performance improvement
3 Issue Write DADS Only When Memory Write Queue Timer or DM Idle or HB Hit
 0 Disable..... default
 1 Enable
2 Compare Partial Address to Decide if CPU-to-Memory Read Hit CPU-to-Memory Write
 0 Compare HA[31:6] (backwards compatible)def
 1 Compare HA[31:12]
1 P2C Write Priority Over Read
 0 Priority not given to Write..... default
 1 Priority given to write
0 DPH5 Performance Improvement
 0 Enable..... default
 1 Disable

Device 0 Offset DF – BIU Control 5..... RO

- 7 Transparent MD to HD Synchronous Mode Performance Improvement def = 0
 0 Disable..... default
 1 Enable
6-0 Reservedalways reads 0

Frame Buffer Control

Device 0 Offset E0 – CPU Direct Access FB Base (00h) RW

- 7-1 **CPU Direct Access FB Base Address[27:21]** . def=0
- 0 **CPU Direct Access Frame Buffer**
 - 0 Disable default
 - 1 Enable

Device 0 Offset E1 – CPU Direct Access FB Size (00h)..RW

- 7 **Internal VGA**
 - 0 Disable default
 - 1 Enable
- 6-4 **Frame Buffer Size**
 - 000 None default
 - 001 -reserved-
 - 010 -reserved-
 - 011 -reserved-
 - 100 16MB
 - 101 32MB
 - 110 64MB
 - 111 -reserved-
- 3-0 **CPU Direct Access FB Base Address[31:28]** . def=0

Device 0 Offset E2 – VGA Arbitration Timer (00h)RW

- 7-4 **VGA High Priority Timer** (units of 16 MCLKs) def=0
- 3-0 **VGA Timer** (units of 16 MCLKs) default = 0

Device 0 Offset E3 – Graphics Arbitration Timer (00h)RW

- 7-4 **Timer to Promote Graphics Priority**
(units of 16 MCLKs) default = 0
- 3-2 **Reserved** always reads 0
- 1-0 **Probing Signal Select** default = 0

DRAM Above 4G Control

Device 0 Offset E4 – Low Top Address Low (00h).....RW

- 7-4 **Low Top Address Low** default = 0
- 3-0 **DRAM Granularity**
 - 0 16M Total DRAM less than 4G default
 - 1 32M Total DRAM less than 8G
 - 2 64M Total DRAM less than 16G
 - 3 128M Total DRAM less than 32G
 - 4 256M Total DRAM less than 64G
 - 5-7 -reserved-

Device 0 Offset E5 – Low Top Address High (FFh).....RW

- 7-0 **Low Top Address High** default = FFH

Device 0 Offset E6 – SMM / APIC Decoding (01h) RW

- 7-6 **Reserved** always reads 0
- 5 **Reserved (Do Not Program)** default = 0
- 4 **I/O APIC Decoding**
 - 0 FECxxxxx accesses go to PCI default
 - 1 FEC00000 to FEC7FFFF accesses go to PCI
 - FEC80000 to FECFFFFF accesses go to AGP
- 3 **MSI (Processor Message) Support**
 - 0 Disable (master access to FEExxxxx will go to PCI) default
 - 1 Enable (master access to FEExxxxx will be passed to host side to do snoop)
- 2 **Top SMM**
 - 0 Disable default
 - 1 Enable
- 1 **Reserved** always reads 0
- 0 **Compatible SMM**
 - 0 Disable
 - 1 Enable default

DRAM Drive Control Registers

Device 0 Offset E8 – DQ Drive Control.....RW

7-4	High Drive – MD and DQM Pins	
0000	Lowest	default
0001		
...	...	
1111	Highest	
3-0	Low Drive – MD and DQM Pins	
0000	Lowest	default
0001		
...	...	
1111	Highest	

Device 0 Offset E9 – CS Drive Control.....RW

7-4	High Drive – CS#, CKE Pins	
0000	Lowest	default
0001		
...	...	
1111	Highest	
3-0	Low Drive – CS#, CKE Pins	
0000	Lowest	default
0001		
...	...	
1111	Highest	

Device 0 Offset EA – MAA Drive Control.....RW

7-4	High Drive – MAA, SRASA, SCASA, SWEA Pins	
0000	Lowest	default
0001		
...	...	
1111	Highest	
3-0	Low Drive – MAA, SRASA, SCASA, SWEA Pins	
0000	Lowest	default
0001		
...	...	
1111	Highest	

Device 0 Offset EC – DRAM S-Port Control.....RW

7	DQ S-Port Control default = 0
6	CS# S-Port Control default = 0
5	MAA S-Port Control default = 0
4	Reserved always reads 0
3	DQS S-Port Control default = 0
2-0	Reserved always reads 0

Device 0 Offset ED – DRAM DQS Drive Control.....RW

7-4	High Drive - DQS	
0000	Lowest	default
0001		
...	...	
1111	Highest	
3-0	Low Drive - DQS	
0000	Lowest	default
0001		
...	...	
1111	Highest	

Device 0 Offset EE – DRAM DQS/MD Duty Cycle CtrlRW

This register is used for duty cycle adjustment.

7-6	DQS / MD Output Rise Time Control	
5-4	DQS / MD Output Fall Time Control	
3-0	Reserved always reads 0

BIOS Scratch

Device 0 Offset F3 – BIOS Scratch Register 3RW

7-0	No hardware function default = 0
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Device 0 Offset F4 – BIOS Scratch Register 4RW

7-0	No hardware function default = 0
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Miscellaneous

Device 0 Offset FD – AGP 2.0 / 3.0 Select.....RW

7-3	Reserved always reads 0
2	AGP Capability Pointer (Rx34) Value	
0	Rx34 = A0h (AGP 2.0) default
1	Rx34 = 80h (AGP 3.0)	
1	Compatible Rx80-AF	
0	AGP 3.0 registers at Rx80-B3 default
1	AGP 2.0 registers at Rx80-B3	
0	AGP Status Register Write	
0	Disable (AGP 3.0 Rx84 is RO) default
1	Enable (AGP 3.0 Rx84 is RW)	

Device 1 Header Registers - PCI-to-PCI Bridge

All registers are located in PCI configuration space. They should be programmed using PCI configuration mechanism 1 through CF8 / CFC with bus number of 0 and function number equal to 0 and device number equal to one.

Device 1 Offset 1-0 - Vendor ID (1106h) RO

15-0 ID Code (reads 1106h to identify VIA Technologies)

Device 1 Offset 3-2 - Device ID (B168h) RO

15-0 ID Code (reads B091h to identify the KM400A PCI-to-PCI Bridge device)

Device 1 Offset 5-4 – Command (0007h).....RW

15-10 Reserved always reads 0
9 Fast Back-to-Back Cycle Enable RO
0 Fast back-to-back transactions only allowed to the same agent default
1 Fast back-to-back transactions allowed to different agents	
8 SERR# Enable RO
0 SERR# driver disabled default
1 SERR# driver enabled	
(SERR# is used to report parity errors if bit-6 is set).	
7 Address / Data Stepping RO
0 Device never does stepping default
1 Device always does stepping	
6 Parity Error Response RW
0 Ignore parity errors & continue default
1 Take normal action on detected parity errors	
5 VGA Palette Snoop (Not Supported) RO
0 Treat palette accesses normally default
1 Don't respond to palette writes on PCI bus (10-bit decode of I/O addresses 3C6-3C9 hex)	
4 Memory Write and Invalidate Command RO
0 Bus masters must use Mem Write default
1 Bus masters may generate Mem Write & Inval	
3 Special Cycle Monitoring RO
0 Does not monitor special cycles default
1 Monitors special cycles	
2 Bus Master RW
0 Never behaves as a bus master	
1 Enable to operate as a bus master on the primary interface on behalf of a master on the secondary interface default
1 Memory Space RW
0 Does not respond to memory space	
1 Enable memory space access default
0 I/O Space RW
0 Does not respond to I/O space	
1 Enable I/O space access default

Device 1 Offset 7-6 - Status (Primary Bus) (0230h).... RWC

15 Detected Parity Error always reads 0
14 Signaled System Error (SERR#) always reads 0
13 Signaled Master Abort	
0 No abort received default
1 Transaction aborted by the master with Master-Abort (except Special Cycles) write 1 to clear
12 Received Target Abort	
0 No abort received default
1 Transaction aborted by the target with Target-Abort
11 Signaled Target Abort always reads 0
10-9 DEVSEL# Timing	
00 Fast	
01 Medium always reads 01
10 Slow	
11 Reserved	
8 Data Parity Error Detected always reads 0
7 Fast Back-to-Back Capable always reads 0
6 User Definable Features always reads 0
5 66MHz Capable always reads 1
4 Supports New Capability list always reads 1
3-0 Reserved always reads 0

Device 1 Offset 8 - Revision ID (0nh) RO†

7-0 KM400A Chip Revision Code (00=First Silicon)

† May be write enabled by Rx44[7])

Device 1 Offset 9 - Programming Interface (00h) RO

This register is defined in different ways for each Base/Sub-Class Code value and is undefined for this type of device.

7-0 Interface Identifier always reads 00

Device 1 Offset A - Sub Class Code (04h).....RO

7-0 Sub Class Code .reads 04 to indicate PCI-PCI Bridge

Device 1 Offset B - Base Class Code (06h).....RO

7-0 Base Class Code .. reads 06 to indicate Bridge Device

Device 1 Offset D - Latency Timer (00h) RO

7-0 Reserved always reads 0

Device 1 Offset E - Header Type (01h) RO

7-0 Header Type Code..... reads 01: PCI-PCI Bridge

Device 1 Offset F - Built In Self Test (BIST) (00h) RO

7 BIST Supported reads 0: no supported functions
6 Start Test write 1 to start but writes ignored
5-4 Reserved always reads 0
3-0 Response Code 0 = test completed successfully

Device 1 Offset 18 - Primary Bus Number (00h).....RW

7-0 Primary Bus Number default = 0
 This register is read write, but internally the chip always uses bus 0 as the primary.

Device 1 Offset 19 - Secondary Bus Number (00h)RW

7-0 Secondary Bus Number default = 0
 Note: AGP must use these bits to convert Type 1 to Type 0.

Device 1 Offset 1A - Subordinate Bus Number (00h)RW

7-0 Primary Bus Number default = 0
 Note: AGP must use these bits to decide if Type 1 to Type 1 command passing is allowed.

Device 1 Offset 1B – Secondary Latency Timer (00h)RO

7-0 Reserved always reads 0

Device 1 Offset 1C - I/O Base (f0h).....RW

7-4 I/O Base AD[15:12] default = 1111b
3-0 I/O Addressing Capability default = 0

Device 1 Offset 1D - I/O Limit (00h).....RW

7-4 I/O Limit AD[15:12] default = 0
3-0 I/O Addressing Capability default = 0

Device 1 Offset 1F-1E - Secondary Status (0000h).....RO

15-0 Rx44[4] = 0: No Function (always reads 0)
Rx44[4] = 1: Read same value as Rx7-6 (Pri Status)

Device 1 Offset 21-20 - Memory Base (fff0h).....RW

15-4 Memory Base AD[31:20] default = FFFh
3-0 Reserved always reads 0

Device 1 Offset 23-22 - Memory Limit (Inclusive) (0000h).....RW

15-4 Memory Limit AD[31:20] default = 0
3-0 Reserved always reads 0

Device 1 Offset 25-24 - Prefetchable Memory Base (fff0h).....RW

15-4 Prefetchable Memory Base AD[31:20] default = FFFh
3-0 Reserved always reads 0

Device 1 Offset 27-26 - Prefetchable Memory Limit (0000h).....RW

15-4 Prefetchable Memory Limit AD[31:20] default = 0
3-0 Reserved always reads 0

Device 1 Offset 2D-2C – Subsystem Vendor ID (0000h)R/W1

15-0 Subsystem Vendor ID default = 0
 This register may be written once and is then read only.

Device 1 Offset 2F-2E – Subsystem ID (0000h).....R/W1

15-0 Subsystem ID default = 0
 This register may be written once and is then read only.

Device 1 Offset 34 – Capability PointerRO

7-0 Capability Pointer . (default) reads 80h if Rx44[5]=1
 reads 00h if Rx44[5]=0

Device 1 Offset 3F-3E – PCI-to-PCI Bridge Control (0000h) RW

15-4 Reserved always reads 0

3 VGA-Present on AGP

0 Forward VGA accesses to PCI Bus default
1 Forward VGA accesses to AGP Bus

Note: VGA addresses are memory A0000-BFFFFh and I/O addresses 3B0-3BBh, 3C0-3CFh and 3D0-3DFh (10-bit decode). "Mono" text mode uses B0000-B7FFFh and "Color" Text Mode uses B8000-BFFFFh. Graphics modes use AxXXxh. Mono VGA uses I/O addresses 3Bx-3Cxh and Color VGA uses 3Cx-3Dxh. If an MDA is present, a VGA will not use the 3Bxh I/O addresses and B0000-B7FFFh memory space; if not, the VGA will use those addresses to emulate MDA modes.

2 Block / Forward ISA I/O Addresses

0 Forward all I/O accesses to the AGP bus if they are in the range defined by the I/O Base and I/O Limit registers (device 1 offset 1C-1D) default

1 Do not forward I/O accesses to the AGP bus that are in the 100-3FFh address range even if they are in the range defined by the I/O Base and I/O Limit registers.

1-0 Reserved always reads 0

Device 1 Configuration Registers - PCI-to-PCI Bridge
AGP Bus Control
Device 1 Offset 40 - CPU-to-AGP Flow Control 1 (00h) RW

7	CPU-AGP Post Write	0 Disable default
	1 Enable	
6	Reserved always reads 0	
5	CPU-AGP One Wait State Burst Write	0 Disable default
	1 Enable	
4-3	Read Prefetch Control	00 Always prefetch default
	x1 Never prefetch	
	10 Prefetch only for Enhance command	
2	MDA Present on AGP	0 Forward MDA accesses to AGP default
	1 Forward MDA accesses to PCI	
Note: Forward despite IO / Memory Base / Limit		
Note: MDA (Monochrome Display Adapter) addresses are memory addresses B0000h-B7FFFh and I/O addresses 3B4-3B5h, 3B8-3BAh, and 3BFh (10-bit decode). 3BC-3BE are reserved for printers.		
Note: If Rx3E bit-3 is 0, this bit is a don't care (MDA accesses are forwarded to the PCI bus).		
1	AGP Master Read Caching	0 Disable default
	1 Enable	
0	AGP Delay Transaction	0 Disable default
	1 Enable	

Table 9. VGA / MDA Memory / IO Redirection

3E[3]	40[2]	VGA	MDA	Axxxx,	B0000	3Cx,	
VGA	MDA	is on	is on	B8xxx	-B7FFF	3Dx	3Bx
Pres.	Pres.			Access	Access	I/O	I/O
0	-	PCI	PCI	PCI	PCI	PCI	PCI
1	0	AGP	AGP	AGP	AGP	AGP	AGP
1	1	AGP	PCI	AGP	PCI	AGP	PCI

Device 1 Offset 41 - CPU-to-AGP Flow Control 2 (08h) RW

7	Retry Status	0 No retry occurred default
	1 Retry Occurred write 1 to clear
6	Retry Timeout Action	0 No action taken except to record status def
	1 Flush buffer for write or return all 1s for read	
5-4	Retry Count	00 Retry 2, backoff CPU default
	01 Retry 4, backoff CPU	
	10 Retry 16, backoff CPU	
	11 Retry 64, backoff CPU	
3	CPU-to-AGP Bursting Timeout	0 Disable
	1 Enable default
2	Reserved always reads 0	
1	CPU-to-PCI/AGP Cycles Invalidate PCI/AGP Buffered Read Data	0 Disable default
	1 Enable	
0	Reserved always reads 0	

Device 1 Offset 42 - AGP Master Control (00h) RW

7	Read Prefetch for Enhance Command	0 Always Perform Prefetch default
	1 Prefetch only if Enhance Command	
6	AGP Master One Wait State Write	0 Disable default
	1 Enable	
5	AGP Master One Wait State Read	0 Disable default
	1 Enable	
4	Break Consecutive PCI Master Accesses	0 Disable default
	1 Enable	
3	Dynamic AGP Memory Read Ready Head / Tail Select	0 Use tail of ready to return data default
	1 Dynamically use head or tail	
2	Claim I/O R/W and Memory Read Cycles	0 Disable default
	1 Enable	
1	Claim Local APIC FEEx xxxx Cycles	0 Disable default
	1 Enable	
0	Support CPU Cycles at 2T Rate	0 Disable default
	1 Enable	

Device 1 Offset 43 - AGP Master Latency Timer (22h) RW

7-4 Host to AGP Time Slot	
0	Disable (no timer)
1	16 GCLKs
2	32 GCLKs default
...	...
F	240 GCLKs
3-0 AGP Master Time Slot	
0	Disable (no timer)
1	16 GCLKs
2	32 GCLKs default
...	...
F	240 GCLKs

Device 1 Offset 44 – Backdoor Register Control (20h).RW

7 Revision ID (Rx8) Write Enable	
0	Disable (Rx8 RO) default
1	Enable (Rx8 RW)
6 Reserved always reads 0
5 Power Management Capability Support	
0	Rx34 reads 00h
1	Rx34 reads 80h default
4 Reflect Rx7-6 Status in Rx1F-1E	
0	Disable (Rx1F-1E always reads 0)..... default
1	Enable (Rx1F-1E reads same as Rx7-6)
3-2 Rx83[2-1] Back Door Value	
1 Rx82[5] Back Door Value (Device Specific Intfc)	
0 Back Door Register Enable for AGP Device ID (Rx47-46)	
0	Disable default
1	Enable

Device 1 Offset 45 – Fast Write Control (72h) RW

7 Force Fast Write Cycle to be QW Aligned (if Rx45[6] = 0)	
0	Disable default
1	Enable
6 Merge Multiple CPU Transactions Into One Fast Write Burst Transaction	
0	Disable
1	Enable default
5 Merge Multiple CPU Write Cycles To Memory Offset 23-20 Into Fast Write Burst Cycles (if Rx45[6] = 0)	
0	Disable
1	Enable default
4 Merge Multiple CPU Write Cycles To Prefetchable Memory Offset 27-24 Into Fast Write Burst Cycles (if Rx45[6] = 0)	
0	Disable
1	Enable default
3 Reserved always reads 0
2 Fast Write Burst 4T Max (No Slave Flow Control)	
0	Disable default
1	Enable
1 Fast Write Fast Back to Back	
0	Disable
1	Enable default
0 Fast Write Initial Block 1 Wait State	
0	Disable default
1	Enable

Rx45 CPU Write CPU Write

Bits	Address 7-4	Address in Mem1	Address in Mem2	Fast Write Cycle
Alignment				
x1xx	-	-	-	QW aligned, burstable
0000	-	-	-	DW aligned, nonburstable
x010	0	0	0	n/a
0010	0	1	1	DW aligned, non-burstable
x010	1	-	-	QW aligned, burstable
x001	0	0	0	n/a
x001	-	1	1	QW aligned, burstable
0001	1	0	0	DW aligned, non-burstable
x011	0	0	0	n/a
x011	1	-	-	QW aligned, burstable
x011	0	1	1	QW aligned, burstable
1000	-	-	-	QW aligned, non-burstable
1010	0	1	1	QW aligned, non-burstable
1001	1	0	0	QW aligned, non-burstable

Device 1 Offset 47-46 – PCI-to-PCI Bridge Device ID...RW

15-0 PCI-to-PCI Bridge Device ID default = 0000

Device 1 Offset 48 – AGP Parity Error Control (00h)...RW

7-2	Reserved always reads 0
1	Pass AGP Data Parity Error to V-Link if Rx4[6]=1 (Parity Error Response Enable)
0	0 Disable default
	1 Enable
0	Pass AGP Address Parity Error to V-Link if Rx5-4[8]=1 (SERR# Enable)
0	0 Disable default
	1 Enable

Device 1 Offset 80 – Capability ID (01h) RO

7-0 Capability ID always reads 01h

Device 1 Offset 81 – Next Pointer (00h) RO

7-0 Next Pointer: Null always reads 00h

Device 1 Offset 82 – Power Mgmt Capabilities 1 (02h) .. RO

7-6	Power Mgmt Capabilities always reads 0
5	Power Mgmt Capabilities programmed via Rx44[1]
4-0	Power Mgmt Capabilities always reads 02h

Device 1 Offset 83 – Power Mgmt Capabilities 2 (00h) .. RO

7-3	Power Mgmt Capabilities always reads 0
2-1	Power Mgmt Capabilities programmed via Rx44[3-2]
0	Power Mgmt Capabilities always reads 0

Device 1 Offset 84 – Power Mgmt Ctrl/Status (00h)..... RW

7-2	Reserved always reads 0
1-0	Power State
00	D0 default
01	-reserved-
10	-reserved-
11	D3 Hot

Device 1 Offset 85 – Power Mgmt Status (00h) RO

7-0 Power Mgmt Status default = 00

Device 1 Offset 86 – P2P Br. Support Extensions (00h) . RO

7-0 P2P Bridge Support Extensions default = 00

Device 1 Offset 87 – Power Management Data (00h) RO

7-0 Power Management Data default = 00

FUNCTIONAL DESCRIPTION - INTEGRATED GRAPHICS

Configuration Strapping

Certain KM400A graphics functions have options that must be selected and fixed at reset (before the register bits controlling these functions can be programmed by software). This is accomplished via power-on configuration strapping.

The strapping pins are pulled low internally and can be individually pulled high through 10 KOhm resistors. These pull-ups and pull-downs do not affect normal operation of the pins, but they do force the pins to a definite state during reset. At the rising edge of the reset signal, this state is sampled, the result is inverted and the data loaded into VGA Sequencer extended register index 12 (EXSR12). The data is used for system configuration. The definitions of the strapping bits at the rising edge of the reset signal are shown in Table 10. Non-graphics straps are described in the pin descriptions for the V-Link signals in the pin descriptions section.

Pin Name	Ball #	CR Bit(s) Value	Description
DP0D10	B7	—	Reserved for test (must be pulled down)
DP0D7	A8	—	Reserved for test (must be pulled down)
DP0D6	B8	EXSR12[6]	Dedicated Display Port 0
			1 = Enable
			0 = Disable
DP0D5	E8	EXSR12[5]	Dedicated Display Port Configuration
			1 = TV Encoder
			0 = TMDS
DP0D4	E9	EXSR12[4]	Panel Port Configuration
			1 = Single 24-bit
			0 = Dual 12-bit
DP0D3	A9	EXSR12[3]	OEM-Defined Panel Type
DP0D2	B9	EXSR12[2]	
DP0D1	C9	EXSR12[1]	
DP0D0	D9	EXSR12[0]	

Table 10. Definition of Strapping Bits at the Rising Edge of the Reset Signal

PCI Configuration and Integrated AGP

PCI Configuration

The KM400A graphics Vendor ID register (Index 00H) in the PCI Configuration space is hardwired to 5333H to specify S3 Graphics Incorporated as the vendor. The Device ID register is hardwired to 8D01H.

Bits 10-9 of the Status register (Index 06H) are hardwired to 01b to specify medium DEVSEL timing. The Class Code register (Index 08H) is hardwired to 30000xxH to specify that the KM400A is a VGA compatible device.

PCI06[4] is hardwired to 1 to indicate a capabilities list is available. PCI34[7-0] point to the PCI power management registers starting at offset DC. The basic power states (D0-D3) are supported as explained by the PCI Bus Power Management Interface Specification, Revision 1.1.

PCI Subsystem ID

The Subsystem ID and Subsystem Vendor ID are located in a 32-bit read only register at PCI Configuration Space Index 2C. These registers reflect the content of 4 read/write CR registers as follows:

Register	CR Space	PCI Config Space
Subsystem Vendor ID Low Byte	CR35	Index 2CH
Subsystem Vendor ID High Byte	CR36	Index 2DH
Subsystem ID Low Byte	CR37	Index 2EH
Subsystem ID High Byte	CR38	Index 2FH

Table 11. PCI Subsystem ID and Subsystem Vendor ID Registers

These registers allow identification of particular vendors using the same graphics chip. The following design allows the subsystem identification to be handled by software (no hardwiring).

All KM400A motherboard designs will incorporate the video BIOS into the system BIOS ROM. The system BIOS must load the subsystem ID information in the KM400A before any ID scanning takes place. To do this, it must turn on the KM400A, enable I/O accesses in the PCI configuration space, unlock the CR registers, program the subsystem ID information in the registers described above, then turn off the KM400A.

Display Memory

The KM400A north bridge utilizes a Shared Memory Architecture (SMA) for Frame Buffer Memory. SMA allows system memory to be efficiently shared by the host CPU and the KM400A north bridge graphics controller. By default, no system memory is allocated for the graphics frame buffer, but up to 32 Mbytes may be allocated depending on user preference, application requirements, and the total size of system memory.

Note: Frame buffer memory is allocated from system memory at bootup time. Changing the display settings to a resolution requiring additional frame buffer memory will require a system reboot to be performed.

Frame Buffer Size	Dev 0 RxFB[6-4] Register Setting	CR36[7-5] † Register Setting
0 Mbytes	000	000
8 Mbytes	011	011
16 Mbytes	100	100
32 Mbytes	101	101

† For driver information only (not connected to hardware)

Table 12. Supported Frame Buffer Memory Configurations

Display Output

S3 Graphics endeavors to provide the maximum available noise-free mode support for any given device. Mode support is influenced by:

- Amount and speed of system memory
- Display resolution and color depth
- Maximum refresh capability detected for the display device
- Single or dual display engine usage

All the tables in this section are based on the use of DDR266 system memory.

Single CRT or Panel Display

Panel displays follow the 60 Hz refresh rate column.

RESOLUTION	BPP	CRT MAXIMUM REFRESH				
		60	75	85	100	120
640x480	8	✓	✓	✓	✓	✓
	16	✓	✓	✓	✓	✓
	32	✓	✓	✓	✓	✓
800x600	8	✓	✓	✓	✓	✓
	16	✓	✓	✓	✓	✓
	32	✓	✓	✓	✓	✓
1024x768	8	✓	✓	✓	✓1	
	16	✓	✓	✓1	✓1	
	32	✓	✓	✓1		
1152x864	8	✓	✓			
	16	✓	✓			
	32	✓	✓			
1280x1024	8	✓	✓	✓		
	16	✓	✓	✓		
	32	✓	✓	✓2		
1440x1050	8	✓	✓	✓		
	16	✓	✓	✓1		
	32	✓	✓2	✓3		
1600x1200	8	✓	✓	✓		
	16	✓	✓1	✓1		
	32	✓2				

Table 13. Single CRT / Panel Display Resolutions

Legend:

- ✓ = Mode and overlay available with either DDR200 or DDR266
- 1 = Overlay not available with DDR200
- 2 = Mode and overlay not available with DDR200
- 3 = Mode and overlay not available with DDR200,
Overlay not available with DDR266

Multiple Displays – CRT + 640x480 (VGA) Panel

CRT RESOLUTION	BPP	LCD 8BPP					LCD 16BPP					LCD 32BPP				
		CRT MAXIMUM REFRESH					CRT MAXIMUM REFRESH					CRT MAXIMUM REFRESH				
		60	75	85	100	120	60	75	85	100	120	60	75	85	100	120
640x480	8	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√
	16	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√
	32	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√
800x600	8	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√1
	16	√	√	√	√	√	√	√	√	√	√1	√	√	√	√	√1
	32	√	√	√	√1		√	√	√	√1		√	√	√	√	√1
1024x768	8	√	√	√	√1		√	√	√	√1		√	√	√1	√1	
	16	√	√	√1			√	√	√1			√	√	√1		
	32	√	√	√1			√	√	√1			√	√	√1		
1152x864	8	√	√				√	√				√	√			
	16	√	√				√	√				√	√1			
	32	√	√				√	√1				√	√1			
1280x1024	8	√	√1	√1			√	√1	√1			√	√1			
	16	√	√1	√1			√	√1	√1			√	√2			
	32	√	√1	√1			√	√				√2				
1400x1050	8	√	√1				√	√1				√2				
	16	√	√1				√2					√2				
	32	√2														
1600x1200	8	√2					√2									
	16	√2														
	32															

Table 14. Supported Resolutions – CRT + 640x480 (VGA) Panel

Legend:

√ = Mode and overlay available with either DDR200 or DDR266

1 = Overlay not available with DDR200

2 = Mode and overlay not available with DDR200

3 = Mode and overlay not available with DDR200, overlay not available with DDR266

Multiple Displays – CRT + 800x600 (SVGA) Panel

CRT RESOLUTION	BPP	LCD 8BPP					LCD 16BPP					LCD 32BPP				
		CRT MAXIMUM REFRESH					CRT MAXIMUM REFRESH					CRT MAXIMUM REFRESH				
		60	75	85	100	120	60	75	85	100	120	60	75	85	100	120
640x480	8	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√
	16	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√
	32	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√
800x600	8	√	√	√	√	√	√	√	√	√	√	√	√	√	√	√1
	16	√	√	√	√	√	√	√	√	√	√1	√	√	√	√	√1
	32	√	√	√	√1		√	√	√	√1		√	√	√	√	√1
1024x768	8	√	√	√	√1		√	√	√	√1		√	√	√1	√1	
	16	√	√	√1			√	√	√1			√	√	√1		
	32	√	√	√1			√	√	√1			√	√	√1		
1152x864	8	√	√				√	√				√	√			
	16	√	√				√	√				√	√1			
	32	√	√				√	√1				√	√1			
1280x1024	8	√	√1	√1			√	√1	√1			√				
	16	√	√1	√1			√	√1	√1			√2				
	32	√	√1	√1			√	√				√2				
1400x1050	8	√	√1				√	√1				√2				
	16	√	√1				√2									
	32	√2														
1600x1200	8	√2														
	16	√2														
	32															

Table 15. Supported Resolutions – CRT + 800x600 (SVGA) Panel

Legend:

√ = Mode and overlay available with either DDR200 or DDR266

1 = Overlay not available with DDR200

2 = Mode and overlay not available with DDR200

3 = Mode and overlay not available with DDR200, overlay not available with DDR266

Multiple Displays – CRT + 1024x768 (XGA) Panel

CRT RESOLUTION	BPP	LCD 8BPP					LCD 16BPP					LCD 32BPP				
		CRT MAXIMUM REFRESH					CRT MAXIMUM REFRESH					CRT MAXIMUM REFRESH				
		60	75	85	100	120	60	75	85	100	120	60	75	85	100	120
640x480	8	$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$
	16	$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$
	32	$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$
800x600	8	$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$
	16	$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$
	32	$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$		$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$		$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$
1024x768	8	$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$		$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$		$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$
	16	$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$			$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$			$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$	
	32	$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$			$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$			$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$	
1152x864	8	$\sqrt{2}$	$\sqrt{2}$				$\sqrt{2}$	$\sqrt{2}$				$\sqrt{2}$	$\sqrt{2}$			
	16	$\sqrt{2}$	$\sqrt{2}$				$\sqrt{2}$	$\sqrt{2}$				$\sqrt{2}$	$\sqrt{2}$			
	32	$\sqrt{2}$	$\sqrt{2}$				$\sqrt{2}$	$\sqrt{2}$				$\sqrt{2}$	$\sqrt{2}$			
1280x1024	8	$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$			$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$			$\sqrt{2}$	$\sqrt{3}$			
	16	$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$			$\sqrt{2}$	$\sqrt{2}$	$\sqrt{2}$			$\sqrt{2}$	$\sqrt{3}$			
	32	$\sqrt{2}$	$\sqrt{2}$				$\sqrt{2}$					$\sqrt{2}$				
1400x1050	8	$\sqrt{2}$	$\sqrt{2}$				$\sqrt{2}$					$\sqrt{2}$				
	16	$\sqrt{2}$					$\sqrt{2}$									
	32	$\sqrt{2}$														
1600x1200	8	$\sqrt{2}$														
	16	$\sqrt{2}$														
	32															

Table 16. Supported Resolutions – CRT + 1024x768 (XGA) Panel

Legend:

$\sqrt{2}$ = Mode and overlay available with either DDR200 or DDR266

1 = Overlay not available with DDR200

2 = Mode and overlay not available with DDR200

3 = Mode and overlay not available with DDR200, overlay not available with DDR266

TV Display

RESOLUTION	BPP	VT1621 TV ENCODER		VT1622 TV ENCODER		CH7009/ CH7010		SAA7108/ SAA7109	
		NTSC	PAL	NTSC	PAL	NTSC	PAL	NTSC	PAL
40x25 Text	color	✓	✓	✓	✓	✓	✓	✓	✓
80x25 Text	color	✓	✓	✓	✓	✓	✓	✓	✓
320x200	8	✓	✓	✓	✓	✓	✓	✓	✓
640x480	4	✓	✓	✓	✓	✓	✓	✓	✓
	8	✓	✓	✓	✓	✓	✓	✓	✓
	16	✓	✓	✓	✓	✓	✓	✓	✓
	32	✓	✓	✓	✓	✓	✓	✓	✓
	8	✓	✓	✓	✓	✓	✓	✓	✓
800x600	16	✓	✓	✓	✓	✓	✓	✓	✓
	32	✓	✓	✓	✓	✓	✓	✓	✓
	8			✓	✓	✓	✓		
1024x768	16			✓	✓	✓	✓		
	32			✓	✓	✓	✓		

Table 17. Supported Resolutions – TV Display

Legend:

✓ = Supported

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Table 18. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes
T _C	Case operating temperature	0	85	°C	1
T _S	Storage temperature	-55	125	°C	1
V _{IN}	Input voltage	-0.5	V _{RAIL} + 10%	Volts	1, 2
V _{OUT}	Output voltage	-0.5	V _{RAIL} + 10%	Volts	1, 2

Note 1. Stress above the conditions listed may cause permanent damage to the device. Functional operation of this device should be restricted to the conditions described under operating conditions.

Note 2. V_{RAIL} is defined as the V_{CC} level of the respective rail. The CPU interface is CPU dependent. Memory can be 1.5V or 3.3V. V-Link can be 2.5V only. Display can be 3.3V only. AGP can be 1.5V only.

DC Characteristics

T_C = 0-85°C, V_{RAIL} = V_{CC} ± 5%, V_{CORE} = 2.5V ± 5%, GND=0V

Table 19. DC Characteristics

Symbol	Parameter	Min	Max	Unit	Condition
V _{IL}	Input Low Voltage	-0.50	0.8	V	
V _{IH}	Input High Voltage	2.0	V _{CC} +0.5	V	
V _{OL}	Output Low Voltage	-	0.55	V	I _{OL} = 4.0mA
V _{OH}	Output High Voltage	2.4	-	V	I _{OH} = -1.0mA
I _{IL}	Input Leakage Current	-	±10	uA	0 < V _{IN} < V _{CC}
I _{OZ}	Tristate Leakage Current	-	±20	uA	0.55 < V _{OUT} < V _{CC}

AC Timing Specifications

AC timing specifications provided are based on external zero-pf capacitance load. Min/max cases are based on the following table:

Table 20. AC Timing Min / Max Conditions

Parameter	Min	Max	Unit
5.0V Power	4.75	5.25	Volts
3.3V Power (I/O Pads, VCCQ for 2x transfer mode)	3.135	3.465	Volts
2.5V Power (Internal Logic)	2.375	2.625	Volts
1.5V Power (VCCQ for 8x/4x transfer mode)	1.425	1.575	Volts
Case Temperature	0	85	°C

Drive strength for selected output pins is programmable. See Rx6D for details.

MECHANICAL SPECIFICATIONS

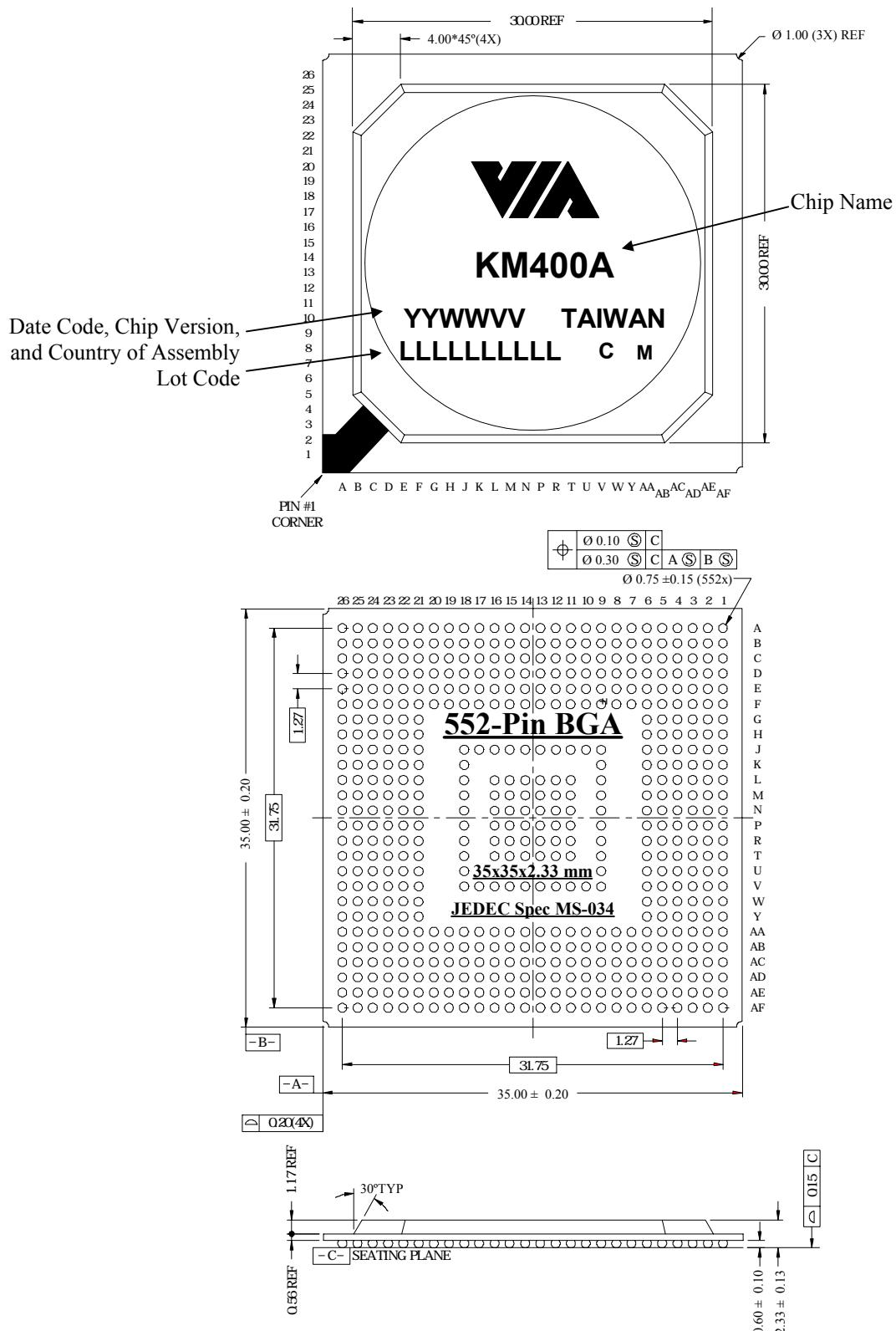


Figure 5. Mechanical Specifications - 552-Pin HSBGA Ball Grid Array Package with Heat Spreader