Data Sheet

K8M800 Desktop North Bridge

with Integrated UniChrome Pro 3D / 2D Graphics Controller

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VIA TECHNOLOGIES, INC.

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Offices:

VIA Technologies Incorporated
Taiwan Office:
8th Floor, No. 533
Chung-Cheng Road, Hsin-Tien
Taipei, Taiwan ROC
Tel: (886-2) 2218-5452
Fax: (886-2) 2218-5453
Home page: http://www.via.com.tw

VIA Technologies Incorporated
USA Office:
940 Mission Court
Fremont, CA 94539
USA
Tel: (510) 683-3300
Fax: (510) 683-3301 or (510) 687-4654
Home Page: http://www.viatech.com

S3 Graphics Incorporated
USA Office:
1045 Mission Court
Fremont, CA 94539
USA
Tel: (510) 687-4900
Fax: (510) 687-4901
Home Page: http://www.s3graphics.com

REVISION HISTORY

Document Release	Date	Revision	Initials
1.0	2/9/04	Initial external release	EY
1.01	2/17/04	Fixed page footer on pages 8-9 Modified HTRST# swing voltage to 1.5V Changed GTVCLK+ / GDVP1CLK+ to GTVCLK / GDVP1CLK Changed GTVCLK- / GDVP1CLK- to GTVCLK# / GDVP1CLK# Removed AC Characteristics table of HT Interface Reset / Stop Updated top marking	EY

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

K8M800
NORTH BRIDGE

800MHz AMD Opteron/Athlon 64 HyperTransport™ Interface
Integrated UniChrome Pro 3D / 2D Graphics Controller
533 MB / Sec V-Link Interface
External 8x / 4x AGP Bus

PRODUCT FEATURES

- **Defines Highly Integrated Solutions for High Performance Workstation & PC Desktop Designs**
  - High performance North Bridge with HyperTransport interface to AMD™ K8 CPU plus AGP 8x external bus to external Graphics Controller plus high-speed V-Link interface to South Bridge
  - Combines with VIA VT8237 V-Link South Bridge for integrated LAN, Audio, Serial-ATA / RAID, ATA133 IDE and 8 USB 2.0 ports
  - 587 Ball Grid Array package with 35 x 35 mm body size, 1.27mm ball pitch and heat spreader
  - 1.5V core, 0.15 u process
- **High Performance HyperTransport CPU Interface**
  - Processor interface via HyperTransport interface
  - 800 / 600 / 400 / 200 MHz clock rates with 1600 / 1200 / 800 / 400 MT/s (Mega-Transfers per second) in both directions simultaneously (up to 6.4 GB/sec using 16-bit data transfer mode)
  - 8 or 16-bit control / address / data transfer both directions (transmit and receive may be different widths and / or speeds)
  - Default 8-bit / 200 MHz operation on startup with speedup to dual 16-bit, 800 MHz operation under software control
  - Supports isochronous AGP-to-CPU and PCI-to-CPU transactions
- **Full Featured Accelerated Graphics Port (AGP) 8x Controller**
  - AGP v3.0 compliant 8x/4x transfer mode with Fast Write support
  - 1.5V AGP IO interface
  - Pipelined split-transaction long-burst transfers up to 2.1 GB/sec (4 bytes x 533 MHz)
  - Supports Side Band Addressing (SBA) mode
  - Supports Flush / Fence commands
  - Supports DBI (Dynamic Bus Inversion)
  - Pseudo-synchronous AGP and CPU interfaces with optimal skew control
  - Thirty-two level read and write request queue
  - One-ninety-two level (quadwords) read data FIFO (1,536 bytes)
  - Sixty-four level (quadwords) write data FIFO (512 bytes)
  - Graphics Address Relocation Table (GART)
    - One level TLB structure
    - Sixteen entry fully associative page table
    - LRU replacement scheme
  - VPX-64 / VPX-II support (see separate VIA VT8101 and VT8102 data sheet)

- **High Bandwidth 533 MB/Sec 8-Bit V-Link Host Controller**
  - Supports 66 MHz, 4x and 8x transfer modes, V-Link Host interface with total bandwidth of 533 MB/sec
  - Half duplex transfers with separate command / strobe for 4x 8-bit mode, full duplex for 8x 4-bit mode
  - Request / Data split transaction
  - Transaction assurance for V-Link Host to Client access eliminates V-Link Host-Client Retry cycles
  - Intelligent V-Link transaction protocol to minimize data wait-state / throttle transfer latency
  - Highly efficient V-Link arbitration with minimum overhead
- **Advanced System Power Management Support**
  - ACPI 1.0B and PCI Bus Power Management 1.1 compliant
  - Supports HTSTOP# (HyperTransport Bus Stop) protocol
  - Low-leakage I/O pads

- **Integrated UniChrome Pro Graphics with 2D / 3D / Video Controllers**
  - Optimized Unified Memory Architecture (UMA)
  - Supports 16 / 32 / 64 MB Frame Buffer sizes
  - 200 MHz Graphics Engine Clock
  - Two independent 128-bit data paths between North Bridge and graphics core to improve the video performance, one for frame buffer access and one for texture / command access
  - PCI v2.2 compliant
  - AGP v3.0 compliant

2D Acceleration Features

- Hardware 2D rotation
- 128-bit 2D graphics engine
- Supports ROP3, 256 operations
- Supports 8 bpp, 15 / 16 bpp and 32 bpp color depth modes
- BitBLT (Bit Block Transfer) functions including alpha BLTs
- True-color hardware cursor (64x64x32 bpp) with 256-level blending effect
- Color expansion, source Color Key and destination Color Key
- Bresenham line drawing / style line function
- Transparency mode
- Window clipping
- Text function

3D Acceleration Features

3D Graphics Processor

- 128-bit 3D graphics engine
- Dual pixel rendering pipes
- Dual texture units
- Floating-point setup engine
- Internal full 32-bit ARGB format for high rendering quality
- 8K Texture Cache

Capability

- ROP2 supported
- Supports various texture formats, including: 16 / 32 bbp ARGB, 8 bbp Palletized (ARGB), YUV 422 / 420 and compressed texture (DXTC)
- Texture sizes up to 2048x2048
- Microsoft DirectX texture compression
- High quality texture filter for Nearest, Linear, Bi-linear, Tri-linear and Anisotropic modes
- Flat and Gouraud shading
- Vertex Fog and Fog Table
- Z-Bias, LOD-Bias, Polygon offset, Edge Anti-aliasing and Alpha Blending
- Bump mapping and cubic mapping
- Hardware Back-Face culling
- Specular Lighting

Performance

- Two textures per pass
- Triangle rate up to 4.5 million triangles per second
- Pixel rate up to 200 million pixels per second for 2 textures each
- Texel bilinear fill rate up to 400 million texels per second
- High quality dithering

Video Acceleration Features

High Quality Video Processor

- RGB555, RGB565, RGB8888 and YUV422 video playback formats
- High quality 5-tap horizontal and 5-tap vertical scaler (up or down) for both horizontal and vertical scaling (linear interpolation for horizontal and vertical p-scaling and filtering for horizontal and vertical down-scaling)
- Independent graphics and video gamma tables
- 2 sets of Color and Chroma key support
- Color enhancement for contrast, hue, saturation and brightness
- YUV-to-RGB color space conversion
- Bob, Weave, Median-filter and Adaptive de-interlacing modes
- 3:2 / 2:2 pull-down detection
- De-blocking mode support
- Combining of many special effects such as filter, scaling up or down, sub-picture blending, de-interlacing and de-blocking to one pass process
- Tear-free double / triple buffer flipping
- Input video vertical blanking or line interrupt
- Video gamma correction

Video Overlay

- Simultaneous graphics and TV video playback overlay
- Supports video window overlay
- Supports both YUV and RGB format Chroma key
- Supports 16 operations for Color and Chroma key
- Hardware sub-picture blending

MPEG Video Playback

- MPEG-2 hardware VLD (Various Length Decode), iDCT and motion compensation for full speed DVD and MPEG-2 playback at full D1 resolution
- MPEG-4 ASP (Advanced Simple Profile) Level 5 with GMC (Global Motion Compensation) L0 / L1 and 1/4 pixel MC support for high video quality and performance
- High quality DVD and streaming video playback
- DVD playback auto-flipping
- DVD sub-picture playback overlay

Video Capture Capability

- 8-bit capture port following ITU-R BT656, VIP1.1 and VIP2.0 standards supporting 16 / 32-bit RGB and YUV422 video capture formats
- Video capture and playback tear free auto flipping
- Multiplexed on Digital Video Port 0 (DVP0 selectable as Video Capture or TV-Out)
- External Hsync / Vsync support

DuoView+™ Capability

- WinXP, WinME and Win98 multi-monitor, extended desktop support
- Provides two independent display engines, each of which can display completely different information at different resolutions, pixel depths and refresh rates
- Improved display flexibility with simultaneous CRT / DVI, CRT / TV, DVI / TV and other combined operation

Full Software Support

- Microsoft DirectX 7.0, 8.0 and 9.0 compatible
- Microsoft DirectX Texture Compression (DXTC / S3TC)
- Supports OpenGL™
- Drivers for major operating systems and APIs: Windows® 9x / ME, Windows 2000, Windows XP, Direct3D™, DirectDraw™, DirectShow™ and OpenGL™ ICD for Windows 9x / ME and XP
- Windows NT 4.0 Standard VGA driver

- **Extensive Display Support for External Video Output**
  - CRT interface
  - Digital Video Port supporting TV-Out or Video Capture
  - 12-bit interface to external TMDS transmitter for driving a DVI monitor
  - 12-bit TV-Out interface to TV encoder

CRT Display

- CRT display interface with 24-bit true-color RAMDAC up to 350 MHz pixel rate with gamma correction capability
- Supports CRT resolutions up to 1920 x 1440

12-bit TMDS Transmitter Interface

- 12-bit, 1.5V low-swing, DVO interface for connecting DVI Monitor through TMDS transmitter
- 12-bit DDR and clock rate up to 165 MHz
- Built-in digital phase adjuster to fine tune signal timing between clock and data bus

TV-Out Interface

- 12-bit DVO interface to external TV encoder for ATSC, NTSC or PAL TV display
- 1.5V signaling on GDVP0 port or 3.3V signaling on DVP0 port

- **Advanced Graphics Power Management Support**
  - Built-in reference voltage generator and monitor sense circuits
  - Automatic panel power sequencing and VESA DPMS (Display Power Management Signaling) CRT power-down
  - External I/O signal controls enabling of graphics controller into standby / suspend-off state
  - Dynamic clock gating for inactive functions to achieve maximum power savings
  - I^2C Serial Bus and DDC / E-DDC Monitor Communications for Plug-and-Play configuration

K8M800 SYSTEM OVERVIEW

The K8M800 is a high performance, cost-effective and energy efficient UMA North Bridge with integrated UniChrome Pro graphics / video controller used for the implementation of 64-bit capable desktop personal computer systems based on AMD Opteron/Athlon 64 processors.

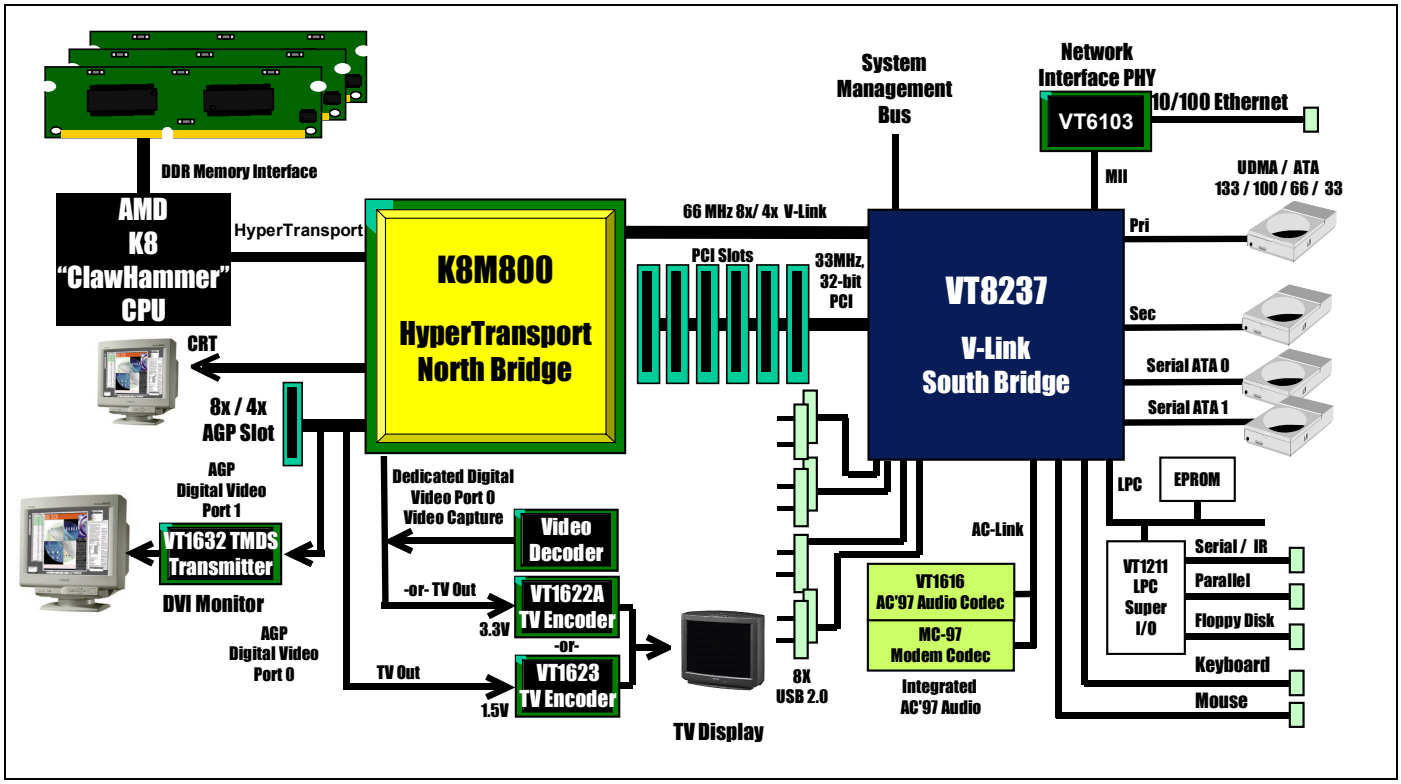


Figure 1. System Block Diagram

A complete 64-bit Opteron/Athlon 64 chip set consists of the K8M800 North Bridge and the VT8237 V-Link South Bridge. The K8M800 integrates VIA's K8T800 system controller with high-performance UniChrome Pro graphics and video controller, and flat panel display and TV out interfaces into a single chip package. The K8M800 provides superior performance between the CPU/HyperTransport, V-Link interface and internal or external AGP 8x bus with pipelined, burst and concurrent operation. The VT8237 is a highly integrated peripheral controller, it includes V-Link-to-PCI / V-Link-to-LPC controllers, and integrates Serial ATA and Ultra DMA IDE controllers, USB2.0 host controller, 10/100Mb networking MAC, AC97 and system power management controllers. Its internal bus structure is based on a 66 MHz PCI bus that provides 2x bandwidth compared to previous generation PCI bridge chips.

K8M800 Overview

The K8M800 interfaces to the AMD Opteron/Athlon 64 processor via the HyperTransport interface with data transfer rate of 1.6 GT/sec, 1.2 GT/sec, 800 MT/sec or 400 MT/sec each direction (input and output), simultaneously, providing a total maximum data transfer bandwidth of 6.4 GB/sec. Isochronous AGP-to-CPU and PCI Master-to-CPU transactions are supported for time constraint, periodic data transmissions.

The AGP controller is AGP v3.0 compliant with up to 2.1GB/second data transfer rate. It supports pseudo-synchronous AGP and HyperTransport interface for optimal system performance. Deep read (1536 bytes) and write (512 bytes) FIFO are integrated for optimal bus utilization and minimum data transfer latency.

The K8M800 North Bridge interfaces to the South Bridge through the high-speed 8x 66 MHz (533MB/sec) V-Link interface. Deep pre-fetch and post write buffers are included to allow for concurrent CPU and V-Link operation. The combined K8M800 North Bridge and VT8237 South Bridge system supports enhanced PCI bus commands such as "Memory-Read-Line", "Memory-Read-

Multiple" and "Memory-Write-Invalid" commands to minimize snoop overhead. In addition, advanced features are supported such as CPU write-back forward to PCI master, and CPU write-back merged with PCI post write buffers to minimize PCI master read latency and DRAM utilization. Delay transaction and read caching mechanisms are also implemented for further improvement of overall system performance.

System Power Management

For sophisticated system power management, the K8M800 supports LDTSTOP# (HyperTransport Bus Stop) protocol to minimize power consumption during suspend system states (S1 and S3). The K8M800 graphics accelerator implements auto clock gating for each engine to achieve power saving, and it moves to standby or suspend states to further reduce power consumption when idle. VESA DPMS (Display Power Management Signaling) CRT power-down is supported. Coupled with the VT8237 South Bridge chip, a complete power conscious PC main board can be implemented with no external TTLs.

3D Graphics Engine

Featuring an integrated 128-bit 3D graphics engine, the K8M800 North Bridge utilizes a highly pipelined architecture that provides high performance along with superior image quality. Several new features enhance the 3D architecture, including two pixel rendering pipes, single-pass multitexturing, bump and cubic mapping, texture compression, edge anti-aliasing, vertex fog and fog table, hardware back-face culling, specular lighting, anisotropic filtering and an 8-bit stencil buffer. The chip also offers the industry's only simultaneous usage of single-pass multitexturing and single-cycle trilinear filtering – enabling stunning image quality without performance loss. Image quality is further enhanced with true 32-bit color rendering throughout the 3D pipeline to produce more vivid and realistic images. The advanced triangle setup engine provides industry leading 3D performance for a realistic user experience in games and other interactive 3D applications.

2D Graphics Engine

The K8M800 North Bridge's advanced 128-bit 2D graphics engine delivers high-speed 2D acceleration for productivity applications. The enhanced 2D architecture with direct access frame buffer capability optimizes UMA performance and provides acceleration of all color depths.

MPEG Video Playback

The K8M800 North Bridge provides the ideal architecture for high quality MPEG-2 based video applications. For MPEG video playback, the integrated video engine offloads the CPU by performing planar-to-packed format conversion and motion video compensation tasks, while its enhanced scaling algorithm delivers incredible full-screen video playback.

Video Capture

The K8M800 North Bridge implements an optional Video Capture Port which supports various video capture standards, including ITU-BT R656, VIP1.1 and VIP2.0 and is compliant with the most common video capture formats: 16 / 32-bit RGB and YUV422. With the integrated video capture feature, the K8M800 can provide high performance video effects for video capturing and playback.

DVI Monitor and TV Output Display Support

The K8M800 provides two AGP-multiplexed "Digital Video Port" interfaces (GDVP0 and GDVP1) plus a dedicated 12-bit digital video port interface (DVP0). Multiplexing display functions with the AGP bus allows the system to support an external AGP connector for future performance upgrades by adding an external AGP graphics controller. It also allows add-in cards to be designed with an AGP-compatible connector for implementation of the display interface logic to reduce cost in the base configuration. In value-system configurations, external AGP upgrade capability is not normally required by the system, allowing all the AGP pins to be used for implementation of very flexible display functions.

AGP-multiplexed digital video port 1 (GDVP1) implements a 12-bit TMDS transmitter interface which is designed to drive a DVI monitor via an external TMDS transmitter chip (such as the VIA VT1632). The dedicated digital video port (DVP0) is normally used for interfacing to a TV encoder (such as the VIA VT1622A or VT1622AM using 3.3V signal levels), however if DVP0 is used for video capture, the AGP-multiplexed GDVP0 digital video port may be configured instead for support of an external TV encoder (VIA VT1623 or VT1623M using low-voltage 1.5V signal levels).

The flexible display configurations of the K8M800 allow support of a flat panel monitor (TMDS / DVI interface), TV display and CRT display at the same time. Internally the K8M800 North Bridge provides two separate display engines, so if two display devices are connected, each can display completely different information at different resolutions, pixel depths and refresh rates. If more than two display devices are connected, the additional displays must have the same resolution, pixel depth, and refresh rate as one of the first two. The maximum display resolutions supported for one display device are listed in the table below. If more than one display is implemented (i.e., if both display engines are functioning at the same time), then available memory bandwidth may limit the display resolutions supported on one or both displays. This will be dependent on many factors including primarily clock rates and memory speeds (contact VIA for additional information).

High Screen Resolution Display Support

Resolutions Supported	Resolution Name	Pixel Depths Supported	System Memory Frame Buffer Size		
			16 MB	32 MB	64 MB
640x480 (4:3)	VGA	8 / 16 / 32	√	√	√
800x600 (4:3)	SVGA	8 / 16 / 32	√	√	√
1024x768 (4:3)	XGA	8 / 16 / 32	√	√	√
1280x1024 (5:4)	SXGA	8 / 16 / 32	√	√	√
1400x1050 (4:3)	SXGA+	8 / 16 / 32	√	√	√
1600x1200 (4:3)	UXGA	8 / 16 / 32	√	√	√
1920x1440 (4:3)	UXGA	8 / 16	√	√	√

Table 1. Supported CRT and Panel Screen Resolutions

PINOUTS

Figure 2. Ball Diagram (Top View) External AGP Interface Enabled

Key	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
A	H SYNC	AB	AG	VCC RGB	VCC PLL2	VCC PLL3	DISP CLKO	GND	VCC HT	VCC HT	G CLK	HT STP#	TCAD 1	TCAD 1#	TCAD 3	TCAD 3#	TCAD 4	TCAD 4#	TCAD 6	TCAD 6#	T CTL	T CTL#	GND	VCC HT	VCC HT	VCC HT
B	V SYNC	VCC DAC	AR	GND RGB	GND PLL2	GND PLL3	GND	GND	VCC HT	VCC HT	HT RST#	TCAD 0	GND	TCAD 2	GND	TCLK 0	GND	TCAD 5	GND	TCAD 7	GND	GND	VCC HT	VCC HT	VCC HT	VCC HT
C	SP DAT2	SP CLK2	GND DAC	RSET	GND PLL1	XIN	GND	GND	VCC HT	VCC HT	VCC HT	TCAD 0#	TCAD 9#	TCAD 2#	TCAD 11#	TCLK 0#	TCAD 12#	TCAD 5#	TCAD 14#	TCAD 7#	GNDA TX	VCCA TX	VCC HT	VCC HT	VCC HT	RT COMP
D	VCC GFX	GP OUT	BIST IN	GND DAC	VCC PLL1	GND	DISP CLKI	GND	VCC HT	VCC HT	VCC HT	GND	TCAD 9	GND	TCAD 11	GND	TCAD 12	GND	TCAD 14	GND	TCAD 15#	VCC HT	VCC HT	VCC HT	RP COMP	RN COMP
E	VCC GFX	VCC GFX	VCC GFX	VCC GFX	GND	GND	INT A#	GND	VCC HT	VCC HT	VCC HT	TCAD 8	TCAD 8#	TCAD 10	TCAD 10#	TCLK 1	TCLK 1#	TCAD 13	TCAD 13#	TCAD 15	VCC HT	VCC HT	VCC HT	VCC HT	VCCA RX	GNDA RX
F	VCC GFX	VCC GFX	VCC GFX	VCC GFX	VCC GFX	VCC GFX	GND	GND	VCC	VCC HT	VCC HT	GND	GND	GND	VCC HT	VCC HT	GND	GND	VCC HT	VCC HT	VCC HT	VCC HT	VCC HT	R CTL	R CTL#	GND
G	GND	VCC GFX	VCC GFX	VCC GFX	VCC GFX	G6	G7	G8	9	10	11	12	13	14	15	16	17	18	G19	G20	VCC HT	VCC HT	RCAD 15#	RCAD 15	GND	RCAD 7#
H	GND	GND	VCC GFX	VCC GFX	VCC GFX	H6		VCC	VCC	VCC	VCC	VCC			VCC	VCC				H	VCC HT	RCAD 14#	GND	RCAD 6	RCAD 6#	RCAD 7
J	DVP0D0 TVD0	GND	GND	VCC GFX	VCC GFX	J		VCC	VCC GFX	VCC HT	VCC HT	VCC HT	VCC HT	VCC HT	VCC HT	VCC HT	VCC HT	GND		J	GND	RCAD 14	RCAD 13#	RCAD 13	GND	RCAD 5#
K	DVP0D4 TVD4	DVP0D1 TVD1	DVP0D2 TVD2	GND	VCC GFX	K		VCC GFX	VCC GFX	GND	GND	GND	GND	GND	GND	GND	GND	VCC HT	VCC	K	VCC HT	RCAD 12#	GND	RCAD 4	RCAD 4#	RCAD 5
L	DVP0D8 TVD8	DVP0D5 TVD5	DVP0D6 TVD6	DVP0D3 TVD3	VCC GFX	L		VCC GFX	VCC GFX	GND	GND	GND	GND	GND	GND	GND	GND	VCC HT	VCC	L	VCC HT	RCAD 12	RCLK 1#	RCLK 1	GND	RCLK 0#
M	DVP0D11 TVD11	DVP0D9 TVD9	DVP0D10 TVD10	DVP0D7 TVD7	VCC GFX	M		VCC AGP	VCC GFX	GND	GND	GND	GND	GND	GND	GND	GND	VCC HT	VCC	M	GND	RCAD 11#	GND	RCAD 3	RCAD 3#	RCLK 0
N	DVP0DE TVDE	GOP0	DVP0VS TVVS	DVP0HS TVHS	VCC GFX	N		VCC AGP	VCC GFX	GND	GND	GND	GND	GND	GND	GND	GND	VCC HT		N	VCC HT	RCAD 11	RCAD 10#	RCAD 10	GND	RCAD 2#
P	SP DAT1	SP CLK1	DVP0CK TVCLK	DVP0DET TVCKR	GND	P		VCC	VCC GFX	GND	GND	GND	GND	GND	GND	GND	GND	VCC HT		P	VCC HT	RCAD 9#	GND	RCAD 1	RCAD 1#	RCAD 2
R	GND	GND	GND	GND	GND	R		VCC	VCC GFX	GND	GND	GND	GND	GND	GND	GND	GND	VCC HT	VCC	R	GND	RCAD 9	RCAD 8#	RCAD 8	GND	RCAD 0#
T	GND QQ	VCC AGP	VCC AGP	VCC AGP	VCC AGP	T		VCC AGP	VCC AGP	GND	GND	GND	GND	GND	GND	GND	GND	VCC HT	VCC	T	VCC HT	VCC HT	VCC HT	VCC HT	VCC HT	RCAD 0
U	VCC QQ	VCC AGP	VCC AGP	VCC AGP	VCC AGP	U		VCC AGP	VCC AGP	GND	GND	GND	GND	GND	GND	GND	GND	VCC HT	VCC	U	VCC HT	VCC HT	VCC HT	VCC HT	VCC HT	VCC HT
V	AGP COMPP	VCC AGP	VCC AGP	VCC AGP	GND	V		VCC AGP	VCC AGP	VCC AGP	VCC AGP	VCC AGP	VCC AGP	VCC AGP	VCC VL	VCC VL	VCC VL	VCC VL	VCC	VCC	VCC HT	VCC HT	VCC HT	VCC HT	VCC HT	VCC HT
W	AGP COMPN	VCC AGP	VCC AGP	VCC AGP	GND	W6			VCC AGP	VCC	VCC	VCC	VCC	VCC	VCC VL	VCC VL	VCC VL	VCC VL	VCC	W	GND	GND	GND	GND	GND	GND
Y	G REQ	AGP8X DT#	VCC AGP	VCC AGP	VCC AGP	Y6														VCC	VCC	VCC	VCC	VCC	VCC	VCC
AA	GST1	GST0	G GNT	VCC AGP	VCC AGP	AA6	7	8	9	10	11	12	13	14	15	16	17	18	19	AA20	VCC	VCC	VCC	VCC	VCC	VCC
AB	GST2	GND	GND	GND	GND	GND	VCC AGP	VCC AGP	GND	GND	VCC AGP	VCC AGP	VCC AGP	VCC AGP	GND	GND	VCC VL	VCC VL	VCC VL	VCC VL	VCC	VCC	VCC	VCC	VCC	VCC
AC	G WBF	GSBA 0#	GSBA 1#	G DBIL	G DBIH	AGP VREF1	GC# BE3	GND	G FRAME	G IRDY	G DEVSEL	G STOP	AGP VREF0	G TRDY	G SERR	G PAR	DE BUG	VCC VL	VCC VL	VCC VL	VCC VL	GND	GND	GND	VCC SUS	TEST IN
AD	GSBA 2#	GSBA 3#	GSBA 5#	GD31	GD27	G RBF	GD25	GD23	GD19	GD16	GC# BE2	GD13	GD10	GD9	GC# BE0	GD5	GD4	GD1	VL PCOMP	VAD 0	VAD 1	DN STB#	DN CMD	VAD 6	RE SET#	SUS ST#
AE	GSBST BS	GND	GSBA 6#	GD30	GND	GD26	GADST B1F	GND	GD22	GD17	GND	GD15	GD11	GND	GADST B0F	GD6	GND	GD2	VAD 4	GND	V BE#	GND	UP STB	VAD 3	GND	PWR OK
AF	GSBST BF	GSBA 4#	GSBA 7#	GD29	GD28	GD24	GADST B1S	GD21	GD20	GD18	GC# BE1	GD14	GD12	GD8	GADST B0S	GD7	GD3	GD0	V PAR	VAD 5	VL VREF	DN STB	UP STB#	VAD 2	VAD 7	UP CMD

Figure 3. Ball Diagram (Top View) – Display Functions Enabled on External AGP

Key	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
A	H SYNC	AB	AG	VCC RGB	VCC PLL2	VCC PLL3	DCLK O	GND	VCC HT	VCC HT	G CLK	HT STP#	TCAD 1	TCAD 1#	TCAD 3	TCAD 3#	TCAD 4	TCAD 4#	TCAD 6	TCAD 6#	T CTL	T CTL#	GND	VCC HT	VCC HT	VCC HT
B	V SYNC	VCC DAC	AR	GND RGB	GND PLL2	GND PLL3	GND	GND	VCC HT	VCC HT	HT RST#	TCAD 0	GND	TCAD 2	GND	TCLK 0	GND	TCAD 5	GND	TCAD 7	GND	GND	VCC HT	VCC HT	VCC HT	VCC HT
C	SP DAT2	SP CLK2	GND DAC	RSET	GND PLL1	XIN	GND	GND	VCC HT	VCC HT	VCC HT	TCAD 0#	TCAD 9#	TCAD 2#	TCAD 11#	TCLK 0#	TCAD 12#	TCAD 5#	TCAD 14#	TCAD 7#	GNDA TX	VCCA TX	VCC HT	VCC HT	VCC HT	RT COMP
D	VCC GFX	GP OUT	BIST IN	GND DAC	VCC PLL1	GND	DCLK I	GND	VCC HT	VCC HT	VCC HT	GND	TCAD 9	GND	TCAD 11	GND	TCAD 12	GND	TCAD 14	GND	TCAD 15#	VCC HT	VCC HT	VCC HT	RP COMP	RN COMP
E	VCC GFX	VCC GFX	VCC GFX	VCC GFX	GND	GND	INT A#	GND	VCC HT	VCC HT	VCC HT	TCAD 8	TCAD 8#	TCAD 10	TCAD 10#	TCLK 1	TCLK 1#	TCAD 13	TCAD 13#	TCAD 15	VCC HT	VCC HT	VCC HT	VCC HT	VCCA RX	GNDA RX
F	VCC GFX	VCC GFX	VCC GFX	VCC GFX	VCC GFX	VCC GFX	GND	GND	VCC	VCC HT	VCC HT	GND	GND	GND	VCC HT	VCC HT	GND	GND	VCC HT	VCC HT	VCC HT	VCC HT	VCC HT	R CTL	R CTL#	GND
G	GND	VCC GFX	VCC GFX	VCC GFX	VCC GFX	G6	G7	G8	9	10	11	12	13	14	15	16	17	18	G19	G20	VCC HT	VCC HT	RCAD 15#	RCAD 15	GND	RCAD 7#
H	GND	GND	VCC GFX	VCC GFX	VCC GFX	H6		VCC	VCC	VCC	VCC	VCC			VCC	VCC				H	VCC HT	RCAD 14#	GND	RCAD 6	RCAD 6#	RCAD 7
J	DVP0D0 TVD0	GND	GND	VCC GFX	VCC GFX	J		VCC	VCC GFX	VCC HT	VCC HT	VCC HT	VCC HT	VCC HT	VCC HT	VCC HT	VCC HT	GND		J	GND	RCAD 14	RCAD 13#	RCAD 13	GND	RCAD 5#
K	DVP0D4 TVD4	DVP0D1 TVD1	DVP0D2 TVD2	GND	VCC GFX	K		VCC GFX	VCC GFX	GND	GND	GND	GND	GND	GND	GND	GND	VCC HT	VCC	K	VCC HT	RCAD 12#	GND	RCAD 4	RCAD 4#	RCAD 5
L	DVP0D8 TVD8	DVP0D5 TVD5	DVP0D6 TVD6	DVP0D3 TVD3	VCC GFX	L		VCC GFX	VCC GFX	GND	GND	GND	GND	GND	GND	GND	GND	VCC HT	VCC	L	VCC HT	RCAD 12	RCLK 1#	RCLK 1	GND	RCLK 0#
M	DVP0D11 TVD11	DVP0D9 TVD9	DVP0D10 TVD10	DVP0D7 TVD7	VCC GFX	M		VCC AGP	VCC GFX	GND	GND	GND	GND	GND	GND	GND	GND	VCC HT	VCC	M	GND	RCAD 11#	GND	RCAD 3	RCAD 3#	RCLK 0
N	DVP0D F	GOP0	DVP0VS TVVS	DVP0HS TVHS	VCC GFX	N		VCC AGP	VCC GFX	GND	GND	GND	GND	GND	GND	GND	GND	VCC HT		N	VCC HT	RCAD 11	RCAD 10#	RCAD 10	GND	RCAD 2#
P	SP DAT1	SP CLK1	DVP0CK TVCLK	DVP0DET TVCKR	GND	P		VCC	VCC GFX	GND	GND	GND	GND	GND	GND	GND	GND	VCC HT		P	VCC HT	RCAD 9#	GND	RCAD 1	RCAD 1#	RCAD 2
R	GND	GND	GND	GND	GND	R		VCC	VCC GFX	GND	GND	GND	GND	GND	GND	GND	GND	VCC HT	VCC	R	GND	RCAD 9	RCAD 8#	RCAD 8	GND	RCAD 0#
T	GND QQ	VCC AGP	VCC AGP	VCC AGP	VCC AGP	T		VCC AGP	VCC AGP	GND	GND	GND	GND	GND	GND	GND	GND	VCC HT	VCC	T	VCC HT	VCC HT	VCC HT	VCC HT	VCC HT	RCAD 0
U	VCC QQ	VCC AGP	VCC AGP	VCC AGP	VCC AGP	U		VCC AGP	VCC AGP	GND	GND	GND	GND	GND	GND	GND	GND	VCC HT	VCC	U	VCC HT	VCC HT	VCC HT	VCC HT	VCC HT	VCC HT
V	AGP COMPP	VCC AGP	VCC AGP	VCC AGP	GND	V		VCC AGP	VCC AGP	VCC AGP	VCC AGP	VCC AGP	VCC AGP	VCC VL	VCC VL	VCC VL	VCC VL	VCC	VCC	V	VCC HT	VCC HT	VCC HT	VCC HT	VCC HT	VCC HT
W	AGP COMPN	VCC AGP	VCC AGP	VCC AGP	GND	W6			VCC AGP	VCC	VCC	VCC	VCC	VCC	VCC VL	VCC VL	VCC VL	VCC VL	VCC	W	GND	GND	GND	GND	GND	GND
Y	DDC CLK	NC	VCC AGP	VCC AGP	VCC AGP	Y6														VCC	VCC	VCC	VCC	VCC	VCC	VCC
AA	ENAVD D	ENAVE E	DDC DAT	VCC AGP	VCC AGP	AA6	7	8	9	10	11	12	13	14	15	16	17	18	19	AA20	VCC	VCC	VCC	VCC	VCC	VCC
AB	ENABL T	GND	GND	GND	GND	GND	VCC AGP	VCC AGP	GND	GND	VCC AGP	VCC AGP	VCC AGP	VCC AGP	GND	GND	VCC VL	VCC VL	VCC VL	VCC VL	VCC	VCC	VCC	VCC	VCC	VCC
AC	GTV CLK#	GDVP1 VS	GDVP1 DE	NC	NC	AGP VREF1	GDVP1 D11	GND	GTV HS	SB CLK	GTV VS	NC	AGP VREF0	NC	NC	NC	DE BUG	VCC VL	VCC VL	VCC VL	VCC VL	GND	GND	GND	VCC SUS	TEST IN
AD	GDVP1 D00	GDVP1 HS	GDVP1 D03	GDVP1 DET	GDVP1 D04	NC	NC	GTVD3	GTV DE	GTVD6	GTV D07	GTV D10	NC	NC	NC	NC	NC	NC	VL PCOMP	VAD 0	VAD 1	DN STB#	DN CMD	VAD 6	RE SET#	SUS ST#
AE	GDVP1 D02	GND	GDVP1 CLK	GDVP1 D08	GND	GDVP1 D10	GTVD0	GND	GTVD1	GTVD5	GND	GTV D09	GTV D11	GND	NC	NC	GND	NC	VAD 4	GND	V BE#	GND	UP STB	VAD 3	GND	PWR OK
AF	GDVP1 D01	GDVP1 D05	GDVP1 CLK#	GDVP1 D06	GDVP1 D07	GDVP1 D09	GTV CLKR	GTV CLK	GTVD2	GTVD4	SB DAT	GTV D08	NC	NC	NC	NC	NC	NC	V PAR	VAD 5	VL VREF	DN STB	UP STB#	VAD 2	VAD 7	UP CMD

Pin Lists

Table 2. Pin List (Listed by Pin Number) – External AGP Interface Enabled

Pin #		Pin Name	Pin #		Pin Name	Pin #		Pin Name	Pin #		Pin Names	Pin #		Pin Name
A01	O	HSYNC	D02	O	GPOUT	L22	I	RCAD12	AC07	IO	GC#BE3	AE18	IO	GD02
A02	AO	AB	D03	I	BISTIN	L23	I	RCLK1#	AC09	IO	GFARME	AE19	IO	VAD4
A03	AO	AG	**D04**	**P**	**GNDDAC**	L24	I	RCLK1	AC10	IO	GIRDY	AE21	IO	VBE#
A04	**P**	**VCCRGB**	**D05**	**P**	**VCCPLL1**	L26	I	RCLK0#	AC11	IO	GDEVSEL	AE23	I	UPSTB
A05	**P**	**VCCPLL2**	D07	I	DISPCLKI	M01	O	DVP0D11 / TVD11	AC12	IO	GSTOP	AE24	IO	VAD3
A06	**P**	**VCCPLL3**	D13	O	TCAD9	M02	O	DVP0D09 / TVD09	**AC13**	**P**	**AGPVREF0**	AE26	I	PWROK
A07	O	DISPCLKO	D15	O	TCAD11	M03	O	DVP0D10 / TVD10 / strap	AC14	IO	GTRDY	AF01	I	GSBSTBF
A11	I	GCLK	D17	O	TCAD12	M04	O	DVP0D07 / TVD07 / strap	AC15	IO	GSERR	AF02	I	GSBA4#
A12	I	HTSTP#	D19	O	TCAD14	M22	I	RCAD11#	AC16	IO	GPAR	AF03	I	GSBA7#
A13	O	TCAD1	D21	O	TCAD15#	M24	I	RCAD3	AC17		DEBUG	AF04	IO	GD29
A14	O	TCAD1#	D25	AI	RPCOMP	M25	I	RCAD3#	**AC25**	**P**	**VCCSUS**	AF05	IO	GD28
A15	O	TCAD3	D26	AI	RNCOMP	M26	I	RCLK0	AC26	I	TESTIN	AF06	IO	GD24
A16	O	TCAD3#	E07	O	INTA#	N01	O	DVP0DE / TVDE	AD01	I	GSBA2#	AF07	IO	GADSTB1S
A17	O	TCAD4	E12	O	TCAD8	N02	O	GPO0	AD02	I	GSBA3#	AF08	IO	GD21
A18	O	TCAD4#	E13	O	TCAD8#	N03	O	DVP0VS / TVVS	AD03	I	GSBA5#	AF09	IO	GD20
A19	O	TCAD6	E14	O	TCAD10	N04	O	DVP0HS / TVHS	AD04	IO	GD31	AF10	IO	GD18
A20	O	TCAD6#	E15	O	TCAD10#	N22	I	RCAD11	AD05	IO	GD27	AF11	IO	GC#BE1
A21	O	TCTL	E16	O	TCLK1	N23	I	RCAD10#	AD06	I	GRBF	AF12	IO	GD14
A22	O	TCTL#	E17	O	TCLK1#	N24	I	RCAD10	AD07	IO	GD25	AF13	IO	GD12
B01	O	VSYNC	E18	O	TCAD13	N26	I	RCAD2#	AD08	IO	GD23	AF14	IO	GD08
B02	**P**	**VCCDAC**	E19	O	TCAD13#	P01	IO	SPDAT1	AD09	IO	GD19	AF15	IO	GADSTB0S
B03	AO	AR	E20	O	TCAD15	P02	IO	SPCLK1	AD10	IO	GD16	AF16	IO	GD07
B04	**P**	**GNDRGB**	**E25**	**P**	**VCCARX**	P03	O	DVP0CLK / TVCLK	AD11	IO	GC#BE2	AF17	IO	GD03
B05	**P**	**GNDPLL2**	**E26**	**P**	**GNDARX**	P04	O	DVP0DET / TVCKR	AD12	IO	GD13	AF18	IO	GD00
B06	**P**	**GNDPLL3**	F24	I	RCTL	P22	I	RCAD9#	AD13	IO	GD10	AF19	IO	VPAR
B11	O	HTRST#	F25	I	RCTL#	P24	I	RCAD1	AD14	IO	GD09	AF20	IO	VAD5
B12	O	TCAD0	G23	I	RCAD15#	P25	I	RCAD1#	AD15	IO	GC#BE0	**AF21**	**P**	**VLVREF**
B14	O	TCAD2	G24	I	RCAD15	P26	I	RCAD2	AD16	IO	GD05	AF22	O	DNSTB
B16	O	TCLK0	G26	I	RCAD7#	R22	I	RCAD9	AD17	IO	GD04	AF23	I	UPSTB#
B18	O	TCAD5	H22	I	RCAD14#	R23	I	RCAD8#	AD18	IO	GD01	AF24	IO	VAD2
B20	O	TCAD7	H24	I	RCAD6	R24	I	RCAD8	AD19	AI	VLPCOMP	AF25	IO	VAD7
C01	IO	SPDAT2	H25	I	RCAD6#	R26	I	RCAD0#	AD20	IO	VAD0	AF26	I	UPCMD
C02	IO	SPCLK2	H26	I	RCAD7	**T01**	**P**	**GNDQQ**	AD21	IO	VAD1			
C03	**P**	**GNDDAC**	J01	O	DVP0D00 / TVD00 / strap	T26	I	RCAD0	AD22	O	DNSTB#			
C04	AI	RSET	J22	I	RCAD14	**U01**	**P**	**VCCQQ**	AD23	O	DNCMD			
C05	**P**	**GNDPLL1**	J23	I	RCAD13#	V01	AI	AGPCOMPP	AD24	IO	VAD6			
C06	I	XIN	J24	I	RCAD13	W01	AI	AGPCOMPN	AD25	I	RESET#			
C12	O	TCAD0#	J26	I	RCAD5#	Y01	I	GREQ	AD26	I	SUSST#			
C13	O	TCAD9#	K01	O	DVP0D04 / TVD04 / strap	Y02	I	AGP8XDT#	AE01	I	GSBSTBS			
C14	O	TCAD2#	K02	O	DVP0D01 / TVD01 / strap	AA01	O	GST1	AE03	I	GSBA6#			
C15	O	TCAD11#	K03	O	DVP0D02 / TVD02 / strap	AA02	O	GST0	AE04	IO	GD30			
C16	O	TCLK0#	K22	I	RCAD12#	AA03	O	GGNT	AE06	IO	GD26			
C17	O	TCAD12#	K24	I	RCAD4	AB01	O	GST2	AE07	IO	GADSTB1F			
C18	O	TCAD5#	K25	I	RCAD4#	AC01	I	GWBF	AE09	IO	GD22			
C19	O	TCAD14#	K26	I	RCAD5	AC02	I	GSBA0#	AE10	IO	GD17			
C20	O	TCAD7#	L01	O	DVP0D08 / TVD08	AC03	I	GSBA1#	AE12	IO	GD15			
C21	**P**	**GNDATX**	L02	O	DVP0D05 / TVD05 / strap	AC04	IO	GDBIL	AE13	IO	GD11			
C22	**P**	**VCCATX**	L03	O	DVP0D06 / TVD06 / strap	AC05	IO	GDBIH / GPIPE#	AE15	IO	GADSTB0F			
C26	AI	RTCOMP	L04	O	DVP0D03 / TVD03 / strap	**AC06**	**P**	**AGPVREF1**	AE16	IO	GD06			

VCCGFX (33 pins): D1, E1-4, F1-6, G2-5, H3-5, J4-5,9, K5,8-9, L5,8-9, M5,9, N5,9, P9, R9

VCCAGP (38 pins): M8, N8, T2-5,8-9, U2-5,8-9, V2-4,8-13, W2-4,9, Y3-5, AA4-5, AB7-8,11-14

VCCVL (16 pins): V14-17, W15-18, AB17-20, AC18-21

VCCHT (79 pins): A9-10,24-26, B9-10,23-26, C9-11,23-25, D9-11,22-24, E9-11,21-24, F10-11,15-16,19-23, G21-22, H21, J10-17, K18,21, L18,21, M18, N18,21, P18,21, R18, T18,21-25, U18,21-26, V21-26

VCC (44 pins): F9, H8-12,15-16, J8, K19, L19, M19, P8, R8,19, T19, U19, V18-19, W10-14,19, Y20-26, AA21-26, AB21-26

GND (149 pins): A8,23, B7-8,13,15,17,19,21-22, C7-8, D6,8,12,14,16,18,20, E5-6,8, F7-8,12-14,17-18,26, G1,25, H1-2,23, J2-3,18,21,25, K4,10-17,23, L10-17,25, M10-17,21,23, N10-17,25, P5,10-17,23, R1-5,10-17,21,25, T10-17, U10-17, V5, W5,21-26, AB2-6,9-10,15-16, AC8,22-24, AE2,5,8,11,14,17,20,22,25

Table 3. Pin List (Listed by Pin Name) - External AGP Interface Enabled

Pin #		Pin Name	Pin #		Pin Name	Pin #		Pin Name	Pin #		Pin Names	Pin #		Pin Name
A02	AO	AB	AD13	IO	GD10	AE01	I	GSBSTBS	AD25	I	RESET#	AF26	I	UPCMD
A03	AO	AG	AE13	IO	GD11	AC15	IO	GSERR	D26	AI	RNCOMP	AE23	I	UPSTB
Y02	I	AGP8XDT#	AF13	IO	GD12	AA02	O	GST0	D25	AI	RPCOMP	AF23	I	UPSTB#
W01	AI	AGPCOMPN	AD12	IO	GD13	AA01	O	GST1	C04	AI	RSET	AD20	IO	VAD0
V01	AI	AGPCOMPP	AF12	IO	GD14	AB01	O	GST2	C26	AI	RTCOMP	AD21	IO	VAD1
AC13	**P**	**AGPVREF0**	AE12	IO	GD15	AC12	IO	GSTOP	P02	IO	SPCLK1	AF24	IO	VAD2
AC06	**P**	**AGPVREF1**	AD10	IO	GD16	AC14	IO	GTRDY	C02	IO	SPCLK2	AE24	IO	VAD3
B03	AO	AR	AE10	IO	GD17	AC01	I	GWBF	P01	IO	SPDAT1	AE19	IO	VAD4
D03	I	BISTIN	AF10	IO	GD18	A01	O	HSYNC	C01	IO	SPDAT2	AF20	IO	VAD5
AC17		DEBUG	AD09	IO	GD19	B11	O	HTRST#	AD26	I	SUSST#	AD24	IO	VAD6
D07	I	DISPCLKI	AF09	IO	GD20	A12	I	HTSTP#	B12	O	TCAD0	AF25	IO	VAD7
A07	O	DISPCLKO	AF08	IO	GD21	E07	O	INTA#	C12	O	TCAD0#	AE21	IO	VBE#
AD23	O	DNCMD	AE09	IO	GD22	AE26	I	PWROK	A13	O	TCAD1	**E25**	**P**	**VCCARX**
AF22	O	DNSTB	AD08	IO	GD23	T26	I	RCAD0	A14	O	TCAD1#	**C22**	**P**	**VCCATX**
AD22	O	DNSTB#	AF06	IO	GD24	R26	I	RCAD0#	B14	O	TCAD2	**B02**	**P**	**VCCDAC**
P03	O	DVP0CLK / TVCLK	AD07	IO	GD25	P24	I	RCAD1	C14	O	TCAD2#	**D05**	**P**	**VCCPLL1**
J01	O	DVP0D00 / TVD00 / strap	AE06	IO	GD26	P25	I	RCAD1#	A15	O	TCAD3	**A05**	**P**	**VCCPLL2**
K02	O	DVP0D01 / TVD01 / strap	AD05	IO	GD27	P26	I	RCAD2	A16	O	TCAD3#	**A06**	**P**	**VCCPLL3**
K03	O	DVP0D02 / TVD02 / strap	AF05	IO	GD28	N26	I	RCAD2#	A17	O	TCAD4	**U01**	**P**	**VCCQQ**
L04	O	DVP0D03 / TVD03 / strap	AF04	IO	GD29	M24	I	RCAD3	A18	O	TCAD4#	**A04**	**P**	**VCCRGB**
K01	O	DVP0D04 / TVD04 / strap	AE04	IO	GD30	M25	I	RCAD3#	B18	O	TCAD5	**AC25**	**P**	**VCCSUS**
L02	O	DVP0D05 / TVD05 / strap	AD04	IO	GD31	K24	I	RCAD4	C18	O	TCAD5#	AD19	AI	VLPCOMP
L03	O	DVP0D06 / TVD06 / strap	AC05	IO	GDBIH / GPIPE#	K25	I	RCAD4#	A19	O	TCAD6	**AF21**	**P**	**VLVREF**
M04	O	DVP0D07 / TVD07 / strap	AC04	IO	GDBIL	K26	I	RCAD5	A20	O	TCAD6#	AF19	IO	VPAR
L01	O	DVP0D08 / TVD08	AC11	IO	GDEVSEL	J26	I	RCAD5#	B20	O	TCAD7	B01	O	VSYNC
M02	O	DVP0D09 / TVD09	AC09	IO	GFARME	H24	I	RCAD6	C20	O	TCAD7#	C06	I	XIN
M03	O	DVP0D10 / TVD10 / strap	AA03	O	GGNT	H25	I	RCAD6#	E12	O	TCAD8			
M01	O	DVP0D11 / TVD11	AC10	IO	GIRDY	H26	I	RCAD7	E13	O	TCAD8#			
N01	O	DVP0DE / TVDE	**E26**	**P**	**GNDARX**	G26	I	RCAD7#	D13	O	TCAD9			
P04	O	DVP0DET / TVCKR	**C21**	**P**	**GNDATX**	R24	I	RCAD8	C13	O	TCAD9#			
N04	O	DVP0HS / TVHS	**C03**	**P**	**GNDDAC**	R23	I	RCAD8#	E14	O	TCAD10			
N03	O	DVP0VS / TVVS	**D04**	**P**	**GNDDAC**	R22	I	RCAD9	E15	O	TCAD10#			
AE15	IO	GADSTB0F	**C05**	**P**	**GNDPLL1**	P22	I	RCAD9#	D15	O	TCAD11			
AF15	IO	GADSTB0S	**B05**	**P**	**GNDPLL2**	N24	I	RCAD10	C15	O	TCAD11#			
AE07	IO	GADSTB1F	**B06**	**P**	**GNDPLL3**	N23	I	RCAD10#	D17	O	TCAD12			
AF07	IO	GADSTB1S	**T01**	**P**	**GNDQQ**	N22	I	RCAD11	C17	O	TCAD12#			
AD15	IO	GC#BE0	**B04**	**P**	**GNDRGB**	M22	I	RCAD11#	E18	O	TCAD13			
AF11	IO	GC#BE1	AC16	IO	GPAR	L22	I	RCAD12	E19	O	TCAD13#			
AD11	IO	GC#BE2	N02	O	GPO0	K22	I	RCAD12#	D19	O	TCAD14			
AC07	IO	GC#BE3	D02	O	GPOUT	J24	I	RCAD13	C19	O	TCAD14#			
A11	I	GCLK	AD06	I	GRBF	J23	I	RCAD13#	E20	O	TCAD15			
AF18	IO	GD00	Y01	I	GREQ	J22	I	RCAD14	D21	O	TCAD15#			
AD18	IO	GD01	AC02	I	GSBA0#	H22	I	RCAD14#	B16	O	TCLK0			
AE18	IO	GD02	AC03	I	GSBA1#	G24	I	RCAD15	C16	O	TCLK0#			
AF17	IO	GD03	AD01	I	GSBA2#	G23	I	RCAD15#	E16	O	TCLK1			
AD17	IO	GD04	AD02	I	GSBA3#	M26	I	RCLK0	E17	O	TCLK1#			
AD16	IO	GD05	AF02	I	GSBA4#	L26	I	RCLK0#	A21	O	TCTL			
AE16	IO	GD06	AD03	I	GSBA5#	L24	I	RCLK1	A22	O	TCTL#			
AF16	IO	GD07	AE03	I	GSBA6#	L23	I	RCLK1#	AC26	I	TESTIN			
AF14	IO	GD08	AF03	I	GSBA7#	F24	I	RCTL						
AD14	IO	GD09	AF01	I	GSBSTBF	F25	I	RCTL#						

VCCGFX (33 pins): D1, E1-4, F1-6, G2-5, H3-5, J4-5,9, K5,8-9, L5,8-9, M5,9, N5,9, P9, R9

VCCAGP (38 pins): M8, N8, T2-5,8-9, U2-5,8-9, V2-4,8-13, W2-4,9, Y3-5, AA4-5, AB7-8,11-14

VCCVL (16 pins): V14-17, W15-18, AB17-20, AC18-21

VCCHT (79 pins): A9-10,24-26, B9-10,23-26, C9-11,23-25, D9-11,22-24, E9-11,21-24, F10-11,15-16,19-23, G21-22, H21, J10-17, K18,21, L18,21, M18, N18,21, P18,21, R18, T18,21-25, U18,21-26, V21-26

VCC (44 pins): F9, H8-12,15-16, J8, K19, L19, M19, P8, R8,19, T19, U19, V18-19, W10-14,19, Y20-26, AA21-26, AB21-26

GND (149 pins): A8,23, B7-8,13,15,17,19,21-22, C7-8, D6,8,12,14,16,18,20, E5-6,8, F7-8,12-14,17-18,26, G1,25, H1-2,23, J2-3,18,21,25, K4,10-17,23, L10-17,25, M10-17,21,23, N10-17,25, P5,10-17,23, R1-5,10-17,21,25, T10-17, U10-17, V5, W5,21-26, AB2-6,9-10,15-16, AC8,22-24, AE2,5,8,11,14,17,20,22,25

Table 4. Pin List (Listed by Pin Number) – Display Functions Enabled on AGP Interface

Pin #		Pin Name	Pin #		Pin Name	Pin #		Pin Name	Pin #		Pin Names
A01	O	HSYNC	**D04**	**P**	**GNDDAC**	M01	O	DVP0D11 / TVD11	AD09	O	GTVDE
A02	AO	AB	**D05**	**P**	**VCCPLL1**	M02	O	DVP0D09 / TVD09	AD10	O	GTVD06
A03	AO	AG	D07	I	DISPCLKI	M03	O	DVP0D10 / TVD10 / strap	AD11	O	GTVD07
A04	**P**	**VCCRGB**	D13	O	TCAD9	M04	O	DVP0D07 / TVD07 / strap	AD12	O	GTVD10
A05	**P**	**VCCPLL2**	D15	O	TCAD11	M22	I	RCAD11#	AD19	AI	VLPCOMP
A06	**P**	**VCCPLL3**	D17	O	TCAD12	M24	I	RCAD3	AD20	IO	VAD0
A07	O	DISPCLKO	D19	O	TCAD14	M25	I	RCAD3#	AD21	IO	VAD1
A11	I	GCLK	D21	O	TCAD15#	M26	I	RCLK0	AD22	O	DNSTB#
A12	I	HTSTP#	D25	AI	RPCOMP	N01	O	DVP0DE / TVDE	AD23	O	DNCMD
A13	O	TCAD1	D26	AI	RNCOMP	N02	O	GPO0	AD24	IO	VAD6
A14	O	TCAD1#	E07	O	INTA#	N03	O	DVP0VS / TVVS	AD25	I	RESET#
A15	O	TCAD3	E12	O	TCAD8	N04	O	DVP0HS / TVHS	AD26	I	SUSST#
A16	O	TCAD3#	E13	O	TCAD8#	N22	I	RCAD11	AE01	O	GDVP1D02
A17	O	TCAD4	E14	O	TCAD10	N23	I	RCAD10#	AE03	O	GDVP1CLK
A18	O	TCAD4#	E15	O	TCAD10#	N24	I	RCAD10	AE04	O	GDVP1D08
A19	O	TCAD6	E16	O	TCLK1	N26	I	RCAD2#	AE06	O	GDVP1D10
A20	O	TCAD6#	E17	O	TCLK1#	P01	IO	SPDAT1	AE07	O	GTVD00
A21	O	TCTL	E18	O	TCAD13	P02	IO	SPCLK1	AE09	O	GTVD01
A22	O	TCTL#	E19	O	TCAD13#	P03	O	DVP0CLK / TVCLK	AE10	O	GTVD05
B01	O	VSYNC	E20	O	TCAD15	P04	O	DVP0DET / TVCKR	AE12	O	GTVD08
B02	**P**	**VCCDAC**	**E25**	**P**	**VCCARX**	P22	I	RCAD9#	AE13	O	GTVD11
B03	AO	AR	**E26**	**P**	**GNDARX**	P24	I	RCAD1	AE19	IO	VAD4
B04	**P**	**GNDRGB**	F24	I	RCTL	P25	I	RCAD1#	AE21	IO	VBE#
B05	**P**	**GNDPLL2**	F25	I	RCTL#	P26	I	RCAD2	AE23	I	UPSTB
B06	**P**	**GNDPLL3**	G23	I	RCAD15#	R22	I	RCAD9	AE24	IO	VAD3
B11	O	HTRST#	G24	I	RCAD15	R23	I	RCAD8#	AE26	I	PWROK
B12	O	TCAD0	G26	I	RCAD7#	R24	I	RCAD8	AF01	O	GDVP1D01
B14	O	TCAD2	H22	I	RCAD14#	R26	I	RCAD0#	AF02	O	GDVP1D05
B16	O	TCLK0	H24	I	RCAD6	**T01**	**P**	**GNDQQ**	AF03	O	GDVP1CLK#
B18	O	TCAD5	H25	I	RCAD6#	T26	I	RCAD0	AF04	O	GDVP1D06
B20	O	TCAD7	H26	I	RCAD7	**U01**	**P**	**VCCQQ**	AF05	O	GDVP1D07
C01	IO	SPDAT2	J01	O	DVP0D00 / TVD00 / strap	V01	AI	AGPCOMPP	AF06	O	GDVP1D09
C02	IO	SPCLK2	J22	I	RCAD14	W01	AI	AGPCOMPN	AF07	I	GTVCLKR
C03	**P**	**GNDDAC**	J23	I	RCAD13#	Y02	I	AGP8XDT#	AF08	O	GTVCLK
C04	AI	RSET	J24	I	RCAD13	AC01	O	GTVCLK#	AF09	O	GTVD02
C05	**P**	**GNDPLL1**	J26	I	RCAD5#	AC02	O	GDVP1VS	AF10	O	GTVD04
C06	I	XIN	K01	O	DVP0D04 / TVD04 / strap	AC03	O	GDVP1DE	AF12	O	GTVD09
C12	O	TCAD0#	K02	O	DVP0D01 / TVD01 / strap	**AC06**	**P**	**AGPVREF1**	AF19	IO	VPAR
C13	O	TCAD9#	K03	O	DVP0D02 / TVD02 / strap	AC07	O	GDVP1D11	AF20	IO	VAD5
C14	O	TCAD2#	K22	I	RCAD12#	AC09	O	GTVHS	**AF21**	**P**	**VLVREF**
C15	O	TCAD11#	K24	I	RCAD4	AC11	O	GTVVS	AF22	O	DNSTB
C16	O	TCLK0#	K25	I	RCAD4#	**AC13**	**P**	**AGPVREF0**	AF23	I	UPSTB#
C17	O	TCAD12#	K26	I	RCAD5	AC17		DEBUG	AF24	IO	VAD2
C18	O	TCAD5#	L01	O	DVP0D08 / TVD08	**AC25**	**P**	**VCCSUS**	AF25	IO	VAD7
C19	O	TCAD14#	L02	O	DVP0D05 / TVD05 / strap	AC26	I	TESTIN	AF26	I	UPCMD
C20	O	TCAD7#	L03	O	DVP0D06 / TVD06 / strap	AD01	O	GDVP1D00			
C21	**P**	**GNDATX**	L04	O	DVP0D03 / TVD03 / strap	AD02	O	GDVP1HS			
C22	**P**	**VCCATX**	L22	I	RCAD12	AD03	O	GDVP1D03			
C26	AI	RTCOMP	L23	I	RCLK1#	AD04	I	GDVP1DET			
D02	O	GPOUT	L24	I	RCLK1	AD05	O	GDVP1D04			
D03	I	BISTIN	L26	I	RCLK0#	AD08	O	GTVD03			

VCCGFX (33 pins): D1, E1-4, F1-6, G2-5, H3-5, J4-5,9, K5,8-9, L5,8-9, M5,9, N5,9, P9, R9

VCCAGP (38 pins): M8, N8, T2-5,8-9, U2-5,8-9, V2-4,8-13, W2-4,9, Y3-5, AA4-5, AB7-8,11-14

VCCVL (16 pins): V14-17, W15-18, AB17-20, AC18-21

VCCHT (79 pins): A9-10,24-26, B9-10,23-26, C9-11,23-25, D9-11,22-24, E9-11,21-24, F10-11,15-16,19-23, G21-22, H21, J10-17, K18,21, L18,21, M18, N18,21, P18,21, R18, T18,21-25, U18,21-26, V21-26

VCC (44 pins): F9, H8-12,15-16, J8, K19, L19, M19, P8, R8,19, T19, U19, V18-19, W10-14,19, Y20-26, AA21-26, AB21-26

GND (149 pins): A8,23, B7-8,13,15,17,19,21-22, C7-8, D6,8,12,14,16,18,20, E5-6,8, F7-8,12-14,17-18,26, G1,25, H1-2,23, J2-3,18,21,25, K4,10-17,23, L10-17,25, M10-17,21,23, N10-17,25, P5,10-17,23, R1-5,10-17,21,25, T10-17, U10-17, V5, W5,21-26, AB2-6,9-10,15-16, AC8,22-24, AE2,5,8,11,14,17,20,22,25

Table 5. Pin List (Listed by Pin Name) - Display Functions Enabled on AGP Interface

Pin #		Pin Name	Pin #		Pin Name	Pin #		Pin Name	Pin #		Pin Names
A02	AO	AB	**E26**	**P**	**GNDARX**	R23	I	RCAD8#	E14	O	TCAD10
A03	AO	AG	**C21**	**P**	**GNDATX**	R22	I	RCAD9	E15	O	TCAD10#
Y02	I	AGP8XDT#	**C03**	**P**	**GNDDAC**	P22	I	RCAD9#	D15	O	TCAD11
W01	AI	AGPCOMPN	**D04**	**P**	**GNDDAC**	N24	I	RCAD10	C15	O	TCAD11#
V01	AI	AGPCOMPP	**C05**	**P**	**GNDPLL1**	N23	I	RCAD10#	D17	O	TCAD12
AC13	**P**	**AGPVREF0**	**B05**	**P**	**GNDPLL2**	N22	I	RCAD11	C17	O	TCAD12#
AC06	**P**	**AGPVREF1**	**B06**	**P**	**GNDPLL3**	M22	I	RCAD11#	E18	O	TCAD13
B03	AO	AR	**T01**	**P**	**GNDQQ**	L22	I	RCAD12	E19	O	TCAD13#
D03	I	BISTIN	**B04**	**P**	**GNDRGB**	K22	I	RCAD12#	D19	O	TCAD14
AC17		DEBUG	N02	O	GPO0	J24	I	RCAD13	C19	O	TCAD14#
D07	I	DISPCLKI	D02	O	GPOUT	J23	I	RCAD13#	E20	O	TCAD15
A07	O	DISPCLKO	AC01	O	GTVCLK#	J22	I	RCAD14	D21	O	TCAD15#
AD23	O	DNCMD	AF08	O	GTVCLK	H22	I	RCAD14#	B16	O	TCLK0
AF22	O	DNSTB	AF07	I	GTVCLKR	G24	I	RCAD15	C16	O	TCLK0#
AD22	O	DNSTB#	AE07	O	GTVD00	G23	I	RCAD15#	E16	O	TCLK1
P03	O	DVP0CLK / TVCLK	AE09	O	GTVD01	M26	I	RCLK0	E17	O	TCLK1#
J01	O	DVP0D00 / TVD00 / strap	AF09	O	GTVD02	L26	I	RCLK0#	A21	O	TCTL
K02	O	DVP0D01 / TVD01 / strap	AD08	O	GTVD03	L24	I	RCLK1	A22	O	TCTL#
K03	O	DVP0D02 / TVD02 / strap	AF10	O	GTVD04	L23	I	RCLK1#	AC26	I	TESTIN
L04	O	DVP0D03 / TVD03 / strap	AE10	O	GTVD05	F24	I	RCTL	AF26	I	UPCMD
K01	O	DVP0D04 / TVD04 / strap	AD10	O	GTVD06	F25	I	RCTL#	AE23	I	UPSTB
L02	O	DVP0D05 / TVD05 / strap	AD11	O	GTVD07	AD25	I	RESET#	AF23	I	UPSTB#
L03	O	DVP0D06 / TVD06 / strap	AE12	O	GTVD08	D26	AI	RNCOMP	AD20	IO	VAD0
M04	O	DVP0D07 / TVD07 / strap	AF12	O	GTVD09	D25	AI	RPCOMP	AD21	IO	VAD1
L01	O	DVP0D08 / TVD08	AD12	O	GTVD10	C04	AI	RSET	AF24	IO	VAD2
M02	O	DVP0D09 / TVD09	AE13	O	GTVD11	C26	AI	RTCOMP	AE24	IO	VAD3
M03	O	DVP0D10 / TVD10 / strap	AD09	O	GTVDE	P02	IO	SPCLK1	AE19	IO	VAD4
M01	O	DVP0D11 / TVD11	AC09	O	GTVHS	C02	IO	SPCLK2	AF20	IO	VAD5
N01	O	DVP0DE / TVDE	AC11	O	GTVVS	P01	IO	SPDAT1	AD24	IO	VAD6
P04	O	DVP0DET / TVCKR	A01	O	HSYNC	C01	IO	SPDAT2	AF25	IO	VAD7
N04	O	DVP0HS / TVHS	B11	O	HTRST#	AD26	I	SUSST#	AE21	IO	VBE#
N03	O	DVP0VS / TVVS	A12	I	HTSTP#	B12	O	TCAD0	**E25**	**P**	**VCCARX**
A11	I	GCLK	E07	O	INTA#	C12	O	TCAD0#	**C22**	**P**	**VCCATX**
AF03	O	GDVP1CLK#	AE26	I	PWROK	A13	O	TCAD1	**B02**	**P**	**VCCDAC**
AE03	O	GDVP1CLK	T26	I	RCAD0	A14	O	TCAD1#	**D05**	**P**	**VCCPLL1**
AD01	O	GDVP1D00	R26	I	RCAD0#	B14	O	TCAD2	**A05**	**P**	**VCCPLL2**
AF01	O	GDVP1D01	P24	I	RCAD1	C14	O	TCAD2#	**A06**	**P**	**VCCPLL3**
AE01	O	GDVP1D02	P25	I	RCAD1#	A15	O	TCAD3	**U01**	**P**	**VCCQQ**
AD03	O	GDVP1D03	P26	I	RCAD2	A16	O	TCAD3#	**A04**	**P**	**VCCRGB**
AD05	O	GDVP1D04	N26	I	RCAD2#	A17	O	TCAD4	**AC25**	**P**	**VCCSUS**
AF02	O	GDVP1D05	M24	I	RCAD3	A18	O	TCAD4#	AD19	AI	VLPCOMP
AF04	O	GDVP1D06	M25	I	RCAD3#	B18	O	TCAD5	**AF21**	**P**	**VLVREF**
AF05	O	GDVP1D07	K24	I	RCAD4	C18	O	TCAD5#	AF19	IO	VPAR
AE04	O	GDVP1D08	K25	I	RCAD4#	A19	O	TCAD6	B01	O	VSYNC
AF06	O	GDVP1D09	K26	I	RCAD5	A20	O	TCAD6#	C06	I	XIN
AE06	O	GDVP1D10	J26	I	RCAD5#	B20	O	TCAD7			
AC07	O	GDVP1D11	H24	I	RCAD6	C20	O	TCAD7#			
AC03	O	GDVP1DE	H25	I	RCAD6#	E12	O	TCAD8			
AD04	I	GDVP1DET	H26	I	RCAD7	E13	O	TCAD8#			
AD02	O	GDVP1HS	G26	I	RCAD7#	D13	O	TCAD9			
AC02	O	GDVP1VS	R24	I	RCAD8	C13	O	TCAD9#			

VCCGFX (33 pins): D1, E1-4, F1-6, G2-5, H3-5, J4-5,9, K5,8-9, L5,8-9, M5,9, N5,9, P9, R9

VCCAGP (38 pins): M8, N8, T2-5,8-9, U2-5,8-9, V2-4,8-13, W2-4,9, Y3-5, AA4-5, AB7-8,11-14

VCCVL (16 pins): V14-17, W15-18, AB17-20, AC18-21

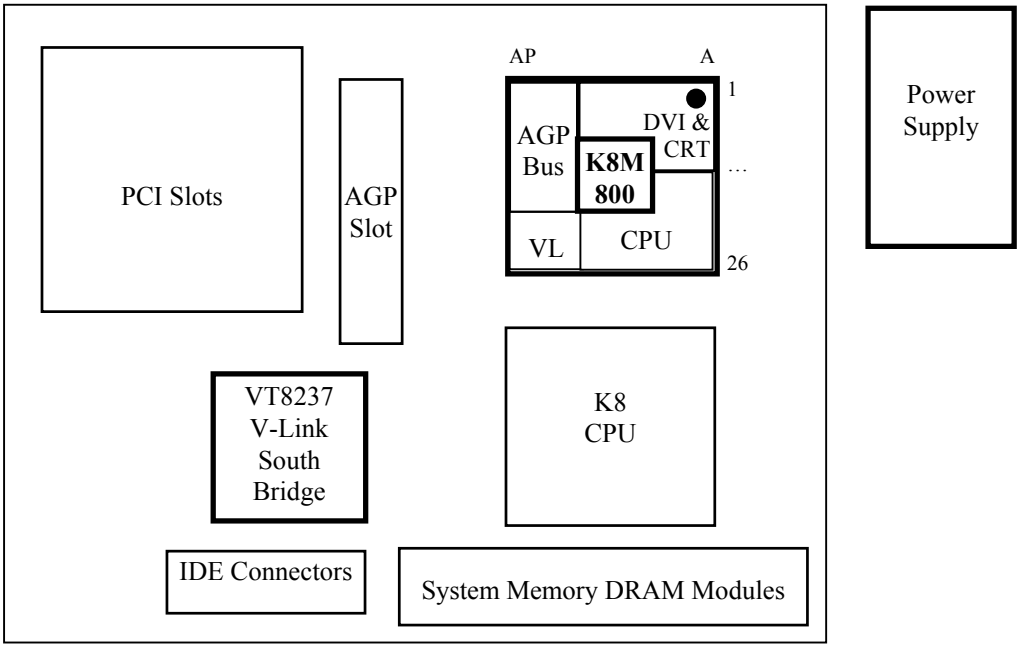
VCCHT (79 pins): A9-10,24-26, B9-10,23-26, C9-11,23-25, D9-11,22-24, E9-11,21-24, F10-11,15-16,19-23, G21-22, H21, J10-17, K18,21, L18,21, M18, N18,21, P18,21, R18, T18,21-25, U18,21-26, V21-26

VCC (44 pins): F9, H8-12,15-16, J8, K19, L19, M19, P8, R8,19, T19, U19, V18-19, W10-14,19, Y20-26, AA21-26, AB21-26

GND (149 pins): A8,23, B7-8,13,15,17,19,21-22, C7-8, D6,8,12,14,16,18,20, E5-6,8, F7-8,12-14,17-18,26, G1,25, H1-2,23, J2-3,18,21,25, K4,10-17,23, L10-17,25, M10-17,21,23, N10-17,25, P5,10-17,23, R1-5,10-17,21,25, T10-17, U10-17, V5, W5,21-26, AB2-6,9-10,15-16, AC8,22-24, AE2,5,8,11,14,17,20,22,25

Pin Arrangement

Pinouts for the K8M800 North Bridge chip were defined assuming the ATX PCB layout model shown below (and general pin layout shown) as a guide for PCB component placement. Other PCB layouts (AT, LPX and NLX) were also considered and can typically follow the same general component placement. If desired by the PCB layout engineer, for better routing, the North Bridge chip can be oriented 45 degrees clockwise rotated from the position shown below.



Pin Descriptions

CPU Interface Pin Descriptions

Signal Name	Pin #	I/O	Signal Description
"HyperTransport" Transmit Interface			
TCAD15 / TCAD15#	E20, D21	O	**Transmit Differential Control / Address / Data Pair 15.**
TCAD14 / TCAD14#	D19, C19	O	**Transmit Differential Control / Address / Data Pair 14.**
TCAD13 / TCAD13#	E18, E19	O	**Transmit Differential Control / Address / Data Pair 13.**
TCAD12 / TCAD12#	D17, C17	O	**Transmit Differential Control / Address / Data Pair 12.**
TCAD11 / TCAD11#	D15, C15	O	**Transmit Differential Control / Address / Data Pair 11.**
TCAD10 / TCAD10#	E14, E15	O	**Transmit Differential Control / Address / Data Pair 10.**
TCAD9 / TCAD9#	D13, C13	O	**Transmit Differential Control / Address / Data Pair 9.**
TCAD8 / TCAD8#	E12, E13	O	**Transmit Differential Control / Address / Data Pair 8.**
TCAD7 / TCAD7#	B20, C20	O	**Transmit Differential Control / Address / Data Pair 7.**
TCAD6 / TCAD6#	A19, A20	O	**Transmit Differential Control / Address / Data Pair 6.**
TCAD5 / TCAD5#	B18, C18	O	**Transmit Differential Control / Address / Data Pair 5.**
TCAD4 / TCAD4#	A17, A18	O	**Transmit Differential Control / Address / Data Pair 4.**
TCAD3 / TCAD3#	A15, A16	O	**Transmit Differential Control / Address / Data Pair 3.**
TCAD2 / TCAD2#	B14, C14	O	**Transmit Differential Control / Address / Data Pair 2.**
TCAD1 / TCAD1#	A13, A14	O	**Transmit Differential Control / Address / Data Pair 1.**
TCAD0 / TCAD0#	B12, C12	O	**Transmit Differential Control / Address / Data Pair 0.**
TCLK0 / TCLK0#	B16, C16	O	**Transmit Differential Clock Pair 0.** Clock for TCAD 0-7.
TCLK1 / TCLK1#	E16, E17	O	**Transmit Differential Clock Pair 1.** Clock for TCAD 8-15.
TCTL / TCTL#	A21, A22	O	**Transmit Differential Control.**
"HyperTransport" Receive Interface			
RCAD15 / RCAD15#	G24, G23	I	**Receive Differential Control / Address / Data Pair 15.**
RCAD14 / RCAD14#	J22, H22	I	**Receive Differential Control / Address / Data Pair 14.**
RCAD13 / RCAD13#	J24, J23	I	**Receive Differential Control / Address / Data Pair 13.**
RCAD12 / RCAD12#	L22, K22	I	**Receive Differential Control / Address / Data Pair 12.**
RCAD11 / RCAD11#	N22, M22	I	**Receive Differential Control / Address / Data Pair 11.**
RCAD10 / RCAD10#	N24, N23	I	**Receive Differential Control / Address / Data Pair 10.**
RCAD9 / RCAD9#	R22, P22	I	**Receive Differential Control / Address / Data Pair 9.**
RCAD8 / RCAD8#	R24, R23	I	**Receive Differential Control / Address / Data Pair 8.**
RCAD7 / RCAD7#	H26, G26	I	**Receive Differential Control / Address / Data Pair 7.**
RCAD6 / RCAD6#	H24, H25	I	**Receive Differential Control / Address / Data Pair 6.**
RCAD5 / RCAD5#	K26, J26	I	**Receive Differential Control / Address / Data Pair 5.**
RCAD4 / RCAD4#	K24, K25	I	**Receive Differential Control / Address / Data Pair 4.**
RCAD3 / RCAD3#	M24, M25	I	**Receive Differential Control / Address / Data Pair 3.**
RCAD2 / RCAD2#	P26, N26	I	**Receive Differential Control / Address / Data Pair 2.**
RCAD1 / RCAD1#	P24, P25	I	**Receive Differential Control / Address / Data Pair 1.**
RCAD0 / RCAD0#	T26, R26	I	**Receive Differential Control / Address / Data Pair 0.**
RCLK0 / RCLK0#	M26, L26	I	**Receive Differential Clock Pair 0.** Clock for RCAD 0-7.
RCLK1 / RCLK1#	L24, L23	I	**Receive Differential Clock Pair 1.** Clock for RCAD 8-15.
RCTL / RCTL#	F24, F25	I	**Receive Differential Control.**
"HyperTransport" Control			
HTRST#	B11	O	**HyperTransport Reset.** Connect to RESET# pin of K8 CPU. 1.5V swing. Active when the RESET# input is active.
HTSTP#	A12	I	**HyperTransport Stop.** Connect to South Bridge DPSLP# pin.

"Transmit" pins should be connected to the K8 CPU "In" pins. "Receive" pins should be connected to the K8 CPU "Out" pins. See the HyperTransport specs and the specs for the K8 CPU models to be supported for additional information.

Accelerated Graphics Port Interface Pin Descriptions

AGP Bus Interface

Signal Name	Pin #	I/O	Signal Description
GD[31:0]	(see pin list)	IO	**Address / Data Bus.** Address is driven with GDS assertion for AGP-style transfers and with GFRAME# assertion for PCI-style transfers.
GC#BE[3:0] (GCBE[3:0]# for 4x mode)	AC7 AD11 AF11 AD15	IO	**Command / Byte Enable.** (Interpreted as GC/BE# for AGP 2x/4x and GC#/BE for 8x). For AGP cycles these pins provide command information (different commands than for PCI) driven by the master (graphics controller) when requests are being enqueued using GPIPE# (2x/4x only as GPIPE# isn't used in 8x mode). These pins provide valid byte information during AGP write transactions and are driven by the master. The target (this chip) drives these lines to "0000" during the return of AGP read data. For PCI cycles, commands are driven with GFRAME# assertion. Byte enables corresponding to supplied or requested data are driven on following clocks.
GPAR	AC16	IO	**AGP Parity.** A single parity bit is provided over GD[31:0] and GC#BE[3:0].
GDBIH / GPIPE# **GDBIL**	AC5 AC4	IO	**Dynamic Bus Inversion High / Low.** AGP 8x transfer mode only. Driven by the source to indicate whether the corresponding data bit group (GDBIH for GD[31:16] and GDBIL for GD[15:0]) needs to be inverted on the receiving end (1 on GDBIx indicates that the corresponding data bit group should be inverted). Used to limit the number of simultaneously switching outputs to 8 for each 16-pin group. **Pipelined Request.** Not used by AGP 8x. Asserted by the master (external graphics controller) to indicate that a full-width request is to be enqueued by the target (North Bridge). The master enqueues one request each rising edge of GCLK while GPIPE# is asserted. When GPIPE# is deasserted no new requests are enqueued across the AD bus. **Note**: See RxAE[1] for GPIPE# / GDBIH pin function selection.
GADSTB0F (GADSTB0 for 4x), **GADSTB0S** (GADSTB0# for 4x)	AE15 AF15	IO	**Bus Strobe 0.** Source synchronous strobes for GD[15:0] (the agent that is providing the data drives these signals). For 8x transfer mode, GADSTB0 is interpreted as GADSTB0F ("First" strobe) and GADSTB0# as GADSTB0S ("Second" strobe). GADSTB0 and GADSTB0# provide timing for 4x mode.
GADSTB1F (GADSTB1 for 4x), **GADSTB1S** (GADSTB1# for 4x)	AE7 AF7	IO	**Bus Strobe 1.** Source synchronous strobes for GD[31:16] (i.e., the agent that is providing the data drives these signals). For 8x transfer mode, GADSTB1 is interpreted as GADSTB1F ("First" strobe) and GADSTB1# as GADSTB1S ("Second" strobe). GADSTB1 and GADSTB1# provide timing for 4x transfer mode.
GFRAME (GFRAME# for 4x)	AC9	IO	**Frame.** Assertion indicates the address phase of a PCI transfer. Negation indicates that one more data transfer is desired by the cycle initiator. Interpreted as active high for 8x.
GIRDY (GIRDY# for 4x)	AC10	IO	**Initiator Ready.** (Interpreted as active low for PCI/AGP2x/4x and high for AGP 8x). For AGP write cycles, the assertion of this pin indicates that the master is ready to provide *all* write data for the current transaction. Once this pin is asserted, the master is not allowed to insert wait states. For AGP read cycles, the assertion of this pin indicates that the master is ready to transfer a subsequent block of read data. The master is *never* allowed to insert a wait state during the initial block of a read transaction. However, it may insert wait states after each block transfers. For PCI cycles, asserted when the initiator is ready for data transfer.
GTRDY (GTRDY# for 4x)	AC14	IO	**Target Ready.** (Interpreted as active low for PCI/AGP2x/4x and high for AGP 8x). For AGP cycles, indicates that the target is ready to provide read data for the entire transaction (when the transaction can complete within four clocks) or is ready to transfer a (initial or subsequent) block of data when the transfer requires more than four clocks to complete. The target is allowed to insert wait states after each block transfer for both read and write transactions. For PCI cycles, asserted when the target is ready for data transfer.
GDEVSEL (GDEVSEL# for 4x mode)	AC11	IO	**Device Select (PCI transactions only).** This signal is driven by the North Bridge when a PCI initiator is attempting to access main memory. It is an input when the chip is acting as PCI initiator. Not used for AGP cycles. Interpreted as active high for AGP 8x.

AGP Bus Interface (continued)			
Signal Name	**Pin #**	**I/O**	**Signal Description**
GSTOP (GSTOP# for 4x)	AC12	IO	**Stop (PCI transactions only).** Asserted by the target to request the master to stop the current transaction. Interpreted as active high for AGP 8x.
AGP8XDT#	Y2	I	**AGP 8x Transfer Mode Detect.** Low indicates that the external graphics card can support 8x transfer mode
GRBF (GRBF# for 4x)	AD6	I	**Read Buffer Full.** Indicates if the master (graphics controller) is ready to accept previously requested low priority read data. When GRBF# is asserted, the North Bridge will not return low priority read data to the graphics controller.
GWBF (GWBF# for 4x)	AC1	I	**Write Buffer Full.**
GSBA[7:0]# (GSBA[7:0] for 4x)	(see pin list)	I	**Side Band Address.** Provides an additional bus to pass address and command information from the master (graphics controller) to the target (North Bridge). These pins are ignored until enabled.
GSBSTBF (GSBSTB for 4x), **GSBSTBS** (GSBSTB# for 4x)	AF1 AE1	I	**Side Band Strobe.** Driven by the master to provide timing for GSBA[7:0]. 8x mode uses GSBSTBF ("First" strobe) and GSBSTBS ("Second" strobe). These signals are interpreted as GSBSTB & GSBSTB# for AGP4x.
GST[2:0]	AB1 AA1 AA2	O	**Status (AGP only).** Provides information from the arbiter to a master to indicate what it may do. Only valid while GGNT# is asserted. 000 Indicates that previously requested low priority read or flush data is being returned to the master (graphics controller). 001 Indicates that previously requested high priority read data is being returned to the master. 010 Indicates that the master is to provide low priority write data for a previously enqueued write command. 011 Indicates that the master is to provide high priority write data for a previously enqueued write command. 100 Reserved. (arbiter must not issue, may be defined in the future). 101 Reserved. (arbiter must not issue, may be defined in the future). 110 Reserved. (arbiter must not issue, may be defined in the future). 111 Indicates that the master (graphics controller) has been given permission to start a bus transaction. The master may enqueue AGP requests by asserting PIPE# or start a PCI transaction by asserting GFRAME#. GST[2:0] are always outputs from the target (North Bridge logic) and inputs to the master (graphics controller).
GREQ (GREQ# for 4x)	Y1	I	**Request.** Master (graphics controller) request for use of the AGP bus.
GGNT (GGNT# for 4x)	AA3	O	**Grant.** Permission is given to the master (graphics controller) to use the AGP bus.
GSERR (GSERR# for 4x)	AC15	IO	**AGP System Error.**

Note: Separate system interrupts are not provided for AGP. The AGP connector provides interrupts via PCI bus INTA-B#.

Note: A separate reset is not required for the AGP bus (RESET# resets both PCI and AGP buses)

Note: Two mechanisms are provided by the AGP bus to enqueue master requests: GPIPE# (to send addresses multiplexed on the AD lines) and the SBA port (to send addresses unmultiplexed). AGP masters implement one or the other or select one at initialization time (they are not allowed to change during runtime). Only one of the two will be used; the signals associated with the other will not be used. GRBF# has an internal pullup to maintain it in the de-asserted state in case it is not implemented on the master device. AGP 8x mode allows only SBA (GPIPE# isn't used in 8x mode).

Note: AGP 8x signal levels are 0V and 0.8V. AGP 8x mode maintains most signals at a low level when inactive resulting in no current flow.

V-Link Interface Pin Descriptions

V-Link Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
VAD7, **VAD6,** **VAD5**, **VAD4**, **VAD3**, **VAD2**, **VAD1**, **VAD0**	AF25 AD24 AF20 AE19 AE24 AF24 AD21 AD20	IO IO IO IO IO IO IO IO	**Address / Data Bus.** Also used to pass strap information from the South Bridge to the North Bridge (the actual straps are on the indicated South Bridge pin and that information is passed to the North Bridge at reset time via the VAD pins).
VPAR	AF19	IO	**Parity.**
VBE#	AE21	IO	**Byte Enable.**
UPCMD	AF26	I	**Command from Client (South Bridge) to Host (North Bridge).**
UPSTB	AE23	I	**Strobe from Client to Host.**
UPSTB#	AF23	I	**Complement Strobe from Client to Host.**
DNCMD	AD23	O	**Command from Host (North Bridge) to Client (South Bridge).**
DNSTB	AF22	O	**Strobe from Host to Client.**
DNSTB#	AD22	O	**Complement Strobe from Host to Client.**

CRT and Serial Bus Pin Interface Pin Descriptions

CRT Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
AR	B3	AO	**Analog Red.** Red output to CRT monitor.
AG	A3	AO	**Analog Green.** Green output to CRT monitor.
AB	A2	AO	**Analog Blue.** Blue output to CRT monitor.
RSET	C4	AI	**CRT Output Reference Resistor.** Tie to GNDRGB through an external 90.9 Ω ± 1% resistor to control the "RGB" RAMDAC full-scale current.
HSYNC	A1	O	**Horizontal Sync.** Digital output to CRT monitor.
VSYNC	B1	O	**Vertical Sync.** Digital output to CRT monitor.

Integrated Graphics SMBus Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
SPCLK[2:1]	C2, P2	IO	**Serial Port (SMB/I2C) Clocks.** Clocks for serial data transfer. SPCLK1 is typically used for I^2C communications. SPCLK2 is typically used for CRT Display DDC communications.
SPDAT[2:1]	C1, P1	IO	**Serial Port (SMB/I2C) Data.** Data signals for serial data transfer. SPDAT1 is typically used for I^2C communications. SPDAT2 is typically used for CRT Display DDC communications.

Dedicated Digital Video Port 0 (DVP0) Pin Descriptions

The DVP0 dedicated Digital Video Port can be configured as either a TV Encoder interface port or a Video Capture input port, selectable via strap pins DVP0D[6:5] (see the TV Encoder Interface and Video Capture Interface pin descriptions for details).

Dedicated Digital Video Port 0 (DVP0)			
Signal Name	**Pin #**	**I/O**	**Signal Description**
DVP0D11 / TVD11 / CAPD11, **DVP0D10** / TVD10 / CAPD10 / strap, **DVP0D9** / TVD9 / CAPD9 / strap, **DVP0D8** / TVD8 / CAPD8 / strap, **DVP0D7** / TVD7 / CAPD7 / strap, **DVP0D6** / TVD6 / CAPD6 / strap, **DVP0D5** / TVD5 / CAPD5 / strap, **DVP0D4** / TVD4 / CAPD4 / strap, **DVP0D3** / TVD3 / CAPD3 / strap, **DVP0D2** / TVD2 / CAPD2 / strap, **DVP0D1** / TVD1 / CAPD1 / strap, **DVP0D0** / TVD0 / CAPD0 / strap	M1 M3 M2 L1 M4 L3 L2 K1 L4 K3 K2 J1	O	**Digital Video Port 0 Data.** Default output drive is 8 mA. 16 mA may be selected via SR3D[6]=1. NOTE: DVP0D[6:0] are also used for power-up reset straps for the embedded graphics controller. Check the Strap Pin table for details.
DVP0HS / TVHS / CAPHS	N4	O	**Digital Video Port 0 Horizontal Sync.** Internally pulled down.
DVP0VS / TVVS / CAPVS	N3	O	**Digital Video Port 0 Vertical Sync.** Internally pulled down.
DVP0DE / TVDE	N1	O	**Digital Video Port 0 Data Enable.** Internally pulled down.
DVP0DET / TVCLKR / CAPBCLK	P4	I	**Digital Video Port 0 Display Detect.** If VGA register 3C5.12[5]=0, 3C5.1A[5] will read 1 if display is connected. Tie to GND if not used.
DVP0CLK / TVCLK / CAPACLK	P3	O	**Digital Video Port 0 Clock.** Internally pulled down.

The terminology "3C5.nn" above refers to the VGA "Sequencer" registers at I/O port 3C5 index "nn"

Dedicated Digital Video Port 0 (DVP0) - TV Encoder Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
TVD11 / DVP0D11 / CAPD11, **TVD10** / DVP0D10 / CAPD10 / strap, **TVD9** / DVP0D9 / CAPD9 / strap, **TVD8** / DVP0D8 / CAPD8 / strap, **TVD7** / DVP0D7 / CAPD7 / strap, **TVD6** / DVP0D6 / CAPD6 / strap, **TVD5** / DVP0D5 / CAPD5 / strap, **TVD4** / DVP0D4 / CAPD4 / strap, **TVD3** / DVP0D3 / CAPD3 / strap, **TVD2** / DVP0D2 / CAPD2 / strap, **TVD1** / DVP0D1 / CAPD1 / strap, **TVD0** / DVP0D0 / CAPD0 / strap	M1 M3 M2 L1 M4 L3 L2 K1 L4 K3 K2 J1	O	**TV Encoder 0 Data.** To configure DVP0 as a TV Out interface port, pins DVP0D[6:5] must be strapped high. Note: One TV Encoder interface is supported through either DVP0 or GDVP1.
TVHS / DVP0HS / CAPHS	N4	O	**TV Encoder 0 Horizontal Sync.** Internally pulled down.
TVVS / DVP0VS / CAPVS	N3	O	**TV Encoder 0 Vertical Sync.** Internally pulled down.
TVDE / DVP0DE	N1	O	**TV Encoder 0 Display Enable.** Internally pulled down.
TVCLKR / DVP0DET / CAPBCLK	P4	I	**TV Encoder 0 Clock Return.** Input from TV encoder. Internally pulled down.
TVCLK / DVP0CLK / CAPACLK	P3	O	**TV Encoder 0 Clock Out.** Output to TV encoder. Internally pulled down.

The above pins may be connected to an external TV Encoder chip such as a VIA VT1622A or VT1622AM for driving a TV set.
I/O pads for the pins on this page are powered by VCCGFX (3.3V I/O).

Dedicated Digital Video Port 0 (DVP0) CCIR601 / CCIR656 / VIP1.1 / VIP2.0 Video Capture Port (VCP)			
Signal Name	**Pin #**	**I/O**	**Signal Description**
		I	**Video Capture Data.** To configure DVP0 as a video capture port, pin DVP0D6 must be strapped low. Pin Function: 8-Bit Mode 16-Bit Mode
CAPD15 / GPO0	N5		CAPBD7 CAPAD15
CAPD14 / GPOUT	D2		CAPBD6 CAPAD14
CAPD13 / SPDAT1	P1		CAPBD5 CAPAD13
CAPD12 / SPCLK1,	P2		CAPBD4 CAPAD12
CAPD11 / DVP0D11 / TVD11,	M1		CAPBD3 CAPAD11
CAPD10 / DVP0D10 / TVD10 / strap,	M3		CAPBD2 CAPAD10
CAPD9 / DVP0D9 / TVD9 / strap,	M2		CAPBD1 CAPAD9
CAPD8 / DVP0D8 / TVD8 / strap,	L1		CAPBD0 CAPAD8
CAPD7 / DVP0D7 / TVD7 / strap,	M4		CAPAD7 CAPAD7
CAPD6 / DVP0D6 / TVD6 / strap,	L3		CAPAD6 CAPAD6
CAPD5 / DVP0D5 / TVD5 / strap,	L2		CAPAD5 CAPAD5
CAPD4 / DVP0D4 / TVD4 / strap,	K1		CAPAD4 CAPAD4
CAPD3 / DVP0D3 / TVD3 / strap,	L4		CAPAD3 CAPAD3
CAPD2 / DVP0D2 / TVD2 / strap,	K3		CAPAD2 CAPAD2
CAPD1 / DVP0D1 / TVD1 / strap,	K2		CAPAD1 CAPAD1
CAPD0 / DVP0D0 / TVD0 / strap	J1		CAPAD0 CAPAD0
CAPHS / DVP0HS / TVHS	N4	I	**Video Capture Horizontal Sync.** For capture port "A" (16-bit and 8-bit mode). Internally pulled down.
CAPVS / DVP0VS / TVVS	N3	I	**Video Capture Vertical Sync.** For capture port "A" (16-bit and 8-bit mode). Internally pulled down.
CAPAFLD / BISTIN	N1	I	**Video Capture "A"-Channel TV Field Indicator.** For capture port "A" (16-bit and 8-bit mode).
CAPBCLK / DVP0DET / TVCLKR	P4	I	**Video Capture Clock B.** Port "B" (8-bit mode) input clock from external video decoder. Internally pulled down. Not used in 16-bit mode.
CAPACLK / DVP0CLK / TVCLK	P3	I	**Video Capture Clock A.** Port "A" (16-bit and 8-bit mode) input clock from external video decoder. Internally pulled down.

Note: I/O pads for the pins on this page are powered by VCCGFX (3.3V I/O).

AGP-Multiplexed Digital Video Port 0 (GDVP0) Pin Descriptions

The GDVP0 Digital Video Port is supported through multiplexing its interface signal pins with AGP pins. It is used as a TV Encoder interface port.

AGP-Multiplexed Digital Video Port 0 (GDVP0) - TV Encoder Interface				
Signal Name	**AGP Name**	**Pin #**	**I/O**	**Signal Description**
GTVD11, **GTVD10,** **GTVD9,** **GTVD8,** **GTVD7,** **GTVD6,** **GTVD5,** **GTVD4,** **GTVD3,** **GTVD2,** **GTVD1,** **GTVD0**	GD11 GD13 GD14 GD15 GC#BE2 GD16 GD17 GD18 GD23 GD20 GD22 GADSTB1F	AE13 AD12 AF12 AE12 AD11 AD10 AE10 AF10 AD08 AF09 AE09 AE07	O	**TV Encoder Data.** 3C5.12[5:4] must be set to 00. The K8M800 North Bridge supports one TV Encoder interface through either GDVP0 or DVP0.
GTVHS	GFRAME	AC09	O	**TV Encoder Horizontal Sync.**
GTVVS	GDEVSEL	AC11	O	**TV Encoder Vertical Sync.**
GTVDE	GD19	AD09	O	**TV Encoder Data Enable.**
GTVCLKR	GADSTB1S	AF07	I	**TV Encoder Clock Return.** Input from TV encoder. Internal pull down.
GTVCLK	GD21	AF08	O	**TV Encoder Clock Out.** Output to TV encoder. Internally pulled down.
GTVCLK#	GWBF	AC01	O	**TV Encoder Clock Out Complement.** Output to TV encoder. Internally pulled down.

AGP-Multiplexed Digital Video Port 1 (GDVP1) Pin Descriptions

The GDVP1 Digital Video Port is supported through multiplexing its interface signal pins with AGP pins. It is used as a TMDS Transmitter interface port.

AGP-Multiplexed Digital Video Port 1 (GDVP1) – TMDS Interface				
Signal Name	**AGP Name**	**Pin #**	**I/O**	**Signal Description**
GDVP1D11, **GDVP1D10**, **GDVP1D9**, **GDVP1D8**, **GDVP1D7**, **GDVP1D6**, **GDVP1D5**, **GDVP1D4**, **GDVP1D3**, **GDVP1D2**, **GDVP1D1**, **GDVP1D0**,	GC#BE3 GD26 GD24 GD30 GD28 GD29 GSBA4# GD27 GSBA5# GSBSTBS GSBSTBF GSBA2#	AC07 AE06 AF06 AE04 AF05 AF04 AF02 AD05 AD03 AE01 AF01 AD01	O	**Data.** 3C5.3E[0] must be set to 1.
GDVP1HS	GSBA3#	AD02	O	**Horizontal Sync.**
GDVP1VS	GSBA0#	AC02	O	**Vertical Sync.**
GDVP1DE	GSBA1#	AC03	O	**Data Enable.**
GDVP1DET	GD31	AD04	I	**Display Detect.** If VGA register 3C5.3E[0] = 1, 3C5.1A[4] will read 1 if a display is connected. Tie to GND if not used.
GDVP1CLK	GSBA6#	AE03	O	**Clock.**
GDVP1CLK#	GSBA7#	AF03	O	**Clock Complement.**

I/O pads for all pins on this page are powered by VCC15AGP (1.5V I/O).

Clock, Reset, Power Control, General Purpose I/O, Interrupts and Test Pin Descriptions

Clock, Reset, Power Control, General Purpose I/O, Interrupts and Test			
Signal Name	**Pin #**	**I/O**	**Signal Description**
GCLK	A11	I	**AGP Clock.** 66 MHz clock for AGP logic.
DISPCLKI	D7	I	**Dot Clock (Pixel Clock) In.** Used for external EMI reduction circuit if used. Connect to GND if external EMI reduction circuit not implemented.
DISPCLKO	A7	O	**Dot Clock (Pixel Clock) Out.** Used for external EMI reduction circuit if used. NC if external EMI reduction circuit not implemented.
RESET#	AD25	I	**Reset.** Input from the South Bridge chip. 3.3V tolerant input. When asserted, this signal resets the chip and sets all register bits to the default value. The rising edge of this signal is used to sample all power-up strap options In addition, HTRST# is driven active to reset the K8 CPU.
PWROK	AE26	I	**Power OK.** Driven by South Bridge PWROK output from the power supply PWRGOOD input to the South Bridge.
SUSST#	AD26	I	**Suspend Status.** For implementation of the Suspend-to-DRAM feature. Connect to an external pull-up to disable.
TESTIN	AC26	I	**Test In.** This pin is used for testing and must be left unconnected or tied high (4.7K Ω to 2.5V) on all board designs.
BISTIN	D3	I	**Built-In-Self-Test In.** Reserved for test. Connect to GND for normal operation.
DEBUG	AC17	I	**Debug.** Reserved for test. Connect to ground for normal operation.
XIN	C6	I	**Reference Frequency In.** 14.31818 MHz.
INTA#	E7	O	**PCI Interrupt Output A.** Connect to the South Bridge.
GPOUT	D2	O	**General Purpose Output.**
GOP0	N2	O	**General Purpose Output.**

Integrated Graphics Power and Ground			
Signal Name	**Pin #**	**I/O**	**Signal Description**
VCCDAC	B2	P	**DAC Voltage.** 3.3V ±5% connected via ferrite bead for isolation of digital switching noise.
GNDDAC	C3, D4	P	**DAC Ground.** Connect to main ground plane.
VCCRGB	A4	P	**Power for CRT RGB Outputs.** 3.3V ±5% connected via ferrite bead for isolation of digital switching noise.
GNDRGB	B4	P	**Connection point for RGB Load Resistors.** Connect to main ground plane via ferrite bead for isolation of digital switching noise.
VCCPLL1	D5	P	**Power for Graphics Controller PLL1 ("E-Clock").** 1.5V ±5% connected via ferrite bead for isolation of digital switching noise.
GNDPLL1	C5	P	**Ground for Graphics Controller PLL1 ("E-Clock").** Connect to main ground plane via ferrite bead for isolation of digital switching noise.
VCCPLL2	A5	P	**Power for Graphics Controller PLL2 ("D-Clock").** 1.5V ±5% connected via ferrite bead for isolation of digital switching noise.
GNDPLL2	B5	P	**Ground for Graphics Controller PLL2 ("D-Clock").** Connect to main ground plane via ferrite bead for isolation of digital switching noise.
VCCPLL3	A6	P	**Power for Graphics Controller PLL3 ("LCD Clock").** 1.5V ±5% connected via ferrite bead for isolation of digital switching noise.
GNDPLL3	B6	P	**Ground for Graphics Controller PLL3 ("LCD Clock").** Connect to main ground plane via ferrite bead for isolation of digital switching noise.

Reference Voltage and Compensation Pin Descriptions

Reference Voltages			
Signal Name	**Pin #**	**I/O**	**Signal Description**
VLVREF	AF21	P	**V-Link Voltage Reference.** 0.625V ±2% derived using a resistive voltage divider (3K Ω to 2.5V and 1K Ω to ground). See Design Guide for details.
AGPVREF	AC6, AC13	P	**AGP Voltage Reference.** 0.5 VCCQQ (0.75V) for AGP 2.0 (4x transfer mode) and 0.23 VCCQQ (0.35V) for AGP 3.0 (8x transfer mode). See the Design Guide for additional information and circuit implementation details..

Compensation			
Signal Name	**Pin #**	**I/O**	**Signal Description**
RPCOMP	D25	AI	**Host CPU P-Channel Compensation.** Connect 50 Ω 1% resistor to GND.
RNCOMP	D26	AI	**Host CPU N-Channel Compensation.** Connect 50 Ω 1% resistor to VCCHT.
RTCOMP	C26	AI	**Host CPU Compensation.** Connect 100 Ω 1% resistor to VCCHT.
VLPCOMP	AD19	AI	**Vlink P-Channel Compensation.** Connect 360 Ω 1% resistor to ground.
AGPCOMPN	W1	AI	**AGP N-Channel Compensation.** Connect 60.4 Ω 1% resistor to VCCAGP.
AGPCOMPP	V1	AI	**AGP P-Channel Compensation.** Connect 60.4 Ω 1% resistor to GND.

Power Pin Descriptions

Analog Power / Ground			
Signal Name	**Pin #**	**I/O**	**Signal Description**
VCCATX	C22	P	**Analog Power for HT Transmit.** 3.3V ±5%. Connect through a ferrite bead for isolation of digital switching noise.
GNDATX	C21	P	**Analog Ground for HT Transmit.** Connect to main ground plane through a ferrite bead for isolation of digital switching noise.
VCCARX	E25	P	**Analog Power for HT Receive.** 3.3V ±5%. Connect through a ferrite bead for isolation of digital switching noise.
GNDARX	E26	P	**Analog Ground for HT Receive.** Connect to main ground plane through a ferrite bead for isolation of digital switching noise.

Digital Power / Ground			
Signal Name	**Pin #**	**I/O**	**Signal Description**
VCCHT	(see pin lists)	P	**Power** for **HyperTransport I/O Interface Logic.** Voltage is HT Interface dependent (typically 1.2V).
VCCVL	(see pin lists)	P	**Power** for **V-Link I/O Interface Logic.** 1.5V ±5%
VCCGFX	(see pin lists)	P	**Power** for **Graphics I/O Interface Logic.** 3.3V ±5%
VCCAGP	(see pin lists)	P	**Power** for **AGP Bus I/O Interface Logic.** 1.5V ±5%
VCCQQ	U1	P	**AGP Quiet Power.** 1.5V ±5%. Connect to VCCAGP (see Design Guide)
GNDQQ	T1	P	**AGP Quiet Ground.** Connect to main ground plane.
VCCSUS	AC25	P	**Suspend Power.** 1.5V ±5%. Used to sustain the on-chip 256-byte SRAM.
VCC	(see pin lists)	P	**Power** for **All Other Internal Logic.** 1.5V ±5%
GND	(see pin lists)	P	**Digital Ground.** Connect to main ground plane.

Strap Pin Descriptions

Strap Pins (External pullup / pulldown straps are required to select "H" / "L")				
Signal	**Actual Strap Pin**	**Function**	**Description**	**Status Bit**
DVP0D[10,7]	DVP0D[10,7]	-reserved-	Pull down for normal operation	-
DVP0D[6]	DVP0D[6]	DP0 Port Enable	L: Disable H: Enable	3C5.12[6]
DVP0D[5]	DVP0D[5]	DP0 Port Configuration	L: Display H: TV out	3C5.12[5]
DVP0D[4]	DVP0D[4]	FP Port Configuration	L: 2x 12-bit FP interface H: 24-bit FP interface	3C5.12[4]
DVP0D[3:0]	DVP0D[3:0]	OEM Panel Type	Reserved for customer configuration	3C5.12[3:0]
VAD7	**VT8235-CD:** SDCS3# **VT8235-CE:** SDCS3# **VT8237:** PDCS3#	Test Mode	L: Disable H: Enable Pull down for normal operation. VAD7 is sampled during system initialization; The actual strapping pin is located on the South Bridge chip.	-
VAD6	**VT8235-CD:** SDA2 **VT8235-CE:** SDA2 **VT8237:** PDA2	Auto-Configure	L: Disable H: Enable VAD6 is sampled during system initialization; The actual strapping pin is located on the South Bridge chip.	-
VAD5	**VT8235-CD:** SDA1 **VT8235-CE:** SDA1 **VT8237:** PDA1	External Loop Test Mode	L: Disable H: Enable Pull down for normal operation. VAD5 is sampled during system initialization; The actual strapping pin is located on the South Bridge chip.	-
VAD[4:3]	**VT8235-CD:** SDA0, SA19 **VT8235-CE:** SDA0, Strap_VAD3 **VT8237:** PDA0, GPIOD	HT Transmit PLL Feed Back Delay	Check Design Guide for details. VAD[4:3] are sampled during system initialization; The actual strapping pin is located on the South Bridge chip.	-
VAD2	**VT8235-CD:** SA18 **VT8235-CE:** Strap_VAD2 **VT8237:** GPIOB	HT Bus Width	L: 8-bit H: 16-bit Pull down for normal operation. VAD2 is sampled during system initialization; The actual strapping pin is located on the South Bridge chip.	-
VAD[1:0]	**VT8235-CD:** SA17, SA16 **VT8235-CE:** Strap_VAD[1:0] **VT8237:** GPIOA, GPIOC	HT Bus Frequency	LL: 200MHz HL: 600MHz LH: 400Mhz HH: 800MHz Pull down for normal operation. VAD[1:0] are sampled during system initialization; The actual strapping pin is located on the South Bridge chip.	-

REGISTERS

Register Overview

The following tables summarize the configuration and I/O registers of the K8M800 North Bridge. These tables also document the power-on default value ("Default") and access type ("Acc") for each register. Access type definitions used are RW (Read/Write), RO (Read/Only), "—" for reserved / used (essentially the same as RO), RWC (or just WC) (Read / Write 1's to Clear individual bits) and W1 (Write Once then Read / Only after that). Registers indicated as RW may have some read/only bits that always read back a fixed value (usually 0 if unused); registers designated as RWC or WC may have some read-only or read write bits (see individual register descriptions following these tables for details). All offset and default values are shown in hexadecimal unless otherwise indicated.

The graphics registers are described in a separate document.

Table 6. Registers

I/O Ports

Port #	I/O Port	Default	Acc
22	PCI / AGP Arbiter Disable	00	RW
CFB-8	Configuration Address	0000 0000	RW
CFF-C	Configuration Data	0000 0000	RW

Device 0 Function 0 Registers – AGP & HyperTransport

Header Registers

Offset	Configuration Space Header	Default	Acc
1-0	Vendor ID	**1106**	RO
3-2	Device ID	**0204**	RO
5-4	Command	**0006**	**RW**
7-6	Status	**0210**	**WC**
8	Revision ID	**0n**	RO
9	Program Interface	00	RO
A	Sub Class Code	00	RO
B	Base Class Code	**06**	RO
C	-reserved-	00	—
D	Latency Timer	00	**RW**
E	Header Type	00	RO
F	Built In Self Test (BIST)	00	RO
13-10	Graphics Aperture Base Address	**0000 0008**	**RW**
14-2B	-reserved-	00	—
2D-2C	Subsystem Vendor ID	0000	**W1**
2F-2E	Subsystem ID	0000	**W1**
30-33	-reserved-	00	—
37-34	Capability Pointer	**0000 0080**	RO
38-3F	-reserved-	00	—

Device-Specific Registers

Offset	AGP Drive Control	Default	Acc
40	AGP Compensation Control / Status	**8x**	RW
41	AGP Output Drive Strength	**63**	RW
42	AGP Pad Drive & Delay Control	00	RW
43	AGP Strobe Drive Strength	**63**	RW
44-49	-reserved-	00	—
4A	AGP Hardware Support 1	**1F**	RW
4B	AGP Hardware Support 2	**C4**	RW
4C	-reserved-	00	—
4D	AGP Capability Header Control	**04**	RW
4E	-reserved-	00	—
4F	Multiple Function Control	00	RW

Offset	AGP Power Management Control	Default	Acc
50	Power Management Capability	**01**	**RO**
51	Power Management Next Pointer	00	**RO**
52	Power Management Capabilities I	02	**RO**
53	Power Management Capabilities II	00	**RO**
54	Power Management Control/Status	00	RW
55	Power Management Status	00	**RO**
56	PCI-to-PCI Bridge Support Extension	00	**RO**
57	Power Management Data	00	**RO**
58-5F	-reserved-	00	—

Device-Specific Registers

Offset	K8 Processor Control	Default	Acc
63-60	HT Link Command Device A	**0060 5808**	RW
67-64	HT Link Config / Control Device A	**??11 0020**	**WC**
6B-68	HT Subordinate Link Status	**0000 00D0**	**RO**
6F-6C	HT Link A Frequency Capablity	**0035 0022**	RW
73-70	HT Link B Frequency Capablity	**0035 0022**	RW
77-74	HT Link Enumeration Scratchpad	0000 0000	RW
78-7F	-reserved-	00	—

Offset	AGP 3.x Control	Default	Acc
83-80	AGP 3.x Capabilities	**0030 C002**	**RO**
87-84	AGP 3.x Status	**1F00 0A03**	**RO**
8B-88	AGP 3.x Command	**1F00 0000**	RW
8F-8C	-reserved-	0000 0000	—
93-90	AGP 3.x GART / TLB Control	0000 0000	RW
97-94	AGP 2.0/3.x Graphics Aperture Size	**0001 0F00**	RW
9B-98	AGP 2.0/3.x GART Table Base	0000 0000	RW
9C-9F	-reserved-	00	—

Offset	Reserved	Default	Acc
A0-AF	-reserved-	00	—
B0-B7	-reserved-	00	—

Offset	AGP Miscellaneous Control	Default	Acc
B8	AGP Pad Power Down	00	RW
B9	AGP Mixed Control	00	RW
BA	Isoch Read GPRI Counter	00	RW
BB	Isoch Write GPRI Counter	00	RW
BC	AGP Control	00	RW
BD	AGP Miscellaneous Control 1	**02**	RW
BE	AGP Miscellaneous Control 2	00	RW
BF	AGP 3.x Control	00	RW

Offset	AGP Duty Control	Default	Acc
C0	AGP Duty Control 1	00	RW
C1	AGP Duty Control 2	00	RW

Offset	Reserved	Default	Acc
C2-CF	-reserved-	00	—
D0-DF	-reserved-	00	—
E0-EF	-reserved-	00	—
F0-FF	-reserved-	00	—

Device 0 Function 1 Registers – Error Reporting

Header Registers

Offset	Configuration Space Header	Default	Acc
1-0	Vendor ID	**1106**	RO
3-2	Device ID	**1204**	RO
5-4	Command	**0006**	**RW**
7-6	Status	**0200**	**WC**
8	Revision ID	**0n**	RO
9	Program Interface	00	RO
A	Sub Class Code	00	RO
B	Base Class Code	**06**	RO
C	-reserved-	00	—
D	Latency Timer	00	**RW**
E	Header Type	00	RO
F	Built In Self Test (BIST)	00	RO
10-3F	-reserved-	00	—

Device-Specific Registers

Offset	V-Link Error Control	Default	Acc
40-4F	-reserved-	00	—
50	NB Vlink Bus Error Status	00	**WC**
51-57	-reserved-	00	—
58	NB Vlink Bus Err Reporting Enable	00	RW
59-5F	-reserved-	00	—

Offset	Reserved	Default	Acc
60-CF	-reserved-	00	—

Offset	AGP Error Control	Default	Acc
D0-DF	-reserved-	00	—
E0	AGP Error Status	00	**WC**
E1	AGP Isochronous Error Status	00	**RO**
E2-E7	-reserved-	00	—
E8	AGP Error Reporting Enable	00	RW
E9-FF	-reserved-	00	—

Device 0 Function 2 Registers – Host CPU

Header Registers

Offset	Configuration Space Header	Default	Acc
1-0	Vendor ID	**1106**	RO
3-2	Device ID	**2204**	RO
5-4	Command	**0006**	**RW**
7-6	Status	**0200**	**WC**
8	Revision ID	**0n**	RO
9	Program Interface	00	RO
A	Sub Class Code	00	RO
B	Base Class Code	**06**	RO
C	-reserved-	00	—
D	Latency Timer	00	**RW**
E	Header Type	00	RO
F	Built In Self Test (BIST)	00	RO
10-3F	-reserved-	00	—

Device-Specific Registers

Offset	Host CPU Control	Default	Acc
40-9F	-reserved-	00	—

Offset	K8 Host CPU Control	Default	Acc
A0	CPU Control 1	00	RW
A1	CPU Control 2	00	RW
A2	RAM Base Address	00	RW
A3	HyperTransport Init Value 1	**B1**	RW
A4	HyperTransport Init Value 2	**30**	RW
A5	Arbitration Control 1	**08**	RW
A6	Arbitration Control 2	00	RW
A7	HyperTransport Control 1	**86**	RW
A8	HyperTransport Control 2	**7F**	RW
A9	HyperTransport Control 3	**CF**	RW
AA	Transmit Data Drive Control	**22**	RW
AB	Transmit Clock Drive Control	**22**	RW
AC	Transmit Autocomp Result	00	RW
AD	HT Controller Misc Control	00	RW
AE	Rcvr Termination Value Control	**22**	RW
AF	Rcvr Termination Autocomp Status	00	RW
B0	Response Flow Control Buffer Depth	**84**	RW
B1	Receive Post-Write Buffer Depth	15	RW
B2	TPM Control	00	RW
B3	-reserved-	00	—
B4	AGP Master Isoc Request Timer	**03**	RW
B5	PCI Master Timer	00	RW
B6	AGP Master Timer	00	RW
B7	AGP Master Iso Req Hi Priority Timr	00	RW
B8-BF	-reserved-	00	—
C0	HT Transmit CAD[7:0],Ctrl R/F Dela	00	RW
C1	HT Transmit Clock0 Rise / Fall Delay	00	RW
C2	HT Transmit CAD[15:8] R/F Delay	00	RW
C3	HT Transmit Clock1 Rise / Fall Delay	00	RW
C4	HT Rcv CAD[7:0],Ctl,Clk0 R/FDelay	00	RW
C5	HT Rcv CAD[15:8], Clk1 R/F Delay	00	RW
C6-FF	-reserved-	00	—

Device 0 Function 3 Registers – DRAM

Header Registers

Offset	Configuration Space Header	Default	Acc
1-0	Vendor ID	**1106**	RO
3-2	Device ID	**3204**	RO
5-4	Command	**0006**	**RW**
7-6	Status	**0200**	**WC**
8	Revision ID	**0n**	RO
9	Program Interface	00	RO
A	Sub Class Code	00	RO
B	Base Class Code	**06**	RO
C	-reserved-	00	—
D	Latency Timer	00	**RW**
E	Header Type	00	RO
F	Built In Self Test (BIST)	00	RO
10-3F	-reserved-	00	—

Device-Specific Registers

Offset	DRAM Control	Default	Acc
40-46	-reserved-	00	—
47	DRAM End Address	**01**	RW
48-6F	-reserved-	00	—

Offset	Timer Control	Default	Acc
70	PCI Timer	00	RW
71	AGP Timer	00	RW
72	VGA Timer	00	RW
73	High Priority Display Timer	00	RW
74	Low Priority Display Timer	00	RW
75-7F	-reserved-	00	—

Offset	ROM Shadow	Default	Acc
80	ROM Shadow Control C0000-CFFFF	00	RW
81	ROM Shadow Control D0000-DFFFF	00	RW
82	ROM Shadow Control E0000-FFFFF	00	RW
83	-reserved-	00	—

Offset	SMM / APIC Control	Default	Acc
84-85	-reserved-	00	—
86	SMM / APIC Decoding	**01**	RW
87-9F	-reserved-	00	—

Offset	UMA Registers	Default	Acc
A0	CPU Direct Access FB Base Addr	00	RW
A1	CPU Direct Access FB Size	00	RW
A2	VGA Timer	00	RW
A3	Reserved (Do Not Program)	00	RW
A4	FIFO / Flow Control 1	00	RW
A5	FIFO / Flow Control 2	**20**	RW
A7-A6	Reserved (Do Not Program)	0000	RW
A8-FF	-reserved-	00	—

Device 0 Function 4 Registers – Power Management

Header Registers

Offset	Configuration Space Header	Default	Acc
1-0	Vendor ID	**1106**	RO
3-2	Device ID	**4204**	RO
5-4	Command	**0006**	**RW**
7-6	Status	**0200**	**WC**
8	Revision ID	**0n**	RO
9	Program Interface	00	RO
A	Sub Class Code	00	RO
B	Base Class Code	**06**	RO
C	-reserved-	00	—
D	Latency Timer	00	**RW**
E	Header Type	00	RO
F	Built In Self Test (BIST)	00	RO
10-3F	-reserved-	00	—

Device-Specific Registers

Offset	Reserved	Default	Acc
40-4F	-reserved-	00	—
50-5F	-reserved-	00	—
60-6F	-reserved-	00	—
70-7F	-reserved-	00	—
80-8F	-reserved-	00	—
90-9F	-reserved-	00	—

Offset	Power Management Control	Default	Acc
A0	Power Management Mode	00	RW
A1	-reserved-	00	—
A2	Dynamic Clock Stop	00	RW
A3-AF	-reserved-	00	—

Above registers A0-A3 were previously BC-BF

Offset	Reserved	Default	Acc
B0-BF	-reserved-	00	—
C0-CF	-reserved-	00	—

Offset	BIOS Scratch	Default	Acc
D0-EF	BIOS Scratch Registers	00	RW

Registers D0-EF above are same as former F3-F4

Offset	Test	Default	Acc
F0-FF	Reserved (Do Not Program)	00	RW

Device 0 Function 7 Registers – V-Link / PCI

Header Registers

Offset	Configuration Space Header	Default	Acc
1-0	Vendor ID	**1106**	RO
3-2	Device ID	**7204**	RO
5-4	Command	**0006**	**RW**
7-6	Status	**0200**	**WC**
8	Revision ID	**0n**	RO
9	Program Interface	00	RO
A	Sub Class Code	00	RO
B	Base Class Code	**06**	RO
C	-reserved-	00	—
D	Latency Timer	00	**RW**
E	Header Type	00	RO
F	Built In Self Test (BIST)	00	RO
10-3F	-reserved-	00	—

Device-Specific Registers

Offset	V-Link Control	Default	Acc
40	V-Link Revision ID	00	**RO**
41	V-Link NB Capability	**19**	**WC**
42	V-Link NB Downlink Command	**88**	RW
43	V-Link NB Uplink Max Req Depth	**80**	**RO**
44	V-Link NB Uplink Buffer Size	**82**	**RO**
45	V-Link NB Bus Timer	**44**	RW
46	V-Link NB Misc Control	00	RW
47	V-Link Control	00	RW
48	V-Link NB/SB Configuration	**18**	RW
49	V-Link SB Capability	**19**	**RO**
4A	V-Link SB Downlink Status	**88**	**RO**
4B	V-Link SB Uplink Max Req Depth	**80**	RW
4C	V-Link SB Uplink Buffer Size	**82**	RW
4D	V-Link SB Bus Timer	**44**	RW
4E	CCA Master High Priority	00	RW
4F	V-Link SB Miscellaneous Control	00	RW

Device-Specific Registers (continued)

Offset	Reserved	Default	Acc
50-5F	-reserved-	00	—
60-6F	-reserved-	00	—

Offset	PCI Bus Control	Default	Acc
70	PCI Buffer Control	00	RW
71	CPU to PCI Flow Control	**48**	**WC**
72	-reserved-	00	—
73	PCI Master Control	00	RW
74	-reserved-	00	—
75	PCI Arbitration 1	00	RW
76	PCI Arbitration 2	00	RW
77-7F	-reserved-	00	—

Offset	Reserved	Default	Acc
80-8F	-reserved-	00	—
90-9F	-reserved-	00	—
A0-AF	-reserved-	00	—

Offset	V-Link Compenation / Drive Ctrl	Default	Acc
B0	V-Link Duty Control 1	00	RW
B1	V-Link Duty Control 2	00	RW
B2-B3	-reserved-	00	—
B4	V-Link NB Compensation Control	00	RW
B5	V-Link NB Strobe Drive Control	00	RW
B6	V-Link NB Data Drive Control	00	RW
B7	-reserved-	00	—
B8	V-Link SB Compensation Control	00	RW
B9	V-Link SB Strobe Drive Control	00	RW
BA	V-Link SB Data Drive Control	00	RW
BB-BF	-reserved-	00	—

Offset	Reserved	Default	Acc
C0-CF	-reserved-	00	—
D0-DF	-reserved-	00	—
E0-EF	-reserved-	00	—
F0-FF	-reserved-	00	—

Device 1 Registers - PCI-to-PCI Bridge

Header Registers

Offset	Configuration Space Header	Default	Acc
1-0	Vendor ID	**1106**	RO
3-2	Device ID	**B204**	RO
5-4	Command	**0007**	**RW**
7-6	Status	**0230**	**WC**
8	Revision ID	**nn**	RO
9	Program Interface	00	RO
A	Sub Class Code	**04**	RO
B	Base Class Code	**06**	RO
C	-reserved-	00	—
D	Latency Timer	00	RO
E	Header Type	**01**	RO
F	-reserved- (Built In Self Test)	00	—
10-17	-reserved-	00	—
18	Primary Bus Number	00	**RW**
19	Secondary Bus Number	00	**RW**
1A	Subordinate Bus Number	00	**RW**
1B	Secondary Latency Timer	00	RO
1C	I/O Base	**F0**	**RW**
1D	I/O Limit	00	**RW**
1F-1E	Secondary Status	0000	RO
21-20	Memory Base	**FFF0**	**RW**
23-22	Memory Limit (Inclusive)	0000	**RW**
25-24	Prefetchable Memory Base	**FFF0**	**RW**
27-26	Prefetchable Memory Limit	0000	**RW**
28-33	-reserved-	00	—
34	Capability Pointer	**80**	RO
35-3D	-reserved-	00	—
3F-3E	PCI-to-PCI Bridge Control	00	**RW**

Device-Specific Registers

Offset	AGP Bus Control	Default	Acc
40	CPU-to-AGP Flow Control 1	00	RW
41	CPU-to-AGP Flow Control 2	**08**	RW
42	AGP Master Control	00	RW
43	AGP Master Latency Timer	**22**	RW
44	Reserved (Do Not Program)	**20**	RW
45	Fast Write Control	**72**	RW
47-46	PCI-to-PCI Bridge Device ID	0000	RW
48-7F	-reserved-	00	—

Offset	Power Management	Default	Acc
80	Capability ID	**01**	**RO**
81	Next Pointer	00	**RO**
82	Power Management Capabilities 1	**02**	**RO**
83	Power Management Capabilities 2	00	**RO**
84	Power Management Control / Status	00	RW
85	Power Management Status	00	**RO**
86	PCI-PCI Bridge Support Extensions	00	**RO**
87	Power Management Data	00	**RO**
88-FF	-reserved-	00	—

Miscellaneous I/O

One I/O port is defined: Port 22h.

Port 22 – PCI / AGP Arbiter Disable .....RW

7-1 Reserved ..... always reads 0

0 PCI / AGP Arbiter Disable

0 Respond to all REQ# signals.....default

1 Do not respond to any REQ# signals

This port can be enabled for read/write access by setting bit-7 of Device 0 Function 7 Configuration Register 76h.

Configuration Space I/O

All North Bridge registers (listed above) are addressed via the following configuration mechanism:

Mechanism #1

These ports respond only to double-word accesses. Byte or word accesses will be passed on unchanged.

Port CFB-CF8 - Configuration Address..... RW

31 Configuration Space Enable

0 Disabled..... default

1 Convert configuration data port writes to configuration cycles on the PCI bus

30-24 Reserved .....always reads 0

23-16 PCI Bus Number

Used to choose a specific PCI bus in the system

15-11 Device Number

Used to choose a specific device in the system (devices 0 and 1 are defined)

10-8 Function Number

Used to choose a specific function if the selected device supports multiple functions (functions 0-4 and 7 are defined for device 0 but the function number is unused / ignored for Device 1).

7-2 Register Number (also called the "Offset")

Used to select a specific DWORD in the configuration space

1-0 Fixed .....always reads 0

Port CFF-CFC - Configuration Data..... RW

Refer to PCI Bus Specification Version 2.2 for further details on operation of the above configuration registers.

Device 0 Function 0 Registers - AGP

Device 0 Function 0 Header Registers

All registers are located in PCI configuration space. They should be programmed using PCI configuration mechanism 1 through CF8 / CFC with bus number, function number and device number equal to zero and function number equal to 0.

Offset 1-0 - Vendor ID (1106h) .....RO

15-0 ID Code (reads 1106h to identify VIA Technologies)

Offset 3-2 - Device ID (0204h).....RO

15-0 ID Code (reads 0204h to identify the K8M800 NB)

Offset 5-4 –Command (0006h).....RW

15-10 Reserved ..... always reads 0

9 Fast Back-to-Back Cycle Enable ..... RO
- 0 Fast back-to-back transactions only allowed to the same agent.....default
- 1 Fast back-to-back transactions allowed to different agents

8 SERR# Enable..... RO
- 0 SERR# driver disabled.....default
- 1 SERR# driver enabled

(SERR# is used to report ECC errors).

7 Address / Data Stepping..... RO
- 0 Device never does stepping.....default
- 1 Device always does stepping

6 Parity Error Response.....**RW**
- 0 Ignore parity errors & continue.....default
- 1 Take normal action on detected parity errors

5 VGA Palette Snoop..... RO
- 0 Treat palette accesses normally.....default
- 1 Don't respond to palette accesses on PCI bus

4 Memory Write and Invalidate Command ..... RO
- 0 Bus masters must use Mem Write.....default
- 1 Bus masters may generate Mem Write & Inval

3 Special Cycle Monitoring..... RO
- 0 Does not monitor special cycles.....default
- 1 Monitors special cycles

2 PCI Bus Master..... RO
- 0 Never behaves as a bus master
- 1 Can behave as a bus master.....default

1 Memory Space..... RO
- 0 Does not respond to memory space
- 1 Responds to memory space.....default

0 I/O Space ..... RO
- 0 Does not respond to I/O space .....default
- 1 Responds to I/O space

Offset 7-6 – Status (0210h)..... RWC

15 Detected Parity Error
- 0 No parity error detected..... default
- 1 Error detected in either address or data phase. This bit is set even if error response is disabled (command register bit-6) **.....write one to clear**

14 Signaled System Error (SERR# Asserted)
..... always reads 0

13 Signaled Master Abort
- 0 No abort received ..... default
- 1 Transaction aborted by the master .....
.....write one to clear

12 Received Target Abort
- 0 No abort received ..... default
- 1 Transaction aborted by the target .....
.....write one to clear

11 Signaled Target Abort ..... always reads 0
- 0 Target Abort never signaled

10-9 DEVSEL# Timing
- 00 Fast
- 01 Medium ..... **always reads 01**
- 10 Slow
- 11 Reserved

8 Data Parity Error Detected
- 0 No data parity error detected ..... default
- 1 Error detected in data phase. Set only if error response enabled via command bit-6 = 1 and the North Bridge was initiator of the operation in which the error occurred... write one to clear

7 Fast Back-to-Back Capable..... always reads 0

6 User Definable Features..... always reads 0

5 66MHz Capable..... always reads 0

4 Supports New Capability list..... **always reads 1**

3-0 Reserved ..... always reads 0

Offset 8 - Revision ID (0nh) ..... RO

7-0 Chip Revision Code..... always reads 0nh

Offset 9 - Programming Interface (00h) ..... RO

7-0 Interface Identifier..... always reads 00h

Offset A - Sub Class Code (00h)..... RO

7-0 Sub Class Code..... reads 00 to indicate Host Bridge

Offset B - Base Class Code (06h)..... RO

7-0 Base Class Code.. reads 06 to indicate Bridge Device

Offset D - Latency Timer (00h) ..... RW

Specifies the latency timer value in PCI bus clocks.

7-3 Guaranteed Time Slice for CPU ..... default=0

2-0 Reserved (fixed granularity of 8 clks).. always read 0
Bits 2-1 are writeable but read 0 for PCI specification compatibility. The programmed value may be read back in Rx75[6-4] (PCI Arbitration 1).

Device 0 Function 0 Header Registers (continued)

Offset E - Header Type (00h) ..... RO

7-0 Header Type Code ..... reads 00: single function

Offset F - Built In Self Test (BIST) (00h) ..... RO

7 BIST Supported .....reads 0: no supported functions

6-0 Reserved ..... always reads 0

Offset 13-10 - Graphics Aperture Base (AGP 3.0) (00000008h) ..... RW

31-22 Programmable Base Address Bits ..... def=0

These bits behave as if hardwired to 0 if the corresponding AGP 3.0 Graphics Aperture Size register bit (Device 0 Function 0 Offset 94h) is 0.

31	30	29	28	-	-	27	26	25	24	23	22	(Base)
11	10	9	8	7	6	5	4	3	2	1	0	(Size)
RW	RW	RW	RW	0	0	RW	RW	RW	RW	RW	RW	4M
RW	RW	RW	RW	0	0	RW	RW	RW	RW	RW	0	8M
RW	RW	RW	RW	0	0	RW	RW	RW	RW	0	0	16M
RW	RW	RW	RW	0	0	RW	RW	RW	0	0	0	32M
RW	RW	RW	RW	0	0	RW	RW	0	0	0	0	64M
RW	RW	RW	RW	0	0	RW	0	0	0	0	0	128M
RW	RW	RW	RW	0	0	0	0	0	0	0	0	256M
RW	RW	RW	0	0	0	0	0	0	0	0	0	512M
RW	RW	0	0	0	0	0	0	0	0	0	0	1G
RW	0	0	0	0	0	0	0	0	0	0	0	2G-max
0	0	0	0	0	0	0	0	0	0	0	0	4G

21-4 Reserved ..... always reads 0

3 Prefetchablealways reads 1

Indicates that the locations in the address range defined by this register are prefetchable.

2-1 Type ..... always reads 0

Indicates the address range in the 32-bit address space.

0 Memory Space..... always reads 0

Indicates the address range in the memory address space.

Offset 2D-2C – Subsystem Vendor ID (0000h) R/W1

15-0 Subsystem Vendor ID ..... default = 0

This register may be written once and is then read only.

Offset 2F-2E – Subsystem ID (0000h) R/W1

15-0 Subsystem ID ..... default = 0

This register may be written once and is then read only.

Offset 34 - Capability Pointer (CAPPTR) ..... RO

Contains an offset from the start of configuration space.

7-0 AGP Capability List Pointer ..... always reads 80h

Device 0 Function 0 Device-Specific Registers

These registers are normally programmed once at system initialization time.

AGP Drive Control

Offset 40 – AGP Pad Control / Status (8xh) .....RW

7 AGP 4x Strobe VREF Control
- 0 STB VREF is STB# and vice versa
- 1 STB VREF is AGPREF **.....default**

6 AGP 4x Strobe & GD Pad Drive Strength
- 0 Drive strength set to compensation circuit default .....default
- 1 Drive strength controlled by RxB1[7-0]

5-3 AGP Compensation Circuit N Control Output.RO

2-0 AGP Compensation Circuit P Control Output .RO

Note: N = low drive, P = high drive

Offset 41 – AGP Output Buffer Drive Strength (63h) ...RW

7-4 AGP Output Buffer Low Drive Strength..... def=6

3-0 AGP Output Buffer High Drive Strength..... def=3

Offset 42 – AGP Pad Drive / Delay (00h) ..... RW

7 GD/GBE/GDS, SBA/SBS Control
- 0 SBA/SBS = no cap ..... default
  GD/GBE/GDS = no cap
- 1 SBA/SBS = **cap**
  GD/GBE/GDS = **cap**

6-5 GD / GC#BE Receive Strobe Delay
- 00 None ..... default
- 01 Delay by 1.5 ns
- 10 Delay by 3.0 ns
- 11 Delay by 4.5 ns

4 GD[31-16] Staggered Delay
- 0 None ..... default
- 1 GD[31:16] delayed by 1 ns

3 AGP Slew Rate Control
- 0 Disable..... default
- 1 Enable

2 SBA Receive Strobe Delay
- 0 None ..... default
- 1 Delay by 1.5 ns

1-0 GDS Output Delay
- 00 None ..... default
- 01 Delay by 1.5 ns
- 10 Delay by 3.0 ns
- 11 Delay by 4.5 ns

(GDS1 & GDS1# will be delayed an additional 1ns if bit-4 = 1)

Offset 43 – AGP Strobe Drive Strength..... RW

7-4 AGP Strobe Output Low Drive Strength..... def=0

3-0 AGP Strobe Output High Drive Strength..... def=0

AGP Miscellaneous Control

Offset 4A – AGP Request Queue Size (1Fh) ..... RW

These bit settings will effect the hardware if Rx4D[1] = 1.

7-0 AGP Request Queue Size ..... default = 1Fh

Offset 4B – AGP Hardware Support (C4h) ..... RW

These bit settings will effect the hardware if Rx4D[1] = 1.

7 AGP SBA Mode
- 0 Disable
- 1 Enable **..... default**

6 AGP
- 0 Disable
- 1 Enable **..... default**

5 Reserved ..... always reads 0

4 AGP Fast Write
- 0 Disable ..... default
- 1 Enable

3 AGP 8x Mode
- 0 Disable ..... default
- 1 Enable

2 AGP 4x Mode
- 0 Disable
- 1 Enable **..... default**

1 AGP 2x Mode
- 0 Disable ..... default
- 1 Enable

0 AGP 1x Mode
- 0 Disable ..... default
- 1 Enable

Offset 4D – AGP Capability Header Control (04h)..... RW

7-4 Reserved ..... always reads 0

3 Reserved ..... always reads 0

2 Select Rx80 as the AGP3x Header
- 0 Disable AGP3.x Header (test mode)
- 1 Enable AGP3.x Header **..... default**

1 AGP Hardware Registers Rx4A-4B
- 0 Disable – AGP hardware is controlled by values in the AGP Capability Header.... default
- 1 Enable – AGP hardware is controlled by values in Device 0 Function 0 Rx4A-4B

0 AGP Capability Header Status Register Write
- 0 Disable – status registers are read-only . default
- 1 Enable – status registers can be written

Offset 4F – Multiple Function Control (00h) ..... RW

7-1 Reserved ..... always reads 0

0 This Bridge Configuration Suports MultiFunction
- 0 Multifunction not supported – other functions 1, 2, 3, 4 and 7 cannot be seen and will return FFFFFFFFh when accessed..... default
- 1 Multifunction supported – reflected on RxE[7]

AGP Power Management Control

Offset 50 – Power Management Capability ID.....RO

7-0 Capability ID..... always reads 01h

Offset 51 – Power Management Next Pointer.....RO

7-0 Next Pointer..... always reads 00h (“Null” Pointer)

Offset 52 – Power Mgmt Capabilities I .....RO

7-0 Power Management Capabilities.. always reads 02h

Offset 53 – Power Mgmt Capabilities II.....RO

7-0 Power Management Capabilities.. always reads 00h

Offset 54 – Power Mgmt Control / Status .....RW

7-2 Reserved ..... always reads 0

1-0 Power State

00 D0 .....default
01 -reserved-
10 -reserved-
11 D3 Hot

Offset 55 – Power Management Status..... RO

7-0 Power Management Status.....always reads 00h

Offset 56 – PCI-to-PCI Bridge Support Ext..... RO

7-0 P2P Bridge Support Extensions....always reads 00h

Offset 57 – Power Management Data ..... RO

7-0 Power Management Data .....always reads 00h

HyperTransport Control

Offset 63-60 – Link Command Device A (0060 5808h)..RW

31-29 Slave / Primary Interface Type..... always reads 0

28-26 Reserved ..... always reads 0

25-21 Unit ID Count.....**always reads 3**
Specifies the number of unit IDs used by the chip (3).

20-16 Base Unit ID ..... default = 0
Specifies the link-protocol base Unit ID. Hardware uses this value to determine the Unit IDs for link request and response packets. When a new value is written to this field, the response includes a Unit ID that is based on the new value in this register.

15-8 Capabilities Pointer .....**always reads 58h**
Capability lists:
Rx34 => Rx80 (AGP3x) / RxA0 (AGP20)
=> Rx50 (PWD)
=> Rx60 (LDT)
=> Rx58 (INT)
=> …

7-0 Capabilities ID .....**always reads 08h**
Specifies the capabilities ID for the link configuration space.

Offset 67-64 – Link Config/Ctrl Device A (??11 0020h) WC

DevA:C4h applies to side A of the tunnel and DevA:C8h applies to the B side of the tunnel. The default value for bit-5 may vary (see bit definitions below)

31 Reserved .....always reads 0

30-28 Link Width Out.....
..... **default depends on width of connected device**
Specifies the operating width of the outgoing link.
000 8 bits
001 16 bits, DevA:C4h only
010 -reserved-
011 -reserved-
100 2 bits
101 4 bits
110 -reserved-
111 Not connected
This field is cleared by PWROK but not by RESET#. The default value of this field depends on the widths of the links of the connecting device per the link specification. After this field is updated, the link width does not change until either RESET# is asserted or a link disconnect sequence occurs via HTSTOP#.

27 Reserved .....always reads 0

26-24 Link Width In.....
..... **default depends on width of connected device**
Specifies the operating width of the incoming link.
000 8 bits
001 16 bits, DevA:C4h only
010 -reserved-
011 -reserved-
100 2 bits
101 4 bits
110 -reserved-
111 Not connected
This field is cleared by PWROK but not by RESET#. The default value of this field depends on the widths of the links of the connecting device per the link specification. After this field is updated, the link width does not change until either RESET# is asserted or a link disconnect sequence occurs via HTSTOP#.

23 Reserved .....always reads 0

22-20 Max Link Width Out ..... **always reads 001b**
Value indicates 16 bits for side A and 8 for side B.

19 Reserved .....always reads 0

18-16 Max Link Width In ..... **always reads 001b**
Value indicates 16 bits for side A and 8 for side B.

(continued on following page)

Offset 67-64 (continued from previous page)

15 Reserved ..... always reads 0

14 Extended Control Time During Initialization
Specifies the time in which HT[B,A]CTL is held asserted during the initialization sequence that follows an HTSTOP# assertion after Receive {B,A} CTL is detected as being asserted. This bit is cleared by PWROK but not by RESET#.
- 0 At least 16 bit times .....default
- 1 About 50 microseconds

13 Link Three-State Enable
During the HTSTOP# disconnect sequence:
- 0 Link transmitter signals are driven but in an undefined state. Link receiver signals are assumed to be driven.....default
- 1 Link transmitter signals are high impedance. Receivers are prepared for high-impedance mode, including cutting power to the receiver differential amps and insuring that there are no resultant high-current paths in the circuits.

This bit is cleared by PWROK but not by RESET#.

12-10 Reserved ..... always reads 0

9-8 CRC Error .....**Write 1 to Clear**
Bit-9 applies to the upper byte of the link (DevA:C4h only) and bit-8 applies to the lower byte. These bits are cleared by PWROK but not by RESET#.
- 0 No CRC error.....default
- 1 Hardware detected a CRC error on the incoming link .....**Write 1 to Clear**

7 Transmitter Off....always reads 0 (not implemented)

6 End of Chain .....always reads 0 (not implemented)

5 Initialization Complete ..... RO
This bit is set by hardware when low-level link initialization completes successfully. If there is no device on the other end of the link, or if the device on the other end of the link is unable to properly perform link initialization, then this bit is not set. This bit is cleared when RESET# is asserted or after the link disconnect sequence completes after the assertion of HTSTOP#.

4 Link Failure..... Write1 to Clear
Set to 1 by hardware when a CRC error is detected on the link (if enabled by bit-1) or if the link is not used in the system. This bit is cleared by PWROK but not by RESET#.

3 CRC Error Command
This bit is intended to be used in test mode only to check the CRC failure detection logic of the device on the other side of the link.
- 0 Transmitted CRC values match the values calculated per the link specification. ..... default
- 1 Link transmission logic generates erroneous CRC values

2 Reserved .....always reads 0

1 CRC Flood
- 0 CRC errors do not result in sync packets to the outgoing link and do not set the Link Fail bit (bit-4 of this register)..... default
- 1 CRC errors result in sync packets to the outgoing link and set the Link Fail bit (bit-4 of this register).

0 Reserved .....always reads 0

Offset 6B-68 – Subordinate Link Status (0000 00D0h) .. RO

31-8 Reserved .....always reads 0

7 Transmitter Off..... **always reads 1**
This bit is hardwired high to indicate that there is no subordinate HyperTransport link.

6 End of HT Chain ..... **always reads 1**
This bit is hardwired high to indicate that there is no subordinate HyperTransport link.

5 Reserved .....always reads 0

4 Link Failure..... **always reads 1**
This bit is hardwired high to indicate that there is no subordinate HyperTransport link.

3-0 Reserved .....always reads 0

Offset 6F-6C – Link A Freq Capability (0035 0022h)....RW

31-16 Link A Frequency Capability ..**always reads 0035h**
These bits indicate that the A side of the tunnel supports 200, 400, 600 and 800 MHz link frequencies.

15-12 Reserved ..... always reads 0

11-8 Link A Frequency
Specifies the link side A frequency.
0000 200 MHz .....default
00x1 -reserved-
0010 400 MHz
0100 600 MHz
0101 800 MHz
011x -reserved-
1xxx -reserved-
After this field is updated, the link frequency does not change until either RESET# is asserted or a link disconnect sequence occurs via HTSTOP#. The default is set on the rising edge of PWROK (the value is unchanged by RESET#).

7-5 Major Revision.....**always reads 001b**

4-0 Minor Revision.....**always reads 00010b**
Bits 7-0 above are hardwired to indicate that the logic was designed to conform to link specification 1.02.

Offset 73-70 – Link B Freq Capability (0035 0022h)..... RW

31-16 Link B Frequency Capability.. **always reads 0035h**
These bits indicate that the B side of the tunnel supports 200, 400, 600 and 800 MHz link frequencies.

15-12 Reserved .....always reads 0

11-8 Link B Frequency
Specifies the link side B frequency.
0000 200 MHz..... default
00x1 -reserved-
0010 400 MHz
0100 600 MHz
0101 800 MHz
011x -reserved-
1xxx -reserved-
After this field is updated, the link frequency does not change until either RESET# is asserted or a link disconnect sequence occurs via HTSTOP#. The default is set on the rising edge of PWROK (the value is unchanged by RESET#).

7-5 Major Revision ..... **always reads 001b**

4-0 Minor Revision ..... **always reads 00010b**
Bits 7-0 above are hardwired to indicate that the logic was designed to conform to link specification 1.02.

Offset 77-74 – Link Enumeration Scratchpad ..... RW

31-16 Reserved .....always reads 0

15-0 Enumeration Scratchpad.....default = 0000h
These bits are reserved for use by software.and control no on-chip logic. These bits are cleared by PWROK but are unaffected by RESET#.

AGP GART / Graphics Aperture

The function of the Graphics Address Relocation Table (GART) is to translate virtual 32-bit addresses issued by an AGP device into 4K-page based physical addresses for system memory access. In this translation, the upper 20 bits (A31-A12) are remapped, while the lower 12 address bits (A11-A0) are used unchanged.

A one-level fully associative lookup scheme is used to implement the address translation. In this scheme, the upper 20 bits of the virtual address are used to point to an entry in a page table located in system memory. Each page table entry contains the upper 20 bits of a physical address (a "physical page" address). For simplicity, each page table entry is 4 bytes. The total size of the page table depends on the GART range (called the "aperture size") which is programmable in the K8M800.

This scheme is shown in the figure below.

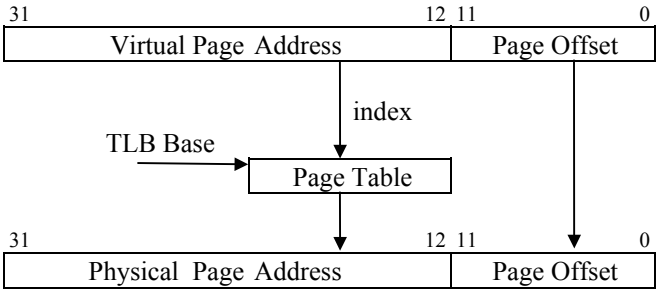


Figure 4. Graphics Aperture Address Translation

Since address translation using the above scheme requires an access to system memory, an on-chip cache (called a "Translation Lookaside Buffer" or TLB) is utilized to enhance performance. The TLB in the K8M800 contains 16 entries. Address "misses" in the TLB require an access of system memory to retrieve translation data. Entries in the TLB are replaced using an LRU (Least Recently Used) algorithm.

Addresses are translated only for accesses within the "Graphics Aperture" (GA). The Graphics Aperture can be any power of two in size from 1MB to 256MB (i.e., 1MB, 2MB, 4MB, 8MB, etc) for AGP 2.0 and 4MB to 2GB for AGP 3.x. The base of the Graphics Aperture can be anywhere in the system virtual address space on an address boundary determined by the aperture size (e.g., if the aperture size is 4MB, the base must be on a 4MB address boundary). The Graphics Aperture Base is defined in Device 0 Function 0 Rx10. The Graphics Aperture Size and TLB Table Base for both AGP 2.0 and AGP 3.x are defined in Rx94 and Rx98 along with various control bits.

AGP 3.x Registers

Offset 83-80 - AGP 3.x Capabilities (0030C002h) .....RO

31-24 Reserved ..... always reads 00
23-20 Major Specification Revision ... always reads 0011b
Major rev # of AGP spec that device conforms to
19-16 Minor Specification Revision ... always reads 0000b
Minor rev # of AGP spec that device conforms to
15-8 Pointer to Next Item ..... always reads C0 (last item)
7-0 AGP Capability ID
(always reads 02 to indicate it is AGP)

Offset 87-84 - AGP 3.x Status (1F000201h) .....RO

31-24 Maximum AGP Requests..... always reads 1Fh
Max # of AGP requests the device can manage (32)
23-16 Reserved .....always reads 0s†
15-13 Optimum Async Request Size.....always reads 0s†
Suggested setting is 010b or 2^(2+4)=64 Bytes for 8QW access
12-10 Calibration Cycle Setting
000 4 ms
001 16 ms
010 64 ms **.....default†**
011 256 ms
9 Supports Side Band Addressing.....**always reads 1**
8 Reserved ..... always reads 0†
7 64-Bit GART Entries..... always reads 0
6 CPU GART Translation Supported. always reads 0
5 Addresses Above 4G Supported..... always reads 0
4 Fast Write Supported..... always reads 0
3 AGP 8x Detected.....Set from AGP8XDT# pin
2 4X Rate Supported .....Reads 0 if bit-3 = 1
.....Reads 1 if bit-3 = 0
1 2X Rate Supported .....**always reads 1**
0 1X Rate Supported .....**always reads 1**

†Writable if Rx4D[0] = 1.

Offset 8B-88 - AGP 3.x Command ..... RW

31-24 Request Depth (reserved for target).. always reads 0s
23-13 Reserved ..... always reads 0s
12-10 Calibration Cycle Select..... default = 0
9 Side Band Addressing
0 Disable..... default
1 Enable
8 AGP
0 Disable..... default
1 Enable
7-6 Reserved ..... always reads 0s
5 Addresses Over 4G
0 Disable..... default
1 Enable
4 Fast Write
0 Disable..... default
1 Enable
3 Reserved ..... always reads 0s
2-0 Transfer Mode Select..... default = 000b
Rx84[3] = 0 (8x mode **not detected** via AGP8XDT#)
001 1x data transfer rate
010 2x data transfer rate
100 4x data transfer rate
Rx84[3] = 1 (8x mode **detected** via AGP8XDT#)
000 -reserved..... default
001 4x data transfer rate
010 8x data transfer rate

Offset 93-90 - AGP 3.x GART / TLB Control .....RW

31-10 Reserved .....always reads 0s

9 Calibration Cycle
- 0 Disable .....default
- 1 Enable

8 Graphics Aperture Base Register (Rx13-10) Read
- 0 Disable .....default
- 1 Enable

7 GART TLB
- 0 Disable (TLB entries are invalidated) ....default
- 1 Enable

6-0 Reserved .....always reads 0s

Offset 97-94 - AGP 3.x Graphics Aperture Size ..... RW

31-28 Aperture Page Size Select.....default = 0000b
Only 4K pages are allowed

27 Reserved ..... always reads 0s

26-16 Page Size Supported.....default = 001h
If bit-n of this field is 1, indicates support of 2^(n+12) page size. Must be set to 001h (field bit-0 set) to indicate only 4K pages allowed.

15-12 Reserved ..... always reads 0s

11-0 Aperture Size.....default = 0

111100111111	4MB
111100111110	8MB
111100111100	16MB
111100111000	32MB
111100110000	64MB
111100100000	128MB
111100000000	256MB
111000000000	512MB
110000000000	1GB
100000000000	2GB <= Max supported
000000000000	4GB <= Do not program

Offset 9B-98 – AGP 2.0 / 3.x GART Table Base ..... RW

31-12 Graphics Aperture Translation Table Base. Pointer to the base of the translation table in system memory used to map addresses in the aperture range (the pointer to the base of the "Directory" table).

11-2 Reserved .....always reads 0

1 Graphics Aperture
- 0 Disable..... default
- 1 Enable

Note: To disable the Graphics Aperture, set this bit to 0 and set all bits of the Graphics Aperture Size to 0. To enable the Graphics Aperture, set this bit to 1 and program the Graphics Aperture Size to the desired aperture size.

0 Reserved .....always reads 0

AGP Miscellaneous Registers

Offset B8 - AGP Pad Power Down (00h).....RW

7-3 Reserved ..... always reads 0

2 AGP Pad Power Down
- 0 Disable .....default
- 1 Enable

1-0 Reserved ..... always reads 0

Offset B9 - AGP Mixed Control (00h).....RW

7 Reserved ..... always reads 0

6 Maintain GD Value by Read Transmit Ready
- 0 Disable .....default
- 1 Enable

5-0 Total Number of Isochronous Requests... def = 00h

Offset BA – Isoch Read GPRI Counter (00h).....RW

7-0 GPRI Counter for Each Isochronous Request to Assert GPRI for Isochronous Read..... def = 00h

Offset BB – Isoch Write GPRI Counter (00h).....RW

7-0 GPRI Counter for Each Isochronous Request to Assert GPRI for Isochronous Write..... def = 00h

Offset BC - AGP Control (00h) ..... RW

7 AGP
- 0 **Enable**..... default
- 1 **Disable**

6 AGP Read Synchronization
- 0 Disable..... default
- 1 Enable

5 AGP Read Snoop DRAM Post-Write Buffer
- 0 Disable..... default
- 1 Enable

4 GREQ Priority
- 0 GREQ has higher priority if FIFO is not over 24QW for low priority reads ..... default
- 1 GREQ priority becomes higher when arbiter is parked at AGP master

3 GGNT Assertion
- 0 GGNT asserted when one block of data is back
- 1 GGNT asserted when all data from this request is back

2 Fence / Flush
- 0 Disable..... default
- 1 Enable

1 GGNT Parking Policy
- 0 Non-parking GGNT – if GFRAME or GPIPE# is asserted, GGNT is deasserted ..... default
- 1 Parking GGNT – if GFRAME or GPIPE# is asserted, GGNT not deasserted until GREQ deasserted or timeout

0 AGP to PCI Master or CPU to PCI Turnaround Cycle
- 0 2T or 3T Timing..... default
- 1 1T Timing

Offset BD – AGP Miscellaneous Control 1 (02h) .....RW

7 Avoid Grant Isochronous Write Data Without Payload Size Information
- 0 Disable .....default
- 1 Enable

6 Pipe Mode Performance Improvement
- 0 Disable .....default
- 1 Enable

5 AGP Data Input Enable (for Power Saving)
- 0 AGP data input always enabled .....default
- 1 AGP data input only enabled when necessary to avoid redundant transitions

4 AGP Performance Improvement
- 0 Disable .....default
- 1 Enable

3-0 AGP Data Phase Latency Timer ..... default = 02h

Offset BE – AGP Miscellaneous Control 2 (00h).....RW

7 NMI / AGPBUSY# Select
- 0 NMI .....default
- 1 AGPBUSY#

6 Assert PP2OFF On Isochronous Request
- 0 Disable .....default
- 1 Enable

5 AGP Isoch Read Snoop DRAM Post-Write Buffer
- 0 Disable .....default
- 1 Enable

4 Guard Bit for Isochronous Request With Length Not Consistent with Isoch Payload Size
(the Isoch Payload Size is in bits 7-6 of the AGP Isoch Command register at CAPPTR + 20h)
- 0 Disable .....default
- 1 Enable

3 Isoch Read Shares FIFO When No Asynch Read Allocated
- 0 Disable .....default
- 1 Enable

2 Reserved ..... always reads 0

1 Isoch Ready Assertion
- 0 When one block of data is received .....default
- 1 When all transaction data is received

0 CPU GART Read, AGP GART Write Coherency
- 0 Disable .....default
- 1 Enable

Offset BF – AGP 3.x Control (00h) ..... RW

7 CPU / PCI Master GART Access
- 0 Disable..... default
- 1 Enable

6 AGP Calibration
- 0 Disable..... default
- 1 Enable

5 Mix Coherent / Non-Coherent Accesses
- 0 Disable..... default
- 1 Enable

4 DBI / PIPE Pin Function Select (Pin AC5)
- 0 GDBIH ..... default
- 1 GPIPE#

3 DBI Function
- 0 Disable (DBI inputs are masked and outputs assume DBI=0)..... default
- 1 Enable

2 DBI Output for AGP Transactions
- 0 Disable..... default
- 1 Enable

1 DBI Output for FRAME# Transactions Including Fast Write
- 0 Disable..... default
- 1 Enable

0 DBI Output From FRAME# Transactions
- 0 Disable..... default
- 1 Enable

Offset C0 – AGP Duty Control 1 (00h)..... RW

7 AGP1 R-Port CKG Rise Time Duty Cycle Control
6 AGP0 R-Port CKG Rise Time Duty Cycle Control
5 AGP1 R-Port CKG Fall Time Duty Cycle Control
4 AGP0 R-Port CKG Fall Time Duty Cycle Control
3 AGP1 S-Port CKG Rise Time Duty Cycle Control
2 AGP0 S-Port CKG Rise Time Duty Cycle Control
1 AGP1 S-Port CKG Fall Time Duty Cycle Control
0 AGP0 S-Port CKG Fall Time Duty Cycle Control

Offset C1 – AGP Duty Control 2 (00h)..... RW

7-4 Reserved.....always reads 0
3 AGP1 D-Port CKG Rise Time Duty Cycle Control
2 AGP0 D-Port CKG Rise Time Duty Cycle Control
1 AGP1 D-Port CKG Fall Time Duty Cycle Control
0 AGP0 D-Port CKG Fall Time Duty Cycle Control

Device 0 Function 1 Registers – Error Reporting

Device 0 Function 1 Header Registers

All registers are located in PCI configuration space. They should be programmed using PCI configuration mechanism 1 through CF8 / CFC with bus number and device number equal to zero and function number equal to 1.

Offset 1-0 - Vendor ID (1106h) ..... RO

15-0 ID Code (reads 1106h to identify VIA Technologies)

Offset 3-2 - Device ID (1204h) ..... RO

15-0 ID Code (reads 1204h to identify K8M800 NB virtual device function 1)

Offset 5-4 –Command (0006h) ..... RW

15-10 Reserved ..... always reads 0

9 Fast Back-to-Back Cycle Enable ..... RO
- 0 Fast back-to-back transactions only allowed to the same agent.....default
- 1 Fast back-to-back transactions allowed to different agents

8 SERR# Enable..... RO
- 0 SERR# driver disabled.....default
- 1 SERR# driver enabled

(SERR# is used to report ECC errors).

7 Address / Data Stepping..... RO
- 0 Device never does stepping.....default
- 1 Device always does stepping

6 Parity Error Response.....**RW**
- 0 Ignore parity errors & continue.....default
- 1 Take normal action on detected parity errors

5 VGA Palette Snoop..... RO
- 0 Treat palette accesses normally.....default
- 1 Don't respond to palette accesses on PCI bus

4 Memory Write and Invalidate Command ..... RO
- 0 Bus masters must use Mem Write.....default
- 1 Bus masters may generate Mem Write & Inval

3 Special Cycle Monitoring..... RO
- 0 Does not monitor special cycles.....default
- 1 Monitors special cycles

2 PCI Bus Master..... RO
- 0 Never behaves as a bus master
- 1 Can behave as a bus master.....default

1 Memory Space..... RO
- 0 Does not respond to memory space
- 1 Responds to memory space.....default

0 I/O Space ..... RO
- 0 Does not respond to I/O space .....default
- 1 Responds to I/O space

Offset 7-6 – Status (0200h)..... RWC

15 Detected Parity Error
- 0 No parity error detected..... default
- 1 Error detected in either address or data phase. This bit is set even if error response is disabled (command register bit-6). ..... write one to clear

14 Signaled System Error (SERR# Asserted) .....always reads 0

13 Signaled Master Abort
- 0 No abort received ..... default
- 1 Transaction aborted by the master .... write one to clear

12 Received Target Abort
- 0 No abort received ..... default
- 1 Transaction aborted by the target .... write one to clear

11 Signaled Target Abort .....always reads 0
- 0 Target Abort never signaled

10-9 DEVSEL# Timing
- 00 Fast
- 01 Medium .....always reads 01
- 10 Slow
- 11 Reserved

8 Data Parity Error Detected
- 0 No data parity error detected ..... default
- 1 Error detected in data phase. Set only if error response enabled via command bit-6 = 1 and the North Bridge was initiator of the operation in which the error occurred... write one to clear

7 Fast Back-to-Back Capable.....always reads 0

6 User Definable Features.....always reads 0

5 66MHz Capable.....always reads 0

4 Supports New Capability list.....always reads 0

3-0 Reserved .....always reads 0

Offset 8 - Revision ID (0nh) ..... RO

7-0 Chip Revision Code.....always reads 0nh

Offset 9 - Programming Interface (00h) ..... RO

7-0 Interface Identifier.....always reads 00h

Offset A - Sub Class Code (00h)..... RO

7-0 Sub Class Code.....reads 00 to indicate Host Bridge

Offset B - Base Class Code (06h)..... RO

7-0 Base Class Code..reads 06 to indicate Bridge Device

Device 0 Function 1 Device-Specific Registers

These registers are normally programmed once at system initialization time.

V-Link Error Control

Offset 50 – North Bridge V-Link Error Status.....WC

7-1 Reserved ..... always reads 0

0 V-Link Parity Error Detected .....WC

0 No error detected.....default

1 V-Link parity error detected (write 1 to clear)

Offset 58 – North Bridge V-Link Error Command .....RW

7 V-Link Parity Error or SERR Reporting to NMI

0 Disable .....default

1 Enable

6 V-Link Parity Error or SERR Reporting to SB via V-Link

0 Disable .....default

1 Enable

5-1 Reserved ..... always reads 0

0 V-Link Parity Check Report

0 Disable .....default

1 Enable

AGP Error Control

Offset E0 – AGP Error Status ..... WC

7 AGP Data Parity Error Detected..... WC

0 No error detected ..... default

1 AGP data parity error detected (write 1 to clear)

6 PCI2 GSERR Detected ..... WC

0 No error detected ..... default

1 PCI2 GSERR detected (write 1 to clear)

5-0 Reserved .....always reads 0

Offset E1 – AGP Isochronous Error Status ..... RO

7-2 Reserved .....always reads 0

1-0 Isochronous Error Code from Func 0 Rx8C[1:0]...

.....default = 0

Offset E8 – AGP Error Command..... RW

7-5 Reserved .....always reads 0

4 AGP Data Parity Error Reporting

0 Disable..... default

1 Enable

3-2 Reserved .....always reads 0

1 PCI2 Data Parity Error Reporting

0 Disable..... default

1 Enable

0 PCI2 Address Parity Error Reporting

0 Disable..... default

1 Enable

Device 0 Function 2 Registers – Host CPU

Device 0 Function 2 Header Registers

All registers are located in PCI configuration space. They should be programmed using PCI configuration mechanism 1 through CF8 / CFC with bus number and device number equal to zero and function number equal to 2.

Offset 1-0 - Vendor ID (1106h) ..... RO

15-0 ID Code (reads 1106h to identify VIA Technologies)

Offset 3-2 - Device ID (2204h) ..... RO

15-0 ID Code (reads 2204h to identify K8M800 NB virtual device function 2)

Offset 5-4 –Command (0006h) ..... RW

15-10 Reserved ..... always reads 0

9 Fast Back-to-Back Cycle Enable ..... RO
- 0 Fast back-to-back transactions only allowed to the same agent ..... default
- 1 Fast back-to-back transactions allowed to different agents

8 SERR# Enable ..... RO
- 0 SERR# driver disabled ..... default
- 1 SERR# driver enabled

(SERR# is used to report ECC errors).

7 Address / Data Stepping ..... RO
- 0 Device never does stepping ..... default
- 1 Device always does stepping

6 Parity Error Response ..... RW
- 0 Ignore parity errors & continue ..... default
- 1 Take normal action on detected parity errors

5 VGA Palette Snoop ..... RO
- 0 Treat palette accesses normally ..... default
- 1 Don't respond to palette accesses on PCI bus

4 Memory Write and Invalidate Command ..... RO
- 0 Bus masters must use Mem Write ..... default
- 1 Bus masters may generate Mem Write & Inval

3 Special Cycle Monitoring ..... RO
- 0 Does not monitor special cycles ..... default
- 1 Monitors special cycles

2 PCI Bus Master ..... RO
- 0 Never behaves as a bus master
- 1 Can behave as a bus master ..... default

1 Memory Space ..... RO
- 0 Does not respond to memory space
- 1 Responds to memory space ..... default

0 I/O Space ..... RO
- 0 Does not respond to I/O space ..... default
- 1 Responds to I/O space

Offset 7-6 – Status (0200h) ..... RWC

15 Detected Parity Error
- 0 No parity error detected ..... default
- 1 Error detected in either address or data phase. This bit is set even if error response is disabled (command register bit-6). ..... write one to clear

14 Signaled System Error (SERR# Asserted) ..... always reads 0

13 Signaled Master Abort
- 0 No abort received ..... default
- 1 Transaction aborted by the master ..... write one to clear

12 Received Target Abort
- 0 No abort received ..... default
- 1 Transaction aborted by the target ..... write one to clear

11 Signaled Target Abort ..... always reads 0
- 0 Target Abort never signaled

10-9 DEVSEL# Timing
- 00 Fast
- 01 Medium ..... always reads 01
- 10 Slow
- 11 Reserved

8 Data Parity Error Detected
- 0 No data parity error detected ..... default
- 1 Error detected in data phase. Set only if error response enabled via command bit-6 = 1 and the North Bridge was initiator of the operation in which the error occurred... write one to clear

7 Fast Back-to-Back Capable ..... always reads 0

6 User Definable Features ..... always reads 0

5 66MHz Capable ..... always reads 0

4 Supports New Capability list ..... always reads 0

3-0 Reserved ..... always reads 0

Offset 8 - Revision ID (0nh) ..... RO

8-0 Chip Revision Code ..... always reads 0nh

Offset 9 - Programming Interface (00h) ..... RO

7-0 Interface Identifier ..... always reads 00h

Offset A - Sub Class Code (00h) ..... RO

7-0 Sub Class Code ..... reads 00 to indicate Host Bridge

Offset B - Base Class Code (06h) ..... RO

7-0 Base Class Code .. reads 06 to indicate Bridge Device

Device 0 Function 2 Device-Specific Registers

These registers are normally programmed once at system initialization time.

Host CPU HyperTransport Control

Offset A0 – CPU Control 1 (00h) ..... RW

7 In-Order Processing of CPU-to-PCI / CPU-to-AGP Requests or HT Ordering Rule
- 0 Disable .....default
- 1 Enable

6 In-Order Response of PCI Master Write Ready and PCI Master Read Ready
- 0 Disable .....default
- 1 Enable

5 In-Order Response of AGP Master Write Ready and AGP Master Read Ready
- 0 Disable .....default
- 1 Enable

4 AGP ADS Read Outstanding Request Number
- 0 16 .....default
- 1 32

3 EOI Cycles to PCI2
- 0 Disable .....default
- 1 Enable

2-0 Number of Outstanding PCI-to-CPU Requests on HT Bus ..... default = 0

Offset A1 – CPU Control 2 (00h) ..... RW

7 ROMSIP Support.....default set from VAD6
- 0 Disable
- 1 Enable

6 Set Isochronous Request Bit for PCI-to-CPU Requests with PMSIO
- 0 Disable..... default
- 1 Enable

5 Set Isochronous Request Bit for AGP-to-CPU Requests with GPRI
- 0 Disable..... default
- 1 Enable

4 Set Isoc Request Bit for All PCI-to-CPU Requests
- 0 Disable..... default
- 1 Enable

3 Set Isoc Request Bit for All AGP-to-CPU Requests
- 0 Disable..... default
- 1 Enable

2 Non-Posted Response of CPU-to-PCI from PCI Will Wait for Previous PCI-to-CPU Write PCI Write Flush
- 0 Disable..... default
- 1 Enable

1 Non-Posted Response of CPU-to-AGP from AGP Will Wait for Previous AGP-to-CPU Write AGP Write Flush
- 0 Disable..... default
- 1 Enable

0 256-Byte RAM Access
- 0 Disable..... default
- 1 Enable

Offset A2 – RAM Base Address (00h)..... RW

7-0 256-Byte RAM Base Address ..... default = 00h

Offset A3 – HyperTransport Init Value 1 (B1h) .....RW

7 CPU Fast Command.....RO
- 0 Disable
- 1 Enable **.....default**

6-4 HT400 Initialization Counter .... default =11b, set from ROMSIP[57:55]

3 AGP Isochronous Read Outstanding Request Number
- 0 16 .....default
- 1 32

2-0 HT200 Initialization Counter .... default =01b, set from ROMSIP[54:52]

Offset A4 – HyperTransport Init Value 2 (30h) .....RW

7 VADS Read Outstanding Request Number
- 0 16 .....default
- 1 32

6-4 HT800 Initialization Counter .... default =11b, set from ROMSIP[63:61]

3 Reserved ..... always reads 0

2-0 HT600 Initialization Counter .... default =00b, set from ROMSIP[60:58]

Offset A5 – Arbitration Control 1 (08h) ..... RW

7 AGP Read Length Could Be 1QW-8QW But Not 1/2/4/8QW For AGP Performance
- 0 Disable..... default
- 1 Enable

6 AGP Write Length
- 0 Issue Byte Writes for all BE Writes ..... default
- 1 Issue DoubleWord Writes for all BE Writes

5 HT Controller Action for PCI-to-CPU Write Cycles With All Byte Enables Set
- 0 Issue DoubleWord Write..... default
- 1 Issue Byte Write

4 AGP 8QW Read Access from HT
- 0 Disable (no 8QW access) ..... default
- 1 Enable (allow 8QW access)

3 CF8 / CFC I/O Cycles
- 0 Disable..... default
- 1 Enable

2 PCI Master Access Bursting
- 0 Allow only 1 request before data phase. default
- 1 Allow up to 4 pipelined requests before data phase

1 Reduce 1T Latency for AGP Access (Allow 8x 4QW Access to Burst)
- 0 Disable..... default
- 1 Enable

0 Reserved (Do Not Program) ..... default = 0

Offset A6 – Arbitration Control 2 (00h) ..... RW

7 Clear CPU-to-PCI Read Response PassPW Bit
- 0 Disable..... default
- 1 Enable

6 Set CPU-to-PCI Target Done PassPW Bit
- 0 Disable..... default
- 1 Enable

5 Clear CPU-to-PCI Target Done PassPW Bit
- 0 Disable..... default
- 1 Enable

4 Legacy NMI Encoding for MT[3]
- 0 Disable..... default
- 1 Enable

3 Legacy External Interrupt Encoding for MT[3]
- 0 Disable..... default
- 1 Enable

2 Reduce 1T Latency for Fast Write Cycles (Allow FW 8QW Access to Burst)
- 0 Disable..... default
- 1 Enable

1 VID / FID Change Delay to P-State Control
- 0 Disable..... default
- 1 Enable

0 Reserved .....always reads 0

Offset A7 – HyperTransport Control 1 (86h) ..... RW

7 SeqID Value in Graphics Engine Packets ..... **default = 1**

6 Set Isoc When VPRI=1 in Graphics Engine Packet
0 Disable ..... default
1 Enable

5 Always Set Isoc in Graphics Engine Packet
0 Disable ..... default
1 Enable

4 VPRI for Graphics Engine As High Priority Arbitration
(independent of bits 5 and 6)
0 Disable ..... default
1 Enable

3 Set Isoc When VDPHPRI=1 in AGP Isochronous Video Display Packet
0 Disable ..... default
1 Enable

2 Always Set Isoc in AGP Isochronous Video Display Packet
0 Disable
1 Enable **..... default**

1 VDPHPRI for AGP Isochronous Video Display As High Priority Arbitration
(independent of Isoc setting)
0 Disable
1 Enable **..... default**

0 GPRI for AGP ADS As High Priority Arbitration
(independent of RxA1 bits 3 and 5)
0 Disable ..... default
1 Enable

Offset A8 – HyperTransport Control 2 (7Fh) ..... RW

7 PCI Master SIO for PCI Master ADS As High Priority Arbitration
0 Disable ..... default
1 Enable

6 Force AGP ADS Read Command Pass PCI Master ADS Write Command When Post Write Channel Is Full But Read Channel Is Available
0 Disable
1 Enable **..... default**

5 Force PCI Master ADS Read Command Pass AGP ADS Write Command When Post Write Channel Is Full But Read Channel Is Available
0 Disable
1 Enable **..... default**

4 Force AGP Isochronous Video Display Read Command Pass VADS Write Command When Post Write Channel Is Full But Read Channel Is Available
0 Disable
1 Enable **..... default**

3 Force Graphics Engine Write Command Pass AGP Isochronous Video Display Low Priority Read Command When Non-Post Write Channel Is Full But Post Write Is Available
0 Disable
1 Enable **..... default**

2 PCI Master Request for PCI Master ADS As Parking Request
0 Disable
1 Enable **..... default**

1 AGP Master Request for AGP ADS As Parking Request
0 Disable
1 Enable **..... default**

0 Video Display Request for AGP Isochronous Video Display As Parking Request
0 Disable
1 Enable **..... default**

Offset A9 – HyperTransport Control 3 (CFh) ..... RW

7 Video Request for Graphics Engine As Parking Request
0 Disable
1 Enable **..... default**

6-4 PCI Master ADS Read Merge Timer .... def = 100b
(for waiting for the next request)

3-0 PCI Master ADS Write Merge Timer . def = 1111b
(for waiting for the next request)

Offset AA – Transmit Data Drive Control (22h).....RW

7 **Data Coarse Delay Control** ..... default = 0
6-4 **Data Pullup Drive Strength** ..... **default = 010b**
3 **Reserved** ..... always reads 0
2-0 **Data Pulldown Drive Strength**..... **default = 010b**

Offset AB – Transmit Clock Drive Control (22h) .....RW

7 **Clock Coarse Delay Control** ..... default = 0
6-4 **Clock Pullup Drive Strength**..... **default = 010b**
3 **Reserved** ..... always reads 0
2-0 **Clock Pulldown Drive Strength**..... **default = 010b**

Offset AC – Transmit Autocomp Result (00h) .....RW

7 **Transmitter Autocomp Select**
0 Manual .....default
1 Automatic
6-4 **Transmit Data / Clock Pullup Drive Strength from Autocomp** ..... **RO**, default = 000b
3 **Reserved** ..... always reads 0
2-0 **Transmit Data / Clock Pulldown Drive Strength from Autocomp** ..... **RO**, default = 000b

Offset AD – HT Controller Misc Control (00h).....RW

7-6 **Read Response Buffer Release Delay**
00 No Delay .....default
01 Delay 1T
10 Delay 2T
11 Delay 3T
5 **SeqID Value for AGP Isochronous Video Display**
0 SeqID = 0 .....default
1 SeqID = 1
4-0 **Reserved** .....**RW**, default = 0

Offset AE – Receive Termination Value Control (22h). RW

7 **Termination Value Autocomp Select**..... default = 0
6-4 **Receive Data Termination Value** ..... **default = 010b**
3 **Reserved** ..... always reads 0
2-0 **Receive Clock Termination Value** ... **default = 010b**

Offset AF – Rcv Termination Autocomp Status (00h) .. RW

7 **Reserved** ..... always reads 0
6-4 **Receive Data / Clock Termination Autocomp Value** ..... **RO**, default = 000b
3 **DB4 Receive Clock Delay .... default set per ROMSIP[47]**
0 1T ..... default
1 2T
2-0 **Transmit PLL Feedback Delay Fine Tune..... ..... default set per ROMSIP[46:44]**
000 Lead by 100 picoseconds..... default
001 Align
010 Lag by 100 picoseconds
011 Lag by 200 picoseconds
1xx -reserved-

Offset B0 – Response Flow Control Buffer Depth (84h) RW

7-4 Flow Control Buffer Depth for Response Command / Data ..... default = 1000b (8 levels)

3-0 Flow Control Buffer Depth for Non-Posted Command / Data ..... default = 0100b (4 levels)

Offset B1 – Receive Post-Write Buffer Depth (15h).....RW

7 AGP Controller Interface (External AGP)
- 0 133 MHz Asynchronous .....default
- 1 133 MHz Pseudo-Asynchronous

(integrated graphics is 160 / 200 MHz async)

6 Value of PassPW Bit in AGP Upstream Request Packet ..... default = 0

5 Value of Sequence ID in PCI Master / AGP Upstream Request Packet ..... default = 0

4 CPU-to=PCI Response Packet Isoc Bit
- 0 Always clear
- 1 Same as corresponding request packet**..... def**

3-0 Receive Post Write Buffer Depth

(programmed value will only take effect after warm boot)
- 0000 -not allowed-
- 0001 Minimum value
- … …
- 0101 Maximum value .....default
- 011x -not allowed-
- 1xxx -not allowed-

Offset B2 – TPM Control (00h) ..... RW

7 Ignore CPU-to-PCI Accesses to Addresses FED4 4000 through FED4 FFFF (TPM Reserved Range)
- 0 Disable..... default
- 1 Enable

6 TPM Special Command Decoding
- 0 Disable..... default
- 1 Enable

5 Protect Start Address 00 FED4 4020, 00FED4 4024 and 00 FED4 4028 in MMIO Range with Command Length of 1DW
- 0 Disable..... default
- 1 Enable

4 Forward TPM Special Commands to V-Link By I/O Commands
- 0 Disable..... default
- 1 Enable

3-0 Reserved .....always reads 0

Offset B4 – AGP Master Isoc Request Timer (03h).....RW

7-4 HT Controller AGP Master Isochronous Request Timer ..... default = 0
(programmed in units of 16 HT clocks)

3-2 HT Controller Parking Arbitration for PCI / AGP / AGP Isochronous Requests
- 00 Park at previous bus .....default
- 01 Park at PCI Master
- 10 Park at AGP Master
- 11 Park at AGP Isochronous Request

1 AGP FIFO Data Depth
- 0 64 QW.....default
- 1 128 QW

0 Fast Write Data Depth
- 0 16 QW.....default
- 1 32 QW

Offset B5 – PCI Master Timer (00h) .....RW

7-4 HT Controller PCI Master Timer ..... def = 0
(programmed in units of 16 HT clocks)

3-0 HT Ctrlr PCI Master Promotion Timer..... def = 0
(programmed in units of 16 HT clocks)

Offset B6 – AGP Master Timer (00h).....RW

7-4 HT Controller AGP Master Timer ..... def = 0
(programmed in units of 16 HT clocks)

3-0 HT Ctrlr AGP Master Promotion Timer .... def = 0
(programmed in units of 16 HT clocks)

Offset B7 – AGP Master Isochronous Request High Priority Timer (00h) .....RW

7-0 HT Controller AGP Master Isochronous Request High Priority Timer..... default = 00h
(programmed in units of 16 HT clocks)

Offset C0 – HT Transmit CAD[7:0], Control Rise / Fall Delay (00h) ..... RW

7-6 Positive Data Signal Rise Delay.....def = 0
5-4 Positive Data Signal Fall Delay .....def = 0
3-2 Negative Data Signal Rise Delay .....def = 0
1-0 Negative Data Signal Fall Delay.....def = 0

Offset C1 – HT Transmit Clock0 Rise/Fall Delay (00h) RW

7-6 Positive Clock Signal Rise Delay.....def = 0
5-4 Positive Clock Signal Fall Delay .....def = 0
3-2 Negative Clock Signal Rise Delay .....def = 0
1-0 Negative Clock Signal Fall Delay.....def = 0

Offset C2 – HT Transmit CAD[15:8] R/F Delay (00h).. RW

7-6 Positive Data Signal Rise Delay.....def = 0
5-4 Positive Data Signal Fall Delay .....def = 0
3-2 Negative Data Signal Rise Delay .....def = 0
1-0 Negative Data Signal Fall Delay.....def = 0

Offset C3 – HT Transmit Clock1 Rise/Fall Delay (00h) RW

7-6 Positive Clock Signal Rise Delay.....def = 0
5-4 Positive Clock Signal Fall Delay .....def = 0
3-2 Negative Clock Signal Rise Delay .....def = 0
1-0 Negative Clock Signal Fall Delay.....def = 0

Offset C4 – HT Receive CAD[7:0], Control, Clock 0 Rise / Fall Delay (00h) ..... RW

7-6 Data Input Rise Delay.....def = 0
5-4 Data Input Fall Delay.....def = 0
3-2 Clock Input Rise Delay .....def = 0
1-0 Clock Input Fall Delay.....def = 0

Offset C5 – HT Receive CAD[15:8], Clock 1 Rise / Fall Delay (00h) ..... RW

7-6 Data Input Rise Delay.....def = 0
5-4 Data Input Fall Delay.....def = 0
3-2 Clock Input Rise Delay .....def = 0
1-0 Clock Input Fall Delay.....def = 0

Device 0 Function 3 Registers – DRAM

Device 0 Function 3 Header Registers

All registers are located in PCI configuration space. They should be programmed using PCI configuration mechanism 1 through CF8 / CFC with bus number and device number equal to zero and function number equal to 3.

Offset 1-0 - Vendor ID (1106h) ..... RO

15-0 ID Code (reads 1106h to identify VIA Technologies)

Offset 3-2 - Device ID (3204h) ..... RO

15-0 ID Code (reads 3204h to identify K8M800 NB virtual device function 3)

Offset 5-4 –Command (0006h) ..... RW

15-10 Reserved ..... always reads 0

9 Fast Back-to-Back Cycle Enable ..... RO
- 0 Fast back-to-back transactions only allowed to the same agent.....default
- 1 Fast back-to-back transactions allowed to different agents

8 SERR# Enable..... RO
- 0 SERR# driver disabled.....default
- 1 SERR# driver enabled

(SERR# is used to report ECC errors).

7 Address / Data Stepping..... RO
- 0 Device never does stepping.....default
- 1 Device always does stepping

6 Parity Error Response.....RW
- 0 Ignore parity errors & continue.....default
- 1 Take normal action on detected parity errors

5 VGA Palette Snoop..... RO
- 0 Treat palette accesses normally.....default
- 1 Don't respond to palette accesses on PCI bus

4 Memory Write and Invalidate Command ..... RO
- 0 Bus masters must use Mem Write.....default
- 1 Bus masters may generate Mem Write & Inval

3 Special Cycle Monitoring..... RO
- 0 Does not monitor special cycles.....default
- 1 Monitors special cycles

2 PCI Bus Master..... RO
- 0 Never behaves as a bus master
- 1 Can behave as a bus master.....default

1 Memory Space..... RO
- 0 Does not respond to memory space
- 1 Responds to memory space.....default

0 I/O Space ..... RO
- 0 Does not respond to I/O space .....default
- 1 Responds to I/O space

Offset 7-6 – Status (0200h)..... RWC

15 Detected Parity Error
- 0 No parity error detected..... default
- 1 Error detected in either address or data phase. This bit is set even if error response is disabled (command register bit-6). ..... write one to clear

14 Signaled System Error (SERR# Asserted)
..... always reads 0

13 Signaled Master Abort
- 0 No abort received ..... default
- 1 Transaction aborted by the master .... write one to clear

12 Received Target Abort
- 0 No abort received ..... default
- 1 Transaction aborted by the target .... write one to clear

11 Signaled Target Abort ..... always reads 0
- 0 Target Abort never signaled

10-9 DEVSEL# Timing
- 00 Fast
- 01 Medium ..... always reads 01
- 10 Slow
- 11 Reserved

8 Data Parity Error Detected
- 0 No data parity error detected ..... default
- 1 Error detected in data phase. Set only if error response enabled via command bit-6 = 1 and the North Bridge was initiator of the operation in which the error occurred... write one to clear

7 Fast Back-to-Back Capable ..... always reads 0

6 User Definable Features..... always reads 0

5 66MHz Capable..... always reads 0

4 Supports New Capability list..... always reads 0

3-0 Reserved ..... always reads 0

Offset 8 - Revision ID (0nh) ..... RO

9-0 Chip Revision Code..... always reads 0nh

Offset 9 - Programming Interface (00h) ..... RO

7-0 Interface Identifier ..... always reads 00h

Offset A - Sub Class Code (00h)..... RO

7-0 Sub Class Code ..... reads 00 to indicate Host Bridge

Offset B - Base Class Code (06h)..... RO

7-0 Base Class Code.. reads 06 to indicate Bridge Device

Device 0 Function 3 Device-Specific Registers

These registers are normally programmed once at system initialization time.

DRAM Control

Offset 47 – DRAM End Address (HA[31:24]) (01h).....RW

Table 7. System Memory Map

Space	Start	Size	Address Range	Comment
DOS	0	640K	00000000-0009FFFF	Cacheable
VGA	640K	128K	000A0000-000BFFFF	Used for SMM
BIOS	768K	16K	000C0000-000C3FFF	Shadow Ctrl 1
BIOS	784K	16K	000C4000-000C7FFF	Shadow Ctrl 1
BIOS	800K	16K	000C8000-000CBFFF	Shadow Ctrl 1
BIOS	816K	16K	000CC000-000CFFFF	Shadow Ctrl 1
BIOS	832K	16K	000D0000-000D3FFF	Shadow Ctrl 2
BIOS	848K	16K	000D4000-000D7FFF	Shadow Ctrl 2
BIOS	864K	16K	000D8000-000DBFFF	Shadow Ctrl 2
BIOS	880K	16K	000DC000-000DFFFF	Shadow Ctrl 2
BIOS	896K	64K	000E0000-000EFFFF	Shadow Ctrl 3
BIOS	960K	64K	000F0000-000FFFFF	Shadow Ctrl 3
Sys	1MB	—	00100000-DRAM Top	Can have hole
Bus	D Top		DRAM Top-FFFEFFFF	
Init	4G-64K	64K	FFFEFFFF-FFFFFFFF	000Fxxxx alias

Timer Control

Offset 70 – PCI Timer (00h) ..... RW

7-4 **PCI Promotion Timer** ..... def = 0
(programmed in units of 8 HT clocks)

3-0 **PCI Timeout Timer** ..... def = 0
(programmed in units of 16 HT clocks)

Offset 71 – AGP Timer (00h)..... RW

7-4 **AGP Promotion Timer** ..... def = 0
(programmed in units of 8 HT clocks)

3-0 **AGP Timeout Timer** ..... def = 0
(programmed in units of 16 HT clocks)

Offset 72 – VGA Timer (00h) ..... RW

7-4 **VGA Promotion Timer** ..... def = 0
(programmed in units of 8 HT clocks)

3-0 **VGA Timeout Timer** ..... def = 0
(programmed in units of 16 HT clocks)

Offset 73 – High Priority Display Timer (00h)..... RW

7-0 **High Priority Display Timer** ..... def = 0
(programmed in units of 16 HT clocks)

Offset 74 – Low Priority Display Timer (00h) ..... RW

7-4 **Reserved** ..... always reads 0

3-0 **Low Priority Display Timer** ..... def = 0
(programmed in units of 16 HT clocks)

ROM Shadow Control

Offset 80 - Shadow RAM Control 1 (00h).....RW

7-6 CC000h-CFFFFh
- 00 Read/write disable.....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

5-4 C8000h-CBFFFh
- 00 Read/write disable.....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

3-2 C4000h-C7FFFh
- 00 Read/write disable.....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

1-0 C0000h-C3FFFh
- 00 Read/write disable.....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

Offset 81 - Shadow RAM Control 2 (00h).....RW

7-6 DC000h-DFFFFh
- 00 Read/write disable.....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

5-4 D8000h-DBFFFh
- 00 Read/write disable.....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

3-2 D4000h-D7FFFh
- 00 Read/write disable.....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

1-0 D0000h-D3FFFh
- 00 Read/write disable.....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

Offset 82 - Shadow RAM Control 3 (00h) ..... RW

7-6 E0000h-EFFFFh
- 00 Read/write disable ..... default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

5-4 F0000h-FFFFFh
- 00 Read/write disable ..... default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

3-2 Memory Hole
- 00 None ..... default
- 01 512K-640K
- 10 15M-16M (1M)
- 11 14M-16M (2M)

1 Disable A,BK SMRAM Direct Access

0 Enable A,BK DRAM Access

SMI Mapping Control:

Bits	SMM		Non-SMM	
1-0	Code	Data	Code	Data
00	DRAM	DRAM	PCI	PCI
01	DRAM	DRAM	DRAM	DRAM
10	DRAM	PCI	PCI	PCI
11	DRAM	DRAM	DRAM	DRAM

SMM / APIC Control

Offset 86 – SMM / APIC Decoding (01h) ..... RW

7-6 Reserved .....always reads 0

5 APIC Lowest Interrupt Arbitration
- 0 Disable..... default
- 1 Enable

4 I/O APIC Decoding
- 0 FECxxxxx accesses go to PCI..... default
- 1 FEC00000 to FEC7FFFF accesses go to PCI
  FEC80000 to FECFFFFF accesses go to AGP

3 MSI (Processor Message) Support
- 0 Disable (master access to FEExxxxx will go to PCI) ..... default
- 1 Enable (master access to FEExxxxx will be passed to host side to do snoop)

2 Top SMM
- 0 Disable..... default
- 1 Enable

1 Reserved .....always reads 0

0 Compatible SMM
- 0 Disable
- 1 Enable**..... default**

UMA Control

Offset A0 – CPU Direct Access FB Base Address (00h).RW

7-1 CPU Direct Access FB Address [27:21] ..... def = 0

0 CPU Direct Access FB

0 Disable .....default

1 Enable

Offset A1 – CPU Direct Access FB Size (00h).....RW

7 VGA

0 Disable .....default

1 Enable

6-4 CPU Direct Access FB Size ..... def = 0

000 None .....default

001 2MB

010 4MB

011 8MB

100 16MB

101 32 MB

11x -reserved-

3-0 CPU Direct Access FB Address [31:28] ..... def = 0

Offset A2 – VGA Timer (00h).....RW

7-4 Reserved ..... always reads 0

3-0 VGA Timer ..... def = 0

(programmed in units of 16 dot clocks)

Offset A4 – FIFO / Flow Control 1 (00h)..... RW

7-6 DBX AGP FIFO and Video Display FIFO Depth

00 AGP FIFO = 64QW, Vid FIFO = 64 QW ... def

01 AGP FIFO = 32 QW, Vid FIFO = 96 QW

10 AGP FIFO = 96 QW, Vid FIFO = 32 QW

11 AGP FIFO = 128 QW, Vid FIFO = 0 QW

5 AGP Interrupt Destination

0 AGP Interrupt to HT Controller ..... default

1 AGP Interrupt to DRAM Controller

4 DRAM Controller Mode

0 Synchronous ..... default

1 Asynchronous (not 166 MHz)

3 Sync 1T From DRAM Controller or DBX to Graphics

0 Disable..... default

1 Enable

2 Sync 1T From DRAM Controller to DBX (Async Mode Only)

0 Disable..... default

1 Enable

1 Merge Graphics Read Address Bit-4 From 1 to 0

0 Don't Merge ..... default

1 Merge

0 Merge Graphics Write Address Bit-4 From 1 to 0

0 Don't Merge ..... default

1 Merge

Offset A5 – FIFO / Flow Control 2 (20h)..... RW

7 DBX Daa Sync

0 No sync..... default

1 Data sync 1T from DBX to internal AGP

6 IntegratedGraphics Controller Clock Frequency (see also bit-0)

0 200 MHz..... default

1 166 MHz

5 IntegratedGraphics Controller Merge Control

0 Only 4 QW-aligned requests can be merged

1 4/8 QW-aligned requests can be merged..... **..... default**

4 Integrated Graphics Controller Read Data Queue

0 64 QW ..... default

1 128 QW

3 Integrated Graphics Controller Clock Frequency

0 Frequcy selected per bit-6 ..... default

1 133 MHz

2-0 Reserved ..... **RW**, default = 0

Device 0 Function 4 Registers – Power Management

Device 0 Function 4 Header Registers

All registers are located in PCI configuration space. They should be programmed using PCI configuration mechanism 1 through CF8 / CFC with bus number and device number equal to zero and function number equal to 4.

Offset 1-0 - Vendor ID (1106h) ..... RO

15-0 ID Code (reads 1106h to identify VIA Technologies)

Offset 3-2 - Device ID (4204h) ..... RO

15-0 ID Code (reads 4204h to identify K8M800 NB virtual device function 4)

Offset 5-4 –Command (0006h) ..... RW

15-10 Reserved ..... always reads 0

9 Fast Back-to-Back Cycle Enable ..... RO
- 0 Fast back-to-back transactions only allowed to the same agent.....default
- 1 Fast back-to-back transactions allowed to different agents

8 SERR# Enable..... RO
- 0 SERR# driver disabled.....default
- 1 SERR# driver enabled

(SERR# is used to report ECC errors).

7 Address / Data Stepping..... RO
- 0 Device never does stepping.....default
- 1 Device always does stepping

6 Parity Error Response.....**RW**
- 0 Ignore parity errors & continue.....default
- 1 Take normal action on detected parity errors

5 VGA Palette Snoop..... RO
- 0 Treat palette accesses normally.....default
- 1 Don't respond to palette accesses on PCI bus

4 Memory Write and Invalidate Command ..... RO
- 0 Bus masters must use Mem Write.....default
- 1 Bus masters may generate Mem Write & Inval

3 Special Cycle Monitoring..... RO
- 0 Does not monitor special cycles.....default
- 1 Monitors special cycles

2 PCI Bus Master..... RO
- 0 Never behaves as a bus master
- 1 Can behave as a bus master.....default

1 Memory Space..... RO
- 0 Does not respond to memory space
- 1 Responds to memory space.....default

0 I/O Space ..... RO
- 0 Does not respond to I/O space .....default
- 1 Responds to I/O space

Offset 7-6 – Status (0200h)..... RWC

15 Detected Parity Error
- 0 No parity error detected..... default
- 1 Error detected in either address or data phase. This bit is set even if error response is disabled (command register bit-6). ..... write one to clear

14 Signaled System Error (SERR# Asserted) .....always reads 0

13 Signaled Master Abort
- 0 No abort received ..... default
- 1 Transaction aborted by the master .... write one to clear

12 Received Target Abort
- 0 No abort received ..... default
- 1 Transaction aborted by the target .... write one to clear

11 Signaled Target Abort .....always reads 0
- 0 Target Abort never signaled

10-9 DEVSEL# Timing
- 00 Fast
- 01 Medium .....always reads 01
- 10 Slow
- 11 Reserved

8 Data Parity Error Detected
- 0 No data parity error detected ..... default
- 1 Error detected in data phase. Set only if error response enabled via command bit-6 = 1 and the North Bridge was initiator of the operation in which the error occurred... write one to clear

7 Fast Back-to-Back Capable.....always reads 0

6 User Definable Features.....always reads 0

5 66MHz Capable.....always reads 0

4 Supports New Capability list.....always reads 0

3-0 Reserved .....always reads 0

Offset 8 - Revision ID (0nh) ..... RO

10-0 Chip Revision Code.....always reads 0nh

Offset 9 - Programming Interface (00h) ..... RO

7-0 Interface Identifier.....always reads 00h

Offset A - Sub Class Code (00h)..... RO

7-0 Sub Class Code.....reads 00 to indicate Host Bridge

Offset B - Base Class Code (06h)..... RO

7-0 Base Class Code..reads 06 to indicate Bridge Device

Device 0 Function 4 Device-Specific Registers

These registers are normally programmed once at system initialization time.

Power Management Control

Offset A0 – Power Management Mode (00h).....RW

7 Dynamic Power Management
- 0 Disable .....default
- 1 Enable

6 Halt / Shutdown Power Management
- 0 Disable .....default
- 1 Enable

5 Stop Clock Power Management
- 0 Disable .....default
- 1 Enable

4 Suspend Status Power Management
- 0 Disable .....default
- 1 Enable

3-0 Reserved ..... always reads 0

Offset A2 – Dynamic Clock Stop Control (00h) .....RW

7 Host Interface Power Management
- 0 Disable .....default
- 1 Enable

6 Reserved ..... always reads 0

5 V-Link Interface Power Management
- 0 Disable .....default
- 1 Enable

4 AGP Interface Power Management
- 0 Disable .....default
- 1 Enable

3 PCI #2 Interface Power Management
- 0 Disable .....default
- 1 Enable

2 Graphics Interface Power Management
- 0 Disable .....default
- 1 Enable

1 Reserved ..... always reads 0

0 Host Fast Power Management (DADS Fast Timing)
- 0 Disable .....default
- 1 Enable

BIOS Scratch

Offset D0-EF – BIOS Scratch Registers ..... RW

7-0 No hardware function ..... default = 0

Device 0 Function 7 Registers – V-Link

Device 0 Function 7 Header Registers

All registers are located in PCI configuration space. They should be programmed using PCI configuration mechanism 1 through CF8 / CFC with bus number and device number equal to zero and function number equal to 7.

Offset 1-0 - Vendor ID (1106h) ..... RO

15-0 ID Code (reads 1106h to identify VIA Technologies)

Offset 3-2 - Device ID (7204h) ..... RO

15-0 ID Code ..... always reads 7204h

Offset 5-4 –Command (0006h) ..... RW

15-10 Reserved ..... always reads 0

9 Fast Back-to-Back Cycle Enable ..... RO
- 0 Fast back-to-back transactions only allowed to the same agent ..... default
- 1 Fast back-to-back transactions allowed to different agents

8 SERR# Enable ..... RO
- 0 SERR# driver disabled ..... default
- 1 SERR# driver enabled

(SERR# is used to report ECC errors).

7 Address / Data Stepping ..... RO
- 0 Device never does stepping ..... default
- 1 Device always does stepping

6 Parity Error Response ..... RW
- 0 Ignore parity errors & continue ..... default
- 1 Take normal action on detected parity errors

5 VGA Palette Snoop ..... RO
- 0 Treat palette accesses normally ..... default
- 1 Don't respond to palette accesses on PCI bus

4 Memory Write and Invalidate Command ..... RO
- 0 Bus masters must use Mem Write ..... default
- 1 Bus masters may generate Mem Write & Inval

3 Special Cycle Monitoring ..... RO
- 0 Does not monitor special cycles ..... default
- 1 Monitors special cycles

2 PCI Bus Master ..... RO
- 0 Never behaves as a bus master
- 1 Can behave as a bus master ..... default

1 Memory Space ..... RO
- 0 Does not respond to memory space
- 1 Responds to memory space ..... default

0 I/O Space ..... RO
- 0 Does not respond to I/O space ..... default
- 1 Responds to I/O space

Offset 7-6 – Status (0200h) ..... RWC

15 Detected Parity Error
- 0 No parity error detected ..... default
- 1 Error detected in either address or data phase. This bit is set even if error response is disabled (command register bit-6). ..... write one to clear

14 Signaled System Error (SERR# Asserted) ..... always reads 0

13 Signaled Master Abort
- 0 No abort received ..... default
- 1 Transaction aborted by the master ..... write one to clear

12 Received Target Abort
- 0 No abort received ..... default
- 1 Transaction aborted by the target ..... write one to clear

11 Signaled Target Abort ..... always reads 0
- 0 Target Abort never signaled

10-9 DEVSEL# Timing
- 00 Fast
- 01 Medium ..... always reads 01
- 10 Slow
- 11 Reserved

8 Data Parity Error Detected
- 0 No data parity error detected ..... default
- 1 Error detected in data phase. Set only if error response enabled via command bit-6 = 1 and the North Bridge was initiator of the operation in which the error occurred... write one to clear

7 Fast Back-to-Back Capable ..... always reads 0

6 User Definable Features ..... always reads 0

5 66MHz Capable ..... always reads 0

4 Supports New Capability list ..... always reads 0

3-0 Reserved ..... always reads 0

Offset 8 - Revision ID (0nh) ..... RO

11-0 Chip Revision Code ..... always reads 0nh

Offset 9 - Programming Interface (00h) ..... RO

7-0 Interface Identifier ..... always reads 00h

Offset A - Sub Class Code (00h) ..... RO

7-0 Sub Class Code ..... reads 00 to indicate Host Bridge

Offset B - Base Class Code (06h) ..... RO

7-0 Base Class Code .. reads 06 to indicate Bridge Device

Device 0 Function 7 Device-Specific Registers

These registers are normally programmed once at system initialization time.

V-Link Control

Offset 40 – V-Link Specification ID (00h).....RO

7-0 Specification Revision..... always reads 00

Offset 41 – NB V-Link Capability (19h).....WC

7 V-Link Parity Error Detected by NB.....WC
- 0 No V-Link Parity Error Detected.....default
- 1 V-Link Parity Error Detected (write 1 to clear)

6 Reserved ..... always reads 0

5 16-bit Bus Width Supported by NB .....RO
- 0 Not Supported .....default
- 1 Supported

4 8-Bit Bus Width Supported by NB.....RO
- 0 Not Supported
- 1 Supported **.....default**

3 4x Rate Supported by NB.....RO
- 0 Not Supported
- 1 Supported **.....default**

2 2x Rate Supported by NB.....RO
- 0 Not Supported .....default
- 1 Supported

1 Reserved ..... always reads 0

0 8x Rate Supported by NB.....RO
- 0 Not Supported
- 1 Supported **.....default**

Offset 42 – NB Downlink Command (88h) .....RW

7-4 DnCmd Max Request Depth (0=1 DnCmd).. def = 8

3-0 DnCmd Write Buffer Size (doublewords)..... def = 8

Offset 43 – NB Uplink Max Req Depth (80h) .....RO

7-4 UpCmd Max Request Depth (0=1 UpCmd).. def = 8
Indicates the maximum allowable number of outstanding UPCMD requests

3-0 Reserved ..... always reads 0

Offset 44 – NB Uplink Buffer Size (82h) .....RO

7-4 UpCmd P2C Write Buffer Size (max lines).. def = 8

3-0 UpCmd P2P Write Buffer Size (max lines).. def = 2

Offset 45 –NB V-Link Bus Timer (44h)..... RW

7-4 Timer for Normal Priority Requests from SB
- 0000 Immediate
- 0001 1*4 VCLKs
- 0010 2*4 VCLKs
- 0011 3*4 VCLKs
- 0100 4*4 VCLKs..... default
- 0101 5*4 VCLKs
- 0110 6*4 VCLKs
- 0111 7*4 VCLKs
- 1000 8*4 VCLKs
- 1001 16*4 VCLKs
- 1010 32*4 VCLKs
- 1011 64*4 VCLKs
- 11xx Own the bus for as long as there is a request

3-0 Timer for High Priority Requests from SB
- 0000 Immediate
- 0001 1*2 VCLKs
- 0010 2*2 VCLKs
- 0011 3*2 VCLKs
- 0100 4*2 VCLKs..... default
- 0101 5*2 VCLKs
- 0110 6*2 VCLKs
- 0111 7*2 VCLKs
- 1000 8*2 VCLKs
- 1001 16*2 VCLKs
- 1010 32*2 VCLKs
- 1011 64*2 VCLKs
- 11xx Own the bus for as long as there is a request

Offset 46 – NB V-Link Misc Control (00h) ..... RW

7 Downstream High Priority
- 0 Disable High Priority Down Commands .....def
- 1 Enable High Priority Down Commands

6 Downlink Priority
- 0 Treat Downlink Cycles as Normal Priority.def
- 1 Treat Downlink Cycles as High Priority

5-4 Combine Multiple STPGNT Cycles Into One V-Link Command
- 00 Compatible, 1 command per V-Link cmd....def
- 01 2 commands per V-Link command
- 10 3 commands per V-Link command
- 11 4 commands per V-Link command

3-2 V-Link Master Access Ordering Rules
- 00 High priority read, pass normal read (not pass write) .....default
- 01 Read (high/normal) pass write (HR>LR>W)
- 1x Read / write in order

1-0 Reserved ..... always reads 0

Offset 47 – V-Link Control (00h) ..... RW

7 Parity Error or SERR# Reported via NMI
- 0 Disable .....default
- 1 Enable

6 Parity Error or SERR# Reported to SB via Vlink
- 0 Disable .....default
- 1 Enable

5 C2P Read L1 Ready Return Timing
- 0 V-Link bus decodes C2P Read Ack cmd.....def
- 1 Wait till previous P2C write cycles all flushed

4 Reserved ..... always reads 0

3 Down Strobe Dynamic Stop
- 0 Disable .....default
- 1 Enable

2 Auto-Disconnect
- 0 Disable .....default
- 1 Enable

1 V-Link Disconnect Cycle for HALT Cycle
- 0 Disable .....default
- 1 Enable

0 V-Link Disconnect Cycle for STPGNT Cycle
- 0 Disable .....default
- 1 Enable

Offset 48 – NB/SB V-Link Configuration (18h) ..... RW

7 V-Link Parity Check
- 0 Disable..... default
- 1 Enable

6 Rest Bus Width Supported
- 0 Not Supported..... default
- 1 Supported

5 16-bit Bus Width Supported
- 0 Not Supported..... default
- 1 Supported

4 8-Bit Bus Width Supported
- 0 Not Supported
- 1 Supported **..... default**

3 4x Rate Supported
- 0 Not Supported
- 1 Supported **..... default**

2 2x Rate Supported
- 0 Not Supported..... default
- 1 Supported

1 Reserved .....always reads 0

0 8x Rate Supported
- 0 Not Supported..... default
- 1 Supported

Offset 49 – SB V-Link Capability (19h) ..... RO

7-6 Reserved .....always reads 0

5 16-bit Bus Width Supported by SB
- 0 Not Supported..... default
- 1 Supported

4 8-Bit Bus Width Supported by SB
- 0 Not Supported
- 1 Supported **..... default**

3 4x Rate Supported by SB
- 0 Not Supported
- 1 Supported **..... default**

2 2x Rate Supported by SB
- 0 Not Supported..... default
- 1 Supported

1 Reserved .....always reads 0

0 8x Rate Supported by SB
- 0 Not Supported
- 1 Supported **..... default**

Offset 4A – SB Downlink Status (88h) .....RO

7-4 DnCmd Max Request Depth (0=1 DnCmd).. def = 8
3-0 DnCmd Write Buffer Size (doublewords)..... def = 8

Offset 4B – SB Uplink Command (80h) .....RW

7-4 UpCmd Max Request Depth (0=1 UpCmd).. def = 8
Indicates the maximum allowable number of outstanding UPCMD requests
3-0 Reserved ..... always reads 0

Offset 4C – SB Uplink Command (82h).....RW

7-4 UpCmd P2C Write Buffer Size (max lines).. def = 8
3-0 UpCmd P2P Write Buffer Size (max lines).. def = 2

Offset 4D – SB V-Link Bus Timer (44h) .....RW

7-4 Timer for Normal Priority Requests from NB
0000 Immediate
0001 1*4 VCLKs
0010 2*4 VCLKs
0011 3*4 VCLKs
0100 4*4 VCLKs .....default
0101 5*4 VCLKs
0110 6*4 VCLKs
0111 7*4 VCLKs
1000 8*4 VCLKs
1001 16*4 VCLKs
1010 32*4 VCLKs
1011 64*4 VCLKs
11xx Own the bus for as long as there is a request

3-0 Timer for High Priority Requests from NB
0000 Immediate
0001 1*2 VCLKs
0010 2*2 VCLKs
0011 3*2 VCLKs
0100 4*2 VCLKs .....default
0101 5*2 VCLKs
0110 6*2 VCLKs
0111 7*2 VCLKs
1000 8*2 VCLKs
1001 16*2 VCLKs
1010 32*2 VCLKs
1011 64*2 VCLKs
11xx Own the bus for as long as there is a request

Offset 4E – CCA Master Priority (00h)..... RW

7 1394 High Priority
0 Low priority..... default
1 High priority
6 LAN / NIC High Priority
0 Low priority..... default
1 High priority
5 Reserved .....always reads 0
4 USB High Priority
0 Low priority..... default
1 High priority
3 Reserved .....always reads 0
2 IDE High Priority
0 Low priority..... default
1 High priority
1 AC97-ISA High Priority
0 Low priority..... default
1 High priority
0 PCI High Priority
0 Low priority..... default
1 High priority

Offset 4F – SB V-Link Misc Control (00h)..... RW

7 Upstream Command High Priority
0 Disable high priority up commands..... default
1 Enable high priority up commands
6-4 Reserved .....always reads 0
3 Up Strobe Dynamic Stop
0 Disable..... default
1 Enable
2-1 Reserved .....always reads 0
0 Down Cycle Wait for Up Cycle Write Flush (Except Down Cycle Post Write)
0 Disable..... default
1 Enable

PCI Bus Control

These registers are normally programmed once at system initialization time.

Offset 70 - PCI Buffer Control (00h).....RW

7 CPU to PCI Post-Write
- 0 Disable .....default
- 1 Enable

6 Reserved ..... always reads 0

5-4 PCI Master to DRAM Prefetch
- 00 Always prefetch .....default
- x1 Never prefetch
- 10 Prefetch only for Enhance command

3 Reserved ..... always reads 0

2 PCI Master Read Buffering
- 0 Disable .....default
- 1 Enable

1 Delay Transaction
- 0 Disable .....default
- 1 Enable

0 Reserved ..... always reads 0

Offset 71 - CPU to PCI Flow Control (48h) .....RWC

7 Retry Status.....RWC
- 0 No retry occurred .....default
- 1 Retry occurred

6 Retry Timeout Action
- 0 Retry forever (record status only)
- 1 Flush buffer or return FFFFFFFFh for reads .....default

5-4 Retry Count and Retry Backoff
- 00 Retry 2 times, backoff CPU .....default
- 01 Retry 16 times
- 10 Retry 4 times
- 11 Retry 64 times

3 PCI Burst
- 0 Disable
- 1 Enable .....default

2 Reserved ..... always reads 0

1 Compatible Type#1 Configuration Cycles
- 0 Disable (fixed AD31).....default
- 1 Enable

0 IDSEL Control
- 0 AD11, AD12 .....default
- 1 AD30, AD31

Offset 73 - PCI Master Control (00h) ..... RW

7 Reserved .....always reads 0

6 PCI Master 1-Wait-State Write
- 0 Zero wait state TRDY# response..... default
- 1 One wait state TRDY# response

5 PCI Master 1-Wait-State Read
- 0 Zero wait state TRDY# response..... default
- 1 One wait state TRDY# response

4 WSC#
- 0 Disable..... default
- 1 Enable

3-1 Reserved .....always reads 0

0 PCI Master Broken Timer Enable
- 0 Disable..... default
- 1 Enable. Force into arbitration when there is no FRAME# 16 PCICLK's after the grant.

Offset 75 - PCI Arbitration 1 (00h).....RW

7 Arbitration Mode
- 0 REQ-based (arbitrate at end of REQ#) ..default
- 1 Frame-based (arbitrate at FRAME# assertion)

6-4 Latency Timer.....read only, reads Rx0D bits 2:0

3 Reserved ..... always reads 0

2-0 PCI Master Bus Time-Out

(force into arbitration after a period of time)
- 000 Disable .....default
- 001 1x16 PCICLKs
- 010 2x16 PCICLKs
- 011 3x16 PCICLKs
- 100 4x16 PCICLKs
- ... ...
- 111 7x16 PCICLKs

Offset 76 - PCI Arbitration 2 (00h)..... RW

7 I/O Port 22 Access
- 0 CPU access to I/O address 22h is passed on to the PCI bus ..... default
- 1 CPU access to I/O address 22h is processed internally

6 Reserved .....always reads 0

5-4 Master Priority Rotation Control
- 00 Disable..... default
- 01 Grant to CPU after every PCI master grant
- 10 Grant to CPU after every 2 PCI master grants
- 11 Grant to CPU after every 3 PCI master grants

Setting 01: the CPU will always be granted access after the current bus master completes, no matter how many PCI masters are requesting.

Setting 10: if other PCI masters are requesting during the current PCI master grant, the highest priority master will get the bus after the current master completes, but the CPU will be guaranteed to get the bus after that master completes.

Setting 11: if other PCI masters are requesting, the highest priority will get the bus next, then the next highest priority will get the bus, then the CPU will get the bus.

In other words, with the above settings, even if multiple PCI masters are continuously requesting the bus, the CPU is guaranteed to get access after every master grant (01), after every other master grant (10) or after every third master grant (11).

3-2 Select REQn# to REQ4# mapping
- 00 REQ4#..... default
- 01 REQ0#
- 10 REQ1#
- 11 REQ2#

1 Reserved .....always reads 0

0 REQ4# is High Priority Master
- 0 Disable..... default
- 1 Enable

V-Link Duty Control

Offset B0 – V-Link Duty Control 1 (00h).....RW

7	**Rise Time Duty Cycle Control – V-Link #1 R-Port**
6	**Rise Time Duty Cycle Control – V-Link #0 R-Port**
5	**Fall Time Duty Cycle Control - V-Link #1 R-Port**
4	**Fall Time Duty Cycle Control - V-Link #0 R-Port**
3	**Rise Time Duty Cycle Control – V-Link #1 S-Port**
2	**Rise Time Duty Cycle Control – V-Link #0 S-Port**
1	**Fall Time Duty Cycle Control - V-Link #1 S-Port**
0	**Fall Time Duty Cycle Control - V-Link #0 S-Port**

Offset B1 – V-Link Duty Control 2 (00h).....RW

7-4	**Reserved** ..... always reads 0
3	**Rise Time Duty Cycle Control - V-Link #1 D-Port**
2	**Rise Time Duty Cycle Control - V-Link #0 D-Port**
1	**Fall Time Duty Cycle Control - V-Link #1 D-Port**
0	**Fall Time Duty Cycle Control - V-Link #0 D-Port**

V-Link Compensation / Drive Control

Offset B4 – V-Link NB Compensation Control (00h).... RW

7-5	**V-Link Autocomp Output Value – High Drive** .RO
4	**Reserved** .....always reads 0
3-1	**V-Link Autocomp Output Value – Low Drive** ..RO
0	**Compensation Select**
	0 Auto Comp (use values in bits 7-5, 3-1) default
	1 Manual Comp (use values in RxB5, B6)

Offset B5 – V-Link NB Strobe Drive Control (00h) ..... RW

7-5	**V-Link Strobe Pullup Manual Setting (High)**
4	**Reserved** .....always reads 0
3-1	**V-Link Strobe Pulldown Manual Setting (Low)**
0	**Reserved** .....always reads 0

Offset B6 – V-Link NB Data Drive Control (00h) ..... RW

7-5	**V-Link Data Pullup Manual Setting (High)**
4	**Reserved** .....always reads 0
3-1	**V-Link Data Pulldown Manual Setting (Low)**
0	Reserved .....always reads 0

Offset B8 – V-Link SB Compensation Control (00h) .... RW

7-5	**V-Link Autocomp Output Value – High Drive** .RO
4	**Reserved** .....always reads 0
3-1	**V-Link Autocomp Output Value – Low Drive** ..RO
0	**Compensation Select**
	0 Auto Comp (use values in bits 7-5, 3-1) default
	1 Manual Comp (use values in RxB9, BA)

Offset B9 – V-Link SB Strobe Drive Control (00h)..... RW

7-5	**V-Link Strobe Pullup Manual Setting (High)**
4	**Reserved** .....always reads 0
3-1	**V-Link Strobe Pulldown Manual Setting (Low)**
0	**Reserved** .....always reads 0

Offset BA – V-Link SB Data Drive Control (00h)..... RW

7-5	**V-Link Data Pullup Manual Setting (High)**
4	**Reserved** .....always reads 0
3-1	**V-Link Data Pulldown Manual Setting (Low)**
0	**Reserved** .....always reads 0

Device 1 Registers – PCI-to-PCI Bridge

Device 1 Header Registers

All registers are located in PCI configuration space. They should be programmed using PCI configuration mechanism 1 through CF8 / CFC with bus number of 0 and function number equal to 0 and device number equal to one.

Device 1 Offset 1-0 - Vendor ID (1106h) ..... RO

15-0 ID Code (reads 1106h to identify VIA Technologies)

Device 1 Offset 3-2 - Device ID (B204h) ..... RO

15-0 ID Code (reads B204h to identify the North Bridge PCI-to-PCI Bridge device)

Device 1 Offset 5-4 – Command (0007h) ..... RW

15-10 Reserved ..... always reads 0

9 Fast Back-to-Back Cycle Enable ..... RO
- 0 Fast back-to-back transactions only allowed to the same agent ..... default
- 1 Fast back-to-back transactions allowed to different agents

8 SERR# Enable ..... RO
- 0 SERR# driver disabled ..... default
- 1 SERR# driver enabled

(SERR# is used to report ECC errors).

7 Address / Data Stepping ..... RO
- 0 Device never does stepping ..... default
- 1 Device always does stepping

6 Parity Error Response ..... RW
- 0 Ignore parity errors & continue ..... default
- 1 Take normal action on detected parity errors

5 Reserved ..... always reads 0

4 Memory Write and Invalidate Command ..... RO
- 0 Bus masters must use Mem Write ..... default
- 1 Bus masters may generate Mem Write & Inval

3 Special Cycle Monitoring ..... RO
- 0 Does not monitor special cycles ..... default
- 1 Monitors special cycles

2 Bus Master ..... RW
- 0 Never behaves as a bus master
- 1 Enable to operate as a bus master on the primary interface on behalf of a master on the secondary interface ..... default

1 Memory Space ..... RW
- 0 Does not respond to memory space
- 1 Enable memory space access ..... default

0 I/O Space ..... RW
- 0 Does not respond to I/O space
- 1 Enable I/O space access ..... default

Device 1 Offset 7-6 - Status (Primary Bus) (0230h) .... RWC

15 Detected Parity Error ..... always reads 0

14 Signaled System Error (SERR#) ..... always reads 0

13 Signaled Master Abort
- 0 No abort received ..... default
- 1 Transaction aborted by the master with Master-Abort (except Special Cycles) ..... write 1 to clear

12 Received Target Abort
- 0 No abort received ..... default
- 1 Transaction aborted by the target with Target-Abort ..... write 1 to clear

11 Signaled Target Abort ..... always reads 0

10-9 DEVSEL# Timing
- 00 Fast
- 01 Medium ..... always reads 01
- 10 Slow
- 11 Reserved

8 Data Parity Error Detected ..... always reads 0

7 Fast Back-to-Back Capable ..... always reads 0

6 User Definable Features ..... always reads 0

5 66MHz Capable ..... always reads 1

4 Supports New Capability list ..... always reads 1

3-0 Reserved ..... always reads 0

Device 1 Offset 8 - Revision ID (00h) ..... RO

7-0 Chip Revision Code (00=First Silicon)

Device 1 Offset 9 - Programming Interface (00h) ..... RO

This register is defined in different ways for each Base/Sub-Class Code value and is undefined for this type of device.

7-0 Interface Identifier ..... always reads 00

Device 1 Offset A - Sub Class Code (04h) ..... RO

7-0 Sub Class Code .reads 04 to indicate PCI-PCI Bridge

Device 1 Offset B - Base Class Code (06h) ..... RO

7-0 Base Class Code .. reads 06 to indicate Bridge Device

Device 1 Offset D - Latency Timer (00h) ..... RO

7-0 Reserved ..... always reads 0

Device 1 Offset E - Header Type (01h) ..... RO

7-0 Header Type Code ..... reads 01: PCI-PCI Bridge

Device 1 Offset 18 - Primary Bus Number (00h).....RW

7-0 Primary Bus Number ..... default = 0

This register is read write, but internally the chip always uses bus 0 as the primary.

Device 1 Offset 19 - Secondary Bus Number (00h) .....RW

7-0 Secondary Bus Number..... default = 0

Note: AGP must use these bits to convert Type 1 to Type 0.

Device 1 Offset 1A - Subordinate Bus Number (00h) ....RW

7-0 Primary Bus Number ..... default = 0

Note: AGP must use these bits to decide if Type 1 to Type 1 command passing is allowed.

Device 1 Offset 1B – Secondary Latency Timer (00h) ....RO

7-0 Reserved ..... always reads 0

Device 1 Offset 1C - I/O Base (F0h).....RW

7-4 I/O Base AD[15:12]..... default = 1111b

3-0 I/O Addressing Capability ..... default = 0

Device 1 Offset 1D - I/O Limit (00h).....RW

7-4 I/O Limit AD[15:12] ..... default = 0

3-0 I/O Addressing Capability ..... default = 0

Device 1 Offset 1F-1E - Secondary Status.....RO

15-0 Secondary Status

Rx44[4] = 0: these bits read back 0000h

Rx44[4] = 1: these bits read back same as Rx7-6

Device 1 Offset 21-20 - Memory Base (FFF0h).....RW

15-4 Memory Base AD[31:20].....default = FFFh

3-0 Reserved ..... always reads 0

Device 1 Offset 23-22 - Memory Limit (Inclusive) (0000h) RW

15-4 Memory Limit AD[31:20] ..... default = 0

3-0 Reserved ..... always reads 0

Device 1 Offset 25-24 - Prefetchable Mem Base (FFF0h) RW

15-4 Prefetchable Memory Base AD[31:20]default = FFFh

3-0 Reserved ..... always reads 0

Device 1 Offset 27-26 - Prefetchable Memory Limit (0000h) .....RW

15-4 Prefetchable Memory Limit AD[31:20] . default = 0

3-0 Reserved ..... always reads 0

Device 1 Offset 34 - Capability Pointer (80h) .....RO

Contains an offset from the start of configuration space.

7-0 AGP Capability List Pointer..... always reads 80h

Device 1 Offset 3F-3E – PCI-to-PCI Bridge Control (0000h) ..... RW

15-4 Reserved .....always reads 0

3 VGA-Present on AGP

0 Forward VGA accesses to PCI Bus..... default

1 Forward VGA accesses to AGP Bus

Note: VGA addresses are memory A0000-BFFFFh and I/O addresses 3B0-3BBh, 3C0-3CFh and 3D0-3DFh (10-bit decode). "Mono" text mode uses B0000-B7FFFh and "Color" Text Mode uses B8000-BFFFFh. Graphics modes use Axxxxh. Mono VGA uses I/O addresses 3Bx-3Cxh and Color VGA uses 3Cx-3Dxh. If an MDA is present, a VGA will not use the 3Bxh I/O addresses and B0000-B7FFFh memory space; if not, the VGA will use those addresses to emulate MDA modes.

2 Block / Forward ISA I/O Addresses

0 Forward all I/O accesses to the AGP bus if they are in the range defined by the I/O Base and I/O Limit registers (device 1 offset 1C-1D)

..... default

1 Do not forward I/O accesses to the AGP bus that are in the 100-3FFh address range even if they are in the range defined by the I/O Base and I/O Limit registers.

1-0 Reserved .....always reads 0

Device 1 Device-Specific Registers

AGP Bus Control

Device 1 Offset 40 - CPU-to-AGP Flow Control 1 (00h) RW

7 CPU-AGP Post Write
- 0 Disable .....default
- 1 Enable

6 Reserved ..... always reads 0

5 CPU-AGP One Wait State Burst Write
- 0 Disable .....default
- 1 Enable

4-3 Read Prefetch Control
- 00 Always prefetch .....default
- x1 Never prefetch
- 10 Prefetch only for Enhance command

2 MDA Present on AGP
- 0 Forward MDA accesses to AGP .....default
- 1 Forward MDA accesses to PCI

Note: Forward despite IO / Memory Base / Limit

Note: MDA (Monochrome Display Adapter) addresses are memory addresses B0000h-B7FFFh and I/O addresses 3B4-3B5h, 3B8-3BAh and 3BFh (10-bit decode). 3BC-3BE are reserved for printers.

Note: If Rx3E bit-3 is 0, this bit is a don't care (MDA accesses are forwarded to the PCI bus).

1 AGP Master Read Caching
- 0 Disable .....default
- 1 Enable

0 AGP Delay Transaction
- 0 Disable .....default
- 1 Enable

Table 8. VGA/MDA Memory/IO Redirection

3E[3] VGA Pres.	40[2] MDA Pres.	VGA is on	MDA is on	Axxxx, B8xxx Access	B0000 -B7FFF Access	3Cx, 3Dx I/O	3Bx I/O
0	-	PCI	PCI	PCI	PCI	PCI	PCI
1	0	AGP	AGP	AGP	AGP	AGP	AGP
1	1	AGP	PCI	AGP	PCI	AGP	PCI

Device 1 Offset 41 - CPU-to-AGP Flow Control 2 (08h) RW

7 Retry Status
- 0 No retry occurred..... default
- 1 Retry Occurred .....**write 1 to clear**

6 Retry Timeout Action
- 0 No action taken except to record status ..... def
- 1 Flush buffer for write or return all 1s for read

5-4 Retry Count
- 00 Retry 2, backoff CPU ..... default
- 01 Retry 4, backoff CPU
- 10 Retry 16, backoff CPU
- 11 Retry 64, backoff CPU

3 CPU-to-AGP Bursting Timeout
- 0 Disable
- 1 Enable**..... default**

2 Reserved .....always reads 0

1 CPU-to-PCI/AGP Cycles Invalidate PCI/AGP Buffered Read Data
- 0 Disable..... default
- 1 Enable

0 Reserved .....always reads 0

Device 1 Offset 42 - AGP Master Control (00h) ..... RW

7 Reserved (Must Be Programmed to 1) .....def = 0

When this bit is set, the North Bridge will automatically resolve the problem of AGP master cycles being blocked by PCI Master Cycles.

6 AGP Master One Wait State Write
- 0 Disable..... default
- 1 Enable

5 AGP Master One Wait State Read
- 0 Disable..... default
- 1 Enable

4 Break Consecutive PCI Master Accesses
- 0 Disable..... default
- 1 Enable

3 Reserved .....always reads 0

2 Claim I/O R/W and Memory Read Cycles
- 0 Disable..... default
- 1 Enable

1 Claim Local APIC FEEx xxxx Cycles
- 0 Disable..... default
- 1 Enable

0 Snoop Write Enable 2T Rate, Support Host Side Snoop Cycles at 2T Rate
- 0 Disable..... default
- 1 Enable

Device 1 Offset 43 - AGP Master Latency Timer (22h) RW

7-4 Host to AGP Time slot
- 0 Disable (no timer)
- 1 16 GCLKs
- 2 32 GCLKs.....default
- … …
- F 128 GCLKs

3-0 AGP Master Time Slot
- 0 Disable (no timer)
- 1 16 GCLKs
- 2 32 GCLKs.....default
- … …
- F 128 GCLKs

Device 1 Offset 45 – Fast Write Control (72h)..... RW

7 Force Fast Write Cycle to be QW Aligned (if Rx45[6] = 0)
- 0 Disable..... default
- 1 Enable

6 Merge Multiple CPU Transactions Into One Fast Write Burst Transaction
- 0 Disable
- 1 Enable..... **default**

5 Merge Multiple CPU Write Cycles To Memory Offset 23-20 Into Fast Write Burst Cycles (if Rx45[6] = 0)
- 0 Disable
- 1 Enable..... **default**

4 Merge Multiple CPU Write Cycles To Prefetchable Memory Offset 27-24 Into Fast Write Burst Cycles (if Rx45[6] = 0)
- 0 Disable
- 1 Enable..... **default**

3 Reserved .....always reads 0

2 Fast Write Burst 4T Max (No Slave Flow Control)
- 0 Disable..... default
- 1 Enable

1 Fast Write Fast Back to Back
- 0 Disable
- 1 Enable..... **default**

0 Fast Write Initial Block 1 Wait State
- 0 Disable..... default
- 1 Enable

Rx45 Bits 7-4	CPU Write Address in Mem1	CPU Write Address in Mem2	Fast Write Cycle Alignment
x1xx	-	-	QW aligned, burstable
0000	-	-	DW aligned, nonburstable
x010	0	0	n/a
0010	0	1	DW aligned, non-burstable
x010	1	-	QW aligned, burstable
x001	0	0	n/a
x001	-	1	QW aligned, burstable
0001	1	0	DW aligned, non-burstable
x011	0	0	n/a
x011	1	-	QW aligned, burstable
x011	0	1	QW aligned, burstable
1000	-	-	QW aligned, non-burstable
1010	0	1	QW aligned, non-burstable
1001	1	0	QW aligned, non-burstable

Device 1 Offset 47-46 – PCI-to-PCI Bridge Device ID .. RW

15-0 PCI-to-PCI Bridge Device ID.....default = 0000

Power Management

Device 1 Offset 80 – Capability ID (01h).....RO

7-0 Capability ID..... always reads 01h

Device 1 Offset 81 – Next Pointer (00h).....RO

7-0 Next Pointer: Null..... always reads 00h

Device 1 Offset 82 – Power Mgmt Capabilities 1 (02h)...RO

7-0 Power Mgmt Capabilities..... always reads 02h

Device 1 Offset 83 – Power Mgmt Capabilities 2 (00h)...RO

7-0 Power Mgmt Capabilities..... always reads 00h

Device 1 Offset 84 – Power Mgmt Ctrl/Status (00h) .....RW

7-2 Reserved ..... always reads 0

1-0 Power State

00 D0 .....default
01 -reserved-
10 -reserved-
11 D3 Hot

Device 1 Offset 85 – Power Mgmt Status (00h)..... RO

7-0 Power Mgmt Status ..... default = 00

Device 1 Offset 86 – P2P Br. Support Extensions (00h) . RO

7-0 P2P Bridge Support Extensions ..... default = 00

Device 1 Offset 87 – Power Management Data (00h) ..... RO

7-0 Power Management Data ..... default = 00

FUNCTIONAL DESCRIPTION - INTEGRATED GRAPHICS

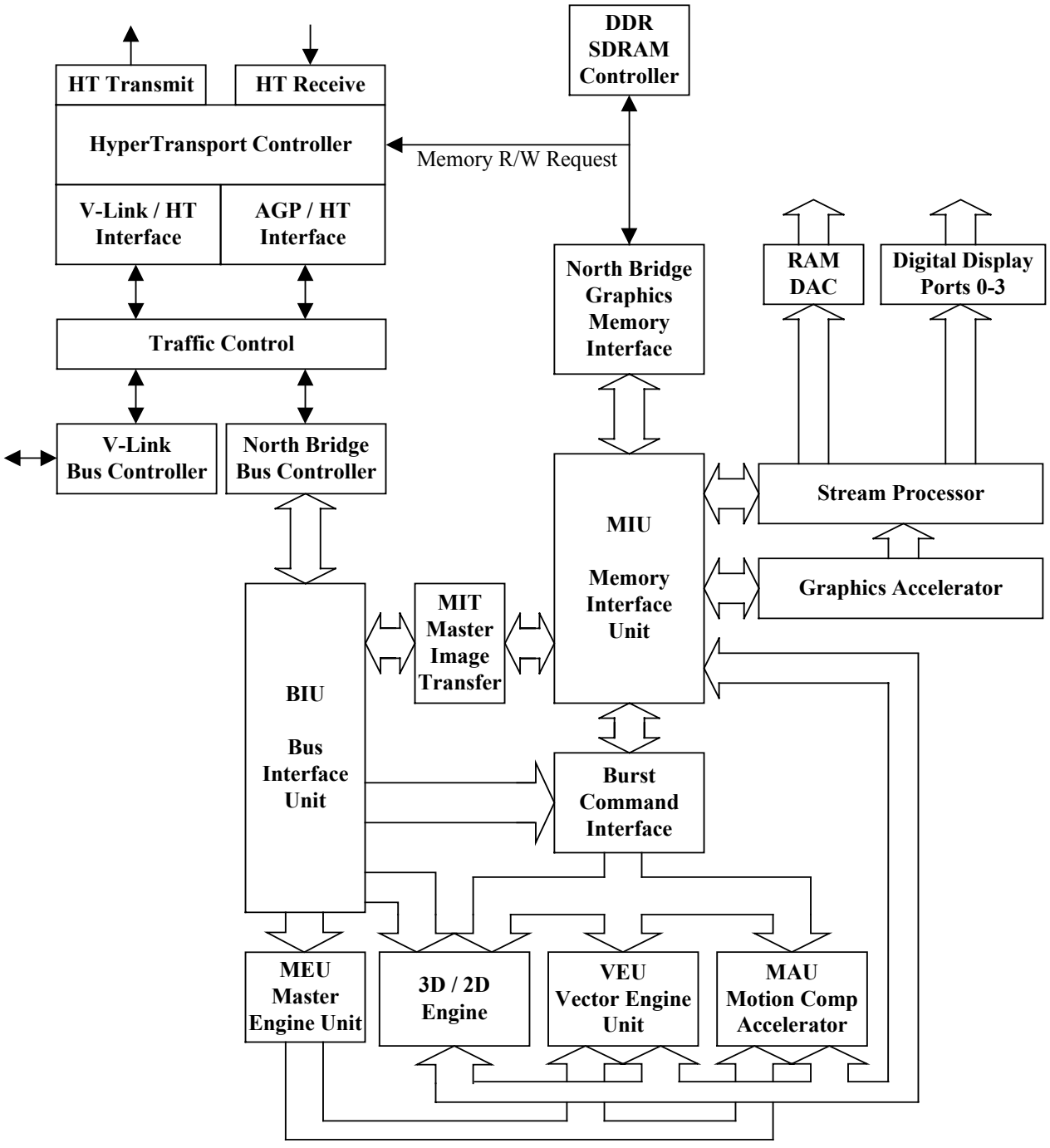


Figure 5. Integrated Graphics Controller Internal Block Diagram

Note: The above highly simplified block diagram is intended to show internal information flow paths only for programming purposes and does not necessarily reflect actual internal circuit implementation.

Configuration Strapping

Certain K8M800 graphics functions have options that must be selected and fixed at reset (before the register bits controlling these functions can be programmed by software). This is accomplished via power-on configuration strapping.

The strapping pins are pulled low internally and can be individually pulled high through 10 Kohm resistors. These pull-ups and pull-downs do not affect normal operation of the pins, but they do force the pins to a definite state during reset. At the rising edge of the reset signal, this state is sampled, the result is inverted and the data loaded into the CR36, CR37, CRB0 and CRF0 registers. The data is used for system configuration. The definitions of the strapping bits at the rising edge of the reset signal are shown in Table 7. Non-graphics straps are described in the pin descriptions for the MA signals in Table 1.

Pin Name	Ball #	CR Bit(s) Value	Description
DP0D6	L3		**DP0 Port Enable**
			0 =
			1 =
DP0D5	L2		**DP0 Port Configuration**
			0 =
			1 =
DP0D4	K1		**FP Port Configuration**
			0 =
			1 =
DP0D3 DP0D2 DP0D1 DP0D0	L4 K3 K2 J1	CRF0[3] CRF0[2] CRF0[1] CRF0[0]	OEM-Defined Panel Type

Table 9. Definition of Strapping Bits at the Rising Edge of the Reset Signal

Important Note: As described above, the signal levels on the strapping pins are inverted before being latched in the various strapping bit registers. Since the strapping pins all have internal pull-downs, the default values for each of the strapping bits is 1. The value latched at reset can be changed to 0 by adding an external pull-up to the appropriate pin. After reset, the strapping bits are written and read normally, i.e., there is no inversion of the register values.

PCI Configuration and Integrated AGP

PCI Configuration

The K8M800 North Bridge graphics Vendor ID register (Index 00H) in the PCI Configuration space is hardwired to 5333H to specify S3 Graphics Incorporated as the vendor. The Device ID register is hardwired to 8D01H.

Bits 10-9 of the Status register (Index 06H) are hardwired to 01b to specify medium DEVSEL timing. The Class Code register (Index 08H) is hardwired to 30000xxH to specify that the K8M800 North Bridge is a VGA compatible device.

There are two MMIO address mappings, as determined by the state of CRB0[7]. By default, CRB0[7] = 1, which selects Mapping 0. This uses the PCI base addresses specified by PCI10 and PCI14. 16 Mbytes of address space is claimed by PCI10 and 128 Mbytes of address space is claimed by PCI14. If the MA4 pin is strapped high at reset, a 0 is latched in CRB0[7] and selects Mapping 1. This uses base addresses PCI10 (same as Mapping 0), PCI14 (redefined from Mapping 0 to claim 16 Mbytes) and adds PCI18, PCI1C, PCI20 and PCI24, each claiming 16 Mbytes. Thus, Mapping 1 allows the address space claimed to be broken up into smaller blocks, as required by some operating systems. The Base Address 0 register (Index 10H) defaults to address 7000 0000H. This is the relocatable base address for memory-mapped I/O register accessing.

PCI06[4] is hardwired to 1 to indicate a capabilities list is available. PCI34[7-0] point to the PCI power management registers starting at offset DC. The basic power states (D0-D3) are supported as explained by the PCI Bus Power Management Interface Specification, Revision 1.1.

PCI Subsystem ID

The Subsystem ID and Subsystem Vendor ID are located in a 32-bit read only register at PCI Configuration Space Index 2C. These registers reflect the content of 4 read/write CR registers as follows:

Register	CR Space	PCI Configuration Space
Subsystem Vendor ID Low Byte	CR81	Index 2CH
Subsystem Vendor ID High Byte	CR82	Index 2DH
Subsystem ID Low Byte	CR83	Index 2EH
Subsystem ID High Byte	CR84	Index 2FH

Table 10. PCI Subsystem ID and Subsystem Vendor ID Registers

These registers allow identification of particular vendors using the same graphics chip. The following design allows the subsystem identification to be handled by software (no hardwiring).

All K8M800 motherboard designs will incorporate the video BIOS into the system BIOS ROM. The system BIOS must load the subsystem ID information into the K8M800 North Bridge before any ID scanning takes place. To do this, it must turn on the K8M800 North Bridge, enable I/O accesses in the PCI configuration space, unlock the CR registers, program the subsystem ID information in the registers described above, then turn off the K8M800 North Bridge.

Integrated AGP

K8M800 graphics conform with the requirements of Revision 2.0 of the AGP Interface Specification. Internal AGP K8M800 graphics are always enabled.

For the most part, AGP configuration is identical to PCI configuration. PCI04[4] is hardwired to 1 to indicate that K8M800 graphics implements a list of capabilities. PCI34[7-0] point to the location of this list, which is at offset 80H. PCI80, PCI84 and PCI88 implement the register bits required by the AGP specification. PCI88[2-0] select the data rate. PCI88[8] = 1 enables AGP bus master operations. PCI88[9] =1 enables side band addressing. This is indicated by PCI84[9] (1 = side band addressing supported). The state of PCI84[9] is determined by the state of CR70[7].

Display Memory

The K8M800 North Bridge utilizes either a dedicated local frame buffer interface or a Shared Memory Architecture (SMA) for Frame Buffer Memory. SMA allows system memory to be efficiently shared by the host CPU and the K8M800 North Bridge graphics controller. By default, no system memory is allocated for the graphics frame buffer, but up to 64 MBytes may be allocated depending on user preference, application requirements and the total size of system memory.

Note: Frame buffer memory is allocated from system memory at boot time. Changing the display settings to a resolution requiring additional frame buffer memory will require a system reboot to be performed.

Frame Buffer Size	Dev 0 RxFB[6-4] Register Setting	CR36[7-5] † Register Setting
0 MBytes	000	000
8 MBytes	011	011
16 MBytes	100	100
32 MBytes	101	101
64 MBytes	110	110

† For driver information only (not connected to hardware)

Table 11. Supported Frame Buffer Memory Configurations

Display Interfaces

The K8M800 North Bridge supports a variety of color TFT flat panels via the DVI interface. CRT and TV display are possible at the same time as flat panel display. All these interfaces are described in this section.

TFT Flat Panel DVI Interface

Figure 6 shows the hardware connections to an external transceiver conforming to the DVI 1.0 standard. This interface allows the K8M800 North Bridge to drive a TFT flat panel over considerable distance and is active when SR71[4] = 1. Panel power sequencing is controlled by the receiver components.

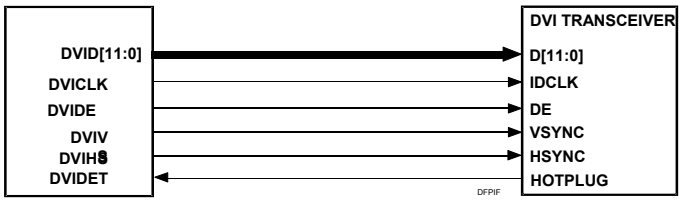


Figure 6. DVI Interface

CRT Interface

The K8M800 North Bridge provides the following CRT interface signals:

- RED (analog red)
- GREEN (analog green)
- BLUE (analog blue)
- HSYNC (horizontal sync)
- VSYNC (vertical sync)

In addition, DDC2 monitor communications can be implemented via the serial communications port controlled by SR26.

I^2C Serial Communications Port

One serial communications port is implemented in a register that can be accessed either via SR31.

This serial port is typically used for I2C interfacing. When SPCLK1 and SPDAT1 are tri-stated, the K8M800 North Bridge can detect an I2C start condition (SPDAT1 driven low while SPCLK1 is not driven low). This condition is generated by another I2C master that wants control of the I2C bus.

Graphics Modes

S3 Graphics endeavors to provide the maximum available noise-free mode support for any given device. Mode support is influenced by:

- Amount, speed and bus width of video memory
- Display resolution and color depth
- Maximum refresh capability detected for the display devices
- Panel Size
- Single IGA or Dual IGA setting
- SAMM setting

The following sections list the available graphics display modes in various system configurations.

Desktop Graphics Modes - CRT or Single DVI Display

Resolution	Bpp	Mode	CRT Maximum Refresh			
			60	75	85	100
640x480	8	101	√	√	√	√
	16	111	√	√	√	√
	32	112	√	√	√	√
800x600	8	103	√	√	√	√
	16	114	√	√	√	√
	32	115	√	√	√	√
1024x768	8	105	√	√	√	√
	16	117	√	√	√	√
	32	118	√	√	√	√
1280x1024	8	107	√	√	√	
	16	11A	√	√	√	
	32	11B	√	√	√2	
1600x1200	8	120	√	√	√	
	16	122	√	√	√	
	32	124	√7	√2,4	√3,4	

Key: √ = Supported
1 = Available for local frame buffer only, not available for SMA
2 = HW assisted Motion Compensation not available for SMA
3 = HW assisted Motion Compensation not available
4 = DVI not supported
5 = Support expected but not confirmed through test (pending receipt of customer panel or monitor)
6 = SAMM not supported for 16MB
7 = DVI support available for local frame buffer, will need tuning for SMA with actual silicon

Table 12. Desktop Graphics Display Modes for CRT or Single DVI Display

Motion compensation is not available for the following modes in any 16MB SAMM configuration:

- All 32-bit modes
- 1024x768x16 and higher
- 1280x1024x8 and higher

Desktop Graphics Modes - LCD XGA 1024x768 Multiple Display

CRT Resolution	BPP	LCD 8BPP				LCD 16BPP				LCD 32BPP			
		CRT Maximum Refresh				CRT Maximum Refresh				CRT Maximum Refresh			
		60	75	85	100	60	75	85	100	60	75	85	100
640x480	8	√	√	√	√	√	√	√	√	√	√	√	√
	16	√	√	√	√	√	√	√	√	√	√	√	√
	32	√	√	√	√	√	√	√	√	√	√	√	√
800x600	8	√	√	√	√	√	√	√	√	√	√	√	√
	16	√	√	√	√	√	√	√	√	√	√	√	√
	32	√	√	√	√	√	√	√	√	√	√	√	√
1024x768	8	√	√	√	√	√	√	√	√	√	√	√	√
	16	√	√	√	√	√	√	√	√	√	√	√	√
	32	√	√	√	√	√	√	√	√	√	√	√2	√2
1280x1024	8	√	√	√		√	√	√		√	√	√	
	16	√	√	√		√	√	√		√	√2	√2	
	32	√	√2	√2		√	√2	√2		√2	√2	√2,3	
1600x1200	8	√	√	√		√	√	√		√	√	√	
	16	√	√2	√2		√	√2	√2		√2	√2	√2	
	32[6]	√2,7	√2,3,4	√1,3,4		√2,7	√1,3,4	√1,3,4		√2,3,7	√1,3,4	√1,3,4	
640x480	8	√	√	√	√	√	√	√	√	√	√	√	√
	16	√	√	√	√	√	√	√	√	√	√	√	√
	32	√	√	√	√	√	√	√	√	√	√	√	√

Key: √ = Supported
1 = Available for local frame buffer only, not available for SMA
2 = HW assisted Motion Compensation not available for SMA
3 = HW assisted Motion Compensation not available
4 = DVI not supported
5 = Support expected but not confirmed through test (pending receipt of customer panel or monitor)
6 = SAMM not supported for 16MB
7 = DVI support available for local frame buffer, will need tuning for SMA with actual silicon

Table 13. Desktop Graphics Modes – LCD XGA 1024x768 Multiple Display

Desktop Graphics Modes - LCD SXGA 1280x1024 Multiple Display

CRT Resolution	BPP	LCD 8BPP CRT Maximum Refresh				LCD 16BPP CRT Maximum Refresh				LCD 32BPP CRT Maximum Refresh			
		60	75	85	100	60	75	85	100	60	75	85	100
640x480	8	√	√	√	√	√	√	√	√	√	√	√	√
	16	√	√	√	√	√	√	√	√	√	√	√	√
	32	√	√	√	√	√	√	√	√	√	√	√	√
800x600	8	√	√	√	√	√	√	√	√	√	√	√	√
	16	√	√	√	√	√	√	√	√	√	√	√	√
	32	√	√	√	√	√	√	√	√	√	√2	√2	√2
1024x768	8	√	√	√	√	√	√	√	√	√	√	√	√
	16	√	√	√	√	√	√	√	√	√	√2	√2	√2
	32	√	√	√	√2	√	√	√2	√2	√2	√2	√2	√2
1280x1024	8	√	√	√		√	√	√		√	√	√2	
	16	√	√	√2		√	√2	√2		√2	√2	√2	
	32	√2	√2	√2		√2	√2	√2		√2	√1,3	√1,3	
640x480	8	√	√	√	√	√	√	√	√	√	√	√	√
	16	√	√	√	√	√	√	√	√	√	√	√	√
	32	√	√	√	√	√	√	√	√	√	√	√	√
1600x1200	8	√	√	√		√	√	√		√2	√2	√2	
	16	√2	√2	√2		√2	√2	√2,3		√2	√2,3	√2,3	
	32[6]	√2,7	√2,3,4	√1,3,4		√2,3,7	√1,3,4	√1,3,4		√1,3,7	√1,3,4		

Key: √ = Supported
1 = Available for local frame buffer only, not available for SMA
2 = HW assisted Motion Compensation not available for SMA
3 = HW assisted Motion Compensation not available
4 = DVI not supported
5 = Support expected but not confirmed through test (pending receipt of customer panel or monitor)
6 = SAMM not supported for 16MB
7 = DVI support available for local frame buffer, will need tuning for SMA with actual silicon

Table 14. Desktop Graphics Modes – LCD SXGA 1280x1024 Multiple Display

Desktop Graphics Modes - LCD SXGA+ 1400x1050 Multiple Display

CRT Resolution	BPP	LCD 8BPP CRT Maximum Refresh				LCD 16BPP CRT Maximum Refresh				LCD 32BPP CRT Maximum Refresh			
		60	75	85	100	60	75	85	100	60	75	85	100
640x480	8	√	√	√	√	√	√	√	√	√	√	√	√
	16	√	√	√	√	√	√	√	√	√	√	√	√
	32	√	√	√	√	√	√	√	√	√	√	√	√
800x600	8	√	√	√	√	√	√	√	√	√	√	√	√
	16	√	√	√	√	√	√	√	√	√	√	√	√
	32	√	√	√	√	√	√	√	√	√	√2	√2	√2
1024x768	8	√	√	√	√	√	√	√	√	√	√	√	√
	16	√	√	√	√	√	√	√	√	√	√2	√2	√2
	32	√	√	√	√2	√	√	√2	√2	√2	√2	√2	√2
1280x1024	8	√	√	√		√	√	√		√	√	√2	
	16	√	√	√2		√	√2	√2		√2	√2	√2	
	32	√2	√2	√2		√2	√2	√2		√2	√1,3	√1,3	
1400x1050	8	√	√	√		√	√	√		√2	√2	√2	
	16	√2	√2	√2		√2	√2	√2		√2	√2	√2	
	32	√2	√2	√2		√2	√2,3	√2,3		√1,3	√1,3	√1,3	
1600x1200	8	√	√	√		√	√	√		√2	√2	√2	
	16	√2	√2	√2		√2	√2	√2,3		√2	√2,3	√2,3	
	32[6]	√2,7	√2,3,4	√1,3,4		√2,3,7	√1,3,4	√1,3,4		√1,3,7	√1,3,4		

Key: √ = Supported
1 = Available for local frame buffer only, not available for SMA
2 = HW assisted Motion Compensation not available for SMA
3 = HW assisted Motion Compensation not available
4 = DVI not supported
5 = Support expected but not confirmed through test (pending receipt of customer panel or monitor)
6 = SAMM not supported for 16MB
7 = DVI support available for local frame buffer, will need tuning for SMA with actual silicon

Table 15. Desktop Graphics Modes – LCD SXGA+ 1400x1050 Multiple Display

Desktop Graphics Modes - LCD UXGA 1600x1200 Multiple Display

CRT Resolution	BPP	LCD 8BPP				LCD 16BPP				LCD 32BPP[8]			
		CRT Maximum Refresh				CRT Maximum Refresh				CRT Maximum Refresh			
		60	75	85	100	60	75	85	100	60	75	85	100
640x480	8	√	√	√	√	√	√	√	√	√	√	√	√
	16	√	√	√	√	√	√	√	√	√	√	√	√
	32	√	√	√	√	√	√	√	√	√	√	√	√
800x600	8	√	√	√	√	√	√	√	√	√	√	√	√
	16	√	√	√	√	√	√	√	√	√	√	√	√
	32	√	√	√	√	√	√2	√2	√2	√	√2	√2	√2
1024x768	8	√	√	√	√	√	√	√	√	√	√	√	√
	16	√	√	√	√	√	√2	√2	√2	√	√	√	√
	32	√	√2	√2	√2	√2	√2	√2	√2	√2	√1	√1	√1
1280x1024	8	√	√	√		√	√	√2		√	√	√	
	16	√	√2	√2		√2	√2	√2		√	√	√1	
	32	√2	√2	√2,3		√2	√2,3	√1,3		√1	√1	√1	
1600x1200	8	√	√	√2		√2	√2	√2		√	√	√	
	16	√2	√2	√2,3		√2,	√2,3	√2,3		√1	√1	√1	
	32[6]	√2,3,7	√1,3,4	√1,3,4		√1,3,7				√1,7			

Key: √ = Supported
1 = Available for local frame buffer only, not available for SMA
2 = HW assisted Motion Compensation not available for SMA
3 = HW assisted Motion Compensation not available
4 = DVI not supported
5 = Support expected but not confirmed through test (pending receipt of customer panel or monitor)
6 = SAMM not supported for 16MB
7 = DVI support available for local frame buffer, will need tuning for SMA with actual silicon
8 = Motion Compensation available for LCD only

Table 16. Desktop Graphics Modes – LCD UXGA+ 1600x1200 Multiple Display

Graphics Modes That Allow LCD Centering and Expansion

When the LCD resolution is smaller than the panel's native resolution, software and hardware may activate centering or expansion depending on the display setting, using the interpolated scaler.

	LCD NATIVE RESOLUTION				
RESOLUTION	LCD XGA 1024x768	LCD SXGA 1280x768	LCD WXGA 1280x1024	LCD SXGA+ 1400x1050	LCD UXGA 1600x1200
640x480	CE	CE	CE	CE	CE
800x600	CE	CE	CE	CE	CE
1024x768		CE	CE	CE	CE
1280x1024				C	C
1400x1050					
1600x1200					

C = Centered
CE = Centering and Expansion possible for LCD

Table 17. Graphics Modes That Allow LCD Centering and Expansion

VGA Graphics Modes

Legacy VGA modes may be supported by BIOS and DOS, but most are not enabled for drivers.

Resolution	Bpp	Colors	Memory	Mode	CRT Refresh				
					60	70	75	85	100
40x25	c	16	text	0,1		√			
80x25	c	16	text	2,3		√			
320x200	2	4	2-bit planar	4,5		√			
640x200	1	2	1-bit planar	6		√			
80x25	bw	mono	text	7		√			
320x200	4	16	4-bit planar	0D		√			
640x200	4	16	4-bit planar	0E		√			
640x350	bw	mono	1-bit planar	0F		√			
640x350	4	16	4-bit planar	10		√			
640x480	1	2	2-bit planar	11	√				
640x480	4	16	4-bit planar	12	√				
320x200*	8	256	8-bit packed	13		√			
800x600**	4	16	4-bit planar	102	√		√	√	√

Key: √ = Supported
* = Legacy VGA Mode 13, 320x200x8 is used by DirectDraw
** = Legacy VESA Mode 102, 800x600x4 is used by Windows XP
bw = Black and White
c = Color

Table 18. VGA Graphics Modes

Direct Draw Graphics Modes

Overlay is enabled for all the Direct Draw modes listed below.

Resolution	Bpp	Mode	CRT Refresh		
			60	70	72
320x200	8	13	√	√	
	16	10E	√	√	
	32	10F	√	√	
320x240	8	131	√		√
	16	133	√		√
	32	134	√		√
400x300	8	141	√		√
	16	143	√		√
	32	144	√		√
512x384	8	151	√	√	
	16	153	√	√	
	32	154	√	√	
640x400	8	100	√	√	
	16	11D	√	√	
	32	11E	√	√	

Key: √ = Supported

Table 19. Direct Draw Graphics Modes

Graphics Modes for TV Display

Modes supported on TV using the integrated TV encoder are listed below.

Resolution	Bpp	Mode	Internal TV	
			NTSC	PAL
40x25_TEXT	c	0	√	√
	c	1	√	√
80x25_TEXT	c	2	√	√
	c	3	√	√
	bw	7		
320x200	8	13	√	√
640x400	8	100	√	√
	16	11D	√	√
	32	11E	√	√
640x480	1	11	√	√
	4	12	√	√
	8	101	√	√
	16	111	√	√
	32	112	√	√
800x600	8	103	√	√
	16	114	√	√
	32	115	√	√
1024x768	8	105	√	√
	16	117	√	√
	32	118	√	√

Key: √ = Supported
bw = Black and White
c = Color

Table 20. Graphics Modes for TV Display

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Table 21. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes
T_C	Case Operating Temperature	0	70	°C	1
T_S	Storage Temperature	–55	125	°C	1
V_{IN}	Input Voltage	–0.5	V_{RAIL} + 10%	Volts	1, 2
V_{OUT}	Output Voltage	–0.5	V_{RAIL} + 10%	Volts	1, 2

Note 1. Stress above the conditions listed may cause permanent damage to the device. Functional operation of this device should be restricted to the conditions described under operating conditions.

Note 2. V_{RAIL} is defined as the V_{CC} level of the respective rail. The HyperTransport CPU interface is CPU dependent (typically 1.2V). V-Link is 1.5V. AGP is 1.5V (4x transfer mode) or 0.8V (8x transfer mode).

Supply Current and Power Characteristics

T_C = 0-85°C, V_{RAIL} = V_{CC} ± 5%, V_{CORE} = 2.5V ± 5%, GND=0V

Table 22. Supply Current & Power Characteristics – Internal / Interface Digital Logic

Symbol	Parameter	Typ	Max	Unit	Condition
I_{CC}	Power Supply Current – VCC	–	76	mA	All conditions
I_{SUS}	Power Supply Current – VCCSUS	1.0	1.1	**uA**	All conditions
I_{CCHT}	Power Supply Current – VCCHT	–		mA	8-bit, 200 MHz
I_{CCVL}	Power Supply Current – VCCVL	–	1.8	mA	4x transfer mode
$I_{CCVLIDLE}$	Power Supply Current – VCCVL	–	8	**uA**	Idle
I_{CCG}	Power Supply Current – VCCAGP	–	16	mA	No AGP cycles active
I_{CCQQ}	Power Supply Current – VCCQQ	–		mA	No AGP cycles active
P_D	Power Dissipation – Entire Chip	–		W	Max operating frequency

Table 23. Supply Current & Power Characteristics – Analog / Reference Voltages

Symbol	Parameter	Typ	Max	Unit	Condition
I_{CCGREF}	Power Supply Current – AGPVREF	–	2.4	mA	No AGP cycles active
$I_{CCVLREF}$	Power Supply Current – VLVREF	–	5.0	mA	4x transfer mode
I_{CCATX}	Power Supply Current – VCCATX			mA	8-bit, 200 MHz
I_{CCARX}	Power Supply Current – VCCARX			mA	8-bit, 200 MHz

DC Characteristics

T_C = 0-85°C, GND = 0V, V_{CC} = 2.5V ±5%, V_{CCHT} = 1.2V±5%, V_{CCAGP} = 1.5V±5% (4x) or 0.8V±5% (8x), V_{CCVL} = 2.5V±5%

Table 24. DC Characteristics – HyperTransport

Symbol	Parameter	Min	Typ	Max	Unit	Condition / Signal
V_{HTIL}	Single-Ended Input Low Voltage	–0.30	–	0.7	V	HTSTP#
V_{HTIH}	Single-Ended Input High Voltage	1.7	–	V_{CC} + 0.3	V	HTSTP#
V_{HTOL}	Single-Ended Output Low Voltage	–	–	0.7	V	HTRST#
V_{HTOH}	Single-Ended Output High Voltage	1.7	–	–	V	HTRST#
I_{HTIL}	Single-Ended Input Leakage	–	–	±500	uA	V_{CC} = Max, V_I = Gnd or V_{CC}
V_{HTOD}	Differential Output Voltage†	495	600	715	mV	TCADx, TCLKx, TCTLx
V_{HTID}	Differential Input Voltage†	300	600	900	mV	RCADx, RCLKx, RCTLx
Delta V_{HTID}		–125	0	125	mV	
V_{ICM}	Input Common Mode Voltage	450	600	800	mV	
Delta V_{ICM}		–110	0	110	mV	
T_R	Differential Signal Rise Time	2		8	V/ns	
T_F	Differential Signal Fall Time	–2		–8	V/ns	

For Reference Only – See HyperTransport Standard documents for detailed specifications
†HyperTransport differential I/O assumes N>P = logical 0 and P>N = logical 1.

Table 25. DC Characteristics – V-Link

Symbol	Parameter	Min	Max	Unit	Condition
V_{VIL}	Input Low Voltage	–0.50	0.8	V	
V_{VIH}	Input High Voltage	2.0	V_{CC} + 0.5	V	
V_{VOL}	Output Low Voltage	-	0.55	V	I_{OL} = 4.0 mA
V_{VOH}	Output High Voltage	2.4	–	V	I_{OH} = –1.0 mA
I_{VIL}	Input Leakage Current	–	±10	uA	$0 < V_{IN} < V_{CCVL}$

Table 26. DC Characteristics – AGP

Symbol	Parameter	Min	Max	Unit	Condition
V_{AIL4x}	Input Low Voltage – 4x Transfer Mode	–0.50		V	
V_{AIH4x}	Input High Voltage – 4x Transfer Mode		V_{CC} + 0.5	V	
V_{AOL4x}	Output Low Voltage – 4x Transfer Mode	-		V	I_{OL} = x.x mA
V_{AOH4x}	Output High Voltage – 4x Transfer Mode		–	V	I_{OH} = –x.x mA
V_{AIL8x}	Input Low Voltage – 8x Transfer Mode	–0.50		V	
V_{AIH8x}	Input High Voltage – 8x Transfer Mode		V_{CC} + 0.5	V	
V_{AOL8x}	Output Low Voltage – 8x Transfer Mode	-		V	I_{OL} = x.x mA
V_{AOH8x}	Output High Voltage – 8x Transfer Mode		–	V	I_{OH} = –x.x mA
I_{AIL}	Input Leakage Current	–	±10	uA	$0 < V_{IN} < V_{CCAGP}$
I_{AOZ}	Tristate Leakage Current	–	±20	uA	$0.55 < V_{OUT} < V_{CCAGP}$

For Reference Only – See AGP 3.0 Standard documents for detailed specifications

AGP Signal Levels

AGP 3.0 (8x transfer mode) specifies a 0.8V voltage swing, end-terminated and referenced to ground as opposed to AGP 2.0 (4x transfer mode), which specified a rail-to-rail 1.5V series-terminated voltage swing.

This change permits a higher data rate and a common signaling voltage, which can be realized in multiple generations of silicon technology. The figure below shows the relationship between the VCCQQ and GNDQQ rails and the corresponding output voltage swing for AGP 3.0-compatible 8x transfer mode.

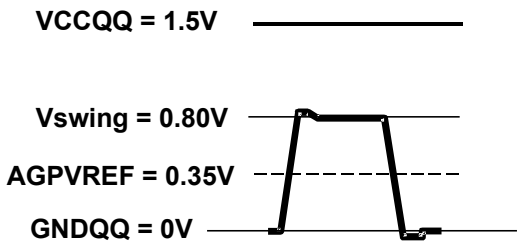


Figure 7. AGP 3.0 (8x) Signal Levels

Table 27. DC Characteristics – Reset, Power OK, Suspend Status and Test

Symbol	Parameter	Min	Max	Unit	Condition
V_{VIL}	Input Low Voltage	–0.50	0.8	V	
V_{VIH}	Input High Voltage	2.0	3.8	V	3.3V Tolerant
I_{VIL}	Input Leakage Current	–	±10	uA	$0 < V_{IN} < V_{CC}$

AC Timing Specifications

AC timing specifications provided are based on external zero-pf capacitance load. Min/max cases are based on the following table:

Table 28. AC Timing Min / Max Conditions

Parameter	Min	Max	Unit
2.5V Power (Internal Logic)	2.375	2.625	Volts
1.5V Power (VCCQQ for 4x transfer mode)	1.425	1.575	Volts
0.8V Power (VCCQQ for 8x transfer mode)	0.76	0.84	Volts
Case Temperature	0	85	°C

Drive strength for selected output pins is programmable and may effect AC timing specifications.

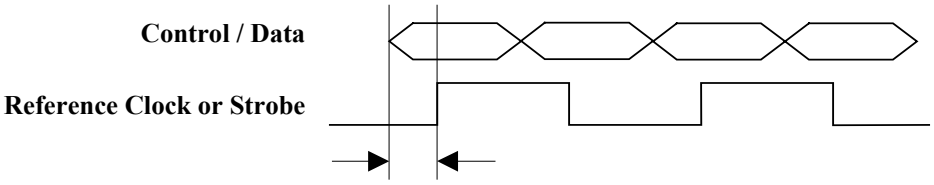
Table 29. AC Characteristics – HyperTransport CPU Interface Receive

Symbol	Parameter	Setup	Hold	Unit
T_{RLS4}, T_{RLH4}	RCAD0-7, RCTL / RCTL# input relative to RCLK0 / RCLK0# - 400 MT/s	300	300	pS
T_{RLS8}, T_{RLH8}	RCAD0-7, RCTL / RCTL# input relative to RCLK0 / RCLK0# - 800 MT/s	200	200	pS
T_{RLS12}, T_{RLH12}	RCAD0-7, RCTL / RCTL# input relative to RCLK0 / RCLK0# - 1.2 GT/s	150	150	pS
T_{RLS16}, T_{RLH16}	RCAD0-7, RCTL / RCTL# input relative to RCLK0 / RCLK0# - 1.6 GT/s	120	120	pS
T_{RHS4}, T_{RHH4}	RCAD8-15 input relative to RCLK1 / RCLK1# - 400 MT/s	300	300	pS
T_{RHS8}, T_{RHH8}	RCAD8-15 input relative to RCLK0 / RCLK0# - 800 MT/s	200	200	pS
T_{RHS12}, T_{RHH12}	RCAD8-15 input relative to RCLK0 / RCLK0# - 1.2 GT/s	150	150	pS
T_{RHS16}, T_{RHH16}	RCAD8-15 input relative to RCLK0 / RCLK0# - 1.6 GT/s	120	120	pS

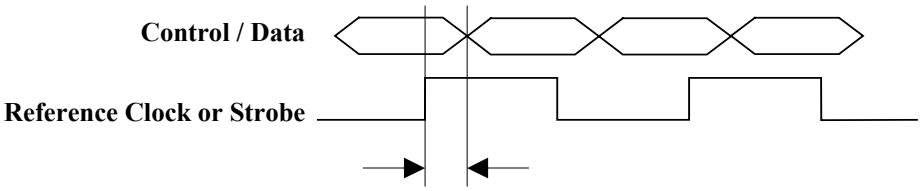
Table 30. AC Characteristics – HyperTransport CPU Interface Transmit

Symbol	Parameter	Min	Max	Unit
T_{TLD4}	TCAD0-7, TCTL / TCTL# output delay from TCLK0 / TCLK0# - 400 MT/s	650	1800	pS
T_{TLD8}	TCAD0-7, TCTL / TCTL# output delay from TCLK0 / TCLK0# - 800 MT/s	325	950	pS
T_{TLD12}	TCAD0-7, TCTL / TCTL# output delay from TCLK0 / TCLK0# - 1.2 GT/s	220	625	pS
T_{TLD16}	TCAD0-7, TCTL / TCTL# output delay from TCLK0 / TCLK0# - 1.6 GT/s	180	475	pS
T_{THD4}	TCAD8-15 output delay from TCLK1 / TCLK1# - 400 MT/s	650	1800	pS
T_{THD8}	TCAD8-15 output delay from TCLK1 / TCLK1# - 800 MT/s	325	950	pS
T_{THD12}	TCAD8-15 output delay from TCLK1 / TCLK1# - 1.2 GT/s	220	625	pS
T_{THD16}	TCAD8-15 output delay from TCLK1 / TCLK1# - 1.6 GT/s	180	475	pS

Termination resistor values: R_{TT} = 100 Ω ±10%, R_{ON} = 50 Ω ±10%



Input: Setup Time
Output: Data Valid before Strobe



Input: Hold Time
Output: Data Valid after Strobe

Figure 8. Timing Diagram – HyperTransport Setup / Hold and Data Valid

Table 31. AC Characteristics – AGP 8x

Symbol	Parameter	Min	Max	Unit
T_{GS8}	Data / Control Input Setup Time Relative to Strobe – 8x Transfer Mode	250	–	pS
T_{GH8}	Data / Control Input Hold Time Relative to Strobe – 8x Transfer Mode	250	–	pS
T_{GS4}	Data / Control Input Setup Time Relative to Strobe – 4x Transfer Mode	500	–	pS
T_{GH4}	Data / Control Input Hold Time Relative to Strobe – 4x Transfer Mode	500	–	pS
T_{GDV8}	Data / Control Output Valid Relative to Strobe – 8x Transfer Mode	–550	650	pS
T_{GDV4}	Data / Control Output Valid Relative to Strobe – 4x Transfer Mode	–1000	1000	pS

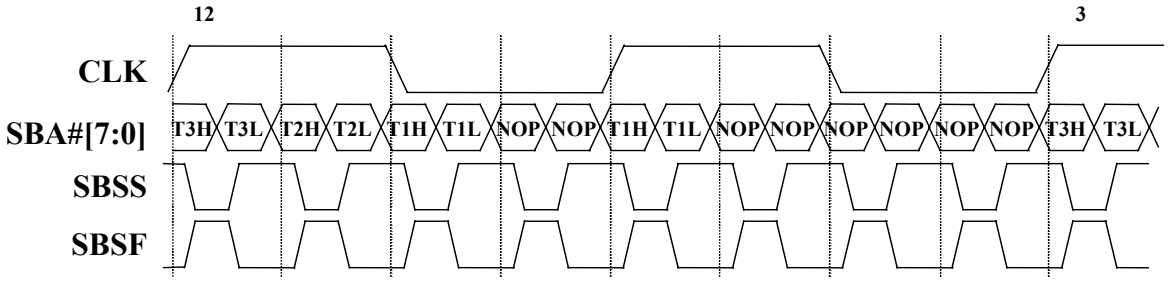


Figure 9. Timing Diagram – AGP 8x Side Band Address Timing

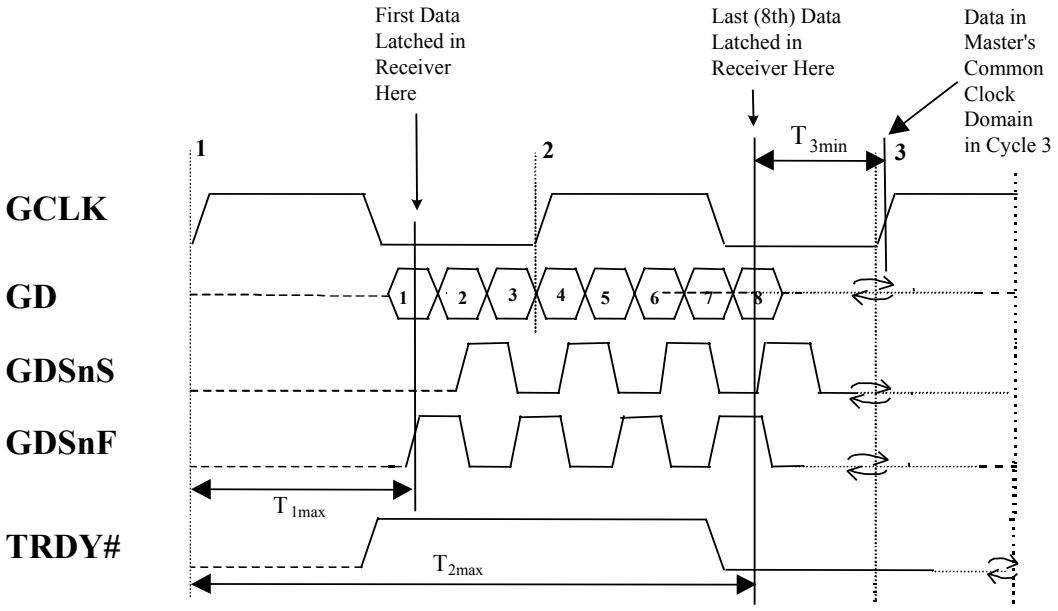
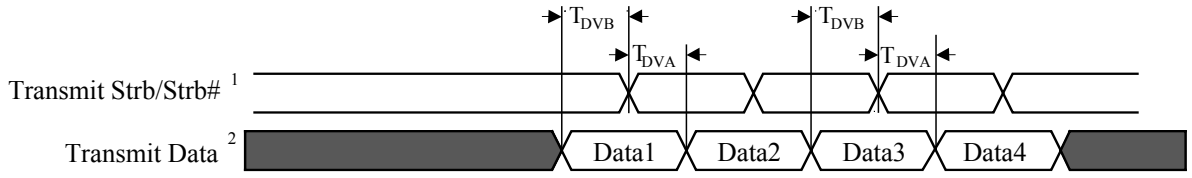
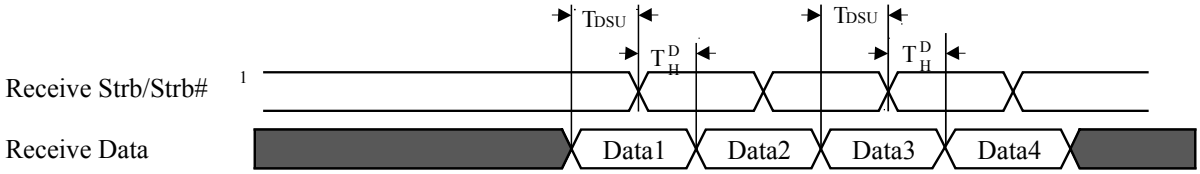


Figure 10. Timing Diagram – AGP 8x Data Transfer Timing



Note 1: This waveform represents two differential strobes
Note 2: Data refers to any of the 2x/4x capable signal groups: GD[31:0], GBE[3:0]# or SBA[7:0]

Figure 11. Timing Diagram – AGP 4x Transmit Timing



Note 1: This waveform represents two differential strobes

Figure 12. Timing Diagram – AGP 4x Receive Timing

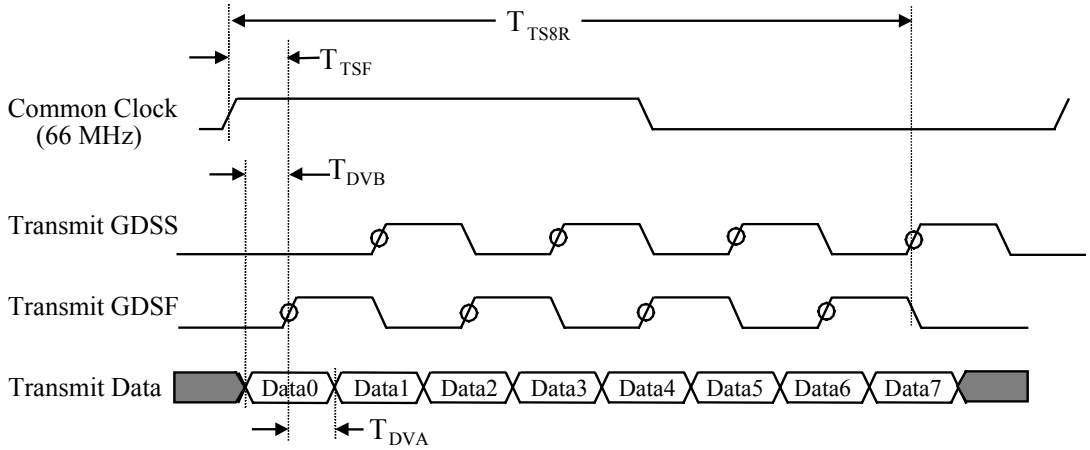


Figure 13. Timing Diagram – AGP 8x Transmit Source-Synchronous Timing

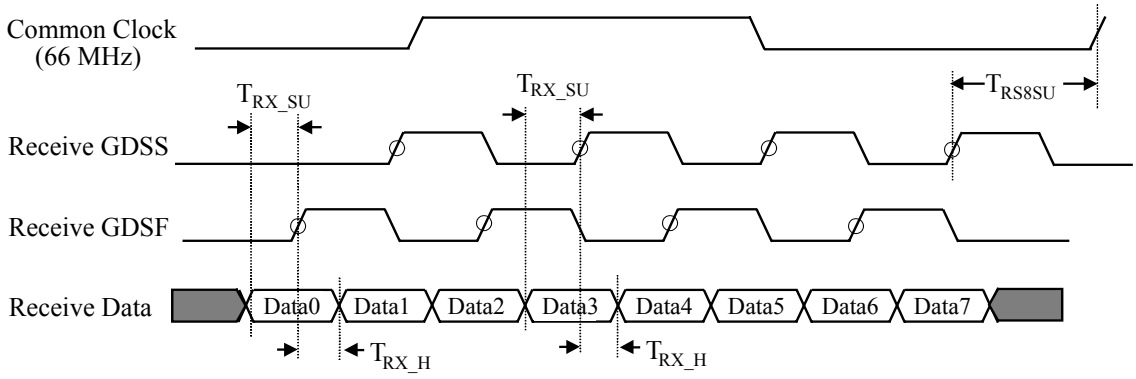


Figure 14. Timing Diagram – AGP 8x Receive Source-Synchronous Timing

Table 32. AC Characteristics – V-Link Interface

Symbol	Parameter	Min	Max	Unit	Condition
T_{VUS4}	VADn, VPAR, VBE#, UPCMD Input Setup to UPSTB / UPSTB#	500	–	**pS**	4x mode
T_{VUH4}	VADn, VPAR, VBE#, UPCMD Input Hold From UPSTB / UPSTB#	500	–	**pS**	4x mode
T_{VUS8}	VADn, VPAR, VBE#, UPCMD Input Setup to UPSTB / UPSTB#	250	–	**pS**	8x mode
T_{VUH8}	VADn, VPAR, VBE#, UPCMD Input Hold From UPSTB / UPSTB#	250	–	**pS**	8x mode
T_{VDD4}	VADn, VPAR, VBE#, DNCMD Output Delay from DNSTB / DNSTB#	–650	750	**pS**	4x mode
T_{VDD8}	VADn, VPAR, VBE#, DNCMD Output Delay from DNSTB / DNSTB#	–1100	1100	**pS**	8x mode
T_{VUP4}	UPSTB / UPSTB# Input Pulse Width			nS	4x mode
T_{VUF4}	UPSTB / UPSTB# Input Frequency		266	MHz	4x mode
T_{VUP8}	UPSTB / UPSTB# Input Pulse Width			nS	8x mode
T_{VUF8}	UPSTB / UPSTB# Input Frequency		533	MHz	8x mode
T_{VDP4}	DNSTB / DNSTB# Output Minimum Pulse Width			nS	4x mode
T_{VDF4}	DNSTB / DNSTB# Output Frequency		266	MHz	4x mode
T_{VDP8}	DNSTB / DNSTB# Output Minimum Pulse Width			nS	8x mode
T_{VDF8}	DNSTB / DNSTB# Output Frequency		533	MHz	8x mode

Table 33. AC Characteristics –Reset, Power OK and Suspend

Symbol	Parameter	Min	Max	Unit
T_{RLPU}	RESET# Low On Power Up	0	–	msec
T_{RLPW}	RESET# Low Pulse Width from PWROK	7	–	msec
T_{PLPU}	PWROK Low On Power Up After Power Supply Voltages Stable	50	–	msec
T_{SLPW}	SUSST# Low Pulse Width	1.2	–	msec
T_{VCSL}	Primary Voltages Removed After SUSST# Goes Low	64	–	**usec**
T_{VCSH}	Primary Voltages Stable (PWROK) Before SUSST# Returns High	250	–	**usec**

MECHANICAL SPECIFICATIONS

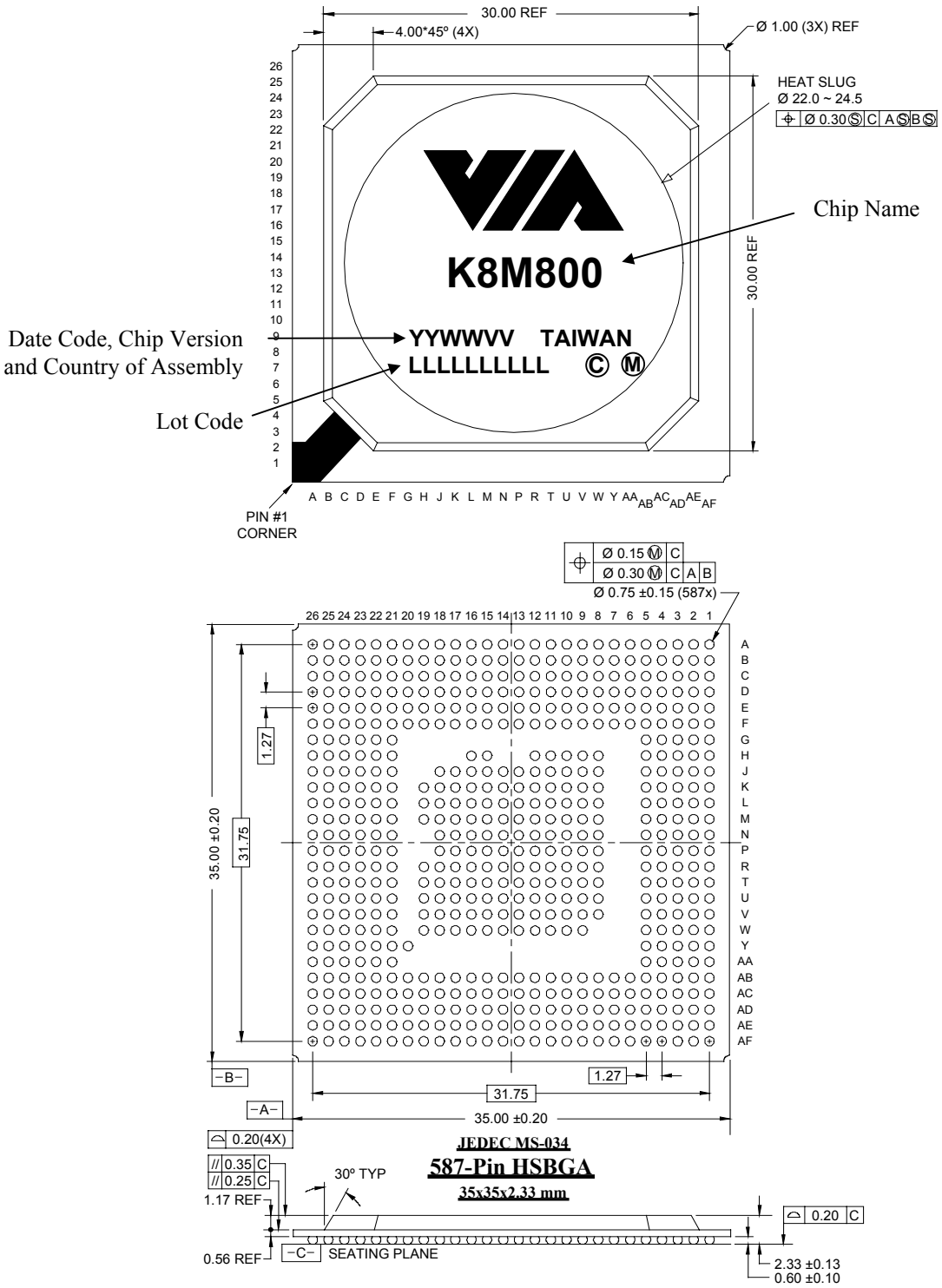


Figure 15. Mechanical Specifications – 587-Pin BGA Package with Heat Spreader