Data Sheet

PN800 Mobile North Bridge

with Integrated UniChrome Pro 3D / 2D Graphics Controller

Revision 1.04
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VIA TECHNOLOGIES, INC.

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1.01	5/18/04	Fixed DVP0D8,6-4 strap definitions; Fixed VIA logo shape in marking specs	DH
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1.03	6/8/04	Moved GTVCLKIN from GDVP1DET to FPDET Updated D0F3Rx52-53 & D0F7Rx57 register definitions	DH
1.04	6/11/04	Fixed AB and AG pin numbers in “CRT Interface” pin description table Fixed GADSTB1F pin name typo in “Flat Panel Interface” pin description table	DH

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PN800 MOBILE NORTH BRIDGE

800 / 533 / 400 MHz Intel Pentium 4 Front Side Bus
Integrated UniChrome Pro 3D / 2D Graphics & Video Controllers
Advanced DDR400 SDRAM Controller
1 GB / sec Ultra V-Link Interface
and External 8x / 4x AGP Bus

PRODUCT FEATURES

- **Defines Highly Integrated Solutions for Full Featured Value PC Mobile Designs**
  - High Performance UMA North Bridge: Integrated Pentium 4 North Bridge with 800 MHz FSB support and UniChrome Pro 3D / 2D Graphics & Video Controllers in a single chip
  - Advanced 64-bit memory controller supporting DDR400 / 333 / 266 SDRAM
  - Combines with VIA VT8235-CE / VT8237 South Bridge for integrated 10/100 LAN, Audio, ATA133 IDE, LPC, USB 2.0 and Serial ATA (VT8237)
  - 1.5V Core and Pentium 4 AGTL+ I/O
  - 37.5 x 37.5mm HSBGA (Ball Grid Array with Heat Spreader) package with 829 balls and 1mm ball pitch
  - Pin compatible with PM800, PM880, PN880, PT800A and PT880 Pentium 4 North Bridges
- **High Performance CPU Interface**
  - Supports Intel 800 / 533 / 400 MHz FSB Pentium 4 and Pentium M processors
  - Supports Intel Hyper-Threading Technology
  - Supports DBI (Dynamic Bus Inversion) and Data, Address, Response Parity
  - Twelve outstanding transactions (twelve level In-Order Queue (IOQ))
  - Built-in Phase Lock Loop circuitry for optimal skew control within and between clocking regions
- **Full Featured Accelerated Graphics Port (AGP) Controller**
  - AGP v3.0 compliant 8x / 4x transfer modes with Fast Write support
  - 1.5V AGP I/O interface
  - Pipelined split-transaction long-burst transfers up to 2.1 GB/sec
  - Supports Side Band Addressing (SBA) mode
  - Supports Flush / Fence commands
  - Supports DBI (Dynamic Bus Inversion)
  - Asynchronous AGP and CPU interface
  - Thirty-two level request queue for read and write
  - One-hundred-twenty-eight level (quadwords) of read data FIFO
  - Sixty-four level (quadwords) of write data FIFO
  - Graphics Address Relocation Table (GART)
    - One level TLB structure
    - Sixteen entry fully associative page table
    - LRU replacement scheme

- **Advanced High-Performance DDR400 SDRAM Controller**
  - Supports DDR400 / 333 / 266 memory types with 2.5V SSTL-2 DRAM interface
  - Supports mixed 64 / 128 / 256 / 512 / 1024Mb DDR SDRAMs in x8 and x16 configurations
  - Supports CL 2 / 2.5 for DDR266 / 333 and CL 2.5 / 3 for DDR400
  - Supports 4 unbuffered or registered double-sided DIMMs and up to 8 GBytes of physical memory
  - Two sets of memory data, address and control signals each of which drives up to 2 DIMMs
  - Programmable timing / drive for memory address, data and control signals independently for each signal set
  - DRAM interface pseudo-synchronous with host CPU for optimal memory performance
  - Concurrent CPU, AGP / integrated graphics controller and V-Link access for minimum memory access latency
  - Bank interleave and up to 16-bank page interleave (i.e., 16 pages open simultaneously) based on LRU to effectively reduce memory access latency
  - Seamless DRAM command scheduling for maximum DRAM bus utilization
    - (e.g., precharge other banks while accessing the current bank)
  - CPU Read-Around-Write capability for non-stalled operation
  - Speculative DRAM read before snoop result to reduce PCI master memory read latency
  - Supports Burst Read and Write operations with burst length of 4 or 8
  - Twelve cache lines (96 quadwords) of integrated CPU-to-DRAM write buffers and twelve separate cache lines of CPU-to-DRAM read prefetch buffers
  - Optional dynamic Clock Enable (CKE) control for DRAM power reduction during normal system state (S0)
  - Supports self-refresh and CAS-before-RAS DRAM refresh with staggered RAS timing
- **High Bandwidth 1 GB / Sec 16-Bit "Ultra V-Link" Host Controller**
  - Supports 66 MHz, 4x and 8x transfer modes, Ultra V-Link Host interface with 1 GB/sec total bandwidth
  - Full duplex transfers with separate command / strobe for 4x and 8x modes
  - Request / Data split transaction
  - Transaction assurance for V-Link Host-to-Client access eliminates V-Link Host-Client Retry cycles
  - Intelligent V-Link transaction protocol to eliminate data wait-states and throttle transfer latency to avoid data overflow
  - Highly efficient V-Link arbitration with minimum overhead
- **Advanced System Power Management Support**
  - ACPI 2.0 and PCI Bus Power Management 1.1 compliant
  - Supports Suspend-to-DRAM (STR) and DRAM self-refresh
  - Supports dynamic Clock Enable (CKE) control for DRAM power reduction during normal system state (S0)
  - Supports SMI, SMM, and STPCLK mechanisms
  - Supports Enhanced Intel Speedstep™ Technology
  - Low-leakage I/O pads

- **Integrated Graphics with 2D / 3D / Video Controllers**
  - Optimized Unified Memory Architecture (UMA)
  - Supports 16 / 32 / 64 MB Frame Buffer sizes
  - 200 MHz Graphics Engine Clock
  - Two independent 128-bit data paths between North Bridge and graphics core to improve video performance, one for frame buffer access and one for texture / command access
  - PCI v2.2 compliant (for control and configuration)
  - AGP v3.0 compliant (for control and data transfer)

2D Acceleration

- 128-bit 2D graphics engine
- Hardware 2D rotation
- Supports ROP3, 256 operations
- Supports 8bpp, 15/16bpp and 32bpp color depth modes
- BitBLT (Bit BLock Transfer) functions including alpha BLTs
- True-color hardware cursor (64x64x32bpp) with 256-level blending effect
- Color expansion, source Color Key and destination Color Key
- Bresenham line drawing / style line function
- Transparency mode
- Window clipping
- Text function

3D Acceleration

3D Graphics Processor

- 128-bit 3D graphics engine
- Dual pixel rendering pipes
- Dual texture units
- Floating-point setup engine
- Internal full 32-bit ARGB format for high rendering quality
- 8K Texture Cache

Capability

- Supports ROP2
- Supports various texture formats including 16/32bpp ARGB, 8bpp Palletized (ARGB), YUV 422/420 and compressed texture (DXTC)
- Texture sizes up to 2048x2048
- Microsoft DirectX texture compression
- High quality texture filter for Nearest, Linear, Bi-linear, Tri-linear, and Anisotropic modes
- Flat and Gouraud shading
- Vertex Fog and Fog Table
- Z-Bias, LOD-Bias, Polygon offset, Edge Anti-aliasing and Alpha Blending
- Bump mapping and cubic mapping
- Hardware back-face culling
- Specular lighting

Performance

- Two textures per pass
- Triangle rate up to 4.5 million triangles per second
- Pixel rate up to 200 million pixels per second for 2 textures each
- Texel bilinear fill rate up to 400 million texels per second
- High quality dithering

Video Acceleration

High Quality Video Processor

- RGB555, RGB565, RGB8888 and YUV422 video playback formats
- High quality 5-tap horizontal and 5-tap vertical scaler (up or down) for both horizontal and vertical scaling (linear interpolation for horizontal and vertical p-scaling and filtering for horizontal and vertical down-scaling)
- Independent graphics and video gamma tables
- 2 sets of Color and Chroma Key support
- Color enhancement for contrast, hue, saturation and brightness
- YUV-to-RGB color space conversion
- Display rotation in clockwise and counter-clockwise directions
- Bob, Weave, Median-filter and Adaptive de-interlacing modes
- 3:2 / 2:2 pull-down detection
- De-blocking mode support
- Combining of many special effects such as filter, scaling up or down, sub-picture blending, de-interlacing and deblocking to one pass process
- Tear-free double / triple buffer flipping
- Input video vertical blanking or line interrupt
- Video gamma correction

Video Overlay

- Simultaneous graphics and TV video playback overlay
- Supports video window overlays
- Supports both YUV and RGB format Chroma Key
- Supports 16 operations for Color and Chroma Key
- Hardware sub-picture blending

MPEG Video Playback

- MPEG-2 hardware VLD (Various Length Decode), iDCT, and motion compensation for full speed DVD and MPEG-2 playback at full D1 resolution
- MPEG-4 ASP (Advanced Simple Profile) Level 5 with GMC (Global Motion Compensation) L0/L1 and ¼ pixel MC support for high video quality and performance
- High quality DVD and streaming video playback
- DVD playback auto-flipping
- DVD sub-picture playback overlay

Video Capture Capability

- 8-bit capture port following ITU-R BT656, VIP 1.1 and VIP 2.0 standards supporting 16 / 32-bit RGB and YUV422 video capture formats
- Video capture and playback tear free auto flipping
- Multiplexed on Digital Video Port 0 (DVP0 selectable as Capture-In or TV-Out)
- External Hsync / Vsync support

• Advanced Graphics Power Management Support

- Built-in reference voltage generator and monitor sense circuits
- Automatic panel power sequencing and VESA DPMS (Display Power Management Signaling) CRT power-down
- External I/O signal controls enabling of graphics accelerator into standby / suspend-off state
- Dynamic clock gating for inactive functions to achieve maximum power savings
- I^2C Serial Bus and DDC / E-DDC Monitor Communications for Plug-and-Play configuration

- **Extensive Display Support for External Video Output**
  - CRT display interface
  - Digital Video Port with support for TV Out or Video Capture In
  - Digital Video Port with support for TV Out or external TMDS transmitter
  - 24-bit / Dual-12-Bit FPD interface to external LVDS transmitter

  Two Display Engines
  - Provides two independent display engines, each of which can display completely different information at different resolutions, pixel depths, and refresh rates (supports different images on different displays simultaneously)
  - CRT, FPD, DVI monitor and TV refresh rates are independently programmable for optimum image quality
  - Improved display flexibility with simultaneous FPD / CRT, FPD / TV, FPD / DVI and other combined operations

  CRT Display
  - CRT display interface with 24-bit true-color RAMDAC up to 350 MHz pixel rate with gamma correction capability
  - Supports CRT resolutions up to 1920 x 1440

  TV-Out Interface
  - 12-bit interface to external TV encoder for ATSC, NTSC or PAL TV display
  - Selectable to use either Digital Video Port 0 (DVP0) or Digital Video Port 1 (GDVP1)
  - Supports 3.3V signaling on DVP0 and 1.5V signaling on GDVP1

  12-Bit TMDS Transmitter Interface
  - Option of AGP-multiplexed digital video port 1 (GDVP1) when that port is not being used for TV out
  - Supports external TMDS transmitter for a driving a DVI monitor
  - Double-data-rate data transfer with clock rates up to 165 MHz
  - Built-in digital phase adjuster to fine-tune signal timing between clock and data bus

  24-Bit Flat Panel Display (FPD) Interface
  - Multiplexed with external AGP port pins
  - Supports 18/24-bit FPD interface with external LVDS transmitter chip using single or double-data rate data transfer
  - Supports panel resolutions up to 1600x1200

  Dual 12-Bit Flat Panel Display (FPD) Interface
  - Alternate operating mode of FPD interface with external LVDS transmitters
  - Single or separate sets of clock and sync signals
  - Supports panel resolutions up to 1600x1200

- **Full Software Support**
  - Microsoft DirectX 7.0, 8.0 and 9.0 compatible
  - Microsoft DirectX Texture Compression (DXTC / S3TC)
  - Supports OpenGL™
  - Drivers for major operating systems and APIs: Windows® 9x/ME, Windows 2000, Windows XP, Direct3D™, DirectDraw™, DirectShow™, and OpenGL™ ICD for Windows 9x/ME and XP
  - Windows NT 4.0 Standard VGA driver

- **DuoView+™ Dual Image Capability**
  - WinXP, WinME and Win98 multi-monitor, extended desktop support
  - Independent resolution, refresh rate and color depth for secondary desktop

OVERVIEW

The PN800 is a high performance, cost-effective and energy efficient UMA North Bridge with integrated UniChrome Pro graphics / video controllers used for the implementation of mobile personal computer systems based on 800 / 533 / 400 MHz FSB Intel Pentium 4 and Pentium M super-scalar processors.

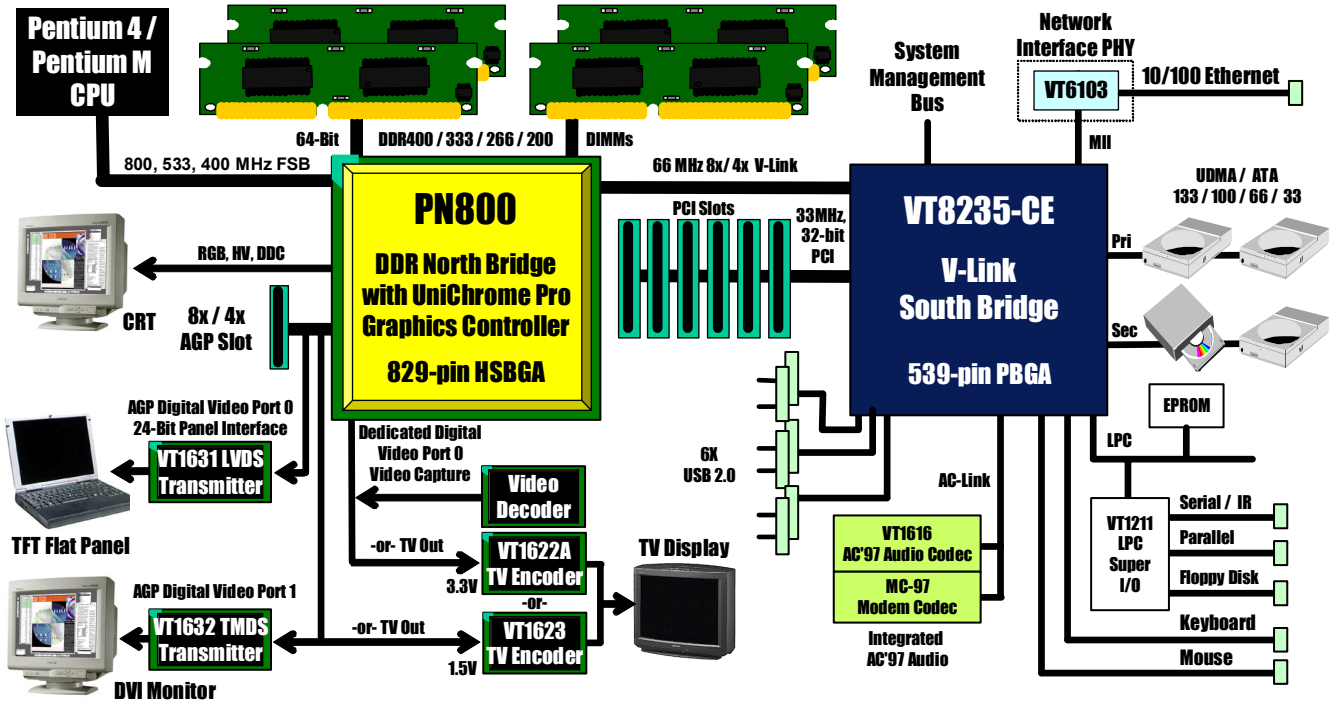


Figure 1. System Block Diagram

The complete mobile chipset consists of the **PN800** North Bridge (829 pin HSBGA) and the **VT8235-CE** V-Link South Bridge (539-pin BGA). The PN800 integrates VIA's PT800 system controller with high-performance UniChrome Pro 3D/2D graphics accelerator plus flat panel, DVI monitor and TV out interfaces. The PN800 provides superior performance between the CPU, DRAM, V-Link bus and internal AGP 8x graphics controller bus with pipelined, burst, and concurrent operation. The VT8235-CE is a highly integrated peripheral controller which includes V-Link-to-PCI / V-Link-to-LPC controllers, Ultra DMA IDE controller, USB2.0 host controller, 10/100Mb networking MAC, AC97, and system power management controllers.

Host CPU Interface

The PN800 supports 800 / 533 / 400 MHz FSB Intel Pentium 4 and Pentium M super-scalar processors. It implements a twelve level In-Order-Queue and supports Intel Hyper-Threading Technology to maximize system performance for multi-threaded software applications. DBI and Pentium M bus protocol, as well as Intel SpeedStep Technology, are supported which effectively reduce overall system power consumption.

AGP Interface

The PN800 AGP controller is AGP 3.0 compliant with up to 2.1 GB / second data transfer rate capability. It supports asynchronous AGP and CPU interfaces for flexible system configuration. Deep read (1024 byte) and write (512 byte) FIFOs are integrated for optimal bus utilization and minimum data transfer latency.

Memory Controller

The PN800 SDRAM Controller supports two sets of 64-bit memory data, address and control signals to minimize signal loading and up to 4 double-sided DDR400 / 333 / 266 DIMMs for 8 GB maximum physical memory. The DDR DRAM interface allows zero wait-state data transfer bursting between the DRAM and the memory controller's data buffers. The different banks of DRAM can be composed of an arbitrary mixture of 64 / 128 / 256 / 512 / 1024Mb DRAMs in x8 and x16 configurations. The DRAM controller can run either synchronous or pseudo-synchronous with the host CPU bus. The PN800 North Bridge is pin compatible with the PN880 North Bridge which connects to the memory modules in exactly the same manner while supporting true 128-bit operation (simultaneous memory access on both sets of 64-bit memory data / address / control signals).

Ultra V-Link

The PN800 North Bridge interfaces to the South Bridge through a high speed (up to 1 GB/sec) 8x, 66 MHz Data Transfer interconnect bus called "Ultra V-Link". Deep pre-fetch and post-write buffers are included to allow for concurrent CPU and V-Link operation. The combined PN800 North Bridge and VT8235-CE South Bridge system supports enhanced PCI bus commands such as "Memory-Read-Line", "Memory-Read-Multiple" and "Memory-Write-Invalid" commands to minimize snoop overhead. In addition, advanced features are supported such as CPU write-back forward to PCI master, and CPU write-back merged with PCI post write buffers to minimize PCI master read latency and DRAM utilization. Delay transaction and read caching mechanisms are also implemented for further improvement of overall system performance.

System Power Management

For sophisticated power management, the PN800 supports dynamic CKE control to minimize DDR SDRAM power consumption during normal system state (S0). A separate suspend power plane is implemented for the memory control logic for Suspend-to-DRAM state. Enhanced Intel SpeedStep™ Technology enables minimization of CPU power consumption while sustaining processing power. The PN800 graphics accelerator implements dynamic clock gating for inactive functions to achieve maximum power savings. The system can also be switched to standby or suspend states to further reduce power consumption when idle. Automatic panel power sequencing and VESA DPMS (Display Power Management Signaling) CRT power-down are supported. Coupled with the VT8235-CE South Bridge chip, a complete power conscious PC main board can be implemented with no external glue logic.

3D Graphics Engine

Featuring an integrated 128-bit 3D graphics engine, the PN800 North Bridge utilizes a highly pipelined architecture that provides high performance along with superior image quality. Several new features enhance the 3D architecture, including two pixel rendering pipes, single-pass multitexturing, bump and cubic mapping, texture compression, edge anti-aliasing, vertex fog and fog table, hardware back-face culling, specular lighting, anisotropic filtering, and an 8-bit stencil buffer. The chip also offers the industry's only simultaneous usage of single-pass multitexturing and single-cycle trilinear filtering – enabling stunning image quality without performance loss. Image quality is further enhanced with true 32-bit color rendering throughout the 3D pipeline to produce more vivid and realistic images. The advanced triangle setup engine provides industry leading 3D performance for a realistic user experience in games and other interactive 3D applications. The 3D engine is optimized for AGP texturing from system memory.

128-bit 2D Graphics Engine

The PN800 North Bridge's advanced 128-bit 2D graphics engine delivers high-speed 2D acceleration for productivity applications. The enhanced 2D architecture with direct access frame buffer capability optimizes UMA performance and provides acceleration of all color depths.

MPEG Playback

The PN800 North Bridge provides the ideal architecture for high quality MPEG-2 based video applications. For MPEG video playback, the integrated video engine offloads the CPU by performing planar-to-packed format conversion and motion video compensation tasks, while its enhanced scaling algorithm delivers incredible full-screen video playback.

Video Capture

The PN800 North Bridge implements an optional Video Capture Port which supports various video capture standards, including ITU-R BT656, VIP 1.1 and VIP 2.0 and is compliant with the most common video capture formats: 16 / 32-bit RGB and

YUV422. With the integrated video capture feature, the PN800 can provide high performance video effects for video capturing and playback.

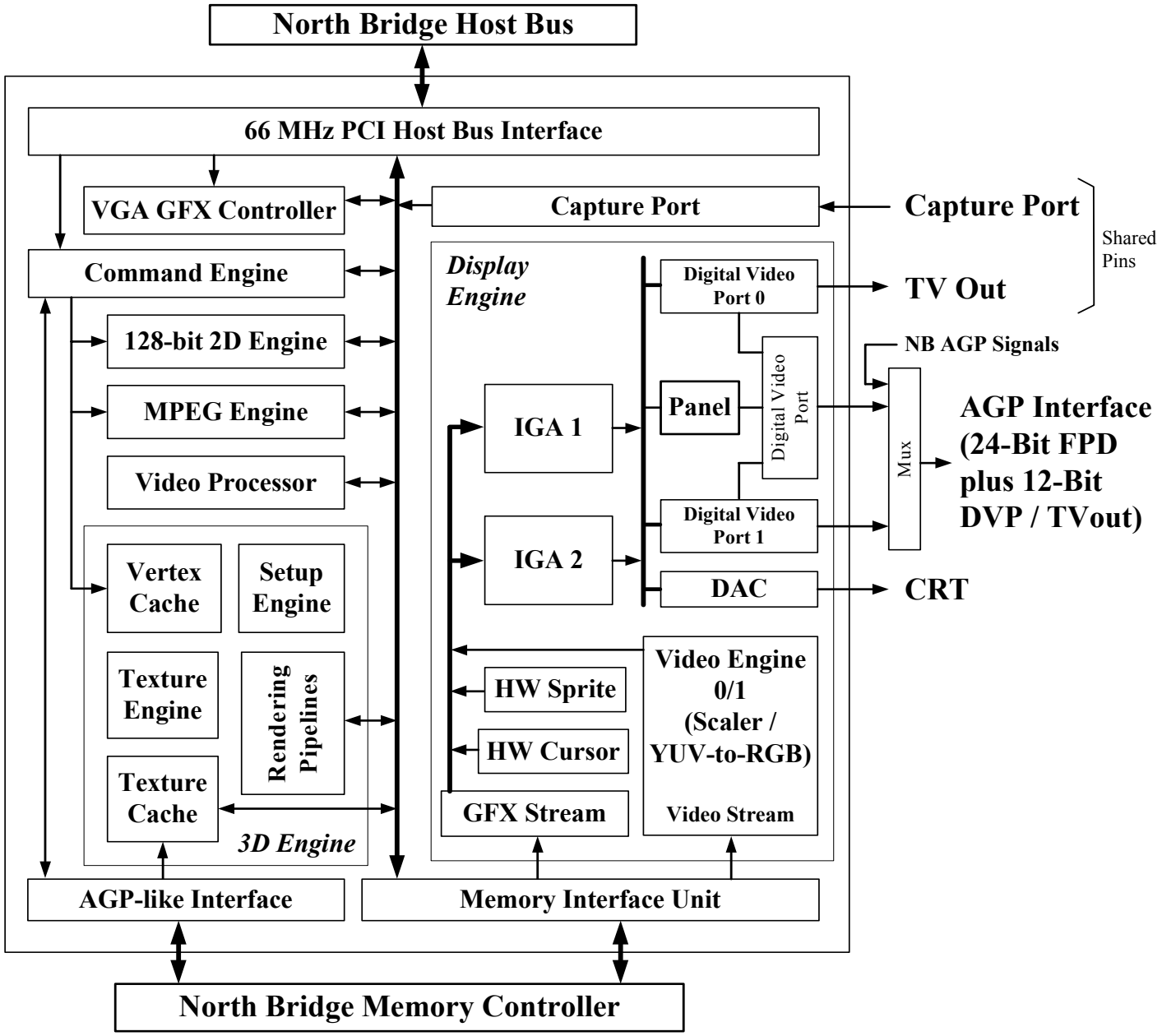


Figure 2. Integrated UniChrome Pro Graphics Controller Internal Block Diagram

LCD, DVI Monitor and TV Output Display Support

The PN800 provides three "Digital Video Port" interfaces: FPDP, GDVP1, and DVP0. The Flat Panel Display Port (FPDP) implements a 24-bit / dual 12-bit interface which is designed to drive a Flat Panel Display via an external LVDS transmitter chip (such as the VIA VT1631, NSC DS90C387R or Chrontel CH7017). The PN800 can be connected to the external LVDS transmitter chip in either 24-bit or dual-12-bit modes. A wide variety of LCD panels are supported including VGA, SVGA, XGA, SXGA+ and up to UXGA-resolution TFT color panels, in either SDR (1 pixel / clock) or DDR (2 pixels / clock) modes. UXGA and higher resolutions require dual-edge data transfer (DDR) mode which is supported by the VIA VT1631 LVDS transmitter chip

Digital Video Port 0 (DVP0) is normally used for interfacing to a TV encoder (such as the VIA VT1622A or VT1622AM using 3.3V signal levels), however if DVP0 is used for video capture, Digital Video Port 1 (GDVP1) may be configured for support of

an external TV encoder (VIA VT1623 or VT1623M using low-voltage 1.5V signal levels). If GDVP1 is not being used for TV out, it can optionally be used to drive a DVI monitor via an external TMDS transmitter chip (such as the VIA VT1632)

The flexible display configurations of the PN800 allow support of a flat panel (LVDS interface) or flat panel monitor (TMDS / DVI interface), TV display, and CRT display at the same time. Internally the PN800 North Bridge provides two separate display engines, so if two display devices are connected, each can display completely different information at different resolutions, pixel depths and refresh rates. If more than two display devices are connected, the additional displays must have the same resolution, pixel depth, and refresh rate as one of the first two. The maximum display resolutions supported for one display device are listed in the table below. If more than one display is implemented (i.e., if both display engines are functioning at the same time), then available memory bandwidth may limit the display resolutions supported on one or both displays. This will be dependent on many factors including primarily clock rates and memory speeds (contact VIA for additional information).

High Screen Resolution Display Support

Resolutions Supported	Resolution Name	Pixel Depths Supported	System Memory Frame Buffer Size		
			16 MB	32 MB	64 MB
640x480 (4:3)	VGA	8 / 16 / 32	✔	✔	✔
800x600 (4:3)	SVGA	8 / 16 / 32	✔	✔	✔
1024x768 (4:3)	XGA	8 / 16 / 32	✔	✔	✔
1280x1024 (5:4)	SXGA	8 / 16 / 32	✔	✔	✔
1400x1050 (4:3)	SXGA+	8 / 16 / 32	✔	✔	✔
1600x1200 (4:3)	UXGA, UXGA+	8 / 16 / 32	✔	✔	✔
1920x1440 (4:3)	n/a	8 / 16	✔	✔	✔

Table 1. Supported CRT and Panel Screen Resolutions

PINOUTS **Pin Diagrams**

Figure 3. Ball Diagram (Top View) – Flat Panel / Digital Video Output Enabled (No External AGP Interface)

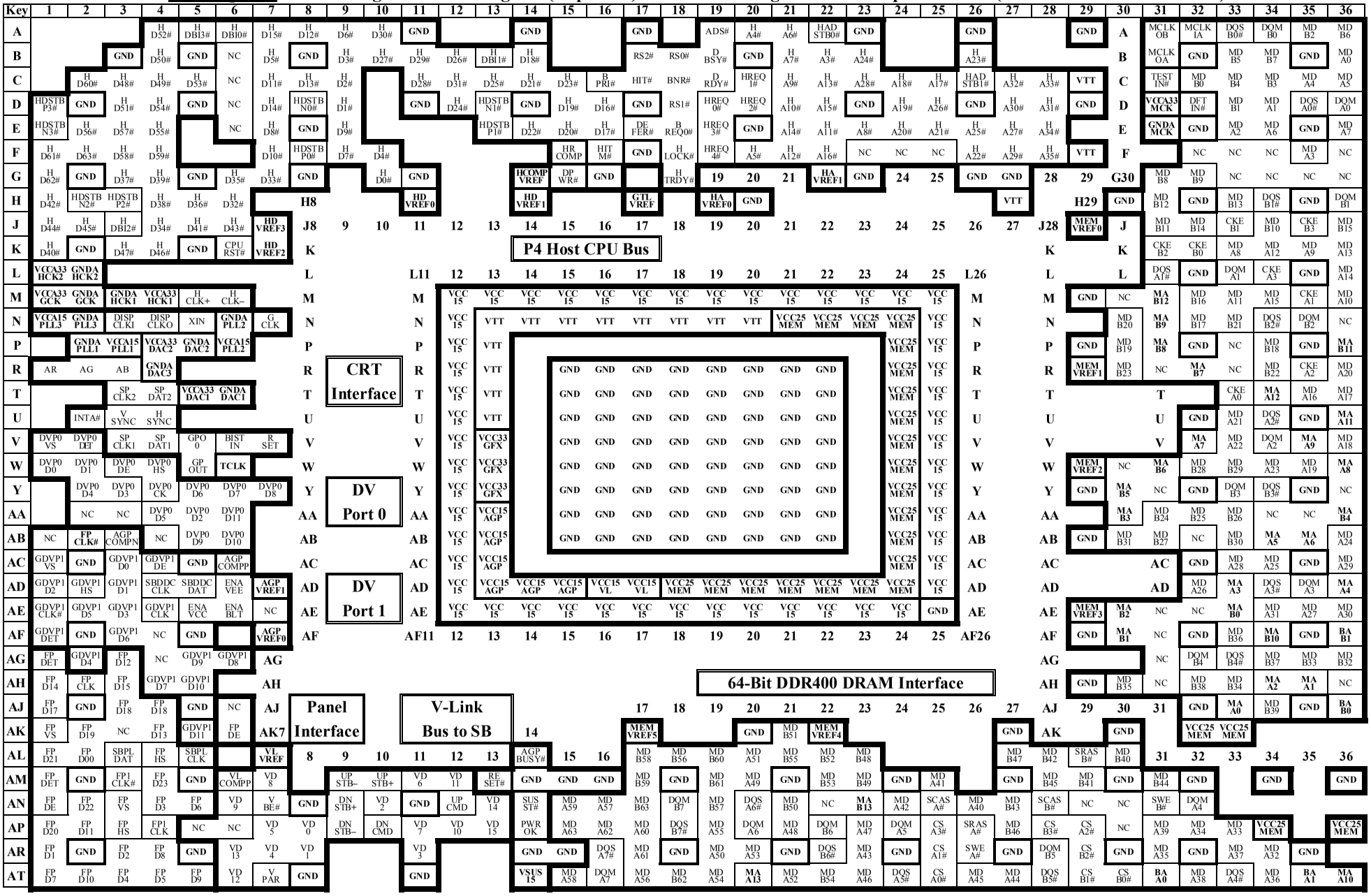
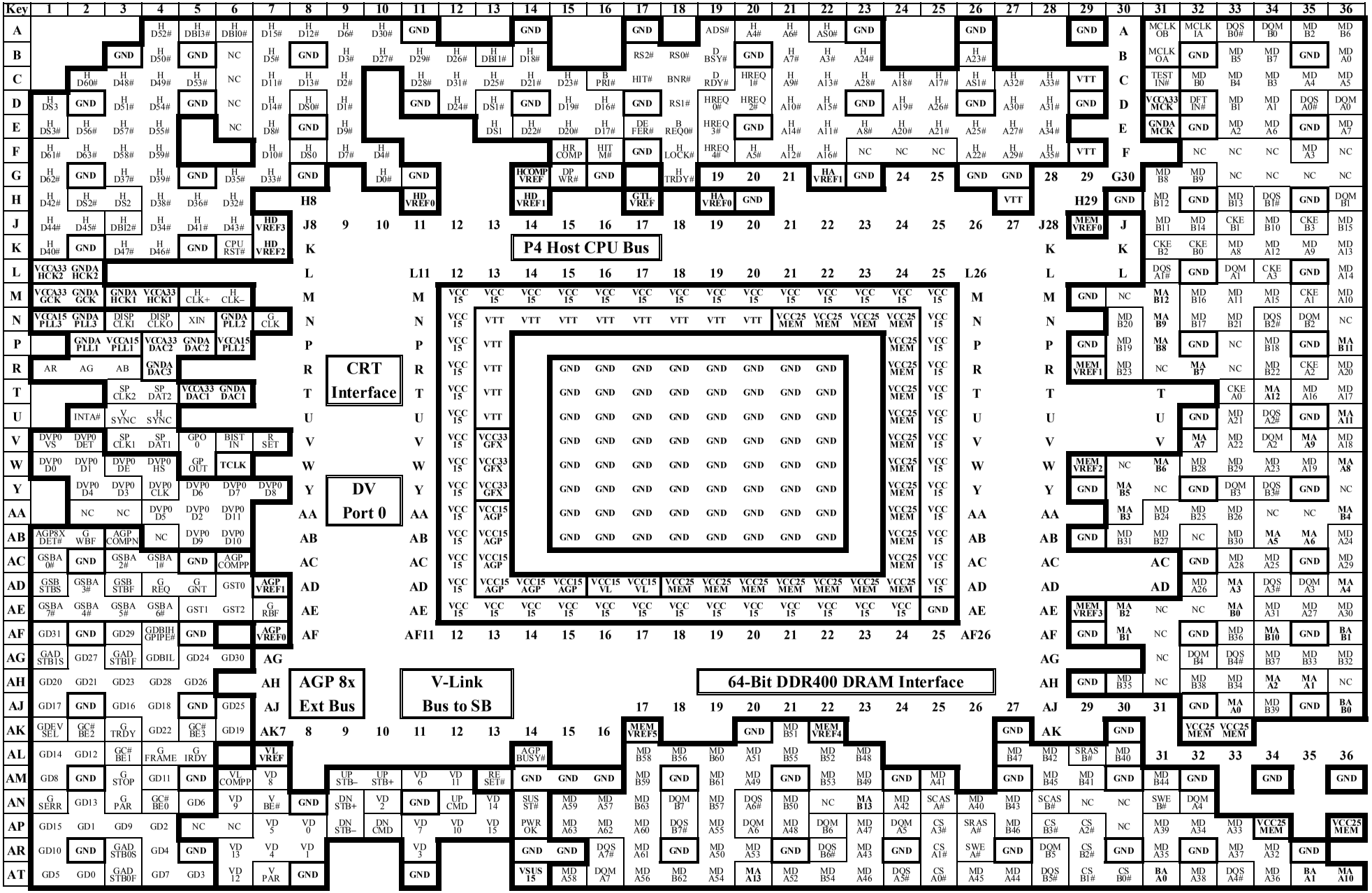


Figure 4. Ball Diagram (Top View) - External AGP Interface Enabled on Display Pins



Pin Lists

Table 2. Signal Pin List (Numerical Order) - Display Functions Enabled

Pin #		Pin Name	Pin #		Pin Name	Pin #		Pin Name	Pin #		Pin Name	Pin #		Pin Name	Pin #		Pin Name
A04	IO	HD52#	D32	I	DFTIN#	J34	IO	MDB10	Y02	O	DVP0D04 / TVD04	AH02	O	FPCLK	AN31	O	SWEB#
A05	IO	HDBI3#	D33	IO	MDB01	J35	O	CKEB3	Y03	O	DVP0D03 / TVD03	AH03	O	FPD15	AN32	O	DQMA4
A06	IO	HDBI0#	D34	IO	MDA01	J36	IO	MDB15	Y04	O	DVP0CLK / TVCLK	AH04	O	GDVP1D07	AP01	O	FPD20
A07	IO	HD15#	D35	IO	DQSA0#	K01	IO	HD40#	Y05	O	DVP0D06 / TVD06	AH05	O	GDVP1D10	AP02	O	FPD11
A08	IO	HD12#	D36	O	DQMA0	K03	IO	HD47#	Y06	O	DVP0D07 / TVD07	AH30	IO	MDB35	AP03	O	FP1HS
A09	IO	HD06#	E01	IO	HDSTBN3#	K04	IO	HD46#	Y07	O	DVP0D08 / TVD08	AH31	–	NC	AP04	O	FP1CLK
A10	IO	HD30#	E02	IO	HD56#	K06	O	CPURST#	Y30	O	MAB05	AH32	IO	MDB38	AP05	–	NC
A19	IO	ADS#	E03	IO	HD57#	K31	O	CKEB2	Y31	–	NC	AH33	IO	MDB34	AP06	–	NC
A20	IO	HA04#	E04	IO	HD55#	K32	O	CKEB0	Y33	O	DQMB3	AH34	O	MAA02	AP07	IO	VAD05
A21	IO	HA06#	E06	–	NC	K33	IO	MDA08	Y34	IO	DQSB3#	AH35	O	MAA01	AP08	IO	VAD00
A22	IO	HADSTB0#	E07	IO	HD08#	K34	IO	MDA12	Y36	–	NC	AH36	–	NC	AP09	O	DNSTB–
A31	O	MCLKOB	E09	IO	HD09#	K35	IO	MDA09	AA02	–	NC	AJ01	O	FPD17	AP10	O	DNCMD
A32	I	MCLKIA	E13	IO	HDSTBP1#	K36	IO	MDA13	AA03	–	NC	AJ03	O	FPD18	AP11	IO	VAD07
A33	IO	DQSB0#	E14	IO	HD22#	L31	IO	DQSA1#	AA04	O	DVP0D05 / TVD05	AJ04	O	FPD16	AP12	IO	VAD10
A34	O	DQMB0	E15	IO	HD20#	L33	O	DQMA1	AA05	O	DVP0D02 / TVD02	AJ06	–	NC	AP13	IO	VAD15
A35	IO	MDB02	E16	IO	HD17#	L34	O	CKEA3	AA06	O	DVP0D11 / TVD11	AJ33	O	MAA00	AP14	I	PWROK
A36	IO	MDB06	E17	IO	DEFER#	L36	IO	MDA14	AA30	O	MAB03	AJ34	IO	MDB39	AP15	IO	MDA63
B04	IO	HD50#	E18	O	BREQ0#	M05	I	HCLK+	AA31	IO	MDB24	AJ36	O	BAB0	AP16	IO	MDA62
B06	–	NC	E19	IO	HREQ3#	M06	I	HCLK–	AA32	IO	MDB25	AK01	O	FPVS	AP17	IO	MDA60
B07	IO	HD05#	E21	IO	HA14#	M30	–	NC	AA33	IO	MDB26	AK02	O	FPD19	AP18	IO	DQSB7#
B09	IO	HD03#	E22	IO	HA11#	M31	O	MAB12	AA34	–	NC	AK03	–	NC	AP19	IO	MDA55
B10	IO	HD27#	E23	IO	HA08#	M32	IO	MDB16	AA35	–	NC	AK04	O	FPD13	AP20	O	DQMA6
B11	IO	HD29#	E24	IO	HA20#	M33	IO	MDA11	AA36	O	MAB04	AK05	O	GDVP1D11	AP21	IO	MDA48
B12	IO	HD26#	E25	IO	HA21#	M34	IO	MDA15	AB01	–	NC	AK06	O	FPDE	AP22	O	DQMB6
B13	IO	HDBI1#	E26	IO	HA25#	M35	O	CKEA1	AB02	O	FPCLK#	AK21	IO	MDB51	AP23	IO	MDA47
B14	IO	HD18#	E27	IO	HA27#	M36	IO	MDA10	AB03	AI	AGPCOMPN	AL01	O	FPD21	AP24	O	DQMA5
B17	IO	RS2#	E28	IO	HA34#	N03	I	DISPCLKI	AB04	–	NC	AL02	O	FPD00	AP25	O	CSA3#
B18	IO	RS0#	E33	IO	MDA02	N04	O	DISPCLKO	AB05	O	DVP0D09 / TVD09	AL03	IO	SBPLDAT	AP26	O	SRASA#
B19	IO	DBSY#	E34	IO	MDA06	N05	I	XIN	AB06	O	DVP0D10 / TVD10	AL04	O	FPHS	AP27	IO	MDB46
B21	IO	HA07#	E36	IO	MDA07	N07	I	GCLK	AB30	IO	MDB31	AL05	IO	SBPLCLK	AP28	O	CSB3#
B22	IO	HA03#	F01	IO	HD61#	N30	IO	MDB20	AB31	IO	MDB27	AL14	O	AGPBUSY#	AP29	O	CSA2#
B23	IO	HA24#	F02	IO	HD63#	N31	O	MAB09	AB32	–	NC	AL17	IO	MDB58	AP30	–	NC
B26	IO	HA23#	F03	IO	HD58#	N32	IO	MDB17	AB33	IO	MDB30	AL18	IO	MDB56	AP31	IO	MDA39
B31	O	MCLKOA	F04	IO	HD59#	N33	IO	MDB21	AB34	O	MAA05	AL19	IO	MDB60	AP32	IO	MDA34
B33	IO	MDB05	F07	IO	HD10#	N34	IO	DQSB2#	AB35	O	MAA06	AL20	IO	MDA51	AP33	IO	MDA33
B34	IO	MDB07	F08	IO	HDSTBP0#	N35	O	DQMB2	AB36	IO	MDA24	AL21	IO	MDB55	AR01	O	FPD01
B36	IO	MDA00	F09	IO	HD07#	N36	–	NC	AC01	O	GDVP1VS	AL22	IO	MDB52	AR03	O	FPD02
C02	IO	HD60#	F10	IO	HD04#	P30	IO	MDB19	AC03	O	GDVP1D00	AL23	IO	MDB48	AR04	O	FPD08
C03	IO	HD48#	F15	AI	HRCOMP	P31	O	MAB08	AC04	O	GDVP1DE	AL27	IO	MDB47	AR06	IO	VAD13
C04	IO	HD49#	F16	I	HITM#	P33	–	NC	AC06	AI	AGPCOMPP	AL28	IO	MDB42	AR07	IO	VAD04
C05	IO	HD53#	F18	I	HLOCK#	P34	IO	MDB18	AC33	IO	MDA28	AL29	O	SRASB#	AR08	IO	VAD01
C06	–	NC	F19	IO	HREQ4#	P36	O	MAB11	AC34	IO	MDA25	AL30	IO	MDB40	AR11	IO	VAD03
C07	IO	HD11#	F20	IO	HA05#	R01	AO	AR	AC36	IO	MDA29	AM01	I	FP1DET	AR16	IO	DQSA7#
C08	IO	HD13#	F21	IO	HA12#	R02	AO	AG	AD01	O	GDVP1D02	AM03	I	FP1CLK#	AR17	IO	MDA61
C09	IO	HD02#	F22	IO	HA16#	R03	AO	AB	AD02	O	GDVP1HS	AM04	O	FPD23	AR19	IO	MDA50
C11	IO	HD28#	F23	–	NC	R30	IO	MDB23	AD03	O	GDVP1D01	AM06	AI	VLCOMPP	AR20	IO	MDA53
C12	IO	HD31#	F24	–	NC	R31	–	NC	AD04	IO	SBDDCCLK	AM07	IO	VAD08	AR22	IO	DQSB6#
C13	IO	HD25#	F25	–	NC	R32	O	MAB07	AD05	IO	SBDDCDAT	AM09	I	UPSTB–	AR23	IO	MDA43
C14	IO	HD21#	F26	IO	HA22#	R33	–	NC	AD06	O	ENAVEE	AM10	I	UPSTB+	AR25	O	CSA1#
C15	IO	HD23#	F27	IO	HA29#	R34	IO	MDB22	AD32	IO	MDA26	AM11	IO	VAD06	AR26	O	SWEA#
C16	IO	BPRI#	F28	IO	HA35#	R35	O	CKEA2	AD33	O	MAA03	AM12	IO	VAD11	AR28	O	DQMB5
C17	IO	HIT#	F32	–	NC	R36	IO	MDA20	AD34	IO	DQSA3#	AM13	I	RESET#	AR29	O	CSB2#
C18	IO	BNR#	F33	–	NC	T03	IO	SPCLK2	AD35	O	DQMA3	AM17	IO	MDB59	AR31	IO	MDA35
C19	IO	DRDY#	F34	–	NC	T04	IO	SPDAT2	AD36	O	MAA04	AM19	IO	MDB61	AR33	IO	MDA37
C20	IO	HREQ1#	F35	IO	MDA03	T33	O	CKEA0	AE01	O	GDVP1CLK#	AM20	IO	MDA49	AR34	IO	MDA32
C21	IO	HA09#	F36	–	NC	T34	O	MAA12	AE02	O	GDVP1D05	AM22	IO	MDB53	AT01	O	FPD07
C22	IO	HA13#	G01	IO	HD62#	T35	IO	MDA16	AE03	O	GDVP1D03	AM23	IO	MDB49	AT02	O	FPD10
C23	IO	HA28#	G03	IO	HD37#	T36	IO	MDA17	AE04	O	GDVP1CLK	AM25	IO	MDA41	AT03	O	FPD04
C24	IO	HA18#	G04	IO	HD39#	U02	O	INTA#	AE05	O	ENAVDD	AM28	IO	MDB45	AT04	O	FPD05
C25	IO	HA17#	G06	IO	HD35#	U03	O	VSYNC	AE06	O	ENABLT	AM29	IO	MDB41	AT05	O	FPD09
C26	IO	HADSTB1#	G07	IO	HD33#	U04	O	HSYNC	AE07	–	NC	AM31	IO	MDB44	AT06	IO	VAD12
C27	IO	HA32#	G10	IO	HD00#	U33	IO	MDA21	AE30	O	MAB02	AN01	O	FP1DE	AT07	IO	VPAR
C28	IO	HA33#	G15	O	DPWR#	U34	IO	DQSA2#	AE31	–	NC	AN02	O	FPD22	AT15	IO	MDA58
C31	I	TESTIN#	G18	IO	HTRDY#	U36	O	MAA11	AE32	–	NC	AN03	O	FP1VS	AT16	O	DQMA7
C32	IO	MDB00	G31	IO	MDB08	V01	O	DVP0VS / TVVS	AE33	O	MAB00	AN04	O	FPD03	AT17	IO	MDA56
C33	IO	MDB04	G32	IO	MDB09	V02	I	DVP0DET/TVCKI	AE34	IO	MDA31	AN05	O	FPD06	AT18	IO	MDB62
C34	IO	MDB03	G33	–	NC	V03	IO	SPCLK1	AE35	IO	MDA27	AN06	IO	VAD09	AT19	IO	MDA54
C35	IO	MDA04	G34	–	NC	V04	IO	SPDAT1	AE36	IO	MDA30	AN07	IO	VBE#	AT20	O	MAA13
C36	IO	MDA05	G35	–	NC	V05	O	GPO0	AF01	I	GDVP1DET	AN09	O	DNSTB+	AT21	IO	MDA52
D01	IO	HDSTBP3#	G36	–	NC	V06	I	BISTIN	AF03	O	GDVP1D06	AN10	IO	VAD02	AT22	IO	MDB54
D03	IO	HD51#	H01	IO	HD42#	V07	AI	RSET	AF04	–	NC	AN12	I	UPCMD	AT23	IO	MDA46
D04	IO	HD54#	H02	IO	HDSTBN2#	V32	O	MAA07	AF30	O	MAB01	AN13	IO	VAD14	AT24	IO	DQSA5#
D06	–	NC	H03	IO	HDSTBP2#	V33	IO	MDA22	AF31	–	NC	AN14	I	SUSST#	AT25	O	CSA0#
D07	IO	HD14#	H04	IO	HD38#	V34	O	DQMA2	AF33	IO	MDB36	AN15	IO	MDA59	AT26	IO	MDA45
D08	IO	HDSTBN0#	H05	IO	HD36#	V35	O	MAA09	AF34	O	MAB10	AN16	IO	MDA57	AT27	IO	MDA44
D09	IO	HD01#	H06	IO	HD32#	V36	IO	MDA18	AF36	O	BAB1	AN17	IO	MDB63	AT28	IO	DQSB5#
D12	IO	HD24#	H31	IO	MDB12	W01	O	DVP0D00 /TVD00	AG01	I	FPDET	AN18	O	DQMB7	AT29	O	CSB1#
D13	IO	HDSTBN1#	H33	IO	MDB13	W02	O	DVP0D01 /TVD01	AG02	O	GDVP1D04	AN19	IO	MDB57	AT30	O	CSB0#
D15	IO	HD19#	H34	IO	DQSB1#	W03	O	DVP0DE / TVDE	AG03	O	FPD12	AN20	IO	DQSA6#	AT31	O	BAA0
D16	IO	HD16#	H36	O	DQMB1	W04	O	DVP0HS / TVHS	AG04	–	NC	AN21	IO	MDB50	AT32	IO	MDA38
D18	IO	RS1#	J01	IO	HD44#	W05	O	GPOUT	AG05	O	GDVP1D09	AN22	–	NC	AT33	IO	DQSA4#
D19	IO	HREQ0#	J02	IO	HD45#	W06	I	TCLK	AG06	O	GDVP1D08	AN23	O	MAB13	AT34	IO	MDA36
D20	IO	HREQ2#	J03	IO	HDBI2#	W30	–	NC	AG31	–	NC	AN24	IO	MDA42	AT35	O	BAA1
D21	IO	HA10#	J04	IO	HD34#	W31	O	MAB06	AG32	O	DQMB4	AN25	O	SCASA#	AT36	O	MAA10
D22	IO	HA15#	J05	IO	HD41#	W32	IO	MDB28	AG33	IO	DQSB4#	AN26	IO	MDA40			
D24	IO	HA19#	J06	IO	HD43#	W33	IO	MDB29	AG34	IO	MDB37	AN27	IO	MDB43			
D25	IO	HA26#	J31	IO	MDB11	W34	IO	MDA23	AG35	IO	MDB33	AN28	O	SCASB#			
D27	IO	HA30#	J32	IO	MDB14	W35	IO	MDA19	AG36	IO	MDB32	AN29	–	NC			
D28	IO	HA31#	J33	O	CKEB1	W36	O	MAA08	AH01	O	FPD14	AN30	–	NC			

Table 3. Signal Pin List (Alphabetical Order) - Display Functions Enabled

Pin #		Pin Name	Pin #		Pin Name	Pin #		Pin Name	Pin #		Pin Name	Pin #		Pin Name	Pin #		Pin Name
R03	AO	AB	W04	O	DVP0HS / TVHS	D27	IO	HA30#	F15	AI	HRCOMP	AM20	IO	MDA49	F36	–	NC
A19	IO	ADS#	V01	O	DVP0VS / TVVS	D28	IO	HA31#	D19	IO	HREQ0#	AR19	IO	MDA50	G33	–	NC
R02	AO	AG	AE06	O	ENABLT	C27	IO	HA32#	C20	IO	HREQ1#	AL20	IO	MDA51	G34	–	NC
AL14	O	AGPBUSY#	AE05	O	ENAVDD	C28	IO	HA33#	D20	IO	HREQ2#	AT21	IO	MDA52	G35	–	NC
AB03	AI	AGPCOMPN	AD06	O	ENAVEE	E28	IO	HA34#	E19	IO	HREQ3#	AR20	IO	MDA53	G36	–	NC
AC06	AI	AGPCOMPP	AP04	O	FP1CLK	F28	IO	HA35#	F19	IO	HREQ4#	AT19	IO	MDA54	M30	–	NC
R01	AO	AR	AM03	O	FP1CLK#	A22	IO	HADSTB0#	U04	O	HSYNC	AP19	IO	MDA55	N36	–	NC
AT31	O	BAA0	AN01	O	FP1DE	C26	IO	HADSTB1#	G18	IO	HTRDY#	AT17	IO	MDA56	P33	–	NC
AT35	O	BAA1	AM01	I	FP1DET	M05	I	HCLK+	U02	O	INTA#	AN16	IO	MDA57	R31	–	NC
AJ36	O	BAB0	AP03	O	FP1HS	M06	I	HCLK–	AJ33	O	MAA00	AT15	IO	MDA58	R33	–	NC
AF36	O	BAB1	AN03	O	FP1VS	G10	IO	HD00#	AH35	O	MAA01	AN15	IO	MDA59	W30	–	NC
V06	I	BISTIN	AH02	O	FPCLK	D09	IO	HD01#	AH34	O	MAA02	AP17	IO	MDA60	Y31	–	NC
C18	IO	BNR#	AB02	O	FPCLK#	C09	IO	HD02#	AD33	O	MAA03	AR17	IO	MDA61	Y36	–	NC
C16	IO	BPRI#	AL02	O	FPD00	B09	IO	HD03#	AD36	O	MAA04	AP16	IO	MDA62	AA02	–	NC
E18	O	BREQ0#	AR01	O	FPD01	F10	IO	HD04#	AB34	O	MAA05	AP15	IO	MDA63	AA03	–	NC
T33	O	CKEA0	AR03	O	FPD02	B07	IO	HD05#	AB35	O	MAA06	C32	IO	MDB00	AA34	–	NC
M35	O	CKEA1	AN04	O	FPD03	A09	IO	HD06#	V32	O	MAA07	D33	IO	MDB01	AA35	–	NC
R35	O	CKEA2	AT03	O	FPD04	F09	IO	HD07#	W36	O	MAA08	A35	IO	MDB02	AB01	–	NC
L34	O	CKEA3	AT04	O	FPD05	E07	IO	HD08#	V35	O	MAA09	C34	IO	MDB03	AA04	–	NC
K32	O	CKEB0	AN05	O	FPD06	E09	IO	HD09#	AT36	O	MAA10	C33	IO	MDB04	AB32	–	NC
J33	O	CKEB1	AT01	O	FPD07	F07	IO	HD10#	U36	O	MAA11	B33	IO	MDB05	AE07	–	NC
K31	O	CKEB2	AR04	O	FPD08	C07	IO	HD11#	T34	O	MAA12	A36	IO	MDB06	AE31	–	NC
J35	O	CKEB3	AT05	O	FPD09	A08	IO	HD12#	AT20	O	MAA13	B34	IO	MDB07	AE32	–	NC
K06	O	CPURST#	AT02	O	FPD10	C08	IO	HD13#	AE33	O	MAB00	G31	IO	MDB08	AF04	–	NC
AT25	O	CSA0#	AP02	O	FPD11	D07	IO	HD14#	AF30	O	MAB01	G32	IO	MDB09	AF31	–	NC
AR25	O	CSA1#	AG03	O	FPD12	A07	IO	HD15#	AE30	O	MAB02	J34	IO	MDB10	AG04	–	NC
AP29	O	CSA2#	AK04	O	FPD13	D16	IO	HD16#	AA30	O	MAB03	J31	IO	MDB11	AG31	–	NC
AP25	O	CSA3#	AH01	O	FPD14	E16	IO	HD17#	AA36	O	MAB04	H31	IO	MDB12	AH31	–	NC
AT30	O	CSB0#	AH03	O	FPD15	B14	IO	HD18#	Y30	O	MAB05	H33	IO	MDB13	AH36	–	NC
AT29	O	CSB1#	AJ04	O	FPD16	D15	IO	HD19#	W31	O	MAB06	J32	IO	MDB14	AJ06	–	NC
AR29	O	CSB2#	AJ01	O	FPD17	E15	IO	HD20#	R32	O	MAB07	J36	IO	MDB15	AK03	–	NC
AP28	O	CSB3#	AJ03	O	FPD18	C14	IO	HD21#	P31	O	MAB08	M32	IO	MDB16	AN22	–	NC
B19	IO	DBSY#	AK02	O	FPD19	E14	IO	HD22#	N31	O	MAB09	N32	IO	MDB17	AN29	–	NC
E17	IO	DEFER#	AP01	O	FPD20	C15	IO	HD23#	AF34	O	MAB10	P34	IO	MDB18	AN30	–	NC
D32	I	DFTIN#	AL01	O	FPD21	D12	IO	HD24#	P36	O	MAB11	P30	IO	MDB19	AP05	–	NC
N03	I	DISPCLKI	AN02	O	FPD22	C13	IO	HD25#	M31	O	MAB12	N30	IO	MDB20	AP06	–	NC
N04	O	DISPCLKO	AM04	O	FPD23	B12	IO	HD26#	AN23	O	MAB13	N33	IO	MDB21	AP30	–	NC
AP10	O	DNCMD	AK06	O	FPDE	B10	IO	HD27#	A32	I	MCLKIA	R34	IO	MDB22	AP14	I	PWROK
AN09	O	DNSTB+	AG01	I	FPDET / GTVCLKIN	C11	IO	HD28#	B31	O	MCLKOA	R30	IO	MDB23	AM13	I	RESET#
AP09	O	DNSTB–	AL04	O	FPHS	B11	IO	HD29#	A31	O	MCLKOB	AA31	IO	MDB24	B18	IO	RS0#
G15	O	DPWR#	AK01	O	FPVS	A10	IO	HD30#	B36	IO	MDA00	AA32	IO	MDB25	D18	IO	RS1#
D36	O	DQMA0	N07	I	GCLK	C12	IO	HD31#	D34	IO	MDA01	AA33	IO	MDB26	B17	IO	RS2#
L33	O	DQMA1	AE04	O	GDVP1CLK / GTVCLK	H06	IO	HD32#	E33	IO	MDA02	AB31	IO	MDB27	V07	AI	RSET
V34	O	DQMA2	AE01	O	GDVP1CLK#/GTVCLK#	G07	IO	HD33#	F35	IO	MDA03	W32	IO	MDB28	AD04	IO	SBDDCCLK
AD35	O	DQMA3	AC03	O	GDVP1D00 / GTVD00	J04	IO	HD34#	C35	IO	MDA04	W33	IO	MDB29	AD05	IO	SBDDCDAT
AN32	O	DQMA4	AD03	O	GDVP1D01 / GTVD01	G06	IO	HD35#	C36	IO	MDA05	AB33	IO	MDB30	AL05	IO	SBPLCLK
AP24	O	DQMA5	AD01	O	GDVP1D02 / GTVD02	H05	IO	HD36#	E34	IO	MDA06	AB30	IO	MDB31	AL03	IO	SBPLDAT
AP20	O	DQMA6	AE03	O	GDVP1D03 / GTVD03	G03	IO	HD37#	E36	IO	MDA07	AG36	IO	MDB32	AN25	O	SCASA#
AT16	O	DQMA7	AG02	O	GDVP1D04 / GTVD04	H04	IO	HD38#	K33	IO	MDA08	AG35	IO	MDB33	AN28	O	SCASB#
A34	O	DQMB0	AE02	O	GDVP1D05 / GTVD05	G04	IO	HD39#	K35	IO	MDA09	AH33	IO	MDB34	V03	IO	SPCLK1
H36	O	DQMB1	AF03	O	GDVP1D06 / GTVD06	K01	IO	HD40#	M36	IO	MDA10	AH30	IO	MDB35	T03	IO	SPCLK2
N35	O	DQMB2	AH04	O	GDVP1D07 / GTVD07	J05	IO	HD41#	M33	IO	MDA11	AF33	IO	MDB36	V04	IO	SPDAT1
Y33	O	DQMB3	AG06	O	GDVP1D08 / GTVD08	H01	IO	HD42#	K34	IO	MDA12	AG34	IO	MDB37	T04	IO	SPDAT2
AG32	O	DQMB4	AG05	O	GDVP1D09 / GTVD09	J06	IO	HD43#	K36	IO	MDA13	AH32	IO	MDB38	AP26	O	SRASA#
AR28	O	DQMB5	AH05	O	GDVP1D10 / GTVD10	J01	IO	HD44#	L36	IO	MDA14	AJ34	IO	MDB39	AL29	O	SRASB#
AP22	O	DQMB6	AK05	O	GDVP1D11 / GTVD11	J02	IO	HD45#	M34	IO	MDA15	AL30	IO	MDB40	AN14	I	SUSST#
AN18	O	DQMB7	AC04	O	GDVP1DE / GTVDE	K04	IO	HD46#	T35	IO	MDA16	AM29	IO	MDB41	AR26	O	SWEA#
D35	IO	DQSA0#	AF01	I	GDVP1DET	K03	IO	HD47#	T36	IO	MDA17	AL28	IO	MDB42	AN31	O	SWEB#
L31	IO	DQSA1#	AD02	O	GDVP1HS / GTVHS	C03	IO	HD48#	V36	IO	MDA18	AN27	IO	MDB43	W06	I	TCLK
U34	IO	DQSA2#	AC01	O	GDVP1VS / GTVVS	C04	IO	HD49#	W35	IO	MDA19	AM31	IO	MDB44	C31	I	TESTIN#
AD34	IO	DQSA3#	V05	O	GPO0	B04	IO	HD50#	R36	IO	MDA20	AM28	IO	MDB45	AN12	I	UPCMD
AT33	IO	DQSA4#	W05	O	GPOUT	D03	IO	HD51#	U33	IO	MDA21	AP27	IO	MDB46	AM10	I	UPSTB+
AT24	IO	DQSA5#	B22	IO	HA03#	A04	IO	HD52#	V33	IO	MDA22	AL27	IO	MDB47	AM09	I	UPSTB–
AN20	IO	DQSA6#	A20	IO	HA04#	C05	IO	HD53#	W34	IO	MDA23	AL23	IO	MDB48	AP08	IO	VD00
AR16	IO	DQSA7#	F20	IO	HA05#	D04	IO	HD54#	AB36	IO	MDA24	AM23	IO	MDB49	AR08	IO	VD01
A33	IO	DQSB0#	A21	IO	HA06#	E04	IO	HD55#	AC34	IO	MDA25	AN21	IO	MDB50	AN10	IO	VD02
H34	IO	DQSB1#	B21	IO	HA07#	E02	IO	HD56#	AD32	IO	MDA26	AK21	IO	MDB51	AR11	IO	VD03
N34	IO	DQSB2#	E23	IO	HA08#	E03	IO	HD57#	AE35	IO	MDA27	AL22	IO	MDB52	AR07	IO	VD04
Y34	IO	DQSB3#	C21	IO	HA09#	F03	IO	HD58#	AC33	IO	MDA28	AM22	IO	MDB53	AP07	IO	VD05
AG33	IO	DQSB4#	D21	IO	HA10#	F04	IO	HD59#	AC36	IO	MDA29	AT22	IO	MDB54	AM11	IO	VD06
AT28	IO	DQSB5#	E22	IO	HA11#	C02	IO	HD60#	AE36	IO	MDA30	AL21	IO	MDB55	AP11	IO	VD07
AR22	IO	DQSB6#	F21	IO	HA12#	F01	IO	HD61#	AE34	IO	MDA31	AL18	IO	MDB56	AM07	IO	VD08
AP18	IO	DQSB7#	C22	IO	HA13#	G01	IO	HD62#	AR34	IO	MDA32	AN19	IO	MDB57	AN06	IO	VD09
C19	IO	DRDY#	E21	IO	HA14#	F02	IO	HD63#	AP33	IO	MDA33	AL17	IO	MDB58	AP12	IO	VD10
Y04	O	DVP0CLK / TVCLK	D22	IO	HA15#	A06	IO	HDBI0#	AP32	IO	MDA34	AM17	IO	MDB59	AM12	IO	VD11
W01	O	DVP0D00 / TVD00	F22	IO	HA16#	B13	IO	HDBI1#	AR31	IO	MDA35	AL19	IO	MDB60	AT06	IO	VD12
W02	O	DVP0D01 / TVD01	C25	IO	HA17#	J03	IO	HDBI2#	AT34	IO	MDA36	AM19	IO	MDB61	AR06	IO	VD13
AA05	O	DVP0D02 / TVD02	C24	IO	HA18#	A05	IO	HDBI3#	AR33	IO	MDA37	AT18	IO	MDB62	AN13	IO	VD14
Y03	O	DVP0D03 / TVD03	D24	IO	HA19#	D08	IO	HDSTBN0#	AT32	IO	MDA38	AN17	IO	MDB63	AP13	IO	VD15
Y02	O	DVP0D04 / TVD04	E24	IO	HA20#	D13	IO	HDSTBN1#	AP31	IO	MDA39	B06	–	NC	AN07	IO	VBE#
AA04	O	DVP0D05 / TVD05	E25	IO	HA21#	H02	IO	HDSTBN2#	AN26	IO	MDA40	C06	–	NC	AM06	AI	VLCOMPP
Y05	O	DVP0D06 / TVD06	F26	IO	HA22#	E01	IO	HDSTBN3#	AM25	IO	MDA41	D06	–	NC	AT07	IO	VPAR
Y06	O	DVP0D07 / TVD07	B26	IO	HA23#	F08	IO	HDSTBP0#	AN24	IO	MDA42	E06	–	NC	U03	O	VSYNC
Y07	O	DVP0D08 / TVD08	B23	IO	HA24#	E13	IO	HDSTBP1#	AR23	IO	MDA43	F23	–	NC	N05	I	XIN
AB05	O	DVP0D09 / TVD09	E26	IO	HA25#	H03	IO	HDSTBP2#	AT27	IO	MDA44	F24	–	NC			
AB06	O	DVP0D10 / TVD10	D25	IO	HA26#	D01	IO	HDSTBP3#	AT26	IO	MDA45	F25	–	NC			
AA06	O	DVP0D11 / TVD11	E27	IO	HA27#	C17	IO	HIT#	AT23	IO	MDA46	F32	–	NC			
W03	O	DVP0DE / TVDE	C23	IO	HA28#	F16	I	HITM#	AP23	IO	MDA47	F33	–	NC			
V02	I	DVP0DET/TVCLKIN	F27	IO	HA29#	F18	I	HLOCK#	AP21	IO	MDA48	F34	–	NC			

Table 4. Signal Pin List (Numerical Order) - External AGP Interface Enabled on Display Pins

Pin #		Pin Name	Pin #		Pin Name	Pin #		Pin Name	Pin #		Pin Name	Pin #		Pin Name	Pin #		Pin Name
A04	IO	HD52#	D32	I	DFTIN#	J34	IO	MDB10	Y02	O	DVP0D04 / TVD04	AH02	IO	GD21	AN31	O	SWEB#
A05	IO	HDBI3#	D33	IO	MDB01	J35	O	CKEB3	Y03	O	DVP0D03 / TVD03	AH03	IO	GD23	AN32	O	DQMA4
A06	IO	HDBI0#	D34	IO	MDA01	J36	IO	MDB15	Y04	O	DVP0CLK / TVCLK	AH04	IO	GD28	AP01	IO	GD15
A07	IO	HD15#	D35	IO	DQSA0#	K01	IO	HD40#	Y05	O	DVP0D06 / TVD06	AH05	IO	GD26	AP02	IO	GD1
A08	IO	HD12#	D36	O	DQMA0	K03	IO	HD47#	Y06	O	DVP0D07 / TVD07	AH30	IO	MDB35	AP03	IO	GD9
A09	IO	HD06#	E01	IO	HDSTBN3#	K04	IO	HD46#	Y07	O	DVP0D08 / TVD08	AH31	–	NC	AP04	IO	GD2
A10	IO	HD30#	E02	IO	HD56#	K06	O	CPURST#	Y30	O	MAB05	AH32	IO	MDB38	AP05	–	NC
A19	IO	ADS#	E03	IO	HD57#	K31	O	CKEB2	Y31	–	NC	AH33	IO	MDB34	AP06	–	NC
A20	IO	HA04#	E04	IO	HD55#	K32	O	CKEB0	Y33	O	DQMB3	AH34	O	MAA02	AP07	IO	VAD05
A21	IO	HA06#	E06	–	NC	K33	IO	MDA08	Y34	IO	DQSB3#	AH35	O	MAA01	AP08	IO	VAD00
A22	IO	HADSTB0#	E07	IO	HD08#	K34	IO	MDA12	Y36	–	NC	AH36	–	NC	AP09	O	DNSTB–
A31	O	MCLKOB	E09	IO	HD09#	K35	IO	MDA09	AA02	–	NC	AJ01	IO	GD17	AP10	O	DNCMD
A32	I	MCLKIA	E13	IO	HDSTBP1#	K36	IO	MDA13	AA03	–	NC	AJ03	IO	GD16	AP11	IO	VAD07
A33	IO	DQSB0#	E14	IO	HD22#	L31	IO	DQSA1#	AA04	O	DVP0D05 / TVD05	AJ04	IO	GD18	AP12	IO	VAD10
A34	O	DQMB0	E15	IO	HD20#	L33	O	DQMA1	AA05	O	DVP0D02 / TVD02	AJ06	IO	GD25	AP13	IO	VAD15
A35	IO	MDB02	E16	IO	HD17#	L34	O	CKEA3	AA06	O	DVP0D11 / TVD11	AJ33	O	MAA00	AP14	I	PWROK
A36	IO	MDB06	E17	IO	DEFER#	L36	IO	MDA14	AA30	O	MAB03	AJ34	IO	MDB39	AP15	IO	MDA63
B04	IO	HD50#	E18	O	BREQ0#	M05	I	HCLK+	AA31	IO	MDB24	AJ36	O	BAB0	AP16	IO	MDA62
B06	–	NC	E19	IO	HREQ3#	M06	I	HCLK–	AA32	IO	MDB25	AK01	IO	GDEVSEL	AP17	IO	MDA60
B07	IO	HD05#	E21	IO	HA14#	M30	–	NC	AA33	IO	MDB26	AK02	IO	GC#BE2	AP18	IO	DQSB7#
B09	IO	HD03#	E22	IO	HA11#	M31	O	MAB12	AA34	–	NC	AK03	IO	GTRDY	AP19	IO	MDA55
B10	IO	HD27#	E23	IO	HA08#	M32	IO	MDB16	AA35	–	NC	AK04	IO	GD22	AP20	O	DQMA6
B11	IO	HD29#	E24	IO	HA20#	M33	IO	MDA11	AA36	O	MAB04	AK05	IO	GC#BE3	AP21	IO	MDA48
B12	IO	HD26#	E25	IO	HA21#	M34	IO	MDA15	AB01	I	AGP8XDET#	AK06	IO	GD19	AP22	O	DQMB6
B13	IO	HDBI1#	E26	IO	HA25#	M35	O	CKEA1	AB02	I	GWBF	AK21	IO	MDB51	AP23	IO	MDA47
B14	IO	HD18#	E27	IO	HA27#	M36	IO	MDA10	AB03	AI	AGPCOMPN	AL01	IO	GD14	AP24	O	DQMA5
B17	IO	RS2#	E28	IO	HA34#	N03	I	DISPCLKI	AB04	–	NC	AL02	IO	GD12	AP25	O	CSA3#
B18	IO	RS0#	E33	IO	MDA02	N04	O	DISPCLKO	AB05	O	DVP0D09 / TVD09	AL03	IO	GC#BE1	AP26	O	SRASA#
B19	IO	DBSY#	E34	IO	MDA06	N05	I	XIN	AB06	O	DVP0D10 / TVD10	AL04	IO	GFRAME	AP27	IO	MDB46
B21	IO	HA07#	E36	IO	MDA07	N07	I	GCLK	AB30	IO	MDB31	AL05	IO	GIRDY	AP28	O	CSB3#
B22	IO	HA03#	F01	IO	HD61#	N30	IO	MDB20	AB31	IO	MDB27	AL14	O	AGPBUSY#	AP29	O	CSA2#
B23	IO	HA24#	F02	IO	HD63#	N31	O	MAB09	AB32	–	NC	AL17	IO	MDB58	AP30	–	NC
B26	IO	HA23#	F03	IO	HD58#	N32	IO	MDB17	AB33	IO	MDB30	AL18	IO	MDB56	AP31	IO	MDA39
B31	O	MCLKOA	F04	IO	HD59#	N33	IO	MDB21	AB34	O	MAA05	AL19	IO	MDB60	AP32	IO	MDA34
B33	IO	MDB05	F07	IO	HD10#	N34	IO	DQSB2#	AB35	O	MAA06	AL20	IO	MDA51	AP33	IO	MDA33
B34	IO	MDB07	F08	IO	HDSTBP0#	N35	O	DQMB2	AB36	IO	MDA24	AL21	IO	MDB55	AR01	IO	GD10
B36	IO	MDA00	F09	IO	HD07#	N36	–	NC	AC01	I	GSBA0#	AL22	IO	MDB52	AR03	IO	GADSTB0S
C02	IO	HD60#	F10	IO	HD04#	P30	IO	MDB19	AC03	I	GSBA2#	AL23	IO	MDB48	AR04	IO	GD4
C03	IO	HD48#	F15	AI	HRCOMP	P31	O	MAB08	AC04	I	GSBA1#	AL27	IO	MDB47	AR06	IO	VAD13
C04	IO	HD49#	F16	I	HITM#	P33	–	NC	AC06	AI	AGPCOMPP	AL28	IO	MDB42	AR07	IO	VAD04
C05	IO	HD53#	F18	I	HLOCK#	P34	IO	MDB18	AC33	IO	MDA28	AL29	O	SRASB#	AR08	IO	VAD01
C06	–	NC	F19	IO	HREQ4#	P36	O	MAB11	AC34	IO	MDA25	AL30	IO	MDB40	AR11	IO	VAD03
C07	IO	HD11#	F20	IO	HA05#	R01	AO	AR	AC36	IO	MDA29	AM01	IO	GD8	AR16	IO	DQSA7#
C08	IO	HD13#	F21	IO	HA12#	R02	AO	AG	AD01	I	GSBSTBS	AM03	IO	GSTOP	AR17	IO	MDA61
C09	IO	HD02#	F22	IO	HA16#	R03	AO	AB	AD02	I	GSBA3#	AM04	IO	GD11	AR19	IO	MDA50
C11	IO	HD28#	F23	–	NC	R30	IO	MDB23	AD03	I	GSBSTBF	AM06	AI	VLCOMPP	AR20	IO	MDA53
C12	IO	HD31#	F24	–	NC	R31	–	NC	AD04	I	GREQ	AM07	IO	VAD08	AR22	IO	DQSB6#
C13	IO	HD25#	F25	–	NC	R32	O	MAB07	AD05	O	GGNT	AM09	I	UPSTB–	AR23	IO	MDA43
C14	IO	HD21#	F26	IO	HA22#	R33	–	NC	AD06	O	GST0	AM10	I	UPSTB+	AR25	O	CSA1#
C15	IO	HD23#	F27	IO	HA29#	R34	IO	MDB22	AD32	IO	MDA26	AM11	IO	VAD06	AR26	O	SWEA#
C16	IO	BPRI#	F28	IO	HA35#	R35	O	CKEA2	AD33	O	MAA03	AM12	IO	VAD11	AR28	O	DQMB5
C17	IO	HIT#	F32	–	NC	R36	IO	MDA20	AD34	IO	DQSA3#	AM13	I	RESET#	AR29	O	CSB2#
C18	IO	BNR#	F33	–	NC	T03	IO	SPCLK2	AD35	O	DQMA3	AM17	IO	MDB59	AR31	IO	MDA35
C19	IO	DRDY#	F34	–	NC	T04	IO	SPDAT2	AD36	O	MAA04	AM19	IO	MDB61	AR33	IO	MDA37
C20	IO	HREQ1#	F35	IO	MDA03	T33	O	CKEA0	AE01	I	GSBA7#	AM20	IO	MDA49	AR34	IO	MDA32
C21	IO	HA09#	F36	–	NC	T34	O	MAA12	AE02	I	GSBA4#	AM22	IO	MDB53	AT01	IO	GD5
C22	IO	HA13#	G01	IO	HD62#	T35	IO	MDA16	AE03	I	GSBA5#	AM23	IO	MDB49	AT02	IO	GD0
C23	IO	HA28#	G03	IO	HD37#	T36	IO	MDA17	AE04	I	GSBA6#	AM25	IO	MDA41	AT03	IO	GADSTB0F
C24	IO	HA18#	G04	IO	HD39#	U02	O	INTA#	AE05	O	GST1	AM28	IO	MDB45	AT04	IO	GD7
C25	IO	HA17#	G06	IO	HD35#	U03	O	VSYNC	AE06	O	GST2	AM29	IO	MDB41	AT05	IO	GD3
C26	IO	HADSTB1#	G07	IO	HD33#	U04	O	HSYNC	AE07	I	GRBF	AM31	IO	MDB44	AT06	IO	VAD12
C27	IO	HA32#	G10	IO	HD00#	U33	IO	MDA21	AE30	O	MAB02	AN01	IO	GSERR	AT07	IO	VPAR
C28	IO	HA33#	G15	O	DPWR#	U34	IO	DQSA2#	AE31	–	NC	AN02	IO	GD13	AT15	IO	MDA58
C31	I	TESTIN#	G18	IO	HTRDY#	U36	O	MAA11	AE32	–	NC	AN03	IO	GPAR	AT16	O	DQMA7
C32	IO	MDB00	G31	IO	MDB08	V01	O	DVP0VS / TVVS	AE33	O	MAB00	AN04	IO	GC#BE0	AT17	IO	MDA56
C33	IO	MDB04	G32	IO	MDB09	V02	I	DVP0DET/TVCKI	AE34	IO	MDA31	AN05	IO	GD6	AT18	IO	MDB62
C34	IO	MDB03	G33	–	NC	V03	IO	SPCLK1	AE35	IO	MDA27	AN06	IO	VAD09	AT19	IO	MDA54
C35	IO	MDA04	G34	–	NC	V04	IO	SPDAT1	AE36	IO	MDA30	AN07	IO	VBE#	AT20	O	MAA13
C36	IO	MDA05	G35	–	NC	V05	O	GPO0	AF01	IO	GD31	AN09	O	DNSTB+	AT21	IO	MDA52
D01	IO	HDSTBP3#	G36	–	NC	V06	I	BISTIN	AF03	IO	GD29	AN10	IO	VAD02	AT22	IO	MDB54
D03	IO	HD51#	H01	IO	HD42#	V07	AI	RSET	AF04	IO	GDBIH / GPIPE#	AN12	I	UPCMD	AT23	IO	MDA46
D04	IO	HD54#	H02	IO	HDSTBN2#	V32	O	MAA07	AF30	O	MAB01	AN13	IO	VAD14	AT24	IO	DQSA5#
D06	–	NC	H03	IO	HDSTBP2#	V33	IO	MDA22	AF31	–	NC	AN14	I	SUSST#	AT25	O	CSA0#
D07	IO	HD14#	H04	IO	HD38#	V34	O	DQMA2	AF33	IO	MDB36	AN15	IO	MDA59	AT26	IO	MDA45
D08	IO	HDSTBN0#	H05	IO	HD36#	V35	O	MAA09	AF34	O	MAB10	AN16	IO	MDA57	AT27	IO	MDA44
D09	IO	HD01#	H06	IO	HD32#	V36	IO	MDA18	AF36	O	BAB1	AN17	IO	MDB63	AT28	IO	DQSB5#
D12	IO	HD24#	H31	IO	MDB12	W01	O	DVP0D00 /TVD00	AG01	IO	GADSTB1S	AN18	O	DQMB7	AT29	O	CSB1#
D13	IO	HDSTBN1#	H33	IO	MDB13	W02	O	DVP0D01 /TVD01	AG02	IO	GD27	AN19	IO	MDB57	AT30	O	CSB0#
D15	IO	HD19#	H34	IO	DQSB1#	W03	O	DVP0DE / TVDE	AG03	IO	GADSTB1F	AN20	IO	DQSA6#	AT31	O	BAA0
D16	IO	HD16#	H36	O	DQMB1	W04	O	DVP0HS / TVHS	AG04	IO	GDBIL	AN21	IO	MDB50	AT32	IO	MDA38
D18	IO	RS1#	J01	IO	HD44#	W05	O	GPOUT	AG05	IO	GD24	AN22	–	NC	AT33	IO	DQSA4#
D19	IO	HREQ0#	J02	IO	HD45#	W06	I	TCLK	AG06	IO	GD30	AN23	O	MAB13	AT34	IO	MDA36
D20	IO	HREQ2#	J03	IO	HDBI2#	W30	–	NC	AG31	–	NC	AN24	IO	MDA42	AT35	O	BAA1
D21	IO	HA10#	J04	IO	HD34#	W31	O	MAB06	AG32	O	DQMB4	AN25	O	SCASA#	AT36	O	MAA10
D22	IO	HA15#	J05	IO	HD41#	W32	IO	MDB28	AG33	IO	DQSB4#	AN26	IO	MDA40			
D24	IO	HA19#	J06	IO	HD43#	W33	IO	MDB29	AG34	IO	MDB37	AN27	IO	MDB43			
D25	IO	HA26#	J31	IO	MDB11	W34	IO	MDA23	AG35	IO	MDB33	AN28	O	SCASB#			
D27	IO	HA30#	J32	IO	MDB14	W35	IO	MDA19	AG36	IO	MDB32	AN29	–	NC			
D28	IO	HA31#	J33	O	CKEB1	W36	O	MAA08	AH01	IO	GD20	AN30	–	NC			

Table 5. Signal Pin List (Alphabetical Order) - External AGP Interface Enabled on Display Pins

Pin #		Pin Name	Pin #		Pin Name	Pin #		Pin Name	Pin #		Pin Name	Pin #		Pin Name	Pin #		Pin Name
R03	AO	AB	V02	I	DVP0DET/TVCLKIN	E24	IO	HA20#	E13	IO	HDSTBP1#	AP31	IO	MDA39	B06	–	NC
A19	IO	ADS#	W04	O	DVP0HS/TVHS	E25	IO	HA21#	H03	IO	HDSTBP2#	AN26	IO	MDA40	C06	–	NC
R02	AO	AG	V01	O	DVP0VS/TVVS	F26	IO	HA22#	D01	IO	HDSTBP3#	AM25	IO	MDA41	D06	–	NC
AB01	I	AGP8XDET#	AT03	IO	GADSTB0F	B26	IO	HA23#	D08	IO	HDSTBN0#	AN24	IO	MDA42	E06	–	NC
AL14	O	AGPBUSY#	AR03	IO	GADSTB0S	B23	IO	HA24#	D13	IO	HDSTBN1#	AR23	IO	MDA43	F23	–	NC
AB03	AI	AGPCOMPN	AG03	IO	GADSTB1F	E26	IO	HA25#	H02	IO	HDSTBN2#	AT27	IO	MDA44	F24	–	NC
AC06	AI	AGPCOMPP	AG01	IO	GADSTB1S	D25	IO	HA26#	E01	IO	HDSTBN3#	AT26	IO	MDA45	F25	–	NC
R01	AO	AR	AN04	IO	GC#BE0	E27	IO	HA27#	C17	IO	HIT#	AT23	IO	MDA46	F32	–	NC
AT31	O	BAA0	AL03	IO	GC#BE1	C23	IO	HA28#	F16	I	HITM#	AP23	IO	MDA47	F33	–	NC
AT35	O	BAA1	AK02	IO	GC#BE2	F27	IO	HA29#	F18	I	HLOCK#	AP21	IO	MDA48	F34	–	NC
AJ36	O	BAB0	AK05	IO	GC#BE3	D27	IO	HA30#	F15	AI	HRCOMP	AM20	IO	MDA49	F36	–	NC
AF36	O	BAB1	N07	I	GCLK	D28	IO	HA31#	D19	IO	HREQ0#	AR19	IO	MDA50	G33	–	NC
V06	I	BISTIN	AT02	IO	GD0	C27	IO	HA32#	C20	IO	HREQ1#	AL20	IO	MDA51	G34	–	NC
C18	IO	BNR#	AP02	IO	GD1	C28	IO	HA33#	D20	IO	HREQ2#	AT21	IO	MDA52	G35	–	NC
C16	IO	BPRI#	AP04	IO	GD2	E28	IO	HA34#	E19	IO	HREQ3#	AR20	IO	MDA53	G36	–	NC
E18	O	BREQ0#	AT05	IO	GD3	F28	IO	HA35#	F19	IO	HREQ4#	AT19	IO	MDA54	M30	–	NC
T33	O	CKEA0	AR04	IO	GD4	A22	IO	HADSTB0#	U04	O	HSYNC	AP19	IO	MDA55	N36	–	NC
M35	O	CKEA1	AT01	IO	GD5	C26	IO	HADSTB1#	G18	IO	HTRDY#	AT17	IO	MDA56	P33	–	NC
R35	O	CKEA2	AN05	IO	GD6	M05	I	HCLK+	U02	O	INTA#	AN16	IO	MDA57	R31	–	NC
L34	O	CKEA3	AT04	IO	GD7	M06	I	HCLK–	AJ33	O	MAA00	AT15	IO	MDA58	R33	–	NC
K32	O	CKEB0	AM01	IO	GD8	G10	IO	HD00#	AH35	O	MAA01	AN15	IO	MDA59	W30	–	NC
J33	O	CKEB1	AP03	IO	GD9	D09	IO	HD01#	AH34	O	MAA02	AP17	IO	MDA60	Y31	–	NC
K31	O	CKEB2	AR01	IO	GD10	C09	IO	HD02#	AD33	O	MAA03	AR17	IO	MDA61	Y36	–	NC
J35	O	CKEB3	AM04	IO	GD11	B09	IO	HD03#	AD36	O	MAA04	AP16	IO	MDA62	AA02	–	NC
K06	O	CPURST#	AL02	IO	GD12	F10	IO	HD04#	AB34	O	MAA05	AP15	IO	MDA63	AA03	–	NC
AT25	O	CSA0#	AN02	IO	GD13	B07	IO	HD05#	AB35	O	MAA06	C32	IO	MDB00	AA34	–	NC
AR25	O	CSA1#	AL01	IO	GD14	A09	IO	HD06#	V32	O	MAA07	D33	IO	MDB01	AA35	–	NC
AP29	O	CSA2#	AP01	IO	GD15	F09	IO	HD07#	W36	O	MAA08	A35	IO	MDB02	AB04	–	NC
AP25	O	CSA3#	AJ03	IO	GD16	E07	IO	HD08#	V35	O	MAA09	C34	IO	MDB03	AB32	–	NC
AT30	O	CSB0#	AJ01	IO	GD17	E09	IO	HD09#	AT36	O	MAA10	C33	IO	MDB04	AE31	–	NC
AT29	O	CSB1#	AJ04	IO	GD18	F07	IO	HD10#	U36	O	MAA11	B33	IO	MDB05	AE32	–	NC
AR29	O	CSB2#	AK06	IO	GD19	C07	IO	HD11#	T34	O	MAA12	A36	IO	MDB06	AF31	–	NC
AP28	O	CSB3#	AH01	IO	GD20	A08	IO	HD12#	AT20	O	MAA13	B34	IO	MDB07	AG31	–	NC
B19	IO	DBSY#	AH02	IO	GD21	C08	IO	HD13#	AE33	O	MAB00	G31	IO	MDB08	AH31	–	NC
E17	IO	DEFER#	AK04	IO	GD22	D07	IO	HD14#	AF30	O	MAB01	G32	IO	MDB09	AH36	–	NC
D32	I	DFTIN#	AH03	IO	GD23	A07	IO	HD15#	AE30	O	MAB02	J34	IO	MDB10	AN22	–	NC
N03	I	DISPCLKI	AG05	IO	GD24	D16	IO	HD16#	AA30	O	MAB03	J31	IO	MDB11	AN29	–	NC
N04	O	DISPCLKO	AJ06	IO	GD25	E16	IO	HD17#	AA36	O	MAB04	H31	IO	MDB12	AN30	–	NC
AP10	O	DNCMD	AH05	IO	GD26	B14	IO	HD18#	Y30	O	MAB05	H33	IO	MDB13	AP05	–	NC
AN09	O	DNSTB+	AG02	IO	GD27	D15	IO	HD19#	W31	O	MAB06	J32	IO	MDB14	AP06	–	NC
AP09	O	DNSTB–	AH04	IO	GD28	E15	IO	HD20#	R32	O	MAB07	J36	IO	MDB15	AP30	–	NC
G15	O	DPWR#	AF03	IO	GD29	C14	IO	HD21#	P31	O	MAB08	M32	IO	MDB16	AP14	I	PWROK
D36	O	DQMA0	AG06	IO	GD30	E14	IO	HD22#	N31	O	MAB09	N32	IO	MDB17	AM13	I	RESET#
L33	O	DQMA1	AF01	IO	GD31	C15	IO	HD23#	AF34	O	MAB10	P34	IO	MDB18	B18	IO	RS0#
V34	O	DQMA2	AF04	IO	GDBIH / GPIPE#	D12	IO	HD24#	P36	O	MAB11	P30	IO	MDB19	D18	IO	RS1#
AD35	O	DQMA3	AG04	IO	GDBIL	C13	IO	HD25#	M31	O	MAB12	N30	IO	MDB20	B17	IO	RS2#
AN32	O	DQMA4	AK01	IO	GDEVSEL	B12	IO	HD26#	AN23	O	MAB13	N33	IO	MDB21	V07	AI	RSET
AP24	O	DQMA5	AL04	IO	GFRAME	B10	IO	HD27#	A32	I	MCLKIA	R34	IO	MDB22	AN25	O	SCASA#
AP20	O	DQMA6	AD05	O	GGNT	C11	IO	HD28#	B31	O	MCLKOA	R30	IO	MDB23	AN28	O	SCASB#
AT16	O	DQMA7	AL05	IO	GIRDY	B11	IO	HD29#	A31	O	MCLKOB	AA31	IO	MDB24	V03	IO	SPCLK1
A34	O	DQMB0	AN03	IO	GPAR	A10	IO	HD30#	B36	IO	MDA00	AA32	IO	MDB25	T03	IO	SPCLK2
H36	O	DQMB1	V05	O	GPO0	C12	IO	HD31#	D34	IO	MDA01	AA33	IO	MDB26	V04	IO	SPDAT1
N35	O	DQMB2	W05	O	GPOUT	H06	IO	HD32#	E33	IO	MDA02	AB31	IO	MDB27	T04	IO	SPDAT2
Y33	O	DQMB3	AE07	I	GRBF	G07	IO	HD33#	F35	IO	MDA03	W32	IO	MDB28	AP26	O	SRASA#
AG32	O	DQMB4	AD04	I	GREQ	J04	IO	HD34#	C35	IO	MDA04	W33	IO	MDB29	AL29	O	SRASB#
AR28	O	DQMB5	AC01	I	GSBA0#	G06	IO	HD35#	C36	IO	MDA05	AB33	IO	MDB30	AN14	I	SUSST#
AP22	O	DQMB6	AC04	I	GSBA1#	H05	IO	HD36#	E34	IO	MDA06	AB30	IO	MDB31	AR26	O	SWEA#
AN18	O	DQMB7	AC03	I	GSBA2#	G03	IO	HD37#	E36	IO	MDA07	AG36	IO	MDB32	AN31	O	SWEB#
D35	IO	DQSA0#	AD02	I	GSBA3#	H04	IO	HD38#	K33	IO	MDA08	AG35	IO	MDB33	W06	I	TCLK
L31	IO	DQSA1#	AE02	I	GSBA4#	G04	IO	HD39#	K35	IO	MDA09	AH33	IO	MDB34	C31	I	TESTIN#
U34	IO	DQSA2#	AE03	I	GSBA5#	K01	IO	HD40#	M36	IO	MDA10	AH30	IO	MDB35	AN12	I	UPCMD
AD34	IO	DQSA3#	AE04	I	GSBA6#	J05	IO	HD41#	M33	IO	MDA11	AF33	IO	MDB36	AM10	I	UPSTB+
AT33	IO	DQSA4#	AE01	I	GSBA7#	H01	IO	HD42#	K34	IO	MDA12	AG34	IO	MDB37	AM09	I	UPSTB–
AT24	IO	DQSA5#	AD03	I	GSBSTBF	J06	IO	HD43#	K36	IO	MDA13	AH32	IO	MDB38	AN07	IO	VBE#
AN20	IO	DQSA6#	AD01	I	GSBSTBS	J01	IO	HD44#	L36	IO	MDA14	AJ34	IO	MDB39	AP08	IO	VD00
AR16	IO	DQSA7#	AN01	IO	GSERR	J02	IO	HD45#	M34	IO	MDA15	AL30	IO	MDB40	AR08	IO	VD01
A33	IO	DQSB0#	AD06	O	GST0	K04	IO	HD46#	T35	IO	MDA16	AM29	IO	MDB41	AN10	IO	VD02
H34	IO	DQSB1#	AE05	O	GST1	K03	IO	HD47#	T36	IO	MDA17	AL28	IO	MDB42	AR11	IO	VD03
N34	IO	DQSB2#	AE06	O	GST2	C03	IO	HD48#	V36	IO	MDA18	AN27	IO	MDB43	AR07	IO	VD04
Y34	IO	DQSB3#	AM03	IO	GSTOP	C04	IO	HD49#	W35	IO	MDA19	AM31	IO	MDB44	AP07	IO	VD05
AG33	IO	DQSB4#	AK03	IO	GTRDY	B04	IO	HD50#	R36	IO	MDA20	AM28	IO	MDB45	AM11	IO	VD06
AT28	IO	DQSB5#	AB02	I	GWBF	D03	IO	HD51#	U33	IO	MDA21	AP27	IO	MDB46	AP11	IO	VD07
AR22	IO	DQSB6#	B22	IO	HA03#	A04	IO	HD52#	V33	IO	MDA22	AL27	IO	MDB47	AM07	IO	VD08
AP18	IO	DQSB7#	A20	IO	HA04#	C05	IO	HD53#	W34	IO	MDA23	AL23	IO	MDB48	AN06	IO	VD09
C19	IO	DRDY#	F20	IO	HA05#	D04	IO	HD54#	AB36	IO	MDA24	AM23	IO	MDB49	AP12	IO	VD10
Y04	O	DVP0CLK / TVCLK	A21	IO	HA06#	E04	IO	HD55#	AC34	IO	MDA25	AN21	IO	MDB50	AM12	IO	VD11
W01	O	DVP0D00 / TVD00	B21	IO	HA07#	E02	IO	HD56#	AD32	IO	MDA26	AK21	IO	MDB51	AT06	IO	VD12
W02	O	DVP0D01 / TVD01	E23	IO	HA08#	E03	IO	HD57#	AE35	IO	MDA27	AL22	IO	MDB52	AR06	IO	VD13
AA05	O	DVP0D02 / TVD02	C21	IO	HA09#	F03	IO	HD58#	AC33	IO	MDA28	AM22	IO	MDB53	AN13	IO	VD14
Y03	O	DVP0D03 / TVD03	D21	IO	HA10#	F04	IO	HD59#	AC36	IO	MDA29	AT22	IO	MDB54	AP13	IO	VD15
Y02	O	DVP0D04 / TVD04	E22	IO	HA11#	C02	IO	HD60#	AE36	IO	MDA30	AL21	IO	MDB55	AM06	AI	VLCOMPP
AA04	O	DVP0D05 / TVD05	F21	IO	HA12#	F01	IO	HD61#	AE34	IO	MDA31	AL18	IO	MDB56	AT07	IO	VPAR
Y05	O	DVP0D06 / TVD06	C22	IO	HA13#	G01	IO	HD62#	AR34	IO	MDA32	AN19	IO	MDB57	U03	O	VSYNC
Y06	O	DVP0D07 / TVD07	E21	IO	HA14#	F02	IO	HD63#	AP33	IO	MDA33	AL17	IO	MDB58	N05	I	XIN
Y07	O	DVP0D08 / TVD08	D22	IO	HA15#	A06	IO	HDBI0#	AP32	IO	MDA34	AM17	IO	MDB59			
AB05	O	DVP0D09 / TVD09	F22	IO	HA16#	B13	IO	HDBI1#	AR31	IO	MDA35	AL19	IO	MDB60			
AB06	O	DVP0D10 / TVD10	C25	IO	HA17#	J03	IO	HDBI2#	AT34	IO	MDA36	AM19	IO	MDB61			
AA06	O	DVP0D11 / TVD11	C24	IO	HA18#	A05	IO	HDBI3#	AR33	IO	MDA37	AT18	IO	MDB62			
W03	O	DVP0DE / TVDE	D24	IO	HA19#	F08	IO	HDSTBP0#	AT32	IO	MDA38	AN17	IO	MDB63			

Table 6. Power, Ground, and Voltage Reference Pin List

Outer Ring Pins (Intermixed with Signal Pins)

AGPVREF[0:1]	(2 pins):	AF7, AD7
GTLVREF	(1 pin):	H17
HAVREF[0:1]	(2 pins):	H19, G22
HDVREF[0:3]	(4 pins):	H11, H14, K7, J7
HCOMPVREF	(1 pin):	G14
MEMVREF[0:5]	(6 pins):	J29, R29, W29, AE29, AK22, AK17
VLVREF	(1 pin):	AL7
VCCA33HCK1	(1 pin):	M4
GNDAHCK1	(1 pin):	M3
VCCA33HCK2	(1 pin):	L1
GNDAHCK2	(1 pin):	L2
VCCA33GCK	(1 pin):	M1
GNDAGCK	(1 pin):	M2
VCCA33MCK	(1 pin):	D31
GNDAMCK	(1 pin):	E31
VCCA15PLL1	(1 pin):	P3
GNDAPLL1	(1 pin):	P2
VCCA15PLL2	(1 pin):	P6
GNDAPLL2	(1 pin):	N6
VCCA15PLL3	(1 pin):	N1
GNDAPLL3	(1 pin):	N2
VCCA33DAC[1:2]	(2 pins):	T5, P4
GNDADAC[1:3]	(3 pins):	T6, P5, R4
VCC25MEM	(4 pins):	AK32-33, AP34, AP36
VTT	(3 pins):	C29, F29, H27
VSUS15	(1 pin):	AT14
GND	(96 pins):	A11,14,17,23,26,29, B3,5,8,20,32,35, D2,5,11,14,17,23,26,29, E8,20,32,35, F17, G2,5,8,11,16,23,26,27, H20,30,32,35, K2,5, L32,35, M29, P29,32,35, U32,35, Y29,32,35, AB29, AC2,5,32,35, AF2,5,29,32,35, AH29, AJ2,5,32,35, AK20,27,30, AM2,5,14-16,18,21,24,27,30,32,34,36, AN8,11, AR2,5,14-15,18,21,24,27,30,32,35, AT8,11

Center Pins

VCC15	(51 pins):	M12-25, N12,25, P12,25, R12,25, T12,25, U12,25, V12,25, , W12,25, Y12,25, AA12,25, AB12,25, AC12,25, AD12,25, AE12-24
VCC25MEM	(21 pins):	N21-24, P24, R24, T24, U24, V24, W24, Y24, AA24, AB24, AC24, AD18-24
VCC15AGP	(6 pins):	AA13, AB13, AC13, AD13-15
VCC15VL	(2 pins):	AD16-17
VCC33GFX	(3 pins):	V13, W13, Y13
VTT	(12 pins):	N13-20, P13, R13, T13, U13
GND	(65 pins):	R15-22, T15-22, U15-22, V15-22, W15-22, Y15-22, AA15-22, AB15-22, AE25

Pin Descriptions

CPU Interface Pin Descriptions

CPU Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
HA[35:3]#	(see pin lists)	IO	**Host CPU Address Bus.** Connect to the address bus of the host CPU. Inputs during CPU cycles and driven by the North Bridge during cache snooping operations. Address signals up through HA[35]# allow future support of a 64 Gbyte memory space (the current design supports up to HA[33]# for support of 16 GB)..
HADSTB [1:0]#	C26, A22	IO	**Host CPU Address Strobe.** Source synchronous strobes used to transfer HA[31:3]# and HREQ[4:0]# at a 2x transfer rate. HASTB1# is the strobe for HA[31:17]# and HASTB0# is the strobe for HA[16:3] and HREQ[4:0]#.
HD[63:0]#	(see pin lists)	IO	**Host CPU Data.** These signals are connected to the CPU data bus.
HDBI[3:0]#	A5, J3, B13, A6	IO	**Host CPU Dynamic Bus Inversion.** Driven along with HD[63:0]# to indicate if the associated signals are inverted or not. Used to limit the number of simultaneously switching signals to 8 for the associated 16-bit data pin group (HDBI3# for HD[63:48]#, HDBI2# for HD[47:32]#, HDBI1# for HD[31:16]#, and HDBI0# for HD[15:0]#). HDBIn# is asserted such that the number of data bits driven low for the corresponding group does not exceed 8.
HDSTBP [3:0]# **HDSTBN [3:0]#**	D1, H3, E13, F8 E1, H2, D13, D8	IO	**Host CPU Differential Data Strobes.** Source synchronous strobes used to transfer HD[63:0]# and HDBI[3:0]# at a 4x transfer rate. HDSTBP3# / HDSTBN3# are the strobes for HD[63:48]# & HDBI3#; HDSTBP2# / HDSTBN2# are the strobes for HD[47:32]# & HDBI2#; HDSTBP1# / HDSTBN1# are the strobes for HD[31:16]# & HDBI1#; and HDSTBP0# / HDSTBN0# are the strobes for HD[15:0]# & HDBI0#.
ADS#	A19	IO	**Address Strobe**. The CPU asserts ADS# in T1 of the CPU bus cycle.
DBSY#	B19	IO	**Data Bus Busy**. Used by the data bus owner to hold the data bus for transfers requiring more than one cycle.
DRDY#	C19	IO	**Data Ready**. Asserted for each cycle that data is transferred.
HIT#	C17	IO	**Hit**. Indicates that a caching agent holds an unmodified version of the requested line. Also driven in conjunction with HITM# by the target to extend the snoop window.
HITM#	F16	I	**Hit Modified**. Asserted by the CPU to indicate that the address is modified in the L1 cache and needs to be written back.
HLOCK#	F18	I	**Host Lock**. All CPU cycles sampled with the assertion of HLOCK# and ADS# until the negation of HLOCK# must be atomic.
HREQ[4:0]#	F19, E19, D20, C20, D19	IO	**Request Command**. Asserted during both clocks of the request phase. In the first clock, the signals define the transaction type to a level of detail that is sufficient to begin a snoop request. In the second clock, the signals carry additional information to define the complete transaction type.
HTRDY#	G18	IO	**Host Target Ready**. Indicates that the target of the processor transaction is able to enter the data transfer phase.

Note: Clocking of the CPU interface is performed with HCLK+ and HCLK– (see clock pin description group).

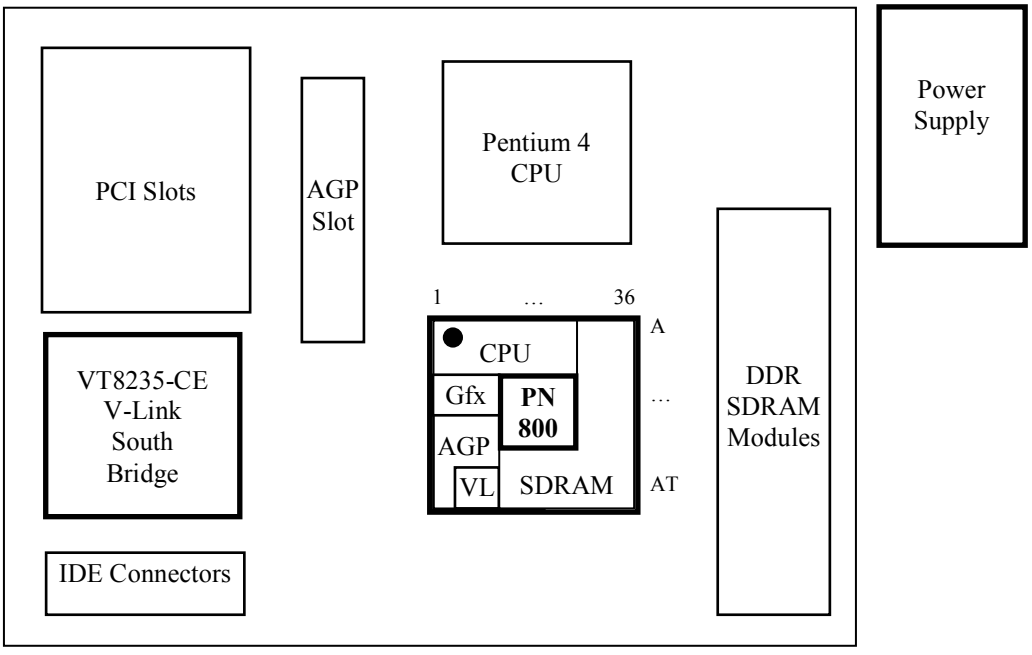
Note: Internal pullup resistors are provided on all AGTL+ interface pins. If the CPU does not have internal pullups, these North Bridge internal pullups may be enabled to allow the interface to meet AGTL+ bus interface specifications (see VD3 strap).

Note: I/O pads for the above pins are powered by VTT. Input voltage levels are referenced to HAVREF, HDVREF, and GTLREF.

CPU Interface (continued)			
Signal Name	**Pin #**	**I/O**	**Signal Description**
RS[2:0]#	B17, D18, B18	IO	**Response Signals**. Indicates the type of response per the table below: **RS[2:0]#** / **Response type** / **RS[2:0]#** / **Response type** 000 Idle State 100 Hard Failure 001 Retry Response 101 Normal Without Data 010 Defer Response 110 Implicit Writeback 011 Reserved 111 Normal With Data
DPWR#	G15	O	**Data Bus Power Reduction.** Request to reduce power on the mobile CPU data bus input buffer. Connect to mobile CPU if used.
BREQ0#	E18	O	**Bus Request 0.** Bus request output to CPU.
BPRI#	C16	IO	**Priority Agent Bus Request**. The owner of this signal will always be the next bus owner. This signal has priority over symmetric bus requests and causes the current symmetric owner to stop issuing new transactions unless the HLOCK# signal is asserted. The PN800 drives this signal to gain control of the processor bus.
BNR#	C18	IO	**Block Next Request**. Used to block the current request bus owner from issuing new requests. This signal is used to dynamically control the processor bus pipeline depth.
DEFER#	E17	IO	**Defer**. The PN800 uses a dynamic deferring policy to optimize system performance. The PN800 also uses the DEFER# signal to indicate a processor retry response.
CPURST#	K6	O	**CPU Reset.** Reset output to CPU. External pullup and filter capacitor to ground should be provided per CPU manufacturer's recommendations.

Note: I/O pads for the above pins are powered by VTT. Input voltage levels are referenced to HAVREF, HDVREF, & GTLREF.

The pinouts were defined assuming the ATX PCB layout model shown below (and general pin layout shown) as a guide for PCB component placement. Other PCB layouts (AT, LPX, and NLX) were also considered and can typically follow the same general component placement.



DDR SDRAM Memory Controller Pin Descriptions

DDR SDRAM Interface – "A" Data			
Signal Name	**Pin #**	**I/O**	**Signal Description**
MDA[63:0]	(see pin lists)	IO	**Memory Data.** These signals are connected to the DRAM data bus. Output drive strength may be set by Device 0 Function 3 RxE2.
DQMA[7:0]	AT16, AP20, AP24, AN32, AD35, V34, L33, D36	O	**Data Mask.** Data mask of each byte lane. Output drive strength may be set by Device 0 Function 3 RxE2.
DQSA[7:0]#	AR16, AN20, AT24, AT33, AD34, U34, L31, D35	IO	**DDR Data Strobe.** Data strobe of each byte lane. Output drive strength may be set by Device 0 Function 3 RxE0.
CSA[3:0]#	AP25, AP29, AR25, AT25	O	**Chip Select.** Chip select of each bank. Output drive strength may be set by Device 0 Function 3 RxE4.
CKEA[3:0]	L34, R35, M35, T33	O	**Clock Enables.** Clock enables for each DRAM bank for powering down the SDRAM or clock control for reducing power usage and for reducing heat / temperature in high-speed memory systems.

DDR SDRAM Interface – "B" Data			
Signal Name	**Pin #**	**I/O**	**Signal Description**
MDB[63:0]	(see pin lists)	IO	**Memory Data.** These signals are connected to the DRAM data bus. Output drive strength may be set by Device 0 Function 3 RxE2.
DQMB[7:0]	AN18, AP22, AR28, AG32, Y33, N35, H36, A34	O	**Data Mask.** Data mask of each byte lane. Output drive strength may be set by Device 0 Function 3 RxE2.
DQSB[7:0]#	AP18, AR22, AT28, AG33, Y34, N34, H34, A33	IO	**DDR Data Strobe.** Data strobe of each byte lane. Output drive strength may be set by Device 0 Function 3 RxE0.
CSB[3:0]#	AP28, AR29, AT29, AT30	O	**Chip Select.** Chip select of each bank. Output drive strength may be set by Device 0 Function 3 RxE4.
CKEB[3:0]	J35, K31, J33, K32	O	**Clock Enables.** Clock enables for each DRAM bank for powering down the SDRAM or clock control for reducing power usage and for reducing heat / temperature in high-speed memory systems.

DDR SDRAM Interface – Address			
Signal Name	**Pin #**	**I/O**	**Signal Description**
MAA[13:0], MAB[13:0]	(see pin lists)	O	**Memory Address A and B.** Two sets for additional drive. Output drive strength may be set by Device 0 Function 3 RxE8 (MAA) and EA (MAB).
BAA[1:0], BAB[1:0]	AT35, AT31, AF36, AJ36	O	**Bank Address A and B.** Two sets for additional drive. Output drive strength may be set by Device 0 Function 3 RxE8 (BA) and EA (BB).
SRASA#, SCASA#, SWEA#, SRASB#, SCASB#, SWEB#	AP26, AN25, AR26, AL29, AN28, AN31	O	**Row Address, Column Address and Write Enable Command Indicators A and B.** Two sets for additional drive. Output drive strength may be set by Device 0 Function 3 Rx E8 (ScmdA) and EA (ScmdB).

Note: I/O pads for all SDRAM pins are powered by VCC25MEM. MD / DQS input voltage levels are referenced to MEMVREF.

Accelerated Graphics Port Pin Descriptions

AGP 8x / 4x Bus Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
GD[31:0]	(see pin list)	IO	**Address / Data Bus.** Address is driven with GADSTB assertion for AGP-style transfers and with GFRAME# assertion for PCI-style transfers.
GC#BE[3:0] (GCBE#[3:0] for 4x mode)	AK5, AK2, AL3, AN4	IO	**Command / Byte Enable.** (Interpreted as C/BE# for AGP 4x and C#/BE for 8x). For AGP cycles these pins provide command information (different commands than for PCI) driven by the master (graphics controller) when requests are being enqueued using GPIPE# (4x only as GPIPE# isn't used in 8x mode). These pins provide valid byte information during AGP write transactions and are driven by the master. The target (this chip) drives these lines to "0000" during the return of AGP read data. For PCI cycles, commands are driven with GFRAME# assertion. Byte enables corresponding to supplied or requested data are driven on following clocks.
GPAR	AN3	IO	**AGP Parity.** A single parity bit is provided over GD[31:0] and GC#BE[3:0].
GDBIH / GPIPE# **GDBIL**	AF4 AG4	IO	**Dynamic Bus Inversion High / Low.** AGP 8x transfer mode only. Driven by the source to indicate whether the corresponding data bit group (GDBIH for GD[31:16] and GDBIL for GD[15:0]) needs to be inverted on the receiving end (1 on GDBIx indicates that the corresponding data bit group should be inverted). Used to limit the number of simultaneously switching outputs to 8 for each 16-pin group. **Pipelined Request.** Not used by AGP 8x. Asserted by the master (external graphics controller) to indicate that a full-width request is to be enqueued by the target (North Bridge). The master enqueues one request each rising edge of GCLK while GPIPE# is asserted. When GPIPE# is deasserted no new requests are enqueued across the AD bus. **Note**: See RxAE[1] for GPIPE# / GDBIH pin function selection.
GADSTB0F (GADSTB0 for 4x), **GADSTB0S** (GADSTB0# for 4x)	AT3 AR3	IO	**Bus Strobe 0.** Source synchronous strobes for GD[15:0] (the agent that is providing the data drives these signals). For 8x transfer mode, GADSTB0 is interpreted as GADSTB0F ("First" strobe) and GADSTB0# as GADSTB0S ("Second" strobe). GADSTB0 and GADSTB0# provide timing for 4x mode.
GADSTB1F (GADSTB1 for 4x), **GADSTB1S** (GADSTB1# for 4x)	AG3 AG1	IO	**Bus Strobe 1.** Source synchronous strobes for GD[31:16] (i.e., the agent that is providing the data drives these signals). For 8x transfer mode, GADSTB1 is interpreted as GADSTB1F ("First" strobe) and GADSTB1# as GADSTB1S ("Second" strobe). GADSTB1 and GADSTB1# provide timing for 4x transfer mode.
GFRAME (GFRAME# for 4x)	AL4	IO	**Frame.** Assertion indicates the address phase of a PCI transfer. Negation indicates that one more data transfer is desired by the cycle initiator. Interpreted as active high for 8x.
GDEVSEL (GDEVSEL# for 4x)	AK1	IO	**Device Select (PCI transactions only).** Driven by the North Bridge when a PCI initiator is attempting to access main memory. Input when the chip is acting as PCI initiator. Not used for AGP cycles. Interpreted as active high for AGP 8x.
GIRDY (GIRDY# for 4x)	AL5	IO	**Initiator Ready.** (Interpreted as active low for PCI/AGP4x and high for AGP 8x). For AGP write cycles, the assertion of this pin indicates that the master is ready to provide all write data for the current transaction. Once this pin is asserted, the master is not allowed to insert wait states. For AGP read cycles, the assertion of this pin indicates that the master is ready to transfer a subsequent block of read data. The master is *never* allowed to insert a wait state during the initial block of a read transaction. However, it may insert wait states after each block transfers. For PCI cycles, asserted when initiator is ready for data transfer.
GTRDY (GTRDY# for 4x)	AK3	IO	**Target Ready.** (Interpreted as active low for PCI/AGP4x and high for AGP 8x). For AGP cycles, indicates that the target is ready to provide read data for the entire transaction (when the transaction can complete within four clocks) or is ready to transfer a (initial or subsequent) block of data when the transfer requires more than four clocks to complete. The target is allowed to insert wait states after each block transfer for both read and write transactions. For PCI cycles, asserted when target is ready for data transfer.

Note: I/O pads for all pins on this page are powered by VCC15AGP. Input voltage levels are referenced to AGPVREF.
Note: The AGP interface pins can be optionally configured as additional interfaces for connecting to external display devices. For simplification of the AGP pin description tables above and on the next page, that multiplexing is not shown here (see "Additional I2C Interfaces" and "Digital Display" pin description tables later in this document for more information).

AGP 8x / 4x Bus Interface (continued)			
Signal Name	**Pin #**	**I/O**	**Signal Description**
AGP8XDET#	AB1	I	**AGP 8x Transfer Mode Detect.** Low indicates that the external graphics card can support 8x transfer mode. Readable in Device 0 Function 0 Rx84[3].
GRBF (GRBF# for 4x)	AE7	I	**Read Buffer Full.** Indicates if the master (graphics controller) is ready to accept previously requested low priority read data. When GRBF# is asserted, the North Bridge will not return low priority read data to the graphics controller.
GWBF (GWBF# for 4x)	AB2	I	**Write Buffer Full.**
GSBA[7:0]# (GSBA[7:0] for 4x)	AE1, AE4, AE3, AE2, AD2, AC3, AC4, AC1	I	**Side Band Address.** Provides an additional bus to pass address and command information from the master (graphics controller) to the target (North Bridge). These pins are ignored until enabled.
GSBSTBF (GSBSTB for 4x), **GSBSTBS** (GSBSTB# for 4x)	AD3 AD1	I	**Side Band Strobe.** Driven by the master to provide timing for GSBA[7:0]. 8x mode uses GSBSTBF ("First" strobe) and GSBSTBS ("Second" strobe). These signals are interpreted as GSBSTB & GSBSTB# for AGP4x.
GST[2:0]	AE6, AE5, AD6	O	**Status (AGP only).** Provides information from the arbiter to a master to indicate what it may do. Only valid while GGNT# is asserted. 000 Indicates that previously requested low priority read or flush data is being returned to the master (graphics controller). 001 Indicates that previously requested high priority read data is being returned to the master. 010 Indicates that the master is to provide low priority write data for a previously enqueued write command. 011 Indicates that the master is to provide high priority write data for a previously enqueued write command. 100 Reserved. (arbiter must not issue, may be defined in the future). 101 Reserved. (arbiter must not issue, may be defined in the future). 110 Reserved. (arbiter must not issue, may be defined in the future). 111 Indicates that the master (graphics controller) has been given permission to start a bus transaction. The master may enqueue AGP requests by asserting GPIPE# or start a PCI transaction by asserting GFRAME#. GST[2:0] are always outputs from the target (North Bridge) and inputs to the master (graphics controller).
GREQ (GREQ# for 4x)	AD4	I	**Request.** Master (graphics controller) request for use of the AGP bus.
GGNT (GGNT# for 4x)	AD5	O	**Grant.** Permission is given to the master (graphics controller) to use the AGP bus.
GSERR (GSERR# for 4x)	AN1	IO	**System Error.**
GSTOP (GSTOP# for 4x)	AM3	IO	**Stop.** Asserted by the target to request the master to stop the current transaction. Interpreted as active high for AGP 8x.

Note: I/O pads for all pins on this page are powered by VCC15AGP. Input voltage levels are referenced to AGPVREF.

Note: The AGP interface pins can be optionally configured as additional interfaces for connecting to external display devices. For simplification of the AGP pin description tables above and on the next page, that multiplexing is not shown here (see "Additional I2C Interfaces" and "Digital Display" pin description tables later in this document for more information).

Note: Separate system interrupts are not provided for AGP. The AGP connector provides interrupts via PCI bus INTA-B#.

Note: A separate reset is not required for the AGP bus (RESET# resets both PCI and AGP buses)

Note: Two mechanisms are provided by the AGP bus to enqueue master requests: GPIPE# (to send addresses multiplexed on the AD lines) and the GSBA port (to send addresses unmultiplexed). AGP masters implement one or the other or select one at initialization time (they are not allowed to change during runtime). Only one of the two will be used; the signals associated with the other will not be used. GRBF# has an internal pullup to maintain it in the de-asserted state in case it is not implemented on the master device. AGP 8x mode allows only GSBA (GPIPE# isn't used in 8x mode).

Note: AGP 8x signal levels are 0V and 0.8V. AGP 8x mode maintains most signals at a low level when inactive resulting in no current flow.

Ultra V-Link Pin Descriptions

Ultra V-Link Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
VD15, **VD14,** **VD13,** **VD12,** **VD11,** **VD10,** **VD9,** **VD8,** **VD7,** **VD6,** **VD5**, **VD4**, **VD3**, **VD2**, **VD1**, **VD0**	AP13 AN13 AR6 AT6 AM12 AP12 AN6 AM7 AP11 AM11 AP7 AR7 AR11 AN10 AR8 AP8	IO IO IO IO IO IO IO IO IO IO IO IO IO IO IO IO	**V-Link Data Bus.** During system initialization, VD[7:0] are used to transmit strap information from the South Bridge (the straps are not on the VD pins but are on the indicated pins of the South Bridge chip). Check the strap pin table for details.
VPAR	AT7	IO	**V-Link Parity.**
VBE#	AN7	IO	**V-Link Byte Enable.**
UPCMD	AN12	I	**V-Link Command from Client (South Bridge) to Host (North Bridge).**
UPSTB+	AM10	I	**V-Link Strobe from Client to Host.**
UPSTB–	AM9	I	**V-Link Complement Strobe from Client to Host.**
DNCMD	AP10	O	**V-Link Command from Host (North Bridge) to Client (South Bridge).**
DNSTB+	AN9	O	**V-Link Strobe from Host to Client.**
DNSTB–	AP9	O	**V-Link Complement Strobe from Host to Client.**

Note: I/O pads for the pins in the above table are powered by VCC15VL. Input voltage levels are referenced to VLVREF.

CRT and Serial Bus Pin Descriptions

CRT Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
AR	R1	AO	**Analog Red.** Analog red output to the CRT monitor.
AG	R2	AO	**Analog Green.** Analog green output to the CRT monitor.
AB	R3	AO	**Analog Blue.** Analog blue output to the CRT monitor.
HSYNC	U4	O	**Horizontal Sync.** Output to CRT.
VSYNC	U3	O	**Vertical Sync.** Output to CRT.
RSET	V7	AI	**Reference Resistor.** Tie to GNDDAC through an external 82Ω 1% resistor to control the RAMDAC full-scale current value. See Design Guide for details.

I/O pads for the pins in the above table are powered by VCC33GFX (i.e., 3.3V I/O).

SMB / I2C Interface				
Signal Name	**AGP Name**	**Pin #**	**I/O**	**Signal Description**
SBPLCLK	GIRDY	AL5	IO	**I2C Serial Bus Clock for Panel (Muxed on AGP Bus Pins).**
SBPLDAT	GC#BE1	AL3	IO	**I2C Serial Bus Data for Panel (Muxed on AGP Bus Pins).**
SBDDCCLK	GREQ	AD4	IO	**I2C Serial Bus Clock for CRT DDC (Muxed on AGP Bus Pins).**
SBDDCDAT	GGNT	AD5	IO	**I2C Serial Bus Data for CRT DDC (Muxed on AGP Bus Pins).**
SPCLK2 **SPCLK1** / CAPD12 **SPDAT2,** **SPDAT1** / CAPD13	n/a n/a n/a n/a	T3 V3 T4 V4	IO	**Serial Port (SMB/I2C) Clock and Data.** The SPCLKn pins are the clocks for serial data transfer. The SPDATn pins are the data signals used for serial data transfer. SPxxx1 is typically used for DVI monitor communications and SPxxx2 is typically used for DDC for CRT monitor communications. These pins are programmed via "Sequencer" graphics registers (port 3C5) in the "Extended" VGA register space (see the UniChrome-II Graphics Registers document for additional details). The SPxxx1 registers are programmed via 3C5.31 ("IIC Serial Port Control 1") and the SPxxx2 registers are programmed via 3C5.26 ("IIC Serial Port Control 0"). In both registers, the clock out state is programmed via bit-5 and the data out state via bit-4, clock in status may be read in bit-3 and data in status in bit-2, and the port may be enabled via bit-0.

I/O pads for SPCLK[2:1] / SPDAT[2:1] above are powered by VCC33GFX (i.e., 3.3V I/O).
All other pins in the above table are powered by VCC15AGP (i.e., 1.5V I/O).

Dedicated Digital Video Port 0 (DVP0) Pin Descriptions

The DVP0 dedicated Digital Video Port can be configured as either a TV Encoder interface port or a Video Capture input port, selectable via strap pins DVP0D[6:5] (see the TV Encoder Interface and Video Capture Interface pin descriptions for details).

Dedicated Digital Video Port 0 (DVP0)			
Signal Name	**Pin #**	**I/O**	**Signal Description**
DVP0D11 / TVD11 / CAPD11, **DVP0D10** / TVD10 / CAPD10 / strap, **DVP0D9** / TVD9 / CAPD9 / strap, **DVP0D8** / TVD8 / CAPD8 / strap, **DVP0D7** / TVD7 / CAPD7 / strap, **DVP0D6** / TVD6 / CAPD6 / strap, **DVP0D5** / TVD5 / CAPD5 / strap, **DVP0D4** / TVD4 / CAPD4 / strap, **DVP0D3** / TVD3 / CAPD3 / strap, **DVP0D2** / TVD2 / CAPD2 / strap, **DVP0D1** / TVD1 / CAPD1 / strap, **DVP0D0** / TVD0 / CAPD0 / strap	AA6 AB6 AB5 Y7 Y6 Y5 AA4 Y2 Y3 AA5 W2 W1	O	**Digital Video Port 0 Data.** Default output drive is 8 mA. 16 mA may be selected via SR3D[6]=1. NOTE: DVP0D[6:0] are also used for power-up reset straps for the embedded graphics controller. Check the Strap Pin table for details.
DVP0HS / TVHS / CAPHS	W4	O	**Digital Video Port 0 Horizontal Sync.** Internally pulled down.
DVP0VS / TVVS / CAPVS	V1	O	**Digital Video Port 0 Vertical Sync.** Internally pulled down.
DVP0DE / TVDE	W3	O	**Digital Video Port 0 Data Enable.** Internally pulled down.
DVP0DET / TVCLKIN / CAPBCLK	V2	I	**Digital Video Port 0 Display Detect.** If VGA register 3C5.12[5]=0, 3C5.1A[5] will read 1 if display is connected. Tie to GND if not used.
DVP0CLK / TVCLK / CAPACLK	Y4	O	**Digital Video Port 0 Clock.** Internally pulled down.

The terminology "3C5.nn" above refers to the VGA "Sequencer" registers at I/O port 3C5 index "nn"

Dedicated Digital Video Port 0 (DVP0) - TV Encoder Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
TVD11 / DVP0D11 / CAPD11, **TVD10** / DVP0D10 / CAPD10 / strap, **TVD9** / DVP0D9 / CAPD9 / strap, **TVD8** / DVP0D8 / CAPD8 / strap, **TVD7** / DVP0D7 / CAPD7 / strap, **TVD6** / DVP0D6 / CAPD6 / strap, **TVD5** / DVP0D5 / CAPD5 / strap, **TVD4** / DVP0D4 / CAPD4 / strap, **TVD3** / DVP0D3 / CAPD3 / strap, **TVD2** / DVP0D2 / CAPD2 / strap, **TVD1** / DVP0D1 / CAPD1 / strap, **TVD0** / DVP0D0 / CAPD0 / strap	AA6 AB6 AB5 Y7 Y6 Y5 AA4 Y2 Y3 AA5 W2 W1	O	**TV Encoder 0 Data.** To configure DVP0 as a TV Out interface port, pins DVP0D[6:5] must be strapped high. Note: One TV Encoder interface is supported through either DVP0 or GDVP1.
TVHS / DVP0HS / CAPHS	W4	O	**TV Encoder 0 Horizontal Sync.** Internally pulled down.
TVVS / DVP0VS / CAPVS	V1	O	**TV Encoder 0 Vertical Sync.** Internally pulled down.
TVDE / DVP0DE	W3	O	**TV Encoder 0 Display Enable.** Internally pulled down.
TVCLKIN / DVP0DET / CAPBCLK	V2	I	**TV Encoder 0 Clock In.** Feedback from TV encoder. Internally pulled down.
TVCLK / DVP0CLK / CAPACLK	Y4	O	**TV Encoder 0 Clock Out.** Output to TV encoder. Internally pulled down.

The above pins may be connected to an external TV Encoder chip such as a VIA VT1622A or VT1622AM for driving a TV set. I/O pads for the pins on this page are powered by VCC33GFX (3.3V I/O).

Dedicated Digital Video Port 0 (DVP0) CCIR601 / CCIR656 / VIP1.1 / VIP2.0 Video Capture Port (VCP)			
Signal Name	**Pin #**	**I/O**	**Signal Description**
		I	**Video Capture Data.** To configure DVP0 as a video capture port, pin DVP0D6 must be strapped low. Pin Function: 8-Bit Mode 16-Bit Mode
CAPD15 / GPO0	V5		CAPBD7 CAPAD15
CAPD14 / GPOUT	W5		CAPBD6 CAPAD14
CAPD13 / SPDAT1	V4		CAPBD5 CAPAD13
CAPD12 / SPCLK1,	V3		CAPBD4 CAPAD12
CAPD11 / DVP0D11 / TVD11,	AA6		CAPBD3 CAPAD11
CAPD10 / DVP0D10 / TVD10 / strap,	AB6		CAPBD2 CAPAD10
CAPD9 / DVP0D9 / TVD9 / strap,	AB5		CAPBD1 CAPAD9
CAPD8 / DVP0D8 / TVD8 / strap,	Y7		CAPBD0 CAPAD8
CAPD7 / DVP0D7 / TVD7 / strap,	Y6		CAPAD7 CAPAD7
CAPD6 / DVP0D6 / TVD6 / strap,	Y5		CAPAD6 CAPAD6
CAPD5 / DVP0D5 / TVD5 / strap,	AA4		CAPAD5 CAPAD5
CAPD4 / DVP0D4 / TVD4 / strap,	Y2		CAPAD4 CAPAD4
CAPD3 / DVP0D3 / TVD3 / strap,	Y3		CAPAD3 CAPAD3
CAPD2 / DVP0D2 / TVD2 / strap,	AA5		CAPAD2 CAPAD2
CAPD1 / DVP0D1 / TVD1 / strap,	W2		CAPAD1 CAPAD1
CAPD0 / DVP0D0 / TVD0 / strap	W1		CAPAD0 CAPAD0
CAPHS / DVP0HS / TVHS	W4	I	**Video Capture Horizontal Sync.** For capture port "A" (16-bit and 8-bit mode). Internally pulled down.
CAPVS / DVP0VS / TVVS	V1	I	**Video Capture Vertical Sync.** For capture port "A" (16-bit and 8-bit mode). Internally pulled down.
CAPAFLD / BISTIN	V6	I	**Video Capture "A"-Channel TV Field Indicator.** For capture port "A" (16-bit and 8-bit mode).
CAPBCLK / DVP0DET / TVCLKIN	V2	I	**Video Capture Clock B.** Port "B" (8-bit mode) input clock from external video decoder. Internally pulled down. Not used in 16-bit mode.
CAPACLK / DVP0CLK / TVCLK	Y4	I	**Video Capture Clock A.** Port "A" (16-bit and 8-bit mode) input clock from external video decoder. Internally pulled down.

Note: I/O pads for the pins on this page are powered by VCC33GFX (3.3V I/O).

AGP-Multiplexed Digital Video Port 1 (GDVP1) Pin Descriptions

The GDVP1 Digital Video Port is supported through multiplexing its interface signal pins with AGP pins. GDVP1 can be configured as either a TMDS transmitter interface port or a TV Encoder interface port. (see the TMDS Transmitter Interface and TV Encoder Interface pin lists below for details).

AGP-Multiplexed Digital Video Port 1 (GDVP1) – TMDS Interface

Signal Name	AGP Name	Pin #	I/O	Signal Description
GDVP1D11 / GTVD11, **GDVP1D10** / GTVD10, **GDVP1D9** / GTVD9, **GDVP1D8** / GTVD8, **GDVP1D7** / GTVD7, **GDVP1D6** / GTVD6, **GDVP1D5** / GTVD5, **GDVP1D4** / GTVD4, **GDVP1D3** / GTVD3, **GDVP1D2** / GTVD2, **GDVP1D1** / GTVD1, **GDVP1D0** / GTVD0,	GC#BE3 GD26 GD24 GD30 GD28 GD29 GSBA4# GD27 GSBA5# GSBSTBS GSBSTBF GSBA2#	AK5 AH5 AG5 AG6 AH4 AF3 AE2 AG2 AE3 AD1 AD3 AC3	O	**Data.**
GDVP1HS / GTVHS	GSBA3#	AD2	O	**Horizontal Sync.**
GDVP1VS / GTVVS	GSBA0#	AC1	O	**Vertical Sync.**
GDVP1DE / GTVDE	GSBA1#	AC4	O	**Data Enable.**
GDVP1DET	GD31	AF1	I	**Display Detect.** If VGA register 3C5.3E[0] = 1, 3C5.1A[4] will read 1 if a display is connected. Tie to GND if not used.
GDVP1CLK / GTVCLK	GSBA6#	AE4	O	**Clock.**
GDVP1CLK# / GTVCLK#	GSBA7#	AE1	O	**Clock Complement.**

AGP-Multiplexed Digital Video Port 1 (GDVP1) – TV Encoder

Signal Name	AGP Name	Pin #	I/O	Signal Description
GTVD11 / GDVP1D11, **GTVD10** / GDVP1D10, **GTVD9** / GDVP1D9, **GTVD8** / GDVP1D8, **GTVD7** / GDVP1D7, **GTVD6** / GDVP1D6, **GTVD5** / GDVP1D5, **GTVD4** / GDVP1D4, **GTVD3** / GDVP1D3, **GTVD2** / GDVP1D2, **GTVD1** / GDVP1D1, **GTVD0** / GDVP1D0	GC#BE3 GD26 GD24 GD30 GD28 GD29 GSBA4# GD27 GSBA5# GSBSTBS GSBSTBF GSBA2#	AK5 AH5 AG5 AG6 AH4 AF3 AE2 AG2 AE3 AD1 AD3 AC3	O	**Data.**
GTVHS / GDVP1HS	GSBA3#	AD2	O	**Horizontal Sync.** Internally pulled down.
GTVVS / GDVP1VS	GSBA0#	AC1	O	**Vertical Sync.** Internally pulled down.
GTVDE / GDVP1DE	GSBA1#	AC4	O	**Display Enable.** Internally pulled down.
GTVCLKIN / FPDET	GADSTB1S	AG1	I	**Clock In.** Input from TV encoder. Internally pulled down.
GTVCLK / GDVP1CLK	GSBA6#	AE4	O	**Clock Out.** Output to TV encoder. Internally pulled down.
GTVCLK# / GDVP1CLK#	GSBA7#	AE1	O	**Clock Out Complement.** Output to TV encoder. Internally pulled down.

The above pins may be connected to an external TV Encoder chip such as a VIA VT1623 or VT1623M for driving a TV set.

I/O pads for the pins on this page are powered by VCC15AGP (1.5V I/O).

Note: If the FPD port is enabled and TV-out capability is required at the same time, the dedicated TV-out port (DVP0) must be used because pin AG1 will be dedicated to the FPDET function.

AGP-Multiplexed Flat Panel Display Port (FPDP) Pin Descriptions

The FPDP Flat Penel Display Port is supported through multiplexing flat panel display interface signal pins with AGP pins.

24-Bit / Dual 12-Bit Flat Panel Display Interface				
Signal Name	**AGP Name**	**Pin #**	**I/O**	**Signal Description**
FPD23 / FPD0D11, **FPD22 / FPD0D10,** **FPD21 / FPD0D09,** **FPD20 / FPD0D08,** **FPD19 / FPD0D07,** **FPD18 / FPD0D06,** **FPD17 / FPD0D05,** **FPD16 / FPD0D04,** **FPD15 / FPD0D03,** **FPD14 / FPD0D02,** **FPD13 / FPD0D01,** **FPD12 / FPD0D00,** **FPD11 / FPD1D11**, **FPD10 / FPD1D10**, **FPD09 / FPD1D09**, **FPD08 / FPD1D08**, **FPD07 / FPD1D07**, **FPD06 / FPD1D06**, **FPD05 / FPD1D05**, **FPD04 / FPD1D04**, **FPD03 / FPD1D03**, **FPD02 / FPD1D02**, **FPD01 / FPD1D01**, **FPD00 / FPD1D00**	GD11 GD13 GD14 GD15 GC#BE2 GD16 GD17 GD18 GD23 GD20 GD22 GADSTB1F GD1 GD0 GD3 GD4 GD5 GD6 GD7 GADSTB0F GC#BE0 GADSTB0S GD10 GD12	AM4 AN2 AL1 AP1 AK2 AJ3 AJ1 AJ4 AH3 AH1 AK4 AG3 AP2 AT2 AT5 AR4 AT1 AN5 AT4 AT3 AN4 AR3 AR1 AL2	O	**Flat Panel Data.** For 24-bit or dual 12-bit flat panel display modes. Two FPD interface modes, 24-bit and dual 12-bit, are supported. Strapping pin DVP0D4 is used to select the interface mode to the LVDS transmitter chip: Strap High (3C5.12[4]=1): 24-bit Strap Low (3C5.12[4]=0): Dual 12-bit In "24-bit" mode, only one set of control pins is required. However, in dual 12-bit mode, the PN800 provides two sets of control signals that are required for certain LVDS transmitter chips. In 24-bit mode, two operating modes are supported: 3C5.12[4]=1 & 3x5.88[2]=0 & 3x5.88[4]=0 Double data rate: each rising & falling clock edge transmits a complete 24-bit pixel 3C5.12[4]=1 & 3x5.88[2]=0 & 3x5.88[4]=1 Single data rate: each clock rising edge transmits a complete 24-bit pixel In dual 12-bit mode, 3C5.12[4]=0 & 3x5.88[2] = 1 Double data rate: each rising and falling clock edge transmits half (12 bits) of two 24-bit pixels
FPHS	GFRAME	AL4	O	**Flat Panel Horizontal Sync.** 24-bit mode or port 0 in dual 12-bit mode.
FPVS	GDEVSEL	AK1	O	**Flat Panel Vertical Sync.** 24-bit mode or port 0 in dual 12-bit mode.
FPDE	GD19	AK6	O	**Flat Panel Data Enable.** 24-bit mode or port 0 in dual 12-bit mode
FPDET	GADSTB1S	AG1	I	**Flat Panel Detect.** 24-bit mode or port 0 in dual 12-bit mode
FPCLK	GD21	AH2	O	**Flat Panel Clock.** 24-bit mode or port 0 in dual 12-bit mode
FPCLK#	GWBF	AB2	O	**Flat Panel Clock Complement.** 24-bit mode or port 0 in dual 12-bit mode. For double-data-rate data transfers.
FP1HS	GD9	AP3	O	**Flat Panel Horizontal Sync.** For port 1 in dual 12-bit mode.
FP1VS	GPAR	AN3	O	**Flat Panel Vertical Sync.** For port 1 in dual 12-bit mode.
FP1DE	GSERR	AN1	O	**Flat Panel Data Enable.** For port 1 in dual 12-bit mode.
FP1DET / GTVCLKIN	GD8	AM1	I	**Flat Panel Detect.** For port 1 in dual 12-bit mode.
FP1CLK	GD2	AP4	O	**Flat Panel Clock.** For port 1 in dual 12-bit mode.
FP1CLK#	GSTOP	AM3	O	**Flat Panel Clock Complement.** For port 1 in dual 12-bit mode. For double-data-rate data transfers.

Flat Panel Power Control (Muxed with AGP)				
Signal Name	**AGP Name**	**Pin #**	**I/O**	**Signal Description**
ENAVDD	ST1	AE5	IO	**Enable Panel VDD Power.**
ENAVEE	ST0	AD6	IO	**Enable Panel VEE Power.**
ENABLT	ST2	AE6	IO	**Enable Panel Back Light.**

Note: I/O pads for all pins on this page are powered by VCC15AGP (i.e., 1.5V I/O).

Clock, Reset, Power Control, GPIO, Interrupt and Test Pin Descriptions

Clocks, Resets, Power Control, General Purpose I/O, Interrupts and Test				
Signal Name	**Pin #**	**I/O**	**Signal Description**	**Power Plane**
HCLK+	M5	I	**Host Clock.** This pin receives the host CPU clock (100 / 133 / 166 / 200 / 266 MHz). This clock is used by all PN800 logic that is in the host CPU domain.	**VTT**
HCLK–	M6	I	**Host Clock Complement.** Used for Quad Data Transfer on host CPU bus.	**VTT**
MCLKOA	B31	O	**Memory (SDRAM) Clock A.** Output from internal clock generator to external memory interface clock buffer (if required for fanout)	**VCC25MEM**
MCLKIA	A32	I	**Memory (SDRAM) Clock Feedback.** Input from MCLKOA.	**VCC25MEM**
MCLKOB	A31	O	**Memory (SDRAM) Clock B.** Output from internal clock generator to external memory interface clock buffer (if required for fanout)	**VCC25MEM**
DISPCLKI	N3	I	**Dot Clock (Pixel Clock) In.** Used for external EMI reduction circuit if used. Connect to GND if external EMI reduction circuit not implemented.	**VCC33GFX**
DISPCLKO	N4	O	**Dot Clock (Pixel Clock) Out.** Used for external EMI reduction circuit if used. NC if external EMI reduction circuit not implemented.	**VCC33GFX**
GCLK	N7	I	**AGP Clock.** Clock for AGP logic.	**VCC15AGP**
XIN	N5	I	**Reference Frequency Input.** External 14.31818 MHz clock source. All internal graphics controller clocks are synthesized on chip using this frequency as a reference.	**VCC33GFX**
RESET#	AM13	I	**Reset.** Input from the South Bridge chip. When asserted, this signal resets the PN800 and sets all register bits to the default value. The rising edge of this signal is used to sample all power-up strap options	**VSUS15**
PWROK	AP14	I	**Power OK.** Connect to South Bridge and Power Good circuitry.	**VSUS15**
SUSST#	AN14	I	**Suspend Status.** For implementation of the Suspend-to-DRAM feature. Connect to an external pull-up to disable.	**VSUS15**
AGPBUSY# / NMI	AL14	O	**AGP Interface Busy.** Connect to a South Bridge GPIO pin for monitoring the status of the internal AGP bus. See Design Guide for details. Pin function selectable with Device 0 Function 0 RxBE[7] (default = NMI).	**VCC25MEM**
GPOUT / CAPD14	W5	O	**General Purpose Output.** This pin reflects the state of SRD[0].	**VCC33GFX**
GPO0 / CAPD15	V5	O	**General Output Port.** When SR1A[4] is cleared, this pin reflects the state of CR5C[0].	**VCC33GFX**
INTA#	U2	O	**Interrupt.** PCI interrupt output (handled by the interrupt controller in the South Bridge)	**VCC33GFX**
TCLK	W6	I	**Test Clock.** This pin is used for testing and must be connected to GND through a 1K-4.7K ohm resistor for all board designs.	**VCC33GFX**
TESTIN#	C31	I	**Test In.** This pin is used for testing and must be connected to VTT through a 1K-4.7K ohm resistor for all board designs.	**VCC25MEM**
DFTIN#	D32	I	**DFT In.** This pin is used for testing and must be connected to VTT through a 1K-4.7K ohm resistor for all board designs.	**VCC25MEM**
BISTIN / CAPAFLD	V6	I	**BIST In.** This pin is used for testing and must be tied to GND with a 1K-4.7K ohm resistor on all board designs.	**VCC33GFX**

Compensation and Reference Voltage Pin Descriptions

Compensation				
Signal Name	**Pin #**	**I/O**	**Signal Description**	**Power Plane**
HRCOMP	F15	AI	**Host CPU Compensation.** Connect 20.5Ω 1% resistor to ground. Used for Host CPU interface I/O buffer calibration.	**VTT**
VLCOMPP	AM6	AI	**V-Link Compensation.** Connect a 360 Ω 1% resistor to ground.	**VCC15VL**
AGPCOMPN	AB3	AI	**AGP N Compensation.** Connect a 60.4 Ω 1% resistor to VCC15AGP.	**VCC15AGP**
AGPCOMPP	AC6	AI	**AGP P Compensation.** Connect a 60.4 Ω 1% resistor to ground.	**VCC15AGP**

Reference Voltages				
Signal Name	**Pin #**	**I/O**	**Signal Description**	**Power Plane**
GTLVREF	H17	P	**Host CPU Interface AGTL+ Voltage Reference.** 2/3 VTT ±2% typically derived using a resistive voltage divider. See Design Guide.	**VTT**
HDVREF[0:3]	H11, H14, K7, J7	P	**Host CPU Data Voltage Reference.** 2/3 VTT ±2% typically derived using a resistive voltage divider. See Design Guide.	**VTT**
HAVREF[0:1]	H19, G22	P	**Host CPU Address Voltage Reference.** 2/3 VTT ±2% typically derived using a resistive voltage divider. See Design Guide.	**VTT**
HCOMPVREF	G14	P	**Host CPU Compensation Voltage Reference.** 1/3 VTT ±2% typically derived using a resistive voltage divider. See Design Guide.	**VTT**
MEMVREF [0:5]	J29, R29, W29, AE29, AK22, AK17	P	**Memory Voltage Reference.** 0.5 VCC25MEM ±2% typically derived using a resistive voltage divider. See Design Guide.	**VCC25MEM**
VLVREF	AL7	P	**V-Link Voltage Reference.** 0.625V ±2% derived using a resistive voltage divider. See Design Guide.	**VCC15VL**
AGPVREF[0:1]	AF7, AD7	P	**AGP Voltage Reference.** ½ VCC15AGP (0.75V) for AGP 2.0 (4x transfer mode) and 0.23 VCC15AGP (0.35V) for AGP 3.0 (8x transfer mode). See the Design Guide for additional information and circuit implementation details.	**VCC15AGP**

Power Pin Descriptions

Analog Power / Ground			
Signal Name	**Pin #**	**I/O**	**Signal Description**
VCCA33HCK1	M4	P	**Power for Host CPU Clock PLL 1** (3.3V ±5%). Host CPU Clock PLL 1 generates 400 MHz for CPU / DRAM frequencies of multiples of 100, 133, and 200 MHz.
GNDAHCK1	M3	P	**Ground for Host CPU Clock PLL 1.** Connect to main ground plane through a ferrite bead.
VCCA33HCK2	L1	P	**Power for Host CPU Clock PLL 2** (3.3V ±5%). Host CPU Clock PLL 2 generates 500 MHz for CPU / DRAM frequencies of multiples of 166 MHz.
GNDAHCK2	L2	P	**Ground for Host CPU Clock PLL 2.** Connect to main ground plane through a ferrite bead.
VCCA33MCK	D31	P	**Power for Memory Clock PLL** (3.3V ±5%)
GNDAMCK	E31	P	**Ground for Memory Clock PLL.** Connect to main ground plane through a ferrite bead.
VCCA33GCK	M1	P	**Power for AGP Clock PLL** (3.3V ±5%)
GNDAGCK	M2	P	**Ground for AGP Clock PLL.** Connect to main ground plane through a ferrite bead.
VCCA15PLL1	P3	P	**Power for Graphics Controller PLL 1** (1.5V ±5%).
GNDAPLL1	P2	P	**Ground for Graphics Controller PLL 1.** Connect to main ground plane through a ferrite bead.
VCCA15PLL2	P6	P	**Power for Graphics Controller PLL 2** (1.5V ±5%).
GNDAPLL2	N6	P	**Ground for Graphics Controller PLL 2.** Connect to main ground plane through a ferrite bead.
VCCA15PLL3	N1	P	**Power for Graphics Controller PLL 3** (1.5V ±5%).
GNDAPLL3	N2	P	**Ground for Graphics Controller PLL 3.** Connect to main ground plane through a ferrite bead.
VCCA33DAC[1:2]	T5, P4	P	**Power for DAC.** (3.3V ±5%)
GNDADAC[1:3]	T6, P5, R4	P	**Ground for DAC.** Connect to main ground plane through a ferrite bead.

Digital Power / Ground			
Signal Name	**Pin #**	**I/O**	**Signal Description**
VTT	(see pin lists)	P	**Power** for **CPU I/O Interface Logic (15 Pins).** Typical 1.65V (CPU dependent)
VCC25MEM	(see pin lists)	P	**Power** for **Memory I/O Interface Logic (25 Pins).** 2.5V ±5%.
VCC15VL	AD16-17	P	**Power** for **V-Link I/O Interface Logic (2 Pins).** 1.5V ±5%
VCC15AGP	(see pin lists)	P	**Power** for **AGP Bus I/O Interface Logic (6 Pins).** 1.5V ±5%
VCC33GFX	V13, W13, Y13	P	**Power for Graphics Display I/O Logic (3 Pins).** 3.3V ±5%
VCC15	(see pin lists)	P	**Power** for **Internal Logic (51 Pins).** 1.5V ±5%
VSUS15	AT14	P	**Suspend Power (1 Pin).** 1.5V ±5%
GND	(see pin lists)	P	**Digital Ground (161 Pins).** Connect to main ground plane.

Strap Pin Descriptions

Strap Pins (External pullup / pulldown straps are required to select "H" / "L")				
Signal	**Actual Strap Pin**	**Function**	**Description**	**Status Bit**
DVP0D[10,9,7]		-reserved-	Always pulled down	
DVP0D8	DVP0D8	AGP Slot Usage	L: AGP graphics card or VIA AGP Riser installed in AGP slot H: AGP Slot is not in use	3C5.13[3]
DVP0D[6:5]	DVP0D[6:5]	DVP0 Port Configuration	Lx: DVP0 is configured as a Video Capture port HH: DVP0 is configured as a TV Out port	3C5.12[6:5]
DVP0D4	DVP0D4	FPDP Port Configuration	L: Dual 12-Bit FPD interface H: 24-bit FPD interface	3C5.12[4]
DVP0D[3:0]	DVP0D[3:0]	OEM Panel Type	Reserved for customer definition	3C5.12[3:0]
VD7	**VT8235-CD,CE:** SDCS3# **VT8237:** PDCS3#	Number of processors installed	L: Single processor H: Dual processor VD7 is sampled during system initialization; the actual strapping pin is located on the South Bridge.	F2Rx50[6]
VD6	**VT8235-CD,CE:** SDA2 **VT8237:** PDA2	Auto-Configure	L: Disable Auto-Configure H: Enable Auto-Configure VD6 is sampled during system initialization; the actual strapping pin is located on the South Bridge.	F2Rx76[2]
VD5	**VT8235-CD,CE:** SDA1 **VT8237:** PDA1	-reserved-	Must be strapped low. VD5 is sampled during system initialization; the actual strapping pin is located on the South Bridge.	-
VD3	**VT8235-CD:** SA19 **VT8235-CE:** Strap_VD3 **VT8237:** GPIOD	AGTL+ Pullups	L: Enable internal AGTL+ Pullups H: Disable internal AGTL+ Pullups VD3 is sampled during system initialization; the actual strapping pin is located on the South Bridge.	F2Rx52[5]
VD2	**VT8235-CD:** SA18 **VT8235-CE:** Strap_VD2 **VT8237:** GPIOB	IOQ Depth	L: 12-Level deep H: 1-Level deep VD2 is sampled during system initialization; the actual strapping pin is located on the South Bridge.	F2Rx50[7]
VD4, VD1, VD0	**VT8235-CD:** SDA0, SA17, SA16 **VT8235-CE:** SDA0, Strap_VD1, Strap_VD0 **VT8237:** PDA0, GPIOA, GPIOC	FSB Frequency	LLL: 100MHz LLH: 133MHz LHL: 200MHz LHH: 166 MHz HLL: 266 MHz HLH: -reserved- HHL: -reserved- HHH: Auto VD4, VD1 and VD0 are sampled during system initialization; the actual strapping pins are located on the South Bridge.	F2Rx54[7:5]

REGISTERS

Register Overview

The following tables summarize the configuration and I/O registers of the PN800 North Bridge. These tables also document the power-on default value ("Default") and access type ("Acc") for each register. Access type definitions used are RW (Read/Write), RO (Read/Only), "—" for reserved / used (essentially the same as RO), RWC (or just WC) (Read / Write 1's to Clear individual bits), and W1 (Write Once then Read / Only after that). Registers indicated as RW may have some read/only bits that always read back a fixed value (usually 0 if unused); registers designated as RWC or WC may have some read-only or read write bits (see individual register descriptions following these tables for details). All offset and default values are shown in hexadecimal unless otherwise indicated.

The graphics registers are described in a separate document.

Table 7. Registers

I/O Ports

Port #	I/O Port	Default	Acc
22	PCI / AGP Arbiter Disable	00	RW
CFB-8	Configuration Address	0000 0000	RW
CFF-C	Configuration Data	0000 0000	RW

Device 0 Function 0 Registers – AGP

Header Registers

Offset	Configuration Space Header	Default	Acc
1-0	Vendor ID	**1106**	RO
3-2	Device ID	**0259**	RO
5-4	Command	**0006**	**RW**
7-6	Status	**0210**	**WC**
8	Revision ID	**0n**	RO
9	Program Interface	00	RO
A	Sub Class Code	00	RO
B	Base Class Code	**06**	RO
C	-reserved- (Cache Line Size)	00	—
D	Latency Timer	00	**RW**
E	Header Type	**00 or 80**	RO
F	-reserved- (Built In Self Test)	00	—
13-10	Graphics Aperture Base	**0000 0008**	**RW**
14-2B	-reserved-	00	—
2D-2C	Subsystem Vendor ID	0000	**W1**
2F-2E	Subsystem ID	0000	**W1**
30-33	-reserved-	00	—
37-34	Capability Pointer	**0000 0080**	RO
38-3F	-reserved-	00	—

Device-Specific Registers

Offset	AGP Drive Control	Default	Acc
40	AGP Compensation Control / Status	**8x**	RW
41	AGP Output Drive Strength	**63**	RW
42	AGP Pad Drive & Delay Control	**08**	RW
43	AGP Strobe Drive Strength	00	RW
44	AGP GSBA Pad Control	00	RW
45-49	-reserved-	00	—
4A	AGP Hardware Support I	**1F**	RW
4B	AGP Hardware Support II	**C4**	RW
4C	-reserved-	00	—
4D	AGP Capability Header Control	**04**	RW
4E	-reserved-	00	—
4F	Multiple Function Control	00	RW

Offset	AGP Power Management Control	Default	Acc
50	Power Management Capability	**01**	**RO**
51	Power Management Next Pointer	00	**RO**
52	Power Management Capabilities I	02	**RO**
53	Power Management Capabilities II	00	**RO**
54	Power Management Control/Status	00	RW
55	Power Management Status	00	**RO**
56	PCI-to-PCI Bridge Support Extension	00	**RO**
57	Power Management Data	00	**RO**

Offset	Reserved	Default	Acc
58-7F	-reserved- (K8)	00	—

Device-Specific Registers

Offset	AGP 3.0 Control	Default	Acc
83-80	AGP Capabilities	**0030 5002**	**RO**
87-84	AGP Status	**1F00 0A03**	**RO**
8B-88	AGP Command	**1F00 0000**	RW
8F-8C	AGP Isoch Status	**0000 0028**	RW
93-90	AGP GART / TLB Control	0000 0000	RW
97-94	AGP Graphics Aperture Size	**0001 0F00**	RW
9B-98	AGP GART Table Base Low	0000 0000	RW
9F-9C	AGP GART Table Base High	0000 0000	RW
A3-A0	AGP Isochronous Command	0000 0000	RW
A4-B8	-reserved-	0000 0000	—

The registers above are actually offsets from CAPPTR (Rx34).

Offset	AGP Control	Default	Acc
B9	AGP Mixed Control	00	RW
BA	GPRI Isoch Read Counter	00	RW
BB	GPRI Isoch Write Counter	00	RW
BC	AGP Control	00	RW
BD	AGP Latency Timer	**02**	RW
BE	AGP Miscellaneous Control	00	RW
BF	AGP 3.0 Control	00	RW
C0	AGP CKG Control 1	00	RW
C1	AGP CKG Control 2	00	RW
C2	AGP Miscellaneous Control 1	00	RW
C3	AGP Miscellaneous Control 2	00	RW
C4-CF	-reserved-	00	—

Offset	Reserved	Default	Acc
D0-DF	-reserved-	00	—
E0-EF	-reserved-	00	—
F0-FF	-reserved-	00	—

Device 0 Function 1 Registers – Error Reporting

Header Registers

Offset	Configuration Space Header	Default	Acc
1-0	Vendor ID	**1106**	RO
3-2	Device ID for Error Reporting	**1259**	RO
5-4	Command	**0006**	**RW**
7-6	Status	**0200**	**WC**
8	Revision ID	**0n**	RO
9	Program Interface	00	RO
A	Sub Class Code	00	RO
B	Base Class Code	**06**	RO
C	-reserved- (Cache Line Size)	00	—
D	-reserved- (Latency Timer)	00	—
E	-reserved- (Header Type)	00	—
F	-reserved- (Built In Self Test)	00	—
10-2B	-reserved-	00	—
2D-2C	Subsystem Vendor ID	00	**W1**
2F-2E	Subsystem ID	00	**W1**
30-33	-reserved-	00	—
37-34	Capability Pointer	0000 0000	RO
38-3F	-reserved-	00	—

Device-Specific Registers

Offset	V-Link Error Control	Default	Acc
40-4F	-reserved-	00	—
50	NB Vlink Bus Error Status	00	**WC**
51-57	-reserved-	00	—
58	NB Vlink Bus Err Reporting Enable	00	RW
59-5F	-reserved-	00	—

Offset	Host CPU Error Control	Default	Acc
60-7F	-reserved-	00	—

Offset	DRAM Error Control	Default	Acc
80-CF	-reserved-	00	—

Offset	AGP Error Control	Default	Acc
D0-DF	-reserved-	00	—
E0	AGP Error Status 1	00	**WC**
E1	AGP Error Status 2	00	**RO**
E2-E7	-reserved-	00	—
E8	AGP Error Reporting Enable	00	RW
E9-FF	-reserved-	00	—

Device 0 Function 2 Registers – Host CPU

Header Registers

Offset	Configuration Space Header	Default	Acc
1-0	Vendor ID	**1106**	RO
3-2	Device ID for Host CPU Bus	**2259**	RO
5-4	Command	**0006**	**RW**
7-6	Status	**0200**	**WC**
8	Revision ID	**0n**	RO
9	Program Interface	00	RO
A	Sub Class Code	00	RO
B	Base Class Code	**06**	RO
C	-reserved- (Cache Line Size)	00	—
D	-reserved- (Latency Timer)	00	—
E	-reserved- (Header Type)	00	—
F	-reserved- (Built In Self Test)	00	—
10-2B	-reserved-	00	—
2D-2C	Subsystem Vendor ID	00	**W1**
2F-2E	Subsystem ID	00	**W1**
30-33	-reserved-	00	—
37-34	Capability Pointer	0000 0000	RO
38-3F	-reserved-	00	—

Device-Specific Registers

Offset	Host CPU Protocol Control	Default	Acc
40-4F	-reserved-	00	—
50	CPU Interface Request Phase Control	00	RW
51	CPU Interface Basic Control	00	RW
52	CPU Interface Advanced Control	00	RW
53	CPU Interface Arbitration Control	00	RW
54	CPU Frequency	00	RW
55	CPU Miscellaneous Control	00	RW
56	Reorder Latency	00	RW
57	CPU FSB Control	00	RW
58	Delivery / Trigger Control	00	RW
59	IPI Control	00	RW
5A	Destination ID	00	RW
5B	Interrupt Vector	00	RW
5C	CPU Miscellaneous Control	00	RW
5D	Write Policy	00	RW
5E	Bandwidth Timer	00	RW
5F	Miscellaneous Control	00	RW
60	DRDY L Timing 1	00	RW
61	DRDY L Timing 2	00	RW
62	DRDY L Timing 3	00	RW
63	DRDY Q Timing 1	00	RW
64	DRDY Q Timing 2	00	RW
65	DRDY Q Timing 3	00	RW
66	Burst DRDY Timing 1	00	RW
67	Burst DRDY Timing 2	00	RW
68	Lowest Priority CPU ID #0	00	RW
69	Lowest Priority CPU ID #1	00	RW
6A	Lowest Priority CPU ID #2	00	RW
6B	Lowest Priority CPU ID #3	00	RW
6C	Lowest Priority CPU ID #4	00	RW
6D	Lowest Priority CPU ID #5	00	RW
6E	Lowest Priority CPU ID #6	00	RW
6F	Lowest Priority CPU ID #7	00	RW

Offset	Host CPU AGTL+ I/O Control	Default	Acc
70	Host Address (2x) Pullup Drive	00	RW
71	Host Address (2x) Pulldown Drive	00	RW
72	Host Data (4x) Pullup Drive	00	RW
73	Host Data (4x) Pulldown Drive	00	RW
74	AGTL+ Output Delay / Stagger Ctrl	00	RW
75	AGTL+ I/O Control	00	RW
76	AGTL+ Compensation Status	00	RW
77	AGTL+ AutoCompensation Offset	00	RW
78	Host CPU FSB CKG Control	00	RW
79-FF	-reserved-	00	—

Device 0 Function 3 Registers – DRAM

Header Registers

Offset	Configuration Space Header	Default	Acc
1-0	Vendor ID	**1106**	RO
3-2	Device ID for DRAM Control	**3259**	RO
5-4	Command	**0006**	**RW**
7-6	Status	**0200**	**WC**
8	Revision ID	**0n**	RO
9	Program Interface	00	RO
A	Sub Class Code	00	RO
B	Base Class Code	**06**	RO
C	-reserved- (Cache Line Size)	00	—
D	-reserved- (Latency Timer)	00	—
E	-reserved- (Header Type)	00	—
F	-reserved- (Built In Self Test)	00	—
10-2B	-reserved-	00	—
2D-2C	Subsystem Vendor ID	00	**W1**
2F-2E	Subsystem ID	00	**W1**
30-33	-reserved-	00	—
37-34	Capability Pointer	0000 0000	RO
38-3F	-reserved-	00	—

Device-Specific Registers

Offset	DRAM Control	Default	Acc
40-47	DRAM Row Ending Address:		
40	Bank 0 Ending (HA[32:25])	**01**	RW
41	Bank 1 Ending (HA[32:25])	**01**	RW
42	Bank 2 Ending (HA[32:25])	**01**	RW
43	Bank 3 Ending (HA[32:25])	**01**	RW
44	Bank 4 Ending (HA[32:25])	**01**	RW
45	Bank 5 Ending (HA[32:25])	**01**	RW
46	Bank 6 Ending (HA[32:25])	**01**	RW
47	Bank 7 Ending (HA[32:25])	**01**	RW
48	DRAM DIMM #0 Control	00	RW
49	DRAM DIMM #1 Control	00	RW
4A	DRAM DIMM #2 Control	00	RW
4B	DRAM DIMM #3 Control	00	RW
4C-4F	-reserved-	00	—
51-50	DRAM MA Map Type	**2222**	RW
52	DRAM Rank End Address Bit-33	00	RW
53	DRAM Rank Begin Address Bit-33	00	RW
54	DRAM Controller Internal Options	00	RW
55	DRAM Timing for All Banks I	00	RW
56	DRAM Timing for All Banks II	**65**	RW
57	DRAM Timing for All Banks III	**01**	RW
58-5F	-reserved-	00	—
60	DRAM Control	00	RW
61-64	-reserved-	00	—
65	DRAM Arbitration Timer	00	RW
66	DRAM Arbitration Control	00	RW
67	DRAM DQS/SDR,MD Read Delay	00	RW
68	DRAM DDR Control	00	RW

Device-Specific Registers (continued)

Offset	Reserved	Default	Acc
69	DRAM Page Policy Control	00	RW
6A	DRAM Refresh Counter	00	RW
6B	DRAM Arbitration Control	**10**	RW
6C	DRAM Clock Control	00	RW
6D	-reserved-	00	—
6E	DRAM Control	00	RW
6F	-reserved-	00	—
70	DRAM DDR Control 1	00	RW
71	DRAM DDR Control 2	00	RW
72	DRAM DDR Control 3	00	RW
73	DRAM DDR Control 4	00	RW
74	DRAM DQS Input Delay	00	RW
75	-reserved-	00	—
76	DRAM Early Clock Select	00	RW
77	-reserved-	00	—
78	DRAM Timing Control	**13**	RW
79	DRAM DQS Output Control	**01**	RW
7A	DRAM DQS Capture Control Chan A	**44**	RW
7B	DRAM DQS Capture Control Chan B	**04**	RW
7C	DIMM0 DQS Input Delay Offset	00	RW
7D	DIMM1 DQS Input Delay Offset	00	RW
7E	DIMM2 DQS Input Delay Offset	00	RW
7F	DIMM3 DQS Input Delay Offset	00	RW

Offset	ROM Shadow	Default	Acc
80	C-ROM Shadow Control	00	RW
81	D-ROM Shadow Control	00	RW
82	F-ROM Shadow/MemHole/SMI Ctrl	00	RW
83	E-ROM Shadow Control	00	RW

Offset	DRAM Above 4G Control	Default	Acc
84	Low Top Address Low	00	RW
85	Low Top Address High	**FF**	RW
86	SMM / APIC Decoding	**01**	RW
87-9F	-reserved-	00	—

Offset	UMA Control	Default	Acc
A0	CPU Direct Access FB Base	00	RW
A1	CPU Direct Access FB Size	00	RW
A2	VGA Timer	00	RW
A3	Graphics Timer	00	RW
A4	Graphics Miscellaneous Control	00	RW
A5-AF	-reserved-	00	—

Function 3 DRAM Device-Specific Registers (continued)

Offset	GMINT Control	Default	Acc
B0	GMINT Control 1	00	RW
B1	GMINT Control 2	00	RW
B2	GMINT Control 3	00	RW
B3	GMINT Control 4	00	RW
B4	GMINT Control 5	00	RW
B5-BF	-reserved-	00	—

Offset	AGP Controller Interface Control	Default	Acc
C0	AGP Controller Interface Control	00	RW
C1-DF	-reserved-	00	—

Offset	DRAM Drive Control	Default	Acc
E0	DRAM DQSA Drive	00	RW
E1	DRAM DQSB Drive	00	RW
E2	DRAM MDA / DQMA Drive	00	RW
E3	DRAM MDB / DQMB Drive	00	RW
E4	DRAM CS / CKE Drive	00	RW
E5	-reserved-	00	—
E6	DRAM S-Port Drive Control	00	RW
E7	-reserved-	00	—
E8	DRAM MAA / BAA / ScmdA Drive	00	RW
E9	-reserved-	00	—
EA	DRAM MAB / BAB / ScmdB Drive	00	RW
EB	-reserved-	00	—
EC	Channel A Duty Cycle Control	00	RW
ED	Channel B Duty Cycle Control	00	RW
EE	DDR CKG Duty Cycle Control 1	00	RW
EF	DDR CKG Duty Cycle Control 2	00	RW
F0-FF	-reserved-	00	—

Device 0 Function 4 Registers – Power Management

Header Registers

Offset	Configuration Space Header	Default	Acc
1-0	Vendor ID	**1106**	RO
3-2	Device ID for Power Manager	**4259**	RO
5-4	Command	**0006**	**RW**
7-6	Status	**0200**	**WC**
8	Revision ID	**0n**	RO
9	Program Interface	00	RO
A	Sub Class Code	00	RO
B	Base Class Code	**06**	RO
C	-reserved- (Cache Line Size)	00	—
D	-reserved- (Latency Timer)	00	—
E	-reserved- (Header Type)	00	—
F	-reserved- (Built In Self Test)	00	—
10-3F	-reserved-	00	—

Device-Specific Registers

Offset	Reserved	Default	Acc
40-4F	-reserved-	00	—
50-5F	-reserved-	00	—
60-6F	-reserved-	00	—
70-7F	-reserved-	00	—
80-8F	-reserved-	00	—
90-9F	-reserved-	00	—

Offset	Power Management Control	Default	Acc
A0	Power Management Mode	00	RW
A1	DRAM Power Management	00	RW
A2	Dynamic Clock Stop	00	RW
A3	MA / SCMD Pad Toggle Reduction	00	RW
A4-AF	-reserved-	00	—

Offset	Reserved	Default	Acc
B0-BF	-reserved-	00	—
C0-CF	-reserved-	00	—

Offset	BIOS Scratch	Default	Acc
D0-EF	BIOS Scratch Registers	00	RW

Offset	Test	Default	Acc
F0-FF	Reserved (Do Not Program)	00	RW

Device 0 Function 7 Registers – V-Link / PCI

Header Registers

Offset	Configuration Space Header	Default	Acc
1-0	Vendor ID	**1106**	RO
3-2	Device ID for V-Link Control	**7259**	RO
5-4	Command	**0006**	**RW**
7-6	Status	**0200**	**WC**
8	Revision ID	**0n**	RO
9	Program Interface	00	RO
A	Sub Class Code	00	RO
B	Base Class Code	**06**	RO
C	-reserved- (Cache Line Size)	00	—
D	-reserved- (Latency Timer)	00	—
E	-reserved- (Header Type)	00	—
F	-reserved- (Built In Self Test)	00	—
10-2B	-reserved-	00	—
2D-2C	Subsystem Vendor ID	00	**W1**
2F-2E	Subsystem ID	00	**W1**
30-33	-reserved-	00	—
37-34	Capability Pointer	0000 0000	RO
38-3F	-reserved-	00	—

Device-Specific Registers

Offset	V-Link Control	Default	Acc
40	V-Link Revision ID	**40**	**RO**
41	V-Link NB Capability	**39**	**RO**
42	V-Link NB Downlink Command	**88**	RW
43	V-Link NB Uplink Max Req Depth	**80**	RW
44	V-Link NB Uplink Buffer Size	**82**	RW
45	V-Link NB Bus Timer	**44**	RW
46	V-Link NB Misc Control	00	RW
47	V-Link Control	00	RW
48	V-Link NB/SB Configuration	**18**	RW
49	V-Link SB Capability	**19**	**WC**
4A	V-Link SB Downlink Status	**88**	**RO**
4B	V-Link SB Uplink Max Req Depth	**80**	RW
4C	V-Link SB Uplink Buffer Size	**82**	RW
4D	V-Link SB Bus Timer	**44**	RW
4E	CCA Master High Priority	00	RW
4F	V-Link SB Miscellaneous Control	00	RW
Offset	**Bank 7 End (same as F3Rx47)**	**Default**	**Acc**
50-56	-reserved-	00	—
57	Bank 7 Ending Address	**01**	**RO**
58-5F	-reserved-	00	—
Offset	**ROM Shadow (same as F3Rx80-82)**	**Default**	**Acc**
60	-reserved-	00	—
61	C-ROM Shadow Control	00	RW
62	D-ROM Shadow Control	00	RW
63	F-ROM Shadow/MemHole/SMI Ctrl	00	RW
64	E-ROM Shadow Control	00	RW
65-6F	-reserved-	00	—

Device-Specific Registers (continued)

Offset	PCI Bus Control	Default	Acc
70	PCI Buffer Control	00	RW
71	CPU to PCI Flow Control	**48**	**WC**
72	-reserved-	00	—
73	PCI Master Control	00	RW
74	-reserved-	00	—
75	PCI Arbitration 1	00	RW
76	PCI Arbitration 2	00	RW
77-7F	-reserved-	00	—

Offset	GART	Default	Acc
80-83	-reserved-	00	—
85-84	Graphics Aperture Size	0000	RW
86-87	-reserved-	00	—
88	GART Base Address	00	RW
89-8F	-reserved-	00	—

Offset	Reserved	Default	Acc
90-9F	-reserved-	00	—
A0-AF	-reserved-	00	—

Offset	V-Link Compenation / Drive Ctrl	Default	Acc
B0	V-Link CKG Control 1	00	RW
B1	V-Link CKG Control 2	00	RW
B2	-reserved-	00	—
B4	V-Link NB Compensation Control	00	RW
B5	V-Link NB Strobe Drive Control	00	RW
B6	V-Link NB Data Drive Control	00	RW
B7	V-Link NB Receive Strobe Delay	00	RW
B8	V-Link SB Compensation Control	00	RW
B9	V-Link SB Strobe Drive Control	00	RW
BA-BF	-reserved-	00	—

Offset	Reserved	Default	Acc
C0-CF	-reserved-	00	—
D0-DF	-reserved-	00	—

Offset	DRAM > 4G (same as F3Rx84-86)	Default	Acc
E0-E3	-reserved-	00	—
E4	Low Top Address Low	00	RW
E5	Low Top Address High	**FF**	RW
E6	SMM / APIC Decoding	**01**	RW
E7-EF	-reserved-	00	—

Offset	Reserved	Default	Acc
F0-FF	-reserved-	00	—

Device 1 Registers - PCI-to-PCI Bridge

Header Registers

Offset	Configuration Space Header	Default	Acc
1-0	Vendor ID	**1106**	RO
3-2	Device ID	**B198**	RO
5-4	Command	**0007**	**RW**
7-6	Status	**0230**	**WC**
8	Revision ID	**nn**	RO
9	Program Interface	00	RO
A	Sub Class Code	**04**	RO
B	Base Class Code	**06**	RO
C	-reserved- (Cache Line Size)	00	—
D	-reserved- (Latency Timer)	00	—
E	Header Type	**01**	RO
F	-reserved- (Built In Self Test)	00	—
13-10	Graphics Aperture Base	**0000 0008**	**RW**
14-17	-reserved-	00	—
18	Primary Bus Number	00	**RW**
19	Secondary Bus Number	00	**RW**
1A	Subordinate Bus Number	00	**RW**
1B	-reserved-	00	—
1C	I/O Base	**F0**	**RW**
1D	I/O Limit	00	**RW**
1F-1E	Secondary Status	0000	RO
21-20	Memory Base	**FFF0**	**RW**
23-22	Memory Limit (Inclusive)	0000	**RW**
25-24	Prefetchable Memory Base	**FFF0**	**RW**
27-26	Prefetchable Memory Limit	0000	**RW**
28-33	-reserved-	00	—
34	Capability Pointer	**70**	RO
35-3F	-reserved-	00	—

Device-Specific Registers

Offset	AGP Bus Control	Default	Acc
40	CPU-to-AGP Flow Control 1	00	RW
41	CPU-to-AGP Flow Control 2	**08**	RW
42	AGP Master Control	00	RW
43	AGP Master Latency Timer	**22**	RW
44	Reserved (Do Not Program)	**20**	RW
45	Fast Write Control	**72**	RW
47-46	PCI-to-PCI Bridge Device ID	0000	RW
48-6F	-reserved-	00	—

Offset	Power Management	Default	Acc
70	Capability ID	**01**	**RO**
71	Next Pointer	00	**RO**
72	Power Management Capabilities 1	**02**	**RO**
73	Power Management Capabilities 2	00	**RO**
74	Power Management Control / Status	00	RW
75	Power Management Status	00	**RO**
76	PCI-PCI Bridge Support Extensions	00	**RO**
77	Power Management Data	00	**RO**
78-FF	-reserved-	00	—

Miscellaneous I/O

One I/O port is defined: Port 22.

Port 22 – PCI / AGP Arbiter Disable ..... RW

- **7-2 Reserved** .....always reads 0
- **1 AGP Arbiter Disable**
  - 0 Respond to GREQ# signal ..... default
  - 1 Do not respond to GREQ# signal
- **0 PCI Arbiter Disable**
  - 0 Respond to all REQ# signals ..... default
  - 1 Do not respond to any REQ# signals, including PREQ#

This port can be enabled for read/write access by setting bit-7 of Device 0 Configuration Register 78.

Configuration Space I/O

All North Bridge registers (listed above) are addressed via the following configuration mechanism:

Mechanism #1

These ports respond only to double-word accesses. Byte or word accesses will be passed on unchanged.

Port CFB-CF8 - Configuration Address.....RW

- **31 Configuration Space Enable**
  - 0 Disabled ..... default
  - 1 Convert configuration data port writes to configuration cycles on the PCI bus
- **30-24 Reserved** .....always reads 0
- **23-16 PCI Bus Number**
  Used to choose a specific PCI bus in the system
- **15-11 Device Number**
  Used to choose a specific device in the system (devices 0 and 1 are defined)
- **10-8 Function Number**
  Used to choose a specific function if the selected device supports multiple functions (functions 0-4 and 7 are defined for device 0 but the function number is unused / ignored for Device 1).
- **7-2 Register Number (also called the "Offset")**
  Used to select a specific DWORD in the configuration space
- **1-0 Fixed** .....always reads 0

Port CFF-CFC - Configuration Data.....RW

Refer to PCI Bus Specification Version 2.2 for further details on operation of the above configuration registers.

Device 0 Function 0 Registers - AGP

Device 0 Function 0 Header Registers

All registers are located in PCI configuration space. They should be programmed using PCI configuration mechanism 1 through CF8 / CFC with bus number, function number, and device number equal to zero and function number equal to 0.

Offset 1-0 - Vendor ID (1106h)..... RO

15-0 ID Code (reads 1106h to identify VIA Technologies)

Offset 3-2 - Device ID (0259h) ..... RO

15-0 ID Code (reads 0259h to identify the PN800 NB)

Offset 5-4 –Command (0006h) ..... RW

15-10 Reserved .....always reads 0

9 Fast Back-to-Back Cycle Enable .....RO
- 0 Fast back-to-back transactions only allowed to the same agent ..... default
- 1 Fast back-to-back transactions allowed to different agents

8 SERR# Enable.....RO
- 0 SERR# driver disabled..... default
- 1 SERR# driver enabled

7 Address / Data Stepping.....RO
- 0 Device never does stepping ..... default
- 1 Device always does stepping

6 Parity Error Response..... **RW**
- 0 Ignore parity errors & continue..... default
- 1 Take normal action on detected parity errors

5 VGA Palette Snoop .....RO
- 0 Treat palette accesses normally ..... default
- 1 Don't respond to palette accesses on PCI bus

4 Memory Write and Invalidate Command.....RO
- 0 Bus masters must use Mem Write ..... default
- 1 Bus masters may generate Mem Write & Inval

3 Special Cycle Monitoring.....RO
- 0 Does not monitor special cycles ..... default
- 1 Monitors special cycles

2 PCI Bus Master.....RO
- 0 Never behaves as a bus master
- 1 Can behave as a bus master ..... default

1 Memory Space.....RO
- 0 Does not respond to memory space
- 1 Responds to memory space..... default

0 I/O Space .....RO
- 0 Does not respond to I/O space ..... default
- 1 Responds to I/O space

Offset 7-6 – Status (0210h) .....RWC

15 Detected Parity Error
- 0 No parity error detected ..... default
- 1 Error detected in either address or data phase. This bit is set even if error response is disabled (command register bit-6). .....write one to clear

14 Signaled System Error (SERR# Asserted) .....always reads 0

13 Signaled Master Abort
- 0 No abort received..... default
- 1 Transaction aborted by the master ....write one to clear

12 Received Target Abort
- 0 No abort received..... default
- 1 Transaction aborted by the target ....write one to clear

11 Signaled Target Abort.....always reads 0
- 0 Target Abort never signaled

10-9 DEVSEL# Timing
- 00 Fast
- 01 Medium .....always reads 01
- 10 Slow
- 11 Reserved

8 Data Parity Error Detected
- 0 No data parity error detected ..... default
- 1 Error detected in data phase. Set only if error response enabled via command bit-6 = 1 and the North Bridge was initiator of the operation in which the error occurred....write one to clear

7 Fast Back-to-Back Capable .....always reads 0

6 User Definable Features.....always reads 0

5 66MHz Capable .....always reads 0

4 Supports New Capability list.....always reads 1

3-0 Reserved .....always reads 0

Offset 8 - Revision ID (0nh).....RO

7-0 Chip Revision Code .....always reads 0nh

Offset 9 - Programming Interface (00h) .....RO

7-0 Interface Identifier .....always reads 00h

Offset A - Sub Class Code (00h) .....RO

7-0 Sub Class Code.....reads 00 to indicate Host Bridge

Offset B - Base Class Code (06h) .....RO

7-0 Base Class Code ..reads 06 to indicate Bridge Device

Offset D - Latency Timer (00h).....RW

Specifies the latency timer value in PCI bus clocks.

7-3 Guaranteed Time Slice for CPU ..... default=0

2-0 Reserved (fixed granularity of 8 clks) ...always read 0

Bits 2-1 are writeable but read 0 for PCI specification compatibility. The programmed value may be read back in Rx75[6-4] (PCI Arbitration 1).

Device 0 Function 0 Header Registers (continued)

Offset E - Header Type (00h) ..... RO

7-0 Header Type Code
.....Rx4F[0]=0: reads 00h: single function
.....Rx4F[0]=1: reads 80h, multi function

Offset F - Built In Self Test (BIST) (00h)..... RO

7 BIST Supported .....reads 0: no supported functions
6-0 Reserved .....always reads 0

Offset 13-10 - Graphics Aperture Base (AGP 2.0) (00000008h) ..... RW

This register is interpreted per the following definition if Rx4D[2]=0 (AGP 2.0 header at Rx80h).

31-28 Upper Programmable Base Address Bits.....def=0
27-20 Lower Programmable Base Address Bits.....def=0
These bits behave as if hardwired to 0 if the corresponding AGP 2.0 Graphics Aperture Size register bit (Device 0 Function 0 Offset B4h) is 0.

27	26	25	24	23	22	21	20	(Base)
7	6	5	4	3	2	1	0	(Size)
RW	RW	RW	RW	RW	RW	RW	RW	1M
RW	RW	RW	RW	RW	RW	RW	0	2M
RW	RW	RW	RW	RW	RW	0	0	4M
RW	RW	RW	RW	RW	0	0	0	8M
RW	RW	RW	RW	0	0	0	0	16M
RW	RW	RW	0	0	0	0	0	32M
RW	RW	0	0	0	0	0	0	64M
RW	0	0	0	0	0	0	0	128M
0	0	0	0	0	0	0	0	256M

19-4 Reserved .....always reads 0
3 Prefetchable..... **always reads 1**
Indicates that the locations in the address range defined by this register are prefetchable.
2-1 Type .....always reads 0
Indicates the address range in the 32-bit address space.
0 Memory Space.....always reads 0
Indicates the address range in the memory address space.

Offset 13-10 - Graphics Aperture Base (AGP 3.0) (00000008h) .....RW

This register is interpreted per the following definition if Rx4D[2]=1 (AGP 3.0 header at Rx80h).

31-22 Programmable Base Address Bits..... def=0
These bits behave as if hardwired to 0 if the corresponding AGP 3.0 Graphics Aperture Size register bit (Device 0 Function 0 Offset 94h) is 0.

31	30	29	28	-	-	27	26	25	24	23	22	(Base)
11	10	9	8	7	6	5	4	3	2	1	0	(Size)
RW	RW	RW	RW	0	0	RW	RW	RW	RW	RW	RW	4M
RW	RW	RW	RW	0	0	RW	RW	RW	RW	RW	0	8M
RW	RW	RW	RW	0	0	RW	RW	RW	RW	0	0	16M
RW	RW	RW	RW	0	0	RW	RW	RW	0	0	0	32M
RW	RW	RW	RW	0	0	RW	RW	0	0	0	0	64M
RW	RW	RW	RW	0	0	RW	0	0	0	0	0	128M
RW	RW	RW	RW	0	0	0	0	0	0	0	0	256M
RW	RW	RW	0	0	0	0	0	0	0	0	0	512M
RW	RW	0	0	0	0	0	0	0	0	0	0	1G
RW	0	0	0	0	0	0	0	0	0	0	0	2G-max
0	0	0	0	0	0	0	0	0	0	0	0	4G

21-4 Reserved .....always reads 0
3 Prefetchable.....**always reads 1**
Indicates that the locations in the address range defined by this register are prefetchable.
2-1 Type .....always reads 0
Indicates the address range in the 32-bit address space.
0 Memory Space.....always reads 0
Indicates the address range in the memory address space.

Offset 2D-2C – Subsystem Vendor ID (0000h) R/W1

15-0 Subsystem Vendor ID..... default = 0
This register may be written once and is then read only.

Offset 2F-2E – Subsystem ID (0000h) R/W1

15-0 Subsystem ID..... default = 0
This register may be written once and is then read only.

Offset 37-34 - Capability Pointer (CAPPTR).....RO

Contains an offset from the start of configuration space.

31-0 AGP Capability List Ptr....always reads 0000 0080h

Device 0 Function 0 Device-Specific Registers

These registers are normally programmed once at system initialization time.

AGP Drive Control

Offset 40 – AGP Pad Control / Status (8xh) ..... RW

7 AGP 4x Strobe VREF Control
- 0 STB VREF is STB# and vice versa
- 1 STB VREF is AGPVREF ..... **default**

This bit is valid only in 4x and 8x mode, otherwise the action is to always use AGPVREF.

6 AGP 4x Strobe & GD Pad Drive Strength
- 0 Drive strength set to compensation circuit default ..... default
- 1 Drive strength controlled by RxF1[7-0]

5-3 AGP Compensation Circuit N Control Output RO

2-0 AGP Compensation Circuit P Control Output. RO

Note: N = low drive, P = high drive

Offset 41 – AGP Drive Strength (63h)..... RW

7-4 AGP Output Buffer Low Drive Strength .....def=6

3-0 AGP Output Buffer High Drive Strength .....def=3

Offset 42 – AGP Pad Drive / Delay (08h)..... RW

7 GD/GBE/GADSTB, GSBA/GSBS Control
- 0 GSBA / GSBS = no cap ..... default
  GD / GC#BE / GADSTB = no cap
- 1 GSBA / GSBS = **cap**
  GD / GC#BE / GADSTB = **cap**

6-5 GD / GC#BE Receive Strobe Delay
- 00 None ..... default
- 01 Delay by 150 psec
- 10 Delay by 300 psec
- 11 Delay by 450 psec

4 GD[31-16] Staggered Delay
- 0 None ..... default
- 1 GD[31:16] delayed by 1 ns

3 AGP Slew Rate Control
- 0 Disable
- 1 Enable..... **default**

2 GSBA Receive Strobe Delay
- 0 None ..... default
- 1 Delay by 150 psec

1-0 GADSTB Output Delay
- 00 None ..... default
- 01 Delay by 150 psec
- 10 Delay by 300 psec
- 11 Delay by 450 psec

(GADSTB1 & GADSTB1# will be delayed an additional 1ns if bit-4 = 1)

Offset 43 – AGP Strobe Drive Strength ..... RW

7-4 AGP Strobe Output Low Drive Strength ..... def=0

3-0 AGP Strobe Output High Drive Strength ..... def=0

AGP Miscellaneous Control

Offset 44 – AGP GSBA Pad Control (00h).....RW

7-3 Reserved ..... always reads 0

2-0 GSBA Pad Control ..... default = 0

Offset 4A – AGP Hardware Support I (1Fh) .....RW

7-0 AGP Request Queue Size..... default = 1Fh

The value in this register will effect the hardware if Rx4D[1]=1

Offset 4B – AGP Hardware Support II (C4h) .....RW

7 AGP Sideband Addressing Mode
- 0 Disable
- 1 Enable .....**default**

6 AGP Enable
- 0 Disable
- 1 Enable .....**default**

5 Reserved ..... always reads 0

4 AGP Fast Write
- 0 Disable ..... default
- 1 Enable

3 AGP 8x Mode
- 0 Disable ..... default
- 1 Enable

2 AGP 4x Mode
- 0 Disable
- 1 Enable .....**default**

1 AGP 2x Mode
- 0 Disable ..... default
- 1 Enable

0 AGP 1x Mode
- 0 Disable ..... default
- 1 Enable

The values in this register will effect the hardware if Rx4D[1]=1

AGP Miscellaneous Control (continued)

Offset 4D – AGP Capability Header Control (04h)..... RW

7-4 Reserved .....always reads 0

3 AGPMajor / Minor Number Backdoor Control
- 0 Major / Minor = 35 ..... default
- 1 Major / Minor = 20

2 Select Rx80 as the AGP20 or AGP30 Header
- 0 Rx80 will be the AGP20 capability header even if the chip is powered up in AGP30 mode
- 1 Rx80 will be the AGP30 capability header when the chip is powered up in AGP30 mode

..... default

1 AGP Hardware Registers Rx4A-4B
- 0 AGP hardware uses the register values defined in the AGP header (either 2.0 or 3.0)..... default
- 1 AGP hardware uses values in Rx4A-4B

0 AGP Header Status Register Write
- 0 Disable..... default
- 1 Enable (status registers in the AGP header can be written)

Offset 4F – Multiple Function Control (00h)..... RW

7-1 Reserved .....always reads 0

0 Bridge Configuration Supports Multiple Functions
- 0 Not supported, other functions 1, 2, 3, 4, and 7 cannot be seen and will return FFFFFFFFh when accessed ..... default
- 1 Supported (this bit is reflected on Rx0E[7])

AGP Power Management Control

Offset 50 – Power Management Capability ID .....RO

7-0 Capability ID.....always reads 01h

Offset 51 – Power Management Next Pointer .....RO

7-0 Next Pointer.....always reads 00h (“Null” Pointer)

Offset 52 – Power Mgmt Capabilities I.....RO

7-0 Power Management Capabilities ..always reads 02h

Offset 53 – Power Mgmt Capabilities II .....RO

7-0 Power Management Capabilities ..always reads 00h

Offset 54 – Power Mgmt Control / Status.....RW

7-2 Reserved .....always reads 0

1-0 Power State
- 00 D0 ..... default
- 01 -reserved-
- 10 -reserved-
- 11 D3 Hot

Offset 55 – Power Management Status .....RO

7-0 Power Management Status .....always reads 00h

Offset 56 – PCI-to-PCI Bridge Support Extensions .....RO

7-0 P2P Bridge Support Extensions ....always reads 00h

Offset 57 – Power Management Data.....RO

7-0 Power Management Data.....always reads 00h

AGP GART / Graphics Aperture

The function of the Graphics Address Relocation Table (GART) is to translate virtual 32-bit addresses issued by an AGP device into 4K-page based physical addresses for system memory access. In this translation, the upper 20 bits (A31-A12) are remapped, while the lower 12 address bits (A11-A0) are used unchanged.

A one-level fully associative lookup scheme is used to implement the address translation. In this scheme, the upper 20 bits of the virtual address are used to point to an entry in a page table located in system memory. Each page table entry contains the upper 20 bits of a physical address (a "physical page" address). For simplicity, each page table entry is 4 bytes. The total size of the page table depends on the GART range (called the "aperture size") which is programmable in the PN800.

This scheme is shown in the figure below.

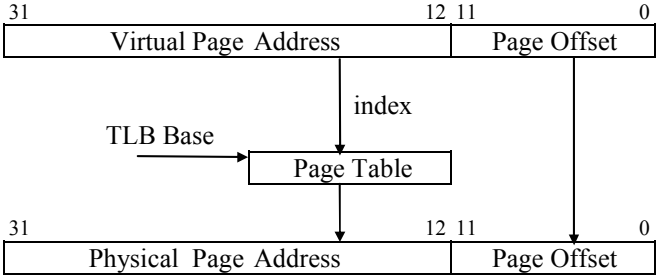


Figure 5. Graphics Aperture Address Translation

Since address translation using the above scheme requires an access to system memory, an on-chip cache (called a "Translation Lookaside Buffer" or TLB) is utilized to enhance performance. The TLB in the PN800 contains 16 entries. Address "misses" in the TLB require an access of system memory to retrieve translation data. Entries in the TLB are replaced using an LRU (Least Recently Used) algorithm.

Addresses are translated only for accesses within the "Graphics Aperture" (GA). The Graphics Aperture can be any power of two in size from 1MB to 256MB (i.e., 1MB, 2MB, 4MB, 8MB, etc) for AGP 2.0 and 4MB to 2GB for AGP 3.0. The base of the Graphics Aperture can be anywhere in the system virtual address space on an address boundary determined by the aperture size (e.g., if the aperture size is 4MB, the base must be on a 4MB address boundary). The Graphics Aperture Base is defined in Device 0 Function 0 Rx10. The Graphics Aperture Size and TLB Table Base are defined in Rx94 and Rx98 along with various control bits.

AGP 3.0 Registers

Offset 83-80 - AGP Capabilities (00305002h)..... RO

31-24 Reserved .....always reads 00
23-20 Major Specification Revision ....always reads 0011b
Major rev # of AGP spec that device conforms to
19-16 Minor Specification Revision ....always reads 0000b
Minor rev # of AGP spec that device conforms to
15-8 Pointer to Next Item ..... always reads 50 (last item)
7-0 AGP Capability ID
(always reads 02 to indicate it is AGP)

Offset 87-84 - AGP Status (1F000A03h) ..... RO

31-18 Reserved ..... always reads 0s†
17 Isochronous Transaction Support
0 Disable..... default
1 Enable
16 Reserved ..... always reads 0s†
15-13 Optimum Async Request Size..... always reads 0s†
Suggested setting is 010b or 2^(2+4)=64 Bytes for 8QW access
12-10 Calibration Cycle Setting for AGP 8x Mode
000 4 ms
001 16 ms
010 64 ms **..... default†**
011 256 ms
9 Supports SideBand Addressing..... **always reads 1**
8 Reserved .....always reads 0†
7 64-Bit GART Entries .....always reads 0
6 CPU GART Translation Not Supported
.....always reads 0
5 Addresses Above 4G Supported.....always reads 0
4 Fast Write Supported .....always reads 0
3 AGP 8x Detected ..... **Set from AGP8XDET# pin**
0 AGP 2.0 Mode
1 AGP 3.0 Mode
2 4X Rate Supported..... Reads 0 if bit-3 = 1
..... Reads 1 if bit-3 = 0
1 2X Rate Supported..... **always reads 1**
0 1X Rate Supported..... **always reads 1**

†Writable if RxFD[0] = 1.

Offset 8B-88 - AGP Command .....RW

31-24 Request Depth (reserved for target).. always reads 0s
23-13 Reserved ..... always reads 0s
12-10 Calibration Cycle Select..... default = 0
9 SideBand Addressing
0 Disable ..... default
1 Enable
8 AGP
0 Disable ..... default
1 Enable
7-6 Reserved ..... always reads 0s
5 Addresses Over 4G
0 Disable ..... default
1 Enable
4 Fast Write
0 Disable ..... default
1 Enable
3 Reserved ..... always reads 0s
2-0 Transfer Mode Select ..... default = 000b
Rx84[3]=0 (8x mode **not detected** via AGP8XDET#)
001 1x data transfer rate
010 2x data transfer rate
100 4x data transfer rate
Rx84[3] = 1 (8x mode **detected** via AGP8XDET#)
000 -reserved..... default
001 4x data transfer rate
010 8x data transfer rate

Offset 8F-8C - AGP Isoch Status (0000 0028h).....RW

31-24 Reserved ..... always reads 0s
23-16 Maximum Bandwidth (Async and Sync).. default=0
(programmed in units of 32 bytes)
15-8 Maximum Number of Isochronous Transactions in a Single Isochronous Period ..... default=0
7-6 Isochronous Payload Sizes Supported
00 32, 64, 128 and 256 bytes ..... default
01 64, 128 and 256 bytes
10 128 and 256 bytes
11 256 bytes
5-3 Maximum Latency for Isochronous Data Transfer
(programmed in units of 1 usec)**..... default = 101b**
2 Reserved ..... always reads 0s
1-0 Isochronous Error Code
00 No error..... default
01 Isoch request overflow
1x -reserved-

AGP 3.0 Registers (continued)

Offset 93-90 - AGP GART / TLB Control ..... RW

31-10 Reserved ..... always reads 0s

9 Calibration Cycle
- 0 Disable..... default
- 1 Enable

8 Graphics Aperture Base Register (Rx13-10) Read
- 0 Disable..... default
- 1 Enable

7 GART TLB
- 0 Disable (TLB entries are invalidated).... default
- 1 Enable

6-0 Reserved ..... always reads 0s

Offset 97-94 - AGP Gfx Aperture Size (0001 0F00h)..... RW

31-28 Aperture Page Size Select..... default = 0000b
Only 4K pages are allowed

27 Reserved ..... always reads 0s

26-16 Page Size Supported .....default = 001h
If bit-n of this field is 1, indicates support of 2^(n+12) page size. Must be set to 001h (field bit-0 set) to indicate only 4K pages allowed.

15-12 Reserved ..... always reads 0s

11-0 Aperture Size

111100111111	4MB
111100111110	8MB
111100111100	16MB
111100111000	32MB
111100110000	64MB
111100100000	128MB
111100000000	256MB**..... default**
111000000000	512MB
110000000000	1GB
100000000000	2GB <= Max supported
000000000000	4GB <= Do not program

Note: When Rx84[3] = 0 (AGP 2.0 mode), only 4MB - 256MB are supported

Offset 9B-98 - AGP 3.0 GART Table Base Low..... RW

31-12 GART Base Address [31:12].....default = 0

11-0 Reserved ..... always reads 0s

Offset 9F-9C - AGP 3.0 GART Table Base High ..... RW

31-0 GART Base Address [63:32].....default = 0
Note: Since aperture sizes over 4G are not presently supported, this register should be written with all zeros.

Offset A3-A0 - AGP Isochronous Command ..... RW

31-8 Reserved ..... always reads 0s

7-6 Isochronous Payload Size.....
..... default = setting of Rx8C[7-6]

5-0 Reserved ..... always reads 0s

AGP Enhanced Control

Offset B9 - AGP Mixed Control .....RW

7 FIFO Control
- 0 MG FIFO=64 QW, IMG FIFO=32 QW.....def
- 1 MG FIFO=96 QW, IMG FIFO=0 QW

6 Hold AGP Data With Transmit Ready
- 0 Disable ..... default
- 1 Enable

5-0 Total # of Isoch Requests ..... default = 000000b

Offset BA - AGP GPRI Isoch Read Counter .....RW

7-0 Counter for Each Isoch Request to Assert GPRI for Isoch Read ..... default = 00h

Offset BB - AGP GPRI Isoch Write Counter.....RW

7-0 Counter for Each Isoch Request to Assert GPRI for Isoch Write ..... default = 00h

Offset BC - AGP Control (00h).....RW

7 AGP
- 0 Disable ..... default
- 1 Enable

6 AGP Read Synchronization
- 0 Disable ..... default
- 1 Enable

5 AGP Read Snoop DRAM Post-Write Buffer
- 0 Disable ..... default
- 1 Enable

4 AGP Read Priority
- 0 GREQ for low priority reads has higher priority if FIFO contains less than 24QW ....def
- 1 GREQ Priority Becomes Higher When Arbiter is Parked at AGP Master

3 GRDY 2T Early Control
- 0 Disable ..... default
- 1 Enable

2 Fence / Flush
- 0 Disable – low priority requests will be executed out of order ..... default
- 1 Enable – all normal priority AGP operations will be executed in order

1 AGP Arbitration Parking
- 0 Disable ..... default
- 1 Enable (GGNT# remains asserted until either GREQ# de-asserts or data phase ready)

0 AGP to PCI Master or CPU to PCI Turnaround Cycle
- 0 2T or 3T Timing ..... default
- 1 1T Timing

Offset BD – AGP Latency Timer (02h) ..... RW

7 AGP Performance Improvement
- 0 Disable ..... default
- 1 Enable

6 Pipe Mode Performance Improvement
- 0 Disable ..... default
- 1 Enable

5 AGP Data Input Enable (for Power Saving)
- 0 AGP data input always enabled ..... default
- 1 AGP data input only enabled when necessary to avoid redundant transitions

4 AGP Performance Improvement
- 0 Disable ..... default
- 1 Enable

3-0 AGP Data Phase Latency Timer ..... default = 02h

Offset BE – AGP Miscellaneous Control (00h) ..... RW

7 NMI / AGPBUSY# Function Select
- 0 NMI ..... default
- 1 AGPBUSY#

6 Assert PP2OFF for Isochronous Requests
- 0 Disable ..... default
- 1 Enable

5 Isoch Read Snoop DRAM Post-Write Buffer
- 0 Disable ..... default
- 1 Enable

4 Guard for Isoch Request With Length Inconsistent with Isoch Payload Size (AGP Isoch Command Register Bits 7-6)
- 0 Isoch read length = payload size ..... default
- 1 Isoch read length = 11b

3-2 Reserved ..... always reads 0s

1 Assert Isochronous Read Ready
- 0 When one block received ..... default
- 1 When entire transaction received

0 CPU GART Read, AGP GART Write Coherency
- 0 Disable ..... default
- 1 Enable

Offset BF – AGP 3.0 Control (00h) ..... RW

7 CPU / PCI Master GART Access
- 0 Disable ..... default
- 1 Enable

6 AGP Calibration
- 0 Disable ..... default
- 1 Enable

5 Mix Coherent / Non-coherent Accesses
- 0 Disable ..... default
- 1 Enable

4 DBIH / PIPE Function Select
- 0 DBIH ..... default
- 1 PIPE#

3 DBI Function
- 0 Disable (DBI input masked and all outputs assume DBI=0) ..... default
- 1 Enable

2 DBI Output for AGP Transactions
- 0 Disable ..... default
- 1 Enable

1 DBI Output for Frame Transactions Including Fast-Write
- 0 Disable ..... default
- 1 Enable

0 DBI Output from Frame Transactions
- 0 Disable ..... default
- 1 Enable

Offset C0 – AGP CKG Control 1 (00h)..... RW

- **7 AGP1 R-Port CKG Rise Time Duty Cycle Control**
- **6 AGP0 R-Port CKG Rise Time Duty Cycle Control**
- **5 AGP1 R-Port CKG Fall Time Duty Cycle Control**
- **4 AGP0 R-Port CKG Fall Time Duty Cycle Control**
- **3 AGP1 S-Port CKG Rise Time Duty Cycle Control**
- **2 AGP0 S-Port CKG Rise Time Duty Cycle Control**
- **1 AGP1 S-Port CKG Fall Time Duty Cycle Control**
- **0 AGP0 S-Port CKG Fall Time Duty Cycle Control**

Offset C1 – AGP CKG Control 2 (00h)..... RW

- **7-4 Reserved** .....always reads 0
- **3 AGP1 D-Port CKG Rise Time Duty Cycle Control**
- **2 AGP0 D-Port CKG Rise Time Duty Cycle Control**
- **1 AGP1 D-Port CKG Fall Time Duty Cycle Control**
- **0 AGP0 D-Port CKG Fall Time Duty Cycle Control**

Offset C2 – AGP Miscellaneous Control 1 (00h) .....RW

- **7 Sync Pipe / Sideband Addressing Request**
  - 0 Disable ..... default
  - 1 Enable
- **6 Fast RM Request**
  - 0 Disable ..... default
  - 1 Enable (decrease 1T from GSBA 2x/4x/8x to access DRAM)
- **5 Fast GADS Conversion**
  - 0 Disable ..... default
  - 1 Enable
- **4-3 AGP Reorder Distance For 16/24/32/48 QW**
- **2 AGP Reorder**
  - 0 Disable ..... default
  - 1 Enable
- **1 Grant Isoch Write When GM FIFO & PWQ are Available for Entire Payload**
  - 0 Disable ..... default
  - 1 Enable
- **0 Grant Assertion Control**
  - 0 Assert GGNT when 1 block of data back.....def
  - 1 Assert GGNT when all data back of this req

Offset C3 – AGP Miscellaneous Control 2 (00h) .....RW

- **7-1 Reserved** ..... always reads 0s
- **0 AGP Data Sync 1T**
  - 0 Disable ..... default
  - 1 Enable

Device 0 Function 1 Registers – Error Reporting

Device 0 Function 1 Header Registers

All registers are located in PCI configuration space. They should be programmed using PCI configuration mechanism 1 through CF8 / CFC with bus number and device number equal to zero and function number equal to 1.

Offset 1-0 - Vendor ID (1106h)..... RO

15-0 ID Code (reads 1106h to identify VIA Technologies)

Offset 3-2 - Device ID for Error Reporting (1259h) ..... RO

15-0 ID Code (reads 1259h to identify PN800 NB virtual device function 1)

Offset 5-4 –Command (0006h) ..... RW

15-10 Reserved .....always reads 0

9 Fast Back-to-Back Cycle Enable .....RO
- 0 Fast back-to-back transactions only allowed to the same agent ..... default
- 1 Fast back-to-back transactions allowed to different agents

8 SERR# Enable.....RO
- 0 SERR# driver disabled..... default
- 1 SERR# driver enabled

7 Address / Data Stepping.....RO
- 0 Device never does stepping ..... default
- 1 Device always does stepping

6 Parity Error Response..... **RW**
- 0 Ignore parity errors & continue..... default
- 1 Take normal action on detected parity errors

5 VGA Palette Snoop .....RO
- 0 Treat palette accesses normally ..... default
- 1 Don't respond to palette accesses on PCI bus

4 Memory Write and Invalidate Command.....RO
- 0 Bus masters must use Mem Write ..... default
- 1 Bus masters may generate Mem Write & Inval

3 Special Cycle Monitoring.....RO
- 0 Does not monitor special cycles ..... default
- 1 Monitors special cycles

2 PCI Bus Master.....RO
- 0 Never behaves as a bus master
- 1 Can behave as a bus master ..... default

1 Memory Space.....RO
- 0 Does not respond to memory space
- 1 Responds to memory space..... default

0 I/O Space .....RO
- 0 Does not respond to I/O space ..... default
- 1 Responds to I/O space

Offset 7-6 – Status (0200h) .....RWC

15 Detected Parity Error
- 0 No parity error detected ..... default
- 1 Error detected in either address or data phase. This bit is set even if error response is disabled (command register bit-6). ..... write 1 to clear

14 Signaled Sys Err (SERR# Asserted) . always reads 0

13 Signaled Master Abort
- 0 No abort received..... default
- 1 Transaction aborted by master . write 1 to clear

12 Received Target Abort
- 0 No abort received..... default
- 1 Transaction aborted by target ... write 1 to clear

11 Signaled Target Abort.....always reads 0
- 0 Target Abort never signaled

10-9 DEVSEL# Timing
- 00 Fast
- 01 Medium .....always reads 01
- 10 Slow
- 11 Reserved

8 Data Parity Error Detected
- 0 No data parity error detected ..... default
- 1 Error detected in data phase. Set only if error response enabled via command bit-6 = 1 and the North Bridge was initiator of the operation in which the error occurred....write one to clear

7 Fast Back-to-Back Capable .....always reads 0

6 User Definable Features.....always reads 0

5 66MHz Capable .....always reads 0

4 Supports New Capability list.....always reads 0

3-0 Reserved .....always reads 0

Offset 8 - Revision ID (0nh).....RO

8-0 Chip Revision Code .....always reads 0nh

Offset 9 - Programming Interface (00h) .....RO

7-0 Interface Identifier .....always reads 00h

Offset A - Sub Class Code (00h) .....RO

7-0 Sub Class Code.....reads 00 to indicate Host Bridge

Offset B - Base Class Code (06h) .....RO

7-0 Base Class Code ..reads 06 to indicate Bridge Device

Offset 2D-2C – Subsystem Vendor ID (0000h) ..... W1 / RO

15-0 Subsystem Vendor ID..... default = 0

This register may be written once and is then read only.

Offset 2F-2E – Subsystem ID (0000h) ..... W1 / RO

15-0 Subsystem ID..... default = 0

This register may be written once and is then read only.

Offset 37-34 - Capability Pointer (CAPPTR).....RO

Contains an offset from the start of configuration space.

31-0 AGP Capability List Ptr....always reads 0000 0000h

Device 0 Function 1 Device-Specific Registers

These registers are normally programmed once at system initialization time.

V-Link Error Reporting

Offset 50 – V-Link Error Status ..... WC

- **7-1 Reserved** .....always reads 0
- **0 V-Link Parity Error Detected by NB..... WC**
  - 0 No V-Link Parity Error Detected..... default
  - 1 V-Link Parity Error Detected (write 1 to clear)

Offset 58 – V-Link Error Reporting Enable..... RW

- **7 Parity Error or SERR# Reported via NMI**
  - 0 Disable..... default
  - 1 Enable
- **6 Parity Error or SERR# Reported to SB via Vlink**
  - 0 Disable..... default
  - 1 Enable
- **5-1 Reserved** .....always reads 0
- **0 V-Link Parity Check Report**
  - 0 Disable..... default
  - 1 Enable

AGP Error Reporting

Offset E0 – AGP / PCI2 Error Status 1 (00h) .....RWC

- **7 AGP Cycle Data Parity Error .....WC**
  - 0 Parity Error did not occur ..... default
  - 1 Parity error occurred..... write 1 to clear
- **6 PCI #2 GSERR Error.....WC**
  - 0 Parity Error did not occur ..... default
  - 1 Parity error occurred..... write 1 to clear
- **5-0 Reserved** .....always reads 0

Offset E1 – AGP / PCI2 Error Status 2 (00h) .....RO

- **7-2 Reserved** .....always reads 0
- **1-0 Isoch Error Code from Func 0 Rx8C[1:0] .....RO**

Offset E8 – AGP / PCI2 Error Reporting Enable (00h).RW

- **7-5 Reserved** .....always reads 0
- **4 Report Data Parity Errors on AGP Cycles**
  - 0 Disable ..... default
  - 1 Enable
- **3-2 Reserved** .....always reads 0
- **1 Report Data Parity Errors on PCI2 Cycles**
  - 0 Disable ..... default
  - 1 Enable
- **0 Report Address Parity Errors on PCI2 Cycles**
  - 0 Disable ..... default
  - 1 Enable

Device 0 Function 2 Registers – Host CPU

Device 0 Function 2 Header Registers

All registers are located in PCI configuration space. They should be programmed using PCI configuration mechanism 1 through CF8 / CFC with bus number and device number equal to zero and function number equal to 2.

Offset 1-0 - Vendor ID (1106h)..... RO

15-0 ID Code (reads 1106h to identify VIA Technologies)

Offset 3-2 - Device ID (2259h) ..... RO

15-0 ID Code (reads 2259h to identify PN800 NB virtual device function 2)

Offset 5-4 –Command (0006h) ..... RW

15-10 Reserved .....always reads 0

9 Fast Back-to-Back Cycle Enable .....RO
- 0 Fast back-to-back transactions only allowed to the same agent ..... default
- 1 Fast back-to-back transactions allowed to different agents

8 SERR# Enable.....RO
- 0 SERR# driver disabled..... default
- 1 SERR# driver enabled

7 Address / Data Stepping.....RO
- 0 Device never does stepping ..... default
- 1 Device always does stepping

6 Parity Error Response..... **RW**
- 0 Ignore parity errors & continue..... default
- 1 Take normal action on detected parity errors

5 VGA Palette Snoop .....RO
- 0 Treat palette accesses normally ..... default
- 1 Don't respond to palette accesses on PCI bus

4 Memory Write and Invalidate Command.....RO
- 0 Bus masters must use Mem Write ..... default
- 1 Bus masters may generate Mem Write & Inval

3 Special Cycle Monitoring.....RO
- 0 Does not monitor special cycles ..... default
- 1 Monitors special cycles

2 PCI Bus Master.....RO
- 0 Never behaves as a bus master
- 1 Can behave as a bus master ..... default

1 Memory Space.....RO
- 0 Does not respond to memory space
- 1 Responds to memory space..... default

0 I/O Space .....RO
- 0 Does not respond to I/O space ..... default
- 1 Responds to I/O space

Offset 7-6 – Status (0200h) .....RWC

15 Detected Parity Error
- 0 No parity error detected ..... default
- 1 Error detected in either address or data phase. This bit is set even if error response is disabled (command register bit-6). .....write one to clear

14 Signaled Sys Err (SERR# Asserted) . always reads 0

13 Signaled Master Abort
- 0 No abort received..... default
- 1 Transaction aborted by master . write 1 to clear

12 Received Target Abort
- 0 No abort received..... default
- 1 Transaction aborted by target ... write 1 to clear

11 Signaled Target Abort.....always reads 0
- 0 Target Abort never signaled

10-9 DEVSEL# Timing
- 00 Fast
- 01 Medium .....always reads 01
- 10 Slow
- 11 Reserved

8 Data Parity Error Detected
- 0 No data parity error detected ..... default
- 1 Error detected in data phase. Set only if error response enabled via command bit-6 = 1 and the North Bridge was initiator of the operation in which the error occurred....write one to clear

7 Fast Back-to-Back Capable .....always reads 0

6 User Definable Features.....always reads 0

5 66MHz Capable .....always reads 0

4 Supports New Capability list.....always reads 0

3-0 Reserved .....always reads 0

Offset 8 - Revision ID (0nh).....RO

9-0 Chip Revision Code .....always reads 0nh

Offset 9 - Programming Interface (00h) .....RO

7-0 Interface Identifier .....always reads 00h

Offset A - Sub Class Code (00h) .....RO

7-0 Sub Class Code.....reads 00 to indicate Host Bridge

Offset B - Base Class Code (06h) .....RO

7-0 Base Class Code ..reads 06 to indicate Bridge Device

Offset 2D-2C – Subsystem Vendor ID (0000h) ..... W1 / RO

15-0 Subsystem Vendor ID..... default = 0

This register may be written once and is then read only.

Offset 2F-2E – Subsystem ID (0000h) ..... W1 / RO

15-0 Subsystem ID..... default = 0

This register may be written once and is then read only.

Offset 37-34 - Capability Pointer (CAPPTR).....RO

Contains an offset from the start of configuration space.

31-0 AGP Capability List Ptr....always reads 0000 0000h

Device 0 Function 2 Device-Specific Registers

These registers are normally programmed once at system initialization time.

Host CPU Control

Offset 50 – Request Phase Control (00h) ..... RW

- **7 CPU Hardwired IOQ (In Order Queue) Size**
  Default set from the inverse of the VD2 strap. This register can be written 0 to restrict the chip to one level of IOQ.
  - 0 1-Level (strap pulled high)
  - 1 12-Level (strap pulled low)
- **6 Dual CPU Support**
  Default set from the VD7 strap (VT8235 South Bridge SDCS3# pin) or ROMSIP.
  - 0 Single (SB strap pulled low)
  - 1 Dual (SB strap pulled high)
- **5 Fast DRAM Access**
  - 0 Disable..... default
  - 1 Enable
- **4-0 Dynamic Defer Snoop Stall Count**
  (granularity = 2T, normally set to 01000b)

Offset 51 – CPU Interface Basic Control (00h) ..... RW

- **7 CPU Read DRAM Fast Ready**
  - 0 Wait until all 8 QWs are received before DRDY is returned ..... default
  - 1 See Rx60-67 for DRDY timing
- **6 Read Around Write**
  - 0 Disable..... default
  - 1 Enable
- **5 DRQ Control**
  - 0 Non pipelined similar to Pro266..... default
  - 1 Pipelined
- **4 CPU to PCI Read Defer**
  - 0 Disable..... default
  - 1 Enable
- **3 Two Defer / Retry Entries**
  - 0 Disable..... default
  - 1 Enable
- **2 Two Defer / Retry Entries Shared**
  - 0 Each entry is dedicated to 1 CPU ..... default
  - 1 Each entry is shared by 2 CPUs
- **1 PCI Master Pipelined Access**
  - 0 Disable..... default
  - 1 Enable
- **0 Reserved** .....always reads 0

Offset 52 – CPU Interface Advanced Ctrl (00h) .....RW

- **7 CPU RW DRAM 0WS for Back-to-Back Pipeline Access**
  - 0 Disable ..... default
  - 1 Enable
- **6 HREQ High Priority**
  - 0 Disable ..... default
  - 1 Enable
- **5 AGTL+ Pullups**
  Default set from the inverse of the VD3 strap.
  - 0 Disable (strap pulled high)
  - 1 Enable (strap pulled low)
- **4 Reserved** .....always reads 0
- **3 Write Retire Policy After 2 Writes**
  - 0 Disable ..... default
  - 1 Enable
- **2 2-Level Defer Queue with Lock**
  - 0 Normal Operation ..... default
  - 1 Enhanced Operation (this bit should always be set to 1)
- **1 Consecutive Speculative Read**
  - 0 Disable ..... default
  - 1 Enable
- **0 Speculative Read**
  - 0 Disable ..... default
  - 1 Enable

Offset 53 – CPU Arbitration Control (00h).....RW

- **7-4 Host Timer** ..... default = 0
- **3-0 BPRI Timer** (units of 4 HCLKs)..... default = 0

Offset 54 – CPU Frequency (00h) ..... RW

7-5 CPU FSB Frequency..... Set from VD4,1,0 Straps
- 000 100 MHz (all three straps pulled low)
- 001 133 MHz
- 010 200 MHz
- 011 166 MHz
- 100 266 MHz
- 101 -reserved-
- 110 -reserved-
- 111 Auto

4 SDRAM Burst Length of 8
- 0 Disable..... default
- 1 Enable (must be set for 128-bit operation)

3 Fast Host Master Read Ready
- 0 Disable (normal) ..... default
- 1 Enable (1T early)

2 PCI Master 8QW Operation
- 0 Disable..... default
- 1 Enable

1 Sync 1T Conversion
- 0 Transparent..... default
- 1 Sync

0 VPX Mode
- 0 Disable (AGP Mode) ..... default
- 1 Enable (VPX Mode)

Offset 55 – CPU Miscellaneous Control (00h)..... RW

7-6 Snoop Queue
- 00 12-level..... default
- 01 13-level
- 1x 16-level

5 4x Clock Timing Enhancement
- 0 Disable..... default
- 1 Enable (should be set if DPWR# pin is used)

4 Fast Command with 8QW Prefetch
- 0 Disable..... default
- 1 Enable

3 Reserved .....always reads 0

2 Medium Threshold for Write Policy
- 0 Disable..... default
- 1 Enable

1 DRDY Early / Late Timing Select
- 0 2T Early..... default
- 1 2T Late

0 Request Reorder
- 0 Disable..... default
- 1 Enable

Offset 56 – Reorder Latency (00h) .....RW

7-4 Medium Threshold for Write Policy to Improve Memory Read / Write Performance
A setting of 2-4 is recommended..... default = 0h

3-0 Maximum Reorder Latency
- 0000 Disable (same as Rx55[0]=0) ..... default
- 0001 Reorder latency 1 (Rx55[0] must be 1)
- 0010 Reorder latency 2 (Rx55[0] must be 1)
- … …
- 1100 Reorder latency 12 (Rx55[0] must be 1)
- 1101 -reserved-
- 1110 -reserved-
- 1111 -reserved-

Offset 57 – CPU FSB Control (00h) .....RW

7 Host FSB 800 MHz Support
- 0 **Enable**..... default
- 1 **Disable**

6-3 Reserved .....always reads 0

2 CPU Power Saving
- 0 Always assert DPWR# ..... default
- 1 Dynamic gating of DPWR#

1 DPWR# Control (active if bit-2=1)
- 0 Assert DPWR# for both reads & writes default
- 1 Assert DPWR# for reads and APIC writes

0 Reserved .....always reads 0

Offset 58 – Delivery / Trigger Control (00h) .....RW

7 Redirection Hint in Register-Triggered APIC
- 0 ..... default
- 1

6 Trigger Register
- 0 ..... default
- 1

5 Trigger Mode
- 0 ..... default
- 1

4 Delivery Status
- 0 ..... default
- 1

3 Destination Mode
- 0 ..... default
- 1

2-0 Delivery Mode
- 000 ..... default
- 001
- 010
- 011
- 100
- 101
- 110
- 111

Offset 59 – IPI Control (00h)..... RW

7-1 Reserved .....always reads 0

0 Lowest Priority IPI Support

0 Disable..... default

1 Enable

Offset 5A – Destination ID (00h)..... RW

7-0 Destination ID in A[19:12] .....default = 00h

Offset 5B – Interrupt Vector (00h)..... RW

7-0 Interrupt Vector in D[7:0] .....default = 00h

Offset 5C – CPU Miscellaneous Control (00h)..... RW

7 Reserved .....always reads 0

6 Copy / Compare Performance Improvement

0 Disable..... default

1 Enable

5 CPU Bus Ownership

0 Disable..... default

1 Enable

4 Patch D11 in APIC Logic Mode

0 Disable..... default

1 Enable

3 Redirection Hint Information Obtained From

0 Address Field ..... default

1 Data Field

2 Destination Mode Information Obtained From

0 Address Field ..... default

1 Data Field

1 APIC Cluster Mode Support

0 Disable..... default

1 Enable

0 Reserved .....always reads 0

Offset 5D – Write Policy (00h) ..... RW

7-4 Write Request Limit .....default = 0h

3-0 Write Request Base.....default = 0h

Offset 5E – Bandwidth Timer (00h) ..... RW

7-4 Host CPU Bandwidth Timer.....default = 0h

3-0 DRAM Bandwidth Timer .....default = 0h

Offset 5F – CPU Miscellaneous Control (00h) .....RW

7 Same Bank But Different Sub-Bank Considered Off-Page

0 Disable ..... default

1 Enable (reduces post-write burst length and may increase performance)

6 Back-to-Back Fast Read, Burst CPU-to-AGP Read and Burst CPU-to-Memory Read

0 Disable ..... default

1 Enable

5 Machine Error Output

0 Disable ..... default

1 Enable

4 Bus Initialization Output

0 Disable ..... default

1 Enable

3 Reserved (Do Not Program) ..... default = 0

2 Host CPU Bandwidth Limited

0 Disable ..... default

1 Enable

1 DRAM Bandwidth Limited

0 Disable ..... default

1 Enable

0 Improve CPU Access DRAM Read After Write

0 Disable ..... default

1 Enable

Offset 60 – DRDY L Timing Control 1 (00h) ..... RW

7-6 Phase 4 L Wait States .....default = 00b
5-4 Phase 3 L Wait States .....default = 00b
3-2 Phase 2 L Wait States .....default = 00b
1-0 Phase 1 L Wait States .....default = 00b

Offset 61 – DRDY L Timing Control 2 (00h) ..... RW

7-6 Phase 8 L Wait States .....default = 00b
5-4 Phase 7 L Wait States .....default = 00b
3-2 Phase 6 L Wait States .....default = 00b
1-0 Phase 5 L Wait States .....default = 00b

Offset 62 – DRDY L Timing Control 3 (00h) ..... RW

7-4 Reserved .....always reads 0
3-2 Phase 10 L Wait States .....default = 00b
1-0 Phase 9 L Wait States .....default = 00b

Offset 63 – DRDY Q Timing Control 1 (00h)..... RW

7-6 Phase 4 Q Wait States.....default = 00b
5-4 Phase 3 Q Wait States.....default = 00b
3-2 Phase 2 Q Wait States.....default = 00b
1-0 Phase 1 Q Wait States.....default = 00b

Offset 64 – DRDY Q Timing Control 2 (00h)..... RW

7-6 Phase 8 Q Wait States.....default = 00b
5-4 Phase 7 Q Wait States.....default = 00b
3-2 Phase 6 Q Wait States.....default = 00b
1-0 Phase 5 Q Wait States.....default = 00b

Offset 65 – DRDY Q Timing Control 3 (00h)..... RW

7-4 Reserved .....always reads 0
3-2 Phase 10 Q Wait States.....default = 00b
1-0 Phase 9 Q Wait States.....default = 00b

Offset 66 – Burst DRDY Timing Control 1 (00h) .....RW

7 Burst DRDY Wait State #8
6 Burst DRDY Wait State #7
5 Burst DRDY Wait State #6
4 Burst DRDY Wait State #5
3 Burst DRDY Wait State #4
2 Burst DRDY Wait State #3
1 Burst DRDY Wait State #2
0 Burst DRDY Wait State #1
0 0 ws DRDY Burst..... default
1 1 ws DRDY Burst

Offset 67 – Burst DRDY Timing Control 2 (00h) .....RW

7-6 Reserved .....always reads 0
5-4 Burst DRDY Wait State #10-9
0 Disable ..... default
1 Enable
3-0 Reserved .....always reads 0

Offset 68 – Lowest Priority CPU ID #0 (00h).....RO

Offset 69 – Lowest Priority CPU ID #1 (00h).....RO

Offset 6A – Lowest Priority CPU ID #2 (00h).....RO

Offset 6B – Lowest Priority CPU ID #3 (00h).....RO

Offset 6C – Lowest Priority CPU ID #4 (00h).....RO

Offset 6D – Lowest Priority CPU ID #5 (00h).....RO

Offset 6E – Lowest Priority CPU ID #6 (00h).....RO

Offset 6F – Lowest Priority CPU ID #7 (00h) .....RO

Host CPU AGTL+ I/O Control

Offset 70 – Host Address (2x) Pullup Drive..... RW

- **7 Reserved** .....always reads 0
- **6-4 Strobe Pullup Drive (HADSTB#)**.....default = 0
- **3 Reserved** .....always reads 0
- **2-0 Address Pullup Drive (HA,HREQ#)**.....default = 0

Offset 71 – Host Address (2x) Pulldown Drive..... RW

- **7 Reserved** .....always reads 0
- **6-4 Strobe Pulldown Drive (HADSTB#)**.....default = 0
- **3 Reserved** .....always reads 0
- **2-0 Address Pulldown Drive (HA,HREQ#)**..default = 0

Offset 72 – Host Data (4x) Pullup Drive..... RW

- **7 Reserved** .....always reads 0
- **6-4 Strobe Pullup Drive (HDSTBP/N#)** .....default = 0
- **3 Reserved** .....always reads 0
- **2-0 Data Pullup Drive (HD,HDBI#)** .....default = 0

Offset 73 – Host Data (4x) Pulldown Drive..... RW

- **7 Reserved** .....always reads 0
- **6-4 Strobe Pulldown Drive (HDSTBP/N#)**....default = 0
- **3 Reserved** .....always reads 0
- **2-0 Data Pulldown Drive (HD,HDBI#)** .....default = 0

Note: Refer to the PN800 BIOS Porting Guide for recommended settings for these bits for typical system configurations.

Offset 74 – Output Delay / Stagger Control..... RW

- **7-6 Data / Strobe Relative Delay**
  - 00 Data delay = strobe delay + 150 psec .... default
  - 01 Data delay = strobe delay
  - 10 Data delay = strobe delay – 150 psec
  - 11 Data delay = strobe delay – 300 psec
- **5 HD[63:48, 31:16], HDBI[3,1]# Output Stagger**
  - 0 No delay ..... default
  - 1 1 nsec delay
- **4 HA[31:17] Output Stagger**
  - 0 No delay ..... default
  - 1 1 nsec delay
- **3-2 HDSTBP# / HDSTBN# Output Extra Delay**
  - 00 No delay ..... default
  - 01 150 psec delay
  - 10 300 psec delay
  - 11 450 psec delay
- **1-0 HADSTB# Output Extra Delay**
  - 00 No delay ..... default
  - 01 150 psec delay
  - 10 300 psec delay
  - 11 450 psec delay

Offset 75 – AGTL+ I/O Control (00h) .....RW

- **7 AGTL+ 4x Input Increase Delay to Filter Noise**
  - 0 Disable ..... default
  - 1 Enable
- **6 AGTL+ 2x Input Increase Delay to Filter Noise**
  - 0 Disable ..... default
  - 1 Enable
- **5 AGTL+ Slew Rate Control**
  - 0 Disable ..... default
  - 1 Enable
- **4 Increase Delay for First HD Strobe**
  - 0 Disable ..... default
  - 1 Enable
- **3 Input Pullup**
  - 0 Disable ..... default
  - 1 Enable
- **2 AGTL+ Strobe Internal Termination Pullups**
  - 0 Disable ..... default
  - 1 Enable
- **1 AGTL+ Data Internal Termination Pullups**
  - 0 Disable ..... default
  - 1 Enable
- **0 AGTL+ Dynamic Compensation**
  - 0 Disable ..... default
  - 1 Enable

Offset 76 – AGTL+ Comp Status (00h) .....RW

- **7 Select AutoCompensation Drive**
  - 0 Disable ..... default
  - 1 Enable (RxD8-DB set automatically on-chip based on auto compensation results)
- **6-4 AGTL+ Compensation Result** ..... default = x
- **3 AGTL+ POS Function**
  - 0 Inputs always powered ..... default
  - 1 Inputs powered down when not in input mode
- **2 Auto Configure..... Set from VD6 Strap**
  - 0 Disable (strap pulled low)
  - 1 Enable (strap pulled high). AGTL+ Drive settings and other chip configuration settings are stored in ROM, transferred from the South Bridge (via the V-Link bus), and loaded into the PN800 automatically after system reset. Refer to the PN800 BIOS Porting Guide for layout of the AutoConfigure settings in ROM and for recommended bit settings.
- **1 DBI (Dynamic Bus Inversion) Function**
  - 0 Enable ..... default
  - 1 Disable (DBI always high) including DBI Double-check
- **0 DBI Function Method**
  - 0 Calculated By Previous..... default
  - 1 Calculated by GTL Pulldown

Offset 77 – AGTL+ Auto Comp Offset (00h) ..... RW

7-4 AGTL+ Drive Offset to Comp Result for 2x Pad
.....default = 0

3-0 AGTL+ Drive Offset to Comp Result for 4x Pad
.....default = 0

Offset 78 – Host CPU FSB CKG Control (00h) ..... RW

7-6 Fall Time Duty Cycle Control – P6IF S-Port
00 Default timing ..... default
01 Lag 100 psec
10 Lag 200 psec
11 Lag 300 psec

5-4 Rise Time Duty Cycle Control – P6IF S-Port
00 Default timing ..... default
01 Lag 100 psec
10 Lag 200 psec
11 Lag 300 psec

3-2 Fall Time Duty Cycle Control – P6IF
00 Default timing ..... default
01 Lag 100 psec
10 Lag 200 psec
11 Lag 300 psec

1-0 Rise Time Duty Cycle Control – P6IF
00 Default timing ..... default
01 Lag 100 psec
10 Lag 200 psec
11 Lag 300 psec

Device 0 Function 3 Registers – DRAM

Device 0 Function 3 Header Registers

All registers are located in PCI configuration space. They should be programmed using PCI configuration mechanism 1 through CF8 / CFC with bus number and device number equal to zero and function number equal to 3.

Offset 1-0 - Vendor ID (1106h)..... RO

15-0 ID Code (reads 1106h to identify VIA Technologies)

Offset 3-2 - Device ID (3259h) ..... RO

15-0 ID Code (reads 3259h to identify PN800 NB virtual device function 3)

Offset 5-4 –Command (0006h) ..... RW

15-10 Reserved .....always reads 0

9 Fast Back-to-Back Cycle Enable .....RO
- 0 Fast back-to-back transactions only allowed to the same agent..... default
- 1 Fast back-to-back transactions allowed to different agents

8 SERR# Enable.....RO
- 0 SERR# driver disabled..... default
- 1 SERR# driver enabled

7 Address / Data Stepping.....RO
- 0 Device never does stepping ..... default
- 1 Device always does stepping

6 Parity Error Response..... **RW**
- 0 Ignore parity errors & continue..... default
- 1 Take normal action on detected parity errors

5 VGA Palette Snoop .....RO
- 0 Treat palette accesses normally ..... default
- 1 Don't respond to palette accesses on PCI bus

4 Memory Write and Invalidate Command.....RO
- 0 Bus masters must use Mem Write ..... default
- 1 Bus masters may generate Mem Write & Inval

3 Special Cycle Monitoring.....RO
- 0 Does not monitor special cycles ..... default
- 1 Monitors special cycles

2 PCI Bus Master.....RO
- 0 Never behaves as a bus master
- 1 Can behave as a bus master ..... default

1 Memory Space.....RO
- 0 Does not respond to memory space
- 1 Responds to memory space..... default

0 I/O Space .....RO
- 0 Does not respond to I/O space ..... default
- 1 Responds to I/O space

Offset 7-6 – Status (0200h) .....RWC

15 Detected Parity Error
- 0 No parity error detected..... default
- 1 Error detected in either address or data phase. This bit is set even if error response is disabled (command register bit-6). .....write one to clear

14 Signaled Sys Err (SERR# Asserted) .always reads 0

13 Signaled Master Abort
- 0 No abort received..... default
- 1 Transaction aborted by master . write 1 to clear

12 Received Target Abort
- 0 No abort received..... default
- 1 Transaction aborted by target ... write 1 to clear

11 Signaled Target Abort.....always reads 0
- 0 Target Abort never signaled

10-9 DEVSEL# Timing
- 00 Fast
- 01 Medium.....always reads 01
- 10 Slow
- 11 Reserved

8 Data Parity Error Detected
- 0 No data parity error detected ..... default
- 1 Error detected in data phase. Set only if error response enabled via command bit-6 = 1 and the North Bridge was initiator of the operation in which the error occurred....write one to clear

7 Fast Back-to-Back Capable .....always reads 0

6 User Definable Features.....always reads 0

5 66MHz Capable .....always reads 0

4 Supports New Capability list.....always reads 0

3-0 Reserved .....always reads 0

Offset 8 - Revision ID (0nh).....RO

10-0 Chip Revision Code .....always reads 0nh

Offset 9 - Programming Interface (00h) .....RO

7-0 Interface Identifier .....always reads 00h

Offset A - Sub Class Code (00h) .....RO

7-0 Sub Class Code.....reads 00 to indicate Host Bridge

Offset B - Base Class Code (06h) .....RO

7-0 Base Class Code ..reads 06 to indicate Bridge Device

Offset 2D-2C – Subsystem Vendor ID (0000h) ..... W1 / RO

15-0 Subsystem Vendor ID..... default = 0

This register may be written once and is then read only.

Offset 2F-2E – Subsystem ID (0000h) ..... W1 / RO

15-0 Subsystem ID..... default = 0

This register may be written once and is then read only.

Offset 37-34 - Capability Pointer (CAPPTR).....RO

Contains an offset from the start of configuration space.

31-0 AGP Capability List Ptr....always reads 0000 0000h

Device 0 Function 3 Device-Specific Registers

These registers are normally programmed once at system initialization time.

DRAM Control

These registers are normally set at system initialization time and not accessed after that during normal system operation. Some of these registers, however, may need to be programmed using specific sequences during power-up initialization to properly detect the type and size of installed memory (refer to the VIA Technologies PN800 BIOS porting guide for details).

Table 8. System Memory Map

Space	Start	Size	Address Range	Comment
DOS	0	640K	00000000-0009FFFF	Cacheable
VGA	640K	128K	000A0000-000BFFFF	Used for SMM
BIOS	768K	16K	000C0000-000C3FFF	Shadow Ctrl 1
BIOS	784K	16K	000C4000-000C7FFF	Shadow Ctrl 1
BIOS	800K	16K	000C8000-000CBFFF	Shadow Ctrl 1
BIOS	816K	16K	000CC000-000CFFFF	Shadow Ctrl 1
BIOS	832K	16K	000D0000-000D3FFF	Shadow Ctrl 2
BIOS	848K	16K	000D4000-000D7FFF	Shadow Ctrl 2
BIOS	864K	16K	000D8000-000DBFFF	Shadow Ctrl 2
BIOS	880K	16K	000DC000-000DFFFF	Shadow Ctrl 2
BIOS	896K	64K	000E0000-000EFFFF	Shadow Ctrl 3
BIOS	960K	64K	000F0000-000FFFFF	Shadow Ctrl 3
Sys Bus Init	1MB D Top 4G-64K	— 64K	00100000-DRAM Top DRAM Top-FFFEFFFF FFFEFFFF-FFFFFFFF	Can have hole 000Fxxxx alias

Offset 40-47 – DRAM Row Ending Address:

- **Offset 40 – Bank 0 Ending (HA[32:25]) (01h) ..... RW**
- **Offset 41 – Bank 1 Ending (HA[32:25]) (01h) ..... RW**
- **Offset 42 – Bank 2 Ending (HA[32:25]) (01h) ..... RW**
- **Offset 43 – Bank 3 Ending (HA[32:25]) (01h) ..... RW**
- **Offset 44 – Bank 4 Ending (HA[32:25]) (01h) ..... RW**
- **Offset 45 – Bank 5 Ending (HA[32:25]) (01h) ..... RW**
- **Offset 46 – Bank 6 Ending (HA[32:25]) (01h) ..... RW**
- **Offset 47 – Bank 7 Ending (HA[32:25]) (01h) ..... RW**

Note : Refer to the BIOS Porting Guide or BIOS Porting Update Note for detailed programming information.

Offset 48 - DRAM DIMM #0 Control (00h) .....RW

7	**Rank 1 Enable**	default = 0
6	**Rank 0 Enable**	default = 0
5	**Rank 1 Is Above 4GB**	default = 0
4	**Rank 0 Is Above 4GB**	default = 0
3-0	**MA Setting** (see Table 9 below)	default = 0

Offset 49 - DRAM DIMM #1 Control (00h) .....RW

7	**Rank 3 Enable**	default = 0
6	**Rank 2 Enable**	default = 0
5	**Rank 3 Is Above 4GB**	default = 0
4	**Rank 2 Is Above 4GB**	default = 0
3-0	**MA Setting** (see Table 9 below)	default = 0

Offset 4A - DRAM DIMM #2 Control (00h) .....RW

7	**Rank 5 Enable**	default = 0
6	**Rank 4 Enable**	default = 0
5	**Rank 5 Is Above 4GB**	default = 0
4	**Rank 4 Is Above 4GB**	default = 0
3-0	**MA Setting** (see Table 9 below)	default = 0

Offset 4B - DRAM DIMM #3 Control (00h) .....RW

7	**Rank 7 Enable**	default = 0
6	**Rank 6 Enable**	default = 0
5	**Rank 7 Is Above 4GB**	default = 0
4	**Rank 6 Is Above 4GB**	default = 0
3-0	**MA Setting** (see Table 9 below)	default = 0

Table 9. DIMM MA Setting

Columns	12 Rows	13 Rows	14 Rows
8	0000 32 MB/Rank	–	–
9	0001 64 MB/Rank	0100 128 MB/Rank	–
10	0010 128 MB/Rank	0101 256 MB/Rank	1000 512 MB/Rank
11	0011 256 MB/Rank	0110 512 MB/Rank	1001 1 GB/Rank
12	–	0111 1 GB/Rank	1010 2 GB/Rank

Offset 51-50 - DRAM MA Map Type (2222h)..... RW

15-13 Bank 5/4 MA Map Type (see Table 10 below)

12 Bank 5/4 1T Command Rate
- 0 2T Command..... default
- 1 1T Command

11-9 Bank 7/6 MA Map Type (see Table 10 below)

8 Bank 7/6 1T Command Rate
- 0 2T Command..... default
- 1 1T Command

7-5 Bank 1/0 MA Map Type (see Table 10 below)

4 Bank 1/0 1T Command Rate
- 0 2T Command..... default
- 1 1T Command

3-1 Bank 3/2 MA Map Type (see Table 10 below)

0 Bank 3/2 1T Command Rate
- 0 2T Command..... default
- 1 1T Command

Table 10. MA Map Type Encoding

000	–	-reserved
001	64/128Mb	8 / 9-bit Column Address ..... default
010	64/128Mb	9 / 10-bit Column Address
011	64/128Mb	10 / 11-bit Column Address
100	1Gb	10 / 11 / 12-bit Column Address
101	256/512Mb	8-bit Column Address
110	256/512Mb	9-bit Column Address
111	256/512Mb	10 / 11 / 12-bit Column Address

Offset 52 - DRAM Rank End Address Bit-33 (00h) .....RW

7-1 Reserved ..... always reads 0

0 Rank End Address Bit-33 ..... default = 0

Offset 53 - DRAM Rank Begin Address Bit-33 (00h).....RW

7-1 Reserved ..... always reads 0

0 Rank Begin Address Bit-33..... default = 0

Offset 54 - DRAM Controller Internal Options (00h)....RW

7-5 Reserved ..... always reads 0

4 Read-Modify-Write Option
- 0 Disable ..... default
- 1 Enable

3 Apply Same-Channel Constraints on Different Channels
- 0 Disable ..... default
- 1 Enable

2 Two S-Command Buses Are Exclusive & Cannot Operate Simultaneously
- 0 Disable ..... default
- 1 Enable

1-0 Reserved ..... always reads 0

Offset 55 - DRAM Timing for All Banks I (00h)..... RW

7-5 Reserved .....always reads 0

4-3 DQSA[7:4] Input Capture Range for Channel A Fine Tuning (Extra Bit for Function 3 Rx7A[4:0])
- 00 ..... default
- 01
- 10
- 11

2 DIMM Combinations for 128-Bit
- 0 Only Support DIMM0, 2/DIMM1, 3 as 128-bit DRAM..... default
- 1 Support DIMM0, 3/DIMM1, 2 as 128-bit DRAM

1-0 DRAM Rank Decode Address Configuration
- 00 ..... default
- 01
- 10
- 11

Offset 56 - DRAM Timing for All Banks II (65h)..... RW

7-6 Active Command to Precharge Command Period
- 00 TRAS = 6T
- 01 TRAS = 7T **..... default**
- 10 TRAS = 8T
- 11 TRAS = 9T

5-4 CAS Latency
- 00 1.5T
- 01 2T
- 10 2.5T **..... default**
- 11 3T

3-2 ACTIVE to CMD
- 00 TRCD = 2T
- 01 TRCD = 3T **..... default**
- 10 TRCD = 4T
- 11 TRCD = 5T

1-0 Precharge Command to Active Command Period
- 00 TRP = 2T
- 01 TRP = 3T **..... default**
- 10 TRP = 4T
- 11 TRP = 5T

Offset 57 - DRAM Timing for All Banks III (01h) .....RW

7-6 Reserved .....always reads 0

5 Active (0) -> Active (1)
- 0 TRRD = 2T..... default
- 1 TRRD = 3T

4 Write Recovery Time
- 0 2T ..... default
- 1 3T

3 TWTR
- 0 TWTR = 1T ..... default
- 1 TWTR = 2T

2 Increase TRFC For 1 Gbit DRAMs
- 0 Disable ..... default
- 1 Enable

1-0 TRFC (Refresh-to-Active or Refresh-to-Refresh)

	Bit-2=0	Bit-2=1
00	12T	21T
01	13T	22T **.....default**
10	14T	23T
11	15T	24T

Offset 60 – DRAM Control (00h)..... RW

7 0WS Back-to-Back Write to Different DDR Bank
- 0 Disable..... default
- 1 Enable

6 Fast Read to Read Turnaround
- 0 Disable..... default
- 1 Enable (DQS postamble overlap with preamble)

5 Fast Read to Write Turnaround
- 0 Disable..... default
- 1 Enable

4 Fast Write to Read Turnaround
- 0 Disable..... default
- 1 Enable

3-0 Reserved .....always reads 0

Offset 65 - DRAM Arbitration Timer (00h) ..... RW

7-4 AGP Timer (units of 4 DRAM clocks) .....default = 0

3-0 CPU Timer (units of 4 DRAM clocks) .....default = 0

Offset 66 - DRAM Arbitration Control (00h) ..... RW

7 DRAM Controller Queue Greater Than 2
- 0 Disable..... default
- 1 Enable

6 DRAM Controller Queue Not Equal To 4
- 0 Disable..... default
- 1 Enable

5-4 Arbitration Parking Policy
- 00 Park at last bus owner ..... default
- 01 Park at CPU
- 10 Park at AGP
- 11 -reserved-

3-0 AGP / CPU Priority (units of 4 DRAM clocks)

Offset 67 – DRAM DQS/SDR, MD Read Delay (00h) ... RW

7-6 DIMM3 Command/Address Select (on Channel B)

5-4 DIMM2 Command/Address Select (on Channel B)

3-2 DIMM1 Command/Address Select (on Channel A)

1-0 DIMM0 Command/Address Select (on Channel A)
- 00 SCMD / MA Bus A
- 01 SCMD / MA Bus B
- 1x -reserved-

Offset 68 – DRAM DDR Control (00h).....RW

7 DRAM Access Timing
- 0 2T ..... default
- 1 3T

6 Non-Burst Write-to-Write Can Be Closer in Non-DQM Mode
- 0 Disable ..... default
- 1 Enable

5 Zero Delay DRAM Channel Switching for Read Cycles
- 0 Disable ..... default
- 1 Enable

4 Zero Delay DRAM Channel Switching for Write Cycles
- 0 Disable ..... default
- 1 Enable

3-0 DRAM Operating Frequency

	CPU / DRAM	
0000	133 / 133 (DDR-266)	default
	166 / 166 (DDR-333)	
	200 / 200 (DDR-400)	
	266 / 133 (DDR-266)	
0001	100 / 133 (DDR-266)	
	133 / 166 (DDR-333)	
	166 / 200 (DDR-400)	
0101	100 / 166 (DDR-333)	
	133 / 200 (DDR-400)	
1001	100 / 200 (DDR-400)	
0010	166 / 133 (DDR-266)	
	200 / 166 (DDR-333)	
	266 / 200 (DDR-400)	
0110	200 / 133 (DDR-266)	
	266 / 166 (DDR-333)	
1010	266 / 133 (DDR-266)	

All other combinations are reserved.

Offset 69 – DRAM Page Policy Control (00h)..... RW

7-6 Bank Interleave
- 00 No Interleave..... default
- 01 2-way
- 10 4-way
- 11 Reserved

For 16Mb DRAMs bank interleave is always 2-way

5 Reserved .....always reads 0

4 Auto-Precharge for TLB Read or CPU Write-Back
- 0 Disable..... default
- 1 Enable

3 DRAM 8K Page Enable
- 0 Disable..... default
- 1 Enable

2 DRAM 4K Page Enable
- 0 Disable..... default
- 1 Enable

1 Page Kept Active When Crossing Banks
- 0 Disable..... default
- 1 Enable

0 Multiple Page Mode
- 0 Disable..... default
- 1 Enable

Offset 6A - Refresh Counter (00h)..... RW

7-0 Refresh Counter (in units of 16 DRAM clocks)
- 00 DRAM Refresh Disabled..... default
- 01 32 DRAM clocks
- 02 48 DRAM clocks
- 03 64 DRAM clocks
- 04 80 DRAM clocks
- 05 96 DRAM clocks
- … …

The programmed value is the desired number of 16-DRAM clock units minus one.

Offset 6B - DRAM Arbitration Control (10h).....RW

7 DQS Input DLL Adjust
- 0 Disable ..... default
- 1 Enable

6 DQS Output DLL Adjust
- 0 Disable ..... default
- 1 Enable

5 Burst Refresh
- 0 Disable ..... default
- 1 Enable

4 Reserved (Do Not Program) ..... default = 1

3 HA14 / HA22 Swap
- 0 Normal ..... default
- 1 Swap to improve performance

2-0 SDRAM Operation Mode Select
- 000 Normal SDRAM Mode..... default
- 001 NOP Command Enable
- 010 All-Banks-Precharge Command Enable (CPU-to-DRAM cycles are converted to All-Banks-Precharge commands).
- 011 MSR to Low DIMM
- 100 CBR Cycle Enable (if this code is selected, CAS-before-RAS refresh is used; if it is not selected, RAS-Only refresh is used)
- 101 MSR to High DIMM
- 11x Reserved

Offset 6C – DRAM Clock Control (00h)..... RW

7-5 Reserved .....always reads 0

4 DQM Removal (Always Perform 4-Burst R/W)
- 0 Disable..... default
- 1 Enable

3-1 Reserved (Do Not Program).....default = 0

0 DIMM Type
- 0 Unbuffered ..... default
- 1 Registered

Offset 6E – DRAM Control (00h).....RW

7 Reserved .....always reads 0

6 DRAM Scrubber
- 0 Disable ..... default
- 1 Enable

5 DRAM Scrubber Redirect
- 0 Disable ..... default
- 1 Enable

4-3 Reserved .....always reads 0

2 For Double-Sided DIMMs, Interleave Using Address Bit-15
- 0 Disable ..... default
- 1 Enable

1 Select Address Bit 19 Instead of 14 as Sub-Bank Address
- 0 Disable ..... default
- 1 Enable

0 Select Address Bit 18 Instead of 13 as Sub-Bank Address
- 0 Disable ..... default
- 1 Enable

Note: Refer to the PN800 BIOS Porting Guide for SDRAM configuration algorithms and recommended settings for these bits for typical memory system configurations.

Offset 70 – DRAM DDR Control 1 (00h)..... RW

7-0 Channel A DQS Output Delay
00h ..... default
FFh

Offset 71 – DRAM DDR Control 2 (00h)..... RW

7-0 Channel A MD Output Delay
00h ..... default
FFh

Offset 72 – DRAM DDR Control 3 (00h)..... RW

7-0 Channel B DQS Output Delay
00h ..... default
FFh

Offset 73 – DRAM DDR Control 4 (00h)..... RW

7-0 Channel B MD Output Delay
00h ..... default
FFh

Offset 74 – DRAM DQS Input Delay (00h) ..... RW

7 DQS Input Delay Setting
0 Auto ..... default
1 Manual

6 Reserved .....always reads 0

5-0 DQS Input Delay
(if bit-7 = 0, reads DLL calibration result)
00h ..... default
FFh

Offset 76 – DRAM Early Clock Select (00h) ..... RW

7 Early Clock Select - Scmd/MA Bit-2 (see bits 3-2)

6 Early Clock Select - CS, CKE Bit-2 (see bits 1-0)

5-4 Reserved (Do Not Program).....default = 0

3-2 Early Clock Select - Scmd/MA Bits 1-0 (see bit-7)
000 ..... default
001
010
011
100
101
110
111

1-0 Early Clock Select - CS, CKE Bits 1-0 (see bit-6)
000 ..... default
001
010
011
100
101
110
111

Offset 78 – DRAM Timing Control (13h).....RW

7-6 Reserved (Do Not Program) ..... default = 0

5-4 Write MD / DQS / CAS Timing Range Control
00
01 ..... default
10
11

3-0 Reserved (Do Not Program) ..... default = 0

Offset 79 – DRAM DQS Output Control (01h).....RW

7-4 Reserved .....always reads 0

3 DQS / MD Output Enable Gated with DQS Input Enable
0 Disable ..... default
1 Enable

2 DQS Output Long Postamble
0 Disable ..... default
1 Enable

1 DQS Output Long Preamble 2
0 Disable ..... default
1 Enable

0 DQS Output Long Preamble
0 Disable
1 Enable **.....default**

Offset 7A – DRAM DQS Capture Ctrl Chan A (44h) ... RW

7-6 MD Input Internal Timing Control
00
01 ..... **default**
10
11

5 Process DQS Input as in QBM Mode
0 Disable..... default
1 Enable

4-0 DQS Input Capture Range - Channel A
00000
00001
00010
00011
00100 ..... default
00101
…
11111
(Rx55[4:3] contains additional fine tuning bits)

Offset 7B – DRAM DQS Capture Ctrl Chan B (04h).... RW

7-5 Reserved (Do Not Program).....default = 0

4-0 DQS Input Capture Range - Channel B
00000
00001
00010
00011
00100 ..... default
00101
…
11111

Offset 7C – DIMM #0 DQS Input Delay Offset (00h) ....RW

Values are programmed as two's-complement

7-5 Rank 1 DQS Input 2nd-Order Delay Offset
000 ..... default
…
111

4-0 Rank 0 DQS Input Delay Offset
00000 ..... default
…
11111

Offset 7D – DIMM #1 DQS Input Delay Offset (00h) ....RW

Values are programmed as two's-complement

7-5 Rank 3 DQS Input 2nd-Order Delay Offset
000 ..... default
…
111

4-0 Rank 2 DQS Input Delay Offset
00000 ..... default
…
11111

Offset 7E – DIMM #2 DQS Input Delay Offset (00h) ....RW

Values are programmed as two's-complement

7-5 Rank 5 DQS Input 2nd-Order Delay Offset
000 ..... default
…
111

4-0 Rank 4 DQS Input Delay Offset
00000 ..... default
…
11111

Offset 7F – DIMM #3 DQS Input Delay Offset (00h).....RW

Values are programmed as two's-complement

7-5 Rank 7 DQS Input 2nd-Order Delay Offset
000 ..... default
…
111

4-0 Rank 6 DQS Input Delay Offset
00000 ..... default
…
11111

Table 11. 1x Bandwidth (64-Bit DDR) Memory Address Mapping Table

MA:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
64/128Mb																	x32 (14,8)
2K page	28	14	24	14	13	12	11	23	22	21	20	19	18	17	16	15	x16 (14,8)
001	31	28	27	14	13	PC	26	25	10	9	8	7	6	5	4	3	x8 (14,9)
4K page	28	14	25	14	13	12	24	23	22	21	20	19	18	17	16	15	x16 (14,9)
010	31	28	27	14	13	PC	26	11	10	9	8	7	6	5	4	3	x4 (14,10)
8K page	28	14	26	14	13	25	24	23	22	21	20	19	18	17	16	15	x8 (14,10)
011	31	28	27	14	13	PC	12	11	10	9	8	7	6	5	4	3	x4 (14,11)
256/512Mb																	
2K page	28	25	24	14	13	12	11	23	22	21	20	19	18	17	16	15	x32 (15,8)
101	31	29	28	14	13	PC	27	26	10	9	8	7	6	5	4	3	
4K page	28	26	25	14	13	12	24	23	22	21	20	19	18	17	16	15	x32 (15,9)
110	31	29	28	14	13	PC	27	11	10	9	8	7	6	5	4	3	x16 (15,9)
8K page	28	27	26	14	13	25	24	23	22	21	20	19	18	17	16	15	x16 (15,10)
111	31	29	28	14	13	PC	12	11	10	9	8	7	6	5	4	3	x8 (15,10)
																	x8 (15,11)
																	x4 (15,11)
																	x4 (15,12)
1Gb																	
8K page	28	27	26	14	13	25	24	23	22	21	20	19	18	17	16	15	x16 (16,10)
100	31	30	29	14	13	PC	12	11	10	9	8	7	6	5	4	3	x8 (16,11)
																	x4 (16,12)

ROM Shadow Control

Offset 80 – C-ROM Shadow Control (00h) RW

7-6 CC000h-CFFFFh
- 00 Read/write disable ..... default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

5-4 C8000h-CBFFFh
- 00 Read/write disable ..... default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

3-2 C4000h-C7FFFh
- 00 Read/write disable ..... default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

1-0 C0000h-C3FFFh
- 00 Read/write disable ..... default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

Offset 81 – D-ROM Shadow Control (00h)..... RW

7-6 DC000h-DFFFFh
- 00 Read/write disable ..... default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

5-4 D8000h-DBFFFh
- 00 Read/write disable ..... default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

3-2 D4000h-D7FFFh
- 00 Read/write disable ..... default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

1-0 D0000h-D3FFFh
- 00 Read/write disable ..... default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

Offset 82 – F-ROM Shadow /Memory Hole / SMI Control (00h) .....RW

7-6 Reserved ..... always reads 0

5-4 F0000h-FFFFFh
- 00 Read/write disable ..... default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

3-2 Memory Hole
- 00 None ..... default
- 01 512K-640K
- 10 15M-16M (1M)
- 11 14M-16M (2M)

1 Disable A,BK SMRAM Direct Access

0 Enable A,BK DRAM Access

SMI Mapping Control:

Bits	SMM		Non-SMM	
1-0	Code	Data	Code	Data
00	DRAM	DRAM	PCI	PCI
01	DRAM	DRAM	DRAM	DRAM
10	DRAM	PCI	PCI	PCI
11	DRAM	DRAM	DRAM	DRAM

Offset 82 – E-ROM Shadow Control (00h) .....RW

7-6 EC000h-EFFFFh
- 00 Read/write disable ..... default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

5-4 E8000h-EBFFFh
- 00 Read/write disable ..... default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

3-2 E4000h-E7FFFh
- 00 Read/write disable ..... default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

1-0 E0000h-E3FFFh
- 00 Read/write disable ..... default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

DRAM Above 4G Control

Offset 84 – Low Top Address Low (00h) ..... RW

7-4 Low Top Address Low .....default = 0

3-0 DRAM Granularity

0 16M Total DRAM less than 4G..... default
1 32M Total DRAM less than 8G
2 64M Total DRAM less than 16G
3 128M Total DRAM less than 32G
4 256M Total DRAM less than 64G
5-7 -reserved-

Offset 85 – Low Top Address High (FFh)..... RW

7-0 Low Top Address High..... default = FFh

Offset 86 – SMM / APIC Decoding (01h) .....RW

7-6 Reserved .....always reads 0

5 APIC Lowest Interrupt Arbitration

0 Disable ..... default
1 Enable

4 I/O APIC Decoding

0 FECxxxxx accesses go to PCI..... default
1 FEC00000 to FEC7FFFF accesses go to PCI
FEC80000 to FECFFFFF accesses go to AGP

3 MSI (Processor Message) Support

0 Disable (master access to FEExxxxx will go to PCI) ..... default
1 Enable (master access to FEExxxxx will be passed to host side to do snoop)

2 Top SMM

0 Disable ..... default
1 Enable

1 Reserved .....always reads 0

0 Compatible SMM

0 Disable
1 Enable **.....default**

UMA Control

Offset A0 – CPU Direct Access FB Base Address (00h) RW

7-1 CPU Direct Access FB Address [27:21] ..... def = 0

0 CPU Direct Access FB

0 Disable..... default

1 Enable

Offset A1 – CPU Direct Access FB Size (00h) ..... RW

7 VGA

0 Disable..... default

1 Enable

6-4 CPU Direct Access FB Size

000 None ..... default

001 2MB†

010 4MB†

011 8MB†

100 16MB

101 32 MB

110 64 MB

111 -reserved-

†Microsoft WHQL DCT certification requires the frame buffer size to be a minimum of 16MB. Smaller frame buffer sizes are supported for non-Windows applications to reserve more available memory for the system.

3-0 CPU Direct Access FB Address [31:28] ..... def = 0

Offset A2 – VGA Timer 1 (00h) ..... RW

7-4 VGA High Priority Timer..... def = 0

3-0 VGA Timer ..... def = 0

(programmed in units of 16 dot clocks)

Offset A3 – VGA Timer 2 (00h) ..... RW

7-4 Timer to Promote Graphics Priority ..... def = 0

(programmed in units of 16 dot clocks)

3-2 Reserved ..... always reads 0

1-0 Reserved (Do Not Program)..... default = 0

Offset A4 – Graphics Miscellaneous Control (00h) .....RW

7-4 Reserved ..... always reads 0

3 AGP DIO (Pad) Clock

0 Disable ..... default

1 Enable

2 Graphics Data Delay to Sync with Clock

0 No sync ..... default

1 Sync with clock

1-0 Graphics DISPCLK Delay Control

00 ..... default

01

10

11

GMINT Control

Offset B0 – GMINT Control 1 (00h) ..... RW

- **7-4 Reserved** .....always reads 0
- **3 Bank Select Control**
  - 0 Select bank per bits 2-0..... default
  - 1 Select original bank
- **2-0 Frame Buffer Bank**

Offset B1 – GMINT Control 2 (00h) ..... RW

- **7-4 Current High Channel Granted (Normal Priority) and Request Pending Low Request Just Arrived**... .....def = 0
- **3-0 Current Low Channel Granted and Request Pending High Request Just Arrived** .....def = 0

Offset B2 – GMINT Control 3 (00h) ..... RW

- **7-4 Lot Counter for High Channel to Extend Arbitration Slot to High Requests**.....def = 0
- **3-0 Lot Counter for Low Channel to Extend Arbitration Slot to Low Requests**.....def = 0

Offset B3 – GMINT Control 4 (00h) ..... RW

- **7 Reserved** .....always reads 0
- **6-4 GMINT Write Queue Threshold**.....def = 0
- **3-0 GMINT VM FIFO Threshold**.....def = 0

Offset B4 – GMINT Control 5 (00h) ..... RW

- **7-4 Reserved** .....always reads 0
- **3 Graphics Read / Write Order Control**
  - 0 R/W may be out of order ..... default
  - 1 Keep original low channel R/W order as received from graphics controller
- **2 Optimize GMINT Arbitration with DRAM Hit / Miss Consideration**
  - 0 Disable..... default
  - 1 Enable
- **1 Qualify Length from Graphics Controller to Differentiate 2QW / 4QW Requests**
  - 0 Disable..... default
  - 1 Enable
- **0 Alternate Arbitration to Low / High Channel Read When Both Hit**
  - 0 Disable..... default
  - 1 Enable

AGP Controller Interface Control

Offset C0 – AGP Controller Interface Control (00h).....RW

- **7-3 Reserved** .....always reads 0
- **2 Graphics AGP Read Data Delay**
  - 0 No delay..... default
  - 1 Delay 1 clock
- **1 AGP Controller Interface Pipe Mode (Graphics)**
  - 0 Pipe ..... default
  - 1 Pipe bypass
- **0 AGP Controller Interface Pipe Mode (North Bridge)**
  - 0 Pipe ..... default
  - 1 Pipe bypass

DRAM Drive Control

Offset E0 – DRAM DQSA Drive..... RW

7-4 High Drive
0000 Lowest..... default
… …
1111 Highest

3-0 Low Drive
0000 Lowest..... default
… …
1111 Highest

Offset E1 – DRAM DQSB Drive..... RW

7-4 High Drive
0000 Lowest..... default
… …
1111 Highest

3-0 Low Drive
0000 Lowest..... default
… …
1111 Highest

Offset E2 – DRAM MDA, DQMA Drive ..... RW

7-4 High Drive
0000 Lowest..... default
… …
1111 Highest

3-0 Low Drive
0000 Lowest..... default
… …
1111 Highest

Offset E3 – DRAM MDB, DQMB Drive..... RW

7-4 High Drive
0000 Lowest..... default
… …
1111 Highest

3-0 Low Drive
0000 Lowest..... default
… …
1111 Highest

Offset E4 – DRAM CS / CKE Drive..... RW

7-4 High Drive
0000 Lowest..... default
… …
1111 Highest

3-0 Low Drive
0000 Lowest..... default
… …
1111 Highest

Offset E6 – Drive Group S-Port Control (00h) .....RW

7 DQ S-Port Control..... default = 0
6 CS S-Port Control..... default = 0
5 MAA S-Port Control ..... default = 0
4 MAB S-Port Control ..... default = 0
3 DQS S-Port Control..... default = 0
2-1 Reserved ..... always reads 0
0 DQ / DQS / DQM Terminator
0 Disable ..... default
1 Enable

Offset E8 – MAA Drive (MAA, BAA, ScmdA) .....RW

7-4 High Drive
0000 Lowest..... default
… …
1111 Highest

3-0 Low Drive
0000 Lowest..... default
… …
1111 Highest

Offset EA – MAB Drive (MAB, BAB, ScmdB) .....RW

7-4 High Drive
0000 Lowest..... default
… …
1111 Highest

3-0 Low Drive
0000 Lowest..... default
… …
1111 Highest

Offset EC – Channel A Duty Cycle Control.....RW

7-6 DQS Duty Cycle Control – Falling ..... default = 0
5-4 DQS Duty Cycle Control - Rising ..... default = 0
3-2 DQ Duty Cycle Control – Falling..... default = 0
1-0 DQ Duty Cycle Control - Rising..... default = 0

Offset ED – Channel B Duty Cycle Control .....RW

7-6 DQS Duty Cycle Control – Falling ..... default = 0
5-4 DQS Duty Cycle Control - Rising ..... default = 0
3-2 DQ Duty Cycle Control – Falling..... default = 0
1-0 DQ Duty Cycle Control - Rising..... default = 0

Offset EE – DDR CKG Duty Cycle Control 1.....RW

7-2 Reserved ..... always reads 0
1-0 DDR CKG Duty Cycle Control..... default = 0

Offset EF – DDR CKG Duty Cycle Control 2.....RW

7-2 Reserved ..... always reads 0
1-0 DDR CKG Duty Cycle Control..... default = 0

Device 0 Function 4 Registers – Power Management

Device 0 Function 4 Header Registers

All registers are located in PCI configuration space. They should be programmed using PCI configuration mechanism 1 through CF8 / CFC with bus number and device number equal to zero and function number equal to 4.

Offset 1-0 - Vendor ID (1106h)..... RO

15-0 ID Code (reads 1106h to identify VIA Technologies)

Offset 3-2 - Device ID for Power Manager (4259h) ..... RO

15-0 ID Code (reads 4259h to identify PN800 NB virtual device function 4)

Offset 5-4 –Command (0006h) ..... RW

15-10 Reserved .....always reads 0

9 Fast Back-to-Back Cycle Enable .....RO
- 0 Fast back-to-back transactions only allowed to the same agent..... default
- 1 Fast back-to-back transactions allowed to different agents

8 SERR# Enable.....RO
- 0 SERR# driver disabled..... default
- 1 SERR# driver enabled

7 Address / Data Stepping.....RO
- 0 Device never does stepping ..... default
- 1 Device always does stepping

6 Parity Error Response..... **RW**
- 0 Ignore parity errors & continue..... default
- 1 Take normal action on detected parity errors

5 VGA Palette Snoop .....RO
- 0 Treat palette accesses normally ..... default
- 1 Don't respond to palette accesses on PCI bus

4 Memory Write and Invalidate Command.....RO
- 0 Bus masters must use Mem Write ..... default
- 1 Bus masters may generate Mem Write & Inval

3 Special Cycle Monitoring.....RO
- 0 Does not monitor special cycles ..... default
- 1 Monitors special cycles

2 PCI Bus Master.....RO
- 0 Never behaves as a bus master
- 1 Can behave as a bus master ..... default

1 Memory Space.....RO
- 0 Does not respond to memory space
- 1 Responds to memory space..... default

0 I/O Space .....RO
- 0 Does not respond to I/O space ..... default
- 1 Responds to I/O space

Offset 7-6 – Status (0200h) .....RWC

15 Detected Parity Error
- 0 No parity error detected ..... default
- 1 Error detected in either address or data phase. This bit is set even if error response is disabled (command register bit-6). .....write one to clear

14 Signaled System Error (SERR# Asserted) .....always reads 0

13 Signaled Master Abort
- 0 No abort received..... default
- 1 Transaction aborted by the master ....write one to clear

12 Received Target Abort
- 0 No abort received..... default
- 1 Transaction aborted by the target ....write one to clear

11 Signaled Target Abort.....always reads 0
- 0 Target Abort never signaled

10-9 DEVSEL# Timing
- 00 Fast
- 01 Medium.....always reads 01
- 10 Slow
- 11 Reserved

8 Data Parity Error Detected
- 0 No data parity error detected ..... default
- 1 Error detected in data phase. Set only if error response enabled via command bit-6 = 1 and the North Bridge was initiator of the operation in which the error occurred....write one to clear

7 Fast Back-to-Back Capable .....always reads 0

6 User Definable Features.....always reads 0

5 66MHz Capable .....always reads 0

4 Supports New Capability list.....always reads 0

3-0 Reserved .....always reads 0

Offset 8 - Revision ID (0nh).....RO

11-0 Chip Revision Code .....always reads 0nh

Offset 9 - Programming Interface (00h) .....RO

7-0 Interface Identifier .....always reads 00h

Offset A - Sub Class Code (00h) .....RO

7-0 Sub Class Code.....reads 00 to indicate Host Bridge

Offset B - Base Class Code (06h) .....RO

7-0 Base Class Code ..reads 06 to indicate Bridge Device

Device 0 Function 4 Device-Specific Registers

These registers are normally programmed once at system initialization time.

Power Management Control

Offset A0 – Power Management Mode (00h) ..... RW

7 Dynamic Power Management
- 0 Disable..... default
- 1 Enable

6 Halt / Shutdown Power Management
- 0 Disable..... default
- 1 Enable

5 Stop Clock Power Management
- 0 Disable..... default
- 1 Enable

4 Suspend Status Power Management
- 0 Disable..... default
- 1 Enable

3-0 Reserved .....always reads 0

Offset A1 – DRAM Power Management (00h)..... RW

7 Reserved .....always reads 0

6 Dynamic CKE when DRAM Idle
- 0 Disable..... default
- 1 Enable

5 Dynamic DRAM I/O Pad Power Down (Float)
- 0 Disable..... default
- 1 Enable

4-0 Reserved .....always reads 0

Offset A2 – Dynamic Clock Stop Control (00h).....RW

7 Host Interface Power Management
- 0 Disable ..... default
- 1 Enable

6 DRAM Interface Power Management
- 0 Disable ..... default
- 1 Enable

5 V-Link Interface Power Management
- 0 Disable ..... default
- 1 Enable

4 AGP Interface Power Management
- 0 Disable ..... default
- 1 Enable

3 PCI #2 Interface Power Management
- 0 Disable ..... default
- 1 Enable

2 Graphics Interface Power Management
- 0 Disable ..... default
- 1 Enable

1 Reserved .....always reads 0

0 Host Fast Power Management (DADS Fast Timing)
- 0 Disable ..... default
- 1 Enable

Offset A3 – DRAM Pad Toggle Reduction (00h).....RW

7 MA / SCMD Pin Toggle Reduction
- 0 Disable ..... default
- 1 Enable (MA and S command pins won't toggle if not accessed)

6-4 Reserved .....always reads 0

3 DIMM #3 MAA / MAB Select
- 0 MAA ..... default
- 1 MAB

2 DIMM #2 MAA / MAB Select
- 0 MAA ..... default
- 1 MAB

1 DIMM #1 MAA / MAB Select
- 0 MAA ..... default
- 1 MAB

0 DIMM #0 MAA / MAB Select
- 0 MAA ..... default
- 1 MAB

BIOS Scratch

Offset D0-EF – BIOS Scratch Registers .....RW

7-0 No hardware function ..... default = 0

Device 0 Function 7 Registers – V-Link

Device 0 Function 7 Header Registers

All registers are located in PCI configuration space. They should be programmed using PCI configuration mechanism 1 through CF8 / CFC with bus number and device number equal to zero and function number equal to 7.

Offset 1-0 - Vendor ID (1106h)..... RO

15-0 ID Code (reads 1106h to identify VIA Technologies)

Offset 3-2 - Device ID for V-Link Control (7259h)..... RO

15-0 ID Code (reads 7259h to identify the PN800 North Bridge virtual device function 7)

Offset 5-4 –Command (0006h) ..... RW

15-10 Reserved .....always reads 0

9 Fast Back-to-Back Cycle Enable .....RO
- 0 Fast back-to-back transactions only allowed to the same agent..... default
- 1 Fast back-to-back transactions allowed to different agents

8 SERR# Enable.....RO
- 0 SERR# driver disabled..... default
- 1 SERR# driver enabled

7 Address / Data Stepping.....RO
- 0 Device never does stepping ..... default
- 1 Device always does stepping

6 Parity Error Response..... **RW**
- 0 Ignore parity errors & continue..... default
- 1 Take normal action on detected parity errors

5 VGA Palette Snoop .....RO
- 0 Treat palette accesses normally ..... default
- 1 Don't respond to palette accesses on PCI bus

4 Memory Write and Invalidate Command.....RO
- 0 Bus masters must use Mem Write ..... default
- 1 Bus masters may generate Mem Write & Inval

3 Special Cycle Monitoring.....RO
- 0 Does not monitor special cycles ..... default
- 1 Monitors special cycles

2 PCI Bus Master.....RO
- 0 Never behaves as a bus master
- 1 Can behave as a bus master ..... default

1 Memory Space.....RO
- 0 Does not respond to memory space
- 1 Responds to memory space..... default

0 I/O Space .....RO
- 0 Does not respond to I/O space ..... default
- 1 Responds to I/O space

Offset 7-6 – Status (0200h) .....RWC

15 Detected Parity Error
- 0 No parity error detected..... default
- 1 Error detected in either address or data phase. This bit is set even if error response is disabled (command register bit-6). .....write one to clear

14 Signaled Sys Err (SERR# Asserted) . always reads 0

13 Signaled Master Abort
- 0 No abort received..... default
- 1 Transaction aborted by master . write 1 to clear

12 Received Target Abort
- 0 No abort received..... default
- 1 Transaction aborted by target ... write 1 to clear

11 Signaled Target Abort.....always reads 0
- 0 Target Abort never signaled

10-9 DEVSEL# Timing
- 00 Fast
- 01 Medium.....always reads 01
- 10 Slow
- 11 Reserved

8 Data Parity Error Detected
- 0 No data parity error detected ..... default
- 1 Error detected in data phase. Set only if error response enabled via command bit-6 = 1 and the North Bridge was initiator of the operation in which the error occurred....write one to clear

7 Fast Back-to-Back Capable .....always reads 0

6 User Definable Features.....always reads 0

5 66MHz Capable .....always reads 0

4 Supports New Capability list.....always reads 0

3-0 Reserved .....always reads 0

Offset 8 - Revision ID (0nh).....RO

12-0 Chip Revision Code .....always reads 0nh

Offset 9 - Programming Interface (00h) .....RO

7-0 Interface Identifier .....always reads 00h

Offset A - Sub Class Code (00h) .....RO

7-0 Sub Class Code.....reads 00 to indicate Host Bridge

Offset B - Base Class Code (06h) .....RO

7-0 Base Class Code ..reads 06 to indicate Bridge Device

Offset 2D-2C – Subsystem Vendor ID (0000h) ..... W1 / RO

15-0 Subsystem Vendor ID..... default = 0

This register may be written once and is then read only.

Offset 2F-2E – Subsystem ID (0000h) ..... W1 / RO

15-0 Subsystem ID..... default = 0

This register may be written once and is then read only.

Offset 37-34 - Capability Pointer (CAPPTR).....RO

Contains an offset from the start of configuration space.

31-0 AGP Capability List Ptr....always reads 0000 0000h

Device 0 Function 7 Device-Specific Registers

These registers are normally programmed once at system initialization time.

V-Link Control

Offset 40 – V-Link Specification ID (40h) ..... RO

7-0 Specification Revision.....always reads 40

Offset 41 – NB V-Link Capability (39h) ..... RO

7-6 Reserved .....always reads 0

5 16-bit Bus Width Supported by NB ..... RO
- 0 Not Supported
- 1 Supported **..... default**

4 8-Bit Bus Width Supported by NB..... RO
- 0 Not Supported
- 1 Supported **..... default**

3 4x Rate Supported by NB..... RO
- 0 Not Supported
- 1 Supported **..... default**

2 2x Rate Supported by NB..... RO
- 0 Not Supported ..... default
- 1 Supported

1 Reserved .....always reads 0

0 8x Rate Supported by NB..... RO
- 0 Not Supported
- 1 Supported **..... default**

Offset 42 – NB Downlink Command (88h) ..... RW

7-4 DnCmd Max Request Depth (0=1 DnCmd) ..def = 8

3-0 DnCmd Write Buffer Size (doublewords) .....def = 8

Offset 43 – NB Uplink Max Req Depth (80h)..... RO

7-4 UpCmd Max Request Depth (0=1 UpCmd) ..def = 8
Indicates the maximum allowable number of outstanding UPCMD requests

3-0 Reserved .....always reads 0

Offset 44 – NB Uplink Buffer Size (82h) ..... RO

7-4 UpCmd P2C Write Buffer Size (max lines) ..def = 8

3-0 UpCmd P2P Write Buffer Size (max lines)...def = 2

Offset 45 –NB V-Link Bus Timer (44h).....RW

7-4 Timer for Normal Priority Requests from SB
- 0000 Immediate
- 0001 1*4 VCLKs
- 0010 2*4 VCLKs
- 0011 3*4 VCLKs
- 0100 4*4 VCLKs ..... default
- 0101 5*4 VCLKs
- 0110 6*4 VCLKs
- 0111 7*4 VCLKs
- 1000 8*4 VCLKs
- 1001 16*4 VCLKs
- 1010 32*4 VCLKs
- 1011 64*4 VCLKs
- 11xx Own the bus for as long as there is a request

3-0 Timer for High Priority Requests from SB
- 0000 Immediate
- 0001 1*2 VCLKs
- 0010 2*2 VCLKs
- 0011 3*2 VCLKs
- 0100 4*2 VCLKs ..... default
- 0101 5*2 VCLKs
- 0110 6*2 VCLKs
- 0111 7*2 VCLKs
- 1000 8*2 VCLKs
- 1001 16*2 VCLKs
- 1010 32*2 VCLKs
- 1011 64*2 VCLKs
- 11xx Own the bus for as long as there is a request

Offset 46 – NB V-Link Misc Control (00h)..... RW

7 Downstream High Priority
- 0 Disable High Priority Down Commands..... def
- 1 Enable High Priority Down Commands

6 Downlink Priority
- 0 Treat Downlink Cycles as Normal Priority def
- 1 Treat Downlink Cycles as High Priority

5-4 Combine Multiple STPGNT Cycles Into One V-Link Command
- 00 Compatible, 1 command per V-Link cmd ... def
- 01 2 commands per V-Link command
- 10 3 commands per V-Link command
- 11 4 commands per V-Link command

3-2 V-Link Master Access Ordering Rules
- 00 High priority read, pass normal read (not pass write) ..... default
- 01 Read (high/normal) pass write (HR>LR>W)
- 1x Read / write in order (ignore bit-1)

1 Read Around Write (ignored if bit-3 = 1)
- 0 Reads always pass writes ..... default
- 1 8RAW

0 Reserved .....always reads 0

Offset 47 – V-Link Control (00h)..... RW

7-6 Reserved .....always reads 0

5 C2P Read L1 Ready Return Timing
- 0 V-Link bus decodes C2P Read Ack cmd..... def
- 1 Wait till previous P2C write cycles all flushed

4 Reserved .....always reads 0

3 Down Strobe Dynamic Stop
- 0 Disable..... default
- 1 Enable

2 Auto-Disconnect
- 0 Disable..... default
- 1 Enable

1 V-Link Disconnect Cycle for STPGNT Cycle
- 0 Disable..... default
- 1 Enable

0 V-Link Disconnect Cycle for HALT Cycle
- 0 Disable..... default
- 1 Enable

Offset 48 – NB/SB V-Link Configuration (18h).....RW

7 V-Link Parity Check
- 0 Disable ..... default
- 1 Enable

6 Reserved .....always reads 0

5 16-bit Bus Width Supported
- 0 Not Supported ..... default
- 1 Supported

4 8-Bit Bus Width Supported
- 0 Not Supported
- 1 Supported **.....default**

3 4x Rate Supported
- 0 Not Supported
- 1 Supported **.....default**

2 Reserved .....always reads 0

1 V-Link Split Bus
- 0 Disable ..... default
- 1 Enable

0 8x Rate Supported
- 0 Not Supported ..... default
- 1 Supported

V-Link Mode	Transfers Per 66MHz Cycle	Bits	Bus Usage	Rx48 Bit-4	Rx48 Bit-5	Rx48 Bit-1
0	4x	8	Bidirectional	0	0	0
1	8x	4+4	Split	1	0	1
2	8x	8	Bidirectional	1	0	0
3	4x	16	Bidirectional	0	1	0
4	8x	8+8	Split	1	1	1

Offset 49 – SB V-Link Capability (19h).....WC

7-6 Reserved .....always reads 0

5 16-bit Bus Width Supported by SB.....RO
- 0 Not Supported ..... default
- 1 Supported

4 8-Bit Bus Width Supported by SB .....RO
- 0 Not Supported
- 1 Supported **.....default**

3 4x Rate Supported by SB .....RO
- 0 Not Supported
- 1 Supported **.....default**

2 2x Rate Supported by SB .....RO
- 0 Not Supported ..... default
- 1 Supported

1 Reserved .....always reads 0

0 8x Rate Supported by SB .....RO
- 0 Not Supported
- 1 Supported **.....default**

Offset 4A – SB Downlink Status (88h) ..... RO

7-4 DnCmd Max Request Depth (0=1 DnCmd) .. def = 8
3-0 DnCmd Write Buffer Size (doublewords) ..... def = 8

Offset 4B – SB Uplink Command (80h) ..... RW

7-4 UpCmd Max Request Depth (0=1 UpCmd) .. def = 8
Indicates the maximum allowable number of outstanding UPCMD requests
3-0 Reserved .....always reads 0

Offset 4C – SB Uplink Command (82h) ..... RW

7-4 UpCmd P2C Write Buffer Size (max lines) .. def = 8
3-0 UpCmd P2P Write Buffer Size (max lines)... def = 2

Offset 4D – SB V-Link Bus Timer (44h) ..... RW

7-4 Timer for Normal Priority Requests from NB
0000 Immediate
0001 1*4 VCLKs
0010 2*4 VCLKs
0011 3*4 VCLKs
0100 4*4 VCLKs ..... default
0101 5*4 VCLKs
0110 6*4 VCLKs
0111 7*4 VCLKs
1000 8*4 VCLKs
1001 16*4 VCLKs
1010 32*4 VCLKs
1011 64*4 VCLKs
11xx Own the bus for as long as there is a request

3-0 Timer for High Priority Requests from NB
0000 Immediate
0001 1*2 VCLKs
0010 2*2 VCLKs
0011 3*2 VCLKs
0100 4*2 VCLKs ..... default
0101 5*2 VCLKs
0110 6*2 VCLKs
0111 7*2 VCLKs
1000 8*2 VCLKs
1001 16*2 VCLKs
1010 32*2 VCLKs
1011 64*2 VCLKs
11xx Own the bus for as long as there is a request

Offset 4E – CCA Master Priority (00h) .....RW

7 1394 High Priority
0 Low priority ..... default
1 High priority

6 LAN / NIC High Priority
0 Low priority ..... default
1 High priority

5 Reserved .....always reads 0

4 USB High Priority
0 Low priority ..... default
1 High priority

3 Reserved .....always reads 0

2 IDE High Priority
0 Low priority ..... default
1 High priority

1 AC97-ISA High Priority
0 Low priority ..... default
1 High priority

0 PCI High Priority
0 Low priority ..... default
1 High priority

Offset 4F – SB V-Link Misc Control (00h).....RW

7 Upstream Command High Priority
0 Disable high priority up commands..... default
1 Enable high priority up commands

6-4 Reserved .....always reads 0

3 Up Strobe Dynamic Stop
0 Disable ..... default
1 Enable

2-1 Reserved .....always reads 0

0 Down Cycle Wait for Up Cycle Write Flush (Except Down Cycle Post Write)
0 Disable ..... default
1 Enable

Offset 57 – Bank 7 Ending (01h).....RO

DRAM Bank 7 Ending Address High (HA[31:24]) sent to the South Bridge. (See also Function 3 Rx47).

Offset 61 – C-ROM Shadow (00h).....RW

(same as Function 3 Rx80)

Offset 62 – D-ROM Shadow (00h).....RW

(same as Function 3 Rx81)

Offset 63 – F-ROM Shadow / Mem Hole / SMI (00h) ....RW

(same as Function 3 Rx82)

Offset 64 – E-ROM Shadow (00h).....RW

(same as Function 3 Rx83)

PCI Bus Control

These registers are normally programmed once at system initialization time.

Offset 70 - PCI Buffer Control (00h)..... RW

- **7 CPU to PCI Post-Write**
  - 0 Disable..... default
  - 1 Enable
- **6 Reserved** .....always reads 0
- **5-4 PCI Master to DRAM Prefetch**
  - 00 Always prefetch ..... default
  - x1 Never prefetch
  - 10 Prefetch only for Enhance command
- **3 Reserved** .....always reads 0
- **2 PCI Master Read Buffering**
  - 0 Disable..... default
  - 1 Enable
- **1 Delay Transaction**
  - 0 Disable..... default
  - 1 Enable
- **0 Reserved** .....always reads 0

Offset 71 - CPU to PCI Flow Control (48h).....RWC

- **7 Retry Status .....RWC**
  - 0 No retry occurred ..... default
  - 1 Retry occurred
- **6 Retry Timeout Action**
  - 0 Retry forever (record status only)
  - 1 Flush buffer or return FFFFFFFFh for reads ..... default
- **5-4 Retry Count and Retry Backoff**
  - 00 Retry 2 times, backoff CPU ..... default
  - 01 Retry 16 times
  - 10 Retry 4 times
  - 11 Retry 64 times
- **3 PCI Burst**
  - 0 Disable
  - 1 Enable ..... default
- **2 Reserved** .....always reads 0
- **1 Compatible Type#1 Configuration Cycles**
  - 0 Disable (fixed AD31)..... default
  - 1 Enable
- **0 IDSEL Control**
  - 0 AD11, AD12 ..... default
  - 1 AD30, AD31

Offset 73 - PCI Master Control (00h) .....RW

- **7 Reserved** .....always reads 0
- **6 PCI Master 1-Wait-State Write**
  - 0 Zero wait state TRDY# response..... default
  - 1 One wait state TRDY# response
- **5 PCI Master 1-Wait-State Read**
  - 0 Zero wait state TRDY# response..... default
  - 1 One wait state TRDY# response
- **4 WSC#**
  - 0 Disable ..... default
  - 1 Enable
- **3-1 Reserved** .....always reads 0
- **0 PCI Master Broken Timer Enable**
  - 0 Disable ..... default
  - 1 Enable. Force into arbitration when there is no FRAME# 16 PCICLK's after the grant.

Offset 75 - PCI Arbitration 1 (00h) ..... RW

7 Arbitration Mode
- 0 REQ-based (arbitrate at end of REQ#) .. default
- 1 Frame-based (arbitrate at FRAME# assertion)

6-4 CPU Latency

3 Reserved .....always reads 0

2-0 PCI Master Bus Time-Out

(force into arbitration after a period of time)
- 000 Disable..... default
- 001 1x16 PCICLKs
- 010 2x16 PCICLKs
- 011 3x16 PCICLKs
- 100 4x16 PCICLKs
- ... ...
- 111 7x16 PCICLKs

Offset 76 - PCI Arbitration 2 (00h) .....RW

7 I/O Port 22 Access
- 0 CPU access to I/O address 22h is passed on to the PCI bus..... default
- 1 CPU access to I/O address 22h is processed internally

6 Reserved .....always reads 0

5-4 Master Priority Rotation Control
- 00 Disable ..... default
- 01 Grant to CPU after every PCI master grant
- 10 Grant to CPU after every 2 PCI master grants
- 11 Grant to CPU after every 3 PCI master grants

Setting 01: the CPU will always be granted access after the current bus master completes, no matter how many PCI masters are requesting.

Setting 10: if other PCI masters are requesting during the current PCI master grant, the highest priority master will get the bus after the current master completes, but the CPU will be guaranteed to get the bus after that master completes.

Setting 11: if other PCI masters are requesting, the highest priority will get the bus next, then the next highest priority will get the bus, then the CPU will get the bus.

In other words, with the above settings, even if multiple PCI masters are continuously requesting the bus, the CPU is guaranteed to get access after every master grant (01), after every other master grant (10) or after every third master grant (11).

3-2 Select REQn# to REQ4# mapping
- 00 REQ4#..... default
- 01 REQ0#
- 10 REQ1#
- 11 REQ2#

1 Reserved .....always reads 0

0 REQ4# is High Priority Master
- 0 Disable ..... default
- 1 Enable

Graphics Aperture Control

Offset 85-84 – Graphics Aperture Size (0000h)..... RW

15-12 Reserved .....always reads 0

11-0 Graphics Aperture Size [31:20].....default = 00h

111100111111	4MB
111100111110	8MB
111100111100	16MB
111100111000	32MB
111100110000	64MB
111100100000	128MB
111100000000	256MB
111000000000	512MB
110000000000	1GB
100000000000	2GB <= Max supported
000000000000	4GB <= Do not program

In AGP 2.0 mode, only 4MB - 256MB are supported

Offset 88 – GART Base (00h)..... RW

7-2 Reserved .....always reads 0

1 GART Window Access

0 Disable..... default

1 Enable

0 Reserved .....always reads 0

V-Link CKG Control

Offset B0 – V-Link CKG Control 1 (00h).....RW

7 Rise Time Duty Cyclc Control - V-Link #1 R-Port

6 Rise Time Duty Cyclc Control - V-Link #0 R-Port

5 Fall Time Duty Cyclc Control - V-Link #1 R-Port

4 Fall Time Duty Cyclc Control - V-Link #0 R-Port

3 Rise Time Duty Cyclc Control - V-Link #1 S-Port

2 Rise Time Duty Cyclc Control - V-Link #0 S-Port

1 Fall Time Duty Cyclc Control - V-Link #1 S-Port

0 Fall Time Duty Cyclc Control - V-Link #0 S-Port

Offset B1 – V-Link CKG Control 2 (00h).....RW

7-4 Reserved .....always reads 0

3 Rise Time Duty Cyclc Control - V-Link #1 D-Port

2 Rise Time Duty Cyclc Control - V-Link #0 D-Port

1 Fall Time Duty Cyclc Control - V-Link #1 D-Port

0 Fall Time Duty Cyclc Control - V-Link #0 D-Port

V-Link Compensation / Drive Control

Offset B4 – V-Link NB Compensation Control (00h).... RW

- **7-5 V-Link Autocomp Output Value – High Drive** .RO
- **4 Reserved** .....always reads 0
- **3-1 V-Link Autocomp Output Value – Low Drive** ..RO
- **0 Compensation Select**
  - 0 Auto Comp (use values in bits 7-5, 3-1) default
  - 1 Manual Comp (use values in RxB5, B6)

Offset B5 – V-Link NB Strobe Drive Control (00h) ..... RW

- **7-5 V-Link Strobe Pullup Manual Setting (High)**
- **4 Reserved** .....always reads 0
- **3-1 V-Link Strobe Pulldown Manual Setting (Low)**
- **0 Reserved** .....always reads 0

Offset B6 – V-Link NB Data Drive Control (00h)..... RW

- **7-5 V-Link Data Pullup Manual Setting (High)**
- **4 Reserved** .....always reads 0
- **3-1 V-Link Data Pulldown Manual Setting (Low)**
- **0 Reserved** .....always reads 0

Offset B7 – V-Link NB Receive Strobe Delay (00h) ..... RW

- 7-2 **Reserved** .....always reads 0
- **1-0 NB V-Link Strobe Delay for Receiving**
  - 00 150 psec early..... default
  - 01 No delay
  - 10 150 psec late
  - 11 300 psec late

VT8235 South Bridge:

Offset B8 – V-Link SB Compensation Control (00h) .....RW

- **7-5 V-Link Autocomp Output Value – High Drive** . RO
- **4-1 Reserved** .....always reads 0
- **0 Compensation Select**
  - 0 Auto Comp (use values in bits 7-5)..... default
  - 1 Manual Comp (use values in RxB9)

Offset B9 – V-Link SB Strobe Drive Control (00h).....RW

- **7-5 V-Link Strobe Pullup Manual Setting (High)**
- **4 Reserved** .....always reads 0
- **3-1 V-Link Strobe Pulldown Manual Setting (Low)**
- **0 Reserved** .....always reads 0

VT8233 South Bridge (VT8233, VT8233A):

Offset B8 – V-Link SB Compensation Control (00h) .....RW

- **7-6 V-Link Autocomp Output Value** .....always reads 0
- **5 Pullup Compensation Selection**
  - 0 Auto Comp (use values in bits 7-6)..... default
  - 1 Manual Comp (use values in bits 3-2)
- **4 Pulldown Compensation Selection**
  - 0 Auto Comp (use values in bits 7-6)..... default
  - 1 Manual Comp (use values in bits 1-0)
- **3-2 Pullup Compensation Manual Setting**..... def = 0
- **1-0 Pulldown Compensation Manual Setting**..... def = 0

Offset B9 – V-Link SB Drive Control (00h) .....RW

- **7-6 SB V-Link Strobe Pullup Manual Setting**
- **5-4 SB V-Link Strobe Pulldown Manual Setting**
- **3-1 Reserved** .....always reads 0
- **0 SB V-Link Slew Rate Control**
  - 0 Disable ..... default
  - 1 Enable

DRAM Above 4G Support

Offset E4 – Low Top Address Low (00h) .....RW

(same as Function 3 Rx84)

Offset E5 – Low Top Address High (FFh).....RW

(same as Function 3 Rx85)

Offset E6 – SMM / APIC Decoding (01h).....RW

(same as Function 3 Rx86)

Device 1 Registers – PCI-to-PCI Bridge

Device 1 Header Registers

All registers are located in PCI configuration space. They should be programmed using PCI configuration mechanism 1 through CF8 / CFC with bus number of 0 and function number equal to 0 and device number equal to one.

Device 1 Offset 1-0 - Vendor ID (1106h) ..... RO

15-0 ID Code (reads 1106h to identify VIA Technologies)

Device 1 Offset 3-2 - Device ID (B198h) ..... RO

15-0 ID Code (reads B198h to identify the North Bridge PCI-to-PCI Bridge device)

Device 1 Offset 5-4 – Command (0007h) ..... RW

15-10 Reserved ..... always reads 0

9 Fast Back-to-Back Cycle Enable ..... RO
- 0 Fast back-to-back transactions only allowed to the same agent ..... default
- 1 Fast back-to-back transactions allowed to different agents

8 SERR# Enable ..... RO
- 0 SERR# driver disabled ..... default
- 1 SERR# driver enabled

7 Address / Data Stepping ..... RO
- 0 Device never does stepping ..... default
- 1 Device always does stepping

6 Parity Error Response ..... **RW**
- 0 Ignore parity errors & continue ..... default
- 1 Take normal action on detected parity errors

5 Reserved ..... always reads 0

4 Memory Write and Invalidate Command ..... RO
- 0 Bus masters must use Mem Write ..... default
- 1 Bus masters may generate Mem Write & Inval

3 Special Cycle Monitoring ..... RO
- 0 Does not monitor special cycles ..... default
- 1 Monitors special cycles

2 Bus Master ..... **RW**
- 0 Never behaves as a bus master
- 1 Enable to operate as a bus master on the primary interface on behalf of a master on the secondary interface ..... default

1 Memory Space ..... **RW**
- 0 Does not respond to memory space
- 1 Enable memory space access ..... default

0 I/O Space ..... **RW**
- 0 Does not respond to I/O space
- 1 Enable I/O space access ..... default

Device 1 Offset 7-6 - Status (Primary Bus) (0230h) ..... RWC

15 Detected Parity Error ..... always reads 0

14 Signaled System Error (SERR#) ..... always reads 0

13 Signaled Master Abort
- 0 No abort received ..... default
- 1 Transaction aborted by the master with Master-Abort (except Special Cycles) ..... write 1 to clear

12 Received Target Abort
- 0 No abort received ..... default
- 1 Transaction aborted by the target with Target-Abort ..... write 1 to clear

11 Signaled Target Abort ..... always reads 0

10-9 DEVSEL# Timing
- 00 Fast
- 01 Medium ..... always reads 01
- 10 Slow
- 11 Reserved

8 Data Parity Error Detected ..... always reads 0

7 Fast Back-to-Back Capable ..... always reads 0

6 User Definable Features ..... always reads 0

5 66MHz Capable ..... always reads 1

4 Supports New Capability list ..... always reads 1

3-0 Reserved ..... always reads 0

Device 1 Offset 8 - Revision ID (00h) ..... RO

7-0 Chip Revision Code (00=First Silicon)

Device 1 Offset 9 - Programming Interface (00h) ..... RO

This register is defined in different ways for each Base/Sub-Class Code value and is undefined for this type of device.

7-0 Interface Identifier ..... always reads 00

Device 1 Offset A - Sub Class Code (04h) ..... RO

7-0 Sub Class Code. reads 04 to indicate PCI-PCI Bridge

Device 1 Offset B - Base Class Code (06h) ..... RO

7-0 Base Class Code ..reads 06 to indicate Bridge Device

Device 1 Offset E - Header Type (01h) ..... RO

7-0 Header Type Code ..... reads 01: PCI-PCI Bridge

Device 1 Offset 13-10 – Graphics Aperture Base (0000 0008h)..... RW

This register is interpreted per the following definition if RxFD[1]=1 (AGP 2.0 registers enabled).

31-22 Programmable Base Address Bits.....def=0
These bits behave as if hardwired to 0 if the corresponding AGP 3.0 Graphics Aperture Size register bit (Device 0 Function 0 Offset 94h) is 0.

31	30	29	28	-	-	27	26	25	24	23	22	(Base)
11	10	9	8	7	6	5	4	3	2	1	0	(Size)
RW	RW	RW	RW	0	0	RW	RW	RW	RW	RW	RW	4M
RW	RW	RW	RW	0	0	RW	RW	RW	RW	RW	0	8M
RW	RW	RW	RW	0	0	RW	RW	RW	RW	0	0	16M
RW	RW	RW	RW	0	0	RW	RW	RW	0	0	0	32M
RW	RW	RW	RW	0	0	RW	RW	0	0	0	0	64M
RW	RW	RW	RW	0	0	RW	0	0	0	0	0	128M
RW	RW	RW	RW	0	0	0	0	0	0	0	0	256M
RW	RW	RW	0	0	0	0	0	0	0	0	0	512M
RW	RW	0	0	0	0	0	0	0	0	0	0	1G
RW	0	0	0	0	0	0	0	0	0	0	0	2G-max
0	0	0	0	0	0	0	0	0	0	0	0	4G

21-4 Reserved.....always reads 0
3 Prefetchable..... **always reads 1**
2-1 Type.....always reads 0
0 Memory Space.....always reads 0

Device 1 Offset 18 - Primary Bus Number (00h)..... RW

7-0 Primary Bus Number.....default = 0
This register is read write, but internally the chip always uses bus 0 as the primary.

Device 1 Offset 19 - Secondary Bus Number (00h)..... RW

7-0 Secondary Bus Number.....default = 0
Note: AGP must use these bits to convert Type 1 to Type 0.

Device 1 Offset 1A - Subordinate Bus Number (00h).... RW

7-0 Primary Bus Number.....default = 0
Note: AGP must use these bits to decide if Type 1 to Type 1 command passing is allowed.

Device 1 Offset 1C - I/O Base (F0h)..... RW

7-4 I/O Base AD[15:12].....default = 1111b
3-0 I/O Addressing Capability.....default = 0

Device 1 Offset 1D - I/O Limit (00h)..... RW

7-4 I/O Limit AD[15:12].....default = 0
3-0 I/O Addressing Capability.....default = 0

Device 1 Offset 1F-1E - Secondary Status .....RO

15-0 Secondary Status
Rx44[4] = 0: these bits read back 0000h
Rx44[4] = 1: these bits read back same as Rx7-6

Device 1 Offset 21-20 - Memory Base (FFF0h).....RW

15-4 Memory Base AD[31:20]..... default = FFFh
3-0 Reserved.....always reads 0

Device 1 Offset 23-22 - Memory Limit (Inclusive) (0000h) RW

15-4 Memory Limit AD[31:20]..... default = 0
3-0 Reserved.....always reads 0

Device 1 Offset 25-24 - Prefetchable Mem Base (FFF0h) RW

15-4 Prefetchable Memory Base AD[31:20]default = FFFh
3-0 Reserved.....always reads 0

Device 1 Offset 27-26 - Prefetchable Memory Limit (0000h) .....RW

15-4 Prefetchable Memory Limit AD[31:20] . default = 0
3-0 Reserved.....always reads 0

Device 1 Offset 34 - Capability Pointer (70h).....RO

Contains an offset from the start of configuration space.

7-0 AGP Capability List Pointer.....always reads 70h

Device 1 Device-Specific Registers

AGP Bus Control

Device 1 Offset 40 - CPU-to-AGP Flow Control 1 (00h) RW

7 CPU-AGP Post Write
- 0 Disable ..... default
- 1 Enable

6 CPU-AGP One Wait State Burst Write
- 0 Disable ..... default
- 1 Enable

5-4 Read Prefetch Control
- 00 Always prefetch ..... default
- x1 Never prefetch
- 10 Prefetch only for Enhance command

3 Reserved ..... always reads 0

2 MDA Present on AGP
- 0 Forward MDA accesses to AGP ..... default
- 1 Forward MDA accesses to PCI

Note: Forward despite IO / Memory Base / Limit

Note: MDA (Monochrome Display Adapter) addresses are memory addresses B0000h-B7FFFh and I/O addresses 3B4-3B5h, 3B8-3BAh, and 3BFh (10-bit decode). 3BC-3BE are reserved for printers.

Note: If Rx3E bit-3 is 0, this bit is a don't care (MDA accesses are forwarded to the PCI bus).

1 AGP Master Read Caching
- 0 Disable ..... default
- 1 Enable

0 AGP Delay Transaction
- 0 Disable ..... default
- 1 Enable

Table 12. VGA/MDA Memory/IO Redirection

3E[3] VGA Pres.	40[2] MDA Pres.	VGA is on	MDA is on	Axxxx, B8xxx Access	B0000 -B7FFF Access	3Cx, 3Dx I/O	3Bx I/O
0	-	PCI	PCI	PCI	PCI	PCI	PCI
1	0	AGP	AGP	AGP	AGP	AGP	AGP
1	1	AGP	PCI	AGP	PCI	AGP	PCI

Device 1 Offset 41 - CPU-to-AGP Flow Control 2 (08h) RW

7 Retry Status
- 0 No retry occurred ..... default
- 1 Retry Occurred ..... **write 1 to clear**

6 Retry Timeout Action
- 0 No action taken except to record status .....def
- 1 Flush buffer for write or return all 1s for read

5-4 Retry Count
- 00 Retry 2, backoff CPU ..... default
- 01 Retry 4, backoff CPU
- 10 Retry 16, backoff CPU
- 11 Retry 64, backoff CPU

3 CPU-to-AGP Bursting Timeout
- 0 Disable
- 1 Enable **.....default**

2 Reserved ..... always reads 0

1 CPU-to-PCI/AGP Cycles Invalidate PCI/AGP Buffered Read Data
- 0 Disable ..... default
- 1 Enable

0 Reserved ..... always reads 0

Device 1 Offset 42 - AGP Master Control (00h) .....RW

7 Reserved (Must Be Programmed to 1) ..... def = 0

When this bit is set, the North Bridge will automatically resolve the problem of AGP master cycles being blocked by PCI Master Cycles.

6 AGP Master One Wait State Write
- 0 Disable ..... default
- 1 Enable

5 AGP Master One Wait State Read
- 0 Disable ..... default
- 1 Enable

4 Break Consecutive PCI Master Accesses
- 0 Disable ..... default
- 1 Enable

3 Reserved ..... always reads 0

2 Claim I/O R/W and Memory Read Cycles
- 0 Disable ..... default
- 1 Enable

1 Claim Local APIC FEEx xxxx Cycles
- 0 Disable ..... default
- 1 Enable

0 Snoop Write Enable 2T Rate, Support Host Side Snoop Cycles at 2T Rate
- 0 Disable ..... default
- 1 Enable

Device 1 Offset 43 - AGP Master Latency Timer (22h) RW

7-4 Host to AGP Time slot
- 0 Disable (no timer)
- 1 16 GCLKs
- 2 32 GCLKs ..... default
- … …
- F 128 GCLKs

3-0 AGP Master Time Slot
- 0 Disable (no timer)
- 1 16 GCLKs
- 2 32 GCLKs ..... default
- … …
- F 128 GCLKs

Device 1 Offset 45 – Fast Write Control (72h).....RW

7 Force Fast Write Cycle to be QW Aligned (if Rx45[6] = 0)
- 0 Disable ..... default
- 1 Enable

6 Merge Multiple CPU Transactions Into One Fast Write Burst Transaction
- 0 Disable
- 1 Enable **.....default**

5 Merge Multiple CPU Write Cycles To Memory Offset 23-20 Into Fast Write Burst Cycles (if Rx45[6] = 0)
- 0 Disable
- 1 Enable **.....default**

4 Merge Multiple CPU Write Cycles To Prefetchable Memory Offset 27-24 Into Fast Write Burst Cycles (if Rx45[6] = 0)
- 0 Disable
- 1 Enable **.....default**

3 Reserved .....always reads 0

2 Fast Write Burst 4T Max (No Slave Flow Control)
- 0 Disable ..... default
- 1 Enable

1 Fast Write Fast Back to Back
- 0 Disable
- 1 Enable **.....default**

0 Fast Write Initial Block 1 Wait State
- 0 Disable ..... default
- 1 Enable

Rx45 Bits 7-4	CPU Write Address in Mem1	CPU Write Address in Mem2	Fast Write Cycle Alignment
x1xx	-	-	QW aligned, burstable
0000	-	-	DW aligned, nonburstable
x010	0	0	n/a
0010	0	1	DW aligned, non-burstable
x010	1	-	QW aligned, burstable
x001	0	0	n/a
x001	-	1	QW aligned, burstable
0001	1	0	DW aligned, non-burstable
x011	0	0	n/a
x011	1	-	QW aligned, burstable
x011	0	1	QW aligned, burstable
1000	-	-	QW aligned, non-burstable
1010	0	1	QW aligned, non-burstable
1001	1	0	QW aligned, non-burstable

Device 1 Offset 47-46 – PCI-to-PCI Bridge Device ID ...RW

15-0 PCI-to-PCI Bridge Device ID ..... default = 0000

Power Management

Device 1 Offset 70 – Capability ID (01h)..... RO

7-0 Capability ID .....always reads 01h

Device 1 Offset 71 – Next Pointer (00h) ..... RO

7-0 Next Pointer: Null .....always reads 00h

Device 1 Offset 72 – Power Mgmt Capabilities 1 (02h) .. RO

7-0 Power Mgmt Capabilities.....always reads 02h

Device 1 Offset 73 – Power Mgmt Capabilities 2 (00h) .. RO

7-0 Power Mgmt Capabilities.....always reads 00h

Device 1 Offset 74 – Power Mgmt Ctrl/Status (00h)..... RW

7-2 Reserved .....always reads 0

1-0 Power State

00 D0 ..... default
01 -reserved-
10 -reserved-
11 D3 Hot

Device 1 Offset 75 – Power Mgmt Status (00h).....RO

7-0 Power Mgmt Status ..... default = 00

Device 1 Offset 76 – P2P Br. Support Extensions (00h)..RO

7-0 P2P Bridge Support Extensions..... default = 00

Device 1 Offset 77 – Power Management Data (00h) .....RO

7-0 Power Management Data..... default = 00

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Table 13. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes
T_C	Case operating temperature	0	85	^oC	1
T_S	Storage temperature	–55	125	^oC	1
V_{IN}	Input voltage	–0.5	V_{RAIL} + 10%	Volts	1, 2
V_{OUT}	Output voltage	–0.5	V_{RAIL} + 10%	Volts	1, 2

Note 1. Stress above the conditions listed may cause permanent damage to the device. Functional operation of this device should be restricted to the conditions described under operating conditions.

Note 2. V_{RAIL} is defined as the V_{CC} level of the respective rail. The CPU interface voltage is CPU dependent (typically 1.65V). AGP is 1.5V (4x transfer mode) or 0.8V (8x transfer mode). VL is 1.5V. Memory is 2.5V. Graphics / Display is 3.3V.

DC Characteristics

T_C = 0-85^{o}C, V_{RAIL} = V_{CC} ±5%, V_{CORE} = 1.5V ±5%, GND=0V

Table 14. DC Characteristics

Symbol	Parameter	Min	Max	Unit	Condition
V_{IL}	Input Low Voltage	–0.50	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage	–	0.55	V	I_{OL} = 4.0mA
V_{OH}	Output High Voltage	2.4	–	V	I_{OH} = –1.0mA
I_{IL}	Input Leakage Current	–	±10	uA	0 < V_{IN} < V_{CC}
I_{OZ}	Tristate Leakage Current	–	±20	uA	0.55 < V_{OUT} < V_{CC}

Package Weight Specifications

Table 15. Package Weight Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Condition
W_P	Package Weight	7.99	8.00	8.02	grams	Standard earth gravity

Power Characteristics

T_C = 0-85°C, V_{RAIL} = V_{CC} ±5%, V_{CORE} = 1.5V ±5%, GND=0V

Table 16. Power Characteristics – Internal and Interface Digital Logic

Symbol	Parameter	Typ	Max	Unit	Condition
I_{TT}	Power Supply Current – VTT			mA	Full-On Operation
I_{TTPOS}	Power Supply Current – VTT			mA	POS
I_{TTSTR}	Power Supply Current – VTT			mA	STR
I_{TTSOF}	Power Supply Current – VTT			mA	Soft-Off
I_{CCG}	Power Supply Current – VCC15AGP			mA	Full-On Operation
I_{CCGPOS}	Power Supply Current – VCC15AGP			mA	POS
I_{CCGSTR}	Power Supply Current – VCC15AGP			mA	STR
I_{CCGSOF}	Power Supply Current – VCC15AGP			mA	Soft-Off
I_{CCV}	Power Supply Current – VCC15VL			mA	Full-On Operation
I_{CCVPOS}	Power Supply Current – VCC15VL			mA	POS
I_{CCVSTR}	Power Supply Current – VCC15VL			mA	STR
I_{CCVSOF}	Power Supply Current – VCC15VL			mA	Soft-Off
I_{CCM}	Power Supply Current – VCC25MEM			mA	Full-On Operation
I_{CCMPOS}	Power Supply Current – VCC25MEM			mA	POS
I_{CCMSTR}	Power Supply Current – VCC25MEM			mA	STR
I_{CCMSOF}	Power Supply Current – VCC25MEM			mA	Soft-Off
I_{CCF}	Power Supply Current – VCC33GFX			mA	Full-On Operation
$I_{CCDDPOS}$	Power Supply Current – VCC33GFX			mA	POS
$I_{CCDDSTR}$	Power Supply Current – VCC33GFX			mA	STR
$I_{CCDDSOF}$	Power Supply Current – VCC33GFX			mA	Soft-Off
I_{CC}	Power Supply Current – VCC15			mA	Full-On Operation
I_{CCPOS}	Power Supply Current – VCC15			mA	POS
I_{CCSTR}	Power Supply Current – VCC15			mA	STR
I_{CCSOF}	Power Supply Current – VCC15			mA	Soft-Off
I_{SUS}	Power Supply Current – VSUS15			mA	Full-On Operation
I_{SUSPOS}	Power Supply Current – VSUS15			mA	POS
I_{SUSSTR}	Power Supply Current – VSUS15			mA	STR
I_{SUSSOF}	Power Supply Current – VSUS15			mA	Soft-Off
I_{CCDAC}	Power Supply Current – VCC33DAC			mA	Max operating frequency
P_D	Power Dissipation			W	Max operating frequency

Table 17. Power Characteristics – Analog and Reference Voltages

Symbol	Parameter	Typ	Max	Unit	Condition
I_{CCGTL}	Power Supply Current – GTLVREF			mA	Max operating frequency
$I_{CCHAREF}$	Power Supply Current – HAVREF			mA	Max operating frequency
$I_{CCHDREF}$	Power Supply Current – HDVREF			mA	Max operating frequency
$I_{CCHCREF}$	Power Supply Current – HCOMPVREF			mA	Max operating frequency
I_{CCMREF}	Power Supply Current – MEMVREF			mA	Max operating frequency
I_{CCGREF}	Power Supply Current – AGPVREF			mA	Max operating frequency
$I_{CCVLREF}$	Power Supply Current – VLVREF			mA	Max operating frequency
I_{CCHCK1}	Power Supply Current – VCCA33HCK1			mA	Max operating frequency
I_{CCHCK2}	Power Supply Current – VCCA33HCK2			mA	Max operating frequency
I_{CCMCK}	Power Supply Current – VCCA33MCK			mA	Max operating frequency
I_{CCGCK}	Power Supply Current – VCCA33GCK			mA	Max operating frequency
I_{CCDAC}	Power Supply Current – VCCA33DAC			mA	Max operating frequency
I_{CCPLL1}	Power Supply Current – VCCA15PLL1			mA	Max operating frequency
I_{CCPLL2}	Power Supply Current – VCCA15PLL2			mA	Max operating frequency
I_{CCPLL3}	Power Supply Current – VCCA15PLL3			mA	Max operating frequency

AC Timing Specifications

AC timing specifications provided are based on external zero-pf capacitance load. Min / max cases are based on the following table:

Table 18. AC Timing Min / Max Conditions

Parameter	Min	Max	Unit
3.3V Power (Graphics CRT / Digital Display ports)	3.135	3.465	Volts
2.5V Power (Memory interface)	2.375	2.625	Volts
1.5V Power (VCC15AGP for 4x transfer mode, VL-bus, and internal logic)	1.425	1.575	Volts
0.8V Power (VCC15AGP for 8x transfer mode)	0.760	0.840	Volts
Case Temperature	0	85	^{o}C

Drive strength for selected output pins is programmable. See Rx6D for details.

Table 19. AC Timing – CPU Interface

Signal	Reference Signal	Setup	Hold	Min Delay	Max Delay	Unit
HD Bus	HDSTBP/N[3:0]#	0.55	0.55	0.85	0.80	ns
HA Bus	HADSTB[1:0]#	0.50	0.55	1.6	1.6	ns
HREQ[4:0]#	HADSTB0#	0.50	0.55	1.6	1.6	ns
ADS#	HCLK+	2.4	–0.20			ns
DBSY#	HCLK+	2.4	–0.20			ns
DRDY#	HCLK+	2.4	–0.20			ns
HIT#	HCLK+	2.4	–0.20			ns
HITM#	HCLK+	2.4	–0.20			ns
HLOCK#	HCLK+	2.4	–0.20			ns

Table 20. AC Timing – Memory Interface

Signal	Reference Signal	Setup	Hold	Min Delay	Max Delay	Unit
MD Bus	DQS[7:0]#	-1.2	2	1.10	1.05	ns
MA Bus	–	–	–			ns
SRAS# Bus	–	–	–			ns
SCAS# Bus	–	–	–			ns
SWE# Bus	–	–	–			ns
CS# Bus	–	–	–			ns
DQM Bus	–	–	–			ns

Table 21. AC Timing – V-Link Interface

Signal	Reference Signal	Setup	Hold	Min Delay	Max Delay	Unit
VD Bus	Strobes	0.45	0.45	1.1	1.1	ns

Table 22. AC Timing – AGP Interface

Signal	Reference Signal	Setup	Hold	Min Delay	Max Delay	Unit
GD Bus	GADSTB[1:0]#			0.90	0.85	ns

MECHANICAL SPECIFICATIONS

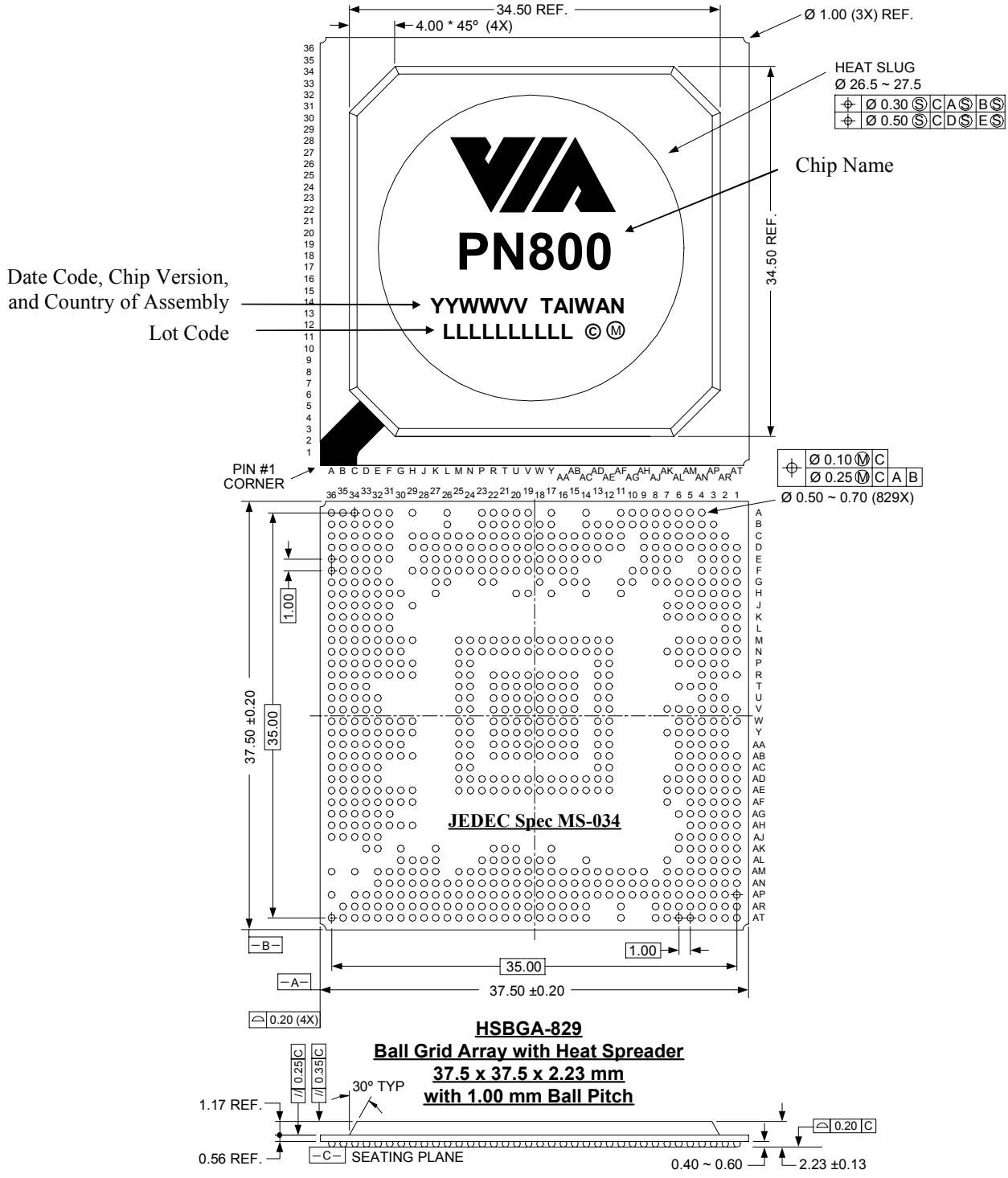


Figure 6. Mechanical Specifications – HSBGA-829 Ball Grid Array Package with Heat Spreader