ProSavage PN133T Chipset

VT8606 “TwisterT”

Single-Chip SMA North Bridge with 133 / 100 / 66 MHz Front Side Bus for VIA™ C3™ and Intel™ Celeron™, Pentium™ III and III-M (Tualatin) CPUs with Integrated ProSavage4 AGP 4x Graphics plus Advanced Memory Controller supporting PC133 / PC100 SDRAM for Mobile PC Systems

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REVISION HISTORY

Document Release	Date	Revision	Initials
1.0	12/5/01	Initial public release (same as internal revision 0.52 with cover logo updated and register #s and panel tables fixed in Function Description section)	DH
1.01	1/4/02	Changed package to HSBGA; Removed DVI/TMDS interface	DH
1.02	2/12/02	Fixed document revision #; Updated trademarks list Added note to Device 1 Rx40[6]	DH
1.03	1/6/03	Removed confidential watermark from cover page Updated VIA logo on cover page and in page headers Fixed minor copyright page formatting issues; corrected VIA USA street address Updated wording in Overview for "LCD and Monitor Support" section Fixed typo in table 13 "DSTN16" heading	DH

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PROSAVAGE PN133T CHIPSET

VT8606 "TWISTERT" NORTH BRIDGE

Single-Chip SMA North Bridge with 133 / 100 / 66 MHz FSB
for VIA C3 and Intel Celeron and Pentium III / III-M (Tualatin) CPUs
with Integrated ProSavage4 AGP 4x Graphics Core
plus Advanced Memory Controller
supporting PC133 / PC100 SDRAM
for Mobile PC Systems

PRODUCT FEATURES

- **Defines Integrated Solutions for Value PC Mobile Designs**
  - High performance SMA North Bridge: Integrated VIA Pro133A and S3 Graphics' ProSavage4™ in a single chip
  - 64-bit Advanced Memory controller supporting PC133 / PC100 SDRAM
  - Combines with VIA VT82C686A/B PCI-ISA South Bridge for state-of-the-art power management
  - Combines with VIA VT8231 PCI-LPC South Bridge for integrated LAN support
- **High Performance CPU Interface**
  - Support for Socket-370 VIA C3 and Intel™ Celeron™ and Pentium™ III / III-M (Tualatin) processors
  - 133 / 100 / 66 MHz CPU Front Side Bus (FSB)
  - Built-in Phase Lock Loop circuitry for optimal skew control within and between clocking regions
  - Five outstanding transactions (four In-Order Queue (IOQ) plus one output latch)
  - Dynamic deferred transaction support
- **Advanced High-Performance DRAM Controller**
  - DRAM interface runs synchronous (133/133 or 100/100) mode or pseudo-synchronous (133/100, 100/133, 100/66) mode with FSB
  - Concurrent CPU, AGP, and PCI access
  - Supports standard PC133 and PC100 SDRAM memory types
  - Support 3 DIMMs or 6 banks for up to 1.5 GB of DRAM (256Mb DRAM technology)
  - 64-bit data width
  - Supports maximum 8-bank interleave (8 pages open simultaneously); banks are allocated based on LRU
  - SDRAM X-1-1-1-1-1-1-1 back-to-back accesses
- **Integrated ProSavage4 2D/3D/Video Accelerator**
  - Optimized Shared Memory Architecture (SMA)
  - Full internal AGP 4x performance
  - Significant internal architectural upgrades from original S3 Savage4 standalone product
  - 8 / 16 / 32 MB frame buffer using system memory
  - Floating point triangle setup engine
  - Single cycle 128-bit 3D architecture
  - 8M triangles/second setup engine
  - 140M pixels/second trilinear fill rate
  - Microsoft Direct X texture compression
  - Next generation, 128-bit 2D graphics engine
  - High quality DVD video playback
  - Flat panel monitor support
  - 2D/3D resolutions up to 1920x1440

- **3D Rendering Features**
  - Single-pass multiple textures
  - Anisotropic filtering
  - 8-bit stencil buffer
  - 32-bit true color rendering
  - Specular lighting and diffuse shading
  - Alpha blending modes
  - Massive 2K x 2K textures
  - MPEG-2 video textures
  - Vertex and table fog
  - 16 or 24-bit Z-buffering
  - Reflection mapping, texture morphing, shadows, procedural textures and atmospheric effects
- **2D Hardware Acceleration Features**
  - ROP3 Ternary Raster Operation BitBLTs
  - 8, 16, and 32 bpp mode acceleration
- **Motion Video Architecture**
  - High quality up/down scaler
  - Planar to packed format conversion
  - Motion compensation for full speed DVD playback
  - Hardware subpicture blending and highlights
  - Multiple video windows for video conferencing
  - Contrast, hue, saturation, brightness and gamma controls
  - ZV-Port Interface for display of video from an external source
  - Digital output port for NTSC/PAL TV encoders
- **Extensive LCD Support**
  - 36-bit DSTN/TFT flat panel interface with 256 gray shade support
  - Integrated 2-channel 110 MHz LVDS interface
  - Support for all resolutions up to 1600x1200
  - Panel power sequencing
  - Hardware Suspend/Standby control
- **Concurrent PCI Bus Controller**
  - PCI 2.2 compliant, 32-bit 3.3V PCI interface with 5V tolerant inputs
  - Supports up to 5 PCI masters
  - PCI to system memory data streaming support
  - Delay transaction from PCI master accessing DRAM
  - Symmetric arbitration between Host/PCI bus for optimized system performance
- **Advanced System Power Management Support**
  - Independent clock stop controls for CPU / SDRAM, AGP, and PCI bus
  - PCI and AGP bus clock run and clock generator control
  - VTT suspend power plane preserves memory data
  - Suspend-to-DRAM and self-refresh power down
  - Low-leakage I/O pads
  - ACPI 1.0B and PCI Bus Power Management 1.1 compliant
- **Full Software Support**
  - Drivers for major operating systems and APIs: [Windows® 9x / ME, Windows NT 4.0, Windows 2000, Windows XP, Direct3D™, DirectDraw™ and DirectShow™, OpenGL™ ICD for Windows 9x, NT, and 2000, and DXVA for Windows 2000 and Windows XP]
  - North Bridge/Chipset and Video BIOS support

- **Additional Features**
  - Simultaneous display of CRT with LCD Panel or TV
  - 250 MHz RAMDAC with Gamma Correction
  - I^2C Serial Bus and DDC Monitor Communications
  - 2.5V Core and Mixed 3.3V/5V Tolerant and GTL+ I/O
  - 35 x 35mm HSBGA package (Ball Grid Array with Heat Spreader) with 552 balls

OVERVIEW

ProSavage PN133T is a high performance, cost-effective and energy efficient SMA chip set for the implementation of mobile personal computer systems with 133 MHz, 100 MHz and 66 MHz CPU host bus ("Front Side Bus") frequencies and based on 64-bit "P6 Bus" Socket-370, FCPGA478, and uFCBGA479, VIA C3 and Intel Celeron and Pentium III / III-M (Tualatin) super-scalar processors. The PN133T chipset includes the **VT8606 "TwisterT"** North Bridge and the **VT8231** South Bridge.

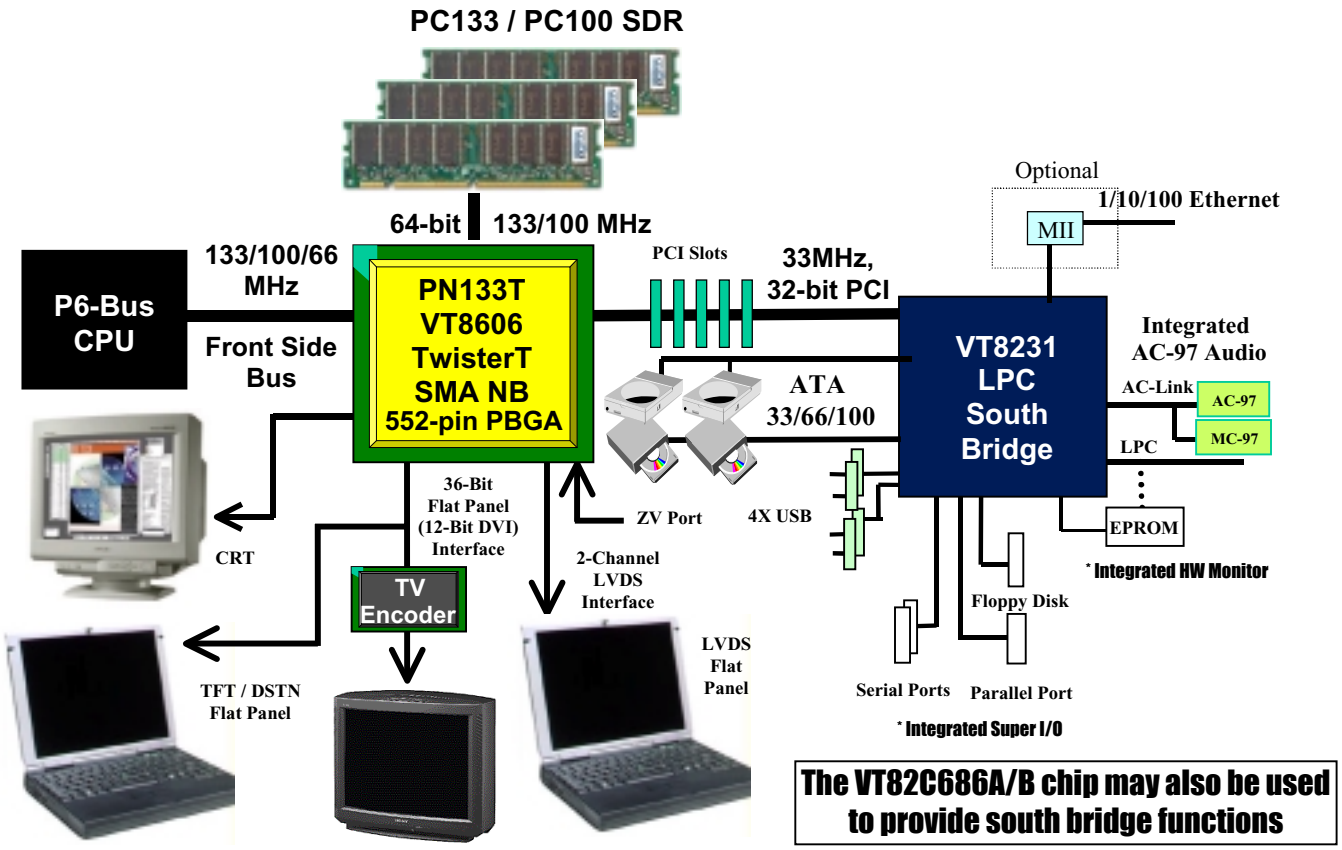


Figure 1. ProSavage PN133T Chipset System Block Diagram

TwisterT integrates VIA's VT82C694T system controller, S3 Graphics' 128-bit ProSavage4 2D/3D graphics accelerator and S3 Graphics' flat panel interfaces into a single 552 BGA package. The TwisterT SMA system controller provides superior performance between the CPU, DRAM and PCI bus with pipelined, burst, and concurrent operation.

TwisterT supports six banks of DRAMs (three memory modules) up to 1.5Gbyte of system memory with 256Mbit DRAM technology. The DRAM controller supports standard PC133 and PC100 Synchronous DRAM (SDRAM). The Synchronous DRAM interface allows zero wait state bursting between the DRAM and the data buffers at 133 / 100 MHz. The six banks of DRAM can be composed of an arbitrary mixture of 1M / 2M / 4M / 8M / 16M / 32MxN DRAMs. The DRAM controller can run at either the host CPU Front Side Bus frequency (133 / 100 MHz) or pseudo-synchronous to the CPU FSB frequency (PC100 with the FSB at 133 MHz or PC133 with the FSB at 100 MHz) with built-in PLL timing control.

TwisterT supports a 32-bit 3.3 / 5V system bus (PCI) that is synchronous / pseudo-synchronous to the CPU bus. The chip also contains a built-in bus-to-bus bridge to allow simultaneous concurrent operations on each bus. Five levels (doublewords) of post write buffers are included to allow for concurrent CPU and PCI operation. For PCI master operation, forty-eight levels (doublewords) of post write buffers and sixteen levels (doublewords) of prefetch buffers are included for concurrent PCI bus and DRAM/cache accesses. The chip also supports enhanced PCI bus commands such as Memory-Read-Line, Memory-Read-Multiple and Memory-Write-Invalid commands to minimize snoop overhead. In addition, advanced features are supported such as snoop

ahead, snoop filtering, L1 write-back forward to PCI master, and L1 write-back merged with PCI post write buffers to minimize PCI master read latency and DRAM utilization. Delay transaction and read caching mechanisms are also implemented for further improvement of overall system performance.

TwisterT also integrates S3 Graphics' 128-bit ProSavage4™ graphics accelerator into a single chip. TwisterT brings mainstream graphics performance to the Value PC with leading-edge 2D, 3D and DVD video acceleration into a cost effective package. Based on its capabilities, TwisterT is an ideal solution for the consumer, corporate mobile users and entry level professionals.

The industry's first integrated AGP 4X solution, TwisterT combines AGP 4X performance with Microsoft Direct-X texture compression and massive 2Kx2K textures to deliver unprecedented 3D performance and image quality for the Value PC mobile market.

The 352-pin VT8231 BGA PCI-LPC bridge supports four levels (doublewords) of line buffers, type F DMA transfers and delay transaction to allow efficient PCI bus utilization and (PCI-2.2 compliant). The VT8231 also includes an integrated Super I/O, integrated DS12885 style real time clock with extended 256 byte CMOS RAM, integrated master mode enhanced IDE controller with full scatter / gather capability and extension to UltraDMA-100 / 66 / 33 for 100 / 66 / 33 MB/sec transfer rate, integrated four USB interface with root hub and two function ports with built-in physical layer transceivers, Distributed DMA support, integrated AC-97 link for basic audio and HSP based modem functions, integrated hardware monitoring and OnNow / ACPI compliant advanced configuration and power management interface. The VT8231 also has an integrated MAC and 10Mbit PHY for LAN connection. It can bypass the internal PHY with external home PNA with a 1Mbit PHY or a 10/100Mbit PHY through the MII interface.

For sophisticated power management, TwisterT provides independent clock stop control for the CPU / SDRAM and PCI. A separate suspend-well plane is implemented for the SDRAM control signals for Suspend-to-DRAM operation. Coupled with the VT8231 south bridge chip, a complete power conscious PC main board can be implemented with no external TTLs.

High-Performance 3D Accelerator

Featuring a new super-pipelined 128-bit engine, TwisterT utilizes a single cycle architecture that provides high performance along with superior image quality. Several new features enhance the 3D architecture, including single-pass multitexturing, anisotropic filtering, and an 8-bit stencil buffer. TwisterT also offers the industry's only simultaneous usage of single-pass multitexturing and single-cycle trilinear filtering – enabling stunning image quality without performance loss. TwisterT further enhances image quality with true 32-bit color rendering throughout the 3D pipeline to produce more vivid and realistic images. TwisterT's advanced triangle setup engine provides industry leading 3D performance for a realistic user experience in games and other interactive 3D applications. The 3D engine is optimized for AGP texturing from system memory.

128-bit 2D Graphics Engine

TwisterT's advanced 128-bit 2D graphics engine delivers high-speed 2D acceleration for productivity applications. Several enhancements have been made to the 2D architecture to optimize SMA performance and to provide acceleration in all color depths.

DVD Playback and Video Conferencing

TwisterT provides the ideal architecture for high quality MPEG-2 based DVD applications and video conferencing. For DVD playback, TwisterT's video accelerator offloads the CPU by performing the planar to packed format conversion and motion compensation tasks, while its enhanced scaling algorithm delivers incredible full-screen video playback. For video conferencing, TwisterT's multiple video windows enable a cost effective solution.

LCD and Flat Panel Monitor Support

TwisterT supports a wide variety of DSTN or TFT panels through a 36-bit CMOS interface. This includes support for VGA, SVGA, XGA, and SXGA+ TFT color panels with 9-bit, 12-bit, 18-bit (both 1 pixel/clock and 2 pixels/clock), and 24-bit CMOS interfaces. Enhanced STN hardware with 256 gray scale support and advanced frame rate control to provide up to 16.7 million colors. In addition, the integrated 2-channel LVDS interface can support 18-bit color panels. All resolutions are supported up to SXGA+ (1400x1050). The integrated ZV-Port allows display of video from an external source.

High Screen Resolution CRT Support

	System Memory Frame Buffer Size	
Resolutions Supported	**8 MB**	**16/32 MB**
640x480x8/16/32	✔	✔
800x600x8/16/32	✔	✔
1024x768x8/16/32	✔	✔
1280x1024x8	✔	✔
1280x1024x16	✔	✔
1280x1024x32	✔	✔
1600x1200x8	✔	✔
1600x1200x16	✔	✔
1600x1200x32		✔
1920x1440x8		✔
1920x1440x16		✔

Table 1. Supported CRT Screen Resolutions

PINOUTS

Figure 2. VT8606 / TwisterT Ball Diagram (Top View)

Key	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
A	GND RGB	X IN	X OUT	GND PLL1	VCC PLL2	HD62	HD57	HD63	GND	HD45	HD38	HD34	HD31	HD16	HD13	HD3	HD12	GND	CPU RST#	HA18	HA20	HA22	HA10	HA28	HA3	GND
B	GND DAC	GND	VCC PLL1	AGP BUSY#	GND PLL2	HD50	HD59	HD48	HD51	HD44	HD22	HD32	HD33	HD19	HD24	HD2	HD10	HD1	HA26	HA29	HA23	HA25	HA21	HA13	HA5	HA6
C	VCC DAC	RED	GOP0	STP AGP#	FP D35	HD60	HD55	GND	HD41	HD49	HD43	HD28	HD26	GND	HD20	HD9	HD5	HD4	GND	HA27	HA31	HA19	HA16	HA9	HA11	HA8
D	VCC RGB	BLUE	GREEN	GND	HD61	HD53	HD54	HD47	HD42	HD37	HD36	HD29	HD25	HD23	HD7	HD11	HD8	HD6	HD15	HA30	HA17	HA12	GND	HA4	HA14	BNR#
E	V SYNC	H SYNC	RSET	COMP	HD56	HD58	HD46	HD40	HD27	HD39	VTT	GTL REF	HD35	HD21	HD30	HD14	HD18	HD17	HD0	HA24	GTL REF	CPU RSTD#	HA7	HREQ 0#	HREQ 4#	BPRI#
F	EN VDD	SP DAT1	SP CLK1	STAND BY	SUS PEND	GND	VTT	HD52	VTT	VTT	DFT IN	VTT	GND	GND	BIST IN	GND	VTT	VTT	VTT	VTT	GND	HA15	HREQ 1#	HREQ 2#	HREQ 3#	DEFER#
G	FP GPIO	FPD0 TVD11	FP VS	FP CLK	FP HS	VCC 3	G7	8	9	10	11	12	13	14	15	16	17	18	19	G20	VTT	HCLK	H LOCK#	HIT#	HT RDY#	HITM#
H	FP D2	FPD1 TVD10	FP DE	FP D5	EN VEE	VCC 3	H									CPU	Pins			H	VCC A	VCC A	RS0#	GND	RS2#	DBSY#
J	FP D4	FP D3	FPD08 TVD9	FP D7	FP D11	VCC 3	J		VCC 25	VCC 25	VCC 25	VCC 25	GND	GND	VCC 25	VCC 25	VCC 25	VCC 25		J	VTT	MCLK	D RDY#	ADS#	BREQ 0#	GND
K	FP D12	FP D10	FP D13	FP D20	FPD16 TVCKR	FP D6	K		VCC 25									VCC 25		K	VTT	MCLK F	RS1#	PLL TST	MD1	MD32
L	FPD17 TVBLK#	FP D15	FP D18	VCC 3	FPD09 TVD8	FP D14	L		VCC 25		GND	GND	GND	GND	GND	GND		VCC 25		L	GND A	GND A	MD33	MD35	MD3	MD2
M	FP D23	SP CLK2	SP DAT2	FP D21	FP D22	FP D19	M	Flat	VCC 25		GND	GND	GND	GND	GND	GND		VCC 25		M	GND	MD34	MD0	MD5	MD36	MD4
N	ZV D14	ZV D13	GND	ZV D15	ZV D12	GND	N	Panel	GND		GND	GND	GND	GND	GND	GND		GND		N	GND	MD39	MD37	MD7	MD38	MD6
P	GND	ZV D9	ZV D10	ZV D11	ZV D8	GND	P	Pins	GND		GND	GND	GND	GND	GND	GND		GND		P	GND	MD12	MD8	MD41	MD9	MD40
R	ZV D6	ZV D4	ZV D7	ZV D5	ZV D3	ZV D0	R		VCC 25		GND	GND	GND	GND	GND	GND		VCC 25		R	VCC 3	MD44	MD10	MD43	MD11	MD42
T	ZV D2	ZV D1	ZV HS	VCC3	FPD25 TVD4	FPD24 TVD6	T		VCC 25		GND	GND	GND	GND	GND	GND		VCC 25	DRAM	T	GND	MD15	MD13	MD46	MD14	MD45
U	ZV VS	FPD27 TVD7	ZV CLK	FPD26 TVD5	FPD33 TVD2	NC	U		VCC 25									VCC 25	Pins	U	VCC 3	SCAS A#	MD47	SWE A#	SWEB# CKE2	SWEC# CKE0
V	FPD28 TVD0	FPD29 TVD1	FPD30 TVD3	FPD32 TVCLK	FPD34 TVHS	VCC 3	V		VCC 25	VCC 25	VCC 25	VCC 25	GND	GND	VCC 25	VCC 25	VCC 25	VCC 25		V	VCC 3	NC	DQM0 CAS0#	SCASC# CKE1	SCASB# CKE3	GND
W	VCCA LVDS	VCCA LVDS	FPD31 TVVS	Y1 P	INTA#	VCC 3	W				PCI	Pins								W	CS5# RAS5#	NC	DQM1 CAS1#	GND	DQM5 CAS5#	DQM4 CAS4#
Y	GNDA LVDS	VCC LVDS	GNDA LPLL	Y1 M	Y2 P	VCC 3	Y7	8	9	10	11	12	13	14	15	16	17	18	19	Y20	VCC 3	CS4# RAS4#	CS3# RAS3#	CS2# RAS2#	CS1# RAS1#	CS0# RAS0#
AA	GNDA LVDS	GND LVDS	Y0 P	Z2 P	Y2 M	GND	VCC 3	AD16	VCC 3	VCC 3	WSC#	GP OUT	GND	GND	GND	FP DET	VCC 3	VCC 3	MD58	VCC 3	GND	VSUS 25	MA0	SRAS A#	SRASB# CKE5#	SRASC# CKE4#
AB	YC P	VCCA LPLL	Y0 M	Z2 M	GNT 0#	AD30	AD25	AD21	DEV SEL#	PAR	C/BE 1#	AD10	AD7	AD5	PCLK	MD63	MD29	MD56	MD54	MD20	MD18	NC	MA1	MA4	MA3	MA2
AC	YC M	Z0 P	Z1 P	GND	REQ 0#	AD29	AD24	AD23	AD17	I RDY#	AD15	AD11	AD6	AD4	P REQ#	MD31	MD60	MD25	MD23	MD52	MD49	SUSST#	GND	MA7	MA6	MA5
AD	ZC P	Z0 M	Z1 M	REQ 3#	REQ 1#	AD28	C/BE 3#	GND	C/BE 2#	T RDY#	AD14	AD9	GND	PWR OK	P GNT#	MD61	MD27	MD57	GND	MD21	MD50	MD16	DQM6 CAS6#	MA11 BA0	MA9	MA8
AE	ZC M	GNT X#	GNT 3#	REQ 2#	LOCK#	AD27	AD20	AD19	FRM#	STOP#	AD13	AD8	AD2	AD1	PCI RST#	MD30	MD59	MD26	MD55	MD22	MD19	MD48	DQM3 CAS3#	MA12 BA1	MA13	MA10
AF	GND	REQ X#	GNT 2#	GNT 1#	AD31	AD26	AD22	AD18	GND	SERR#	AD12	C/BE 0#	AD3	AD0	PCK RUN#	MD62	MD28	GND	MD24	MD53	MD51	MD17	DQM7 CAS7#	DQM2 CAS2#	MA14	GND

Table 2. VT8606 / TwisterT Pin List (Numerical Order)

Pin #		Pin Name	Pin #		Pin Name	Pin		Pin Name	Pin #		Pin Name	Pin #		Pin Names	Pin #		Pin Name
A01	**P**	**GNDRGB**	D03	A	GREEN	G05	O	FPHS	**P01**	**P**	**GND**	Y23	O	CS3# / RAS3#	AC25	O	MA06
A02	I	XIN	**D04**	**P**	**GND**	**G06**	**P**	**VCC3**	P02	I	ZVD09	Y24	O	CS2# / RAS2#	AC26	O	MA05
A03	O	XOUT	D05	IO	HD61	**G21**	**P**	**VTT**	P03	I	ZVD10	Y25	O	CS1# / RAS1#	AD01	A	ZCP
A04	**P**	**GNDPLL1**	D06	IO	HD53	G22	I	HCLK	P04	I	ZVD11	Y26	O	CS0# / RAS0#	AD02	A	Z0M
A05	**P**	**VCCPLL2**	D07	IO	HD54	G23	I	HLOCK#	P05	I	ZVD08	**AA01**	**P**	**GNDALVDS**	AD03	A	Z1M
A06	IO	HD62	D08	IO	HD47	G24	IO	HIT#	**P06**	**P**	**GND**	**AA02**	**P**	**GNDLVDS**	AD04	I	REQ3#
A07	IO	HD57	D09	IO	HD42	G25	IO	HTRDY#	**P21**	**P**	**GND**	AA03	A	Y0P	AD05	I	REQ1#
A08	IO	HD63	D10	IO	HD37	G26	I	HITM#	P22	IO	MD12	AA04	A	Z2P	AD06	IO	AD28
A09	**P**	**GND**	D11	IO	HD36	H01	O	FPD02	P23	IO	MD08	AA05	A	Y2M	AD07	IO	C/BE3#
A10	IO	HD45	D12	IO	HD29	H02	O	FPD01 / TVD10	P24	IO	MD41	**AA06**	**P**	**GND**	**AD08**	**P**	**GND**
A11	IO	HD38	D13	IO	HD25	H03	O	FPDE	P25	IO	MD09	**AA07**	**P**	**VCC3**	AD09	IO	C/BE2#
A12	IO	HD34	D14	IO	HD23	H04	O	FPD05	P26	IO	MD40	AA08	IO	AD16	AD10	IO	TRDY#
A13	IO	HD31	D15	IO	HD07	H05	O	ENVEE	R01	I	ZVD06	**AA09**	**P**	**VCC3**	AD11	IO	AD14
A14	IO	HD16	D16	IO	HD11	**H06**	**P**	**VCC3**	R02	I	ZVD04	**AA10**	**P**	**VCC3**	AD12	IO	AD09
A15	IO	HD13	D17	IO	HD08	**H21**	**P**	**VCCA**	R03	I	ZVD07	AA11	O	WSC#	**AD13**	**P**	**GND**
A16	IO	HD03	D18	IO	HD06	**H22**	**P**	**VCCA**	R04	I	ZVD05	AA12	O	GPOUT	AD14	I	PWROK
A17	IO	HD12	D19	IO	HD15	H23	IO	RS0#	R05	I	ZVD03	**AA13**	**P**	**GND**	AD15	O	PGNT#
A18	**P**	**GND**	D20	IO	HA30	**H24**	**P**	**GND**	R06	I	ZVD00	**AA14**	**P**	**GND**	AD16	IO	MD61
A19	O	CPURST#	D21	IO	HA17	H25	IO	RS2#	**R21**	**P**	**VCC3**	**AA15**	**P**	**GND**	AD17	IO	MD27
A20	IO	HA18	D22	IO	HA12	H26	IO	DBSY#	R22	IO	MD44	AA16	I	FPDET	AD18	IO	MD57
A21	IO	HA20	**D23**	**P**	**GND**	J01	O	FPD04	R23	IO	MD10	**AA17**	**P**	**VCC3**	**AD19**	**P**	**GND**
A22	IO	HA22	D24	IO	HA04	J02	O	FPD03	R24	IO	MD43	**AA18**	**P**	**VCC3**	AD20	IO	MD21
A23	IO	HA10	D25	IO	HA14	J03	O	FPD08 / TVD9	R25	IO	MD11	AA19	IO	MD58	AD21	IO	MD50
A24	IO	HA28	D26	IO	BNR#	J04	O	FPD07	R26	IO	MD42	**AA20**	**P**	**VCC3**	AD22	IO	MD16
A25	IO	HA03	E01	O	VSYNC	J05	O	FPD11	T01	I	ZVD02	**AA21**	**P**	**GND**	AD23	O	DQM6 / CAS6#
A26	**P**	**GND**	E02	O	HSYNC	**J06**	**P**	**VCC3**	T02	I	ZVD01	**AA22**	**P**	**VSUS25**	AD24	O	MA11 / BA0
B01	**P**	**GNDDAC**	E03	A	RSET	**J21**	**P**	**VTT**	T03	I	ZVHS	AA23	O	MA00	AD25	O	MA09
B02	**P**	**GND**	E04	A	COMP	J22	O	MCLK	**T04**	**P**	**VCC3**	AA24	O	SRASA#	AD26	O	MA08
B03	**P**	**VCCPLL1**	E05	IO	HD56	J23	IO	DRDY#	T05	O	FPD25 / TVD4	AA25	O	SRASB# / CKE5	AE01	A	ZCM
B04	IO	AGPBUSY#	E06	IO	HD58	J24	IO	ADS#	T06	O	FPD24 / TVD6	AA26	O	SRASC# / CKE4	AE02	O	GNTX#
B05	**P**	**GNDPLL2**	E07	IO	HD46	J25	O	BREQ0#	**T21**	**P**	**GND**	AB01	A	YCP	AE03	O	GNT3#
B06	IO	HD50	E08	IO	HD40	**J26**	**P**	**GND**	T22	IO	MD15	**AB02**	**P**	**VCCALPLL**	AE04	I	REQ2#
B07	IO	HD59	E09	IO	HD27	K01	O	FPD12	T23	IO	MD13	AB03	A	Y0M	AE05	IO	LOCK#
B08	IO	HD48	E10	IO	HD39	K02	O	FPD10	T24	IO	MD46	AB04	A	Z2M	AE06	IO	AD27
B09	IO	HD51	**E11**	**P**	**VTT**	K03	O	FPD13	T25	IO	MD14	AB05	O	GNT0#	AE07	IO	AD20
B10	IO	HD44	**E12**	**P**	**GTLREF**	K04	O	FPD20	T26	IO	MD45	AB06	IO	AD30	AE08	IO	AD19
B11	IO	HD22	E13	IO	HD35	K05	O	FPD16 / TVCLKR	U01	I	ZVVS	AB07	IO	AD25	AE09	IO	FRAME#
B12	IO	HD32	E14	IO	HD21	K06	O	FPD06	U02	O	FPD27 / TVD7	AB08	IO	AD21	AE10	IO	STOP#
B13	IO	HD33	E15	IO	HD30	**K21**	**P**	**VTT**	U03	I	ZVCLK	AB09	IO	DEVSEL#	AE11	IO	AD13
B14	IO	HD19	E16	IO	HD14	K22	I	MCLKF	U04	O	FPD26 / TVD5	AB10	IO	PAR	AE12	IO	AD08
B15	IO	HD24	E17	IO	HD18	K23	IO	RS1#	U05	O	FPD33 / TVD2	AB11	IO	C/BE1#	AE13	IO	AD02
B16	IO	HD02	E18	IO	HD17	K24	I	PLLTST	U06		NC	AB12	IO	AD10	AE14	IO	AD01
B17	IO	HD10	E19	IO	HD00	K25	IO	MD01	**U21**	**P**	**VCC3**	AB13	IO	AD07	AE15	I	RESET#
B18	IO	HD01	E20	IO	HA24	K26	IO	MD32	U22	O	SCASA#	AB14	IO	AD05	AE16	IO	MD30
B19	IO	HA26	**E21**	**P**	**GTLREF**	L01	O	FPD17 / TVBLK#	U23	IO	MD47	AB15	I	PCLK	AE17	IO	MD59
B20	IO	HA29	E22	O	CPURSTD#	L02	O	FPD15	U24	O	SWEA#	AB16	IO	MD63	AE18	IO	MD26
B21	IO	HA23	E23	IO	HA07	L03	O	FPD18	U25	O	SWEB# / CKE2	AB17	IO	MD29	AE19	IO	MD55
B22	IO	HA25	E24	IO	HREQ0#	**L04**	**P**	**VCC3**	U26	O	SWEC# / CKE0	AB18	IO	MD56	AE20	IO	MD22
B23	IO	HA21	E25	IO	HREQ4#	L05	O	FPD09 / TVD8	V01	O	FPD28 / TVD0	AB19	IO	MD54	AE21	IO	MD19
B24	IO	HA13	E26	IO	BPRI#	L06	O	FPD14	V02	O	FPD29 / TVD1	AB20	IO	MD20	AE22	IO	MD48
B25	IO	HA05	F01	O	ENVDD	**L21**	**P**	**GNDA**	V03	O	FPD30 / TVD3	AB21	IO	MD18	AE23	O	DQM3 / CAS3#
B26	IO	HA06	F02	IO	SPDAT1	**L22**	**P**	**GNDA**	V04	O	FPD32 / TVCLK	AB22	P	NC	AE24	O	MA12 / BA1
C01	**P**	**VCCDAC**	F03	IO	SPCLK1	L23	IO	MD33	V05	O	FPD34 / TVHS	AB23	O	MA01	AE25	O	MA13
C02	A	RED	F04	I	STANDBY	L24	IO	MD35	**V06**	**P**	**VCC3**	AB24	O	MA04	AE26	O	MA10
C03	O	GOP0	F05	I	SUSPEND	L25	IO	MD03	**V21**	**P**	**VCC3**	AB25	O	MA03	**AF01**	**P**	**GND**
C04	I	STPAGP#	**F06**	**P**	**GND**	L26	IO	MD02	V22	P	NC	AB26	O	MA02	AF02	I	REQX#
C05	IO	FPD35	**F07**	**P**	**VTT**	M01	O	FPD23	V23	O	DQM0 / CAS0#	AC01	A	YCM	AF03	O	GNT2#
C06	IO	HD60	F08	IO	HD52	M02	IO	SPCLK2	V24	O	SCASC# / CKE1	AC02	A	Z0P	AF04	O	GNT1#
C07	IO	HD55	**F09**	**P**	**VTT**	M03	IO	SPDAT2	V25	O	SCASB# / CKE3	AC03	A	Z1P	AF05	IO	AD31
C08	**P**	**GND**	**F10**	**P**	**VTT**	M04	O	FPD21	**V26**	**P**	**GND**	**AC04**	**P**	**GND**	AF06	IO	AD26
C09	IO	HD41	F11	I	DFTIN	M05	O	FPD22	**W01**	**P**	**VCCALVDS**	AC05	I	REQ0#	AF07	IO	AD22
C10	IO	HD49	**F12**	**P**	**VTT**	M06	O	FPD19	**W02**	**P**	**VCCALVDS**	AC06	IO	AD29	AF08	IO	AD18
C11	IO	HD43	**F13**	**P**	**GND**	**M21**	**P**	**GND**	W03	O	FPD31 / TVVS	AC07	IO	AD24	**AF09**	**P**	**GND**
C12	IO	HD28	**F14**	**P**	**GND**	M22	IO	MD34	W04	A	Y1P	AC08	IO	AD23	AF10	IO	SERR#
C13	IO	HD26	F15	I	BISTIN	M23	IO	MD00	W05	O	INTA#	AC09	IO	AD17	AF11	IO	AD12
C14	**P**	**GND**	**F16**	**P**	**GND**	M24	IO	MD05	**W06**	**P**	**VCC3**	AC10	IO	IRDY#	AF12	IO	C/BE0#
C15	IO	HD20	**F17**	**P**	**VTT**	M25	IO	MD36	W21	O	CS5# / RAS5#	AC11	IO	AD15	AF13	IO	AD03
C16	IO	HD09	**F18**	**P**	**VTT**	M26	IO	MD04	W22	-	NC	AC12	IO	AD11	AF14	IO	AD00
C17	IO	HD05	**F19**	**P**	**VTT**	N01	I	ZVD14	W23	O	DQM1 / CAS1#	AC13	IO	AD06	AF15	IO	PCKRUN#
C18	IO	HD04	**F20**	**P**	**VTT**	N02	I	ZVD13	**W24**	**P**	**GND**	AC14	IO	AD04	AF16	IO	MD62
C19	**P**	**GND**	**F21**	**P**	**GND**	**N03**	**P**	**GND**	W25	O	DQM5 / CAS5#	AC15	I	PREQ#	AF17	IO	MD28
C20	IO	HA27	F22	IO	HA15	N04	I	ZVD15	W26	O	DQM4 / CAS4#	AC16	IO	MD31	**AF18**	**P**	**GND**
C21	IO	HA31	F23	IO	HREQ1#	N05	I	ZVD12	**Y01**	**P**	**GNDALVDS**	AC17	IO	MD60	AF19	IO	MD24
C22	IO	HA19	F24	IO	HREQ2#	**N06**	**P**	**GND**	**Y02**	**P**	**VCCLVDS**	AC18	IO	MD25	AF20	IO	MD53
C23	IO	HA16	F25	IO	HREQ3#	**N21**	**P**	**GND**	**Y03**	**P**	**GNDALPLL**	AC19	IO	MD23	AF21	IO	MD51
C24	IO	HA09	F26	IO	DEFER#	N22	IO	MD39	Y04	A	Y1M	AC20	IO	MD52	AF22	IO	MD17
C25	IO	HA11	G01	IO	FPGPIO	N23	IO	MD37	Y05	A	Y2P	AC21	IO	MD49	AF23	O	DQM7 / CAS7#
C26	IO	HA08	G02	O	FPD0 / TVD11	N24	IO	MD07	**Y06**	**P**	**VCC3**	AC22	I	SUSST#	AF24	O	DQM2 / CAS2#
D01	**P**	**VCCRGB**	G03	O	FPVS	N25	IO	MD38	**Y21**	**P**	**VCC3**	**AC23**	**P**	**GND**	AF25	O	MA14
D02	A	BLUE	G04	O	FPCLK	N26	IO	MD06	Y22	O	CS4# / RAS4#	AC24	O	MA07	**AF26**	**P**	**GND**

Center **VCC25** Pins (28 pins): **J9-12,15-18, K9,18, L9,18, M9,18, R9,18, T9,18, U9,18, V9-12,15-18**

Center **GND** Pins (44 pins): **J13-14, L11-16, M11-16, N9,11-16,18, P9,11-16,18, R11-16, T11-16, V13-14**

Table 3. VT8606 / TwisterT Pin List (Alphabetical Order)

Pin #		Pin Name	Pin #		Pin Name	Pin #		Pin	Pin #		Pin Name	Pin #		Pin Names	Pin #		Pin Name
AF14	IO	AD00	K01	O	FPD12	AB05	O	GNT0#	E08	IO	HD40	AE18	IO	MD26	**G06**	**P**	**VCC3**
AE14	IO	AD01	K03	O	FPD13	AF04	O	GNT1#	C09	IO	HD41	AD17	IO	MD27	**H06**	**P**	**VCC3**
AE13	IO	AD02	L06	O	FPD14	AF03	O	GNT2#	D09	IO	HD42	AF17	IO	MD28	**J06**	**P**	**VCC3**
AF13	IO	AD03	L02	O	FPD15	AE03	O	GNT3#	C11	IO	HD43	AB17	IO	MD29	**L04**	**P**	**VCC3**
AC14	IO	AD04	K05	O	FPD16 / TVCLKR	AE02	O	GNTX#	B10	IO	HD44	AE16	IO	MD30	**R21**	**P**	**VCC3**
AB14	IO	AD05	L01	O	FPD17 / TVBLK#	C03	O	GOP0	A10	IO	HD45	AC16	IO	MD31	**T04**	**P**	**VCC3**
AC13	IO	AD06	L03	O	FPD18	AA12	O	GPOUT	E07	IO	HD46	K26	IO	MD32	**U21**	**P**	**VCC3**
AB13	IO	AD07	M06	O	FPD19	D03	A	GREEN	D08	IO	HD47	L23	IO	MD33	**V06**	**P**	**VCC3**
AE12	IO	AD08	K04	O	FPD20	**E12**	**P**	**GTLREF**	B08	IO	HD48	M22	IO	MD34	**V21**	**P**	**VCC3**
AD12	IO	AD09	M04	O	FPD21	**E21**	**P**	**GTLREF**	C10	IO	HD49	L24	IO	MD35	**W06**	**P**	**VCC3**
AB12	IO	AD10	M05	O	FPD22	A25	IO	HA03	B06	IO	HD50	M25	IO	MD36	**Y06**	**P**	**VCC3**
AC12	IO	AD11	M01	O	FPD23	D24	IO	HA04	B09	IO	HD51	N23	IO	MD37	**Y21**	**P**	**VCC3**
AF11	IO	AD12	T06	O	FPD24 / TVD6	B25	IO	HA05	F08	IO	HD52	N25	IO	MD38	**AA07**	**P**	**VCC3**
AE11	IO	AD13	T05	O	FPD25 / TVD4	B26	IO	HA06	D06	IO	HD53	N22	IO	MD39	**AA09**	**P**	**VCC3**
AD11	IO	AD14	U04	O	FPD26 / TVD5	E23	IO	HA07	D07	IO	HD54	P26	IO	MD40	**AA10**	**P**	**VCC3**
AC11	IO	AD15	U02	O	FPD27 / TVD7	C26	IO	HA08	C07	IO	HD55	P24	IO	MD41	**AA17**	**P**	**VCC3**
AA08	IO	AD16	V01	O	FPD28 / TVD0	C24	IO	HA09	E05	IO	HD56	R26	IO	MD42	**AA18**	**P**	**VCC3**
AC09	IO	AD17	V02	O	FPD29 / TVD1	A23	IO	HA10	A07	IO	HD57	R24	IO	MD43	**AA20**	**P**	**VCC3**
AF08	IO	AD18	V03	O	FPD30 / TVD3	C25	IO	HA11	E06	IO	HD58	R22	IO	MD44	**H21**	**P**	**VCCA**
AE08	IO	AD19	W03	O	FPD31 / TVVS	D22	IO	HA12	B07	IO	HD59	T26	IO	MD45	**H22**	**P**	**VCCA**
AE07	IO	AD20	V04	O	FPD32 / TVCLK	B24	IO	HA13	C06	IO	HD60	T24	IO	MD46	**AB02**	**P**	**VCCALPLL**
AB08	IO	AD21	U05	O	FPD33 / TVD2	D25	IO	HA14	D05	IO	HD61	U23	IO	MD47	**W01**	**P**	**VCCALVDS**
AF07	IO	AD22	V05	O	FPD34 / TVHS	F22	IO	HA15	A06	IO	HD62	AE22	IO	MD48	**W02**	**P**	**VCCALVDS**
AC08	IO	AD23	C05	IO	FPD35	C23	IO	HA16	A08	IO	HD63	AC21	IO	MD49	**C01**	**P**	**VCCDAC**
AC07	IO	AD24	H03	O	FPDE	D21	IO	HA17	G24	IO	HIT#	AD21	IO	MD50	**Y02**	**P**	**VCCLVDS**
AB07	IO	AD25	AA16	I	FPDET	A20	IO	HA18	G26	I	HITM#	AF21	IO	MD51	**B03**	**P**	**VCCPLL1**
AF06	IO	AD26	G01	IO	FPGPIO	C22	IO	HA19	G23	I	HLOCK#	AC20	IO	MD52	**A05**	**P**	**VCCPLL2**
AE06	IO	AD27	G05	O	FPHS	A21	IO	HA20	E24	IO	HREQ0#	AF20	IO	MD53	**D01**	**P**	**VCCRGB**
AD06	IO	AD28	G03	O	FPVS	B23	IO	HA21	F23	IO	HREQ1#	AB19	IO	MD54	**AA22**	**P**	**VSUS25**
AC06	IO	AD29	AE09	IO	FRAME#	A22	IO	HA22	F24	IO	HREQ2#	AE19	IO	MD55	**E11**	**P**	**VTT**
AB06	IO	AD30	**A09**	**P**	**GND**	B21	IO	HA23	F25	IO	HREQ3#	AB18	IO	MD56	**F07**	**P**	**VTT**
AF05	IO	AD31	**A18**	**P**	**GND**	E20	IO	HA24	E25	IO	HREQ4#	AD18	IO	MD57	**F09**	**P**	**VTT**
J24	IO	ADS#	**A26**	**P**	**GND**	B22	IO	HA25	E02	O	HSYNC	AA19	IO	MD58	**F10**	**P**	**VTT**
B04	IO	AGPBUSY#	**B02**	**P**	**GND**	B19	IO	HA26	G25	IO	HTRDY#	AE17	IO	MD59	**F12**	**P**	**VTT**
F15	I	BISTIN	**C08**	**P**	**GND**	C20	IO	HA27	W05	O	INTA#	AC17	IO	MD60	**F17**	**P**	**VTT**
D02	A	BLUE	**C14**	**P**	**GND**	A24	IO	HA28	AC10	IO	IRDY#	AD16	IO	MD61	**F18**	**P**	**VTT**
D26	IO	BNR#	**C19**	**P**	**GND**	B20	IO	HA29	AE05	IO	LOCK#	AF16	IO	MD62	**F19**	**P**	**VTT**
E26	IO	BPRI#	**D04**	**P**	**GND**	D20	IO	HA30	AA23	O	MA00	AB16	IO	MD63	**F20**	**P**	**VTT**
J25	O	BREQ0#	**D23**	**P**	**GND**	C21	IO	HA31	AB23	O	MA01	U6		NC	**G21**	**P**	**VTT**
AF12	IO	C/BE0#	**F06**	**P**	**GND**	G22	I	HCLK	AB26	O	MA02	V22		NC	**J21**	**P**	**VTT**
AB11	IO	C/BE1#	**F13**	**P**	**GND**	E19	IO	HD00	AB25	O	MA03	W22		NC	**K21**	**P**	**VTT**
AD09	IO	C/BE2#	**F14**	**P**	**GND**	B18	IO	HD01	AB24	O	MA04	AB22		NC	E01	O	VSYNC
AD07	IO	C/BE3#	**F16**	**P**	**GND**	B16	IO	HD02	AC26	O	MA05	AB10	IO	PAR	AA11	O	WSC#
E04	A	COMP	**F21**	**P**	**GND**	A16	IO	HD03	AC25	O	MA06	AF15	IO	PCKRUN#	A02	I	XIN
A19	O	CPURST#	**H24**	**P**	**GND**	C18	IO	HD04	AC24	O	MA07	AB15	I	PCLK	A03	O	XOUT
E22	O	CPURSTD#	**J26**	**P**	**GND**	C17	IO	HD05	AD26	O	MA08	AD15	O	PGNT#	AB03	A	Y0M
Y26	O	CS0# / RAS0#	**M21**	**P**	**GND**	D18	IO	HD06	AD25	O	MA09	K24	I	PLLTST	AA03	A	Y0P
Y25	O	CS1# / RAS1#	**N03**	**P**	**GND**	D15	IO	HD07	AE26	O	MA10	AC15	I	PREQ#	Y04	A	Y1M
Y24	O	CS2# / RAS2#	**N06**	**P**	**GND**	D17	IO	HD08	AD24	O	MA11 / BA0	AD14	I	PWROK	W04	A	Y1P
Y23	O	CS3# / RAS3#	**N21**	**P**	**GND**	C16	IO	HD09	AE24	O	MA12 / BA1	C02	A	RED	AA05	A	Y2M
Y22	O	CS4# / RAS4#	**P01**	**P**	**GND**	B17	IO	HD10	AE25	O	MA13	AC05	I	REQ0#	Y05	A	Y2P
W21	O	CS5# / RAS5#	**P06**	**P**	**GND**	D16	IO	HD11	AF25	O	MA14	AD05	I	REQ1#	AC01	A	YCM
H26	IO	DBSY#	**P21**	**P**	**GND**	A17	IO	HD12	J22	O	MCLK	AE04	I	REQ2#	AB01	A	YCP
F26	IO	DEFER#	**T21**	**P**	**GND**	A15	IO	HD13	K22	I	MCLKF	AD04	I	REQ3#	AD02	A	Z0M
AB09	IO	DEVSEL#	**V26**	**P**	**GND**	E16	IO	HD14	M23	IO	MD00	AF02	I	REQX#	AC02	A	Z0P
F11	I	DFTIN	**W24**	**P**	**GND**	D19	IO	HD15	K25	IO	MD01	AE15	I	RESET#	AD03	A	Z1M
V23	O	DQM0 / CAS0#	**AA06**	**P**	**GND**	A14	IO	HD16	L26	IO	MD02	H23	IO	RS0#	AC03	A	Z1P
W23	O	DQM1 / CAS1#	**AA13**	**P**	**GND**	E18	IO	HD17	L25	IO	MD03	K23	IO	RS1#	AB04	A	Z2M
AF24	O	DQM2 / CAS2#	**AA14**	**P**	**GND**	E17	IO	HD18	M26	IO	MD04	H25	IO	RS2#	AA04	A	Z2P
AE23	O	DQM3 / CAS3#	**AA15**	**P**	**GND**	B14	IO	HD19	M24	IO	MD05	E03	A	RSET	AE01	A	ZCM
W26	O	DQM4 / CAS4#	**AA21**	**P**	**GND**	C15	IO	HD20	N26	IO	MD06	U22	O	SCASA#	AD01	A	ZCP
W25	O	DQM5 / CAS5#	**AC04**	**P**	**GND**	E14	IO	HD21	N24	IO	MD07	V25	O	SCASB# / CKE3	U03	I	ZVCLK
AD23	O	DQM6 / CAS6#	**AC23**	**P**	**GND**	B11	IO	HD22	P23	IO	MD08	V24	O	SCASC# / CKE1	R06	I	ZVD00
AF23	O	DQM7 / CAS7#	**AD08**	**P**	**GND**	D14	IO	HD23	P25	IO	MD09	AF10	IO	SERR#	T02	I	ZVD01
J23	IO	DRDY#	**AD13**	**P**	**GND**	B15	IO	HD24	R23	IO	MD10	F03	IO	SPCLK1	T01	I	ZVD02
F01	O	ENVDD	**AD19**	**P**	**GND**	D13	IO	HD25	R25	IO	MD11	M02	IO	SPCLK2	R05	I	ZVD03
H05	O	ENVEE	**AF01**	**P**	**GND**	C13	IO	HD26	P22	IO	MD12	F02	IO	SPDAT1	R02	I	ZVD04
G04	O	FPCLK	**AF09**	**P**	**GND**	E09	IO	HD27	T23	IO	MD13	M03	IO	SPDAT2	R04	I	ZVD05
G02	O	FPD0 / TVD11	**AF18**	**P**	**GND**	C12	IO	HD28	T25	IO	MD14	AA24	O	SRASA#	R01	I	ZVD06
H02	O	FPD01 / TVD10	**AF26**	**P**	**GND**	D12	IO	HD29	T22	IO	MD15	AA25	O	SRASB# / CKE5	R03	I	ZVD07
H01	O	FPD02	**L21**	**P**	**GNDA**	E15	IO	HD30	AD22	IO	MD16	AA26	O	SRASC# / CKE4	P05	I	ZVD08
J02	O	FPD03	**L22**	**P**	**GNDA**	A13	IO	HD31	AF22	IO	MD17	F04	I	STANDBY	P02	I	ZVD09
J01	O	FPD04	**Y03**	**P**	**GNDALPLL**	B12	IO	HD32	AB21	IO	MD18	AE10	IO	STOP#	P03	I	ZVD10
H04	O	FPD05	**AA01**	**P**	**GNDALVDS**	B13	IO	HD33	AE21	IO	MD19	C04	I	STPAGP#	P04	I	ZVD11
K06	O	FPD06	**Y01**	**P**	**GNDALVDS**	A12	IO	HD34	AB20	IO	MD20	F05	I	SUSPEND	N05	I	ZVD12
J04	O	FPD07	**B01**	**P**	**GNDDAC**	E13	IO	HD35	AD20	IO	MD21	AC22	I	SUSST#	N02	I	ZVD13
J03	O	FPD08 / TVD9	**AA02**	**P**	**GNDLVDS**	D11	IO	HD36	AE20	IO	MD22	U24	O	SWEA#	N01	I	ZVD14
L05	O	FPD09 / TVD8	**A04**	**P**	**GNDPLL1**	D10	IO	HD37	AC19	IO	MD23	U25	O	SWEB# / CKE2	N04	I	ZVD15
K02	O	FPD10	**B05**	**P**	**GNDPLL2**	A11	IO	HD38	AF19	IO	MD24	U26	O	SWEC# / CKE0	T03	I	ZVHS
J05	O	FPD11	**A01**	**P**	**GNDRGB**	E10	IO	HD39	AC18	IO	MD25	AD10	IO	TRDY#	U01	I	ZVVS

Center **VCC25** Pins (28 pins): **J9-12,15-18, K9,18, L9,18, M9,18, R9,18, T9,18, U9,18, V9-12,15-18**
Center **GND** Pins (44 pins): **J13-14, L11-16, M11-16, N9,11-16,18, P9,11-16,18, R11-16, T11-16, V13-14**

PIN DESCRIPTIONS

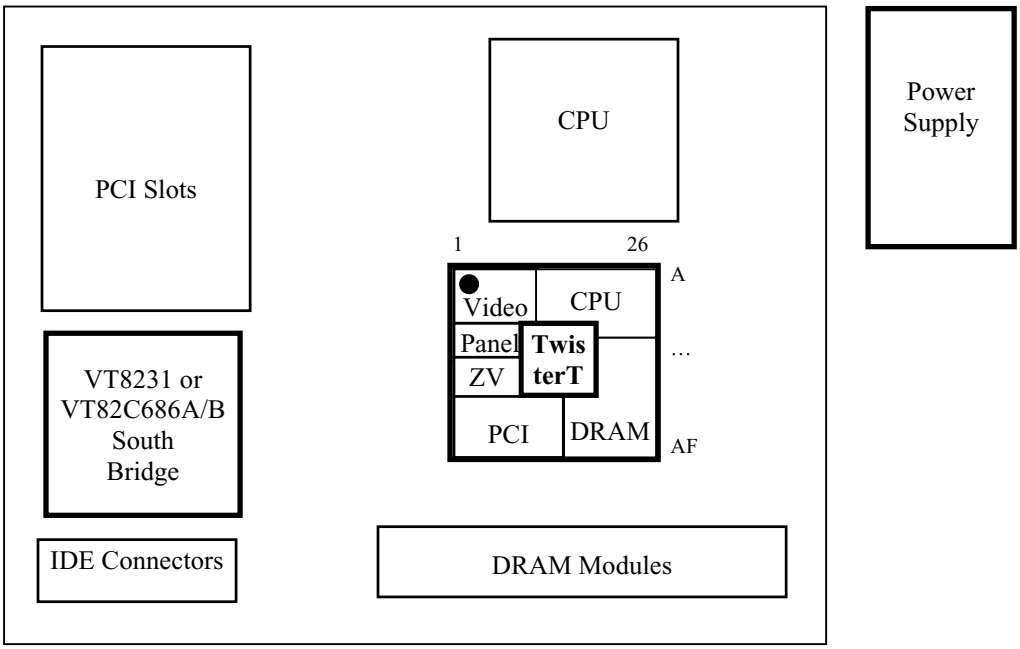
Table 4. VT8606 / TwisterT Pin Descriptions

CPU Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
HA[31:3]#	(see pinout tables)	IO	**Host Address Bus.** HA[31:3] connect to the address bus of the host CPU. During CPU cycles HA[31:3] are inputs. These signals are driven by the TwisterT during cache snooping operations.
HD[63:0]#	(see pinout tables)	IO	**Host CPU Data.** These signals are connected to the CPU data bus.
ADS#	J24	IO	**Address Strobe**. The CPU asserts ADS# in T1 of the CPU bus cycle.
BNR#	D26	IO	**Block Next Request**. Used to block the current request bus owner from issuing new requests. This signal is used to dynamically control the processor bus pipeline depth.
BPRI#	E26	IO	**Priority Agent Bus Request**. The owner of this signal will always be the next bus owner. This signal has priority over symmetric bus requests and causes the current symmetric owner to stop issuing new transactions unless the HLOCK# signal is asserted. The TwisterT drives this signal to gain control of the processor bus.
DBSY#	H26	IO	**Data Bus Busy**. Used by the data bus owner to hold the data bus for transfers requiring more than one cycle.
DEFER#	F26	IO	**Defer**. The TwisterT uses a dynamic deferring policy to optimize system performance. The TwisterT also uses the DEFER# signal to indicate a processor retry response.
DRDY#	J23	IO	**Data Ready**. Asserted for each cycle that data is transferred.
HIT#	G24	IO	**Hit**. Indicates that a caching agent holds an unmodified version of the requested line. Also driven in conjunction with HITM# by the target to extend the snoop window.
HITM#	G26	I	**Hit Modified**. Asserted by the CPU to indicate that the address presented with the last assertion of EADS# is modified in the L1 cache and needs to be written back.
HLOCK#	G23	I	**Host Lock**. All CPU cycles sampled with the assertion of HLOCK# and ADS# until the negation of HLOCK# must be atomic.
HREQ[4:0]#	E25, F25, F24, F23 E24	IO	**Request Command**. Asserted during both clocks of the request phase. In the first clock, the signals define the transaction type to a level of detail that is sufficient to begin a snoop request. In the second clock, the signals carry additional information to define the complete transaction type.
HTRDY#	G25	IO	**Host Target Ready**. Indicates that the target of the processor transaction is able to enter the data transfer phase.
RS[2:0]#	H25, K23 H23	IO	**Response Signals**. Indicates the type of response per the table below: **RS[2:0]# — Response type** 000 — Idle State 001 — Retry Response 010 — Defer Response 011 — Reserved 100 — Hard Failure 101 — Normal Without Data 110 — Implicit Writeback 111 — Normal With Data
CPURST#	A19	O	**CPU Reset.** Reset output to CPU. External pullup and filter capacitor to ground should be provided per CPU manufacturer's recommendations.
CPURSTD#	E22	O	**CPU Reset Delayed.** CPU reset output delayed by 2T.
BREQ0#	J25	O	**Bus Request 0.** Bus request output to CPU.

Note: Clocking of the CPU interface is performed with HCLK.

Note: Internal pullup resistors are provided on all GTL interface pins. If the CPU does not have internal pullups, these north bridge internal pullups may be enabled to allow the interface to meet GTL bus interface specifications (see MA6 strap description).

The pinouts were defined assuming the ATX PCB layout model shown below (and general pin layout shown) as a guide for PCB component placement. Other PCB layouts (AT, LPX, and NLX) were also considered and can typically follow the same general component placement.



DRAM Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
MD[63:0]	(see pinout tables)	IO	**Memory Data.** These signals are connected to the DRAM data bus.
MA14 /graphics strap **MA13** /graphics strap **MA12 / BA1** / strap, **MA11 / BA0** / strap, **MA10** **MA9** / strap, **MA8** / strap, **MA7** / strap, **MA6** / strap, **MA5** / strap, **MA4** / graphics strap, **MA3** / graphics strap, **MA2** / graphics strap, **MA1** / graphics strap, **MA0** / graphics strap	AF25 AE25 AE24 AD24 AE26 AD25 AD26 AC24 AC25 AC26 AB24 AB25 AB26 AB23 AA23	O / I	**Memory Address.** DRAM address lines / strap options MA12 strap – Host Freq Select lsb (see MA8 below for msb) MA11 strap – IOQ Level (0=4-level, 1=1-level) MA9 strap – Clock select (0=Use PLLs, 1=Clocks on XIN/PD10 pins) MA8 strap – Host Freq Select msb (00=66, 01=100, 10=auto, 11=133) MA7 strap – Graphics Test Mode (0=Normal, 1=Test) MA6 strap – GTL Internal Pullups (0=Enable, 1=Disable) MA5 strap – PCI Frequency (0=33 MHz, 1=66 MHz) MA4 strap – Graphics PCI Interrupt (0=Enable, 1=Disable) MA3 strap – Graphics I/O (0=Enable, 1=Disable) MA2 strap – Graphics PCI Base Address (0=Map0, 1=Map1) MA14,13,1,0 – Graphics OEM-Defined Panel Type (Note: all non-graphics straps default to 0 if not connected to a strap resistor. See Table 9 for graphics strap definitions and defaults.)
CS[5:0]# **RAS[5:0]#**	W21, Y22 Y23, Y24 Y25, Y26	O	**Chip Select.** (Synchronous DRAM) Chip select of each bank. **RAS.** (FPG/EDO DRAM)
DQM[7:0] **CAS[7:0]#**	AF23, AD23, W25, W26, AE23, AF24, W23, V23	O	**Data Mask.** (Synchronous DRAM) Data mask of each byte lane **CAS.** (FPG/EDO DRAM)
SRASA# **SRASB# / CKE5** **SRASC# / CKE4**	AA24 AA25 AA26	O	**Row Address Command Indicator.** For support of up to three synchronous DRAM DIMM slots. "A" controls banks 0-1 (module 0), "B" controls banks 2-3 (module 1) and "C" controls banks 4-5 (module 2).
SCASA# **SCASB# / CKE3** **SCASC# / CKE1**	U22 V25 V24	O	**Column Address Command Indicator.** For support of up to three synchronous DRAM DIMM slots. "A" controls banks 0-1 (module 0), "B" controls banks 2-3 (module 1) and "C" controls banks 4-5 (module 2).
SWEA# / MWEA **SWEB# / MWEB#/CKE2** **SWEC# / MWEC#/CKE0**	U24 U25 U26	O	**Write Enable Command Indicator.** For support of up to three synchronous DRAM DIMM slots. Used as MWE# for FPG/EDO memory. "A" controls banks 0-1 (module 0), "B" controls banks 2-3 (module 1) and "C" controls banks 4-5 (module 2).
CKE0 / SWEC# **CKE1 / SCASC#** **CKE2 / SWEB#** **CKE3 / SCASB#** **CKE4 / SRASC#** **CKE5 / SRASB#**	U26 V24 U25 V25 AA26 AA25	O	**SDRAM Clock Enables.** Clock enables for each DRAM bank for powering down the SDRAM or clock control for reducing power usage and for reducing heat / temperature in high-speed memory systems.

PCI Bus Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
AD[31:0]	(see pinout tables)	IO	**Address/Data Bus.** The standard PCI address and data lines. The address is driven with FRAME# assertion and data is driven or received in following cycles.
CBE[3:0]#	AD7, AD9, AB11, AF12	IO	**Command/Byte Enable.** Commands are driven with FRAME# assertion. Byte enables corresponding to supplied or requested data are driven on following clocks.
FRAME#	AE9	IO	**Frame.** Assertion indicates the address phase of a PCI transfer. Negation indicates that one more data transfer is desired by the cycle initiator.
IRDY#	AC10	IO	**Initiator Ready.** Asserted when the initiator is ready for data transfer.
TRDY#	AD10	IO	**Target Ready.** Asserted when the target is ready for data transfer.
STOP#	AE10	IO	**Stop.** Asserted by the target to request the master to stop the current transaction.
DEVSEL#	AB9	IO	**Device Select.** This signal is driven by the TwisterT when a PCI initiator is attempting to access main memory. It is an input when the TwisterT is acting as a PCI initiator.
PAR	AB10	IO	**Parity.** A single parity bit is provided over AD[31:0] and C/BE[3:0].
SERR#	AF10	IO	**System Error.** The TwisterT will pulse this signal when it detects a system error condition.
LOCK#	AE5	IO	**Lock.** Used to establish, maintain, and release resource lock.
PREQ#	AC15	I	**South Bridge Request.** This signal comes from the South Bridge. PREQ# is the South Bridge request for the PCI bus.
PGNT#	AD15	O	**South Bridge Grant.** This signal driven by the TwisterT to grant PCI access to the South Bridge.
REQ[3:0]#	AD4, AE4, AD5, AC5	I	**PCI Master Request.** PCI master requests for PCI.
GNT[3:0]#	AE3, AF3, AF4, AB5	O	**PCI Master Grant.** Permission is given to the master to use PCI.
REQX#	AF2	I	**PCI Master Request.** PCI master request for PCI.
GNTX#	AE2	O	**PCI Master Grant.** Permission is given to the master to use PCI.
PCLK	AB15	I	**PCI Clock.** From external clock generator.
PCKRUN#	AF15	IO	**PCI Clock Run.** May be used to stop PCI clock.
INTA#	W5	O	**PCI Interrupt Out.** An asynchronous active low output used to signal an event that requires handling on behalf of the internal integrated graphics controller. If MA2 is strapped high at reset (clearing CR36[0]) no interrupt will be requested during PCI configuration. The default drive strength is 24 mA (other drive strengths may be selected via CR80[1-0]).
WSC#	AA11	O	**Write Snoop Complete.** Sideband PCI signal (used on the planar only in multiprocessor configurations) asserted to indicate that all snoop activity on the CPU bus initiated by the last PCI-to-DRAM write is complete and that it is safe to send an APIC interrupt message. Basically this signal is always active except when PCI master write data is not flushed.

LCD Panel Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
FPD[35:0]	(see pin table)	O	**Panel Data.** Internally pulled down during reset. 8mA is the default. 16mA is selected via SR3D[6]=1.
FPDET	AA16	I	**Panel Detect.** If SR30[1]=0, SR30[2] will read 1 if a Flat Panel is appropriately connected. Must be tied to GND if not used.
FPVS	G3	O	**Panel VSYNC.** Internally pulled down.
FPHS	G5	O	**Panel HSYNC.** Internally pulled down.
FPDE	H3	O	**Panel Data Enable.** Internally pulled down.
FPCLK	G4	O	**Panel Clock.** Internally pulled down during reset. 8mA is the default. 16mA may also be selected.
ENVDD	F1	O	**Enable VDD.** This signal is driven high to external logic to initiate a flat panel power up sequence.
ENVEE	H5	O	**Enable VEE.** This signal is driven high to a programmable time after ENVDD is driven high during a flat panel power up sequence.
FPGPIO	G1	I/O	**General Purpose Input / Output.**

TV Encoder Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
TVD[11:0]	(see pin table)	O	**TV Data.** Internally pulled down during reset
TVCLK	V4	I	**TV Clock.** Input clock from encoder. Internally pulled down.
TVCLKR	K5	O	**TV Return Clock.** Output clock to TV encoder. Internally pulled down.
TVVS	W3	O	**TV VSYNC.** Internally pulled down during reset
TVHS	V5	O	**TV HSYNC.** Internally pulled down during reset
TVBLK#	L1	O	**TV Blanking.** Internally pulled down during reset

CRT Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
RSET	E3	A	**Reference Resistor.** Tie to GNDRGB through an external 140Ω resistor to control the RAMDAC full-scale current value.
COMP	E4	A	**Compensation.** Tie to VCC25 through a 0.1 µF capacitor**.**
RED	C2	A	**Analog Red.** Analog red output to the CRT monitor.
BLUE	D2	A	**Analog Blue.** Analog blue output to the CRT monitor.
GREEN	D3	A	**Analog Green.** Analog green output to the CRT monitor.
HSYNC	E2	O	**Horizontal Sync.** Output to CRT.
VSYNC	E1	O	**Vertical Sync.** Output to CRT.

LVDS Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
Y[2:0]P	Y5, W4, AA3	A	**LVDS Data Positive Output.**
Y[2:0]M	AA5, Y4, AB3	A	**LVDS Data Negative Output.**
YCP	AB1	A	**LVDS Clock Positive Output.**
YCM	AC1	A	**LVDS Clock Negative Output.**
Z[2:0]P	AA4, AC3, AC2	A	**2nd LVDS Data Positive Output.**
Z[2:0]M	AB4, AD3, AD2	A	**2nd LVDS Data Negative Output.**
ZCP	AD1	A	**2nd LVDS Clock Positive Output.**
ZCM	AE1	A	**2nd LVDS Clock Negative Output.**

ZV-Port Interface			
Signal Name	**Pin #**	**IO**	**Signal Description**
ZVD[15:0]	(see pin table)	I	**ZV-Port Data Bus.** Video Input
ZVCLK	U3	I	**ZV-Port Clock.**
ZVHS	T3	I	**ZV-Port Horizontal Sync.**
ZVVS	U1	I	**ZV-Port Vertical Sync.**

Miscellaneous Functions			
Signal Name	**Pin #**	**I/O**	**Signal Description**
XIN	A2	I	**Reference Frequency Input.** An external 14.318 MHz crystal is connected between XOUT and this pin. Alternatively, an external oscillator can be connected.
XOUT	A3	O	**Crystal Output.** This pin drives the crystal via an internal oscillator. If an external oscillator is connected to XIN, this pin can be left unconnected.
SPCLK[2:1]	M2, F3	IO	**Serial Port Clocks.** These are the clocks for serial data transfer. SPCLK1 is typically used for I^2C communications. As an output, it is programmed via CRA0[0]. As an input, its status is read via CRA0[2]. In either case the serial port must be enabled by CRA0[4] = 1. SPCLK2 is typically used for DDC monitor communications. As an output, it is programmed via CRB1[0]. As an input, its status is read via CRB1[2]. The port is enabled via CRB1[4] = 1.
SPDAT[2:1]	M3, F2	IO	**Serial Port Data.** These are the data signals used for serial data transfer. SPDAT1 is typically used for I^2C communications. As an output, it is programmed via CRA0[1]. As an input, its status is read via CRA0[3]. In either case the serial port must be enabled by CRA0[4] = 1. SPDAT2 is typically used for DDC monitor communications. As an output, it is programmed via CRB1[1]. As an input, its status is read via CRB1[3]. The port is enabled via CRB1[4] = 1.
GPOUT	AA12	O	**General Purpose Output.** This pin reflects the state of SRD[0].
GOP0	C3	O	**General Output Port.** When SR1A[4] is cleared, this pin reflects the state of CR5C[0].
STPAGP#	C4	I	**Stop AGP.** Power management for internal AGP.
AGPBUSY#	B4	I/O	**AGP Busy.** Power management for internal AGP.
STANDBY	F4	I	**Standby.** Used to put the integrated graphics controller in the standby state.
SUSPEND	F5	I	**Suspend.** Used to put the integrated graphics controller in the suspend state.
SUSST#	AC22	I	**Suspend Status.** For implementation of the Suspend-to-DRAM feature. Connect to an external pullup to disable.

Clock / Reset Control

Signal Name	Pin #	I/O	Signal Description
HCLK	G22	I	**Host Clock.** This pin receives the host CPU clock (66 / 100 / 133 MHz). This clock is used by all TwisterT logic that is in the host CPU domain.
PCLK	AB15	I	**PCI Clock.** This pin receives a buffered host clock divided-by-2, 3, or 4 to create 33 MHz. This clock is used by all of the TwisterT logic that is in the PCI clock domain. This clock input must be 33 MHz maximum to comply with PCI specification requirements and must be synchronous with the host CPU clock, HCLK, with an HCLK:PCLK frequency ratio of 2:1, 3:1, or 4:1 as shown in the table below. The host CPU clock must lead the PCI clock by 2.0 ± 1.0 nsec. Typical Clock Frequency Combinations Rx68[1:0] / Mode / Host Clock / AGP Clock / PCI Clock 00 / 2x / 66 MHz / 66 MHz / 33 MHz 01 / 3x / 100 MHz / 66 MHz / 33 MHz 10 / 4x / 133 MHz / 66 MHz / 33 MHz 11 / Reserved
MCLK	J22	O	**DRAM Clock.** Output from internal clock generator to the external clock buffer.
MCLKF	K22	I	**DRAM Clock Feedback.** Input from the external clock buffer.
RESET#	AE15	I	**Reset.** Input from South Bridge chip. When asserted, this signal resets the TwisterT and sets all register bits to the default value. The rising edge of this signal is used to sample all power-up strap options
PWROK	AD14	I	**Power OK.** Connect to South Bridge and Power Good circuitry.
CPURST#	A19	O	**CPU Reset.** GTL output level.
CPURSTD#	E22	O	**CPU Reset Delayed.** Reset output delayed by 2T.

Power, Ground, and Test			
Signal Name	**Pin #**	**I/O**	**Signal Description**
VTT	(see pin list)	P	**Power** for **CPU Interface Logic.** 1.5V for "Coppermine" CPUs, 1.25V for Pentium III-M "Tualatin" CPUs. (Refer to CPU specifications for voltage requirements)
VCC3	(see pin list)	P	**Power** for **I/O Interface Logic** (3.3V ±5%).
VCC25	(see pin list)	P	**Power** for **Internal Logic** (2.5V ±5%).
VSUS25	AA22	P	**Suspend Power** (2.5V ±5%).
VCCRGB	D1	P	**Power for CRT RGB Outputs** (2.5V ±5%).
VCCA	H21, H22	P	**Power for Analog** (2.5V ±5%)
VCCDAC	C1	P	**Power for DAC Digital Logic** (2.5V ±5%)
VCCPLL1	B3	P	**Power for Graphics Controller PLL1** (2.5V ±5%).
VCCPLL2	A5	P	**Power for Graphics Controller PLL2** (2.5V ±5%).
VCCLPLL	AB2	P	**Analog Power for LVDS PLL** (2.5V ±5%).
VCCLVDS	W1, W2	P	**Analog Power for LVDS** (3.3V ±5%).
VDDD	Y2	P	**Digital Power for LVDS** (2.5V ±5%).
GND	(see pin table)	P	**Ground**
GNDA	L21, L22	P	**Ground for North Bridge Host CPU Clock Circuitry.** Connect to main ground plain through a ferrite bead.
GNDRGB	A1	P	**Connection point for RGB load resistors**
GNDDAC	B1	P	**Ground for DAC Analog Circuitry**
GNDPLL1	A4	P	**Ground for PLL1**
GNDPLL2	B5	P	**Ground for PLL2**
GNDALPLL	Y3	P	**Ground for LVDS PLL**
GNDALVDS	Y1, AA1	P	**Ground for LVDS Analog Circuitry**
GNDLVDS	AA2	P	**Ground for LVDS Digital Circuitry**
GTLREF	E12, E21	P	**CPU Interface GTL+ Voltage Reference.** 2/3 VTT ±2%
PLLTST	K24	I	**PLL Test Input.** Pull down with 4.7K resistor for normal operation.
BISTIN	F15	I	**BIST In.** This pin is used for testing and must be left unconnected or tied high on all board designs.
DFTIN	F11	I	**DFT In.** This pin is used for testing and must be left unconnected or tied high on all board designs.
NC	U6, V22, W22, AB22	-	**No Connect.** Reserved for future use. Do not connect.

REGISTERS

Register Overview

The following tables summarize the configuration and I/O registers of the TwisterT. These tables also document the power-on default value ("Default") and access type ("Acc") for each register. Access type definitions used are RW (Read/Write), RO (Read/Only), "—" for reserved / used (essentially the same as RO), and RWC (or just WC) (Read / Write 1's to Clear individual bits). Registers indicated as RW may have some read/only bits that always read back a fixed value (usually 0 if unused); registers designated as RWC or WC may have some read-only or read write bits (see individual register descriptions following these tables for details). All offset and default values are shown in hexadecimal unless otherwise indicated.

The graphics registers are described in a separate document.

Table 5. VT8606 / TwisterT Registers

TwisterT I/O Ports

Port #	I/O Port	Default	Acc
22	PCI / AGP Arbiter Disable	00	RW
CFB-8	Configuration Address	0000 0000	RW
CFF-C	Configuration Data	0000 0000	RW

TwisterT Device 0 Registers - Host Bridge

Header Registers

Offset	Configuration Space Header	Default	Acc
1-0	Vendor ID	**1106**	RO
3-2	Device ID	**0605**	RO
5-4	Command	**0006**	**RW**
7-6	Status	**0210**	**WC**
8	Revision ID	**0n**	RO
9	Program Interface	00	RO
A	Sub Class Code	00	RO
B	Base Class Code	**06**	RO
C	-reserved-	00	—
D	Latency Timer	00	**RW**
E	Header Type	00	RO
F	Built In Self Test (BIST)	00	RO
13-10	Graphics Aperture Base	**0000 0008**	**RW**
14-2B	-reserved-	00	—
2D-2C	Subsystem Vendor ID	0000	**W1**
2F-2E	Subsystem ID	0000	**W1**
30-33	-reserved-	00	—
37-34	Capability Pointer	**0000 0080**	RO
38-3F	-reserved-	00	—

Device-Specific Registers

Offset	Host CPU Protocol Control	Default	Acc
40-4F	-reserved-	00	—
50	Request Phase Control	00	RW
51	Response Phase Control	00	RW
52	Dynamic Defer Timer	**10**	RW
53	Miscellaneous 1	**03**	RW
54	Miscellaneous 2	00	RW
55-57	-reserved-	00	—

Offset	DRAM Control	Default	Acc
59-58	MA Map Type	0000	RW
5F-5A	DRAM Row Ending Address:		
5A	Bank 0 Ending (HA[31:24])	**01**	RW
5B	Bank 1 Ending (HA[31:24])	**01**	RW
5C	Bank 2 Ending (HA[31:24])	**01**	RW
5D	Bank 3 Ending (HA[31:24])	**01**	RW
5E	Bank 4 Ending (HA[31:24])	**01**	RW
5F	Bank 5 Ending (HA[31:24])	**01**	RW
60	DRAM Type	**undefined**	RW
61	ROM Shadow Control C0000-CFFFF	00	RW
62	ROM Shadow Control D0000-DFFFF	00	RW
63	ROM Shadow Control E0000-FFFFF	00	RW
64	DRAM Timing for Banks 0,1	**EC**	RW
65	DRAM Timing for Banks 2,3	**EC**	RW
66	DRAM Timing for Banks 4,5	**EC**	RW
67	-reserved-	00	—
68	DRAM Control	00	RW
69	DRAM Clock Control	00	RW
6A	DRAM Refresh Counter	00	RW
6B	DRAM Arbitration Control	**01**	RW
6C	SDRAM Control	00	RW
6D	DRAM Control Drive Strength	00	RW
6E-6F	-reserved-	00	RW

Device-Specific Registers (continued)

Offset	PCI Bus Control	Default	Acc
70	PCI Buffer Control	00	RW
71	CPU to PCI Flow Control 1	00	RW
72	CPU to PCI Flow Control 2	00	**WC**
73	PCI Master Control 1	00	RW
74	PCI Master Control 2	00	RW
75	PCI Arbitration 1	00	RW
76	PCI Arbitration 2	00	RW
77	Chip Test (do not program)	00	RW
78	PMU Control	00	RW
79	PMU Control	00	RW
7A	Miscellaneous Control 1	00	RW
7B	Miscellaneous Control 2	**02**	RW
7C-7D	-reserved-	00	—
7E-7F	PLL Test Mode (do not program)	00	RW

Offset	GART/TLB Control	Default	Acc
83-80	GART/TLB Control	0000 0000	RW
84	Graphics Aperture Size	00	RW
85-87	-reserved-	00	—
8B-88	Gr. Aperture TLB Base Register Base	0000 0000	RW
8C-9F	-reserved-	00	—

Offset	AGP Control	Default	Acc
A0	AGP ID	**02**	RO
A1	AGP Next Item Pointer	00	RO
A2	AGP Specification Revision	**20**	RO
A3	-reserved-	00	—
A7-A4	AGP Status	**1F00 0207**	RO
AB-A8	AGP Command	0000 0000	**RW**
AC	AGP Control	00	**RW**
AD	AGP Latency Timer	**02**	RW
AE	AGP Miscellaneous Control	00	RW
AF	-reserved-	00	—
B0	AGP Compensation Control / Status	**8x**	RW
B1	AGP Drive Strength	**63**	RW
B2	AGP Pad Drive & Delay Control	00	RW
B3-BF	-reserved-	00	—

Offset	Power Mgt. &Misc. Control	Default	Acc
C0	Power Management Capability	**01**	RO
C1	Power Management New Pointer	00	RO
C2	Power Management Capabilities I	02	RO
C3	Power Management Capabilities II	00	RO
C4	Power Management Control/Status	00	RW
C5	Power Management Status	00	RO
C6	PCI-to-PCI Bridge Support Extension	00	RO
C7	Power Management Data	00	RO
C8-DF	-reserved-	00	—
E0	Miscellaneous Control	00	RW
E1-EF	-reserved-	00	—
F7-F0	BIOS Scratch Registers	00	RW
F8	DRAM Arbitration Timer Control	00	RW
F9	VGA Timer Control	00	RW
FA	CPU Direct Access FB Address	00	RW
FB	Frame Buffer Size	00	RW
FC	Back-Door Control 1	00	RW
FD	Back-Door Control 2	00	RW
FF-FE	Back-Door Device ID	0000	RW

TwisterT Device 1 Registers - PCI-to-PCI Bridge

Header Registers

Offset	Configuration Space Header	Default	Acc
1-0	Vendor ID	**1106**	RO
3-2	Device ID	**8605**	RO
5-4	Command	**0007**	**RW**
7-6	Status	**0230**	**WC**
8	Revision ID	**nn**	RO
9	Program Interface	00	RO
A	Sub Class Code	**04**	RO
B	Base Class Code	**06**	RO
C	-reserved-	00	—
D	Latency Timer	00	RO
E	Header Type	**01**	RO
F	Built In Self Test (BIST)	00	RO
10-17	-reserved-	00	—
18	Primary Bus Number	00	**RW**
19	Secondary Bus Number	00	**RW**
1A	Subordinate Bus Number	00	**RW**
1B	Secondary Latency Timer	00	RO
1C	I/O Base	**F0**	**RW**
1D	I/O Limit	00	**RW**
1F-1E	Secondary Status	0000	RO
21-20	Memory Base	**FFF0**	**RW**
23-22	Memory Limit (Inclusive)	0000	**RW**
25-24	Prefetchable Memory Base	**FFF0**	**RW**
27-26	Prefetchable Memory Limit	0000	**RW**
28-33	-reserved-	00	—
34	Capability Pointer	**80**	RO
35-3D	-reserved-	00	—
3F-3E	PCI-to-PCI Bridge Control	00	**RW**

Device-Specific Registers

Offset	AGP Bus Control	Default	Acc
40	CPU-to-AGP Flow Control 1	00	RW
41	CPU-to-AGP Flow Control 2	00	RW
42	AGP Master Control	00	RW
43	AGP Master Latency Timer	00	RW
44	Back-Door Register Control	00	RW
45	Fast Write Control	**72**	RW
47-46	PCI-to-PCI Bridge Device ID	0000	RW
48-7F	-reserved-	00	—
80	Capability ID	**01**	**RO**
81	Next Pointer	00	**RO**
82	Power Management Capabilities 1	**02**	**RO**
83	Power Management Capabilities 2	00	**RO**
84	Power Management Control / Status	00	RW
85	Power Management Status	00	**RO**
86	PCI-PCI Bridge Support Extensions	00	**RO**
87	Power Management Data	00	**RO**
88-FF	-reserved-	00	—

Miscellaneous I/O

One I/O port is defined in the TwisterT: Port 22.

Port 22 – PCI / AGP Arbiter Disable ..... RW

7-2 Reserved ..... always reads 0

1 AGP Arbiter Disable
- 0 Respond to GREQ# signal .....default
- 1 Do not respond to GREQ# signal

0 PCI Arbiter Disable
- 0 Respond to all REQ# signals .....default
- 1 Do not respond to any REQ# signals, including PREQ#

This port can be enabled for read/write access by setting bit-7 of Device 0 Configuration Register 78.

Configuration Space I/O

All registers in the TwisterT (listed above) are addressed via the following configuration mechanism:

Mechanism #1

These ports respond only to double-word accesses. Byte or word accesses will be passed on unchanged.

Port CFB-CF8 - Configuration Address..... RW

31 Configuration Space Enable
- 0 Disabled..... default
- 1 Convert configuration data port writes to configuration cycles on the PCI bus

30-24 Reserved .....always reads 0

23-16 PCI Bus Number
Used to choose a specific PCI bus in the system

15-11 Device Number
Used to choose a specific device in the system (devices 0 and 1 are defined for the TwisterT)

10-8 Function Number
Used to choose a specific function if the selected device supports multiple functions (only function 0 is defined for the TwisterT).

7-2 Register Number (also called the "Offset")
Used to select a specific DWORD in the TwisterT configuration space

1-0 Fixed .....always reads 0

Port CFF-CFC - Configuration Data..... RW

Refer to PCI Bus Specification Version 2.2 for further details on operation of the above configuration registers.

Device 0 Register Descriptions

Device 0 Header Registers - Host Bridge

All registers are located in PCI configuration space. They should be programmed using PCI configuration mechanism 1 through CF8 / CFC with bus number, function number, and device number equal to zero.

Device 0 Offset 1-0 - Vendor ID (1106h) .....RO

15-0 ID Code (reads 1106h to identify VIA Technologies)

Device 0 Offset 3-2 - Device ID (0605h).....RO

15-0 ID Code (reads 0605h to identify the TwisterT)

Device 0 Offset 5-4 –Command (0006h).....RW

15-10 Reserved ..... always reads 0

9 Fast Back-to-Back Cycle Enable ..... RO
- 0 Fast back-to-back transactions only allowed to the same agent.....default
- 1 Fast back-to-back transactions allowed to different agents

8 SERR# Enable..... RO
- 0 SERR# driver disabled.....default
- 1 SERR# driver enabled

(SERR# is used to report parity errors if bit-6 is set).

7 Address / Data Stepping..... RO
- 0 Device never does stepping.....default
- 1 Device always does stepping

6 Parity Error Response.....**RW**
- 0 Ignore parity errors & continue.....default
- 1 Take normal action on detected parity errors

5 VGA Palette Snoop..... RO
- 0 Treat palette accesses normally.....default
- 1 Don't respond to palette accesses on PCI bus

4 Memory Write and Invalidate Command ..... RO
- 0 Bus masters must use Mem Write.....default
- 1 Bus masters may generate Mem Write & Inval

3 Special Cycle Monitoring..... RO
- 0 Does not monitor special cycles.....default
- 1 Monitors special cycles

2 PCI Bus Master.....
- 0 Never behaves as a bus master
- 1 Can behave as a bus master.....default

1 Memory Space..... RO
- 0 Does not respond to memory space
- 1 Responds to memory space.....default

0 I/O Space ..... RO
- 0 Does not respond to I/O space .....default
- 1 Responds to I/O space

Device 0 Offset 7-6 – Status (0210h).....RWC

15 Detected Parity Error
- 0 No parity error detected..... default
- 1 Error detected in either address or data phase. This bit is set even if error response is disabled (command register bit-6). .....write one to clear

14 Signaled System Error (SERR# Asserted)
.....always reads 0

13 Signaled Master Abort
- 0 No abort received ..... default
- 1 Transaction aborted by the master .....
.....write one to clear

12 Received Target Abort
- 0 No abort received ..... default
- 1 Transaction aborted by the target .....
.....write one to clear

11 Signaled Target Abort .....always reads 0
- 0 Target Abort never signaled

10-9 DEVSEL# Timing
- 00 Fast
- 01 Medium .....always reads 01
- 10 Slow
- 11 Reserved

8 Data Parity Error Detected
- 0 No data parity error detected ..... default
- 1 Error detected in data phase. Set only if error response enabled via command bit-6 = 1 and TwisterT was initiator of the operation in which the error occurred
. .....write one to clear

7 Fast Back-to-Back Capable.....always reads 0

6 User Definable Features .....always reads 0

5 66MHz Capable.....always reads 0

4 Supports New Capability list.....always reads 1

3-0 Reserved .....always reads 0

Device 0 Offset 8 - Revision ID (0nh)..... RO

7-0 Chip Revision Code.....always reads 0nh

Device 0 Offset 9 - Programming Interface (00h)..... RO

7-0 Interface Identifier.....always reads 00h

RO

Device 0 Offset A - Sub Class Code (00h)..... RO

7-0 Sub Class Code.....reads 00 to indicate Host Bridge

Device 0 Offset B - Base Class Code (06h)..... RO

7-0 Base Class Code.. reads 06 to indicate Bridge Device

Device 0 Offset D - Latency Timer (00h)..... RW

Specifies the latency timer value in PCI bus clocks.

7-3 Guaranteed Time Slice for CPU .....default=0

2-0 Reserved (fixed granularity of 8 clks).. always read 0

Bits 2-1 are writeable but read 0 for PCI specification compatibility. The programmed value may be read back in Offset 75 bits 5-4 (PCI Arbitration 1).

Device 0 Host Bridge Header Registers (continued)

Device 0 Offset E - Header Type (00h).....RO

7-0 Header Type Code ..... reads 00: single function

Device 0 Offset F - Built In Self Test (BIST) (00h).....RO

7 BIST Supported .....reads 0: no supported functions
6-0 Reserved ..... always reads 0

Device 0 Offset 13-10 - Graphics Aperture Base (00000008h) .....RW

31-28 Upper Programmable Base Address Bits ..... def=0
27-20 Lower Programmable Base Address Bits ..... def=0
These bits behave as if hardwired to 0 if the corresponding Graphics Aperture Size register bit (Device 0 Offset 84h) is 0.

27	26	25	24	23	22	21	20	(This Register)
7	6	5	4	3	2	1	0	(Gr Aper Size)
RW	RW	RW	RW	RW	RW	RW	RW	1M
RW	RW	RW	RW	RW	RW	RW	0	2M
RW	RW	RW	RW	RW	RW	0	0	4M
RW	RW	RW	RW	RW	0	0	0	8M
RW	RW	RW	RW	0	0	0	0	16M
RW	RW	RW	0	0	0	0	0	32M
RW	RW	0	0	0	0	0	0	64M
RW	0	0	0	0	0	0	0	128M
0	0	0	0	0	0	0	0	256M

19-0 Reserved ..... always reads 00008
Note: The locations in the address range defined by this register are prefetchable.

Device 0 Offset 2D-2C – Subsystem Vendor ID (0000h)R/W1

15-0 Subsystem Vendor ID..... default = 0
This register may be written once and is then read only.

Device 0 Offset 2F-2E – Subsystem ID (0000h) R/W1

15-0 Subsystem ID..... default = 0
This register may be written once and is then read only.

Device 0 Offset 37-34 - Capability Pointer (00000080h) .RO

Contains an offset from the start of configuration space.

31-0 AGP Capability List Pointer..... always reads 80h

Device 0 Configuration Registers - Host Bridge

These registers are normally programmed once at system initialization time.

Host CPU Control

Device 0 Offset 50 – Request Phase Control (00h)..... RW

7 CPU Hardwired IOQ (In Order Queue) Size
Default per strap on pin MA11. During reset. This register can be written 0 to restrict the chip to one level of IOQ.
0 1-Level
1 4-Level

6 Read-Around-Write
0 Disable..... default
1 Enable

5 Reserved .....always reads 0

4 Defer Retry When HLOCK Active
0 Disable..... default
1 Enable
Note: always set this bit to 1

3-1 Reserved .....always reads 0

0 CPU / PCI Master Read DRAM Timing
0 Start DRAM read after snoop complete ..... def
1 Start DRAM read before snoop complete

Device 0 Offset 51 – Response Phase Control (00h).....RW

7 CPU Read DRAM 0ws for Back-to-Back Read Transactions
- 0 Disable .....default
- 1 Enable

Setting this bit enables maximum read performance by allowing continuous 0 wait state reads for pipelined line reads. If this bit is not set, there will be at least 1T idle time between read transactions.

6 CPU Write DRAM 0ws for Back-to-Back Write Transactions
- 0 Disable .....default
- 1 Enable

Setting this bit enables maximum write performance by allowing continuous 0 wait state writes for pipelined line writes ands sustained 3T single writes. If this bit is not set, there will be at least 1T idle time between write transactions.

5 Reserved ..... always reads 0

4 Fast Response (HIT/HITM sample 1T earlier)
- 0 Disable .....default
- 1 Enable

3 Non-Posted IOW
- 0 Disable .....default
- 1 Enable

2 CPU Read DRAM Prefetch Buffer Depth
- 0 1-level prefetch buffer.....default
- 1 4-level prefetch buffer

1 CPU-to-DRAM Post-Write Buffer Depth
- 0 1-level post-write buffer.....default
- 1 4-level post-write buffer

0 Concurrent PCI Master / Host Operation
- 0 Disable – the CPU bus will be occupied (BPRI asserted) during the entire PCI operation.....def
- 1 Enable – the CPU bus is only requested before ADS# assertion

Device 0 Offset 52 – Dynamic Defer Timer (10h).....RW

7 GTL I/O Buffer Pullup.....default = MA6 Strap
- 0 Disable
- 1 Enable

The default value of this bit is determined by a strap on the MA6 pin during reset.

6 RAW Write Retire Policy (After 2 Writes)
- 0 Disable .....default
- 1 Enable

5 Quick Start Select .....default = MA10 Strap
- 0 Disable .....default
- 1 Enable

The default value of this bit is determined by a strap on the MA10 pin during reset.

4-0 Snoop Stall Count
- 00 Disable dynamic defer
- 01-1F Snoop stall count ..... default = 10h

Device 0 Offset 53 – Miscellaneous 1 (03h)..... RW

7 HREQ
- 0 Disable..... default
- 1 Enable

6 SDRAM Frequency Higher Than CPU Front Side Bus Frequency
- 0 Disable..... default
- 1 Enable

Setting this bit enables the DRAM subsystem to run at a higher frequency than the CPU FSB frequency. When setting this bit, register bit Rx69[6] must also be set and only SDRAM type DIMM modules may be used.

5 PCI/AGP Master-to-CPU / CPU-to-PCI/AGP Slave Concurrency
- 0 Disable..... default
- 1 Enable

4 HPRI Function
- 0 Disable..... default
- 1 Enable

3 P6Lock Function
- 0 Disable..... default
- 1 Enable

2 Line Write / Write Back Without Implicit Write Back Data
- 0 Disable..... default
- 1 Enable

1 PCI Master Pipeline Access
- 0 Disable
- 1 Enable ..... default

0 Reserved .....Always reads 0

Device 0 Offset 54 – Miscellaneous 2 (00h)..... RW

7-3 Reserved .....always reads 0

2 Zero Length Write
- 0 Disable..... default
- 1 Enable (this bit must be set to 1)

1 Invalidate CPU Internal Cache on PCI Master Access
- 0 Disable..... default
- 1 Enable

0 1-1-1-1 PMRDY for PCI Master Access
- 0 Disable..... default
- 1 Enable

DRAM Control

These registers are normally set at system initialization time and not accessed after that during normal system operation. Some of these registers, however, may need to be programmed using specific sequences during power-up initialization to properly detect the type and size of installed memory (refer to the VIA Technologies TwisterT BIOS porting guide for details).

Table 6. System Memory Map

Space	Start	Size	Address Range	Comment
DOS	0	640K	00000000-0009FFFF	Cacheable
VGA	640K	128K	000A0000-000BFFFF	Used for SMM
BIOS	768K	16K	000C0000-000C3FFF	Shadow Ctrl 1
BIOS	784K	16K	000C4000-000C7FFF	Shadow Ctrl 1
BIOS	800K	16K	000C8000-000CBFFF	Shadow Ctrl 1
BIOS	816K	16K	000CC000-000CFFFF	Shadow Ctrl 1
BIOS	832K	16K	000D0000-000D3FFF	Shadow Ctrl 2
BIOS	848K	16K	000D4000-000D7FFF	Shadow Ctrl 2
BIOS	864K	16K	000D8000-000DBFFF	Shadow Ctrl 2
BIOS	880K	16K	000DC000-000DFFFF	Shadow Ctrl 2
BIOS	896K	64K	000E0000-000EFFFF	Shadow Ctrl 3
BIOS	960K	64K	000F0000-000FFFFF	Shadow Ctrl 3
Sys Bus Init	1MB D Top 4G-64K	— 64K	00100000-DRAM Top DRAM Top-FFFEFFFF FFFEFFFF-FFFFFFFF	Can have hole 000Fxxxx alias

Device 0 Offset 59-58 - DRAM MA Map Type (0000h). RW

15-13 **Bank 5/4 MA Map Type (see below)**

12 Bank 5/4 Virtual Channel Enable ..... def=0

11-8 Reserved ..... def=0

7-5 **Bank 0/1 MA Map Type (SDRAM)**

- 000 16Mbit SDRAM.....default
- 001 -reserved-
- 01x -reserved-
- 100 64Mbit / 128Mbit SDRAM
- 101 256Mbit SDRAM x32
- 110 256Mbit SDRAM x16
- 111 256Mbit SDRAM x8 or x4

4 Bank 1/0 Virtual Channel Enable ..... def=0

3-1 **Bank 3/2 MA Map Type (see above)**

0 Bank 3/2 Virtual Channel Enable ..... def=0

Device 0 Offset 5F-5A – DRAM Row Ending Address:

Offset 5A – Bank 0 Ending (HA[31:24]) (01h)..... RW

Offset 5B – Bank 1 Ending (HA[31:24]) (01h)..... RW

Offset 5C – Bank 2 Ending (HA[31:24]) (01h)..... RW

Offset 5D – Bank 3 Ending (HA[31:24]) (01h)..... RW

Offset 5E – Bank 4 Ending (HA[31:24]) (01h)..... RW

Offset 5F – Bank 5 Ending (HA[31:24]) (01h)..... RW

Note : BIOS is required to fill the ending address registers for all banks even if no memory is populated. The endings have to be in incremental order.

Device 0 Offset 60 – DRAM Type ..... RW

7- 6 **Reserved** .....always reads 0

5-4 **DRAM Type for Bank 5/4** ..... default undefined

- 00 -reserved-
- 01 -reserved-
- 10 -reserved-
- 11 SDRAM

3-2 **DRAM Type for Bank 3/2** ..... default undefined

1-0 **DRAM Type for Bank 1/0** ..... default undefined

Table 7. Memory Address Mapping Table

SDRAM

MA:	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
16Mb (0xx)				**11** *11*	22 PC	21 24	20 23	19 10	18 9	17 8	16 7	15 6	14 5	13 4	12 3	11x10, 11x9, 11x8
64/128Mb (100) 2/4 bank		**24** ***27/ 24***	*13* *13*	*12* *12*	22 PC	21 *26*	20 *25*	19 10	18 9	17 8	16 7	15 6	14 5	*11* 4	*23* 3	x4: 14x10 x8: 14x9
256Mb (101) 2/4B	**25**	*24* *28*	*13* *13*	*12* *12*	22 PC	21 *26*	20 *25*	19 10	18 9	17 8	16 7	15 6	14 5	*11* 4	*23* 3	x32: 14x8
256Mb (110) 2/4B	**26**	*24* *28*	*13* *13*	*12* *12*	22 PC	21 *26*	20 *25*	19 10	18 9	17 8	16 7	15 6	14 5	*11* 4	*23* 3	x16: 14x9
256Mb (111) 2/4B	**27**	*24* *28*	*13* *13*	*12* *12*	22 PC	21 *26*	20 *25*	19 10	18 9	17 8	16 7	15 6	14 5	*11* 4	*23* 3	x8: 14x10 x4: 14x11

"PC" = "Precharge Control" (refer to SDRAM specifications)

Device 0 Offset 61 - Shadow RAM Control 1 (00h).....RW

7-6 CC000h-CFFFFh
- 00 Read/write disable.....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

5-4 C8000h-CBFFFh
- 00 Read/write disable.....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

3-2 C4000h-C7FFFh
- 00 Read/write disable.....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

1-0 C0000h-C3FFFh
- 00 Read/write disable.....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

Device 0 Offset 62 - Shadow RAM Control 2 (00h).....RW

7-6 DC000h-DFFFFh
- 00 Read/write disable.....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

5-4 D8000h-DBFFFh
- 00 Read/write disable.....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

3-2 D4000h-D7FFFh
- 00 Read/write disable.....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

1-0 D0000h-D3FFFh
- 00 Read/write disable.....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

Device 0 Offset 63 - Shadow RAM Control 3 (00h)..... RW

7-6 E0000h-EFFFFh
- 00 Read/write disable ..... default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

5-4 F0000h-FFFFFh
- 00 Read/write disable ..... default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

3-2 Memory Hole
- 00 None ..... default
- 01 512K-640K
- 10 15M-16M (1M)
- 11 14M-16M (2M)

1 A000/B000 SMRAM Direct Access
- 0 Enable..... default
- 1 Disable

0 A000/B000 DRAM Access
- 0 Disable..... default
- 1 Enable

SMI Mapping Control

Bits	SMM		Non-SMM	
1-0	Code	Data	Code	Data
00	DRAM	DRAM	PCI	PCI
01	DRAM	DRAM	DRAM	DRAM
10	DRAM	PCI	PCI	PCI
11	DRAM	DRAM	DRAM	DRAM

Device 0 Offset 64 - DRAM Timing for Banks 0,1 (ECh)RW
Device 0 Offset 65 - DRAM Timing for Banks 2,3 (ECh)RW
Device 0 Offset 66 - DRAM Timing for Banks 4,5 (ECh)RW

SDRAM Settings for Registers 66-64

7 Precharge Command to Active Command Period
- 0 TRP = 2T
- 1 TRP = 3T .....default

6 Active Command to Precharge Command Period
- 0 TRAS = 5T
- 1 TRAS = 6T .....default

5-4 CAS Latency
- 00 1T
- 01 2T
- 10 3T .....default
- 11 reserved

3 DIMM Type
- 0 Standard
- 1 Registered .....default

2 ACTIVE Command to CMD Command Period
- 0 2T
- 1 3T .....default

1-0 Bank Interleave
- 00 No Interleave.....default
- 01 2-way
- 10 4-way
- 11 Reserved

Device 0 Offset 68 - DRAM Control (00h) .....RW

7 SDRAM Open Page Control
- 0 Always precharge SDRAM banks .....default
- 1 SDRAM banks remain active

6 Bank Page Control
- 0 Allow only pages of the same bank active..def.
- 1 Allow pages of different banks to be active

5-4 Reserved ..... always reads 0

3 EDO Test Mode
- 0 Disable .....default
- 1 Enable

2 Burst Refresh
- 0 Disable .....default
- 1 Enable (burst 4 times)

1-0 System Frequency Divider ..... RO

Bit 1 is latched from MA8 and bit 0 is latched from MA12 at the rising edge of RESET#.
- 00 CPU Frequency = 66 MHz
- 01 CPU Frequency = 100 MHz
- 10 Autodetect
- 11 CPU Frequency = 133 MHz

Note: See also Rx69[7-6]

Device 0 Offset 69 – DRAM Clock Select (00h) ..... RW

7 CPU Operating Frequency Faster Than DRAM
- 0 CPU Same As or Equal to DRAM ..... default
- 1 CPU Faster Than DRAM by 33 MHz

6 DRAM Operating Frequency Faster Than CPU
- 0 DRAM Same As or Equal to CPU ..... default
- 1 DRAM Faster Than CPU by 33 MHz

Rx68[1-0]	Rx69[7-6]	Rx69[0]	CPU / DRAM
00	00	0	66 / 66 (def)
00	01	0	66 / 100†
00	01	**1**	66 / 133†
01	10	0	100 / 66
01	00	0	100 / 100
01	01	0	100 / 133†
10	10	0	133 / 100
10	00	0	133 / 133

†Rx53[6] must also be set to 1 for DRAM > CPU

5 256Mbit DRAM Support
- 0 Disable (pin AB22 is DCLKRD)..... default
- 1 Enable (pin AB22 is MAA14)

4 DRAM Controller Command Register Output
- 0 Disable..... default
- 1 Enable

3 Fast DRAM Precharge for Different Bank
- 0 Disable..... default
- 1 Enable

2 DRAM 4K Page Enable (64Mbit DRAM Only)
- 0 Disable..... default
- 1 Enable

1 DIMM Type
- 0 Unbuffered ..... default
- 1 Registered

0 CPU / DRAM 66 / 133MHz Support†
- 0 Disable..... default
- 1 Enable (see also bits 7-6)

†Rx53[6] must also be set to 1 for DRAM > CPU

Device 0 Offset 6A - Refresh Counter (00h) ..... RW

7-0 Refresh Counter (in units of 16 MCLKs)
- 00 DRAM Refresh Disabled .....default
- 01 32 MCLKs
- 02 48 MCLKs
- 03 64 MCLKs
- 04 80 MCLKs
- 05 96 MCLKs
- … …

The programmed value is the desired number of 16-MCLK units minus one.

Device 0 Offset 6B - DRAM Arbitration Control (01h). RW

7-6 Arbitration Parking Policy
- 00 Park at last bus owner .....default
- 01 Park at CPU side
- 10 Park at AGP side
- 11 Reserved

5 Fast Read to Write turn-around
- 0 Disable .....default
- 1 Enable

4 Memory Module Configuration ..... RO
- 0 Normal Operation .....default
- 1 Unused Outputs Tristated (CSB#, DQMB, CKE, MA, DCLKO)

This bit is latched from MA7 at the rising edge of RESET#.

3 MD Bus Second Level Strength Control
- 0 Normal slew rate control.....default
- 1 More slew rate control

2 CAS Bus Second Level Strength Control
- 0 Normal slew rate control.....default
- 1 More slew rate control

1 AGP Pad Slew Rate Control
- 0 Disable .....default
- 1 Enable

0 Multi-Page Open
- 0 Disable (page registers marked invalid and no page register update which causes non page-mode operation)
- 1 Enable .....default

Device 0 Offset 6C - SDRAM Control (00h) ..... RW

7-5 Reserved .....always reads 0

4 CKE Configuration
- 0 Rx6B[4]=0 CSA = CSA, CSB = CSB, CKE0=CKE0, CKE1 = CKE1
- x Rx6B[4]=1 CSA = CSA, CSB = Float, CSB = Float, MA = Float, CKE0 = CKE0, CKE1 = CKE0
- 1 Rx6B[4]=0 CSA = CSA, CSB = CSB, CKE3-2 = CSA7-6, CKE5-4 = CSB7-6, CKE1 = GCKE (Global CKE), CKE0 = FENA (FET Enable)

3 Fast TLB Lookup
- 0 Disable..... default
- 1 Enable

2-0 SDRAM Operation Mode Select
- 000 Normal SDRAM Mode ..... default
- 001 NOP Command Enable
- 010 All-Banks-Precharge Command Enable (CPU-to-DRAM cycles are converted to All-Banks-Precharge commands).
- 011 MSR Enable
  CPU-to-DRAM cycles are converted to commands and the commands are driven on MA[14:0]. The BIOS selects an appropriate host address for each row of memory such that the right commands are generated on MA[14:0].
- 100 CBR Cycle Enable (if this code is selected, CAS-before-RAS refresh is used; if it is not selected, RAS-Only refresh is used)
- 101 Reserved
- 11x Reserved

Device 0 Offset 6D - DRAM Drive Strength (00h) .....RW

7 Reserved

6-5 Delay DRAM Read Latch
- 00 No Delay .....default
- 01 0.5 ns
- 10 1.0 ns
- 11 1.5 ns

4 Memory Data Drive (MD, MECC)
- 0 6 mA .....default
- 1 8 mA

3 SDRAM Command Drive (SRAS#, SCAS#, SWE#)
- 0 16mA .....default
- 1 24mA

2 Memory Address Drive (MA, WE#)
- 0 16mA .....default
- 1 24mA

1 CAS# Drive
- 0 8 mA .....default
- 1 12 mA

0 RAS# Drive
- 0 16mA .....default
- 1 24mA

Device 0 Offset 6E - Reserved (00h)..... RW

Device 0 Offset 6F - Reserved (00h)..... RW

PCI Bus Control

These registers are normally programmed once at system initialization time.

Device 0 Offset 70 - PCI Buffer Control (00h).....RW

7 CPU to PCI Post-Write
- 0 Disable .....default
- 1 Enable

6 PCI Master to DRAM Post-Write
- 0 Disable .....default
- 1 Enable

5 Reserved ..... always reads 0

4 PCI Master to DRAM Prefetch
- 0 Enable .....default
- 1 Disable

3 Enhance CPU-to-PCI Write
- 0 Normal operation .....default
- 1 Reduce 1 cycle when the CPU-to-PCI buffer becomes available after being full (PCI and AGP buses)

2 PCI Master Read Caching
- 0 Disable .....default
- 1 Enable

1 Delay Transaction
- 0 Disable .....default
- 1 Enable

0 Slave Device Stopped Idle Cycle Reduction
- 0 Normal Operation .....default
- 1 Reduce 1 PCI idle cycle when stopped by a slave device (PCI and AGP buses)

Device 0 Offset 71 - CPU to PCI Flow Control 1 (00h) . RW

7 Dynamic Burst
- 0 Disable..... default
- 1 Enable (see note under bit-3 below)

6 Byte Merge
- 0 Disable..... default
- 1 Enable

5 Reserved .....always reads 0

4 PCI I/O Cycle Post Write
- 0 Disable..... default
- 1 Enable

3 PCI Burst
- 0 Disable..... default
- 1 Enable (bit7=1 will override this option)

bit-7	bit-3	Operation
0	0	Every write goes into the write buffer and no PCI burst operations occur.
0	1	If the write transaction is a burst transaction, the information goes into the write buffer and burst transfers are later performed on the PCI bus. If the transaction is not a burst, PCI write occurs immediately (after a write buffer flush).
1	x	Every write transaction goes to the write buffer; burstable transactions will then burst on the PCI bus and non-burstable won't. This is the normal setting.

2 PCI Fast Back-to-Back Write
- 0 Disable..... default
- 1 Enable

1 Quick Frame Generation
- 0 Disable..... default
- 1 Enable

0 1 Wait State PCI Cycles
- 0 Disable..... default
- 1 Enable

Device 0 Offset 72 - CPU to PCI Flow Control 2 (00h) RWC

7 Retry Status
- 0 No retry occurred ..... default
- 1 Retry occurred..... **write 1 to clear**

6 Retry Timeout Action
- 0 Retry Forever (record status only) ..... default
- 1 Flush buffer for write or return all 1s for read

5-4 Retry Limit
- 00 Retry 2 times ..... default
- 01 Retry 16 times
- 10 Retry 4 times
- 11 Retry 64 times

3 Clear Failed Data and Continue Retry
- 0 Flush the entire post-write buffer..... default
- 1 When data is posting and master (or target) abort fails, pop the failed data if any, and keep posting

2 CPU Backoff on PCI Read Retry Failure
- 0 Disable ..... default
- 1 Backoff CPU when reading data from PCI and retry fails

1 Reduce 1T for FRAME# Generation
- 0 Disable ..... default
- 1 Enable

0 Reduce 1T for CPU read PCI slave
- 0 Disable ..... default
- 1 Enable

Device 0 Offset 73 - PCI Master Control 1 (00h)..... RW

7 Reserved ..... always reads 0

6 PCI Master 1-Wait-State Write
- 0 Zero wait state TRDY# response..... default
- 1 One wait state TRDY# response

5 PCI Master 1-Wait-State Read
- 0 Zero wait state TRDY# response..... default
- 1 One wait state TRDY# response

4 Reserved ..... always reads 0

3 Assert STOP# after PCI Master Write Timeout
- 0 Disable..... default
- 1 Enable

2 Assert STOP# after PCI Master Read Timeout
- 0 Disable..... default
- 1 Enable

1 LOCK# Function
- 0 Disable..... default
- 1 Enable

0 PCI Master Broken Timer Enable
- 0 Disable..... default
- 1 Enable. Force into arbitration when there is no FRAME# 16 PCICLK's after the grant.

Device 0 Offset 74 - PCI Master Control 2 (00h)..... RW

7 PCI Master Read Prefetch by Enhance Command
- 0 Always Prefetch ..... default
- 1 Prefetch only if Enhance command

6 Reserved (Do Not Program) ..... default = 0

5 Reserved ..... always reads 0

4 Dummy Request ..... default = 0

3 PCI Delay Transaction Timeout
- 0 Disable..... default
- 1 Enable

2 Backoff CPU Immediately on CPU-to-AGP
- 0 Disable..... default
- 1 Enable

1-0 CPU/PCI Master Latency Timer Control
- 00 AGP master reloads MLT timer ..... default
- 01 AGP master falling edge reloads MLT timer
- 10 AGP master rising edge resets timer to 00 and AGP master falling edge reloads MLT timer
- 11 Reserved (do not program)

Device 0 Offset 75 - PCI Arbitration 1 (00h) .....RW

7 Arbitration Mechanism
- 0 PCI has priority .....default
- 1 Fair arbitration between PCI and CPU

6 Arbitration Mode
- 0 REQ-based (arbitrate at end of REQ#) ..default
- 1 Frame-based (arbitrate at FRAME# assertion)

5-4 Latency Timer.....read only, reads Rx0D bits 2:1

3-0 PCI Master Bus Time-Out

(force into arbitration after a period of time)
- 0000 Disable .....default
- 0001 1x32 PCICLKs
- 0010 2x32 PCICLKs
- 0011 3x32 PCICLKs
- 0100 4x32 PCICLKs
- ... ...
- 1111 15x32 PCICLKs

Device 0 Offset 76 - PCI Arbitration 2 (00h)..... RW

7 PCI CPU-to-PCI Post-Write Retry Failed
- 0 Continue retry attempt..... default
- 1 Go to arbitration

6 CPU Latency Timer Bit-0.....RO
- 0 CPU has at least 1 PCLK time slot when CPU has PCI bus
- 1 CPU has no time slot

5-4 Master Priority Rotation Control
- 0x Grant to CPU after every PCI master grant..... .....def=00
- 10 Grant to CPU after every 2 PCI master grants
- 11 Grant to CPU after every 3 PCI master grants

Setting 0x: the CPU will always be granted access after the current bus master completes, no matter how many PCI masters are requesting.

Setting 10: if other PCI masters are requesting during the current PCI master grant, the highest priority master will get the bus after the current master completes, but the CPU will be guaranteed to get the bus after that master completes.

Setting 11: if other PCI masters are requesting, the highest priority will get the bus next, then the next highest priority will get the bus, then the CPU will get the bus.

In other words, with the above settings, even if multiple PCI masters are continuously requesting the bus, the CPU is guaranteed to get access after every master grant (01), after every other master grant (10) or after every third master grant (11).

3-2 Select REQn to RQ4 mappin
- 00 REQ4 ..... default
- 01 REQ0
- 10 REQ1
- 11 REQ2

1 CPU-to-PCI QW High DW Read Access to PCI Slave Allowed to be Backed Off
- 0 Disable..... default
- 1 Enable

0 Enable RQ4 as High Priority Master
- 0 Disable..... default
- 1 Enable

Device 0 Offset 77 - Chip Test Mode (00h)..... RW

7 Reserved (no function).....always reads 0

6-0 Reserved (do not use).....default=0

Device 0 Offset 78 - PMU Control I (00h).....RW

7 I/O Port 22 Access
- 0 CPU access to I/O address 22h is passed on to the PCI bus.....default
- 1 CPU access to I/O address 22h is processed internally

6 Suspend Refresh Type
- 0 CBR Refresh.....default
- 1 Self Refresh

5 Reserved ..... always reads 0

4 Dynamic Clock Control
- 0 Normal (clock is always running).....default
- 1 Clock to various internal functional blocks is disabled when those blocks are not being used

3 Reserved ..... always reads 0

2 GSTOP# Assertion
- 0 Disable (GSTOP# is always high) .....default
- 1 Enable (GSTOP# could be low)

1 Reserved ..... always reads 0

0 Memory Clock Enable (CKE) Function
- 0 CKE Function Disable .....default
- 1 CKE Function Enable

Device 0 Offset 79 - PMU Control 2 (00h)..... RW

7 Cache Controller Module Clock Dynamic Stop
- 0 Disable..... default
- 1 Enable

6 DRAM Controller Module Clock Dynamic Stop
- 0 Disable..... default
- 1 Enable

5 AGP Controller Module Clock Dynamic Stop
- 0 Disable..... default
- 1 Enable

4 PCI Controller Module Clock Dynamic Stop
- 0 Disable..... default
- 1 Enable

3 Pseudo Power Good
- 0 Disable..... default
- 1 Enable

2 Indicate SIO Request to DRAM Controller
- 0 Disable..... default
- 1 Enable

1-0 Reserved .....always reads 0

Device 0 Offset 7A – Miscellaneous Control 1 (00h) .....RW

7 No Time-Out Arbitration for Consecutive Frame Accesses
- 0 **Enable** .....default
- 1 **Disable**

6-5 Reserved ..... always reads 0

4 Invalidate PCI / AGP Buffered (Cached) Read Data for CPU to PCI / AGP Accesses
- 0 Disable .....default
- 1 Enable

3 Background PCI-to-PCI Write Cycle Mode
- 0 Disable .....default
- 1 Enable

2-1 Reserved ..... always reads 0

0 South Bridge PCI Master Force Timeout When PCI Master Occupancy Timer Is Up
- 0 Disable .....default
- 1 Enable

Device 0 Offset 7B – Miscellaneous Control 2 (02h)..... RW

7-2 Reserved .....always reads 0

1 PCI Master Access PMRDY Select
- 0 Tail
- 1 Head **..... default**

0 PCI Bus Operating Freq..... strapped from MA5
- 0 33 MHz..... default
- 1 66 MHz

Device 0 Offset 7E – PLL Test Mode (00h) ..... RW

7-6 Reserved (status) .....RO

5-0 Reserved (do not use) ..... default=0

Device 0 Offset 7F – PLL Test Mode (00h) ..... RW

7-0 Reserved (do not use) ..... default=0

GART / Graphics Aperture Control

The function of the Graphics Address Relocation Table (GART) is to translate virtual 32-bit addresses issued by an AGP device into 4K-page based physical addresses for system memory access. In this translation, the upper 20 bits (A31-A12) are remapped, while the lower 12 address bits (A11-A0) are used unchanged.

A one-level fully associative lookup scheme is used to implement the address translation. In this scheme, the upper 20 bits of the virtual address are used to point to an entry in a page table located in system memory. Each page table entry contains the upper 20 bits of a physical address (a "physical page" address). For simplicity, each page table entry is 4 bytes. The total size of the page table depends on the GART range (called the "aperture size") which is programmable in the TwisterT.

This scheme is shown in the figure below.

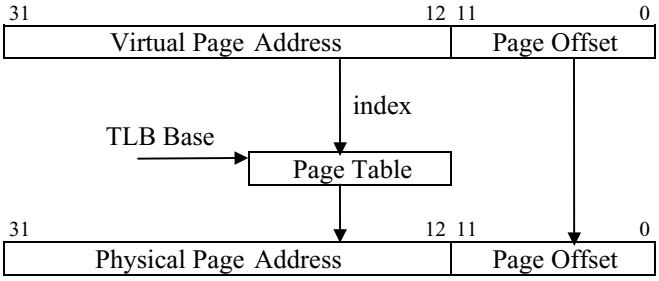


Figure 3. Graphics Aperture Address Translation

Since address translation using the above scheme requires an access to system memory, an on-chip cache (called a "Translation Lookaside Buffer" or TLB) is utilized to enhance performance. The TLB in the TwisterT contains 16 entries. Address "misses" in the TLB require an access of system memory to retrieve translation data. Entries in the TLB are replaced using an LRU (Least Recently Used) algorithm.

Addresses are translated only for accesses within the "Graphics Aperture" (GA). The Graphics Aperture can be any power of two in size from 1MB to 256MB (i.e., 1MB, 2MB, 4MB, 8MB, etc). The base of the Graphics Aperture can be anywhere in the system virtual address space on an address boundary determined by the aperture size (e.g., if the aperture size is 4MB, the base must be on a 4MB address boundary). The Graphics Aperture Base is defined in register offset 10 of device 0. The Graphics Aperture Size and TLB Table Base are defined in the following register group (offsets 84 and 88 respectively) along with various control bits.

Device 0 Offset 83-80 - GART/TLB Control (00000000h) RW

31-16 Reserved ..... always reads 0

15-8 Reserved (test mode status) ..... RO

7 Flush Page TLB
- 0 Disable..... default
- 1 Enable

6-4 Reserved (always program to 0) ..... RW

3 PCI Master Address Translation for GA Access
- 0 Addresses generated by PCI Master accesses of the Graphics Aperture will not be translateddefault
- 1 PCI Master GA addresses will be translated

2 AGP Master Address Translation for GA Access
- 0 Addresses generated by AGP Master accesses of the Graphics Aperture will not be translateddefault
- 1 AGP Master GA addresses will be translated

1 CPU Address Translation for GA Access
- 0 Addresses generated by CPU accesses of the Graphics Aperture will not be translated..... def
- 1 CPU GA addresses will be translated

0 AGP Address Translation for GA Access
- 0 Addresses generated by AGP accesses of the Graphics Aperture will not be translated..... def
- 1 AGP GA addresses will be translated

Note: For any master access to the Graphics Aperture range, snoop will not be performed.

Device 0 Offset 84 - Graphics Aperture Size (00h) ..... RW

7-0 Graphics Aperture Size

11111111	1M	1111000	16M
11111110	2M	1110000	32M
11111100	4M	11000000	64M
11111000	8M	10000000	128M
		00000000	256M

Offset 8B-88 - GA Translation Table Base (00000000h) RW

31-12 Graphics Aperture Translation Table Base. Pointer to the base of the translation table in system memory used to map addresses in the aperture range (the pointer to the base of the "Directory" table).

11-3 Reserved ..... always reads 0

2 PCI Master Directly Accesses DRAM if in GART Range
- 0 Disable..... default
- 1 Enable

1 Graphics Aperture Enable
- 0 Disable..... default
- 1 Enable

Note: To disable the Graphics Aperture, set this bit to 0 and set all bits of the Graphics Aperture Size to 0. To enable the Graphics Aperture, set this bit to 1 and program the Graphics Aperture Size to the desired aperture size.

0 Reserved ..... always reads 0

AGP Control

Device 0 Offset A3-A0 - AGP Capability Identifier (00200002h) ..... RO

31-24 Reserved ..... always reads 00
23-20 Major Specification Revision ..... always reads 0010
Major rev # of AGP spec that device conforms to
19-16 Minor Specification Revision ..... always reads 0000
Minor rev # of AGP spec that device conforms to
15-8 Pointer to Next Item ..... always reads 00 (last item)
7-0 AGP ID .. (always reads 02 to indicate it is AGP)

Device 0 Offset A7-A4 - AGP Status (1F000207h) ..... RO

31-24 Maximum AGP Requests ..... always reads 1F†
Max # of AGP requests the device can manage (32)
† See also RxFC[1] and RxFD[2-0]
23-10 Reserved ..... always reads 0s
9 Supports SideBand Addressing ..... always reads 1
8-6 Reserved ..... always reads 0s
5 4G Supported ..... (can be written at RxAE[5]
4 Fast Write Supported .... (can be written at RxAE[4]
3 Reserved ..... always reads 0s
2 4X Rate Supported ..... (can be written at RxAE[2])
1 2X Rate Supported ..... (can be written at RxAC[3])
0 1X Rate Supported ..... always reads 1

Device 0 Offset AB-A8 - AGP Command (00000000h).. RW

31-24 Request Depth (reserved for target) .. always reads 0s
23-10 Reserved ..... always reads 0s
9 SideBand Addressing Enable
0 Disable ..... default
1 Enable
8 AGP Enable
0 Disable ..... default
1 Enable
7-6 Reserved ..... always reads 0s
5 4G Enable
0 Disable ..... default
1 Enable
4 Fast Write Enable
0 Disable ..... default
1 Enable
3 Reserved ..... always reads 0s
2 4X Mode Enable
0 Disable ..... default
1 Enable
1 2X Mode Enable
0 Disable ..... default
1 Enable
0 1X Mode Enable
0 Disable ..... default
1 Enable

Device 0 Offset AC - AGP Control (00h)..... RW

7 AGP Disable ..... RO
0 Disable ..... default
1 Enable
This bit is latched from MA9 at the rising edge of RESET#.
6 AGP Read Synchronization
0 Disable ..... default
1 Enable
5 AGP Read Snoop DRAM Post-Write Buffer
0 Disable ..... default
1 Enable
4 GREQ# Priority Becomes Higher When Arbiter is Parked at AGP Master
0 Disable ..... default
1 Enable
3 2X Rate Supported (read also at RxA4[1])
0 Not supported ..... default
1 Supported
2 LPR In-Order Access (Force Fence)
0 Fence/Flush functions not guaranteed. AGP read requests (low/normal priority and high priority) may be executed before previously issued write requests. ..... default
1 Force all requests to be executed in order (automatically enables Fence/Flush functions). Low (i.e., normal) priority AGP read requests will never be executed before previously issued writes. High priority AGP read requests may still be executed prior to previously issued write requests as required.
1 AGP Arbitration Parking
0 Disable ..... default
1 Enable (GGNT# remains asserted until either GREQ# de-asserts or data phase ready)
0 AGP to PCI Master or CPU to PCI Turnaround Cycle
0 2T or 3T Timing ..... default
1 1T Timing

Device 0 Offset AD – AGP Latency Timer (02h).....RW

7-5 Reserved ..... always reads 0
4 Choose First or Last Ready of DRAM
0 Last ready chosen.....default
1 First ready chosen
3-0 AGP Data Phase Latency Timer ..... default = 02h

Device 0 Offset AE – AGP Miscellaneous Control (00h)RW

7-6 Reserved ..... always reads 0
5 4G Supported
0 4G not supported.....default
1 4G supported
4 Fast Write Supported
0 Fast Write not supported.....default
1 Fast Write supported
3 Reserved ..... always reads 0
2 4x Rate Supported
0 4x Rate not supported .....default
1 4x Rate supported
1-0 Reserved ..... always reads 0

Device 0 Offset B0 – AGP Pad Control / Status (8xh) ...RW

7 AGP 4x Strobe VREF Control
0 STB VREF is STB# and vice versa
1 STB VREF is AGPREF **.....default**
6 AGP 4x Strobe & GD Pad Drive Strength
0 Drive strength set to compensation circuit default .....default
1 Drive strength controlled by RxB1[7-0]
5-3 AGP Compensation Circuit N Control Output.RO
2-0 AGP Compensation Circuit P Control Output.RO

Device 0 Offset B1 – AGP Drive Strength (63h).....RW

7-4 AGP Output Buffer Drive Strength N Ctrl ... def=6
3-0 AGP Output Buffer Drive Strength P Ctrl.... def=3

Device 0 Offset B2 – AGP Pad Drive & Delay Ctrl (00h)RW

7 GD/GDS/GDS#/GBE Pad Control ..... default = 0

		SA / SBS	GD / GBE / GDS
0	VDDQ=1.5V:	Normal	Normal
	VDDQ=3.3V:	Delayed	Normal
1	VDDQ=1.5V:	Normal	Delayed
	VDDQ=3.3V	Delayed	Delayed

6-5 Reserved ..... always reads 0
4 GD[31:16] Output Stagger Delay
0 No delay.....def
1 Delay GD[31:16] by 1 ns
3-1 Reserved ..... always reads 0
0 GDS Output Delay
0 No delay.....def
1 Delay GDS by 400 ps
(GDS & GDS# will be delayed 1 ns more if bit-4 = 1)

Device 0 Offset C0 – Power Management Capability ID RO

7-0 Capability ID .....always reads 01h

Device 0 Offset C1 – Power Management New Pointer . RO

7-0 New Pointer ..... always reads 00h ("Null" Pointer)

Device 0 Offset C2 – Power Mgmt Capabilities I ..... RO

7-0 Power Management Capabilities ..always reads 02h

Device 0 Offset C3 – Power Mgmt Capabilities II..... RO

7-0 Power Management Capabilities ..always reads 00h

Device 0 Offset C4 – Power Mgmt Control / Status ..... RW

7-2 Reserved .....always reads 0
1-0 Power State
00 D0 ..... default
01 -reserved-
10 -reserved-
11 D3 Hot

Device 0 Offset C5 – Power Management Status..... RO

7-0 Power Management Status.....always reads 00h

Device 0 Offset C6 – PCI-to-PCI Bridge Support Ext.... RO

7-0 P2P Bridge Support Extensions ....always reads 00h

Device 0 Offset C7 – Power Management Data ..... RO

7-0 Power Management Data .....always reads 00h

Device 0 Offset E0 – Miscellaneous Control (00h)..... RW

7 AGP Pad Power Down
0 Disable..... default
1 Enable
6 Reserved (Do Not Program) .....default=0
5 Internal Graphics AGP/PCI Concurrent
0 Disable..... default
1 Enable
4 CKE Drive Select .....default=0
3-1 Bank Where Frame Buffer Is Located ....default=0
0 Latch DRAM Data Using
0 Internal DRAM DCLK..... default
1 External Feedback DRAM DCLK

Device 0 Offset E0 – Miscellaneous Control (00h) .....RW

7 AGP Pad Power Down
- 0 Normal .....default
- 1 Power Down

6 Reserved (Do Not Program)..... default = 0

5 Internal Graphics
- 0 Disable .....default
- 1 Enable (& allow CPU-AGP concurrent access)

4 CKE Drive Select ..... default = 0

3-1 Frame Buffer Bank
- 000 FB located in bank 0 .....default
- 001 FB located in bank 1
- 010 FB located in bank 2
- 011 FB located in bank 3
- 100 FB located in bank 4
- 101 -reserved-
- 11x -reserved-

0 Latch DRAM Data Using
- 0 Internal DRAM DCLK .....default
- 1 External Feedback DRAM DCLK

Device 0 Offset F7-F0 – BIOS Scratch Registers.....RW

7-0 No hardware function..... default = 0

Device 0 Offset F8 – DRAM Arbitration Timers (00h)..RW

7-4 AGP Timer (units of 4 MCLKs) ..... default = 0

3-0 Host CPU Timer (units of 4 MCLKs)..... default = 0

Device 0 Offset F9 – VGA Arbitration Timers (00h).....RW

7-4 VGA High Priority Timer (units of 16 MCLKs)def=0

3-0 VGA Timer (units of 16 MCLKs) ..... default = 0

Device 0 Offset FA – CPU Direct Access FB Base (00h) RW

7-0 CPU Direct Access FB Base Address[28:21].. def=0

Device 0 Offset FB – Frame Buffer Size (00h) ..... RW

7 VGA
- 0 Disable..... default
- 1 Enable

6-4 Frame Buffer Size
- 000 None ..... default
- 001 Reserved
- 010 Reserved
- 011 8MB
- 100 16MB
- 101 32MB
- 11x -reserved-

3 CPU Direct Access Frame Buffer
- 0 Disable..... default
- 1 Enable

2-0 CPU Direct Access FB Base Address[31:29].. def=0

Device 0 Offset FC – Back Door Control 1 (00h)..... RW

7-4 Priority Timer ..... default = 0

3-2 Reserved (Do Not Program)..... default = 0

1 Back-Door Max # of AGP Requests ..... default = 0
- 0 Read of RxA7 always returns a value of 1Fhdef
- 1 Read of RxA7 returns the value programmed in RxFD[2-0]

0 Back-Door Device ID Enable ..... default = 0
- 0 Use Rx3-2 value for Rx3-2 readback .... default
- 1 Use RxFE-FF Back-Door Device ID for Rx3-2 read

Device 0 Offset FD – Back-DoorControl 2 (00h) ..... RW

7-5 Reserved .....always reads 0

4-0 Max # of AGP Requests..... default = 0
(see also RxA7 and RxFC[1])

Device 0 Offset FF-FE – Back-Door Device ID (0000h) RW

15-0 Back-Door Device ID ..... default=00

Device 1 Register Descriptions

Device 1 Header Registers - PCI-to-PCI Bridge

All registers are located in PCI configuration space. They should be programmed using PCI configuration mechanism 1 through CF8 / CFC with bus number of 0 and function number equal to 0 and device number equal to one.

Device 1 Offset 1-0 - Vendor ID (1106h) .....RO

15-0 ID Code (reads 1106h to identify VIA Technologies)

Device 1 Offset 3-2 - Device ID (8605h).....RO

15-0 ID Code (reads 8605h to identify the TwisterT PCI-to-PCI Bridge device)

Device 1 Offset 5-4 – Command (0007h).....RW

15-10 Reserved ..... always reads 0

9 Fast Back-to-Back Cycle Enable ..... RO
- 0 Fast back-to-back transactions only allowed to the same agent.....default
- 1 Fast back-to-back transactions allowed to different agents

8 SERR# Enable..... RO
- 0 SERR# driver disabled.....default
- 1 SERR# driver enabled

(SERR# is used to report parity errors if bit-6 is set).

7 Address / Data Stepping..... RO
- 0 Device never does stepping.....default
- 1 Device always does stepping

6 Parity Error Response.....**RW**
- 0 Ignore parity errors & continue.....default
- 1 Take normal action on detected parity errors

5 VGA Palette Snoop (Not Supported) ..... RO
- 0 Treat palette accesses normally.....default
- 1 Don't respond to palette writes on PCI bus (10-bit decode of I/O addresses 3C6-3C9 hex)

4 Memory Write and Invalidate Command ..... RO
- 0 Bus masters must use Mem Write.....default
- 1 Bus masters may generate Mem Write & Inval

3 Special Cycle Monitoring..... RO
- 0 Does not monitor special cycles.....default
- 1 Monitors special cycles

2 Bus Master .....**RW**
- 0 Never behaves as a bus master
- 1 Enable to operate as a bus master on the primary interface on behalf of a master on the secondary interface .....default

1 Memory Space.....**RW**
- 0 Does not respond to memory space
- 1 Enable memory space access .....default

0 I/O Space .....**RW**
- 0 Does not respond to I/O space
- 1 Enable I/O space access .....default

Device 1 Offset 7-6 - Status (Primary Bus) (0230h).....RWC

15 Detected Parity Error .....always reads 0

14 Signaled System Error (SERR#).....always reads 0

13 Signaled Master Abort
- 0 No abort received ..... default
- 1 Transaction aborted by the master with Master-Abort (except Special Cycles)..... ..... write 1 to clear

12 Received Target Abort
- 0 No abort received ..... default
- 1 Transaction aborted by the target with Target-Abort ..... write 1 to clear

11 Signaled Target Abort .....always reads 0

10-9 DEVSEL# Timing
- 00 Fast
- 01 Medium .....always reads 01
- 10 Slow
- 11 Reserved

8 Data Parity Error Detected .....always reads 0

7 Fast Back-to-Back Capable.....always reads 0

6 User Definable Features .....always reads 0

5 66MHz Capable.....always reads 1

4 Supports New Capability list.....always reads 1

3-0 Reserved .....always reads 0

Device 1 Offset 8 - Revision ID (00h) ..... RO

7-0 TwisterT Chip Revision Code (00=First Silicon)

Device 1 Offset 9 - Programming Interface (00h)..... RO

This register is defined in different ways for each Base/Sub-Class Code value and is undefined for this type of device.

7-0 Interface Identifier.....always reads 00

Device 1 Offset A - Sub Class Code (04h)..... RO

7-0 Sub Class Code.reads 04 to indicate PCI-PCI Bridge

Device 1 Offset B - Base Class Code (06h)..... RO

7-0 Base Class Code.. reads 06 to indicate Bridge Device

Device 1 Offset D - Latency Timer (00h)..... RO

7-0 Reserved .....always reads 0

Device 1 Offset E - Header Type (01h) ..... RO

7-0 Header Type Code..... reads 01: PCI-PCI Bridge

Device 1 Offset F - Built In Self Test (BIST) (00h) ..... RO

7 BIST Supported..... reads 0: no supported functions

6 Start Test ..... write 1 to start but writes ignored

5-4 Reserved .....always reads 0

3-0 Response Code.....0 = test completed successfully

Device 1 Offset 18 - Primary Bus Number (00h).....RW

7-0 Primary Bus Number ..... default = 0

This register is read write, but internally the chip always uses bus 0 as the primary.

Device 1 Offset 19 - Secondary Bus Number (00h) .....RW

7-0 Secondary Bus Number..... default = 0

Note: AGP must use these bits to convert Type 1 to Type 0.

Device 1 Offset 1A - Subordinate Bus Number (00h) ....RW

7-0 Primary Bus Number ..... default = 0

Note: AGP must use these bits to decide if Type 1 to Type 1 command passing is allowed.

Device 1 Offset 1B – Secondary Latency Timer (00h) ....RO

7-0 Reserved ..... always reads 0

Device 1 Offset 1C - I/O Base (f0h).....RW

7-4 I/O Base AD[15:12]..... default = 1111b

3-0 I/O Addressing Capability ..... default = 0

Device 1 Offset 1D - I/O Limit (00h).....RW

7-4 I/O Limit AD[15:12] ..... default = 0

3-0 I/O Addressing Capability ..... default = 0

Device 1 Offset 1F-1E - Secondary Status.....RO

15-0 Secondary Status

Rx44[4] = 0: these bits read back 0000h

Rx44[4] = 1: these bits read back same as Rx7-6

Device 1 Offset 21-20 - Memory Base (fff0h).....RW

15-4 Memory Base AD[31:20].....default = FFFh

3-0 Reserved ..... always reads 0

Device 1 Offset 23-22 - Memory Limit (Inclusive) (0000h) RW

15-4 Memory Limit AD[31:20] ..... default = 0

3-0 Reserved ..... always reads 0

Device 1 Offset 25-24 - Prefetchable Memory Base (fff0h) RW

15-4 Prefetchable Memory Base AD[31:20]default = FFFh

3-0 Reserved ..... always reads 0

Device 1 Offset 27-26 - Prefetchable Memory Limit (0000h) .....RW

15-4 Prefetchable Memory Limit AD[31:20] . default = 0

3-0 Reserved ..... always reads 0

Device 1 Offset 37-34 - Capability Pointer (00000080h) .RO

Contains an offset from the start of configuration space.

31-0 AGP Capability List Pointer..... always reads 80h

Device 1 Offset 3F-3E – PCI-to-PCI Bridge Control (0000h) ..... RW

15-4 Reserved .....always reads 0

3 VGA-Present on AGP

0 Forward VGA accesses to PCI Bus..... default

1 Forward VGA accesses to AGP Bus

Note: VGA addresses are memory A0000-BFFFFh and I/O addresses 3B0-3BBh, 3C0-3CFh and 3D0-3DFh (10-bit decode). "Mono" text mode uses B0000-B7FFFh and "Color" Text Mode uses B8000-BFFFFh. Graphics modes use Axxxxh. Mono VGA uses I/O addresses 3Bx-3Cxh and Color VGA uses 3Cx-3Dxh. If an MDA is present, a VGA will not use the 3Bxh I/O addresses and B0000-B7FFFh memory space; if not, the VGA will use those addresses to emulate MDA modes.

2 Block / Forward ISA I/O Addresses

0 Forward all I/O accesses to the AGP bus if they are in the range defined by the I/O Base and I/O Limit registers (device 1 offset 1C-1D)

..... default

1 Do not forward I/O accesses to the AGP bus that are in the 100-3FFh address range even if they are in the range defined by the I/O Base and I/O Limit registers.

1-0 Reserved .....always reads 0

Device 1 Configuration Registers - PCI-to-PCI Bridge

AGP Bus Control

Device 1 Offset 40 - CPU-to-AGP Flow Control 1 (00h) RW

7 CPU-AGP Post Write
- 0 Disable .....default
- 1 Enable

6 CPU-AGP Dynamic Burst
- 0 Disable .....default
- 1 Enable

It is recommended that this bit be set to 0.

5 CPU-AGP One Wait State Burst Write
- 0 Disable .....default
- 1 Enable

4 AGP to DRAM Prefetch
- 0 Disable .....default
- 1 Enable

3 CPU to AGP Post Write
- 0 Disable .....default
- 1 Enable

2 MDA Present on AGP
- 0 Forward MDA accesses to AGP .....default
- 1 Forward MDA accesses to PCI

Note: Forward despite IO / Memory Base / Limit

Note: MDA (Monochrome Display Adapter) addresses are memory addresses B0000h-B7FFFh and I/O addresses 3B4-3B5h, 3B8-3BAh, and 3BFh (10-bit decode). 3BC-3BE are reserved for printers.

Note: If Rx3E bit-3 is 0, this bit is a don't care (MDA accesses are forwarded to the PCI bus).

1 AGP Master Read Caching
- 0 Disable .....default
- 1 Enable

0 AGP Delay Transaction
- 0 Disable .....default
- 1 Enable

Table 8. VGA/MDA Memory/IO Redirection

3E[3] VGA Pres.	40[2] MDA Pres.	VGA is on	MDA is on	Axxxx, B8xxx Access	B0000 -B7FFF Access	3Cx, 3Dx I/O	3Bx I/O
0	-	PCI	PCI	PCI	PCI	PCI	PCI
1	0	AGP	AGP	AGP	AGP	AGP	AGP
1	1	AGP	PCI	AGP	PCI	AGP	PCI

Device 1 Offset 41 - CPU-to-AGP Flow Control 2 (00h) RW

7 Retry Status
- 0 No retry occurred..... default
- 1 Retry Occurred .....**write 1 to clear**

6 Retry Timeout Action
- 0 No action taken except to record status ..... def
- 1 Flush buffer for write or return all 1s for read

5-4 Retry Count
- 00 Retry 2, backoff CPU ..... default
- 01 Retry 4, backoff CPU
- 10 Retry 16, backoff CPU
- 11 Retry 64, backoff CPU

3 Post Write Data on Abort
- 0 Flush entire post-write buffer on target-abort or master abort..... default
- 1 Pop one data output on target-abort or master-abort

2 CPU Backoff on AGP Read Retry Timeout
- 0 Disable..... default
- 1 Enable

1-0 Reserved .....always reads 0

Device 1 Offset 42 - AGP Master Control (00h) ..... RW

7 Read Prefetch for Enhance Command
- 0 Always Perform Prefetch ..... default
- 1 Prefetch only if Enhance Command

6 AGP Master One Wait State Write
- 0 Disable..... default
- 1 Enable

5 AGP Master One Wait State Read
- 0 Disable..... default
- 1 Enable

4 Extend AGP Internal Master for Efficient Handling of Dummy Request Cycles
- 0 Disable..... default
- 1 Enable

This bit is normally set to 1.

3 AGP Delay Transaction Timeout
- 0 Disable..... default
- 1 Enable

2 Prefetch Disable when Delay Transaction Occurred
- 0 Normal operation..... default
- 1 Disable prefetch when doing fast response to the previous delay transaction or doing read caching

1 Reserved .....always reads 0

0 Shorten AGP Master to TRFCTL
- 0 Disable..... default
- 1 Enable

Device 1 Offset 43 - AGP Master Latency Timer (00h) RW

7-4 Host to AGP Time slot
- 0 Disable (no timer) .....default
- 1 16 GCLKs
- 2 32 GCLKs
- … …
- F 128 GCLKs

3-0 AGP Master Time Slot
- 0 Disable (no timer) .....default
- 1 16 GCLKs
- 2 32 GCLKs
- … …
- F 128 GCLKs

Device 1 Offset 44 – Backdoor Register Control (00h) ..RW

7-5 Reserved ..... always reads 0

4 Secondary Status Access
- 0 Rx1F-1E read 0000h .....default
- 1 Rx1F-1E read same as Rx7-6

3 Back Door Register for Rx83[2], D2 Support

2 Back Door Register for Rx83[1], D1 Support

1 Back Door Register for Rx82[5], Device Specific Initialization

0 Back Door Register
- 0 Disable .....default
- 1 Enable

Device 1 Offset 45 – Fast Write Control (72h).....RW

7 Force Fast Write Cycle to be QW Aligned (if Rx45[6] = 0)
- 0 Disable .....default
- 1 Enable

6 Merge Multiple CPU Transactions Into One Fast Write Burst Transaction
- 0 Disable
- 1 Enable **.....default**

5 Merge Multiple CPU Write Cycles To Memory Offset 23-20 Into Fast Write Burst Cycles (if Rx45[6] = 0)
- 0 Disable
- 1 Enable **.....default**

4 Merge Multiple CPU Write Cycles To Prefetchable Memory Offset 27-24 Into Fast Write Burst Cycles (if Rx45[6] = 0)
- 0 Disable
- 1 Enable **.....default**

3 Reserved ..... always reads 0

2 Fast Write Burst 4T Max (No Slave Flow Control)
- 0 Disable .....default
- 1 Enable

1 Fast Write Fast Back to Back
- 0 Disable
- 1 Enable **.....default**

0 Fast Write Initial Block 1 Wait State
- 0 Disable .....default
- 1 Enable

Rx45 Bits 7-4	CPU Write Address in Mem1	CPU Write Address in Mem2	Fast Write Cycle Alignment
x1xx	-	-	QW aligned, burstable
0000	-	-	DW aligned, nonburstable
x010	0	0	n/a
0010	0	1	DW aligned, non-burstable
x010	1	-	QW aligned, burstable
x001	0	0	n/a
x001	-	1	QW aligned, burstable
0001	1	0	DW aligned, non-burstable
x011	0	0	n/a
x011	1	-	QW aligned, burstable
x011	0	1	QW aligned, burstable
1000	-	-	QW aligned, non-burstable
1010	0	1	QW aligned, non-burstable
1001	1	0	QW aligned, non-burstable

Device 1 Offset 47-46 – PCI-to-PCI Bridge Device ID .. RW

15-0 PCI-to-PCI Bridge Device ID..... default = 0000

Device 1 Offset 80 – Capability ID (01h) ..... RO

7-0 Capability ID ..... always reads 01h

Device 1 Offset 81 – Next Pointer (00h) ..... RO

7-0 Next Pointer: Null ..... always reads 00h

Device 1 Offset 82 – Power Mgmt Capabilities 1 (02h) .. RO

7-0 Power Mgmt Capabilities ..... always reads 02h

Device 1 Offset 83 – Power Mgmt Capabilities 2 (00h) .. RO

7-0 Power Mgmt Capabilities ..... always reads 00h

Device 1 Offset 84 – Power Mgmt Ctrl/Status (00h)..... RW

7-2 Reserved ..... always reads 0

1-0 Power State
- 00 D0 ..... default
- 01 -reserved-
- 10 -reserved-
- 11 D3 Hot

Device 1 Offset 85 – Power Mgmt Status (00h)..... RO

7-0 Power Mgmt Status ..... default = 00

Device 1 Offset 86 – P2P Br. Support Extensions (00h) . RO

7-0 P2P Bridge Support Extensions ..... default = 00

Device 1 Offset 87 – Power Management Data (00h) ..... RO

7-0 Power Management Data ..... default = 00

FUNCTIONAL DESCRIPTION - INTEGRATED PROSAVAGE4 GRAPHICS

Configuration Strapping

Certain TwisterT graphics functions have options that must be selected and fixed at reset (before the register bits controlling these functions can be programmed by software). This is accomplished via power-on configuration strapping.

The strapping pins are pulled low internally and can be individually pulled high through 10 KOhm resistors. These pull-ups and pull-downs do not affect normal operation of the pins, but they do force the pins to a definite state during reset. At the rising edge of the reset signal, this state is sampled, the result is inverted and the data loaded into the CR36, CR37, CRB0 and CRF0 registers. The data is used for system configuration. The definitions of the strapping bits at the rising edge of the reset signal are shown in Table 9. Non-graphics straps are described in the pin descriptions for the MA signals in Table 1.

Pin Name	Ball #	CR Bit(s) Value	Description
MA4	AB24	CR36[0]	**PCI Interrupt**
		1	Disable INTA# claim (00H in PCI3D)
		0	Enable INTA# claim (01H in PCI3D)
MA3	AB25	CR36[4]	**IO Disable**
		1	Disable I/O access PCI04[0] ignored
		0	Enable I/O access via PCI04[0] = 1.
MA2	AB26	CRB0[7]	**PCI Base Address Mapping**
		1	Address Mapping 1
		0	Address Mapping 0 (PCI10, 14) (16M assigned to PCI0; 128M assigned to PCI14)
MA14 MA13 MA1 MA0	AF25 AE25 AB23 AA23	CRF0[3] CRF0[2] CRF0[1] CRF0[0]	OEM-Defined Panel Type

Table 9. Definition of Strapping Bits at the Rising Edge of the Reset Signal

Important Note: As described above, the signal levels on the strapping pins are inverted before being latched in the various strapping bit registers. Since the strapping pins all have internal pull-downs, the default values for each of the strapping bits is 1. The value latched at reset can be changed to 0 by adding an external pull-up to the appropriate pin. After reset, the strapping bits are written and read normally, i.e., there is no inversion of the register values.

PCI Configuration and Integrated AGP

PCI Configuration

The TwisterT graphics Vendor ID register (Index 00H) in the PCI Configuration space is hardwired to 5333H to specify S3 Graphics as the vendor. The Device ID register is hardwired to 8D01H.

Bits 10-9 of the Status register (Index 06H) are hardwired to 01b to specify medium DEVSEL timing. The Class Code register (Index 08H) is hardwired to 30000xxH to specify that the TwisterT is a VGA compatible device.

There are two MMIO address mappings, as determined by the state of CRB0[7]. By default, CRB0[7] = 1, which selects Mapping 0. This uses the PCI base addresses specified by PCI10 and PCI14. 16 Mbytes of address space is claimed by PCI10 and 128 Mbytes of address space is claimed by PCI14. If the MA4 pin is strapped high at reset, a 0 is latched in CRB0[7] and selects Mapping 1. This uses base addresses PCI10 (same as Mapping 0), PCI14 (redefined from Mapping 0 to claim 16 Mbytes) and adds PCI18, PCI1C, PCI20 and PCI24, each claiming 16 Mbytes. Thus, Mapping 1 allows the address space claimed to be broken up into smaller blocks, as required by some operating systems. The Base Address 0 register (Index 10H) defaults to address 7000 0000H. This is the relocatable base address for memory-mapped I/O register accessing.

PCI06[4] is hardwired to 1 to indicate a capabilities list is available. PCI34[7-0] point to the PCI power management registers starting at offset DC. The basic power states (D0-D3) are supported as explained by the PCI Bus Power Management Interface Specification, Revision 1.1.

PCI Subsystem ID

The Subsystem ID and Subsystem Vendor ID are located in a 32-bit read only register at PCI Configuration Space Index 2C. These registers reflect the content of 4 read/write CR registers as follows:

Register	CR Space	PCI Configuration Space
Subsystem Vendor ID Low Byte	CR81	Index 2CH
Subsystem Vendor ID High Byte	CR82	Index 2DH
Subsystem ID Low Byte	CR83	Index 2EH
Subsystem ID High Byte	CR84	Index 2FH

Table 10. PCI Subsystem ID and Subsystem Vendor ID Registers

These registers allow identification of particular vendors using the same graphics chip. The following design allows the subsystem identification to be handled by software (no hardwiring).

All TwisterT motherboard designs will incorporate the video BIOS into the system BIOS ROM. The system BIOS must load the subsystem ID information in the TwisterT before any ID scanning takes place. To do this, it must turn on the TwisterT, enable I/O accesses in the PCI configuration space, unlock the CR registers, program the subsystem ID information in the registers described above, then turn off the TwisterT.

Integrated AGP

TwisterT graphics conform with the requirements of Revision 2.0 of the AGP Interface Specification. Internal AGP TwisterT graphics are always enabled.

For the most part, AGP configuration is identical to PCI configuration. PCI04[4] is hardwired to 1 to indicate that TwisterT graphics implements a list of capabilities. PCI34[7-0] point to the location of this list, which is at offset 80H. PCI80, PCI84 and PCI88 implement the register bits required by the AGP specification. PCI88[2-0] select the data rate. PCI88[8] = 1 enables AGP bus master operations. PCI88[9] =1 enables sideband addressing. This is indicated by PCI84[9] (1 = sideband addressing supported). The state of PCI84[9] is determined by the state of CR70[7].

Display Memory

The TwisterT north bridge utilizes a Shared Memory Architecture (SMA) for Frame Buffer Memory. SMA allows system memory to be efficiently shared by the host CPU and the TwisterT north bridge graphics controller. By default, no system memory is allocated for the graphics frame buffer, but up to 32 Mbytes may be allocated depending on user preference, application requirements, and the total size of system memory.

Note: Frame buffer memory is allocated from system memory at bootup time. Changing the display settings to a resolution requiring additional frame buffer memory will require a system reboot to be performed.

Frame Buffer Size	Dev 0 RxFB[6-4] Register Setting	CR36[7-5] † Register Setting
0 Mbytes	000	000
8 Mbytes	011	011
16 Mbytes	100	100
32 Mbytes	101	101

† For driver information only (not connected to hardware)

Table 11. Supported Frame Buffer Memory Configurations

Interrupt Generation

Whatever the mode of operation (VGA or Enhanced), bit 4 of CR32 must be set to 1 to enable interrupt generation. When an enabled interrupt is generated, INTA# is pulled low unless CR36[0] = 0 (MA2 pulled high at reset), for which case no PCI interrupt line is claimed during PCI configuration.

When TwisterT graphics are being operated in VGA mode (CR66[0] = 0), only vertical retrace can generate an interrupt. This is enabled when CR11[5] = 0 and CR11[4] = 1. When an interrupt occurs, it is cleared by writing a 0 to CR11[4]. The interrupt must then be re-enabled by writing a 1 to the same bit. Note that the BIOS clears both bit 4 and bit 5 of CR11 during power-on, a mode set, or a reset. Thus, interrupt generation is disabled until bit 4 is set to 1.

In Enhanced mode (CR66[0] = 1 or 3D operation), interrupts can be generated by vertical retrace, command or bus FIFO overflow, command or bus FIFO empty, or by a BCI command. These interrupts are enabled and cleared and their status reported via MM8504. Serial port interrupts are controlled via MMFF08. If interrupts are used, they should be cleared before they are enabled.

Multiple interrupts can be enabled at the same time in Enhanced mode. The interrupt pin will remain asserted until all interrupt status bits are cleared.

Display Interfaces

TwisterT supports a variety of color STN and TFT flat panels. Flat panel display is enabled by setting SR31_4 = 1. TwisterT also provides an integrated industry standard LVDS driver interface. CRT and TV display are possible at the same time as flat panel display. All these interfaces are described in this section.

STN Panel Interfaces

STN panel support is selected when SR79[1-0] = 10b.

TwisterT supports either a single-scan (SS-STN) or a dual-scan (DD-STN) STN panel. The type is selected via SR70[0] as follows:

0 = DD-STN panel
1 = SS-STN panel

SR7D[2-0] define the pixel data bus size as follows:

000 = 16-bit STN
001 = 8-bit STN
010 = 24-bit STN

Pixel data is output on some combination of the FPD[35:0] pins, depending on the pixel data bus size and the setting of SR7D[3]. This is shown in Table 13 at the end of this section.

Selection of an STN panel configures several pins specifically for STN control.

The polarity of the flat panel data can be changed to active low by programming SR72[4] to 1. The drive strength of the panel data is specified via SR7D[6]. The drive strength for the clock is specified via SR7D[7].

The polarity of FPHS can be changed to active low by programming SR72[6] to 1.

Several controls are provided for FPHS and FPCLK during vertical blanking.

FPCLK is normally stopped during non-display time by setting SR80[5] to 1. When SR7D[4] = 0, FPHS will run during vertical blanking. Setting SR7D[4] to 1 disables FPHS during vertical blank. Setting SR73[6] to 1 adds an extra FPHS when FPHS is disabled during vertical blanking. If SR7D[4] = 0 and SR7D[5] = 1, FPCLK is disabled during the first line of vertical blanking. If SR80[5] = 0, FPCLK runs continuously. FPCLK can be delayed via SR80[3-1]. Its polarity can be inverted via SR72[3]

The polarity of FPVS can be changed to active low by programming SR72[7] to 1.

Setting SR80[4] to 1 forces all flat panel data and control signals to logic 0.

DD-STN panel operation requires off-screen video memory. The amount of memory is programmed in SR50 and SR51. The starting location of the DD-STN memory is specified in SR4F. These values are all programmed by the video BIOS at reset.

TFT Panel Interfaces

TFT panel support is selected when SR79[1-0] = 00b.

SR7D[2-0] define the pixel data bus size as follows:

000 = 1 pixel/clock TFT (9-, 12-, 15-, 18-bit)
001 = 1 pixel/clock TFT (24-bit)
010 = 2 pixels/clock TFT (2x12-, 2x18-bit)

The 2 pixels per clock modes halve the clock rate and clock two pixels on the falling edge of FPCLK, thereby lowering EMI levels. SR80[6] is set to 1 to support this mode of operation.

Pixel data is output on some combination of the FPD[35:0] pins. The data outputs are shown in Table 14 and Table 15 at the end of this section.

Selection of a TFT panel configures several pins specifically for TFT control. The drive strengths of the panel clock and data are specified via SR7D[7-6].

The polarity of the flat panel data can be changed to active low by programming SR72[4] to 1. The polarity of the FPDE signal can be changed to active low by setting SR72[5] to 1. The polarity of the FPHS signal can be changed to active low by setting SR72[6] to 1. The polarity of the FPVS signal can be changed to active low by setting SR72[7] to 1.

SR80[5] allows FPCLK to be enabled (0) or disabled (1) during non-display time. FPCLK can be delayed via SR80[3-1].

Flat Panel LVDS Interface

TwisterT provides either a 1- or 2-channel integrated LVDS interface. This is available independently of the other panel interfaces. A single channel interface uses the Y[2:0]–, Y[2:0]+, YC– and YC+ outputs. A 2-channel interface uses the Yxx outputs for the first channel and the Z[2:0]–, Z[2:0]+, ZC– and ZC+ outputs for the second channel.

CRT Interface

TwisterT provides the following CRT interface signals:

- RED (analog red)
- GREEN (analog green)
- BLUE (analog blue)
- HSYNC (horizontal sync)
- VSYNC (vertical sync)

In addition, DDC2 monitor communications can be implemented via the serial communications port controlled by CRB1[4:0]. These bits control two-way communications over the SPCLK2 (clock) and SPDAT2 (data) lines. The operation is the same as described for the I^2C serial communications port section except that interrupts and wait states are not supported.

External TV Encoder Interface

Figure 4 shows the interface to an external Bt868/869 TV encoder (or compatible device). The TV outputs are generated whenever the clock input from the decoder is present on the TVCLK pin and CRB0[4] = 0. The encoder is controlled via the I^2C interface. TV monitor detection is also done via this interface. The TV encoder interface and the flat panel interface are multiplexed on common pins, so only one of the two (either the TV interface or the flat panel interface) can be enabled at any given time

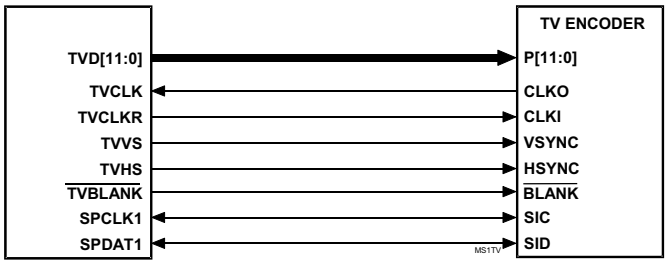


Figure 4. External TV Encoder Interface

TwisterT supports three output formats as shown in Table 12. As shown in Figure 4, P[11:0] on the encoder connect to TVD[11:0] on TwisterT. The CLKI pin on the encoder connects to the TVCLKR pin on TwisterT.

	SR35[5-4] = 00		SR35[5-4] = 01		SR35[5-4] = 10	
Pin	CLK1 Rising	CLKI Falling	CLK1 Rising	CLKI Falling	CLK1 Rising	CLKI Falling
P11	G4	R7	B7	G3	R7	G3
P10	G3	R6	B6	G2	R6	G2
P9	G2	R5	B5	G1	R5	G1
P8	B7	R4	B4	G0	R4	G0
P7	B6	R3	B3	R7	R3	B7
P6	B5	G7	B2	R6	R2	B6
P5	B4	G6	B1	R5	R1	B5
P4	B3	G5	B0	R4	R0	B4
P3	G0	R2	G7	R3	G7	B3
P2	B2	R1	G6	R2	G6	B2
P1	B1	R0	G5	R1	G5	B1
P0	B0	G1	G4	R0	G4	B0

Table 12. External TV Encoder Output Data Formats

I²C Serial Communications Port

One serial communications port is implemented in a register that can be accessed either via MMFF20 or CRA0. Bit 4 is set to 1 to enable the interface. The clock is written to bit 0 (= 0) and data to bit 1 (= 0), driving the SPCLK1 and SPDAT1 pins low respectively. The state of the SPCLK1 pin can be read via bit 2 and the state of the SPDAT1 pin can be read via bit 3. The SPCLK1 and SPDAT1 pins are tri-stated when their corresponding control bits are reset to 0, allowing other devices to drive the serial bus.

This serial port is typically used for I2C interfacing. When SPCLK1 and SPDAT1 are tri-stated, the TwisterT can detect an I2C start condition (SPDAT1 driven low while SPCLK1 is not driven low). This condition is generated by another I2C master that wants control of the I2C bus. If bit 19 of MMFF08 is set to 1, detection of a start condition generates an interrupt and sets bit 3 of MMFF08 to 1. If bit 24 of MMFF08 is set to 1, the TwisterT drives SPCLK1 low to generate I2C wait states until the Host can clear the interrupt and service the I2C bus.

ZV-Port Interface

The ZV-Port, or Zoomed Video Port, allows direct transmission of video data from a PC Card to TwisterT. TwisterT supports ZV Port operation when MMFF00_0 = 1). The following setup is done for ZV Port operation:

- Video 16 mode is selected (MMFF00_3-1 = 001b)
- MMFF09_9 and MMFF00_10 must be set to 1 to specify active high HSYNC (ZVHS) and VSYNC (ZVVS).
- Byte swapping is disabled by setting MMFF00_6 to 1.
- One or two frame buffer starting addresses are defined (MMFF0C, MMFF10). One is required. The second is required for double buffering.
- The horizontal and vertical decimation registers are programmed (MMFF2C, MMFF30). This is optional.
- The video input window size (height in lines and width in pixels) is programmed in MMFF24.
- The video data horizontal and vertical offsets are programmed in MMFF28.
- The line offset (stride) is programmed (MMFF34_10-0).

During ZV-Port operation, TwisterT automatically detects even and odd video fields based on the state of ZVHS on the falling edge of ZVVS. The status of this detection is given by MMFF00_28.

The interface is shown in Figure 5.

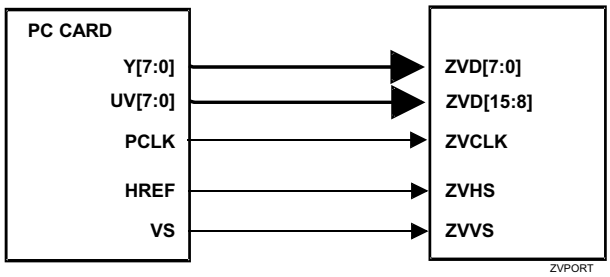


Figure 5. ZV-Port Interface

SR7D[3]	0	0	0	0	0	0	1	1
SR70[0]	1	1	1	0	0	0	0	0
SR79[1-0]	10	10	10	10	10	10	10	10
SR7D[2-0]	001	000	010	010	000	010	000	010
Pin Name	**STN8**	**STN16**	**STN24**	**DSTN8**	**DSTN16**	**DSTN24**	**DSTN16**	**DSTN24**
FPD0	R0	R0	R0	LR0	LR0	LR0		LB3
FPD1	G0	G0	G0			LR3		LB2
FPD2	B0	B0	B0	LG0	LG0	LG0	LB1	LB1
FPD3	R1	R1	R1				LB0	LB0
FPD4	G1	G1	G1	LB0	LB0	LB0		UB3
FPD5	B1	B1	B1					UB2
FPD6	R2	R2	R2	LR1	LR1	LR1	UB1	UB1
FPD7	G2	G2	G2			LG3	UB0	UB0
FPD8		B2	B2		LG1	LG1		LG3
FPD9		R3	R3				LG2	LG2
FPD10		G3	G3		LB1	LB1	LG1	LG1
FPD11		B3	B3				LG0	LG0
FPD12		R4	R4		LR2	LR2		UG3
FPD13		G4	G4			LB3	UG2	UG2
FPD14		B4	B4		LG2	LG2	UG1	UG1
FPD15		R5	R5				UG0	UG0
FPD16			G5			LB2		LR3
FPD17			B5				LR2	LR2
FPD18			R6	UR0	UR0	UR0	LR1	LR1
FPD19			G6			UR3	LR0	LR0
FPD20			B6	UG0	UG0	UG0		UR3
FPD21			R7				UR2	UR2
FPD22			G7	UB0	UB0	UB0	UR1	UR1
FPD23			B7				UR0	UR0
FPD24				UR1	UR1	UR1		
FPD25						UG3		
FPD26					UG1	UG1		
FPD27								
FPD28					UB1	UB1		
FPD29						UB3		
FPD30					UR2	UR2		
FPD31						UB3		
FPD32					UG2	UG2		
FPD33								
FPD34						UB2		
FPD35								

Table 13. STN Flat Panel Data Outputs

SR7D[3]	0	0	0	0	0	0	0	0	0
SR70[0]	1	1	1	1	1	1	1	1	1
SR79[1-0]	00	00	00	00	00	00	00	00	00
SR7D[2-0]	000	010	000	010	000	010	000	010	001
Pin Name	**TFT9**	**TFT2x9**	**TFT12**	**TFT2x12**	**TFT15**	**TFT2x15**	**TFT18**	**TFT2x18**	**TFT24**
FPD0							R0	R00	R2
FPD1								R10	R0
FPD2					R0	R00	R1	R01	R3
FPD3						R10		R11	
FPD4			R0	R00	R1	R01	R2	R02	R4
FPD5				R10		R11		R12	
FPD6	R0	R00	R1	R01	R2	R02	R3	R03	R5
FPD7		R10		R11		R12		R13	R1
FPD8	R1	R01	R2	R02	R3	R03	R4	R04	R6
FPD9		R11		R12		R13		R14	
FPD10	R2	R02	R3	R03	R4	R04	R5	R05	R7
FPD11		R12		R13		R14		R15	
FPD12							G0	G00	G2
FPD13								G10	G0
FPD14					G0	G00	G1	G01	R3
FPD15						G10		G11	
FPD16			G0	G00	G1	G01	G2	G02	G4
FPD17				G10		G11		G12	
FPD18	G0	G00	G1	G01	G2	G02	G3	G03	G5
FPD19		G10		G11		G12		G13	G1
FPD20	G1	G01	G2	G02	G3	G03	G4	G04	G6
FPD21		G11		G12		G13		G14	
FPD22	G2	G02	G3	G03	G4	G04	G5	G05	G7
FPD23		G12		G13		G14		G15	
FPD24							B0	B00	B2
FPD25								B10	B0
FPD26					B0	B00	B1	B01	B3
FPD27						B10		B11	
FPD28			B0	B00	B1	B01	B2	B02	B4
FPD29				B10		B11		B12	
FPD30	B0	B00	B1	B01	B2	B02	B3	B03	B5
FPD31		B10		B11		B12		B13	B1
FPD32	B1	B01	B2	B02	B3	B03	B4	B04	B6
FPD33		B11		B12		B13		B14	
FPD34	B2	B02	B3	B03	B4	B04	B5	B05	B7
FPD35		B12		B13		B14		B15	

Table 14. TFT Flat Panel Data Outputs (SR7D[3] = 0)

SR7D[3]	1	1	10
SR70[0]	1	1	1
SR79[1-0]	00	00	00
SR7D[2-0]	000	010	001
Pin Name	**TFT18**	**TFT2x18**	**TFT24**
FPD0		R14	B0
FPD1		R15	B1
FPD2	B0	B00	B2
FPD3	B1	B01	B3
FPD4	B2	B02	B4
FPD5	B3	B03	B5
FPD6	B4	B04	B6
FPD7	B5	B05	B7
FPD8		R12	G0
FPD9		R13	G1
FPD10	G0	G00	G2
FPD11	G1	G01	G3
FPD12	G2	G02	G4
FPD13	G3	G03	G5
FPD14	G4	G04	G6
FPD15	G5	G05	G7
FPD16		R10	R0
FPD17		R11	R1
FPD18	R0	R00	R2
FPD19	R1	R01	R3
FPD20	R2	R02	R4
FPD21	R3	R03	R5
FPD22	R4	R04	R6
FPD23	R5	R05	R7
FPD24		G10	
FPD25		G11	
FPD26		G12	
FPD27		G13	
FPD28		G14	
FPD29		G15	
FPD30		B10	
FPD31		B11	
FPD32		B12	
FPD33		B13	
FPD34		B14	
FPD35		B15	

Table 15. TFT Flat Panel Data Outputs (SR7D[3] = 1)

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Table 16. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes
T_C	Case operating temperature	0	85	^oC	1
T_S	Storage temperature	-55	125	^oC	1
V_{IN}	Input voltage	-0.5	V_{RAIL} + 10%	Volts	1, 2
V_{OUT}	Output voltage	-0.5	V_{RAIL} + 10%	Volts	1, 2

Note 1. Stress above the conditions listed may cause permanent damage to the device. Functional operation of this device should be restricted to the conditions described under operating conditions.

Note 2. V_{RAIL} is defined as the V_{CC} level of the respective rail. The CPU interface can be 3.3V or 2.5V. Memory can be 3.3V only. PCI can be 3.3V or 5.0V. Video can be 3.3V or 5.0V. Flat Panel can be 3.3V only. AGP can be 1.5V (4x transfer mode) or 3.3V (2x transfer mode).

DC Characteristics

T_C = 0-85^oC, V_{RAIL} = V_{CC} +/- 5%, V_{CORE} = 2.5V +/- 5%, GND=0V

Table 17. DC Characteristics

Symbol	Parameter	Min	Max	Unit	Condition
V_{IL}	Input Low Voltage	-0.50	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}+0.5	V	
V_{OL}	Output Low Voltage	-	0.55	V	I_{OL}=4.0mA
V_{OH}	Output High Voltage	2.4	-	V	I_{OH}=-1.0mA
I_{IL}	Input Leakage Current	-	+/-10	uA	$0<V_{IN}<V_{CC}$
I_{OZ}	Tristate Leakage Current	-	+/-20	uA	$0.55<V_{OUT}<V_{CC}$

Power Characteristics

T_C = 0-85°C, V_{RAIL} = V_{CC} +/- 5%, V_{CORE} = 2.5V +/- 5%, GND=0V

Table 18. Power Characteristics

Symbol	Parameter	Typ	Max	Unit	Condition
I_{CC3}	Power Supply Current – VCC3	91		mA	Full-On Operation
I_{CC3POS}	Power Supply Current – VCC3	2		mA	POS
I_{CC3STR}	Power Supply Current – VCC3	0		mA	STR
I_{CC3SOF}	Power Supply Current – VCC3	0		mA	Soft-Off
I_{CC25}	Power Supply Current – VCC25	682		mA	Full-On Operation
$I_{CC25POS}$	Power Supply Current – VCC25	29		mA	POS
$I_{CC25STR}$	Power Supply Current – VCC25	0		mA	STR
$I_{CC25SOF}$	Power Supply Current – VCC25	0		mA	Soft-Off
I_{TT}	Power Supply Current – VTT			mA	Full-On Operation
I_{TTPOS}	Power Supply Current – VTT			mA	POS
I_{TTSTR}	Power Supply Current – VTT			mA	STR
I_{TTSOF}	Power Supply Current – VTT			mA	Soft-Off
I_{SUS25}	Power Supply Current – VSUS25	2		mA	Full-On Operation
$I_{SUS25POS}$	Power Supply Current – VSUS25	0.0003		mA	POS
$I_{SUS25STR}$	Power Supply Current – VSUS25	0.0042		mA	STR
$I_{SUS25SOF}$	Power Supply Current – VSUS25	0		mA	Soft-Off
I_{CC5}	Power Supply Current – VCC5			mA	Max operating frequency
I_{CCRGB}	Power Supply Current – VCCRGB			mA	Max operating frequency
I_{CCA}	Power Supply Current – VCCA			mA	Max operating frequency
I_{CCDAC}	Power Supply Current – VCCDAC			mA	Max operating frequency
I_{CCPLL1}	Power Supply Current – VCCPLL1			mA	Max operating frequency
I_{CCPLL2}	Power Supply Current – VCCPLL2			mA	Max operating frequency
I_{CCLPLL}	Power Supply Current – VCCLPLL			mA	Max operating frequency
I_{CCLVDS}	Power Supply Current – VCCLVDS			mA	Max operating frequency
I_{DDD}	Power Supply Current – VDDD			mA	Max operating frequency
P_D	Power Dissipation			W	Max operating frequency

AC Timing Specifications

AC timing specifications provided are based on external zero-pf capacitance load. Min/max cases are based on the following table:

Table 19. AC Timing Min / Max Conditions

Parameter	Min	Max	Unit
3.3V Power (I/O Pads, VCCQ for 2x transfer mode)	3.135	3.465	Volts
2.5V Power (Internal Logic)	2.375	2.625	Volts
2.5V Power (CPU Interface Logic)	2.375	2.625	Volts
1.5V Power (VCCQ for 4x transfer mode)	1.425	1.575	Volts
Case Temperature	0	85	^{O}C

Drive strength for selected output pins is programmable. See Rx6D for details.

MECHANICAL SPECIFICATIONS

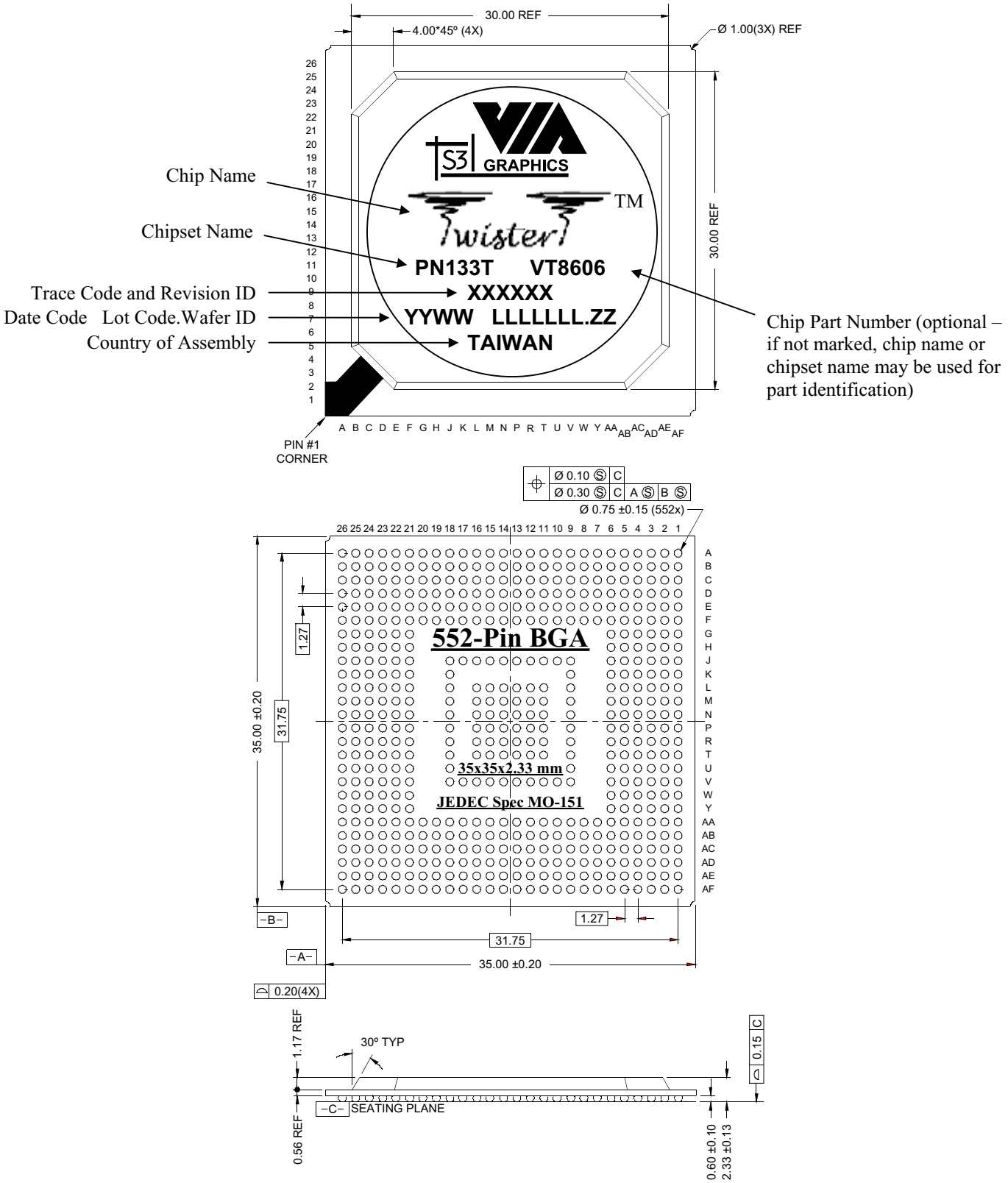


Figure 6. Mechanical Specifications - 552-Pin HSBGA Ball Grid Array Package with Heat Spreader