P4X400 Chipset

VT8754

Single-Chip North Bridge
for Pentium 4 CPUs with 533 / 400 MHz FSB
and 8x / 4x / 2x AGP Bus
plus Advanced ECC Memory Controller
supporting DDR333, 266, and 200
(PC2700 / 2100 / 1600) DDR DRAM
for Desktop PC Systems

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REVISION HISTORY

Document Release	Date	Revision	Initials
0.1	12/18/01	Initial internal release based on P4X266A data sheet rev 1.0 published 12/5/01 Updated cover, block diagram and feature bullets to add AGP 8x and DDR 333 Updated pin diagram per project #3168 engg ballout rev 1.2 dated 12/7/01 Updated pin lists, updated AGP pin descriptions for AGP 8x mode Added missing CPU, AGP, DRAM, V-Link and Miscellaneous pins Replaced mechanical spec with HSBGA-859	DH
0.2	1/3/02	Fixed SDRAM feature bullets; Changed mechanical spec to HSBGA-858 Updated pinouts to match engineering ballout 1.5 (removed VCC25 ball at AA10)	DH
0.3	2/8/02	Fixed PC2700 notation; fixed various formatting and typographical errors Fixed/updated ball count, AGP 8x, V-Link and DRAM feature bullets & overview Updated block diagram, feature bullets & overview to use VT8235 south bridge Updated strap definitions; Removed SDR support Updated Device 0 Rx13-10, 41, 43-44, 47-49, 4B-4C, 4F-52, 54-55, 60, 63, 66-67, 6A-6E, 70, 80-83, A4-B0, B2, B4-B6, B8-BA, BC-BE, D0-D6, DA-DB, E0-E3, E6, E8-EF, Device 1 Rx3-2, F, 48 Replaced mech spec with correct 858-ball diagram	DH
0.31	2/11/02	Regenerated pdf file to fix non-printing mechnical spec diagram	DH
0.4	2/27/02	Added P4X333 “product logo” to cover page and page headers Fixed first main feature bullet to target high performance PC desktop systems Fixed Figure 1 block diagram (bad diagram printout due to MS-Word bug) Changed V-Link to 533 MB/sec in feature bullets and overview Fixed errors and typos (package pin count, # of PCI slots, etc) in Overview text Fixed mistakes in power/ground pin lists at bottom of pin list tables 1 and 2 Fixed part number and product name typos in pin descriptions Fixed register references in memory pin descriptions and electrical specs Fixed voltages in AGPVREF, VCCMEM, and VCCAGP pin descriptions	DH
0.5	2/28/02	Fixed AGPVREF and AGPVCC pin descriptions Device 0 Fixed Rx3-2 default, 52[5], 53-54, A7-A4 default, 64[6-4], 69[6], B2[7] Device 0 Removed Rx52[4], 67[7-6], B4 (8233 configuration only)	DH
0.6	3/11/02	Fixed P4X400 logo to print in color; changed max memory to 16GB Added feature bullet to include support for both registered and unbuffered DIMMs Changed pins AK7 and AJ16 to NC; Updated AGPVREF pin description Added pin type and pin name to GCKE, HDP[3-0], AP[1-0], RSP#, NMI, GSERR# Updated Table 7 MA Mapping to add 512Mb and 1Gb DRAMs; Updated Rx69[6]	DH
0.7	4/5/02	Fixed VIA USA address and VIA Taiwan fax # on legal page Fixed VLVREF pin description; Fixed typographical error in mech spec drawing	DH
0.71	4/22/02	Corrected TW fax number; Corrected typo in pin diagram in VCCVL pin names Updated block diagram to show six PCI slots for VT8235 south bridge	DH
0.72	5/29/02	Fixed feature bullet error (AGP 8x not 4x in first sub-bullet); Updated table 6	DH
0.8	6/25/02	Changed chip name from P4X333 to P4X400	DH
0.9	7/19/02	Updated Device 0 Rx0D[2-1], 47[7-6,1], 4D, 51[0], 60[7-6] (default), 69[6], A8[7-6,3], B0[7] (& register name in sumary tables), B1 (register name), EE, EF[1-0] Replaced Rx80-B3, F0-FF (AGP 2.0/3.0 regs) from KT400 data sheet rev 0.42	DH
0.91	7/19/02	Increased size of figure 1 block diagram; Fixed Rx13-10, 34	DH
0.92	1/14/03	Updated VIA logos on cover page and page headers to use new corporate logo Updated DDR notation; Fixed VAD7 strap definition and updated Rx50[6] Removed misleading “strap” label from VAD pins (straps are on south bridge)	DH

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PRODUCT FEATURES

- **Defines Highly Integrated Solutions for Performance PC Desktop Designs**
  - High performance North Bridge with 533 MHz Front Side Bus for Pentium™ 4 plus AGP 8x external bus
  - 64-bit Advanced ECC Memory controller supporting DDR333 / 266 / 200 DDR Synchronous DRAM
  - Combines with VIA VT8235 V-Link South Bridge for integrated LAN, Audio, ATA133 IDE, and 6 USB 2.0 ports
  - 2.5V Core and AGTL+ I/O
  - 35 x 35mm HSBGA package (Ball Grid Array with Heat Spreader) with 858 balls and 1mm ball pitch
- **High Performance CPU Interface**
  - Support for Intel™ Pentium 4 processors with 533 MHz (4 x 133 MHz) CPU Front Side Bus (FSB)
  - Built-in Phase Lock Loop circuitry for optimal skew control within and between clocking regions
  - Thirteen outstanding transactions (twelve In-Order Queue (IOQ) plus one output latch)
  - Dynamic deferred transaction support
- **Full Featured Accelerated Graphics Port (AGP) Controller**
  - Supports 533 MHz 8x, 266 MHz 4x, and 133 MHz 2x transfer modes for AD and SBA signaling
  - AGP v3.0 compliant with 8x transfer mode
  - Pseudo-synchronous with the host CPU bus with optimal skew control
  - Supports SideBand Addressing (SBA) mode (non-multiplexed address / data)
  - AGP pipelined split-transaction long-burst transfers up to 1GB/sec
  - Eight level read request queue
  - Four level posted-write request queue
  - Thirty-two level (quadwords) read data FIFO (256 bytes)
  - Sixteen level (quadwords) write data FIFO (128 bytes)
  - Intelligent request reordering for maximum AGP bus utilization
  - Supports Flush/Fence commands
  - Graphics Address Relocation Table (GART)
    - One level TLB structure
    - Sixteen entry fully associative page table
    - LRU replacement scheme
    - Independent GART lookup control for host / AGP / PCI master accesses
  - Windows 95 OSR-2 VXD and integrated Windows 98 / Windows 2000 miniport driver support

- **Advanced High-Performance DDR DRAM Controller**
  - Supports DDR333, DDR266, and DDR200 double-data-rate synchronous DRAM
  - DRAM interface pseudo-synchronous with host CPU (166 / 133 / 100 MHz) for most flexible configuration
  - DRAM interface may be faster or slower than CPU FSB by 33 MHz
  - Concurrent CPU, AGP, and V-Link access
  - Clock Enable (CKE) control for DRAM power reduction in high speed systems
  - Mixed 1M / 2M / 4M / 8M / 16M / 32M / 64M / 128M x 8/16/32 DRAMs
  - Supports 8 banks up to 16 GB DRAMs
  - Allows use of either unbuffered or registered memory modules
  - Flexible row and column addresses. 64-bit data width only
  - 2.5V SSTL-2 DRAM interface
  - Programmable I/O drive capability for MA, MD, and command signals
  - Dual copies of MA and control signals for improved drive
  - ECC (single-bit error correction and multi-bit error detection) or EC (error checking only) for DRAM integrity
  - Two-bank interleaving for 16Mbit DRAM support
  - Four bank interleaving for 64Mb, 128Mb, 256Mb, 512Mb, and 1Gb DRAM support
  - Supports maximum 16-bank interleave (i.e., 16 pages open simultaneously); banks are allocated based on LRU
  - Seamless DRAM command scheduling for maximum DRAM bus utilization
    - (e.g., precharge other banks while accessing the current bank)
  - Four cache lines (16 quadwords) of CPU to DRAM write buffers
  - Four cache lines of CPU to DRAM read prefetch buffers
  - Read around write capability for non-stalled CPU read
  - Speculative DRAM read before snoop result
  - Burst read and write operation
  - Burst length 4 and 8
  - Supports CL 2/2.5 and 1T per command
  - 1T and 2T command rate which can be specified bank by bank
  - Decoupled and burst DRAM refresh with staggered RAS timing (CAS before RAS or self refresh)
- **High Bandwidth 533 MB / Sec 8-bit V-Link Host Controller**
  - Supports 66 MHz V-Link Host interface with peak bandwidth of 533 MB/sec
  - Operates in 2x, 4x, and 8x modes
  - Full duplex commands with separate command / strobe
  - Request / Data split transaction
  - Configurable outstanding transaction queue for Host to V-Link Client accesses
  - Supports Defer / Defer-Reply transactions
  - Transaction assurance for V-Link Host to Client access eliminates V-Link Host-Client Retry cycles
  - Intelligent V-Link transaction protocol to eliminate data wait-state / throttle transfer latency
  - All V-Link transactions for both Host and Client have a consistent view of transaction data depth and buffer size to avoid data overflow
  - Highly efficient V-Link arbitration with minimum overhead
  - All V-Link transactions have predictable cycle length with known command / data duration
- **Advanced System Power Management Support**
  - Dynamic power down of DRAM (CKE)
  - VTT suspend power plane preserves memory data
  - Suspend-to-DRAM and self-refresh power down
  - Low-leakage I/O pads
  - ACPI 1.0B and PCI Bus Power Management 1.1 compliant

OVERVIEW

The P4X400 (VT8754 North Bridge plus VT8235 South Bridge) is a high performance, cost-effective and energy efficient chip set for the implementation of desktop personal computer systems with 533 MHz (4x133 MHz) or 400 MHz (4x100 MHz) CPU host bus ("Front Side Bus") based on 64-bit Intel Pentium-4 super-scalar processors.

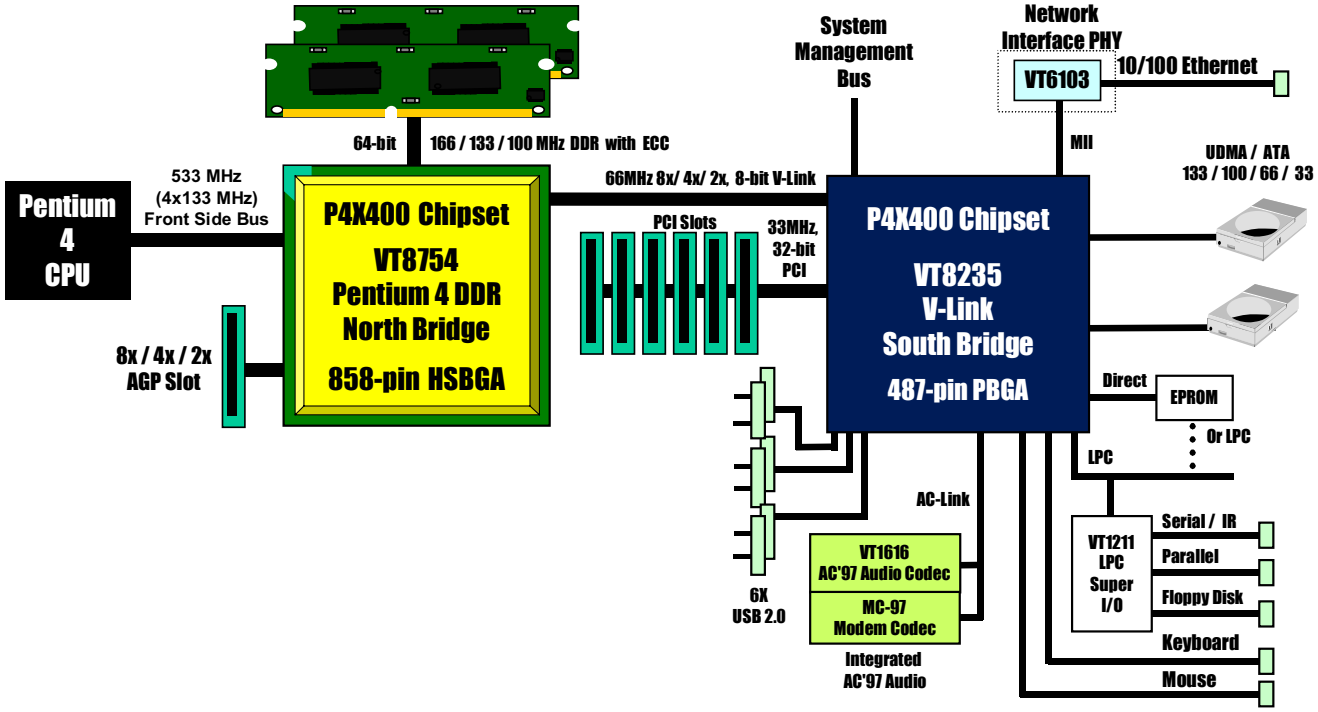


Figure 1. P4X400 Chipset System Block Diagram

The P4X400 chip set consists of the VT8754 North Bridge (858-pin BGA) and the VT8235 V-Link South Bridge (487 pin BGA). The VT8754 (sometimes also called a "Host System Controller") is an update of VIA's VT8753A (P4X266A) with a faster DDR memory interface and a new pinout enhanced to add AGP 8x functionality. The VT8754 provides superior performance between the CPU, DRAM, V-Link bus and AGP 8x graphics controller bus with pipelined, burst, and concurrent operation. The VT8235 (which may also be referred to as a "V-Link Client Controller") is a highly integrated PCI / LPC controller. Its internal bus structure is based on a 66 MHz PCI bus that provides 2x / 4x / 8x bandwidth compared to previous generation PCI bridge chips. The VT8235 also provides a 533 MB/sec bandwidth Host / Client V-Link interface with V-Link-PCI and V-Link-LPC controllers. It supports six PCI slots of arbitration and decoding for all integrated functions and LPC bus.

The VT8754 supports eight banks of DDR Synchronous DRAMs (SDRAMs) up to 16 GB. The DRAM controller supports DDR333, DDR266, and DDR200 (PC2700 / PC2100 / PC1600) Double-Data-Rate (DDR) SDRAM. The DDR DRAM interface allows zero wait state bursting between the DRAM and the data buffers at 166 / 133 / 100 MHz. The different banks of DRAM can be composed of an arbitrary mixture of 1M / 2M / 4M / 8M / 16M / 32M / 64M / 128M x 8/16/32 DRAMs. Both unbuffered and registered memory modules are supported. The DRAM controller also supports optional ECC (single-bit error correction and multi-bit detection) or EC (error checking) capability. The DRAM controller can run either synchronous or pseudo-synchronous with the host CPU bus.

The VT8754 supports a high speed 8-bit 8x 66 MHz Quad Data Transfer interconnect (V-Link) to the VT8235 South Bridge. The chip also contains a built-in bus-to-bus bridge to allow simultaneous concurrent operations on each bus. Five levels (doublewords) of post write buffers are included to allow for concurrent CPU and V-Link operation. For V-Link Host operation, forty-eight levels (doublewords) of post write buffers and sixteen levels (doublewords) of prefetch buffers are included for concurrent V-Link bus and DRAM/cache accesses. When combined, the V-Link Host / Client controllers realize a complete PCI sub-system and

support enhanced PCI bus commands such as “Memory-Read-Line”, “Memory-Read-Multiple” and “Memory-Write-Invalid” commands to minimize snoop overhead. In addition, advanced features are supported such as snoop ahead, snoop filtering, L1 write-back forward to PCI master, and L1 write-back merged with PCI post write buffers to minimize PCI master read latency and DRAM utilization. Delay transaction and read caching mechanisms are also implemented for further improvement of overall system performance.

The 487-pin Ball Grid Array VT8235 Client V-Link PCI / LPC controller supports four levels (doublewords) of line buffers, type F DMA transfers and delay transaction to allow efficient PCI bus utilization and (PCI-2.1 compliant). The VT8235 integrated PCI controller and PCI arbitration for up to five PCI slots. One of the PCI REQ / GNT pairs can be configured as high-priority to better support a low latency PCI bus master device. The VT8235 integrated networking MAC controller with standard MII interface to an external PHY for 10/100Mb base-T Ethernet or 1/10Mb PNA home networking.

The VT8235 also includes an integrated keyboard controller with PS2 mouse support, integrated DS12885 style real time clock with extended 256 byte CMOS RAM, integrated master mode enhanced IDE controller with full scatter / gather capability and extension to UltraDMA-133/100/66/33 for 133/100/66/33 MB/sec transfer rate, integrated USB 2.0 interface with three root hubs and six functional ports with built-in physical layer transceivers, Distributed DMA support, and OnNow / ACPI compliant advanced configuration and power management interface.

For sophisticated power management, the P4X400 chipset provides independent clock stop controls for the CPU / SDRAM and AGP bus plus Dynamic CKE control for powerdown of the SDRAM. A separate suspend-well plane is implemented for the SDRAM control signals for Suspend-to-DRAM operation. Coupled with the VT8235 south bridge chip, a complete power conscious PC main board can be implemented with no external TTLs.

PINOUTS

Figure 2. VT8754 / P4X400 Ball Diagram (Top View)

Key	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34
A	G STOP#	G DSEL#	G TRDY#	GD18	GD17	GD19	G BE3#	GD23	GD28	SBA 5	SBA 3	G RBF#	G GNT#	AGP 8XDT#	VCC 25	VCC 25	VCC 25	CPU RST#	HD62#	HD63#	HD55#	HD51#	HD48#	HD43#	HDBI 2#	HDS 2#	HD37#	HD P0	HD26#	HD28#	HD30#	HD22#	HD19#	HD20#
B	VCC AGP	GND	GND	G BE2#	GD16	GND	GD21	GD26	GND	SBA 7	SBA 1	GND	ST1	GND	VCC 25	VCC 25	VCC 25	GND	HD60#	HD56#	GND	HD54#	HD49#	GND	HD42#	HDS 2	GND	HD P2	HD31#	GND	HDS 1#	HD16#	GND	HD21#
C	VCC AGP	VCC AGP	GND	G IRDY#	G FRM#	GD25	GD22	GDS1 GDS1F	GD29	SBA 6	SBS# SBSS	SBA 2	G PIPE#	G REQ#	VCC 25	VCC 25	VCC 25	GND	HD61#	HD57#	HDS 3	HD53#	HD50#	HD44#	HD41#	HD38#	HD39#	HD35#	HD29#	HDBI 1#	HDS 1	HD23#	HD17#	HD18#
D	VCC AGP	VCC AGP	VCC AGP	GND	GND	GD20	GD27	GDS1# GDS1S	GD30	GDBIL	SBS SBSF	SBA 0	G WBF#	ST0	VCC 25	VCC 25	VCC 25	GND	HD58#	HD59#	HDS 3#	HD52#	HD47#	HD45#	HD34#	HD33#	HD32#	HD P3	HD25#	HD24#	HD7#	HD14#	GND	HD15#
E	VCC AGP	VCC AGP	VCC AGP	VCC AGP	GND	GND	GD24	GD31	GND	GDBIH GPIPE#	SBA 4	GND	ST2	VCC 25	VCC 25	VCC 25	VCC 25	GND	GND	GND	GND	HDBI 3#	HD46#	GND	HD40#	HD36#	GND	HD P1	HD27#	GND	HD10#	HDS 0#	HD13#	HD12#
F	G SERR#	VCC AGP	VCC AGP	VCC AGP	VCC AGP	GND	GND	GND	GND	AGP VREF	GND	GND	GND	VCC 25	VCC 25	VCC 25	VCC 25	GND	HD VREF	GND	GND	GND	GND	HD VREF	GND TT	GND	GND	HD VREF	GND	HD11#	GND	HDS 0	GND	HD9#
G	GD14	G BE1#	VCC AGP	VCC AGP	VCC AGP	VCC AGP	F7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	G28	GND	HDBI 0#	HD3#	HD8#	HD2#	HD6#
H	GD12	GND	GND	VCC AGP	VCC AGP	VCC AGP	H	AGP Pins																				H	GND	HCMP VREF	HR COMP	HD5#	HD4#	HD1#
J	GD8	GD10	G PAR	GND	VCC AGP	VCC AGP	J					J12	13	J14				J18	19	20	21	J22						J	HD VREF	GND	GND	GND	GND	HD0#
K	G BE0#	GD7	GDS0 GDS0F	GDS0# GDS0S	GND	VCC AGP	K				K11	VCC 25	VCC 25	VCC 25	K15	16	K17	VCC 25	VCC 25	VCC 25	VCC 25	VCC 25	K23					K	VTT	VTT	VTT	VTT	VTT	VTT
L	GD6	GND	GD5	GD11	GD15	GND	L				L11	VCC AGP	VCC AGP	VCC AGP	VCC AGP	VCC AGP	VCC AGP	VTT	VTT	VTT	VTT	VTT	VTT	L24				L	VTT	VTT	VTT	VTT	VTT	VTT
M	GD2	GD4	GD0	GND	GD13	AGP VREF	M			M10	VCC AGP	VCC AGP	VCC AGP	VCC AGP	VCC AGP	VCC AGP	VCC AGP	VTT	VTT	VTT	VTT	VTT	VTT	VTT	M25		CPU	M	VTT	VTT	VTT	VTT	VTT	VTT
N	GD1	VAD 4	GD3	GD9	G CLK	VCC QQ	N			N10	VCC AGP	VCC AGP	N13	14	15	16	17	18	19	20	21	N22	VTT	VTT	N		Pins	N	VTT	VTT	VTT	VTT	VTT	VTT
P	VAD 5	GND	V PAR	GND QQ	AGP COMP	GND	P		P9	VCC 25	VCC AGP	VCC AGP	P	GND	GND	GND	GND	GND	GND	GND	GND	P	VTT	VTT	P			P	VTT	VTT	VTT	VTT	VTT	NMI
R	V BE#	VAD 1	VAD 0	GND	GND	GND	R		R	VCC 25	VCC AGP	VCC AGP	R	GND	GND	GND	GND	GND	GND	GND	GND	R	VTT	VTT	R25			R	GND	GND	GND	GND	GND	BPRI#
T	UP STB#	UP STB	DN STB#	DN STB	DN CMD	GND	T	V- Link Pins	T9	VCC 25	VCC VL	VCC VL	T	GND	GND	GND	GND	GND	GND	GND	GND	T	VTT	VTT	VCC 25	T26		T	H CLK#	VCC HCK1	GND HCK1	DE FER#	GND	HITM#
U	VAD 6	GND	VAD 7	VAD 3	VAD 2	VL COMP	U			U10	VCC VL	VCC VL	U	GND	GND	GND	GND	GND	GND	GND	GND	U	VTT	VTT	VCC 25	U		U	H CLK	VCC HCK2	GND HCK2	RS 2#	RS 0#	HIT#
V	SUS ST#	UP CMD	VL VREF	GND	VSUS 25	GND	V			V10	VCC VL	VCC MEM	V	GND	GND	GND	GND	GND	GND	GND	GND	V	VTT	VTT	VCC 25	V		V	GTL VREF	RS1#	BNR#	D BSY#	H LOCK#	ADS#
W	RE SET#	GND	PWR OK#	GND	GND	VCC VL	W		W9	VCC 25	VCC MEM	VCC MEM	W	GND	GND	GND	GND	GND	GND	GND	GND	W	VTT	VTT	VCC 25	W		W	GND	GND	HT RDY#	B REQ#	GND	D RDY#
Y	VCC VL	VCC VL	VCC VL	VCC VL	VCC VL	VCC VL	Y			Y10	VCC MEM	VCC MEM	Y	GND	GND	GND	GND	GND	GND	GND	GND	Y	VTT	VTT	VCC 25	Y		Y	GND	HA4	HREQ 2#	HA3	HREQ 0#	HREQ 4#
AA	VCC VL	VCC VL	VCC VL	VCC VL	VCC VL	VCC VL	AA			AA10	VCC MEM	VCC MEM	AA	GND	GND	GND	GND	GND	GND	GND	GND	AA	VTT	VTT	VCC 25	AA		AA	HA VREF	HAS 0#	HREQ 3#	HA9	HA7	HA6
AB	VCC MEM	VCC MEM	VCC MEM	VCC MEM	VCC MEM	VCC MEM	AB		AB9	VCC 25	VCC MEM	VCC MEM	AB13	14	15	16	17	18	19	20	21	AB22	GND	VCC MEM	VCC 25	AB26		AB	GND TT	GND	HA5	HREQ 1#	GND	HA11
AC	VCC MEM	VCC MEM	VCC MEM	VCC MEM	VCC MEM	VCC MEM	AC			AC10	VCC MEM	VCC MEM	VCC MEM	VCC MEM	VCC MEM	VCC MEM	VCC MEM	VCC MEM	VCC MEM	VCC MEM	VCC MEM	VCC MEM	VCC MEM	VCC MEM	AC25			AC	GND	HA16	HA8	HA14	HA13	HA10
AD	VCC MEM	VCC MEM	VCC MEM	VCC MEM	VCC MEM	VCC MEM	AD				AD11	VCC MEM	VCC MEM	VCC MEM	VCC MEM	VCC MEM	VCC MEM	VCC MEM	VCC MEM	VCC MEM	VCC MEM	VCC MEM	VCC MEM	AD24				AD	HA VREF	HA24	HA20	HA18	HA15	HA12
AE	MD63	GND	MD59	GND	GND	GND	AE				AE11	VCC 25	VCC 25	VCC 25	VCC 25	VCC 25	VCC 25	VCC 25	VCC 25	VCC 25	VCC 25	AE22	AE23					AE	GND	GND	HA19	HA21	GND	HA17
AF	MD62	MD58	DQS 7#	SCAS B#	SCAS A#	MEM VREF	AF					AF12	13	14	15	16	17	18	19	20	AF21							AF	GND	HA28	HAS 1#	HA25	HA23	HA22
AG	MD57	MD61	DQM 7	SWE A#	SWE B#	GND	AG										Mem Pins											AG	GND	HA26	HA30	HA33	HA27	HA32
AH	MD56	GND	MD60	MD51	GND	GND	AH7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	AH28	GND	GND	RSP#	HAP 1	GND	HA29
AJ	MD55	MD50	MD54	GND	SRAS A#	MAA 10	MAB 10	GND	GND	GND	MEM VREF	VCC MDLL	GND MDLL	GND	GND	NC	MEM VREF	GND	GND	GND	GND	GND	MEM VREF	GND	GND	VCC MEM	VCC MEM	VCC MEM	VCC MEM	VCC MEM	HAP 0	HA35	HA31	HA34
AK	DQS 6#	DQM 6	MAB 11	SRAS B#	MAA 11	MAA 12	NC	GND	MAB 1	GND	GND	MAA 3	GND	GND	MAB 6	MAA 5	GND	MAB 8	MAA 7	GND	MAA 14	MAA 15	GND	MAB 15	GCKE	VCC MEM	VCC MEM	VCC MEM	VCC MEM	VCC MEM	VCC MEM	VCC MCK	GND MCK	MCLK
AL	MD53	GND	MD52	MD49	GND	MAB 12	MD45	MAB 0	MAA 1	MAA 2	MAB 2	MECC 6	MECC 2	MAA 4	MD27	MAA 6	MAA 8	MD24	MAB 7	MAA 13	MAB 13	MAB 14	MD20	DQS 1#	GND	VCC MEM	VCC MEM	VCC MEM	VCC MEM	VCC MEM	VCC MEM	VCC MEM	VCC MEM	MCLK FB
AM	MD48	MD47	MD46	CS5#	MD42	CS2#	MD40	MAA 0	MD38	MD34	MAB 3	MD32	MECC 1	MAB 4	MD31	MAB 5	DQS 3#	MD28	MD22	MAA 9	MAB 9	MD21	MD11	DQM 1	MD8	MD3	MD2	MD1	VCC MEM	VCC MEM	VCC MEM	VCC MEM	VCC MEM	TEST IN#
AN	MD43	GND	CS4#	DQS 5#	GND	CS0#	MD35	GND	DQS 4#	MD37	GND	MECC 7	DQS 8#	GND	MECC 5	MD26	GND	MD29	MD19	GND	DQM 2	MD17	GND	MD15	MD12	GND	MD6	DQS 0#	GND	MD4	VCC MEM	VCC MEM	VCC MEM	VCC MEM
AP	CS7#	CS6#	CS3#	DQM 5	CS1#	MD41	MD44	MD39	DQM 4	MD33	MD36	MECC 3	DQM 8	MECC 0	MECC 4	MD30	DQM 3	MD25	MD23	MD18	DQS 2#	MD16	MD10	MD14	MD13	MD9	MD7	DQM 0	MD5	MD0	VCC MEM	VCC MEM	VCC MEM	VCC MEM

Table 1. Pin List (Numerical Order)

Pin #		Pin Name	Pin #		Pin Name	Pin #		Pin Name	Pin #		Pin Name	Pin #		Pin Names	Pin #		Pin Name
A01	IO	GSTOP#	C26	IO	HD38#	H32	IO	HD05#	W01	I	RESET#	AJ06	O	MAA10	AM13	IO	MECC1 / CKE1
A02	IO	GDEVSEL#	C27	IO	HD39#	H33	IO	HD04#	W03	I	PWROK	AJ07	O	MAB10	AM14	O	MAB04
A03	IO	GTRDY#	C28	IO	HD35#	H34	IO	HD01#	W31	IO	HTRDY#	**AJ11**	**P**	**MEMVREF**	AM15	IO	MD31
A04	IO	GD18	C29	IO	HD29#	J01	IO	GD8	W32	O	BREQ#	**AJ12**	**P**	**VCCMDLL**	AM16	O	MAB05
A05	IO	GD17	C30	IO	HDBI1#	J02	IO	GD10	W34	IO	DRDY#	**AJ13**	**P**	**GNDMDLL**	AM17	IO	DQS3# / CKE3
A06	IO	GD19	C31	IO	HDS1	J03	IO	GPAR	Y30	IO	HA04	AJ16		NC	AM18	IO	MD28
A07	IO	GBE3#	C32	IO	HD23#	**J29**	**P**	**HDVREF**	Y31	IO	HREQ2#	**AJ17**	**P**	**MEMVREF**	AM19	IO	MD22
A08	IO	GD23	C33	IO	HD17#	J34	IO	HD00#	Y32	IO	HA03	**AJ23**	**P**	**MEMVREF**	AM21	O	MAB09
A09	IO	GD28	C34	IO	HD18#	K01	IO	GBE0#	Y33	IO	HREQ0#	AJ31	IO	HAP0	AM22	IO	MD21
A10	I	SBA5	D06	IO	GD20	K02	IO	GD7	Y34	IO	HREQ4#	AJ32	IO	HA35	AM23	IO	MD11
A11	I	SBA3	D07	IO	GD27	K03	IO	GDS0 / GDS0F	**AA29**	**P**	**HAVREF**	AJ33	IO	HA31	AM24	O	DQM1 / CKE1
A12	I	GRBF#	D08	IO	GDS1# / GDS1S	K04	IO	GDS0# / GDS0S	AA30	IO	HAS0#	AJ34	IO	HA34	AM25	IO	MD08
A13	O	GGNT#	D09	IO	GD30	L01	IO	GD6	AA31	IO	HREQ3#	AK01	IO	DQS6# / CKE6	AM26	IO	MD03
A14	I	AGP8XDT#	D10	IO	GDBIL	L03	IO	GD5	AA32	IO	HA09	AK02	O	DQM6 / CKE6	AM27	IO	MD02
A18	O	CPURST#	D11	I	SBS / SBSF	L04	IO	GD11	AA33	IO	HA07	AK03	O	MAB11	AM28	IO	MD01
A19	IO	HD62#	D12	I	SBA0	L05	IO	GD15	AA34	IO	HA06	AK04	O	SRASB#	AM30	O	MAA09
A20	IO	HD63#	D13	I	GWBF#	M01	IO	GD2	**AB29**	**P**	**GNDTT**	AK05	O	MAA11	AM34	I	TESTIN#
A21	IO	HD55#	D14	O	ST0	M02	IO	GD4	AB31	IO	HA05	AK06	O	MAA12	AN01	IO	MD43
A22	IO	HD51#	D19	IO	HD58#	M03	IO	GD0	AB32	IO	HREQ1#	AK07	–	NC	AN03	O	CS4#
A23	IO	HD48#	D20	IO	HD59#	M05	IO	GD13	AB34	IO	HA11	AK09	O	MAB01	AN04	IO	DQS5# / CKE5
A24	IO	HD43#	D21	IO	HDS3#	**M06**	**P**	**AGPVREF**	AC30	IO	HA16	AK12	O	MAA03	AN06	O	CS0#
A25	IO	HDBI2#	D22	IO	HD52#	N01	IO	GD1	AC31	IO	HA08	AK15	O	MAB06	AN07	IO	MD35
A26	IO	HDS2#	D23	IO	HD47#	N02	IO	VAD4	AC32	IO	HA14	AK16	O	MAA05	AN09	IO	DQS4# / CKE4
A27	IO	HD37#	D24	IO	HD45#	N03	IO	GD3	AC33	IO	HA13	AK18	O	MAB08	AN10	IO	MD37
A28	IO	HDP0	D25	IO	HD34#	N04	IO	GD9	AC34	IO	HA10	AK19	O	MAA07	AN12	IO	MECC7 / CKE7
A29	IO	HD26#	D26	IO	HD33#	N05	I	GCLK	**AD29**	**P**	**HAVREF**	AK21	O	MAA14	AN13	IO	DQS8#
A30	IO	HD28#	D27	IO	HD32#	**N06**	**P**	**VCCQQ**	AD30	IO	HA24	AK22	O	MAA15	AN15	IO	MECC5 / CKE5
A31	IO	HD30#	D28	IO	HDP3	P01	IO	VAD5	AD31	IO	HA20	AK24	O	MAB15	AN16	IO	MD26
A32	IO	HD22#	D29	IO	HD25#	P03	IO	VPAR	AD32	IO	HA18	AK25	O	GCKE	AN18	IO	MD29
A33	IO	HD19#	D30	IO	HD24#	**P04**	**P**	**GNDQQ**	AD33	IO	HA15	**AK32**	**P**	**VCCMCK**	AN19	IO	MD19
A34	IO	HD20#	D31	IO	HD07#	P05	AI	AGPCOMP	AD34	IO	HA12	**AK33**	**P**	**GNDMCK**	AN21	O	DQM2 / CKE2
B04	IO	GBE2#	D32	IO	HD14#	P34	O	NMI	AE01	IO	MD63	AK34	O	MCLK	AN22	IO	MD17
B05	IO	GD16	D34	IO	HD15#	R01	IO	VBE#	AE03	IO	MD59	AL01	IO	MD53	AN24	IO	MD15
B07	IO	GD21	E07	IO	GD24	R02	IO	VAD1	AE31	IO	HA19	AL03	IO	MD52	AN25	IO	MD12
B08	IO	GD26	E08	IO	GD31	R03	IO	VAD0	AE32	IO	HA21	AL04	IO	MD49	AN27	IO	MD06
B10	I	SBA7	E10	IO	GDBIH / GPIPE#	R34	IO	BPRI#	AE34	IO	HA17	AL06	O	MAB12	AN28	IO	DQS0# / CKE0
B11	I	SBA1	E11	I	SBA4	T01	I	UPSTB#	AF01	IO	MD62	AL07	IO	MD45	AN30	IO	MD04
B13	O	ST1	E13	O	ST2	T02	I	UPSTB	AF02	IO	MD58	AL08	O	MAB00	AP01	O	CS7#
B19	IO	HD60#	E22	IO	HDBI3#	T03	O	DNSTB#	AF03	IO	DQS7# / CKE7	AL09	O	MAA01	AP02	O	CS6#
B20	IO	HD56#	E23	IO	HD46#	T04	O	DNSTB	AF04	O	SCASB#	AL10	O	MAA02	AP03	O	CS3#
B22	IO	HD54#	E25	IO	HD40#	T05	O	DNCMD	AF05	O	SCASA#	AL11	O	MAB02	AP04	O	DQM5 / CKE5
B23	IO	HD49#	E26	IO	HD36#	T29	I	HCLK#	**AF06**	**P**	**MEMVREF**	AL12	IO	MECC6 / CKE6	AP05	O	CS1#
B25	IO	HD42#	E28	IO	HDP1	**T30**	**P**	**VCCHCK1**	AF30	IO	HA28	AL13	IO	MECC2 / CKE2	AP06	IO	MD41
B26	IO	HDS2	E29	IO	HD27#	**T31**	**P**	**GNDHCK1**	AF31	IO	HAS1#	AL14	O	MAA04	AP07	IO	MD44
B28	IO	HDP2	E31	IO	HD10#	T32	IO	DEFER#	AF32	IO	HA25	AL15	IO	MD27	AP08	IO	MD39
B29	IO	HD31#	E32	IO	HDS0#	T34	I	HITM#	AF33	IO	HA23	AL16	O	MAA06	AP09	O	DQM4 / CKE4
B31	IO	HDS1#	E33	IO	HD13#	U01	IO	VAD6	AF34	IO	HA22	AL17	O	MAA08	AP10	IO	MD33
B32	IO	HD16#	E34	IO	HD12#	U03	IO	VAD7	AG01	IO	MD57	AL18	IO	MD24	AP11	IO	MD36
B34	IO	HD21#	F01	IO	GSERR#	U04	IO	VAD3	AG02	IO	MD61	AL19	O	MAB07	AP12	IO	MECC3 / CKE3
C04	IO	GIRDY#	**F10**	**P**	**AGPVREF**	U05	IO	VAD2	AG03	O	DQM7 / CKE7	AL20	O	MAA13	AP13	O	DQM8
C05	IO	GFRM#	**F19**	**P**	**HDVREF**	U06	AI	VLCOMP	AG04	O	SWEA#	AL21	O	MAB13	AP14	IO	MECC0 / CKE0
C06	IO	GD25	**F24**	**P**	**HDVREF**	U29	I	HCLK	AG05	O	SWEB#	AL22	O	MAB14	AP15	IO	MECC4 / CKE4
C07	IO	GD22	**F25**	**P**	**GNDTT**	**U30**	**P**	**VCCHCK2**	AG30	IO	HA26	AL23	IO	MD20	AP16	IO	MD30
C08	IO	GDS1 / GDS1F	**F28**	**P**	**HDVREF**	**U31**	**P**	**GNDHCK2**	AG31	IO	HA30	AL24	IO	DQS1# / CKE1	AP17	O	DQM3 / CKE3
C09	IO	GD29	F30	IO	HD11#	U32	IO	RS2#	AG32	IO	HA33	AL34	I	MCLKF	AP18	IO	MD25
C10	I	SBA6	F32	IO	HDS0	U33	IO	RS0#	AG33	IO	HA27	AM01	IO	MD48	AP19	IO	MD23
C11	I	SBS# / SBSS	F34	IO	HD09#	U34	IO	HIT#	AG34	IO	HA32	AM02	IO	MD47	AP20	IO	MD18
C12	I	SBA2	G01	IO	GD14	V01	I	SUSST#	AH01	IO	MD56	AM03	IO	MD46	AP21	IO	DQS2# / CKE2
C13	I	GPIPE#	G02	IO	GBE1#	V02	I	UPCMD	AH03	IO	MD60	AM04	O	CS5#	AP22	IO	MD16
C14	I	GREQ#	G30	IO	HDBI0#	**V03**	**P**	**VLVREF**	AH04	IO	MD51	AM05	IO	MD42	AP23	IO	MD10
C19	IO	HD61#	G31	IO	HD03#	**V05**	**P**	**VSUS25**	AH31	O	RSP#	AM06	O	CS2#	AP24	IO	MD14
C20	IO	HD57#	G32	IO	HD08#	**V29**	**P**	**GTLVREF**	AH32	IO	HAP1	AM07	IO	MD40	AP25	IO	MD13
C21	IO	HDS3	G33	IO	HD02#	V30	IO	RS1#	AH34	IO	HA29	AM08	O	MAA00	AP26	IO	MD09
C22	IO	HD53#	G34	IO	HD06#	V31	IO	BNR#	AJ01	IO	MD55	AM09	IO	MD38	AP27	IO	MD07
C23	IO	HD50#	H01	IO	GD12	V32	IO	DBSY#	AJ02	IO	MD50	AM10	IO	MD34	AP28	O	DQM0 / CKE0
C24	IO	HD44#	**H30**	**P**	**HCMPVREF**	V33	I	HLOCK#	AJ03	IO	MD54	AM11	O	MAB03	AP29	IO	MD05
C25	IO	HD41#	H31	AI	HRCOMP	V34	IO	ADS#	AJ05	O	SRASA#	AM12	IO	MD32	AP30	IO	MD00

VCC25	(50 pins):	A15-17, B15-17, C15-17, D15-17, E14-17, F14-17, K12-14,18-22, P10, R10, T10,25, U25, V25, W10,25, Y25, AA25, AB10,25, AE12-21
VCCMEM	(86 pins):	V12, W11-12, Y11-12, AA11-12, AB1-6,11-12,24, AC1-6,11-24, AD1-6,12-23, AJ26-30, AK26-31, AL26-33, AM29-33, AN31-34, AP31-34
VCCAGP	(43 pins):	B1, C1-2, D1-3, E1-4, F2-5, G3-6, H4-6, J5-6, K6, L12-17, M11-17, N11-12, P11-12, R11-12
VCCVL	(18 pins):	T11-12, U11-12, V11, W6, Y1-6, AA1-6
VTT	(60 pins):	K29-34, L18-23,29-34, M18-24,29-34, N23-24,29-34, P23-24,29-33, R23-24, T23-24, U23-24, V23-24, W23-24, Y23-24, AA23-24
GND	(199 pins):	B2-3,6,9,12,14,18,21,24,27,30,33, C3,18, D4-5,18,33, E5-6,9,12,18-21,24,27,30, F6-9,11-13,18,20-23,26-27,29,31,33, G29, H2-3,29, J4,30-33, K5, L2,6, M4, P2,6,14-21, R4-6,14-21,29-33, T6,14-21,33, U2,14-21, V4,6,14-21, W2,4-5,14-21,29-30,33, Y14-21,29, AA14-21, AB23,30,33, AC29, AE2,4-6,29-30,33, AF29, AG6,29, AH2,5-6,29-30,33, AJ4,8-10,14-15,18-22,24-25, AK8,10-11,13-14,17,20,23, AL2,5,25, AN2,5,8,11,14,17,20,23,26,29

Table 2. Pin List (Alphabetical Order)

Pin #		Pin Name	Pin #		Pin Name	Pin #		Pin Name	Pin #		Pin Name	Pin #		Pin Names	Pin #		Pin Name
V34	IO	ADS#	D06	IO	GD20	AG34	IO	HA32	B22	IO	HD54#	AK03	O	MAB11	AH03	IO	MD60
A14	I	AGP8XDT#	B07	IO	GD21	AG32	IO	HA33	A21	IO	HD55#	AL06	O	MAB12	AG02	IO	MD61
P05	AI	AGPCOMP	C07	IO	GD22	AJ34	IO	HA34	B20	IO	HD56#	AL21	O	MAB13	AF01	IO	MD62
F10	**P**	**AGPVREF**	A08	IO	GD23	AJ32	IO	HA35	C20	IO	HD57#	AL22	O	MAB14	AE01	IO	MD63
M06	**P**	**AGPVREF**	E07	IO	GD24	AJ31	IO	HAP0	D19	IO	HD58#	AK24	O	MAB15	AP14	IO	MECC0 / CKE0
V31	IO	BNR#	C06	IO	GD25	AH32	IO	HAP1	D20	IO	HD59#	AK34	O	MCLK	AM13	IO	MECC1 / CKE1
R34	IO	BPRI#	B08	IO	GD26	AA30	IO	HAS0#	B19	IO	HD60#	AL34	I	MCLKF	AL13	IO	MECC2 / CKE2
W32	O	BREQ#	D07	IO	GD27	AF31	IO	HAS1#	C19	IO	HD61#	AP30	IO	MD00	AP12	IO	MECC3 / CKE3
A18	O	CPURST#	A09	IO	GD28	**AA29**	**P**	**HAVREF**	A19	IO	HD62#	AM28	IO	MD01	AP15	IO	MECC4 / CKE4
AN06	O	CS0#	C09	IO	GD29	**AD29**	**P**	**HAVREF**	A20	IO	HD63#	AM27	IO	MD02	AN15	IO	MECC5 / CKE5
AP05	O	CS1#	D09	IO	GD30	U29	I	HCLK	G30	IO	HDBI0#	AM26	IO	MD03	AL12	IO	MECC6 / CKE6
AM06	O	CS2#	E08	IO	GD31	T29	I	HCLK#	C30	IO	HDBI1#	AN30	IO	MD04	AN12	IO	MECC7 / CKE7
AP03	O	CS3#	E10	IO	GDBIH / GPIPE#	**H30**	**P**	**HCMPVREF**	A25	IO	HDBI2#	AP29	IO	MD05	**AF06**	**P**	**MEMVREF**
AN03	O	CS4#	D10	IO	GDBIL	J34	IO	HD00#	E22	IO	HDBI3#	AN27	IO	MD06	**AJ11**	**P**	**MEMVREF**
AM04	O	CS5#	K03	IO	GDS0 / GDS0F	H34	IO	HD01#	A28	IO	HDP0	AP27	IO	MD07	**AJ17**	**P**	**MEMVREF**
AP02	O	CS6#	K04	IO	GDS0# / GDS0S	G33	IO	HD02#	E28	IO	HDP1	AM25	IO	MD08	**AJ23**	**P**	**MEMVREF**
AP01	O	CS7#	C08	IO	GDS1 / GDS1F	G31	IO	HD03#	B28	IO	HDP2	AP26	IO	MD09	AK07	–	NC
V32	IO	DBSY#	D08	IO	GDS1# / GDS1S	H33	IO	HD04#	D28	IO	HDP3	AP23	IO	MD10	AJ16	–	NC
T32	IO	DEFER#	A02	IO	GDEVSEL#	H32	IO	HD05#	F32	IO	HDS0	AM23	IO	MD11	P34	O	NMI
T05	O	DNCMD	C05	IO	GFRM#	G34	IO	HD06#	E32	IO	HDS0#	AN25	IO	MD12	W03	I	PWROK
T04	O	DNSTB	A13	O	GGNT#	D31	IO	HD07#	C31	IO	HDS1	AP25	IO	MD13	W01	I	RESET#
T03	O	DNSTB#	C04	IO	GIRDY#	G32	IO	HD08#	B31	IO	HDS1#	AP24	IO	MD14	U33	IO	RS0#
AP28	O	DQM0 / CKE0	**T31**	**P**	**GNDHCK1**	F34	IO	HD09#	B26	IO	HDS2	AN24	IO	MD15	V30	IO	RS1#
AM24	O	DQM1 / CKE1	**U31**	**P**	**GNDHCK2**	E31	IO	HD10#	A26	IO	HDS2#	AP22	IO	MD16	U32	IO	RS2#
AN21	O	DQM2 / CKE2	**AK33**	**P**	**GNDMCK**	F30	IO	HD11#	C21	IO	HDS3	AN22	IO	MD17	AH31	O	RSP#
AP17	O	DQM3 / CKE3	**AJ13**	**P**	**GNDMDLL**	E34	IO	HD12#	D21	IO	HDS3#	AP20	IO	MD18	D12	I	SBA0
AP09	O	DQM4 / CKE4	**P04**	**P**	**GNDQQ**	E33	IO	HD13#	**F19**	**P**	**HDVREF**	AN19	IO	MD19	B11	I	SBA1
AP04	O	DQM5 / CKE5	**F25**	**P**	**GNDTT**	D32	IO	HD14#	**F24**	**P**	**HDVREF**	AL23	IO	MD20	C12	I	SBA2
AK02	O	DQM6 / CKE6	**AB29**	**P**	**GNDTT**	D34	IO	HD15#	**F28**	**P**	**HDVREF**	AM22	IO	MD21	A11	I	SBA3
AG03	O	DQM7 / CKE7	J03	IO	GPAR	B32	IO	HD16#	**J29**	**P**	**HDVREF**	AM19	IO	MD22	E11	I	SBA4
AP13	O	DQM8	C13	I	GPIPE#	C33	IO	HD17#	U34	IO	HIT#	AP19	IO	MD23	A10	I	SBA5
AN28	IO	DQS0# / CKE0	A12	I	GRBF#	C34	IO	HD18#	T34	I	HITM#	AL18	IO	MD24	C10	I	SBA6
AL24	IO	DQS1# / CKE1	C14	I	GREQ#	A33	IO	HD19#	V33	I	HLOCK#	AP18	IO	MD25	B10	I	SBA7
AP21	IO	DQS2# / CKE2	F01	IO	GSERR#	A34	IO	HD20#	H31	AI	HRCOMP	AN16	IO	MD26	D11	I	SBS / SBSF
AM17	IO	DQS3# / CKE3	A01	IO	GSTOP#	B34	IO	HD21#	Y33	IO	HREQ0#	AL15	IO	MD27	C11	I	SBS# / SBSS
AN09	IO	DQS4# / CKE4	**V29**	**P**	**GTLVREF**	A32	IO	HD22#	AB32	IO	HREQ1#	AM18	IO	MD28	AF05	O	SCASA#
AN04	IO	DQS5# / CKE5	A03	IO	GTRDY#	C32	IO	HD23#	Y31	IO	HREQ2#	AN18	IO	MD29	AF04	O	SCASB#
AK01	IO	DQS6# / CKE6	D13	I	GWBF#	D30	IO	HD24#	AA31	IO	HREQ3#	AP16	IO	MD30	AJ05	O	SRASA#
AF03	IO	DQS7# / CKE7	Y32	IO	HA03	D29	IO	HD25#	Y34	IO	HREQ4#	AM15	IO	MD31	AK04	O	SRASB#
AN13	IO	DQS8#	Y30	IO	HA04	A29	IO	HD26#	W31	IO	HTRDY#	AM12	IO	MD32	D14	O	ST0
W34	IO	DRDY#	AB31	IO	HA05	E29	IO	HD27#	AM08	O	MAA00	AP10	IO	MD33	B13	O	ST1
K01	IO	GBE0#	AA34	IO	HA06	A30	IO	HD28#	AL09	O	MAA01	AM10	IO	MD34	E13	O	ST2
G02	IO	GBE1#	AA33	IO	HA07	C29	IO	HD29#	AL10	O	MAA02	AN07	IO	MD35	V01	I	SUSST#
B04	IO	GBE2#	AC31	IO	HA08	A31	IO	HD30#	AK12	O	MAA03	AP11	IO	MD36	AG04	O	SWEA#
A07	IO	GBE3#	AA32	IO	HA09	B29	IO	HD31#	AL14	O	MAA04	AN10	IO	MD37	AG05	O	SWEB#
AK25	O	GCKE	AC34	IO	HA10	D27	IO	HD32#	AK16	O	MAA05	AM09	IO	MD38	AM34	I	TESTIN#
N05	I	GCLK	AB34	IO	HA11	D26	IO	HD33#	AL16	O	MAA06	AP08	IO	MD39	V02	I	UPCMD
M03	IO	GD0	AD34	IO	HA12	D25	IO	HD34#	AK19	O	MAA07	AM07	IO	MD40	T02	I	UPSTB
N01	IO	GD1	AC33	IO	HA13	C28	IO	HD35#	AL17	O	MAA08	AP06	IO	MD41	T01	I	UPSTB#
M01	IO	GD2	AC32	IO	HA14	E26	IO	HD36#	AM30	O	MAA09	AM05	IO	MD42	R03	IO	VAD0
N03	IO	GD3	AD33	IO	HA15	A27	IO	HD37#	AJ06	O	MAA10	AN01	IO	MD43	R02	IO	VAD1
M02	IO	GD4	AC30	IO	HA16	C26	IO	HD38#	AK05	O	MAA11	AP07	IO	MD44	U05	IO	VAD2
L03	IO	GD5	AE34	IO	HA17	C27	IO	HD39#	AK06	O	MAA12	AL07	IO	MD45	U04	IO	VAD3
L01	IO	GD6	AD32	IO	HA18	E25	IO	HD40#	AL20	O	MAA13	AM03	IO	MD46	N02	IO	VAD4
K02	IO	GD7	AE31	IO	HA19	C25	IO	HD41#	AK21	O	MAA14	AM02	IO	MD47	P01	IO	VAD5
J01	IO	GD8	AD31	IO	HA20	B25	IO	HD42#	AK22	O	MAA15	AM01	IO	MD48	U01	IO	VAD6
N04	IO	GD9	AE32	IO	HA21	A24	IO	HD43#	AL08	O	MAB00	AL04	IO	MD49	U03	IO	VAD7
J02	IO	GD10	AF34	IO	HA22	C24	IO	HD44#	AK09	O	MAB01	AJ02	IO	MD50	R01	IO	VBE#
L04	IO	GD11	AF33	IO	HA23	D24	IO	HD45#	AL11	O	MAB02	AH04	IO	MD51	**T30**	**P**	**VCCHCK1**
H01	IO	GD12	AD30	IO	HA24	E23	IO	HD46#	AM11	O	MAB03	AL03	IO	MD52	**U30**	**P**	**VCCHCK2**
M05	IO	GD13	AF32	IO	HA25	D23	IO	HD47#	AM14	O	MAB04	AL01	IO	MD53	**AK32**	**P**	**VCCMCK**
G01	IO	GD14	AG30	IO	HA26	A23	IO	HD48#	AM16	O	MAB05	AJ03	IO	MD54	**AJ12**	**P**	**VCCMDLL**
L05	IO	GD15	AG33	IO	HA27	B23	IO	HD49#	AK15	O	MAB06	AJ01	IO	MD55	**N06**	**P**	**VCCQQ**
B05	IO	GD16	AF30	IO	HA28	C23	IO	HD50#	AL19	O	MAB07	AH01	IO	MD56	U06	AI	VLCOMP
A05	IO	GD17	AH34	IO	HA29	A22	IO	HD51#	AK18	O	MAB08	AG01	IO	MD57	**V03**	**P**	**VLVREF**
A04	IO	GD18	AG31	IO	HA30	D22	IO	HD52#	AM21	O	MAB09	AF02	IO	MD58	P03	IO	VPAR
A06	IO	GD19	AJ33	IO	HA31	C22	IO	HD53#	AJ07	O	MAB10	AE03	IO	MD59	**V05**	**P**	**VSUS25**

VCC25 (50 pins): A15-17, B15-17, C15-17, D15-17, E14-17, F14-17, K12-14,18-22, P10, R10, T10,25, U25, V25, W10,25, Y25, AA25, AB10,25, AE12-21

VCCMEM (86 pins): V12, W11-12, Y11-12, AA11-12, AB1-6,11-12,24, AC1-6,11-24, AD1-6,12-23, AJ26-30, AK26-31, AL26-33, AM29-33, AN31-34, AP31-34

VCCAGP (43 pins): B1, C1-2, D1-3, E1-4, F2-5, G3-6, H4-6, J5-6, K6, L12-17, M11-17, N11-12, P11-12, R11-12

VCCVL (18 pins): T11-12, U11-12, V11, W6, Y1-6, AA1-6

VTT (60 pins): K29-34, L18-23,29-34, M18-24,29-34, N23-24,29-34, P23-24,29-33, R23-24, T23-24, U23-24, V23-24, W23-24, Y23-24, AA23-24

GND (199 pins): B2-3,6,9,12,14,18,21,24,27,30,33, C3,18, D4-5,18,33, E5-6,9,12,18-21,24,27,30, F6-9,11-13,18,20-23,26-27,29,31,33, G29, H2-3,29, J4,30-33, K5, L2,6, M4, P2,6,14-21, R4-6,14-21,29-33, T6,14-21,33, U2,14-21, V4,6,14-21, W2,4-5,14-21,29-30,33, Y14-21,29, AA14-21, AB23,30,33, AC29, AE2,4-6,29-30,33, AF29, AG6,29, AH2,5-6,29-30,33, AJ4,8-10,14-15,18-22,24-25, AK8,10-11,13-14,17,20,23, AL2,5,25, AN2,5,8,11,14,17,20,23,26,29

Pin Descriptions

Table 3. VT8754 / P4X400 Pin Descriptions

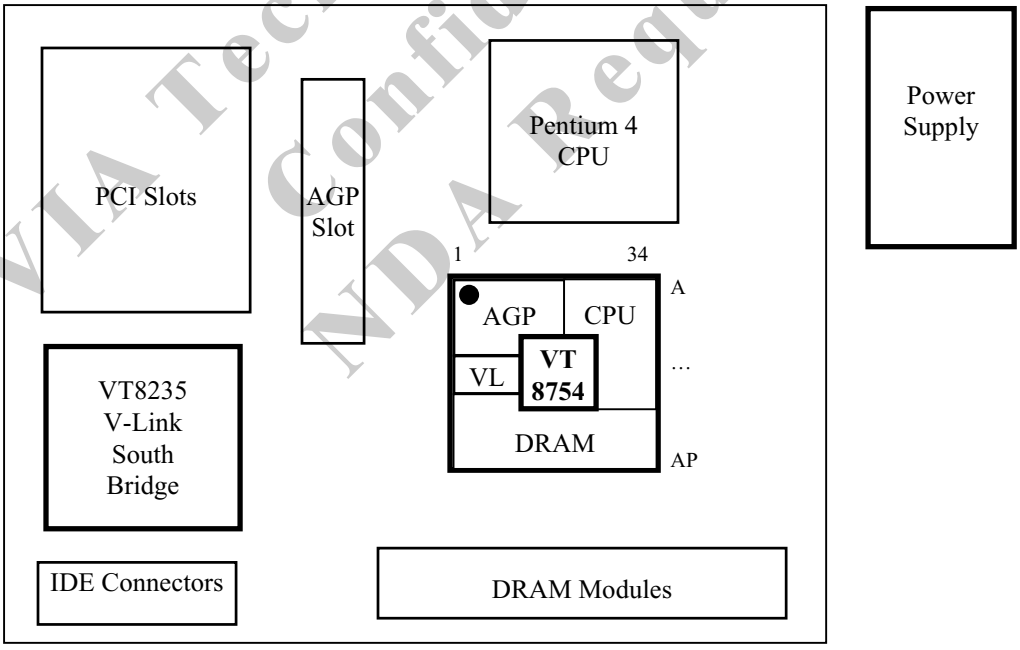
CPU Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
HA[35:3]#	(see pinout tables)	IO	**Host CPU Address Bus.** Connect to the address bus of the host CPU. Inputs during CPU cycles and driven by the VT8754 during cache snooping operations. Address signals up through HA[35] allow support of a 64 Gbyte memory space.
HAP[1:0]	AH32, AJ31	IO	**Host CPU Addres Parity.**
HAS[1:0]#	AF31, AA30	IO	**Host CPU Address Strobe.** Source synchronous strobes used to transfer HA[31:3]# and HREQ[4:0]# at a 2x transfer rate. HAS1# is the strobe for HA[31:17]# and HAS0# is the strobe for HA[16:3] and HREQ[4:0]#.
HD[63:0]#	(see pinout tables)	IO	**Host CPU Data.** These signals are connected to the CPU data bus.
HDP[3:0]	D28, B28, E28, A28	IO	**Host Data Parity.**
HDBI[3:0]#	E22, A25, C30, G30	IO	**Host CPU Dynamic Bus Inversion.** Driven along with HD[63:0]# to indicate if the associated signals are inverted or not. Used to limit the number of simultaneously switching signals to 8 for the associated 16-bit data pin group (HDBI3# for HD[63:48]#, HDBI2# for HD[47:32]#, HDBI1# for HD[31:16]#, and HDBI0# for HD[15:0]#). HDBIn# is asserted such that the number of data bits driven low for the corresponding group does not exceed 8.
HDS[3:0] **HDS[3:0]#**	C21, B26, C31, F32 D21, A26, B31, E32	IO	**Host CPU Differential Data Strobes.** Source synchronous strobes used to transfer HD[63:0]# and HDBI[3:0]# at a 4x transfer rate. HDS3 / HDS3# are the strobes for HD[63:48]# and HDBI3#; HDS2 / HDS2# are the strobes for HD[47:32]# and HDBI2#; HDS1 / HDS1# are the strobes for HD[31:16]# and HDBI1#; and HDS0 / HDS0# are the strobes for HD[15:0]# and HDBI0#.
ADS#	V34	IO	**Address Strobe**. The CPU asserts ADS# in T1 of the CPU bus cycle.
DBSY#	V32	IO	**Data Bus Busy**. Used by the data bus owner to hold the data bus for transfers requiring more than one cycle.
DRDY#	W34	IO	**Data Ready**. Asserted for each cycle that data is transferred.
HIT#	U34	IO	**Hit**. Indicates that a caching agent holds an unmodified version of the requested line. Also driven in conjunction with HITM# by the target to extend the snoop window.
HITM#	T34	I	**Hit Modified**. Asserted by the CPU to indicate that the address is modified in the L1 cache and needs to be written back.
HLOCK#	V33	I	**Host Lock**. All CPU cycles sampled with the assertion of HLOCK# and ADS# until the negation of HLOCK# must be atomic.
HREQ[4:0]#	Y34, AA31, Y31, AB32, Y33	IO	**Request Command**. Asserted during both clocks of the request phase. In the first clock, the signals define the transaction type to a level of detail that is sufficient to begin a snoop request. In the second clock, the signals carry additional information to define the complete transaction type.
HTRDY#	W31	IO	**Host Target Ready**. Indicates that the target of the processor transaction is able to enter the data transfer phase.

Note: Clocking of the CPU interface is performed with HCLK and HCLK# (see clock pin description group).
Note: Internal pullup resistors are provided on all AGTL+ interface pins. If the CPU does not have internal pullups, these north bridge internal pullups may be enabled to allow the interface to meet AGTL+ bus interface specifications (see VAD3 strap).

CPU Interface (continued)

Signal Name	Pin #	I/O	Signal Description
RS[2:0]#	U32, V30, U33	IO	**Response Signals**. Indicates the type of response per the table below: **RS[2:0]#** / **Response type** / **RS[2:0]#** / **Response type** 000 Idle State — 100 Hard Failure 001 Retry Response — 101 Normal Without Data 010 Defer Response — 110 Implicit Writeback 011 Reserved — 111 Normal With Data
RSP#	AH31	O	**Response Parity.**
BREQ#	W32	O	**Bus Request.** Bus request output to CPU.
BPRI#	R34	IO	**Priority Agent Bus Request**. The owner of this signal will always be the next bus owner. This signal has priority over symmetric bus requests and causes the current symmetric owner to stop issuing new transactions unless the HLOCK# signal is asserted. The VT8754 drives this signal to gain control of the processor bus.
BNR#	V31	IO	**Block Next Request**. Used to block the current request bus owner from issuing new requests. This signal is used to dynamically control the processor bus pipeline depth.
DEFER#	T32	IO	**Defer**. The VT8754 uses a dynamic deferring policy to optimize system performance. The VT8754 also uses the DEFER# signal to indicate a processor retry response.
CPURST#	A18	O	**CPU Reset.** Reset output to CPU. External pullup and filter capacitor to ground should be provided per CPU manufacturer's recommendations.

The pinouts were defined assuming the ATX PCB layout model shown below (and general pin layout shown) as a guide for PCB component placement. Other PCB layouts (AT, LPX, and NLX) were also considered and can typically follow the same general component placement.



DRAM Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
MD[63:0]	(see pin lists)	IO	**Memory Data.** These signals are connected to the DRAM data bus. Output drive strength may be set by Device 0 RxE8.
MECC[7:0] / CKE[7:0]	AN12, AL12, AN15, AP15, AP12, AL13, AM13, AP14	IO	**DRAM ECC or EC Data:** when ECC is enabled. **Clock Enables:** For each DRAM bank for powering down the SDRAMs in notebook applications. Also used in desktop systems for clock control to reduce power usage and for reducing heat/temperature in high-speed memory systems.
MAA[15:0]	(see pin lists)	O	**Memory Address A.** DRAM address lines (two sets for better drive). Output drive strength may be set by Device 0 RxEA.
MAB[15:0]	(see pin lists)	O	**Memory Address B.** DRAM address lines (two sets for better drive). Output drive strength may be set by Device 0 RxEB.
SRASA#, **SCASA#, SWEA#**	AJ5, AF5, AG4	O	**Row Address, Column Address and Write Enable Command Indicator Set A.** (two sets for better drive). Output drive strength may be set by Device 0 RxEA.
SRASB#, **SCASB#, SWEB#**	AK4, AF4, AG5	O	**Row Address, Column Address and Write Enable Command Indicator Set B.** (two sets for better drive). Output drive strength may be set by Device 0 RxEB.
CS[7:0]#	AP1, AP2, AM4, AN3, AP3, AM6, AP5, AN6	O	**Chip Select.** Chip select of each bank. Output drive strength may be set by Device 0 RxE9.
DQM[8], **DQM[7:0]** / CKE[7:0]	AP13, AG3, AK2, AP4, AP9, AP17, AN21, AM24, AP28	O	**Data Mask.** Data mask of each byte lane plus DQM8 for ECC byte. Output drive strength may be set by Device 0 RxE8.
DQS[8], **DQS[7:0]**# / CKE[7:0]	AN13, AF3, AK1, AN4, AN9, AM17, AP21, AL24, AN28	IO	**DDR Data Strobe.** Data strobe of each byte lane plus DQS8# for ECC byte. Output drive strength may be set by Device 0 RxE8.
CKE[7:0] / MECC[7:0] **-or-** **CKE[7:0]** / DQM[7:0] **-or-** **CKE[7:0]** / DQS[7:0]#	(see above)	O	**Clock Enables.** Clock enables for each DRAM bank for powering down the SDRAM or clock control for reducing power usage and for reducing heat / temperature in high-speed memory systems. See Device 0 RxBD[6] for CKE function enable.
GCKE	AK25	O	**Global Clock Enable.**
NC	AJ16, AK7	–	**No Connect.** Reserved for future use.

AGP Bus Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
GD[31:0]	(see pin list)	IO	**Address / Data Bus.** Address is driven with GDS assertion for AGP-style transfers and with GFRM# assertion for PCI-style transfers.
GBE[3:0]# (GBE[3:0] for 8x mode)	A7, B4, G2, K1	IO	**Command / Byte Enable.** (Interpreted as C/BE# for AGP 2x/4x and C#/BE for 8x) **AGP:** These pins provide command information (different commands than for PCI) driven by the master (graphics controller) when requests are being enqueued using GPIPE# (2x/4x only as GPIPE# isn't used in 8x mode). These pins provide valid byte information during AGP write transactions and are driven by the master. The target (this chip) drives these lines to "0000" during the return of AGP read data. **PCI:** Commands are driven with GFRM# assertion. Byte enables corresponding to supplied or requested data are driven on following clocks.
GPAR	J3	IO	**AGP Parity.** A single parity bit is provided over GD[31:0] and GBE[3:0].
GDBIH / GPIPE#, **GDBIL**	E10 D10	IO	**Dynamic Bus Inversion High / Low.** AGP 8x transfer mode only. Driven by the source to indicate whether the corresponding data bit group (GDBIH for GD[31:16] and GDBIL for GD[15:0]) needs to be inverted on the receiving end (1 on GDBIx indicates that the corresponding data bit group should be inverted). Used to limit the number of simultaneously switching outputs to 8 for each 16-pin group.
GDS0 (GDS0F for 8x), **GDS0#** (GDS0S for 8x)	K3 K4	IO	**Bus Strobe 0.** Source synchronous strobes for GD[15:0] (the agent that is providing the data drives these signals). GDS0 provides timing for 2x data transfer mode; GDS0 and GDS0# provide timing for 4x transfer mode. For 8x transfer mode, GDS0 is interpreted as GDS0F ("First" strobe) and GDS0# as GDS0S ("Second" strobe).
GDS1 (GDS1F for 8x), **GDS1#** (GDS1S for 8x)	C8 D8	IO	**Bus Strobe 1.** Source synchronous strobes for GD[31:16] (i.e., the agent that is providing the data drives these signals). GDS1 provides timing for 2x data transfer mode; GDS1 and GDS1# provide timing for 4x transfer mode. For 8x transfer mode, GDS1 is interpreted as GDS1F ("First" strobe) and GDS1# as GDS1S ("Second" strobe).
GFRM# (GFRM for 8x)	C5	IO	**Frame.** Assertion indicates the address phase of a PCI transfer. Negation indicates that one more data transfer is desired by the cycle initiator. Interpreted as active high for 8x.
GIRDY# (GIRDY for 8x)	C4	IO	**Initiator Ready.** (Interpreted as active low for PCI/AGP2x/4x and high for AGP 8x) **AGP:** For write operations, the assertion of this pin indicates that the master is ready to provide *all* write data for the current transaction. Once this pin is asserted, the master is not allowed to insert wait states. For read operations, the assertion of this pin indicates that the master is ready to transfer a subsequent block of read data. The master is *never* allowed to insert a wait state during the initial block of a read transaction. However, it may insert wait states after each block transfers. **PCI:** Asserted when the initiator is ready for data transfer.
GTRDY# (GTRDY for 8x)	A3	IO	**Target Ready.** (Interpreted as active low for PCI/AGP2x/4x and high for AGP 8x) **AGP:** Indicates that the target is ready to provide read data for the entire transaction (when the transaction can complete within four clocks) or is ready to transfer a (initial or subsequent) block of data when the transfer requires more than four clocks to complete. The target is allowed to insert wait states after each block transfer for both read and write transactions. **PCI:** Asserted when the target is ready for data transfer.
GSTOP# (GSTOP for 8x)	A1	IO	**Stop (PCI transactions only).** Asserted by the target to request the master to stop the current transaction. Interpreted as active high for AGP 8x.
GDEVSEL# (GDEVSEL for 8x mode)	A2	IO	**Device Select (PCI transactions only).** This signal is driven by the VT8754 when a PCI initiator is attempting to access main memory. It is an input when the VT8754 is acting as PCI initiator. Not used for AGP cycles. Interpreted as active high for AGP 8x.
GPIPE# (GPIPE for 8x)	C13	I	**Pipelined Request.** Asserted by the master (the external graphics controller) to indicate that a full-width request is to be enqueued by the target VT8754. The master enqueues one request each rising edge of GCLK while GPIPE# is asserted. When GPIPE# is deasserted no new requests are enqueued across the AD bus. Not used by AGP 8x.

AGP Bus Interface (continued)			
Signal Name	**Pin #**	**I/O**	**Signal Description**
AGP8DT#	A14	I	**AGP 8x Transfer Mode Detect.** Low indicates that the external graphics card can support 8x transfer mode
GRBF# (GRBF for 8x)	A12	I	**Read Buffer Full.** Indicates if the master (graphics controller) is ready to accept previously requested low priority read data. When GRBF# is asserted, the VT8754 will not return low priority read data to the graphics controller.
GWBF# (GWBF for 8x)	D13	I	**Write Buffer Full.**
SBA[7:0] (SBA[7:0]# for 8x)	B10, C10, A10, E11, A11, C12, B11, D12	I	**SideBand Address.** Provides an additional bus to pass address and command information from the master (graphics controller) to the target (VT8754 north bridge logic). These pins are ignored until enabled.
SBS (SBSF for 8x), **SBS#** (SBSS for 8x)	D11 C11	I	**Sideband Strobe.** Driven by the master to provide timing for SBA[7:0]. SBS is used for AGP 2x while SBS and SBS# are used together for AGP 4x. For 8x mode, the strobe mechanism works differently with SBS interpreted as SBSF ("First" strobe) and SBS# as SBSS ("Second" strobe).
ST[2:0]	E13, B13, D14	O	**Status (AGP only).** Provides information from the arbiter to a master to indicate what it may do. Only valid while GGNT# is asserted. 000 Indicates that previously requested low priority read or flush data is being returned to the master (graphics controller). 001 Indicates that previously requested high priority read data is being returned to the master. 010 Indicates that the master is to provide low priority write data for a previously enqueued write command. 011 Indicates that the master is to provide high priority write data for a previously enqueued write command. 100 Reserved. (arbiter must not issue, may be defined in the future). 101 Reserved. (arbiter must not issue, may be defined in the future). 110 Reserved. (arbiter must not issue, may be defined in the future). 111 Indicates that the master (graphics controller) has been given permission to start a bus transaction. The master may enqueue AGP requests by asserting PIPE# or start a PCI transaction by asserting GFRM#. ST[2:0] are always outputs from the target (north bridge logic) and inputs to the master (graphics controller).
GREQ# (GREQ for 8x)	C14	I	**Request.** Master (graphics controller) request for use of the AGP bus.
GGNT# (GGNT for 8x)	A13	O	**Grant.** Permission is given to the master (graphics controller) to use the AGP bus.
GSERR#	F1	IO	**AGP System Error.**

Note: For PCI operation on the AGP bus, the following pins are not required:
- PERR# (parity and error reporting not required on transient data devices such as graphics controllers)
- LOCK# (no lock requirement on AGP)
- IDSEL (internally connected to AD16 on AGP-compliant masters)

Note: Separate system interrupts are not provided for AGP. The AGP connector provides interrupts via PCI bus INTA-B#.

Note: The AGP bus supports only one master directly (REQ[3:0]# and GNT[3:0]# are not provided). External logic is required to implement additional master capability. Note that the arbitration mechanism on the AGP bus is different from the PCI bus.

Note: A separate reset is not required for the AGP bus (RESET# resets both PCI and AGP buses)

Note: Two mechanisms are provided by the AGP bus to enqueue master requests: GPIPE# (to send addresses multiplexed on the AD lines) and the SBA port (to send addresses unmultiplexed). AGP masters implement one or the other or select one at initialization time (they are not allowed to change during runtime). Only one of the two will be used; the signals associated with the other will not be used. GRBF# has an internal pullup to maintain it in the de-asserted state in case it is not implemented on the master device. AGP 8x mode allows only SBA (GPIPE# isn't used in 8x mode).

Note: AGP 8x signal levels are 0V and 0.8V. AGP 8x mode maintains most signals at a low level when inactive resulting in no current flow.

V-Link Interface

Signal Name	Pin #	I/O	Signal Description
VAD7, **VAD6,** **VAD5**, **VAD4**, **VAD3**, **VAD2**, **VAD1**, **VAD0**	U3 U1 P1 N2 U4 U5 R2 R3	IO	**Address / Data Bus.** Also used to pass strap information at reset time to the north bridge from the south bridge (the actual straps are not on the north bridge VAD pin but instead are on the indicated south bridge pin). VAD7 – reserved (do not use) — Connection: Must be strapped L — Register: Rx50[6] — SB Pin: SDCS3# VAD6 – Auto-Configure — L=Disable, H=Enable — Rx54[5] — SDA2 VAD5 – AGTL+ Drive Strength 4x — L=1x, H=4x — SDA1 VAD4 – AGTL+ Drive Strength 2x — L=1x, H=2x — SDA0 VAD3 – Internal AGTL+ Pullups — L=Enable, H=Disable — Rx52[5] — SA19 VAD2 – IOQ Depth — L=1-level, H=12-level — Rx50[7] — SA18 VAD1 – -reserved- — SA17 VAD0 – CPU FSB Frequency — L=100 MHz, H=133 MHz — Rx54[6] — SA16
VPAR	P3	IO	**Parity.**
VBE#	R1	IO	**Byte Enable.**
UPCMD	V2	I	**Command from Client (South Bridge) to Host (North Bridge).**
UPSTB	T2	I	**Strobe from Client to Host.**
UPSTB#	T1	I	**Complement Strobe from Client to Host.**
DNCMD	T5	O	**Command from Host (North Bridge) to Client (South Bridge).**
DNSTB	T4	O	**Strobe from Host to Client.**
DNSTB#	T3	O	**Complement Strobe from Host to Client.**

Clocks, Resets, Power Control, General Purpose I/O, Interrupts and Test			
Signal Name	**Pin #**	**I/O**	**Signal Description**
HCLK	U29	I	**Host Clock.** This pin receives the host CPU clock (100 / 133 MHz). This clock is used by all P4X400 logic that is in the host CPU domain.
HCLK#	T29	I	**Host Clock Complement.** Used for Quad Data Transfer on host CPU bus.
MCLK	AK34	O	**Memory (SDRAM) Clock.** Output from internal clock generator to the external clock buffer.
MCLKF	AL34	I	**Memory (SDRAM) Clock Feedback.** Input from the external clock buffer.
GCLK	N5	I	**AGP Clock.** Clock for AGP logic.
RESET#	W1	I	**Reset.** Input from the South Bridge chip. When asserted, this signal resets P4X400 and sets all register bits to the default value. The rising edge of this signal is used to sample all power-up strap options
PWROK	W3	I	**Power OK.** Connect to South Bridge and Power Good circuitry.
SUSST#	V1	I	**Suspend Status.** For implementation of the Suspend-to-DRAM feature. Connect to an external pull-up to disable.
NMI	P34	O	**Non Maskable Interrupt.** Connect to South Bridge NMI input.
TESTIN#	AM34	I	**Test In.** This pin is used for testing and must be left unconnected or tied high on all board designs.

Reference Voltages			
Signal Name	**Pin #**	**I/O**	**Signal Description**
GTLVREF	V29	P	**Host CPU Interface AGTL+ Voltage Reference.** 2/3 VTT ±2% typically derived using a resistive voltage divider. See P4X400 Design Guide.
HDVREF	F19, F24, F28, J29	P	**Host CPU Data Voltage Reference.** 2/3 VTT ±2% typically derived using a resistive voltage divider. See P4X400 Design Guide.
HAVREF	AA29, AD29	P	**Host CPU Address Voltage Reference.** 2/3 VTT ±2% typically derived using a resistive voltage divider. See P4X400 Design Guide.
HCMPVREF	H30	P	**Host CPU Compensation Voltage Reference.** 1/3 VTT ±2% typically derived using a resistive voltage divider. See P4X400 Design Guide.
MEMVREF	AF6, AJ11, AJ17, AJ23	P	**Memory Voltage Reference.** 1/2 VCC25 ±2% typically derived using a resistive voltage divider. See P4X400 Design Guide.
VLVREF	V3	P	**V-Link Voltage Reference.** 0.625V ±2% derived using a resistive voltage divider. See P4X400 Design Guide.
AGPVREF	F10, M6	P	**AGP Voltage Reference.** 0.5 VCCQQ (0.75V) for AGP 2.0 (4x transfer mode) and 0.23 VCCQQ (0.35V) for AGP 3.0 (8x transfer mode). See the P4X400 Design Guide for additional information and circuit implementation details..

Compensation			
Signal Name	**Pin #**	**I/O**	**Signal Description**
HRCOMP	H31	AI	**Host CPU Compensation.** Connect 20.5Ω 1% resistor to ground. Used for Host CPU interface I/O buffer calibration.
VLCOMP	U6	AI	**Vlink Compensation.** Connect 70Ω 1% resistor to ground.
AGPCOMP	P5	AI	**AGP Compensation.**

Analog Power / Ground			
Signal Name	**Pin #**	**I/O**	**Signal Description**
VCCHCK1	T30	P	**Power for Host CPU Clock PLL 1** (2.5V ±5%)
GNDHCK1	T31	P	**Ground for Host CPU Clock 1 Circuitry.** Connect to main ground plane through a ferrite bead.
VCCHCK2	U30	P	**Power for Host CPU Clock PLL 2** (2.5V ±5%)
GNDHCK2	U31	P	**Ground for Host CPU Clock 2 Circuitry.** Connect to main ground plane through a ferrite bead.
VCCMCK	AK32	P	**Power for Memory Clock PLL** (2.5V ±5%)
GNDMCK	AK33	P	**Ground for Memory Clock Circuitry.** Connect to main ground plane through a ferrite bead.
VCCMDLL	AJ12	P	**Power for Memory Strobe DLL** (2.5V ±5%)
GNDMDLL	AJ13	P	**Ground for Memory Strobe DLL Circuitry.** Connect to main ground plane through a ferrite bead.

Digital Power / Ground			
Signal Name	**Pin #**	**I/O**	**Signal Description**
VTT	(see pin lists)	P	**Power** for **CPU I/O Interface Logic (60 Pins).** Voltage is CPU dependent.
GNDTT	F25, AB29	P	**Ground** for **CPU I/O Interface Logic (2 Pins).**
VCCMEM	(see pin lists)	P	**Power** for **Memory I/O Interface Logic (86 Pins).** 2.5V ±5%.
VCCVL	(see pin lists)	P	**Power** for **V-Link I/O Interface Logic (18 Pins).** 2.5V ±5%
VCCAGP	(see pin lists)	P	**Power** for **AGP Bus I/O Interface Logic (43 Pins).** 1.5V ±5%
VCCQQ	N6	P	**AGP Quiet Power.** Connect to main AGP power (VCCAGP) through a ferrite bead.
GNDQQ	P4	P	**Ground for AGP Quiet Power.** Connect to main ground plane.
VCC25	(see pin lists)	P	**Power** for **Internal Logic (50 Pins).** 2.5V ±5%
VSUS25	V5	P	**Suspend Power.** 2.5V ±5%
GND	(see pin lists)	P	**Digital Ground (199 Pins).** Connect to main ground plane.

REGISTERS

Register Overview

The following tables summarize the configuration and I/O registers of the P4X400. These tables also document the power-on default value ("Default") and access type ("Acc") for each register. Access type definitions used are RW (Read/Write), RO (Read/Only), "—" for reserved / used (essentially the same as RO), RWC (or just WC) (Read / Write 1's to Clear individual bits), and W1 (Write Once then Read / Only after that). Registers indicated as RW may have some read/only bits that always read back a fixed value (usually 0 if unused); registers designated as RWC or WC may have some read-only or read write bits (see individual register descriptions following these tables for details). All offset and default values are shown in hexadecimal unless otherwise indicated.

The graphics registers are described in a separate document.

Table 4. VT8754 / P4X400 Registers

P4X400 I/O Ports

Port #	I/O Port	Default	Acc
22	PCI / AGP Arbiter Disable	00	RW
CFB-8	Configuration Address	0000 0000	RW
CFF-C	Configuration Data	0000 0000	RW

P4X400 Device 0 Registers - Host Bridge

Header Registers

Offset	Configuration Space Header	Default	Acc
1-0	Vendor ID	**1106**	RO
3-2	Device ID	**3168**	RO
5-4	Command	**0006**	**RW**
7-6	Status	**0210**	**WC**
8	Revision ID	**0n**	RO
9	Program Interface	00	RO
A	Sub Class Code	00	RO
B	Base Class Code	**06**	RO
C	-reserved-	00	—
D	Latency Timer	00	**RW**
E	Header Type	00	RO
F	Built In Self Test (BIST)	00	RO
13-10	Graphics Aperture Base	**0000 0008**	**RW**
14-2B	-reserved-	00	—
2D-2C	Subsystem Vendor ID	0000	**W1**
2F-2E	Subsystem ID	0000	**W1**
30-33	-reserved-	00	—
34	Capability Pointer **AGP 2.0:**	**A0**	RO
	(CAPPTR) **AGP 3.0:**	**80**	RO
35-3F	-reserved-	00	—

Device-Specific Registers

Offset	V-Link Control	Default	Acc
40	V-Link Revision ID	00	**RO**
41	V-Link NB Capability	**19**	**WC**
42	V-Link NB Downlink Command	**88**	RW
43	V-Link NB Uplink Max Req Depth	**80**	RW
44	V-Link NB Uplink Buffer Size	**82**	RW
45	V-Link NB Bus Timer	**44**	RW
46	V-Link NB Misc Control	00	RW
47	V-Link Control	00	RW
48	V-Link NB/SB Configuration	**18**	RW
49	V-Link SB Capability	**19**	**WC**
4A	V-Link SB Downlink Status	**88**	**RO**
4B	V-Link SB Uplink Max Req Depth	**80**	RW
4C	V-Link SB Uplink Buffer Size	**82**	RW
4D	V-Link SB Bus Timer	**44**	RW
4E	CCA Master High Priority	00	RW
4F	V-Link SB Miscellaneous Control	00	RW

Offset	Host CPU Protocol Control	Default	Acc
50	CPU Interface Request Phase Control	00	RW
51	CPU Interface Basic Control	00	RW
52	CPU Interface Advanced Control	00	RW
53	CPU Interface Arbitration Control	00	RW
54	CPU Frequency	00	RW

Device-Specific Registers (continued)

Offset	DRAM Control	Default	Acc
55	DRAM Control	00	RW
56-57	(see below)		
59-58	MA Map Type	**2222**	RW
5F-5A	DRAM Row Ending Address:		
5A	Bank 0 Ending (HA[31:24])	**01**	RW
5B	Bank 1 Ending (HA[31:24])	**01**	RW
5C	Bank 2 Ending (HA[31:24])	**01**	RW
5D	Bank 3 Ending (HA[31:24])	**01**	RW
5E	Bank 4 Ending (HA[31:24])	**01**	RW
5F	Bank 5 Ending (HA[31:24])	**01**	RW
56	Bank 6 Ending (HA[31:24])	**01**	RW
57	Bank 7 Ending (HA[31:24])	**01**	RW
60	DRAM Type	**80**	RW
61	ROM Shadow Control C0000-CFFFF	00	RW
62	ROM Shadow Control D0000-DFFFF	00	RW
63	ROM Shadow Control E0000-FFFFF	00	RW
64	DRAM Timing for All Banks	**E4**	RW
65	DRAM Arbitration Timer	00	RW
66	DRAM Arbitration Control	00	RW
67	DRAM Strobe Input Delay	00	RW
68	DRAM Strobe Output Delay	00	RW
69	DRAM Clock Select	00	RW
6A	DRAM Refresh Counter	00	RW
6B	DRAM Arbitration Control	**10**	RW
6C	DRAM Clock Control	00	RW
6D	-reserved-	00	—
6E	ECC Control	00	RW
6F	ECC Status	00	**WC**

Offset	PCI Bus Control	Default	Acc
70	PCI Buffer Control	00	RW
71	CPU to PCI Flow Control	**48**	**WC**
72	-reserved-	00	—
73	PCI Master Control	00	RW
74	-reserved-	00	—
75	PCI Arbitration 1	00	RW
76	PCI Arbitration 2	00	RW
77-7F	-reserved-	00	—

Device 0 Device-Specific Registers (continued)

Offset	AGP 2.0 Control (RxFD[1]=1)	Default	Acc
83-80	AGP 2.0 GART/TLB Control	0000 0000	RW
84	AGP 2.0 Graphics Aperture Size	00	RW
85	AGP 2.0 Write Policy	00	RW
86	CPU / DRAM Bandwidth Timer Ctrl	00	RW
87	CPU / DRAM Bandwidth Limit	00	RW
8B-88	AGP 2.0 GART Table Base	0000 0000	RW
8C-9F	-reserved-	00	—
A3-A0	AGP 2.0 Capabilities	**0020 C002**	**RO**
A7-A4	AGP 2.0 Status	**1F00 0201**	**RO**
AB-A8	AGP 2.0 Command	0000 0000	RW

Registers A0-AB in the AGP 2.0 register group in the table above are actually offsets from CAPPTR (Rx34) which (with Rx34 = A0h for AGP 2.0) result in the offsets listed above.

Offset	AGP 3.0 Control (RxFD[1]=0)	Default	Acc
83-80	AGP 3.0 Capabilities	**0030 C002**	**RO**
87-84	AGP 3.0 Status	**1F00 0A03**	**RO**
8B-88	AGP 3.0 Command	**1F00 0000**	RW
8F-8C	-reserved-	0000 0000	—
93-90	AGP 3.0 GART / TLB Control	0000 0000	RW
97-94	AGP 3.0 Graphics Aperture Size	**0001 0F00**	RW
9B-98	AGP 3.0 GART Table Base	0000 0000	RW
9C-AB	-reserved-	00	—

Registers 80-AB in the AGP 3.0 register group in the table above are actually offsets from CAPPTR (Rx34) which (with Rx34 = 80h for AGP 3.0) result in the offsets listed above.

Offset	AGP 2.0 / 3.0 Control	Default	Acc
AC	AGP Control	00	RW
AD	AGP Latency Timer	**02**	RW
AE	AGP Miscellaneous Control	00	RW
AF	AGP 3.0 Control	00	RW
B0	AGP Pad Control / Status	**8x**	RW
B1	AGP Drive Strength	**63**	RW
B2	AGP Pad Drive / Delay Control	**08**	RW
B3	AGP Strobe Output Drive Control	00	RW

Offset	V-Link Compenation / Drive Ctrl	Default	Acc
B4	V-Link NB Compensation Control	00	RW
B5	V-Link NB Strobe Drive Control	00	RW
B6	V-Link NB Data Drive Control	00	RW
B7	-reserved-	00	—
B8	V-Link SB Compensation Control	00	RW
B9	V-Link SB Strobe Drive Control	00	RW
BA	V-Link SB Data Drive Control	00	RW
BB	-reserved-	00	—

Offset	Power Management Control	Default	Acc
BC	Power Management Mode	00	RW
BD	DRAM Power Management	00	RW
BE	Dynamic Clock Stop	00	RW
BF	MA / SCMD Pad Toggle Reduction	00	RW

Device 0 Device-Specific Registers (continued)

Offset	Extended Power Management Ctrl	Default	Acc
C0	Power Management Capability	**01**	**RO**
C1	Power Management Next Pointer	00	**RO**
C2	Power Management Capabilities I	02	**RO**
C3	Power Management Capabilities II	00	**RO**
C4	Power Management Control/Status	00	RW
C5	Power Management Status	00	**RO**
C6	PCI-to-PCI Bridge Support Extension	00	**RO**
C7	Power Management Data	00	**RO**
C8-CF	-reserved-	00	—

Offset	Error Control	Default	Acc
D3-D0	DRAM ECC Error Address	xx	**RO**
D4	DRAM ECC Error Syndrome Bit	xx	**RO**
D5	Host CPU Parity Status	00	**WC**
D6	Host CPU Parity Enable	00	RW
D7	-reserved-	00	—

Offset	Host CPU AGTL+ I/O Control	Default	Acc
D8	Host Address (2x) Pullup Drive	00	RW
D9	Host Address (2x) Pulldown Drive	00	RW
DA	Host Data (4x) Pullup Drive	00	RW
DB	Host Data (4x) Pulldown Drive	00	RW
DC	AGTL+ Output Delay / Stagger Ctrl	00	RW
DD	AGTL+ I/O Control	00	RW
DE	AGTL+ Compensation Status	00	RW
DF	AGTL+ AutoCompensation Offset	00	RW

Offset	DRAM Control	Default	Acc
E0-E3	-reserved-	00	—
E4	Low Top Address Low	00	RW
E5	Low Top Address High	**FF**	RW
E6	SMM / APIC Decoding	**01**	RW
E7	-reserved-	00	—
E8	DRAM DQ Drive	00	RW
E9	DRAM CS Drive	00	RW
EA	DRAM MAA Drive	00	RW
EB	DRAM MAB Drive	00	RW
EC-ED	-reserved-	00	—

Offset	P6 Interface DRDY Timing Control	Default	Acc
EE	DRDY Timing 1	00	RW
EF	DRDY Timing 2	00	RW

Offset	Miscellaneous	Default	Acc
F0-FC	-reserved- (Do Not Program)	00	—
FD	AGP 2.0 / 3.0 Select	00	RW
FE-FF	-reserved- (Do Not Program)	00	—

P4X400 Device 1 Registers - PCI-to-PCI Bridge

Header Registers

Offset	Configuration Space Header	Default	Acc
1-0	Vendor ID	**1106**	RO
3-2	Device ID	**B168**	RO
5-4	Command	**0007**	**RW**
7-6	Status	**0230**	**WC**
8	Revision ID	**nn**	RO
9	Program Interface	00	RO
A	Sub Class Code	**04**	RO
B	Base Class Code	**06**	RO
C	-reserved-	00	—
D	Latency Timer	00	RO
E	Header Type	**01**	RO
F	-reserved- (Built In Self Test)	00	—
10-17	-reserved-	00	—
18	Primary Bus Number	00	**RW**
19	Secondary Bus Number	00	**RW**
1A	Subordinate Bus Number	00	**RW**
1B	Secondary Latency Timer	00	RO
1C	I/O Base	**F0**	**RW**
1D	I/O Limit	00	**RW**
1F-1E	Secondary Status	0000	RO
21-20	Memory Base	**FFF0**	**RW**
23-22	Memory Limit (Inclusive)	0000	**RW**
25-24	Prefetchable Memory Base	**FFF0**	**RW**
27-26	Prefetchable Memory Limit	0000	**RW**
28-33	-reserved-	00	—
34	Capability Pointer	**80**	RO
35-3D	-reserved-	00	—
3F-3E	PCI-to-PCI Bridge Control	00	**RW**

Device-Specific Registers

Offset	AGP Bus Control	Default	Acc
40	CPU-to-AGP Flow Control 1	00	RW
41	CPU-to-AGP Flow Control 2	**08**	RW
42	AGP Master Control	00	RW
43	AGP Master Latency Timer	**22**	RW
44	Reserved (Do Not Program)	00	RW
45	Fast Write Control	**72**	RW
47-46	PCI-to-PCI Bridge Device ID	0000	RW
48	AGP / PCI2 Error Reporting	00	**WC**
49-7F	-reserved-	00	—

Offset	Power Management	Default	Acc
80	Capability ID	**01**	**RO**
81	Next Pointer	00	**RO**
82	Power Management Capabilities 1	**02**	**RO**
83	Power Management Capabilities 2	00	**RO**
84	Power Management Control / Status	00	RW
85	Power Management Status	00	**RO**
86	PCI-PCI Bridge Support Extensions	00	**RO**
87	Power Management Data	00	**RO**
88-FF	-reserved-	00	—

Miscellaneous I/O

One I/O port is defined in the P4X400: Port 22.

Port 22 – PCI / AGP Arbiter Disable .....RW

7-2 Reserved ..... always reads 0

1 AGP Arbiter Disable
- 0 Respond to GREQ# signal .....default
- 1 Do not respond to GREQ# signal

0 PCI Arbiter Disable
- 0 Respond to all REQ# signals .....default
- 1 Do not respond to any REQ# signals, including PREQ#

This port can be enabled for read/write access by setting bit-7 of Device 0 Configuration Register 78.

Configuration Space I/O

All registers in the P4X400 (listed above) are addressed via the following configuration mechanism:

Mechanism #1

These ports respond only to double-word accesses. Byte or word accesses will be passed on unchanged.

Port CFB-CF8 - Configuration Address..... RW

31 Configuration Space Enable
- 0 Disabled..... default
- 1 Convert configuration data port writes to configuration cycles on the PCI bus

30-24 Reserved .....always reads 0

23-16 PCI Bus Number
Used to choose a specific PCI bus in the system

15-11 Device Number
Used to choose a specific device in the system (devices 0 and 1 are defined for the P4X400)

10-8 Function Number
Used to choose a specific function if the selected device supports multiple functions (only function 0 is defined for the P4X400).

7-2 Register Number (also called the "Offset")
Used to select a specific DWORD in the P4X400 configuration space

1-0 Fixed .....always reads 0

Port CFF-CFC - Configuration Data..... RW

Refer to PCI Bus Specification Version 2.2 for further details on operation of the above configuration registers.

Device 0 Register Descriptions

Device 0 Host Bridge Header Registers

All registers are located in PCI configuration space. They should be programmed using PCI configuration mechanism 1 through CF8 / CFC with bus number, function number, and device number equal to zero.

Device 0 Offset 1-0 - Vendor ID (1106h) .....RO

15-0 ID Code (reads 1106h to identify VIA Technologies)

Device 0 Offset 3-2 - Device ID (3168h).....RO

15-0 ID Code (reads 3168h to identify the P4X400)

Device 0 Offset 5-4 –Command (0006h).....RW

15-10 Reserved ..... always reads 0

9 Fast Back-to-Back Cycle Enable ..... RO
- 0 Fast back-to-back transactions only allowed to the same agent.....default
- 1 Fast back-to-back transactions allowed to different agents

8 SERR# Enable..... RO
- 0 SERR# driver disabled.....default
- 1 SERR# driver enabled

(SERR# is used to report ECC errors).

7 Address / Data Stepping..... RO
- 0 Device never does stepping.....default
- 1 Device always does stepping

6 Parity Error Response.....RW
- 0 Ignore parity errors & continue.....default
- 1 Take normal action on detected parity errors

5 VGA Palette Snoop..... RO
- 0 Treat palette accesses normally.....default
- 1 Don't respond to palette accesses on PCI bus

4 Memory Write and Invalidate Command ..... RO
- 0 Bus masters must use Mem Write.....default
- 1 Bus masters may generate Mem Write & Inval

3 Special Cycle Monitoring..... RO
- 0 Does not monitor special cycles.....default
- 1 Monitors special cycles

2 PCI Bus Master..... RO
- 0 Never behaves as a bus master
- 1 Can behave as a bus master.....default

1 Memory Space..... RO
- 0 Does not respond to memory space
- 1 Responds to memory space.....default

0 I/O Space ..... RO
- 0 Does not respond to I/O space .....default
- 1 Responds to I/O space

Device 0 Offset 7-6 – Status (0210h).....RWC

15 Detected Parity Error
- 0 No parity error detected..... default
- 1 Error detected in either address or data phase. This bit is set even if error response is disabled (command register bit-6). .....write one to clear

14 Signaled System Error (SERR# Asserted) .....always reads 0

13 Signaled Master Abort
- 0 No abort received ..... default
- 1 Transaction aborted by the master ....write one to clear

12 Received Target Abort
- 0 No abort received ..... default
- 1 Transaction aborted by the target ....write one to clear

11 Signaled Target Abort .....always reads 0
- 0 Target Abort never signaled

10-9 DEVSEL# Timing
- 00 Fast
- 01 Medium .....always reads 01
- 10 Slow
- 11 Reserved

8 Data Parity Error Detected
- 0 No data parity error detected ..... default
- 1 Error detected in data phase. Set only if error response enabled via command bit-6 = 1 and P4X400 was initiator of the operation in which the error occurred. .....write one to clear

7 Fast Back-to-Back Capable.....always reads 0

6 User Definable Features .....always reads 0

5 66MHz Capable.....always reads 0

4 Supports New Capability list.....always reads 1

3-0 Reserved .....always reads 0

Device 0 Offset 8 - Revision ID (0nh)..... RO

7-0 Chip Revision Code.....always reads 0nh

Device 0 Offset 9 - Programming Interface (00h)..... RO

7-0 Interface Identifier.....always reads 00h

Device 0 Offset A - Sub Class Code (00h)..... RO

7-0 Sub Class Code.....reads 00 to indicate Host Bridge

Device 0 Offset B - Base Class Code (06h)..... RO

7-0 Base Class Code.. reads 06 to indicate Bridge Device

Device 0 Offset D - Latency Timer (00h)..... RW

Specifies the latency timer value in PCI bus clocks.

7-3 Guaranteed Time Slice for CPU ..... default=0

2-0 Reserved (fixed granularity of 8 clks).. always read 0
Bits 2-1 are writeable but read 0 for PCI specification compatibility. The programmed value may be read back in Rx75[6-4] (PCI Arbitration 1).

Device 0 Host Bridge Header Registers (continued)

Device 0 Offset E - Header Type (00h).....RO

7-0 Header Type Code ..... reads 00: single function

Device 0 Offset F - Built In Self Test (BIST) (00h).....RO

7 BIST Supported .....reads 0: no supported functions

6-0 Reserved ..... always reads 0

Device 0 Offset 13-10 - Graphics Aperture Base (AGP 2.0) (00000008h) .....RW

This register is interpreted per the following definition if RxFD[1]=1 (AGP 2.0 registers enabled).

31-28 Upper Programmable Base Address Bits ..... def=0

27-20 Lower Programmable Base Address Bits ..... def=0

These bits behave as if hardwired to 0 if the corresponding AGP 2.0 Graphics Aperture Size register bit (Device 0 Offset 84h) is 0.

27	26	25	24	23	22	21	20	(Base)
7	6	5	4	3	2	1	0	(Size)
RW	RW	RW	RW	RW	RW	RW	RW	1M
RW	RW	RW	RW	RW	RW	RW	0	2M
RW	RW	RW	RW	RW	RW	0	0	4M
RW	RW	RW	RW	RW	0	0	0	8M
RW	RW	RW	RW	0	0	0	0	16M
RW	RW	RW	0	0	0	0	0	32M
RW	RW	0	0	0	0	0	0	64M
RW	0	0	0	0	0	0	0	128M
0	0	0	0	0	0	0	0	256M

19-4 Reserved ..... always reads 0

3 Prefetchablealways reads 1

Indicates that the locations in the address range defined by this register are prefetchable.

2-1 Type ..... always reads 0

Indicates the address range in the 32-bit address space.

0 Memory Space..... always reads 0

Indicates the address range in the memory address space.

Device 0 Offset 13-10 - Graphics Aperture Base (AGP 3.0) (00000008h) ..... RW

This register is interpreted per the following definition if RxFD[1]=0 (AGP 3.0 registers enabled). This register may only be read if AGP 3.0 register Rx90[8] = 1.

31-22 Programmable Base Address Bits ..... def=0

These bits behave as if hardwired to 0 if the corresponding AGP 3.0 Graphics Aperture Size register bit (Device 0 Offset 94h) is 0.

31	30	29	28	-	-	27	26	25	24	23	22	(Base)
11	10	9	8	7	6	5	4	3	2	1	0	(Size)
RW	RW	RW	RW	0	0	RW	RW	RW	RW	RW	RW	4M
RW	RW	RW	RW	0	0	RW	RW	RW	RW	RW	0	8M
RW	RW	RW	RW	0	0	RW	RW	RW	RW	0	0	16M
RW	RW	RW	RW	0	0	RW	RW	RW	0	0	0	32M
RW	RW	RW	RW	0	0	RW	RW	0	0	0	0	64M
RW	RW	RW	RW	0	0	RW	0	0	0	0	0	128M
RW	RW	RW	RW	0	0	0	0	0	0	0	0	256M
RW	RW	RW	0	0	0	0	0	0	0	0	0	512M
RW	RW	0	0	0	0	0	0	0	0	0	0	1G
RW	0	0	0	0	0	0	0	0	0	0	0	2G-max
0	0	0	0	0	0	0	0	0	0	0	0	4G

21-4 Reserved ..... always reads 0

3 Prefetchablealways reads 1

Indicates that the locations in the address range defined by this register are prefetchable.

2-1 Type ..... always reads 0

Indicates the address range in the 32-bit address space.

0 Memory Space..... always reads 0

Indicates the address range in the memory address space.

Device 0 Offset 2D-2C – Subsystem Vendor ID (0000h)R/W1

15-0 Subsystem Vendor ID ..... default = 0

This register may be written once and is then read only.

Device 0 Offset 2F-2E – Subsystem ID (0000h)..... R/W1

15-0 Subsystem ID ..... default = 0

This register may be written once and is then read only.

Device 0 Offset 34 - Capability Pointer (CAPPTR)..... RO

Contains an offset from the start of configuration space.

7-0 AGP Capability List Pointer ..... always reads A0h

Device 0 Host Bridge Device-Specific Registers

These registers are normally programmed once at system initialization time.

V-Link Control

Device 0 Offset 40 – V-Link Specification ID (00h) .....RO

7-0 Specification Revision..... always reads 00

Device 0 Offset 41 – NB V-Link Capability (19h) .....WC

7 V-Link Parity Error Detected by NB.....WC
- 0 No V-Link Parity Error Detected.....default
- 1 V-Link Parity Error Detected (write 1 to clear)

6 Reserved ..... always reads 0

5 16-bit Bus Width Supported by NB .....RO
- 0 Not Supported.....default
- 1 Supported

4 8-Bit Bus Width Supported by NB.....RO
- 0 Not Supported
- 1 Supported**.....default**

3 4x Rate Supported by NB.....RO
- 0 Not Supported
- 1 Supported**.....default**

2 2x Rate Supported by NB.....RO
- 0 Not Supported.....default
- 1 Supported

1 Reserved ..... always reads 0

0 8x Rate Supported by NB.....RO
- 0 Not Supported
- 1 Supported**.....default**

Device 0 Offset 42 – NB Downlink Command (88h) .....RW

7-4 DnCmd Max Request Depth (0=1 DnCmd) . def = 8

3-0 DnCmd Write Buffer Size (doublewords)..... def = 8

Device 0 Offset 43 – NB Uplink Max Req Depth (80h)...RO

7-4 UpCmd Max Request Depth (0=1 UpCmd) . def = 8
Indicates the maximum allowable number of outstanding UPCMD requests

3-0 Reserved ..... always reads 0

Device 0 Offset 44 – NB Uplink Buffer Size (82h).....RO

7-4 UpCmd P2C Write Buffer Size (max lines).. def = 8

3-0 UpCmd P2P Write Buffer Size (max lines).. def = 2

Device 0 Offset 45 –NB V-Link Bus Timer (44h)..... RW

7-4 Timer for Normal Priority Requests from SB
- 0000 Immediate
- 0001 1*4 VCLKs
- 0010 2*4 VCLKs
- 0011 3*4 VCLKs
- 0100 4*4 VCLKs ..... default
- 0101 5*4 VCLKs
- 0110 6*4 VCLKs
- 0111 7*4 VCLKs
- 1000 8*4 VCLKs
- 1001 16*4 VCLKs
- 1010 32*4 VCLKs
- 1011 64*4 VCLKs
- 11xx Own the bus for as long as there is a request

3-0 Timer for High Priority Requests from SB
- 0000 Immediate
- 0001 1*2 VCLKs
- 0010 2*2 VCLKs
- 0011 3*2 VCLKs
- 0100 4*2 VCLKs ..... default
- 0101 5*2 VCLKs
- 0110 6*2 VCLKs
- 0111 7*2 VCLKs
- 1000 8*2 VCLKs
- 1001 16*2 VCLKs
- 1010 32*2 VCLKs
- 1011 64*2 VCLKs
- 11xx Own the bus for as long as there is a request

Device 0 Offset 46 – NB V-Link Misc Control (00h).....RW

7 Downstream High Priority
- 0 Disable High Priority Down Commands .....def
- 1 Enable High Priority Down Commands

6 Downlink Priority
- 0 Treat Downlink Cycles as Normal Priority.def
- 1 Treat Downlink Cycles as High Priority

5-4 Combine Multiple STPGNT Cycles Into One V-Link Command
- 00 Compatible, 1 command per V-Link cmd....def
- 01 2 commands per V-Link command
- 10 3 commands per V-Link command
- 11 4 commands per V-Link command

3-2 V-Link Master Access Ordering Rules
- 00 High priority read, pass normal read (not pass write) .....default
- 01 Read (high/normal) pass write (HR>LR>W)
- 1x Read / write in order

1-0 Reserved ..... always reads 0

Device 0 Offset 47 – V-Link Control (00h) .....RW

7 Parity Error or SERR# Reported via NMI
- 0 Disable .....default
- 1 Enable

6 Parity Error or SERR# Reported to SB via Vlink
- 0 Disable .....default
- 1 Enable

5 C2P Read L1 Ready Return Timing
- 0 V-Link bus decodes C2P Read Ack cmd.....def
- 1 Wait till previous P2C write cycles all flushed

4 Reserved ..... always reads 0

3 Down Strobe Dynamic Stop
- 0 Disable .....default
- 1 Enable

2 Auto-Disconnect
- 0 Disable .....default
- 1 Enable

1 V-Link Disconnect Cycle for HALT Cycle
- 0 Disable .....default
- 1 Enable

0 V-Link Disconnect Cycle for STPGNT Cycle
- 0 Disable .....default
- 1 Enable

Device 0 Offset 48 – NB/SB V-Link Configuration (18h)RW

7 V-Link Parity Check
- 0 Disable..... default
- 1 Enable

6 Rest Bus Width Supported
- 0 Not Supported ..... default
- 1 Supported

5 16-bit Bus Width Supported
- 0 Not Supported ..... default
- 1 Supported

4 8-Bit Bus Width Supported
- 0 Not Supported
- 1 Supported ..... **default**

3 4x Rate Supported
- 0 Not Supported
- 1 Supported ..... **default**

2 2x Rate Supported
- 0 Not Supported ..... default
- 1 Supported

1 Reserved .....always reads 0

0 8x Rate Supported
- 0 Not Supported ..... default
- 1 Supported

Device 0 Offset 49 – SB V-Link Capability (19h) ..... WC

7 V-Link Parity Error Detected by SB..... WC
- 0 No parity error detected..... default
- 1 Parity error detected

6 Reserved .....always reads 0

5 16-bit Bus Width Supported by SB ..... RO
- 0 Not Supported ..... default
- 1 Supported

4 8-Bit Bus Width Supported by SB..... RO
- 0 Not Supported
- 1 Supported ..... **default**

3 4x Rate Supported by SB..... RO
- 0 Not Supported
- 1 Supported ..... **default**

2 2x Rate Supported by SB..... RO
- 0 Not Supported ..... default
- 1 Supported

1 Reserved .....always reads 0

0 8x Rate Supported by SB..... RO
- 0 Not Supported
- 1 Supported ..... **default**

Device 0 Offset 4A – SB Downlink Status (88h) .....RO

7-4 DnCmd Max Request Depth (0=1 DnCmd) . def = 8
3-0 DnCmd Write Buffer Size (doublewords)..... def = 8

Device 0 Offset 4B – SB Uplink Command (80h).....RW

7-4 UpCmd Max Request Depth (0=1 UpCmd) . def = 8
Indicates the maximum allowable number of outstanding UPCMD requests
3-0 Reserved ..... always reads 0

Device 0 Offset 4C – SB Uplink Command (82h).....RW

7-4 UpCmd P2C Write Buffer Size (max lines).. def = 8
3-0 UpCmd P2P Write Buffer Size (max lines) .. def = 2

Device 0 Offset 4D – SB V-Link Bus Timer (44h).....RW

7-4 Timer for Normal Priority Requests from NB
0000 Immediate
0001 1*4 VCLKs
0010 2*4 VCLKs
0011 3*4 VCLKs
0100 4*4 VCLKs.....default
0101 5*4 VCLKs
0110 6*4 VCLKs
0111 7*4 VCLKs
1000 8*4 VCLKs
1001 16*4 VCLKs
1010 32*4 VCLKs
1011 64*4 VCLKs
11xx Own the bus for as long as there is a request

3-0 Timer for High Priority Requests from NB
0000 Immediate
0001 1*2 VCLKs
0010 2*2 VCLKs
0011 3*2 VCLKs
0100 4*2 VCLKs.....default
0101 5*2 VCLKs
0110 6*2 VCLKs
0111 7*2 VCLKs
1000 8*2 VCLKs
1001 16*2 VCLKs
1010 32*2 VCLKs
1011 64*2 VCLKs
11xx Own the bus for as long as there is a request

Device 0 Offset 4E – CCA Master Priority (00h)..... RW

7 1394 High Priority
0 Low priority..... default
1 High priority
6 LAN / NIC High Priority
0 Low priority..... default
1 High priority
5 Reserved .....always reads 0
4 USB High Priority
0 Low priority..... default
1 High priority
3 Reserved .....always reads 0
2 IDE High Priority
0 Low priority..... default
1 High priority
1 AC97-ISA High Priority
0 Low priority..... default
1 High priority
0 PCI High Priority
0 Low priority..... default
1 High priority

Device 0 Offset 4F – SB V-Link Misc Control (00h) ..... RW

7 Upstream Command High Priority
0 Disable high priority up commands..... default
1 Enable high priority up commands
6-4 Reserved .....always reads 0
3 Up Strobe Dynamic Stop
0 Disable..... default
1 Enable
2-1 Reserved .....always reads 0
0 Down Cycle Wait for Up Cycle Write Flush (Except Down Cycle Post Write)
0 Disable..... default
1 Enable

Host CPU Control

Device 0 Offset 50 – Request Phase Control (00h) .....RW

7 CPU Hardwired IOQ (In Order Queue) Size
Default set from the inverse of the VAD2 strap. This register can be written 0 to restrict the chip to one level of IOQ.
- 0 1-Level (strap pulled high)
- 1 12-Level (strap pulled low)

6 Reserved (Do Not Program)
Default set from the VAD7 strap (South Bridge SDCS3# pin) or ROMSIP.
- 0 South Bridge strap pin pulled low..... must be 0
- 1 South Bridge strap pin pulled high

5 Fast DRAM Access
- 0 Disable .....default
- 1 Enable

4-0 Dynamic Defer Snoop Stall Count
(granularity = 2T, normally set to 01000b)

Device 0 Offset 51 – CPU Interface Basic Control (00h)RW

7 CPU Read DRAM Fast Ready
- 0 Wait until all 8 QWs are received before DRDY is returned..... default
- 1 See RxEE/EF for DRDY timing

6 Read Around Write
- 0 Disable..... default
- 1 Enable

5 DRQ Control
- 0 Non pipelined similar to VT8633 ..... default
- 1 Pipelined

4 CPU to PCI Read Defer
- 0 Disable..... default
- 1 Enable

3 Two Defer / Retry Entries
- 0 Disable..... default
- 1 Enable

2 Two Defer / Retry Entries Shared
- 0 Each entry is dedicated to 1 CPU ..... default
- 1 Each entry is shared by 2 CPUs

1 PCI Master Pipelined Access
- 0 Disable..... default
- 1 Enable

0 Fast DRDY#
- 0 Synchronize DMRRDY to DRDY# ..... default
- 1 DMRRDY to DRDY# fall-through

Device 0 Offset 52 – CPU Interface Advanced Ctrl (00h)RW

7 CPU RW DRAM 0WS for Back-to-Back Pipeline Access
- 0 Disable .....default
- 1 Enable

6 HREQ High Priority
- 0 Disable .....default
- 1 Enable

5 AGTL+ Pullups
Default set from the inverse of the VAD3 strap.
- 0 Disable (strap pulled high)
- 1 Enable (strap pulled low)

4 Reserved ..... always reads 0

3 Write Retire Policy After 2 Writes
- 0 Disable .....default
- 1 Enable

2 2-Level Defer Queue with Lock
- 0 Normal Operation .....default
- 1 Enhanced Operation (this bit should always be set to 1)

1 Consecutive Speculative Read
- 0 Disable .....default
- 1 Enable

0 Speculative Read
- 0 Disable .....default
- 1 Enable

Device 0 Offset 53 – CPU Arbitration Control (00h).....RW

7-4 Host Timer ..... default = 0

3-0 BPRI Timer (units of 4 HCLKs)..... default = 0

Device 0 Offset 54 – CPU Frequency (00h) ..... RW

7-6 CPU FSB Frequency.....Set from VAD1-0 Straps
- 00 100 MHz (both straps pulled low)
- 01 133 MHz (VAD1 pulled low, VAD0 pulled hi)
- 1x 166 MHz (VAD1 pulled high, VAD0 ignored)

(166 MHz capability is new in the VT8754; the VT8753 was fixed at 100 MHz FSB and the VT8753A allowed 100 and 133 MHz)

5 Auto Configure..... Set from VAD6 Strap
- 0 Disable (strap pulled low)
- 1 Enable (strap pulled high). AGTL+ Drive settings and other chip configuration settings are stored in ROM, transferred from the south bridge (via the V-Link bus), and loaded into the VT8754 automatically after system reset. Refer to the VT8754 BIOS Porting Guide for layout of the AutoConfigure settings in ROM and for recommended bit settings.

4 SDRAM Burst Length of 8
- 0 Disable..... default
- 1 Enable

3 Rx85, 86, and 87 Writeable
- 0 Disable..... default
- 1 Enable

2 PCI Master 8QW Operation
- 0 Disable..... default
- 1 Enable

1 Reserved .....always reads 0

0 VPX Mode
- 0 Disable (AGP Mode)..... default
- 1 Enable (VPX Mode)

DRAM Control

These registers are normally set at system initialization time and not accessed after that during normal system operation. Some of these registers, however, may need to be programmed using specific sequences during power-up initialization to properly detect the type and size of installed memory (refer to the VIA Technologies VT8754 BIOS porting guide for details).

Table 5. System Memory Map

Space	Start	Size	Address Range	Comment
DOS	0	640K	00000000-0009FFFF	Cacheable
VGA	640K	128K	000A0000-000BFFFF	Used for SMM
BIOS	768K	16K	000C0000-000C3FFF	Shadow Ctrl 1
BIOS	784K	16K	000C4000-000C7FFF	Shadow Ctrl 1
BIOS	800K	16K	000C8000-000CBFFF	Shadow Ctrl 1
BIOS	816K	16K	000CC000-000CFFFF	Shadow Ctrl 1
BIOS	832K	16K	000D0000-000D3FFF	Shadow Ctrl 2
BIOS	848K	16K	000D4000-000D7FFF	Shadow Ctrl 2
BIOS	864K	16K	000D8000-000DBFFF	Shadow Ctrl 2
BIOS	880K	16K	000DC000-000DFFFF	Shadow Ctrl 2
BIOS	896K	64K	000E0000-000EFFFF	Shadow Ctrl 3
BIOS	960K	64K	000F0000-000FFFFF	Shadow Ctrl 3
Sys Bus Init	1MB D Top 4G-64K	— 64K	00100000-DRAM Top DRAM Top-FFFEFFFF FFFEFFFF-FFFFFFFF	Can have hole 000Fxxxx alias

Device 0 Offset 55 – DRAM Control (00h)..... RW

7 0WS Back-to-Back Write to Different DDR Bank
- 0 Disable..... default
- 1 Enable

6 Fast Read to Read Turnaround
- 0 Disable..... default
- 1 Enable (DQS postamble overlap with preamble)

5 DQS Input DLL Adjust
- 0 Disable..... default
- 1 Enable

4 DQS Output DLL Adjust
- 0 Disable..... default
- 1 Enable

3 DQM Removal (Always Perform 4-Burst RW)
- 0 Disable..... default
- 1 Enable

2 DQS Output
- 0 Disable..... default
- 1 Enable

1 Auto Precharge for TLB Read or CPU WriteBack
- 0 Disable..... default
- 1 Enable

0 Write Recovery Time
- 0 2T (for DDR 266)..... default
- 1 3T (for DDR 333)

Device 0 Offset 59-58 - DRAM MA Map Type (2222h).RW

15-13 Bank 5/4 MA Map Type (see table below)

12 Bank 5/4 1T Command Rate
- 0 2T Command .....default
- 1 1T Command

11-9 Bank 7/6 MA Map Type (see table below)

8 Bank 7/6 1T Command Rate
- 0 2T Command .....default
- 1 1T Command

7-5 Bank 1/0 MA Map Type (see table below)

4 Bank 1/0 1T Command Rate
- 0 2T Command .....default
- 1 1T Command

3-1 Bank 3/2 MA Map Type (see table below)

0 Bank 3/2 1T Command Rate
- 0 2T Command .....default
- 1 1T Command

Table 6. Device 0 Rx58 MA Map Type Encoding

000	16Mb	8 / 9 / 10-bit Column Address
001	64/128Mb	8 / 9-bit Column Address.....default
010	64/128Mb	9 / 10-bit Column Address
011	64/128Mb	10 / 11-bit Column Address
100	1Gb	10 / 11 / 12-bit Column Address
101	256/512Mb	8-bit Column Address
110	256/512Mb	9-bit Column Address
111	256/512Mb	10 / 11 / 12-bit Column Address

Device 0 Offset 5F-5A – DRAM Row Ending Address:

Offset 5A – Bank 0 Ending (HA[31:24]) (01h)..... RW
Offset 5B – Bank 1 Ending (HA[31:24]) (01h)..... RW
Offset 5C – Bank 2 Ending (HA[31:24]) (01h)..... RW
Offset 5D – Bank 3 Ending (HA[31:24]) (01h)..... RW
Offset 5E – Bank 4 Ending (HA[31:24]) (01h)..... RW
Offset 5F – Bank 5 Ending (HA[31:24]) (01h)..... RW
Offset 56 – Bank 6 Ending (HA[31:24]) (01h)..... RW
Offset 57 – Bank 7 Ending (HA[31:24]) (01h)..... RW

Note : BIOS is required to fill the ending address registers for all banks even if no memory is populated. The endings have to be in incremental order.

Device 0 Offset 60 – DRAM Type (80h)..... RW

7-6 DRAM Type for All Banks
- 00 -reserved- (do not program)
- 01 -reserved- (do not program)
- 10 DDR SDRAM ..... **default**
- 11 -reserved-

Different DRAM types cannot be mixed.

5-0 Reserved .....always reads 0

Table 7. DDR DRAM Memory Address Mapping Table

MA:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
16Mb (000)			24		13	12	11	14	22	21	20	19	18	17	16	15	12 row
					13	PC	24	23	10	9	8	7	6	5	4	3	10,9,8 col
64/128Mb																	x16 (14,8)
2K page		14	24	14	13	12	11	23	22	21	20	19	18	17	16	15	x32 (14,8)
001			27	14	13	PC	26	25	10	9	8	7	6	5	4	3	x8 (14,9)
4K page		14	25	14	13	12	24	23	22	21	20	19	18	17	16	15	x16 (14,9)
010			27	14	131	PC	26	11	10	9	8	7	6	5	4	3	x4 (14,10)
8K page		14	26	14	3	25	24	23	22	21	20	19	18	17	16	15	x8 (14,10)
011			27	14	13	PC	12	11	10	9	8	7	6	5	4	3	x4 (14,11)
256/512Mb																	
2K page		25	24	14	13	12	11	23	22	21	20	19	18	17	16	15	x32 (15,8)
101			27	14	13	PC	26	25	10	9	8	7	6	5	4	3	
4K page		26	25	14	13	12	24	23	22	21	20	19	18	17	16	15	x16 (15,9)
110			27	14	131	PC	26	11	10	9	8	7	6	5	4	3	x32 (15,9)
8K page		27	26	14	3	25	24	23	22	21	20	19	18	17	16	15	x8 (15,10)
111			28	14	13	PC	12	11	10	9	8	7	6	5	4	3	x16 (15,10)
																	x8 (15,11)
																	x4 (15,11)
																	x4 (15,12)
1Gb																	
8K page	28	27	26	14	13	25	24	23	22	21	20	19	18	17	16	15	x16 (16,10)
100	31	30	29	14	13	PC	12	11	10	9	8	7	6	5	4	3	x8 (16,11)
																	x4 (16,12)

Device 0 Offset 61 - Shadow RAM Control 1 (00h).....RW

7-6 CC000h-CFFFFh
- 00 Read/write disable.....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

5-4 C8000h-CBFFFh
- 00 Read/write disable.....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

3-2 C4000h-C7FFFh
- 00 Read/write disable.....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

1-0 C0000h-C3FFFh
- 00 Read/write disable.....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

Device 0 Offset 62 - Shadow RAM Control 2 (00h).....RW

7-6 DC000h-DFFFFh
- 00 Read/write disable.....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

5-4 D8000h-DBFFFh
- 00 Read/write disable.....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

3-2 D4000h-D7FFFh
- 00 Read/write disable.....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

1-0 D0000h-D3FFFh
- 00 Read/write disable.....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

Device 0 Offset 63 - Shadow RAM Control 3 (00h)..... RW

7-6 E0000h-EFFFFh
- 00 Read/write disable ..... default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

5-4 F0000h-FFFFFh
- 00 Read/write disable ..... default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

3-2 Memory Hole
- 00 None ..... default
- 01 512K-640K
- 10 15M-16M (1M)
- 11 14M-16M (2M)

1 Disable A,BK SMRAM Direct Access

0 Enable A,BK DRAM Access

SMI Mapping Control:

Bits	SMM		Non-SMM	
1-0	Code	Data	Code	Data
00	DRAM	DRAM	PCI	PCI
01	DRAM	DRAM	DRAM	DRAM
10	DRAM	PCI	PCI	PCI
11	DRAM	DRAM	DRAM	DRAM

Device 0 Offset 64 - DRAM Timing for All Banks (E4h)RW

7 Precharge Command to Active Command Period
- 0 TRP = 2T
- 1 TRP = 3T.....**default**

6 Active Command to Precharge Command Period
- 0 TRAS = 6T
- 1 TRAS = 7T.....**default**

5-4 CAS Latency
- 00 1.5T
- 01 2T
- 10 2.5T .....**default**
- 11 3T

3 Reserved ..... always reads 0

2 ACTIVE to CMD
- 0 2T
- 1 3T .....**default**

1-0 Bank Interleave
- 00 No Interleave.....default
- 01 2-way
- 10 4-way
- 11 Reserved

For 16Mb DRAMs bank interleave is always 2-way

Device 0 Offset 65 - DRAM Arbitration Timer (00h) ....RW

7-4 AGP Timer (units of 4 DRAM clocks) .... default = 0

3-0 CPU Timer (units of 4 DRAM clocks)..... default = 0

Device 0 Offset 66 - DRAM Arbitration Control (00h)..RW

7 DQS Input Delay Setting
- 0 Auto (Rx67 reads DLL calibration result) ...def
- 1 Manual (Rx67 reads DQS input delay)

6 DRAM Access Timing
- 0 2T .....default
- 1 3T (set this bit for 133 MHz DRAM clock)

5-4 Arbitration Parking Policy
- 00 Park at last bus owner .....default
- 01 Park at CPU
- 10 Park at AGP
- 11 -reserved-

3-0 AGP / CPU Priority (units of 4 DRAM clocks)

Device 0 Offset 67 – Strobe Input Delay (00h).....RW

7-6 Reserved ..... always reads 0

5-0 DQS Input Delay..... default = 0

(if Rx66[7]=0, read DLL calibration result)

Device 0 Offset 68 – Strobe Output Delay (00h).....RW

7-0 DQS Output Delay ..... default = 0

Device 0 Offset 69 – DRAM Clock Select (00h) ..... RW

7 Host CPU 100 MHz, DRAM 166 MHz
- 0 Disable..... default
- 1 Enable

6 DRAM Operating Frequency Faster Than CPU
- 0 DRAM Same As or Equal to CPU ..... default
- 1 DRAM Faster Than CPU

	CPU / DRAM	Rx54[7-6]	Rx69[7]
0	100 / 100 (DDR-200)	00	0 ..... def
0	133 / 133 (DDR-266)	01	0
0	166 / 166 (DDR-333)	1x	0
1	100 / 133 (DDR-266)	00	0
1	133 / 166 (DDR-333)	01	0
1	100 / 166 (DDR-333)	00	1

All other combinations are reserved.

5 DRAM Ctrlr Queue Greater Than 2
- 0 Disable..... default
- 1 Enable

4 DRAM Ctrlr Queue Not Equal To 4
- 0 Disable..... default
- 1 Enable

3 DRAM 8K Page Enable
- 0 Disable..... default
- 1 Enable

2 DRAM 4K Page Enable
- 0 Disable..... default
- 1 Enable

1 DIMM Type
- 0 Unbuffered ..... default
- 1 Registered

0 Multiple Page Mode
- 0 Disable..... default
- 1 Enable

Device 0 Offset 6A - Refresh Counter (00h) .....RW

7-0 Refresh Counter (in units of 16 DRAM clocks)

00 DRAM Refresh Disabled.....default
01 32 DRAM clocks
02 48 DRAM clocks
03 64 DRAM clocks
04 80 DRAM clocks
05 96 DRAM clocks
… …

The programmed value is the desired number of 16-DRAM clock units minus one.

Device 0 Offset 6B - DRAM Arbitration Control (10h).RW

7 Fast Read to Write Turn-around

0 Disable .....default
1 Enable

6 Page Kept Active When Cross Bank

0 Disable .....default
1 Enable

5 Burst Refresh

0 Disable .....default
1 Enable

4 Reserved (Do Not Program)..... default = 1

3 HA14 / HA22 Swap

0 Normal .....default
1 Swap to improve performance

2-0 SDRAM Operation Mode Select

000 Normal SDRAM Mode.....default
001 NOP Command Enable
010 All-Banks-Precharge Command Enable (CPU-to-DRAM cycles are converted to All-Banks-Precharge commands).
011 MSR Enable
CPU-to-DRAM cycles are converted to commands and the commands are driven on MA[14:0]. The BIOS selects an appropriate host address for each row of memory such that the right commands are generated on MA[14:0].
100 CBR Cycle Enable (if this code is selected, CAS-before-RAS refresh is used; if it is not selected, RAS-Only refresh is used)
101 Reserved
11x Reserved

Device 0 Offset 6C – DRAM Clock Control (00h) ..... RW

7-6 Early Clock Select for CS, CKE

00 Latest ..... default
01
10
11 Earliest

5-4 Early Clock Select for SCMD, MA

00 Latest ..... default
01
10
11 Earliest

3-0 Reserved .....always reads 0

Note: Refer to the VT8754 BIOS Porting Guide for SDRAM configuration algorithms and recommended settings for these bits for typical memory system configurations.

Device 0 Offset 6E - ECC Control (00h) .....RW

7 ECC / EC Mode Select
- 0 ECC Checking and Reporting.....default
- 1 ECC Checking, Reporting, and Correcting

6 Reserved ..... always reads 0

5 Enable SERR# on ECC / EC Multi-Bit Error
- 0 Don't assert SERR# for multi-bit errors .....def
- 1 Assert SERR# for multi-bit errors

4 Enable SERR# on ECC / EC Single-Bit Error
- 0 Don't assert SERR# for single-bit errors .....def
- 1 Assert SERR# for single-bit errors

3 ECC / EC Enable - Bank 7/6 (DIMM 3)
- 0 Disable (no ECC or EC for banks 7/6)...default
- 1 Enable (ECC or EC per bit-7)

2 ECC / EC Enable - Bank 5/4 (DIMM 2)
- 0 Disable (no ECC or EC for banks 5/4)...default
- 1 Enable (ECC or EC per bit-7)

1 ECC / EC Enable - Bank 3/2 (DIMM 1)
- 0 Disable (no ECC or EC for banks 3/2)...default
- 1 Enable (ECC or EC per bit-7)

0 ECC / EC Enable - Bank 1/0 (DIMM 0)
- 0 Disable (no ECC or EC for banks 1/0)...default
- 1 Enable (ECC or EC per bit-7)

Error checking / correction may be enabled bank-pair by bank-pair (DIMM by DIMM) by using bits 0-3 above. Bank pairs must be populated with 72-bit memory to enable for EC or ECC since the additional data bits must be present in either case. For this reason, if 64-bit memory is populated in a particular bank pair, the corresponding bit 0-3 should be set to 0 to disable both EC and ECC for that bank pair. For those bank pairs that have 72-bit memory available (and have the corresponding bit 0-3 set), either EC or ECC may be selected via bit-7 above (i.e., all enabled bank pairs will use EC or all will use ECC).

If error checking / reporting only (EC) is selected, all read and write cycles will use normal timing. Partial writes (with EC or ECC enabled) will use read-modify-write cycles to maintain correct error correction codes in the additional 8 data bits. If EC and ECC are disabled for a particular bank pair, partial writes to that bank pair will use the byte enables to write only the selected bytes (using normal write cycles and cycle timing). If error correction (ECC) is selected, the first read of a transaction will always have one additional cycle of latency.

Bit-7	Bits 3-0	RMW	Error Checking	Error Correction
0/1	0	No	No	No
0	1	Yes	Yes	No
1	1	Yes	Yes	Yes

Device 0 Offset 6F - ECC Status (00h).....RWC

7 Multi-bit Error Detected ..... write of '1' resets

6-4 Multi-bit Error DRAM Bank..... default=0
Encoded value of the bank with the multi-bit error.

3 Single-bit Error Detected ..... write of '1' resets

2-0 Single-bit Error DRAM Bank ..... default=0
Encoded value of the bank with the single-bit error.

(see RxD0-4 for ECC Error Address and Error Syndrome)

Table 8. DIMM Module Configuration

Rx6E [3-0] ECC Ena	Rx55 [3] No DQM	DIMM Module Configuration	MECC [7-0] Pins	DQM [8-0] Pins	DQS# [8-0] Pins
1	**1**	**DDR x8 with ECC**	**MECC[7-0]**	**CKE[7-0]**	**DQS[8-0]#**
0	**0**	**DDR x8 no ECC**	**CKE[7-0]**	**DQM[7-0]**	**DQS[7-0]#**

PCI Bus Control

These registers are normally programmed once at system initialization time.

Device 0 Offset 70 - PCI Buffer Control (00h).....RW

- **7 CPU to PCI Post-Write**
  - 0 Disable .....default
  - 1 Enable
- **6 Reserved** ..... always reads 0
- **5-4 PCI Master to DRAM Prefetch**
  - 00 Always prefetch .....default
  - x1 Never prefetch
  - 10 Prefetch only for Enhance command
- **3 Reserved** ..... always reads 0
- **2 PCI Master Read Buffering**
  - 0 Disable .....default
  - 1 Enable
- **1 Delay Transaction**
  - 0 Disable .....default
  - 1 Enable
- **0 Reserved** ..... always reads 0

Device 0 Offset 71 - CPU to PCI Flow Control (48h).. RWC

- **7 Retry Status.....RWC**
  - 0 No retry occurred .....default
  - 1 Retry occurred
- **6 Retry Timeout Action**
  - 0 Retry forever (record status only)
  - 1 Flush buffer or return FFFFFFFFh for reads .....default
- **5-4 Retry Count and Retry Backoff**
  - 00 Retry 2 times, backoff CPU .....default
  - 01 Retry 16 times
  - 10 Retry 4 times
  - 11 Retry 64 times
- **3 PCI Burst**
  - 0 Disable
  - 1 Enable .....default
- **2 Reserved** ..... always reads 0
- **1 Compatible Type#1 Configuration Cycles**
  - 0 Disable (fixed AD31).....default
  - 1 Enable
- **0 IDSEL Control**
  - 0 AD11, AD12 .....default
  - 1 AD30, AD31

Device 0 Offset 73 - PCI Master Control (00h)..... RW

- **7 Reserved** .....always reads 0
- **6 PCI Master 1-Wait-State Write**
  - 0 Zero wait state TRDY# response..... default
  - 1 One wait state TRDY# response
- **5 PCI Master 1-Wait-State Read**
  - 0 Zero wait state TRDY# response..... default
  - 1 One wait state TRDY# response
- **4 WSC#**
  - 0 Disable..... default
  - 1 Enable
- **3-1 Reserved** .....always reads 0
- **0 PCI Master Broken Timer Enable**
  - 0 Disable..... default
  - 1 Enable. Force into arbitration when there is no FRAME# 16 PCICLK's after the grant.

Device 0 Offset 75 - PCI Arbitration 1 (00h) .....RW

7 Arbitration Mode
- 0 REQ-based (arbitrate at end of REQ#) ..default
- 1 Frame-based (arbitrate at FRAME# assertion)

6-4 Latency Timer.....read only, reads Rx0D bits 2:0

3 Reserved ..... always reads 0

2-0 PCI Master Bus Time-Out

(force into arbitration after a period of time)
- 000 Disable .....default
- 001 1x16 PCICLKs
- 010 2x16 PCICLKs
- 011 3x16 PCICLKs
- 100 4x16 PCICLKs
- ... ...
- 111 7x16 PCICLKs

Device 0 Offset 76 - PCI Arbitration 2 (00h)..... RW

7 I/O Port 22 Access
- 0 CPU access to I/O address 22h is passed on to the PCI bus ..... default
- 1 CPU access to I/O address 22h is processed internally

6 Reserved .....always reads 0

5-4 Master Priority Rotation Control
- 00 Disable..... default
- 01 Grant to CPU after every PCI master grant
- 10 Grant to CPU after every 2 PCI master grants
- 11 Grant to CPU after every 3 PCI master grants

Setting 01: the CPU will always be granted access after the current bus master completes, no matter how many PCI masters are requesting.

Setting 10: if other PCI masters are requesting during the current PCI master grant, the highest priority master will get the bus after the current master completes, but the CPU will be guaranteed to get the bus after that master completes.

Setting 11: if other PCI masters are requesting, the highest priority will get the bus next, then the next highest priority will get the bus, then the CPU will get the bus.

In other words, with the above settings, even if multiple PCI masters are continuously requesting the bus, the CPU is guaranteed to get access after every master grant (01), after every other master grant (10) or after every third master grant (11).

3-2 Select REQn# to REQ4# mapping
- 00 REQ4#..... default
- 01 REQ0#
- 10 REQ1#
- 11 REQ2#

1 Reserved .....always reads 0

0 REQ4# is High Priority Master
- 0 Disable..... default
- 1 Enable

GART / Graphics Aperture

The function of the Graphics Address Relocation Table (GART) is to translate virtual 32-bit addresses issued by an AGP device into 4K-page based physical addresses for system memory access. In this translation, the upper 20 bits (A31-A12) are remapped, while the lower 12 address bits (A11-A0) are used unchanged.

A one-level fully associative lookup scheme is used to implement the address translation. In this scheme, the upper 20 bits of the virtual address are used to point to an entry in a page table located in system memory. Each page table entry contains the upper 20 bits of a physical address (a "physical page" address). For simplicity, each page table entry is 4 bytes. The total size of the page table depends on the GART range (called the "aperture size") which is programmable in the VT8377.

This scheme is shown in the figure below.

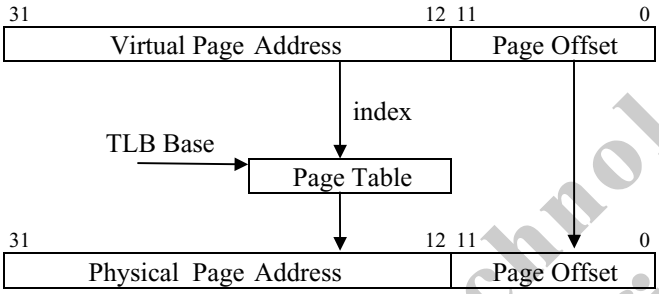


Figure 3. Graphics Aperture Address Translation

Since address translation using the above scheme requires an access to system memory, an on-chip cache (called a "Translation Lookaside Buffer" or TLB) is utilized to enhance performance. The TLB in the VT8377 contains 16 entries. Address "misses" in the TLB require an access of system memory to retrieve translation data. Entries in the TLB are replaced using an LRU (Least Recently Used) algorithm.

Addresses are translated only for accesses within the "Graphics Aperture" (GA). The Graphics Aperture can be any power of two in size from 1MB to 256MB (i.e., 1MB, 2MB, 4MB, 8MB, etc) for AGP 2.0 and 4MB to 2GB for AGP 3.0. The base of the Graphics Aperture can be anywhere in the system virtual address space on an address boundary determined by the aperture size (e.g., if the aperture size is 4MB, the base must be on a 4MB address boundary). The Graphics Aperture Base is defined in register offset 10 of device 0. The Graphics Aperture Size and TLB Table Base are defined in the following register groups (Rx84 and 88 respectively for AGP 2.0 and Rx94 and 98 for AGP 3.0) along with various control bits.

AGP 2.0 Registers

AGP 2.0 registers Rx80-AB are enabled if RxFD[1] = 1 and AGP 3.0 registers Rx80-AB are enabled if RxFD[1] = 0.

Device 0 Offset 83-80 – AGP 2.0 GART/TLB Control...RW

31-16 Reserved ..... always reads 0
15-8 Reserved (test mode status)..... RO
7 Flush Page TLB
0 Disable .....default
1 Enable
6-0 Reserved (always program to 0)..... RW

Note: For any master access to the Graphics Aperture range, snoop will not be performed.

Device 0 Offset 84 – AGP 2.0 Graphics Aperture Size ..RW

7-0 Graphics Aperture Size
11111111 1M
11111110 2M
11111100 4M
11111000 8M
11110000 16M
11100000 32M
11000000 64M
10000000 128M
00000000 256M

CPU-to-Memory Access Control

Offset 85 – AGP 2.0 CPU-to-Mem Write Policy. RO / RW†

7-4 Write Request Limit ..... default = 0
3-0 Write Request Base..... default = 0

When the number of outstanding write requests is eqaul to the "limit", the P4X400 will put a priority on decreasing write requests until the number pending is equal to the "base".

Offset 86 – CPU-to-Memory Bandwidth Timer.. RO / RW†

7-4 Host Bandwidth Timer ..... default = 0
3-0 DRAM Bandwidth Timer..... default = 0

Offset 87 – CPU-to-Memory Bandwidth Limit... RO / RW†

7-3 Reserved ..... always reads 0
2-1 Bandwidth Limit
00 Disable..... default
01 Fixed DRAM bandwidth limit
10 Fixed CPU bandwidth limit
11 Dynamically toggle between two CPU / DRAM bandwidth limits (two timers Rx86[7-4] and Rx86[3-0] are used)
0 CPU Access DRAM Read After Write
0 Normal..... default
1 Improved

Rx85, 86 and 87 should be programmed to optimum values recommended by VIA to increase system performance.

† Rx85, 86 and 87 are Write Enabled via Rx54[3]

Offset 8B-88 – AGP 2.0 GART Table Base.....RW

31-12 Graphics Aperture Translation Table Base. Pointer to the base of the translation table in system memory used to map addresses in the aperture range (the pointer to the base of the "Directory" table).

11-2 Reserved ..... always reads 0

1 Graphics Aperture

0 Disable .....default

1 Enable

Note: To disable the Graphics Aperture, set this bit to 0 and set all bits of the Graphics Aperture Size to 0. To enable the Graphics Aperture, set this bit to 1 and program the Graphics Aperture Size to the desired aperture size.

0 Reserved ..... always reads 0

Device 0 Offset A3-A0 - AGP 2.0 Capabilities (0020C002h) .....RO

31-24 Reserved ..... always reads 00

23-20 Major Specification Revision ... always reads 0010b
Major rev # of AGP spec that device conforms to

19-16 Minor Specification Revision ... always reads 0000b
Minor rev # of AGP spec that device conforms to

15-8 Pointer to Next Item ..... always reads C0 (last item)

7-0 AGP Capability ID
(always reads 02 to indicate it is AGP)

Device 0 Offset A7-A4 - AGP 2.0 Status (1F000201h) ....RO

31-24 Maximum AGP Requests..... always reads 1Fh
Max # of AGP requests the device can manage (32)

23-10 Reserved .....always reads 0s

9 Supports SideBand Addressing ..... **always reads 1**

8-6 Reserved .....always reads 0s

5 Addresses Above 4G Supported..... always reads 0†

4 Fast Write Supported..... always reads 0†

3 Reserved .....always reads 0s

2 4X Rate Supported ..... always reads 0†

1 2X Rate Supported ..... always reads 0†

0 1X Rate Supported ..... **always reads 1**

†Writable if RxFD[0] = 1.

Device 0 Offset AB-A8 - AGP 2.0 Command ..... RW

31-24 Request Depth (reserved for target).. always reads 0s

23-10 Reserved ..... always reads 0s

9 SideBand Addressing Enable

0 Disable..... default

1 Enable

8 AGP Enable

0 Disable..... default

1 Enable

7-6 Reserved ..... always reads 0s

5 4G Enable

0 Disable..... default

1 Enable

4 Fast Write Enable

0 Disable..... default

1 Enable

3 Reserved ..... always reads 0s

2 4X Mode Enable

0 Disable..... default

1 Enable

1 2X Mode Enable

0 Disable..... default

1 Enable

0 1X Mode Enable

0 Disable..... default

1 Enable

AGP 3.0 Registers

AGP 3.0 registers Rx80-AB are enabled if RxFD[1] = 0 and AGP 2.0 registers Rx80-AB are enabled if RxFD[1] = 1.

Device 0 Offset 83-80 - AGP 3.0 Capabilities (0030C002h) ..... RO

31-24 Reserved ..... always reads 00
23-20 Major Specification Revision ... always reads 0011b
Major rev # of AGP spec that device conforms to
19-16 Minor Specification Revision ... always reads 0000b
Minor rev # of AGP spec that device conforms to
15-8 Pointer to Next Item ..... always reads C0 (last item)
7-0 AGP Capability ID
(always reads 02 to indicate it is AGP)

Device 0 Offset 87-84 - AGP 3.0 Status (1F000201h) ..... RO

31-24 Maximum AGP Requests..... always reads 1Fh
Max # of AGP requests the device can manage (32)
23-16 Reserved ..... always reads 0s†
15-13 Optimum Async Request Size..... always reads 0s†
Suggested setting is 010b or 2^(2+4)=64 Bytes for 8QW access
12-10 Calibration Cycle Setting
000 4 ms
001 16 ms
010 64 ms ..... **default†**
011 256 ms
9 Supports SideBand Addressing ..... **always reads 1**
8 Reserved ..... always reads 0†
7 64-Bit GART Entries ..... always reads 0
6 CPU GART Translation Supported. always reads 0
5 Addresses Above 4G Supported ..... always reads 0
4 Fast Write Supported..... always reads 0
3 AGP 8x Detected..... Set from AGP8XDT# pin
2 4X Rate Supported ..... Reads 0 if bit-3 = 1
..... Reads 1 if bit-3 = 0
1 2X Rate Supported ..... **always reads 1**
0 1X Rate Supported ..... **always reads 1**

†Writable if RxFD[0] = 1.

Device 0 Offset 8B-88 - AGP 3.0 Command ..... RW

31-24 Request Depth (reserved for target).. always reads 0s
23-13 Reserved ..... always reads 0s
12-10 Calibration Cycle Select ..... default = 0
9 SideBand Addressing
0 Disable..... default
1 Enable
8 AGP
0 Disable..... default
1 Enable
7-6 Reserved ..... always reads 0s
5 Addresses Over 4G
0 Disable..... default
1 Enable
4 Fast Write
0 Disable..... default
1 Enable
3 Reserved ..... always reads 0s
2-0 Transfer Mode Select..... default = 000b
Rx84[3] = 0 (8x mode **not detected** via AGP8XDT#)
001 1x data transfer rate
010 2x data transfer rate
100 4x data transfer rate
Rx84[3] = 1 (8x mode **detected** via AGP8XDT#)
000 -reserved..... default
001 4x data transfer rate
010 8x data transfer rate

Device 0 Offset 93-90 - AGP 3.0 GART / TLB Control . RW

31-10 Reserved ..... always reads 0s

9 Calibration Cycle
- 0 Disable ..... default
- 1 Enable

8 Graphics Aperture Base Register (Rx13-10) Read
- 0 Disable ..... default
- 1 Enable

7 GART TLB
- 0 Disable (TLB entries are invalidated) .... default
- 1 Enable

6-0 Reserved ..... always reads 0s

Device 0 Offset 97-94 - AGP 3.0 Graphics Aperture SizeRW

31-28 Aperture Page Size Select ..... default = 0000b
Only 4K pages are allowed

27 Reserved ..... always reads 0s

26-16 Page Size Supported..... default = 001h
If bit-n of this field is 1, indicates support of 2^(n+12) page size. Must be set to 001h (field bit-0 set) to indicate only 4K pages allowed.

15-12 Reserved ..... always reads 0s

11-0 Aperture Size ..... default = 0

111100111111	4MB
111100111110	8MB
111100111100	16MB
111100111000	32MB
111100110000	64MB
111100100000	128MB
111100000000	256MB
111000000000	512MB
110000000000	1GB
100000000000	2GB <= Max supported
000000000000	4GB <= Do not program

Device 0 Offset 9B-98 - AGP 3.0 GART Table Base..... RW

31-12 GART Base Address [31:12] ..... default = 0

11-0 Reserved ..... always reads 0s

AGP 2.0 / 3.0 Registers

Device 0 Offset AC - AGP Control (00h) ..... RW

7 AGP .....RO per strap on MAB9
- 0 Disable .....default
- 1 Enable

6 AGP Read Synchronization
- 0 Disable .....default
- 1 Enable

5 AGP Read Snoop DRAM Post-Write Buffer
- 0 Disable .....default
- 1 Enable

4 GREQ# Priority Becomes Higher When Arbiter is Parked at AGP Master
- 0 Disable .....default
- 1 Enable

3-2 Reserved .....always reads 0s

1 AGP Arbitration Parking
- 0 Disable .....default
- 1 Enable (GGNT# remains asserted until either GREQ# de-asserts or data phase ready)

0 AGP to PCI Master or CPU to PCI Turnaround Cycle
- 0 2T or 3T Timing.....default
- 1 1T Timing

Device 0 Offset AD – AGP Latency Timer (02h).....RW

7 AGP Performance Improvement
- 0 Disable .....default
- 1 Enable

6 Pipe Mode Performance Improvement
- 0 Disable .....default
- 1 Enable

5 AGP Data Input Enable (for Power Saving)
- 0 AGP data input always enabled .....default
- 1 AGP data input only enabled when necessary to avoid redundant transitions

4 AGP Performance Improvement
- 0 Disable .....default
- 1 Enable

3-0 AGP Data Phase Latency Timer ..... default = 02h

Device 0 Offset AE – AGP Misc Control (00h) ..... RW

7-3 Reserved .....always reads 0

2 AGP Performance Improvement
- 0 Disable..... default
- 1 Enable

1 DBI / PIPE Mux Function
- 0 From DBIH (0.95)..... default
- 1 From PIPE (0.9)

0 CPU GART Read, AGP GART Write Coherency
- 0 Disable..... default
- 1 Enable

Device 0 Offset AF – AGP 3.0 Control (00h)..... RW

7 CPU / PCI Master GART Access
- 0 Disable..... default
- 1 Enable

6 AGP Calibration
- 0 Disable..... default
- 1 Enable

5 Mix Coherent / Non-coherent Accesses
- 0 Disable..... default
- 1 Enable

4 Reserved .....always reads 0

3 DBI Function
- 0 Disable (DBI input masked and all outputs assume DBI=0)..... default
- 1 Enable

2 DBI Output for AGP Transactions
- 0 Disable..... default
- 1 Enable

1 DBI Output for Frame Transactions Including Fast-Write
- 0 Disable..... default
- 1 Enable

0 DBI Output from Frame Transactions
- 0 Disable..... default
- 1 Enable

Device 0 Offset B0 – AGP Pad Control / Status (8xh) ...RW

7 AGP 4x Strobe VREF Control
- 0 STB VREF is STB# and vice versa
- 1 STB VREF is AGPREF **.....default**

6 AGP 4x Strobe & GD Pad Drive Strength
- 0 Drive strength set to compensation circuit default .....default
- 1 Drive strength controlled by RxB1[7-0]

5-3 AGP Compensation Circuit N Control Output. RO

2-0 AGP Compensation Circuit P Control Output . RO

Note: N = low drive, P = high drive

Device 0 Offset B1 – AGP Drive Strength (63h).....RW

7-4 AGP Output Buffer Low Drive Strength..... def=6

3-0 AGP Output Buffer High Drive Strength..... def=3

Device 0 Offset B2 – AGP Pad Drive / Delay (08h)..... RW

7 GD/GBE/GDS, SBA/SBS Control
- 0 SBA/SBS = no cap ..... default
  GD/GBE/GDS = no cap
- 1 SBA/SBS = **cap**
  GD/GBE/GDS = **cap**

6-5 GD / GBE Receive Strobe Delay
- 00 None ..... default
- 01 Delay by 1.5 ns
- 10 Delay by 3.0 ns
- 11 Delay by 4.5 ns

4 GD[31-16] Staggered Delay
- 0 None ..... default
- 1 GD[31:16] delayed by 1 ns

3 AGP Slew Rate Control
- 0 Disable
- 1 Enable**..... default**

2 SBA Receive Strobe Delay
- 0 None ..... default
- 1 Delay by 1.5 ns

1-0 GDS Output Delay
- 00 None ..... default
- 01 Delay by 1.5 ns
- 10 Delay by 3.0 ns
- 11 Delay by 4.5 ns

(GDS1 & GDS1# will be delayed an additional 1ns if bit-4 = 1)

Device 0 Offset B3 – AGP Strobe Drive Strength..... RW

7-4 AGP Strobe Output Low Drive Strength..... def=0

3-0 AGP Strobe Output High Drive Strength ..... def=0

V-Link Compensation / Drive Control

VT8235 South Bridge:

Device 0 Offset B4 – V-Link NB Compensation Ctrl (00h)RW

- **7-5 V-Link Autocomp Output Value – High Drive**. RO
- **4 Reserved** ..... always reads 0
- **3-1 V-Link Autocomp Output Value – Low Drive**.. RO
- **0 Compensation Select**
  - 0 Auto Comp (use values in bits 7-5, 3-1) default
  - 1 Manual Comp (use values in RxB5, B6)

Device 0 Offset B5 – V-Link NB Strobe Drive Ctrl (00h)RW

- **7-5 V-Link Strobe Pullup Manual Setting (High)**
- **4 Reserved** ..... always reads 0
- **3-1 V-Link Strobe Pulldown Manual Setting (Low)**
- **0 Reserved** ..... always reads 0

Device 0 Offset B6 – V-Link NB Data Drive Ctrl (00h).RW

- **7-5 V-Link Data Pullup Manual Setting (High)**
- **4 Reserved** ..... always reads 0
- **3-1 V-Link Data Pulldown Manual Setting (Low)**
- **0 Reserved** ..... always reads 0

VT8233 South Bridge (VT8233, 8233C, 8233A):

Device 0 Offset B5 – V-Link NB Drive Control (00h)....RW

- **7-6 NB V-Link Strobe Pullup Manual Setting**
- **5-4 NB V-Link Strobe Pulldown Manual Setting**
- **3-1 Reserved** ..... always reads 0
- **0 NB V-Link Slew Rate Control**
  - 0 Disable .....default
  - 1 Enable

VT8235 South Bridge:

Device 0 Offset B8 – V-Link SB Compensation Ctrl (00h)RW

- **7-5 V-Link Autocomp Output Value – High Drive** .RO
- **4 Reserved** .....always reads 0
- **3-1 V-Link Autocomp Output Value – Low Drive** ..RO
- **0 Compensation Select**
  - 0 Auto Comp (use values in bits 7-5, 3-1) default
  - 1 Manual Comp (use values in RxB9, BA)

Device 0 Offset B9 – V-Link SB Strobe Drive Ctrl (00h)RW

- **7-5 V-Link Strobe Pullup Manual Setting (High)**
- **4 Reserved** .....always reads 0
- **3-1 V-Link Strobe Pulldown Manual Setting (Low)**
- **0 Reserved** .....always reads 0

Device 0 Offset BA – V-Link SB Data Drive Ctrl (00h) RW

- **7-5 V-Link Data Pullup Manual Setting (High)**
- **4 Reserved** .....always reads 0
- **3-1 V-Link Data Pulldown Manual Setting (Low)**
- **0 Reserved** .....always reads 0

VT8233 South Bridge (VT8233, 8233C, 8233A):

Device 0 Offset B8 – V-Link SB Compensation Ctrl (00h)RW

- **7-6 V-Link Autocomp Output Value** .....always reads 0
- **5 Pullup Compensation Selection**
  - 0 Auto Comp (use values in bits 7-6)..... default
  - 1 Manual Comp (use values in bits 3-2)
- **4 Pulldown Compensation Selection**
  - 0 Auto Comp (use values in bits 7-6)..... default
  - 1 Manual Comp (use values in bits 1-0)
- **3-2 Pullup Compensation Manual Setting**.....def = 0
- **1-0 Pulldown Compensation Manual Setting**.....def = 0

Device 0 Offset B9 – V-Link SB Drive Control (00h).... RW

- **7-6 SB V-Link Strobe Pullup Manual Setting**
- **5-4 SB V-Link Strobe Pulldown Manual Setting**
- **3-1 Reserved** .....always reads 0
- **0 SB V-Link Slew Rate Control**
  - 0 Disable..... default
  - 1 Enable

Power Management Control

Device 0 Offset BC – Power Management Mode (00h)..RW

7 Dynamic Power Management
- 0 Disable .....default
- 1 Enable

6 Halt / Shutdown Power Management
- 0 Disable .....default
- 1 Enable

5 Stop Clock Power Management
- 0 Disable .....default
- 1 Enable

4 Suspend Status Power Management
- 0 Disable .....default
- 1 Enable

3-0 Reserved ..... always reads 0

Device 0 Offset BD – DRAM Power Management (00h)RW

7 DRAM Self-Refresh in PM Mode
- 0 Disable .....default
- 1 Enable

6 Dynamic CKE when DRAM Idle
- 0 Disable .....default
- 1 Enable

5 Dynamic DRAM I/O Pad Power Down (Float)
- 0 Disable .....default
- 1 Enable

4-0 Reserved ..... always reads 0

Device 0 Offset BE – Dynamic Clock Stop Control (00h)RW

7 Host Interface Power Management
- 0 Disable..... default
- 1 Enable

6 DRAM Interface Power Management
- 0 Disable..... default
- 1 Enable

5 V-Link Interface Power Management
- 0 Disable..... default
- 1 Enable

4 AGP Interface Power Management
- 0 Disable..... default
- 1 Enable

3 PCI #2 Interface Power Management
- 0 Disable..... default
- 1 Enable

2 Graphics Interface Power Management
- 0 Disable..... default
- 1 Enable

1 Reserved .....always reads 0

0 Host Fast Power Management (DADS Fast Timing)
- 0 Disable..... default
- 1 Enable

Device 0 Offset BF – DRAM Pad Toggle Reduction (00h)RW

7 MA / SCMD Pin Toggle Reduction
- 0 Disable..... default
- 1 Enable (MA and S command pins won't toggle if not accessed)

6-4 Reserved .....always reads 0

3 DIMM #3 MAA / MAB Select
- 0 MAA ..... default
- 1 MAB

2 DIMM #2 MAA / MAB Select
- 0 MAA ..... default
- 1 MAB

1 DIMM #1 MAA / MAB Select
- 0 MAA ..... default
- 1 MAB

0 DIMM #0 MAA / MAB Select
- 0 MAA ..... default
- 1 MAB

Extended Power Management Control

Device 0 Offset C0 – Power Management Capability ID RO

7-0 Capability ID..... always reads 01h

Device 0 Offset C1 – Power Management Next Pointer . RO

7-0 Next Pointer.....always reads 00h (“Null” Pointer)

Device 0 Offset C2 – Power Mgmt Capabilities I ..... RO

7-0 Power Management Capabilities.. always reads 02h

Device 0 Offset C3 – Power Mgmt Capabilities II ..... RO

7-0 Power Management Capabilities.. always reads 00h

Device 0 Offset C4 – Power Mgmt Control / Status ..... RW

7-2 Reserved ..... always reads 0

1-0 Power State

00 D0 .....default
01 -reserved-
10 -reserved-
11 D3 Hot

Device 0 Offset C5 – Power Management Status ..... RO

7-0 Power Management Status ..... always reads 00h

Device 0 Offset C6 – PCI-to-PCI Bridge Support Ext. ... RO

7-0 P2P Bridge Support Extensions.... always reads 00h

Device 0 Offset C7 – Power Management Data..... RO

7-0 Power Management Data..... always reads 00h

Error Control

Device 0 Offset D3-D0 – DRAM ECC Error Address.... RO

Device 0 Offset D4 – DRAM ECC Error Syndrome ..... RO

Device 0 Offset D5 – Host CPU Parity Status ..... WC

7 Host CPU Address Parity Error Detected ..... WC
0 No Address Parity Error Detected..... default
1 Addr Parity Error Detected (write 1 to clear)

6 Host CPU Data Parity Error Detected ..... WC
0 No Data Parity Error Detected ..... default
1 Data Parity Error Detected (write 1 to clear)

5 AGP Access Above 4G Detected ..... WC
0 No Access Detected..... default
1 Access Detected (write 1 to clear)

4 Host CPU Lock Cycle to PCI Detected ..... WC
0 No Lock Cycle Detected ..... default
1 Lock Cycle Detected (write 1 to clear)

3-0 Reserved .....always reads 0

Device 0 Offset D6 – Host CPU Parity Enable..... RW

7 Host CPU Address Parity Generation and Checking (AP[1:0]#)
0 Disable..... default
1 Enable

6 Host CPU Data Parity Generation and Checking (DP[3:0]#)
0 Disable..... default
1 Enable

5 Host CPU Response Parity Generation (RSP#)
0 Disable..... default
1 Enable

4 Parity Error Generates SERR# / NMI
0 Disable..... default
1 Enable (either SERR# or NMI generated depending on Rx47[7-6])

3 Parity Test Mode
0 Normal Parity Bit ..... default
1 Invert Parity Bit for Generation and Checking

2-0 Reserved .....always reads 0

Host CPU AGTL+ I/O Control

Device 0 Offset D8 – Host Address (2x) Pullup Drive....RW

- **7 Reserved** ..... always reads 0
- **6-4 Strobe Pullup Drive (HAS#)** ..... default = 0
- **3 Reserved** ..... always reads 0
- **2-0 Address Pullup Drive (HA,HREQ#)** ..... default = 0

Device 0 Offset D9 – Host Address (2x) Pulldown DriveRW

- **7 Reserved** ..... always reads 0
- **6-4 Strobe Pulldown Drive (HAS#)** ..... default = 0
- **3 Reserved** ..... always reads 0
- **2-0 Address Pulldown Drive (HA,HREQ#)** . default = 0

Device 0 Offset DA – Host Data (4x) Pullup Drive.....RW

- **7 Reserved** ..... always reads 0
- **6-4 Strobe Pullup Drive (HDS,HDS#)** ..... default = 0
- **3 Reserved** ..... always reads 0
- **2-0 Data Pullup Drive (HD,HDBI#)** ..... default = 0

Device 0 Offset DB – Host Data (4x) Pulldown Drive....RW

- **7 Reserved** ..... always reads 0
- **6-4 Strobe Pulldown Drive (HDS,HDS#)** ..... default = 0
- **3 Reserved** ..... always reads 0
- **2-0 Data Pulldown Drive (HD,HDBI#)**..... default = 0

Note: Refer to the VT8754 BIOS Porting Guide for recommended settings for these bits for typical system configurations.

Device 0 Offset DC – Output Delay / Stagger Control...RW

- **7-6 Data / Strobe Relative Delay**
  - 00 Data delay = strobe delay + 150 psec.....default
  - 01 Data delay = strobe delay
  - 10 Data delay = strobe delay – 150 psec
  - 11 Data delay = strobe delay – 300 psec
- **5 HD[63:48, 31:16], HDBI[3,1]# Output Stagger**
  - 0 No delay.....default
  - 1 1 nsec delay
- **4 HA[31:17] Output Stagger**
  - 0 No delay.....default
  - 1 1 nsec delay
- **3-2 HDS / HDS# Output Extra Delay**
  - 00 No delay.....default
  - 01 150 psec delay
  - 10 300 psec delay
  - 11 450 psec delay
- **1-0 HAS # Output Extra Delay**
  - 00 No delay.....default
  - 01 150 psec delay
  - 10 300 psec delay
  - 11 450 psec delay

Device 0 Offset DD – AGTL+ I/O Control (00h) ..... RW

- **7 AGTL+ 4x Input Increase Delay to Filter Noise**
  - 0 Disable..... default
  - 1 Enable
- **6 AGTL+ 2x Input Increase Delay to Filter Noise**
  - 0 Disable..... default
  - 1 Enable
- **5 AGTL+ Slew Rate Control**
  - 0 Disable..... default
  - 1 Enable
- **4 Reserved** .....always reads 0
- **3 Input Pullup**
  - 0 Disable..... default
  - 1 Enable
- **2 AGTL+ Strobe Internal Termination Pullups**
  - 0 Disable..... default
  - 1 Enable
- **1 AGTL+ Data Internal Termination Pullups**
  - 0 Disable..... default
  - 1 Enable
- **0 AGTL+ Dynamic Compensation**
  - 0 Disable..... default
  - 1 Enable

Device 0 Offset DE – AGTL+ Comp Status (00h) ..... RW

- **7 Select AutoCompensation Drive**
  - 0 Disable..... default
  - 1 Enable (RxD8-DB set automatically on-chip based on auto compensation results)
- **6-4 AGTL+ Compensation Result** .....default = 0
- **3 AGTL+ POS Function**
  - 0 Inputs always powered ..... default
  - 1 Inputs powered down when not in input mode
- **2 DBI Double Check**
  - 0 Disable..... default
  - 1 Enable (bit-1 must also be 1)
- **1 DBI (Dynamic Bus Inversion) Function**
  - 0 Enable..... default
  - 1 Disable (DBI always high)
- **0 Reserved** .....always reads 0

Device 0 Offset DF – AGTL+ Auto Comp Offset (00h). RW

- **7-4 AGTL+ Drive Offset to Comp Result for 2x Pad** .....default = 0
- **3-0 AGTL+ Drive Offset to Comp Result for 4x Pad** .....default = 0

DRAM Above 4G Control

Device 0 Offset E4 – Low Top Address Low (00h).....RW

7-4 Low Top Address Low ..... default = 0

3-0 DRAM Granularity

0	16M	Total DRAM less than 4G.....default
1	32M	Total DRAM less than 8G
2	64M	Total DRAM less than 16G
3	128M	Total DRAM less than 32G
4	256M	Total DRAM less than 64G
5-7	-reserved-	

Device 0 Offset E5 – Low Top Address High (FFh).....RW

7-0 Low Top Address High .....default = FFh

Device 0 Offset E6 – SMM / APIC Decoding (01h).....RW

7-6 Reserved ..... always reads 0

5 APIC Lowest Interrupt Arbitration

0 Disable .....default

1 Enable

4 I/O APIC Decoding

0 FECxxxxx accesses go to PCI .....default

1 FEC00000 to FEC7FFFF accesses go to PCI
FEC80000 to FECFFFFF accesses go to AGP

3 MSI (Processor Message) Support

0 Disable (master access to FEExxxxx will go to PCI) .....default

1 Enable (master access to FEExxxxx will be passed to host side to do snoop)

2 Top SMM

0 Disable .....default

1 Enable

1 Reserved ..... always reads 0

0 Compatible SMM

0 Disable

1 Enable **.....default**

Device 0 Offset E8 – DQ Drive (MD,MECC,DQS,DQM)RW

7-4 High Drive

0000 Lowest ..... default
… …
1111 Highest

3-0 Low Drive

0000 Lowest ..... default
… …
1111 Highest

Device 0 Offset E9 – CS Drive (CS, CKE)..... RW

7-4 High Drive

0000 Lowest ..... default
… …
1111 Highest

3-0 Low Drive

0000 Lowest ..... default
… …
1111 Highest

Device 0 Offset EA – MAA Drive (MAA, ScmdA) ..... RW

7-4 High Drive

0000 Lowest ..... default
… …
1111 Highest

3-0 Low Drive

0000 Lowest ..... default
… …
1111 Highest

Device 0 Offset EB – MAB Drive (MAB, ScmdB) ..... RW

7-4 High Drive

0000 Lowest ..... default
… …
1111 Highest

3-0 Low Drive

0000 Lowest ..... default
… …
1111 Highest

Host CPU P6 Interface DRDY Timing Control

Device 0 Offset EE – DRDY Timing Control 1 (00h)..... RW

7-6 Phase 4 Wait States..... default = 00b
5-4 Phase 3 Wait States..... default = 00b
3-2 Phase 2 Wait States..... default = 00b
1-0 Phase 1 Wait States..... default = 00b

Device 0 Offset EF – DRDY Timing Control 2 (00h)..... RW

7 Burst DRDY Wait States
0 0 ws DRDY Burst .....default
1 1 ws DRDY Burst
6-2 Reserved ..... always reads 0
1-0 Phase 5 Wait States..... default = 00b

BIOS Scratch

Device 0 Offset F3-F4 – BIOS Scratch Registers..... RW

7-0 No hardware function..... default = 0

Miscellaneous Registers

Device 0 Offset FD – AGP 2.0 / 3.0 Select..... RW

7-3 Reserved .....always reads 0
2 AGP Capability Pointer (Rx34) Value
0 Rx34 = A0h (AGP 2.0)..... default
1 Rx34 = 80h (AGP 3.0)
1 Compatible Rx80-AF
0 AGP 3.0 registers at Rx80-B3 ..... default
1 AGP 2.0 registers at Rx80-B3
0 AGP Status Register Write
0 Disable (AGP 3.0 Rx84 is RO) ..... default
1 Enable (AGP 3.0 Rx84 is RW)

Device 1 Register Descriptions

Device 1 PCI-to-PCI Bridge Header Registers

All registers are located in PCI configuration space. They should be programmed using PCI configuration mechanism 1 through CF8 / CFC with bus number of 0 and function number equal to 0 and device number equal to one.

Device 1 Offset 1-0 - Vendor ID (1106h) ..... RO

15-0 ID Code (reads 1106h to identify VIA Technologies)

Device 1 Offset 3-2 - Device ID (B168h) ..... RO

15-0 ID Code (reads B168h to identify the P4X400 PCI-to-PCI Bridge device)

Device 1 Offset 5-4 – Command (0007h) ..... RW

15-10 Reserved ..... always reads 0

9 Fast Back-to-Back Cycle Enable ..... RO
- 0 Fast back-to-back transactions only allowed to the same agent ..... default
- 1 Fast back-to-back transactions allowed to different agents

8 SERR# Enable ..... RO
- 0 SERR# driver disabled ..... default
- 1 SERR# driver enabled

(SERR# is used to report ECC errors).

7 Address / Data Stepping ..... RO
- 0 Device never does stepping ..... default
- 1 Device always does stepping

6 Parity Error Response ..... RW
- 0 Ignore parity errors & continue ..... default
- 1 Take normal action on detected parity errors

5 Reserved ..... always reads 0

4 Memory Write and Invalidate Command ..... RO
- 0 Bus masters must use Mem Write ..... default
- 1 Bus masters may generate Mem Write & Inval

3 Special Cycle Monitoring ..... RO
- 0 Does not monitor special cycles ..... default
- 1 Monitors special cycles

2 Bus Master ..... RW
- 0 Never behaves as a bus master
- 1 Enable to operate as a bus master on the primary interface on behalf of a master on the secondary interface ..... default

1 Memory Space ..... RW
- 0 Does not respond to memory space
- 1 Enable memory space access ..... default

0 I/O Space ..... RW
- 0 Does not respond to I/O space
- 1 Enable I/O space access ..... default

Device 1 Offset 7-6 - Status (Primary Bus) (0230h) .....RWC

15 Detected Parity Error ..... always reads 0

14 Signaled System Error (SERR#) ..... always reads 0

13 Signaled Master Abort
- 0 No abort received ..... default
- 1 Transaction aborted by the master with Master-Abort (except Special Cycles) ..... write 1 to clear

12 Received Target Abort
- 0 No abort received ..... default
- 1 Transaction aborted by the target with Target-Abort ..... write 1 to clear

11 Signaled Target Abort ..... always reads 0

10-9 DEVSEL# Timing
- 00 Fast
- 01 Medium ..... always reads 01
- 10 Slow
- 11 Reserved

8 Data Parity Error Detected ..... always reads 0

7 Fast Back-to-Back Capable ..... always reads 0

6 User Definable Features ..... always reads 0

5 66MHz Capable ..... always reads 1

4 Supports New Capability list ..... always reads 1

3-0 Reserved ..... always reads 0

Device 1 Offset 8 - Revision ID (00h) ..... RO

7-0 P4X400 Chip Revision Code (00=First Silicon)

Device 1 Offset 9 - Programming Interface (00h) ..... RO

This register is defined in different ways for each Base/Sub-Class Code value and is undefined for this type of device.

7-0 Interface Identifier ..... always reads 00

Device 1 Offset A - Sub Class Code (04h) ..... RO

7-0 Sub Class Code .reads 04 to indicate PCI-PCI Bridge

Device 1 Offset B - Base Class Code (06h) ..... RO

7-0 Base Class Code .. reads 06 to indicate Bridge Device

Device 1 Offset D - Latency Timer (00h) ..... RO

7-0 Reserved ..... always reads 0

Device 1 Offset E - Header Type (01h) ..... RO

7-0 Header Type Code ..... reads 01: PCI-PCI Bridge

Device 1 Offset 18 - Primary Bus Number (00h).....RW

7-0 Primary Bus Number ..... default = 0

This register is read write, but internally the chip always uses bus 0 as the primary.

Device 1 Offset 19 - Secondary Bus Number (00h) .....RW

7-0 Secondary Bus Number..... default = 0

Note: AGP must use these bits to convert Type 1 to Type 0.

Device 1 Offset 1A - Subordinate Bus Number (00h) ....RW

7-0 Primary Bus Number ..... default = 0

Note: AGP must use these bits to decide if Type 1 to Type 1 command passing is allowed.

Device 1 Offset 1B – Secondary Latency Timer (00h) ....RO

7-0 Reserved ..... always reads 0

Device 1 Offset 1C - I/O Base (F0h).....RW

7-4 I/O Base AD[15:12]..... default = 1111b

3-0 I/O Addressing Capability ..... default = 0

Device 1 Offset 1D - I/O Limit (00h).....RW

7-4 I/O Limit AD[15:12] ..... default = 0

3-0 I/O Addressing Capability ..... default = 0

Device 1 Offset 1F-1E - Secondary Status.....RO

15-0 Secondary Status

Rx44[4] = 0: these bits read back 0000h

Rx44[4] = 1: these bits read back same as Rx7-6

Device 1 Offset 21-20 - Memory Base (FFF0h).....RW

15-4 Memory Base AD[31:20].....default = FFFh

3-0 Reserved ..... always reads 0

Device 1 Offset 23-22 - Memory Limit (Inclusive) (0000h) RW

15-4 Memory Limit AD[31:20] ..... default = 0

3-0 Reserved ..... always reads 0

Device 1 Offset 25-24 - Prefetchable Mem Base (FFF0h) RW

15-4 Prefetchable Memory Base AD[31:20]default = FFFh

3-0 Reserved ..... always reads 0

Device 1 Offset 27-26 - Prefetchable Memory Limit (0000h) .....RW

15-4 Prefetchable Memory Limit AD[31:20] . default = 0

3-0 Reserved ..... always reads 0

Device 1 Offset 34 - Capability Pointer (80h) .....RO

Contains an offset from the start of configuration space.

7-0 AGP Capability List Pointer..... always reads 80h

Device 1 Offset 3F-3E – PCI-to-PCI Bridge Control (0000h) ..... RW

15-4 Reserved .....always reads 0

3 VGA-Present on AGP

0 Forward VGA accesses to PCI Bus..... default

1 Forward VGA accesses to AGP Bus

Note: VGA addresses are memory A0000-BFFFFh and I/O addresses 3B0-3BBh, 3C0-3CFh and 3D0-3DFh (10-bit decode). "Mono" text mode uses B0000-B7FFFh and "Color" Text Mode uses B8000-BFFFFh. Graphics modes use Axxxxh. Mono VGA uses I/O addresses 3Bx-3Cxh and Color VGA uses 3Cx-3Dxh. If an MDA is present, a VGA will not use the 3Bxh I/O addresses and B0000-B7FFFh memory space; if not, the VGA will use those addresses to emulate MDA modes.

2 Block / Forward ISA I/O Addresses

0 Forward all I/O accesses to the AGP bus if they are in the range defined by the I/O Base and I/O Limit registers (device 1 offset 1C-1D)

..... default

1 Do not forward I/O accesses to the AGP bus that are in the 100-3FFh address range even if they are in the range defined by the I/O Base and I/O Limit registers.

1-0 Reserved .....always reads 0

Device 1 PCI-to-PCI Bridge Device-Specific Registers

AGP Bus Control

Device 1 Offset 40 - CPU-to-AGP Flow Control 1 (00h) RW

7 CPU-AGP Post Write
- 0 Disable .....default
- 1 Enable

6 Reserved ..... always reads 0

5 CPU-AGP One Wait State Burst Write
- 0 Disable .....default
- 1 Enable

4-3 Read Prefetch Control
- 00 Always prefetch .....default
- x1 Never prefetch
- 10 Prefetch only for Enhance command

2 MDA Present on AGP
- 0 Forward MDA accesses to AGP .....default
- 1 Forward MDA accesses to PCI

Note: Forward despite IO / Memory Base / Limit

Note: MDA (Monochrome Display Adapter) addresses are memory addresses B0000h-B7FFFh and I/O addresses 3B4-3B5h, 3B8-3BAh, and 3BFh (10-bit decode). 3BC-3BE are reserved for printers.

Note: If Rx3E bit-3 is 0, this bit is a don't care (MDA accesses are forwarded to the PCI bus).

1 AGP Master Read Caching
- 0 Disable .....default
- 1 Enable

0 AGP Delay Transaction
- 0 Disable .....default
- 1 Enable

Table 9. VGA/MDA Memory/IO Redirection

3E[3] VGA Pres.	40[2] MDA Pres.	VGA is on	MDA is on	Axxxx, B8xxx Access	B0000 -B7FFF Access	3Cx, 3Dx I/O	3Bx I/O
0	-	PCI	PCI	PCI	PCI	PCI	PCI
1	0	AGP	AGP	AGP	AGP	AGP	AGP
1	1	AGP	PCI	AGP	PCI	AGP	PCI

Device 1 Offset 41 - CPU-to-AGP Flow Control 2 (08h) RW

7 Retry Status
- 0 No retry occurred..... default
- 1 Retry Occurred .....**write 1 to clear**

6 Retry Timeout Action
- 0 No action taken except to record status ..... def
- 1 Flush buffer for write or return all 1s for read

5-4 Retry Count
- 00 Retry 2, backoff CPU ..... default
- 01 Retry 4, backoff CPU
- 10 Retry 16, backoff CPU
- 11 Retry 64, backoff CPU

3 CPU-to-AGP Bursting Timeout
- 0 Disable
- 1 Enable**..... default**

2 Reserved .....always reads 0

1 CPU-to-PCI/AGP Cycles Invalidate PCI/AGP Buffered Read Data
- 0 Disable..... default
- 1 Enable

0 Reserved .....always reads 0

Device 1 Offset 42 - AGP Master Control (00h) ..... RW

7 Reserved (Must Be Programmed to 1) .....def = 0

When this bit is set, the P4X400 will automatically resolve the problem of AGP master cycles being blocked by PCI Master Cycles.

6 AGP Master One Wait State Write
- 0 Disable..... default
- 1 Enable

5 AGP Master One Wait State Read
- 0 Disable..... default
- 1 Enable

4 Break Consecutive PCI Master Accesses
- 0 Disable..... default
- 1 Enable

3 Reserved .....always reads 0

2 Claim I/O R/W and Memory Read Cycles
- 0 Disable..... default
- 1 Enable

1 Claim Local APIC FEEx xxxx Cycles
- 0 Disable..... default
- 1 Enable

0 Snoop Write Enable 2T Rate, Support Host Side Snoop Cycles at 2T Rate
- 0 Disable..... default
- 1 Enable

Device 1 Offset 43 - AGP Master Latency Timer (22h) RW

7-4 Host to AGP Time slot
- 0 Disable (no timer)
- 1 16 GCLKs
- 2 32 GCLKs.....default
- … …
- F 128 GCLKs

3-0 AGP Master Time Slot
- 0 Disable (no timer)
- 1 16 GCLKs
- 2 32 GCLKs.....default
- … …
- F 128 GCLKs

Device 1 Offset 45 – Fast Write Control (72h)..... RW

7 Force Fast Write Cycle to be QW Aligned (if Rx45[6] = 0)
- 0 Disable..... default
- 1 Enable

6 Merge Multiple CPU Transactions Into One Fast Write Burst Transaction
- 0 Disable
- 1 Enable**..... default**

5 Merge Multiple CPU Write Cycles To Memory Offset 23-20 Into Fast Write Burst Cycles (if Rx45[6] = 0)
- 0 Disable
- 1 Enable**..... default**

4 Merge Multiple CPU Write Cycles To Prefetchable Memory Offset 27-24 Into Fast Write Burst Cycles (if Rx45[6] = 0)
- 0 Disable
- 1 Enable**..... default**

3 Reserved .....always reads 0

2 Fast Write Burst 4T Max (No Slave Flow Control)
- 0 Disable..... default
- 1 Enable

1 Fast Write Fast Back to Back
- 0 Disable
- 1 Enable**..... default**

0 Fast Write Initial Block 1 Wait State
- 0 Disable..... default
- 1 Enable

Rx45 Bits 7-4	CPU Write Address in Mem1	CPU Write Address in Mem2	Fast Write Cycle Alignment
x1xx	-	-	QW aligned, burstable
0000	-	-	DW aligned, nonburstable
x010	0	0	n/a
0010	0	1	DW aligned, non-burstable
x010	1	-	QW aligned, burstable
x001	0	0	n/a
x001	-	1	QW aligned, burstable
0001	1	0	DW aligned, non-burstable
x011	0	0	n/a
x011	1	-	QW aligned, burstable
x011	0	1	QW aligned, burstable
1000	-	-	QW aligned, non-burstable
1010	0	1	QW aligned, non-burstable
1001	1	0	QW aligned, non-burstable

AGP Bus Control (continued)

Device 1 Offset 47-46 – PCI-to-PCI Bridge Device ID... RW

15-0 PCI-to-PCI Bridge Device ID ..... default = 0000

Device 1 Offset 48 – AGP / PCI2 Error Reporting ..... RW

7 AGP Cycle Data Parity Error..... WC
- 0 Parity Error did not occur.....default
- 1 Parity error occurred .....write 1 to clear

6 PCI #2 GSERR Error..... WC
- 0 Parity Error did not occur.....default
- 1 Parity error occurred .....write 1 to clear

5 Reserved ..... always reads 0

4 Generate Parity Error on AGP Data Parity Error
- 0 Disable .....default
- 1 Enable

3-2 Reserved ..... always reads 0

1 Generate Parity Error on PCI #2 Data Parity Error
- 0 Disable .....default
- 1 Enable

0 Generate Parity Error on PCI #2 Address Parity Error

Power Management

Device 1 Offset 80 – Capability ID (01h) ..... RO

7-0 Capability ID .....always reads 01h

Device 1 Offset 81 – Next Pointer (00h)..... RO

7-0 Next Pointer: Null .....always reads 00h

Device 1 Offset 82 – Power Mgmt Capabilities 1 (02h).. RO

7-0 Power Mgmt Capabilities .....always reads 02h

Device 1 Offset 83 – Power Mgmt Capabilities 2 (00h).. RO

7-0 Power Mgmt Capabilities .....always reads 00h

Device 1 Offset 84 – Power Mgmt Ctrl/Status (00h)..... RW

7-2 Reserved .....always reads 0

1-0 Power State
- 00 D0 ..... default
- 01 -reserved-
- 10 -reserved-
- 11 D3 Hot

Device 1 Offset 85 – Power Mgmt Status (00h)..... RO

7-0 Power Mgmt Status..... default = 00

Device 1 Offset 86 – P2P Br. Support Extensions (00h) . RO

7-0 P2P Bridge Support Extensions ..... default = 00

Device 1 Offset 87 – Power Management Data (00h) ..... RO

7-0 Power Management Data ..... default = 00

FUNCTIONAL DESCRIPTION

Configuration Strapping

TBD

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Table 10. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes
T_C	Case Operating Temperature	0	85	°C	1
T_S	Storage Temperature	–55	125	°C	1
V_{IN}	Input Voltage	–0.5	V_{RAIL} + 10%	Volts	1, 2
V_{OUT}	Output Voltage	–0.5	V_{RAIL} + 10%	Volts	1, 2

Note 1. Stress above the conditions listed may cause permanent damage to the device. Functional operation of this device should be restricted to the conditions described under operating conditions.

Note 2. V_{RAIL} is defined as the V_{CC} level of the respective rail. The CPU interface is 2.5V. Memory is 2.5V. AGP can be 1.5V (4x transfer mode) or 0.8V (8x transfer mode).

DC Characteristics

T_C = 0-85°C, V_{RAIL} = V_{CC} ±5%, V_{CORE} = 2.5V ±5%, GND = 0V

Table 11. DC Characteristics

Symbol	Parameter	Min	Max	Unit	Condition
V_{IL}	Input Low Voltage	–0.50	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage	-	0.55	V	I_{OL} = 4.0 mA
V_{OH}	Output High Voltage	2.4	–	V	I_{OH} = –1.0 mA
I_{IL}	Input Leakage Current	–	±10	uA	0 < V_{IN} < V_{CC}
I_{OZ}	Tristate Leakage Current	–	±20	uA	0.55 <V_{OUT} < V_{CC}

Drive strength for selected output pins is programmable. See Device 0 RxB0[6], B1, B3, B5, B6, B9, BA, D8-DB, E8-EB and straps VAD4-5 for details.

Power Characteristics

T_C = 0-85°C, V_{RAIL} = V_{CC} ± 5%, V_{CORE} = 2.5V ± 5%, GND=0V

Table 12. Power Characteristics – Internal and Interface Digital Logic

Symbol	Parameter	Typ	Max	Unit	Condition
I_{TT}	Power Supply Current – VTT			mA	Full-On Operation
I_{TTPOS}	Power Supply Current – VTT			mA	POS
I_{TTSTR}	Power Supply Current – VTT			mA	STR
I_{TTSOF}	Power Supply Current – VTT			mA	Soft-Off
I_{CCG}	Power Supply Current – VCCAGP			mA	Full-On Operation
I_{CCGPOS}	Power Supply Current – VCCAGP			mA	POS
I_{CCGSTR}	Power Supply Current – VCCAGP			mA	STR
I_{CCGSOF}	Power Supply Current – VCCAGP			mA	Soft-Off
I_{CCV}	Power Supply Current – VCCVL			mA	Full-On Operation
I_{CCVPOS}	Power Supply Current – VCCVL			mA	POS
I_{CCVSTR}	Power Supply Current – VCCVL			mA	STR
I_{CCVSOF}	Power Supply Current – VCCVL			mA	Soft-Off
I_{CCM}	Power Supply Current – VCCMEM			mA	Full-On Operation
I_{CCMPOS}	Power Supply Current – VCCMEM			mA	POS
I_{CCMSTR}	Power Supply Current – VCCMEM			mA	STR
I_{CCMSOF}	Power Supply Current – VCCMEM			mA	Soft-Off
I_{CC25}	Power Supply Current – VCC25			mA	Full-On Operation
$I_{CC25POS}$	Power Supply Current – VCC25			mA	POS
$I_{CC25STR}$	Power Supply Current – VCC25			mA	STR
$I_{CC25SOF}$	Power Supply Current – VCC25			mA	Soft-Off
I_{SUS25}	Power Supply Current – VSUS25			mA	Full-On Operation
$I_{SUS25POS}$	Power Supply Current – VSUS25			mA	POS
$I_{SUS25STR}$	Power Supply Current – VSUS25			mA	STR
$I_{SUS25SOF}$	Power Supply Current – VSUS25			mA	Soft-Off
I_{CCQQ}	Power Supply Current – VCCQQ			mA	Max operating frequency
P_D	Power Dissipation			W	Max operating frequency

Table 13. Power Characteristics – Analog and Reference Voltages

Symbol	Parameter	Typ	Max	Unit	Condition
I_{CCGTL}	Power Supply Current – GTLVREF			mA	Max operating frequency
$I_{CCHAREF}$	Power Supply Current – HAVREF			mA	Max operating frequency
$I_{CCHDREF}$	Power Supply Current – HDVREF			mA	Max operating frequency
$I_{CCHCREF}$	Power Supply Current – HCMPVREF			mA	Max operating frequency
I_{CCMREF}	Power Supply Current – MEMVREF			mA	Max operating frequency
I_{CCGREF}	Power Supply Current – AGPVREF			mA	Max operating frequency
$I_{CCVLREF}$	Power Supply Current – VLVREF			mA	Max operating frequency
I_{CCHCK}	Power Supply Current – VCCHCK			mA	Max operating frequency
I_{CCMCK}	Power Supply Current – VCCMCK			mA	Max operating frequency
I_{CCMDLL}	Power Supply Current – VCCMDLL			mA	Max operating frequency

AC Timing Specifications

AC timing specifications provided are based on external zero-pf capacitance load. Min/max cases are based on the following table:

Table 14. AC Timing Min / Max Conditions

Parameter	Min	Max	Unit
2.5V Power (Internal Logic)	2.375	2.625	Volts
1.5V Power (VCCQQ for 4x transfer mode)	1.425	1.575	Volts
0.8V Power (VCCQQ for 8x transfer mode)	0.76	0.84	Volts
Case Temperature	0	85	^{o}C

Drive strength for selected output pins is programmable and may effect AC timing specifications. See Device 0 RxB0[6], B1, B3, B5, B6, B9, BA, D8-DB, E8-EB and straps VAD4-5 for details.

MECHANICAL SPECIFICATIONS

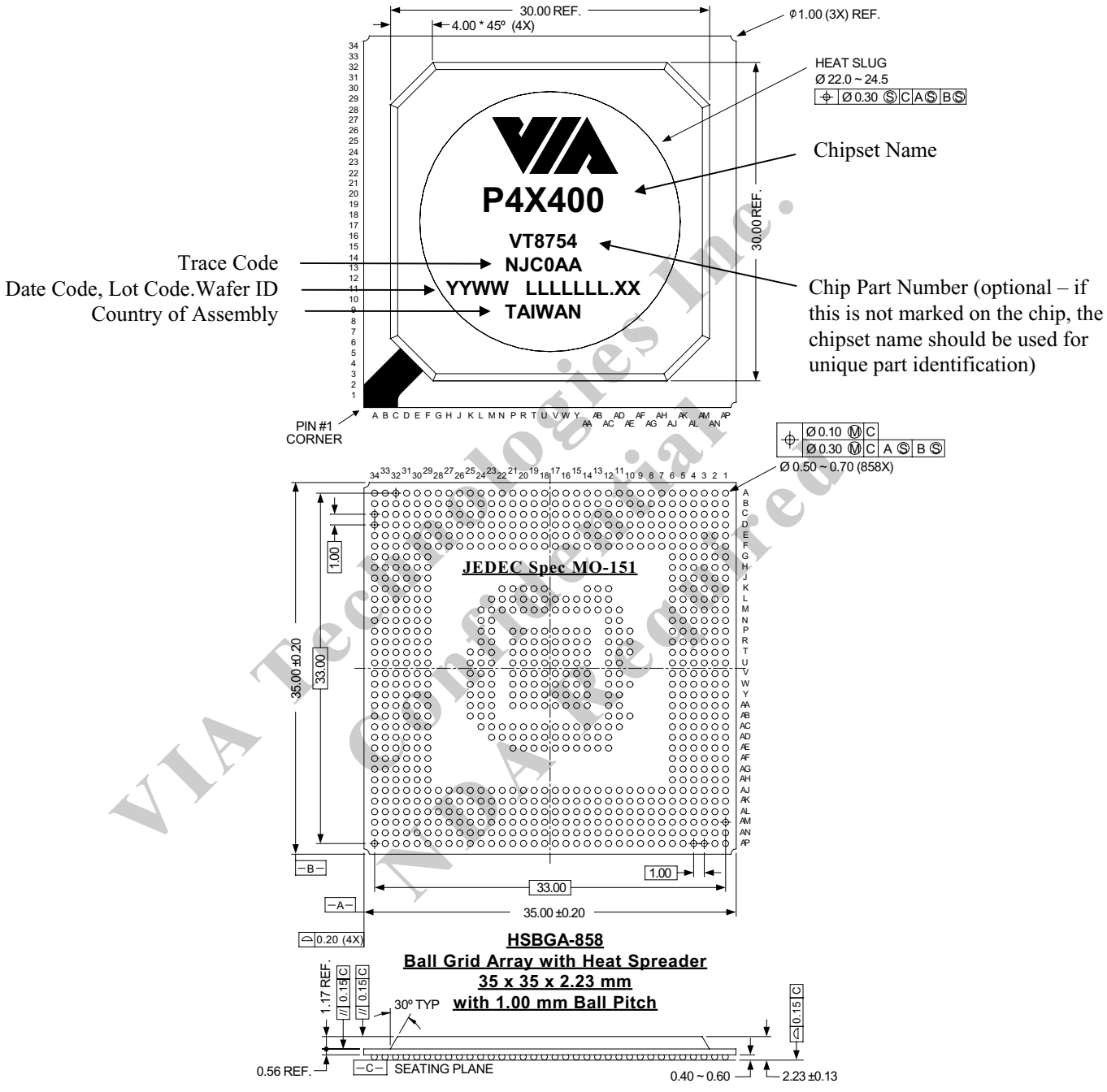


Figure 4. Mechanical Specifications – HSBGA-858 Ball Grid Array Package with Heat Spreader