Apollo KT266A Chipset

VT8366A Single-Chip North Bridge for Socket-A Based Athlon™ CPUs with 266 MHz Front Side Bus with AGP4x and V-Link plus Advanced ECC Memory Controller supporting PC133 / PC100 SDR SDRAM and PC2100 / PC1600 DDR SDRAM for Desktop & Mobile PC Systems

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REVISION HISTORY

Document Release	Date	Revision	Initials
2.0	8/31/01	Initial release based on VT8366 data sheet rev 1.61 Changed Product Number from VT8366 to VT8366A Changed Chipset Name from KT266 to KT266A Updated Device 0 Rx46[0], 4E[7], 54[5-4], 55[6], 66[6], 69[5-4], 90-91, 95[7-5], 96, 9E, AD[5]; Device 1 Rx2D-2F, 40[6], 41[3-2], 42[7,3] Updated chip marking to make Chipset Name most prominent	DH
2.1	9/14/01	Changed cover, page headers, features & overview to emphasize chipset name Updated system block diagram; Fixed miscellaneous typographical errors Added VAD6 strap and updated strap information table, pin diagram and pin lists Removed DQS pin functions from DQM pins due to removal of x4 DRAM support Fixed register summary entries for Device 0 Rx40-41, 43-44, 49, 4B-4C Updated Device 0 Rx55[6] (x4 DRAM capability removed), 67[2-0] (MD Latch Clock Select & Clock Delay), 9E[1] (new bit), 97[7-3] (CPU Clock Divide) Updated chip marking to remove chip number (to match production part marking)	DH

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with 266 MHz Front Side Bus
with AGP 4x and V-Link
plus Advanced ECC Memory Controller
supporting PC133 / PC100 SDR SDRAM
and PC2100 / PC1600 DDR SDRAM
for Desktop & Mobile PC Systems

PRODUCT FEATURES

- **High Performance and High Integration Athlon AGP 4x / DDR Chipset with Advanced System Power Management**
  - **KT266A** Chipset: **VT8366A** system controller and **VT8233** V-Link south bridge
  - Single chip Athlon system controller with 64-bit Socket-A Athlon CPU, 64-bit SDR/DDR system memory, 266 MB/sec high bandwidth V-Link NB/SB, and 32-bit AGP interfaces
  - V-Link south bridge chip includes UltraDMA-33/66/100 EIDE, 6 USB Ports, 10/100 Fast Etherlet LAN controller, AC97 / MC97 link (for Audio and Modem support), LPC, SMBus, Power Management, and Keyboard / PS2-Mouse Interfaces plus RTC / CMOS on chip
  - Supports separately powered 3.3V (5V tolerant) interface to system memory and AGP
  - Modular power management and clock control for advanced system power management
- **High Performance Athlon CPU Interface**
  - Supports Socket-A (Socket-462) AMD Athlon processors
  - HSTL-like 1.5V high-speed transceiver logic signal levels
  - Support independent address, data, and snoop interfaces
  - 100/133 MHz DDR (Double Data Rate) transfer on Athlon CPU address and data buses
  - Built-in PLL (Phase Lock Loop) circuitry for optimal skew control within and between clocking regions
  - Four-entry command queue to accommodate maximum CPU throughput
  - Four-entry probe queue to stores probes from the system to the processor
  - Twenty four-entry processor system data and control queue to store system data control commands in two separate read and write buffers for data movement in and out of processor interface
  - Supports WC (Write Combining) cycles
  - Sleep mode support
  - System management interrupt, memory remap and STPCLK mechanism

- **Full Featured Accelerated Graphics Port (AGP) Controller**
  - Synchronous and pseudo-synchronous with the host CPU bus with optimal skew control

V-Link	AGP	CPU	Mode
66 MHz	66 MHz	100 MHz DDR	Pseudo synchronous
66 MHz	66 MHz	133 MHz DDR	Synchronous

  - AGP v2.0 compliant
  - Supports SideBand Addressing (SBA) mode (non-multiplexed address / data)
  - Supports 66 MHz 1x, 2x and 4x modes for AD and SBA signaling
  - Pipelined split-transaction long-burst transfers up to 1GB/sec
  - Thirty-two level read request queue
  - Four level posted-write request queue
  - Thirty-two level (quadwords) read data FIFO (256 bytes)
  - Sixteen level (quadwords) write data FIFO (128 bytes)
  - Intelligent request reordering for maximum AGP bus utilization
  - Supports Flush/Fence commands
  - Graphics Address Relocation Table (GART)
    - One level TLB structure
    - Sixteen entry fully associative page table
    - LRU replacement scheme
  - Windows 95 OSR-2 VXD and integrated Windows 98 / Windows 2000 miniport driver support

- **High Bandwidth 266 MB/sec 8-bit V-Link Host Controller**
  - Supports 66 MHz V-Link Host interface with peak bandwidth of 266MB/S
  - V-Link operates at 2X or 4X modes
  - Full duplex commands with separate STB/CMD
  - Request/Data split transaction
  - Configurable outstanding transaction queue for Host to V-Link Client accesses
  - Supports Defer/Defer-Reply transaction
  - Transaction assurance for V-Link Host to Client access. Eliminate V-Link Host-Client Retry cycles
  - Intelligent V-Link transaction protocol to eliminate data wait-state/throttle transfer latency. All V-Link transaction both Host and Client have consistent view of transaction data depth and buffer size to avoid data overflow.
  - High efficient V-Link arbitration with minimum overhead. All V-Link transaction with predictable cycle length with known CMD/Date duration.

- **Advanced High-Performance SDR/DDR DRAM Controller**
  - DRAM interface synchronous with host CPU (100/133 MHz) for most flexible configuration
  - DRAM interface may be faster than CPU by 33 MHz to allow use of 133 MHz memory with 100 MHz FSB
  - DRAM interface may be slower than CPU by 33 MHz to allow use of 100 MHz memory with 133 MHz FSB
  - Concurrent CPU, AGP, and V-Link access
  - Supports SDR and DDR SDRAM memory types
  - Dynamic Clock Enable (CKE) control for SDRAM power reduction in high speed systems
  - Mixed 1M / 2M / 4M / 8M / 16M / 32M / 64MxN DRAMs
  - Supports 8 banks up to 4 GB DRAMs (512Mb x8/x16 DRAM technology) for registered SDR/DDR modules
  - Supports 6 banks up to 3 GB DRAMs (512Mb x8/x16 DRAM technology) for unbuffered SDR/DDR modules
  - Flexible row and column addresses. 64-bit data width only
  - LVTTL 3.3V DRAM interface with 5V-tolerant inputs for SDR SDRAM and 2.5V SSTL-2 DRAM interface for DDR SDRAM
  - Programmable I/O drive capability for MA, command, and MD signals
  - Dual copies of MA and control signals for improved drive
  - Optional ECC (single-bit error correction and multi-bit error detection) or EC (error checking only) for DRAM integrity
  - Two-bank interleaving for 16Mbit SDRAM support
  - Two-bank and four bank interleaving for 64Mbit SDRAM support
  - Supports maximum 8-bank interleave (i.e., 8 pages open simultaneously); banks are allocated based on LRU
  - Seamless DRAM command scheduling for maximum DRAM bus utilization (e.g., precharge other banks while accessing the current bank)
  - Four cache lines (16 quadwords) of CPU to DRAM write buffers
  - Four cache lines of CPU to DRAM read prefetch buffers
  - Read around write capability for non-stalled CPU read
  - Speculative DRAM read before snoop result
  - Burst read and write operation
  - x-1-1-1-1-1-1-1 back-to-back accesses for SDR SDRAM
  - x-1/2-1/2-1/2-1-1/2-1/2-1/2 back-to-back accesses for DDR SDRAM
  - Supports DDR SDRAM CL 2/2.5/3 and 1T per command
  - Decoupled and burst DRAM refresh with staggered RAS timing (CAS before RAS or self refresh)
- **Advanced System Power Management Support**
  - Dynamic power down of SDRAM (CKE)
  - PCI and AGP bus clock run and clock generator control
  - VTT suspend power plane preserves memory data
  - Suspend-to-DRAM and Self-Refresh operation
  - SDRAM self-refresh power down
  - 8 bytes of BIOS scratch registers
  - Low-leakage I/O pads
- **Built-in NAND-tree pin scan test capability**
- **2.5V, 0.22um, high speed / low power CMOS process**
- **35 x 35 mm, 552 pin BGA Package**

OVERVIEW

The **Apollo KT266A (VT8366A** North Bridge plus **VT8233** South Bridge**)** is a high performance, cost-effective and energy efficient chipset for the implementation of AGP / PCI desktop personal computer systems based on 64-bit Socket-A (AMD Athlon) processors.

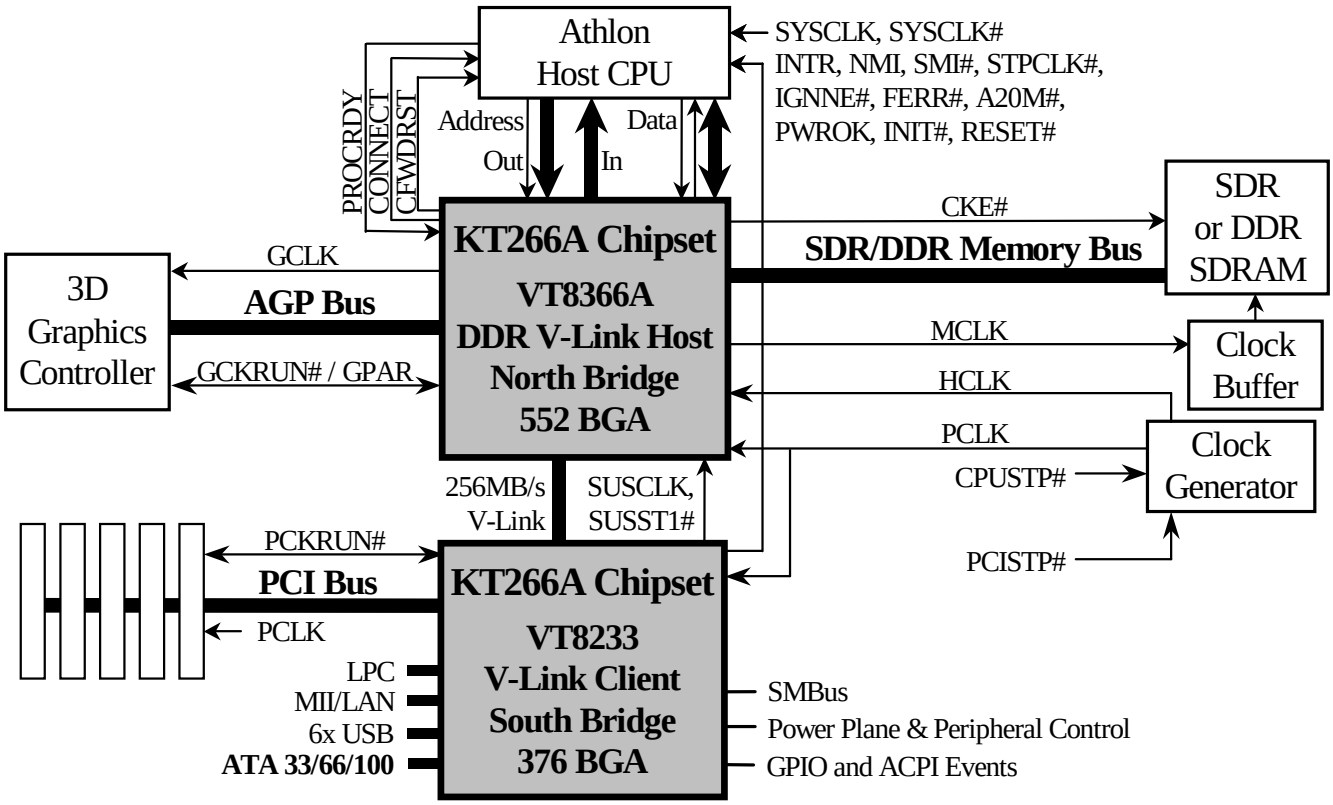

Figure 1. Apollo KT266A Chipset System Block Diagram

The KT266A chipset consists of the VT8366A north bridge "host system controller" (552 pin BGA) and the VT8233 V-Link south bridge (376 pin BGA). The VT8366A provides superior performance between the CPU, DRAM, AGP bus, and V-Link bus with pipelined, burst, and concurrent operation. The VT8233 (also referred to as a "V-Link Client controller") is a highly integrated PCI / LPC controller. Its internal bus structure is based on 66 MHz PCI bus that provides 2x bandwidth compare to previous generation PCI / ISA bridge chips. The VT8233 also provides a 266MB/sec bandwidth Host/Client V-Link interface with V-Link-PCI and V-Link-LPC controllers. It supports five PCI slots of arbitration and decoding for all integrated functions and LPC bus.

The VT8366A north bridge supports eight banks of SDR / DDR SDRAMs up to 4 GB for registered modules (six banks up to 3GB for unbuffered modules). The DRAM controller supports standard PC133 / PC100 Synchronous DRAM (SDRAM) or can be configured to support PC2100 / PC1600 Double-Data-Rated (DDR) SDRAM. The SDR / DDR DRAM interface allows zero wait state bursting between the DRAM and the data buffers at 66 / 100 / 133 MHz. The different banks of DRAM can be composed of an arbitrary mixture of 1M / 2M / 4M / 8M / 16M / 32M / 64M xN DRAMs. The DRAM controller also supports optional ECC (single-bit error correction and multi-bit detection) or EC (error checking) capability. The DRAM controller can run either synchronous or pseudo-synchronous with the host CPU bus (66 / 100 / 133 MHz).

The VT8366A north bridge also supports full AGP v2.0 capability for maximum bus utilization including 2x and 4x mode transfers, SBA (SideBand Addressing), Flush/Fence commands, and pipelined grants. An eight level request queue plus a four level post-write request queue with thirty-two and sixteen quadwords of read and write data FIFO's respectively are included for

deep pipelined and split AGP transactions. A single-level GART TLB with 16 full associative entries and flexible CPU / AGP / PCI remapping control is also provided for operation under protected mode operating environments. Both Windows-95 VXD and Windows-98 / NT5 miniport drivers are supported for interoperability with major AGP-based 3D and DVD-capable multimedia accelerators.

The VT8366A host system controller supports a high speed 8-bit 66 MHz Quad Data Transfer interconnect (V-Link) to the VT8233 South Bridge. The chip also contains a built-in bus-to-bus bridge to allow simultaneous concurrent operations on each bus. Five levels (doublewords) of post write buffers are included to allow for concurrent CPU and V-Link operation. For V-Link Host operation, forty-eight levels (doublewords) of post write buffers and sixteen levels (doublewords) of prefetch buffers are included for concurrent V-Link bus and DRAM/cache accesses. When combined the V-Link Host / Client controllers, it realizes a complete PCI sub-system and supports enhanced PCI bus commands such as Memory-Read-Line, Memory-Read-Multiple and Memory-Write-Invalid commands to minimize snoop overhead. In addition, advanced features are supported such as snoop ahead, snoop filtering, L1 write-back forward to PCI master, and L1 write-back merged with PCI post write buffers to minimize PCI master read latency and DRAM utilization. Delay transaction and read caching mechanisms are also implemented for further improvement of overall system performance.

The 376-pin Ball Grid Array VT8233 Client V-Link PCI / LPC controller supports four levels (doublewords) of line buffers, type F DMA transfers and delay transaction to allow efficient PCI bus utilization and (PCI-2.1 compliant). The VT8233 integrated PCI controller and PCI arbitration for up to five PCI slots. One of the PCI REQ / GNT pair can be configured as high-priority to better support a low latency PCI bus master device. The VT8233 integrated networking MAC controller with standard MII interface to an external PHY for 10/100Mb base-T Ethernet or 1/10Mb PNA home networking.

The VT8233 also includes an integrated keyboard controller with PS2 mouse support, integrated DS12885 style real time clock with extended 256 byte CMOS RAM, integrated master mode enhanced IDE controller with full scatter / gather capability and extension to UltraDMA-33/66/100 for 33/66/100 MB/sec transfer rate, integrated USB interface with root hubs and six function ports with built-in physical layer transceivers, Distributed DMA support, and OnNow / ACPI compliant advanced configuration and power management interface.

For sophisticated power management, the Apollo KT266A chipset provides independent clock stop control for the CPU / SDRAM, PCI, and AGP buses and Dynamic CKE control for powering down of the SDRAM. A separate suspend-well plane is implemented for the SDRAM control signals for Suspend-to-DRAM operation. Coupled with the VT8233 south bridge chip, a complete power conscious PC main board can be implemented with no external TTLs.

The Apollo KT266A chipset is ideal for high performance, high quality, high energy efficient and high integration desktop and notebook AGP / PCI / LPC computer systems.

PINOUTS

Figure 2. VT8366A North Bridge Chip Ball Diagram (Top View)

Key	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
A	VCC AGP	VCC AGP	GD16	GD17	AGP VREF	VCC AGP	GD23	GD24	GD28	VCC AGP	SB A7	SB STB#	SB A0	VCC AGP	AIN 9#	AIN 13#	AIN 6#	D11#	D10#	D12#	D1#	D15#	D17#	D18#	D28#	D29#
B	GD15	GBE1#	GBE2#	GND	GD21	VCC AGP	GBE3#	GD27	GD30	VCC AGP	SB A4	SB STB	SB A1	VCC AGP	AIN 12#	GND	AIN 3#	D9#	GND	D8#	D3#	GND	D24#	D27#	GND	DI CLK1#
C	GD11	GD12	GD13	GD14	GD19	GD20	GD22	GD26	GD31	GRBF#	SB A5	GND	G GNT#	CFWD RST	CON NECT	AIN 10#	AIN 7#	AIN 11#	DO CLK0#	D5#	D7#	D6#	D16#	D25#	D21#	D23#
D	GD8	GND	GBE0#	GND	GD18	GND	GDEV SEL#	GD25	ST0	ST2	G PIPE#	SB A3	SB A2	G REQ#	VCCH	AIN 4#	AIN 2#	VCCH	DI CLK0#	D0#	VCCH	D4#	VCCH	D22#	D31#	DO CLK1#
E	VCC AGP	VCC AGP	G DS0#	GD10	G STOP#	G TRDY#	G FRM#	G DS1	G WBF#	GND	SB A6	VCC AGP	ST1	PROC RDY	AIN 14#	DIN VAL#	AIN CLK#	AIN 5#	D14#	D13#	D2#	D26#	D19#	D20#	GND	D30#
F	GD7	GD4	GD6	G DS0	GD9	GND	GND	G DS1#	GD29	GND	G IRDY#	VCC AGP	GND	GND	AIN 8#	S2K VREF	GND	GND	VCCH	GND	GND	S2K GND	D32#	DI CLK2#	D33#	D41#
G	GD5	GND	G CLK	GND	G PAR	VCC AGP	G7	8	9	10	11	12	13	14	15	16	17	18	19	G20	S2K VCC	S2K COMP	VCCH	D40#	D42#	DO CLK2#
H	GD1	GD3	GD0	GD2	VCC Q	VCC AGP	H		AGP Pins								CPU Pins			H	H CLK	S2K VTT	D46#	D36#	GND	D43#
J	VID	G COMP	GND Q	VAD0 strap	GND	GND	J		VCC AGP	VCC AGP	VCC 25	VCC 25	VCC AGP	VCCH	VCC 25	VCC 25	VCCH	VCCH		J	H CLK#	AGND HCK	D45#	D44#	D38#	D34#
K	UP STB	UP STB#	UP CMD	V BE#	VL VREF	VAD1 strap	K		VCC AGP	K10	11	12	13	14	15	16	K17	VCCH		K	VCCH	AVCC HCK	VCCH	D35#	D37#	D39#
L	DN CMD	DN STB	DN STB#	V PAR	VAD4 strap	VAD2 strap	L	VLink	VCC 25	L	GND	GND	GND	GND	GND	GND	L	VCC 25		L	GND	GND	D47#	D58#	GND	D56#
M	VCC VL	VCC VL	GND	GND	VCC VL	VCC VL	M	Pins	VCC 25	M	GND	GND	GND	GND	GND	GND	M	VCC 25		M	D59#	D48#	DI CLK3#	D57#	D60#	D62#
N	VCC VK	VAD6 strap	VAD7	VAD5 strap	VAD3 strap	VCC VL	N		VCC VL	N	GND	GND	GND	GND	GND	GND	N	VCCH		N	D51#	D63#	VCCH	D52#	D53#	DO CLK3#
P	VL COMP	GND	PWR OK	RE SET#	GND	GND	P		VCCM	P	GND	GND	GND	GND	GND	GND	P	VCCH		P	GND	D49#	D50#	D54#	GND	D61#
R	MD58	MD63	MD59	VSUS 25	SUS ST#	VCCM	R		VCC 25	R	GND	GND	GND	GND	GND	GND	R	VCC 25		R	VCCH	D55#	AOUT 4#	AOUT 6#	AOUT 2#	AOUT 3#
T	VCCM	VCCM	GND	GND	MD62	VCCM	T		VCC 25	T	GND	GND	GND	GND	GND	GND	T	VCC 25		T	S2K VREF	AOUT 8#	VCCH	AOUT 5#	AOUT 9#	AO CLK#
U	MD57	DQM 7	DQS 7#	MD61	MD56	MD60	U		VCCM	U10	11	12	13	14	15	16	U17	VCCM		U	AVCC MCK	AGND MCK	AOUT 11#	AOUT 13#	GND	AOUT 12#
V	MD51	MD55	MD50	MD54	MD53	M VREF	V		VCCM	VCCM	VCC 25	VCC 25	VCCM	VCCM	VCC 25	VCC 25	VCCM	VCCM		V	MCLK FB	MCLK	GND	AOUT 10#	AOUT 7#	AOUT 14#
W	DQS 6#	DQM 6	MD52	AGND DL2	AVCC DL2	GND	W						DRAM Pins							W	VCCM	VCCM	MD0	TEST IN#	VCCM	VCCM
Y	VCCM	VCCM	GND	GND	CS7#	VCCM	Y7	8	9	10	11	12	13	14	15	16	17	18	19	Y20	GND	MAB 14	MAA 14	GND	MD5	MD4
AA	MD49	MD48	MD47	MD46	CS6#	GND	VCCM	GND	VCCM	MD36	GND	VCCM	GND	VCCM	VCCM	GND	VCCM	AVCC DL1	M VREF	VCCM	GND	MAA 8	MD2	DQM 0	MD1	DQS 0#
AB	MD43	DQM 5	MD42	MAA 11	MAB 12	MAA 12	MAB 10	MAA 10	VCCM	MD32	DQM 8	VCCM	MAA 1	MAB 2	MAA 2	MAA 3	VCCM	AGND DL1	MD16	VCCM	MAA 5	MAB 8	GND	MAA 13	GND	MD6
AC	MD41	GND	DQS 5#	MAB 11	GND	SRAS A#	MD39	GND	MAB 0	MECC7 CKE7	GND	MECC4 CKE4	GND	MD26	MD25	GND	MAA 4	MD18	MD17	MAA 6	MAB 5	DQM 1	MAB 7	MAA 9	MAB 13	MD7
AD	MD45	MD44	MD40	CS1#	CS5#	SWE B#	MD38	DQS 4#	DQS FB	MECC2 CKE2	MAA 0	MECC5 CKE5	MAB 1	MD30	MD29	MAB 3	MAB 4	MD22	DQS 2#	GND	GND	MD14	MD13	MAA 7	MAB 9	MD3
AE	CS3#	CS2#	SCAS A#	CS4#	GND	SRAS B#	DQM 4	GND	MD37	MECC6 CKE6	GND	MECC0 CKE0	GND	MD27	DQS 3#	GND	MD24	MD23	DQM 2	MAB 6	MD11	MD10	GND	MD9	GND	VCCM
AF	VCCM	VCCM	CS0#	SCAS B#	SWE A#	MD35	VCCM	MD34	MD33	MECC3 CKE3	DQS 8#	MECC1 CKE1	VCCM	MD31	DQM 3	VCCM	MD28	MD19	MD21	VCCM	MD20	MD15	DQS 1#	MD12	MD8	VCCM

Table 1. VT8366A North Bridge Chip Pin List (Numerical Order)

Pin #		Pin Name	Pin #		Pin Name	Pin #		Pin Name	Pin #		Pin Name	Pin #		Pin Names	Pin #		Pin Name
A01	**P**	**VCCAGP**	D03	IO	GBE0#	G05	IO	GPAR / GCKRUN#	P01	I	VLCOMP	Y23	O	MAA14	AC25	O	MAB13
A02	**P**	**VCCAGP**	**D04**	**P**	**GND**	**G06**	**P**	**VCCAGP**	P03	I	PWROK	**Y24**	**P**	**GND**	AC26	IO	MD07
A03	IO	GD16	D05	IO	GD18	**G21**	**P**	**S2KVCC**	Y25	IO	MD05	AD01	IO	MD45			
A04	IO	GD17	**D06**	**P**	**GND**	G22	I	S2KCOMP	P04	I	RESET#	Y26	IO	MD04	AD02	IO	MD44
A05	**P**	**AGPVREF**	D07	IO	GDEVSEL#	**G23**	**P**	**VCCH**	**P05**	**P**	**GND**	AA01	IO	MD49	AD03	IO	MD40
A06	**P**	**VCCAGP**	D08	IO	GD25	G24	IO	D40#	AA02	IO	MD48	AD04	O	CS1#			
A07	IO	GD23	D09	O	ST0	G25	IO	D42#	**P06**	**P**	**GND**	AA03	IO	MD47	AD05	O	CS5#
A08	IO	GD24	D10	O	ST2	G26	I	DOCLK2#	**P21**	**P**	**GND**	AA04	IO	MD46	AD06	O	SWEB#
A09	IO	GD28	D11	I	GPIPE#	H01	IO	GD1	P22	IO	D49#	AA05	O	CS6#	AD07	IO	MD38
A10	**P**	**VCCAGP**	D12	I	SBA3	H02	IO	GD3	P23	IO	D50#	**AA06**	**P**	**GND**	AD08	O	DQS4# / CKE4
A11	I	SBA7	D13	I	SBA2	H03	IO	GD0	P24	IO	D54#	**AA07**	**P**	**VCCM**	AD09	I	DQSFB
A12	I	SBS#	D14	I	GREQ#	H04	IO	GD2	**P25**	**P**	**GND**	**AA08**	**P**	**GND**	AD10	IO	MECC2 / CKE2
A13	I	SBA0	**D15**	**P**	**VCCH**	**H05**	**P**	**VCCQ**	P26	IO	D61#	**AA09**	**P**	**VCCM**	AD11	O	MAA00
A14	**P**	**VCCAGP**	D16	O	AIN04#	**H06**	**P**	**VCCAGP**	R01	IO	MD58	AA10	IO	MD36	AD12	IO	MECC5 / CKE5
A15	O	AIN09#	D17	O	AIN02#	H21	I	HCLK	R02	IO	MD63	**AA11**	**P**	**GND**	AD13	O	MAB01
A16	O	AIN13#	**D18**	**P**	**VCCH**	**H22**	**P**	**S2KVTT**	R03	IO	MD59	**AA12**	**P**	**VCCM**	AD14	IO	MD30
A17	O	AIN06#	D19	O	DICLK0#	H23	IO	D46#	**R04**	**P**	**VSUS25**	**AA13**	**P**	**GND**	AD15	IO	MD29
A18	IO	D11#	D20	IO	D00#	H24	IO	D36#	R05	I	SUSST#	**AA14**	**P**	**VCCM**	AD16	O	MAB03
A19	IO	D10#	**D21**	**P**	**VCCH**	**H25**	**P**	**GND**	**R06**	**P**	**VCCM**	**AA15**	**P**	**VCCM**	AD17	O	MAB04
A20	IO	D12#	D22	IO	D04#	H26	IO	D43#	**R21**	**P**	**VCCH**	**AA16**	**P**	**GND**	AD18	IO	MD22
A21	IO	D01#	**D23**	**P**	**VCCH**	J01	I	VID	R22	IO	D55#	**AA17**	**P**	**VCCM**	AD19	O	DQS2# / CKE2
A22	IO	D15#	D24	IO	D22#	J02	I	GCOMP	R23	I	AOUT04#	**AA18**	**P**	**AVCCDL1**	**AD20**	**P**	**GND**
A23	IO	D17#	D25	IO	D31#	**J03**	**P**	**GNDQ**	R24	I	AOUT06#	**AA19**	**P**	**MVREF**	**AD21**	**P**	**GND**
A24	IO	D18#	D26	I	DOCLK1#	J04	IO	VAD0 / strap	R25	I	AOUT02#	**AA20**	**P**	**VCCM**	AD22	IO	MD14
A25	IO	D28#	**E01**	**P**	**VCCAGP**	**J05**	**P**	**GND**	R26	I	AOUT03#	**AA21**	**P**	**GND**	AD23	IO	MD13
A26	IO	D29#	**E02**	**P**	**VCCAGP**	**J06**	**P**	**GND**	**T01**	**P**	**VCCM**	**AA22**	**P**	**VCCM**	AD24	O	MAA07
B01	IO	GD15	E03	IO	GDS0#	J21	I	HCLK#	**T02**	**P**	**VCCM**	AA22	O	MAA08	AD25	O	MAB09
B02	IO	GBE1#	E04	IO	GD10	**J22**	**P**	**AGNDHCK**	**T03**	**P**	**GND**	AA23	IO	MD02	AD26	IO	MD03
B03	IO	GBE2#	E05	IO	GSTOP#	J23	IO	D45#	**T04**	**P**	**GND**	AA24	O	DQM0 / CKE0	AE01	O	CS3#
B04	**P**	**GND**	E06	IO	GTRDY#	J24	IO	D44#	T05	IO	MD62	AA25	IO	MD01	AE02	O	CS2#
B05	IO	GD21	E07	IO	GFRM#	J25	IO	D38#	**T06**	**P**	**VCCM**	AA26	O	DQS0# / CKE0	AE03	O	SCASA#
B06	**P**	**VCCAGP**	E08	IO	GDS1	J26	IO	D34#	**T21**	**P**	**S2KVREF**	AB01	IO	MD43	AE04	O	CS4#
B07	IO	GBE3#	E09	I	GWBF#	K01	I	UPSTB	T22	I	AOUT08#	AB02	O	DQM5 / CKE5	**AE05**	**P**	**GND**
B08	IO	GD27	**E10**	**P**	**GND**	K02	I	UPSTB#	**T23**	**P**	**VCCH**	AB03	IO	MD42	AE06	O	SRASB#
B09	IO	GD30	E11	I	SBA6	K03	I	UPCMD	T24	I	AOUT05#	AB04	O	MAA11	AE07	O	DQM4 / CKE4
B10	**P**	**VCCAGP**	**E12**	**P**	**VCCAGP**	K04	IO	VBE#	T25	I	AOUT09#	AB05	O	MAB12	**AE08**	**P**	**GND**
B11	I	SBA4	E13	O	ST1	**K05**	**P**	**VLVREF**	T26	I	AOUTCLK#	AB06	O	MAA12	AE09	IO	MD37
B12	I	SBS	E14	I	PROCRDY	K06	IO	VAD1 / strap	U01	IO	MD57	AB07	O	MAB10	AE10	IO	MECC6 / CKE6
B13	I	SBA1	E15	O	AIN14#	**K21**	**P**	**VCCH**	U02	O	DQM7 / CKE7	AB08	O	MAA10	**AE11**	**P**	**GND**
B14	**P**	**VCCAGP**	E16	O	DINVAL#	**K22**	**P**	**AVCCHCK**	U03	O	DQS7# / CKE7	**AB09**	**P**	**VCCM**	AE12	IO	MECC0 / CKE0
B15	O	AIN12#	E17	O	AINCLK#	**K23**	**P**	**VCCH**	U04	IO	MD61	AB10	IO	MD32	**AE13**	**P**	**GND**
B16	**P**	**GND**	E18	O	AIN05#	K24	IO	D35#	U05	IO	MD56	AB11	O	DQM8	AE14	IO	MD27
B17	O	AIN03#	E19	IO	D14#	K25	IO	D37#	U06	IO	MD60	**AB12**	**P**	**VCCM**	AE15	O	DQS3# / CKE3
B18	IO	D09#	E20	IO	D13#	K26	IO	D39#	**U21**	**P**	**AVCCMCK**	AB13	O	MAA01	**AE16**	**P**	**GND**
B19	**P**	**GND**	E21	IO	D02#	L01	O	DNCMD	**U22**	**P**	**AGNDMCK**	AB14	O	MAB02	AE17	IO	MD24
B20	IO	D08#	E22	IO	D26#	L02	O	DNSTB	U23	I	AOUT11#	AB15	O	MAA02	AE18	IO	MD23
B21	IO	D03#	E23	IO	D19#	L03	O	DNSTB#	U24	I	AOUT13#	AB16	O	MAA03	AE19	O	DQM2 / CKE2
B22	**P**	**GND**	E24	IO	D20#	L04	IO	VPAR	**U25**	**P**	**GND**	**AB17**	**P**	**VCCM**	AE20	O	MAB06
B23	IO	D24#	**E25**	**P**	**GND**	L05	IO	VAD4 / strap	U26	I	AOUT12#	**AB18**	**P**	**AGNDDL1**	AE21	IO	MD11
B24	IO	D27#	E26	IO	D30#	L06	IO	VAD2 / strap	V01	IO	MD51	AB19	IO	MD16	AE22	IO	MD10
B25	**P**	**GND**	F01	IO	GD7	**L21**	**P**	**GND**	V02	IO	MD55	**AB20**	**P**	**VCCM**	**AE23**	**P**	**GND**
B26	O	DICLK1#	F02	IO	GD4	**L22**	**P**	**GND**	V03	IO	MD50	AB21	O	MAA05	AE24	IO	MD09
C01	IO	GD11	F03	IO	GD6	L23	IO	D47#	V04	IO	MD54	AB22	O	MAB08	**AE25**	**P**	**GND**
C02	IO	GD12	F04	IO	GDS0	L24	IO	D58#	V05	IO	MD53	**AB23**	**P**	**GND**	**AE26**	**P**	**VCCM**
C03	IO	GD13	F05	IO	GD9	**L25**	**P**	**GND**	**V06**	**P**	**MVREF**	AB24	O	MAA13			
C04	IO	GD14	**F06**	**P**	**GND**	L26	IO	D56#	V21	I	MCLKFB	**AB25**	**P**	**GND**	**AF01**	**P**	**VCCM**
C05	IO	GD19	**F07**	**P**	**GND**	**M01**	**P**	**VCCVL**	V22	O	MCLK	AB26	IO	MD06	**AF02**	**P**	**VCCM**
C06	IO	GD20	F08	IO	GDS1#	**M02**	**P**	**VCCVL**	**V23**	**P**	**GND**	AC01	IO	MD41	AF03	O	CS0#
C07	IO	GD22	F09	IO	GD29	**M03**	**P**	**GND**	V24	I	AOUT10#	**AC02**	**P**	**GND**	AF04	O	SCASB#
C08	IO	GD26	**F10**	**P**	**GND**	**M04**	**P**	**GND**	V25	I	AOUT07#	AC03	O	DQS5# / CKE5	AF05	O	SWEA#
C09	IO	GD31	F11	IO	GIRDY#	**M05**	**P**	**VCCVL**	V26	I	AOUT14#	AC04	O	MAB11	AF06	IO	MD35
C10	I	GRBF#	**F12**	**P**	**VCCAGP**	**M06**	**P**	**VCCVL**	W01	O	DQS6# / CKE6	**AC05**	**P**	**GND**	**AF07**	**P**	**VCCM**
C11	I	SBA5	**F13**	**P**	**GND**	M21	IO	D59#	W02	O	DQM6 / CKE6	AC06	O	SRASA#	AF08	IO	MD34
C12	**P**	**GND**	**F14**	**P**	**GND**	M22	IO	D48#	W03	IO	MD52	AC07	IO	MD39	AF09	IO	MD33
C13	O	GGNT#	F15	O	AIN08#	M23	O	DICLK3#	**W04**	**P**	**AGNDDL2**	**AC08**	**P**	**GND**	AF10	IO	MECC3 / CKE3
C14	O	CFWDRST	**F16**	**P**	**S2KVREF**	M24	IO	D57#	**W05**	**P**	**AVCCDL2**	AC09	O	MAB00	AF11	O	DQS8#
C15	O	CONNECT	**F17**	**P**	**GND**	M25	IO	D60#	**W06**	**P**	**GND**	AC10	IO	MECC7 / CKE7	AF12	IO	MECC1 / CKE1
C16	O	AIN10#	**F18**	**P**	**GND**	M26	IO	D62#	**W21**	**P**	**VCCM**	**AC11**	**P**	**GND**	**AF13**	**P**	**VCCM**
C17	O	AIN07#	**F19**	**P**	**VCCH**	**N01**	**P**	**VCCVK**	**W22**	**P**	**VCCM**	AC12	IO	MECC4 / CKE4	AF14	IO	MD31
C18	O	AIN11#	**F20**	**P**	**GND**	N02	IO	VAD6 / strap	W23	IO	MD00	**AC13**	**P**	**GND**	AF15	O	DQM3 / CKE3
C19	I	DOCLK0#	**F21**	**P**	**GND**	N03	IO	VAD7	W24	I	TESTIN#	AC14	IO	MD26	**AF16**	**P**	**VCCM**
C20	IO	D05#	**F22**	**P**	**S2KGND**	N04	IO	VAD5 / strap	**W25**	**P**	**VCCM**	AC15	IO	MD25	AF17	IO	MD28
C21	IO	D07#	F23	IO	D32#	N05	IO	VAD3 / strap	**W26**	**P**	**VCCM**	**AC16**	**P**	**GND**	AF18	IO	MD19
C22	IO	D06#	F24	O	DICLK2#	**N06**	**P**	**VCCVL**	**Y01**	**P**	**VCCM**	AC17	O	MAA04	AF19	IO	MD21
C23	IO	D16#	F25	IO	D33#	N21	IO	D51#	**Y02**	**P**	**VCCM**	AC18	IO	MD18	**AF20**	**P**	**VCCM**
C24	IO	D25#	F26	IO	D41#	N22	IO	D63#	**Y03**	**P**	**GND**	AC19	IO	MD17	AF21	IO	MD20
C25	IO	D21#	G01	IO	GD5	**N23**	**P**	**VCCH**	**Y04**	**P**	**GND**	AC20	O	MAA06	AF22	IO	MD15
C26	IO	D23#	**G02**	**P**	**GND**	N24	IO	D52#	Y05	O	CS7#	AC21	O	MAB05	AF23	O	DQS1# / CKE1
D01	IO	GD8	G03	I	GCLK	N25	IO	D53 #	**Y06**	**P**	**VCCM**	AC22	O	DQM1 / CKE1	AF24	IO	MD12
D02	**P**	**GND**	**G04**	**P**	**GND**	N26	I	DOCLK3#	**Y21**	**P**	**GND**	AC23	O	MAB07	AF25	IO	MD08
									Y22	O	MAB14	AC24	O	MAA09	**AF26**	**P**	**VCCM**

Center **VCC25** Pins (16 pins): **J11-12,15-16,L9,18,M9,18,R9,18,T9,18,V11-12,15-16**
Center **VCCH** (6 pins): **J14, 17-18,K18,N18,P18**
Center **VCCAGP** (4 pins): **J9-10,13,K9**
Center **GND** Pins (36 pins): **L11-16,M11-16,N11-16,P11-16,R11-16,T11-16**
Center **VCCM** (9 pins): **P9,U9,18,V9-10,13-14,17-18**
Center **VCCVL** (1 pin): **N9**

Table 2. VT8366A North Bridge Chip Pin List (Alphabetical Order)

Pin #		Pin Name	Pin #		Pin Name	Pin #		Pin Name	Pin #		Pin Name	Pin #		Pin Names	Pin #		Pin Name
AB18	**P**	**AGNDDL1**	F25	IO	D33#	C02	IO	GD12	**AC02**	**P**	**GND**	AE18	IO	MD23	W24	I	TESTIN#
W04	**P**	**AGNDDL2**	J26	IO	D34#	C03	IO	GD13	**AC05**	**P**	**GND**	AE17	IO	MD24	K03	I	UPCMD
J22	**P**	**AGNDHCK**	K24	IO	D35#	C04	IO	GD14	**AC08**	**P**	**GND**	AC15	IO	MD25	K01	I	UPSTB
U22	**P**	**AGNDMCK**	H24	IO	D36#	B01	IO	GD15	**AC11**	**P**	**GND**	AC14	IO	MD26	K02	I	UPSTB#
AA18	**P**	**AVCCDL1**	K25	IO	D37#	A03	IO	GD16	**AC13**	**P**	**GND**	AE14	IO	MD27	J04	IO	VAD0 / strap
W05	**P**	**AVCCDL2**	J25	IO	D38#	A04	IO	GD17	**AC16**	**P**	**GND**	AF17	IO	MD28	K06	IO	VAD1 / strap
K22	**P**	**AVCCHCK**	K26	IO	D39#	D05	IO	GD18	**AD20**	**P**	**GND**	AD15	IO	MD29	L06	IO	VAD2 / strap
U21	**P**	**AVCCMCK**	G24	IO	D40#	C05	IO	GD19	**AD21**	**P**	**GND**	AD14	IO	MD30	N05	IO	VAD3 / strap
A05	**P**	**AGPVREF**	F26	IO	D41#	C06	IO	GD20	**AE05**	**P**	**GND**	AF14	IO	MD31	L05	IO	VAD4 /strap
D17	O	AIN02#	G25	IO	D42#	B05	IO	GD21	**AE08**	**P**	**GND**	AB10	IO	MD32	N04	IO	VAD5 / strap
B17	O	AIN03#	H26	IO	D43#	C07	IO	GD22	**AE11**	**P**	**GND**	AF09	IO	MD33	N02	IO	VAD6 / strap
D16	O	AIN04#	J24	IO	D44#	A07	IO	GD23	**AE13**	**P**	**GND**	AF08	IO	MD34	N03	IO	VAD7
E18	O	AIN05#	J23	IO	D45#	A08	IO	GD24	**AE16**	**P**	**GND**	AF06	IO	MD35	K04	IO	VBE#
A17	O	AIN06#	H23	IO	D46#	D08	IO	GD25	**AE23**	**P**	**GND**	AA10	IO	MD36	**A01**	**P**	**VCCAGP**
C17	O	AIN07#	L23	IO	D47#	C08	IO	GD26	**AE25**	**P**	**GND**	AE09	IO	MD37	**A02**	**P**	**VCCAGP**
F15	O	AIN08#	M22	IO	D48#	B08	IO	GD27	**J03**	**P**	**GNDQ**	AD07	IO	MD38	**A06**	**P**	**VCCAGP**
A15	O	AIN09#	P22	IO	D49#	A09	IO	GD28	G05	IO	GPAR / GCKRUN#	AC07	IO	MD39	**A10**	**P**	**VCCAGP**
C16	O	AIN10#	P23	IO	D50#	F09	IO	GD29	D11	I	GPIPE#	AD03	IO	MD40	**A14**	**P**	**VCCAGP**
C18	O	AIN11#	N21	IO	D51#	B09	IO	GD30	C10	I	GRBF#	AC01	IO	MD41	**B06**	**P**	**VCCAGP**
B15	O	AIN12#	N24	IO	D52#	C09	IO	GD31	D14	I	GREQ#	AB03	IO	MD42	**B10**	**P**	**VCCAGP**
A16	O	AIN13#	N25	IO	D53 #	D07	IO	GDEVSEL#	E05	IO	GSTOP#	AB01	IO	MD43	**B14**	**P**	**VCCAGP**
E15	O	AIN14#	P24	IO	D54#	F04	IO	GDS0	E06	IO	GTRDY#	AD02	IO	MD44	**E01**	**P**	**VCCAGP**
E17	O	AINCLK#	R22	IO	D55#	E03	IO	GDS0#	E09	I	GWBF#	AD01	IO	MD45	**E02**	**P**	**VCCAGP**
R25	I	AOUT02#	L26	IO	D56#	E08	IO	GDS1	H21	I	HCLK	AA04	IO	MD46	**E12**	**P**	**VCCAGP**
R26	I	AOUT03#	M24	IO	D57#	F08	IO	GDS1#	J21	I	HCLK#	AA03	IO	MD47	**F12**	**P**	**VCCAGP**
R23	I	AOUT04#	L24	IO	D58#	E07	IO	GFRM#	AD11	O	MAA00	AA02	IO	MD48	**G06**	**P**	**VCCAGP**
T24	I	AOUT05#	M21	IO	D59#	C13	O	GGNT#	AB13	O	MAA01	AA01	IO	MD49	**H06**	**P**	**VCCAGP**
R24	I	AOUT06#	M25	IO	D60#	F11	IO	GIRDY#	AB15	O	MAA02	V03	IO	MD50	**D15**	**P**	**VCCH**
V25	I	AOUT07#	P26	IO	D61#	**B04**	**P**	**GND**	AB16	O	MAA03	V01	IO	MD51	**D18**	**P**	**VCCH**
T22	I	AOUT08#	M26	IO	D62#	**B16**	**P**	**GND**	AC17	O	MAA04	W03	IO	MD52	**D21**	**P**	**VCCH**
T25	I	AOUT09#	N22	IO	D63#	**B19**	**P**	**GND**	AB21	O	MAA05	V05	IO	MD53	**D23**	**P**	**VCCH**
V24	I	AOUT10#	D19	O	DICLK0#	**B22**	**P**	**GND**	AC20	O	MAA06	V04	IO	MD54	**F19**	**P**	**VCCH**
U23	I	AOUT11#	B26	O	DICLK1#	**B25**	**P**	**GND**	AD24	O	MAA07	V02	IO	MD55	**G23**	**P**	**VCCH**
U26	I	AOUT12#	F24	O	DICLK2#	**C12**	**P**	**GND**	AA22	O	MAA08	U05	IO	MD56	**K21**	**P**	**VCCH**
U24	I	AOUT13#	M23	O	DICLK3#	**D02**	**P**	**GND**	AC24	O	MAA09	U01	IO	MD57	**K23**	**P**	**VCCH**
V26	I	AOUT14#	E16	O	DINVAL#	**D04**	**P**	**GND**	AB08	O	MAA10	R01	IO	MD58	**N23**	**P**	**VCCH**
T26	I	AOUTCLK#	C19	I	DOCLK0#	**D06**	**P**	**GND**	AB04	O	MAA11	R03	IO	MD59	**R21**	**P**	**VCCH**
C14	O	CFWDRST	D26	I	DOCLK1#	**E10**	**P**	**GND**	AB06	O	MAA12	U06	IO	MD60	**T23**	**P**	**VCCH**
C15	O	CONNECT	G26	I	DOCLK2#	**E25**	**P**	**GND**	AB24	O	MAA13	U04	IO	MD61	**R06**	**P**	**VCCM**
AF03	O	CS0#	N26	I	DOCLK3#	**F06**	**P**	**GND**	Y23	O	MAA14	T05	IO	MD62	**T01**	**P**	**VCCM**
AD04	O	CS1#	L01	O	DNCMD	**F07**	**P**	**GND**	AC09	O	MAB00	R02	IO	MD63	**T02**	**P**	**VCCM**
AE02	O	CS2#	L02	O	DNSTB	**F10**	**P**	**GND**	AD13	O	MAB01	AE12	IO	MECC0 / CKE0	**T06**	**P**	**VCCM**
AE01	O	CS3#	L03	O	DNSTB#	**F13**	**P**	**GND**	AB14	O	MAB02	AF12	IO	MECC1 / CKE1	**W21**	**P**	**VCCM**
AE04	O	CS4#	AA24	O	DQM0 / CKE0	**F14**	**P**	**GND**	AD16	O	MAB03	AD10	IO	MECC2 / CKE2	**W22**	**P**	**VCCM**
AD05	O	CS5#	AC22	O	DQM1 / CKE1	**F17**	**P**	**GND**	AD17	O	MAB04	AF10	IO	MECC3 / CKE3	**W25**	**P**	**VCCM**
AA05	O	CS6#	AE19	O	DQM2 / CKE2	**F18**	**P**	**GND**	AC21	O	MAB05	AC12	IO	MECC4 / CKE4	**W26**	**P**	**VCCM**
Y05	O	CS7#	AF15	O	DQM3 / CKE3	**F20**	**P**	**GND**	AE20	O	MAB06	AD12	IO	MECC5 / CKE5	**Y01**	**P**	**VCCM**
D20	IO	D00#	AE07	O	DQM4 / CKE4	**F21**	**P**	**GND**	AC23	O	MAB07	AE10	IO	MECC6 / CKE6	**Y02**	**P**	**VCCM**
A21	IO	D01#	AB02	O	DQM5 / CKE5	**G02**	**P**	**GND**	AB22	O	MAB08	AC10	IO	MECC7 / CKE7	**Y06**	**P**	**VCCM**
E21	IO	D02#	W02	O	DQM6 / CKE6	**G04**	**P**	**GND**	AD25	O	MAB09	**V06**	**P**	**MVREF**	**AA07**	**P**	**VCCM**
B21	IO	D03#	U02	O	DQM7 / CKE7	**H25**	**P**	**GND**	AB07	O	MAB10	**AA19**	**P**	**MVREF**	**AA09**	**P**	**VCCM**
D22	IO	D04#	AB11	O	DQM8	**J05**	**P**	**GND**	AC04	O	MAB11	E14	I	PROCRDY	**AA12**	**P**	**VCCM**
C20	IO	D05#	AA26	O	DQS0# / CKE0	**J06**	**P**	**GND**	AB05	O	MAB12	P03	I	PWROK	**AA14**	**P**	**VCCM**
C22	IO	D06#	AF23	O	DQS1# / CKE1	**L21**	**P**	**GND**	AC25	O	MAB13	P04	I	RESET#	**AA15**	**P**	**VCCM**
C21	IO	D07#	AD19	O	DQS2# / CKE2	**L22**	**P**	**GND**	Y22	O	MAB14	G22	I	S2KCOMP	**AA17**	**P**	**VCCM**
B20	IO	D08#	AE15	O	DQS3# / CKE3	**L25**	**P**	**GND**	V22	O	MCLK	**F22**	**P**	**S2KGND**	**AA20**	**P**	**VCCM**
B18	IO	D09#	AD08	O	DQS4# / CKE4	**M03**	**P**	**GND**	V21	I	MCLKFB	**G21**	**P**	**S2KVCC**	**AB09**	**P**	**VCCM**
A19	IO	D10#	AC03	O	DQS5# / CKE5	**M04**	**P**	**GND**	W23	IO	MD00	**F16**	**P**	**S2KVREF**	**AB12**	**P**	**VCCM**
A18	IO	D11#	W01	O	DQS6# / CKE6	**P02**	**P**	**GND**	AA25	IO	MD01	**T21**	**P**	**S2KVREF**	**AB17**	**P**	**VCCM**
A20	IO	D12#	U03	O	DQS7# / CKE7	**P05**	**P**	**GND**	AA23	IO	MD02	**H22**	**P**	**S2KVTT**	**AB20**	**P**	**VCCM**
E20	IO	D13#	AF11	O	DQS8#	**P06**	**P**	**GND**	AD26	IO	MD03	A13	I	SBA0	**AE26**	**P**	**VCCM**
E19	IO	D14#	AD09	I	DQSFB	**P21**	**P**	**GND**	Y26	IO	MD04	B13	I	SBA1	**AF01**	**P**	**VCCM**
A22	IO	D15#	D03	IO	GBE0#	**P25**	**P**	**GND**	Y25	IO	MD05	D13	I	SBA2	**AF02**	**P**	**VCCM**
C23	IO	D16#	B02	IO	GBE1#	**T03**	**P**	**GND**	AB26	IO	MD06	D12	I	SBA3	**AF07**	**P**	**VCCM**
A23	IO	D17#	B03	IO	GBE2#	**T04**	**P**	**GND**	AC26	IO	MD07	B11	I	SBA4	**AF13**	**P**	**VCCM**
A24	IO	D18#	B07	IO	GBE3#	**U25**	**P**	**GND**	AF25	IO	MD08	C11	I	SBA5	**AF16**	**P**	**VCCM**
E23	IO	D19#	G03	I	GCLK	**V23**	**P**	**GND**	AE24	IO	MD09	E11	I	SBA6	**AF20**	**P**	**VCCM**
E24	IO	D20#	J02	I	GCOMP	**W06**	**P**	**GND**	AE22	IO	MD10	A11	I	SBA7	**AF26**	**P**	**VCCM**
C25	IO	D21#	H03	IO	GD0	**Y03**	**P**	**GND**	AE21	IO	MD11	B12	I	SBS	**H05**	**P**	**VCCQ**
D24	IO	D22#	H01	IO	GD1	**Y04**	**P**	**GND**	AF24	IO	MD12	A12	I	SBS#	**N1**	**P**	**VCCVK**
C26	IO	D23#	H04	IO	GD2	**Y21**	**P**	**GND**	AD23	IO	MD13	AE03	O	SCASA#	**M01**	**P**	**VCCVL**
B23	IO	D24#	H02	IO	GD3	**Y24**	**P**	**GND**	AD22	IO	MD14	AF04	O	SCASB#	**M02**	**P**	**VCCVL**
C24	IO	D25#	F02	IO	GD4	**AA06**	**P**	**GND**	AF22	IO	MD15	AC06	O	SRASA#	**M05**	**P**	**VCCVL**
E22	IO	D26#	G01	IO	GD5	**AA08**	**P**	**GND**	AB19	IO	MD16	AE06	O	SRASB#	**M06**	**P**	**VCCVL**
B24	IO	D27#	F03	IO	GD6	**AA11**	**P**	**GND**	AC19	IO	MD17	D09	O	ST0	**N06**	**P**	**VCCVL**
A25	IO	D28#	F01	IO	GD7	**AA13**	**P**	**GND**	AC18	IO	MD18	E13	O	ST1	J01	I	VID
A26	IO	D29#	D01	IO	GD8	**AA16**	**P**	**GND**	AF18	IO	MD19	D10	O	ST2	P01	I	VLCOMP
E26	IO	D30#	F05	IO	GD9	**AA21**	**P**	**GND**	AF21	IO	MD20	R05	I	SUSST#	**K05**	**P**	**VLVREF**
D25	IO	D31#	E04	IO	GD10	**AB23**	**P**	**GND**	AF19	IO	MD21	AF05	O	SWEA#	L04	IO	VPAR
F23	IO	D32#	C01	IO	GD11	**AB25**	**P**	**GND**	AD18	IO	MD22	AD06	O	SWEB#	**R04**	**P**	**VSUS25**

Center **VCC25** Pins (16 pins): **J11-12,15-16,L9,18,M9,18,R9,18,T9,18,V11-12,15-16**
Center **GND** Pins (36 pins): **L11-16,M11-16,N11-16,P11-16,R11-16,T11-16**
Center **VCCH** (6 pins): **J14, 17-18,K18,N18,P18**
Center **VCCM** (9 pins): **P9,U9,18,V9-10,13-14,17-18**
Center **VCCAGP** (4 pins): **J9-10,13,K9**
Center **VCCVL** (1 pin): **N9**

PIN DESCRIPTIONS

Table 3. VT8366A North Bridge Pin Descriptions

CPU Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
CFWDRST	C14	O	**CLK Forward Reset.** Reset the CLK forward circuitry for the Athlon™ interface.
CONNECT	C15	O	**Connect.** Used for power management and CLK-forward initialization at reset.
PROCRDY	E14	I	**Processor Ready.** Used for power management and CLK-forward initialization at reset.
AIN[14-2]#	(see pin list)	O	**Host CPU Address / Command Output.** Unidirectional system address / command interface to the processor from the system controller. It is used to transfer probes or data movement commands into the processor during PCI-to-DRAM cycles to snoop the CPU internal Cache. AIN[14:2]# is skew-aligned with the forward clock, AINCLK#
AINCLK#	E17	O	**Host CPU Address Output Clock.** Single-ended forwarded clock for the AIN[14:2]# bus that is driven by the system controller. Both rising and falling edges are used to transfer addresses or commands to the processor.
AOUT[14-2]#	(see pin list)	I	**Host CPU Address Input.** Unidirectional system address / command interface from the processor to the system controller. It is used to transfer processor commands or probes responses to the system controller. AOUT[14:2]# is skew-aligned with the forward clock, AOUTCLK#
AOUTCLK#	T26	I	**Host CPU Address Input Clock.** Single-ended forwarded clock for the AOUT[14:2]# bus that is driven by the processor. Both rising and falling edges are used to transfer commands or probe responses.
D[63-0]#	(see pin list)	IO	**Host CPU Data.** Bi-directional interface between the processor and the system controller for data movement. D[63:0]# bus is skew-aligned with either the DICLK[3:0]# or DOCLK[3:0]# forward clocks.
DICLK[3-0]#	M23, F24, B26, D19	O	**Host CPU Data Input Clock.** Single-ended forwarded clocks for the D[63:0]# bus, driven by the system controller to the processor. Each 16-bit data word is skew-aligned with one of these clocks. Both rising and falling edges are used to transfer data to the pocessor.
DOCLK[3-0]#	N26, G26, D26, C19	I	**Host CPU Data Output Clock.** Single-ended forwarded clocks for the D[63:0]# bus, driven by the processor to the system controller. Each 16-bit data word is skew-aligned with one of these clocks. Both rising and falling edges are used to transfer data to the system controller.
DINVAL#	E16	O	**Host CPU Data Read In Valid.** Driven by the system controller to control the flow of data into the processor. DINVAL# can be used to introduce an arbitrary number of cycles between octawords into the processor.

The pinouts were defined assuming the ATX PCB layout model shown below (and general pin layout shown) as a guide for PCB component placement. Other PCB layouts (AT, LPX, and NLX) were also considered and can typically follow the same general component placement.

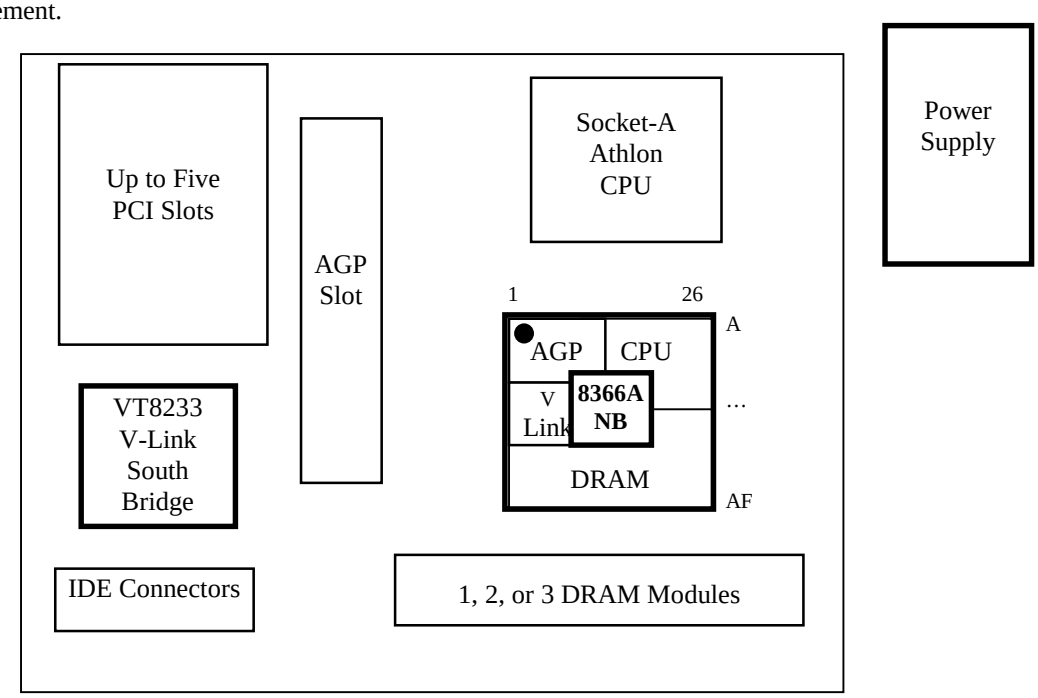

Figure 3. Apollo KT266A Chipset PCB Layout Component Placement Guide

DRAM Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
MD[63:0]	(See Pin List)	IO	**Memory Data.** These signals are connected to the DRAM data bus.
MECC[7:0] / CKE[7:0]	AC10, AE10, AD12, AC12, AF10, AD10, AF12, AE12	IO	**DRAM ECC or EC Data:** when ECC is enabled. **Clock Enables:** For each DRAM bank for powering down the SDRAMs in notebook applications. Also used in desktop systems for clock control to reduce power usage and for reducing heat / temperature in high-speed memory systems.
MAA[14:0]	(See Pin List)	O	**Memory Address A.** DRAM address lines (two sets for better drive)
MAB[14-0]	(See Pin List)	O	**Memory Address B.** DRAM address lines (two sets for better drive).
CS[7:0]#	Y5, AA5, AD5, AE4, AE1, AE2, AD4, AF3	O	**Memory Chip Select.** Chip select of each bank.
DQM8, **DQM7** / CKE7, **DQM6** / CKE6, **DQM5** / CKE5, **DQM4** / CKE4, **DQM3** / CKE3, **DQM2** / CKE2, **DQM1** / CKE1, **DQM0** / CKE0	AB11, U2, W2, AB2, AE7, AF15, AE19, AC22, AA24	O	**Memory Data Mask:** Data mask of each byte lane. DQM8 is used for the ECC bit.
SRASA#, SRASB#	AC6, AE6	O	**Row Address Command Indicator.** (two pins for better drive)
SCASA#, **SCASB#**	AE3, AF4	O	**Column Address Command Indicator.** (2 pins for better drive)
SWEA#, **SWEB#**	AF5, AD6	O	**Write Enable Command Indicator.** (two pins for better drive)
DQS[8]#, **DQS[7:0]#** / CKE[7:0]	AF11, U3, W1, AC3, AD8, AE15, AD19, AF23, AA26	IO	**DDR Data Strobe.** DQS[8]# for ECC bit.
DQSFB	AD9	I	**DDR Data Strobe Feedback.** Connect to ground through a 1K ohm resistor. See also KT266A Design Guide.

V-Link Interface

Signal Name	Pin #	I/O	Signal Description
VAD7, **VAD6** / strap**,** **VAD5** / strap, **VAD4** / strap, **VAD3** / strap, **VAD2** / strap, **VAD1** / strap, **VAD0** / strap	N3, N2, N4, L5, N5, L6, K6, J4	IO	**Address/Data Bus.** VAD6 strap – CPU DQ Mode VAD5 strap – Strap Source VAD4 strap – CPU FSB Clock Speed VAD3 strap – CPU Clock Divide Bit-3 VAD2 strap – CPU Clock Divide Bit-2 VAD1 strap – CPU Clock Divide Bit-1 VAD0 strap – CPU Clock Divide Bit-0 The VAD pins are used by the KT266A chipset to communicate strap information to the VT8366A north bridge from the VT8233 south bridge at system power up (i.e., the actual straps are on the indicated pin of the south bridge chip) Connection: 0=Center DQ, 1=Edge DQ; 0=MA, SCASA, SWEA, 1=ROM; 0=100 MHz (default), 1=133 MHz; (see Device 0 Rx97[6]); (see Device 0 Rx97[5]); (see Device 0 Rx97[4]); (see Device 0 Rx97[3]) VT8233 Strap Pin: SDA2; SDA1; SDA0; SA19; SA18; SA17; SA16
VPAR	L4	IO	**Parity.**
VBE#	K4	IO	**Byte Enable.**
UPCMD	K3	I	**Command from Client-to-Host.**
UPSTB	K1	I	**Strobe from Client-to-Host.**
UPSTB#	K2	I	**Complement Strobe from Client-to-Host.**
DNCMD	L1	O	**Command from Host-to-Client.**
DNSTB	L2	O	**Strobe from Host-to-Client.**
DNSTB#	L3	O	**Complement Strobe from Host-to-Client.**

AGP Bus Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
GD[31:0]	(see pinout tables)	IO	**Address/Data Bus.** The standard AGP/PCI address and data lines. The address is driven with GDS0# and GDS1# assertion for AGP transfers and is driven with GFRM# assertion for PCI transfers.
GDS0	F4	IO	**Bus Strobe 0 (AGP transactions only).** Provides timing for 2x data transfer mode on AD[15:0]. The agent that is providing the data drives this signal.
GDS0#	E3	IO	**Bus Strobe 0 complement and Bus Strobe 0 (AGP transactions only).** Provides timing for 4x data transfer mode on AD[15:0]. The agent that is providing the data drives this signal.
GDS1	E8	IO	**Bus Strobe 1 (AGP transactions only).** Provides timing for 2x data transfer mode on AD[31:16]. The agent that is providing the data drives this signal.
GDS1#	F8	IO	**Bus Strobe 1 complement and Bus Strobe 1 (AGP transactions only).** Provides timing for 4x data transfer mode on AD[31:16]. The agent that is providing the data drives this signal.
GBE[3:0]#	B7, B3, B2, D3	IO	**Command/Byte Enable.** **AGP:** These pins provide command information (different commands than for PCI) driven by the master (graphics controller) when requests are being enqueued using PIPE#. These pins provide valid byte information during AGP write transactions and are driven by the master. The target (this chip) drives these lines to "0000" during the return of AGP read data, but the state of these pins is ignored by the AGP master. **PCI:** Commands are driven with GFRM# assertion. Byte enables corresponding to supplied or requested data are driven on following clocks.
GFRM#	E7	IO	**Frame (PCI transactions only).** Assertion indicates the address phase of a PCI transfer. Negation indicates that one more data transfer is desired by the cycle initiator.
GIRDY#	F11	IO	**Initiator Ready** **AGP:** For write operations, the assertion of this pin indicates that the master is ready to provide *all* write data for the current transaction. Once this pin is asserted, the master is not allowed to insert wait states. For read operations, the assertion of this pin indicates that the master is ready to transfer a subsequent block of read data. The master is *never* allowed to insert a wait state during the initial block of a read transaction. However, it may insert wait states after each block transfers. **PCI:** Asserted when the initiator is ready for data transfer.
GTRDY#	E6	IO	**Target Ready:** **AGP:** Indicates that the target is ready to provide read data for the entire transaction (when the transaction can complete within four clocks) or is ready to transfer a (initial or subsequent) block of data when the transfer requires more than four clocks to complete. The target is allowed to insert wait states after each block transfers on both read and write transactions. **PCI:** Asserted when the target is ready for data transfer.
GSTOP#	E5	IO	**Stop (PCI transactions only).** Asserted by the target to request the master to stop the current transaction.
GDEVSEL#	D7	IO	**Device Select (PCI transactions only).** This signal is driven by the VT8366A when a PCI initiator is attempting to access main memory. It is an input when the VT8366A is acting as PCI initiator. Not used for AGP cycles.

Note: Clocking of the AGP interface is performed with GCLK; see the clock pin group for descriptions of the clock pins.

Note: PCB Layout Guidelines (reference from AGP specification)

1. Total motherboard trace length 10" max, trace impedance = 65 ohms ± 15 ohms, minimize signal crosstalk
2. Trace lengths within groups matched to within 2 inches or better. Group a: GDS0#, GDS0, GD15-0, GBE1-0#
   Group b. GDS1#, GDS1, GD31-16, GBE3-2#
   Group c. SBS#, SBS, SBA7-0
3. Ground isolation should be provided around GDS0#, GDS0, GDS1# and GDS1 to prevent crosstalk with GD[31:0]. Ideally ground traces should be provided adjacent to GDSn# on the same signal layer, but at a minimum wider spaces should be provided on either side (e.g., 16 mil spaces on either side of GDSn# if GDSn# signal traces are 8 mil).

AGP Bus Interface (continued)

Signal Name	Pin #	IO	Signal Description
GPIPE#	D11	I	**Pipelined Request.** Asserted by the master (graphics controller) to indicate that a full-width request is to be enqueued by the target VT8366A. The master enqueues one request each rising edge of GCLK while GPIPE# is asserted. When GPIPE# is deasserted no new requests are enqueued across the AD bus.
GRBF#	C10	I	**Read Buffer Full.** Indicates if the master (graphics controller) is ready to accept previously requested low priority read data. When GRBF# is asserted, the VT8366A will not return low priority read data to the master.
GWBF#	E9	I	**Write Buffer Full.**
SBA[7:0]	A11, E11, C11, B11, D12, D13, B13, A13	I	**SideBand Address.** Provides an additional bus to pass address and command information from the master (graphics controller) to the target (the VT8366A). These pins are ignored until enabled.
SBS	B12	I	**Sideband Strobe.** Provides timing for SBA[7:0] (driven by the master)
SBS#	A12	I	**Sideband Strobe complement and SBS .** Provides timing for SBA[7:0] (driven by the master) when 4x timing is supported.
ST[2:0]	D10, E13, D9	O	**Status (AGP only).** Provides information from the arbiter to a master to indicate what it may do. Only valid while GGNT# is asserted. 000 Indicates that previously requested low priority read or flush data is being returned to the master (graphics controller). 001 Indicates that previously requested high priority read data is being returned to the master. 010 Indicates that the master is to provide low priority write data for a previously enqueued write command. 011 Indicates that the master is to provide high priority write data for a previously enqueued write command. 100 Reserved. (arbiter must not issue, may be defined in the future). 101 Reserved. (arbiter must not issue, may be defined in the future). 110 Reserved. (arbiter must not issue, may be defined in the future). 111 Indicates that the master (graphics controller) has been given permission to start a bus transaction. The master may enqueue AGP requests by asserting PIPE# or start a PCI transaction by asserting GFRM#. ST[2:0] are always outputs from the VT8366A and inputs to the master.
GREQ#	D14	I	**Request.** Master request for AGP.
GGNT#	C13	O	**Grant.** Permission is given to the master to use AGP.
GPAR / GCKRUN#	G5	IO	Rx78[1]=0: **AGP Parity.** A single parity bit is provided over GD[31:0] and GBE[3:0]. Rx78[1]=1: **AGP Clock Run.** Used to stop the AGP bus clock to reduce bus power usage.
GCLK	G3	I	**AGP Clock.**

Note: For PCI operation on the AGP bus, the following pins are not required:
- PERR# (parity and error reporting not required on transient data devices such as graphics controllers)
- LOCK# (no lock requirement on AGP)
- IDSEL (internally connected to AD16 on AGP-compliant masters)

Note: Separate system interrupts are not provided for AGP. The AGP connector provides interrupts via PCI bus INTA-B#.

Note: The AGP bus supports only one master directly (REQ[3:0]# and GNT[3:0]# are not provided). External logic is required to implement additional master capability. Note that the arbitration mechanism on the AGP bus is different from the PCI bus.

Note: A separate reset is not required for the AGP bus (RESET# resets both PCI and AGP buses)

Note: Two mechanisms are provided by the AGP bus to enqueue master requests: GPIPE# (to send addresses multiplexed on the AD lines) and the SBA port (to send addresses unmultiplexed). AGP masters implement one or the other or select one at initialization time (they are not allowed to change during runtime). Therefore only one of the two will be used and the signals associated with the other will not be used. Therefore the VT8366A has an internal pullup on GRBF# to maintain it in the de-asserted state in case it is not implemented on the master device.

Test Functions			
Signal Name	**Pin #**	**I/O**	**Signal Description**
TESTIN#	W24	I	**PLL Test Input.** Normally connected to VCC25 with a 4.7K pullup.

Clock / Reset Control			
Signal Name	**Pin #**	**I/O**	**Signal Description**
HCLK	H21	I	**Host Clock.** This pin receives the host CPU clock (66 / 100 / 133 MHz). This clock is used by all VT8366A logic that is in the host CPU domain. The memory interface logic will also use this clock if selected (memory system timing can alternately be selected to use the AGP bus clock). The CPU clock must lead the AGP clock by 0.2 ± 0.5 nsec.
HCLK#	J21	I	**Host Clock Complement.**
GCLK	G3	I	**AGP Clock.** 66 MHz clock used by all VT8366A logic that is in the AGP clock domain. The AGP clock must be synchronous to the 200 MHz host CPU clock.
MCLK	V22	O	**DRAM Clock.** Output from internal clock generator to the external clock buffer.
MCLKFB	V21	I	**DRAM Clock Feedback.** Input from MCLK via the external clock buffer.
RESET#	P4	I	**Reset.** Input from south bridge chip. When asserted, this signal resets the VT8366A and sets all register bits to the default value. The rising edge of this signal is used to sample all power-up strap options
PWROK	P3	I	**Power OK.**
SUSST#	R5	I	**Suspend Status.** For implementation of the Suspend-to-DRAM feature. Connect to an external pullup to disable.

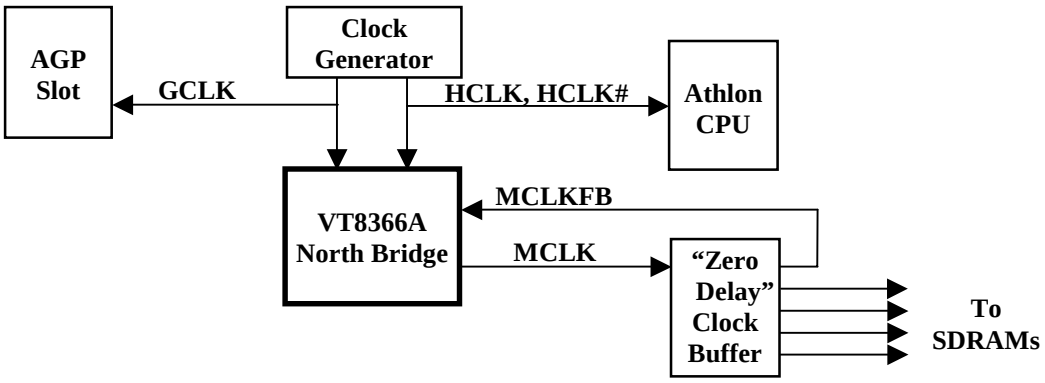

Figure 4. VT8366A North Bridge Clock Distribution

Figure 5. CPU / SDRAM / AGP Clock Connections

Power, Ground, and Test

Signal Name	Pin #	I/O	Signal Description
VCC25	(see pin list)	P	**Power** for **Internal Logic** and **I/O Interface Logic** (2.5V ±5%).
VSUS25	R4	P	**Suspend Power** (2.5V ±5%).
GND	(see pin list)	P	**Ground.** Connect to main ground plane.
VCCH	D15, D18, D21, D23, F19, G23, K21, K23, N23, R21, T23	P	**Host CPU Interface Power.** Connect to same voltage as S2KVTT. Voltage is CPU dependent. See KT266A Design Guide for recommended power circuit.
S2KVTT	H22	P	**S2K Bus Termination Voltage.** Connect to same voltage as VCCH. Voltage is CPU dependent. See KT266A Design Guide for recommended power circuit.
S2KVREF	F16, T21	P	**S2K Bus Voltage Reference.** ½ S2KVTT derived using 100 Ω 1% + 100 Ω 1% resistive voltage divider. See KT266A Design Guide.
S2KVCC	G21	P	**S2K Bus Interface Power.** (2.5V ±5%)
S2KGND	F22	P	**S2K Bus Ground.** Connect to main ground plane.
S2KCOMP	G22	I	**S2K Bus Compensation.** Connect to 70 Ω 1% resistor to ground.
VCCM	(see pin list)	P	**Memory Interface Power.** (2.5V ±5%)
MVREF	V6, AA19	P	**DDR SDRAM Voltage Reference.** ½ VCC25 derived using a 1K Ω 1% + 1K Ω 1% resistive voltage divider. See KT266A Design Guide.
VCCVL	M1-2, M5-6, N6, N9	P	**V-Link Interface Power.** (2.5V ±5%)
VCCVK	N1	P	**V-Link Compensation Circuit Power.** (2.5V ±5%)
VLVREF	K5	P	**V-Link Reference Voltage.** 0.9V derived using a resistive voltage divider consisting of 2K Ω 1% to VCC25 and 1.13K Ω 1% to ground.
VLCOMP	P1	I	**V-Link P-Channel Compensation.** Connect 70Ω 1% resistor to ground.
VCCAGP	A1-A2, A6, A10, A14, B6, B10, B14, E1-E2, E12, F12, G6, H6, J9-J10, J13, K9	P	**AGP Interface Power.** 1.5V(4x mode) / 3.3V (1x and 2x mode) ±5%
VCCQ	H5	P	**AGP Quiet Power.** 1.5V(4x mode) / 3.3V (1x and 2x mode) ±5%
GNDQ	J3	P	**AGP Quiet Ground.** Connect to main ground plane.
AGPVREF	A5	P	**AGP Voltage Reference.** 0.39 VCC3 to 0.41 VCC3. Typical value is 1.32V (0.40 times 3.3V). This can be provided with a resistive divider (150 Ω 1% to VCCQ and 100 Ω 1% to ground). See KT266A Design Guide.
GCOMP	J2	I	**AGP Compensation.** Connect to 60Ω 1% resistor to VCCQ.
VID	J1	I	**Voltage ID.** CPU FSB interface voltage select. 0 = desktop, 1 = mobile.
AVCCHCK	K22	P	**Host CPU Clock Power** (2.5V ±5%). For internal Host CPU clock logic. Connect to main 2.5V supply through a ferrite bead.
AGNDHCK	J22	P	**Host CPU Clock Ground.** Connect to main ground plane through a ferrite bead.
AVCCMCK	U21	P	**DRAM Clock Power** (2.5V ±5%). For internal DRAM clock deskew logic. Connect to main 2.5V supply through a ferrite bead.
AGNDMCK	U22	P	**DRAM Clock Ground.** Connect to main ground plane through a ferrite bead.
AVCCDL1	AA18	P	**Internal Delay Circuit Power** (2.5V ±5%). Connect to main 2.5V supply through a ferrite bead.
AGNDDL1	AB18	P	**Internal Delay Circuit Ground.** Connect to main ground plane.
AVCCDL2	W5	P	**Internal Delay Circuit Power** (2.5V ±5%). Connect to main 2.5V supply through a ferrite bead.
AGNDDL2	W4	P	**Internal Delay Circuit Ground.** Connect to main ground plane.

REGISTERS

Register Overview

The following tables summarize the configuration and I/O registers of the VT8366A North Bridge chip of the Apollo KT266A chipset (refer to the separate VT8233 data sheet for the register definitions of the South Bridge chip). These tables also document the power-on default value ("Default") and access type ("Acc") for each register. Access type definitions used are RW (Read/Write), RO (Read/Only), "—" for reserved / used (essentially the same as RO), and RWC (or just WC) (Read / Write 1's to Clear individual bits). Registers indicated as RW may have some read/only bits that always read back a fixed value (usually 0 if unused); registers designated as RWC or WC may have some read-only or read write bits (see individual register descriptions following these tables for details). All offset and default values are shown in hexadecimal unless otherwise indicated.

Table 4. VT8366A North Bridge Registers

VT8366A I/O Ports

Port #	I/O Port	Default	Acc
22	PCI / AGP Arbiter Disable	00	RW
CFB-8	Configuration Address	0000 0000	RW
CFF-C	Configuration Data	0000 0000	RW

VT8366A Device 0 Registers - Host Bridge

Header Registers

Offset	Configuration Space Header	Default	Acc
1-0	Vendor ID	**1106**	RO
3-2	Device ID	**3099**	RO
5-4	Command	**0006**	**RW**
7-6	Status	**0210**	**WC**
8	Revision ID	**0n**	RO
9	Program Interface	00	RO
A	Sub Class Code	00	RO
B	Base Class Code	**06**	RO
C	-reserved-	00	—
D	Latency Timer	00	**RW**
E	Header Type	00	RO
F	Built In Self Test (BIST)	00	RO
13-10	Graphics Aperture Base	**0000 0008**	**RW**
14-2B	-reserved-	00	—
2D-2C	Subsystem Vendor ID	0000	**W1**
2F-2E	Subsystem ID	0000	**W1**
30-33	-reserved-	00	—
37-34	Capability Pointer	**0000 00A0**	RO
38-3F	-reserved-	00	—

Device-Specific Registers

Offset	V-Link Control	Default	Acc
40	V-Link Revision ID	00	**RO**
41	V-Link NB Capability	**18**	**RO**
42	V-Link NB Downlink Command	**88**	RW
44-43	V-Link NB Uplink Status	**8280**	**RO**
45	V-Link NB Bus Timer	**44**	RW
46	V-Link Misc NB Control	00	RW
47	V-Link Control	00	RW
48	V-Link NB/SB Configuration	**18**	RW
49	V-Link SB Capability	**18**	**RO**
4A	V-Link SB Downlink Status	**88**	**RO**
4C-4B	V-Link SB Uplink Command	**8280**	RW
4D	V-Link SB Bus Timer	**44**	RW
4E	CCA Master High Priority	00	RW
4F	V-Link SB Miscellaneous Control	00	RW

Offset	CPU Configuration	Default	Acc
50-53	-reserved-	00	—
54	CPU Frequency Select	x0	RW

Device-Specific Registers (continued)

Offset	DRAM Control	Default	Acc
55	DRAM Control	00	RW
56-57	(see below)		
59-58	MA Map Type	**2222**	RW
5F-5A	DRAM Row Ending Address:		
5A	Bank 0 Ending (HA[31:24])	**01**	RW
5B	Bank 1 Ending (HA[31:24])	**01**	RW
5C	Bank 2 Ending (HA[31:24])	**01**	RW
5D	Bank 3 Ending (HA[31:24])	**01**	RW
5E	Bank 4 Ending (HA[31:24])	**01**	RW
5F	Bank 5 Ending (HA[31:24])	**01**	RW
56	Bank 6 Ending (HA[31:24])	**01**	RW
57	Bank 7 Ending (HA[31:24])	**01**	RW
60	DRAM Type	00	RW
61	ROM Shadow Control C0000-CFFFF	00	RW
62	ROM Shadow Control D0000-DFFFF	00	RW
63	ROM Shadow Control E0000-FFFFF	00	RW
64	DRAM Timing for All Banks	**E4**	RW
65	DRAM Arbitration Timer	00	RW
66	DRAM Arbitration Control	**40**	RW
67	DRAM DQS/SDR/MD Read Delay	00	RW
68	DRAM DDR Control	00	RW
69	Extended SMRAM Control	00	RW
6A	DRAM Refresh Counter	00	RW
6B	DRAM Arbitration Control	**10**	RW
6C	SDRAM Control	00	RW
6D	DRAM Control Drive Strength	00	RW
6E	ECC Control	00	RW
6F	ECC Status	00	**RO**

Offset	PCI Bus Control	Default	Acc
70	PCI Buffer Control	00	RW
71	CPU to PCI Flow Control	**48**	RW
72	-reserved-	00	—
73	PCI Master Control	00	RW
74	-reserved-	00	—
75	PCI Arbitration 1	00	RW
76	PCI Arbitration 2	00	RW
77-7F	-reserved-	00	—

Offset	GART/TLB Control	Default	Acc
83-80	GART/TLB Control	0000 0000	RW
84	Graphics Aperture Size	00	RW
85-87	-reserved-	00	—
8B-88	Gr. Aperture TLB Base Register Base	0000 0000	RW
8C-8F	-reserved-	00	—

Offset	Host CPU Control	Default	Acc
90-91	-reserved-	00	—
92	S2K Timing Control	**78**	RW
93	BIU Arbitration Control	00	RW
94	BIU Control 1	00	RW
95	BIU Control 2	00	RW
96	BIU Control 3	00	RW
97	CPU Strapping	**strapping**	**RO**
98	S2K Compensation Strapping	00	RW
99	S2K Compensation Result 1	00	**RO**
9A	S2K Compensation Result 2	00	RW
9B	S2K Compensation Result 3	00	**RO**
9C	S2K Compensation Result 4	**07**	RW
9D	S2K Compensation Result 5	00	RW
9E	BIU Control 4	00	RW
9F	-reserved-	00	—

Offset	AGP Control	Default	Acc
A0	AGP ID	**02**	**RO**
A1	AGP Next Item Pointer	**C0**	**RO**
A2	AGP Specification Revision	**20**	**RO**
A3	-reserved-	00	—
A7-A4	AGP Status	**1F00 0201**	**RO**
AB-A8	AGP Command	0000 0000	RW
AC	AGP Control	00	RW
AD	AGP Latency Timer	**02**	RW
AE	AGP Miscellaneous Control	00	RW
AF	AGP Strobe Output Drive Strength	00	RW
B0	AGP Pad Control / Status	**8x**	RW
B1	AGP Drive Strength	**63**	RW
B2	AGP Pad Drive / Delay Control	**08**	RW
B3	-reserved-	00	—

Offset	V-Link Control	Default	Acc
B4	V-Link NB Compensation Control	00	RW
B5	V-Link NB Drive Control	00	RW
B6-B7	-reserved-	00	—
B8	V-Link SB Compensation Control	00	RW
B9	V-Link SB Drive Control	00	RW
BA-BD	-reserved-	00	—

Offset	DRAM Power Control	Default	Acc
BE	MPD Drive Strength	00	RW
BF	MA / SCMD Pad Toggle Reduction	00	RW

Offset	Extended Power Management	Default	Acc
C0	Power Management Capability ID	**01**	**RO**
C1	Power Management New Pointer	00	**RO**
C2	Power Management Capabilities I	**02**	**RO**
C3	Power Management Capabilities II	00	**RO**
C4	Power Management Control / Status	00	RW
C5	Power Management Status	00	RW
C6	PCI-to-PCI Bridge Support Extension	00	RW
C7	Power Management Data	00	RW
C8-DF	-reserved-	00	—

Offset	Reserved	Default	Acc
E0-EF	-reserved-	00	—
F0-F7	-reserved- (test)	00	—
F8-FF	-reserved- (backdoor)	00	—

VT8366A Device 1 - PCI-to-PCI Bridge

Header Registers

Offset	Configuration Space Header	Default	Acc
1-0	Vendor ID	**1106**	RO
3-2	Device ID	**B099**	RO
5-4	Command	**0007**	**RW**
7-6	Status	**0230**	**WC**
8	Revision ID	**nn**	RO
9	Program Interface	00	RO
A	Sub Class Code	**04**	RO
B	Base Class Code	**06**	RO
C	-reserved-	00	—
D	Latency Timer	00	**RW**
E	Header Type	**01**	RO
F	Built In Self Test (BIST)	00	RO
10-17	-reserved-	00	—
18	Primary Bus Number	00	**RW**
19	Secondary Bus Number	00	**RW**
1A	Subordinate Bus Number	00	**RW**
1B	Secondary Latency Timer	00	RO
1C	I/O Base	**F0**	**RW**
1D	I/O Limit	00	**RW**
1F-1E	Secondary Status	0000	RO
21-20	Memory Base	**FFF0**	**RW**
23-22	Memory Limit (Inclusive)	0000	**RW**
25-24	Prefetchable Memory Base	**FFF0**	**RW**
27-26	Prefetchable Memory Limit	0000	**RW**
28-2B	-reserved-	00	—
2D-2C	Subsystem Vendor ID	0000	**W1**
2F-2E	Subsystem ID	0000	**W1**
30-33	-reserved-	00	—
34	Capability Pointer	**80**	RO
35-3D	-reserved-	00	—
3F-3E	PCI-to-PCI Bridge Control	00	**RW**

Device-Specific Registers

Offset	AGP Bus Control	Default	Acc
40	CPU-to-AGP Flow Control 1	00	RW
41	CPU-to-AGP Flow Control 2	00	RW
42	AGP Master Control	00	RW
43	AGP Master Latency Timer	**22**	RW
44	Back-Door Register Control	**20**	RW
45	Fast Write Control	**72**	RW
47-46	PCI-to-PCI Bridge Device ID	0000	RW
48-7F	-reserved-	00	—
80	Capability ID	**01**	**RO**
81	Next Pointer	00	**RO**
82	Power Management Capabilities 1	**02**	**RO**
83	Power Management Capabilities 2	00	**RO**
84	Power Management Control / Status	00	RW
85	Power Management Status	00	**RO**
86	PCI-PCI Bridge Support Extensions	00	**RO**
87	Power Management Data	00	**RO**
88-FF	-reserved-	00	—

Miscellaneous I/O

One I/O port is defined in the VT8366A: Port 22.

Port 22 – PCI / AGP Arbiter Disable .....RW

7-2 Reserved ..... always reads 0

1 AGP Arbiter Disable
- 0 Respond to GREQ# signal .....default
- 1 Do not respond to GREQ# signal

0 PCI Arbiter Disable
- 0 Respond to all REQ# signals.....default
- 1 Do not respond to any REQ# signals, including PREQ#

This port can be enabled for read/write access by setting bit-7 of Device 0 Configuration Register 76.

Configuration Space I/O

All registers in the VT8366A (listed above) are addressed via the following configuration mechanism:

Mechanism #1

These ports respond only to double-word accesses. Byte or word accesses will be passed on unchanged.

Port CFB-CF8 - Configuration Address..... RW

31 Configuration Space Enable
- 0 Disabled..... default
- 1 Convert configuration data port writes to configuration cycles on the PCI bus

30-24 Reserved .....always reads 0

23-16 PCI Bus Number
Used to choose a specific PCI bus in the system

15-11 Device Number
Used to choose a specific device in the system (devices 0 and 1 are defined for the VT8366A)

10-8 Function Number
Used to choose a specific function if the selected device supports multiple functions (only function 0 is defined for the VT8366A).

7-2 Register Number (also called the "Offset")
Used to select a specific DWORD in the VT8366A configuration space

1-0 Fixed .....always reads 0

Port CFF-CFC - Configuration Data..... RW

Refer to PCI Bus Specification Version 2.1 for further details on operation of the above configuration registers.

Register Descriptions

Device 0 Header Registers - Host Bridge

All registers are located in PCI configuration space. They should be programmed using PCI configuration mechanism 1 through CF8 / CFC with bus number, function number, and device number equal to zero.

Device 0 Offset 1-0 - Vendor ID (1106h) .....RO

15-0 ID Code (reads 1106h to identify VIA Technologies)

Device 0 Offset 3-2 - Device ID (3099h).....RO

15-0 ID Code (reads 3099h to identify the VT8366A)

Device 0 Offset 5-4 –Command (0006h) .....RW

15-10 Reserved ..... always reads 0

9 Fast Back-to-Back Cycle Enable ..... RO
- 0 Fast back-to-back transactions only allowed to the same agent .....default
- 1 Fast back-to-back transactions allowed to different agents

8 SERR# Enable..... RO
- 0 SERR# driver disabled.....default
- 1 SERR# driver enabled

(SERR# is used to report parity errors if bit-6 is set).

7 Address / Data Stepping ..... RO
- 0 Device never does stepping.....default
- 1 Device always does stepping

6 Parity Error Response.....**RW**
- 0 Ignore parity errors & continue .....default
- 1 Take normal action on detected parity errors

5 VGA Palette Snoop ..... RO
- 0 Treat palette accesses normally .....default
- 1 Don't respond to palette accesses on PCI bus

4 Memory Write and Invalidate Command..... RO
- 0 Bus masters must use Mem Write .....default
- 1 Bus masters may generate Mem Write & Inval

3 Special Cycle Monitoring ..... RO
- 0 Does not monitor special cycles .....default
- 1 Monitors special cycles

2 PCI Bus Master..... RO
- 0 Never behaves as a bus master
- 1 Can behave as a bus master .....default

1 Memory Space..... RO
- 0 Does not respond to memory space
- 1 Responds to memory space .....default

0 I/O Space ..... RO
- 0 Does not respond to I/O space .....default
- 1 Responds to I/O space

Device 0 Offset 7-6 – Status (0210h)..... RWC

15 Detected Parity Error
- 0 No parity error detected..... default
- 1 Error detected in either address or data phase. This bit is set even if error response is disabled (command register bit-6). .....write one to clear

14 Signaled System Error (SERR# Asserted)
..... always reads 0

13 Signaled Master Abort
- 0 No abort received ..... default
- 1 Transaction aborted by the master .....
.....write one to clear

12 Received Target Abort
- 0 No abort received ..... default
- 1 Transaction aborted by the target.....
.....write one to clear

11 Signaled Target Abort..... always reads 0
- 0 Target Abort never signaled

10-9 DEVSEL# Timing
- 00 Fast
- 01 Medium..... always reads 01
- 10 Slow
- 11 Reserved

8 Data Parity Error Detected
- 0 No data parity error detected ..... default
- 1 Error detected in data phase. Set only if error response enabled via command bit-6 = 1 and VT8366A was initiator of the operation in which the error occurred. .....write one to clear

7 Fast Back-to-Back Capable ..... always reads 0

6 User Definable Features..... always reads 0

5 66MHz Capable..... always reads 0

4 Supports New Capability list..... always reads 1

3-0 Reserved ..... always reads 0

Device 0 Offset 8 - Revision ID (0nh) ..... RO

7-0 Chip Revision Code ...always reads 0nh (n=rev code)

Device 0 Offset 9 - Programming Interface (00h) ..... RO

7-0 Interface Identifier ..... always reads 00

Device 0 Offset A - Sub Class Code (00h) ..... RO

7-0 Sub Class Code .....reads 00 to indicate Host Bridge

Device 0 Offset B - Base Class Code (06h)..... RO

7-0 Base Class Code .. reads 06 to indicate Bridge Device

Device 0 Offset D - Latency Timer (00h) ..... RW

Specifies the latency timer value in PCI bus clocks.

7-3 Guaranteed Time Slice for CPU.....default=0

2-0 Reserved (fixed granularity of 8 clks) .. always read 0

Bits 2-1 are writeable but read 0 for PCI specification compatibility. The programmed value may be read back in Offset 75 bits 5-4 (PCI Arbitration 1).

Device 0 Host Bridge Header Registers (continued)

Device 0 Offset E - Header Type (00h).....RO

7-0 Header Type Code .....reads 00: single function

Device 0 Offset F - Built In Self Test (BIST) (00h).....RO

7 BIST Supported .....reads 0: no supported functions

6-0 Reserved ..... always reads 0

Device 0 Offset 13-10 - Graphics Aperture Base (00000008h) .....RW

31-28 Upper Programmable Base Address Bits..... def=0

27-20 Lower Programmable Base Address Bits ..... def=0

These bits behave as if hardwired to 0 if the corresponding Graphics Aperture Size register bit (Device 0 Offset 84h) is 0.

27	26	25	24	23	22	21	20	(This Register)
7	6	5	4	3	2	1	0	(Gr Aper Size)
RW	RW	RW	RW	RW	RW	RW	RW	1M
RW	RW	RW	RW	RW	RW	RW	0	2M
RW	RW	RW	RW	RW	RW	0	0	4M
RW	RW	RW	RW	RW	0	0	0	8M
RW	RW	RW	RW	0	0	0	0	16M
RW	RW	RW	0	0	0	0	0	32M
RW	RW	0	0	0	0	0	0	64M
RW	0	0	0	0	0	0	0	128M
0	0	0	0	0	0	0	0	256M

19-0 Reserved ..... always reads 00008

Note: The locations in the address range defined by this register are prefetchable.

Device 0 Offset 2D-2C – Subsystem Vendor ID (0000h)R/W1

15-0 Subsystem Vendor ID.....default = 0

This register may be written once and is then read only.

Device 0 Offset 2F-2E – Subsystem ID (0000h)..... R/W1

15-0 Subsystem ID .....default = 0

This register may be written once and is then read only.

Device 0 Offset 37-34 - Capability Pointer (000000A0h) RO

Contains an offset from the start of configuration space.

31-0 AGP Capability List Pointer ..... always reads A0h

Device 0 Configuration Registers - Host Bridge

These registers are normally programmed once at system initialization time.

V-Link Control

Device 0 Offset 40 – V-Link Specification ID (00h).....RO

7-0 Specification Revision..... always reads 00

Device 0 Offset 41 – NB V-Link Capability (18h) .....RO

7-6 Reserved ..... always reads 0

5 16-bit Bus Width Supported .....RO
- 0 Not Supported .....default
- 1 Supported

4 8-Bit Bus Width Supported.....RO
- 0 Not Supported
- 1 Supported .....default

3 4x Rate Supported.....RO
- 0 Not Supported
- 1 Supported .....default

2 2x Rate Supported.....RO
- 0 Not Supported .....default
- 1 Supported

1-0 Reserved ..... always reads 0

Device 0 Offset 42 – NB Downlink Command (88h) .....RW

7-4 DnCmd Max Request Depth (0=1 DnCmd).. def = 8

3-0 DnCmd Write Buffer Size (doublewords)..... def = 8

Device 0 Offset 44-43 – NB Uplink Status (8280h).....RO

15-12 UpCmd P2C Write Buffer Size (max lines).. def = 8

11-8 UpCmd P2P Write Buffer Size (max lines)... def = 2

7-4 UpCmd Max Request Depth (0=1 UpCmd).. def = 8

3-0 Reserved ..... always reads 0

Device 0 Offset 45 –NB V-Link Bus Timer (44h)..... RW

7-4 Timer for Normal Priority Requests from SB
- 0000 Immediate
- 0001 1*4 VCLKs
- 0010 2*4 VCLKs
- 0011 3*4 VCLKs
- 0100 4*4 VCLKs..... default
- 0101 5*4 VCLKs
- 0110 6*4 VCLKs
- 0111 7*4 VCLKs
- 1000 8*4 VCLKs
- 1001 16*4 VCLKs
- 1010 32*4 VCLKs
- 1011 64*4 VCLKs
- 11xx Own the bus for as long as there is a request

3-0 Timer for High Priority Requests from SB
- 0000 Immediate
- 0001 1*2 VCLKs
- 0010 2*2 VCLKs
- 0011 3*2 VCLKs
- 0100 4*2 VCLKs..... default
- 0101 5*2 VCLKs
- 0110 6*2 VCLKs
- 0111 7*2 VCLKs
- 1000 8*2 VCLKs
- 1001 16*2 VCLKs
- 1010 32*2 VCLKs
- 1011 64*2 VCLKs
- 11xx Own the bus for as long as there is a request

Device 0 Offset 46 – NB V-Link Misc Control (00h).....RW

7 Downstream High Priority
- 0 Disable High Priority Down Commands ..... def
- 1 Enable High Priority Down Commands

6 Downlink Priority
- 0 Treat Downlink Cycles as Normal Priority def
- 1 Treat Downlink Cycles as High Priority

5-4 Combine Multiple STPGNT Cycles into One V-Link Command
- 00 Compatible, 1 command per V-Link cmd ... def
- 01 2 commands per V-Link command
- 10 3 commands per V-Link command
- 11 4 commands per V-Link command

3-2 V-Link Master Access Ordering Rules
- 00 High priority read, pass normal read (not pass write) .....default
- 01 Read (high/normal) pass write (HR>LR>W)
- 1x Read / write in order

1 Reserved ..... always reads 0

0 Ready Queue Full Performance
- 0 Full Performance .....default
- 1 Backwards Compatible

Device 0 Offset 47 – V-Link Control (00h).....RW

7-3 Reserved ..... always reads 0

2 Auto-Disconnect
- 0 Disable .....default
- 1 Enable

1 V-Link Disconnect Cycle for HALT cycle
- 0 Disable .....default
- 1 Enable

0 V-Link Disconnect Cycle for STPGNT Cycle
- 0 Disable .....default
- 1 Enable

Device 0 Offset 48 – NB/SB V-Link Configuration (18h)RW

7 Reserved .....always reads 0

6 Rest Bus Width Supported
- 0 Not Supported..... default
- 1 Supported

5 16-bit Bus Width Supported
- 0 Not Supported..... default
- 1 Supported

4 8-Bit Bus Width Supported
- 0 Not Supported
- 1 Supported..... default

3 4x Rate Supported
- 0 Not Supported
- 1 Supported..... default

2 2x Rate Supported
- 0 Not Supported..... default
- 1 Supported

1-0 Reserved .....always reads 0

Device 0 Offset 49 – SB V-Link Capability (18h)..... RO

7-6 Reserved .....always reads 0

5 16-bit Bus Width Supported..... RO
- 0 Not Supported..... default
- 1 Supported

4 8-Bit Bus Width Supported ..... RO
- 0 Not Supported
- 1 Supported..... default

3 4x Rate Supported..... RO
- 0 Not Supported
- 1 Supported..... default

2 2x Rate Supported..... RO
- 0 Not Supported..... default
- 1 Supported

1-0 Reserved .....always reads 0

Device 0 Offset 4A – SB Downlink Status (88h)..... RO

7-4 DnCmd Max Request Depth (0=1 DnCmd) ..def = 8

3-0 DnCmd Write Buffer Size (doublewords).....def = 8

Device 0 Offset 4C-4B – SB Uplink Command (8280h). RW

15-12 UpCmd P2C Write Buffer Size (max lines)...def = 8

11-8 UpCmd P2P Write Buffer Size (max lines)...def = 2

7-4 UpCmd Max Request Depth (0=1 UpCmd) ..def = 8

3-0 Reserved .....always reads 0

Device 0 Offset 4D – SB V-Link Bus Timer (44h) .....RW

7-4 Timer for Normal Priority Requests from NB
- 0000 Immediate
- 0001 1*4 VCLKs
- 0010 2*4 VCLKs
- 0011 3*4 VCLKs
- 0100 4*4 VCLKs .....default
- 0101 5*4 VCLKs
- 0110 6*4 VCLKs
- 0111 7*4 VCLKs
- 1000 8*4 VCLKs
- 1001 16*4 VCLKs
- 1010 32*4 VCLKs
- 1011 64*4 VCLKs
- 11xx Own the bus for as long as there is a request

3-0 Timer for High Priority Requests from NB
- 0000 Immediate
- 0001 1*2 VCLKs
- 0010 2*2 VCLKs
- 0011 3*2 VCLKs
- 0100 4*2 VCLKs .....default
- 0101 5*2 VCLKs
- 0110 6*2 VCLKs
- 0111 7*2 VCLKs
- 1000 8*2 VCLKs
- 1001 16*2 VCLKs
- 1010 32*2 VCLKs
- 1011 64*2 VCLKs
- 11xx Own the bus for as long as there is a request

Device 0 Offset 4E – CCA Master Priority (00h)..... RW

7 1394 High Priority
- 0 Low priority..... default
- 1 High priority

6 LAN / NIC High Priority
- 0 Low priority..... default
- 1 High priority

5 Reserved .....always reads 0

4 USB High Priority
- 0 Low priority..... default
- 1 High priority

3 Reserved .....always reads 0

2 IDE High Priority
- 0 Low priority..... default
- 1 High priority

1 AC97-ISA High Priority
- 0 Low priority..... default
- 1 High priority

0 PCI High Priority
- 0 Low priority..... default
- 1 High priority

Device 0 Offset 4F – SB V-Link Misc Control (00h)..... RW

7 Upstream Command High Priority
- 0 Disable high priority up commands ..... default
- 1 Enable high priority up commands

6-1 Reserved .....always reads 0

0 Down Cycle Wait for Up Cycle Write Flush (Except Down Cycle Post Write)
- 0 Disable..... default
- 1 Enable

Device 0 Offset 54 – CPU Frequency Select (x0h) ..... RW

7 Reserved .....always reads 0

6 CPU FSB Frequency SelectRO, Set by Strap VAD4
Default set from the VT8233 South Bridge SDA0 pin communicated to the VT8366A via VAD4
- 0 100 MHz
- 1 133 MHz

5 ROMSIP Configuration....RO, Set by Strap VAD5
- 0 Disable (config per MA / SCASA / SWEA straps)
- 1 Enable (configure per ROMSIP)

4 SDRAM Burst Length 8QW
- 0 Disable..... default
- 1 Enable

3-0 Reserved .....always reads 0

DRAM Control

These registers are normally set at system initialization time and not accessed after that during normal system operation. Some of these registers, however, may need to be programmed using specific sequences during power-up initialization to properly detect the type and size of installed memory (refer to the VIA Technologies VT8633 BIOS porting guide for details).

Table 5. System Memory Map

Space	Start	Size	Address Range	Comment
DOS	0	640K	00000000-0009FFFF	Cacheable
VGA	640K	128K	000A0000-000BFFFF	Used for SMM
BIOS	768K	16K	000C0000-000C3FFF	Shadow Ctrl 1
BIOS	784K	16K	000C4000-000C7FFF	Shadow Ctrl 1
BIOS	800K	16K	000C8000-000CBFFF	Shadow Ctrl 1
BIOS	816K	16K	000CC000-000CFFFF	Shadow Ctrl 1
BIOS	832K	16K	000D0000-000D3FFF	Shadow Ctrl 2
BIOS	848K	16K	000D4000-000D7FFF	Shadow Ctrl 2
BIOS	864K	16K	000D8000-000DBFFF	Shadow Ctrl 2
BIOS	880K	16K	000DC000-000DFFFF	Shadow Ctrl 2
BIOS	896K	64K	000E0000-000EFFFF	Shadow Ctrl 3
BIOS	960K	64K	000F0000-000FFFFF	Shadow Ctrl 3
Sys Bus	1MB D Top	—	00100000-DRAM Top DRAM Top-FFFEFFFF	Can have hole
Init	4G-64K	64K	FFFEFFFF-FFFFFFFF	000Fxxxx alias

Device 0 Offset 55 – DRAM Control (00h)..... RW

7 0WS Back-to-Back Write to Different DDR Bank
- 0 Disable..... default
- 1 Enable

6 Reserved ..... always reads 0

5 DQS Input DLL Adjustment
- 0 Disable..... default
- 1 Enable

4 DQS Output DLL Adjustment
- 0 Disable..... default
- 1 Enable

3 DQM Removal (Always Perform 4-Burst RW)
- 0 Disable..... default
- 1 Enable

2 DQS Output
- 0 Disable..... default
- 1 Enable

1 Auto Precharge for TLB Read or CPU WriteBack
- 0 Disable..... default
- 1 Enable

0 Write Recovery Time
- 0 1T ..... default
- 1 2T

Device 0 Offset 59-58 - DRAM MA Map Type (2222h).RW

15-13 Bank 5/4 MA Map Type (see table below)
12 Bank 5/4 1T Command Rate
0 2T Command.....default
1 1T Command
11-9 Bank 7/6 MA Map Type (see table below)
8 Bank 7/6 1T Command Rate
0 2T Command.....default
1 1T Command
7-5 Bank 1/0 MA Map Type (see table below)
4 Bank 1/0 1T Command Rate
0 2T Command.....default
1 1T Command
3-1 Bank 3/2 MA Map Type (see table below)
0 Bank 3/2 1T Command Rate
0 2T Command.....default
1 1T Command

Table 6. Device 0 Rx58 MA Map Type Encoding

000	16Mb	8-bit, 9-bit, 10-bit Column Address
001	64/128Mb	8-bit Column Address.....default
010	64/128Mb	9-bit Column Address
011	64/128Mb	10/11-bit Column Address
100		-reserved-
101	256Mb	8-bit Column Address
110	256Mb	9-bit Column Address
111	256Mb	10/11-bit Column Address

Device 0 Offset 5F-5A – DRAM Row Ending Address:

Offset 5A – Bank 0 Ending (HA[31:24]) (01h).....RW
Offset 5B – Bank 1 Ending (HA[31:24]) (01h).....RW
Offset 5C – Bank 2 Ending (HA[31:24]) (01h).....RW
Offset 5D – Bank 3 Ending (HA[31:24]) (01h).....RW
Offset 5E – Bank 4 Ending (HA[31:24]) (01h).....RW
Offset 5F – Bank 5 Ending (HA[31:24]) (01h).....RW
Offset 56 – Bank 6 Ending (HA[31:24]) (01h) .....RW
Offset 57 – Bank 7 Ending (HA[31:24]) (01h) .....RW

Note : BIOS is required to fill the ending address registers for all banks even if no memory is populated. The endings have to be in incremental order.

Device 0 Offset 60 – DRAM Type (00h)..... RW

7-6 DRAM Type for Bank 7/6
5-4 DRAM Type for Bank 5/4
3-2 DRAM Type for Bank 3/2
1-0 DRAM Type for Bank 1/0
00 SDR SDRAM ..... default
01 -reserved-
10 DDR SDRAM
11 -reserved-

Table 7. Memory Address Mapping Table

SDR / DDR SDRAM (x4 DRAMs supported by SDR only)

MA:	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
16Mb		24		13	12	11	14	22	21	20	19	18	17	16	15	12 row
(000)				13	PC	24	23	10	9	8	7	6	5	4	3	10,9,8 col
64/128Mb																x16 (14,8)
2K page	14	24	14	13	12	11	23	22	21	20	19	18	17	16	15	x32 (14,8)
001		27	14	13	PC	26	25	10	9	8	7	6	5	4	3	x8 (14,9)
4K page	14	25	14	13	12	24	23	22	21	20	19	18	17	16	15	x16 (14,9)
010		27	14	13	PC	26	11	10	9	8	7	6	5	4	3	**x4 (14,10)**
8K page	14	26	14	13	25	24	23	22	21	20	19	18	17	16	15	x8 (14,10)
011		27	14	13	PC	12	11	10	9	8	7	6	5	4	3	**x4 (14,11)**
256Mb																
2K page	25	24	14	13	12	11	23	22	21	20	19	18	17	16	15	x32 (15,8)
101		27	14	13	PC	26	25	10	9	8	7	6	5	4	3	
4K page	26	25	14	13	12	24	23	22	21	20	19	18	17	16	15	x16 (15,9)
110		27	14	13	PC	26	11	10	9	8	7	6	5	4	3	
8K page	27	26	14	13	25	24	23	22	21	20	19	18	17	16	15	x8 (15,10)
111		28	14	13	PC	12	11	10	9	8	7	6	5	4	3	**x4 (15,11)**

Device 0 Offset 61 - Shadow RAM Control 1 (00h) .....RW

7-6 CC000h-CFFFFh
- 00 Read/write disable .....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

5-4 C8000h-CBFFFh
- 00 Read/write disable .....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

3-2 C4000h-C7FFFh
- 00 Read/write disable .....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

1-0 C0000h-C3FFFh
- 00 Read/write disable .....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

Device 0 Offset 62 - Shadow RAM Control 2 (00h) .....RW

7-6 DC000h-DFFFFh
- 00 Read/write disable .....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

5-4 D8000h-DBFFFh
- 00 Read/write disable .....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

3-2 D4000h-D7FFFh
- 00 Read/write disable .....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

1-0 D0000h-D3FFFh
- 00 Read/write disable .....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

Device 0 Offset 63 - Shadow RAM Control 3 (00h)..... RW

7-6 E0000h-EFFFFh
- 00 Read/write disable ..... default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

5-4 F0000h-FFFFFh
- 00 Read/write disable ..... default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

3-2 Memory Hole
- 00 None ..... default
- 01 512K-640K
- 10 15M-16M (1M)
- 11 14M-16M (2M)

1-0 SMI Mapping Control
(Bit-1 = A,BK Direct Access SMRAM Disable)
(Bit-0 = A,BK DRAM Access Enable)

	SMM		Non-SMM	
	Code	Data	Code	Data
00	DRAM	DRAM	PCI	PCI
01	DRAM	DRAM	DRAM	DRAM
10	DRAM	PCI	PCI	PCI
11	DRAM	DRAM	DRAM	DRAM

Device 0 Offset 64 - DRAM Timing for All Banks (E4h)RW

7 Precharge Command to Active Command Period
- 0 TRP = 2T
- 1 TRP = 3T .....default

6 Active Command to Precharge Command Period
- 0 TRAS = 5T
- 1 TRAS = 6T ..... def

5-4 CAS Latency

	SDR	DDR	
00	1T	-	
01	2T	2T	
10	3T	2.5T	.....default
11	-	3T	

For VCM, CAS Latency is fixed at 2T, independent of the above bits

3 Reserved ..... always reads 0

2 ACTIVE to CMD
- 0 2T
- 1 3T .....default

1-0 Bank Interleave
- 00 No Interleave.....default
- 01 2-way
- 10 4-way
- 11 Reserved

For 16Mb SDRAMs, bank interleave is always 2-way

Device 0 Offset 65 - DRAM Arbitration Timer (00h) ....RW

7-4 AGP Timer (units of 4 MCLKs)..... default = 0

3-0 CPU Timer (units of 4 MCLKs)..... default = 0

Device 0 Offset 66 - DRAM Arbitration Control (40h) .RW

7 SDR – Feedback Clock Select
DDR - DQS Input Delay Setting
- 0 Auto (Rx67 reads DLL calibration result)... def
- 1 Manual (Rx67 reads DQS input delay)

6 DDR - DQS Output Delay Setting .....RO
- 0 Auto
- 1 Manual ..... always reads 1

5-4 Arbitration Parking Policy
- 00 Park at last bus owner.....default
- 01 Park at CPU
- 10 Park at AGP
- 11 -reserved-

3-0 AGP / CPU Priority (units of 4 MCLKs)

Device 0 Offset 67 – DDR Strobe Input Delay (00h)..... RW

DDR:

7-0 DQS Input Delay .....default = 0
(if Rx66[7]=0, read DLL calibration result)

SDR:

7-3 Reserved .....always reads 0

2-0 MD Latch Clock Select and Clock Delay

	MD Latch Clock	Delay Value	
000	Internal clock	0.27	default
001	Internal clock	0.45	
010	Internal clock	1.02	
011	External feedback clock	2.10	
100	Internal clock	1.32	
101	Internal clock	1.50	
110	Internal clock	2.07	
111	External feedback clock	3.15	

Device 0 Offset 68 – DDR Strobe Output Delay (00h)... RW

7-0 DDR DQS Output Delay .....default = 0

Device 0 Offset 69 – DRAM Clock Select (00h).....RW

7 CPU Operating Frequency Faster Than DRAM
- 0 CPU Same As or Equal to DRAM .....default
- 1 CPU Faster Than DRAM by 33 MHz

6 DRAM Operating Frequency Faster Than CPU
- 0 DRAM Same As or Equal to CPU .....default
- 1 DRAM Faster Than CPU by 33 MHz

5 DRAM Queue More Than 2
- 0 Disable .....default
- 1 Enable

4 DRAM Queue Not Equal to 4
- 0 Disable .....default
- 1 Enable

3 DRAM 8K Page Enable
- 0 Disable .....default
- 1 Enable

2 DRAM 4K Page Enable
- 0 Disable .....default
- 1 Enable

1 DIMM Type
- 0 Unbuffered .....default
- 1 Registered

0 Multiple Page Mode
- 0 Disable .....default
- 1 Enable

Device 0 Offset 6A - Refresh Counter (00h)..... RW

7-0 Refresh Counter (in units of 16 MCLKs)
- 00 DRAM Refresh Disabled..... default
- 01 32 MCLKs
- 02 48 MCLKs
- 03 64 MCLKs
- 04 80 MCLKs
- 05 96 MCLKs
- … …

The programmed value is the desired number of 16-MCLK units minus one.

Device 0 Offset 6B - DRAM Arbitration Control (10h).RW

7 Fast Read to Write turn-around
- 0 Disable .....default
- 1 Enable

6 Page Kept Active When Cross Bank
- 0 Disable .....default
- 1 Enable

5 Burst Refresh
- 0 Disable .....default
- 1 Enable

4 CKE Function
- 0 Disable
- 1 Enable .....default

3 Swap CA22 / CA14
- 0 Disable .....default
- 1 Enable

2-0 SDRAM Operation Mode Select
- 000 Normal SDRAM Mode .....default
- 001 NOP Command Enable
- 010 All-Banks-Precharge Command Enable (CPU-to-DRAM cycles are converted to All-Banks-Precharge commands).
- 011 MSR Enable CPU-to-DRAM cycles are converted to commands and the commands are driven on MA[14:0]. The BIOS selects an appropriate host address for each row of memory such that the right commands are generated on MA[14:0].
- 100 CBR Cycle Enable (if this code is selected, CAS-before-RAS refresh is used; if it is not selected, RAS-Only refresh is used)
- 101 Reserved
- 11x Reserved

Device 0 Offset 6C - Drive Control 1 (00h)..... RW

7-6 SDRAM A Drive – SRASA/SCASA/SWEA, MAA
- 00 Lowest ..... default
- 01
- 10
- 11 Highest

5-4 SDRAM B Drive – SRASB/SCASB/SWEB, MAB
- 00 Lowest ..... default
- 01
- 10
- 11 Highest

3-2 DDR DQS Drive
- 00 Lowest ..... default
- 01
- 10
- 11 Highest

1-0 MD / MECC / CAS / CKE Early Clock Select
- 00 Latest ..... default
- 01
- 10
- 11 Earliest

Device 0 Offset 6D - Drive Control 2 (00h)..... RW

7-6 Early Clock Select for SCMD, MA Output (for 1T Command)
- 00 Latest ..... default
- 01
- 10
- 11 Earliest

5-4 DQM Drive
- 00 Lowest ..... default
- 01
- 10
- 11 Highest

3-2 RAS# Drive
- 00 Lowest ..... default
- 01
- 10
- 11 Highest

1-0 Memory Data Drive (MD, MECC)
- 00 Lowest ..... default
- 01
- 10
- 11 Highest

Note: Refer to the BIOS Developers Guide for recommended memory configuration detection algorithms and recommended settings for the bits of the above two registers.

Device 0 Offset 6E - ECC Control (00h).....RW

7 ECC / EC Mode Select
- 0 ECC Checking and Reporting .....default
- 1 ECC Checking, Reporting, and Correcting

6 Perform Read-Modify-Write for Partial Write
- 0 Disable .....default
- 1 Enable

5 Enable SERR# on ECC / EC Multi-Bit Error
- 0 Don't assert SERR# for multi-bit errors..... def
- 1 Assert SERR# for multi-bit errors

4 Enable SERR# on ECC / EC Single-Bit Error
- 0 Don't assert SERR# for single-bit errors..... def
- 1 Assert SERR# for single-bit errors

3 ECC / EC Enable - Bank 7/6 (DIMM 3)
- 0 Disable (no ECC or EC for banks 7/6)...default
- 1 Enable (ECC or EC per bit-7)

2 ECC / EC Enable - Bank 5/4 (DIMM 2)
- 0 Disable (no ECC or EC for banks 5/4)...default
- 1 Enable (ECC or EC per bit-7)

1 ECC / EC Enable - Bank 3/2 (DIMM 1)
- 0 Disable (no ECC or EC for banks 3/2)...default
- 1 Enable (ECC or EC per bit-7)

0 ECC / EC Enable - Bank 1/0 (DIMM 0)
- 0 Disable (no ECC or EC for banks 1/0)...default
- 1 Enable (ECC or EC per bit-7)

Error checking / correction may be enabled bank-pair by bank-pair (DIMM by DIMM) by using bits 0-2 above. Bank pairs must be populated with 72-bit memory to enable for EC or ECC since the additional data bits must be present in either case. For this reason, if 64-bit memory is populated in a particular bank pair, the corresponding bit 0-2 should be set to 0 to disable both EC and ECC for that bank pair. For those bank pairs that have 72-bit memory available (and have the corresponding bit 0-2 set), either EC or ECC may be selected via bit-7 above (i.e., all enabled bank pairs will use EC or all will use ECC).

If error checking / reporting only (EC) is selected, all read and write cycles will use normal timing. Partial writes (with EC or ECC enabled) will use read-modify-write cycles to maintain correct error correction codes in the additional 8 data bits. If EC and ECC are disabled for a particular bank pair, partial writes to that bank pair will use the byte enables to write only the selected bytes (using normal write cycles and cycle timing). If error correction (ECC) is selected, the first read of a transaction will always have one additional cycle of latency.

Bit-7	Bits 2-0	RMW	Error Checking	Error Correction
0/1	0	No	No	No
0	1	Yes	Yes	No
1	1	Yes	Yes	Yes

Device 0 Offset 6F - ECC Status (00h)..... RWC

7 Multi-bit Error Detected..... write of '1' resets

6-4 Multi-bit Error DRAM Bank.....default=0
Encoded value of the bank with the multi-bit error.

3 Single-bit Error Detected..... write of '1' resets

2-0 Single-bit Error DRAM Bank .....default=0
Encoded value of the bank with the single-bit error.

Host PCI Bridge Control

These registers are normally programmed once at system initialization time.

Device 0 Offset 70 - PCI Buffer Control (00h).....RW

7 CPU to PCI Post-Write
- 0 Disable .....default
- 1 Enable

6 Reserved ..... always reads 0

5-4 PCI Master to DRAM Prefetch Control
- 00 Always Prefetch .....default
- x1 Never Prefetch
- 10 Prefetch only for enhance command

3 Reserved ..... always reads 0

2 PCI Master Read Buffering
- 0 Disable .....default
- 1 Enable

1 Delay Transaction
- 0 Disable .....default
- 1 Enable

0 Reserved ..... always reads 0

Device 0 Offset 71 - CPU to PCI Flow Control (48h) .... RW

7 Retry Status
- 0 No retry occurred..... default
- 1 Retry occurred

6 Retry Timeout Action
- 0 Retry forever (record status only)
- 1 Flush buffer or return FFFFFFFF for read... def

5-4 Retry Count and Retry Backoff
- 00 Retry 2 times, Boff CPU..... default
- 01 Retry 16 times
- 10 Retry 4 times
- 11 Retry 64 times

3 PCI Burst
- 0 Disable
- 1 Enable..... default

2 Reserved .....always reads 0

1 Configuration Cycle
- 0 Fix AD31..... default
- 1 Compatible Type #1 AD31

0 IDSEL Control
- 0 AD11 / AD12..... default
- 1 AD30 / AD31

Device 0 Offset 73 - PCI Master Control (00h) .....RW

7 Reserved ..... always reads 0

6 PCI Master 1-Wait-State Write
- 0 Zero wait state TRDY# response .....default
- 1 One wait state TRDY# response

5 PCI Master 1-Wait-State Read
- 0 Zero wait state TRDY# response .....default
- 1 One wait state TRDY# response

4 WSC#
- 0 Disable .....default
- 1 Enable

3-1 Reserved ..... always reads 0

0 PCI Master Broken Timer Enable
- 0 Disable .....default
- 1 Enable. Force into arbitration when there is no FRAME# 16 PCICLK's after the grant.

Device 0 Offset 75 - PCI Arbitration 1 (00h)..... RW

7 Arbitration Mode
- 0 REQ-based (arbitrate at end of REQ#) .. default
- 1 Frame-based (arbitrate at FRAME# assertion)

6-4 CPU Latency

3 Reserved .....always reads 0

2-0 PCI Master Bus Time-Out
(force into arbitration after a period of time)
- 000 Disable..... default
- 001 1x16 PCICLKs
- 010 2x16 PCICLKs
- 011 3x16 PCICLKs
- 100 4x16 PCICLKs
- ... ...
- 111 7x16 PCICLKs

Device 0 Offset 76 - PCI Arbitration 2 (00h)..... RW

7 I/O Port 22 Enable
- 0 CPU access to I/O address 22h is passed on to the PCI bus ..... default
- 1 CPU access to I/O port 22h is processed by internal I/O

6 Reserved .....always reads 0

5-4 Master Priority Rotation Control
- 00 Disable..... def
- 01 Grant to CPU after every PCI master grant
- 10 Grant to CPU after every 2 PCI master grants
- 11 Grant to CPU after every 3 PCI master grants

With setting 01, the CPU will always be granted access after the current bus master completes, no matter how many PCI masters are requesting. With setting 10, if other PCI masters are requesting during the current PCI master grant, the highest priority master will get the bus after the current master completes, but the CPU will be guaranteed to get the bus after that master completes. With setting 11, if other PCI masters are requesting, the highest priority will get the bus next, then the next highest priority will get the bus, then the CPU will get the bus. In other words, with the above settings, even if multiple PCI masters are continuously requesting the bus, the CPU is guaranteed to get access after every master grant (01), after every other master grant (10) or after every third master grant (11).

3-2 REQn# to REQ4# Mapping
- 00 REQ4#
- 01 REQ0#
- 10 REQ1#
- 11 REQ2#

1 Reserved .....always reads 0

0 REQ4# Master Priority
- 0 Normal..... default
- 1 High

GART / Graphics Aperture Control

The function of the Graphics Address Relocation Table (GART) is to translate virtual 32-bit addresses issued by an AGP device into 4K-page based physical addresses for system memory access. In this translation, the upper 20 bits (A31-A12) are remapped, while the lower 12 address bits (A11-A0) are used unchanged.

A one-level fully associative lookup scheme is used to implement the address translation. In this scheme, the upper 20 bits of the virtual address are used to point to an entry in a page table located in system memory. Each page table entry contains the upper 20 bits of a physical address (a "physical page" address). For simplicity, each page table entry is 4 bytes. The total size of the page table depends on the GART range (called the "aperture size") which is programmable in the VT8366A.

This scheme is shown in the figure below.

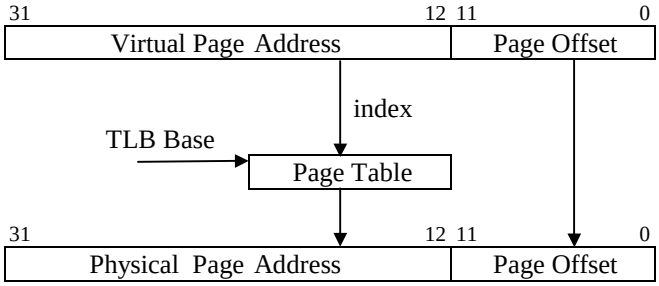

Figure 6. Graphics Aperture Address Translation

Since address translation using the above scheme requires an access to system memory, an on-chip cache (called a "Translation Lookaside Buffer" or TLB) is utilized to enhance performance. The TLB in the VT8366A contains 16 entries. Address "misses" in the TLB require an access of system memory to retrieve translation data. Entries in the TLB are replaced using an LRU (Least Recently Used) algorithm.

Addresses are translated only for accesses within the "Graphics Aperture" (GA). The Graphics Aperture can be any power of two in size from 1MB to 256MB (i.e., 1MB, 2MB, 4MB, 8MB, etc). The base of the Graphics Aperture can be anywhere in the system virtual address space on an address boundary determined by the aperture size (e.g., if the aperture size is 4MB, the base must be on a 4MB address boundary). The Graphics Aperture Base is defined in register offset 10 of device 0. The Graphics Aperture Size and TLB Table Base are defined in the following register group (offsets 84 and 88 respectively) along with various control bits.

Device 0 Offset 83-80 - GART/TLB Control (00000000h) RW

31-16 Reserved ..... always reads 0

15-8 Reserved (test mode status) ..... RO

7 Flush Page TLB

0 Disable .....default

1 Enable

6-0 Reserved (always program to 0) ..... RW

Note: For any master access to the Graphics Aperture range, snoop will not be performed.

Device 0 Offset 84 - Graphics Aperture Size (00h) ..... RW

7-0 Graphics Aperture Size

11111111 1M
11111110 2M
11111100 4M
11111000 8M
11110000 16M
11100000 32M
11000000 64M
10000000 128M
00000000 256M

Offset 8B-88 - GA Translation Table Base (00000000h) RW

31-12 Graphics Aperture Translation Table Base. Pointer to the base of the translation table in system memory used to map addresses in the aperture range (the pointer to the base of the "Directory" table).

11-2 Reserved ..... always reads 0

1 Graphics Aperture

0 Disable..... default

1 Enable

Note: To disable the Graphics Aperture, set this bit to 0 and set all bits of the Graphics Aperture Size to 0. To enable the Graphics Aperture, set this bit to 1 and program the Graphics Aperture Size to the desired aperture size.

0 Reserved ..... always reads 0

Host CPU Control

Device 0 Offset 92 – S2K Timing Control III (78h).....RW

The contents of this register are preserved during suspend. Bits 2-0 have no default value.

- **7 Disconnect Enable When STPGNT Detected**
- **6 Write to Read Delay** ..... default = 1
- **5-4 Read to Write Delay** ..... default = 11b
- **3 Reserved (Do Not Program)**..... default = 1
- **2-0 Write Data Delay from SYSDC to CPU Data Output** ..... (WrDataDly)

Device 0 Offset 93 – BIU Arbitration Control.....RW

- **7-6 Max of Contiguous Probe SysDC Before Switch to Other Type of SysDC**
- **5-3 Max of Contiguous Read SysDC Before Switch to Other Type of SysDC**
- **2-0 Max of Contiguous Write SysDC Before Switch to Other Type of SysDC**

Device 0 Offset 94 – BIU Control 1.....RW

- **7 SDRAM Self-Refresh When Disconnected**
  - 0 Disable .....default
  - 1 Enable
- **6 Probe Next Tag State T1 When PCI Master Read Caching Enabled**
  - 0 Disable .....default
  - 1 Enable
- **5-4 Reserved** ..... always reads 0
- **3 DRAM Speculative Read for PCI Master Read (Before Probe Result is Known)**
  - 0 Disable .....default
  - 1 Enable
- **2 PCI Master Pipeline Request**
  - 0 Disable .....default
  - 1 Enable
- **1 PCI-to-CPU / CPU-to-PCI (P2C / C2P) Concurrency**
  - 0 Disable .....default
  - 1 Enable
- **0 Fast Write-to-Read Turnaround**
  - 0 Disable .....default
  - 1 Enable

Device 0 Offset 95 – BIU Control 2 ..... RW

- **7 FWDVLD / PSQHPTR Concurrency**
  - 0 Backwards Compatible ..... default
  - 1
- **6 RHOCTW**
  - 0 ..... default
  - 1
- **5 PMW Address Compare**
  - 0 Backward compatible ..... default
  - 1 Compare address qualified with PMW
- **4 Write Policy for CPU Write to DRAM**
  - 0 Issue DRAM write when FIFO holds more than two requests or DRAM controller idle . def
  - 1 Disable Write Policy
- **3 PMR Cycle Control**
  - 0 Stall PMR cycle if MWQ is full ..... default
  - 1 Execute PMR cycles normally whether MWQ is full or not
- **2 FID Command Detect**
  - 0 Disable (command will not have new FID) . def
  - 1 Enable
- **1 HALT Command Detect**
  - 0 Disable (command will not do self refresh) . def
  - 1 Enable
- **0 Reserved** ..... always reads 0

Device 0 Offset 96 – BIU Control 3 ..... RW

- **7 Memory Write Queue Timer Function**
  - 0 Disable..... default
  - 1 Enable
- **6 Memory Write Queue Timer Function Trigger**
  - 0 Trigger by data ready for C2M Wr Req..... def
  - 1 Trigger by command FIFO utilization
- **5-3 Memory Write Queue Timer High Bound** .....def=0
- **2-0 Memory Write Queue Timer Low Bound** .....def=0

Bits 5-0 are defined in units of 4QW / request number

Device 0 Offset 97 – CPU Strapping Control.....RO

7-3 CPU Clock Divide .....set from VAD[3-0] straps
- 00000 11 .....no strap default
- 00001 11.5
- 00010 12
- 00011 12.5
- 00100 5
- 00101 5.5
- 00110 6
- 00111 6.5
- 01000 7
- 01001 7.5
- 01010 8
- 01011 8.5
- 01100 9
- 01101 9.5
- 01110 10
- 01111 10.5
- 10000 3
- 10001 3.5
- 10010 4
- 10011 4.5
- 101xx -reserved-

3 Reserved ..... always reads 0

2 S2K Drive Strength
- 0 Determined by register settings .....default
- 1 Determined by auto compensation

1 Fast Address Out Decode .....set from ROMSIP#
- 0 Normal .....no strap default
- 1 Fast

0 S2K Compensation Circuit
- 0 Always Enable.....default
- 1 Enable on Disconnect

Device 0 Offset 98 – S2K Compensation Strapping (00h)RW

7-4 S2K Pullup Drive Strength..... default = 0

3-0 S2K Pulldown Drive Strength ..... default = 0

Device 0 Offset 99 – S2K Compensation Result 1 (00h)..RO

7-4 Pullup Auto Compensation Result..... default = 0

3-0 Pulldown Auto Compensation Result .... default = 0

Device 0 Offset 9A – S2K Compensation Result 2 ..... RW

7 S2K Edge DQ Mode .....RO, set from MA11 strap
- 0 Central DQ..... default
- 1 Edge DQ

6-0 S2K Strobe Delay (EdgeDQ) .... set from MA[8-4] straps
- 0 Auto Mode..... no-strap default
- ~0 Strapping Mode

Device 0 Offset 9B – S2K Compensation Result 3 ..... RO

7-0 S2K Strobe DLL Delay Counter (Auto) .....def = 0

Device 0 Offset 9C – S2K Compensation Result 4 (07h) RW

7 S2K Compensation Circuit Trigger

6 DLL Autodetect ..... RO

5 Delay Compensation Counter Control

4-3 S2K Pad AC Coupling to VREF Signal in Address / Data Output Clock

2-0 S2K Pad Slew Rate Ctrl (7h is strongest).... def=7h

Device 0 Offset 9D – S2K Compensation Result 5 ..... RW

7-4 S2K Strobe Output Drive Strength P Control

3-0 S2K Strobe Output Drive Strength N Control

Device 0 Offset 9E – BIU Control 4 ..... RW

7 Pending Memory Read
- 0 Read not pending..... default
- 1 Read pending

6 Issue Memory Write Queue Ready When Command FIFO is Empty Enough (>24)
- 0 Disable..... default
- 1 Enable

5 Issue Memory Write Queue If More Than 4 CPU Requests Are Pending
- 0 Disable..... default
- 1 Enable

4 Fast Write Performance Improvement
- 0 Backwards Compatible..... default
- 1 Enable performance improvement

3 Issue Write DADS Only When Memory Write Queue Timer or DM Idle or HB Hit
- 0 Disable..... default
- 1 Enable

2 Compare Partial Address to Decide if CPU-to-Memory Read Hit CPU-to-Memory Write
- 0 Compare HA[31:6] (backwards compatible)def
- 1 Compare HA[31:12]

1 Memory Read Guard Bit
- 0 Backwards Compatible..... default
- 1 Enable

0 Reserved .....always reads 0

AGP Control

Device 0 Offset A3-A0 - AGP Capability Identifier (0020C002h) .....RO

31-24 **Reserved** ..... always reads 00
23-20 **Major Specification Revision** ... always reads 0010b
Major rev # of AGP spec that device conforms to
19-16 **Minor Specification Revision** ... always reads 0000b
Minor rev # of AGP spec that device conforms to
15-8 **Pointer to Next Item**.....always reads C0 (last item)
7-0 **AGP ID** .. (always reads 02 to indicate it is AGP)

Device 0 Offset A7-A4 - AGP Status (1F000201h) .....RO

31-24 **Maximum AGP Requests** ..... always reads 1Fh†
Max # of AGP requests the device can manage (32)
† See also RxFC[1] and RxFD[4-0]
23-10 **Reserved** .....always reads 0s
9 **Supports SideBand Addressing** ..... always reads 1
8-6 **Reserved** .....always reads 0s
5 **4G Supported** .....(can be written at RxAE[5]
4 **Fast Write Supported** .....(can be written at RxAE[4]
3 **Reserved** .....always reads 0s
2 **4X Rate Supported**..... (can be written at RxAE[2])
1 **2X Rate Supported**..... (can be written at RxAC[3])
0 **1X Rate Supported**..... always reads 1

Device 0 Offset AB-A8 - AGP Command (00000000h) . RW

31-24 **Request Depth** (reserved for target).. always reads 0s
23-10 **Reserved** ..... always reads 0s
9 **SideBand Addressing Enable**
0 Disable..... default
1 Enable
8 **AGP Enable**
0 Disable..... default
1 Enable
7-6 **Reserved** ..... always reads 0s
5 **4G Enable**
0 Disable..... default
1 Enable
4 **Fast Write Enable**
0 Disable..... default
1 Enable
3 **Reserved** ..... always reads 0s
2 **4X Mode Enable**
0 Disable..... default
1 Enable
1 **2X Mode Enable**
0 Disable..... default
1 Enable
0 **1X Mode Enable**
0 Disable..... default
1 Enable

Device 0 Offset AC - AGP Control (00h) .....RW

7 AGP .....RO per strap on MAB9
- 0 Disable .....default
- 1 Enable

6 AGP Read Synchronization
- 0 Disable .....default
- 1 Enable

5 AGP Read Snoop DRAM Post-Write Buffer
- 0 Disable .....default
- 1 Enable

4 GREQ# Priority Becomes Higher When Arbiter is Parked at AGP Master
- 0 Disable .....default
- 1 Enable

3 2X Rate Supported (read also at RxA4[1])
- 0 Not supported .....default
- 1 Supported

2 LPR In-Order Access (Force Fence)
- 0 Fence/Flush functions not guaranteed. AGP read requests (low/normal priority and high priority) may be executed before previously issued write requests.....default
- 1 Force all requests to be executed in order (automatically enables Fence/Flush functions). Low (i.e., normal) priority AGP read requests will never be executed before previously issued writes. High priority AGP read requests may still be executed prior to previously issued write requests as required.

1 AGP Arbitration Parking
- 0 Disable .....default
- 1 Enable (GGNT# remains asserted until either GREQ# de-asserts or data phase ready)

0 AGP to PCI Master or CPU to PCI Turnaround Cycle
- 0 2T or 3T Timing.....default
- 1 1T Timing

Device 0 Offset AD – AGP Latency Timer (02h) ..... RW

7-6 Reserved .....always reads 0

5 AGP Data Input Enable (for Power Saving)
- 0 AGP data input always enabled ..... default
- 1 AGP data input only enabled when necessary to avoid redundant transitions

4 Choose First or Last Ready of DRAM
- 0 Last ready chosen ..... default
- 1 First ready chosen

3-0 AGP Data Phase Latency Timer ..... default = 02h

Device 0 Offset AE – AGP Miscellaneous Control (00h)RW

7-6 Reserved .....always reads 0

5 Greater Than 4GB Supported
- 0 Disable..... default
- 1 Enable

4 Fast Write Supported
- 0 Fast Write not supported..... default
- 1 Fast Write supported

3 Reserved .....always reads 0

2 4x Rate Supported
- 0 4x Rate not supported ..... default
- 1 4x Rate supported

1-0 Reserved .....always reads 0

Device 0 Offset AF – AGP Strobe Drive Strength (00h) RW

7-4 AGP Strobe Output Drive Strength N Control

3-0 AGP Strobe Output Drive Strength P Control

Device 0 Offset B0 – AGP Pad Control / Status (8xh)....RW

7 AGP 4x Strobe VREF Control
- 0 STB VREF is STB# and vice versa
- 1 STB VREF is AGPREF **.....default**

6 AGP 4x Strobe & GD Pad Drive Strength
- 0 Drive strength set to compensation circuit default.....default
- 1 Drive strength controlled by RxB1[7-0]

5-3 AGP Compensation Circuit N Control Output .RO

2-0 AGP Compensation Circuit P Control Output .RO

Device 0 Offset B1 – AGP Drive Strength (63h).....RW

7-4 AGP Output Buffer Drive Strength N Ctrl ... def=6

3-0 AGP Output Buffer Drive Strength P Ctrl.... def=3

Device 0 Offset B2 – AGP Pad Drive / Delay Ctrl (08h) RW

7 GD/GBE/GDS, SBA/SBS Control

1.5V (Bit-1 = 0)
- 0 SBA/SBS = no cap ..... default
  GD/GBE/GDS = no cap
- 1 SBA/SBS = no cap
  GD/GBE/GDS = **cap**

3.3V (Bit-1 = 1)
- 0 SBA/SBS = **cap** ..... default
  GD/GBE/GDS = no cap
- 1 SBA/SBS = **cap**
  GD/GBE/GDS = **cap**

6-5 Reserved ..... always reads 0

4 GD[31-16] Staggered Delay
- 0 None ..... default
- 1 GD[31:16] delayed by 1 ns

3 AGP Slew Rate Control
- 0 Disable
- 1 Enable **..... default**

2 AGP Preamble Control
- 0 Disable ..... default
- 1 Enable

1 AGP Voltage
- 0 1.5V ..... default
- 1 3.3V

0 GDS Output Delay
- 0 None ..... default
- 1 GDS[1-0] & GDS[1-0]# delayed by 0.4 ns (GDS1 & GDS1# will be delayed an additional 1ns if bit-4 = 1)

V-Link Control

Device 0 Offset B4 – V-Link NB Compensation Ctrl (00h)RW

- **7-6 V-Link Autocomp Output Value** ..... always reads 0
- **5 Pullup Compensation Selection**
  - 0 Auto Comp (use values in bits 7-6).....default
  - 1 Manual Comp (use values in bits 3-2)
- **4 Pulldown Compensation Selection**
  - 0 Auto Comp (use values in bits 7-6).....default
  - 1 Manual Comp (use values in bits 1-0)
- **3-2 Pullup Compensation Manual Setting**..... def = 0
- **1-0 Pulldown Compensation Manual Setting**..... def = 0

Device 0 Offset B5 – V-Link NB Drive Control (00h)....RW

- **7-6 Strobe Pullup Manual Setting**
- **5-4 Strobe Pulldown Manual Setting**
- **3-1 Reserved** ..... always reads 0
- **0 V-Link Slew Rate Control**
  - 0 Disable .....default
  - 1 Enable

Device 0 Offset B8 – V-Link SB Compensation Ctrl (00h)RW

- **7-6 V-Link Autocomp Output Value** ..... always reads 0
- **5 Pullup Compensation Selection**
  - 0 Auto Comp (use values in bits 7-6).....default
  - 1 Manual Comp (use values in bits 3-2)
- **4 Pulldown Compensation Selection**
  - 0 Auto Comp (use values in bits 7-6).....default
  - 1 Manual Comp (use values in bits 1-0)
- **3-2 Pullup Compensation Manual Setting**..... def = 0
- **1-0 Pulldown Compensation Manual Setting**..... def = 0

Device 0 Offset B9 – V-Link SB Drive Control (00h).....RW

- **7-1 Reserved** ..... always reads 0
- **0 V-Link Slew Rate Control**
  - 0 Disable .....default
  - 1 Enable

DRAM Power Control

Device 0 Offset BE – MECC Drive Strength (00h)..... RW

- **7-6 MECC Drive Strength**
- **5-0 Reserved** .....always reads 0

Device 0 Offset BF – DRAM Pad Toggle Reduction (00h)RW

- **7 MA / SCMD Pin Toggle Reduction**
  - 0 Disable..... default
  - 1 Enable (MA and S command pins won't toggle if not accessed)
- **6 Slew Rate Control for MA / S-Command Group A**
  - 0 Disable..... default
  - 1 Enable
- **5 Slew Rate Control for MA / S-Command Group B**
  - 0 Disable..... default
  - 1 Enable
- **4 Reserved** .....always reads 0
- **3 DIMM #3 MAA / MAB Select**
  - 0 MAA ..... default
  - 1 MAB
- **2 DIMM #2 MAA / MAB Select**
  - 0 MAA ..... default
  - 1 MAB
- **1 DIMM #1 MAA / MAB Select**
  - 0 MAA ..... default
  - 1 MAB
- **0 DIMM #0 MAA / MAB Select**
  - 0 MAA ..... default
  - 1 MAB

Extended Power Management Control

Device 0 Offset C0 – Power Management Capability ID RO

7-0 Capability ID ..... always reads 01h

Device 0 Offset C1 – Power Management New Pointer ..RO

7-0 New Pointer .....always reads 00h ("Null" Pointer)

Device 0 Offset C2 – Power Mgmt Capabilities I .....RO

7-0 Power Management Capabilities .. always reads 02h

Device 0 Offset C3 – Power Mgmt Capabilities II.....RO

7-0 Power Management Capabilities .. always reads 00h

Device 0 Offset C4 – Power Mgmt Control / Status .....RW

7-2 Reserved ..... always reads 0

1-0 Power State

00 D0 .....default
01 -reserved-
10 -reserved-
11 D3 Hot

Device 0 Offset C5 – Power Management Status .....RW

7-0 Power Management Status ..... default = 0

Device 0 Offset C6 – PCI-to-PCI Bridge Support Ext. ..RW

7-0 P2P Bridge Support Extensions..... default = 0

Device 0 Offset C7 – Power Management Data.....RW

7-0 Power Management Data ..... default = 0

Device 1 Header Registers - PCI-to-PCI Bridge

All registers are located in PCI configuration space. They should be programmed using PCI configuration mechanism 1 through CF8 / CFC with bus number of 0 and function number equal to 0 and device number equal to one.

Device 1 Offset 1-0 - Vendor ID (1106h) .....RO

15-0 ID Code (reads 1106h to identify VIA Technologies)

Device 1 Offset 3-2 - Device ID (B099h) .....RO

15-0 ID Code (reads B099h to identify the VT8366A PCI-to-PCI Bridge device)

Device 1 Offset 5-4 – Command (0007h) .....RW

15-10 Reserved ..... always reads 0

9 Fast Back-to-Back Cycle Enable ..... RO
- 0 Fast back-to-back transactions only allowed to the same agent .....default
- 1 Fast back-to-back transactions allowed to different agents

8 SERR# Enable..... RO
- 0 SERR# driver disabled .....default
- 1 SERR# driver enabled

(SERR# is used to report parity errors if bit-6 is set).

7 Address / Data Stepping ..... RO
- 0 Device never does stepping .....default
- 1 Device always does stepping

6 Parity Error Response.....**RW**
- 0 Ignore parity errors & continue .....default
- 1 Take normal action on detected parity errors

5 VGA Palette Snoop (Not Supported)..... RO
- 0 Treat palette accesses normally .....default
- 1 Don't respond to palette writes on PCI bus (10-bit decode of I/O addresses 3C6-3C9 hex)

4 Memory Write and Invalidate Command..... RO
- 0 Bus masters must use Mem Write .....default
- 1 Bus masters may generate Mem Write & Inval

3 Special Cycle Monitoring ..... RO
- 0 Does not monitor special cycles .....default
- 1 Monitors special cycles

2 Bus Master .....**RW**
- 0 Never behaves as a bus master
- 1 Enable to operate as a bus master on the primary interface on behalf of a master on the secondary interface .....default

1 Memory Space.....**RW**
- 0 Does not respond to memory space
- 1 Enable memory space access .....default

0 I/O Space .....**RW**
- 0 Does not respond to I/O space
- 1 Enable I/O space access .....default

Device 1 Offset 7-6 - Status (Primary Bus) (0230h).... RWC

15 Detected Parity Error .....always reads 0

14 Signaled System Error (SERR#) .....always reads 0

13 Signaled Master Abort
- 0 No abort received ..... default
- 1 Transaction aborted by the master with Master-Abort (except Special Cycles) .... write 1 to clear

12 Received Target Abort
- 0 No abort received ..... default
- 1 Transaction aborted by the target with Target-Abort ..... write 1 to clear

11 Signaled Target Abort.....always reads 0

10-9 DEVSEL# Timing
- 00 Fast
- 01 Medium.....always reads 01
- 10 Slow
- 11 Reserved

8 Data Parity Error Detected .....always reads 0

7 Fast Back-to-Back Capable .....always reads 0

6 User Definable Features.....always reads 0

5 66MHz Capable.....always reads 1

4 Supports New Capability list.....always reads 1

3-0 Reserved .....always reads 0

Device 1 Offset 8 - Revision ID (00h) ..... RO

7-0 VT8366A Chip Revision Code (00=First Silicon)

Device 1 Offset 9 - Programming Interface (00h) ..... RO

This register is defined in different ways for each Base/Sub-Class Code value and is undefined for this type of device.

7-0 Interface Identifier .....always reads 00

Device 1 Offset A - Sub Class Code (04h) ..... RO

7-0 Sub Class Code .reads 04 to indicate PCI-PCI Bridge

Device 1 Offset B - Base Class Code (06h)..... RO

7-0 Base Class Code.. reads 06 to indicate Bridge Device

Device 1 Offset D - Latency Timer (00h) ..... RO

7-0 Reserved .....always reads 0

Device 1 Offset E - Header Type (01h) ..... RO

7-0 Header Type Code..... reads 01: PCI-PCI Bridge

Device 1 Offset F - Built In Self Test (BIST) (00h) ..... RO

7 BIST Supported..... reads 0: no supported functions

6 Start Test ..... write 1 to start but writes ignored

5-4 Reserved .....always reads 0

3-0 Response Code.....0 = test completed successfully

Device 1 Offset 18 - Primary Bus Number (00h).....RW

7-0 Primary Bus Number..... default = 0

This register is read write, but internally the chip always uses bus 0 as the primary.

Device 1 Offset 19 - Secondary Bus Number (00h).....RW

7-0 Secondary Bus Number..... default = 0

Note: AGP must use these bits to convert Type 1 to Type 0.

Device 1 Offset 1A - Subordinate Bus Number (00h).....RW

7-0 Primary Bus Number..... default = 0

Note: AGP must use these bits to decide if Type 1 to Type 1 command passing is allowed.

Device 1 Offset 1B – Secondary Latency Timer (00h) ....RO

7-0 Reserved ..... always reads 0

Device 1 Offset 1C - I/O Base (f0h).....RW

7-4 I/O Base AD[15:12]..... default = 1111b

3-0 I/O Addressing Capability..... default = 0

Device 1 Offset 1D - I/O Limit (00h).....RW

7-4 I/O Limit AD[15:12] ..... default = 0

3-0 I/O Addressing Capability..... default = 0

Device 1 Offset 1F-1E - Secondary Status (0000h).....RO

15-0 Rx44[4] = 0: No Function (always reads 0)
Rx44[4] = 1: Read same value as Rx7-6 (Pri Status)

Device 1 Offset 21-20 - Memory Base (FFF0h).....RW

15-4 Memory Base AD[31:20].....default = FFFh

3-0 Reserved ..... always reads 0

Device 1 Offset 23-22 - Memory Limit (Inclusive) (0000h) RW

15-4 Memory Limit AD[31:20]..... default = 0

3-0 Reserved ..... always reads 0

Device 1 Offset 25-24 - Prefetchable Mem Base (FFF0h) RW

15-4 Prefetchable Memory Base AD[31:20]...def = FFFh

3-0 Reserved ..... always reads 0

Device 1 Offset 27-26 - Prefetchable Memory Limit (0000h) .....RW

15-4 Prefetchable Memory Limit AD[31:20] .....
..... default = 0

3-0 Reserved ..... always reads 0

Device 0 Offset 2D-2C – Subsystem Vendor ID (0000h)R/W1

15-0 Subsystem Vendor ID.....default = 0

This register may be written once and is then read only.

Device 0 Offset 2F-2E – Subsystem ID (0000h)..... R/W1

15-0 Subsystem ID .....default = 0

This register may be written once and is then read only.

Device 1 Offset 34 – Capability Pointer (80h) ..... RO

7-0 Capability Pointer .....always reads 80h

Device 1 Offset 3F-3E – PCItoPCI Bridge Ctrl (0000h) RW

15-4 Reserved .....always reads 0

3 VGA-Present on AGP

0 Forward VGA accesses to PCI Bus ..... default

1 Forward VGA accesses to AGP Bus

Note: VGA addresses are memory A0000-BFFFFh and I/O addresses 3B0-3BBh, 3C0-3CFh and 3D0-3DFh (10-bit decode). "Mono" text mode uses B0000-B7FFFh and "Color" Text Mode uses B8000-BFFFFh. Graphics modes use Axxxxh. Mono VGA uses I/O addresses 3Bx-3Cxh and Color VGA uses 3Cx-3Dxh. If an MDA is present, a VGA will not use the 3Bxh I/O addresses and B0000-B7FFFh memory space; if not, the VGA will use those addresses to emulate MDA modes.

2 Block / Forward ISA I/O Addresses

0 Forward all I/O accesses to the AGP bus if they are in the range defined by the I/O Base and I/O Limit registers (device 1 offset 1C-1D) ..... default

1 Do not forward I/O accesses to the AGP bus that are in the 100-3FFh address range even if they are in the range defined by the I/O Base and I/O Limit registers.

1-0 Reserved .....always reads 0

Device 1 Configuration Registers - PCI-to-PCI Bridge

AGP Bus Control

Device 1 Offset 40 - CPU-to-AGP Flow Control 1 (00h)RW

7 CPU-AGP Post Write
- 0 Disable .....default
- 1 Enable

6 Reserved ..... always reads 0

5 CPU-AGP One Wait State Burst Write
- 0 Disable .....default
- 1 Enable

4 AGP to DRAM Prefetch
- 0 Disable .....default
- 1 Enable

3 CPU to AGP Post Write Halt
- 0 Disable .....default
- 1 Enable

If set to 1, CPU-to-PCI posted cycles can be delayed for PCI master accesses (i.e., PCI master access is allowed even if the CPU-to-PCI buffer is not flushed)

2 MDA Present on AGP
- 0 Forward MDA accesses to AGP.....default
- 1 Forward MDA accesses to PCI

Note: Forward despite IO / Memory Base / Limit

Note: MDA (Monochrome Display Adapter) addresses are memory addresses B0000h-B7FFFh and I/O addresses 3B4-3B5h, 3B8-3BAh, and 3BFh (10-bit decode). 3BC-3BE are reserved for printers.

Note: If Rx3E bit-3 is 0, this bit is a don't care (MDA accesses are forwarded to the PCI bus).

1 AGP Master Read Caching
- 0 Disable .....default
- 1 Enable

0 AGP Delay Transaction
- 0 Disable .....default
- 1 Enable

Table 8. VGA/MDA Memory/IO Redirection

3E[3] VGA Pres.	40[2] MDA Pres.	VGA is on	MDA is on	Axxxx, B8xxx Access	B0000 -B7FFF Access	3Cx, 3Dx I/O	3Bx I/O
0	-	PCI	PCI	PCI	PCI	PCI	PCI
1	0	AGP	AGP	AGP	AGP	AGP	AGP
1	1	AGP	PCI	AGP	PCI	AGP	PCI

Device 1 Offset 41 - CPU-to-AGP Flow Control 2 (00h) RW

7 Retry Status
- 0 No retry occurred..... default
- 1 Retry Occurred .....**write 1 to clear**

6 Retry Timeout Action
- 0 No action taken except to record status ..... def
- 1 Flush buffer for write or return all 1s for read

5-4 Retry Count
- 00 Retry 2, backoff CPU ..... default
- 01 Retry 4, backoff CPU
- 10 Retry 16, backoff CPU
- 11 Retry 64, backoff CPU

3 CPU-to-AGP Bursting Timeout
- 0 Disable..... default
- 1 Enable

2-0 Reserved .....always reads 0

Device 1 Offset 42 - AGP Master Control (00h) ..... RW

7 Disconnect PCI on AGP Data Ready
- 0 Continue current PCI master even if AGP data is ready..... default
- 1 Disconnect current PCI master when AGP data is ready

6 AGP Master One Wait State Write
- 0 Disable..... default
- 1 Enable

5 AGP Master One Wait State Read
- 0 Disable..... default
- 1 Enable

4 Reserved .....always reads 0

3 RPM2
- 0 Use tail of AGP-to-Memory Read Ready to return data..... default
- 1 Dynamically use head or tail of AGP-to-Memory Read Ready to return data

2 Prefetch Disable when Delay Transaction Occurs
- 0 Normal operation..... default
- 1 Disable prefetch when doing fast response to the previous delay transaction or doing read caching

1 Reserved .....always reads 0

0 Generate STOP# When AGP Master Access Crosses Cache Line Boundary
- 0 Disable..... default
- 1 Enable

Device 1 Offset 43 - AGP Master Latency Timer (22h) RW

7-4 Host to AGP Time Slot
- 0 Disable (no timer
- 1 16 GCLKs
- 2 32 GCLKs).....default
- 3 48 GCLKs
- … …
- F 240 GCLKs

3-0 AGP Master Time Slot
- 0 Disable (no timer)
- 1 16 GCLKs
- 2 32 GCLKs .....default
- 3 48 GCLKs
- … …
- F 240 GCLKs

Device 1 Offset 44 – Backdoor Register Control (20h) .RW

7 Revision ID Writeable
- 0 Revision ID is RO .....default
- 1 Revision ID is RW

6 Reserved ..... always reads 0

5 Power Management Capability Support
- 0 Rx34 reads 00
- 1 Rx34 reads 80h .....default

4 Reflect Rx7-6 Status in Rx1F-1E
- 0 Disable (Rx1F-1E always reads 0).....default
- 1 Enable (Rx1F-1E reads same as Rx7-6)

3-2 Rx83[2-1] Back Door Value

1 Rx82[5] Back Door Value (Device Specific Intfc)

0 Back Door Register Enable for AGP Device ID (Rx47-46)
- 0 Disable .....default
- 1 Enable

Device 1 Offset 45 – Fast Write Control (72h)..... RW

7 Force Fast Write Cycle to be QW Aligned (if Rx45[6] = 0)
- 0 Disable..... default
- 1 Enable

6 Merge Multiple CPU Transactions Into One Fast Write Burst Transaction
- 0 Disable
- 1 Enable..... **default**

5 Merge Multiple CPU Write Cycles To Memory Offset 23-20 Into Fast Write Burst Cycles (if Rx45[6] = 0)
- 0 Disable
- 1 Enable..... **default**

4 Merge Multiple CPU Write Cycles To Prefetchable Memory Offset 27-24 Into Fast Write Burst Cycles (if Rx45[6] = 0)
- 0 Disable
- 1 Enable..... **default**

3 Reserved .....always reads 0

2 Fast Write Burst 4T Max (No Slave Flow Control)
- 0 Disable..... default
- 1 Enable

1 Fast Write Fast Back to Back
- 0 Disable
- 1 Enable..... **default**

0 Fast Write Initial Block 1 Wait State
- 0 Disable..... default
- 1 Enable

Rx45 Bits 7-4	CPU Write Address in Mem1	CPU Write Address in Mem2	Fast Write Cycle Alignment
x1xx	-	-	QW aligned, burstable
0000	-	-	DW aligned, nonburstable
x010	0	0	n/a
0010	0	1	DW aligned, non-burstable
x010	1	-	QW aligned, burstable
x001	0	0	n/a
x001	-	1	QW aligned, burstable
0001	1	0	DW aligned, non-burstable
x011	0	0	n/a
x011	1	-	QW aligned, burstable
x011	0	1	QW aligned, burstable
1000	-	-	QW aligned, non-burstable
1010	0	1	QW aligned, non-burstable
1001	1	0	QW aligned, non-burstable

Device 1 Offset 47-46 – PCI-to-PCI Bridge Device ID...RW

15-0 PCI-to-PCI Bridge Device ID..... default = 0000

Device 1 Offset 80 – Capability ID (01h) ..... RO

7-0 Capability ID ..... always reads 01h

Device 1 Offset 81 – Next Pointer (00h) ..... RO

7-0 Next Pointer: Null..... always reads 00h

Device 1 Offset 82 – Power Mgmt Capabilities 1 (02h) .. RO

7-6 Power Mgmt Capabilities ..... always reads 0
5 Power Mgmt Capabilities . programmed via Rx44[1]
4-0 Power Mgmt Capabilities ..... always reads 02h

Device 1 Offset 83 – Power Mgmt Capabilities 2 (00h) .. RO

7-3 Power Mgmt Capabilities ..... always reads 0
2-1 Power Mgmt Capabilities programmed via Rx44[3-2]
0 Power Mgmt Capabilities ..... always reads 0

Device 1 Offset 84 – Power Mgmt Ctrl/Status (00h)..... RW

7-2 Reserved ..... always reads 0
1-0 Power State
00 D0 ..... default
01 -reserved-
10 -reserved-
11 D3 Hot

Device 1 Offset 85 – Power Mgmt Status (00h)..... RO

7-0 Power Mgmt Status ..... default = 00

Device 1 Offset 86 – P2P Br. Support Extensions (00h) . RO

7-0 P2P Bridge Support Extensions..... default = 00

Device 1 Offset 87 – Power Management Data (00h) ..... RO

7-0 Power Management Data..... default = 00

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Min	Max	Unit
Storage Temperature	-55	125	^{o}C
Case Operating Temperature	0	85	^{o}C
Input Voltage	-0.5	5.5	Volts
Output Voltage (V_{CC} = 3.1 - 3.6V)	-0.5	V_{CC} + 0.5	Volts

Note: Stress above the conditions listed may cause permanent damage to the device. Functional operation of this device should be restricted to the conditions described under operating conditions.

DC Characteristics

T_C = 0-85^{o}C, V_{CC3}=3.3V+/-5%, GND=0V

Symbol	Parameter	Min	Max	Unit	Condition
V_{IL}	Input low voltage	-0.50	0.8	V	
V_{IH}	Input high voltage	2.0	V_{CC}+0.5	V	
V_{OL}	Output low voltage	-	0.45	V	I_{OL}=4.0mA
V_{OH}	Output high voltage	2.4	-	V	I_{OH}=-1.0mA
I_{IL}	Input leakage current	-	+/-10	uA	$0<V_{IN}<V_{CC}$
I_{OZ}	Tristate leakage current	-	+/-20	uA	$0.45<V_{OUT}<V_{CC}$

Power Characteristics

T_C = 0-85^{o}C, V_{RAIL} = V_{CC} +/- 5%, V_{CORE} = 2.5V +/- 5%, GND=0V

Symbol	Parameter	Typ	Max	Unit	Condition
I_{CC33}	Power Supply Current - Internal Logic & I/O Intfc			mA	Max operating frequency
I_{CCSUS}	Power Supply Current - Suspend Power			mA	Max operating frequency
I_{CCTT}	Power Supply Current - CPU Interface Termination			mA	Max operating frequency
I_{CCHCK}	Power Supply Current - Host CPU Clock Logic			mA	Max operating frequency
I_{CCMCK}	Power Supply Current - DRAM Clock Logic			mA	Max operating frequency
I_{CCGCK}	Power Supply Current - AGP Clock Deskew Logic			mA	Max operating frequency
I_{CCQ}	Power Supply Current - AGP 1.5V or 3.3V Power			mA	Max operating frequency
I_{CCQQ}	Power Supply Current - AGP Quiet Power			mA	Max operating frequency
$I_{CCS2KREF}$	Power Supply Current - CPU Interface Voltage Ref			uA	Max operating frequency
$I_{CCCLKREF}$	Power Supply Current - Clock Voltage Reference			uA	Max operating frequency
$I_{CCAGPREF}$	Power Supply Current - AGP Voltage Reference			uA	Max operating frequency
P_D	Power Dissipation			W	Max operating frequency

AC Timing Specifications

AC timing specifications provided are based on external zero-pf capacitance load. Min/max cases are based on the following table:

Table 9. AC Timing Min / Max Conditions

Parameter	Min	Max	Unit
3.3V Power	3.135	3.465	Volts
2.5V Power	2.375	2.625	Volts
Case Temperature	0	85	^{o}C

Drive strength for each output pin is programmable. See Rx6D for details.

MECHANICAL SPECIFICATIONS

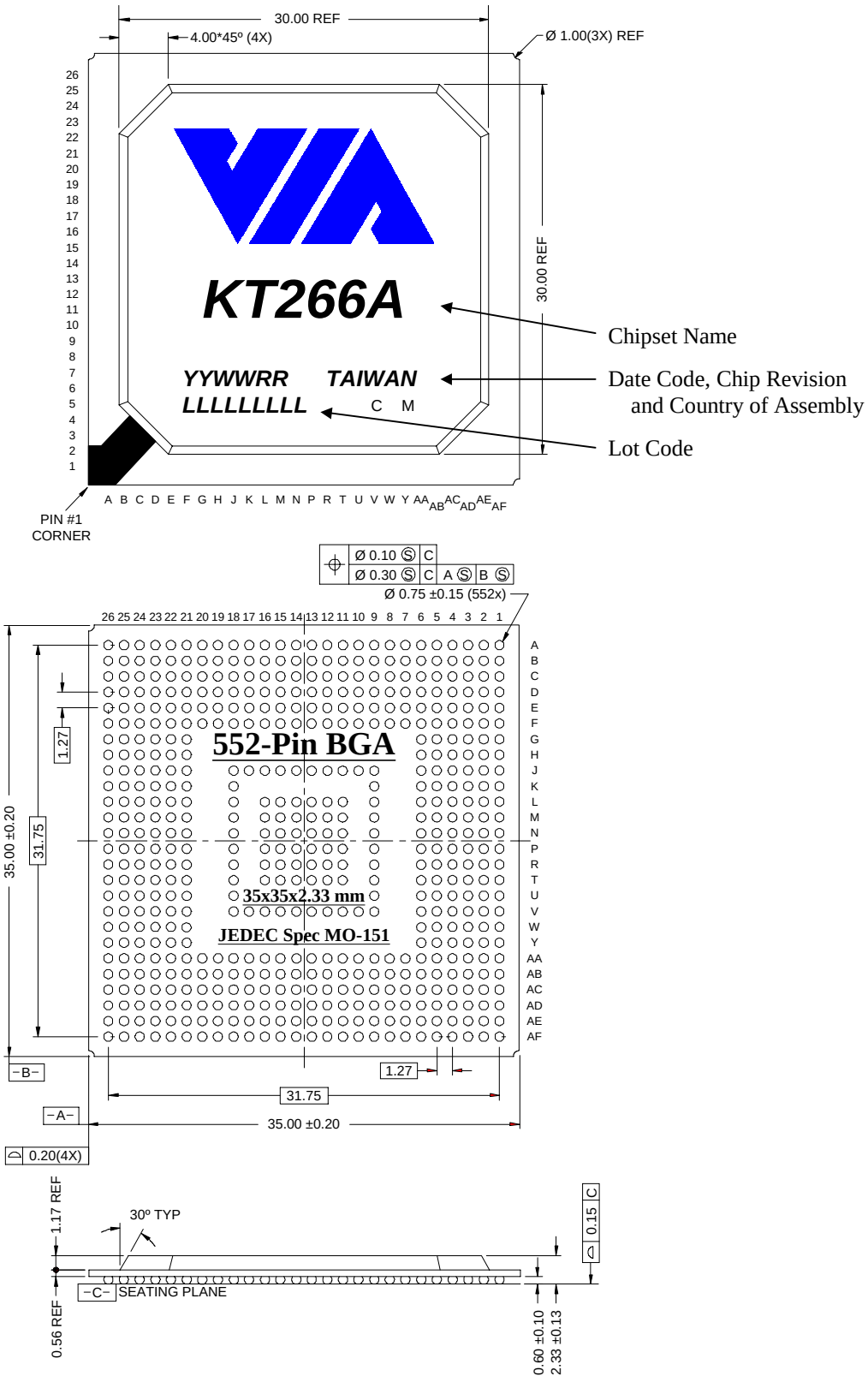

Figure 7. Mechanical Specifications – VT8366A 552-Pin Ball Grid Array Package