VT8231
South Bridge

PC99 COMPLIANT
INTEGRATED SUPER-I/O (FDC, LPT, COM, FIR, GAME PORT),
INTEGRATED FAST ETHERNET, LPC, ISA / LPC BIOS ROM,
DIRECTSOUND AC97 AUDIO AND MC97 MODEM INTERFACE,
INTEGRATED SOUNDBLASTER PRO
ULTRADMA-33/66/100 MASTER MODE EIDE CONTROLLER,
4 PORT USB CONTROLLER, KEYBOARD CONTROLLER, RTC,
SERIAL IRQ, SMBUS,
PLUG AND PLAY, ACPI, ENHANCED POWER MANAGEMENT,
TEMPERATURE, VOLTAGE, AND FAN-SPEED MONITORING

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REVISION HISTORY

Document Release	Date	Revision	Initials
1.0	5/31/00	Initial public release – removed "NDA Required" watermark Fixed USBOC2# pin description, F0 Rx40[0], E4[6], PMIO Rx1-0[9], 45[4-0]	DH
1.1	8/1/00	Removed "high speed baud rate support", fixed VREF pin direction Fixed Dev0 F0Rx42[6], F4Rx55[6,2], E0-E1, F4 PM IO Rx21-20, 52 Deleted ambient temp spec, added max power & power specs table Fixed mech spec pin 1 orientation	DH
1.11	8/22/00	Fixed IDE registers Rx40-45 descriptions and defaults (added Rx42)	DH
1.2	11/13/00	Added note to ROMCS# pin description Added F0Rx34, Updated F0Rx41; Updated F4Rx56[3-0] Updated F1Rx4[7,1],6[4],9[2,0],10[0],14[0],18[0],1C[0],20[0],40[3],45[2]	DH
1.3	12/6/00	Removed "NDA Required" watermark from cover page Removed ACSDIN2-3 (only 2 codecs supported) Fixed typos in F4RxE4[5,0], E5[7,3-1] Replaced F4Rx56[3-0] definition from revision 1.11 (incorrect change)	DH
1.31	12/11/00	Fixed definition of VCCH and GNDH pins.	DH
1.4	1/19/01	Updated copyright notice; Added missing item in table of contents Fixed ACRST# pin name polarity Fixed pin lists / pin descriptions for HREQ/HGNT/LREQ/LGNT#, USBOC2/3#, SDD[15-0], JAB2/JBB2, IRTX/IRRX, IOR/IOW#, LA20/21, MSCK/DT, KBCK/DT, KBCS#, ROMCS#, LDRQ#, SLPBTN#, GPI0-8, 19, 26-27, GPO0-5, 19, 25-27 Fixed register descriptions Func 4 RxE4[7-6], E5[1] and PMIO Rx10[10], 4C	DH
1.5	2/1/01	Removed ACSDIN2 & fixed Device 0 Function 4 RxE5[1] Fixed pin descriptions PCS1#, GPI19-27,30-31, GPO19	DH
1.6	3/1/01	Removed ATEST and DTEST functions (reserved for internal test purposes) Fixed GPI10-13 & GPO10-13 pin descriptions and Device 0 F4 RxE5[3-2] Fixed note under General Purpose Inputs pin description table Fixed STPCLK# errors in F4 Rx4C[0], PMIO Rx10[9], Rx2C[3] Changed F5/6 Rx1C-1F to reserved and removed I/O Base 3 registers	DH
1.7	3/19/01	Fixed heading in pin descriptions for UDMA pins Fixed pin descriptions for JAB1, JBB1, GPI10-13, GPI28-29, GPO8-11 Added notes in pin descriptions for register bit cross references Clarified general notes for GPI pin descriptions Fixed Device 0 Function 0 Rx40[2], Device 0 Function 4 RxE5[3-2]	DH
1.8	4/30/01	Updated title page, fixed typographical error in table of contents Updated north bridge compatibility list in feature bullets Added IRQ8# function to GPI1 pin; Added IOCHRDY to LREQ2#/GPI13 pin Fixed typo on L/HREQ/GNT pins in pinout diagram Added function summary at beginning of Registers section Added F0 Rx67[3-2] and added related notes in pin descriptions section Removed SMB I/O register E;; Removed Temp Reading 3 from HWM I/O registers Fixed definitions of F1 Rx43[3-0]; 50[28,20,12,4], F4 Rx55[7-6]	DH
1.81	7/2/01	Updated company addresses; Updated Func 0 Rx4C[3:0] Changed INIT pin to INIT# and added note to pin description	DH
1.82	11/19/01	Fixed LAN Device ID, Elec specs FERR# input voltage; Updated marking specs	DH
1.83	2/4/02	Updated logos and legal page formatting; Fixed THRM pin polarity in descriptions Fixed figure 1 (# of serial ports); Fixed IRRX/IRTX pin descriptions Fixed register descriptions: Port 71, Func 4 RxE5[5], PMIO Rx4[0]	DH
1.84	2/12/02	Fixed Figure 7 PM Block Diagram to fix pdf print problem; removed "Preliminary"	DH

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PRODUCT FEATURES

- **Inter-operable with VIA and other Host-to-PCI Bridges**
  - Combine with VT8363A (Apollo KT133A) for a complete Athlon AGP 4x desktop system with 200/266 MHz FSB
  - Combine with VT8361 (Apollo KLE133) or VT8365A (Apollo KM133A) for a complete Athlon system with integrated 2D / 3D graphics
  - Combine with VT82C694X (Apollo Pro133A) for a complete 66 / 100 / 133 MHz Socket370 / Slot1 AGP 4x system
  - Combine with VT8601A (Apollo PLE133) or VT8605 (Apollo PM133) for a complete Socket370 / Slot1 system with integrated 2D / 3D graphics
  - Combine with VT82C598 (Apollo MVP3) for a complete Super-7 (66 / 75 / 83 / 100 MHz) AGP 2x system
  - Combine with VT8501 (Apollo MVP4) for a complete Super-7 system with integrated 2D / 3D graphics
  - Inter-operable with Intel or other Host-to-PCI bridges for a complete PC99 compliant PCI / AGP / LPC system
- **Integrated Peripheral Controllers**
  - Integrated Fast Ethernet Controller with 1 / 10 / 100 Mbit capability
  - Integrated USB Controller with two root hub and four function ports
  - Dual channel UltraDMA-33 / 66 /100 master mode EIDE controller
  - AC-link interface for AC-97 audio codec and modem codec
  - HSP modem support
  - Integrated SoundBlasterPro / DirectSound compatible digital audio controller
  - LPC interface for Low Pin Count interface to Super-I/O or ROM
- **Integrated Legacy Functions**
  - Integrated Keyboard Controller with PS2 mouse support
  - Integrated DS12885-style Real Time Clock with extended 256 byte CMOS RAM and Day/Month Alarm for ACPI
  - Integrated Bus Controller including DMA, timer, and interrupt controller
  - Serial IRQ for docking and non-docking applications
  - Flash EPROM, 32Mbit (4Mbyte) EPROM and combined BIOS support
  - Fast reset and Gate A20 operation

- **Fast Ethernet Controller**
  - High performance PCI master interface with scatter / gather and bursting capability
  - Standard MII interface to Ethernet or HomePNA PHYceiver
  - 1 / 10 / 100 MHz full and half duplex operation
  - Transmit data buffer byte alignment for low CPU utilization
  - Separate 2K byte FIFOs for receive and transmit of full Ethernet packets
  - Flexible dynamically loadable EEPROM algorithm
  - Physical, Broadcast, and Multicast address filtering using hashing function
  - Flexible wakeup events: link status change, magic packet, unicast physical address match, predefined pattern match
  - Software controllable power down
- **UltraDMA-33 / 66 / 100 Master Mode PCI EIDE Controller**
  - Dual channel master mode PCI supporting four Enhanced IDE devices
  - Transfer rate up to 100MB/sec to cover up to PIO mode 4, multi-word DMA mode 2, and UltraDMA mode 5
  - Thirty-two levels (doublewords) of prefetch and write buffers per channel
  - Dual DMA engine for concurrent dual channel operation
  - Bus master programming interface for SFF-8038i rev.1.0 and Windows-95 / 98 / 2000 compliant
  - Full scatter gather capability
  - Support ATAPI compliant devices including DVD devices
  - Support PCI native and ATA compatibility modes
  - Complete software driver support
- **Integrated Super IO Controller**
  - Supports serial port, IR port, parallel port, and floppy disk controller functions
  - Serial Port
    - Programmable character lengths (5,6,7,8)
    - Even, odd, stick or no parity bit generation and detection
    - Programmable baud rate generator
    - Independent transmit/receiver FIFOs
    - Modem Control
    - Plug and play with 96 base IO address and 12 IRQ options
  - Fast IR (FIR) port
    - IrDA 1.0 SIR and IrDA 1.1 FIR compliant
    - IR function through the second serial port
    - Infrared-IrDA (HPSIR) and ASK (Amplitude Shift Keyed) IR
  - Multi-mode parallel port
    - Standard mode, ECP and EPP support
    - Dynamic and static switch between parallel port pinout and FDC pinout
    - Plug and play with 192 base IO address, 12 IRQ and 4 DMA options
  - Floppy Disk Controller
    - 16 bytes of FIFO
    - Data rates up to 1Mbps
    - Perpendicular recording driver support
    - Two FDDs with drive swap support
    - Plug and play with 48 base IO address, 12 IRQ and 4 DMA options
- **Low Pin Count (LPC) Bus Interface**
  - Provides connection to external LPC I/O controllers and LPC BIOS ROMs
  - Enables removal of legacy ISA bus and related pins
  - Low pin count interface: two control pins and four address / data pins

- **SoundBlaster Pro Hardware and Direct Sound Ready AC97 Digital Audio Controller**
  - Dual full-duplex Direct Sound channels between system memory and AC97 link
  - PCI master interface with scatter / gather and bursting capability
  - 32 byte FIFO of each direct sound channel
  - Host based sample rate converter and mixer
  - Standard v1.0 or v2.0 AC97 Codec interface for single or cascaded AC97 Codec's from multiple vendors
  - Loopback capability for re-directing mixed audio streams into USB and 1394 speakers
  - Hardware SoundBlaster Pro for Windows DOS box and real-mode DOS legacy compatibility
  - Plug and play with 4 IRQ, 4 DMA, and 4 I/O space options for SoundBlaster Pro and MIDI hardware
  - Hardware assisted FM synthesis for legacy compatibility
  - Direct two game ports and one MIDI port interface
  - Complete software driver support for Windows-95/98/2000 and Windows-NT
- **MC97 HSP Modem Controller**
  - PCI bus master interface with scatter / gather and burst capability
  - Standard AC97 codec interface for MC or AMC codec
  - Wake on ring in APM or ACPI mode through AC97 link
  - Supported by most HSP modem vendors
- **Universal Serial Bus Controller**
  - USB v.1.1 and Intel Universal HCI v.1.1 compatible
  - Eighteen level (doublewords) data FIFO with full scatter and gather capability
  - Root hub and four function ports
  - Integrated physical layer transceivers with optional over-current detection status on USB inputs
  - Legacy keyboard and PS/2 mouse support
- **System Management Bus Interface**
  - One master / slave SMBus and one slave-only SMBus
  - Host interface for processor communications
  - Slave interface for external SMBus masters

- **Voltage, Temperature, Fan Speed Monitor and Controller**
  - Five universal input channels for voltage or temperature sensing
  - Two fan-speed monitoring channels
  - Input channel for thermal diode in Intel™ high speed Pentium II™ / Pentium III™ CPUs
  - Programmable control, status, monitor and alarm for flexible desktop management
  - External thermister or internal bandgap temperature sensing
  - Automatic clock throttling with integrated temperature sensing
  - Internal core VCC voltage sensing
  - Flexible external voltage sensing arrangement (any positive supply and battery)
- **Sophisticated PC99-Compatible Mobile Power Management**
  - Supports both ACPI (Advanced Configuration and Power Interface) and legacy (APM) power management
  - ACPI v1.0 Compliant
  - APM v1.2 Compliant
  - CPU clock throttling and clock stop control for complete ACPI C0 to C3 state support
  - PCI bus clock run, Power Management Enable (PME) control, and PCI/CPU clock generator stop control
  - Supports multiple system suspend types: power-on suspends with flexible CPU/PCI bus reset options, suspend to DRAM, and suspend to disk (soft-off), all with hardware automatic wake-up
  - Multiple suspend power plane controls and suspend status indicators
  - One idle timer, one peripheral timer and one general purpose timer, plus 24/32-bit ACPI compliant timer
  - Normal, doze, sleep, suspend and conserve modes
  - Global and local device power control
  - System event monitoring with two event classes
  - Primary and secondary interrupt differentiation for individual channels
  - Dedicated input pins for power and sleep buttons, external modem ring indicator, and notebook lid open/close for system wake-up
  - Multiple internal and external SMI sources for flexible power management models
  - One programmable chip select and one microcontroller chip select
  - Enhanced integrated real time clock (RTC) with date alarm, month alarm, and century field
  - Thermal alarm on either external or any combination of three internal temperature sensing circuits
  - Hot docking support
  - I/O pad leakage control
- **Plug and Play Controller**
  - PCI interrupts steerable to any interrupt channel
  - Steerable interrupts for integrated peripheral controllers: USB, floppy, serial, parallel, audio, soundblaster, MIDI
  - Steerable DMA channels for integrated floppy, parallel, and soundblaster pro controllers
  - One additional steerable interrupt channel for on-board plug and play devices
  - Microsoft Windows 2000™, Windows 98SE™, Windows 98™, Windows NT™, Windows 95™ and plug and play BIOS compliant
- **Built-in NAND-tree pin scan test capability**
- **0.30um, 3.3V, low power CMOS process**
- **Single chip 27x27 mm, 376 pin BGA**

OVERVIEW

The VT8231 South Bridge is a high integration, high performance, power-efficient, and high compatibility device that supports Intel, AMD, and VIA / Cyrix based processor to PCI bus bridge functionality to make a complete Microsoft PC99-compliant PCI / LPC system. The VT8231 includes standard intelligent peripheral controllers:

a) Master mode enhanced IDE controller with dual channel DMA engine and interlaced dual channel commands. Dedicated FIFO coupled with scatter and gather master mode operation allows high performance transfers between PCI and IDE devices. In addition to standard PIO and DMA mode operation, the VT8231 also supports the UltraDMA-33, 66, and 100 standards to allow reliable data transfer rates up to 100 MB/sec throughput. The IDE controller is SFF-8038i v1.0 and Microsoft Windows-family compliant.

b) Integrated LAN Fast Ethernet controller (MAC) with Media Independent Interface (MII) to external Ethernet PHY or HomePNA PHY. The LAN controller operates at 1 / 10 / 100 Mbit/sec transfer rates using either full and half duplex operation and has separate 2Kbyte FIFOs for receive and transmit of full ethernet packets. The internal high-performance PCI interface has scatter / gather and bursting capability and can align bytes in the transmit data buffer to reduce CPU utilization. The LAN interface can perform address filtering on physical, broadcast, and multicast packets. The interface can also be configured for system wake up on link status change, receipt of magic packet, unicast physical address match on incoming packets, and predefined pattern match in the incoming data.

c) LPC (Low Pin Count) interface for BIOS ROM plus optional conventional BIOS ROM support

d) Universal Serial Bus controller that is USB v1.1 and Universal HCI v1.1 compliant. The VT8231 includes the root hub with four function ports with integrated physical layer transceivers. The USB controller allows hot plug and play and isochronous peripherals to be inserted into the system with universal driver support. The controller also implements legacy keyboard and mouse support so that legacy software can run transparently in a non-USB-aware operating system environment.

e) Keyboard controller with PS2 mouse support

f) Real Time Clock with 256 byte extended CMOS. In addition to standard RTC functionality, the integrated RTC also includes the date alarm, century field, and other enhancements for compatibility with the ACPI standard.

g) Notebook-class power management functionality compliant with ACPI and legacy APM requirements. Multiple sleep states (power-on suspend, suspend-to-DRAM, and suspend-to-Disk) are supported with hardware automatic wake-up. Additional functionality includes event monitoring, CPU clock throttling and stop (Intel processor protocol), PCI bus clock stop control, modular power, clock and leakage control, hardware-based and software-based event handling, general purpose I/O, chip select and external SMI.

h) Hardware monitoring subsystem for managing system / motherboard voltage levels, temperatures, and fan speeds

i) Full System Management Bus (SMBus) interface with one master / slave port and one slave-only port

j) 16550-compatible serial I/O port with “Fast-IR” infrared communications port option.

k) Integrated PCI-mastering dual full-duplex direct-sound AC97-link-compatible sound system. Hardware soundblaster-pro and hardware-assisted FM blocks are included for Windows DOS box and real-mode DOS compatibility. Loopback capability is also implemented for directing mixed audio streams into USB and 1394 speakers for high quality digital audio.

l) Game port and MIDI port

m) Standard floppy disk drive interface

n) ECP/EPP-capable parallel port with floppy disk controller pinout option

o) Serial IRQ for docking and non-docking applications

p) Plug and Play controller that allows complete steerability of all PCI interrupts and internal interrupts to any interrupt channel. One additional steerable interrupt channel is provided to allow plug and play and reconfigurability of on-board peripherals for Windows family compliance.

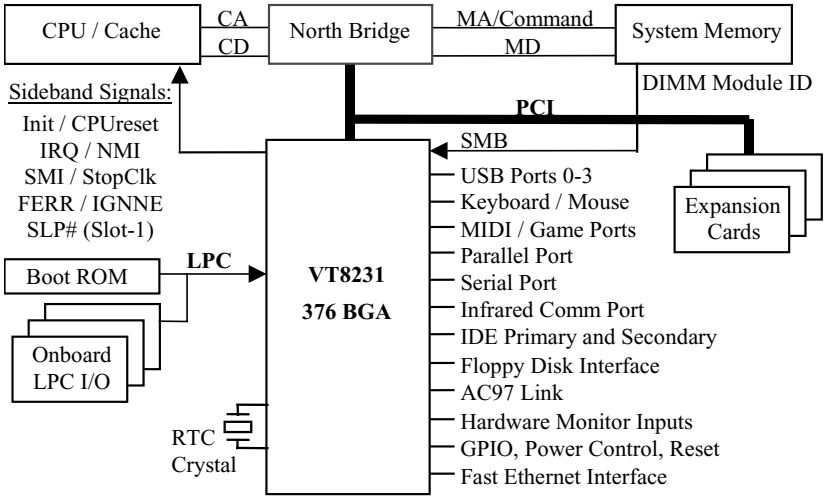

Figure 1. PC System Configuration Using the VT8231

PINOUTS

Pin Diagram

Figure 2. VT8231 Ball Diagram (Top View)

Key	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	AD 30	AD 31	AD 26	AD 24	AD 21	AD 16	DEV SEL#	CBE 1#	AD 9	AD 5	STR#	PD 2	PD 6	BUSY	RTS#	DTR#	USB OC0#	USB P0-	USB P1-	USB P2-
B	PINT B#	PINT A#	AD 28	AD 25	AD 23	AD 18	T RDY#	AD 15	AD 10	AD 4	AD 1	P INIT#	PD 5	ACK#	TXD	CTS#	USB P3-	USB P0+	USB P1+	USB P2+
C	PREQ H#	PINT D#	PINT C#	AD 27	CBE 3#	AD 19	I RDY#	PAR	AD 12	AD 6	AD 0	PD 1	PD 4	PD 7	USB CLK	RI#	USB P3+	EE CS#	MRX CLK	MD CK
D	PGNT L#	PREQ L#	PGNT H#	AD 29	AD 20	CBE 2#	STOP #	AD 14	AD 7	AD 2	PD 0	SLCT IN#	PE	DSR#	DCD#	USB OC1#	EE DO	MD IO	MRX D3	MRX D2
E	V BAT	PWR GD	RTC X1	PCI RST#	AD 22	AD 17	SERR #	AD 13	AD 8	AD 3	AUTO FD#	PD 3	SLCT	RXD	**VCC USB**	EE CK	EE DI	MRX D1	MRX D0	MRX DV
F	JB B1	RSM RST#	INTR UDR#	GPI 0	RTC X2	FRM#	**VCC**	AD 11	**VCC**	CBE 0#	ERR#	**VCC**	**VCC**	**GND USB**	**VCC**	**VCC MII**	MTX CLK	MRX ERR	MTX ENA	MTX D0
G	AC SYNC	AC RST#	JA B1	MSI	PCS1# SDIN2	**VCC**	**GND**	**VCC**	**VCC**	**VCC**	**GND**	**VCC**	**GND RAM**	**GND**	**VCC RAM**	M CRS	M COL	MTX D1	MTX D2	MTX D3
H	AC SDIN0	AC SDIN1	AC SDO	JB B2	JA B2	**VCC**	**H7**	**8**	**9**	**10**	**11**	**12**	**13**	**H14**	**GND**	TRK 00#	WRT PRT#	DSK CHG#	HD SEL#	R DATA#
J	JA X	JB Y	AC BCLK	MSO	GPIO C	**VCC**	**J**	**GND**	**GND**	**GND**	**GND**	**GND**	**GND**	**J**	**VCC**	MTR 1#	DS 0#	STEP#	W DATA#	W GATE#
K	**VREF**	FAN 1	FAN2 SLPB#	JA Y	JB X	**GND**	**K**	**GND**	**GND**	**GND**	**GND**	**GND**	**GND**	**K**	**VCC**	**VCC MII**	DRV DEN1	MTR 0#	DS 1#	DIR#
L	UIC 5	DTD +	DTD -	UIC 4	**GND HWM**	**VCC**	**L**	**GND**	**GND**	**GND**	**GND**	**GND**	**GND**	**L**	**GND**	**VCC PLL**	DRV DEN0	PDCS 1#	PDCS 3#	IN DEX#
M	UIC 1	UIC 3	UIC 2	KB CK	**VCC HWM**	**VCC**	**M**	**GND**	**GND**	**GND**	**GND**	**GND**	**GND**	**M**	**VCC**	**GND PLL**	PCI CLK	PD A1	PD A0	PD A2
N	KB DT	MS CK	SUS C#	MS DT	SUS ST#	**VCC**	**N7**	**8**	**9**	**10**	**11**	**12**	**13**	**N14**	**GND**	PD D10	PD D5	PD IOR#	PD RDY	PD DACK#
P	SUSA #/strap	SUS B#	AOL GPI	CPU STP#	**VCC SUS**	**VCC SUS**	**GND**	**VCC**	**VCC**	**GND**	**VCC**	**VCC**	**VCC**	**GND**	**VCC**	PD D4	PD D11	PD D8	PD DRQ	PD IOW#
R	SMB CK2	SMB DT2	SMB CK1	GPO 0	PCK RUN#	INTR	**VCC**	IR TX	**VCC**	**VCC**	SD 6	SD 0	**VCC**	**VCC**	**VCC**	PD D1	PD D14	PD D7	PD D9	PD D6
T	SMB DT1	SMB ALRT#	BAT LOW#	PCI STP#	NMI	IGN NE#	IO W#	IR RX2	ROM CS#	HG2# GPO9	SD 7	OSC	SA17 /strap	IRQ 14	SA8 SDD8	PD D0	PD D15	PD D13	PD D3	PD D12
U	PME#	PWR BTN#	RING #	CPU RST	FERR #	SLP#	IO R#	IR RX	SPKR	LR1# GPI12	SD 5	SD 4	SA 18	IRQ 15	SA7 SDD7	SA6 SDD6	SD DRQ	SDCS 1#	SDCS 3#	PD D2
V	CPU MISS	LID	GPI1 IRQ8#	WSC#	INIT #	STP CLK#	L AD3	L AD0	SER IRQ	LG2# GPO11	HR2# GPI11	SD 1	SA 19	SA5 SDD5	SA11 SDD11	SA2 SDD2	SA14 SDD14	SD A1	SD A0	SD A2
W	EXT SMI#	SUS CLK	GPIO E	APIC D0	A20 M#	MCCS #/strap	L AD2	L FRM#	MEM R#	LR2# RDY	HG1# GPO8	SD 2	LA 20	SA9 SDD9	SA4 SDD4	SA12 SDD12	SA1 SDD1	SA15 SDD15	SD IOR#	SD DACK#
Y	GPIO D	GPIO A	APIC CLK	APIC D1	SMI#	PCS0# /strap	L AD1	L DRQ#	MEM W#	LG1# GPO10	HR1# GPI10	SD 3	LA 21	SA16 /strap	SA10 SDD10	SA3 SDD3	SA13 SDD13	SA0 SDD0	SD IOW#	SD RDY
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20

Note: Some of the pins above have alternate functions and alternate names. The table above contains only one name (usually the most often used function), but the pin lists and pin descriptions contain all names.

Pin Lists

Figure 3. VT8231 Pin List (Numerical Order)

Pin		Pin Name	Pin		Pin Name	Pin		Pin Name	Pin		Pin Name	Pin		Pin Name
A01	IO	AD30	D12	IO	SLCTIN#/STEP#	H03	O	ACSDOUT	P02	O	SUSB# / GPIO2	U13	IO	SA18
A02	IO	AD31	D13	I	PE / WDATA#	H04	I	JBB2 / GPO13	P03	I	AOLGPI/THRM/I17	U14	I	IRQ15
A03	IO	AD26	D14	I	DSR#	H05	I	JAB2 / GPO12	P04	O	CPUSTP# / GPO5	U15	IO	SA07 / SDD07
A04	IO	AD24	D15	I	DCD#	**H06**	**P**	**VCC**	**P05**	**P**	**VCCSUS**	U16	IO	SA06 / SDD06
A05	IO	AD21	D16	I	USBOC1#	**H15**	**P**	**GND**	**P06**	**P**	**VCCSUS**	U17	I	SDDRQ
A06	IO	AD16	D17	O	EEDO	H16	I	TRK00#	**P07**	**P**	**GND**	U18	O	SDCS1#
A07	IO	DEVSEL#	D18	IO	MDIO	H17	I	WRTPRT#	**P08**	**P**	**VCC**	U19	O	SDCS3#
A08	IO	CBE1#	D19	I	MRXD3	H18	I	DSKCHG#	**P09**	**P**	**VCC**	U20	IO	PDD02
A09	IO	AD09	D20	I	MRXD2	H19	O	HDSEL#	**P10**	**P**	**GND**	V01	I	CPUMISS / GPI16
A10	IO	AD05	**E01**	**P**	**VBAT**	H20	I	RDATA#	**P11**	**P**	**VCC**	V02	I	LID / GPI4
A11	IO	STROBE#	E02	I	PWRGD	J01	I	JAX	**P12**	**P**	**VCC**	V03	I	GPI1 / IRQ8#
A12	IO	PD2 / WRTPRT#	E03	I	RTCX1	J02	I	JBY	**P13**	**P**	**VCC**	V04	I	WSC# / GPI24
A13	IO	PD6	E04	O	PCIRST#	J03	I	ACBITCLK	**P14**	**P**	**GND**	V05	OD	INIT#
A14	I	BUSY / MTR1#	E05	IO	AD22	J04	O	MSO	**P15**	**P**	**VCC**	V06	OD	STPCLK#
A15	O	RTS#	E06	IO	AD17	J05	IO	GPIOC/IO25/CHSIO	P16	IO	PDD04	V07	IO	LAD3
A16	O	DTR#	E07	I	SERR#	**J06**	**P**	**VCC**	P17	IO	PDD11	V08	IO	LAD0
A17	I	USBOC0#	E08	IO	AD13	**J15**	**P**	**VCC**	P18	IO	PDD08	V09	I	SERIRQ
A18	IO	USBP0-	E09	IO	AD08	J16	O	MTR1#	P19	I	PDDRQ	V10	O	LGNT2# / GPO11
A19	IO	USBP1-	E10	IO	AD03	J17	O	DS0#	P20	O	PDIOW#	V11	I	HREQ2# / GPI11
A20	IO	USBP2-	E11	IO	AUTOFD#/DRV0	J18	O	STEP#	R01	IO	SMBCK2 / GPIO27	V12	IO	SD01
B01	I	PINTB#	E12	IO	PD3 / RDATA#	J19	O	WDATA#	R02	IO	SMBDT2 / GPIO26	V13	IO	SA19
B02	I	PINTA#	E13	I	SLCT/WGATE#	J20	O	WGATE#	R03	IO	SMBCK1	V14	IO	SA05 / SDD05
B03	IO	AD28	E14	I	RXD	**K01**	**O**	**VREF**	R04	O	SLOWCLK / O0	V15	IO	SA11 / SDD11
B04	IO	AD25	**E15**	**P**	**VCCUSB**	K02	I	FAN1	R05	IO	PCKRUN#	V16	IO	SA02 / SDD02
B05	IO	AD23	E16	O	EECK	K03	I	FAN2/SLPB#/IO18	R06	OD	INTR	V17	IO	SA14 / SDD14
B06	IO	AD18	E17	I	EEDI	K04	I	JAY	**R07**	**P**	**VCC**	V18	O	SDA1
B07	IO	TRDY#	E18	I	MRXD1	K05	I	JBX	R08	O	IRTX / GPO14	V19	O	SDA0
B08	IO	AD15	E19	I	MRXD0	**K06**	**P**	**GND**	**R09**	**P**	**VCC**	V20	O	SDA2
B09	IO	AD10	E20	I	MRXDV	**K15**	**P**	**VCC**	**R10**	**P**	**VCC**	W01	IOD	EXTSMI# / GPI2
B10	IO	AD04	F01	I	JBB1 / GPI29	**K16**	**P**	**VCCMII**	R11	IO	SD06	W02	O	SUSCLK / GPO4
B11	IO	AD01	F02	I	RSMRST#	K17	O	DRVDEN1	R12	IO	SD00	W03	IO	GPIOE / GPIO31
B12	IO	PINIT# / DIR#	F03	I	INTRUDER#/GPI8	K18	O	MTR0#	**R13**	**P**	**VCC**	W04	O	APICD0 / GPIO28
B13	IO	PD5	F04	I	GPI0	K19	O	DS1#	**R14**	**P**	**VCC**	W05	OD	A20M#
B14	I	ACK# / DS1#	F05	O	RTCX2	K20	O	DIR#	**R15**	**P**	**VCC**	W06	O	MCCS#/O17/strap
B15	O	TXD	F06	IO	FRAME#	L01	AI	UIC5	R16	IO	PDD01	W07	IO	LAD2
B16	I	CTS#	**F07**	**P**	**VCC**	L02	AI	DTD+	R17	IO	PDD14	W08	O	LFRAME#
B17	IO	USBP3-	F08	IO	AD11	L03	AI	DTD-	R18	IO	PDD07	W09	IO	MEMR#
B18	IO	USBP0+	**F09**	**P**	**VCC**	L04	AI	UIC4	R19	IO	PDD09	W10	I	LREQ2#/GPI13/OCHRD
B19	IO	USBP1+	F10	IO	CBE0#	**L05**	**P**	**GNDHWM**	R20	IO	PDD06	W11	O	HGNT1# / GPO8
B20	IO	USBP2+	F11	I	ERROR#/HDSEL#	**L06**	**P**	**VCC**	T01	IO	SMBDT1	W12	IO	SD02
C01	O	PREQH#	**F12**	**P**	**VCC**	**L15**	**P**	**GND**	T02	I	SMBALRT# / GPI7	W13	IO	LA20/OC2#/IO20
C02	I	PINTD#	**F13**	**P**	**VCC**	**L16**	**P**	**VCCPLL**	T03	I	BATLOW# / GPI5	W14	IO	SA09 / SDD09
C03	I	PINTC#	**F14**	**P**	**GNDUSB**	L17	O	DRVDEN0	T04	O	PCISTP# / GPO6	W15	IO	SA04 / SDD04
C04	IO	AD27	**F15**	**P**	**VCC**	L18	O	PDCS1#	T05	OD	NMI	W16	IO	SA12 / SDD12
C05	IO	CBE3#	**F16**	**P**	**VCCMII**	L19	O	PDCS3#	T06	OD	IGNNE#	W17	IO	SA01 / SDD01
C06	IO	AD19	F17	I	MTXCLK	L20	I	INDEX#	T07	IO	IOW# / GPIO23	W18	IO	SA15 / SDD15
C07	IO	IRDY#	F18	I	MRXERR	M01	AI	UIC1	T08	I	IRRX2 / GPIOB	W19	O	SDIOR#
C08	IO	PAR	F19	O	MTXENA	M02	AI	UIC3	T09	O	ROMCS# / KBCS#	W20	O	SDDACK#
C09	IO	AD12	F20	O	MTXD0	M03	AI	UIC2	T10	O	HGNT2# / GPO9	Y01	IO	GPIOD / GPIO30
C10	IO	AD06	G01	O	ACSYNC	M04	IO	KBCK / A20G	T11	IO	SD07	Y02	IO	GPIOA / GPIO24
C11	IO	AD00	G02	O	ACRST#	**M05**	**P**	**VCCHWM**	T12	I	OSC	Y03	I	APICCLK / GPI9
C12	IO	PD1 / TRK00#	G03	I	JAB1 / GPI28	**M06**	**P**	**VCC**	T13	IO	SA17 / strap	Y04	O	APICD1 / GPO29
C13	IO	PD4 / DSKCHG#	G04	I	MSI	**M15**	**P**	**VCC**	T14	I	IRQ14	Y05	OD	SMI#
C14	IO	PD7	G05	O	PCS1# / IO19 / SDIN2	**M16**	**P**	**GNDPLL**	T15	IO	SA08 / SDD08	Y06	O	PCS0# / GPO16
C15	I	USBCLK	**G06**	**P**	**VCC**	M17	I	PCICLK	T16	IO	PDD00	Y07	IO	LAD1
C16	I	RI#	**G07**	**P**	**GND**	M18	O	PDA1	T17	IO	PDD15	Y08	I	LDRQ# / GPI15
C17	IO	USBP3+	**G08**	**P**	**VCC**	M19	O	PDA0	T18	IO	PDD13	Y09	IO	MEMW#
C18	O	EECS#	**G09**	**P**	**VCC**	M20	O	PDA2	T19	IO	PDD03	Y10	O	LGNT1# / GPO10
C19	I	MRXCLK	**G10**	**P**	**VCC**	N01	IO	KBDT / KBRC	T20	IO	PDD12	Y11	I	HREQ1# / GPI10
C20	O	MDCK	**G11**	**P**	**GND**	N02	IO	MSCK / IRQ1	U01	I	PME# / GPI6	Y12	IO	SD03
D01	I	PGNTL#	**G12**	**P**	**VCC**	N03	O	SUSC# / GPO	U02	I	PWRBTN#	Y13	IO	LA21/OC3#/IO21
D02	O	PREQL#	**G13**	**P**	**GNDRAM**	N04	IO	MSDT / IRQ12	U03	I	RING# / GPI3	Y14	IO	SA16 / strap
D03	I	PGNTH#	**G14**	**P**	**GND**	N05	O	SUSST1# / GPO3	U04	OD	CPURST	Y15	IO	SA10 / SDD10
D04	IO	AD29	**G15**	**P**	**VCCRAM**	**N06**	**P**	**VCC**	U05	I	FERR#	Y16	IO	SA03 / SDD03
D05	IO	AD20	G16	I	MCRS	**N15**	**P**	**GND**	U06	OD	SLP# / GPO7	Y17	IO	SA13 / SDD13
D06	IO	CBE2#	G17	I	MCOL	N16	IO	PDD10	U07	IO	IOR# / GPIO22	Y18	IO	SA00 / SDD00
D07	IO	STOP#	G18	O	MTXD1	N17	IO	PDD05	U08	I	IRRX / GPO15	Y19	O	SDIOW#
D08	IO	AD14	G19	O	MTXD2	N18	O	PDIOR#	U09	O	SPKR	Y20	I	SDRDY
D09	IO	AD07	G20	O	MTXD3	N19	I	PDRDY	U10	I	LREQ1# / GPI12			
D10	IO	AD02	H01	I	ACSDIN0	N20	O	PDDACK#	U11	IO	SD05			
D11	IO	PD0 / INDEX#	H02	I	ACSDIN1	P01	O	SUSA#/GPO1/strap	U12	IO	SD04			

Center **GND** pins (24 pins): J8-J13, K8-K13, L8-L13, M8-M13

Figure 4. VT8231 Pin List (Alphabetical Order)

Pin		Pin Name	Pin		Pin Name	Pin		Pin Name	Pin		Pin Name	Pin		Pin Name
W05	OD	A20M#	F11	I	ERROR#/HDSEL#	D18	IO	MDIO	C03	I	PINTC#	P01	O	SUSA# / GPO1
J03	I	ACBITCLK	W01	IOD	EXTSMI# / GPI2	W09	IO	MEMR#	C02	I	PINTD#	P02	O	SUSB# / GPO2
B14	I	ACK# / DS1#	K02	I	FAN1	Y09	IO	MEMW#	U01	I	PME# / GPI6	N03	O	SUSC#
G02	O	ACRST#	K03	I	FAN2/SLPB#/IO18	C19	I	MRXCLK	C01	O	PREQH#	W02	O	SUSCLK
H01	I	ACSDIN0	U05	I	FERR#	E19	I	MRXD0	D02	O	PREQL#	N05	O	SUSST1# / GPO3
H02	I	ACSDIN1	F06	IO	FRAME#	E18	I	MRXD1	U02	I	PWRBTN#	B07	IO	TRDY#
H03	O	ACSDOUT	**G07**	**P**	**GND**	D20	I	MRXD2	E02	I	PWRGD	H16	I	TRK00#
G01	O	ACSYNC	**G11**	**P**	**GND**	D19	I	MRXD3	H20	I	RDATA#	B15	O	TXD
C11	IO	AD00	**G14**	**P**	**GND**	E20	I	MRXDV	C16	I	RI#	M01	I	UIC1
B11	IO	AD01	**H15**	**P**	**GND**	F18	I	MRXERR	U03	I	RING# / GPI3	M03	I	UIC2
D10	IO	AD02	**K06**	**P**	**GND**	N02	IO	MSCK / IRQ1	T09	O	ROMCS#/KBCS#	M02	I	UIC3
E10	IO	AD03	**L15**	**P**	**GND**	N04	IO	MSDT / IRQ12	F02	I	RSMRST#	L04	I	UIC4
B10	IO	AD04	**N15**	**P**	**GND**	G04	I	MSI	E03	I	RTCX1	L01	I	UIC5
A10	IO	AD05	**P07**	**P**	**GND**	J04	O	MSO	F05	O	RTCX2	C15	I	USBCLK
C10	IO	AD06	**P10**	**P**	**GND**	K18	O	MTR0#	A15	O	RTS#	A17	I	USBOC0#
D09	IO	AD07	**P14**	**P**	**GND**	J16	O	MTR1#	E14	I	RXD	D16	I	USBOC1#
E09	IO	AD08	**L05**	**P**	**GNDHWM**	F17	I	MTXCLK	Y18	IO	SA00 / SDD00	A18	IO	USBP0-
A09	IO	AD09	**M16**	**P**	**GNDPLL**	F20	O	MTXD0	W17	IO	SA01 / SDD01	B18	IO	USBP0+
B09	IO	AD10	**G13**	**P**	**GNDRAM**	G18	O	MTXD1	V16	IO	SA02 / SDD02	A19	IO	USBP1-
F08	IO	AD11	**F14**	**P**	**GNDUSB**	G19	O	MTXD2	Y16	IO	SA03 / SDD03	B19	IO	USBP1+
C09	IO	AD12	F04	I	GPI0	G20	O	MTXD3	W15	IO	SA04 / SDD04	A20	IO	USBP2-
E08	IO	AD13	V03	I	GPI1 / IRQ8#	F19	O	MTXENA	V14	IO	SA05 / SDD05	B20	IO	USBP2+
D08	IO	AD14	Y02	IO	GPIOA / GPIO24	T05	OD	NMI	U16	IO	SA06 / SDD06	B17	IO	USBP3-
B08	IO	AD15	J05	IO	GPIOC / GPIO25	T12	I	OSC	U15	IO	SA07 / SDD07	C17	IO	USBP3+
A06	IO	AD16	Y01	IO	GPIOD / GPIO30	C08	IO	PAR	T15	IO	SA08 / SDD08	**E01**	**P**	**VBAT**
E06	IO	AD17	W03	IO	GPIOE	R05	IO	PCKRUN#	W14	IO	SA09 / SDD09	**F07**	**P**	**VCC**
B06	IO	AD18	H19	O	HDSEL#	M17	I	PCICLK	Y15	IO	SA10 / SDD10	**F09**	**P**	**VCC**
C06	IO	AD19	W11	O	HGNT1# / GPO8	E04	O	PCIRST#	V15	IO	SA11 / SDD11	**F12**	**P**	**VCC**
D05	IO	AD20	T10	O	HGNT2# / GPO9	T04	O	PCISTP# / GPO6	W16	IO	SA12 / SDD12	**F13**	**P**	**VCC**
A05	IO	AD21	Y11	I	HREQ1# / GPI10	Y06	O	PCS0# / GPO16	Y17	IO	SA13 / SDD13	**F15**	**P**	**VCC**
E05	IO	AD22	V11	I	HREQ2# / GPI11	G05	O	PCS1# /	V17	IO	SA14 / SDD14	**G06**	**P**	**VCC**
B05	IO	AD23	T06	OD	IGNNE#	D11	IO	PD0/INDEX#	W18	IO	SA15 / SDD15	**G08**	**P**	**VCC**
A04	IO	AD24	L20	I	INDEX#	C12	IO	PD1/TRK00#	Y14	IO	SA16 / strap	**G09**	**P**	**VCC**
B04	IO	AD25	V05	OD	INIT#	A12	IO	PD2/WRTPRT#	T13	IO	SA17 / strap	**G10**	**P**	**VCC**
A03	IO	AD26	R06	OD	INTR	E12	IO	PD3/RDATA#	U13	IO	SA18	**G12**	**P**	**VCC**
C04	IO	AD27	F03	I	INTRUDER#/GPI8	C13	IO	PD4/DSKCHG#	V13	IO	SA19	**H06**	**P**	**VCC**
B03	IO	AD28	U07	IO	IOR# / GPIO22	B13	IO	PD5	R12	IO	SD00	**J06**	**P**	**VCC**
D04	IO	AD29	T07	IO	IOW# / GPIO23	A13	IO	PD6	V12	IO	SD01	**J15**	**P**	**VCC**
A01	IO	AD30	C07	IO	IRDY#	C14	IO	PD7	W12	IO	SD02	**K15**	**P**	**VCC**
A02	IO	AD31	T14	I	IRQ14	M19	O	PDA0	Y12	IO	SD03	**L06**	**P**	**VCC**
P03	I	AOLGPI/THRM/I17	U14	I	IRQ15	M18	O	PDA1	U12	IO	SD04	**M06**	**P**	**VCC**
Y03	O	APICLK / GPI9	U08	I	IRRX / GPO15	M20	O	PDA2	U11	IO	SD05	**M15**	**P**	**VCC**
W04	O	APICD0 / GPIO28	T08	I	IRRX2 / GPIOB	L18	O	PDCS1#	R11	IO	SD06	**N06**	**P**	**VCC**
Y04	O	APICD1 / GPIO29	R08	O	IRTX / GPO14	L19	O	PDCS3#	T11	IO	SD07	**P08**	**P**	**VCC**
E11	IO	AUTOFD# / DRV0	G03	I	JAB1 / GPI28	T16	IO	PDD00	V19	O	SDA0	**P09**	**P**	**VCC**
T03	I	BATLOW# / GPI5	H05	I	JAB2 / GPO12	R16	IO	PDD01	V18	O	SDA1	**P11**	**P**	**VCC**
A14	I	BUSY / MTR1#	J01	I	JAX	U20	IO	PDD02	V20	O	SDA2	**P12**	**P**	**VCC**
F10	IO	CBE0#	K04	I	JAY	T19	IO	PDD03	U18	O	SDCS1#	**P13**	**P**	**VCC**
A08	IO	CBE1#	F01	I	JBB1 / GPI29	P16	IO	PDD04	U19	O	SDCS3#	**P15**	**P**	**VCC**
D06	IO	CBE2#	H04	I	JBB2 / GPO13	N17	IO	PDD05	W20	O	SDDACK#	**R07**	**P**	**VCC**
C05	IO	CBE3#	K05	I	JBX	R20	IO	PDD06	U17	I	SDDRQ	**R09**	**P**	**VCC**
V01	I	CPUMISS / GPI16	J02	I	JBY	R18	IO	PDD07	W19	O	SDIOR#	**R10**	**P**	**VCC**
U04	OD	CPURST	M04	IO	KBCK / A20G	P18	IO	PDD08	Y19	O	SDIOW#	**R13**	**P**	**VCC**
P04	O	CPUSTP# / GPO5	N01	IO	KBDT / KBRC	R19	IO	PDD09	Y20	I	SDRDY	**R14**	**P**	**VCC**
B16	I	CTS#	W13	IO	LA20/OC2#/GPIO20	N16	IO	PDD10	V09	I	SERIRQ	**R15**	**P**	**VCC**
D15	I	DCD#	Y13	IO	LA21/OC3#/GPIO21	P17	IO	PDD11	E07	I	SERR#	**M05**	**P**	**VCCHWM**
A07	IO	DEVSEL#	V08	IO	LAD0	T20	IO	PDD12	E13	I	SLCT/WGATE#	**F16**	**P**	**VCCMII**
K20	O	DIR#	Y07	IO	LAD1	T18	IO	PDD13	D12	IO	SLCTIN#/STEP#	**K16**	**P**	**VCCMII**
L17	O	DRVDEN0	W07	IO	LAD2	R17	IO	PDD14	R04	O	SLOWCLK / O0	**L16**	**P**	**VCCPLL**
K17	O	DRVDEN1	V07	IO	LAD3	T17	IO	PDD15	U06	OD	SLP# / GPO7	**G15**	**P**	**VCCRAM**
J17	O	DS0#	Y08	I	LDRQ#/ / GPI15	N20	O	PDDACK#	T02	I	SMBALRT# / I7	**P05**	**P**	**VCCSUS**
K19	O	DS1#	W08	O	LFRAME#	P19	I	PDDRQ	R03	IO	SMBCK1	**P06**	**P**	**VCCSUS**
H18	I	DSKCHG#	Y10	O	LGNT1# / GPO10	N18	O	PDIOR#	R01	IO	SMBCK2 / IO27	**E15**	**P**	**VCCUSB**
D14	I	DSR#	V10	O	LGNT2# / GPO11	P20	O	PDIOW#	T01	IO	SMBDT1	**K01**	**O**	**VREF**
L02	AI	DTD+	V02	I	LID / GPI4	N19	I	PDRDY	R02	IO	SMBDT2 / IO26	J19	O	WDATA#
L03	AI	DTD–	U10	I	LREQ1# / GPI12	D13	I	PE / WDATA#	Y05	OD	SMI#	J20	O	WGATE#
A16	O	DTR#	W10	I	LREQ2#/GPI13/IOCHRD	D03	I	PGNTH#	U09	O	SPKR	H17	I	WRTPRT#
E16	O	EECK	W06	O	MCCS#/O17/strap	D01	I	PGNTL#	J18	O	STEP#	V04	I	WSC# / GPI14
C18	O	EECS#	G17	I	MCOL	B12	IO	PINIT# / DIR#	D07	IO	STOP#			
E17	I	EEDI	G16	I	MCRS	B02	I	PINTA#	V06	OD	STPCLK#			
D17	O	EEDO	C20	O	MDCK	B01	I	PINTB#	A11	IO	STROBE#			

Center **GND** pins (24 pins): J8-J13, K8-K13, L8-L13, M8-M13

Pin Descriptions

Table 1. Pin Descriptions

PCI Bus Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
AD[31:0]	(see pin list)	IO	**Address/Data Bus.** The standard PCI address and data lines. The address is driven with FRAME# assertion and data is driven or received in following cycles. IDSEL is internally connected to AD28.
C/BE[3:0]#	C5, D6, A8, F10	IO	**Command/Byte Enable.** The command is driven with FRAME# assertion. Byte enables corresponding to supplied or requested data are driven on following clocks.
FRAME#	F6	IO	**Frame.** Assertion indicates the address phase of a PCI transfer. Negation indicates that one more data transfer is desired by the cycle initiator.
IRDY#	C7	IO	**Initiator Ready.** Asserted when the initiator is ready for data transfer.
TRDY#	B7	IO	**Target Ready.** Asserted when the target is ready for data transfer.
STOP#	D7	IO	**Stop.** Asserted by the target to request the master to stop the current transaction.
DEVSEL#	A7	IO	**Device Select.** The VT8231 asserts this signal to claim PCI transactions through positive or subtractive decoding. As an input, DEVSEL# indicates the response to a VT8231-initiated transaction and is also sampled when decoding whether to subtractively decode the cycle.
PAR	C8	IO	**Parity.** A single parity bit is provided over AD[31:0] and C/BE[3:0]#.
SERR#	E7	I	**System Error.** SERR# can be pulsed active by any PCI device that detects a system error condition. Upon sampling SERR# active, the VT8231 can be programmed to generate an NMI to the CPU.
PINTA-D#	B2, B1, C3, C2	I	**PCI Interrupt Request**. These pins are typically connected to the PCI bus INTA#-INTD# pins as follows: PCI Slot 1: PINTA# INTA#, PINTB# INTB#, PINTC# INTC#, PINTD# INTD# PCI Slot 2: INTB#, INTC#, INTD#, INTA# PCI Slot 3: INTC#, INTD#, INTA#, INTB# PCI Slot 4: INTD#, INTA#, INTB#, INTC# PCI Slot 5: INTA#, INTB#, INTC#, INTD#
PCICLK	M17	I	**PCI Clock.** PCLK provides timing for all transactions on the PCI Bus.
PCKRUN#	R5	IO	**PCI Bus Clock Run.** This signal indicates whether the PCI clock is or will be stopped (high) or running (low). The VT8231 drives this signal low when the PCI clock is running (default on reset) and releases it when it stops the PCI clock. External devices may assert this signal low to request that the PCI clock be restarted or prevent it from stopping. Connect this pin to ground using a 100 Ω resistor if the function is not used. Refer to the "PCI Mobile Design Guide" and the VIA "Apollo MVP4 Design Guide" for more details.
PCIRST#	E4	O	**PCI Reset.**
PCISTP# / GPO6	T4	O	**PCI Stop.**
CPUSTP# / GPO5	P4	O	**CPU Stop.**

PCI Bus Interface (continued)			
Signal Name	**Pin #**	**I/O**	**Signal Description**
PREQH#	C1	O	**PCI Request.** This signal goes to the North Bridge REQ4# input to request the PCI bus for high priority access. The internal LAN requests the PCI bus using this signal, so if the LAN subsystem is used, this signal must be connected (one of the H/LREQ/GNT 1 and 2 pairs provided by the VT8231 may be used to implement the fifth PCI slot if desired). If the LAN subsystem is not used, PREQH# / PGNTH# may optionally remain unconnected.
PGNTH#	D3	I	**PCI Grant.** This signal is driven by the North Bridge GNT4# signal to grant high priority PCI access to the VT8231.
PREQL#	D2	O	**PCI Request.** This signal goes to the North Bridge PREQ# input to request the PCI bus for normal priority access.
PGNTL#	D1	I	**PCI Grant.** This signal is driven by the North Bridge PGNT# output to grant normal priority PCI access to the VT8231.
HREQ1# / GPI10	Y11	I / IO	**High Priority Request 1.** Device 0 Function 4 RxE5[3] = 1.
HGNT1# / GPO8	W11	O / IO	**High Priority Grant 1.** Device 0 Function 4 RxE5[3] = 1.
HREQ2# / GPI11	V11	I / IO	**High Priority Request 2.** Device 0 Function 4 RxE5[3] = 1.
HGNT2# / GPO9	T10	O / IO	**High Priority Grant 2.** Device 0 Function 4 RxE5[3] = 1.
LREQ1# / GPI12	U10	I / IO	**Low Priority Request 1.** Device 0 Function 4 RxE5[2] = 1.
LGNT1# / GPO10	Y10	O / IO	**Low Priority Grant 1.** Device 0 Function 4 RxE5[2] = 1.
LREQ2# / GPI13 / IOCHRDY	W10	I / IO	**Low Priority Request 2.** Device 0 Func 4 RxE5[2]=1, Func 0 Rx67[3]=0
LGNT2# / GPO11	V10	O / IO	**Low Priority Grant 2.** Device 0 Function 4 RxE5[2] = 1.

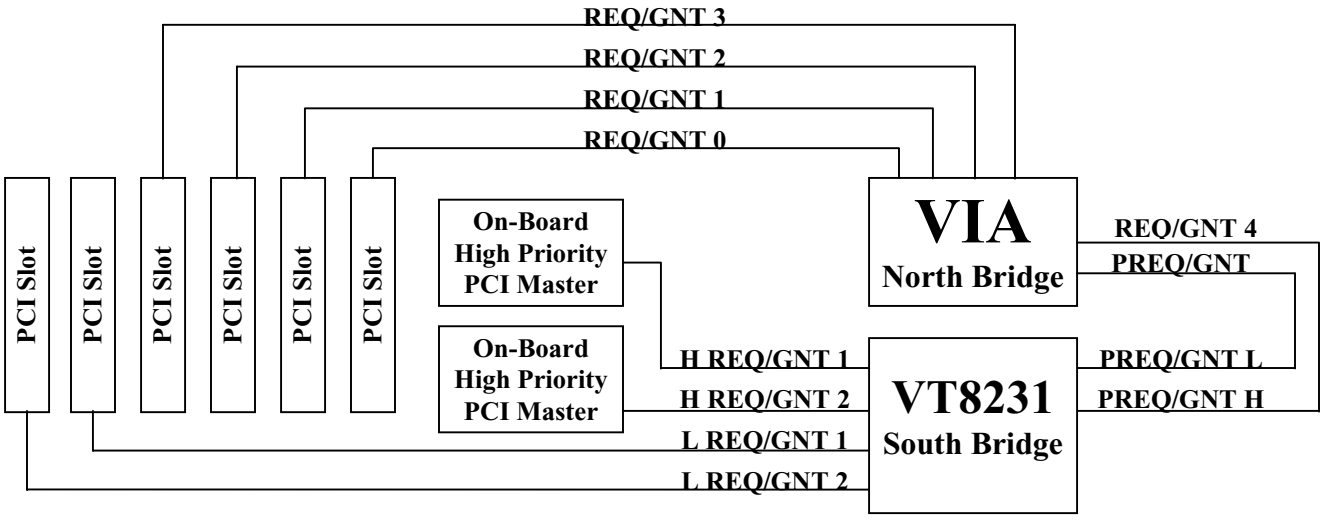

Figure 5. PCI Request / Grant Connections Using the VT8231

CPU Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
CPURST	U4	OD	**CPU Reset.** The VT8231 asserts CPURST to reset the CPU during power-up.
INTR	R6	OD	**CPU Interrupt.** INTR is driven by the VT8231 to signal the CPU that an interrupt request is pending and needs service.
NMI	T5	OD	**Non-Maskable Interrupt.** NMI is used to force a non-maskable interrupt to the CPU. The VT8231 generates an NMI when either SERR# or IOCHK# is asserted.
INIT#	V5	OD	**Initialization.** The VT8231 asserts INIT# if it detects a shut-down special cycle on the PCI bus or if a soft reset is initiated by the register. See strap on SUSA# / GPO1 for polarity selection.
STPCLK#	V6	OD	**Stop Clock.** STPCLK# is asserted by the VT8231 to the CPU to throttle the processor clock.
SMI#	Y5	OD	**System Management Interrupt.** SMI# is asserted by the VT8231 to the CPU in response to different Power-Management events.
FERR#	U5	I	**Numerical Coprocessor Error.** This signal is tied to the coprocessor error signal on the CPU. Internally generates interrupt 13 if active. A threshold of 1.5V or 2.5V is selectable via Device 0 Function 0 Rx67[2].
IGNNE#	T6	OD	**Ignore Numeric Error.** This pin is connected to the "ignore error" pin on the CPU.
SLP# / GPO7	U6	OD	**Sleep** (F4 RxE4[4] = 1). Used to put the CPU to sleep. Used with slot-1 CPUs only. Not currently used with socket-7 CPUs.
A20M#	W5	OD	**A20 Mask.** Connect to A20 mask input of the CPU to control address bit-20 generation. Logical combination of the A20GATE input (from internal or external keyboard controller) and Port 92 bit-1 (Fast A20). See Device 0 Function 0 Rx59[1].
DTD+	L2	Analog I	**CPU DTD (Thermal Diode) Channel Plus.** Connect to cathode of first external temperature sensing diode.
DTD-	L3	Analog I	**CPU DTD (Thermal Diode) Channel Minus.** Connect to anode of first external temperature sensing diode.

Note: Connect each of the above signals to 4.7K Ω pullup resistors to VCC3.

Strap Options			
Signal Name	**Pin #**	**I/O**	**Signal Description**
Strap / SUSA# / GPO1	P1	I / O	**CPURST / INIT# Polarity** H: Slot-1 / Socket-370 / Slot-A / Socket-A L: Socket-7
Strap / MCCS# / GPO17	W6	I / O	**CPU Frequency Strapping** H: Disable L: Enable
Strap / SA16	Y14	I / IO	**BIOS ROM Interface** H: LPC L: Conventional
Strap / SA17	T13	I / IO	**Auto Reboot** H: Disable (recommended) L: Enable

Note: External strap option values may be set by connecting the indicated external pin to a 4.7K ohm pullup (for 1 or H) or driving it low during reset with a 7407 TTL open collector buffer (for 0 or L) as shown in the suggested circuit below:

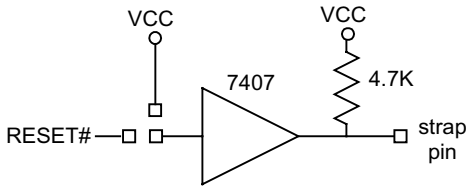

Figure 6. Strap Option Circuit

Advanced Programmable Interrupt Controller (APIC) Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
WSC# / GPI14	V4	I / I	**Internal APIC Write Snoop Complete.** F0 Rx58[6] = 1. Asserted by the north bridge to indicate that all snoop activity on the CPU bus initiated by the last PCI-to-DRAM write is complete and that it is safe to perform an APIC interrupt.
APICD0 / GPO28	W4	O / O	**Internal APIC Data 0.** F0 Rx58[6] = 1.
APICD1 / GPO29	Y4	O / O	**Internal APIC Data 1.** F0 Rx58[6] = 1.
APICCLK / GPI9	Y3	I / I	**APIC Clock.** F0 Rx58[6] = 1.

Low Pin Count (LPC) Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
LFRAME#	W8	O	**LPC Frame.**
LDRQ# / GPI15	Y8	I / I	**LPC Data Request.** F0 Rx58[5] = 1 and F4 RxE5[7] = 0.
LAD[3-0]	V7, W7, Y7, V8	IO	**LPC Address / Data.**

Note: For LPC control, see Device 0 Function 0 Rx58[5] and Rx59[4-3]
Note: Connect the LPC interface LPCRST# (LPC Reset) signal to PCIRST#

LAN Controller - Media Independent Interface (MII)			
Signal Name	**Pin #**	**I/O**	**Signal Description**
MCOL	G17	I	**MII Collision Detect.** From the external PHY.
MCRS	G16	I	**MII Carrier Sense.** Asserted by the external PHY when the media is active.
MDCK	C20	O	**MII Management Data Clock.** Sent to the external PHY as a timing reference for MDIO
MDIO	D18	IO	**MII Management Data I/O.** Read from the MDI bit or written to the MDO bit.
MRXCLK	C19	I	**MII Receive Clock.** 2.5 or 25 MHz clock recovered by the PHY.
MRXD[3], **MRXD[2]**, **MRXD[1]**, **MRXD[0]**	D19 D20 E18 E19	I I I I	**MII Receive Data.** Parallel receive data lines driven by the external PHY synchronous with MRXCLK.
MRXDV	E20	I	**MII Receive Data Valid.**
MRXERR	F18	I	**MII Receive Error.** Asserted by the PHY when it detects a data decoding error.
MTXCLK	F17	I	**MII Transmit Clock.** Always active 2.5 or 25 MHz clock supplied by the PHY.
MTXD[3], **MTXD[2]**, **MTXD[1]**, **MTXD[0]**	G20 G19 G18 F20	O O O O	**MII Transmit Data.** Parallel transmit data lines synchronized to MTXCLK.
MTXENA	F19	O	**MII Transmit Enable.** Indicates transmit active from the MII port to the PHY.

The internal LAN controller uses the high priority PCI bus request / grant pair (PREQH# / PGNTH#) to request PCI bus access from the chipset north bridge.

Serial EEPROM Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
EECS#	C18	O	**Serial EEPROM Chip Select.**
EECK	E16	O	**Serial EEPROM Clock.**
EEDO	D17	O	**Serial EEPROM Data Output.**
EEDI	E17	I	**Serial EEPROM Data Input.**

Universal Serial Bus Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
USBP0+	B18	IO	**USB Port 0 Data +**
USBP0-	A18	IO	**USB Port 0 Data -**
USBP1+	B19	IO	**USB Port 1 Data +**
USBP1-	A19	IO	**USB Port 1 Data -**
USBP2+	B20	IO	**USB Port 2 Data +**
USBP2-	A20	IO	**USB Port 2 Data -**
USBP3+	C17	IO	**USB Port 3 Data +**
USBP3-	B17	IO	**USB Port 3 Data -**
USBCLK	C15	I	**USB Clock.** 48MHz clock input for the USB interface
USBOC0#	A17	I	**USB Port 0 Over Current Detect.** Port 0 is disabled if this input is low.
USBOC1#	D16	I	**USB Port 1 Over Current Detect.** Port 1 is disabled if this input is low
USBOC2# / LA20 / GPI20 / GPO20	W13	I / IO / I / O	**USB Port 2 Over Current Detect.** Port 2 is disabled if this input is low. Device 0 Function 4 RxE4[6] = 0 and Power Management I/O Rx4E[4] = 1
USBOC3# / LA21 / GPI21 / GPO21	Y13	I / IO / I / O	**USB Port 3 Over Current Detect.** Port 3 is disabled if this input is low. Device 0 Function 4 RxE4[6] = 0 and Power Management I/O Rx4E[5] = 1

For USB interface configuration and control see also Functions 2 and 3 plus Function 0 Rx48[3-2], 4A[1], 4D[1-0], 50[5-4]

System Management Bus (SMB) Interface (I^2C Bus)			
Signal Name	**Pin #**	**I/O**	**Signal Description**
SMBCK1	R3	IO	**SMB / I^2C Channel 1 Clock.**
SMBCK2 / GPIO27	R1	IO / IO	**SMB / I^2C Channel 2 Clock†.** F4 Rx55[3] = 0.
SMBDT1	T1	IO	**SMB / I^2C Channel 1 Data.**
SMBDT2 / GPIO26	R2	IO / IO	**SMB / I^2C Channel 2 Data†.** F4 Rx55[3] = 0.
SMBALRT# / GPI7	T2	I / I	**SMB Alert.** (System Management Bus I/O space Rx08[3] = 1) When the chip is enabled to allow it, assertion generates an IRQ or SMI interrupt or a power management resume event. The same pin is used as General Purpose Input 6 whose value is reflected in Rx48[6] of function 4 I/O space

For SMB interface configuration and control see also Function 4 Rx54[7], 55[3-2], 56[4], 90-93, D2-D6 plus SMB I/O Rx0-F, HWM I/O Rx48, and PMIO Rx45[1-0]

† Note: SMBus #2 is a slave-only device used to supply status for external Alert-On-LAN (AOL)

UltraDMA-33 / 66 / 100 Enhanced IDE Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
PDRDY / PDDMARDY / PDSTROBE	N19	I	EIDE Mode: **Primary I/O Channel Ready.** Device ready indicator UltraDMA Mode: **Primary Device DMA Ready**. Output flow control. The device may assert DDMARDY to pause output transfers **Primary Device Strobe**. Input data strobe (both edges). The device may stop DSTROBE to pause input data transfers
SDRDY / SDDMARDY / SDSTROBE	Y20	I	EIDE Mode: **Secondary I/O Channel Ready.** Device ready indicator UltraDMA Mode: **Secondary Device DMA Ready**. Output flow control. The device may assert DDMARDY to pause output transfers **Secondary Device Strobe**. Input data strobe (both edges). The device may stop DSTROBE to pause input data transfers
PDIOR# / PHDMARDY / PHSTROBE	N18	O	EIDE Mode: **Primary Device I/O Read.** Device read strobe UltraDMA Mode: **Primary Host DMA Ready**. Primary channel input flow control**.** The host may assert HDMARDY to pause input transfers **Primary Host Strobe**. Output data strobe (both edges). The host may stop HSTROBE to pause output data transfers
SDIOR# / SHDMARDY / SHSTROBE	W19	O	EIDE Mode: **Secondary Device I/O Read.** Device read strobe UltraDMA Mode: **Secondary Host DMA Ready**. Input flow control. The host may assert HDMARDY to pause input transfers **Host Strobe B**. Output strobe (both edges). The host may stop HSTROBE to pause output data transfers
PDIOW# / PSTOP	P20	O	EIDE Mode: **Primary Device I/O Write.** Device write strobe UltraDMA Mode: **Primary Stop**. Stop transfer: Asserted by the host prior to initiation of an UltraDMA burst; negated by the host before data is transferred in an UltraDMA burst. Assertion of STOP by the host during or after data transfer in UltraDMA mode signals the termination of the burst.
SDIOW# / SSTOP	Y19	O	EIDE Mode: **Secondary Device I/O Write.** Device write strobe UltraDMA Mode: **Secondary Stop**. Stop transfer: Asserted by the host prior to initiation of an UltraDMA burst; negated by the host before data is transferred in an UltraDMA burst. Assertion of STOP by the host during or after data transfer in UltraDMA mode signals the termination of the burst.
PDDRQ	P19	I	**Primary Device DMA Request.** Primary channel DMA request
SDDRQ	U17	I	**Secondary Device DMA Request.** Secondary channel DMA request
PDDACK#	N20	O	**Primary Device DMA Acknowledge.** Primary channel DMA acknowledge
SDDACK#	W20	O	**Secondary Device DMA Acknowledge.** Secondary channel DMA acknowledge
IRQ14	T14	I	**Primary Channel Interrupt Request.**
IRQ15	U14	I	**Secondary Channel Interrupt Request.**

UltraDMA-33 / 66 / 100 Enhanced IDE Interface (continued)			
Signal Name	**Pin #**	**I/O**	**Signal Description**
PDCS1#	L18	O	**Primary Master Chip Select.** This signal corresponds to CS1FX# on the primary IDE connector.
PDCS3#	L19	O	**Primary Slave Chip Select.** This signal corresponds to CS3FX# on the primary IDE connector.
SDCS1#	U18	O	**Secondary Master Chip Select.** This signal corresponds to CS17X# on the secondary IDE connector.
SDCS3#	U19	O	**Secondary Slave Chip Select.** This signal corresponds to CS37X# on the secondary IDE connector.
PDA[2-0]	M20, M18, M19	O	**Primary Disk Address.** PDA[2:0] are used to indicate which byte in either the ATA command block or control block is being accessed.
SDA[2-0]	V20, V18, V19	O	**Secondary Disk Address.** SDA[2:0] are used to indicate which byte in either the ATA command block or control block is being accessed.
PDD[15-0]	T17, R17, T18, T20, P17, N16, R19, P18, R18, R20, N17, P16, T19, U20, R16, T16	IO	**Primary Disk Data**
SDD[15-0] / SA[15-0]	W18, V17, Y17, W16, V15, Y15, W14, T15, U15, U16, V14, W15, Y16, V16, W17, Y18	IO	**Secondary Disk Data / ISA Address**

For IDE / UDMA interface configuration and control see also Function 1 plus Function 0 Rx48[1-0], 4A[0], 4C, 50[3] 7C[5-4]

MIDI Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
MSI	G4	I	**MIDI Serial In**
MSO	J4	O	**MIDI Serial Out**

For MIDI interface configuration and control see also SuperIO RxF9[0], Function 0 Rx6D[2-0], Function 4 Rx40[0], Function 5 Rx18 and I/O Base 2 Rx0, and Function 5/6 Rx42[7,6,1], 43[3-2]

AC97 Audio / Modem Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
ACRST#	G2	O	**AC97 Reset**
ACSYNC	G1	O	**AC97 Sync**
ACSDOUT	H3	O	**AC97 Serial Data Out**
ACSDIN0	H1	I	**AC97 Serial Data In 0**
ACSDIN1	H2	I	**AC97 Serial Data In 1**
ACBITCLK	J3	I	**AC97 Bit Clock**

For AC97 interface configuration and control see also Functions 5 and 6 plus Function 0 Rx4D[3-2], 50[7-6], PMIO Rx20[13].

Game Port Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
JAX	J1	I	**Joystick A X-axis**
JAY	K4	I	**Joystick A Y-axis**
JBX	K5	I	**Joystick B X-axis**
JBY	J2	I	**Joystick B Y-axis**
JAB1 / GPI28	G3	I	**Joystick A Button 1.**
JAB2 / GPO12	H5	I	**Joystick A Button 2.** Device 0 Function 4 RxE5[4] = 1.
JBB1 / GPI29	F1	I	**Joystick B Button 1.**
JBB2 / GPO13	H4	I	**Joystick B Button 2.** Device 0 Function 4 RxE5[4] = 1.

For Game Port interface configuration and control see also Game Port I/O registers (port 201h), Function 0 Rx6D[3], Function 4 Rx40[2], and Function 5/6 Rx42[3] and 4A

Floppy Disk Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
DRVDEN0	L17	O	**Drive Density Select 0.**
DRVDEN1	K17	O	**Drive Density Select 1.**
MTR0#	K18	O	**Motor Control 0.** Select motor on drive 0.
MTR1#	J16	O	**Motor Control 1.** Select motor on drive 1
DS0#	J17	O	**Drive Select 0.** Select drive 0.
DS1#	K19	O	**Drive Select 1.** Select drive 1
DIR#	K20	O	**Direction.** Direction of head movement (0 = inward motion, 1 = outward motion)
STEP#	J18	O	**Step.** Low pulse for each track-to-track movement of the head.
INDEX#	L20	I	**Index.** Sense to detect that the head is positioned over the beginning of a track
HDSEL#	H19	O	**Head Select.** Selects the side for R/W operations (0 = side 1, 1 = side 0)
TRK00#	H16	I	**Track 0.** Sense to detect that the head is positioned over track 0.
RDATA#	H20	I	**Read Data.** Raw serial bit stream from the drive for read operatrions.
WDATA#	J19	O	**Write Data.** Encoded data to the drive for write operations.
WGATE#	J20	O	**Write Gate.** Signal to the drive to enable current flow in the write head.
DSKCHG#	H18	I	**Disk Change.** Sense that the drive door is open or the diskette has been changed since the last drive selection.
WRTPRT#	H17	I	**Write Protect.** Sense for detection that the diskette is write protected (causes write commands to be ignored)

See also Parallel Port pin descriptions for optional Floppy Disk interface functionality

Parallel Port Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
PINIT# / DIR#	B12	IO / O	**Initialize.** Initialize printer. Output in standard mode, I/O in ECP/EPP mode.
STROBE# / nc	A11	IO / -	**Strobe.** Output used to strobe data into the printer. I/O in ECP/EPP mode.
AUTOFD# / DRVEN0	E11	IO / O	**Auto Feed.** Output used to cause the printer to automatically feed one line after each line is printed. I/O pin in ECP/EPP mode.
SLCTIN# / STEP#	D12	IO / O	**Select In.** Output used to select the printer. I/O pin in ECP/EPP mode.
SLCT / WGATE#	E13	I / O	**Select.** Status output from the printer. High indicates that it is powered on.
ACK# / DS1#	B14	I / O	**Acknowledge.** Status output from the printer. Low indicates that it has received the data and is ready to accept new data
ERROR# / HDSEL#	F11	I / O	**Error.** Status output from the printer. Low indicates an error condition in the printer.
BUSY / MTR1#	A14	I / O	**Busy.** Status output from the printer. High indicates not ready to accept data.
PE / WDATA#	D13	I / O	**Paper End.** Status output from the printer. High indicates that it is out of paper.
PD7 / nc, **PD6** / nc, **PD5** / nc, **PD4** / DSKCHG#, **PD3** / RDATA#, **PD2** / WRTPRT#, **PD1** / TRK00#, **PD0** / INDEX#	C14 A13 B13 C13 E12 A12 C12 D11	IO / - IO / - IO / - IO / I IO / I IO / I IO / I IO / I	**Parallel Port Data.**

As shown by the alternate functions above, in mobile applications the parallel port pins can optionally be selected to function as a floppy disk interface for attachment of an external floppy drive using the parallel port connector (see Super I/O Configuration Index F6[5]).

Serial Port and Infrared Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
TXD	B15	O	**Transmit Data.** Serial port transmit data out.
RXD	E14	I	**Receive Data.** Serial port receive data in.
IRTX / GPO14	R8	O / O	**Infrared Transmit.** IR transmit data out (Function 4 RxE5[5] = 0).
IRRX / GPO15	U8	I / O	**Infrared Receive.** IR receive data in (Function 4 RxE5[5] = 0).
IRRX2 / GPIOB	T8	I	**Infrared Receive.** IR receive data in (see FIR I/O Rx33 and 34)
RTS#	A15	O	**Request To Send.** Indicator that the serial output port is ready to transmit data. Typically used as hardware handshake with CTS# for low level flow control. Designed for direct input to external RS-232C driver.
CTS#	B16	I	**Clear To Send.** Indicator to the serial port that an external communications device is ready to receive data. Typically used as hardware handshake with RTS# for low level flow control. Designed for input from external RS-232C receiver.
DTR#	A16	O	**Data Terminal Ready.** Indicator that serial port is powered, initialized, and ready. Typically used as hardware handshake with DSR# for overall readiness to communicate. Designed for direct input to external RS-232C driver.
DSR#	D14	I	**Data Set Ready.** Indicator to serial port that an external serial communications device is powered, initialized, and ready. Typically used as hardware handshake with DTR# for overall readiness to communicate. Designed for direct input from external RS-232C receiver.
DCD#	D15	I	**Data Carrier Detect.** Indicator to serial port that an external modem is detecting a carrier signal (i.e., a communications channel is currently open). In direct connect environments, this input will typically be driven by DTR# as part of the DTR/DSR handshake. Designed for direct input from external RS-232C receiver.
RI#	C16	I	**Ring Indicator.** Indicator to serial port that an external modem is detecting a ring condition. Used by software to initiate operations to answer and open the communications channel. Designed for direct input from external RS-232C receiver (whose input is typically not connected in direct connect environments).

Conventional BIOS ROM / ISA Bus Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
LA21 / USBOC3# / GPI21 / GPO21 **LA20** / USBOC2# / GPI20 / GPO20	Y13 W13	O O	**System Address Bus**. Allows access to physical memory devices (e.g., BIOS ROMs) up to 4 Mbytes. F4 RxE4[6] = 1.
SA[19:18], **SA17** / strap, **SA16** / strap, **SA[15:0]** / SDD[15:0]	V13, U13, T13, Y14, W18, V17, Y17, W16, V15, Y15, W14, T15, U15, U16, V14, W15, Y16, V16, W17, Y18	IO	**System Address Bus**. These address lines are used to interface to BIOS ROMs but may also be used to implement a subset of the ISA bus if required. SA[19-16] are connected to ISA bus SA[19-16] directly. SA[19-17] are also connected to LA[19-17] of the ISA bus. SA17 strap – 0/1 = Enable / Disable Auto Reboot SA16 strap – 0/1 = Disable / Enable LPC ROM
SD[7-0]	T11, R11, U11, U12, Y12, W12, V12, R12	IO	**System Data.** SD[7:0] provide the data path for BIOS ROMs and other 8-bit devices residing on the ISA bus.
IOR# / GPI22 / GPO22	U7	IO	**I/O Read** (Function 4 RxE4[7] = 1.). Command to ISA I/O slave devices to indicate that the slave may drive data on to the ISA data bus.
IOW# / GPI23 / GPO23	T7	IO	**I/O Write** (Function 4 RxE4[7] = 1.). Command to ISA I/O slave devices to indicate that the slave may latch data from the ISA data bus.
MEMR#	W9	IO	**Memory Read.** Command to memory slave to indicate that it may drive data onto the ISA data bus.
MEMW#	Y9	IO	**Memory Write.** Command to memory slave to indicate that it may latch data from the ISA data bus.
IOCHRDY / LREQ2# / GPI13	W10	I	**I/O Channel Ready** (Function 0 Rx67[3] = 1). Normally pulled high on the motherboard. Devices on the ISA Bus assert IOCHRDY low to indicate that additional time (wait states) is required to complete the cycle.
IRQ1 / MSCK	N2	I	**Interrupt 1 (optional external Keyboard Controller).**
IRQ8# / GPI1	V3	I	**Interrupt 8 (optional external RTC).** Enabled if Rx51[3] = 0.
IRQ12 / MSDT	N4	I	**Interrupt 12 (optional external PS2 Mouse Controller).**
IRQ14	T14	I	**Interrupt 14 (IDE Primary Channel).**
IRQ15	U14	I	**Interrupt 15 (IDE Secondary Channel).**
SPKR	U9	O	**Speaker Drive.** Output of internal timer/counter 2.

Serial IRQ			
Signal Name	**Pin #**	**I/O**	**Signal Description**
SERIRQ	V9	I	**Serial IRQ.**

Internal Keyboard Controller			
Signal Name	**Pin #**	**I/O**	**Signal Description**
MSCK / IRQ1	N2	IO / I	**MultiFunction Pin** (Internal mouse controller enabled by F0 Rx51[2]) Rx51[2]=1 **Mouse Clock.** From internal mouse controller. Rx51[2]=0 **Interrupt Request 1**. Interrupt 1 (external KBC).
MSDT / IRQ12	N4	IO / I	**MultiFunction Pin** (Internal mouse controller enabled by F0 Rx51[2]) Rx51[2]=1 **Mouse Data.** From internal mouse controller. Rx51[2]=0 **Interrupt Request 12**. Interrupt 12 (ext PS2 mouse ctlr).
KBCK / A20GATE	M4	IO / I	**MultiFunction Pin** (Internal keyboard controller enabled by F0 Rx51[0]) Rx51[0]=1 **Keyboard Clock.** From internal keyboard controller Rx51[0]=0 **Gate A20.** Input from external keyboard controller.
KBDT / KBRC	N1	IO / I	**MultiFunction Pin** (Internal keyboard controller enabled by F0 Rx51[0]) Rx51[0]=1 **Keyboard Data.** From internal keyboard controller. Rx51[0]=0 **Keyboard Reset.** From external keyboard controller (KBC) for CPURST# generation
KBCS# / ROMCS#	T9	O / O	**Keyboard Chip Select** (Rx51[0]=0). To external keyboard controller chip.

For Keyboard Controller configuration and control see also I/O Ports 60h and 64h, Configuration Index ports 3F0h and 3F1h (and configuration registers at offsets E0-E6h) plus Function 0 Rx51[2-0] and PMIO Rx20[2], 30[9], 34[9], and 38[7].

Chip Selects			
Signal Name	**Pin #**	**I/O**	**Signal Description**
ROMCS# / KBCS#	T9	O / O	**ROM Chip Select** (Rx51[0]=1). Chip Select to the BIOS ROM. See also Device 0 Rx40[5-4] and Rx41.
MCCS# / GPO17 / strap	W6	O / IO	**Microcontroller Chip Select** (Device 0 Function 4 RxE4[3] = 0). Asserted during read or write accesses to I/O ports 62h or 66h. Strap: 0/1 = Enable / Disable CPU Frequency Strapping
PCS0# / GPO16	Y6	O / IO / IO	**Programmable Chip Select 0.** (Device 0 Function 4 RxE4[2] = 0). Asserted during I/O cycles to programmable read or write ISA I/O port ranges.
PCS1# / GPI19 / GPO19	G5	O / I / O	**Programmable Chip Select 1.** (Device 0 Function 4 RxE4[5] = 1)

General Purpose Inputs			
Signal Name	**Pin #**	**I/O**	**Signal Description**
GPI0 **[VBAT]**	F4	I	**General Purpose Input 0.**
GPI1 / IRQ8# **[VCCSUS]**	V3	I	**General Purpose Input 1.** F0 Rx51[3] = 1.
GPI2 / EXTSMI# **[VCCSUS]**	W1	I / IO	**General Purpose Input 2.** (Use as GPI **-or-** as EXTSMI#)
GPI3 / RING# **[VCCSUS]**	U3	I / I	**General Purpose Input 3.** (Use as GPI **-or-** as RING#)
GPI4 / LID **[VCCSUS]**	V2	I / I	**General Purpose Input 4.** (Use as GPI **-or-** as LID)
GPI5 / BATLOW# **[VCCSUS]**	T3	I / I	**General Purpose Input 5.** (Use as GPI **-or-** as BATLOW#)
GPI6 / PME# **[VCCSUS]**	U1	I / I	**General Purpose Input 6.** (Use as GPI **-or-** as PME#)
GPI7 / SMBALRT# **[VCCSUS]**	T2	I / I	**General Purpose Input 7.** (Use as GPI **-or-** as SMBALRT#)
GPI8 / INTRUDER# **[VBAT]**	F3	I / I	**General Purpose Input 8.** (Use as GPI **-or-** as INTRUD#)
GPI9 / APICCLK	Y3	I / I	**General Purpose Input 9.** Rx58[6]=0
GPI10 / HREQ1#	Y11	I / I	**General Purpose Input 10.** F4 RxE5[3]=1
GPI11 / HREQ2#	V11	I / I	**General Purpose Input 11.** F4 RxE5[3]=1
GPI12 / LREQ1#	U10	I / I	**General Purpose Input 12.** F4 RxE5[2]=1
GPI13 / LREQ2# / IOCHRDY	W10	I / I	**General Purpose Input 13.** F4 RxE5[2]=1, F0 Rx67[3]=0
GPI14 / WSC#	V4	I / I	**General Purpose Input 14.** Rx58[6]=0
GPI15 / LDRQ#	Y8	I / I	**General Purpose Input 15.** Rx58[5]=0 & F4 RxE5[7]=0
GPI16 / CPUMISS	V1	I / I	**General Purpose Input 16.** (Use as GPI **-or-** as CPUMISS)
GPI17 / AOLGPI / THRM	P3	I / I / I	**General Purpose Input 17.** F4 Rx40[7]=1
GPI18 / GPO18 / FAN2 / SLPBTN#	K3	I / O / I / I	**General Purpose Input 18.** F4 RxE5[0]=0
GPI19 / GPO19 / PCS1#	G5	I / O / O	**General Purpose Input 19.** F4 RxE5[1]=0 & E4[5]=0
GPI20 / GPO20 / LA20 / USBOC2#	W13	I / OD / IO / I	**General Purpose Input 20.** F4 RxE4[6]=0 & PMIO 4E[4]=1
GPI21 / GPO21 / LA21 / USBOC3#	Y13	I / OD / IO / I	**General Purpose Input 21.** F4 RxE4[6]=0 & PMIO 4E[5]=1
GPI22 / GPO22 / IOR#	U7	I / OD / IO	**General Purpose Input 22.** F4 RxE4[7]=0 & PMIO 4E[6]=1
GPI23 / GPO23 / IOW#	T7	I / OD / IO	**General Purpose Input 23.** F4 RxE4[7]=0 & PMIO 4E[7]=1
GPI24 / GPO24 / GPIOA	Y2	I / OD / IO	**General Purpose Input 24.** F4 RxE6[0]=0
GPI25 / GPO25 / GPIOC / CHSINOUT	J5	I / OD / IO / IO	**General Purpose Input 25.** F4 RxE6[1]=0 & E5[6]=0 (F4 RxE5[6]=1 to enable CHSINOUT function on this pin)
GPI26 / GPO26 / SMBDT2 **[VCCSUS]**	R2	I / OD / IO	**General Purpose Input 26.** F4 Rx55[2]=1 & 55[3]=0
GPI27 / GPO27 / SMBCK2 **[VCCSUS]**	R1	I / OD / IO	**General Purpose Input 27.** F4 Rx55[2]=1 & 55[3]=0
GPI28 / JAB1	G3	I / I	**General Purpose Input 28.** (Use as GPI **-or-** as JAB1)
GPI29 / JBB1	F1	I / I	**General Purpose Input 29.** (Use as GPI **-or-** as JBB1)
GPI30 / GPO30 / GPIOD	Y1	I / OD / IO	**General Purpose Input 30.** F4 RxE6[6]=0
GPI31 / GPO31 / GPIOE	W3	I / OD / IO	**General Purpose Input 31.** F4 RxE6[7]=0

Note: See also Power Management I/O Registers Rx50 and 52 for GPI pin status and SCI/SMI select.
Note. The state of each GPI pin may be read at the corresponding bit of PMIO Rx4B-48.
Note: Each of the pins above may be used as a GPI pin or as one of the alternate functions listed above for that pin. Descriptions of these alternate functions are given elsewhere in the pin descriptions section of this document. If a control bit must be set to enable / select each of the above pins for use as a General Purpose Input, the bit setting is listed above. If no bit setting is listed, either function may be used (no bit setting is required to select the GPI function), however note that typical designs may use the pin as one or the other (but not both GPI and alternate function at the same time).

General Purpose Outputs			
Signal Name	**Pin #**	**I/O**	**Signal Description**
GPO0 / SLOWCLK **[VCCSUS]**	R4	O / O	**General Purpose Output 0.** (Func 4 Rx54[1-0] = 00). Output value determined by PMU I/O Rx4C[0]
GPO1 / SUSA# / strap **[VCCSUS]**	P1	O / O / I	**General Purpose Output 1.** F4 Rx54[2]=1
GPO2 / SUSB# **[VCCSUS]**	P2	O / O	**General Purpose Output 2.** F4 Rx54[3]=1
GPO3 / SUSST1# **[VCCSUS]**	N5	O / O	**General Purpose Output 3.** F4 Rx54[4]=1
GPO4 / SUSCLK **[VCCSUS]**	W2	O / O	**General Purpose Output 4.** F4 Rx55[1]=1
GPO5 / CPUSTP#	P4	O / O	**General Purpose Output 5.** F4 RxE4[0]=1
GPO6 / PCISTP#	T4	O / O	**General Purpose Output 6.** F4 RxE4[1]=1
GPO7 / SLP#	U6	O / O	**General Purpose Output 7.** F4 RxE4[4]=1
GPO8 / HGNT1#	W11	O / O	**General Purpose Output 8.** F4 RxE5[3]=1
GPO9 / HGNT2#	T10	O / O	**General Purpose Output 9.** F4 RxE5[3]=1
GPO10 / LGNT1#	Y10	O / O	**General Purpose Output 10.** F4 RxE5[2]=1
GPO11 / LGNT2#	V10	O / O	**General Purpose Output 11.** F4 RxE5[2]=1
GPO12 / JAB2	H5	O / I	**General Purpose Output 12.** F4 RxE5[4]=1 & F0Rx53[7]=0
GPO13 / JBB2	H4	O / I	**General Purpose Output 13.** F4 RxE5[4]=1 & F0Rx53[7]=0
GPO14 / IRTX	R8	O / O	**General Purpose Output 14.** F4 RxE5[5]=1
GPO15 / IRRX	U8	O / I	**General Purpose Output 15.** F4 RxE5[5]=1
GPO16 / PCS0#	Y6	O / O	**General Purpose Output 16.** F4 RxE4[2]=1
GPO17 / MCCS#	W6	O / O	**General Purpose Output 17.** F4 RxE4[3]=1
GPO18 / **GPI18** / FAN2 / SLPBTN#	K3	O / I / I / I	**General Purpose Output 18.** F4 RxE5[0]=1
GPO19 / **GPI19** / PCS1#	G5	O / I / O	**General Purpose Output 19.** F4 RxE4[5]=0 & RxE5[1]=1
GPO20 / **GPI20** / LA20 / USBOC2#	W13	OD / I / IO / I	**General Purpose Output 20.** F4 RxE4[6]=0
GPO21 / **GPI21** / LA21 / USBOC3#	Y13	OD / I / IO / I	**General Purpose Output 21.** F4 RxE4[6]=0
GPO22 / **GPI22** / IOR#	U7	OD / I / IO	**General Purpose Output 22.** F4 RxE4[7]=0
GPO23 / **GPI23** / IOW#	T7	OD / I / IO	**General Purpose Output 23.** F4 RxE4[7]=0
GPO24 / **GPI24** / GPIOA	Y2	OD / I / IO	**General Purpose Output 24.** F4 RxE6[0]=1
GPO25 / **GPI25** / GPIOC /CHSINOUT	J5	OD / I / IO / IO	**General Purpose Output 25.** F4 RxE6[1]=1 & RxE5[5]=0
GPO26 / **GPI26** / SMBDT2**[VCCSUS]**	R2	OD / I / IO	**General Purpose Output 26.** F4 Rx55[3-2]=11
GPO27 / **GPI27** / SMBCK2**[VCCSUS]**	R1	OD / I / IO	**General Purpose Output 27.** F4 Rx55[3-2]=11
GPO28 / APICD0	W4	O / O	**General Purpose Output 28.** Rx58[7-6]=00
GPO29 / APICD1	Y4	O / O	**General Purpose Output 29.** Rx58[7-6]=00
GPO30 / **GPI30** / GPIOD	Y1	OD / I / IO	**General Purpose Output 30.** F4 RxE6[6]=1
GPO31 / **GPI31** / GPIOE	W3	OD / I / IO	**General Purpose Output 31.** F4 RxE6[7]=1

Note: See also Power Management I/O Registers Rx4C-4F to set GPO pin output values. General purpose outputs 20-27 and 30-31 are OD, so to use these pins as input pins, a one must be written to the corresponding bit of PMIO Rx4C-4F.

General Purpose I/Os			
Signal Name	**Pin #**	**I/O**	**Signal Description**
GPIOA / GPI24 / GPO24	Y2	IO / I / O	**General Purpose I/O A / 24.** (F4 RxE6[0] defines as GPI or GPO)
GPIOB / IRRX2	T8	IO / I	**General Purpose I/O B.** (See FIR I/O Rx33 and 34)
GPIOC / GPI25 / GPO25 / CHSINOUT	J5	IO / I / O / IO	**General Purpose I/O C / 25.** (F4 RxE6[1] defines as GPI or GPO)
GPIOD / GPI30 / GPO30	Y1	IO / I / O	**General Purpose I/O D / 30.** (F4 RxE6[6] defines as GPI or GPO)
GPIOE / GPI31 / GPO31	W3	IO	**General Purpose I/O E / 31.** (F4 RxE6[7] defines as GPI or GPO)

Hardware Monitoring			
Signal Name	**Pin #**	**I/O**	**Signal Description**
UIC1	M1	Analog I	**Universal Input Channel.** For temperature / voltage monitoring.
UIC2	M3	Analog I	**Universal Input Channel.** For temperature / voltage monitoring.
UIC3	M2	Analog I	**Universal Input Channel.** For temperature / voltage monitoring.
UIC4	L4	Analog I	**Universal Input Channel.** For temperature / voltage monitoring.
UIC5	L1	Analog I	**Universal Input Channel.** For temperature / voltage monitoring.
DTD+	L2	Analog I	**CPU DTD (Thermal Diode) Channel Plus.**
DTD-	L3	Analog I	**CPU DTD (Thermal Diode) Channel Minus.**
VREF	K1	O	**Voltage Reference for Thermal Sensing** (2.2V ±5%)
FAN1	K2	I	**Fan Speed Monitor 1.** (3.3V only)
FAN2 / SLPBTN# / GPI18 / GPO18	K3	I / I / I / O	**Fan Speed Monitor 2.** (3.3V only) (F4 RxE5[0] = 0)

For HWM configuration and control, see also HWM I/O Space Registers on page 113 plus Function 4 Rx45[2], 70, and 74

Power Management and External State Monitoring			
Signal Name	**Pin #**	**I/O**	**Signal Description**
PME# / GPI6	U1	I / I	**Power Management Event.** (Rx74[1]=0) (1K PU to VCCS if not used)
EXTSMI# / GPI2	W1	IOD / I	**External System Management Interrupt.** When enabled to allow it, a falling edge on this input causes an SMI# to be generated to the CPU to enter SMI mode. (10K PU to VCCS if not used) (3.3V only)
SMBALRT# / GPI7	T2	I / I	**SMB Alert** (System Management Bus I/O space Rx08[3] = 1). When the chip is enabled to allow it, assertion generates an IRQ or SMI or power management event. (10K PU to VCCS if not used)
THRM / AOLGPI / GPI17	P3	I / I / I	**Monitor Input - Thermal Alarm.** (F4 Rx40[7]=0) (1K PU to VCCS if not used)
LID / GPI4	V2	I / I	**Monitor Input - Notebook Computer Display Lid Open / Closed.** Used by the Power Management subsystem to monitor the opening and closing of the display lid of notebook computers. Can be used to detect either low-to-high and/or high-to-low transitions to generate an SMI#. The VT8231 performs a 200 usec debounce of this input if Function 4 Rx40[5] is set to 1. (10K PU to VCCS if not used)
RING# / GPI3	U3	I / I	**Monitor Input – Modem Ring.** May be connected to external modem circuitry to allow the system to be re-activated by a received phone call. (10K PU to VCCS if not used)
BATLOW# / GPI5	T3	I / I	**Monitor Input - Battery Low.** (10K PU to VCCS if not used)
CPUMISS / GPI16	V1	I / I	**Monitor Input - CPU Missing.** Indicates whether the CPU is plugged in correctly.
AOLGPI / GPI17 / THRM	P3	I / I / I	**Monitor Input - Awake On LAN External Event.** F4 Rx40[7]=1
INTRUDER# / GPI8	F3	I / I	**Monitor Input – Chassis Intrusion.**
RSMRST#	F2	I	**Resume Reset.** Resets the internal logic connected to the VCCS power plane and also resets portions of the internal RTC logic.
SUSA# / GPO1 / strap	P1	O / O / I	**Suspend Plane A Control** (Function 4 Rx54[2]=0). Asserted during power management POS, STR, and STD suspend states. Used to control the primary power plane. (10K PU to VCCS if not used)
SUSB# / GPO2	P2	O / O	**Suspend Plane B Control** (Function 4 Rx54[3]=0). Asserted during power management STR and STD suspend states. Used to control the secondary power plane. (10K PU to VCCS if not used)
SUSC# / GPO	N3	O / O	**Suspend Plane C Control.** Asserted during power management STD suspend state. Used to control the tertiary power plane. Also connected to ATX power-on circuitry.
SUSST1# / GPO3	N5	O / O	**Suspend Status 1** (Function 4 Rx54[4] = 0). Typically connected to the North Bridge to provide information on host clock status. Asserted when the system may stop the host clock, such as Stop Clock or during POS, STR, or STD suspend states. Connect 10K PU to VCCS.
SUSCLK / GPO4	W2	O / O	**Suspend Clock** (Function 4 Rx55[1]=0). 32.768 KHz output clock for use by the North Bridge (e.g., Apollo MVP3 or MVP4) for DRAM refresh purposes. Stopped during Suspend-to-Disk and Soft-Off modes. Connect 10K PU to VCCS.

Resets, Clocks, and Clock Control			
Signal Name	**Pin #**	**I/O**	**Signal Description**
PWRGD	E2	I	**Power Good.** Connected to the PWRGOOD signal on the Power Supply.
PWRBTN#	U2	I	**Power Button.** Used by the Power Management subsystem to monitor an external system on/off button or switch. The VT8231 performs a 200us debounce of this input if Function 4 Rx40[5] is set to 1. (3.3V only)
SLPBTN# / FAN2 / GPIO18	K3	I / I / IO	**Sleep Button** (Function 4 Rx40[6] = 0). Used by the power management subsystem to monitor an external system sleep button or switch. Connect to VCC if not used.
PCIRST#	E4	O	**PCI Reset.** Active low reset signal for the PCI bus. The VT8231 will assert this pin during power-up or from the control register.
RTCX1	E3	I	**RTC Crystal Input**: 32.768 KHz crystal or oscillator input. This input is used for the internal RTC and for power-well power management logic.
RTCX2	F5	O	**RTC Crystal Output**: 32.768 KHz crystal output
OSC	T12	I	**Oscillator.** 14.31818 MHz clock signal used by the internal Timer.
SLOWCLK / GPO0	R4	O	**Slow Clock.** Frequency selectable if PMU function 4 Rx54[1-0] is nonzero (set to 01, 10, or 11).
CPUSTP# / GPO5	P4	O / O	**CPU Clock Stop** (Function 4 RxE4[0] = 0). Signals the system clock generator to disable the CPU clock outputs. Not connected if not used. See also PMU I/O Rx2C[3].
PCISTP# / GPO6	T4	O / O	**PCI Clock Stop** (Function 4 RxE4[1] = 0). Signals the system clock generator to disable the PCI clock outputs. Not connected if not used.

Power and Ground			
Signal Name	**Pin #**	**I/O**	**Signal Description**
VCC (27 Pins)	F7, F9, F12-F13, F15, G6, G8-G10, G12, H6, J6, J15, K15, L6, M6, M15, N6, P8-P9, P11-P13, P15, R7, R9-R10, R13-R15	P	**Core Power.** 3.3V nominal (3.15V to 3.45V). This supply is turned on only when the mechanical switch on the power supply is turned on and the PWRON signal is conditioned high. These pins should be connected to the same voltage as the CPU I/O circuitry. Internally connected to hardware monitoring system voltage detection circuitry for 3.3V monitoring.
GND (27 Pins)	G7, G11, G14, H15, J8-J13, K6, K8-K13, L8-L13, L15, M8-M13, N15, P7, P10, P14	P	**Ground.** Connect to primary motherboard ground plane.
VCCSUS	P5, P6	P	**Suspend Power.** Always available unless the mechanical switch of the power supply is turned off. If the "soft-off" state is not implemented, then this pin can be connected to VCC. Signals powered by or referenced to this plane are: SMBCK1/DT1, KBCK/DT, MSCK/DT, PWRBTN#, SUSC#, GPO0 / SLOWCLK, GPO1 / SUSA#, GPO2 / SUSB#, GPO3 / SUSST1#, GPO4 / SUSCLK, GPI1, GPI2 / EXTSMI#, GPI3 / RING#, GPI4 / LID, GPI5 / BATLOW#, GPI6 / PME#, GPI7 / SMBALRT#, GPI16 / CPUMISS, GPI17 / AOLGPI / THRM, GPIO26 / SMBDT2, GPIO27 / SMBCK2
VBAT	E1	P	**RTC Battery.** Battery input for internal RTC. Signals powered by or referenced to this plane are: RTCX1, RTCX2, PWRGD, RSMRST#, GPI0, and INTRUDER#.
VCCHWM	M5	P	**Hardware Monitor / Game Port Power.** Power for hardware monitoring subsystem (voltage monitoring, temperature monitoring, and fan speed monitoring) and game port pins. Connect to VCC through a ferrite bead. Signals powered by or referenced to this plane are: UIC[5:1], DTD+/-, FAN1, FAN2 / SLPBTN# / GPIO18, JAX/Y, JBX/Y, JAB1/2 and JBB1/2.
GNDHWM	L5	P	**Hardware Monitor / Game Port Ground.** Connect to GND through a ferrite bead.
VCCMII	F16, K16	P	**LAN MII Power.** Power for LAN Media Independent Interface (interface to external PHY). Connect to VCC through a ferrite bead. Signals powered by or referenced to this plane are: MCRS, MCOL, MDCK, MDIO, MTXD[3:0], MTXENA, MTXCLK, MRXERR, MRXCLK, MRXDV, and MRXD[3:0]
VCCRAM	G15	P	**LAN RAM Power.** Power for LAN internal RAM. Connect to VCC through a ferrite bead.
GNDRAM	G13	P	**LAN RAM Ground.** Connect to GND through a ferrite bead.
VCCPLL	L16	P	**PLL Power.** Power for internal UDMA PLL. Connect to VCC through a ferrite bead.
GNDPLL	M16	P	**PLL Ground.** Connect to GND through a ferrite bead.
VCCUSB	E15	P	**USB Differential Output Power.** Power for USB differential outputs (USBP0+, P0-, P1+, P1-, P2+, P2-, P3+, P3-). Connect to VCC through a ferrite bead.
GNDUSB	F14	P	**USB Differential Output Ground.** Connect to GND through a ferrite bead.

REGISTERS

Register Overview

The following tables summarize the configuration and I/O registers of the VT8231. These tables also document the power-on default value ("Default") and access type ("Acc") for each register. Access type definitions used are RW (Read/Write), RO (Read/Only), "—" for reserved / used (essentially the same as RO), and RWC (or just WC) (Read / Write 1's to Clear individual bits). Registers indicated as RW may have some read/only bits that always read back a fixed value (usually 0 if unused); registers designated as RWC or WC may have some read-only or read write bits (see individual register descriptions for details).

Detailed register descriptions are provided in the following section of this document. All offset and default values are shown in hexadecimal unless otherwise indicated

Table 2. Memory Mapped Registers

FEC00000	APIC Index	(8-bit)
FEC00010	APIC Data	(32-bit)
FEC00020	APIC IRQ Pin Assertion	(8-bit)
FEC00040	APIC EOI	(8-bit)

"APIC" = "Advanced Programmable Interrupt Controller"

Table 3. Function Summary

Bus	Dev	Func	Device ID	Function
0	0	0	8231h	PCI-to-ISA Bridge
0	0	1	0571h	IDE Controller
0	0	2	3038h	USB Controller Ports 0-1
0	0	3	3038h	USB Controller Ports 2-3
0	0	4	8235h	PM, SMB, & HWM
0	0	5	3058h	AC97 Audio Codec Controller
0	0	6	3058h	MC97 Modem Codec Controller
0	1	0	3065h	VIA LAN Controller

Table 4. System I/O Map

Port	Function	Actual Port Decoding
00-1F	Master DMA Controller	0000 0000 000x nnnn
20-3F	Master Interrupt Controller	0000 0000 001x xxxn
40-5F	Timer / Counter	0000 0000 010x xxnn
60-6F	Keyboard Controller	0000 0000 0110 xnxn
(60h)	KBC Data	0000 0000 0110 x0x0
(61h)	Misc Functions & Spkr Ctrl	0000 0000 0110 xxx1
(64h)	KBC Command / Status	0000 0000 0110 x1x0
70-77	RTC/CMOS/NMI-Disable	0000 0000 0111 0nnn
78-7F	-available for system use-	0000 0000 0111 1xxx
80	-reserved- (debug port)	0000 0000 1000 0000
81-8F	DMA Page Registers	0000 0000 1000 nnnn
90-91	-available for system use-	0000 0000 1001 000x
92	System Control	0000 0000 1001 0010
93-9F	-available for system use-	0000 0000 1001 nnnn
A0-BF	Slave Interrupt Controller	0000 0000 101x xxxn
C0-DF	Slave DMA Controller	0000 0000 110n nnnx
E0-FF	-available for system use-	0000 0000 111x xxxx
100-CF7	-available for system use*	
CF8-CFB	PCI Configuration Address	0000 1100 1111 10xx
CFC-CFF	PCI Configuration Data	0000 1100 1111 11xx
D00-FFFF	-available for system use-	

* On-Chip Super-I/O Functions – PC-Standard Port Addresses

200-20F	Game Port
2E8-2EF	COM4
2F8-2FF	COM2
378-37F	Parallel Port (Standard & EPP)
3E8-3EF	COM3
3F0-3F1	Configuration Index / Data
3F0-3F7	Floppy Controller
3F8-3FF	COM1
778-77A	Parallel Port (ECP Extensions)

Table 5. Registers

Legacy I/O Registers

Port	Master DMA Controller Registers	Default	Acc
00	Channel 0 Base & Current Address		RW
01	Channel 0 Base & Current Count		RW
02	Channel 1 Base & Current Address		RW
03	Channel 1 Base & Current Count		RW
04	Channel 2 Base & Current Address		RW
05	Channel 2 Base & Current Count		RW
06	Channel 3 Base & Current Address		RW
07	Channel 3 Base & Current Count		RW
08	Status / Command		RW
09	Write Request		**WO**
0A	Write Single Mask		**WO**
0B	Write Mode		**WO**
0C	Clear Byte Pointer FF		**WO**
0D	Master Clear		**WO**
0E	Clear Mask		**WO**
0F	Read / Write Mask		RW

Port	Master Interrupt Controller Regs	Default	Acc
20	Master Interrupt Control	—	*
21	Master Interrupt Mask	—	*
20	Master Interrupt Control Shadow	—	**RW**
21	Master Interrupt Mask Shadow	—	**RW**

* RW if shadow registers are disabled

Port	Timer/Counter Registers	Default	Acc
40	Timer / Counter 0 Count		RW
41	Timer / Counter 1 Count		RW
42	Timer / Counter 2 Count		RW
43	Timer / Counter Control		**WO**

Port	Keyboard Controller Registers	Default	Acc
60	Keyboard Controller Data		RW
61	Misc Functions & Speaker Control		RW
64	Keyboard Ctrlr Command / Status		RW

Port	CMOS / RTC / NMI Registers	Default	Acc
70	CMOS Memory Address & NMI Disa		**WO**
71	CMOS Memory Data (128 bytes)		RW
74	CMOS Memory Address		RW
75	CMOS Memory Data (256 bytes)		RW

NMI Disable is port 70h (CMOS Memory Address) bit-7.
RTC control occurs via specific CMOS data locations (0-Dh).
Ports 72-73 may be used to access all 256 locations of CMOS.
Ports 74-75 may be used to access CMOS if the internal RTC is disabled.

Legacy I/O Registers (continued)

Port	DMA Page Registers	Default	Acc
87	DMA Page – DMA Channel 0		RW
83	DMA Page – DMA Channel 1		RW
81	DMA Page – DMA Channel 2		RW
82	DMA Page – DMA Channel 3		RW
8F	DMA Page – DMA Channel 4		RW
8B	DMA Page – DMA Channel 5		RW
89	DMA Page – DMA Channel 6		RW
8A	DMA Page – DMA Channel 7		RW

Port	System Control Registers	Default	Acc
92	System Control		RW

Port	Slave Interrupt Controller Regs	Default	Acc
A0	Slave Interrupt Control	—	*
A1	Slave Interrupt Mask	—	*
A0	Slave Interrupt Control Shadow	—	**RW**
A1	Slave Interrupt Mask Shadow	—	**RW**

* RW accessible if shadow registers are disabled

Port	Slave DMA Controller Registers	Default	Acc
C0	Channel 0 Base & Current Address		RW
C2	Channel 0 Base & Current Count		RW
C4	Channel 1 Base & Current Address		RW
C6	Channel 1 Base & Current Count		RW
C8	Channel 2 Base & Current Address		RW
CA	Channel 2 Base & Current Count		RW
CC	Channel 3 Base & Current Address		RW
CE	Channel 3 Base & Current Count		RW
D0	Status / Command		RW
D2	Write Request		**WO**
D4	Write Single Mask		**WO**
D6	Write Mode		**WO**
D8	Clear Byte Pointer FF		**WO**
DA	Master Clear		**WO**
DC	Clear Mask		**WO**
DE	Read / Write Mask		RW

Super-IO / KBC Configuration Registers (I/O Space)

Port	Super-IO / KBC Config Registers	Default	Acc
3F0	Super-I/O Config Index †	00	RW
3F1	Super-I/O Config Data †	00	RW

† Keyboard / Mouse Controller configuration registers (index values E0-EF) accessible if Function 0 PCI Configuration register Rx51[1] = 1. Super-I/O configuration registers (index values F0-FF) accessible if Function 0 PCI Configuration register Rx50[2] = 1.

Super-IO / KBC Config Registers (Indexed via Port 3F0/1)

Offset	Reserved	Default	Acc
00-DF	-reserved-	--	RO

Offset	Keyboard Ctrlr Cfg (Rx51[1]=1)	Default	Acc
E0	Keyboard / Mouse Wakeup Enable	**80**	**RW**
E1	Keyboard Scan Code Reference Set 0	**F0**	**RW**
E2	Keyboard Scan Code Reference Set 1	00	**RW**
E3	Keyboard Scan Code Reference Set 2	00	**RW**
E4	Keyboard Scan Code Reference Set 3	00	**RW**
E5	Keyboard Scan Code Reference Set 4	00	**RW**
E6	PS/2 Mouse Button Status Scan Code	**09**	**RW**
E7-EF	-reserved-	--	RO

Offset	Super-I/O Config (Rx50[2]=1)	Default	Acc
F0	Super-I/O Device ID	**3C**	RO
F1	Super-I/O Device Revision	**01**	RO
F2	Function Select	**03**	**RW**
F3	Power Down Control	00	**RW**
F4	Serial Port Base Addr (def = 3F8-F)	**FE**	**RW**
F5	-reserved-	--	RO
F6	Parallel Port Base Addr (def = 378-F)	**DE**	**RW**
F7	Floppy Ctrlr Base Addr (def = 3F0-7)	**FC**	**RW**
F8	-reserved-	--	RO
F9	Serial Port Control	00	**RW**
FA	Parallel Port Control	00	**RW**
FB	Floppy Controller Control	00	**RW**
FC	Floppy Controller Drive Type	00	**RW**
FD	-reserved-	--	RO
FE	Test Mode A (Do Not Program)	00	**RW**
FF	Test Mode B (Do Not Program) 2	00	**RW**

Super-I/O I/O Ports

Offset	Floppy Disk Controller (3F0-3F7)	Default	Acc
00-01	-reserved-	00	--
02	FDC Command	--	RW
03	-reserved-	00	--
04	FDC Main Status	--	**RO**
04	FDC Data Rate Select	**02**	**WO**
05	FDC Data	--	RW
06	-reserved-	00	--
07	Diskchange Status	--	**RO**

Offset	Parallel Port (378-37F typical)	Default	Acc
00	Parallel Port Data	--	RW
01	Parallel Port Status	--	**RO**
02	Parallel Port Control	--	RW
03	EPP Address		RW
04	EPP Data Port 0		RW
05	EPP Data Port 1		RW
06	EPP Data Port 2		RW
07	EPP Data Port 3		RW
400h	ECP Data / Configuration A		RW
401h	ECP Configuration B		RW
402h	ECP Extended Control		RW

Offset	Serial Port (COM1=3F8, 3=3E8)	Default	Acc
0	Transmit (Wr) / Receive (Rd) Buffer		RW
1	Interrupt Enable		RW
2	FIFO Control		**WO**
2	Interrupt Status		**RO**
3	UART Control		RW
4	Handshake Control		RW
5	UART Status		RW
6	Handshake Status		RW
7	Scratchpad		RW
9-8	Baud Rate Generator Divisor		RW
A-F	-undefined-		--

Fast IR Registers (I/O Space)

Offset	Fast IR	Default	Acc
0-F	-reserved-	00	--
11-10	Infrared Configuration 0	0000	RW
12	Infrared SIR BOF	**C0**	RW
13	Infrared SIR EOF	**C1**	RW
14	-reserved-	00	--
15	Infrared Status and Control 0	00	RW
17-16	Infrared Status 1	0000	**RO**
19-18	Infrared Configuration 1	0000	RW
1B-1A	Infrared Configuration 2	0000	RW
1D-1C	-reserved-	00	--
1E	Infrared Configuration 3	**04**	RW
1F	-reserved-	00	--
20	Host Control	00	RW
21	Host Status	00	**RO**
22	Miscellaneous Control	00	RW
23	Tx Control 1	00	RW
24	Tx Control 2	00	RW
25	Tx Status	00	**RO**
26	Rx Control	00	RW
27	Rx Status	00	**RO**
28	Reset Command	00	**WO**
29	Packet Address	00	RW
2B-2A	Rx Byte Count	0000	**RO**
2D-2C	Rx Ring Packet Pointer	0000	**RO**
2F-2E	Tx Byte Count	0000	RW
30-7F	-reserved-	00	--

See Function 0 Rx6B-6A[15:7] for the “FIR I/O Base”. The registers in the table above are located at offsets from this base.

PCI Device 0 Function 0 Registers – PCI-to-ISA Bridge

Configuration Space PCI-to-ISA Bridge Header Registers

Offset	PCI Configuration Space Header	Default	Acc
1-0	Vendor ID	**1106**	RO
3-2	Device ID	**8231**	RO
5-4	Command	**0087**	**RW**
7-6	Status	**0200**	**WC**
8	Revision ID	**nn**	RO
9	Programming Interface	00	RO
A	Sub Class Code	**01**	RO
B	Base Class Code	**06**	RO
C	-reserved- (cache line size)	00	—
D	-reserved- (latency timer)	00	—
E	Header Type	**80**	RO
F	Built In Self Test (BIST)	00	RO
10-27	-reserved- (base address registers)	00	—
28-2B	-reserved- (unassigned)	00	—
2F-2C	Subsystem ID Read	00	RO
30-33	-reserved- (expan. ROM base addr)	00	—
34	Capability Pointer	**C0**	RO
35-3B	-reserved- (unassigned)	00	—
3C	-reserved- (interrupt line)	00	—
3D	-reserved- (interrupt pin)	00	—
3E	-reserved- (min gnt)	00	—
3F	-reserved- (max lat)	00	—

Configuration Space PCI-to-ISA Bridge-Specific Registers

Offset	ISA Bus Control	Default	Acc
40	ISA Bus Control	00	RW
41	BIOS ROM Decode Control	00	RW
42	Line Buffer Control	00	RW
43	Delay Transaction Control	00	RW
44	ISA PNP DMA Request Control	00	RW
45	ISA PNP IRQ Routing Control 1	00	RW
46	ISA PNP IRQ Routing Control 2	00	RW
47	ISA PNP IRQ Routing Control 3	00	RW

Offset	PCI Bus ArbitrationControl	Default	Acc
48	Grant Timeout Select 1	00	RW
49	Grant Timeout Select 2	00	RW
4A	PCI Master Arbitration Control	00	RW
4B	-reserved-	00	—

Offset	Miscellaneous Control	Default	Acc
4C	IDE Interrupt Routing	00	RW
4D	External APIC IRQ Output Control	00	RW
4E	Internal RTC Test Mode	00	RW
4F	PCI Bus & CPU Interface Control	00	RW

Offset	Function Control	Default	Acc
50	Function Control 1	00	RW
51	Function Control 2	00	RW

Offset	Serial IRQ & PC/PCI Control	Default	Acc
52	Serial IRQ Control	00	RW
53	Reserved (Do Not Program)	00	RW

Offset	Plug and Play Control	Default	Acc
54	PCI Interrupt Polarity	00	RW
55	PnP Routing for PCI INTA	00	RW
56	PnP Routing for PCI INTB-C	00	RW
57	PnP Routing for PCI INTD	00	RW

Offset	Miscellaneous Control	Default	Acc
58	Miscellaneous Control 0	**40**	RW
59	Miscellaneous Control 1	00	RW
5A-5B	-reserved-	00	—

Offset	Programmable Chip Select Control	Default	Acc
5D-5C	PCS0# I/O Port Address	0000	RW
5F-5E	PCS1# I/O Port Address	0000	RW
61-60	PCS2# I/O Port Address	0000	RW
63-62	PCS3# I/O Port Address	0000	RW
65-64	PCSn# I/O Port Address Mask	0000	RW
66	PCSn# Control	00	RW

Offset	Fast IR Control	Default	Acc
67	Fast IR, FERR, IOCHRDY Config	**08**	RW
68-69	-reserved-	00	—
6B-6A	Fast IR I/O Base	**0001**	RW

Offset	Miscellaneous	Default	Acc
6C	ISA Positive Decoding Control 1	00	RW
6D	ISA Positive Decoding Control 2	00	RW
6E	ISA Positive Decoding Control 3	00	RW
6F	ISA Positive Decoding Control 4	00	RW
73-70	Subsystem ID Write	n/a	WO
74-77	-reserved-	00	—
79-78	PnP IRQ/DRQ Test (do not program)	00	RW
7A	IDE / USB Test (do not program)	00	RW
7B	PLL Test (do not program)	00	RW
7C	I/O Pad Control	00	RW
7D-FF	-reserved-	00	—

PCI Device 0 Function 1 Registers – IDE Controller

Configuration Space IDE Header Registers

Offset	PCI Configuration Space Header	Default	Acc
1-0	Vendor ID	**1106**	RO
3-2	Device ID	**0571**	RO
5-4	Command	**0080**	RO
7-6	Status	**0290**	**RW**
8	Revision ID	**nn**	RO
9	Programming Interface	**85**	**RW**
A	Sub Class Code	**01**	RO
B	Base Class Code	**01**	RO
C	-reserved- (cache line size)	00	—
D	Latency Timer	00	**RW**
E	Header Type	00	RO
F	Built In Self Test (BIST)	00	RO
13-10	Base Address – Pri Data / Command	**000001F0**	RO
17-14	Base Address – Pri Control / Status	**000003F4**	RO
1B-18	Base Address – Sec Data / Command	**00000170**	RO
1F-1C	Base Address – Sec Control / Status	**00000374**	RO
23-20	Base Address – Bus Master Control	**0000CC01**	**RW**
24-2F	-reserved- (unassigned)	00	—
30-33	-reserved- (expan ROM base addr)	00	—
34	Capability Pointer	**C0**	RO
35-3B	-reserved- (unassigned)	00	—
3C	Interrupt Line	**0E**	**RW**
3D	Interrupt Pin	00	RO
3E	Minimum Grant	00	RO
3F	Maximum Latency	00	RO

Configuration Space IDE-Specific Registers

Offset	Configuration Space IDE Registers	Default	Acc
40	IDE Chip Enable	**08**	RW
41	IDE Configuration 1	**06**	RW
42	IDE Configuration 2	**C0**	RW
43	IDE FIFO Configuration	**0A**	RW
44	IDE Miscellaneous Control 1	**68**	RW
45	IDE Miscellaneous Control 2	00	RW
46	IDE Miscellaneous Control 3	**C0**	RW
4B-48	IDE Drive Timing Control	**A8A8A8A8**	RW
4C	IDE Address Setup Time	**FF**	RW
4D	-reserved- (do not program)	00	RW
4E-4F	-reserved-	00	—

Configuration Space IDE-Specific Registers (continued)

Offset	Configuration Space IDE Registers	Default	Acc
53-50	UltraDMA Extended Timing Control	**03030303**	RW
54	UltraDMA FIFO Control	**06**	RW
55-5F	-reserved-	00	—
61-60	IDE Primary Sector Size	**0200**	RW
62-67	-reserved-	00	—
69-68	IDE Secondary Sector Size	**0200**	RW
69-6F	-reserved-	00	—
70	IDE Primary Status	00	RW
71	IDE Primary Interrupt Control	00	RW
72-77	-reserved-	00	—
78	IDE Secondary Status	00	RW
79	IDE Secondary Interrupt Control	00	RW
7A-7F	-reserved-	00	—
83-80	IDE Primary S/G Descriptor Address	0000 0000	RW
84-87	-reserved-	00	—
8B-88	IDE Secondary S/G Descriptor Addr	0000 0000	RW
8C-BF	-reserved-	00	—
C3-C0	PCI PM Block 1	**0002 0001**	**RO**
C7-C4	PCI PM Block 2	0000 0000	RW
C8-FF	-reserved-	00	—

I/O Registers – IDE Controller (SFF 8038 v1.0 Compliant

Offset	IDE I/O Registers	Default	Acc
0	Primary Channel Command	00	RW
1	-reserved-	00	—
2	Primary Channel Status	00	**WC**
3	-reserved-	00	—
4-7	Primary Channel PRD Table Addr	00	RW
8	Secondary Channel Command	00	RW
9	-reserved-	00	—
A	Secondary Channel Status	00	**WC**
B	-reserved-	00	—
C-F	Secondary Channel PRD Table Addr	00	RW

PCI Device 0 Function 2 Registers – USB Ports 0-1

Configuration Space USB Header Registers

Offset	PCI Configuration Space Header	Default	Acc
1-0	Vendor ID	**1106**	RO
3-2	Device ID	**3038**	RO
5-4	Command	0000	**RW**
7-6	Status	**0200**	**WC**
8	Revision ID	**nn**	RO
9	Programming Interface	00	RO
A	Sub Class Code	**03**	RO
B	Base Class Code	**0C**	RO
C	Cache Line Size	00	RO
D	Latency Timer	**16**	**RW**
E	Header Type	00	RO
F	BIST	00	RO
10-1F	-reserved-	00	—
23-20	USB I/O Register Base Address	**00000301**	**RW**
24-3B	-reserved-	00	—
3C	Interrupt Line	00	**RW**
3D	Interrupt Pin	**04**	**RO**
3E-3F	-reserved-	00	—

Configuration Space USB-Specific Registers

Offset	USB Control	Default	Acc
40	USB Miscellaneous Control 1	00	**RW**
41	USB Miscellaneous Control 2	**10**	**RW**
42	USB FIFO Control	00	**RW**
43	-reserved-	00	RO
44-45	-reserved- (test, do not program)		**RW**
46-47	-reserved- (test)		RO
48	CRC Control	00	RW
49-5F	-reserved-	00	—
60	USB Serial Bus Release Number	**10**	RO
61-7F	-reserved-	00	—
83-80	PM Capability	**0002 0001**	RO
84	PM Capability Status	00	**RW**
85-BF	-reserved-	00	—
C1-C0	USB Legacy Support	**2000**	**RW**
C2-FF	-reserved-	00	—

I/O Registers – USB Controller

Offset	USB I/O Registers	Default	Acc
1-0	USB Command	0000	RW
3-2	USB Status	0000	**WC**
5-4	USB Interrupt Enable	0000	RW
7-6	Frame Number	0000	RW
B-8	Frame List Base Address	00000000	RW
C	Start Of Frame Modify	**40**	RW
11-10	Port 0 Status / Control	**0080**	**WC**
13-12	Port 1 Status / Control	**0080**	**WC**
14-1F	-reserved-	00	—

PCI Device 0 Function 3 Registers – USB Ports 2-3

Configuration Space USB Header Registers

Offset	PCI Configuration Space Header	Default	Acc
1-0	Vendor ID	**1106**	RO
3-2	Device ID	**3038**	RO
5-4	Command	0000	**RW**
7-6	Status	**0200**	**WC**
8	Revision ID	**nn**	RO
9	Programming Interface	00	RO
A	Sub Class Code	**03**	RO
B	Base Class Code	**0C**	RO
C	Cache Line Size	00	RO
D	Latency Timer	**16**	**RW**
E	Header Type	00	RO
F	BIST	00	RO
10-1F	-reserved-	00	—
23-20	USB I/O Register Base Address	**00000301**	**RW**
24-3B	-reserved-	00	—
3C	Interrupt Line	00	**RW**
3D	Interrupt Pin	**04**	**RO**
3E-3F	-reserved-	00	—

Configuration Space USB-Specific Registers

Offset	USB Control	Default	Acc
40	USB Miscellaneous Control 1	00	**RW**
41	USB Miscellaneous Control 2	**10**	**RW**
42	USB FIFO Control	00	**RW**
43	-reserved-	00	RO
44-45	-reserved- (test only, do not program)		**RW**
46-47	-reserved- (test)		RO
48	CRC Control	00	RW
49-5F	-reserved-	00	—
60	USB Serial Bus Release Number	**10**	RO
61-7F	-reserved-	00	—
83-80	PM Capability	**0002 0001**	RO
84	PM Capability Status	00	**RW**
85-BF	-reserved-	00	—
C1-C0	USB Legacy Support	**2000**	**RW**
C2-FF	-reserved-	00	—

I/O Registers - USB Controller

Offset	USB I/O Registers	Default	Acc
1-0	USB Command	0000	RW
3-2	USB Status	0000	**WC**
5-4	USB Interrupt Enable	0000	RW
7-6	Frame Number	0000	RW
B-8	Frame List Base Address	00000000	RW
C	Start Of Frame Modify	**40**	RW
11-10	Port 2 Status / Control	**0080**	**WC**
13-12	Port 3 Status / Control	**0080**	**WC**
14-1F	-reserved-	00	—

PCI Device 0 Function 4 Registers - Power Management

Configuration Space Power Mgmt Header Registers

Offset	PCI Configuration Space Header	Default	Acc
1-0	Vendor ID	**1106**	RO
3-2	Device ID	**8235**	RO
5-4	Command	0000	RO
7-6	Status	**0280**	**WC**
8	Revision ID	**nn**	RO
9	Programming Interface	00†	RO
A	Sub Class Code	00†	RO
B	Base Class Code	00†	RO
C	Cache Line Size	00	RO
D	Latency Timer	00	RO
E	Header Type	00	RO
F	BIST	00	RO
10-3F	-reserved-	00	—

† The default values for these registers may be changed by writing to offsets 61-63h (see below).

Configuration Space Power Management Registers

Offset	Power Management	Default	Acc
40	General Configuration 0	00	RW
41	General Configuration 1	00	RW
42	ACPI Interrupt Select	00	RW
43	Internal Timer Read Test	—	**RO**
45-44	Primary Interrupt Channel	0000	RW
47-46	Secondary Interrupt Channel	0000	RW
4B-48	Power Mgmt I/O Base (256 Bytes)	**0000 0001**	RW
4C	Host Bus Power Management Control	00	RW
4D	Throttle / Clock Stop Control	00	RW
4E-4F	-reserved-	00	—
53-50	GP Timer Control	0000 0000	RW
54	Power Well Control	00	RW
55	Miscellaneous Control	00	RW
56	Power On / Reset Control	00	RW
57	-reserved-	00	—
58	GP2 / GP3 Timer Control	00	RW
59	GP2 Timer	00	RW
5A	GP3 Timer	00	RW
5B-60	-reserved-	00	—
61	Write value for Offset 9 (Prog Intfc)	00	**WO**
62	Write value for Offset A (Sub Class)	00	**WO**
63	Write value for Offset B (Base Class)	00	**WO**
64-7F	-reserved-	00	—

Configuration Space Hardware Monitor Registers

Offset	System Management Bus	Default	Acc
71-70	Hardware Mon IO Base (128 Bytes)	**0001**	RW
72-73	-reserved-	00	—
74	Hardware Monitor Control	00	RW
75-8F	-reserved-	00	—

Configuration Space SMBus Registers

Offset	System Management Bus	Default	Acc
93-90	SMBus I/O Base (16 Bytes)	**0000 0001**	RW
94-D1	-reserved-	00	—
D2	SMBus Host Configuration	00	RW
D3	SMBus Host Slave Command	00	RW
D4	SMBus Slave Address Shadow Port 1	00	RW
D5	SMBus Slave Address Shadow Port 2	00	RW
D6	SMBus Revision ID	**nn**	**RO**
D7-DF	-reserved-	00	—

Configuration Space General Purpose I/O Registers

Offset	General Purpose I/O	Default	Acc
E0	GPI Inversion Control	00	RW
E1	GPI SCI / SMI Select	00	RW
E2-E3	-reserved-	00	—
E4	GPO Pin Select	00	RW
E5	GPIO I/O Select 1	00	RW
E6	GPIO I/O Select 2	00	RW
E7	GPO Output Type	00	RW
E8-FF	-reserved-	00	—

I/O Space Power Management- Registers

Offset	Basic Control / Status Registers	Default	Acc
1-0	Power Management Status	0000	**WC**
3-2	Power Management Enable	0000	RW
5-4	Power Management Control	0000	RW
6-7	-reserved-	00	—
B-8	Power Management Timer	0000 0000	RW
C-F	-reserved-	00	—

Offset	Processor Registers	Default	Acc
13-10	Processor and PCI Bus Control	0000 0000	RW
14	Processor LVL2	00	**RO**
15	Processor LVL3	00	**RO**
16-1F	-reserved-	00	—

Offset	General Purpose Registers	Default	Acc
21-20	General Purpose Status	0000	**WC**
23-22	General Purpose SCI Enable	0000	RW
25-24	General Purpose SMI Enable	0000	RW
26-27	-reserved-	00	—

Offset	Generic Registers	Default	Acc
29-28	Global Status	0000	**WC**
2B-2A	Global Enable	0000	RW
2D-2C	Global Control	**0010**	RW
2E	-reserved-	00	—
2F	SMI Command	00	RW
33-30	Primary Activity Detect Status	0000 0000	**WC**
37-34	Primary Activity Detect Enable	0000 0000	RW
3B-38	GP Timer Reload Enable	0000 0000	RW
3C-3F	-reserved-	00	—

Offset	General Purpose I/O Registers	Default	Acc
40	Extended I/O Trap Status	00	**WC**
41	-reserved-	00	—
42	Extended I/O Trap Enable	00	RW
43-44	-reserved-	00	—
45	Miscellaneous Status	00	RW
46-47	-reserved-	00	—
4B-48	GPI Port Input Value	**input**	**RO**
4F-4C	GPO Port Output Value	**FFFFFFFF**	RW
50	GPI Pin Change Status	00	RW
51	-reserved-	00	—
52	GPI Pin Change SCI/SMI Select	00	RW
53-57	-reserved-	00	—
59-58	I/O Trap PCI I/O Address	0000	**RO**
5A	I/O Trap PCI Command / Byte Ena	00	**RO**
5B-FF	-reserved-	00	—

I/O Space System Management Bus Registers

Offset	System Management Bus	Default	Acc
0	SMBus Host Status	00	**WC**
1	SMBus Slave Status	00	RW
2	SMBus Host Control	00	RW
3	SMBus Host Command	00	RW
4	SMBus Host Address	00	RW
5	SMBus Host Data 0	00	RW
6	SMBus Host Data 1	00	RW
7	SMBus Block Data	00	RW
8	SMBus Slave Control	00	RW
9	SMBus Shadow Command	00	**RO**
A-B	SMBus Slave Event	0000	RW
C-D	SMBus Slave Data	0000	**RO**
E	-reserved-	00	—
F	SMBus Slave Address	00	RW

I/O Space Hardware Monitor Registers

Offset	Hardware Monitor	Default	Acc
00-3F	Value RAM		
00-0F	-reserved-	00	—
10	Digital Filter Parameter 7-0	00	RW
11	Digital Filter Parameter 15-8	00	RW
12	Digital Filter Parameter 19-16	00	RW
13	Analog Data 15-8	00	RW
14	Analog Data 7-0	00	RW
15	Digital Data 7-0	00	RW
16	Channel Counter	00	RW
17	Data Valid & Channel Indications	00	RW
18-1E	-reserved-	00	—
1F	Temp Reading 1 - CPU Thermal D.	00	RW
20	-reserved-	00	—
21	Temp Reading 2 - UIC1	00	RW
22	Voltage Input Default – UIC2	00	RW
23	Voltage Input Default – UIC3	00	RW
24	Voltage Input Default – UIC4	00	RW
25	Voltage Input Default – UIC5	00	RW
26	Voltage Reading – 3.3V internal vcc	00	RW
27	Voltage Reading – 2.5V or –12V	00	RW
28	-reserved- (-5V Voltage Reading)	00	—
29	FAN1 (K2) Count Reading	00	RW
2A	FAN2 (K3) Count Reading	00	RW
2B	Hi Limit – UIC2	00	RW
2C	Lo Limit – UIC2	00	RW
2D	Hi Limit – UIC3	00	RW
2E	Lo Limit – UIC3	00	RW
2F	Hi Limit – UIC4	00	RW
30	Lo Limit – UIC4	00	RW
31	Hi Limit – UIC5	00	RW
32	Lo Limit – UIC5	00	RW
33	Hi Limit - Internal 3.3V	00	RW
34	Lo Limit - Internal 3.3V	00	RW
35	Hi Limit – 2.5V / -12V (reserved)	00	RW
36	Lo Limit – 2.5V / -12V (reserved)	00	RW
37	-reserved- (-5V Sense High Limit)	00	—
38	-reserved- (-5V Sense Low Limit)	00	—
39	Hi Limit – Temp Reading 1	00	RW
3A	Lo Limit – Hot Temp 1 Hysteresis	00	RW
3B	FAN1 Fan Count Limit	00	RW
3C	FAN2 Fan Count Limit	00	RW
3D	Hi Limit – UIC1 (temp 2 default)	00	RW
3E	Lo Limit – UIC1	00	RW
3F	Stepping ID Number	00	RW

Offset	Hardware Monitor (continued)	Default	Acc
40	Hardware Monitor Configuration	**08**	RW
41	Hardware Monitor Interrupt Status 1	00	**RO**
42	Hardware Monitor Interrupt Status 2	00	**RO**
43	Hardware Monitor Interrupt Mask 1	00	RW
44	Hardware Monitor Interrupt Mask 2	00	RW
45	AFE Control	00	RW
46	AFE Test Control	00	RW
47	Fan Configuration	**50**	RW
48	SMBus Address	**2D**	RW
49	Temperature Control	00	RW
4A	Universal Channel Configuration	**07**	RW
4B	Temperature Configuration 1	**15**	RW
4C	Temperature Configuration 2	**55**	RW
4D	Extended Temperature Resolution	00	**RO**
4E	Over Temperature Control	**0F**	RW
4F-FF	-reserved-	00	—

PCI Device 0 Function 5 & 6 Registers – AC/MC97 Codecs

Function 5 Configuration Space AC97 Header Registers

Offset	PCI Configuration Space Header	Default	Acc
1-0	Vendor ID	**1106**	RO
3-2	Device ID	**3058**	RO
5-4	Command	0000	**RW**
7-6	Status	**0210**	**WC**
8	Revision ID	**40**	RO
9	Programming Interface	00	RO
A	Sub Class Code	**01**	RO
B	Base Class Code	**04**	RO
C	Cache Line Size	00	RO
D	Latency Timer	00	**RW**
E	Header Type	00	RO
F	BIST	00	RO
13-10	Base Address 0 - SGD Control/Status	**0000 0001**	**RW**
17-14	Base Address 1 - FM NMI Status	**0000 0001**	**RW**
1B-18	Base Address 2 - MIDI Port	**0000 0331**	**RW**
1F-1C	Base Address 3 - (reserved)	0000 0000	—
23-20	Base Address 4 - (reserved)	0000 0000	—
27-24	Base Address 5 - (reserved)	0000 0000	—
28-29	-reserved-	00	—
2F-2C	Subsystem ID / SubVendor ID	0000 0000	**RW**
33-30	Expansion ROM (reserved)	0000 0000	—
34	Capture Pointer	00	**RW**
35-3B	-reserved-	00	—
3C	Interrupt Line	00	**RW**
3D	Interrupt Pin	**03**	RO
3E	Minimum Grant	00	RO
3F	Maximum Latency	00	RO

Configuration Space Audio Codec-Specific Registers

Offset	Audio Codec Link Control	Default	Acc
40	AC-Link Interface Status	00	**RO**
41	AC-Link Interface Control	00	RW
42	Function Enable	00	RW
43	Plug and Play Control	**1C**	RW
44	MC97 Interface Control	00	**RO**
45-47	-reserved-	00	—
48	FM NMI Control	**01**	RW
49	-reserved-	00	—
4B-4A	Game Port Base Address	**0200**	RW
4C-FF	-reserved-	00	—

Function 6 Configuration Space MC97 Header Registers

Offset	PCI Configuration Space Header	Default	Acc
1-0	Vendor ID	**1106**	RO
3-2	Device ID	**3068**	RO
5-4	Command	0000	**RW**
7-6	Status	**0200**	**WC**
8	Revision ID	**40**	RO
9	Programming Interface	00	RO
A	Sub Class Code	**80**	RO
B	Base Class Code	**07**	RO
C	Cache Line Size	00	RO
D	Latency Timer	00	**RW**
E	Header Type	00	RO
F	BIST	00	RO
13-10	Base Address 0 - SGD Control/Status	**0000 0001**	**RW**
17-14	Base Address 1 - (reserved)	0000 0000	—
1B-18	Base Address 2 - (reserved)	0000 0000	—
1F-1C	Base Address 3 - (reserved)	0000 0000	—
23-20	Base Address 4 - (reserved)	0000 0000	—
27-24	Base Address 5 - (reserved)	0000 0000	—
28-29	-reserved-	00	—
2F-2C	Subsystem ID / SubVendor ID	0000 0000	**RW**
33-30	Expansion ROM (reserved)	0000 0000	—
34	Capture Pointer	00	**RW**
35-3B	-reserved-	00	—
3C	Interrupt Line	00	**RW**
3D	Interrupt Pin	**03**	RO
3E	Minimum Grant	00	RO
3F	Maximum Latency	00	RO

Configuration Space Modem Codec-Specific Registers

Offset	Modem Codec Link Control	Default	Acc
40	AC-Link Interface Status	00	**RO**
41	AC-Link Interface Control	00	RW
42	Function Enable	00	**RO**
43	Plug and Play Control	**1C**	**RO**
44	MC97 Interface Control	00	RW
45-47	-reserved-	00	—
48	FM NMI Control	**01**	**RO**
49	-reserved-	00	—
4B-4A	Game Port Base Address	**0200**	**RO**
4C-FF	-reserved-	00	—

Function 5 I/O Base 0 Registers – AC97 Audio S/G DMA

Offset	AC97 SGD I/O Registers	Default	Acc
0	SGD Read Channel Status	00	**WC**
1	SGD Read Channel Control	00	RW
2	SGD Read Channel Type	00	RW
3	-reserved-	00	—
7-4	SGD Read Chan Table Pointer Base SGD Read Channel Current Address	0000 0000	WR RD
B-8	Reserved (Test)	0000 0000	**RO**
F-C	SGD Read Chan Current Count	0000 0000	**RO**
10	SGD Write Channel Status	00	**WC**
11	SGD Write Channel Control	00	RW
12	SGD Write Channel Type	00	RW
13	-reserved-	00	—
17-14	SGD Write Chan Table Pointer Base SGD Write Channel Current Address	0000 0000	WR RD
1B-18	Reserved (Test)	0000 0000	**RO**
1F-1C	SGD Write Channel Current Count	0000 0000	**RO**
20	SGD FM Channel Status	00	**WC**
21	SGD FM Channel Control	00	RW
22	SGD FM Type	00	RW
23	-reserved-	00	—
27-24	SGD FM Channel Table Pointer Base SGD FM Channel Current Address	0000 0000	WR RD
2B-28	Reserved (Test)	0000 0000	**RO**
2F-2C	SGD FM Channel Current Count	0000 0000	**RO**
30-7F	-reserved-	00	—
Offset	**AC97 / Audio Codec I/O Registers**	**Default**	**Acc**
83-80	AC97 Controller Command / Status	0000 0000	RW
87-84	SGD Status Shadow	0000 0000	**RO**
88-FF	-reserved-	00	—

Function 5 I/O Base 1 Registers – FM NMI Status

Offset	FM NMI Status Registers	Default	Acc
0	FM NMI Status	00	**RO**
1	FM NMI Data	00	**RO**
2	FM NMI Index	00	**RO**
3	-reserved-	00	—

Function 5 I/O Base 2 Registers – MIDI / Game Port

Offset	FM NMI Status Registers	Default	Acc
1-0	MIDI Port Base	0330	RW
3-2	Game Port Base	0200	RW

Function 5/6 I/O Base 3 Registers – Codec Reg Shadow

Offset	Codec Register Shadow	Default	Acc
00-7F	Primary Codec Register 0-7F Shadow		RW
80-FF	Secondary Codec Reg 0-7F Shadow		RW

Function 6 I/O Base 0 Registers – MC97 Modem S/G DMA

Offset	MC97 SGD I/O Registers	Default	Acc
40	SGD Read Channel Status	00	**WC**
41	SGD Read Channel Control	00	RW
42	SGD Read Channel Type	00	RW
43	-reserved-	00	—
47-44	SGD Read Chan Table Pointer Base SGD Read Channel Current Address	0000 0000	WR RD
4B-48	-reserved- (Test)	0000 0000	**RO**
4F-4C	SGD Read Chan Current Count	0000 0000	**RO**
50	SGD Write Channel Status	00	**WC**
51	SGD Write Channel Control	00	RW
52	SGD Write Channel Type	00	RW
53	-reserved-	00	—
57-54	SGD Write Chan Table Pointer Base SGD Write Channel Current Address	0000 0000	WR RD
5B-58	Reserved (Test)	0000 0000	**RO**
5F-5C	SGD Write Channel Current Count	0000 0000	**RO**
60-7F	-reserved-	00	—
Offset	**AC97 / Modem Codec I/O Registers**	**Default**	**Acc**
83-80	AC97 Controller Command / Status	0000 0000	RW
87-84	SGD Status Shadow	0000 0000	**RO**
8B-88	Modem Codec GPI Intr Status / GPIO	0000 0000	**WC**
8F-8C	Modem Codec GPI Interrupt Enable	0000 0000	RW
90-FF	-reserved-	00	—

I/O Registers – SoundBlaster Pro

Offset	SB Pro Registers (220 or 240h typ)	Default	Acc
0	FM Left Channel Index / Status		RW
1	FM Left Channel Data		**WO**
2	FM Right Channel Index / Status		RW
3	FM Right Channel Data		**WO**
4	Mixer Index		**WO**
5	Mixer Data		RW
6	Sound Processor Reset		**WO**
7	-reserved-	00	--
8	FM Index / Status (Both Channels)		RW
9	FM Data (Both Channels)		**WO**
A	Sound Processor Data		**RO**
B	-reserved-	00	--
C	Sound Processor Command / Data Sound Processor Buffer Status		WR RD
D	-reserved-	00	--
E	Snd Processor Data Available Status		**RO**
F	-reserved-	00	--

Port	SB Pro Regs (same as offsets 8 & 9)	Default	Acc
388h	FM Index / Status		RW
389h	FM Data		**WO**

The above group of registers emulates the "FM", "Mixer", and "Sound Processor" functions of the SoundBlaster Pro.

I/O Registers – Game Port

Offset	Game Port (200-20F typical)	Default	Acc
0	-reserved-	00	--
1	Game Port Status		**RO**
1	Start One-Shot		**WO**
2-F	-reserved-	00	--

Memory Mapped Registers – IOAPIC

Address	APIC Index / Data	Default	Acc
FEC00000	APIC Register Index	00	RW
FEC00001-0F	-reserved-	00	--
FEC00013-10	APIC Register 32-bit Data	0000 0000	RW
FEC00014-1F	-reserved-	00	--
FEC00020	APIC IRQ Pin Assertion	xx	**WO**
FEC00021-3F	-reserved-	00	--
FEC00040	APIC EOI	xx	**WO**
FEC00041-FF	-reserved-	00	--

Offset	APIC 32-bit Registers	Default	Acc
0	APIC ID	0000 0000	RW
1	APIC Version	0017 0011	**RO**
2	APIC Arbitration	0000 0000	**RO**
3-F	-reserved-	0000 0000	--
11-10	I/O Redirection– AIRQ0	xxx1xxxx xxxxxxxx	RW
13-12	I/O Redirection– AIRQ1	xxx1xxxx xxxxxxxx	RW
15-14	I/O Redirection– AIRQ2	xxx1xxxx xxxxxxxx	RW
17-16	I/O Redirection– AIRQ3	xxx1xxxx xxxxxxxx	RW
19-18	I/O Redirection– AIRQ4	xxx1xxxx xxxxxxxx	RW
1B-1A	I/O Redirection– AIRQ5	xxx1xxxx xxxxxxxx	RW
1D-1C	I/O Redirection– AIRQ6	xxx1xxxx xxxxxxxx	RW
1F-1E	I/O Redirection– AIRQ7	xxx1xxxx xxxxxxxx	RW
21-20	I/O Redirection– AIRQ8	xxx1xxxx xxxxxxxx	RW
23-20	I/O Redirection– AIRQ9	xxx1xxxx xxxxxxxx	RW
25-24	I/O Redirection– AIRQ10	xxx1xxxx xxxxxxxx	RW
27-26	I/O Redirection– AIRQ11	xxx1xxxx xxxxxxxx	RW
29-28	I/O Redirection– AIRQ12	xxx1xxxx xxxxxxxx	RW
2B-2A	I/O Redirection– AIRQ13	xxx1xxxx xxxxxxxx	RW
2D-2C	I/O Redirection– AIRQ14	xxx1xxxx xxxxxxxx	RW
2F-2E	I/O Redirection– AIRQ15	xxx1xxxx xxxxxxxx	RW
31-30	I/O Redirection– AIRQ16	xxx1xxxx xxxxxxxx	RW
33-32	I/O Redirection– AIRQ17	xxx1xxxx xxxxxxxx	RW
35-34	I/O Redirection– AIRQ18	xxx1xxxx xxxxxxxx	RW
37-36	I/O Redirection– AIRQ19	xxx1xxxx xxxxxxxx	RW
39-38	I/O Redirection– AIRQ20	xxx1xxxx xxxxxxxx	RW
3B-3A	I/O Redirection– AIRQ21	xxx1xxxx xxxxxxxx	RW
3D-3C	I/O Redirection– AIRQ22	xxx1xxxx xxxxxxxx	RW
3F-3E	I/O Redirection– AIRQ23	xxx1xxxx xxxxxxxx	RW
40-4F	-reserved-	0000 0000	--

Note: The "I/O Redirection" registers are 64-bit registers, so each uses two consecutive index locations, with the lower 32 bits at the even index and the upper 32 bits at the odd index.

PCI Device 1 Function 0 Registers - LAN

Configuration Space LAN Header Registers

Offset	PCI Configuration Space Header	Default	Acc
1-0	Vendor ID	**1106**	RO
3-2	Device ID	**3065**	RO
5-4	Command	0000	RO
7-6	Status	**0400**	**WC**
8	Revision ID	**40**	RO
9	Programming Interface	00	RO
A	Sub Class Code	00	RO
B	Base Class Code	00	RO
C	Cache Line Size	00	**RW**
D	Latency Timer	00	**RW**
E	Header Type	00	RO
F	BIST	00	RO
13-10	I/O Base Address	0000 0000	RW
17-14	Memory Base Address	0000 0000	RW
18-27	-reserved-	00	—
2B-28	Card Bus CIS Pointer	0000 0000	RW
2C-2F	-reserved-	00	—
33-30	Expansion ROM Base Address		RW
34	Capabilities Offset		**RO**
35-3F	-reserved-	00	—

Configuration Space LAN Registers

Offset	Power Management	Default	Acc
40	Capability ID	**01**	**RO**
41	Next Item Pointer	00	**RO**
43-42	Power Management Configuration	**0002**	**RO**
47-44	Power Management Control / Status	0000 0000	**WC**
48-FF	-reserved-	00	—

I/O Space LAN Registers

Offset	Power Management	Default	Acc
5-0	Ethernet Address		RW
6	Receive Control	00	RW
7	Transmit Control	**08**	RW
8	Command 0	00	RW
9	Command 1	00	RW
A-B	-reserved-	00	—
C	Interrupt Status 0	00	RW
D	Interrupt Status 1	00	RW
E	Interrupt Mask 0	00	RW
F	Interrupt Mask 1	00	RW
17-10	Multicast Address		RW
1B-18	Receive Address		RW
1F-1C	Transmit Address		RW
23-20	Receive Status	0000 0000	RW
27-24	Receive Data Buffer Control	0000 0000	**RO**
2B-28	Receive Data Buffer Start Address		**RO**
2F-2C	Receive Data Buffer Branch Address		**RO**
30-3F	-reserved-	00	—

I/O Space LAN Registers (continued)

Offset	Power Management	Default	Acc
43-40	Transmit Status	0000 0000	RW
47-44	Transmit Data Buffer Control	0000 0000	**RO**
4B-48	Transmit Data Buffer Start Address		**RO**
4F-4C	Transmit Data Buffer Branch Addr		**RO**
50-6B	-reserved-	00	—
6C	PHY Address	**01**	RW
6D	MII Status	**13**	RW
6E	Buffer Control 0	00	RW
6F	Buffer Control 1	00	RW
70	MII Management Port Command	00	RW
71	MII Management Port Address	**81**	RW
72-73	-reserved-	00	—
74	EEPROM Command / Status	00	RW
75-78	-reserved-	00	—
79	Configuration 1	00	RW
7A	Configuration 2	00	RW
7B	Configuration 3	00	RW
7C-7F	-reserved-	00	—
80	Miscellaneous 1	00	RW
81	Miscellaneous 2	00	RW
82	-reserved-	00	—
83	Sticky Hardware Control	00	RW
84	MII Interrupt Status	00	**WC**
85	-reserved-	00	—
86	MII Interrupt Mask	00	RW
87-92	-reserved-	00	—
93	EEPROM Checksum	00	RW
95-94	Suspend Mode MII Address	0000	RW
96	Suspend Mode PHY Address	00	RW
97	-reserved-	00	—
99-98	Pause Timer	0000	RW
9A	Pause Status	00	RW
9B	-reserved-	00	—
9D-9C	Soft Timer 0	0000	RW
9F-9E	Soft Timer 1	0000	RW
A0/A4	Wake On LAN Control Set / Clear	00 / 00	RW
A1/A5	Power Configuration Set / Clear	00 / 00	RW
A2/A6	Test Set / Clear	00 / 00	RW
A3/A7	Wake On LAN Config Set / Clear	00 / 00	RW
A8-AF	-reserved-	00	—
B3-B0	Pattern CRC 0	0000 0000	RW
B7-B4	Pattern CRC 1	0000 0000	RW
BB-B8	Pattern CRC 2	0000 0000	RW
BF-BC	Pattern CRC 3	0000 0000	RW
CF-C0	Byte Mask 0	0000 0000	RW
DF-D0	Byte Mask 1	0000 0000	RW
EF-E0	Byte Mask 2	0000 0000	RW
FF-F0	Byte Mask 3	0000 0000	RW

Register Descriptions

Legacy I/O Ports

This group of registers includes the DMA Controllers, Interrupt Controllers, and Timer/Counters as well as a number of miscellaneous ports originally implemented using discrete logic on original PC/AT motherboards. All of the registers listed are integrated on-chip. These registers are implemented in a precise manner for backwards compatibility with previous generations of PC hardware. These registers are listed for information purposes only. Detailed descriptions of the actions and programming of these registers are included in numerous industry publications (duplication of that information here is beyond the scope of this document). All of these registers reside in I/O space.

Port 61 - Misc Functions & Speaker Control ..... RW

7-6 Reserved .....always reads 0

5 Timer/Counter 2 Output .....RO
This bit reflects the output of Timer/Counter 2 without any synchronization.

4 Refresh Detected .....RO
This bit toggles on every rising edge of the ISA bus REFRESH# signal.

3-2 Reserved .....RW, default=0

1 Speaker Enable.....RW
- 0 Disable..... default
- 1 Enable Timer/Ctr 2 output to drive SPKR pin

0 Timer/Counter 2 Enable.....RW
- 0 Disable..... default
- 1 Enable Timer/Counter 2

Port 92h - System Control ..... RW

7-6 Hard Disk Activity LED Status
- 0 Off ..... default
- 1-3 On

5-4 Reserved .....always reads 0

3 Power-On Password Bytes Inaccessable .. default=0

2 Reserved .....always reads 0

1 A20 Address Line Enable
- 0 A20 disabled / forced 0 (real mode)..... default
- 1 A20 address line enabled

0 High Speed Reset
- 0 Normal
- 1 Briefly pulse system reset to switch from protected mode to real mode

Keyboard Controller I/O Registers

The keyboard controller handles the keyboard and mouse interfaces. Two ports are used: port 60 and port 64. Reads from port 64 return a status byte. Writes to port 64h are command codes (see command code list following the register descriptions). Input and output data is transferred via port 60.

A "Control" register is also available. It is accessable by writing commands 20h / 60h to the command port (port 64h); The control byte is written by first sending 60h to the command port, then sending the control byte value. The control register may be read by sending a command of 20h to port 64h, waiting for "Output Buffer Full" status = 1, then reading the control byte value from port 60h.

Traditional (non-integrated) keyboard controllers have an "Input Port" and an "Output Port" with specific pins dedicated to certain functions and other pins available for general purpose I/O. Specific commands are provided to set these pins high and low. All outputs are "open-collector" so to allow input on one of these pins, the output value for that pin would be set high (non-driving) and the desired input value read on the input port. These ports are defined as follows:

Bit	Input Port	Lo Code	Hi Code
0	P10 - Keyboard Data In	B0	B8
1	P11 - Mouse Data In	B1	B9
2	P12 - Turbo Pin (PS/2 mode only)	B2	BA
3	P13 - user-defined	B3	BB
4	P14 - user-defined	B6	BE
5	P15 - user-defined	B7	BF
6	P16 - user-defined	–	–
7	P17 - undefined	–	–

Bit	Output Port	Lo Code	Hi Code
0	P20 - SYSRST (1=execute reset)	–	–
1	P21 - GATEA20 (1=A20 enabled)	–	–
2	P22 - Mouse Data Out	B4	BC
3	P23 - Mouse Clock Out	B5	BD
4	P24 - Keyboard OBF Interrupt (IRQ1)	–	–
5	P25 - Mouse OBF Interrupt (IRQ 12)	–	–
6	P26 - Keyboard Clock Out	–	–
7	P27 - Keyboard Data Out	–	–

Bit	Test Port	Lo Code	Hi Code
0	T0 - Keyboard Clock In	–	–
1	T1 - Mouse Clock In	–	–

Note: Command code C0h transfers input port data to the output buffer. Command code D0h copies output port values to the output buffer. Command code E0h transfers test input port data to the output buffer.

Port 60 - Keyboard Controller Input Buffer.....WO

Only write to port 60h if port 64h bit-1 = 0 (1=full).

Port 60 - Keyboard Controller Output Buffer.....RO

Only read from port 60h if port 64h bit-0 = 1 (0=empty).

Port 64 - Keyboard / Mouse Status..... RO

7 Parity Error
- 0 No parity error (odd parity received) .... default
- 1 Even parity occurred on last byte received from keyboard / mouse

6 General Receive / Transmit Timeout
- 0 No error ..... default
- 1 Error

5 Mouse Output Buffer Full
- 0 Mouse output buffer empty ..... default
- 1 Mouse output buffer holds mouse data

4 Keylock Status
- 0 Locked
- 1 Free

3 Command / Data
- 0 Last write was data write..... default
- 1 Last write was command write

2 System Flag
- 0 Power-On Default ..... default
- 1 Self Test Successful

1 Input Buffer Full
- 0 Input Buffer Empty ..... default
- 1 Input Buffer Full

0 Keyboard Output Buffer Full
- 0 Keyboard Output Buffer Empty ..... default
- 1 Keyboard Output Buffer Full

KBC Control Register.....(R/W via Commands 20h/60h)

7 Reserved .....always reads 0

6 PC Compatibility
- 0 Disable scan conversion
- 1 Convert scan codes to PC format; convert 2-byte break sequences to 1-byte PC-compatible break codes..... default

5 Mouse Disable
- 0 Enable Mouse Interface..... default
- 1 Disable Mouse Interface

4 Keyboard Disable
- 0 Enable Keyboard Interface..... default
- 1 Disable Keyboard Interface

3 Reserved .....always reads 0

2 System Flag .....default=0
This bit may be read back as status register bit-2

1 Mouse Interrupt Enable
- 0 Disable mouse interrupts..... default
- 1 Generate interrupt on IRQ12 when mouse data comes in output bufer

0 Keyboard Interrupt Enable
- 0 Disable Keyboard Interrupts ..... default
- 1 Generate interrupt on IRQ1 when output buffer has been written.

Port 64 - Keyboard / Mouse Command .....WO

This port is used to send commands to the keyboard / mouse controller. The command codes recognized by the VT8231 are listed n the table below.

Note: The VT8231 Keyboard Controller is compatible with the VIA VT82C42 Industry-Standard Keyboard Controller except that due to its integrated nature, many of the input and output port pins are not available externally for use as general purpose I/O pins (even though P13-P16 are set on power-up as strapping options). In other words, many of the commands below are provided and "work", but otherwise perform no useful function (e.g., commands that set P12-P17 high or low). Also note that setting P10-11, P22-23, P26-27, and T0-1 high or low directly serves no useful purpose, since these bits are used to implement the keyboard and mouse ports and are directly controlled by keyboard controller logic.

Table 6. Keyboard Controller Command Codes

Code	Keyboard Command Code Description
20h	Read Control Byte (next byte is Control Byte)
21-3Fh	Read SRAM Data (next byte is Data Byte)
60h	Write Control Byte (next byte is Control Byte)
61-7Fh	Write SRAM Data (next byte is Data Byte)
9xh	Write low nibble (bits 0-3) to P10-P13
A1h	Output Keyboard Controller Version #
A4h	Test if Password is installed (always returns F1h to indicate not installed)
A7h	Disable Mouse Interface
A8h	Enable Mouse Interface
A9h	Mouse Interface Test (puts test results in port 60h) (value: 0=OK, 1=clk stuck low, 2=clk stuck high, 3=data stuck lo, 4=data stuck hi, FF=general error)
AAh	KBC self test (returns 55h if OK, FCh if not)
ABh	Keyboard Interface Test (see A9h Mouse Test)
ADh	Disable Keyboard Interface
AEh	Enable Keyboard Interface
AFh	Return Version #
B0h	Set P10 low
B1h	Set P11 low
B2h	Set P12 low
B3h	Set P13 low
B4h	Set P22 low
B5h	Set P23 low
B6h	Set P14 low
B7h	Set P15 low
B8h	Set P10 high
B9h	Set P11 high
BAh	Set P12 high
BBh	Set P13 high
BCh	Set P22 high
BDh	Set P23 high
BEh	Set P14 high
BFh	Set P15 high
C0h	Read input port (read P10-17 input data to the output buffer)
C1h	Poll input port low (read input data on P11-13 repeatably & put in bits 5-7 of status
C2h	Poll input port high (same except P15-17)
C8h	Unblock P22-23 (use before D1 to change active mode)
C9h	Reblock P22-23 (protection mechanism for D1)
CAh	Read mode (output KBC mode info to port 60 output buffer (bit-0=0 if ISA, 1 if PS/2)
D0h	Read Output Port (copy P10-17 output port values to port 60)
D1h	Write Output Port (data byte following is written to keyboard output port as if it came from keyboard)
D2h	Write Keyboard Output Buffer & clear status bit-5 (write following byte to keyboard)
D3h	Write Mouse Output Buffer & set status bit-5 (write following byte to mouse; put value in mouse input buffer so it appears to have come from the mouse)
D4h	Write Mouse (write following byte to mouse)
E0h	Read test inputs (T0-1 read to bits 0-1 of resp byte)
Exh	Set P23-P21 per command bits 3-1
Fxh	Pulse P23-P20 low for 6usec per command bits 3-0

All other codes not listed are undefined.

DMA Controller I/O Registers

Ports 00-0F - Master DMA Controller

Channels 0-3 of the Master DMA Controller control System DMA Channels 0-3. There are 16 Master DMA Controller registers:

I/O Address Bits 15-0	Register Name	
0000 0000 000x 0000	Ch 0 Base / Current Address	RW
0000 0000 000x 0001	Ch 0 Base / Current Count	RW
0000 0000 000x 0010	Ch 1 Base / Current Address	RW
0000 0000 000x 0011	Ch 1 Base / Current Count	RW
0000 0000 000x 0100	Ch 2 Base / Current Address	RW
0000 0000 000x 0101	Ch 2 Base / Current Count	RW
0000 0000 000x 0110	Ch 3 Base / Current Address	RW
0000 0000 000x 0111	Ch 3 Base / Current Count	RW
0000 0000 000x 1000	Status / Command	RW
0000 0000 000x 1001	Write Request	WO
0000 0000 000x 1010	Write Single Mask	WO
0000 0000 000x 1011	Write Mode	WO
0000 0000 000x 1100	Clear Byte Pointer F/F	WO
0000 0000 000x 1101	Master Clear	WO
0000 0000 000x 1110	Clear Mask	WO
0000 0000 000x 1111	R/W All Mask Bits	RW

Ports C0-DF - Slave DMA Controller

Channels 0-3 of the Slave DMA Controller control System DMA Channels 4-7. There are 16 Slave DMA Controller registers:

I/O Address Bits 15-0	Register Name	
0000 0000 1100 000x	Ch 4 Base / Current Address	RW
0000 0000 1100 001x	Ch 4 Base / Current Count	RW
0000 0000 1100 010x	Ch 5 Base / Current Address	RW
0000 0000 1100 011x	Ch 5 Base / Current Count	RW
0000 0000 1100 100x	Ch 6 Base / Current Address	RW
0000 0000 1100 101x	Ch 6 Base / Current Count	RW
0000 0000 1100 110x	Ch 7 Base / Current Address	RW
0000 0000 1100 111x	Ch 7 Base / Current Count	RW
0000 0000 1101 000x	Status / Command	RW
0000 0000 1101 001x	Write Request	WO
0000 0000 1101 010x	Write Single Mask	WO
0000 0000 1101 011x	Write Mode	WO
0000 0000 1101 100x	Clear Byte Pointer F/F	WO
0000 0000 1101 101x	Master Clear	WO
0000 0000 1101 110x	Clear Mask	WO
0000 0000 1101 111x	Read/Write All Mask Bits	WO

Note that not all bits of the address are decoded.

The Master and Slave DMA Controllers are compatible with the Intel 8237 DMA Controller chip. Detailed description of 8237 DMA controller operation can be obtained from the Intel Peripheral Components Data Book and numerous other industry publications.

Ports 80-8F - DMA Page Registers

There are eight DMA Page Registers, one for each DMA channel. These registers provide bits 16-23 of the 24-bit address for each DMA channel (bits 0-15 are stored in registers in the Master and Slave DMA Controllers). They are located at the following I/O Port addresses:

I/O Address Bits 15-0	Register Name	
0000 0000 1000 0111	Channel 0 DMA Page (M-0)	RW
0000 0000 1000 0011	Channel 1 DMA Page (M-1)	RW
0000 0000 1000 0001	Channel 2 DMA Page (M-2)	RW
0000 0000 1000 0010	Channel 3 DMA Page (M-3)	RW
0000 0000 1000 1111	Channel 4 DMA Page (S-0)	RW
0000 0000 1000 1011	Channel 5 DMA Page (S-1)	RW
0000 0000 1000 1001	Channel 6 DMA Page (S-2)	RW
0000 0000 1000 1010	Channel 7 DMA Page (S-3)	RW

DMA Controller Shadow Registers

The DMA Controller shadow registers are enabled by setting function 0 Rx77 bit 0. If the shadow registers are enabled, they are read back at the indicated I/O port instead of the standard DMA controller registers (writes are unchanged).

Port 0 –Channel 0 Base Address ..... RO
Port 1 –Channel 0 Byte Count ..... RO
Port 2 –Channel 1 Base Address ..... RO
Port 3 –Channel 1 Byte Count ..... RO
Port 4 –Channel 2 Base Address ..... RO
Port 5 –Channel 2 Byte Count ..... RO
Port 6 –Channel 3 Base Address ..... RO
Port 7 –Channel 3 Byte Count ..... RO

Port 8 –1st Read Channel 0-3 Command Register..... RO
Port 8 –2nd Read Channel 0-3 Request Register ..... RO
Port 8 –3rd Read Channel 0 Mode Register..... RO
Port 8 –4th Read Channel 1 Mode Register ..... RO
Port 8 –5th Read Channel 2 Mode Register ..... RO
Port 8 –6th Read Channel 3 Mode Register ..... RO

Port F –Channel 0-3 Read All Mask..... RO

Port C4 –Channel 5 Base Address ..... RO
Port C6 –Channel 5 Byte Count..... RO
Port C8 –Channel 6 Base Address ..... RO
Port CA –Channel 6 Byte Count..... RO
Port CC –Channel 7 Base Address ..... RO
Port CE –Channel 7 Byte Count ..... RO

Port D0 –1st Read Channel 4-7 Command Register..... RO
Port D0 –2nd Read Channel 4-7 Request Register ..... RO
Port D0 –3rd Read Channel 4 Mode Register..... RO
Port D0 –4th Read Channel 5 Mode Register ..... RO
Port D0 –5th Read Channel 6 Mode Register ..... RO
Port D0 –6th Read Channel 7 Mode Register ..... RO

Port DE –Channel 4-7 Read All Mask..... RO

Interrupt Controller I/O Registers

Ports 20-21 - Master Interrupt Controller

The Master Interrupt Controller controls system interrupt channels 0-7. Two registers control the Master Interrupt Controller. They are:

I/O Address Bits 15-0	Register Name	
0000 0000 001x xxx0	**Master Interrupt Control**	**RW**
0000 0000 001x xxx1	**Master Interrupt Mask**	**RW**

Note that not all bits of the address are decoded.

The Master Interrupt Controller is compatible with the Intel 8259 Interrupt Controller chip. Detailed descriptions of 8259 Interrupt Controller operation can be obtained from the Intel Peripheral Components Data Book and numerous other industry publications.

Ports A0-A1 - Slave Interrupt Controller

The Slave Interrupt Controller controls system interrupt channels 8-15. The slave system interrupt controller also occupies two register locations:

I/O Address Bits 15-0	Register Name	
0000 0000 101x xxx0	**Slave Interrupt Control**	**RW**
0000 0000 101x xxx1	**Slave Interrupt Mask**	**RW**

Note that not all address bits are decoded.

The Slave Interrupt Controller is compatible with the Intel 8259 Interrupt Controller chip. Detailed descriptions of 8259 Interrupt Controller operation can be obtained from the Intel Peripheral Components Data Book and numerous other industry publications.

Interrupt Controller Shadow Registers

The following shadow registers are enabled by setting function 0 Rx47[4]. If the shadow registers are enabled, they are read back at the indicated I/O port instead of the standard interrupt controller registers (writes are unchanged).

Port 20 - Master Interrupt Control Shadow ..... RO
Port A0 - Slave Interrupt Control Shadow ..... RO

- **7 Reserved** ..... always reads 0
- **6 OCW3 bit 2 (POLL)**
- **5 OCW3 bit 0 (RIS)**
- **4 OCW3 bit 5 (SMM)**
- **3 OCW2 bit 7 (R)**
- **2 ICW4 bit 4 (SFNM)**
- **1 ICW4 bit 1 (AEOI)**
- **0 ICW1 bit 3 (LTIM)**

Port 21 - Master Interrupt Mask Shadow..... RO
Port A1 - Slave Interrupt Mask Shadow ..... RO

- **7-5 Reserved** ..... always reads 0
- **4-0 T7-T3 of Interrupt Vector Address**

Timer / Counter Registers

Ports 40-43 - Timer / Counter I/O Registers

There are 4 Timer / Counter registers:

I/O Address Bits 15-0	Register Name	
0000 0000 010x xx00	**Timer / Counter 0 Count**	**RW**
0000 0000 010x xx01	**Timer / Counter 1 Count**	**RW**
0000 0000 010x xx10	**Timer / Counter 2 Count**	**RW**
0000 0000 010x xx11	**Timer / Counter Cmd Mode**	**WO**

Note that not all bits of the address are decoded.

The Timer / Counters are compatible with the Intel 8254 Timer / Counter chip. Detailed descriptions of 8254 Timer / Counter operation can be obtained from the Intel Peripheral Components Data Book and numerous other industry publications.

Timer / Counter Shadow Registers

The following shadow registers are enabled for readback by setting function 0 Rx47[4]. If the shadow registers are enabled, they are read back at the indicated I/O port instead of the standard timer / counter registers (writes are unchanged).

Port 40 – Counter 0 Base Count Value (LSB 1st MSB 2nd)RO
Port 41 – Counter 1 Base Count Value (LSB 1st MSB 2nd)RO
Port 42 – Counter 2 Base Count Value (LSB 1st MSB 2nd)RO

CMOS / RTC I/O Registers

Port 70 - CMOS Address.....RW

7 **NMI Disable** ..... RW
- 0 Enable NMI Generation. NMI is asserted on encountering SERR# on the PCI bus.
- 1 Disable NMI Generation.....default

6-0 **CMOS Address** (lower 128 bytes) ..... RW

Port 71 - CMOS Data .....RW

7-0 **CMOS Data** (128 bytes)

Note: Ports 70-71 may be accessed if Rx51 bit-3 is set to one to select the internal RTC. If Rx51 bit-3 is set to zero, accesses to ports 70-71 will be directed to an external RTC.

Port 74 - CMOS Address.....RW

7-0 **CMOS Address** (256 bytes) ..... RW

Port 75 - CMOS Data .....RW

7-0 **CMOS Data** (256 bytes)

Note: Ports 74-75 may be accessed only if Function 0 Rx5B bit-1 is set to one to enable the internal RTC SRAM and if Rx48 bit-3 (Port 74/75 Access Enable) is set to one to enable port 74/75 access.

Note: Ports 70-71 are compatible with PC industry-standards and may be used to access the lower 128 bytes of the 256-byte on-chip CMOS RAM. Ports 74-75 may be used to access the full on-chip extended 256-byte space in cases where the on-chip RTC is disabled.

Note: The system Real Time Clock (RTC) is part of the "CMOS" block. The RTC control registers are located at specific offsets in the CMOS data area (0-0Dh and 7D-7Fh). Detailed descriptions of CMOS / RTC operation and programming can be obtained from the VIA VT82887 Data Book or numerous other industry publications. For reference, the definition of the RTC register locations and bits are summarized in the following table:

Offset	Description		Binary Range	BCD Range
00	**Seconds**		00-3Bh	00-59h
01	**Seconds Alarm**		00-3Bh	00-59h
02	**Minutes**		00-3Bh	00-59h
03	**Minutes Alarm**		00-3Bh	00-59h
04	**Hours**	am 12hr:	01-1Ch	01-12h
		pm 12hr:	81-8Ch	81-92h
		24hr:	00-17h	00-23h
05	**Hours Alarm**	am 12hr:	01-1Ch	01-12h
		pm 12hr:	81-8Ch	81-92h
		24hr:	00-17h	00-23h
06	**Day of the Week**	Sun=1:	01-07h	01-07h
07	**Day of the Month**		01-1Fh	01-31h
08	**Month**		01-0Ch	01-12h
09	**Year**		00-63h	00-99h

0A **Register A**

7	**UIP**	Update In Progress
6-4	**DV2-0**	Divide (010=ena osc & keep time)
3-0	**RS3-0**	Rate Select for Periodic Interrupt

0B **Register B**

7	**SET**	Inhibit Update Transfers
6	**PIE**	Periodic Interrupt Enable
5	**AIE**	Alarm Interrupt Enable
4	**UIE**	Update Ended Interrupt Enable
3	**SQWE**	No function (read/write bit)
2	**DM**	Data Mode (0=BCD, 1=binary)
1	**24/12**	Hours Byte Format (0=12, 1=24)
0	**DSE**	Daylight Savings Enable

0C **Register C**

7	**IRQF**	Interrupt Request Flag
6	**PF**	Periodic Interrupt Flag
5	**AF**	Alarm Interrupt Flag
4	**UF**	Update Ended Flag
3-0	**0**	Unused (always read 0)

0D **Register D**

7	**VRT**	Reads 1 if VBAT voltage is OK
6-0	**0**	Unused (always read 0)

0E-7C **Software-Defined Storage Registers** (111 Bytes)

Offset	Extended Functions	Binary Range	BCD Range
7D	**Date Alarm**	01-1Fh	01-31h
7E	**Month Alarm**	01-0Ch	01-12h
7F	**Century Field**	13-14h	19-20h

80-FF **Software-Defined Storage Registers** (128 Bytes)

Table 7. CMOS Register Summary

Super-IO / KBC Configuration Index / Data Registers

Super-IO and Keyboard / Mouse Controller configuration registers are accessed by performing I/O operations to / from an index / data pair of registers in system I/O space at port addresses 3F0h and 3F1h. The configuration registers accessed using this mechanism are used to configure the Keyboard / Mouse Controller at index values in the range of E0-EF and Super-I/O registers (parallel port, serial ports, IR port, and floppy controller) at index values in the range of F0-FF.

Super IO and/or Keyboard / Mouse Controller configuration is accomplished in three steps:

1) Enter configuration mode (set Function 0 Rx50[2] = 0 to enable Super-IO configuration and/or Rx51[1] = 1 to enable Keyboard / Mouse Controller configuration)
2) Configure the chip
   a) Write index to port 3F0
   b) Read / write data from / to port 3F1
   c) Repeat a and b for all desired registers
3) Exit configuration mode (set Function 0 Rx51[1] = 0)

Port 3F0h – Super-IO Configuration Index ..... RW

7-0 Index value

Function 0 PCI configuration space register Rx50[2] must be set to 1 to enable access to the Super-I/O configuration registers.

Port 3F1h – Super-I/O Configuration Data..... RW

7-0 Data value

This register shares a port with the Floppy Status Port (which is read only). This port is accessible only when Rx50[2] is set to 1 (the floppy status port is accessed if Rx50[2] = 0).

Keyboard / Mouse Controller Configuration Registers

These registers are accessed via the port 3F0 / 3F1 index / data register pair with Function 0 Rx51[1] = 1 using the indicated index values below

Index E0 – KBC Wakeup Enable (80h)..... RW

7 Win98 Keyboard Power Key Wake-up
- 0 Disable
- 1 Enable ..... default

6-3 Reserved ..... always reads 0

2 Reserved (Do Not Program)..... default = 0

1 PS/2 Mouse Wake-up
- 0 Disable..... default
- 1 Enable

0 Keyboard Wake-up
- 0 Disable..... default
- 1 Enable

Index E1 – Keyboard Scan Code Reference Set 0 (F0h) RW

7-0 Keyboard First Reference Scan Code .....def = F0h

Index E2 – Keyboard Scan Code Reference Set 1 (00h) RW

7-0 Keyboard Second Reference Scan Code .. def = 00h

Index E3 – Keyboard Scan Code Reference Set 2 (00h) RW

7-0 Keyboard Third Reference Scan Code .... def = 00h

Index E4 – Keyboard Scan Code Reference Set 3 (00h) RW

7-0 Keyboard Fourth Reference Scan Code .. def = 00h

Index E5 – Keyboard Scan Code Reference Set 4 (00h) RW

7-0 Keyboard Fifth Reference Scan Code..... def = 00h

Index E6 – PS2 Mouse Button Status Scan Code (09h) RW

7-0 PS2 Mouse Button Status Ref Scan Code def = 00h

Super-I/O Configuration Registers

These registers are accessed via the port 3F0 / 3F1 index / data register pair with Function 0 Rx50[2] = 1using the indicated index values below

Index F0 – Super-IO Device ID (3Ch).....RO

7-0 Super-IO ID .....default = 3Ch

Index F1 – Super-IO Device Revision (01h) .....RO

7-0 Super-IO Revision Code ..... default = 01h

Index F2 – Super-IO Function Select (03h).....RW

7-5 Reserved ..... always reads 0

4 Floppy Controller Enable
- 0 Disable .....default
- 1 Enable

3 Reserved ..... always reads 0

2 Serial Port Enable
- 0 Disable .....default
- 1 Enable

1-0 Parallel Port Mode / Enable
- 00 SPP (Unidirectional mode)
- 01 ECP
- 10 EPP
- 11 Parallel Port Disabled .....default

Index F3 – Super-IO Power Down Control ..... RW

7 Reserved .....always reads 0

6 Software Power Down
- 0 Normal operation..... default
- 1 Power Down

5 Clock Power Down
- 0 Normal operation..... default
- 1 Power Down

4 Parallel Port Power Down
- 0 Normal operation..... default
- 1 Power Down

3 Reserved .....always reads 0

2 Serial Port Power Down
- 0 Normal operation..... default
- 1 Power Down

1 FDC Power Down
- 0 Normal operation..... default
- 1 Power Down

0 All Power Down
- 0 Normal operation..... default
- 1 Power Down All

Index F4 – Serial Port I/O Base Address ..... RW

7-1 I/O Address 9-3 ..... default = 0
0 Must be 0 ..... default = 0

Index F6 – Parallel Port I/O Base Address ..... RW

7-0 I/O Address 9-2 ..... default = 0

If EPP is not enabled, the parallel port can be set to 192 locations on 4-byte boundaries from 100h to 3FCh. If EPP is enabled, the parallel port can be set to 96 locations on 8-byte boundaries from 100h to 3F8h. 16-bit address decode will be performed with upper address bits 10-15 equal to zero.

Index F7 – Floppy Controller I/O Base Address ..... RW

7-2 I/O Address 9-4 ..... default = 0
1-0 Must be 0 ..... default = 0

Index F9 – Serial Port Control ..... RW

7-4 Reserved ..... always reads 0
3 Serial Port Power-Down State
0 Normal ..... default
1 Tristate output in power down mode
2 Reserved ..... always reads 0
1 High Speed Serial Port
0 Disable ..... default
1 Enable
0 Serial Port MIDI
0 Disable ..... default
1 Enable

Index FA – Parallel Port Control ..... RW

7 PS2 Type BiDirectionl Parallel Port
0 Disable ..... default
1 Enable
6 EPP Direction by Register not by IOW
0 Disable ..... default
1 Enable
5 EPP+ECP
0 Disable ..... default
1 Enable
4 EPP Version
0 Version 1.9 ..... default
1 Version 1.7
3 SPP Mode IRQ Polarity
0 Normal ..... default
1 Inverted
2-0 Reserved ..... always reads 0

Index FB – Floppy Controller Control ..... RW

7 Reserved ..... always reads 0

6 "GPI Pin" Floppy Drive On Parallel Port

0 Parallel Port (SPP) Mode .....default
1 FDC or SPP Mode determined by GPI Pin

5 "Software" Floppy Drive On Parallel Port

0 Parallel Port (SPP) Mode .....default
1 FDC Mode

Bits 6-5 are used in notebook applications to allow attachment of an external floppy drive using the parallel port I/O connector (bit-6 enables the mode to be determined via a general purpose input pin and bit-5 allows control of the mode unconditionally via software).

SPP Mode	Pin Type	FDC Mode	Pin Type
STROBE#	I/O	-	n/a
PD0	I/O	INDEX#	I
PD1	I/O	TRK00#	I
PD2	I/O	WRTPRT#	I
PD3	I/O	RDATA#	I
PD4	I/O	DSKCHG#	I
PD5	I/O	-	n/a
PD6	I/O	-	n/a
PD7	I/O	-	n/a
ACK#	I	DS1#	O
BUSY	I	MTR1#	O
PE	I	WDATA#	O
SLCT	I	WGATE#	O
AUTOFD#	I/O	DRVEN0	O
ERROR#	I	HDSEL#	O
PINIT#	I/O	DIR#	O
SLCTIN#	I/O	STEP#	O

4 3-Mode FDD

0 Disable .....default
1 Enable

3 FDC IRQ Polarity

0 Normal .....default
1 Inverted

2 Four Floppy Drive Option

0 Internal 2-Drive Decoder .....default
1 External 4-Drive Decoder

1 FDC DMA Non-Burst

0 Burst .....default
1 Non-Burst

0 FDC Drive Swap

0 Disable .....default
1 Enable

Index FC – Floppy Controller Drive Type..... RW

7-6 Floppy Drive 3 (see table below)
5-4 Floppy Drive 2 (see table below)
3-2 Floppy Drive 1 (see table below)
1-0 Floppy Drive 0 (see table below)

	DRVEN1	DRVEN0
00	DRATE0	DENSEL
01	DRATE0	DRATE1
10	DRATE0	DENSEL#
11	DRATE1	DRATE0

Index FE – Test Mode A (Do Not Program)..... RW

Index FF – Test Mode B (Do Not Program) ..... RW

Super-I/O I/O Ports

Floppy Disk Controller Registers

These registers are located at I/O ports which are offsets from "FDCBase" (index F7h of the Super-I/O configuration registers). FDCBase is typically set to allow these ports to be accessed at the standard floppy disk controller address range of 3F0-3F7h.

Port FDCBase+2 – FDC Command ..... RW

- **7 Motor 3 (unused in VT8231: no MTR3# pin)**
- **6 Motor 2 (unused in VT8231: no MTR2# pin)**
- **5 Motor 1**
  - 0 Motor Off
  - 1 Motor On
- **4 Motor 0**
  - 0 Motor Off
  - 1 Motor On
- **3 DMA and IRQ Channels**
  - 0 Disabled
  - 1 Enabled
- **2 FDC Reset**
  - 0 Execute FDC Reset
  - 1 FDC Enabled
- **1-0 Drive Select**
  - 00 Select Drive 0
  - 01 Select Drive 1
  - 1x -reserved-

Port FDCBase+4 – FDC Main Status ..... RO

- **7 Main Request**
  - 0 Data register not ready
  - 1 Data register ready
- **6 Data Input / Output**
  - 0 CPU => FDC
  - 1 FDC => CPU
- **5 Non-DMA Mode**
  - 0 FDC in DMA mode
  - 1 FDC not in DMA mode
- **4 FDC Busy**
  - 0 FDC inactive
  - 1 FDC active
- **3-2 Reserved** ..... always reads 0
- **1 Drive 1 Active**
  - 0 Drive inactive
  - 1 Drive performing a positioning change
- **0 Drive 0 Active**
  - 0 Drive inactive
  - 1 Drive performing a positioning change

Port FDCBase+4 – FDC Data Rate Select ..... WO

- **7 Software Reset**
  - 0 Normal operation..... default
  - 1 Execute FDC reset (this bit is self clearing)
- **6 Power Down**
  - 0 Normal operation..... default
  - 1 Power down FDC logic
- **5 Reserved** ..... always reads 0
- **4-2 Precompensation Select**

  Selects the amount of write precompensation to be used on the WDATA output:
  - 000 Default..... default
  - 001 41.7 ns
  - 010 93.3 ns
  - 011 125.0 ns
  - 100 166.7 ns
  - 101 208.3 ns
  - 110 250.0 ns
  - 111 0.0 ns (disable)
- **1-0 Data Rate**

	MFM	FM	Drive Type
00	500K	250K bps	1.2MB 5" or 1.44 MB 3"
01	300K	150K bps	360KB 5"
10	250K	125K bps	720KB 3" ..... default
11	1M	illegal bps	

Note: these bits are not changed by software reset

Port FDCBase+5 – FDC Data ..... RW

Port FDCBase+7 – FDC Disk Change Status ..... RO

- **7 Disk Change**
  - 0 Floppy not changed
  - 1 Floppy changed since last instruction
- **6-3 Undefined** ..... always read 1
- **2-1 Data Rate**
  - 00 500 Kbit/sec (1.2MB 5" or 1.44 MB 3" drive)
  - 01 300 Kbit/sec (360KB 5" drive)
  - 10 250 Kbit/sec (720KB 3" drive)
  - 11 1 Mbit/sec
- **0 High Density Rate**
  - 0 500 Kbit/sec or 1 Mbit/sec selected
  - 1 250 Kbit/set or 300 Kbit/sec selected

Parallel Port Registers

These registers are located at I/O ports which are offsets from "LPTBase" (index F6h of the Super-I/O configuration registers). LPTBase is typically set to allow these ports to be accessed at the standard parallel port address range of 378-37Fh.

Port LPTBase+0 – Parallel Port Data ..... RW

7-0 Parallel Port Data

Port LPTBase+1 – Parallel Port Status ..... RO

7 BUSY#
- 0 Printer busy, offline, or error
- 1 Printer not busy

6 ACK#
- 0 Data transfer to printer complete
- 1 Data transfer to printer in progress

5 PE
- 0 Paper available
- 1 No paper available

4 SLCT
- 0 Printer offline
- 1 Printer online

3 ERROR#
- 0 Printer error
- 1 Printer OK

2-0 Reserved ..... always read 1 bits

Port LPTBase+2 – Parallel Port Control ..... RW

7-5 Undefined ..... always read back 1

4 Hardware Interrupt
- 0 Disable ..... default
- 1 Enable

3 Printer Select
- 0 Deselect printer ..... default
- 1 Select printer

2 Printer Initialize
- 0 Initialize Printer ..... default
- 1 Allow printer to operate normally

1 Automatic Line Feed
- 0 Host handles line feeds ..... default
- 1 Printer does automatic line feeds

0 Strobe
- 0 No data transfer ..... default
- 1 Transfer data to printer

Port LPTBase+3 – Parallel Port EPP Address ..... RW

Port LPTBase+4 – Parallel Port EPP Data Port 0 ..... RW

Port LPTBase+5 – Parallel Port EPP Data Port 1 ..... RW

Port LPTBase+6 – Parallel Port EPP Data Port 2 ..... RW

Port LPTBase+7 – Parallel Port EPP Data Port 3 ..... RW

Port LPTBase+400h – Parallel Port ECP Data / Cfg A RW

Port LPTBase+401h – Parallel Port ECP Config B ..... RW

Port LPTBase+402h – Parallel Port ECP Extd Ctrl ..... RW

7-5 Parallel Port Mode Select
- 000 Standard Mode ..... default
- 001 PS/2 Mode
- 010 FIFO Mode
- 011 ECP Mode
- 100 EPP Mode
- 101 -reserved-
- 110 -reserved-
- 111 Configuration Mode

4 Parallel Port Interrupt Disable
- 0 Enable an interrupt pulse to be generated on the high to low edge of the fault. An interrupt will also be generated if the fault condition is asserted and this bit is written from 1 to 0.
- 1 Disable the interrupt generated on the asserting edge of the fault condition

3 Parallel Port DMA Enable
- 0 Disable DMA unconditionally
- 1 Enable DMA

2 Parallel Port Interrupt Pending
- 0 Interrupt not pending
- 1 Interrupt pending (DMA & interrupts disabled)

This bit is set to 1 by hardware and must be written to 0 to re-enable interrupts

1 FIFO Full ..... RO
- 0 FIFO has at least 1 free byte
- 1 FIFO full or cannot accept byte

0 FIFO Empty ..... RO
- 0 FIFO contains at least 1 byte of data
- 1 FIFO is completely empty

Serial Port 1 Registers

These registers are located at I/O ports which are offsets from "COM1Base" (index F4h of the Super-I/O configuration registers). COM1Base is typically set to allow these ports to be accessed at the standard serial port 1 address range of 3F8-3FFh.

Port COM1Base+0 – Transmit / Receive Buffer.....RW

7-0 Serial Data

Port COM1Base+1 – Interrupt Enable.....RW

7-4 Undefined .....always read 0
3 Interrupt on Hnadshake Input State Change
2 Intr on Parity, Overrun, Framing Error or Break
1 Interrupt on Transmit Buffer Empty
0 Interrupt on Receive Data Ready

Port COM1Base+2 – Interrupt Status.....RO

7-3 Undefined .....always read 0
2-1 Interrupt ID (0=highest priority)
00 Priority 3 (Handshake Input Changed State)
01 Priority 2 (Transmit Buffer Empty)
10 Priority 1 (Data Received)
11 Priority 0 (Serialization Error or Break)
0 Interrupt Pending
0 Interrupt Pending
1 No Interrupt Pending

Port COM1Base+2 – FIFO Control.....WO

Port COM1Base+3 – UART Control .....RW

7 Divisor Latch Access
0 Select transmit / receive registers
1 Select divisor latch
6 Break
0 Break condition off
1 Break condition on
5-3 Parity
000 None
001 Odd
011 Even
101 Mark
111 Space
2 Stop Bits
0 1
1 2
1-0 Data Bits
00 5
01 6
10 7
11 8

Port COM1Base+4 – Handshake Control..... RW

7-5 Undefined ..... always read 0
4 Loopback Check
0 Normal operation
1 Loopback enabled
3 General Purpose Output 2 (unused in VT8231)
2 General Purpose Output 1 (unused in VT8231)
1 Request To Send
0 Disabled
1 Enabled
0 Data Terminal Ready
0 Disabled
1 Enabled

Port COM1Base+5 – UART Status ..... RW

7 Undefined ..... always read 0
6 Transmitter Empty
0 1 byte in transmit hold or transmit shift register
1 0 bytes transmit hold and transmit shift regs
5 Transmit Buffer Empty
0 1 byte in transmit hold register
1 Transmit hold register empty
4 Break Detected
0 No break detected
1 Break detected
3 Framing Error Detected
0 No error
1 Error
2 Parity Error Detected
0 No error
1 Error
1 Overrun Error Detected
0 No error
1 Error
0 Received Data Ready
0 No received data available
1 Received data in receiver buffer register

Port COM1Base+6 – Handshake Status ..... RW

7 DCD Status (1=Active, 0=Inactive)
6 RI Status (1=Active, 0=Inactive)
5 DSR Status (1=Active, 0=Inactive)
4 CTS Status (1=Active, 0=Inactive)
3 DCD Changed (1=Changed Since Last Read)
2 RI Changed (1=Changed Since Last Read)
1 DSR Changed (1=Changed Since Last Read)
0 CTS Changed (1=Changed Since Last Read)

Port COM1Base+7 – Scratchpad..... RW

7 Scratchpad Data

Port COM1Base+9-8 – Baud Rate Generator Divisor.. RW

15-0 Divisor Value for Baud Rate Generator
Baud Rate = 115,200 / Divisor
(e.g., setting this register to 1 selects 115.2 Kbaud)

SoundBlaster Pro Port Registers

These registers are located at offsets from "SBPBase" (defined in Rx43 of Audio Function 5 PCI configuration space). SBPBase is typically set to allow these ports to be accessed at the standard SoundBlaster Pro port address of 220h or 240h.

FM Registers

Port SBPBase+0 – FM Left Channel Index / Status .....RW

7-0 FM Right Channel Index / Status

Port SBPBase+1 – FM Left Channel Data .....WO

7-0 Right Channel FM Data

Port SBPBase+2 – FM Right Channel Index / Status....RW

7-0 FM Right Channel Index / Status

Port SBPBase+3 – FM Right Channel Data .....WO

7-0 Right Channel FM Data

Port 388h or SBPBase+8 – FM Index / Status.....RW

7-0 FM Index / Status (Both Channels)

Writing to this port programs both the left and right channels (the write programms port offsets 0 and 2 as well)

Port 389h or SBPBase+9 – FM Data .....WO

7-0 FM Data (Both Channels)

Writing to this port programs both the left and right channels (the write programms port offsets 1 and 3 as well)

Mixer Registers

Port SBPBase+4 – Mixer Index .....WO

7-0 Mixer Index

Port SBPBase+5 – Mixer Data.....RW

7-0 Mixer Data

Sound Processor Registers

Port SBPBase+6 – Sound Processor Reset.....WO

0 1 = Sound Processor Reset

Port SBPBase+A – Sound Processor Read Data .....RO

7-0 Sound Processor Read Data

Port SBPBase+C – Sound Processor Command / Data.WO

7-0 Sound Processor Command / Write Data

Port SBPBase+C – Sound Processor Buffer Status .....RO

7 1 = Sound Processor Command / Data Port Busy

Port SBPBase+E – Sound Processor Data Avail Status .RO

7 1 = Sound Processor Data Available

Register Summary - FM

Index	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
01	Test							
02	Fast Counter (80 usec)							
03	Slow Counter (320 usec)							
04	IRQ	MFC	MSC				SSSC	SSFC
08	CSM	SEL						
20-35	AM	VIB	EGT	KSR	Multi			
40-55	KSL		Total Level (TL)					
60-75	Attack Rate (AR)				Decay Rate (DR)			
80-95	Sustain Level (SL)				Release Rate (RR)			
A0-A8	F-Number							
B0-B8			Key	Block			F-Number	
BD	Int AM VIB		Ryth	Bass	Snare	Tom	Cym	HiHat
C0-C8					Feedback			FM
E0-F5							WS	

MFC=Mask Fast Counter SSFC=Start / Stop Fast Counter
MSC=Mask Slow Counter SSSC=Start / Stop Slow Counter

Register Summary – Mixer

Index	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
00	Data Reset							
02	SP Volume L				SP Volume R			
0A						Mic Vol		
0C			Finp		TFIL	Select		
0E			Fout				ST	
22	General Volume				General Volume			
26	FM Volume L				FM Volume R			
28	CD Volume L				CD Volume R			
2E	Line Volume L				Line Volume R			

Finp = Input Filter
Fout = Output Filter
TFIL = Input Filter Type
ST = Stereo / Mono Mode
Select = Input Choices (0=Microphone, 1=CD, 3=Line)

Command Summary – Sound Processor (see next page)

Command Summary – Sound Processor

#	Type	Command
10	Play	8 bits directly
14	Play	8 bits via DMA
91	Play	High-speed 8 bits via DMA
16	Play	2-bit compressed via DMA
17	Play	2-bit compressed via DMA with reference
74	Play	4-bit compressed via DMA
75	Play	4-bit compressed via DMA with reference
76	Play	2.6-bit compressed via DMA
77	Play	2.6-bit compressed via DMA with reference
20	Record	Direct
24	Record	Via DMA
99	Record	High-speed 8 bits via DMA
D1	Speaker	Turn on speaker connection
D3	Speaker	Turn off speaker connection
D8	Speaker	Get speaker setting
40	Misc	Set sample rate
48	Misc	Set block length
80	Misc	Set silence block
D0	Misc	Stop DMA
D4	Misc	Continue DMA
E1	Misc	Get version
30	MIDI	Direct MIDI input
31	MIDI	MIDI input via interrupt
32	MIDI	Direct MIDI input with time stamp
33	MIDI	MIDI input via interrupt with time stamp
34	MIDI	Direct MIDI UART mode
35	MIDI	MIDI UART mode via interrupt
36	MIDI	Direct MIDI UART mode with time stamp
37	MIDI	MIDI UART mode via interrupt with time stamp
38	MIDI	Send MIDI code

Game Port Registers

These registers are fixed at the standard game port address of 201h.

I/O Port 201h – Game Port Status ..... RO

7	**Joystick B Button 2 Status**
6	**Joystick B Button 1 Status**
5	**Joystick A Button 2 Status**
4	**Joystick A Button 1 Status**
3	**Joystick B One-Shot Status for Y-Potentiometer**
2	**Joystick B One-Shot Status for X-Potentiometer**
1	**Joystick A One-Shot Status for Y-Potentiometer**
0	**Joystick A One-Shot Status for X-Potentiometer**

I/O Port 201h – Start One-Shot ..... WO

7-0 (Value Written is Ignored)

Fast IR Registers

These registers are located ain the I/O address space at offsets from the "FIR I/O Address Base" located in Function 0 Rx6B-6A[15:7].

I/O Port Offset 11-10 – Infrared Configuration (0000). RW

15-13 Reserved ..... always reads 0

12 Physical Layer Transmitter
- 0 Disable .....default
- 1 Enable

11 Physical Layer Receiver
- 0 Disable .....default
- 1 Enable (if transmitter active (see bit-4), loopback must be enabled, otherwise the receiver will not be enabled even if this bit is set).

10 Memory Access by ISA DMA Controller
- 0 Disable .....default
- 1 Enable

9 Receive Small / Runtime Packets (<4 bytes) (SIR Mode Only)
- 0 Disable .....default
- 1 Enable

8 SIR Receive Filter Transparency Destuffing
- 0 Enable .....default
- 1 Disable

7 CRC
- 0 32-bit CRC.....default
- 1 16-bit CRC

6 FIR Mode
- 0 Disable .....default
- 1 Enable

5 MIR Mode
- 0 Disable .....default
- 1 Enable

4 SIR Mode
- 0 Disable .....default
- 1 Enable

3 Receive SIR Byte Filter
- 0 Disable .....default
- 1 Enable (if SIR mode bit is set)

2 SIR Test Mode
- 0 Disable .....default
- 1 Enable (allow SIR filter to be used when not in SIR mode)

1 Tx LED Output Inversion (TXD Pin)
- 0 Don't Invert .....default
- 1 Invert

0 Rx LED Input Inversion (FIRRXD & SIRRXD)
- 0 Don't Invert .....default
- 1 Invert

I/O Port Offset 12 – Infrared SIR BOF (C0h)..... RW

7-0 SIR Format Begin of Flag ..... default = C0h

I/O Port Offset 13 – Infrared SIR EOF (C1h)..... RW

7-0 SIR Format End of Flag ..... default = C1h

I/O Port Offset 15 – Infrared Status & Control 0 (00).. RW

7 Physical Layer Interface and Clock Generation Circuits
- 0 Disable..... default
- 1 Enable

6 Configuration Error ..... RO
- 0 No error ..... default
- 1 More than one mode selected

5 FIR On ..... RO
- 0 FIR not configured ..... default
- 1 Valid FIR Configuration

4 MIR On ..... RO
- 0 MIR not configured..... default
- 1 Valid MIR Configuration

3 SIR On ..... RO
- 0 SIR not configured ..... default
- 1 Valid SIR Configuration

2 Physical Layer Transmitter ..... RO
- 0 Disabled..... default
- 1 Enabled

1 Physical Layer Receiver ..... RO
- 0 Disabled..... default
- 1 Enabled

0 16-bit CRC ..... RO
- 0 32-bit CRC Enabled ..... default
- 1 16-bit CRC Enabled

I/O Port Offset 17-16 – Infrared Status1 (0000) .....RO

15-10 Baud Rate ..... default = 0
9-5 SIR / Indication Pulse Width ..... default = 0
4-0 MIR Start / FIR Preamble Bytes to Send default = 0
MIR: # of start flags plus one (0 = 1 byte)
FIR: # of preamble bytes plus one (0 = 1 byte)

I/O Port Offset 19-18 – Infrared Configuration 1 (0000)RW

15-10 Baud Rate ..... default = 0
9-5 SIR / Indication Pulse Width ..... default = 0
4-0 MIR Start / FIR Preamble Bytes to Send default = 0
MIR: # of start flags plus one (0 = 1 byte)
FIR: # of preamble bytes plus one (0 = 1 byte)

	Baud Rate	Pulse Width			
Mode	Setting	Min	Nom	Max	Preamble
SIR (2400)	47	0	12	12	Don't Care
SIR (9600)	11	0	12	12	Don't Care
SIR (19200)	5	1	12	12	Don't Care
SIR (38400)	2	3	12	14	Don't Care
SIR (57600)	1	5	12	16	Don't Care
SIR (115200)	0	11	12	20	Don't Care
MIR	0		8		1
FIR	0		Don't Care		14

I/O Port Offset 1B-1A – Infrared Configuration 2 (0000)RW

15-13 Reserved ..... always reads 0
12-0 Max Receive Packet Length (Bytes)..... default = 0

I/O Port Offset 1E – Infrared Configuration 3 (04h).... RW

7-6 FIR Adjustment Filter Rate
00 High Filter ..... default
01 Medium High Filter
10 Medium Low Filter
11 Low Filter
5 FIR Adjacent Pulse Width Packet Circuit
0 Enable..... default
1 Disable
4 FIR Pulse Width Adjustment Circuit
0 Enable..... default
1 Disable
3-2 Physical Layer Clock Speed
..... Always reads 01 (48MHz)
1 # of Receive Paths
0 1 Receive & 1 Output Pin (slow or fast) ..... def
1 2 Receive Paths
0 Optical Module Mode Pin Polarity (1 Rcv Path)
0 High Signal Select Slow Speed..... default
1 Low Signal Selects Slow Speed

I/O Port Offset 20 – IR Host Control (00h) ..... RW

7 Interrupt Enable
- 0 Disable ..... default
- 1 Enable

6 Transmit Start

Writing a 1 to this bit initiates execution of the IR transmit mode programmed in the IR configuraton registers. DMA and all necessary registers must be set up prior to writing a 1 to this register. Writing 0 has no effect. This bit always reads 0; the "Host Busy" bit (offset 21 bit-0) can be used to determine when the IR Host Controller has finished executing the transmission.

5 Receive Start

Writing a 1 to this bit initiates execution of the IR receive mode programmed in the IR configuraton registers. DMA and all necessary registers must be set up prior to writing a 1 to this register. Writing 0 has no effect. This bit always reads 0; the "Host Busy" bit (offset 21 bit-0) can be used to determine when the IR Host Controller has finished executing the reception.

4 Interrupt Clear
- 0 Disable Interript Output ..... default
- 1 Enable Interrupt Output

3-0 Reserved ..... always reads 0

I/O Port Offset 21 – IR Host Status (00h) ..... RO

7 Reserved ..... always reads 0

6 Timer Interrupt Pending
- 0 Timer Interript Not Pending ..... default
- 1 Timer Interrupt Pending

5 Transmit Interrupt Pending
- 0 Transmit Interript Not Pending ..... default
- 1 Transmit Interrupt Pending

4 Receive Interrupt Pending
- 0 Receive Interript Not Pending ..... default
- 1 Receive Interrupt Pending

The following condtions clear this interrupt:
1) Reading the Receive Ring Packet Counter Low register
2) Issuing a Reset Receive Special Condition Interrupt Command
3) Hardware Reset
4) Software Reset

3-1 Interrupt Identification

This code provides an alternative method for identifying the interrupt source by indicating the interrupt type and priority level.

	Priority	Interrupt Type
0xx	n/a	-reserved-
100	Highest	Receive Special Condition - FIFO Overrun, CRC Error, End of Packet (EOF), PHY Error)
101	Second	Receive Data Available
110	Third	Transmit Buffer Empty
111	Fourth	Transmit Special Condition - FIFO Underrun, EOM, Early EOM

0 IR Host Controller Busy
- 0 IR Controller host interface is not processing a transaction ..... default
- 1 IR Controller host interface is in the process of completing any receive or transmit transaction (no other registers should be accessed)

I/O Port Offset 22 – Miscellaneous Control (00h).....RW

7 Transmit DMA Enable
- 0 Disable Transmit DMA Channel .....default
- 1 Enable DREQ1# as transmit DMA channel (if "Dual DMA Channel" is selected)

6 Receive DMA Enable
- 0 Disable Receive DMA Channel.....default (DREQ0# is used also for transmit if the "Single DMA Channel" and "Transmit DMA Channel Enable" bits are both set)
- 1 Enable DREQ0# as receive DMA channel (if a single DMA channel is selected)

5 Swap DMA Channels
- 0 Normal DREQ0/1 .....default
- 1 Swap DREQ0 and DREQ1

4 Physical Layer Internal Loopback
- 0 Disable .....default
- 1 Enable

3 Transmit on Loopback
- 0 Disable .....default
- 1 Enable transmission to LED when internal loopback enabled (bit-4 = 1)

2-0 Reserved ..... always reads 0

I/O Port Offset 23 – Transmit Control 1 (00h) ..... RW

7 Reserved .....always reads 0

6 Transmit FIFO Ready Interrupt
- 0 Disable..... default
- 1 Enable interrupt when FIFO reaches threshold

5 Transmit FIFO Underrun/EOM Interrupt
- 0 Disable..... default
- 1 Enable interrupt on underrun or EOM

4 Transmit FIFO Level
- 0 Threshold set at empty level..... default
- 1 Threshold at half-empty level (less than 8 bytes remaining)

3-0 Reserved .....always reads 0

I/O Port Offset 24 – Transmit Control 2 (00h).....RW

7 Force Underrun
Write 1 to force an underrun on this packet (for testing). For an underrun to occur, the transmit count should be greater than 18 bytes. This bit will be cleared by hardware when the packet has been transmitted.

6 Transmit CRC
0 Disable (for SIR mode or bridging applications where CRC should not be generated by hardware).....def
1 Enable for synchronous packets. This bit will be cleared by hardware when the packet has been transmitted.

5 Bad CRC
Write 1 to send inverted or bad CRC to allow test of CRC verification hardware by the receiver. This bit will be cleared by hardware when the packet has been transmitted.

4 Need Pulse
Write 1 to transmit an indication pulse after this packet has been transmitted. This bit will be cleared by hardware when the packet has been transmitted.

3 Request to Clear "Transmit Enable" Bit
Write 1 to clear the "Enable Transmit" bit (offset 10h bit-5) after this packet has been transmitted. Should be set on the last packet of a transmit seuence.

2-0 Early EOM Interrupt Level
This field specifies the number of bytes that must remain in the Transmit Byte Count before an Early EOM interrupt is generated. The reason for having an interrupt occur before transmission is actually completed is to allow enough time for software to enter the proper interrupt handler routine, turn the DMA channel around for reception (Singe DMA mode), and perpare for another back-to-back transmission. Once in the interrupt handler routine, software can poll the EOM bit in the Transmit Status register to determine exactly when the transmission ends.

000 Interrupt by EOM
001 EOM int occurs when remaining count is 16
010 EOM int occurs when remaining count is 32
011 EOM int occurs when remaining count is 64
100 EOM int occurs when remaining count is 128
101 EOM int occurs when remaining count is 256
110 EOM int occurs when remaining count is 512
111 EOM int occurs when remaining count is 1024

I/O Port Offset 25 – Transmit Status (00h)..... RO

7-4 Reserved .....always reads 0

3 Transmit FIFO Underrun
1 indicates that the Transmit FIFO ran out of data before the transmitter could finish transmitting all the data (i.e., Transmit FIFO empty and a Transmit Byte Count value greater than zero). This bit must be reset by an explicit FIFO Underrun / EOM Latch command.

2 End Of Message (EOM)
1 indicates transmission completed successfully. The EOM interrupt occurs immediately after the CRC and ending flag have been transmitted. This bit is reset by reading the Transmit Status register or by a Reset FIFO Underrun / EOM Latch command from the Reset Command register.

1 Transmit FIFO Ready
1 indicates that the Transmit FIFO is ready for more data transfers. When the "Enable Transmit FIFO Ready Interrupt" bit is set ("Transmit Control Register 1" bit-6), an interrupt is generated when this condition becomes true.

0 Early End Of Message
1 indicates that the Transmit Byte Count has reached the level set by the Early EOM Interrupt Level ("Transmit Control Register 2" bits 2-0). This bit is cleared by reading the Transmit Status register.

I/O Port Offset 26 – Receive Control (00h) .....RW

7 Receive FIFO Level
- 0 Not Empty (more than 1 byte of receive data remaining in the FIFO) .....def
- 1 Half Full (more than 8 bytes of receive data remaining in the FIFO)

6 Reserved ..... always reads 0

5-4 Receive Address Mode

Specifies the type of address filtering to apply for determining which receive packets to accept.
- 00 All packets received; no filtering applied ...def
- 01 Packets with addresses that match the address setting in bits 7-1 of the "Packet Address" register will be received
- 10 Packets with addresses that match the address setting in bits 7-4 of the "Packet Address" register will be received
- 11 Packets with addresses that match the address setting in bits 7-0 of the "Packet Address" register will be received

3-2 Reserved ..... always reads 0

1 Receive FIFO Ready Interrupt
- 0 Disable .....default
- 1 Enable interrupt on receive FIFO ready

0 Receive FIFO Special Condition Interrupt
- 0 Disable .....default
- 1 Enable interrupt on Overrun, CRC error, End of Packet (EOF), PHY error (physical layer detected an encoding error), max length exceeded, or SIR bad

I/O Port Offset 27 – Receive Status (00h)..... RO

7 PHY Error

1 indicates that the physical layer has detected an encoding error. This bit is automatically cleared upon detection of the beginning / start flag of the next incoming packet.

6 CRC Error

1 indicates that a CRC error was detected on an incoming packet. CRC values are checked against known constants for either 16 or 32 bits depending on the length chosen in IR Configuration Register 0 (offset 10h). Valid for MIR and FIR modes only. This bit is automatically cleared upon detection of the beginning / start flag of the next incoming packet.

5 FIFO Overrun Interrupt

1 indicates that the Receive FIFO overflowed. This bit is cleared by a Reset Receive Special Condition Interrupt command from the Reset Command register.

4 EOF (End of Packet)

1 indicates reception of a complete packet. This bit is automatically cleared upon detection of the beginning / start flag of the next incoming packet.

3 Receive Data Available
- 0 Receive FIFO empty
- 1 Receive FIFO not empty (i.e., FIFO contains receive data). Does not cause an interrupt.

2 Reserved .....always reads 0

1 Maximum Receive Packet Length

1 indicates that a maximum length packet was encountered. For SIR, this means that the packet was closed and another will be opened without any data being truncated. In other modes, once the maximum length is reached, no other data will be received. This bit is automatically cleared upon detection of the beginning / start flag of the next incoming packet.

0 SIR Bad

1 indicates (if the SIR filter is on) that a begin flag was seen followed by valid data, then followed by another begin flag (without an end flag). This bit is automatically cleared upon detection of the beginning / start flag of the next incoming packet.

I/O Port Offset 28 – Reset Command (00h).....WO

7-4 Reset Command
Used to send a reset signal to the appropriate hardware in order to clear a particular status condition, clear a counter, or send a general reset. These bits are self clearing (i.e., the programmer does not have to write 0 to the Reset Command register).
0000 No reset.....default
0001 -reserved-
0010 Reset Receive FIFO Pointer
0011 Reset Receive Special Condition Interrupt
0100 Reset Receive Ring Packet Pointer
0101 Reset FIFO Underrun / EOM Latch
0110 Reset Transmit FIFO Pointer
0111 Software Reset
1xxx -reserved-

3-0 Reserved ..... always reads 0

I/O Port Offset 29 – Packet Address (00).....RW

7-0 Receive Packet Address ..... default = 0
Specifies the address value that must be contained in the address field of incoming packets. See also the "Receive Address Mode" setting in Receive Control Register bits 5-4.

I/O Port Offset 2B-2A – Receive Byte Count (0000).....RO

15-13 Reserved ..... always reads 0

12-0 Receive Byte Count..... default = 0
Provides a running count of the number of bytes of data being received. This information is useful for checking if a reception is in progress and may be used to determine packet length.

I/O Port Offset 2D-2C – Receive Ring Packet Ptr (0000)RO

15 Reserved ..... always reads 0

14-0 Receive Byte Count
Used in back-to-back packet reception to provide the end-of-packet pointer value (i.e., pointer to the last byte of a frame received in the receive buffer). The order of byte access to the Ring Packet Pointer is critical for obtaining a valid pointer value. The programmer must ensure that the low byte is read first, followed by the high byte.

I/O Port Offset 2F-2E – Transmit Byte Count (0000) ...RW

15-12 Reserved ..... always reads 0

11-0 Transmit Byte Count
Provides a running count of the number of bytes remaining to be transmitted. Before enabling transmission, software loads this register with the byte length of the data packet. Each time the Transmit FIFO is written to, the value of this counter decrements by one. When the counter reaches zero, the transmitter ceases to make DMA requests. Transmission continues until the Transmit FIFO is depleted.

I/O Port Offset 32 – General Purpose Timer (00) ..... RW

7-0 Timer Target Value (W) / Current Value (R)
This counter increments every 125 usec and stops when it reaches the programmed target value. Reading this register returns the current value of the up counter. Writes set the target value and reset the counter to 0.

I/O Port Offset 33 – IR Configuration 4 (00)..... RW

7 IRRX2 Source
0 IRRX2 source depends on Rx10[6-4] IrDA FIR / SIR / MIR mode selection and Rx1E[1-0] Mode Pin Polarity ..... default
1 IRRX2 source is GPIOB (data is in Rx34[7])

6-2 Reserved .....always reads 0

1 Timer Interrupt Enable
0 Disable..... default
1 Enable

0 Timer Interrupt Pending
0 Not Pending..... default
1 Pending

I/O Port Offset 35-34 – IR Transceiver Control (0000) RW

15 IRRX2 Drive
0 Disable..... default
1 Enable

14-8 Reserved .....always reads 0

7 GPIOB Data for I/O from/to IRRX2 (don't care if Rx33[7] is not set to 1)

6-4 Reserved .....always reads 0

3 IRRX Pin Value..... RO

2-1 Reserved .....always reads 0

0 Force IRTX
0 IRTX pin deasserted..... default
1 IRTX pin asserted

PCI Configuration Space I/O

PCI configuration space accesses for functions 0-6 use PCI configuration mechanism 1 (see PCI specification revision 2.2 for more details). The ports respond only to double-word accesses. Byte or word accesses will be passed on unchanged.

Port CFB-CF8 - Configuration Address.....RW

31 Configuration Space Enable
- 0 Disabled .....default
- 1 Convert configuration data port writes to configuration cycles on the PCI bus

30-24 Reserved ..... always reads 0

23-16 PCI Bus Number
Used to choose a specific PCI bus in the system

15-11 Device Number
Used to choose a specific device in the system

10-8 Function Number
Used to choose a specific function if the selected device supports multiple functions

7-2 Register Number
Used to select a specific DWORD in the device's configuration space

1-0 Fixed ..... always reads 0

Port CFF-CFC - Configuration Data.....RW

There are 7 "functions" implemented in the VT8231:

Function #	Function
0	PCI to ISA Bridge
1	IDE Controller
2	USB Controller Ports 0-1
3	USB Controller Ports 2-3
4	Power Management, SMBus & Hardware Monitor
5	AC97 Audio Codec Controller
6	MC97 Modem Codec Controller

The following sections describe the registers and register bits of these functions.

Device 0 Function 0 Registers - PCI to ISA Bridge

All registers are located in the device 0 function 0 PCI configuration space of the VT8231. These registers are accessed through PCI configuration mechanism #1 via I/O address CF8/CFC.

PCI Configuration Space Header

Offset 1-0 - Vendor ID = 1106h.....RO

Offset 3-2 - Device ID = 8231h .....RO

Offset 5-4 - Command .....RW

- **15-8 Reserved** ..... always reads 0
- **7 Address / Data Stepping**
  - 0 Disable
  - 1 Enable .....default
- **6-4 Reserved** ..... always reads 0
- **3 Special Cycle Enable** ....Normally RW†, default = 0
- **2 Bus Master** ..... always reads 1
- **1 Memory Space** ..... Normally RO†, reads as 1
- **0 I/O Space** ..... Normally RO†, reads as 1

† If the test bit at offset 46 bit-4 is set, access to the above indicated bits is reversed: bit-3 above becomes read only (reading back 1) and bits 0-1 above become read / write (with a default of 1).

Offset 7-6 - Status.....RWC

- **15 Detected Parity Error**.....write one to clear
- **14 Signalled System Error** ..... always reads 0
- **13 Signalled Master Abort**.....write one to clear
- **12 Received Target Abort**.....write one to clear
- **11 Signalled Target Abort**.....write one to clear
- **10-9 DEVSEL# Timing**.....fixed at 01 (medium)
- **8 Data Parity Detected** ..... always reads 0
- **7 Fast Back-to-Back** ..... always reads 0
- **6-0 Reserved** ..... always reads 0

Offset 8 - Revision ID = nn.....RO

- **7-0 Revision ID**

Offset 9 - Program Interface = 00h .....RO

Offset A - Sub Class Code = 01h.....RO

Offset B - Class Code = 06h.....RO

Offset E - Header Type = 80h .....RO

- **7-0 Header Type Code**.....80h (Multifunction Device)

Offset F - BIST = 00h.....RO

Offset 2F-2C - Subsystem ID .....RO

Use offset 70-73 to change the value returned.

Offset 34 - Capability Pointer = C0h.....RO

ISA Bus Control

Offset 40 - ISA Bus Control (00h)..... RW

- **7 Reserved** .....always reads 0
- **6 I/O Recovery Time**
  - 0 Disable..... default
  - 1 Enable
- **5 ROM Wait States**
  - 0 1 Wait State ..... default
  - 1 0 Wait States
- **4 ROM Write**
  - 0 Disable..... default
  - 1 Enable
- **3 Double DMA Clock**
  - 0 Disable..... default
  - 1 Enable
- **2 EISA 4D0 / 4D1h**
  - 0 Disable (ignore ports 4D0 / 4D1h)..... default
  - 1 Enable
- **1 DMA / Interrupt / Timer Shadow Register Read**
  - 0 Disable..... default
  - 1 Enable
- **0 Reserved** .....always reads 0

Offset 41 – BIOS ROM Decode Control (00h)..... RW

Setting these bits enables the indicated address range to be included in the ROMCS# decode:

- **7 Reserved** .....always reads 0
- **6 FFF00000h-FFF7FFFFh** ..... default=0
- **5 FFE80000h-FFEFFFFFh**..... default=0
- **4 FFE00000h-FFE7FFFFh**..... default=0
- **3 FFD80000h-FFDFFFFFh** ..... default=0
- **2 FFD00000h-FFD7FFFFh** ..... default=0
- **1 FFC80000h-FFCFFFFFh** ..... default=0
- **0 FFC00000h-FFC7FFFFh**..... default=0

Note: ROMCS# is always active when ISA addresses FFF80000-FFFFFFFF and 000E0000-000FFFFF are decoded

Offset 42 – Line Buffer Control (00h) ..... RW

7 ISA Master Line Buffer
0 Disable .....default
1 Enable

6 Gate IRQ Until Line Buffer Flush Complete
0 Disable .....default
1 Enable

5 Flush Line Buffer for Interrupt
0 Disable .....default
1 Enable

4 Uninterruptable Burst Read
0 Disable .....default
1 Enable

3-0 Reserved ..... always reads 0

Offset 43 – Delay Transaction Control (00h) ..... RW

7 Reset Counter Test Mode (Do Not Program)
0 Disable .....default
1 Enable

6-5 Test Bit Readback..... RO

4 Delay Transaction Timer Test Mode (Do Not Pr.)
0 Disable .....default
1 Enable

3 Delay Transaction (PCI Spec Rev 2.1)
0 Disable .....default
1 Enable

2 Posted Write Only
0 Disable .....default
1 Enable

1 Write Delay Transaction Timeout Timer
0 Disable .....default
1 Enable

0 Read Delay Transaction Timeout Timer
0 Disable .....default
1 Enable

Offset 44 – ISA PNP DMA Request Control ..... RW

7-6 PnP Routing for FIR2 DRQ.....def = DRQ1
5-4 PnP Routing for FIR1 DRQ.....def = DRQ0
3-2 PnP Routing for Parallel Port DRQ.....def = DRQ3
1-0 PnP Routing for Floppy DRQ.....def = DRQ2
DRQ Mapping: 00=DRQ0, 01=DRQ1, 10=DRQ2, 11=DRQ3

Offset 45 – ISA PNP IRQ Routing 1..... RW

7-4 PnP Routing for Parallel Port IRQ (see PnP IRQ routing table)
3-0 PnP Routing for Floppy IRQ (see PnP IRQ routing table)

Offset 46 – ISA PNP IRQ Routing 2..... RW

7-4 Reserved .....always reads 0
3-0 PnP Routing for COM Port A IRQ (see PnP IRQ routing table)

Offset 47 – ISA PNP IRQ Routing 3..... RW

7-4 Reserved .....always reads 0
3-0 PnP Routing for FIR IRQ (see PnP IRQ routing table)

Table 8 - PnP IRQ Routing Table

0000 Disabled..... default
0001 IRQ1
0010 Reserved
0011 IRQ3
0100 IRQ4
0101 IRQ5
0110 IRQ6
0111 IRQ7
1000 Reserved
1001 IRQ9
1010 IRQ10
1011 IRQ11
1100 IRQ12
1101 Reserved
1110 IRQ14
1111 IRQ15

PCI Master Arbitration Control

Offset 48 – Grant Timeout Select 1 .....RW

- **7-6 Reserved** ..... always reads 0
- **5-4 LAN Grant Timeout Select** (see table below)
- **3-2 USB Grant Timeout Select** (see table below)
- **1-0 IDE Grant Timeout Select** (see table below)

Offset 49 – Grant Timeout Select 2 .....RW

- **7-6 High Priority PCI Master Device 1 Grant Timeout Select** (see table below)
- **5-4 High Priority PCI Master Device 0 Grant Timeout Select** (see table below)
- **3-2 Low Priority PCI Master Device 1 Grant Timeout Select** (see table below)
- **1-0 Low Priority PCI Master Device 0 Grant Timeout Select**
  - 00 Disable Timeout Mechanism .....default
  - 01 16 PCI Clocks
  - 10 32 PCI Clocks
  - 11 96 PCI Clocks

Note: When the master receives the grant, the counter starts to count. When the grant or the master request is deasserted, the counter is reset.

Offset 4A – PCI Master Arbitration Control ..... RW

- **7-4 Reserved** .....always reads 0
- **3 Dummy PCI Request**
  - 0 Disable..... default
  - 1 Enable
- **2 PCI REQ High / Low Priority Exchange**
  - 0 Disable..... default
  - 1 Enable
- **1 PCI REQ USB Priority**
  - 0 Low ..... default
  - 1 High
- **0 PCI REQ IDE Priority**
  - 0 Low ..... default
  - 1 High

Default Groupings

Low Priority: USB -> IDE -> LREQ1# -> USB1 -> ISA/AC97 -> LREQ2#

High Priority: LAN -> USB -> HREQ1# -> IDE -> USB1 -> HREQ2#

Note: Both are rotating arbitration. Only IDE and USB can be programmed as high or low priority masters. USB occupies two positions in the rotating table to get more chances to get a grant.

Miscellaneous Control

Offset 4C - IDE Interrupt Routing.....RW

7-6 I/O Recovery Time
- 00 1 BCLK.....default
- 01 2 BCLKs
- 10 4 BCLKs
- 11 8 BCLKs

5-4 Reserved (do not program)..... default = 0

3-2 IDE Secondary Channel IRQ Routing
- 00 -reserved-
- 01 IRQ15 .....default
- 10 -reserved-
- 11 -reserved-

1-0 IDE Primary Channel IRQ Routing
- 00 IRQ14 .....default
- 01 -reserved-
- 10 -reserved-
- 11 -reserved-

Offset 4D – External APIC IRQ Output Control .....RW

7-6 Reserved ..... always reads 0

5 LAN IRQ to APIC[23:16] with LAN device F0/Rx3C[2:0]
- 0 Disable .....default
- 1 Enable

4 ACPI IRQ to APIC[23:16] with F6/Rx42[2:0]
- 0 Disable .....default
- 1 Enable

3 MC97 IRQ to APIC[23:16] with F6/Rx3C[2:0]
- 0 Disable .....default
- 1 Enable

2 AC97 IRQ to APIC[23:16] with F5/Rx3C[2:0]
- 0 Disable .....default
- 1 Enable

1 USB Port 1 IRQ to APIC[23:16] with F2/Rx3C[2:0]
- 0 Disable .....default
- 1 Enable

0 USB Port 0 IRQ to APIC[23:16] with F3/Rx3C[2:0]
- 0 Disable .....default
- 1 Enable

Offset 4E - Internal RTC Test Mode..... RW

7-4 Reserved .....always reads 0

3 Extra RTC Port 74/75 Enable
- 0 Disable..... default
- 1 Enable

2 RTC Reset Enable (do not program)
- 0 Disable..... default
- 1 Enable

1 RTC SRAM Access Enable
- 0 Disable..... default
- 1 Enable

Set if internal RTC is disabled but SRAM access is desired via ports 74-75 (bit-3 must also be set). If the internal RTC is enabled, setting this bit does nothing (internal RTC SRAM may be accessed at either ports 70/71).

0 RTC Test Mode Enable (do not program). default=0

Offset 4F – PCI Bus and CPU Interface Control ..... RW

7-4 Reserved .....always reads 0

3 CPU Reset Source
- 0 Use CPURST as CPU Reset..... default
- 1 Use INIT# as CPU Reset

2 Config Command Reg Rx04 Access (Test Only)
- 0 Normal: Bits 0-1=RO, Bit 3=RW..... default
- 1 Test Mode: Bits 0-1=RW, Bit-3=RO

1 IRDY# Wait States
- 0 0 Wait States..... default
- 1 1 Wait State

0 Software PCI Reset.....write 1 to generate PCI reset

Function Control

Offset 50 – Function Control 1 (09h) ..... RW

7 Function 6 MC97
- 0 Enable .....default
- 1 Disable

6 Function 5 AC97
- 0 Enable .....default
- 1 Disable

5 Function 3 USB
- 0 Enable .....default
- 1 Disable

4 Function 2 USB
- 0 Enable .....default
- 1 Disable

3 IDE
- 0 Enable
- 1 Disable .....default

2 Super-IO Configuration (Ports 3F0 / 3F1 offsets F0-FF)
- 0 Disable .....default
- 1 Enable

1 Super-IO
- 0 Disable .....default
- 1 Enable

0 Internal Audio..... RO
- 0 Disable
- 1 Enable .....default

Offset 51 – Function Control 2 ..... RW

7-6 Reserved ..... always reads 0

5 LAN Clock Gating
- 0 Disable .....default
- 1 Enable

4 Internal LAN
- 0 Disable .....default
- 1 Enable

3 Internal RTC
- 0 Disable
- 1 Enable .....default

2 Internal PS2 Mouse
- 0 Disable .....default
- 1 Enable

1 Internal KBC Configuration (Ports 3F0 / 3F1 offsets E0-EF)
- 0 Disable .....default
- 1 Enable

0 Internal KBC
- 0 Disable .....default
- 1 Enable

Serial IRQ and PC/PCI DMA Control

Offset 52 – Serial IRQ Control..... RW

7-4 Reserved .....always reads 0

3 ISA IRQ Asserted Via Serial IRQ (Pin V9)
- 0 Disable..... default
- 1 Enable

2 Serial IRQ Mode
- 0 Continuous Mode ..... default
- 1 Quiet Mode

1-0 Serial IRQ Start-Frame Width
- 00 4 PCI Clocks..... default
- 01 6 PCI Clocks
- 10 8 PCI Clocks
- 11 10 PCI Clocks

The frame size is fixed at 21 PCI clocks.

Offset 53 – Reserved (Do Not Program)..... RW

7-0 Reserved (Do Not Program)..... default = 0

Plug and Play Control - PCI

Offset 54 - PCI Interrupt Polarity.....RW

7-4 Reserved ..... always reads 0

The following bits all default to "level" triggered (0)

3 PINTA# Invert (edge) / Non-invert (level).....(1/0)
2 PINTB# Invert (edge) / Non-invert (level).....(1/0)
1 PINTC# Invert (edge) / Non-invert (level).....(1/0)
0 PINTD# Invert (edge) / Non-invert (level).....(1/0)

Note: PINTA-D# normally connect to PCI interrupt pins INTA-D# (see pin definitions for more information).

Offset 55 – PCI PNP Interrupt Routing 1 .....RW

7-4 PINTA# Routing (see PnP IRQ routing table)
3-0 Reserved ..... always reads 0

Offset 56 – PCI PNP Interrupt Routing 2 .....RW

7-4 PINTC# Routing (see PnP IRQ routing table)
3-0 PINTB# Routing (see PnP IRQ routing table)

Offset 57 – PCI PNP Interrupt Routing 3 .....RW

7-4 PINTD# Routing (see PnP IRQ routing table)
3-0 Reserved ..... always reads 0

Table 9 - PnP IRQ Routing Table

0000 Disabled..... default
0001 IRQ1
0010 Reserved
0011 IRQ3
0100 IRQ4
0101 IRQ5
0110 IRQ6
0111 IRQ7
1000 Reserved
1001 IRQ9
1010 IRQ10
1011 IRQ11
1100 IRQ12
1101 Reserved
1110 IRQ14
1111 IRQ15

Miscellaneous Control

Offset 58 – Miscellaneous Control 0 (40h).....RW

7 Reserved (Do Not Program) ..... default = 0

6 Internal APIC
- 0 Disable
- 1 Enable **.....default**

5 LPC DRQ Input
- 0 Disable (Pin Y8 = GPI15).....default
- 1 Enable (Pin Y8 = LDRQ#)

4 Address Decode
- 0 Subtractive .....default
- 1 Positive

3 RTC High Bank Access
- 0 Disable .....default
- 1 Enable

2 RTC Rx32 Write Protect
- 0 Disable .....default
- 1 Enable

1 RTC Rx0D Write Protect
- 0 Disable .....default
- 1 Enable

0 RTC Rx32 Map to Century Byte
- 0 Disable .....default
- 1 Enable

Offset 59 – Miscellaneous Control 1 (00h) ..... RW

7 PCS3# as LPC Device
- 0 Disable..... default
- 1 Enable

6 PCS2# as LPC Device
- 0 Disable..... default
- 1 Enable

5 Reserved .....always reads 0

4 LPC Keyboard
- 0 Disable..... default
- 1 Enable

3 MCCS# to LPC
- 0 Disable..... default
- 1 Enable

2 MCCS#
- 0 Disable..... default
- 1 Enable

1 A20M Active
- 0 Disable..... default
- 1 Enable

0 Super-I/O Recovery Time
- 0 Disable..... default
- 1 Enable

Programmable Chip Select Control

Offset 5D-5C – PCS0# I/O Port Address ..... RW

15-0 PCS0# I/O Port Address Bits 15-0

Offset 5F-5E – PCS1# I/O Port Address ..... RW

15-0 PCS1# I/O Port Address Bits 15-0

Offset 61-60 – PCS2# I/O Port Address ..... RW

15-0 PCS2# I/O Port Address Bits 15-0

Offset 63-62 – PCS3# I/O Port Address ..... RW

15-0 PCS3# I/O Port Address Bits 15-0

Offset 65-64 – PCSn# I/O Port Address Mask ..... RW

15-12 PCS3# I/O Port Address Bits 3-0
11-8 PCS2# I/O Port Address Bits 3-0
7-4 PCS1# I/O Port Address Bits 3-0
3-0 PCS0# I/O Port Address Bits 3-0

Offset 66 – PCSn# Control (00h) ..... RW

7 PCS3# for Internal I/O
0 Disable ..... default
1 Enable

6 PCS2# for Internal I/O
0 Disable ..... default
1 Enable

5 PCS1# for Internal I/O
0 Disable ..... default
1 Enable

4 PCS0# for Internal I/O
0 Disable ..... default
1 Enable

3 PCS3#
0 Disable ..... default
1 Enable

2 PCS2#
0 Disable ..... default
1 Enable

1 PCS1#
0 Disable ..... default
1 Enable

0 PCS0#
0 Disable ..... default
1 Enable

Fast IR Control

Offset 67 – Fast IR / IOCHRDY / FERR# Config (08h) RW

7-4 Reserved ..... always reads 0

3 IOCHRDY Function
0 Pin W10 = LREQ2# / GPI13 (see F4 RxE5[2])
1 Pin W10 = ISA Bus IOCHRDY ..... default

2 CPU FERR# Threshold
0 2.5V ..... default
1 1.5V

1 FIR Single DMA Channel
0 Disable ..... default
1 Enable

0 FIR
0 Disable ..... default
1 Enable

Offset 6B-6A – Fast IR I/O Base (0001h) ..... RW

15-7 FIR I/O Base ..... default = 0
6-0 Reserved ..... always reads 01h

ISA Decoding Control

Offset 6C – ISA Positive Decoding Control 1 ..... RW

7 On-Board I/O Port Positive Decoding
- 0 Disable ..... default
- 1 Enable

6 Microsoft-Sound System I/O Port Positive Decoding
- 0 Disable ..... default
- 1 Enable

5-4 Microsoft-Sound System I/O Decode Range
- 00 0530h-0537h ..... default
- 01 0604h-060Bh
- 10 0E80-0E87h
- 11 0F40h-0F47h

3 APIC Positive Decoding
- 0 Disable ..... default
- 1 Enable

2 BIOS ROM Positive Decoding
- 0 Disable ..... default
- 1 Enable

1 PCS1# Positive Decoding
- 0 Disable ..... default
- 1 Enable

0 PCS0# Positive Decoding
- 0 Disable ..... default
- 1 Enable

Offset 6D – ISA Positive Decoding Control 2 ..... RW

7 FDC Positive Decoding
- 0 Disable ..... default
- 1 Enable

6 LPT Positive Decoding
- 0 Disable ..... default
- 1 Enable

5-4 LPT Decode Range
- 00 3BCh-3BFh, 7BCh-7BEh ..... default
- 01 378h-37Fh, 778h-77Ah
- 10 278h-27Fh, 678h-67Ah
- 11 -reserved-

3 Game Port Positive Decoding
- 0 Disable ..... default
- 1 Enable

2 MIDI Positive Decoding
- 0 Disable ..... default
- 1 Enable

1-0 MIDI Decode Range
- 00 300h-303h ..... default
- 01 310h-313h
- 10 320h-323h
- 11 330h-333h

Offset 6E – ISA Positive Decoding Control 3 ..... RW

7 COM Port B Positive Decoding
- 0 Disable ..... default
- 1 Enable

6-4 COM-Port B Decode Range
- 000 3F8h-3FFh (COM1) ..... default
- 001 2F8h-2FFh (COM2)
- 010 220h-227h
- 011 228h-22Fh
- 100 238h-23Fh
- 101 2E8h-2EFh (COM4)
- 110 338h-33Fh
- 111 3E8h-3EFh (COM3)

3 COM Port A Positive Decoding
- 0 Disable ..... default
- 1 Enable

2-0 COM-Port A Decode Range
- 000 3F8h-3FFh (COM1) ..... default
- 001 2F8h-2FFh (COM2)
- 010 220h-227h
- 011 228h-22Fh
- 100 238h-23Fh
- 101 2E8h-2EFh (COM4)
- 110 338h-33Fh
- 111 3E8h-3EFh (COM3)

Offset 6F – ISA Positive Decoding Control 4 ..... RW

7-5 Reserved ..... always reads 0

4 FIR Positive Decoding
- 0 Disable ..... default
- 1 Enable

3 FDC Decoding Range
- 0 Primary ..... default
- 1 Secondary

2 Sound Blaster Positive Decoding
- 0 Disable ..... default
- 1 Enable

1-0 Sound Blaster Decode Range
- 00 220h-22Fh, 230h-233h ..... default
- 01 240h-24Fh, 250h-253h
- 10 260h-26Fh, 270h-273h
- 11 280h-28Fh, 290h-293h

Subsystem ID

Offset 73-70 - Subsystem ID.....WO

31-0 Subsystem ID / Vendor ID ..... always reads 0
Contents may be read at offset 2C.

Test

Offset 79-78 – PNP IRQ/DRQ Test (Do Not Program) . RW

15 PNP Test Mode (Do Not Program)
0 Disable .....default
1 Enable
14 Reserved ..... always reads 0
5-0 Test Bits 13-0 for PNP Input

Offset 7A – IDE/USB Test (Do Not Program) (00h)..... RW

7 UDMA66 Test Mode (Do Not Program)
0 Disable .....default
1 Enable
6 USB Port Test Mode (Do Not Program)
0 Disable .....default
1 Enable
5-4 USB Port Test Select
3 USB Port Test Output Source
2 MIDI Test Mode (Do Not Program)
0 Disable .....default
1 Enable
1-0 Reserved ..... always reads 0

Offset 7B – PLL Test ..... RW

7-5 Reserved ..... always reads 0
4 PLL PU (Do Not Program)
0 Disable .....default
1 Enable
3 PLL Test Mode (Do Not Program)
0 Disable .....default
1 Enable
2-0 PLL Test Mode Select

I/O Pad Control

Offset 7C – I/O Pad Control (00h)..... RW

7-6 Reserved .....always reads 0
5-4 IDE Pad Drive Select
3-2 PLL PCLK Input Delay Select
1-0 PLL CLK66 Feedback Delay Select

Device 0 Function 1 Registers - Enhanced IDE Controller

This Enhanced IDE controller interface is fully compatible with the SFF 8038i v.1.0 specification. There are two sets of software accessible registers -- PCI configuration registers and Bus Master IDE I/O registers. The PCI configuration registers are located in the function 1 PCI configuration space of the VT8231. The Bus Master IDE I/O registers are defined in the SFF8038i v1.0 specification.

PCI Configuration Space Header

Offset 1-0 - Vendor ID (1106h=VIA).....RO

Offset 3-2 - Device ID (0571h=IDE Controller) .....RO

Offset 5-4 – Command (0080h).....RW

15-10 Reserved ..... always reads 0
9 Fast Back to Back Cycles ..... default = 0 (disabled)
8 SERR# Enable ..... default = 0 (disabled)
7 Address Stepping .....**default = 1 (enabled)**
A value of 1 provides additional address decode time to IDE devices.
6 Parity Error Response..... default = 0 (disabled)
5 VGA Palette Snoop.....fixed at 0 (disabled)
4 Memory Write & Invalidate.....fixed at 0 (disabled)
3 Special Cycles.....fixed at 0 (disabled)
2 Bus Master ..... default = 0 (disabled)
S/G operation can be issued only when the "Bus Master" bit is enabled.
1 Memory Space ..... default = 0 (disabled)
0 I/O Space ..... default = 0 (disabled)
When the "I/O Space" bit is disabled, the device will not respond to any I/O addresses for both compatible and native mode.

Offset 7-6 – Status (0290h).....RO

15 Detected Parity Error.....fixed at 0
14 Signalled System Error .....fixed at 0
13 Received Master Abort .....fixed at 0
12 Received Target Abort .....fixed at 0
11 Signalled Target Abort.....fixed at 0
10-9 DEVSEL# Timing.....**default = 01 (medium)**
8 Data Parity Detected .....fixed at 0
7 Fast Back to Back .....**fixed at 1**
6-5 Reserved ..... always reads 0
4 Reserved .....**always reads 1**
3-0 Reserved ..... always reads 0

Offset 8 - Revision ID (06).....RO

7-0 Revision Code for IDE Controller Logic Block

Offset 9 - Programming Interface..... RW

7 Master IDE Capability ..... fixed at 1 (Supported)
6-4 Reserved .....always reads 0
3 Programmable Indicator - Secondary..... fixed at 1
Supports both modes (may be set to either mode by writing bit-2)
2 Secondary Channel Mode
0 Compatibility Mode ..... default
1 Native Mode
1 Programmable Indicator - Primary ..... fixed at 1
Supports both modes (may be set to either mode by writing bit-0)
0 Primary Channel Mode
0 Compatibility Mode ..... default
1 Native Mode

Compatibility Mode (fixed IRQs and I/O addresses):

Channel	Command Block Registers	Control Block Registers	IRQ
Pri	1F0-1F7	3F6	14
Sec	170-177	376	15

Native PCI Mode (registers are programmable in I/O space)

Channel	Command Block Registers	Control Block Registers
Pri	BA @offset 10h	BA @offset 14h
Sec	BA @offset 18h	BA @offset 1Ch

Command register blocks are 8 bytes of I/O space
Control registers are 4 bytes of I/O space (only byte 2 is used)

Offset A - Sub Class Code (01h=IDE Controller) ..... RO

Offset B - Base Class Code (01h=Mass Storage Ctrlr)... RO

Offset C – Cache Line Size (00h) ..... RO

Offset D - Latency Timer (Default=0) ..... RW

Offset E - Header Type (00h) ..... RO

Offset F - BIST (00h)..... RO

Offset 13-10 - Pri Data / Command Base Address.....RW

Specifies an 8 byte I/O address space.

31-16 Reserved .....always read 0
15-3 Port Address..... default=01F0h
2-0 Fixed at 001b if native mode enabled.....fixed
2-0 Fixed at 000b if compatibility mode enabled ..fixed

Offset 17-14 - Pri Control / Status Base Address .....RW

Specifies a 4 byte I/O address space of which only the third byte is active (i.e., 3F6h for the default base address of 3F4h).

31-16 Reserved .....always read 0
15-2 Port Address..... default=03F4h
1-0 Fixed at 01b if native mode enabled.....fixed
1-0 Fixed at 00b if compatibility mode enabled ....fixed

Offset 1B-18 - Sec Data / Command Base Address.....RW

Specifies an 8 byte I/O address space.

31-16 Reserved .....always read 0
15-3 Port Address ..... default=0170h
2-0 Fixed at 001b if native mode enabled.....fixed
2-0 Fixed at 000b if compatibility mode enabled ..fixed

Offset 1F-1C - Sec Control / Status Base Address .....RW

Specifies a 4 byte I/O address space of which only the third byte is active (i.e., 376h for the default base address of 374h).

31-16 Reserved .....always read 0
15-2 Port Address ..... default=0374h
1-0 Fixed at 01b if native mode enabled.....fixed
1-0 Fixed at 00b if compatibility mode enabled ....fixed

Offset 23-20 - Bus Master Control Regs Base Address .RW

Specifies a 16 byte I/O address space compliant with the **SFF-8038i rev 1.0** specification.

31-16 Reserved .....always read 0
15-4 Port Address ..... default=CC0h
3-0 Fixed at 0001b if native mode enabled.....fixed
3-0 Fixed at 0000b if compatibility mode enabled fixed

Offset 34 - Capability Pointer (C0h)..... RO

Offset 3C - Interrupt Line (0Eh)..... RO

Offset 3D - Interrupt Pin (00h) ..... RO

7-0 Interrupt Routing Mode
00h Legacy mode interrupt routing ..... default
01h Native mode interrupt routing

Offset 3E - Min Gnt (00h)..... RO

Offset 3F - Max Latency (00h) ..... RO

IDE-Controller-Specific Confiiguration Registers

Offset 40 - Chip Enable (08h) .....RW

7-4 Reserved ..... always reads 0
3-2 Reserved (Do Not Program) .....R/W, **default = 10b**
1 Primary Channel Enable ..... default = 0 (disabled)
0 Secondary Channel Enable.... default = 0 (disabled)

Offset 41 - IDE Configuration 1 (06h) .....RW

7 Primary IDE Read Prefetch Buffer
0 Disable .....default
1 Enable
6 Primary IDE Post Write Buffer
0 Disable .....default
1 Enable
5 Secondary IDE Read Prefetch Buffer
0 Disable .....default
1 Enable
4 Secondary IDE Post Write Buffer
0 Disable .....default
1 Enable
3 SERR# Response
0 Disable .....default
1 Enable
2 Reserved (Do Not Change)..... default=1
1 Reserved (Do Not Change)..... default=1
0 PERR# Response
0 Disable .....default
1 Enable

Offset 42 - IDE Configuration 2 (C0h).....RW

7 Primary PIO Operating Mode Select
0 Compatibility Mode (Fixed Addressing)
1 Native Mode (Flexible Addressing).....default
6 Secondary PIO Operating Mode Select
0 Compatibility Mode (Fixed Addressing)
1 Native Mode (Flexible Addressing).....default
5-0 Reserved (Do Not Program) ..... default = 0

Offset 43 - FIFO Configuration (0Ah)..... RW

7-4 Reserved .....always reads 0
3-2 Threshold for Primary Channel
00 1/4
01 1/2
10 3/4 ..... default
11 1
1-0 Threshold for Secondary Channel
00 1/4
01 1/2
10 3/4 ..... default
11 1

Offset 44 - Miscellaneous Control 1 (68h)..... RW

7 Reserved ..... always reads 0

6 Master Read Cycle IRDY# Wait States
- 0 0 wait states
- 1 1 wait state .....default

5 Master Write Cycle IRDY# Wait States
- 0 0 wait states
- 1 1 wait state .....default

4 PIO Read Prefetch Byte Counter
- 0 Disable .....default
- 1 Enable

3 Bus Master IDE Status Register Read Retry

Retry bus master IDE status register read when master write operation for DMA read is not complete
- 0 Disabled
- 1 Enabled .....default

2 Packet Command Prefetching
- 0 Disable .....default
- 1 Enable

1 Reserved ..... always reads 0

0 UltraDMA Host Must Wait for First Strobe Before Termination
- 0 Enabled .....default
- 1 Disabled

Offset 45 - Miscellaneous Control 2 (00h) ..... RW

7 Reserved .....always reads 0

6 Interrupt Steering Swap
- 0 Don't swap channel interrupts..... default
- 1 Swap interrupts between the two channels

5-4 Reserved .....always reads 0

3 Memory Read Multiple Command
- 0 Disable..... default
- 1 Enable

2 Memory Write and Invalidate Command
- 0 Disable..... default
- 1 Enable

1-0 Reserved .....always reads 0

Offset 46 - Miscellaneous Control 3 (C0h) ..... RW

7 Primary Channel Read DMA FIFO Flush

1 = Enable FIFO flush for read DMA when interrupt asserts primary channel. .....default=1 (enabled)

6 Secondary Channel Read DMA FIFO Flush

1 = Enable FIFO flush for Read DMA when interrupt asserts secondary channel. .....Default=1 (enabled)

5-0 Reserved .....always reads 0

Offset 4B-48 - Drive Timing Control .....RW

The following fields define the Active Pulse Width and Recovery Time for the IDE DIOR# and DIOW# signals:

31-28 Primary Drive 0 Active Pulse Width ..... def=1010b
27-24 Primary Drive 0 Recovery Time ..... def=1000b
23-20 Primary Drive 1 Active Pulse Width ..... def=1010b
19-16 Primary Drive 1 Recovery Time ..... def=1000b
15-12 Secondary Drive 0 Active Pulse Width .. def=1010b
11-8 Secondary Drive 0 Recovery Time ..... def=1000b
7-4 Secondary Drive 1 Active Pulse Width .. def=1010b
3-0 Secondary Drive 1 Recovery Time ..... def=1000b

The actual value for each field is the encoded value in the field plus one and indicates the number of PCI clocks.

Offset 4C - Address Setup Time .....RW

7-6 Primary Drive 0 Address Setup Time
5-4 Primary Drive 1 Address Setup Time
3-2 Secondary Drive 0 Address Setup Time
1-0 Secondary Drive 1 Address Setup Time

For each field above:
00 1T
01 2T
10 3T
11 4T .....default

Offset 53-50 - UltraDMA Extended Timing Control .... RW

31 Pri Drive 0 UltraDMA-Mode Enable Method
0 Enable by using "Set Feature" command.... def
1 Enable by setting bit-30 of this register
30 Pri Drive 0 UltraDMA-Mode Enable
0 Disable..... default
1 Enable UltraDMA-Mode Operation
29 Pri Drive 0 Transfer Mode
0 DMA or PIO Mode ..... default
1 UltraDMA Mode
28 Pri Drive 0 Cable Type Reporting
0 40-pin ..... default
1 80-pin
27 Reserved .....always reads 0
26-24 Pri Drive 0 Cycle Time (T = 10 nsec)
000 2T
001 3T
010 4T
011 5T
100 6T
101 7T
110 8T
111 9T ..... default

23 Pri Drive 1 UltraDMA-Mode Enable Method
22 Pri Drive 1 UltraDMA-Mode Enable
21 Pri Drive 1 Transfer Mode
20 Pri Drive 1 Cable Type Reporting
0 40-pin ..... default
1 80-pin
19 Reserved .....always reads 0
18-16 Pri Drive 1 Cycle Time

15 Sec Drive 0 UltraDMA-Mode Enable Method
14 Sec Drive 0 UltraDMA-Mode Enable
13 Sec Drive 0 Transfer Mode
12 Sec Drive 0 Cable Type Reporting
0 40-pin ..... default
1 80-pin
11 Reserved .....always reads 0
10-8 Sec Drive 0 Cycle Time

7 Sec Drive 1 UltraDMA-Mode Enable Method
6 Sec Drive 1 UltraDMA-Mode Enable
5 Sec Drive 1 Transfer Mode
4 Sec Drive 1 Cable Type Reporting
0 40-pin ..... default
1 80-pin
3 Reserved .....always reads 0
2-0 Sec Drive 1 Cycle Time

Each byte defines UltraDMA operation for the indicated drive. The bit definitions are the same within each byte.

Offset 54 – UltraDMA FIFO Control.....RW

7-5 Reserved ..... always reads 0

4 One Frame For Each PCI Request For IDE PCI Master Cycles

0 Disabled .....default

1 Enabled

3 Reserved ..... always reads 0

2 Change Drive to Clear All FIFO & Internal States

0 Disabled

1 Enabled .....default

1 Reserved ..... always reads 0

0 Complete DMA Cycle with Transfer Size Less Than FIFO Size

0 Enabled .....default

1 Disabled

Offset 61-60 - Primary Sector Size .....RW

15-12 Reserved ..... always reads 0

11-0 Number of Bytes Per Sector .. def=200h (512 bytes)

Offset 69-68 - Secondary Sector Size.....RW

15-12 Reserved ..... always reads 0

11-0 Number of Bytes Per Sector .. def=200h (512 bytes)

Offset 70 – Primary IDE Status ..... RW

7 Interrupt Status

6 Prefetch Buffer Status

5 Post Write Buffer Status

4 DMA Read Prefetch Status

3 DMA Write Prefetch Status

2 S/G Operation Complete

1-0 Reserved .....always reads 0

Offset 71 – Primary Interrupt Control..... RW

7-1 Reserved .....always reads 0

0 Flush FIFO Before Generating IDE Interrupt

0 Disable..... default

1 Enable

Offset 78 – Secondary IDE Status..... RW

7 Interrupt Status

6 Prefetch Buffer Status

5 Post Write Buffer Status

4 DMA Read Prefetch Status

3 DMA Write Prefetch Status

2 S/G Operation Complete

1-0 Reserved .....always reads 0

Offset 79 - Secondary Interrupt Control..... RW

7-1 Reserved .....always reads 0

0 Flush FIFO Before Generating IDE Interrupt

0 Disable..... default

1 Enable

Offset 83-80 – Primary S/G Descriptor Address.....RW

Offset 8B-88 – Secondary S/G Descriptor Address.....RW

Offset C3-C0 – PCI PM Block 1 (0002 0001h).....RO

31-0 PCI PM Block 1 ..... always reads 0002 0001h

Offset C7-C4 – PCI PM Block 2 (0000 0000h).....RO

31-2 Reserved ..... always reads 0

1-0 Power State

00 On .....default
01 Off
1x -reserved-

IDE I/O Registers

These registers are compliant with the SFF 8038I v1.0 standard. Refer to the SFF 8038I v1.0 specification for further details.

I/O Offset 0 - Primary Channel Command

I/O Offset 2 - Primary Channel Status

I/O Offset 4-7 - Primary Channel PRD Table Address

I/O Offset 8 - Secondary Channel Command

I/O Offset A - Secondary Channel Status

I/O Offset C-F - Secondary Channel PRD Table Address

Device 0 Function 2 Registers - USB Controller Ports 0-1

This Universal Serial Bus host controller interface is fully compatible with UHCI specification v1.1. There are two sets of software accessible registers: PCI configuration registers and USB I/O registers. The PCI configuration registers are located in the function 2 PCI configuration space of the VT8231. The USB I/O registers are defined in UHCI specification v1.1. The registers in this function control USB ports 0-1 (see function 3 for ports 2-3).

PCI Configuration Space Header

Offset 1-0 - Vendor ID ..... RO

7-0 Vendor ID ..... (1106h = VIA Technologies)

Offset 3-2 - Device ID ..... RO

7-0 Device ID (3038h = VT8231 USB Controller)

Offset 5-4 - Command ..... RW

15-8 Reserved ..... always reads 0
7 Address Stepping ..... default=0 (disabled)
6 Reserved (parity error response) ..... fixed at 0
5 Reserved (VGA palette snoop) ..... fixed at 0
4 Memory Write and Invalidate. default=0 (disabled)
3 Reserved (special cycle monitoring) ..... fixed at 0
2 Bus Master ..... default=0 (disabled)
1 Memory Space ..... default=0 (disabled)
0 I/O Space ..... default=0 (disabled)

Offset 7-6 - Status ..... RWC

15 Reserved (detected parity error) ..... always reads 0
14 Signalled System Error ..... default=0
13 Received Master Abort ..... default=0
12 Received Target Abort ..... default=0
11 Signalled Target Abort ..... default=0
10-9 DEVSEL# Timing
00 Fast
01 Medium ..... default (fixed)
10 Slow
11 Reserved
8-0 Reserved ..... always reads 0

Offset 8 - Revision ID (nnh) ..... RO

7-0 Silicon Revision Code (0 indicates first silicon)
06h Corresponds to Chip Revision D

Offset 9 - Programming Interface (00h) ..... RO

Offset A - Sub Class Code (03h=USB Controller) ..... RO

Offset B - Base Class Code (0Ch=Serial Bus Controller) RO

Offset C – Cache Line Size (00h) ..... RO

Offset D - Latency Timer ..... RW

7-0 Timer Value ..... default = 16h

Offset E - Header Type (00h) ..... RO

Offset F - BIST (00h) ..... RO

Offset 23-20 - USB I/O Register Base Address ..... RW

31-16 Reserved ..... always reads 0
15-5 USB I/O Register Base Address. Port Address for the base of the 32-byte USB I/O Register block, corresponding to AD[15:5]
4-0 00001b

Offset 3C - Interrupt Line (00h) ..... RW

7-4 Reserved ..... always reads 0
3-0 USB Interrupt Routing ..... default = 16h
0000 Disabled ..... default
0001 IRQ1
0010 Reserved
0011 IRQ3
0100 IRQ4
0101 IRQ5
0110 IRQ6
0111 IRQ7
1000 IRQ8
1001 IRQ9
1010 IRQ10
1011 IRQ11
1100 IRQ12
1101 IRQ13
1110 IRQ14
1111 Disabled

Offset 3D - Interrupt Pin (04h) ..... RO

USB-Specific Configuration Registers

Offset 40 - Miscellaneous Control 1 ..... RW

7 PCI Memory Command Option
- 0 Support Memory-Read-Line, Memory-Read-Multiple, & Memory-Write-&-Invalidate....def
- 1 Only support Mem Read, Mem Write Cmds

6 Babble Option
- 0 Automatically disable babbled port when EOF babble occurs .....default
- 1 Don't disable babbled port

5 PCI Parity Check Option
- 0 Disable PERR# generation .....default
- 1 Enable parity check and PERR# generation

4 Frame Interval Select
- 0 1 ms frame .....default
- 1 0.1 ms frame

3 USB Data Length Option
- 0 Support TD length up to 1280 .....default
- 1 Support TD length up to 1023

2 USB Power Management
- 0 Disable USB power management .....default
- 1 Enable USB power management

1 DMA Option
- 0 8 DW burst access with better FIFO latencydef
- 1 16 DW burst access (original performance)

0 PCI Wait States
- 0 Zero wait.....default
- 1 One wait

Offset 41 - Miscellaneous Control 2..... RW

7 USB 1.1 Improvement for EOP
- 0 USB Specification 1.1 Compliant ..... default
  If a bit stuffing error occurs before EOP, the receiver will accept the packet
- 1 USB Specification 1.0 Compliant
  If a bit stuffing error occurs before EOP, the receiver will ignore the packet

6-5 Reserved (Do Not Program)..... default = 0

4 Hold PCI Request for Successive Accesses
- 0 Disable
- 1 Enable..... default

Setting this bit to "enable" causes the system to treat the USB request as higher priority

3 Frame Counter Test Mode
- 0 Disable..... default
- 1 Enable

2 Trap Option
- 0 Set trap 60/64 status bits only when trap 60/64 enable bits are set. ..... default
- 1 Set trap 60/64 status bits without checking enable bits

1 A20gate Pass Through Option
- 0 Pass through A20GATE command sequence defined in UHCI..... default
- 1 Don't pass through Write I/O port 64 (ff)

0 USB IRQ Test Mode
- 0 Normal Operation..... default
- 1 Generate USB IRQ

Offset 42 - FIFO Control.....RW

7-4 Reserved ..... always reads 0
3-2 Reserved (Do Not Program) ..... default = 0
1-0 Release Continuous REQ After "N" PCICLKs
00 Do Not Release .....default
01 N = 32 PCICLKs
10 N = 64 PCICLKs
11 N = 96 PCICLKs

Offset 48 - CRC Control.....RW

7-2 Reserved ..... always reads 0
1 Lengthen PRESOF Time
0 Disable .....default
1 Enable
0 Issue Zero Bad CRC Code on FIFO Under-run
0 Issue Non-Zero CRC .....default
1 Issue All Zero CRC

Offset 60 - Serial Bus Release Number .....RO

7-0 Release Number ..... always reads 10h

Offset 83-80 – PM Capability .....RO

31-0 PM Capability..... always reads 00020001h

Offset 84 – PM Capability Status .....RW

7-0 PM Capability Status ..... default = 00h
Supports 00h (Off) and 11h (On) only

Offset C1-C0 - Legacy Support .....RO

15-0 UHCI v1.1 Compliant ..... always reads 2000h

USB I/O Registers

These registers are compliant with the UHCI v1.1 standard. Refer to the UHCI v1.1 specification for further details.

I/O Offset 1-0 - USB Command

I/O Offset 3-2 - USB Status

I/O Offset 5-4 - USB Interrupt Enable

I/O Offset 7-6 - Frame Number

I/O Offset B-8 - Frame List Base Address

I/O Offset 0C - Start Of Frame Modify

I/O Offset 11-10 - Port 0 Status / Control

I/O Offset 13-12 - Port 1 Status / Control

Device 0 Function 3 Registers - USB Controller Ports 2-3

This Universal Serial Bus host controller interface is fully compatible with UHCI specification v1.1. There are two sets of software accessible registers: PCI configuration registers and USB I/O registers. The PCI configuration registers are located in the function 3 PCI configuration space of the VT8231. The USB I/O registers are defined in UHCI specification v1.1. The registers in this function control USB ports 2-3 (see function 2 for ports 0-1).

PCI Configuration Space Header

Offset 1-0 - Vendor ID ..... RO

7-0 Vendor ID ..... (1106h = VIA Technologies)

Offset 3-2 - Device ID ..... RO

7-0 Device ID (3038h = VT8231 USB Controller)

Offset 5-4 - Command ..... RW

15-8 Reserved ..... always reads 0
7 Address Stepping ..... default=0 (disabled)
6 Reserved (parity error response) ..... fixed at 0
5 Reserved (VGA palette snoop) ..... fixed at 0
4 Memory Write and Invalidate. default=0 (disabled)
3 Reserved (special cycle monitoring) ..... fixed at 0
2 Bus Master ..... default=0 (disabled)
1 Memory Space ..... default=0 (disabled)
0 I/O Space ..... default=0 (disabled)

Offset 7-6 - Status ..... RWC

15 Reserved (detected parity error) ..... always reads 0
14 Signalled System Error ..... default=0
13 Received Master Abort ..... default=0
12 Received Target Abort ..... default=0
11 Signalled Target Abort ..... default=0
10-9 DEVSEL# Timing
00 Fast
01 Medium ..... default (fixed)
10 Slow
11 Reserved
8-0 Reserved ..... always reads 0

Offset 8 - Revision ID (nnh) ..... RO

7-0 Silicon Revision Code (0 indicates first silicon)

Offset 9 - Programming Interface (00h) ..... RO

Offset A - Sub Class Code (03h=USB Controller) ..... RO

Offset B - Base Class Code (0Ch=Serial Bus Controller) RO

Offset C – Cache Line Size (00h) ..... RO

Offset D - Latency Timer ..... RW

7-0 Timer Value ..... default = 16h

Offset E - Header Type (00h) ..... RO

Offset F - BIST (00h) ..... RO

Offset 23-20 - USB I/O Register Base Address ..... RW

31-16 Reserved ..... always reads 0
15-5 USB I/O Register Base Address. Port Address for the base of the 32-byte USB I/O Register block, corresponding to AD[15:5]
4-0 00001b

Offset 3C - Interrupt Line (00h) ..... RW

7-4 Reserved ..... always reads 0
3-0 USB Interrupt Routing ..... default = 16h
0000 Disabled ..... default
0001 IRQ1
0010 Reserved
0011 IRQ3
0100 IRQ4
0101 IRQ5
0110 IRQ6
0111 IRQ7
1000 IRQ8
1001 IRQ9
1010 IRQ10
1011 IRQ11
1100 IRQ12
1101 IRQ13
1110 IRQ14
1111 Disabled

Offset 3D - Interrupt Pin (04h) ..... RO

USB-Specific Configuration Registers

Offset 40 - Miscellaneous Control 1 ..... RW

7 PCI Memory Command Option
- 0 Support Memory-Read-Line, Memory-Read-Multiple, & Memory-Write-&-Invalidate....def
- 1 Only support Mem Read, Mem Write Cmds

6 Babble Option
- 0 Automatically disable babbled port when EOF babble occurs .....default
- 1 Don't disable babbled port

5 PCI Parity Check Option
- 0 Disable PERR# generation .....default
- 1 Enable parity check and PERR# generation

4 Frame Interval Select
- 0 1 ms frame .....default
- 1 0.1 ms frame

3 USB Data Length Option
- 0 Support TD length up to 1280 .....default
- 1 Support TD length up to 1023

2 USB Power Management
- 0 Disable USB power management .....default
- 1 Enable USB power management

1 DMA Option
- 0 8 DW burst access with better FIFO latencydef
- 1 16 DW burst access (original performance)

0 PCI Wait States
- 0 Zero wait.....default
- 1 One wait

Offset 41 - Miscellaneous Control 2..... RW

7 USB 1.1 Improvement for EOP
- 0 USB Specification 1.1 Compliant ..... default
  If a bit stuffing error occurs before EOP, the receiver will accept the packet
- 1 USB Specification 1.0 Compliant
  If a bit stuffing error occurs before EOP, the receiver will ignore the packet

6-5 Reserved (Do Not Program)..... default = 0

4 Hold PCI Request for Successive Accesses
- 0 Disable
- 1 Enable..... default

Setting this bit to "enable" causes the system to treat the USB request as higher priority

3 Frame Counter Test Mode
- 0 Disable..... default
- 1 Enable

2 Trap Option
- 0 Set trap 60/64 status bits only when trap 60/64 enable bits are set. ..... default
- 1 Set trap 60/64 status bits without checking enable bits

1 A20gate Pass Through Option
- 0 Pass through A20GATE command sequence defined in UHCI..... default
- 1 Don't pass through Write I/O port 64 (ff)

0 USB IRQ Test Mode
- 0 Normal Operation..... default
- 1 Generate USB IRQ

Offset 42 - FIFO Control.....RW

7-4 Reserved ..... always reads 0
3-2 Reserved (Do Not Program) ..... default = 0
1-0 Release Continuous REQ After "N" PCICLKs
00 Do Not Release .....default
01 N = 32 PCICLKs
10 N = 64 PCICLKs
11 N = 96 PCICLKs

Offset 48 - CRC Control.....RW

7-2 Reserved ..... always reads 0
1 Lengthen PRESOF Time
0 Disable .....default
1 Enable
0 Issue Zero Bad CRC Code on FIFO Under-run
0 Issue Non-Zero CRC .....default
1 Issue All Zero CRC

Offset 60 - Serial Bus Release Number .....RO

7-0 Release Number ..... always reads 10h

Offset 83-80 – PM Capability .....RO

31-0 PM Capability ..... always reads 00020001h

Offset 84 – PM Capability Status .....RW

7-0 PM Capability Status ..... supports 00h and 11h only

Offset C1-C0 - Legacy Support .....RO

15-0 UHCI v1.1 Compliant ..... always reads 2000h

USB I/O Registers

These registers are compliant with the UHCI v1.1 standard. Refer to the UHCI v1.1 specification for further details.

I/O Offset 1-0 - USB Command

I/O Offset 3-2 - USB Status

I/O Offset 5-4 - USB Interrupt Enable

I/O Offset 7-6 - Frame Number

I/O Offset B-8 - Frame List Base Address

I/O Offset 0C - Start Of Frame Modify

I/O Offset 11-10 - Port 2 Status / Control

I/O Offset 13-12 - Port 3 Status / Control

Device 0 Function 4 Regs - Power Management, SMBus and HWM

This section describes the ACPI (Advanced Configuration and Power Interface) Power Management system of the VT8231 which includes a System Management Bus (SMBus) interface controller and Hardware Monitoring (HWM) subsystem. The power management system of the VT8231 supports both ACPI and legacy power management functions and is compatible with the APM v1.2 and ACPI v1.0 specifications.

PCI Configuration Space Header

Offset 1-0 - Vendor ID ..... RO

7-0 Vendor ID ..... (1106h = VIA Technologies)

Offset 3-2 - Device ID ..... RO

7-0 Device ID ..... (8235h = ACPI Power Mgmt)

Offset 5-4 - Command ..... RW

15-8 Reserved ..... always reads 0
7 Address Stepping ..... fixed at 0
6 Reserved (parity error response) ..... fixed at 0
5 Reserved (VGA palette snoop) ..... fixed at 0
4 Memory Write and Invalidate ..... fixed at 0
3 Reserved (special cycle monitoring) ..... fixed at 0
2 Bus Master ..... fixed at 0
1 Memory Space ..... fixed at 0
0 I/O Space ..... fixed at 0

Offset 7-6 - Status ..... RWC

15 Detected Parity Error ..... always reads 0
14 Signalled System Error ..... always reads 0
13 Received Master Abort ..... always reads 0
12 Received Target Abort ..... always reads 0
11 Signalled Target Abort ..... always reads 0
10-9 DEVSEL# Timing
00 Fast
01 Medium ..... default (fixed)
10 Slow
11 Reserved
8 Data Parity Detected ..... always reads 0
7 Fast Back to Back Capable ..... always reads 1
6-0 Reserved ..... always reads 0

Offset 8 - Revision ID (nnh) ..... RO

7-0 Silicon Revision Code

Offset 9 - Programming Interface (00h) ..... RO

The value returned by this register may be changed by writing the desired value to PCI Configuration Function 4 offset 61h.

Offset A - Sub Class Code (00h) ..... RO

The value returned by this register may be changed by writing the desired value to PCI Configuration Function 4 offset 62h.

Offset B - Base Class Code (00h) ..... RO

The value returned by this register may be changed by writing the desired value to PCI Configuration Function 4 offset 63h.

Offset 0D - Latency Timer ..... RW

7-0 Timer Value ..... default = 0

Offset 0E - Header Type (00h) ..... RO

Power Management-Specific PCI Configuration Registers

Offset 40 – General Configuration 0 ..... RW

7 Thermal Alarm Source Select
- 0 From GPI17 (pin P3) .....default
- 1 From any of the three internal temperature sensing circuits (see Rx43 and Rx44 of Hardware Monitoring configuration space)

6 Sleep Button
- 0 Disable .....default
- 1 Sleep Button is on GPI18 (pin K3)

5 Debounce LID and PWRBTN# Inputs for 200us
- 0 Disable .....default
- 1 Enable

4 Reserved ..... always reads 0

3 Microsoft Sound Monitor in Audio Access
- 0 Disable .....default
- 1 Enable

2 Game Port Monitor in Audio Access
- 0 Disable .....default
- 1 Enable

1 SoundBlaster Monitor in Audio Access
- 0 Disable .....default
- 1 Enable

0 MIDI Monitor in Audio Access
- 0 Disable .....default
- 1 Enable

Offset 41 - General Configuration 1 ..... RW

7 I/O Enable for ACPI I/O Base
- 0 Disable access to ACPI I/O block ..... default
- 1 Allow access to Power Management I/O Register Block (see offset 4B-48 to set the base address for this register block). The definitions of the registers in the Power Management I/O Register Block are included later in this document, following the Power Management Subsystem overview.

6 ACPI Timer Reset
- 0 Normal Timer Operation ..... default
- 1 Reset Timer

5-4 PMU Timer Test Mode (Do Not Program).... def = 0

3 ACPI Timer Count Select
- 0 24-bit Timer..... default
- 1 32-bit Timer

2 RTC Enable Signal Gated with PSON (SUSC#) in Soft-Off Mode
- 0 Disable..... default
- 1 Enable

1 Clock Throttling Clock Selection
- 0 30 usec (512 usec cycle time)..... default
- 1 1 msec (16 msec cycle time)

0 DEVSEL# Test Mode (Do Not Program) ..... def = 0

Offset 42 - ACPI Interrupt Select.....RW

7 ATX / AT Power Indicator ..... RO
- 0 ATX
- 1 AT

6 SUSC# State ..... RO

5 Reserved ..... always reads 0

4 SUSC# AC-Power-On Default Value..... RO

This bit is written at RTC Index 0A bit-7.

3-0 SCI Interrupt Assignment

0000 Disabled .....default
0001 IRQ1
0010 Reserved
0011 IRQ3
0100 IRQ4
0101 IRQ5
0110 IRQ6
0111 IRQ7
1000 IRQ8
1001 IRQ9
1010 IRQ10
1011 IRQ11
1100 IRQ12
1101 IRQ13
1110 IRQ14
1111 IRQ15

Offset 43 – Internal Timer Read Test .....RO

7-0 Internal Timer Read Test

Offset 45-44 - Primary Interrupt Channel (0000h)..... RW

15 1/0 = Ena/Disa IRQ15 as Primary Intrpt Channel
14 1/0 = Ena/Disa IRQ14 as Primary Intrpt Channel
13 1/0 = Ena/Disa IRQ13 as Primary Intrpt Channel
12 1/0 = Ena/Disa IRQ12 as Primary Intrpt Channel
11 1/0 = Ena/Disa IRQ11 as Primary Intrpt Channel
10 1/0 = Ena/Disa IRQ10 as Primary Intrpt Channel
9 1/0 = Ena/Disa IRQ9 as Primary Intrpt Channel
8 1/0 = Ena/Disa IRQ8 as Primary Intrpt Channel
7 1/0 = Ena/Disa IRQ7 as Primary Intrpt Channel
6 1/0 = Ena/Disa IRQ6 as Primary Intrpt Channel
5 1/0 = Ena/Disa IRQ5 as Primary Intrpt Channel
4 1/0 = Ena/Disa IRQ4 as Primary Intrpt Channel
3 1/0 = Ena/Disa IRQ3 as Primary Intrpt Channel
2 Reserved .....always reads 0
1 1/0 = Ena/Disa IRQ1 as Primary Intrpt Channel
0 1/0 = Ena/Disa IRQ0 as Primary Intrpt Channel

Offset 47-46 - Secondary Interrupt Channel (0000h) ... RW

15 1/0 = Ena/Disa IRQ15 as Secondary Intr Channel
14 1/0 = Ena/Disa IRQ14 as Secondary Intr Channel
13 1/0 = Ena/Disa IRQ13 as Secondary Intr Channel
12 1/0 = Ena/Disa IRQ12 as Secondary Intr Channel
11 1/0 = Ena/Disa IRQ11 as Secondary Intr Channel
10 1/0 = Ena/Disa IRQ10 as Secondary Intr Channel
9 1/0 = Ena/Disa IRQ9 as Secondary Intr Channel
8 1/0 = Ena/Disa IRQ8 as Secondary Intr Channel
7 1/0 = Ena/Disa IRQ7 as Secondary Intr Channel
6 1/0 = Ena/Disa IRQ6 as Secondary Intr Channel
5 1/0 = Ena/Disa IRQ5 as Secondary Intr Channel
4 1/0 = Ena/Disa IRQ4 as Secondary Intr Channel
3 1/0 = Ena/Disa IRQ3 as Secondary Intr Channel
2 Reserved .....always reads 0
1 1/0 = Ena/Disa IRQ1 as Secondary Intr Channel
0 1/0 = Ena/Disa IRQ0 as Secondary Intr Channel

Offset 4B-48 – Power Management I/O Base .....RW

31-16 Reserved ..... always reads 0

15-7 Power Management I/O Register Base Address. Port Address for the base of the 128-byte Power Management I/O Register block, corresponding to AD[15:7]. The "I/O Space" bit at offset 41 bit-7 enables access to this register block. The definitions of the registers in the Power Management I/O Register Block are included later in this document, following the Power-Management-Specific PCI Configuration register descriptions and the Power Management Subsystem overview.

6-0 0000001b

Offset 4C – Host Bus Power Management Control .....RW

7-4 Thermal Duty Cycle

This 4-bit field determines the duty cycle of the STPCLK# signal when the THRM pin is asserted low. The field is decoded as follows:

0000 Reserved.....default
0001 0-6.25%
0010 6.25-12.50%
0011 18.75-25.00%
0100 31.25-37.50%
0101 37.50-43.75%
0110 43.75-50.00%
0111 50.00-56.25%
1000 56.25-62.50%
1001 62.50-68.75%
1010 68.75-75.00%
1011 75.00-87.50%
1100 75.00-81.25%
1101 81.25-87.50%
1110 87.50-93.75%
1111 93.75-100%

3 THRM Enable

0 Disable .....default
1 Enable

2 Frame Input as Resume Event in C3

0 Disable .....default
1 Enable

1 Reserved ..... always reads 0

0 CPU Stop Grant Cycle Select

0 From Halt and Stop Grant Cycle ..... default
1 From Stop Grant Cycle

This bit is combined with I/O space Rx2C[3] for controlling the start of STPCLK# assertion during system suspend mode (PMIO Rx10[9] should be set to 0):

Rx2C[3] Function 4 I/O Space	Rx4C[0] Function 4 Cfg Space	STPCLK# Assertion
0	x	Immediate
1	0	Wait for CPU Halt / Stop Grant cycle
1	1	Wait for CPU Stop Grant cycle

Offset 4D – Throttle / Clock Stop Control ..... RW

7 Throttle Timer Reset .....def = 0

6-5 Throttle Timer

0x 4-Bit ..... default
10 3-Bit
11 2-Bit

4 Fast Clock (7.5us) as Throttle Timer Tick

0 Disable..... default
1 Enable

3 SMI Level Output (Low)

0 Disable..... default
1 Enable

2 Internal Clock Stop for PCI Idle

0 Disable..... default
1 Enable

1 Internal Clock Stop During C3

0 Disable..... default
1 Enable

0 Internal Clock Stop During Suspend

0 Disable..... default
1 Enable

Offset 53-50 - GP Timer Control (0000 0000h).....RW

31-30 Conserve Mode Timer Count Value
- 00 1/16 second .....default
- 01 1/8 second
- 10 1 second
- 11 1 minute

29 Conserve Mode Status
This bit reads 1 when in Conserve Mode

28 Conserve Mode Enable
- 0 Disable .....default
- 1 Enable

27-26 Secondary Event Timer Count Value
- 00 2 milliseconds .....default
- 01 64 milliseconds
- 10 ½ second
- 11 by EOI + 0.25 milliseconds

25 Secondary Event Occurred Status
This bit reads 1 to indicate that a secondary event has occurred (to resume the system from suspend) and the secondary event timer is counting down.

24 Secondary Event Timer Enable
- 0 Disable .....default
- 1 Enable

23-16 GP1 Timer Count Value (base defined by bits 5-4)
Write to load count value; Read to get current count

15-8 GP0 Timer Count Value (base defined by bits 1-0)
Write to load count value; Read to get current count

7 GP1 Timer Start
On setting this bit to 1, the GP1 timer loads the value defined by bits 23-16 of this register and starts counting down. The GP1 timer is reloaded at the occurrence of certain peripheral events enabled in the GP Timer Reload Enable Register (Power Management I/O Space Offset 38h). If no such event occurs and the GP1 timer counts down to zero, then the GP1 Timer Timeout Status bit is set to one (bit-3 of the Global Status register at Power Management Register I/O Space Offset 28h). Additionally, if the GP1 Timer Timeout Enable bit is set (bit-3 of the Global Enable register at Power Management Register I/O Space Offset 2Ah), then an SMI is generated.

6 GP1 Timer Automatic Reload
- 0 GP1 Timer stops at 0 .....default
- 1 Reload GP1 timer automatically after counting down to 0

5-4 GP1 Timer Base
- 00 Disable .....default
- 01 1/16 second
- 10 1 second
- 11 1 minute

3 GP0 Timer Start
On setting this bit to 1, the GP0 timer loads the value defined by bits 15-8 of this register and starts counting down. The GP0 timer is reloaded at the occurrence of certain peripheral events enabled in the GP Timer Reload Enable Register (Power Management I/O Space Offset 38h). If no such event occurs and the GP0 timer counts down to zero, then the GP0 Timer Timeout Status bit is set to one (bit-2 of the Global Status register at Power Management Register I/O Space Offset 28h). Additionally, if the GP0 Timer Timeout Enable bit is set (bit-2 of the Global Enable register at Power Management Register I/O Space Offset 2Ah), then an SMI is generated.

2 GP0 Timer Automatic Reload
- 0 GP0 Timer stops at 0 ..... default
- 1 Reload GP0 timer automatically after counting down to 0

1-0 GP0 Timer Base
- 00 Disable..... default
- 01 1/16 second
- 10 1 second
- 11 1 minute

Offset 54 – Power Well Control.....WO

7 SMBus Clock Select
- 0 SMBus Clock from 14.31818 MHz Divider
- 1 SMBus Clock from RTC 32.768 KHz ... defult

6 STR Power Well Output Gating
- 0 Disable .....default
- 1 Enable

5 SUSC# = 0 for STR
- 0 Disable .....default
- 1 Enable

4 SUSST1# / GPO3 Select (Pin N5)
- 0 SUSST1# .....default
- 1 GPO3

3 GPO2 / SUSB# Select (Pin P2)
- 0 SUSB# .....default
- 1 GPO2

2 GPO1 / SUSA# Select (Pin P1)
- 0 SUSA# .....default
- 1 GPO1

1-0 GPO0 (SLOWCLK) Output Selection (Pin R4)
- 00 From GPO0 (PMU I/O Rx4C[0]) .....default
- 01 1 Hz
- 10 4 Hz
- 11 16 Hz

Offset 55 – Miscellaneous Control ..... RW

7 CPUSTP# Deasserted to SUST# Deasserted Time
- 0 1-2 msec ..... default
- 1 125-250 usec

6 SUSST# Deasserted Before PWRGD for STD Wakeup
- 0 Disable..... default
- 1 Enable

5-4 Reserved .....always reads 0

3 SMB2 / GPO Select
- 0 SMBDT2 / SMBCK2 ..... default
- 1 GPO26 / GPO27

2 Alert On LAN (AOL) 2 SMB Slave
- 0 Enable..... default
- 1 Disable

1 SUSCLK / GPO4 Select
- 0 SUSCLK ..... default
- 1 GPO4

0 USB Wakeup for STR / STD / SoftOff
- 0 Disable..... default
- 1 Enable

Offset 56 – Power On / Reset Control..... RW

7-5 Reserved .....always reads 0

4 Power On / Reset via AOL2 SMBus GPIO
- 0 Disable..... default
- 1 Enable

3-0 CPU Frequency Strapping Value Output to NMI, INTR, IGNNE#, and A20M# during RESET#

Offset 58 – GP2 / GP3 Timer Control.....RW

7 GP3 Timer Start

On setting this bit to 1, the GP3 timer loads the value defined by Rx5A and starts counting down. The GP3 timer is reloaded at the occurrence of certain events enabled in the GP Timer Reload Enable Register (Power Management I/O Space Offset 38h). If no such event occurs and the GP3 timer counts down to zero, then the GP3 Timer Timeout Status bit is set to one (bit-13 of the Global Status register at Power Management Register I/O Space Offset 28h). Additionally, if the GP3 Timer Timeout Enable bit is set (bit-13 of the Global Enable register at Power Management Register I/O Space Offset 2Ah), then an SMI is generated.

6 GP3 Timer Automatic Reload

0 GP3 Timer stops at 0 .....default
1 Reload GP3 timer automatically after counting down to 0

5-4 GP3 Timer Tick Select

00 Disable .....default
01 1/16 second
10 1 second
11 1 minute

3 GP2 Timer Start

On setting this bit to 1, the GP2 timer loads the value defined by Rx59 and starts counting down. The GP2 timer is reloaded at the occurrence of certain events enabled in the GP Timer Reload Enable Register (Power Management I/O Space Offset 38h). If no such event occurs and the GP2 timer counts down to zero, then the GP2 Timer Timeout Status bit is set to one (bit-12 of the Global Status register at Power Management Register I/O Space Offset 28h). Additionally, if the GP2 Timer Timeout Enable bit is set (bit-12 of the Global Enable register at Power Management Register I/O Space Offset 2Ah), then an SMI is generated.

2 GP2 Timer Automatic Reload

0 GP2 Timer stops at 0 .....default
1 Reload GP2 timer automatically after counting down to 0

1-0 GP2 Timer Tick Select

00 Disable .....default
01 1/16 second
10 1 second
11 1 minute

Offset 59 – GP2 Timer ..... RW

7 Write: GP2 Timer Load Value ..... default = 0
Read: GP2 Timer Current Count

Offset 5A – GP3 Timer ..... RW

7 Write: GP3 Timer Load Value ..... default = 0
Read: GP3 Timer Current Count

Offset 61 – Program Interface Read Value .....WO

7-0 Rx09 Read Value

The value returned by the register at offset 9h (Programming Interface) may be changed by writing the desired value to this location.

Offset 62 - Sub Class Read Value .....WO

7-0 Rx0A Read Value

The value returned by the register at offset 0Ah (Sub Class Code) may be changed by writing the desired value to this location.

Offset 63 - Base Class Read Value.....WO

7-0 Rx0B Read Value

The value returned by the register at offset 0Bh (Base Class Code) may be changed by writing the desired value to this location.

Hardware-Monitor-Specific Configuration Registers

Offset 71-70 – Hardware Monitor I/O Base ..... RW

15-7 I/O Base (128-byte I/O space) ..... default = 0
must be multiple of 256

6-0 Fixed ..... always reads 0000001b

Offset 74 –Hardware Monitor Control ..... RW

7-4 Reserved ..... always reads 0

3 Hardware Monitoring Interrupt
- 0 SMI .....default
- 1 SCI

2-1 Reserved ..... always reads 0

0 Hardware Monitoring I/O Enable
- 0 Disable hardware monitor functions .....default
- 1 Enable hardware monitor functions

System Management Bus-Specific Configuration Registers

Offset 93-90 – SMBus I/O Base ..... RW

31-16 Reserved .....always reads 0

15-4 I/O Base (16-byte I/O space) ..... default = 00h

3-0 Fixed .....always reads 0001b

Offset D2 – SMBus Host Configuration ..... RW

7-4 Reserved .....always reads 0

3 SMBus Interrupt Select
- 0 SMI ..... default
- 1 SCI

2 SMBus 64KHz Clock
- 0 Disable..... default
- 1 Enable. Valid only if Function 4 Rx54[7] = 1 (SMBus clock selected from RTC 32.768KHz)

1 SMBus IRQ
- 0 Disable..... default
- 1 Enable

0 SMBus Host Controller Enable
- 0 Disable SMB controller functions..... default
- 1 Enable SMB controller functions

Offset D3 – SMBus Host Slave Command ..... RW

7-0 SMBus Host Slave Command Code .....default=0

Offset D4 – SMBus Slave Address for Port 1 ..... RW

7-0 SMBus Slave Address for Port 1 .....default=0

Bit-0 must be set to 0 for proper operation

Offset D5 – SMBus Slave Address for Port 2 ..... RW

7-0 SMBus Slave Address for Port 2 .....default=0

Bit-0 must be set to 0 for proper operation

Offset D6 – SMBus Revision ID ..... RO

7-0 SMBus Revision Code

General Purpose I/O Control Registers

Offset E0 – GPI Inversion Control ..... RW

7-0 GPI[27-24, 19-16] Inversion Control
- 0 Non-inverted input, falling edge ..... default
- 1 Inverted input, rising edge

Offset E1 – GPI SCI / SMI Select ..... RW

7-0 GPI[27-24, 19-16] SCI / SMI Select
- 0 SCI ..... default
- 1 SMI

Offset E4 – GPO Pin Select ..... RW

7 GPO22-23 / IOR#, IOW# Select (Pins U7, T7)
- 0 U7 = GPIO22, T7 = GPIO23 ..... default
- 1 U7 = IOR#, T7 = IOW#

6 GPO20-21 / LA20-21 Select (Pins W13, Y13)
- 0 W13 = GPIO20, Y13 = GPIO21 ..... default
  (also USBOC2-3# if PMIO Rx4E[4-5] = 1)
- 1 W13 = LA20, Y13 = LA21

5 GPIO19, PCS1# Select (Pin G5)
- 0 G5 = GPIO19 ..... default
- 1 G5 = PCS1#

4 SLP# / GPO7 Select (Pin U6)
- 0 U6 = SLP# ..... default
- 1 U6 = GPO7

3 MCCS# / GPO17 Select (Pin W6)
- 0 W6 = MCCS# ..... default
- 1 W6 = GPO17

2 PCS0# / GPO16 Select (Pin Y6)
- 0 Y6 = PCS0# ..... default
- 1 Y6 = GPO16

1 PCISTP# / GPO6 Select (Pin T4)
- 0 T4 = PCISTP# ..... default
- 1 T4 = GPO6

0 CPUSTP# / GPO5 Select (Pin W2)
- 0 W2 = CPUSTP# ..... default
- 1 W2 = GPO5

Offset E5 – GPIO I/O Select 1 ..... RW

7 GPI15 Pin Function (Pin Y8)
- 0 F0 Rx58[5] = 0: Y8 = GPI15 ..... default
  F0 Rx58[5] = 1: Y8 = LDRQ
- 1 Reserved (Do Not Program)

6 GPIOC Pin Function (Pin J5)
- 0 J5 = GPIOC ..... default
- 1 J5 = CHSINOUT

5 GPO14-15 Pin Function (Pins R8 and U8)
- 0 IRTX and IRRX ..... default
- 1 GPO14-15

4 GPO12-13 Pin Function (Pins H5 & H4)
- 0 GPO12-13 ..... default
- 1 JAB2 and JBB2

3 GPO8-9, GPI10-11 (Pins W11, T10, Y11, V11)
- 0 GPO8/9 pins are HGNT1# / HGNT2#,
  GPI10/11 pins are HREQ1# / HREQ2# default
- 1 GPO8-9, GPI10-11

2 GPO10-11, GPI12-13 (Pins Y10, V10, U10, W10)
- 0 GPO10/11 pins are LGNT1# / LGNT2#
  GPI12/13 pins are LREQ1# / LREQ2#. default
- 1 GPO10-11, GPI12/13

1 GPI19 / GPO19 Pin Function (Pin G5)
- 0 G5 = GPI19 ..... default
- 1 G5 = GPO19

0 GPI18 / GPO18 Pin Function (Pin K3)
- 0 K3 = GPI18 ..... default
- 1 K3 = GPO18 / FAN2

Offset E6 – GPIO I/O Select 2 ..... RW

7 GPI31 / GPO31 (GPIOE) Pin Function (Pin W3)
- 0 GPI31 ..... default
- 1 GPO31 / GPIOE

6 GPI30 / GPO30 (GPIOD) Pin Function (Pin Y1)
- 0 GPI30 ..... default
- 1 GPO30 / GPIOD

5-2 Reserved ..... always reads 0

1 GPI25 / GPO25 (GPIOC) Pin Function (Pin J5)
- 0 GPI25 ..... default
- 1 GPO25 / GPIOC

0 GPI24 / GPO24 (GPIOA) Pin Function (Pin Y2)
- 0 GPI24 ..... default
- 1 GPO24 / GPIOA

Offset E7 – GPO Output Type ..... RW

7 GPO31 OD/TTL Select (Pin W3)
- 0 OD ..... default
- 1 TTL

6 GPO30 OD/TTL Select (Pin Y1)
- 0 OD ..... default
- 1 TTL

5-2 Reserved ..... always reads 0

1 GPO25 OD/TTL Select (Pin J5)
- 0 OD ..... default
- 1 TTL

0 GPO24 OD/TTL Select (Pin Y2)
- 0 OD ..... default
- 1 TTL

Power Management I/O-Space Registers

Basic Power Management Control and Status

I/O Offset 1-0 - Power Management Status..... RWC

The bits in this register are set only by hardware and can be reset by software by writing a one to the desired bit position.

15 Wakeup Status ..... default = 0
This bit is set when the system is in the suspend state and an enabled resume event occurs. Upon setting this bit, the system automatically transitions from the suspend state to the normal working state (from C3 to C0 for the processor).

14-12 Reserved ..... always reads 0

11 Abnormal Power-Off..... default = 0

10 RTC Status default = 0
This bit is set when the RTC generates an alarm (on assertion of the RTC IRQ signal).

9 Sleep Button Status..... default = 0
This bit is set when the sleep button (SLPBTN# / GPI18) is pressed.

8 Power Button Status..... default = 0
This bit is set when the PWRBTN# signal is asserted LOW. If the PWRBTN# signal is held LOW for more than four seconds, this bit is cleared, the Power Button Status bit is set, and the system will transition into the soft off state.

7-6 Reserved ..... always reads 0

5 Global Status..... default = 0
This bit is set by hardware when BIOS Release is set (typically by an SMI routine to release control of the SCI / SMI lock). When this bit is cleared by software (by writing a one to this bit position) the BIOS Release bit is also cleared at the same time by hardware.

4 Bus Master Status..... default = 0
This bit is set when a system bus master requests the system bus. All PCI master, ISA master and ISA DMA devices are included.

3-1 Reserved ..... always reads 0

0 ACPI Timer Carry Status..... default = 0
The bit is set when the 23rd (31st) bit of the 24 (32) bit ACPI power management timer changes.

I/O Offset 3-2 - Power Management Enable..... RW

The bits in this register correspond to the bits in the Power Management Status Register at offset 1-0.

15 Reserved .....always reads 0

14-12 Reserved .....always reads 0

11 Reserved .....always reads 0

10 RTC Enabledefault = 0
This bit may be set to trigger either an SCI or an SMI (depending on the setting of the SCI Enable bit) to be generated when the RTC Status bit is set.

9 Sleep Button Enable.....default = 0
This bit may be set to trigger either an SCI or SMI when the Sleep Button Status bit is set.

8 Power Button Enable.....default = 0
This bit may be set to trigger either an SCI or an SMI (depending on the setting of the SCI Enable bit) to be generated when the Power Button Status bit is set.

7-6 Reserved .....always reads 0

5 Global Enable.....default = 0
This bit may be set to trigger either an SCI or an SMI (depending on the setting of the SCI Enable bit) to be generated when the Global Status bit is set.

4 Reserved .....always reads 0

3-1 Reserved .....always reads 0

0 ACPI Timer Enable.....default = 0
This bit may be set to trigger either an SCI or an SMI (depending on the setting of the SCI Enable bit) to be generated when the Timer Status bit is set.

I/O Offset 5-4 - Power Management Control.....RW

15 Soft Resume

14 Reserved ..... always reads 0

13 Sleep Enable..... always reads 0

This is a write-only bit; reads from this bit always return zero. Writing a one to this bit causes the system to sequence into the sleep (suspend) state defined by the Sleep Type field (bits 12-10 of this register).

12-10 Sleep Type

000 Normal On
001 Suspend to RAM (STR)
010 Suspend to Disk (STD) (also called Soft Off). The VCC power plane is turned off while the VCCS and VBAT planes remain on.
011 Reserved
100 Power On Suspend without Reset
101 Power On Suspend with CPU Reset
110 Power On Suspend with CPU/PCI Reset
111 Reserved

In any sleep state, there is minimal interface between powered and non-powered planes so that the effort for hardware design may be well managed.

9 Reserved ..... always reads 0

8 STD Command Generates System Reset Only

0 Disable .....default
1 Enable

7-3 Reserved ..... always reads 0

2 Global Release..... **WO**, default = 0

This bit is set by ACPI software to indicate the release of the SCI / SMI lock. Upon setting of this bit, the hardware automatically sets the BIOS Status bit. The bit is cleared by hardware when the BIOS Status bit is cleared by software. Note that the setting of this bit will cause an SMI to be generated if the BIOS Enable bit is set (bit-5 of the Global Enable register at offset 2Ah).

1 Bus Master Reload

0 Bus master requests are ignored by power management logic .....default
1 Bus master requests transition the processor from the C3 state to the C0 state

0 SCI Enable

Selects the power management event to generate either an SCI or SMI:

0 Generate SMI.....default
1 Generate SCI

Note that certain power management events can be programmed individually to generate an SCI or SMI independent of the setting of this bit (refer to the General Purpose SCI Enable and General Purpose SMI Enable registers at offsets 22 and 24). Also, Timer Status & Global Status always generate SCI and BIOS Status always generates SMI.

I/O Offset 0B-08 - Power Management Timer..... RW

31-24 Extended Timer Value

This field reads back 0 if the 24-bit timer option is selected (Rx41 bit-3).

23-0 Timer Value

This read-only field returns the running count of the power management timer. This is a 24/32-bit counter that runs off a 3.579545 MHz clock, and counts while in the S0 (working) system state. The timer is reset to an initial value of zero during a reset, and then continues counting until the 14.31818 MHz input to the chip is stopped. If the clock is restarted without a reset, then the counter will continue counting from where it stopped.

Processor Power Management Registers

I/O Offset 13-10 - Processor & PCI Bus Control .....RW

31-12 Reserved ..... always reads 0

11 PCI Stop (PCISTP# asserted) when PCKRUN# is Deasserted

0 Enable .....default
1 Disable

10 PCI Bus Clock Run Without Stop

0 PCKRUN# is always asserted.....default
1 PCKRUN# will be de-activated after the PCI bus is idle for 26 clocks

9 Host Clock Stop Enable

0 STPCLK# will be asserted in C3 state...default
1 STPCLK# will be asserted in C3 and S1 state

8 Assert SLP# for Processor Level 3 Read

0 Disable .....default
1 Enable

Used in Slot-1 systems only.

7-5 Reserved ..... always reads 0

4 Throttling Enable

Setting this bit starts clock throttling (modulating the STPCLK# signal) regardless of the CPU state. The throttling duty cycle is determined by bits 3-0 of this register.

3-0 Throttling Duty Cycle

This 4-bit field determines the duty cycle of the STPCLK# signal when the system is in throttling mode (the "Throttling Enable" bit is set to one). The duty cycle indicates the percentage of time the STPCLK# signal is asserted while the Throttling Enable bit is set. The field is decoded as follows:

0000 Reserved
0001 0-6.25%
0010 6.25-12.50%
0011 18.75-25.00%
0100 31.25-37.50%
0101 37.50-43.75%
0110 43.75-50.00%
0111 50.00-56.25%
1000 56.25-62.50%
1001 62.50-68.75%
1010 68.75-75.00%
1011 75.00-87.50%
1100 75.00-81.25%
1101 81.25-87.50%
1110 87.50-93.75%
1111 93.75-100%

I/O Offset 14 - Processor Level 2 ..... RO

7-0 Level 2 .....always reads 0

Reads from this register put the processor into the Stop Grant state (the VT8231 asserts STPCLK# to suspend the processor). Wake up from Stop Grant state is by interrupt (INTR, SMI, and SCI).

Reads from this register return all zeros; writes to this register have no effect.

I/O Offset 15 - Processor Level 3 ..... RO

7-0 Level 3 .....always reads 0

Reads from this register put the processor in the C3 clock state with the STPCLK# signal asserted. If Rx10[9] = 1 then the CPU clock is also stopped by asserting CPUSTP#. Wakeup from the C3 state is by interrupt (INTR, SMI, and SCI).

Reads from this register return all zeros; writes to this register have no effect.

General Purpose Power Management Registers

I/O Offset 21-20 - General Purpose Status ..... RWC

15 Reserved ..... always reads 0

14 USB Wake-Up Status
For STR / STD / Soff

13 AC97 Wake-Up Status
Can be set only in suspend mode

12 Battery Low Status
This bit is set when the BATLOW# input is asserted low.

11 Notebook Lid Status
This bit is set when the LID input detects the edge selected by Rx2C bit-7 (0=rising, 1=falling).

10 Thermal Detect Status
This bit is set when the THRM input detects the edge selected by Rx2C bit-6 (0=rising, 1=falling).

9 USB Resume Status
This bit is set when a USB peripheral generates a resume event.

8 Ring Status
This bit is set when the RING# input is asserted low.

7 Reserved ..... always reads 0

6 INTRUDER# Status
This bit is set when the INTRUDER# pin is asserted low.

5 PME# Status
This bit is set when the PME# pin is asserted low.

4 EXTSMI# Status
This bit is set when the EXTSMI# pin is asserted low.

3 Internal LAN PME Status
This bit is set when the internal LAN PME signal is asserted.

2 Internal KBC PME Status
This bit is set when the internal KBC PME signal is asserted.

1 GPI1 Status
This bit is set when the GPI1 pin is asserted low.

0 GPI0 Status
This bit is set when the GPI0 pin is asserted low.

Note that the above bits correspond one for one with the bits of the General Purpose SCI Enable and General Purpose SMI Enable registers at offsets 22 and 24: an SCI or SMI is generated if the corresponding bit of the General Purpose SCI or SMI Enable registers, respectively, is set to one and the condition occurs.

The above bits are set by hardware only and can only be cleared by writing a one to the desired bit.

I/O Offset 23-22 - General Purpose SCI Enable..... RW

15 Reserved ..... always reads 0
14 Enable SCI on setting of PMIO Rx20[14]..... def=0
13 Enable SCI on setting of PMIO Rx20[13]..... def=0
12 Enable SCI on setting of PMIO Rx20[12]..... def=0
11 Enable SCI on setting of PMIO Rx20[11]..... def=0
10 Enable SCI on setting of PMIO Rx20[10]..... def=0
9 Enable SCI on setting of PMIO Rx20[9]..... def=0
8 Enable SCI on setting of PMIO Rx20[8]..... def=0
7 Reserved ..... always reads 0
6 Enable SCI on setting of PMIO Rx20[6]..... def=0
5 Enable SCI on setting of PMIO Rx20[5]..... def=0
4 Enable SCI on setting of PMIO Rx20[4]..... def=0
3 Enable SCI on setting of PMIO Rx20[3]..... def=0
2 Enable SCI on setting of PMIO Rx20[2]..... def=0
1 Enable SCI on setting of PMIO Rx20[1]..... def=0
0 Enable SCI on setting of PMIO Rx20[0]..... def=0

These bits allow generation of an SCI using a separate set of conditions from those used for generating an SMI.

I/O Offset 25-24 - General Purpose SMI Enable..... RW

15-14 Reserved ..... always reads 0
13 Enable SMI on setting of PMIO Rx20[13]..... def=0
12 Enable SMI on setting of PMIO Rx20[12]..... def=0
11 Enable SMI on setting of PMIO Rx20[11]..... def=0
10 Enable SMI on setting of PMIO Rx20[10]..... def=0
9 Enable SMI on setting of PMIO Rx20[9]..... def=0
8 Enable SMI on setting of PMIO Rx20[8]..... def=0
7 Reserved ..... always reads 0
6 Enable SMI on setting of PMIO Rx20[6]..... def=0
5 Enable SMI on setting of PMIO Rx20[5]..... def=0
4 Enable SMI on setting of PMIO Rx20[4]..... def=0
3 Enable SMI on setting of PMIO Rx20[3]..... def=0
2 Enable SMI on setting of PMIO Rx20[2]..... def=0
1 Enable SMI on setting of PMIO Rx20[1]..... def=0
0 Enable SMI on setting of PMIO Rx20[0]..... def=0

These bits allow generation of an SMI using a separate set of conditions from those used for generating an SCI.

Generic Power Management Registers

I/O Offset 29-28 - Global Status ..... RWC

15 GPIO Range 1 Access Status ..... def=0

14 GPIO Range 0 Access Status ..... def=0

13 GP3 Timer Timeout Status ..... def=0

12 GP2 Timer Timeout Status ..... def=0

11 SERIRQ SMI Status ..... def=0

10-9 Reserved ..... always reads 0

8 PCKRUN# Resume Status ..... def=0
This bit is set when PCI bus peripherals wake up the system by asserting PCKRUN#

7 Primary IRQ Resume Status ..... def=0
This bit is set at the occurrence of primary IRQs as defined in Rx45-44 of PCI configuration space

6 Software SMI Status ..... def=0
This bit is set when the SMI Command port (offset 2F) is written.

5 BIOS Status def=0
This bit is set when the Global Release bit is set to one (typically by the ACPI software to release control of the SCI/SMI lock). When this bit is reset (by writing a one to this bit position) the Global Release bit is reset at the same time by hardware.

4 Legacy USB Status ..... def=0
This bit is set when a legacy USB event occurs.

3 GP1 Timer Time Out Status ..... def=0
This bit is set when the GP1 timer times out.

2 GP0 Timer Time Out Status ..... def=0
This bit is set when the GP0 timer times out.

1 Secondary Event Timer Time Out Status ..... def=0
This bit is set when the secondary event timer times out.

0 Primary Activity Status ..... def=0
This bit is set at the occurrence of any enabled primary system activity (see the Primary Activity Detect Status register at offset 30h and the Primary Activity Detect Enable register at offset 34h). After checking this bit, software can check the status bits in the Primary Activity Detect Status register at offset 30h to identify the specific source of the primary event. Note that setting this bit can be enabled to reload the GP0 timer (see bit-0 of the GP Timer Reload Enable register at offset 38).

Note that SMI can be generated based on the setting of any of the above bits (see the offset 2Ah Global Enable register bit descriptions in the right hand column of this page).

The bits in this register are set by hardware only and can only be cleared by writing a one to the desired bit position.

I/O Offset 2B-2A - Global Enable ..... RW

15 GPIO Range 1 SMI Enable ..... def=0

14 GPIO Range 0 SMI Enable ..... def=0

13 GP3 Timer Timeout SMI Enable ..... def=0

12 GP2 Timer Timeout SMI Enable ..... def=0

11 SERIRQ SMI Enable ..... def=0

10-9 Reserved ..... always reads 0

8 PCKRUN# Resume Enable ..... def=0
This bit may be set to trigger an SMI to be generated when the PCKRUN# Resume Status bit is set.

7 Primary IRQ Resume Enable ..... def=0
This bit may be set to trigger an SMI to be generated when the Primary IRQ Resume Status bit is set.

6 SMI on Software SMI ..... def=0
This bit may be set to trigger an SMI to be generated when the Software SMI Status bit is set.

5 SMI on BIOS Status ..... def=0
This bit may be set to trigger an SMI to be generated when the BIOS Status bit is set.

4 SMI on Legacy USB ..... def=0
This bit may be set to trigger an SMI to be generated when the Legacy USB Status bit is set.

3 SMI on GP1 Timer Time Out ..... def=0
This bit may be set to trigger an SMI to be generated when the GP1 Timeout Status bit is set.

2 SMI on GP0 Timer Time Out ..... def=0
This bit may be set to trigger an SMI to be generated when the GP0 Timeout Status bit is set.

1 SMI on Secondary Event Timer Time Out .... def=0
This bit may be set to trigger an SMI to be generated when the Secondary Event Timer Timeout Status bit is set.

0 SMI on Primary Activity ..... def=0
This bit may be set to trigger an SMI to be generated when the Primary Activity Status bit is set.

I/O Offset 2D-2C - Global Control ..... RW

15-12 Reserved ..... always reads 0

11 IDE Secondary Bus Power-Off
- 0 Disable .....default
- 1 Enable

10 IDE Primary Bus Power-Off
- 0 Disable .....default
- 1 Enable

9 Reserved ..... always reads 0

8 SMI Active (INSMI)
- 0 SMI Inactive .....default
- 1 SMI Active. If the SMIIG bit is set, this bit needs to be written with a 1 to clear it before the next SMI can be generated.

7 LID Triggering Polarity
- 0 Rising Edge.....default
- 1 Falling Edge

6 THRM Triggering Polarity
- 0 Rising Edge.....default
- 1 Falling Edge

5 Battery Low Resume Disable
- 0 Enable resume.....default
- 1 Disable resume from suspend when BATLOW# is asserted

4 SMI Lock (SMIIG)
- 0 Disable SMI Lock
- 1 Enable SMI Lock (SMI low to gate for the next SMI) .....default

3 Wait for Halt / Stop Grant Cycle for STPCLK# Assertion
- 0 Don't wait .....default
- 1 Wait

This bit works with Function 4 Rx4C[7] to control the start of STPCLK# assertion.

2 Power Button Triggering Select
- 0 SCI/SMI generated by PWRBTN# rising edge .....default
- 1 SCI/SMI generated by PWRBTN# low level

Set to zero to avoid the situation where Power Button Status is set to wake up the system then reset again by Power Button Status to switch the system into the soft-off state.

1 BIOS Release

This bit is set by legacy software to indicate release of the SCI / SMI lock. Upon setting of this bit, hardware automatically sets the Global Status bit. This bit is cleared by hardware when the Global Status bit cleared by software.

Note that if the Global Enable bit is set (bit-5 of the Power Management Enable register at offset 2), then setting this bit causes an SCI to be generated (because setting this bit causes the Global Status bit to be set).

0 SMI Enable
- 0 Disable all SMI generation .....default
- 1 Enable SMI generation

I/O Offset 2F - SMI Command ..... RW

7-0 SMI Command

Writing to this port sets the Software SMI Status bit. Note that if the Software SMI Enable bit is set (see bit-6 of the Global Enable register at offset 2Ah), then an SMI is generated.

I/O Offset 33-30 - Primary Activity Detect Status ..... RWC

These bits correspond to the Primary Activity Detect Enable bits in offset 37-34. All bits default to 0, are set by hardware only, and may only be cleared by writing 1s to the desired bit.

31-11 Reserved ..... always read 0

10 Audio Access Status
Set if Audio is accessed.

9 Keyboard Controller Access Status
Set if the KBC is accessed via I/O port 60h.

8 VGA Access Status
Set if the VGA port is accessed via I/O ports 3B0-3DFh or memory space A0000-BFFFFh.

7 Parallel Port Access Status
Set if the parallel port is accessed via I/O ports 278-27Fh or 378-37Fh (LPT2 or LPT1).

6 Serial Port B Access Status
Set if the serial port is accessed via I/O ports 2F8-2FFh or 2E8-2EFh (COM2 & COM4 respectively).

5 Serial Port A Access Status
Set if the serial port is accessed via I/O ports 3F8-3FFh or 3E8-3EFh (COM1 & COM3, respectively).

4 Floppy Access Status
Set if the floppy controller is accessed via I/O ports 3F0-3F5h or 3F7h.

3 Secondary IDE Access Status
Set if the IDE controller is accessed via I/O ports 170-177h or 376h.

2 Primary IDE Access Status
Set if the IDE controller is accessed via I/O ports 1F0-1F7h or 3F6h.

1 Primary Interrupt Activity Status
Set on the occurrence of a primary interrupt (enabled via the "Primary Interrupt Channel" register at Function 4 PCI configuration register offset 44h).

0 PCI Master Access Status
Set on the occurrence of PCI master activity.

Note: The bits above correspond to the bits of the Primary Activity Detect Enable register at offset 34 (see right hand column of this page): if the corresponding bit is set in that register, setting of the above bits will cause the Primary Activity Status bit to be set (bit-0 of the Global Status register at offset 28). Setting of Primary Activity Status may be set up to enable a "Primary Activity Event": an SMI will be generated if Primary Activity Enable is set (bit-0 of the Global Enable register at offset 2Ah) and/or the GP0 timer will be reloaded if the "GP0 Timer Reload on Primary Activity" bit is set (bit-0 of the GP Timer Reload Enable register at offset 38 on this page).
Note: Bits 2-9 above also correspond to bits of the GP Timer Reload Enable register (see offset 38 on next page): If bits are set in that register, setting a corresponding bit in this register will cause the GP1 timer to be reloaded.

I/O Offset 37-34 - Primary Activity Detect Enable ..... RW

These bits correspond to the Primary Activity Detect Status bits in offset 33-30. Setting of any of these bits also sets the Primary Activity Status bit (PMIO Rx28[0]) which causes the GP0 timer to be reloaded (if Primary Activity GP0 Enable is set) or generates an SMI (if Primary Activity Enable is set).

31-11 Reserved ..... always read 0

10 SMI on Audio Status
0 Don't set Rx28[0] if Audio Status is set ..... def
1 Set Rx28[0] if Audio Status is set

9 SMI on Keyboard Controller Status
0 Don't set Rx28[0] if KBC Status is set ..... def
1 Set Rx28[0] if KBC Status is set

8 SMI on VGA Status
0 Don't set Rx28[0] if VGA Status is set..... def
1 Set Rx28[0] if VGA Status is set

7 SMI on Parallel Port Status
0 Don't set Rx28[0] if LPT Status is set ..... def
1 Set Rx28[0] if LPT Status is set

6 SMI on Serial Port B Status
0 Don't set Rx28[0] if COMB Status is set..... def
1 Set Rx28[0] if COMB Status is set

5 SMI on Serial Port A Status
0 Don't set Rx28[0] if COMA Status is set .... def
1 Set Rx28[0] if COMA Status is set

4 SMI on Floppy Status
0 Don't set Rx28[0] if FDC Status is set ..... def
1 Set Rx28[0] if FDC Status is set

3 SMI on Secondary IDE Status
0 Don't set Rx28[0] if SIDE Status is set ..... def
1 Set Rx28[0] if SIDE Status is set

2 SMI on PrimaryIDE Status
0 Don't set Rx28[0] if PIDE Status is set ..... def
1 Set Rx28[0] if PIDE Status is set

1 SMI on Primary INTR Status
0 Don't set Rx28[0] if PIRQ Status is set ..... def
1 Set Rx28[0] if PIRQ Status is set

0 SMI on PCI Master Status
0 Don't set Rx28[0] if DRQ Status is set..... def
1 Set Rx28[0] if DRQ Status is set

I/O Offset 3B-38 - GP Timer Reload Enable.....RW

All bits in this register default to 0 on power up.

31-8 Reserved .....always read 0

7 GP1 Timer Reload on KBC Access
- 0 Normal GP1 Timer Operation.....default
- 1 Setting of KBC Status causes the GP1 timer to reload.

6 GP1 Timer Reload on Serial Port Access
- 0 Normal GP1 Timer Operation .....default
- 1 Setting of COM Status causes the GP1 timer to reload.

5 Reserved .....always read 0

4 GP1 Timer Reload on VGA Access
- 0 Normal GP1 Timer Operation .....default
- 1 Setting of VGA Status causes the GP1 timer to reload.

3 GP1 Timer Reload on IDE/Floppy Access
- 0 Normal GP1 Timer Operation .....default
- 1 Setting of FDC Status, Secondary IDE Status, or Primary IDE Status causes the GP1 timer to reload.

2 GP3 Timer Reload on GPIO Range 1 Access
- 0 Normal GP3 Timer Operation .....default
- 1 Setting of GR1 Status causes the GP3 timer to reload.

1 GP2 Timer Reload on GPIO Range 0 Access
- 0 Normal GP2 Timer Operation .....default
- 1 Setting of GR0 Status causes the GP2 timer to reload.

0 GP0 Timer Reload on Primary Activity
- 0 Normal GP0 Timer Operation .....default
- 1 Setting of Primary Activity Status causes the GP0 timer to reload. Primary activities are enabled via the Primary Activity Detect Enable register (offset 37-34) with status recorded in the Primary Activity Detect Status register (offset 33-30).

I/O Offset 40 – Extended I/O Trap Status .....RWC

7-5 Reserved ..... always read 0
4 BIOS Write Access Status
3 GP3 Timer Second Timeout With No Cycle
2 GP3 Timer Second Timeout Status
1 GPIO Range 3 Access Status
0 GPIO Range 2 Access Status

I/O Offset 42 – Extended I/O Trap Enable ..... RW

7-5 Reserved ..... always read 0

4 SMI on BIOS Write Access
- 0 Disable..... default
- 1 Enable (can be reset only by OCI Reset)

3 Reserved ..... always read 0

2 GP3 Timer Second Timeout Reboot
- 0 Disable..... default
- 1 Enable

1 SMI on GPIO Range 3 Access
- 0 Disable..... default
- 1 Enable

0 SMI on GPIO Range 2 Access
- 0 Disable..... default
- 1 Enable

I/O Offset 45 – Miscellanous Status..... RW

7-5 Reserved ..... always read 0
4 Lateset PCSn# By IOR/IOW# (0/1) Status
3 FM SMI or Serial SMI Status
2 HWM IRQ Status
1 SMBus IRQ Status
0 SMBus Resume Status

General Purpose I/O Registers

I/O Offset 4B-48 - GPI Port Input Value (GPIVAL).....RO

31-0 GPI[31-0] Input Value .....Read Only

I/O Offset 4F-4C - GPO Port Output Value (GPOVAL)RW

Reads from this register return the last value written (held on chip). For pins that can be used as both input and output (GPIO pins 20-27 and 30-31) the output is OD (open drain) so to use one of these pins as an input pin, a one must be written to the corresponding bit of this register.

31-0 GPO[31-0] Output Value .....def = FFFFFFFFh

I/O Offset 50 – GPI Pin Change Status ..... RW

7 GPI27 Pin Change Status ..... default = 0
6 GPI26 Pin Change Status ..... default = 0
5 GPI25 Pin Change Status ..... default = 0
4 GPI24 Pin Change Status ..... default = 0
3 GPI19 Pin Change Status ..... default = 0
2 GPI18 Pin Change Status ..... default = 0
1 GPI17 Pin Change Status ..... default = 0
0 GPI16 Pin Change Status ..... default = 0

I/O Offset 52 – GPI Pin Change SCI/SMI Select..... RW

7 GPI27 Pin Change SCI / SMI Select
6 GPI26 Pin Change SCI / SMI Select
5 GPI25 Pin Change SCI / SMI Select
4 GPI24 Pin Change SCI / SMI Select
3 GPI19 Pin Change SCI / SMI Select
2 GPI18 Pin Change SCI / SMI Select
1 GPI17 Pin Change SCI / SMI Select
0 GPI16 Pin Change SCI / SMI Select
0 SCI on pin input change ..... default
1 SMI on pin input change

I/O Offset 59-58 – I/O Trap PCI I/O Address ..... RO

15-0 PCI Address During I/O Trap SMI

I/O Offset 5A – I/O Trap PCI Command / Byte Enable RO

7-4 PCI Command Type During I/O Trap SMI
3-0 PCI Byte Enable During I/O Trap SMI

System Management Bus I/O-Space Registers

The base address for these registers is defined in Rx93-90 of the Function 4 PCI configuration registers. The System Management Bus I/O space is enabled for access by the system if RxD2[0] = 1.

I/O Offset 00 – SMBus Host Status ..... RWC

7-5 Reserved ..... always reads 0

4 Failed Bus Transaction ..... RWC
- 0 SMBus interrupt not caused by failed bus transaction.....default
- 1 SMBus interrupt caused by failed bus transaction. This bit may be set when the KILL bit (I/O Rx02[1]) is set and can be cleared by writing a 1 to this bit position.

3 Bus Collision..... RWC
- 0 SMBus interrupt not caused by transaction collision.....default
- 1 SMBus interrupt caused by transaction collision. This bit is only set by hardware and can be cleared by writing a 1 to this bit position.

2 Device Error..... RWC
- 0 SMBus interrupt not caused by generation of an SMBus transaction error .....default
- 1 SMBus interrupt caused by generation of an SMBus transaction error (illegal command field, unclaimed host-initiated cycle, or host device timeout). This bit is only set by hardware and can be cleared by writing a 1 to this bit position.

1 SMBus Interrupt..... RWC
- 0 SMBus interrupt not caused by host command completion .....default
- 1 SMBus interrupt caused by host command completion. This bit is only set by hardware and can be cleared by writing a 1 to this bit position.

0 Host Busy ..... RO
- 0 SMBus controller host interface is not processing a command.....default
- 1 SMBus host controller is busy processing a command. None of the other SMBus registers should be accessed if this bit is set.

I/O Offset 01h – SMBus Slave Status ..... RWC

7-6 Reserved ..... always reads 0

5 Alert Status ..... RWC
- 0 SMBus interrupt not caused by SMBALERT# signal ..... default
- 1 SMBus interrupt caused by SMBALERT# signal. This bit will be set only if the Alert Enable bit is set in the SMBus Slave Control Register at I/O Offset R08[3]. This bit is only set by hardware and can be cleared by writing a 1 to this bit position.

4 Shadow 2 Status ..... RWC
- 0 SMBus interrupt not caused by address match to SMBus Shadow Address Port 2 ..... default
- 1 SMBus interrupt or resume event caused by slave cycle address match to SMBus Shadow Address Port 2. This bit is only set by hardware and can be cleared by writing a 1 to this bit position.

3 Shadow 1 Status ..... RWC
- 0 SMBus interrupt not caused by address match to SMBus Shadow Address Port 1 ..... default
- 1 SMBus interrupt or resume event caused by slave cycle address match to SMBus Shadow Address Port 1. This bit is only set by hardware and can be cleared by writing a 1 to this bit position.

2 Slave Status ..... RWC
- 0 SMBus interrupt not caused by slave event match ..... default
- 1 SMBus interrupt or resume event caused by slave cycle event match of the SMBus Slave Command Register at PCI Function 4 Configuration Offset D3h (command match) and the SMBus Slave Event Register at SMBus Base + Offset 0Ah (data event match). This bit is only set by hardware and can be cleared by writing a 1 to this bit position.

1 Reserved ..... always reads 0

0 Slave Busy ..... RO
- 0 SMBus controller slave interface is not processing data ..... default
- 1 SMBus controller slave interface is busy receiving data. None of the other SMBus registers should be accessed if this bit is set.

I/O Offset 02h – SMBus Host Control ..... RW

7 Reserved ..... always reads 0

6 Start ..... always reads 0

0 Writing 0 has no effect.....default

1 Start Execution of Command

Writing a 1 to this bit causes the SMBus controller host interface to initiate execution of the command programmed in the SMBus Command Protocol field (bits 4-2). All necessary registers should be programmed prior to writing a 1 to this bit. The Host Busy bit (SMBus Host Status Register bit-0) can be used to identify when the SMBus controller has completed command execution.

5 Reserved ..... always reads 0

4-2 SMBus Command Protocol

000 Quick Read or Write.....default

001 Byte Read or Write

010 Byte Data Read or Write

011 Word Data Read or Write

100 Reserved

101 Block Read or Write

110 Reserved

111 Reserved

1 Kill Transaction in Progress

0 Normal host controller operation.....default

1 Stop host transaction currently in progress.

Setting this bit also sets the FAILED status bit (Host Status bit-4) and asserts the interrupt selected by the SMB Interrupt Select bit (Function 4 SMBus Host Configuration Register RxD2[3]).

0 Interrupt Enable

0 Disable interrupt generation.....default

1 Enable generation of interrupts on completion of the current host transaction.

I/O Offset 03h – SMBus Host Command ..... RW

7-0 SMBUS Host Command.....default = 0

This field contains the data transmitted in the command field of the SMBus host transaction.

I/O Offset 04h – SMBus Host Address ..... RW

The contents of this register are transmitted in the address field of the SMBus host transaction.

7-1 SMBUS Address.....default = 0

This field contains the 7-bit address of the targeted slave device.

0 SMBUS Read or Write

0 Execute a WRITE command..... default

1 Execute a READ command

I/O Offset 05h – SMBus Host Data 0..... RW

The contents of this register are transmitted in the Data 0 field of SMBus host transaction writes. On reads, Data 0 bytes are stored here.

7-0 SMBUS Data 0.....default = 0

For Block Write commands, this field is programmed with the block transfer count (a value between 1 and 32). Counts of 0 or greater than 32 are undefined. For Block Read commands, the count received from the SMBus device is stored here.

I/O Offset 06h – SMBus Host Data 1..... RW

The contents of this register are transmitted in the Data 1 field of SMBus host transaction writes. On reads, Data 1 bytes are stored here.

7-0 SMBUS Data 1.....default = 0

I/O Offset 07h – SMBus Block Data ..... RW

Reads and writes to this register are used to access the 32-byte block data storage array. An internal index pointer is used to address the array. It is reset to 0 by reads of the SMBus Host Control register (I/O Offset 2) and incremented automatically by each access to this register. The transfer of block data into (read) or out of (write) this storage array during an SMBus transaction always starts at index address 0.

7-0 SMBUS Block Data.....default = 0

I/O Offset 08h – SMBus Slave Control ..... RW

7-4 Reserved ..... always reads 0

3 SMBus Alert Enable
- 0 Disable .....default
- 1 Enable generation of an interrupt or resume event on the assertion of the SMBALERT# signal

2 SMBus Shadow Port 2 Enable
- 0 Disable .....default
- 1 Enable generation of an interrupt or resume event on external SMBus master generation of a transaction with an address that matches the SMBus Slave Shadow Port 2 register (PCI function 4 configuration register RxD5).

1 SMBus Shadow Port 1 Enable
- 0 Disable .....default
- 1 Enable generation of an interrupt or resume event on external SMBus master generation of a transaction with an address that matches the SMBus Slave Shadow Port 1 register (PCI function 4 configuration register RxD4).

0 SMBus Slave Enable
- 0 Disable .....default
- 1 Enable generation of an interrupt or resume event on external SMBus master generation of a transaction with an address that matches the SMBus host controller slave port of 10h, a command field which matches the SMBus Slave Command register (PCI function 4 configuration register RxD3), and a match of one of the corresponding enabled events in the SMBus Slave Event Register (I/O Offset 0Ah).

I/O Offset 09h – SMBus Shadow Command ..... RO

This register is used to store command values for external SMBus master accesses to the host slave and slave shadow ports.

7-0 Shadow Command..... default = 0
This field contains the command value which was received during an external SMBus master access whose address field matched the host slave address (10h) or one of the slave shadow port addresses.

I/O Offset 0B-0Ah – SMBus Slave Event ..... RW

This register is used to enable generation of interrupt or resume events for accesses to the host controller's slave port.

15-0 SMBus Slave Event..... default = 0
This field contains data bits used to compare against incoming data to the SMBus Slave Data Register (I/O Offset 0Ch). When a bit in this register is set and the corresponding bit the Slave Data register is also set, an interrupt or resume event will be generated if the command value matches the value in the SMBus Slave Command register and the access was to SMBus host address 10h.

I/O Offset 0D-0Ch – SMBus Slave Data..... RO

This register is used to store data values for external SMBus master accesses to the shadow ports or the SMBus host controller's slave port.

15-0 SMBus Slave Data..... default = 0
This field contains the data value which was transmitted during an external SMBus master access whose address field matched one of the slave shadow port addresses or the SMBus host controller slave port address of 10h.

I/O Offset 0Fh – SMBus Slave Address..... RO

7-1 SMBus Slave Address ..... bits 7-4 are fixed at 0011b

0 Reserved .....always reads 0

Hardware Monitor I/O Space Registers

The I/O base address for access to the Hardware Monitor registers is defined in Rx71-70 of function 4 PCI configuration space. The hardware monitor I/O space is enabled for I/O access by the system if Rx74[0] = 1.

Offset 10 – Digital Filter Parameter 7-0 ..... RW

Offset 11 – Digital Filter Parameter 15-8 ..... RW

Offset 12 – Digital Filter Parameter 19-16 ..... RW

Offset 13 – Analog Data 15-8 ..... RW

Offset 14 – Analog Data 7-0 ..... RW

Offset 15 – Digital Data 7-0 ..... RW

Offset 16 – Channel Counter ..... RW

Offset 17 – Data Valid & Channel Indicators ..... RW

Offset 1F –Temp Reading 1 – CPU Thermal Diode ..... RW

Offset 21 – Temp Reading 2 - UIC1 (Pin M1) ..... RW

Temperature sensor 2 is an external sensor input on pin M1 which has 10-bit resolution. The high order 8 bits are stored here and the low order 2 bits are stored in Rx49[5-4]. Only the high order 8 bits are used for comparison with the limit values in offsets 3D and 3E.

Offset 22 – Voltage Input Default – UIC2 (Pin M3) ..... RW

Offset 23 – Voltage Input Default – UIC3 (Pin M2) ..... RW

Offset 24 – Voltage Input Default – UIC4 (Pin L4) ..... RW

Offset 25 – Voltage Input Default – UIC5 (Pin L1) ..... RW

Offset 26 – Voltage Reading – 3.3V Internal VCC ..... RW

Offset 27 – Voltage Reading – 2.5V or –12V ..... RW

Offset 28 – Reserved (-5V Sense Voltage Reading)..... RW

Offset 29 – FAN1 (Pin K2) Count Reading..... RW

Offset 2A – FAN2 (Pin K3) Count Reading..... RW

The above two locations store the number of counts of the internal clock per fan revolution.

Offset 2B – High Limit – UIC2..... RW

Offset 2C – Low Limit – UIC2 ..... RW

Offset 2D – High Limit – UIC3 ..... RW

Offset 2E – Low Limit – UIC3 ..... RW

Offset 2F – High Limit – UIC4..... RW

Offset 30 – Low Limit – UIC4 ..... RW

Offset 31 – High Limit – UIC5 ..... RW

Offset 32 – Low Limit – UIC5 ..... RW

Offset 33 – High Limit – Internal 3.3V..... RW

Offset 34 – Low Limit – Internal 3.3V..... RW

Offset 35 – High Limit – 2.5V / -12V (reserved)..... RW

Offset 36 – Low Limit – 2.5V / -12V (reserved)..... RW

Offset 37 – Reserved (-5V Sense High Limit) ..... RW

Offset 38 – Reserved (-5V Sense Low Limit) ..... RW

Offset 39 – High Limit – Temperature Reading 1..... RW

Offset 3A – Low Limit – Hot Temp 1 Hysteresis..... RW

Offset 3B – FAN1 Fan Count Limit..... RW

Offset 3C – FAN2 Fan Count Limit..... RW

The above two locations store the number of counts of the internal clock per fan revolution for the low limit of the fan speed.

Offset 3D – High Limit – UIC1 (Temp 2 Default)..... RW

Offset 3E – Low Limit – UIC1 ..... RW

Offset 3F – Stepping ID Number ..... RW

Note: For high limits, comparisons are “greater than” comparisons. For low limits, comparisons are “less than or equal” comparisons.

One consequence of the above is that if high limits are set to all ones (FFh or 11111111b), interrupts are disabled for high limits (i.e., interrupts will only be generated for cases when voltages are equal to or below the low limits).

Offset 40 – Hardware Monitor Configuration .....RW

7 Initialization
- 0 Normal operation .....default
- 1 Restore power-up default values to this register, the interrupt status and mask registers, the FAN/RST#/OS# register, and the OS# Configuration / Temperature Resolution register. This bit automatically clears itself since the power-on default is 0.

6 Chassis Intrusion Reset
- 0 Normal operation .....default
- 1 Reset the Chassis Intrusion pin

5 Analog Front End Test Data Output
- 0 Normal operation .....default
- 1 Test Data Output

4 Analog Front End
- 0 Disable .....default
- 1 Enable

3 Hardware Monitor Interrupt Clear
- 0 Normal operation
- 1 Clear the hardware monitor interrupt output (does not effect the contents of the interrupt status register). Normally set during interrupt service .....default

2 Reserved ..... always reads 0

1 Hardware Monitor Interrupt Enable
- 0 Disable hardware monitor interrupt output..def
- 1 Enable hardware monitor interrupt output

0 Start
- 0 Place hardware monitor in standby mode....def
- 1 Enable startup of hardware monitor logic. At startup, limit checking functions and scanning begins. All high and low limits should be set prior to turning on this bit. Note: the hardware monitor interrupt output will not be cleared if the user writes a zero to this bit after an interrupt has occurred (the hardware monitor interrupt clear bit must be used for this purpose).

Offset 41 – Hardware Monitor Interrupt Status 1.....RO

7 Fan 2 Error
- 0 No error.....default
- 1 Fan 2 count limit exceeded

6 Fan 1 Error
- 0 No error.....default
- 1 Fan 1 count limit exceeded

5 Reserved ..... always reads 0

4 CPU Internal Tewmperature (DTD) Error
- 0 No error.....default
- 1 High or low hot temperature limit exceeded. The interrupt mode is determined by Temperature Resolution register Rx4B[1-0].

3 UIC4 5V / AFE Channel 5 Voltage Error
- 0 No error.....default
- 1 High or low limit exceeded

2 Internal (VCC/3.3V) / AFE Chan 7 Voltage Error
- 0 No error.....default
- 1 High or low limit exceeded

1 North Bridge Core / AFE Chan 4 Voltage Error
- 0 No error.....default
- 1 High or low limit exceeded

0 CPU Core / AFE Channel 3 Voltage Error
- 0 No error.....default
- 1 High or low limit exceeded

Offset 42 – Hardware Monitor Interrupt Status 2.....RO

7-5 Reserved ..... always reads 0

4 Chassis Error
- 0 No error.....default
- 1 Chassis Intrusion has gone high

3 UIC1 Temperature Error
- 0 No error.....default
- 1 High or low hot temperature limit exceeded. Interrupt mode is determined by Rx4B[3-2].

2 Reserved (-5V Error - Analog In 6) . always reads 0

1 Reserved (-12V Error – Analog In 5)always reads 0

0 UIC5 +12V Voltage Error
- 0 No error.....default
- 1 High or low limit exceeded

Note: When either status register is read, status conditions in that register are reset. In the case of voltage priority indications, if two or more voltages were out of limits, then another indication would automatically be generated if it was not handled during interrupt service. Errant voltages may be disabled in the control register until the operator has time to clear the errant condition or set the limit higher or lower.

Offset 43 – Hardware Monitor Interrupt Mask 1 ..... RW

7 Fan 2 Count Error Mask
- 0 Enable interrupt on error status bit set..... def
- 1 Disable interrupt on error status bit set

6 Fan 1 Count Error Mask
- 0 Enable interrupt on error status bit set..... def
- 1 Disable interrupt on error status bit set

5 CPU Internal Temp (DTD) Over Temp Thermal Alarm Mask
- 0 Enable temperature 1 over-temp condition to control the thermal alarm (function 4 Rx40[7] automatic CPU clock throttling must be set)def
- 1 Disable

4 CPU Internal Temp (DTD) Error Mask
- 0 Enable interrupt on error status bit set..... def
- 1 Disable interrupt on error status bit set

3 UIC4 5V / AFE-5 Voltage Error Mask
- 0 Enable interrupt on error status bit set..... def
- 1 Disable interrupt on error status bit set

2 Internal (VCC 3.3V) / AFE-7 Voltage Error Mask
- 0 Enable interrupt on error status bit set..... def
- 1 Disable interrupt on error status bit set

1 North Bridge Core / AFE-4 Voltage Error Mask
- 0 Enable interrupt on error status bit set..... def
- 1 Disable interrupt on error status bit set

0 CPU Core / AFE-3 Voltage Error Mask
- 0 Enable interrupt on error status bit set..... def
- 1 Disable interrupt on error status bit set

Offset 44 – Hardware Monitor Interrupt Mask 2 ..... RW

7-6 Reserved .....always reads 0

5 UIC1 Over Temp Thermal Alarm Mask
- 0 Enable UIC1over-temp condition to control the thermal alarm (function 4 Rx40[7] automatic CPU clock throttling must be set)def
- 1 Disable

4 Chassis Intrusion Error Mask
- 0 Enable interrupt on error status bit set..... def
- 1 Disable interrupt on error status bit set

3 UIC1 Temperature Error Mask
- 0 Enable interrupt on error status bit set..... def
- 1 Disable interrupt on error status bit set

2 Reserved (-5V Error Mask) .....always reads 0

1 Reserved (-12V Error Mask) .....always reads 0

0 UIC5 +12V Voltage Error Mask
- 0 Enable interrupt on error status bit set..... def
- 1 Disable interrupt on error status bit set

Offset 45 – Analog Front End Control (00h).....RW

7 **Internal Current Source Select**..... default = 0
6 **Oscillator Output Select**..... default = 0
5 **Clock Source Select** ..... default = 0
4 **Clock Frequency Select** ..... default = 0
3 **Negative Voltage Input Select**..... default = 0
2 **Cycle Time Select**..... default = 0
1 **Cycle Type Select**..... default = 0
0 **Data Input Select** ..... default = 0

Offset 46 – Analog Front End Test Control (00h) .....RW

7 **Built In Self Test (BIST)**
0 Disable .....default
1 Enable
6-4 **BIST Mode Select** ..... default = 0
3-1 **Reserved** ..... always reads 0
0 **Channel Setting**
0 Disable .....default
1 Enable

Offset 47 – Hardware Monitor Fan Configuration..... RW

7-6 **Fan 2 RPM Control**
00 Divide by 1
01 Divide by 2 ..... default
10 Divide by 4
11 Divide by 8
5-4 **Fan 1 RPM Control**
00 Divide by 1
01 Divide by 2 ..... default
10 Divide by 4
11 Divide by 8
3-0 **Reserved** .....always reads 0

Offset 48 – SMBus Address (2Dh) ..... RW

7 **SMBus Busy..... RO**
0 Not Busy..... default
1 Busy (SMBus Transaction In Progress)
6-0 **SMBus Address** ..... default = 0101101b

Offset 49 – Hardware Monitor Temp Low Order ValueRW

7-6 Internal Temperature Value Low-Order Bits
Upper 8 bits are stored in offset 1Fh

5-4 UIC1 Temperature Value Low-Order Bits
Upper 8 bits are stored in offset 21h

3 Over Temperature Active Low for PMU to Control Stop Clock
0 Disable .....default
1 Enable

2 Chassis Active Low Output 20 msec
0 Disable .....default
1 Enable

1 Interrupt Active High Output
0 Disable .....default
1 Enable

0 Analog Front End (AFE)
0 Disable .....default
1 Enable

Offset 4A – Universal Input Channel Config (07h)..... RW

7 Reserved .....always reads 0

6 UIC5 Configuration
0 Voltage Monitoring ..... default
1 Temperature Monitoring (NTC Thermister)

5 UIC4 Configuration
0 Voltage Monitoring ..... default
1 Temperature Monitoring (NTC Thermister)

4 UIC3 Configuration
0 Voltage Monitoring ..... default
1 Temperature Monitoring (NTC Thermister)

3 UIC2 Configuration
0 Voltage Monitoring ..... default
1 Temperature Monitoring (NTC Thermister)

2 UIC1 Configuration
0 Voltage Monitoring
1 Temp Monitoring (NTC Thermister) **... default**

1-0 Reserved ..... always reads1

Offset 4B – Temperature Configuration 1 (15h).....RW

7-4 Reserved ..... always reads 0001b
3-2 UIC1 Hot Temp Interrupt Mode Select..... def=01b
1-0 CPU DTD Hot Temp Intrpt Mode Select .. def=01b

Offset 4C – Temperature Configuration 2 (55h) .....RW

7-6 UIC5 Hot Temp Interrupt Mode Select..... def=01
5-4 UIC4 Hot Temp Interrupt Mode Select..... def=01
3-2 UIC3 Hot Temp Interrupt Mode Select..... def=01
1-0 UIC2 Hot Temp Interrupt Mode Select..... def=01

The following applies to the Interrupt Mode Select fields of the above two registers:

00 Default Interrupt Mode. An interrupt occurs if the temperature goes above the hot limit. The interrupt will be cleared once the status register is read, but will be generated again when the next conversion is completed. Interrupts will continue to be generated until the temperature goes below the hysteresis limit.
01 One-Time Interrupt Mode. An interrupt is generated if the temperrature goes above the hot limit. The interrupt will be cleared when the status register is read. Another interrupt will not be generated until the temperature first drops below the hysteresis limit.....default
10 Comparator mode. An interrupt occurs if the temperature goes above the hot limit. This interrupt remains active until the temperature goes below the hot limit (i.e., no hysteresis).
11 Default Interrupt Mode (same as 00)

Offset 4D – Temperature Resolution (00h)..... RO

7-6 UIC5 Temperature LSBs
5-4 UIC4 Temperature LSBs
3-2 UIC3 Temperature LSBs
1-0 UIC2 Temperature LSBs

Offset 4E – Over Temperature Control (0Fh)..... RW

7-4 Reserved .....always reads 0
3 UIC5 Over Temp Condition Activates OT Status
0 Enable
1 Disable ..... default
2 UIC4 Over Temp Condition Activates OT Status
0 Enable
1 Disable ..... default
1 UIC3 Over Temp Condition Activates OT Status
0 Enable
1 Disable ..... default
0 UIC2 Over Temp Condition Activates OT Status
0 Enable
1 Disable ..... default

Device 0 Function 5 & 6 Registers - AC97 Audio & Modem Codecs

The codec interface is hardware compatible with AC97 and SoundBlaster Pro. There are two sets of software accessible registers: PCI configuration registers and I/O registers. The PCI configuration registers for the **Audio Codec** are located in the **function 5** PCI configuration space of the VT8231. The PCI configuration registers for the **Modem Codec** are located in the **function 6** PCI configuration space. The I/O registers are located in the system I/O space.

PCI Configuration Space Header – Function 5 Audio

Offset 1-0 - Vendor ID ..... RO

7-0 Vendor ID ..... (1106h = VIA Technologies)

Offset 3-2 - Device ID ..... RO

7-0 Device ID (3058h = VT8231 Audio Codec)

Offset 5-4 - Command ..... RW

15-10 Reserved ..... always reads 0
9 Fast Back-to-Back ..... fixed at 0
8 SERR# Enable ..... fixed at 0
7 Address Stepping ..... fixed at 0
6 Parity Error Response ..... fixed at 0
5 VGA Palette Snoop ..... fixed at 0
4 Memory Write and Invalidate ..... fixed at 0
3 Special Cycle Monitoring ..... fixed at 0
2 Bus Master ..... fixed at 0
1 Memory Space ..... fixed at 0
0 I/O Space ..... default=0 (disabled)

Offset 7-6 - Status ..... RWC

15 Detected Parity Error ..... always reads 0
14 Signalled System Error ..... default=0
13 Received Master Abort ..... fixed at 0
12 Received Target Abort ..... fixed at 0
11 Signalled Target Abort ..... fixed at 0
10-9 DEVSEL# Timing
00 Fast
01 Medium ..... fixed
10 Slow
11 Reserved
8 Data Parity Error ..... fixed at 0
7 Fast Back-to-Back Capable ..... fixed at 0
6-5 Reserved ..... always reads 0
4 PM 1.1 ..... fixed at 1
3-0 Reserved ..... always reads 0

Offset 8 - Revision ID (nnh) ..... **RO**

7-0 Silicon Revision Code

Offset 9 - Programming Interface (00h) ..... **RO**

Offset A - Sub Class Code (01h=Audio Device) ..... **RO**

Offset B - Base Class Code (04h=Multimedia Device) ..... **RO**

Offset D - Latency Timer (00h) ..... **RO**

Offset E - Header Type (00h) ..... **RO**

Offset F - BIST (00h) ..... **RO**

Offset 13-10 - Base Address 0 – SGD Control / Status.. RW

31-16 Reserved ..... always reads 0
15-8 Base Address ..... default = 00h
7-0 00000001b (256 bytes)

Offset 17-14 - Base Address 1 – FM NMI Status ..... RW

31-16 Reserved ..... always reads 0
15-2 Base Address ..... default = 0000h
1-0 01b (4 bytes)

Offset 1B-18 - Base Address 2 – MIDI Port ..... RW

31-16 Reserved ..... always reads 0
15-2 Base Address ..... default = 0330h
1-0 01b (4 bytes)

Offset 2F-2C – Subsystem ID / Sub Vendor ID ..... RO*

*This register is RW if function 5-6 Rx42[5] = 1

Offset 34 – Capture Pointer (C0h) ..... RO

Offset 3C - Interrupt Line ..... RW

7-4 Reserved ..... always reads 0
3-0 Audio Interrupt Routing
0000 Disabled ..... default
0001 IRQ1
0010 Reserved
0011 IRQ3
0100 IRQ4
0101 IRQ5
0110 IRQ6
0111 IRQ7
1000 IRQ8
1001 IRQ9
1010 IRQ10
1011 IRQ11
1100 IRQ12
1101 IRQ13
1110 IRQ14
1111 Disabled

Offset 3D - Interrupt Pin (03h) ..... **RO**

Offset 3E - Minimum Grant (00h) ..... **RO**

Offset 3F - Minimum Latency (00h) ..... **RO**

PCI Configuration Space Header – Function 6 Modem

Offset 1-0 - Vendor ID ..... RO

7-0 Vendor ID ..... (1106h = VIA Technologies)

Offset 3-2 - Device ID ..... RO

7-0 Device ID (3068h = VT8231 Modem Codec)

Offset 5-4 - Command ..... RW

15-10 Reserved ..... always reads 0
9 Fast Back-to-Back ..... fixed at 0
8 SERR# Enable ..... fixed at 0
7 Address Stepping ..... fixed at 0
6 Parity Error Response ..... fixed at 0
5 VGA Palette Snoop ..... fixed at 0
4 Memory Write and Invalidate ..... fixed at 0
3 Special Cycle Monitoring ..... fixed at 0
2 Bus Master ..... fixed at 0
1 Memory Space ..... fixed at 0
0 I/O Space ..... default=0 (disabled)

Offset 7-6 - Status ..... RWC

15 Detected Parity Error ..... always reads 0
14 Signalled System Error ..... fixed at 0
13 Received Master Abort ..... fixed at 0
12 Received Target Abort ..... fixed at 0
11 Signalled Target Abort ..... fixed at 0
10-9 DEVSEL# Timing
00 Fast
01 Medium ..... fixed
10 Slow
11 Reserved
8 Data Parity Error ..... fixed at 0
7 Fast Back-to-Back Capable ..... fixed at 0
6-0 Reserved ..... always reads 0

Offset 8 - Revision ID (nnh) ..... **RO**

7-0 Silicon Revision Code (0 indicates first silicon)

Offset 9 - Programming Interface (00h) ..... ***RO**

Offset A - Sub Class Code (80h) ..... ***RO**

Offset B - Base Class Code (07h) ..... ***RO**

*Registers 9-B are RW if function 5-6 Rx44[5] = 1

Offset D - Latency Timer (00h) ..... **RO**

Offset E - Header Type (00h) ..... **RO**

Offset F - BIST (00h) ..... **RO**

Offset 13-10 - Base Address 0 – SGD Control / Status.. RW

31-16 Reserved ..... always reads 0
15-8 Base Address ..... default = 00h
7-0 00000001b (256 bytes)

Offset 3C - Interrupt Line ..... RW

7-4 Reserved ..... always reads 0
3-0 Audio Interrupt Routing
0000 Disabled ..... default
0001 IRQ1
0010 Reserved
0011 IRQ3
0100 IRQ4
0101 IRQ5
0110 IRQ6
0111 IRQ7
1000 IRQ8
1001 IRQ9
1010 IRQ10
1011 IRQ11
1100 IRQ12
1101 IRQ13
1110 IRQ14
1111 Disabled

Offset 3D - Interrupt Pin (03h) ..... **RO**

Offset 3E - Minimum Grant (00h) ..... **RO**

Offset 3F - Minimum Latency (00h) ..... **RO**

Function 5 & 6 Codec-Specific Configuration Registers

Offset 40 – AC97 Interface Status ..... RO

7-3 Reserved ..... always reads 0

2 Secondary Codec Ready Status ..... RO
- 0 Codec Not Ready
- 1 Codec Ready (AC97 ctrlr can access codec)

1 AC97 Codec Low-Power Status ..... RO
- 0 AC97 Codec not in low-power mode
- 1 AC97 Codec in low-power mode

0 AC97 Codec Ready Status ..... RO
- 0 Codec Not Ready
- 1 Codec Ready (AC97 ctrlr can access codec)

Offset 41 – AC Link Interface Control..... RW

7 AC-Link Interface Enable (ENAC97)
- 0 Disable..... default
- 1 Enable

6 AC-Link Reset (ACRST#)
- 0 Assert AC-Link Reset ..... default
- 1 De-assert AC-Link Reset

5 AC-Link Sync (RSYNCHI)
- 0 Release SYNC..... default
- 1 Force SYNC High

4 AC-Link Serial Data Out
- 0 Release SDO ..... default
- 1 Force SDO High

3 Variable-Sample-Rate On-Demand Mode
- 0 Disable..... default
- 1 Enable

Bit valid in function 5 only (reserved in function 6)

2 AC Link SGD Read Channel PCM Data Output
- 0 Disable..... default
- 1 Enable

Bit valid in function 5 only (reserved in function 6)

1 AC Link FM Channel PCM Data Out (SELFM)
- 0 Disable..... default
- 1 Enable

Bit valid in function 5 only (reserved in function 6)

0 AC Link SB PCM Data Output (SELSB)
- 0 Disable..... default
- 1 Enable

Bit valid in function 5 only (reserved in function 6)

Offset 42 – Function Enable.....RW (Function 5)
Offset 42 – Function Enable.....RO (Function 6)

7 MIDI PnP
- 0 MIDI Port Address Selected by Rx43[3-2] .def
- 1 MIDI Port Address Selected by IOBase2

6 Mask MIDI IRQ
- 0 Disable .....default
- 1 Enable

5 Function 5 Config Reg Rx2C Writable
- 0 F5Rx2C-2F RO.....default
- 1 F5Rx2C-2F RW

4 Gate SoundBlaster PCM When FIFO Empty
- 0 Disable .....default
- 1 Enable

3 Game Port Enable (ENGAME)
- 0 Disable .....default
- 1 Enable (200-207h)

2 FM Enable (ENFM)
- 0 Disable .....default
- 1 Enable (388-38B)

1 MIDI Enable (ENMIDI)
- 0 Disable .....default
- 1 Enable

0 SoundBlaster Enable (ENSB)
- 0 Disable .....default
- 1 Enable

Offset 43 – Plug and Play Control.....RW (Function 5)
Offset 43 – Plug and Play Control.....RO (Function 6)

7-6 SoundBlaster IRQ Select (SBIRQS[1:0])
- 00 IRQ5 .....default
- 01 IRQ7
- 10 IRQ9
- 11 IRQ10

5-4 SoundBlaster DRQ Select (SBDRQS[1:0])
- 00 DMA Channel 0
- 01 DMA Channel 1.....default
- 10 DMA Channel 2
- 11 DMA Channel 3

3-2 MIDI Decode Select (MIDIBASE)
- 00 300-303h
- 01 310-313h
- 10 320-323h
- 11 330-333h.....default

1-0 SoundBlaster Decode Select (SBBASE)
- 00 220-22Fh.....default
- 01 240-24Fh
- 10 260-26Fh
- 11 280-28Fh

Offset 44 – MC97 Interface Control..... RO (Function 5)
Offset 44 – MC97 Interface Control..... RW (Function 6)

7 AC-Link Interface for Slot-5
- 0 Disable..... default
- 1 Enable

6 Secondary Codec Support
- 0 Disable..... default
- 1 Enable

5 Function 6 Config Reg Rx9-B Writable
- 0 F6Rx9-B RO ..... default
- 1 F6Rx9-B RW

4 Function 6 Config Reg 2Ch Writable
- 0 F6Rx2C-2F RO ..... default
- 1 F6Rx2C-2F RW

3-0 Reserved .....always reads 0

Offset 48 – FM NMI Control..... RW (Function 5)
Offset 48 – FM NMI Control..... RO (Function 6)

7-3 Reserved .....always reads 0

2 FM IRQ Select
- 0 Route FM Trap interrupt to NMI ..... default
- 1 Route FM Trap interrupt to SMI

1 FM SGD Data for SoundBlaster Mixing
- 0 Disable..... default
- 1 Enable

0 FM Trap Interrupt
- 0 Enable
- 1 Disable ..... default

Offset 4B-4A – Game Port Base Address..... RW

15-0 Game Port Base Address.....default = 0200h

I/O Base 0 Registers –Audio/Modem Scatter/Gather DMA

Read / Write through function 5, R/O through function 6.

I/O Offset 0 – Audio SGD Read Channel Status ..... RWC

- **7 SGD Active (0 = completed or terminated) ..... RO**
- **6 SGD Paused ..... RO**
- **5-4 Reserved** ..... always reads 0
- **3 SGD Trigger Queued (will restart after EOL) .. RO**
- **2 SGD Stopped (write 1 to resume) ..... RWC**
- **1 SGD EOL ..... RWC**
- **0 SGD Flag ..... RWC**

I/O Offset 1 – Audio SGD Read Channel Control ..... RW

- **7 SGD Start ..... WO (always reads 0)**
  - 0 No effect
  - 1 Start SGD read channel operation
- **6 SGD Terminate ..... WO (always reads 0)**
  - 0 No effect
  - 1 Terminate SGD read channel operation
- **5-4 Reserved** .... always reads 0, writing 1 not allowed
- **3 SGD Pause**
  - 0 Release SGD read channel pause and resume the transfer from the paused line
  - 1 Pause SGD read channel operation (SGD read channel pointer stays at the current address)
- **2-0 Reserved** ..... always reads 0

I/O Offset 2 – Audio SGD Read Channel Type ..... RW

- **7 Auto-Start SGD at EOL** (1=Enable)..... default = 0
- **6 Recording FIFO** (1=Enable)..... default = 0
- **5 PCM 16-Bit Format**
  - 0 8-Bit Format.....default
  - 1 16-Bit Format
- **4 PCM Stereo Format**
  - 0 Mono Format .....default
  - 1 Stereo Format
- **3-2 Interrupt Select**
  - 00 Interrupt at PCI Read of Last Line.....default
  - 01 Interrupt at Last Sample Sent
  - 10 Interrupt at Less Than One Line to Send
  - 11 -reserved-
- **1 Interrupt on EOL @ End of Block** (1=Ena) .. def=0
- **0 Interrupt on FLAG @ End-of-Blk** (1=Ena)... def=0

I/O Offset 7-4 – Audio SGD R Ch Table Pointer Base .. RW

- **31-0 SGD Table Pointer Base Address (even addr) .... W**
  Current Pointer Address..... R

I/O Offset F-C – Audio SGD R Ch Current Count ..... RO

- **31-24 Reserved** ..... always reads 0
- **23-0 Current SGD Read Channel Count**

SGD Table Format

63	62	61	60-56	55-32	31-0
EOL	FLAG	STOP	-reserved-	Base Count [23:0]	Base Address [31:0]

I/O Offset 10 – Audio SGD Write Channel Status ..... RO

- **7 SGD Active (0 = completed or terminated)..... RO**
- **6 SGD Paused ..... RO**
- **5-4 Reserved** .....always reads 0
- **3 SGD Trigger Queued (will restart after EOL) . RO**
- **2 SGD Stopped (write 1 to resume) .....RWC**
- **1 SGD EOL .....RWC**
- **0 SGD Flag .....RWC**

I/O Offset 11 – Audio SGD Write Channel Control ..... RW

- **7 SGD Start .....WO (always reads 0)**
  - 0 No effect
  - 1 Start SGD write channel operation
- **6 SGD Terminate .....WO (always reads 0)**
  - 0 No effect
  - 1 Terminate SGD write channel operation
- **5-4 Reserved** ....always reads 0, writing 1 not allowed
- **3 SGD Pause**
  - 0 Release SGD write channel pause and resume the transfer from the paused line
  - 1 Pause SGD write channel operation (SGD write channel pointer stays at current address)
- **2-0 Reserved** .....always reads 0

I/O Offset 12 – Audio SGD Write Channel Type ..... RW

- **7 Auto-Start SGD at EOL** (1=Enable) ..... default = 0
- **6 Recording FIFO** (1=Enable) ..... default = 0
- **5 PCM 16-Bit Format**
  - 0 8-Bit Format ..... default
  - 1 16-Bit Format
- **4 PCM Stereo Format**
  - 0 Mono Format..... default
  - 1 Stereo Format
- **3-2 Reserved** .....always reads 0
- **1 Interrupt on EOL @ End of Block** (1=Ena)... def=0
- **0 Interrupt on FLAG @ End-of-Blk** (1=Ena) ... def=0

I/O Offset 17-14 – Audio SGD W Ch Table Pointer BaseRW

- **31-0 SGD Table Pointer Base Address (even addr) ... W**
  Current Pointer Address ..... R

I/O Offset 1F-1C – Audio SGD W Ch Current Count... RO

- **31-24 Reserved** .....always reads 0
- **23-0 Current SGD Write Channel Count**

EOL End Of Link. 1 indicates this block is the last of the link. If the channel "Interrupt on EOL" bit is set, then an interrupt is generated at the end of the transfer.

FLAG Block Flag. If set, transfer pauses at the end of this block. If the channel "Interrupt on FLAG" bit is set, then an interrupt is generated at the end of this block.

STOP Block Stop. If set, transfer pauses at the end of this block. To resume the transfer, write 1 to Rx?0[2].

Read / Write through function 5, R/O through function 6.

The following set of registers is dedicated for FM:

I/O Offset 20 – FM SGD Read Channel Status ..... RWC

- **7 SGD Active (0 = completed or terminated) ..... RO**
- **6 SGD Paused ..... RO**
- **5-4 Reserved** ..... always reads 0
- **3 SGD Trigger Queued (will restart after EOL) .. RO**
- **2 SGD Stopped (write 1 to resume) ..... RWC**
- **1 SGD EOL ..... RWC**
- **0 SGD Flag ..... RWC**

I/O Offset 21 – FM SGD Read Channel Control ..... RW

- **7 SGD Start ..... WO (always reads 0)**
  - 0 No effect
  - 1 Start SGD read channel operation
- **6 SGD Terminate ..... WO (always reads 0)**
  - 0 No effect
  - 1 Terminate SGD read channel operation
- **5-4 Reserved** .... always reads 0, writing 1 not allowed
- **3 SGD Pause ..... RW**
  - 0 Release SGD read channel pause and resume the transfer from the paused line
  - 1 Pause SGD read channel operation (SGD read channel pointer stays at the current address)
- **2-0 Reserved** ..... always reads 0

I/O Offset 22 – FM SGD Read Channel Type ..... RW

- **7 Auto-Start SGD at EOL** (1=Enable)..... default = 0
- **6-4 Reserved** ..... always reads 0
- **3-2 Interrupt Select**
  - 00 Interrupt at PCI Read of Last Line.....default
  - 01 Interrupt at Last Sample Sent
  - 10 Interrupt at Less Than One Line to Send
  - 11 -reserved-
- **1 Interrupt on EOL @ End of Block**
  - 0 Disable .....default
  - 1 Enable
- **0 Interrupt on FLAG @ End-of-Blk**
  - 0 Disable .....default
  - 1 Enable

I/O Offset 27-24 – FM SGD Rd Ch Table Pointer Base RW

- **31-0 SGD Table Pointer Base Address (even addr) .... W**
  Current Pointer Address ..... R

I/O Offset 2F-2C – FM SGD Rd Chan Current Count .. RO

- **31-24 Reserved** ..... always reads 0
- **23-0 Current SGD FM Read Channel Count**

Read / Write through function 6, R/O through function 5.

I/O Offset 40 – Modem SGD Read Channel Status .... RWC

7 SGD Active (0 = completed or terminated) ..... RO
6 SGD Paused ..... RO
5-4 Reserved ..... always reads 0
3 SGD Trigger Queued (will restart after EOL) .. RO
2 SGD Stopped (write 1 to resume) ..... RWC
1 SGD EOL ..... **RWC**
0 SGD Flag ..... **RWC**

I/O Offset 41 – Modem SGD Read Channel Control .... RW

7 SGD Start ..... **WO (always reads 0)**
0 No effect
1 Start SGD read channel operation
6 SGD Terminate ..... **WO (always reads 0)**
0 No effect
1 Terminate SGD read channel operation
5-4 Test (Do Not Program).....always write 0
3 SGD Pause ..... **RW**
0 Release SGD read channel pause and resume the transfer from the paused line
1 Pause SGD read channel operation (SGD read channel pointer stays at the current address)
2-0 Reserved ..... always reads 0

I/O Offset 42 – Modem SGD Read Channel Type ..... RW

7 Auto-Start SGD at EOL (1=Enable)..... default = 0
6-4 Reserved ..... always reads 0
3-2 Interrupt Select
00 Interrupt at PCI Read of Last Line.....default
01 Interrupt at Last Sample Sent
10 Interrupt at Less Than One Line to Send
11 -reserved-
1 Interrupt on EOL @ End of Block
0 Disable .....default
1 Enable
0 Interrupt on FLAG @ End-of-Blk
0 Disable .....default
1 Enable

I/O Offset 47-44 – Modem SGD R Ch Table Ptr Base .. RW

31-0 SGD Table Pointer Base Address (even addr) .... W
Current Pointer Address..... R

I/O Offset 4F-4C – Modem SGD R Ch Current Count .. RO

31-24 Reserved ..... always reads 0
23-0 Current SGD Read Channel Count

SGD Table Format

63	62	61	60-56	55-32	31-0
EOL	FLAG	STOP	-reserved-	Base Count [23:0]	Base Address [31:0]

I/O Offset 50 – Modem SGD Write Channel Status ..... RO

7 SGD Active (0 = completed or terminated)..... RO
6 SGD Paused ..... RO
5-4 Reserved .....always reads 0
3 SGD Trigger Queued (will restart after EOL) . RO
2 SGD Stopped (write 1 to resume) .....RWC
1 SGD EOL .....**RWC**
0 SGD Flag .....**RWC**

I/O Offset 51 – Modem SGD Write Channel Control... RW

7 SGD Start .....**WO (always reads 0)**
0 No effect
1 Start SGD write channel operation
6 SGD Terminate .....**WO (always reads 0)**
0 No effect
1 Terminate SGD write channel operation
5-4 Test (Do Not Program) ..... always write 0
3 SGD Pause ..... **RW**
0 Release SGD write channel pause and resume the transfer from the paused line
1 Pause SGD write channel operation (SGD write channel pointer stays at current address)
2-0 Reserved .....always reads 0

I/O Offset 52 – Modem SGD Write Channel Type ..... RW

7 Auto-Start SGD at EOL (1=Enable) ..... default = 0
6-2 Reserved .....always reads 0
1 Interrupt on EOL @ End of Block (1=Ena)... def=0
0 Interrupt on FLAG @ End-of-Blk (1=Ena) ... def=0

I/O Offset 57-54 – Modem SGD W Ch Table Ptr Base. RW

31-0 SGD Table Pointer Base Address (even addr) ... W
Current Pointer Address ..... R

I/O Offset 5F-5C – Modem SGD W Ch Current Count RO

31-24 Reserved .....always reads 0
23-0 Current SGD Write Channel Count

EOL End Of Link. 1 indicates this block is the last of the link. If the channel "Interrupt on EOL" bit is set, then an interrupt is generated at the end of the transfer.

FLAG Block Flag. If set, transfer pauses at the end of this block. If the channel "Interrupt on FLAG" bit is set, then an interrupt is generated at the end of this block.

STOP Block Stop. If set, transfer pauses at the end of this block. To resume the transfer, write 1 to Rx?0[2].

The audio / modem interface is compliant with AC97. Refer to the AC97 specification and AC97 Codec data sheets for further details.

Read / Write through both functions 5 and 6.

Offset 83-80 – AC97 Controller Command / Status .....RW

Read / Write through both functions 5 and 6.

31-30 Codec ID .....
- 00 Select Primary Codec
- 01 Select Secondary Codec
- 1x -reserved-

29-28 Reserved ..... always reads 0

27 Secondary Codec Data / Status / Index Valid RWC
- 0 Not Valid
- 1 Valid (OK to Read bits 0-23)

26 Reserved ..... always reads 0

25 Primary Codec Data / Status / Index Valid ....RWC
- 0 Not Valid
- 1 Valid (OK to Read bits 0-23)

24 AC97 Controller Busy ..... RO
- 0 Primary Codec is ready for a register access command
- 1 AC97 Controller is sending a command to the primary codec (commands are not accepted)

23 Codec Command Register Write Mode..... RW
- 0 Select Codec command register write mode
- 1 Select Codec command register read mode

22-16 Codec Command Register Index [7:1]..... RW

Index of the AC97 codec command register to access (in the attached codec). Data must be written before or at the same time as Index as writing to the index triggers the AC97 controller to access the addressed codec register over the AC-link interface.

15-0 Codec Command Register Data / Status ..... RW
- W Codec Command Register Data
- R Codec Status Register Data

Offset 87-84 – SGD Status Shadow..... RO

Read / Only through both functions 5 and 6.

31-30 Reserved .....always reads 0
29 Modem Write Chan SGD Active Shadow(Rx50[7])
28 Modem Read Chan SGD Active Shadow (Rx40[7])
27-26 Reserved .....always reads 0
25 Modem Write Chan SGD STOP Shadow(Rx50[2])
24 Modem Read Chan SGD STOP Shadow (Rx40[2])
RW

23-22 Reserved .....always reads 0
21 Modem Write Chan SGD EOL Shadow . (Rx50[1])
20 Modem Read Chan SGD EOL Shadow .. (Rx40[1])
19-18 Reserved .....always reads 0
17 Modem Write Chan SGD FLAG Shadow(Rx50[0])
16 Modem Read Chan SGD FLAG Shadow (Rx40[0])

15 Reserved .....always reads 0
14 FM Channel SGD Active Shadow ..... (Rx20[7])
13 Audio Write Chan SGD Active Shadow . (Rx10[7])
12 Audio Read Chan SGD Active Shadow .. (Rx00[7])
11 Reserved .....always reads 0
10 FM Channel SGD STOP Shadow..... (Rx20[2])
9 Audio Write Chan SGD STOP Shadow.. (Rx10[2])
8 Audio Read Chan SGD STOP Shadow... (Rx00[2])

7 Reserved .....always reads 0
6 FM Channel SGD EOL Shadow..... (Rx20[1])
5 Audio Write Chan SGD EOL Shadow.... (Rx10[1])
4 Audio Read Chan SGD EOL Shadow..... (Rx00[1])
3 Reserved .....always reads 0
2 FM Channel SGD FLAG Shadow ..... (Rx20[0])
1 Audio Write Chan SGD FLAG Shadow . (Rx10[0])
0 Audio Read Chan SGD FLAG Shadow .. (Rx00[0])

Read / Only through function 5 and Read / Write through function 6:

Offset 8B-88 – Codec GPI Interrupt Status / GPIO....RWC

31-16 GPI Interrupt Status..... RWC
- R GPI[15-0] Interrupt Status
- W 1 to clear

15-0 Codec GPIO.....RW
- R Reflect status of Codec GPI[15-0]
- W Triggers AC-Link slot-12 output to codec

Offset 8F-8C – Codec GPI Interrupt Enable..... RW

31-16 Interrupt on GPI[15-0] Change of Status.....RW
- 0 Disable
- 1 Enable

15-0 Reserved .....always reads 0

I/O Base 1 Registers – Audio FM NMI Status Registers

These registers are accessable through **function 5 only.**

I/O Offset 0 – FM NMI Status .....RO

7-2 Reserved ..... always reads 0

1-0 FM NMI Status

00 Undefined
01 OPL3 Bank 0
10 OPL3 Bank 1
11 Undefined

I/O Offset 1 – FM NMI Data.....RO

7-0 FM NMI Data

This register allows readback of the data written to the FM data port

I/O Offset 2 – FM NMI Index .....RO

7-0 FM NMI Index

This register allows readback of the data written to the FM index port

I/O Base 2 Registers – MIDI / Game Port

These registers are accessable through **function 5 only.**

I/O Offset 1-0 – MIDI Base..... RW

15-0 MIDI Port Base Address ..... default = 0330h

I/O Offset 3-2 – Game Port Base..... RW

15-0 Game Port Base Address..... default = 0200h

These registers are functional only if Rx42[6] = 1

Memory Mapped I/O APIC Registers

Memory Address FEC00000 – APIC Index .....RW

7-0 APIC Index ..... default = 00h
8-bit pointer to APIC registers.

Memory Address FEC00013-10 – APIC 32-bit Data.....RW

31-0 APIC 32-bit Data ..... default = 0000 0000h
Data for the APIC register pointed to by the APIC index

Memory Address FEC00020 – APIC IRQ Pin AssertionWO

7-5 Reserved ..... always reads 0
4-0 APIC IRQ Number.....default undefined
IRQ # for this interrupt. Valid values are 0-23 only.

Memory Address FEC00040 – APIC EOI.....WO

7-0 Redirection Entry Clear.....default undefined
When a write is issued to this register, the APIC will check this field and compare it with the vector field for each entry in the I/O redirection table. When a match is found, the "Remote IRR" bit for that I/O Redirection Entry will be cleared.

Indexed I/O APIC 32-bit Registers

Offset 0 – APIC Identification (0000 0000h)..... RW

31-28 Reserved .....always reads 0
27-24 APIC Identification.....default = 0
Software must program this value before using the APIC.
23-0 Reserved .....always reads 0

Offset 1 – APIC Version (0017 0011h) ..... RO

31-24 Reserved .....always reads 00h
23-16 Maximum Redirection.....always reads 17h
Equal to the number of APIC interrupt pins minus one. For this APIC, this value is 17h (23 decimal).
15-8 Reserved .....always reads 00h
7-0 APIC Version .....always reads 11h
The implementation version for this APIC is 11h.

Offset 2 – APIC Arbitration (0000 0000h)..... RO

31-28 Reserved .....always reads 00h
27-24 APIC Arbitration ID.....always reads 00h
23-0 Reserved .....always reads 00h

Offset 3F-10 – I/O Redirection Table

This table contains 24 registers, with one dedicated table entry for each of the 24 APIC interrupt signals. Each 64-bit register consists of two 32-bit values at consecutive index locations, with the low 32 bits at the even index and the upper 32 bits at the odd index. The default value for all registers is xxx1 xxxx xxxx xxxxh.

Format for Each I/O Redirection Table Entry:

Physical Mode (bit-11=0)

63-60 Reserved ..... always reads 0
59-56 APIC ID ..... default = undefined

Logical Mode (bit-11=1)

63-56 Destination ..... default = undefined

55-17 Reserved ..... always reads 0

16 Interrupt Masked
- 0 Not masked..... default
- 1 Masked

15 Trigger Mode
- 0 Edge Sensitive ..... default
- 1 Level Sensitive

14 Remote IRR (Level Sensitive Interrupts Only) RO
- 0 EOI message with a matching interrupt vector received from a local APIC
- 1 Level sensitive interrupt sent by IOAPIC accepted by local APIC(s)

13 Interrupt Input Pin Polarity
- 0 Active High ..... default
- 1 Active Low

12 Delivery Status ..... RO

Contains the current status of the delivery of this interrupt.
- 0 Idle (no activity)
- 1 Send Pending (the interrupt has been injected but its delivery is temporarily delayed either because the APIC bus is busy or because the receiving APIC unit cannot currently accept the interrupt)

11 Destination Mode

Determines the interpretation of bits 56-63.
- 0 Physical Mode ..... default
- 1 Lowest Priority

10-8 Delivery Mode

Specifies how the APICs listed in the destination field should act upon reception of this signal
- 000 Fixed ..... default
- 001 Logical Mode
- 010 SMI
- 011 -reserved-
- 100 NMI
- 101 INIT#
- 110 -reserved-
- 111 External INT

7-0 Interrupt Vector

Contains the interrupt vector for this interrupt. Vector values range from 10h to FEh.

Device 1 Function 0 Registers - LAN

All registers are located in the device 1 function 0 PCI configuration space of the VT8231. These registers are accessed through PCI configuration mechanism #1 via I/O address CF8/CFC.

PCI Configuration Space Header

Offset 1-0 - Vendor ID = 1106h.....RO

Offset 3-2 - Device ID = 3065h .....RO

Offset 5-4 - Command .....RW

15-10	**Reserved**	..... always reads 0
9	**Fast Back-to-Back Cycles**	..... always reads 0
8	**SERR# Enable**	..... always reads 0
7	**Address / Data Stepping**	..... always reads 0
6	**Parity Error Response**	..... always reads 0
5	**VGA Palette Snoop**	..... always reads 0
4	**Memory Write and Invalidate**	..... always reads 0
3	**Special Cycles Monitoring**	..... always reads 0
2	**Bus Master**	..... always reads 0
1	**Memory Space**	..... always reads 0
0	**I/O Space**	.....RW, default = 0

Offset 7-6 – Status (0400h) .....RO

15	**Detected Parity Error**	..... always reads 0
14	**Signalled System Error**	..... always reads 0
13	**Received Master Abort**	..... always reads 0
12	**Received Target Abort**	..... always reads 0
11	**Signalled Target Abort**	..... always reads 0
10-9	**DEVSEL# Timing**	..... fixed at 10 (slow)
8	**Data Parity Detected**	..... always reads 0
7	**Fast Back-to-Back Capable**	..... always reads 0
6-0	**Reserved**	..... always reads 0

Offset 8 - Revision ID (40h).....RO

Offset 9 - Program Interface.....RO

Offset A - Sub Class Code .....RO

Offset B - Class Code .....RO

Offset C – Cache Line Size.....RW

This register must be implemented by master devices that can generate the memory-write-and-invalidate command.

Offset D – Latency Timer.....RW

This register must be implemented as writable by any master that can burst more than two data phases.

Offset E - Header Type (00h).....RO

Offset F - BIST (00h) .....RO

Offset 13-10 – I/O Base Address (0000 0000h)..... RW

Offset 17-14 – Memory Base Address (0000 0000h)..... RW

Offset 2B-28 – Card Bus CIS Pointer (0000 0000h)..... RW

Offset 33-30 – Expansion ROM Base Address ..... RW

Offset 34 – Capabilities Offset..... RO

7-0 Capabilities Offset
Offset into the LAN function PCI space pointing to the location of the first item in the function's capability list.

LAN-Specific PCI Configuration Registers

Offset 40 – Capability ID (01h) ..... RO

7-0 Capability ID .....always reads 01h
Identifies the linked list item as being PCI power management registers

Offset 41 – Next Item Pointer (00h)..... RO

7-0 Next Item Pointer.....always reads 00h
Offset into the LAN function PCI space pointing to the location of the next item in the function's capability list.

Offset 43-42 – Power Mgmt Configuration (0002h) .....RO

15-11 Power State In Which LAN Can Assert PME# .... default = 0

1xxxx PME# can be asserted from D3C
x1xxx PME# can be asserted from D3H
xx1xx PME# can be asserted from D2
xxx1x PME# can be asserted from D1
xxxx1 PME# can be asserted from D0

10 D2 PM State
0 Not Supported.....default
1 Supported

9 D1 PM State
0 Not Supported.....default
1 Supported

8-6 PCI 3.3V Auxiliary Current Requirements .... always reads 0

5 Device-Specific Initialization ..... always reads 0

4 Reserved ..... always reads 0

3 PME# Operation Uses PCI Clock
0 No PCI clock req'd for PME# generation....def
1 PME# generated using PCI clock

2-0 Power Management Interface Revision. reads 010b
Readback of 010b indicates compliance with revision 1.1 of the power mangement interface specification

Offset 47-44 – Power Management Control / Status...RWC

31-0 Control / Status ..... default = 0000 0000h
(see Power Management Specification 1.0)

LAN I/O Registers

Offset 05-00 – Ethernet Address.....RW

Offset 06 – Receive Control (00h).....RW

7-5 Receive FIFO Threshold
- 000 64 byte .....default
- 001 32 byte
- 010 128 byte
- 011 256 byte
- 100 512 byte
- 101 768 byte
- 110 1024 byte
- 111 Store & Forward

4 Physical Address Packets Accepted
- 0 Packets are accepted if the physical address matches the node address in the Ethernet Address register .....default
- 1 All packets with physical destination address are accepted.....default

3 Broadcast Packets Accepted
- 0 Broadcast packets are rejected.....default
- 1 Broadcast packets are accepted

2 Multicast Packets Accepted
- 0 Multicast packets are rejected.....default
- 1 Multicast packets are accepted

1 Small Packets Accepted
- 0 Packets smaller than 64 bytes are rejected...def
- 1 Packets smaller than 64 bytes are accepted

0 Error Packets Accepted
- 0 Packets with receive errors are rejected.....def
- 1 Packets with receive errors are accepted

Offset 07 – Transmit Control (08h).....RW

7-5 Transmit FIFO Threshold

	100T	10T	
000	128 byte	64 byte	.....default
001	256 byte	128 byte	
010	512 byte	256 byte	
011	1024 byte	512 byte	
1xx	Store & Forward		

4 Reserved ..... always reads 0

3 Backoff Priority Selection
- 0 VIA backoff algorithm
- 1 NSC compatible backoff algorithm **.....default**

2-1 Transmit Loopback Mode
- 00 Normal .....default
- 01 Internal loopback (MAC only)
- 10 MII loopback (MAC-PHY)
- 11 223 or other loopback

0 Reserved ..... always reads 0

Offset 08 – Command 0 (00h)..... RW

7 Reserved .....always reads 0

6 Receive Poll Demand ..... default = 0
If bit-5 is set to 1, this bit may be set to 1 to poll the RD once (if set, this bit will be cleared by hardware after the polling is complete)

5 Transmit Poll Demand..... default = 0
This bit may be set to 1 to poll the TD once (if set, this bit will be cleared by hardware after the polling is complete)

4 Transmit Process
- 0 Not in transmit state ..... default
- 1 Turn on the transmit DMA state

3 Receive Process
- 0 Not in receive state..... default
- 1 Turn on the receive DMA state

2 Stop NIC
- 0 Command processing is in process..... default
- 1 No command procesing is in process

1 Start NIC
- 0 No command entered..... default
- 1 Start processing a command

0 Begin Initialization Process ..... default = 0

Offset 09 – Command 1 (00h)..... RW

7 Software Reset
- 0 Command processing is in process..... default
- 1 No command procesing is in process

6 Receive Poll Demand 1 ..... default = 0
If Rx9[5] is set to 1, this bit may be set to 1 to poll the RD once (if set, this bit will be cleared by hardware after the polling is complete)

5 Transmit Poll Demand 1..... default = 0
If Rx9[5] is set to 1, this bit may be set to 1 to poll the TD once (if set, this bit will be cleared by hardware after the polling is complete)

4 Reserved .....always reads 0

3 TX / RX Auto Polling
- 0 Enable..... default
- 1 Disable

2 Full Duplex
- 0 Set MAC to half duplex mode..... default
- 1 Set MAC to full duplex mode

1 Reserved .....always reads 0

0 Early Receive Mode
- 0 Disable..... default
- 1 Enable

Offset 0C – Interrupt Status 0 (00h) ..... RW

- **7 CRC or Miss Packet Tally Counter Overflow**
- **6 PCI Bus Error**
- **5 Receive Buffer Link Error**
- **4 Transmit Buffer Underflow**
- **3 Transmit Error (Packet Transmit Aborted)**
  Set due to excessive collision, transmit underflow, or transmit data linking error
- **2 Receive Error**
  Set due to CRC error, frame alignment error, FIFO overflow, or received data linking error
- **1 Packet Transmitted Successfully**
- **0 Packet Received Successfully**

Offset 0D – Interrupt Status 1 (00h) ..... RW

- **7 General Purpose Interrupt**
- **6 Port State Change**
- **5 Transmit Abort Due to Excessive Collisions**
- **4 Receive Buffer Full**
- **3 FIFO Overflow**
- **2 Receive FIFO Overflow**
- **1 Transmit FIFO Underflow**
- **0 Early Receive Interrupt**

Offset 0E – Interrupt Mask 0 (00h) ..... RW

Bits correspond to the bits in Interrupt Status Register 0

Offset 0F – Interrupt Mask 1 (00h) ..... RW

Bits correspond to the bits in Interrupt Status Register 1

Offset 17-10 – Multicast Address ..... RW

Offset 1B-18 – RX Address..... RW

Offset 1F-1C – TX Address ..... RW

Offset 23-20 – Receive Status (0000 0400h) ..... RW

31 Descriptor Owner (Set By Driver At Initialization)
- 0 Descriptor Owned By Host ..... default
- 1 Descriptor Owned by NIC

30-27 Extended Byte Count for Abnormal Size Ethernet Frames ..... **RO,** default = 0

26-16 Received Packet Length ..... **RO,** default = 0

15 Received Packet Successfully ..... **RO,** default = 0

14 Reserved ..... always reads 0

13 NIC Accepted Multicast Packet ..... **RO,** default = 0

12 NIC Accepted Broadcast Packet .... **RO,** default = 0

11 NIC Accepted Physical Address Packet **RO,** def = 0

10 Packet Start ..... **RO,** default = 1

9-8 Buffer Descriptor Start / End ..... **RO**
- 00 Chain Buffer Start Middle Descriptor .... default
- 01 Chain Buffer End Descriptor
- 10 Chain Buffer Start Descriptor
- 11 Single Buffer Descriptor

7 Buffer Underflow Error ..... **RO,** default = 0

6 System Error ..... **RO,** default = 0

5 Run Packet ..... **RO,** default = 0

4 Long Packet ..... **RO,** default = 0

3 FIFO Overflow Error ..... **RO,** default = 0

2 Frame Alignment Error ..... **RO,** default = 0

1 CRC Error ..... **RO,** default = 0

0 Receiver Error ..... **RO,** default = 0

Offset 27-24 – Rx Data Buffer Control (0000 0000h) .... RO

31-16 Reserved ..... always reads 0

15 Chain Buffer ..... default = 0

14-11 Frame Length Extend Fragment ..... always reads 0

10-0 Rx Data Buffer Size ..... default = 0

The receive data buffer size for this descriptor. The total byte count of the entire frame will be stored in the last descriptor.

Offset 2B-28 – Rx Data Buffer Start Address ..... RO

31-0 Rx Data Buffer Start Address

Offset 2F-2C – Rx Data Buffer Branch Address ..... RO

31-0 Rx Data Buffer Branch Address

Offset 43-40 – Transmit Status (0000 0000h) ..... RW

31 Descriptor Owner (Set By Driver At Initialization)
- 0 Descriptor Owned By Host ..... default
- 1 Descriptor Owned by NIC

30-16 Reserved ..... always reads 0

15 Transmit Error ..... **RO,** default = 0
- 0 Transmit Successful ..... default
- 1 Excessive Collisions During Transmit Attempt

14 Reserved ..... always reads 0

13 System Error ..... **RO,** default = 0

12 Invalid TD Format or Structure or TD Overflow ..... **RO,** default = 0

11 Transmit Data FIFO Underflow ..... **RO,** def = 0

10 Carrier Sense Lost During Transmit ... **RO,** def = 0

9 Out of Window Collision ..... **RO,** def = 0

8 Transmit Abort (Excessive Collisions) . **RO,** def = 0

7 CD Heartbeat ..... **RO,** def = 0

10baseT mode heartbeat collision check failure

6-5 Reserved ..... always reads 0

4 Collision Detected During Transmit ..... **RO,** def = 0

3-0 Collision Retry Count ..... **RO,** def = 0

Offset 47-44 – Tx Data Buffer Control (0000 0000h) ..... RO

31-24 Reserved ..... always reads 0

23 Send Complete Interrupt Asserted ..... default = 0

22 End of Transmit Packet ..... default = 0

21 Start of Transmit Packet ..... default = 0

20-17 Reserved ..... always reads 0

16 Disable CRC Generation ..... default = 0

15 Chain Buffer ..... default = 0

14-11 Frame Length Extend Fragment ..... always reads 0

10-0 Tx Data Buffer Size ..... default = 0

The transmit data buffer size for this descriptor. The total byte count of the entire frame will be stored in the last descriptor.

Offset 4B-48 – Tx Data Buffer Start Address ..... RO

31-0 Tx Data Buffer Start Address

Offset 4F-4C – Tx Data Buffer Branch Address ..... RO

31-4 Tx Data Buffer Branch Address

3-1 Reserved ..... always reads 0

0 Tx Interrupt Enable
- 0 Issue interrupt for this packet ..... default
- 1 No interrupt generated

Offset 6C – PHY Address (01h).....RW

7-6 MII Management Polling Timer Interval
- 00 1024 MDC Clock Cycles.....default
- 01 512 MDC Clock Cycles
- 10 128 MDC Clock Cycles
- 11 64 MDC Clock Cycles

5 Accelerate MDC Speed
- 0 Normal .....default
- 1 4x Accelerated

4-0 Extend PHY Device Address ..... default = 01h
Stored from EEPROM during power-up or EEPROM auto-reload but can be programmed by software

Offset 6D – MII Status (13h).....RW

7 PHY Reset
- 0 PHY reset not asserted.....default
- 1 PHY reset asserted

6-5 Reserved ..... always reads 0

4 PHY Option
- 0 PHY address updated from EEPROM
- 1 Use default PHY address of 0001h .....default

3 PHY Device Received Error
- 0 No error.....default
- 1 Error

2 Reserved ..... always reads 0

1 Link Failure
- 0 Link successful
- 1 Link unsuccessful (no connection) .....default

0 PHY Speed
- 0 100 MB
- 1 10 MB .....default

Offset 6E – Buffer Control 0 (00h) ..... RW

7-6 Reserved .....always reads 0

5-3 Rx FIFO Threshold Control
- 000 Determined by Rx6 Receive Ctrl Reg ... default
- ~000 Determined by bits 2-0 of this register

2-0 DMA Length
- 000 32 bytes 8 DW..... default
- 001 64 bytes 16 DW
- 010 128 bytes 32 DW
- 011 256 bytes 64 DW
- 100 512 bytes 128 DW
- 101 1024 bytes 256 DW
- 11x Store & Forward

Offset 6F – Buffer Control 1 (00h)..... RW

7-6 Reserved .....always reads 0

5-3 Rx FIFO Threshold Control
- 000 Determined by Rx7 Transmit Ctrl Reg.. default
- ~000 Determined by this register

2-0 Reserved .....always reads 0

Offset 70 – MII Management Port Command (00h)..... RW

7 Auto Polling
- 0 Disable..... default
- 1 Enable

6-0 Reserved .....always reads 0

Offset 71 – MII Mnagement Port Address (81h)..... RW

7 Polling Status
- 0 Polling
- 1 Idle ..... default

6 Polling Type
- 0 Poll One Cycle ..... default
- 1 Auto polling

5 Polling Complete
- 0 Polling not complete..... default
- 1 Polling complete (auto polling data ready)

4-0 MII Management Port Address Bits 4-0.. def = 01h

Offset 74 – EEPROM Command / Status (00h) ..... RW

7 EEPROM Program Complete .....def = 0

6 EEPROM Embedded Program Enable .....def = 0

5 Dynamically Reload EEPROM Content.....def = 0
Ethernet ID will be updated

4-0 Reserved .....always reads 0

Offset 79 – Configuration 1 (00h) ..... RW

7 Transmit Frame Queueing
- 0 Enable ..... default
- 1 Disable

6 Data Parity Generation and Checking
- 0 Enable ..... default
- 1 Disable

5 Memory Read Line Support
- 0 Enable ..... default
- 1 Disable

4 Transmit FIFO DMA Interleaved to Receiving FIFO DMA After 32 DW Transaction
- 0 Disable ..... default
- 1 Enable

3 Receive FIFO DMA Interleaved to Transmitting FIFO DMA After 32 DW Transaction
- 0 Disable ..... default
- 1 Enable

2 Memory Read Wait States
- 0 None ..... default
- 1 Insert one wait state 2222

1 Memory Write Wait States
- 0 None ..... default
- 1 Insert one wait state 2222

0 Latency Timer
- 0 Disable ..... default
- 1 Enable

Offset 7A – Configuration 2 (00h) ..... RW

7 Reserved ..... always reads 0

6 Unused BootROM Address MA
- 0 ..... default
- 1 Tie High

5 Delay Transaction for BootROM Memory Read
- 0 Disable ..... default
- 1 Enable

4-0 Reserved ..... always reads 0

Offset 7B – Configuration 3 (00h) ..... RW

7 Memory Mapped I/O Access
- 0 Disable ..... default
- 1 Enable

6 Diagnostic Mode
- 0 Disable ..... default
- 1 Enable

5 PCI Memory Read Line Capable
- 0 Not Capable ..... default
- 1 Capable

4 Reserved ..... always reads 0

3 Backoff Algorithm
- 0 Fixed ..... default
- 1 Random

2 DEC Capture Effect Solution
- 0 Disable ..... default
- 1 Enable

1 AMD Capture Effect Solution
- 0 Disable ..... default
- 1 Enable

0 Backoff Algorithm Optional
- 0 Disable ..... default
- 1 Enable

Offset 80 – Miscellaneous 1 (00h) ..... RW

7-4 Reserved ..... always reads 0
3 Full Duplex Rx Flow Control
0 Disable .....default
1 Enable
2 Half Duplex Rx Flow Control
0 Disable .....default
1 Enable
1 Soft Timer 0 Status / Start
0 Timer Counting.....default
(write 0 after time out to start timer counting)
1 Timer Timed Out
0 Soft Timer 0 Enable
0 Disable .....default
1 Enable timer to count

Offset 81 – Miscellaneous 2 (00h) ..... RW

7 Reserved ..... always reads 0
6 Force Software Reset
0 Normal .....default
1 Force Reset
5 Auxiliary Power
0 Not available .....default
1 Available
4-1 Reserved ..... always reads 0
0 Soft Timer 1 Enable
0 Disable .....default
1 Enable timer to count

Offset 83 – Sticky Hardware Control (00h)..... RW

7 Legacy WOL Status (for software reference) ...RO
0 Disable .....default
1 Enable
This bit is set per jumper on pin MD5
6-2 Reserved ..... always reads 0
1 Sticky DS1 Shadow (R/W by Software) ..... def = 0
0 Sticky DS0 Shadow (Susp Mode DS Wr Port)def = 0

Offset 84 – MII Interrupt Status (00h)..... RWC

7 Power Event Report in Test Mode ..... def = 0
6 User Defined Host Driven Interrupt ..... def = 0
5 User Defined Host Driven Interrupt ..... def = 0
4 Suspend Mode MII Polling Status Change .. def = 0
3 Transmit Data Write Buffer Queue Race .... def = 0
(will be set by transmit shutdown)
2 Reserved ..... always reads 0
1 Soft Timer 1 Timeout..... def = 0
0 Soft Timer 0 Timeout..... def = 0
All bits above: write 0 to clear the interrupt

Offset 86 – MII Interrupt Mask (00h)..... RW

7 Interrupt on MII Interrupt Status (Rx84) Bit-7
6 Interrupt on MII Interrupt Status (Rx84) Bit-6
5 Interrupt on MII Interrupt Status (Rx84) Bit-5
4 Interrupt on MII Interrupt Status (Rx84) Bit-4
3 Interrupt on MII Interrupt Status (Rx84) Bit-3
2 Reserved ..... always reads 0
1 Interrupt on MII Interrupt Status (Rx84) Bit-1
0 Interrupt on MII Interrupt Status (Rx84) Bit-0
All bits above:
0 Disable..... default
1 Enable

Offset 93 – EEPROM Checksum (00h) ..... RW

7-0 EEPROM Checksum ..... default = 0

Offset 95-94 – Suspend Mode MII Address (0000h) ..... RW

15-0 MII Address During Suspend ..... default = 0

Offset 96 – Suspend Mode PHY Address (00h) ..... RW

7-0 PHY Address During Suspend..... default = 0

Offset 99-98 – Pause Timer (0000h)..... RW

7-0 Pause Timer Value (Used for Flow Control) . def = 0

Offset 9A – Pause Status (00h) ..... RW

7-1 Reserved ..... always reads 0
0 Pause Status
0 Not paused..... default
1 Paused

Offset 9D-9C – Soft Timer 0 (0000h)..... RW

7-0 Soft Timer 0 Count Value ..... default = 0

Offset 9F-9E – Soft Timer 1 (0000h)..... RW

7-0 Soft Timer 1 Count Value ..... default = 0

Offset A0 – Wake On LAN Control Set (00h).....RW

Offset A4 – Wake On LAN Control Clear (00h).....RW

- **7 Link Off Detected**
- **6 Link On Detected**
- **5 Magic Packet Filter**
- **4 Unicast Filter**
- **3 CRC3 Pattern Match Filtering**
- **2 CRC2 Pattern Match Filtering**
- **1 CRC1 Pattern Match Filtering**
- **0 CRC0 Pattern Match Filtering**

All bits above:

0 Disable .....default
1 Enable

Offset A1 – Power Configuration Set (00h).....RW

Offset A5 – Power Configuration Clear (00h).....RW

- **7 Internal MII Interface Timing**
  - 0 Disable .....default
  - 1 Enable
- **6 Reserved** ..... always reads 0
- **5 WOL Output**
  - 0 Driven by Level .....default
  - 1 Driven By Pulse
- **4 Legacy WOL**
  - 0 Disable .....default
  - 1 Enable
- **3-2 Reserved** ..... always reads 0
- **1 Legacy WOL Status (Rx83[3] Back Door)**
  - 0 Disable .....default
  - 1 Enable
- **0 Legacy WOL Enable (Rx83[2] Back Door)**
  - 0 Disable .....default
  - 1 Enable

Offset A2 – Test Set (00h).....RW

Offset A6 – Test Clear (00h) .....RW

- **7-1 Reserved** ..... always reads 0
- **0 Power State Capabilities**
  - 0 Disable .....default
  - 1 Enable

Offset A3 – Wake On LAN Configuration Set (00h) .... RW

Offset A7 – Wake On LAN Configuration Clear (00h) RW

- **7 Force Power Management Enable over PME Enable Bit (Legacy Use Only)**
- **6 Full Duplex During Suspend**
- **5 Accept Multicast During Suspend**
- **4 Accept Broadcast During Suspend**
- **3 MDC Acceleration**
- **2 Extend Clock During Suspend**
- **1-0 Reserved** .....always reads 0

All bits above:

0 Disable..... default
1 Enable

Offset B3-B0 – Pattern CRC0 ..... RW

127-0 CRC0 Pattern ..... default = 0

Offset B7-B4 – Pattern CRC1 ..... RW

127-0 CRC1 Pattern ..... default = 0

Offset BB-B8 – Pattern CRC2..... RW

127-0 CRC2 Pattern ..... default = 0

Offset BF-BC – Pattern CRC3..... RW

127-0 CRC3 Pattern ..... default = 0

FUNCTIONAL DESCRIPTIONS

Power Management

Power Management Subsystem Overview

The power management function of the VT8231 is indicated in the following block diagram:

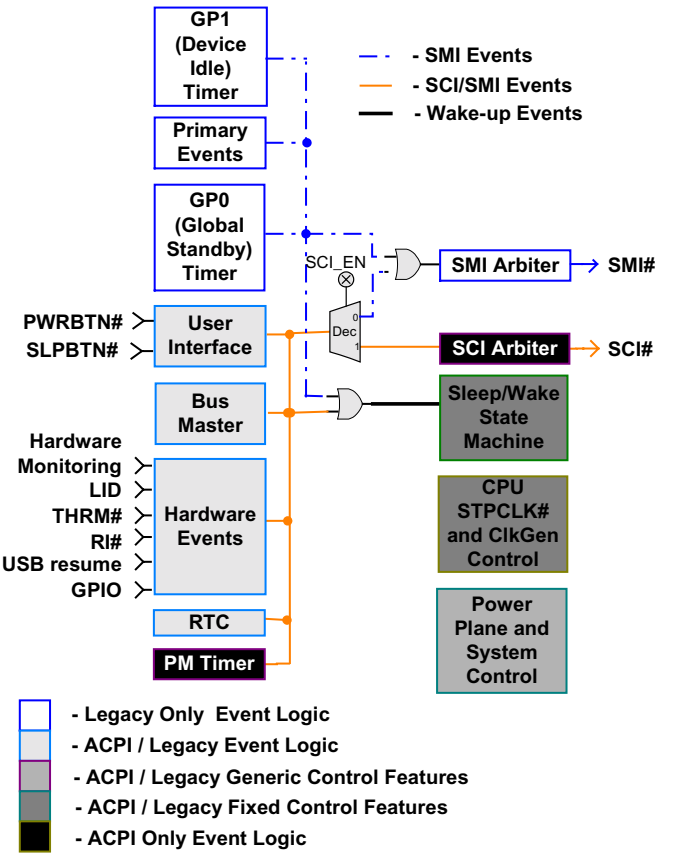

Figure 7. Power Management Subsystem Block Diagram

Refer to ACPI Specification v1.0 and APM specification v1.2 for additional information.

Processor Bus States

The VT8231 supports the complete set of C0 to C3 processor states as specified in the Advanced Configuration and Power Interface (ACPI) specification (and defined in ACPI I/O space Registers 10-15):

C0: Normal Operation

C1: CPU Halt (controlled by software).

C2: Stop Clock. Entered when the Processor Level2 register is read. The STPCLK# signal is asserted to put the processor in the Stop Grant State. The CPUSTP# signal is not asserted so that host clocks remain running. To exit this state, the chip negates STPCLK#.

C3: Suspend. Entered when the Processor Level3 register is read. In addition to STPCLK# assertion as in the C2 state, the SUSST1# (suspend status 1) signal is asserted to tell the north bridge to switch to "Suspend DRAM Refresh" mode based on the 32KHz suspend clock (SUSCLK) provided by the VT8231. If the Host Stop bit is enabled, then CPUSTP# is also asserted to stop clock generation and put the CPU into Stop Clock State. To exit this state, the chip negates CPUSTP# and allows time for the processor PLL to lock. Then the SUSST1# and STPCLK# signals are negated to resume to normal operation.

During normal operation, two mechanisms are provided to modulate CPU execution and control power consumption by throttling the duty cycle of STPCLK#:

a. Setting the Throttle Enable bit to 1, the duty cycle defined in Throttle Duty Cycle (IO space Rx10) is used.

b. THRM pin assertion enables automatic clock throttling with duty cycle pre-configured in Thermal Duty Cycle (PCI configuration Rx4C).

System Suspend States and Power Plane Control

There are three power planes inside the VT8231. The first power plane (VCCS) is always on unless turned off by the mechanical switch. The second power plane (VCC) is controlled by chip output SUSC# (also called "PSON"). The third plane (VCCRTC) is powered by the combination of the VCCS and the external battery (VBAT) for the integrated real time clock. Most of the circuitry inside the VT8231 is powered by VCC. The amount of logic powered by VCCS is very small; its main function is to control the supply of VCC and other power planes. VCCRTC is always on unless both the mechanical switch and VBAT are removed.

The VT8231 supports multiple system suspend states by configuring the Sleep Type field of ACPI I/O space (PMIO) register Rx4-5:

a) **POS (Power On Suspend):** Most devices in the system remain powered. The host bus is put into an equivalent of the C3 state. In particular, the CPU is put into the Stop Grant State or Stop Clock State depending on the setting of the Host Stop bit. SUSST1# is asserted to tell the north bridge to switch to "Suspend DRAM Refresh" mode based on the 32KHz SUSCLK provided by the VT8231. As to the PCI bus, setting the PCI Clock Run bit to 0 enables the CLKRUN protocol defined in the PCI Mobile Design Guide. That is, the PCKRUN# pin will be de-activated after the PCI bus is idle for 26 clocks. Any PCI bus masters including the north bridge may resume PCI clock operation by pulling the PCKRUN# pin low. During the PCKRUN# de-activation period, the PCISTP# pin may be activated to disable the output of the PCI clock generator if the PCI Stop bit is enabled. When the system resumes from POS, the VT8231 can optionally resume without resetting the system, can reset the processor only, or can reset the entire system. When no reset is performed, the chip only needs to wait for the clock synthesizer and processor PLL to lock before the system is resumed, which typically takes 20ms.

b) **STR (Suspend to RAM):** Power is removed from most of the system except the system DRAM. Power is supplied to the suspend refresh logic in the north bridge (VTT of VT82C598) and the suspend logic of the VT8231 (VCCS). The VT8231 provides a 32KHz suspend clock to the north bridge for it to use to continue DRAM refresh.

c) **STD (Suspend to Disk, also called Soft-off):** Power is removed from most of the system except the suspend logic of VT8231 (VCCS).

d) **Mechanical Off:** This is not a suspend state. All power in the system is removed except the RTC battery.

The suspend state is entered by setting the Sleep Enable bit to 1. Three power plane control signals (SUSA#, SUSB# and SUSC#) are provided to turn off more system power planes as the system moves to deeper power-down states, i.e., from normal operation to POS (only SUSA# asserted), to STR (both SUSA# and SUSB# asserted), and to STD (all three SUS# signals asserted). In particular, the assertion of SUSC# can be used to turn off the VCC supply to the VT8231.

One additional suspend status indicator (SUSST1#) is provided to inform the north bridge and the rest of the system of the processor and system suspend states. SUSST1# is asserted when the system enters the suspend state or the processor enters the C3 state. SUSST1# is connected to the north bridge to switch between normal and suspend-DRAM-refresh modes.

General Purpose I/O Ports

As ACPI compliant hardware, the VT8231 includes PWRBTN#, SLPBTN#, and RI# pins to implement power button, sleep button, and ring indicator functionality, respectively. Furthermore, the VT8231 offers many general-purpose I/O ports with the following capabilities:

- **I^2C/SMB Support**
- **Thermal Detect**
- **Notebook Lid Open/Close Detect**
- **Battery Low Detect**
- **Twelve General Purpose Input Ports** (multiplexed with other functions).
- **Nineteen General Purpose Output Ports** (1 dedicated and 18 multiplexed with other functions)
- **Four General Purpose Input / Output Ports** (multiplexed with other functions)

In addition, the VT8231 provides an external dedicated SMI pin (EXTSMI#). The external SMI input can be programmed to trigger an SCI or SMI at both the rising and falling edges of the corresponding input signal. Software can check the status of the input pin and take appropriate actions.

Power Management Events

Three types of power management events are supported:

1) **ACPI-required Fixed Events** defined in the PM1A Status and PM1A Enable registers. These events can trigger either SCI or SMI depending on the SCI Enable bit:
   - PWRBTN# Triggering
   - RTC Alarm
   - Sleep Button
   - ACPI Power Management Timer Carry (always SCI)
   - BIOS Release (always SCI)

2) **ACPI-aware General Purpose Function Events** defined in the GP Status and GP SCI Enable, and GP SMI Enable registers. These events can trigger either SCI or SMI depending on the setting of individual SMI and SCI enable bits:
   - External SMI triggering
   - USB Resume
   - Ring Indicator (RI#)
   - Battery Low Detect (BATLOW#)
   - Notebook Lid Open/Close Detect (LID)
   - Thermal Detect (THRM)

3) **Generic Global Events** defined in the Global Status and Global Enable registers. These registers are mainly used for SMI:
   - PCI Bus Clock Run Resume
   - Primary Interrupt Occurance
   - GP0 and GP1 Timer Time Out
   - Secondary Event Timer Time Out
   - Occurrence of Primary Events
     (defined in the Primary Activity Status and Primary Activity Enable registers)
   - Legacy USB accesses (keyboard and mouse)
   - Software SMI

System and Processor Resume Events

Depending on the system suspend state, different features can be enabled to resume the system. There are two classes of resume events:

a) VCCS-based events. Event logic resides in the VCCS plane and thus can resume the system from any suspend state. Such events include PWRBTN#, RI#, BATLOW#, LID, SMBus resume event, RTC alarm, EXTSMI#, and GP1 (EXTSMI1#).

b) VCC-Based Events. Event logic resides in the VCC plane and thus can only resume the system from the POS state. Such events include the ACPI PM timer, USB resume, and EXTSMIn#.

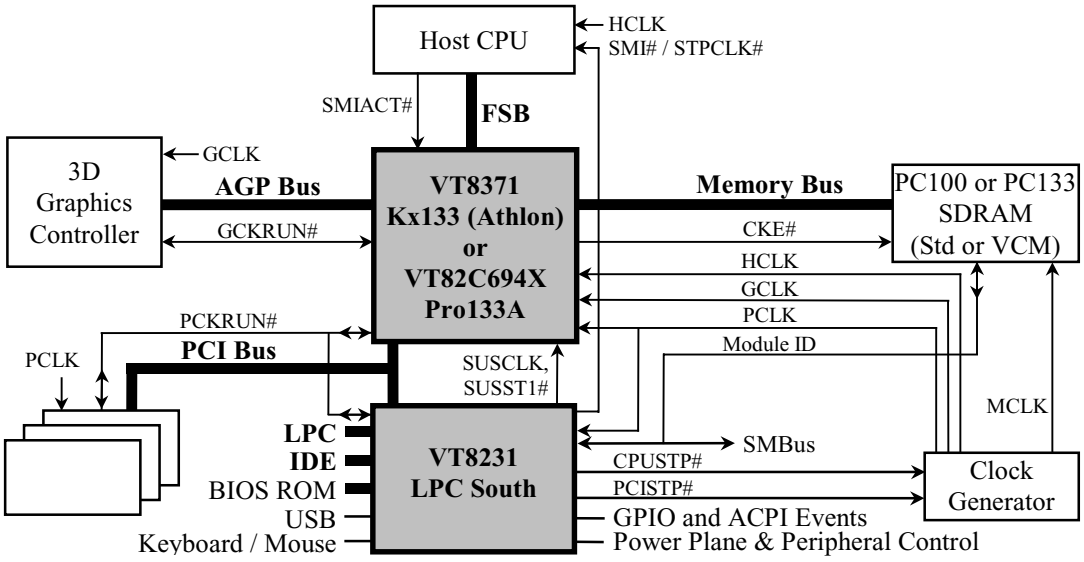

Figure 8. System Block Diagram Using the VT8231 Super South Bridge

Legacy Power Management Timers

In addition to the ACPI power management timer, the VT8231 includes the following four legacy power management timers:

GP0 Timer: general purpose timer with primary event

GP1 Timer: GP timer with peripheral event reload

Secondary Event Timer: to monitor secondary events

Conserve Mode Timer: Hardware-controlled return to standby

The normal sequence of operations for a general purpose timer (GP0 or GP1) is to

1) First program the time base and timer value of the initial count (register GP Timer Count).
2) Then activate counting by setting the GP0 Start or GP1 Start bit to one: the timer will start with the initial count and count down towards 0.
3) When the timer counts down to zero, an SMI will be generated if enabled (GP0 Timeout Enable and GP1 Timeout Enable in the Global Enable register) with status recorded (GP0 Timeout Status and GP1 Timeout Status in the Global Status register).
4) Each timer can also be programmed to reload the initial count and restart counting automatically after counting down to 0. This feature is not used in the standard VIA BIOS.

The GP0 and GP1 timers can be used just as the general purpose timers described above. However, they can also be programmed to reload the initial count by system primary events or peripheral events thus used as primary event (global standby) timer and peripheral timer, respectively. The secondary event timer is solely used to monitor secondary events.

System Primary and Secondary Events

Primary system events are distinguished in the Primary Activity Status and Primary Activity Enable registers:

Bit	Event	Trigger
7	**Keyboard Access**	I/O port 60h
6	**Serial Port Access**	I/O ports 3F8h-3FFh, 2F8h-2FFh, 3E8h-3EFh, or 2E8h-2EFh
5	**Parallel Port Access**	I/O ports 378h-37Fh or 278h-27Fh
4	**Video Access**	I/O ports 3B0h-3DFh or memory A/B segments
3	**IDE/Floppy Access**	I/O ports 1F0h-1F7h, 170h-177h, or 3F5h
2	**Reserved**	
1	**Primary Interrupts**	Each channel of the interrupt controller can be programmed to be a primary or secondary interrupt
0	**ISA Master/DMA Activity**	

Each category can be enabled as a primary event by setting the corresponding bit of the Primary Activity Enable register to 1. If enabled, the occurrence of the primary event reloads the GP0 timer if the Primary Activity GP0 Enable bit is also set to 1. The cause of the timer reload is recorded in the corresponding bit of Primary Activity Status register while the timer is reloaded. If no enabled primary event occurs during the count down, the GP0 timer will time out (count down to 0) and the system can be programmed (setting the GP0 Timeout Enable bit in the Global Enable register to one) to trigger an SMI to switch the system to a power down mode.

The VT8231 distinguishes two kinds of interrupt requests as far as power management is concerned: the primary and secondary interrupts. Like other primary events, the occurrence of a primary interrupt demands that the system be restored to full processing capability. Secondary interrupts, however, are typically used for housekeeping tasks in the background unnoticeable to the user. The VT8231 allows each channel of interrupt request to be declared as either primary, secondary, or ignorable in the Primary IRQ Channel and Secondary IRQ Channel registers. Secondary interrupts are the only system secondary events defined in the VT8231.

Like primary events, primary interrupts can be made to reload the GP0 timer by setting the PIRQ Enable bit to 1. Secondary interrupts do not reload the GP0 timer. Therefore the GP0 timer will time out and the SMI routine can put the system into power down mode if no events other than secondary interrupts are happening periodically in the background.

Primary events can be programmed to trigger an SMI (setting of the Primary Activity Enable bit). Typically, this SMI triggering is turned off during normal system operation to avoid degrading system performance. Triggering is turned on by the SMI routine before entering the power down mode so that the system may be returned to normal operation at the occurrence of primary events. At the same time, the GP0 timer is reloaded and the count down process is restarted.

Peripheral Events

Primary and secondary events define system events in general and the response is typically expressed in terms of system events. Individual peripheral events can also be monitored by the VT8231 through the GP1 timer. The following four categories of peripheral events are distinguished (via register GP Reload Enable):

Bit-7 **Keyboard Access**
Bit-6 **Serial Port Access**
Bit-4 **Video Access**
Bit-3 **IDE/Floppy Access**

The four categories are subsets of the primary events as defined in Primary Activity Enable and the occurrence of these events can be checked through a common register Primary Activity Status. As a peripheral timer, GP1 can be used to monitor one (or more than one) of the above four device types by programming the corresponding bit to one and the other bits to zero. Time out of the GP1 timer indicates no activity of the corresponding device type and appropriate action can be taken as a result.

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Min	Max	Unit	Comment
Storage Temperature	-55	125	°C	T_S
Case Operating Temperature	0	85	°C	T_C
Core Voltage	0	3.6	Volts	V_{CC}
Suspend Voltage	-0.5	V_{CC} + 0.3	Volts	V_{SUS}
USB Voltage	-0.5	V_{CC} + 0.3	Volts	V_{USB}
Hardware Monitor Voltage	-0.5	V_{CC} + 0.3	Volts	V_{HWM}
LAN MII Voltage	-0.5	V_{CC} + 0.3	Volts	V_{MII}
LAN RAM Voltage	-0.5	V_{CC} + 0.3	Volts	V_{RAM}
PLL Voltage	-0.5	V_{CC} + 0.3	Volts	V_{PLL}
Battery Voltage	-0.5	V_{CC} + 0.3	Volts	V_{BAT}
Input voltage (3.3V only inputs)	-0.5	V_{CC} + 0.3	Volts	FERR#, USBCLK, PWRBTN#, EXTSMI#, BATLOW#, FAN1, FAN2, SMBCLK, SMBDATA
Input voltage (5V tolerant inputs)	-0.5	5.5	Volts	All other inputs

Note: Stress above the conditions listed may cause permanent damage to the device. Functional operation of this device should be restricted to the conditions described under operating conditions.

DC Characteristics

T_C =0-85°C, V_{CC}=V_{CCSUS}=V_{CCHWM}=V_{CCUSB}=V_{CCMII}=V_{CCRAM}=V_{CCPLL}=3.3V ±0.15V, V_{BAT}=3.3V +0.3/-1.3V, GND=0V

Symbol	Parameter	Min	Max	Unit	Condition
V_{IL}	Input Low Voltage	-0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}+0.3	V	
V_{OL}	Output Low Voltage	-	0.45	V	I_{OL} = 4.0mA
V_{OH}	Output High Voltage	2.4	-	V	I_{OH} = -1.0mA
I_{IL}	Input Leakage Current	-	±10	uA	0 < V_{IN} < V_{CC}
I_{OZ}	Tristate Leakage Current	-	±20	uA	0.45 < V_{OUT} < V_{CC}

Power Characteristics

T_C =0-85°C, V_{CC}=V_{CCSUS}=V_{CCHWM}=V_{CCUSB}=V_{CCMII}=V_{CCRAM}=V_{CCPLL}=3.3V ±0.15V, V_{BAT}=3.3V +0.3/-1.3V, GND=0V

Symbol	Parameter	Typ	Max	Unit	Condition
I_{CC}	Power Supply Current - Core			mA	Max operating frequency
I_{CCSUS}	Power Supply Current - Suspend			mA	Max operating frequency
I_{CCHWM}	Power Supply Current - Hardware Monitor			mA	Max operating frequency
I_{CCUSB}	Power Supply Current - USB			mA	Max operating frequency
I_{CCMII}	Power Supply Current - LAN MII			mA	Max operating frequency
I_{CCRAM}	Power Supply Current - LAN RAM			mA	Max operating frequency
I_{CCPLL}	Power Supply Current - PLL			mA	Max operating frequency
P_{CHIP}	Power Dissipation		2.5	W	Max operating frequency

Output Drive

T_C = 0-85°C, V_{CC}=V_{CCSUS}=V_{CCHWM}=V_{CCUSB}=V_{CCMII}=V_{CCRAM}=V_{CCPLL}=3.3V ±0.15V, V_{BAT}=3.3V +0.3/-1.3V, GND=0V

Drive	Signal	Load	Delay
4 mA	GPO0, GPIOA, GPIOC, GPIOD, GPIOE, EECS#, EECK, EEDO, APICD[1:0], SMBCK1, SMBCK2, SMBDT1, SMBDT2, SUSA#, SUSB#, SUSC#, SUSCLK, SUSST1#, A20M#, INIT#, INTR, NMI, ROMCS#, STPCLK#, CPURST, SMI#, IGNNE#, SLP#, TXD, RTS#, DTR#, IRTX	50 pF 50 pF 50 pF 50 pF 50 pF	15 ns 15 ns 15 ns 15 ns 15 ns
8 mA	KBDT, KBCK, MSDT, MSCK, PCISTP#, CPUSTP#, SD[15:0], PDD[15:0], SDD[15:0], MDCK, MDIO, MTXENA, MTXD[3:0], PREQL#, PREQH#	50 pF 50 pF 50 pF 50 pF 30 pF	10 ns 8 ns 8 ns 8 ns 6 nS
12 mA	PDCS1#, PDCS3#, SDCS1#, SDCS3#, PDA[2:0], SDA[2:0], PDDACK#, SDDACK#, PDIOR#, PDIOW#, SDIOR#, SDIOW#	40 pF 40 pF	8 ns 8 ns
16 mA	LA[21:20], SA[19:0], MEMR#, MEMW#, IOR#, IOW#, PCIRST#	85 pF	10 ns
PCI	AD[31:0], CBE[3:0]#, FRAME#, DEVSEL#, IRDY#, TRDY#, STOP#, PAR, PCKRUN#	50 pF 50 pF	6 ns 5 ns
	LFRAME#, LAD[3:0], USBP[3:0]+/-		
	ACRST, ACSYNC, ACSDOUT, MSO		
	PCS0#, PCS1#, MCCS#, SPKR		
	DRVDEN[1:0], MTR[1:0]#, DS[1:0]#, DIR#, STEP#, HDSEL#, WDATA#, WGATE#		
	PINIT#, STROBE#, AUTOFD#, SLCTIN#, PD[7:0]		
	RTCX2		

Input Voltage

T_C = 0-85°C, V_{CC}=V_{CCSUS}=V_{CCHWM}=V_{CCUSB}=V_{CCMII}=V_{CCRAM}=V_{CCPLL}=3.3V ±0.15V, V_{BAT}=3.3V +0.3/-1.3V, GND=0V

Input Voltage	Signal
Analog	DTD+/-, UIC[5:1]
Function 0 Rx6[2] Selectable 1.5V or 2.5V Threshold	FERR#
5V	AD[31:0], CBE[3:0]#, FRAME#, DEVSEL#, IRDY#, TRDY#, STOP#, SERR#, PAR, SERIRQ, PCKRUN#
3.3V (5V Tolerant)	PGNTH#, PGNTL#, PINT[A:D]#, SA[19:0], SD[15:0], MEMR#, MEMW#, IOR#, IOW#, OSC, PDD[15:0], SDD[15:0], PDDRQ, SDDRQ, PDRDY, SDRDY, IRQ14, IRQ15, KBCK, KBDT, MSCK, MSDT, GAMED[7:0], INDEX#, TRK00#, RDATA#, DSKCHG#, WRTPRT#, PD[7:0], PINIT#, STROBE#, AUTOFD#, SLCTIN#, SLCT, ACK#, ERROR#, BUSY, PE, RXD, CTS#, DSR#, DCD#, RI#, IRRX, IRRX2, SMBCK1, SMBCK2, SMBDT1, SMBDT2, SMBALRT#, MCOL, MCRS, MDIO, MRXCLK, MRXD[3:0], MRXDV, MRXERR, MTXCLK, MSI, ACSDIN[2:0], ACBITCLK, GPIOA, GPIOC, GPIOD, GPIOE, GPI0, GPI1, PWRGD, BATLOW#, THRM
3.3 V	USBP[3:0]+/-, USBCLK, USBOC[1:0]#, LDRQ#, LAD[3:0], EEDI, PCICLK, APICCLK, WSC#, FAN1, FAN2 / SLPBTN#, PWRBTN#, RTCX1, EXTSMI#, RSMRST#, PME#, LID, RING#, CPUMISS, INTRUDER#

PACKAGE MECHANICAL SPECIFICATIONS

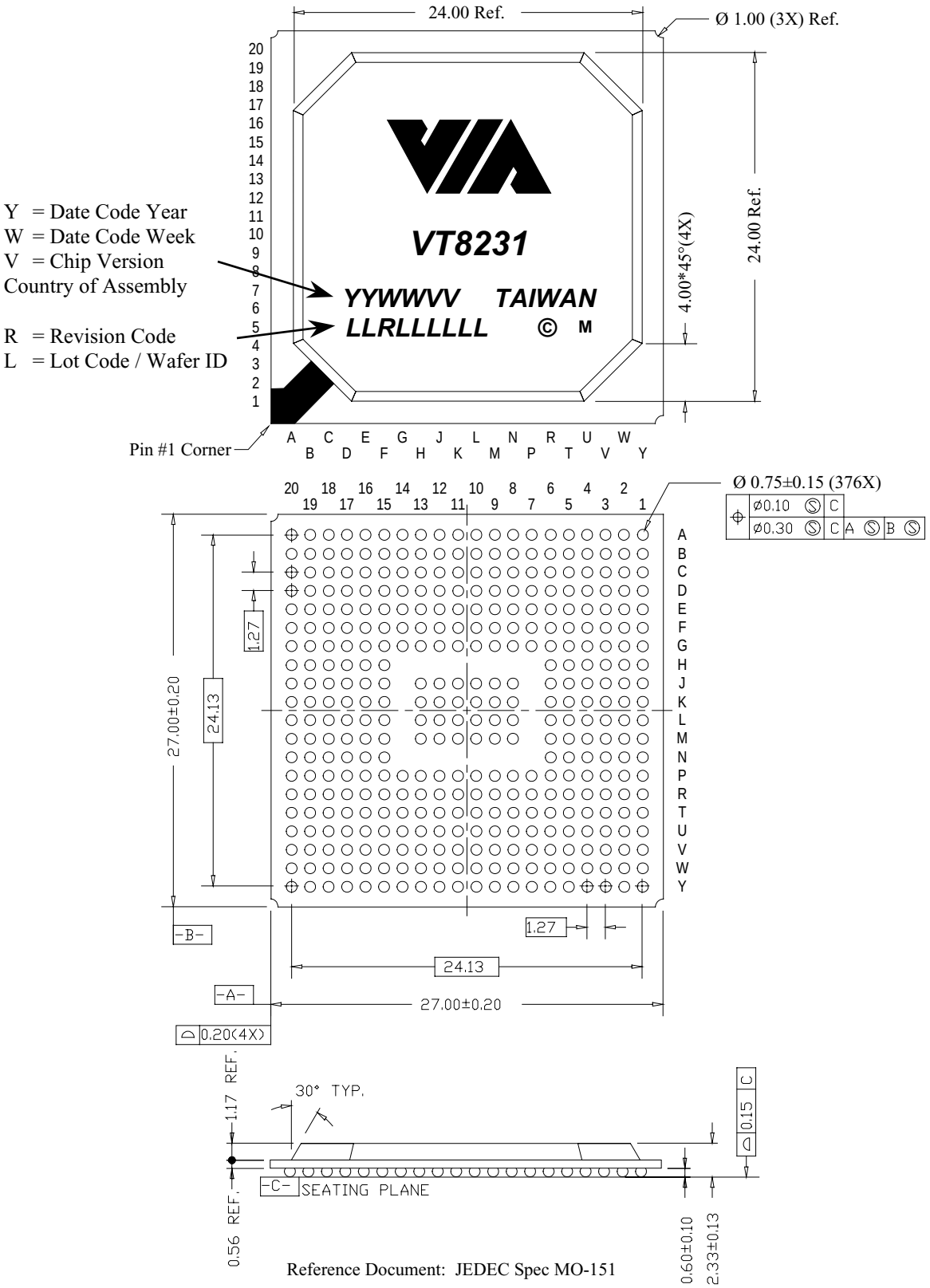

Figure 9. Mechanical Specifications – 376 Pin Ball Grid Array Package