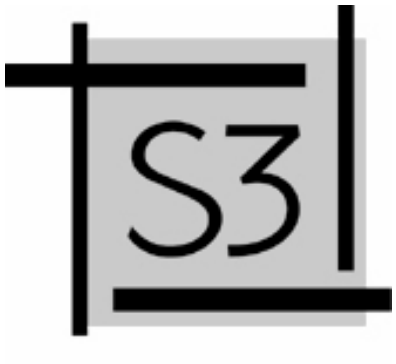

VT8605 / 86C370

66 / 100 / 133 MHz
Single-Chip Slot-1 / Socket-370 North Bridge for Desktop PC Systems with Integrated Savage4 AGP4X Graphics Core plus Advanced Memory Controller supporting PC100 / PC133 SDRAM, Virtual Channel Memory (VCM), & ESDRAM

Preliminary Revision 0.7
September 8, 1999

VIA TECHNOLOGIES, INC. **S3 INC.**

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REVISION HISTORY

Document Release	Date	Revision	Initials
0.1	7/7/99	Initial internal release	EC
0.2	7/9/99	Fixed document formatting	DH
0.3	8/17/99	Added pinouts and pin descriptions; Updated mechanical spec to 552 pins.	DH
0.4	8/19/99	Added S3 logos and changed disclaimer to "VIA and S3 Confidential" Updated feature bullets, overview, register summary tables, and register bits Added Case Temperature spec	DH
0.5	8/24/99	Added "86C370" S3 part number Fixed typos in feature bullets, overview, pin descriptions & func descriptions Fixed TVOUT pinouts and INTA# pin description	DH
0.6	8/27/99	Updated feature bullets and overview text Fixed typos in pin diagram and MD, MA, PANELD & GOP0 pin descriptions Removed incorrect note under panel interface pin descriptions Moved BISTON and DFTON in pin descriptions to group with test pins Changed pin names to match S3 docs: RED, GRN, BLU => AR, AG, AB, IRSET => RSET, SCL[2:1] => SPCLK[2:1], SDA[2:1] => SPDAT[2:1] Changed CRAA to CRB1 (global change) Fixed diagram formatting problem in Functional Description section Changed Case Operating temperature to 110 degrees and AC conditions temperature to 55 degrees Added S3 logo to mechanical specification diagram	DH
0.7	9/8/99	Changed pinouts of GPOUT, GOP0, PWROK (and added 1 GND & removed 1 VSUS25) per latest engineering pinout document (rev 1.3, 9/8/99) Fixed "VIA" capitalization in feature bullets	DH

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

VT8605 (VIA)
86C370 (S3)

66 / 100 /133 MHz
Single-Chip Slot-1 / Socket-370 North Bridge
for Desktop PC Systems with
Integrated Savage4 AGP 4X Graphics core
plus Advanced Memory Controller
supporting PC100 / PC133 SDRAM,
Virtual Channel Memory (VCM), and ESDRAM

- **Defines Integrated Solutions for Value PC Desktops**
  - High performance SMA North Bridge: Integrated VIA Apollo Pro133A and S3® Savage4™ in a single chip
  - 64-bit Advanced Memory controller supporting PC100/PC133 SDRAM, VCM, and ESDRAM
  - AGP Expansion Interface supporting AGP 4x, 2x, or 1x external AGP graphics card upgrade
  - Combines with VIA VT8231 PCI-LPC South Bridge for state-of-the-art power management
- **High Performance CPU Interface**
  - Slot 1 and Socket 370 support for Intel® Pentium® III, Pentium II, and Celeron™ processors
  - 66/100/133 MHz CPU Front Side Bus (FSB)
  - Built-in Phase Lock Loop circuitry for optimal skew control within and between clocking regions
  - Five outstanding transactions (four In-Order Queue (IOQ) plus one output latch)
  - Dynamic deferred transaction support
- **Advanced High-Performance DRAM Controller**
  - DRAM interface runs synchronous (66/66, 100/100, 133/133) mode or pseudo-synchronous (66/100, 100/66, 100/133, 133/100) mode with FSB
  - Concurrent CPU, AGP, and PCI access
  - Supports SDRAM, VCM SDRAM, and ESDRAM memory types
  - Support 3 DIMMs or 6 banks for up to 1.5 GB of DRAM (256Mb DRAM technology)
  - 64-bit data width
  - Supports maximum 8-bank interleave (8 pages open simultaneously); banks are allocated based on LRU
  - SDRAM X-1-1-1-1-1-1-1 back-to-back accesses
- **Accelerated Graphics Port (AGP) Controller**
  - AGP Specification Rev. 2.0 compliant
  - Supports 266 MHz 4x mode for AD and SBA signaling
  - Supports SideBand Addressing (SBA) mode (non-multiplexed address/data)
  - Pipelined split-transaction long-burst transfers up to 1GB/sec
  - Intelligent request reordering for maximum AGP bus utilization
  - AGP Expansion graphics override the integrated graphics by default with no SMA frame buffer

- **Integrated Savage4 2D/3D/Video Accelerator**
  - Optimized Shared Memory Architecture (SMA)
  - 2 to 32 MB frame buffer using system memory
  - Floating point triangle setup engine
  - Single cycle 128-bit 3D architecture
  - 8M triangles/second setup engine
  - 140M pixels/second trilinear fill rate
  - Full AGP 4x, including sideband addressing and execute mode
  - S3 DX6 texture compression (S3TC)
  - Next generation, 128-bit 2D graphics engine
  - High quality DVD video playback
  - Flat panel monitor support
  - 2D/3D resolutions up to 1920x1440
- **3D Rendering Features**
  - Single-pass multiple textures
  - Anisotropic filtering
  - 8-bit stencil buffer
  - 32-bit true color rendering
  - Specular lighting and diffuse shading
  - Alpha blending modes
  - Massive 2K x 2K textures
  - MPEG-2 video textures
  - Vertex and table fog
  - 16 or 24-bit Z-buffering
  - Sprite anti-aliasing, reflection mapping, texture morphing, shadows, procedural textures and atmospheric effects
- **2D Hardware Acceleration Features**
  - ROP3 Ternary Raster Operation BitBLTs
  - 8, 16, and 32 bpp mode acceleration
- **Motion Video Architecture**
  - High quality up/down scaler
  - Planar to packed format conversion
  - Motion compensation for full speed DVD playback
  - Hardware subpicture blending and highlights
  - Multiple video windows for video conferencing
  - Contrast, hue, saturation, brightness and gamma controls
  - Digital port for NTSC/PAL TV encoders
- **Flat Panel Monitor Support**
  - 12-bit digital interface for Flat Panel encoders
  - Auto-expansion and centering for VGA modes
  - Support for all resolutions up to 1280x1024
  - Digital Visual Interface (DVI) 1.0 compliant
- **Concurrent PCI Bus Controller**
  - PCI 2.1 compliant, 32-bit 3.3V PCI interface with 5V tolerant inputs
  - Supports up to 5 PCI masters
  - PCI to system memory data streaming support
  - Delay transaction from PCI master accessing DRAM
  - Symmetric arbitration between Host/PCI bus for optimized system performance

- **Advanced System Power Management Support**
  - Dynamic power down of SDRAM (CKE)
  - Independent clock stop controls for CPU / SDRAM, AGP, and PCI bus
  - PCI and AGP bus clock run and clock generator control
  - VTT suspend power plane preserves memory data
  - Suspend-to-DRAM and self-refresh power down
  - Low-leakage I/O pads
  - ACPI 1.0 and PCI Bus Power Management 1.1 compliant
- **Full Software Support**
  - Drivers for major operating systems and APIs: [Windows® 9x, Windows NT 4.0, Windows 2000, Windows 3.x, OS/2® 2.1/3.0 (Warp™), Linux, Direct3D™, DirectDraw™ and DirectShow™, OpenGL™ ICD for Windows 9x, NT, and 2000]
  - North Bridge/Chipset and Video BIOS support
- **Additional Features**
  - 300 MHz RAMDAC with Gamma Correction
  - I^2C Serial Bus and DDC Monitor Communications
  - 2.5V Core and Mixed 3.3V/5V Tolerant and GTL+ I/O
  - 35 x 35mm PBGA package with 552 balls

OVERVIEW

The VT8605 / 86C370 is a high performance, cost-effective and energy efficient SMA chip set for the implementation of AGP / PCI / LPC desktop personal computer systems with 66 MHz, 100 MHz and 133 MHz CPU host bus ("Front Side Bus") frequencies and based on 64-bit Socket-370 and Slot-1 (Intel Pentium III, Pentium-II and Celeron) super-scalar processors. VT8605 is the VIA part number and 86C370 is the S3 part number.

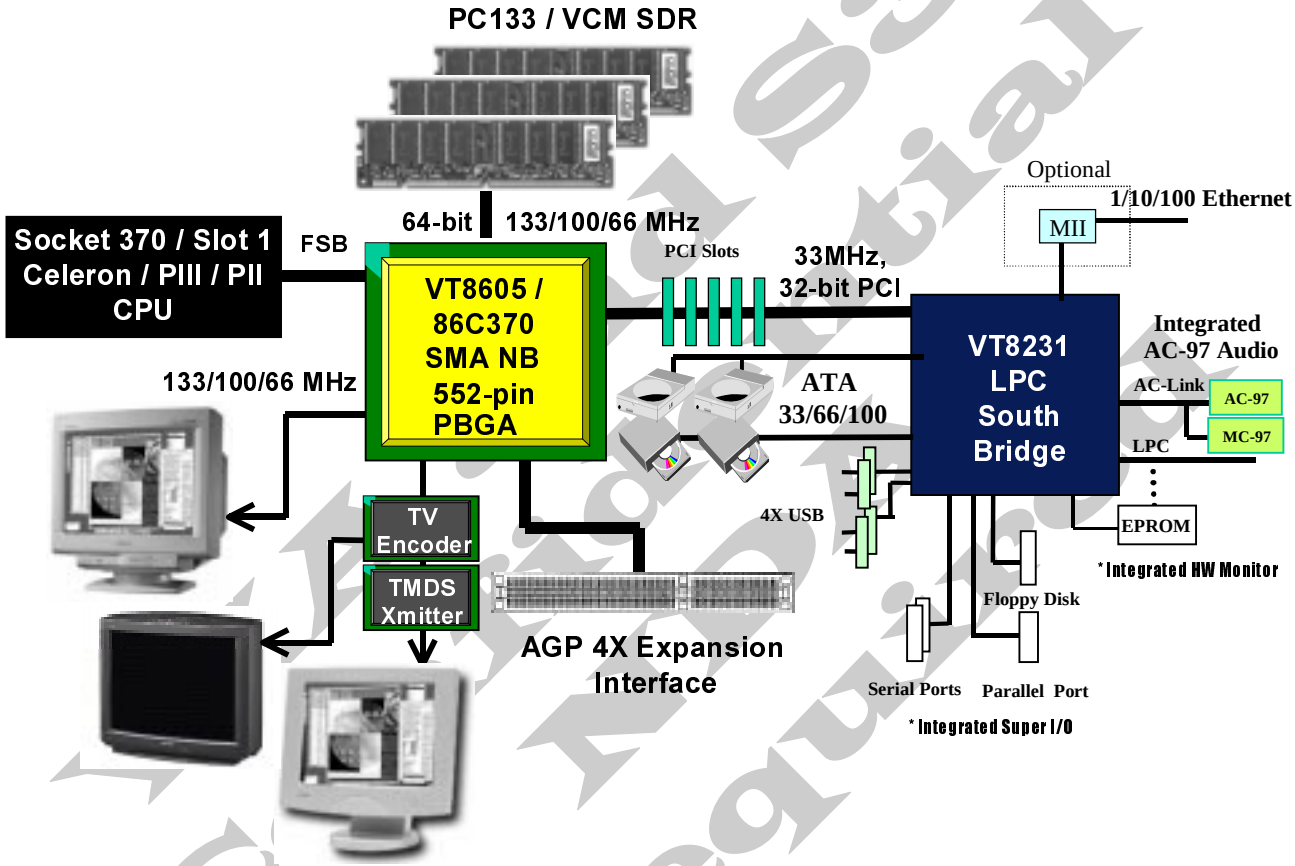


Figure 1. VT8605 / 86C370 System Block Diagram with VT8231 PCI-LPC South Bridge

The VT8605 / 86C370 integrates VIA's VT82C694X system controller and S3's Savage4 2D/3D graphics accelerator into a single 552 BGA package. The VT8605 / 86C370 SMA system controller provides superior performance between the CPU, DRAM, AGP bus, and PCI bus with pipelined, burst, and concurrent operation.

The VT8605 / 86C370 supports six banks of DRAMs up to 1.5Gbyte of system memory with 256Mbit DRAM technology. The DRAM controller supports standard Synchronous DRAM (SDRAM) and Virtual Channel SDRAM (VC SDRAM), in a flexible mix / match manner. The Synchronous DRAM interface allows zero wait state bursting between the DRAM and the data buffers at 66/100/133 MHz. The six banks of DRAM can be composed of an arbitrary mixture of 1M / 2M / 4M / 8M / 16M / 32MxN DRAMs. The DRAM controller can run at either the host CPU bus frequency (66 /100 /133 MHz) or pseudo-synchronous to the CPU bus frequency (66/100/133 MHz) with built-in PLL timing control.

The VT8605 / 86C370 system controller also supports full AGP v2.0 capability for maximum bus utilization including 1x/2x/4x mode transfers, SBA (SideBand Addressing), Flush/Fence commands, and pipelined grants. An eight level request queue plus a four level post-write request queue with thirty-two and sixteen quadwords of read and write data FIFO's respectively are included for deep pipelined and split AGP transactions. A single-level GART TLB with 16 full associative entries and flexible CPU / AGP / PCI remapping control is also provided for operation under protected mode operating environments. Both Windows-95 VXD

and Windows-98 / Windows 2000 miniport drivers are supported for interoperability with integrated Savage4 graphics, AGP Expansion graphics, and DVD-capable multimedia accelerators.

The VT8605 / 86C370 supports two 32-bit 3.3 / 5V system buses (one AGP and one PCI) that are synchronous / pseudo-synchronous to the CPU bus. The chip also contains a built-in bus-to-bus bridge to allow simultaneous concurrent operations on each bus. Five levels (doublewords) of post write buffers are included to allow for concurrent CPU and PCI operation. For PCI master operation, forty-eight levels (doublewords) of post write buffers and sixteen levels (doublewords) of prefetch buffers are included for concurrent PCI bus and DRAM/cache accesses. The chip also supports enhanced PCI bus commands such as Memory-Read-Line, Memory-Read-Multiple and Memory-Write-Invalid commands to minimize snoop overhead. In addition, advanced features are supported such as snoop ahead, snoop filtering, L1 write-back forward to PCI master, and L1 write-back merged with PCI post write buffers to minimize PCI master read latency and DRAM utilization. Delay transaction and read caching mechanisms are also implemented for further improvement of overall system performance.

The VT8605 / 86C370 also integrates S3®'s Savage4™ graphics accelerator into a single chip. The VT8605 / 86C370 brings mainstream graphics performance to the Value PC with leading-edge 2D, 3D and DVD video acceleration into a cost effective package. Based on its capabilities, the VT8605 / 86C370 is an ideal solution for the consumer, corporate desktop users and entry level professionals.

The industry's first integrated AGP 4X solution, the VT8605 / 86C370 combines AGP 4X with S3's DX6 texture compression (S3TC) and massive 2Kx2K textures to deliver unprecedented 3D performance and image quality for the Value PC desktop market.

The 352-pin VT8231 BGA PCI-LPC bridge supports four levels (doublewords) of line buffers, type F DMA transfers and delay transaction to allow efficient PCI bus utilization and (PCI-2.1 compliant). The VT8231 also includes an integrated Super I/O, integrated DS12885 style real time clock with extended 256 byte CMOS RAM, integrated master mode enhanced IDE controller with full scatter / gather capability and extension to UltraDMA-33/66/100 for 33/66/100 MB/sec transfer rate, integrated four USB interface with root hub and two function ports with built-in physical layer transceivers, Distributed DMA support, integrated AC-97 link for basic audio and HSP based modem functions, integrated hardware monitoring and OnNow / ACPI compliant advanced configuration and power management interface. VT8231 also integrated MAC and 10Mbit PHY for LAN connection. It can bypass the internal PHY with external home PNA with a 1Mbit PHY or a 10/100Mbit PHY through the MII interface.

For sophisticated power management, the VT8605 / 86C370 provides independent clock stop control for the CPU / SDRAM, PCI, and AGP buses and Dynamic CKE control for powering down of the SDRAM. A separate suspend-well plane is implemented for the SDRAM control signals for Suspend-to-DRAM operation. Coupled with the VT8231 south bridge chip, a complete power conscious PC main board can be implemented with no external TTLs.

High-Performance 3D Accelerator

Featuring a new super-pipelined 128-bit engine, the VT8605 / 86C370 utilizes a single cycle architecture that provides high performance along with superior image quality. Several new features enhance the 3D architecture, including single-pass multitexturing, full scene anti-aliasing, anisotropic filtering, and an 8-bit stencil buffer. The VT8605 / 86C370 also offers the industry's only simultaneous usage of single-pass multitexturing and single-cycle trilinear filtering – enabling stunning image quality without performance loss. the VT8605 / 86C370 further enhances image quality with true 32-bit color rendering throughout the 3D pipeline to produce more vivid and realistic images. The VT8605 / 86C370's advanced triangle setup engine provides industry leading 3D performance for a realistic user experience in games and other interactive 3D applications. The 3D engine is optimized for AGP texturing from system memory.

128-bit 2D Graphics Engine

The VT8605 / 86C370's advanced 128-bit 2D graphics engine delivers high-speed 2D acceleration for productivity applications. Several enhancements have been made to the 2D architecture to optimize SMA performance and to provide acceleration in all color depths.

DVD Playback and Video Conferencing

The VT8605 / 86C370 provides the ideal architecture for high quality MPEG-2 based DVD applications and video conferencing. For DVD playback, the VT8605 / 86C370's video accelerator offloads the CPU by performing the planar to packed format conversion and motion compensation tasks, while its enhanced scaling algorithm delivers incredible full-screen video playback. For video conferencing, the VT8605 / 86C370's multiple video windows enable a cost effective solution.

Flat Panel Desktop Monitor Support

The VT8605 / 86C370 has the capability of displaying graphics on TFT flat panel desktop monitors using a 12-bit digital interface to an external encoder. The VT8605 / 86C370 also supports autoexpansion and centering of all VGA text and graphics modes to ensure that the entire flat panel display will be utilized. All resolutions are supported up to 1280x1024. The solution is Digital Visual Interface 1.0 specification compliant.

High Screen Resolution CRT Support

	System Memory Frame Buffer Size (8MB Default)		
Resolutions Supported	**4 MB**	**8 MB**	**16/32 MB**
640x480x8/16/32	✔	✔	✔
800x600x8/16/32	✔	✔	✔
1024x768x8/16/32	✔	✔	✔
1280x1024x8	✔	✔	✔
1280x1024x16	✔	✔	✔
1280x1024x32		✔	✔
1600x1200x8	✔	✔	✔
1600x1200x16	✔	✔	✔
1600x1200x32		✔	✔
1920x1440x8	✔	✔	✔
1920x1440x16		✔	✔

PINOUTS

Figure 2. VT8605 / 86C370 Ball Diagram (Top View)

Key	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
A	GND RGB	HD61	HD60	HD54	HD55	HD59	HD40	HD27	HD39	HD34	HD33	HD24	HD7	HD13	HD2	HD4	HA29	HA30	HA20	HA19	HA5	HA11	HA14	BNR#	BPRI#	DEFER#
B	GND DAC	AB	HD62	HD58	HD63	HD48	HD41	HD45	HD36	HD28	HD25	HD21	HD3	HD9	HD10	HD6	HD0	HA24	HA17	HA10	HA16	HA6	HA7	HREQ 0#	HREQ 2#	H LOCK#
C	VCC DAC	VCC RGB	GND	HD56	HD53	GND	HD52	HD44	GND	HD31	HD26	GND	HD20	HD14	GND	HD1	CPU RST#	GND	HA22	HA21	GND	HA9	HREQ 4#	GND	HREQ 3#	HT RDY#
D	GND PLL2	GND PLL1	AG	XIN	HD50	HD57	HD47	HD51	HD37	HD22	HD29	HD23	HD30	HD18	HD5	HD8	HA26	HA27	HA25	HA28	HA15	HA13	HREQ 1#	RS1#	HIT#	RS0#
E	VCC PLL2	VCC PLL1	AR	DFT ON	XOUT	HD46	HD42	HD49	HD43	HD38	HD32	HD35	HD16	HD11	HD12	HD15	HA18	HA23	HA31	HA3	HA12	HA8	HITM#	DRDY#	DBSY#	RS2#
F	H SYNC	V SYNC	RSET	SPDAT 2	SPCLK 2	VCC3	GND	GTL REF	VCC3	GND	HD19	VCC3	GND	GND	VCC3	HD17	GND	VCC3	GTL REF	GND	VCC3	HA4	BREQ 0#	GND	ADS#	MD63
G	SPCLK 1	SPDAT 1	GND	GP OUT	PANEL VS	PANEL DE	G7	8	9	10	11	12	13	14	15	16	17	18	19	G20	GND HCK	HCLK	PLL TEST	C RESET	MD31	MD62
H	PANEL DET	PANEL D0	BIST ON	PANEL HS	PANEL D4	VCC3	H	GFX					CPU	Pins						H	GND	VCC HCK	MD30	MD61	MD29	MD60
J	PANEL D1	PANEL D2	GOP 0	PANEL D3	PANEL D5	GND	J	Pins	VCC3	VCC3	VCC 25	VCC 25	VCC3	VCC3	VCC 25	VCC 25	VCC3	VCC3		J	VCC3	MD28	MD59	GND	MD27	MD58
K	PANEL D6	PANEL D7	PANEL D8	PANEL D10	GNT 4#	PANEL CLK	K		VCC3	K10	11	12	13	14	15	16	K17	VCC3		K	VCC3	MD26	MD57	MD25	MD56	MD24
L	PANEL D9	PANEL D11	GND	GNT 3#	GNT 2#	VCC3	L		VCC 25	L	GND	GND	GND	GND	GND	GND	L	VCC 25		L	GND	MD55	MD23	MD54	MD22	MD53
M	GNT 1#	GNT 0#	REQ 0#	REQ 1#	PGNT#	GND	M		VCC 25	M	GND	GND	GND	GND	GND	GND	M	VCC 25		M	VCC3	MD21	MD52	GND	MD51	MD20
N	WSC#	REQ 4#	REQ 3#	VCC3	REQ 2#	PREQ#	N	PCI	VCC3	N	GND	GND	GND	GND	GND	GND	N	VCC3	DRAM	N	MD50	MD19	MD49	MD18	MD48	MD17
P	AD31	AD30	AD29	AD28	AD27	VCC3	P	Pins	VCC3	P	GND	GND	GND	GND	GND	GND	P	VCC3	Pins	P	GND MCK	VCC MCK	MCLK F	MD16	DQM 7	DQM 6
R	AD25	AD26	GND	AD24	CBE3#	GND	R		VCC 25	R	GND	GND	GND	GND	GND	GND	R	VCC3		R	VCC3	MCLK	DQM 2	DQM 3	CS 0#	CS 1#
T	AD23	AD22	AD21	AD20	AD19	AD18	T		VCC 25	T	GND	GND	GND	GND	GND	GND	T	VCC 25		T	GND	CS 2#	VCC3	GND	CS 3#	CS 4#
U	AD17	AD16	CBE2#	FRM#	IRDY#	PCLK	U		VCC3	U10	11	12	13	14	15	16	U17	VCC 25		U	CS 5#	SRAS A#	CKE0 SRASB#	CKE1 SRASC#	SCAS A#	CKE2 SCASB
V	TRDY#	DEV SEL#	STOP#	LOCK#	SERR#	VCC3	V		VCCQ	VCC 25	VCCQ	VCCQ	VCC 25	VCCQ	VCC 25	VCCQ	VCC3	VCC3		V	VCC3	SUST#	CKE3 SCASC#	SWE A#	CKE4 SWEB#	CKE5 SWEC#
W	PAR	CBE1#	GND	AD15	AD10	GND	W						AGP	Pins						W	VSUS 25	PWR OK	MA0	MA1#	MA2	MA3
Y	AD13	AD12	AD11	AD14	PCK RUN#	GND	Y7	8	9	10	11	12	13	14	15	16	17	18	19	Y20	GND	MA4	MA5	GND	MA6	MA7
AA	CBE0#	AD8	AD7	AD6	AD9	VCC3	VCCQ	GND	GD26	VCCQ	GND	VCCQ	GND	VCC GCK	VCCQ	GND	VCC QQ	VCCQ	GND	VCC3	VCC3	MA8	MA9	MA10	MA11	MA12
AB	AD5	AD2	GND	AD1	AD4	G PIPE#	SBA5	GD30	GD22	GD20	GBE2#	GD16	GD11	GCLK	GND GCK	GD12	GND QQ	N COMP	MD2	MD36	MD38	MA13	MA14	DQM 0	DQM 1	DQM 4
AC	AD3	INT A#	AD0	RE SET#	VCCQ	SBA6	GD29	VCCQ	GD21	GD18	VCCQ	GD15	GFRM#	VCCQ	GCLK F	GD9	VCCQ	P COMP	MD33	MD4	MD6	MD40	DQM 5	MD47	MD15	MD46
AD	G REQ#	G GNT#	ST0	SBA0	SBS	SBA4	GD31	GD24	GD23	GD17	GD SEL#	GT RDY#	GD13	GD10	GD8	GD5	GD4	GD1	MD1	MD35	GND	MD8	MD10	GND	MD14	MD45
AE	ST2	GND	SBA1	SBA2	GND	SBA7	GD27	GND	GDS1#	GD19	GND	G STOP#	GPAR GCKR#	GND	GDS0	GD7	GND	GD2	MD32	MD3	MD37	MD39	MD41	MD11	MD13	MD44
AF	ST1	G RBF#	G WBF#	SBA3	SBS#	GD28	GD25	GDS1	GBE3#	AGP REF	GI RDY#	GBE1#	GD14	GBE0#	GDS0#	GD6	GD3	GD0	MD0	MD34	MD5	MD7	MD9	MD42	MD43	MD12

Figure 3. VT8605 / 86C370 Pin List (Numerical Order)

Pin #		Pin Name	Pin #		Pin Name	Pin #		Pin Name	Pin #		Pin Name	Pin #		Pin Names	Pin #		Pin Name
A01	**P**	**GNDRGB**	D03	O	AG	G05	O	PANELVS / TVVS	P01	IO	AD31	Y23	O	MA05 / strap	AC25	IO	MD15
A02	IO	HD61	D04	I	XIN	G06	O	PANELDE / TVCLK	P02	IO	AD30	**Y24**	**P**	**GND**	AC26	IO	MD46
A03	IO	HD60	D05	IO	HD50	**G21**	**P**	**GNDHCK**	P03	IO	AD29	Y25	O	MA06 / strap	AD01	I	GREQ#
A04	IO	HD54	D06	IO	HD57	G22	I	HCLK	P04	IO	AD28	Y26	O	MA07 / strap	AD02	O	GGNT#
A05	IO	HD55	D07	IO	HD47	G23	I	PLLTEST	P05	IO	AD27	AA01	IO	CBE0#	AD03	O	ST0
A06	IO	HD59	D08	IO	HD51	G24	O	CRESET	**P06**	**P**	**VCC3**	AA02	IO	AD08	AD04	I	SBA0
A07	IO	HD40	D09	IO	HD37	G25	IO	MD31	**P21**	**P**	**GNDMCK**	AA03	IO	AD07	AD05	I	SBS
A08	IO	HD27	D10	IO	HD22	G26	IO	MD62	**P22**	**P**	**VCCMCK**	AA04	IO	AD06	AD06	I	SBA4
A09	IO	HD39	D11	IO	HD29	H01	I	PANELDET / TVD11	P23	I	MCLKF	AA05	IO	AD09	AD07	IO	GD31
A10	IO	HD34	D12	IO	HD23	H02	O	PANELD00 / TVD0	P24	IO	MD16	**AA06**	**P**	**VCC3**	AD08	IO	GD24
A11	IO	HD33	D13	IO	HD30	H03	I	BISTON	P25	O	DQM7 / CAS7#	**AA07**	**P**	**VCCQ**	AD09	IO	GD23
A12	IO	HD24	D14	IO	HD18	H04	O	PANELHS / TVHS	P26	O	DQM6 / CAS6#	**AA08**	**P**	**GND**	AD10	IO	GD17
A13	IO	HD07	D15	IO	HD05	H05	O	PANELD04 / TVD4	R01	IO	AD25	AA09	IO	GD26	AD11	IO	GDSEL#
A14	IO	HD13	D16	IO	HD08	**H06**	**P**	**VCC3**	R02	IO	AD26	**AA10**	**P**	**VCCQ**	AD12	IO	GTRDY#
A15	IO	HD02	D17	IO	HA26	**H21**	**P**	**GND**	**R03**	**P**	**GND**	**AA11**	**P**	**GND**	AD13	IO	GD13
A16	IO	HD04	D18	IO	HA27	**H22**	**P**	**VCCHCK**	R04	IO	AD24	**AA12**	**P**	**VCCQ**	AD14	IO	GD10
A17	IO	HA29	D19	IO	HA25	H23	IO	MD30	R05	IO	CBE3#	**AA13**	**P**	**GND**	AD15	IO	GD8
A18	IO	HA30	D20	IO	HA28	H24	IO	MD61	**R06**	**P**	**GND**	**AA14**	**P**	**VCCGCK**	AD16	IO	GD5
A19	IO	HA20	D21	IO	HA15	H25	IO	MD29	**R21**	**P**	**VCC3**	**AA15**	**P**	**VCCQ**	AD17	IO	GD4
A20	IO	HA19	D22	IO	HA13	H26	IO	MD60	R22	O	MCLK	**AA16**	**P**	**GND**	AD18	IO	GD1
A21	IO	HA05	D23	IO	HREQ1#	J01	O	PANELD01 / TVD1	R23	O	DQM2 / CAS2#	**AA17**	**P**	**VCCQQ**	AD19	IO	MD01
A22	IO	HA11	D24	IO	RS1#	J02	O	PANELD02 / TVD2	R24	O	DQM3 / CAS3#	**AA18**	**P**	**VCCQ**	AD20	IO	MD35
A23	IO	HA14	D25	IO	HIT#	J03	O	GOP0	R25	O	CS0# / RAS0#	**AA19**	**P**	**GND**	**AD21**	**P**	**GND**
A24	IO	BNR#	D26	IO	RS0#	J04	O	PANELD03 / TVD3	R26	O	CS1# / RAS1#	**AA20**	**P**	**VCC3**	AD22	IO	MD08
A25	IO	BPRI#	**E01**	**P**	**VCCPLL2**	J05	O	PANELD05 / TVD5	T01	IO	AD23	**AA21**	**P**	**VCC3**	AD23	IO	MD10
A26	IO	DEFER#	**E02**	**P**	**VCCPLL1**	**J06**	**P**	**GND**	T02	IO	AD22	AA22	O	MA08 / strap	**AD24**	**P**	**GND**
B01	**P**	**GNDDAC**	E03	O	AR	**J21**	**P**	**VCC3**	T03	IO	AD21	AA23	O	MA09 / strap	AD25	IO	MD14
B02	O	AB	E04	I	DFTON	J22	IO	MD28	T04	IO	AD20	AA24	O	MA10 / strap	AD26	IO	MD45
B03	IO	HD62	E05	O	XOUT	J23	IO	MD59	T05	IO	AD19	AA25	O	MA11 / strap	AE01	O	ST2
B04	IO	HD58	E06	IO	HD46	**J24**	**P**	**GND**	T06	IO	AD18	AA26	O	MA12 / strap	**AE02**	**P**	**GND**
B05	IO	HD63	E07	IO	HD42	J25	IO	MD27	**T21**	**P**	**GND**	AB01	IO	AD05	AE03	I	SBA1
B06	IO	HD48	E08	IO	HD49	J26	IO	MD58	T22	O	CS2# / RAS2#	AB02	IO	AD02	AE04	I	SBA2
B07	IO	HD41	E09	IO	HD43	K01	O	PANELD06 / TVD6	**T23**	**P**	**VCC3**	**AB03**	**P**	**GND**	**AE05**	**P**	**GND**
B08	IO	HD45	E10	IO	HD38	K02	O	PANELD07 / TVD7	**T24**	**P**	**GND**	AB04	IO	AD01	AE06	I	SBA7
B09	IO	HD36	E11	IO	HD32	K03	O	PANELD08 / TVD8	T25	O	CS3# / RAS3#	AB05	IO	AD04	AE07	IO	GD27
B10	IO	HD28	E12	IO	HD35	K04	O	PANELD10 / TVD10	T26	O	CS4# / RAS4#	AB06	I	GPIPE#	**AE08**	**P**	**GND**
B11	IO	HD25	E13	IO	HD16	K05	O	GNT4#	U01	IO	AD17	AB07	I	SBA5	AE09	IO	GDS1#
B12	IO	HD21	E14	IO	HD11	K06	O	PANELCLK / TVCKR	U02	IO	AD16	AB08	IO	GD30	AE10	IO	GD19
B13	IO	HD03	E15	IO	HD12	**K21**	**P**	**VCC3**	U03	IO	CBE2#	AB09	IO	GD22	**AE11**	**P**	**GND**
B14	IO	HD09	E16	IO	HD15	K22	IO	MD26	U04	IO	FRAME#	AB10	IO	GD20	AE12	IO	GSTOP#
B15	IO	HD10	E17	IO	HA18	K23	IO	MD57	U05	IO	IRDY#	AB11	IO	GBE2#	AE13	IO	GPAR/GCKRUN#
B16	IO	HD06	E18	IO	HA23	K24	IO	MD25	U06	I	PCLK	AB12	IO	GD16	**AE14**	**P**	**GND**
B17	IO	HD00	E19	IO	HA31	K25	IO	MD56	U21	O	CS5# / RAS5#	AB13	IO	GD11	AE15	IO	GDS0
B18	IO	HA24	E20	IO	HA03	K26	IO	MD24	U22	O	SRASA#	AB14	O	GCLK	AE16	IO	GD7
B19	IO	HA17	E21	IO	HA12	L01	O	PANELD09 / TVD9	U23	O	CKE0 / SRASB#	**AB15**	**P**	**GNDGCK**	**AE17**	**P**	**GND**
B20	IO	HA10	E22	IO	HA08	L02	O	PANELD11 / TVBL#	U24	O	CKE1 / SRASC#	AB16	IO	GD12	AE18	IO	GD2
B21	IO	HA16	E23	I	HITM#	**L03**	**P**	**GND**	U25	O	SCASA#	**AB17**	**P**	**GNDQQ**	AE19	IO	MD32
B22	IO	HA06	E24	IO	DRDY#	L04	O	GNT3#	U26	O	CKE2 / SCASB#	AB18	I	NCOMP	AE20	IO	MD03
B23	IO	HA07	E25	IO	DBSY#	L05	O	GNT2#	V01	IO	TRDY#	AB19	IO	MD02	AE21	IO	MD37
B24	IO	HREQ0#	E26	IO	RS2#	**L06**	**P**	**VCC3**	V02	IO	DEVSEL#	AB20	IO	MD36	AE22	IO	MD39
B25	IO	HREQ2#	F01	O	HSYNC	**L21**	**P**	**GND**	V03	IO	STOP#	AB21	IO	MD38	AE23	IO	MD41
B26	I	HLOCK#	F02	O	VSYNC	L22	IO	MD55	V04	IO	LOCK#	AB22	O	MA13 / strap	AE24	IO	MD11
C01	**P**	**VCCDAC**	F03	A	RSET	L23	IO	MD23	V05	IO	SERR#	AB23	O	MA14 / strap	AE25	IO	MD13
C02	**P**	**VCCRGB**	F04	IO	SPDAT2	L24	IO	MD54	**V06**	**P**	**VCC3**	AB24	O	DQM0 / CAS0#	AE26	IO	MD44
C03	**P**	**GND**	F05	IO	SPCLK2	L25	IO	MD22	**V21**	**P**	**VCC3**	AB25	O	DQM1 / CAS1#	AF01	O	ST1
C04	IO	HD56	**F06**	**P**	**VCC3**	L26	IO	MD53	V22	I	SUST#	AB26	O	DQM4 / CAS4#	AF02	I	GRBF#
C05	IO	HD53	**F07**	**P**	**GND**	M01	O	GNT1#	V23	O	CKE3 / SCASC#	AC01	IO	AD03	AF03	I	GWBF#
C06	**P**	**GND**	**F08**	**P**	**GTLREF**	M02	O	GNT0#	V24	O	SWEA#	AC02	O	INTA#	AF04	I	SBA3
C07	IO	HD52	**F09**	**P**	**VCC3**	M03	I	REQ0#	V25	O	CKE4 / SWEB#	AC03	IO	AD00	AF05	I	SBS#
C08	IO	HD44	**F10**	**P**	**GND**	M04	I	REQ1#	V26	O	CKE5 / SWEC#	AC04	I	RESET#	AF06	IO	GD28
C09	**P**	**GND**	F11	IO	HD19	M05	O	PGNT#	W01	IO	PAR	**AC05**	**P**	**VCCQ**	AF07	IO	GD25
C10	IO	HD31	**F12**	**P**	**VCC3**	**M06**	**P**	**GND**	W02	IO	CBE1#	AC06	I	SBA6	AF08	IO	GDS1
C11	IO	HD26	**F13**	**P**	**GND**	**M21**	**P**	**VCC3**	**W03**	**P**	**GND**	AC07	IO	GD29	AF09	IO	GBE3#
C12	**P**	**GND**	**F14**	**P**	**GND**	M22	IO	MD21	W04	IO	AD15	**AC08**	**P**	**VCCQ**	**AF10**	**P**	**AGPREF**
C13	IO	HD20	**F15**	**P**	**VCC3**	M23	IO	MD52	W05	IO	AD10	AC09	IO	GD21	AF11	IO	GIRDY#
C14	IO	HD14	F16	IO	HD17	**M24**	**P**	**GND**	**W06**	**P**	**GND**	AC10	IO	GD18	AF12	IO	GBE1#
C15	**P**	**GND**	**F17**	**P**	**GND**	M25	IO	MD51	**W21**	**P**	**VSUS25**	**AC11**	**P**	**VCCQ**	AF13	IO	GD14
C16	IO	HD01	**F18**	**P**	**VCC3**	M26	IO	MD20	W22	I	PWROK	AC12	IO	GD15	AF14	IO	GBE0#
C17	O	CPURST#	**F19**	**P**	**GTLREF**	N01	O	WSC#	W23	O	MA00 / strap	AC13	IO	GFRM#	AF15	IO	GDS0#
C18	**P**	**GND**	**F20**	**P**	**GND**	N02	I	REQ4#	W24	O	MA01 / strap	**AC14**	**P**	**VCCQ**	AF16	IO	GD6
C19	IO	HA22	**F21**	**P**	**VCC3**	N03	I	REQ3#	W25	O	MA02 / strap	AC15	I	GCLKF	AF17	IO	GD3
C20	IO	HA21	F22	IO	HA04	**N04**	**P**	**VCC3**	W26	O	MA03 / strap	AC16	IO	GD9	AF18	IO	GD0
C21	**P**	**GND**	F23	O	BREQ0#	N05	I	REQ2#	Y01	IO	AD13	**AC17**	**P**	**VCCQ**	AF19	IO	MD00
C22	IO	HA09	**F24**	**P**	**GND**	N06	I	PREQ#	Y02	IO	AD12	AC18	I	PCOMP	AF20	IO	MD34
C23	IO	HREQ4#	F25	IO	ADS#	N21	IO	MD50	Y03	IO	AD11	AC19	IO	MD33	AF21	IO	MD05
C24	**P**	**GND**	F26	IO	MD63	N22	IO	MD19	Y04	IO	AD14	AC20	IO	MD04	AF22	IO	MD07
C25	IO	HREQ3#	G01	IO	SPCLK1	N23	IO	MD49	Y05	IO	PCKRUN#	AC21	IO	MD06	AF23	IO	MD09
C26	IO	HTRDY#	G02	IO	SPDAT1	N24	IO	MD18	**Y06**	**P**	**GND**	AC22	IO	MD40	AF24	IO	MD42
D01	**P**	**GNDPLL2**	**G03**	**P**	**GND**	N25	IO	MD48	**Y21**	**P**	**GND**	AC23	O	DQM5 / CAS5#	AF25	IO	MD43
D02	**P**	**GNDPLL1**	G04	O	GPOUT	N26	IO	MD17	Y22	O	MA04 / strap	AC24	IO	MD47	AF26	IO	MD12

Center **VCC3** Pins (16 pins): **J9-10,13-14,17-18, K9,18, N9,18, P9,18, R18, U9, V17-18**
Center **VCC25** Pins (15 pins): **J11-12,15-16, L9,18, M9,18, R9, T9,18, U18, V10,13,15**
Center **GND** Pins (36 pins): **L11-16, M11-16, N11-16, P11-16, R11-16, T11-16**
Center **VCCQ** Pins (5 pins): **V9,11-12,14,16**

Figure 4. VT8605 / 86C370 Pin List (Alphabetical Order)

Pin #		Pin Name	Pin #		Pin Name	Pin #		Pin Name	Pin #		Pin Name	Pin #		Pin Names	Pin #		Pin Name
B02	O	AB	AD18	IO	GD1	**AE05**	**P**	**GND**	B12	IO	HD21	AF22	IO	MD07	G23	I	PLLTEST
AC03	IO	AD00	AE18	IO	GD2	**AE08**	**P**	**GND**	D10	IO	HD22	AD22	IO	MD08	N06	I	PREQ#
AB04	IO	AD01	AF17	IO	GD3	**AE11**	**P**	**GND**	D12	IO	HD23	AF23	IO	MD09	W22	I	PWROK
AB02	IO	AD02	AD17	IO	GD4	**AE14**	**P**	**GND**	A12	IO	HD24	AD23	IO	MD10	M03	I	REQ0#
AC01	IO	AD03	AD16	IO	GD5	**AE17**	**P**	**GND**	B11	IO	HD25	AE24	IO	MD11	M04	I	REQ1#
AB05	IO	AD04	AF16	IO	GD6	**B01**	**P**	**GNDDAC**	C11	IO	HD26	AF26	IO	MD12	N05	I	REQ2#
AB01	IO	AD05	AE16	IO	GD7	**AB15**	**P**	**GNDGCK**	A08	IO	HD27	AE25	IO	MD13	N03	I	REQ3#
AA04	IO	AD06	AD15	IO	GD8	**G21**	**P**	**GNDHCK**	B10	IO	HD28	AD25	IO	MD14	N02	I	REQ4#
AA03	IO	AD07	AC16	IO	GD9	**P21**	**P**	**GNDMCK**	D11	IO	HD29	AC25	IO	MD15	AC04	I	RESET#
AA02	IO	AD08	AD14	IO	GD10	**D02**	**P**	**GNDPLL1**	D13	IO	HD30	P24	IO	MD16	D26	IO	RS0#
AA05	IO	AD09	AB13	IO	GD11	**D01**	**P**	**GNDPLL2**	C10	IO	HD31	N26	IO	MD17	D24	IO	RS1#
W05	IO	AD10	AB16	IO	GD12	**AB17**	**P**	**GNDQQ**	E11	IO	HD32	N24	IO	MD18	E26	IO	RS2#
Y03	IO	AD11	AD13	IO	GD13	**A01**	**P**	**GNDRGB**	A11	IO	HD33	N22	IO	MD19	F03	A	RSET
Y02	IO	AD12	AF13	IO	GD14	M02	O	GNT0#	A10	IO	HD34	M26	IO	MD20	AD04	I	SBA0
Y01	IO	AD13	AC12	IO	GD15	M01	O	GNT1#	E12	IO	HD35	M22	IO	MD21	AE03	I	SBA1
Y04	IO	AD14	AB12	IO	GD16	L05	O	GNT2#	B09	IO	HD36	L25	IO	MD22	AE04	I	SBA2
W04	IO	AD15	AD10	IO	GD17	L04	O	GNT3#	D09	IO	HD37	L23	IO	MD23	AF04	I	SBA3
U02	IO	AD16	AC10	IO	GD18	K05	O	GNT4#	E10	IO	HD38	K26	IO	MD24	AD06	I	SBA4
U01	IO	AD17	AE10	IO	GD19	J03	O	GOP0	A09	IO	HD39	K24	IO	MD25	AB07	I	SBA5
T06	IO	AD18	AB10	IO	GD20	AE13	IO	GPAR / GCKRUN#	A07	IO	HD40	K22	IO	MD26	AC06	I	SBA6
T05	IO	AD19	AC09	IO	GD21	AB06	I	GPIPE#	B07	IO	HD41	J25	IO	MD27	AE06	I	SBA7
T04	IO	AD20	AB09	IO	GD22	G04	O	GPOUT	E07	IO	HD42	J22	IO	MD28	AD05	I	SBS
T03	IO	AD21	AD09	IO	GD23	AF02	I	GRBF#	E09	IO	HD43	H25	IO	MD29	AF05	I	SBS#
T02	IO	AD22	AD08	IO	GD24	AD01	I	GREQ#	C08	IO	HD44	H23	IO	MD30	U25	O	SCASA#
T01	IO	AD23	AF07	IO	GD25	AE12	IO	GSTOP#	B08	IO	HD45	G25	IO	MD31	V05	IO	SERR#
R04	IO	AD24	AA09	IO	GD26	**F08**	**P**	**GTLREF**	E06	IO	HD46	AE19	IO	MD32	G01	IO	SPCLK1
R01	IO	AD25	AE07	IO	GD27	**F19**	**P**	**GTLREF**	D07	IO	HD47	AC19	IO	MD33	F05	IO	SPCLK2
R02	IO	AD26	AF06	IO	GD28	AD12	IO	GTRDY#	B06	IO	HD48	AF20	IO	MD34	G02	IO	SPDAT1
P05	IO	AD27	AC07	IO	GD29	AF03	I	GWBF#	E08	IO	HD49	AD20	IO	MD35	F04	IO	SPDAT2
P04	IO	AD28	AB08	IO	GD30	E20	IO	HA03	D05	IO	HD50	AB20	IO	MD36	U22	O	SRASA#
P03	IO	AD29	AD07	IO	GD31	F22	IO	HA04	D08	IO	HD51	AE21	IO	MD37	AD03	O	ST0
P02	IO	AD30	AE15	IO	GDS0	A21	IO	HA05	C07	IO	HD52	AB21	IO	MD38	AF01	O	ST1
P01	IO	AD31	AF15	IO	GDS0#	B22	IO	HA06	C05	IO	HD53	AE22	IO	MD39	AE01	O	ST2
F25	IO	ADS#	AF08	IO	GDS1	B23	IO	HA07	A04	IO	HD54	AC22	IO	MD40	V03	IO	STOP#
D03	O	AG	AE09	IO	GDS1#	E22	IO	HA08	A05	IO	HD55	AE23	IO	MD41	V22	I	SUST#
AF10	**P**	**AGPREF**	AD11	IO	GDSEL#	C22	IO	HA09	C04	IO	HD56	AF24	IO	MD42	V24	O	SWEA#
E03	O	AR	AC13	IO	GFRM#	B20	IO	HA10	D06	IO	HD57	AF25	IO	MD43	V01	IO	TRDY#
H03	I	BISTON	AD02	O	GGNT#	A22	IO	HA11	B04	IO	HD58	AE26	IO	MD44	**F06**	**P**	**VCC3**
A24	IO	BNR#	AF11	IO	GIRDY#	E21	IO	HA12	A06	IO	HD59	AD26	IO	MD45	**F09**	**P**	**VCC3**
A25	IO	BPRI#	**C03**	**P**	**GND**	D22	IO	HA13	A03	IO	HD60	AC26	IO	MD46	**F12**	**P**	**VCC3**
F23	O	BREQ0#	**C06**	**P**	**GND**	A23	IO	HA14	A02	IO	HD61	AC24	IO	MD47	**F15**	**P**	**VCC3**
AA01	IO	CBE0#	**C09**	**P**	**GND**	D21	IO	HA15	B03	IO	HD62	N25	IO	MD48	**F18**	**P**	**VCC3**
W02	IO	CBE1#	**C12**	**P**	**GND**	B21	IO	HA16	B05	IO	HD63	N23	IO	MD49	**F21**	**P**	**VCC3**
U03	IO	CBE2#	**C15**	**P**	**GND**	B19	IO	HA17	D25	IO	HIT#	N21	IO	MD50	**H06**	**P**	**VCC3**
R05	IO	CBE3#	**C18**	**P**	**GND**	E17	IO	HA18	E23	I	HITM#	M25	IO	MD51	**J21**	**P**	**VCC3**
U23	O	CKE0 / SRASB#	**C21**	**P**	**GND**	A20	IO	HA19	B26	I	HLOCK#	M23	IO	MD52	**K21**	**P**	**VCC3**
U24	O	CKE1 / SRASC#	**C24**	**P**	**GND**	A19	IO	HA20	B24	IO	HREQ0#	L26	IO	MD53	**L06**	**P**	**VCC3**
U26	O	CKE2 / SCASB#	**F07**	**P**	**GND**	C20	IO	HA21	D23	IO	HREQ1#	L24	IO	MD54	**M21**	**P**	**VCC3**
V23	O	CKE3 / SCASC#	**F10**	**P**	**GND**	C19	IO	HA22	B25	IO	HREQ2#	L22	IO	MD55	**N04**	**P**	**VCC3**
V25	O	CKE4 / SWEB#	**F13**	**P**	**GND**	E18	IO	HA23	C25	IO	HREQ3#	K25	IO	MD56	**P06**	**P**	**VCC3**
V26	O	CKE5 / SWEC#	**F14**	**P**	**GND**	B18	IO	HA24	C23	IO	HREQ4#	K23	IO	MD57	**R21**	**P**	**VCC3**
C17	O	CPURST#	**F17**	**P**	**GND**	D19	IO	HA25	F01	O	HSYNC	J26	IO	MD58	**T23**	**P**	**VCC3**
G24	O	CRESET	**F20**	**P**	**GND**	D17	IO	HA26	C26	IO	HTRDY#	J23	IO	MD59	**V06**	**P**	**VCC3**
R25	O	CS0# / RAS0#	**F24**	**P**	**GND**	D18	IO	HA27	AC02	O	INTA#	H26	IO	MD60	**V21**	**P**	**VCC3**
R26	O	CS1# / RAS1#	**G03**	**P**	**GND**	D20	IO	HA28	U05	IO	IRDY#	H24	IO	MD61	**AA06**	**P**	**VCC3**
T22	O	CS2# / RAS2#	**H21**	**P**	**GND**	A17	IO	HA29	V04	IO	LOCK#	G26	IO	MD62	**AA20**	**P**	**VCC3**
T25	O	CS3# / RAS3#	**J06**	**P**	**GND**	A18	IO	HA30	W23	O	MA00 / strap	F26	IO	MD63	**AA21**	**P**	**VCC3**
T26	O	CS4# / RAS4#	**J24**	**P**	**GND**	E19	IO	HA31	W24	O	MA01# / strap	AB18	I	NCOMP	**C01**	**P**	**VCCDAC**
U21	O	CS5# / RAS5#	**L03**	**P**	**GND**	G22	I	HCLK	W25	O	MA02 / strap	K06	O	PANELCLK / TVCKR	**AA14**	**P**	**VCCGCK**
E25	IO	DBSY#	**L21**	**P**	**GND**	B17	IO	HD00	W26	O	MA03 / strap	H02	O	PANELD00 / TVD0	**H22**	**P**	**VCCHCK**
A26	IO	DEFER#	**M06**	**P**	**GND**	C16	IO	HD01	Y22	O	MA04 / strap	J01	O	PANELD01 / TVD1	**P22**	**P**	**VCCMCK**
V02	IO	DEVSEL#	**M24**	**P**	**GND**	A15	IO	HD02	Y23	O	MA05 / strap	J02	O	PANELD02 / TVD2	**E02**	**P**	**VCCPLL1**
E04	I	DFTON	**R03**	**P**	**GND**	B13	IO	HD03	Y25	O	MA06 / strap	J04	O	PANELD03 / TVD3	**E01**	**P**	**VCCPLL2**
AB24	O	DQM0 / CAS0#	**R06**	**P**	**GND**	A16	IO	HD04	Y26	O	MA07 / strap	H05	O	PANELD04 / TVD4	**AA07**	**P**	**VCCQ**
AB25	O	DQM1 / CAS1#	**T21**	**P**	**GND**	D15	IO	HD05	AA22	O	MA08 / strap	J05	O	PANELD05 / TVD5	**AA10**	**P**	**VCCQ**
R23	O	DQM2 / CAS2#	**T24**	**P**	**GND**	B16	IO	HD06	AA23	O	MA09 / strap	K01	O	PANELD06 / TVD6	**AA12**	**P**	**VCCQ**
R24	O	DQM3 / CAS3#	**W03**	**P**	**GND**	A13	IO	HD07	AA24	O	MA10 / strap	K02	O	PANELD07 / TVD7	**AA15**	**P**	**VCCQ**
AB26	O	DQM4 / CAS4#	**W06**	**P**	**GND**	D16	IO	HD08	AA25	O	MA11 / strap	K03	O	PANELD08 / TVD8	**AA18**	**P**	**VCCQ**
AC23	O	DQM5 / CAS5#	**Y06**	**P**	**GND**	B14	IO	HD09	AA26	O	MA12 / strap	L01	O	PANELD09 / TVD9	**AC05**	**P**	**VCCQ**
P26	O	DQM6 / CAS6#	**Y21**	**P**	**GND**	B15	IO	HD10	AB22	O	MA13 / strap	K04	O	PANELD10 / TVD10	**AC08**	**P**	**VCCQ**
P25	O	DQM7 / CAS7#	**Y24**	**P**	**GND**	E14	IO	HD11	AB23	O	MA14 / strap	L02	O	PANELD11 / TVBL#	**AC11**	**P**	**VCCQ**
E24	IO	DRDY#	**AA08**	**P**	**GND**	E15	IO	HD12	P23	I	MCLKF	G06	O	PANELDE / TVCLK	**AC14**	**P**	**VCCQ**
U04	IO	FRAME#	**AA11**	**P**	**GND**	A14	IO	HD13	R22	O	MCLK	H01	I	PANELDET / TVD11	**AC17**	**P**	**VCCQ**
AF14	IO	GBE0#	**AA13**	**P**	**GND**	C14	IO	HD14	AF19	IO	MD00	H04	O	PANELHS / TVHS	**AA17**	**P**	**VCCQQ**
AF12	IO	GBE1#	**AA16**	**P**	**GND**	E16	IO	HD15	AD19	IO	MD01	G05	O	PANELVS / TVVS	**C02**	**P**	**VCCRGB**
AB11	IO	GBE2#	**AA19**	**P**	**GND**	E13	IO	HD16	AB19	IO	MD02	W01	IO	PAR	**W21**	**P**	**VSUS25**
AF09	IO	GBE3#	**AB03**	**P**	**GND**	F16	IO	HD17	AE20	IO	MD03	Y05	IO	PCKRUN#	F02	O	VSYNC
AB14	O	GCLK	**AD21**	**P**	**GND**	D14	IO	HD18	AC20	IO	MD04	U06	I	PCLK	N01	O	WSC#
AC15	I	GCLKF	**AD24**	**P**	**GND**	F11	IO	HD19	AF21	IO	MD05	AC18	I	PCOMP	D04	I	XIN
AF18	IO	GD0	**AE02**	**P**	**GND**	C13	IO	HD20	AC21	IO	MD06	M05	O	PGNT#	E05	O	XOUT

Center **VCC3** Pins (16 pins): **J9-10,13-14,17-18, K9,18, N9,18, P9,18, R18, U9, V17-18**
Center **GND** Pins (36 pins): **L11-16, M11-16, N11-16, P11-16, R11-16, T11-16**
Center **VCC25** Pins (15 pins): **J11-12,15-16, L9,18, M9,18, R9, T9,18, U18, V10,13,15**
Center **VCCQ** Pins (5 pins): **V9,11-12,14,16**

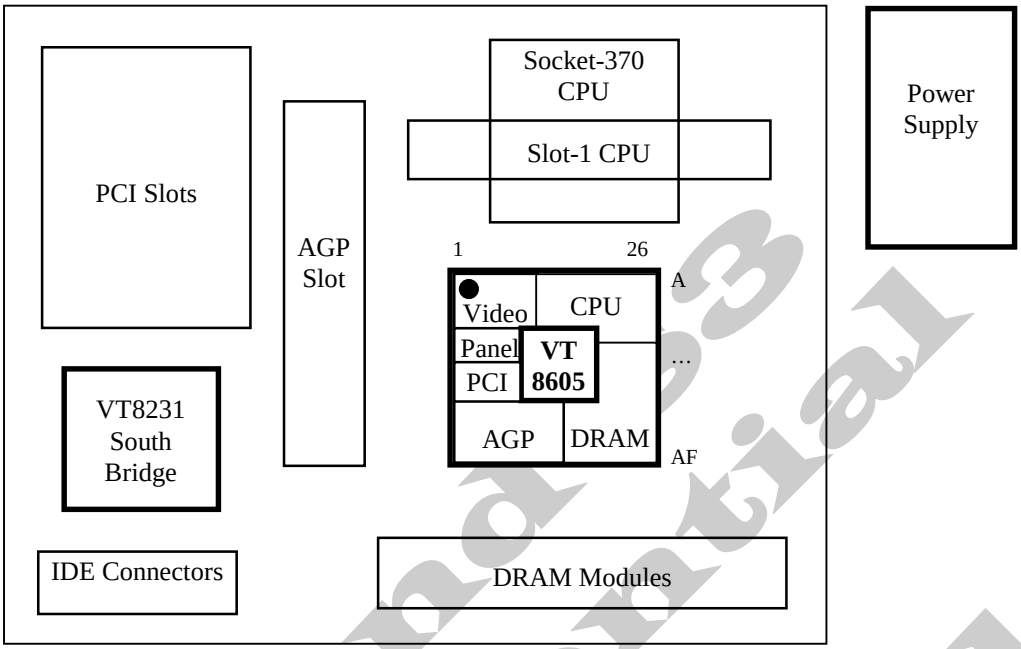
PIN DESCRIPTIONS

Table 1. VT8605 / 86C370 Pin Descriptions

CPU Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
HA[31:3]#	(see pinout tables)	IO	**Host Address Bus.** HA[31:3] connect to the address bus of the host CPU. During CPU cycles HA[31:3] are inputs. These signals are driven by the VT8605 / 86C370 during cache snooping operations.
HD[63:0]#	(see pinout tables)	IO	**Host CPU Data.** These signals are connected to the CPU data bus.
ADS#	F25	IO	**Address Strobe**. The CPU asserts ADS# in T1 of the CPU bus cycle.
BNR#	A24	IO	**Block Next Request**. Used to block the current request bus owner from issuing new requests. This signal is used to dynamically control the processor bus pipeline depth.
BPRI#	A25	IO	**Priority Agent Bus Request**. The owner of this signal will always be the next bus owner. This signal has priority over symmetric bus requests and causes the current symmetric owner to stop issuing new transactions unless the HLOCK# signal is asserted. The VT8605 / 86C370 drives this signal to gain control of the processor bus.
DBSY#	E25	IO	**Data Bus Busy**. Used by the data bus owner to hold the data bus for transfers requiring more than one cycle.
DEFER#	A26	IO	**Defer**. The VT8605 / 86C370 uses a dynamic deferring policy to optimize system performance. The VT8605 / 86C370 also uses the DEFER# signal to indicate a processor retry response.
DRDY#	E24	IO	**Data Ready**. Asserted for each cycle that data is transferred.
HIT#	D25	IO	**Hit**. Indicates that a cacheing agent holds an unmodified version of the requested line. Also driven in conjunction with HITM# by the target to extend the snoop window.
HITM#	E23	I	**Hit Modified**. Asserted by the CPU to indicate that the address presented with the last assertion of EADS# is modified in the L1 cache and needs to be written back.
HLOCK#	B26	I	**Host Lock**. All CPU cycles sampled with the assertion of HLOCK# and ADS# until the negation of HLOCK# must be atomic.
HREQ[4:0]#	C23, C25, B25, D23, B24	IO	**Request Command**. Asserted during both clocks of the request phase. In the first clock, the signals define the transaction type to a level of detail that is sufficient to begin a snoop request. In the second clock, the signals carry additional information to define the complete transaction type.
HTRDY#	C26	IO	**Host Target Ready**. Indicates that the target of the processor transaction is able to enter the data transfer phase.
RS[2:0]#	E26, D24, D26	IO	**Response Signals**. Indicates the type of response per the table below: **RS[2:0]#** **Response type** 000 Idle State 001 Retry Response 010 Defer Response 011 Reserved 100 Hard Failure 101 Normal Without Data 110 Implicit Writeback 111 Normal With Data
CPURST#	C17	O	**CPU Reset.** Reset output to CPU
BREQ0#	F23	O	**Bus Request 0.** Bus request output to CPU.

Note: Clocking of the CPU interface is performed with HCLK. See the clock pin group at the end of the pin descriptions section for descriptions of the clock pins.

The pinouts were defined assuming the ATX PCB layout model shown below (and general pin layout shown) as a guide for PCB component placement. Other PCB layouts (AT, LPX, and NLX) were also considered and can typically follow the same general component placement.



DRAM Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
MD[63:0]	(see pinout tables)	IO	**Memory Data.** These signals are connected to the DRAM data bus.
MA14, **MA13,** **MA12,** **MA11,** **MA10,** **MA9,** **MA8** **MA7,** **MA6,** **MA5,** **MA4,** **MA3,** **MA2** / strap, **MA1,** **MA0**	AB23, AB22, AA26, AA25, AA24, AA23, AA22, Y26, Y25, Y23, Y22, W26, W25, W24, W23	O / I	**Memory Address.** DRAM address lines MA2 strap (see INTA# pin description)
CS[5:0]#	U21, T26, T25, T22, R26, R25	O	**Chip Select.** Chip select of each bank.
DQM[7:0]	P25, P26, AC23, AB26, R24, R23, AB25, AB24	O	**Data Mask.** Data mask of each byte lane
SRASA#	U22	O	**Row Address Command Indicator.**
SCASA#	U25	O	**Column Address Command Indicator.**
SWEA#	V24	O	**Write Enable Command Indicator.**
CKE0 / SRASB#, **CKE1** / SRASC#, **CKE2** / SCASB#, **CKE3** / SCASC#, **CKE4** / SWEB#, **CKE5** / SWEC#	U23, U24, U26, V23, V25, V26	O	**Clock Enables.** Clock enables for each DRAM bank for powering down the SDRAM or clock control for reducing power usage and for reducing heat / temperature in high-speed memory systems.

PCI Bus Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
AD[31:0]	(see pinout tables)	IO	**Address/Data Bus.** The standard PCI address and data lines. The address is driven with FRAME# assertion and data is driven or received in following cycles.
CBE[3:0]#	R5, U3, W2, AA1	IO	**Command/Byte Enable.** Commands are driven with FRAME# assertion. Byte enables corresponding to supplied or requested data are driven on following clocks.
FRAME#	U4	IO	**Frame.** Assertion indicates the address phase of a PCI transfer. Negation indicates that one more data transfer is desired by the cycle initiator.
IRDY#	U5	IO	**Initiator Ready.** Asserted when the initiator is ready for data transfer.
TRDY#	V1	IO	**Target Ready.** Asserted when the target is ready for data transfer.
STOP#	V3	IO	**Stop.** Asserted by the target to request the master to stop the current transaction.
DEVSEL#	V2	IO	**Device Select.** This signal is driven by the VT8605 / 86C370 when a PCI initiator is attempting to access main memory. It is an input when the VT8605 / 86C370 is acting as a PCI initiator.
PAR	W1	IO	**Parity.** A single parity bit is provided over AD[31:0] and C/BE[3:0].
SERR#	V5	IO	**System Error.** The VT8605 / 86C370 will pulse this signal when it detects a system error condition.
LOCK#	V4	IO	**Lock.** Used to establish, maintain, and release resource lock.
PREQ#	N6	I	**South Bridge Request.** This signal comes from the South Bridge. PREQ# is the South Bridge request for the PCI bus.
PGNT#	M5	O	**South Bridge Grant.** This signal driven by the VT8605 / 86C370 to grant PCI access to the South Bridge.
REQ[4:0]#	N2, N3, N5, M4, M3	I	**PCI Master Request.** PCI master requests for PCI.
GNT[4:0]#	K5, L4, L5, M1, M2	O	**PCI Master Grant.** Permission is given to the master to use PCI.
PCLK	U6	I	**PCI Clock.** From external clock generator.
PCKRUN#	Y5	IO	**PCI Clock Run.** May be used to stop PCI clock.
INTA#	AC2	O	**PCI Interrupt Out.** An asynchronous active low output used to signal an event that requires handling on behalf of the internal integrated graphics controller. If MA2 is strapped high at reset (clearing CR36[0]) no interrupt will be requested during PCI configuration. The default drive strength is 24 mA (other drive strengths may be selected via CR80[1-0]).
WSC#	N1	O	**Write Snoop Complete.** Sideband PCI signal (used on the planar only in multiprocessor configurations) asserted to indicate that all snoop activity on the CPU bus initiated by the last PCI-to-DRAM write is complete and that it is safe to send an APIC interrupt message. Basically this signal is always active except when PCI master write data is not flushed.

AGP Bus Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
GD[31:0]	(see pinout tables)	IO	**Address/Data Bus.** The standard AGP/PCI address and data lines. The address is driven with GDS0# and GDS1# assertion for AGP transfers and is driven with GFRM# assertion for PCI transfers.
GDS0	AE15	IO	**Bus Strobe 0 (AGP transactions only).** Provides timing for 2x data transfer mode on AD[15:0]. The agent that is providing the data drives this signal.
GDS0#	AF15	IO	**Bus Strobe 0 complement and Bus Strobe 0 (AGP transactions only).** Provides timing for 4x data transfer mode on AD[15:0]. The agent that is providing the data drives this signal.
GDS1	AF8	IO	**Bus Strobe 1 (AGP transactions only).** Provides timing for 2x data transfer mode on AD[31:16]. The agent that is providing the data drives this signal.
GDS1#	AE9	IO	**Bus Strobe 1 complement and Bus Strobe 1 (AGP transactions only).** Provides timing for 4x data transfer mode on AD[31:16]. The agent that is providing the data drives this signal.
GBE[3:0]#	AF9, AB11, AF12, AF14	IO	**Command/Byte Enable.** **AGP:** These pins provide command information (different commands than for PCI) driven by the master (graphics controller) when requests are being enqueued using PIPE#. These pins provide valid byte information during AGP write transactions and are driven by the master. The target (this chip) drives these lines to "0000" during the return of AGP read data, but the state of these pins is ignored by the AGP master. **PCI:** Commands are driven with GFRM# assertion. Byte enables corresponding to supplied or requested data are driven on following clocks.
GFRM#	AC13	IO	**Frame (PCI transactions only).** Assertion indicates the address phase of a PCI transfer. Negation indicates that one more data transfer is desired by the cycle initiator.
GIRDY#	AF11	IO	**Initiator Ready** **AGP:** For write operations, the assertion of this pin indicates that the master is ready to provide *all* write data for the current transaction. Once this pin is asserted, the master is not allowed to insert wait states. For read operations, the assertion of this pin indicates that the master is ready to transfer a subsequent block of read data. The master is *never* allowed to insert a wait state during the initial block of a read transaction. However, it may insert wait states after each block transfers. **PCI:** Asserted when the initiator is ready for data transfer.
GTRDY#	AD12	IO	**Target Ready:** **AGP:** Indicates that the target is ready to provide read data for the entire transaction (when the transaction can complete within four clocks) or is ready to transfer a (initial or subsequent) block of data when the transfer requires more than four clocks to complete. The target is allowed to insert wait states after each block transfers on both read and write transactions. **PCI:** Asserted when the target is ready for data transfer.
GSTOP#	AE12	IO	**Stop (PCI transactions only).** Asserted by the target to request the master to stop the current transaction.
GDSEL#	AD11	IO	**Device Select (PCI transactions only).** This signal is driven by the VT8605 / 86C370 when a PCI initiator is attempting to access main memory. It is an input when the VT8605 / 86C370 is acting as PCI initiator. Not used for AGP cycles.

Note: Clocking of the AGP interface is performed with GCLK; see the clock pin group for descriptions of the clock pins.

Note: PCB Layout Guidelines (reference from AGP specification)

1. Total motherboard trace length 10" max, trace impedance = 65 ohms ± 15 ohms, minimize signal crosstalk
2. Trace lengths within groups matched to within 2 inches or better
   Groups are:
   a. GDS0#, GDS0, GD15-0, GBE1-0#
   b. GDS1#, GDS1, GD31-16, GBE3-2#
   c. SBS#, SBS, SBA7-0
3. Ground isolation should be provided around GDS0#, GDS0, GDS1# and GDS1 to prevent crosstalk with GD[31:0]. Ideally ground traces should be provided adjacent to GDSn# on the same signal layer, but at a minimum wider spaces should be provided on either side (e.g., 16 mil spaces on either side of GDSn# if GDSn# signal traces are 8 mil).

AGP Bus Interface (continued)			
Signal Name	**Pin #**	**IO**	**Signal Description**
GPIPE#	AB6	I	**Pipelined Request.** Asserted by the master (graphics controller) to indicate that a full-width request is to be enqueued by the target VT8605 / 86C370. The master enqueues one request each rising edge of GCLK while PIPE# is asserted. When PIPE# is deasserted no new requests are enqueued across the AD bus.
GRBF#	AF2	I	**Read Buffer Full.** Indicates if the master (graphics controller) is ready to accept previously requested low priority read data. When RBF# is asserted, the VT8605 / 86C370 will not return low priority read data to the master.
GWBF#	AF3	I	**Write Buffer Full.**
SBA[7:0]	AE6, AC6, AB7, AD6, AF4, AE4, AE3, AD4	I	**SideBand Address.** Provides an additional bus to pass address and command information from the master (graphics controller) to the target (the VT8605 / 86C370). These pins are ignored until enabled.
SBS	AD5	I	**Sideband Strobe.** Provides timing for SBA[7:0] (driven by the master)
SBS#	AF5	I	**Sideband Strobe complement and SBS .** Provides timing for SBA[7:0] (driven by the master) when 4x timing is supported.
ST[2:0]	AE1, AF1, AD3	O	**Status (AGP only).** Provides information from the arbiter to a master to indicate what it may do. Only valid while GGNT# is asserted. 000 Indicates that previously requested low priority read or flush data is being returned to the master (graphics controller). 001 Indicates that previously requested high priority read data is being returned to the master. 010 Indicates that the master is to provide low priority write data for a previously enqueued write command. 011 Indicates that the master is to provide high priority write data for a previously enqueued write command. 100 Reserved. (arbiter must not issue, may be defined in the future). 101 Reserved. (arbiter must not issue, may be defined in the future). 110 Reserved. (arbiter must not issue, may be defined in the future). 111 Indicates that the master (graphics controller) has been given permission to start a bus transaction. The master may enqueue AGP requests by asserting PIPE# or start a PCI transaction by asserting GFRM#. ST[2:0] are always outputs from the VT8605 / 86C370 and inputs to the master.
GREQ#	AD1	I	**Request.** Master request for AGP.
GGNT#	AD2	O	**Grant.** Permission is given to the master to use AGP.
GPAR / GCKRUN#	AE13	IO	Rx78[1]=0: **AGP Parity.** A single parity bit is provided over GD[31:0] and GBE[3:0]. Rx78[1]=1: **AGP Clock Run.** Used to stop the AGP bus clock to reduce bus power usage.
GCLK	AB14	O	**AGP Clock.** Generated by on-chip clock logic.
GCLKF	AC15	I	**AGP Clock Feedback.** Connect to GCLK.

Note: For PCI operation on the AGP bus, the following pins are not required:
- PERR# (parity and error reporting not required on transient data devices such as graphics controllers)
- LOCK# (no lock requirement on AGP)
- IDSEL (internally connected to AD16 on AGP-compliant masters)

Note: Separate system interrupts are not provided for AGP. The AGP connector provides interrupts via PCI bus INTA-B#.

Note: The AGP bus supports only one master directly (REQ[3:0]# and GNT[3:0]# are not provided). External logic is required to implement additional master capability. Note that the arbitration mechanism on the AGP bus is different from the PCI bus.

Note: A separate reset is not required for the AGP bus (RESET# resets both PCI and AGP buses)

Note: Two mechanisms are provided by the AGP bus to enqueue master requests: GPIPE# (to send addresses multiplexed on the AD lines) and the SBA port (to send addresses unmultiplexed). AGP masters implement one or the other or select one at initialization time (they are not allowed to change during runtime). Therefore only one of the two will be used and the signals associated with the other will not be used. Therefore the VT8605 / 86C370 has an internal pullup on GRBF# to maintain it in the de-asserted state in case it is not implemented on the master device.

TFT Flat Panel / External TV Encoder Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
PANELD[11] / TVBLANK#	L2	O	**Multifunction Pins** 1. Panel Data. Internally pulled down during reset. 8mA is the default. 16mA is selected via SR3D[6]=1. 2. TV Blanking Signal. Internally pulled down during reset.
PANELD[10:0] / TVD[10:0]	K4, L1, K3, K2, K1, J5, H5, J4, J2, J1, H2	O	**Multifunction Pins** 1. Panel Data. Internally pulled down during reset. 8mA is the default. 16mA is selected via SR3D[6]=1. 2. TV Data. RGB data is output at one pixel/clock. Internally pulled down during reset.
PANELVS / TVVS	G5	O	**Multifunction Pin** 1. Panel VSYNC. Internally pulled down. 2. TV VSYNC. Internally pulled down during reset.
PANELHS / TVHS	H4	O	**Multifunction Pin** 1. Panel HSYNC. Internally pulled down. 2. TV HSYNC. Internally pulled down during reset.
PANELCLK / TVCLKR	K6	O	**Multifunction Pin** 1. Panel Clock. Internally pulled down. 8mA is the default. 16mA is selected via SR3D[6]=1. 2. TV Return Clock. Output clock to TV encoder. Internally pulled down.
PANELDE / TVCLK	G6	O	**Multifunction Pin** 1. Panel Data Enable. Internally pulled down. 2. TV Clock. Input clock from TV encoder. Internally pulled down.
PANELDET / TVD[11]	H1	I / O	**Multifunction Pin** 1. Panel Detect. If SR30[1]=0, SR30[2] will read 1 if a Flat Panel is appropriately connected. Must be tied to GND if not used. 2. TV Data. RGB data is output at one pixel/clock. Internally pulled down during reset.
GPOUT	G4	O	**General Purpose Output.** This pin reflects the state of SRD[0].
GOP0	J3	O	**General Output Port.** When SR1A[4] is cleared, this pin reflects the state of CR5C[0].

CRT Interface			
Signal Name	**Pin #**	**I/O**	**Signal Description**
RSET	F3	A	**Reference Resistor.** Tie to GNDRGB through an external 140Ω resistor to control the RAMDAC full-scale current value.
AR	E3	O	**Analog Red.** Analog red output to the CRT monitor.
AB	B2	O	**Analog Blue.** Analog blue output to the CRT monitor.
AG	D3	O	**Analog Green.** Analog green output to the CRT monitor.
HSYNC	F1	O	**Horizontal Sync.** Output to CRT.
VSYNC	F2	O	**Vertical Sync.** Output to CRT.

Miscellaneous Functions			
Signal Name	**Pin #**	**I/O**	**Signal Description**
XIN	D4	I	**Reference Frequency Input.** An external 14.318 MHz crystal is connected between XOUT and this pin. Alternatively, an external oscillator can be connected.
XOUT	E5	O	**Crystal Output.** This pin drives the crystal via an internal oscillator. If an external oscillator is connected to XIN, this pin can be left unconnected.
SPCLK[2:1]	F5, G1	IO	**Serial Port Clocks.** These are the clocks for serial data transfer. SPCLK1 is typically used for I^2C communications. As an output, it is programmed via MMFF20[0] or CRA0[0]. As an input, its status is read via MMFF20[2] or CRA0[2]. In either case the serial port must be enabled by MMFF20[4] = 1 or CRA0[4] = 1. SPCLK2 is typically used for DDC monitor communications. As an output, it is programmed via CRB1[0]. As an input, its status is read via CRB1[2]. The port is enabled via CRB1[4] = 1.
SPDAT[2:1]	F4, G2	IO	**Serial Port Data.** These are the data signals used for serial data transfer. SPDAT1 is typically used for I^2C communications. As an output, it is programmed via MMFF20[1] or CRA0[1]. As an input, its status is read via MMFF20[3] or CRA0[3]. In either case the serial port must be enabled by MMFF20[4] = 1 or CRA0[4] = 1. SPDATT2 is typically used for DDC monitor communications. As an output, it is programmed via CRB1[1]. As an input, its status is read via CRB1[3]. The port is enabled via CRB1[4] = 1.

Clock / Reset Control

Signal Name	Pin #	I/O	Signal Description
HCLK	G22	I	**Host Clock.** This pin receives the host CPU clock (66 / 100 / 133 MHz). This clock is used by all VT8605 / 86C370 logic that is in the host CPU domain. The memory interface logic will also use this clock if selected (memory system timing can alternately be selected to use the AGP bus clock). The CPU clock must lead the AGP clock by 0.2 ± 0.5 nsec.
PCLK	U6	I	**PCI Clock.** This pin receives a buffered host clock divided-by-2, 3, or 4 to create 33 MHz. This clock is used by all of the VT8605 / 86C370 logic that is in the PCI clock domain. This clock input must be 33 MHz maximum to comply with PCI specification requirements and must be synchronous with the host CPU clock, HCLK, with an HCLK:PCLK frequency ratio of 2:1, 3:1, or 4:1 as shown in the table below. The host CPU clock must lead the PCI clock by 1.5 ± 0.5 nsec. Typical Clock Frequency Combinations Rx68[1:0] / Mode / Host Clock / AGP Clock / PCI Clock 00 / 2x / 66 MHz / 66 MHz / 33 MHz 01 / 3x / 100 MHz / 66 MHz / 33 MHz 10 / 4x / 133 MHz / 66 MHz / 33 MHz 11 / Reserved
GCLK	AB14	O	**AGP Clock.** This pin drives the AGP bus clock (66 MHz). This clock is used by all VT8605 / 86C370 logic that is in the AGP clock domain. The AGP clock is synchronous / pseudo-synchronous to the host CPU clock (selectable as shown in the table above).
GCLKF	AC15	I	**AGP Clock Feedback.** Connect to GCLK.
MCLK	R22	O	**DRAM Clock.** Output from internal clock generator to the external clock buffer.
MCLKF	P23	I	**DRAM Clock Feedback.** Input from MCLK via the external clock buffer.
RESET#	AC4	I	**Reset.** Input from south bridge chip. When asserted, this signal resets the VT8605 / 86C370 and sets all register bits to the default value. The rising edge of this signal is used to sample all power-up strap options
PWROK	W22	I	**Power OK.**
CPURST#	C17	O	**CPU Reset.** GTL output level.
CRESET	G24	O	**System Reset.** TTL output level.
SUST#	V22	I	**Suspend Status.** For implementation of the Suspend-to-DRAM feature. Connect to an external pullup to disable.

Power, Ground, and Test			
Signal Name	**Pin #**	**I/O**	**Signal Description**
VCC3	(see pin list)	P	**Power** for **I/O Interface Logic** (3.3V ±0.3V).
VCC25	J11, J12, J15, J16, L9, L18, M9, M18, R9, T9, T18, U18, V10, V13, V15	P	**Power** for **Internal Logic** (2.5V ±0.3V).
VSUS25	W21	P	**Suspend Power** (2.5V ±0.3V).
GND	(see pin list)	P	**Ground**
VCCHCK	H22	P	**Host CPU Clock Power** (3.3V ±0.3V). For Host CPU clock logic.
GNDHCK	G21	P	**Host CPU Clock Ground.** Connect to main ground plane.
VCCMCK	P22	P	**DRAM Clock Power** (3.3V ±0.3V). For DRAM clock deskew logic.
GNDMCK	P21	P	**DRAM Clock Ground.** Connect to main ground plane.
VCCGCK	AA14	P	**AGP Clock Power** (3.3V ±0.3V). For AGP clock deskew logic
GNDGCK	AB15	P	**AGP Clock Ground.** Connect to main ground plane.
VCCRGB	C2	P	**RGB Output Power** (3.3V ±0.3V). For analog RGB outputs.
GNDRGB	A1	P	**RGB Output Ground.** Connect to main ground plane.
VCCDAC	C1	P	**DAC Power** (3.3V ±0.3V). For internal RAMDAC logic
GNDDAC	B1	P	**DAC Ground.** Connect to main ground plane.
VCCPLL1	E2	P	**PLL 1 Power** (3.3V ±0.3V). For internal graphics clock 1 logic
GNDPLL1	D2	P	**PLL 1 Ground.** Connect to main ground plane.
VCCPLL2	E1	P	**PLL 2 Power** (3.3V ±0.3V). For internal graphics clock 2 logic
GNDPLL2	D1	P	**PLL 2 Ground.** Connect to main ground plane.
VCCQ	V9, V11, V12, V14, V16, AA7, AA10, AA12, AA15, AA18, AC5, AC8, AC11, AC14, AC17	P	**AGP 1.5V Power.**
VCCQQ	AA17	P	**AGP Quiet Power.**
GNDQQ	AB17	P	**AGP Quiet Ground.**
GTLREF	F8, F19	P	**CPU Interface GTL+ Voltage Reference.** 2/3 VTT ±2%
AGPREF	AF10	P	**AGP Voltage Reference.** 0.39 VCC3 to 0.41 VCC3. Typical value is 1.32V (0.40 times 3.3V). This can be provided with a resistive divider on VCC3 using 270 ohm and 180 ohm (2%) resistors.
NCOMP	AB18	I	**Compensation.** Connect to VCCQ through a 60 ohm resistor.
PCOMP	AC18	I	**Compensation.** Connect to GND through a 60 ohm resistor.
PLLTEST	G23	I	**PLL Test Input.**
BISTON	H3	I	**BIST On.** This pin is used for testing and must be tied to GND on all board designs.
DFTON	E4	I	**DFT On.** This pin is used for testing and must be tied to GND on all board designs.

REGISTERS

Register Overview

The following tables summarize the configuration and I/O registers of the VT8605 / 86C370. These tables also document the power-on default value ("Default") and access type ("Acc") for each register. Access type definitions used are RW (Read/Write), RO (Read/Only), "—" for reserved / used (essentially the same as RO), and RWC (or just WC) (Read / Write 1's to Clear individual bits). Registers indicated as RW may have some read/only bits that always read back a fixed value (usually 0 if unused); registers designated as RWC or WC may have some read-only or read write bits (see individual register descriptions following these tables for details). All offset and default values are shown in hexadecimal unless otherwise indicated.

NOTE: The integrated Savage4 graphics registers are discussed in detail in a separate document, "VT8605 / 86C370 Savage4 Registers".

Table 2. VT8605 / 86C370 Registers

VT8605 / 86C370 I/O Ports

Port #	I/O Port	Default	Acc
22	PCI / AGP Arbiter Disable	00	RW
CFB-8	Configuration Address	0000 0000	RW
CFF-C	Configuration Data	0000 0000	RW

VT8605 / 86C370 Device 0 Registers - Host Bridge

Header Registers

Offset	Configuration Space Header	Default	Acc
1-0	Vendor ID	**1106**	RO
3-2	Device ID	**TBD**	RO
5-4	Command	**0006**	**RW**
7-6	Status	**0290**	**WC**
8	Revision ID	**4n**	RO
9	Program Interface	00	RO
A	Sub Class Code	00	RO
B	Base Class Code	**06**	RO
C	-reserved-	00	—
D	Latency Timer	00	**RW**
E	Header Type	00	RO
F	Built In Self Test (BIST)	00	RO
13-10	Graphics Aperture Base	**0000 0008**	**RW**
14-2B	-reserved-	00	—
2D-2C	Subsystem Vendor ID	0000	**W1**
2F-2E	Subsystem ID	0000	**W1**
30-33	-reserved-	00	—
37-34	Capability Pointer	**0000 00A0**	RO
38-3F	-reserved-	00	—

Device-Specific Registers

Offset	Host CPU Protocol Control	Default	Acc
50	Request Phase Control	00	RW
51	Response Phase Control	00	RW
52	Dynamic Defer Timer	**10**	RW
53	Miscellaneous 1	**03**	RW
54	Miscellaneous 2	00	RW
55	-reserved-	00	—

Offset	DRAM Control	Default	Acc
59-58	MA Map Type	**0040**	RW
5F-5A	DRAM Row Ending Address:		
5A	Bank 0 Ending (HA[31:24])	**01**	RW
5B	Bank 1 Ending (HA[31:24])	**01**	RW
5C	Bank 2 Ending (HA[31:24])	**01**	RW
5D	Bank 3 Ending (HA[31:24])	**01**	RW
5E	Bank 4 Ending (HA[31:24])	**01**	RW
5F	Bank 5 Ending (HA[31:24])	**01**	RW
56	Bank 6 Ending (HA[31:24])	**01**	RW
57	Bank 7 Ending (HA[31:24])	**01**	RW
60	DRAM Type	00	RW
61	ROM Shadow Control C0000-CFFFF	00	RW
62	ROM Shadow Control D0000-DFFFF	00	RW
63	ROM Shadow Control E0000-FFFFF	00	RW
64	DRAM Timing for Banks 0,1	**EC**	RW
65	DRAM Timing for Banks 2,3	**EC**	RW
66	DRAM Timing for Banks 4,5	**EC**	RW
67	DRAM Timing for Banks 6,7	**EC**	RW
68	DRAM Control	00	RW
69	DRAM Clock Select	00	RW
6A	DRAM Refresh Counter	00	RW
6B	DRAM Arbitration Control	**01**	RW
6C	SDRAM Control	00	RW
6D	DRAM Control Drive Strength	00	RW
6E-6F	-reserved-	00	—

Device-Specific Registers (continued)

Offset	PCI Bus Control	Default	Acc
70	PCI Buffer Control	00	RW
71	CPU to PCI Flow Control 1	00	RW
72	CPU to PCI Flow Control 2	00	RW
73	PCI Master Control 1	00	RW
74	PCI Master Control 2	00	RW
75	PCI Arbitration 1	00	RW
76	PCI Arbitration 2	00	RW
77	Chip Test (do not program)	00	RW
78	PMU Control	00	RW
79	PMU Control	00	RW
7A	Miscellaneous Control 1	00	RW
7B	Miscellaneous Control 2	**02**	RW
7C-7D	-reserved-	00	—
7E-7F	PLL Test Mode (do not program)	00	RW

Offset	GART/TLB Control	Default	Acc
83-80	GART/TLB Control	0000 0000	RW
84	Graphics Aperture Size	00	RW
85-87	-reserved-	00	—
8B-88	Gr. Aperture TLB Base Register Base	0000 0000	RW
8C-9F	-reserved-	00	—

Offset	AGP Control	Default	Acc
A0	AGP ID	**02**	RO
A1	AGP Next Item Pointer	00	RO
A2	AGP Specification Revision	**10**	RO
A3	-reserved-	00	—
A7-A4	AGP Status	**0700 0203**	RO
AB-A8	AGP Command	0000 0000	**RW**
AC	AGP Control	**08**	**RW**
AD	AGP Latency Timer	**02**	RW
AE	AGP Miscellaneous Control	00	RW
AF	-reserved-	00	—
B0	AGP Compensation Control / Status	**8x**	RW
B1	AGP Drive Strength	**63**	RW
B2-BF	-reserved-	00	—

Offset	Miscellaneous Control	Default	Acc
C0-DF	-reserved-	00	—
E0	Miscellaneous Control	00	RW
E1-EF	-reserved-	00	—
F7-F0	BIOS Scratch Registers	00	RW
F8	DRAM Arbitration Timer	00	RW
F9	VGA Timer	00	RW
FA-FB	-reserved-	0000	RW
FC	Back-Door Control 1	00	RW
FD	Back-Door Control 2	00	RW
FF-FE	Back-Door Device ID	0000	RW

VT8605 / 86C370 Device 1 Registers - PCI-to-PCI Bridge

Header Registers

Offset	Configuration Space Header	Default	Acc
1-0	Vendor ID	**1106**	RO
3-2	Device ID	**8598**	RO
5-4	Command	**0007**	**RW**
7-6	Status	**0220**	**WC**
8	Revision ID	**nn**	RO
9	Program Interface	00	RO
A	Sub Class Code	**04**	RO
B	Base Class Code	**06**	RO
C	-reserved-	00	—
D	Latency Timer	00	**RW**
E	Header Type	**01**	RO
F	Built In Self Test (BIST)	00	RO
10-17	-reserved-	00	—
18	Primary Bus Number	00	**RW**
19	Secondary Bus Number	00	**RW**
1A	Subordinate Bus Number	00	**RW**
1B	Secondary Latency Timer	00	RO
1C	I/O Base	**F0**	**RW**
1D	I/O Limit	00	**RW**
1F-1E	Secondary Status	0000	RO
21-20	Memory Base	**FFF0**	**RW**
23-22	Memory Limit (Inclusive)	0000	**RW**
25-24	Prefetchable Memory Base	**FFF0**	**RW**
27-26	Prefetchable Memory Limit	0000	**RW**
28-3D	-reserved-	00	—
3F-3E	PCI-to-PCI Bridge Control	00	**RW**

Device-Specific Registers

Offset	AGP Bus Control	Default	Acc
40	CPU-to-AGP Flow Control 1	00	RW
41	CPU-to-AGP Flow Control 2	00	RW
42	AGP Master Control	00	RW
43	AGP Master Latency Timer	00	RW
44	Back-Door Register Control	00	RW
45	Fast Write Control	**72**	RW
47-46	PCI-to-PCI Bridge Device ID	0000	RW
48-7F	-reserved-	00	—
80	Capability ID	**01**	**RO**
81	Next Pointer	00	**RO**
82	Power Management Capabilities 1	**02**	**RO**
83	Power Management Capabilities 2	00	**RO**
84	Power Management Control / Status	00	RW
85	Power Management Status	00	**RO**
86	PCI-PCI Bridge Support Extensions	00	**RO**
87	Power Management Data	00	**RO**
88-FF	-reserved-	00	—

Miscellaneous I/O

One I/O port is defined in the VT8605 / 86C370: Port 22.

Port 22 – PCI / AGP Arbiter Disable .....RW

7-2 Reserved ..... always reads 0

1 AGP Arbiter Disable
- 0 Respond to GREQ# signal .....default
- 1 Do not respond to GREQ# signal

0 PCI Arbiter Disable
- 0 Respond to all REQ# signals.....default
- 1 Do not respond to any REQ# signals, including PREQ#

This port can be enabled for read/write access by setting bit-7 of Device 0 Configuration Register 78.

Configuration Space I/O

All registers in the VT8605 / 86C370 (listed above) are addressed via the following configuration mechanism:

Mechanism #1

These ports respond only to double-word accesses. Byte or word accesses will be passed on unchanged.

Port CFB-CF8 - Configuration Address..... RW

31 Configuration Space Enable
- 0 Disabled..... default
- 1 Convert configuration data port writes to configuration cycles on the PCI bus

30-24 Reserved .....always reads 0

23-16 PCI Bus Number
Used to choose a specific PCI bus in the system

15-11 Device Number
Used to choose a specific device in the system (devices 0 and 1 are defined for the VT8605 / 86C370)

10-8 Function Number
Used to choose a specific function if the selected device supports multiple functions (only function 0 is defined for the VT8605 / 86C370).

7-2 Register Number (also called the "Offset")
Used to select a specific DWORD in the VT8605 / 86C370 configuration space

1-0 Fixed .....always reads 0

Port CFF-CFC - Configuration Data..... RW

Refer to PCI Bus Specification Version 2.1 for further details on operation of the above configuration registers.

Device 0 Register Descriptions

Device 0 Header Registers - Host Bridge

All registers are located in PCI configuration space. They should be programmed using PCI configuration mechanism 1 through CF8 / CFC with bus number, function number, and device number equal to zero.

Device 0 Offset 1-0 - Vendor ID (1106h) .....RO

15-0 ID Code (reads 1106h to identify VIA Technologies)

Device 0 Offset 3-2 - Device ID (TBDh).....RO

15-0 ID Code (reads TBDh to identify the VT8605 / 86C370)

Device 0 Offset 5-4 –Command (0006h) .....RW

15-10 Reserved ..... always reads 0

9 Fast Back-to-Back Cycle Enable ..... RO
- 0 Fast back-to-back transactions only allowed to the same agent .....default
- 1 Fast back-to-back transactions allowed to different agents

8 SERR# Enable..... RO
- 0 SERR# driver disabled.....default
- 1 SERR# driver enabled

(SERR# is used to report parity errors if bit-6 is set).

7 Address / Data Stepping ..... RO
- 0 Device never does stepping.....default
- 1 Device always does stepping

6 Parity Error Response.....**RW**
- 0 Ignore parity errors & continue .....default
- 1 Take normal action on detected parity errors

5 VGA Palette Snoop ..... RO
- 0 Treat palette accesses normally .....default
- 1 Don't respond to palette accesses on PCI bus

4 Memory Write and Invalidate Command..... RO
- 0 Bus masters must use Mem Write .....default
- 1 Bus masters may generate Mem Write & Inval

3 Special Cycle Monitoring ..... RO
- 0 Does not monitor special cycles .....default
- 1 Monitors special cycles

2 Bus Master ..... RO
- 0 Never behaves as a bus master
- 1 Can behave as a bus master .....default

1 Memory Space..... RO
- 0 Does not respond to memory space
- 1 Responds to memory space .....default

0 I/O Space ..... RO
- 0 Does not respond to I/O space .....default
- 1 Responds to I/O space

Device 0 Offset 7-6 – Status (0210h)..... RWC

15 Detected Parity Error
- 0 No parity error detected..... default
- 1 Error detected in either address or data phase. This bit is set even if error response is disabled (command register bit-6). .....write one to clear

14 Signaled System Error (SERR# Asserted)
..... always reads 0

13 Signaled Master Abort
- 0 No abort received ..... default
- 1 Transaction aborted by the master .....
.....write one to clear

12 Received Target Abort
- 0 No abort received ..... default
- 1 Transaction aborted by the target.....
.....write one to clear

11 Signaled Target Abort..... always reads 0
- 0 Target Abort never signaled

10-9 DEVSEL# Timing
- 00 Fast
- 01 Medium..... always reads 01
- 10 Slow
- 11 Reserved

8 Data Parity Error Detected
- 0 No data parity error detected ..... default
- 1 Error detected in data phase. Set only if error response enabled via command bit-6 = 1 and VT8605 / 86C370 was initiator of the operation in which the error occurred.write one to clear

7 Fast Back-to-Back Capable ..... always reads 0

6 User Definable Features..... always reads 0

5 66MHz Capable ..... always reads 0

4 Supports New Capability list..... always reads 1

3-0 Reserved ..... always reads 0

Device 0 Offset 8 - Revision ID (00h) ..... RO

7-0 Chip Revision Code .....

Device 0 Offset 9 - Programming Interface (00h) ..... RO

7-0 Interface Identifier ..... always reads 00

Device 0 Offset A - Sub Class Code (00h)..... RO

7-0 Sub Class Code ..... reads 00 to indicate Host Bridge

Device 0 Offset B - Base Class Code (06h)..... RO

7-0 Base Class Code .. reads 06 to indicate Bridge Device

Device 0 Offset D - Latency Timer (00h) ..... RW

Specifies the latency timer value in PCI bus clocks.

7-3 Guaranteed Time Slice for CPU..... default=0

2-0 Reserved (fixed granularity of 8 clks) .. always read 0

Bits 2-1 are writeable but read 0 for PCI specification compatibility. The programmed value may be read back in Offset 75 bits 5-4 (PCI Arbitration 1).

Device 0 Host Bridge Header Registers (continued)

Device 0 Offset E - Header Type (00h).....RO

7-0 Header Type Code .....reads 00: single function

Device 0 Offset F - Built In Self Test (BIST) (00h).....RO

7 BIST Supported .....reads 0: no supported functions
6-0 Reserved ..... always reads 0

Device 0 Offset 13-10 - Graphics Aperture Base (00000008h) .....RW

31-28 Upper Programmable Base Address Bits..... def=0
27-20 Lower Programmable Base Address Bits ..... def=0
These bits behave as if hardwired to 0 if the corresponding Graphics Aperture Size register bit (Device 1 Offset 84h) is 0.

27	26	25	24	23	22	21	20	(This Register)
7	6	5	4	3	2	1	0	(Gr Aper Size)
RW	RW	RW	RW	RW	RW	RW	RW	1M
RW	RW	RW	RW	RW	RW	RW	0	2M
RW	RW	RW	RW	RW	RW	0	0	4M
RW	RW	RW	RW	RW	0	0	0	8M
RW	RW	RW	RW	0	0	0	0	16M
RW	RW	RW	0	0	0	0	0	32M
RW	RW	0	0	0	0	0	0	64M
RW	0	0	0	0	0	0	0	128M
0	0	0	0	0	0	0	0	256M

19-0 Reserved ..... always reads 00008
Note: The locations in the address range defined by this register are prefetchable.

Device 0 Offset 2D-2C – Subsystem Vendor ID (0000h)R/W1

15-0 Subsystem Vendor ID ..... default = 0
This register may be written once and is then read only.

Device 0 Offset 2F-2E – Subsystem ID (0000h) R/W1

15-0 Subsystem ID..... default = 0
This register may be written once and is then read only.

Device 0 Offset 37-34 - Capability Pointer (000000A0h) RO

Contains an offset from the start of configuration space.

31-0 AGP Capability List Pointer.....always reads A0h

Device 0 Configuration Registers - Host Bridge

These registers are normally programmed once at system initialization time.

Host CPU Control

Device 0 Offset 50 – Request Phase Control (00h)..... RW

7 CPU Hardwired IOQ (In Order Queue) Size
Default per strap on pin MAB11#During reset. This register can be written 0 to restrict the chip to one level of IOQ.
0 1-Level
1 4-Level
6 Read-Around-Write
0 Disable..... default
1 Enable
5 Reserved .....always reads 0
4 Defer Retry When HLOCK Active
0 Disable..... default
1 Enable
Note: always set this bit to 1
3-1 Reserved .....always reads 0
0 CPU / PCI Master Read DRAM Timing
0 Start DRAM read after snoop complete..... def
1 Start DRAM read before snoop complete

Device 0 Offset 51 – Response Phase Control (00h).....RW

7 CPU Read DRAM 0ws for Back-to-Back Read Transactions
0 Disable .....default
1 Enable
Setting this bit enables maximum read performance by allowing continuous 0 wait state reads for pipelined line reads. If this bit is not set, there will be at least 1T idle time between read transactions.

6 CPU Write DRAM 0ws for Back-to-Back Write Transactions
0 Disable .....default
1 Enable
Setting this bit enables maximum write performance by allowing continuous 0 wait state writes for pipelined line writes ands sustained 3T single writes. If this bit is not set, there will be at least 1T idle time between write transactions.

5 Reserved ..... always reads 0

4 Fast Response (HIT/HITM sample 1T earlier)
0 Disable .....default
1 Enable

3 Non-Posted IOW
0 Disable .....default
1 Enable

2 CPU Read DRAM Prefetch Buffer Depth
0 1-level prefetch buffer.....default
1 4-level prefetch buffer

1 CPU-to-DRAM Post-Write Buffer Depth
0 1-level post-write buffer.....default
1 4-level post-write buffer

0 Concurrent PCI Master / Host Operation
0 Disable – the CPU bus will be occupied (BPRI asserted) during the entire PCI operation .... def
1 Enable – the CPU bus is only requested before ADS# assertion
2

Device 0 Offset 52 – Dynamic Defer Timer (10h).....RW

7 GTL I/O Buffer Pullup.....default = MAB6# Strap
0 Disable
1 Enable
The default value of this bit is determined by a strap on the MAB6# pin during reset.

6 RAW Write Retire Policy (After 2 Writes)
0 Disable .....default
1 Enable

5 Quick Start Select .....default = MAB10 Strap
0 Disable .....default
1 Enable
The default value of this bit is determined by a strap on the MAB10 pin during reset.

4-0 Snoop Stall Count
00 Disable dynamic defer
01-1F Snoop stall count ..... default = 10h

Device 0 Offset 53 – Miscellaneous 1 (03h)..... RW

7 HREQ
0 Disable..... default
1 Enable

6 SDRAM Frequency Higher Than CPU Front Side Bus Frequency
0 Disable..... default
1 Enable
Setting this bit enables the DRAM subsystem to run at a higher frequency than the CPU FSB frequency. When setting this bit, register bit Rx69[6] must also be set and only SDRAM type DIMM modules may be used.

5 PCI/AGP Master-to-CPU / CPU-to-PCI/AGP Slave Concurrency
0 Disable..... default
1 Enable

4 HPRI Function
0 Disable..... default
1 Enable

3 P6Lock Function
0 Disable..... default
1 Enable

2 Line Write / Write Back Without Implicit Write Back Data
0 Disable..... default
1 Enable

1 PCI Master Pipeline Access
0 Disable
1 Enable **..... default**

0 Initialization of Fast Write Address Selection
0 Tail
1 Head **..... default**

Device 0 Offset 54 – Miscellaneous 2 (00h)..... RW

7-6 Reserved (Do Not Program) .....default = 0

5-2 Reserved .....always reads 0

1 Invalidate CPU Internal Cache on PCI Master Access
0 Disable..... default
1 Enable

0 1-1-1-1 PMRDY for PCI Master Access
0 Disable..... default
1 Enable

DRAM Control

These registers are normally set at system initialization time and not accessed after that during normal system operation. Some of these registers, however, may need to be programmed using specific sequences during power-up initialization to properly detect the type and size of installed memory (refer to the VIA Technologies VT8605 / 86C370 BIOS porting guide for details).

Table 3. System Memory Map

Space	Start	Size	Address Range	Comment
DOS	0	640K	00000000-0009FFFF	Cacheable
VGA	640K	128K	000A0000-000BFFFF	Used for SMM
BIOS	768K	16K	000C0000-000C3FFF	Shadow Ctrl 1
BIOS	784K	16K	000C4000-000C7FFF	Shadow Ctrl 1
BIOS	800K	16K	000C8000-000CBFFF	Shadow Ctrl 1
BIOS	816K	16K	000CC000-000CFFFF	Shadow Ctrl 1
BIOS	832K	16K	000D0000-000D3FFF	Shadow Ctrl 2
BIOS	848K	16K	000D4000-000D7FFF	Shadow Ctrl 2
BIOS	864K	16K	000D8000-000DBFFF	Shadow Ctrl 2
BIOS	880K	16K	000DC000-000DFFFF	Shadow Ctrl 2
BIOS	896K	64K	000E0000-000EFFFF	Shadow Ctrl 3
BIOS	960K	64K	000F0000-000FFFFF	Shadow Ctrl 3
Sys Bus Init	1MB D Top 4G-64K	— 64K	00100000-DRAM Top DRAM Top-FFFEFFFF FFFEFFFF-FFFFFFFF	Can have hole 000Fxxxx alias

Device 0 Offset 59-58 - DRAM MA Map Type (0000h).RW

15-13 Bank 5/4 MA Map Type (see below)
12 Bank 5/4 Virtual Channel Enable..... def=0

11-8 Reserved ..... def=0

7-5 **Bank 0/1 MA Map Type (SDRAM)**
- 000 16Mbit SDRAM.....default
- 001 -reserved-
- 01x -reserved-
- 100 64Mbit / 128Mbit SDRAM
- 101 256Mbit SDRAM x32
- 110 256Mbit SDRAM x16
- 111 256Mbit SDRAM x8 or x4

4 Bank 1/0 Virtual Channel Enable..... def=0

3-1 Bank 3/2 MA Map Type (see above)
0 Bank 3/2 Virtual Channel Enable..... def=0

Device 0 Offset 5F-5A – DRAM Row Ending Address:

Offset 5A – Bank 0 Ending (HA[31:24]) (01h)..... RW

Offset 5B – Bank 1 Ending (HA[31:24]) (01h)..... RW

Offset 5C – Bank 2 Ending (HA[31:24]) (01h)..... RW

Offset 5D – Bank 3 Ending (HA[31:24]) (01h)..... RW

Offset 5E – Bank 4 Ending (HA[31:24]) (01h)..... RW

Offset 5F – Bank 5 Ending (HA[31:24]) (01h)..... RW

Note : BIOS is required to fill the ending address registers for all banks even if no memory is populated. The endings have to be in incremental order.

Device 0 Offset 60 – DRAM Type (3Fh)..... RW

7- 6 Reserved
5-4 DRAM Type for Bank 5/4
- 00 -reserved-
- 01 -reserved-
- 10 -reserved-
- 11 SDRAM ..... default

3-2 DRAM Type for Bank 3/2.....default=SDRAM
1-0 DRAM Type for Bank 1/0.....default=SDRAM

Table 4. Memory Address Mapping Table

SDRAM

MA:	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
16Mb (0xx)				**11** *11*	22 PC	21 24	20 23	19 10	18 9	17 8	16 7	15 6	14 5	13 4	12 3	11x10, 11x9, 11x8
64/128Mb (100) 2/4 bank		**24** ***27/ 24***	*13* *13*	*12* *12*	22 PC	21 *26*	20 *25*	19 10	18 9	17 8	16 7	15 6	14 5	*11* 4	*23* 3	x4: 14x10 x8: 14x9
256Mb (101) 2/4B	**25**	*24* *28*	*13* *13*	*12* *12*	22 PC	21 *26*	20 *25*	19 10	18 9	17 8	16 7	15 6	14 5	*11* 4	*23* 3	x32: 14x8
256Mb (110) 2/4B	**26**	*24* *28*	*13* *13*	*12* *12*	22 PC	21 *26*	20 *25*	19 10	18 9	17 8	16 7	15 6	14 5	*11* 4	*23* 3	x16: 14x9
256Mb (111) 2/4B	**27**	*24* *28*	*13* *13*	*12* *12*	22 PC	21 *26*	20 *25*	19 10	18 9	17 8	16 7	15 6	14 5	*11* 4	*23* 3	x8: 14x10 x4: 14x11

"PC" = "Precharge Control" (refer to SDRAM specifications)

Device 0 Offset 61 - Shadow RAM Control 1 (00h) .....RW

7-6 CC000h-CFFFFh
- 00 Read/write disable .....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

5-4 C8000h-CBFFFh
- 00 Read/write disable .....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

3-2 C4000h-C7FFFh
- 00 Read/write disable .....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

1-0 C0000h-C3FFFh
- 00 Read/write disable .....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

Device 0 Offset 62 - Shadow RAM Control 2 (00h) .....RW

7-6 DC000h-DFFFFh
- 00 Read/write disable .....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

5-4 D8000h-DBFFFh
- 00 Read/write disable .....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

3-2 D4000h-D7FFFh
- 00 Read/write disable .....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

1-0 D0000h-D3FFFh
- 00 Read/write disable .....default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

Device 0 Offset 63 - Shadow RAM Control 3 (00h)..... RW

7-6 E0000h-EFFFFh
- 00 Read/write disable ..... default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

5-4 F0000h-FFFFFh
- 00 Read/write disable ..... default
- 01 Write enable
- 10 Read enable
- 11 Read/write enable

3-2 Memory Hole
- 00 None ..... default
- 01 512K-640K
- 10 15M-16M (1M)
- 11 14M-16M (2M)

1-0 SMI Mapping Control

	SMM		Non-SMM	
	Code	Data	Code	Data
00	DRAM	DRAM	PCI	PCI
01	DRAM	DRAM	DRAM	DRAM
10	DRAM	PCI	PCI	PCI
11	DRAM	DRAM	DRAM	DRAM

Device 0 Offset 64 - DRAM Timing for Banks 0,1 (ECh)RW

Device 0 Offset 65 - DRAM Timing for Banks 2,3 (ECh)RW

Device 0 Offset 66 - DRAM Timing for Banks 4,5 (ECh)RW

Device 0 Offset 67 - Reserved.....RW

SDRAM Settings for Registers 66-64

7 Precharge Command to Active Command Period
- 0 TRP = 2T
- 1 TRP = 3T .....default

6 Active Command to Precharge Command Period
- 0 TRAS = 5T
- 1 TRAS = 6T .....default

5-4 CAS Latency
- 00 1T
- 01 2T
- 10 3T .....default
- 11 reserved

3 DIMM Type
- 0 Standard
- 1 Registered .....default

2 ACTIVE Command to CMD Command Period
- 0 2T
- 1 3T .....default

1-0 Bank Interleave
- 00 No Interleave.....default
- 01 2-way
- 10 4-way
- 11 Reserved

Device 0 Offset 68 - DRAM Control (00h).....RW

7 SDRAM Open Page Control
- 0 Always precharge SDRAM banks.....default
- 1 SDRAM banks remain active

6 Bank Page Control
- 0 Allow only pages of the same bank active.. def.
- 1 Allow pages of different banks to be active

5 Reserved ..... always reads 0

4 - 3 Reserved ..... always reads 0

2 Burst Refresh
- 0 Disable .....default
- 1 Enable (burst 4 times)

1 System Frequency Divider ..... RO
This bit is latched from MAB8# at the rising edge of RESET# (see table below).

0 System Frequency Divider ..... RO
This bit is latched from MAB12# at the rising edge of RESET#.
- 00 CPU Frequency = 66 MHz
- 01 CPU Frequency = 100 MHz
- 10 CPU Frequency = 133 MHz
- 11 Reserved

Note: See also Rx69[7-6]
Note: MD0 is internally pulled up for EDO detection.

Device 0 Offset 69 – DRAM Clock Select (00h) ..... RW

7 CPU Operating Frequency Faster Than DRAM
- 0 CPU Same As or Equal to DRAM..... default
- 1 CPU Faster Than DRAM by 33 MHz

6 DRAM Operating Frequency Faster Than CPU
- 0 DRAM Same As or Equal to CPU..... default
- 1 DRAM Faster Than CPU by 33 MHz

Rx68[1-0]	Rx69[7-6]	CPU / DRAM
00	00	66 / 66 (def)
00	01	66 / 100†
01	10	100 / 66
01	00	100 / 100
01	01	100 / 133†
10	10	133 / 100
10	00	133 / 133

†Rx53[6] must also be set to 1 for DRAM > CPU

5 256Mbit DRAM Support
- 0 Disable (pin AB22 is DCLKRD)..... default
- 1 Enable (pin AB22 is MAA14)

4 DRAM Controller Command Register Output
- 0 Disable..... default
- 1 Enable

3 Fast DRAM Precharge for Different Bank
- 0 Disable..... default
- 1 Enable

2 DRAM 4K Page Enable (for 64Mbit DRAM)
- 0 Disable..... default
- 1 Enable

1 DIMM Type
- 0 Unbuferred..... default
- 1 Registered

0 CPU/DRAM 66/133MHz support*
- 0 Disable..... default
- 1 Enable

†Rx53[6] must also be set to 1 for DRAM > CPU

Device 0 Offset 6A - Refresh Counter (00h).....RW

7-0 Refresh Counter (in units of 16 CPUCLKs)

00 DRAM Refresh Disabled .....default
01 32 CPUCLKs
02 48 CPUCLKs
03 64 CPUCLKs
04 80 CPUCLKs
05 96 CPUCLKs
… …

The programmed value is the desired number of 16-CPUCLK units minus one.

Device 0 Offset 6B - DRAM Arbitration Control (01h).RW

7-6 Arbitration Parking Policy

00 Park at last bus owner.....default
01 Park at CPU side
10 Park at AGP side
11 Reserved

5 Fast Read to Write turn-around

0 Disable .....default
1 Enable

4 Memory Module Configuration.....RO

0 Normal Operation.....default
1 Unused Outputs Tristated (CSB#, DQMB, CKE, MAB, DCLKO)

This bit is latched from MAB7# at the rising edge of RESET#.

3 MD Bus Second Level Strength Control

0 Normal slew rate control .....default
1 More slew rate control

2 CAS Bus Second Level Strength Control

0 Normal slew rate control .....default
1 More slew rate control

1 Virtual Channel-DRAM Enable

0 Disable .....default
1 Enable

0 Multi-Page Open

0 Disable (page registers marked invalid and no page register update which causes non page-mode operation)
1 Enable .....default

Device 0 Offset 6C - SDRAM Control (00h) ..... RW

7-5 Reserved .....always reads 0

4 CKE Configuration

0 Rx6B[4]=0 CSA = CSA, CSB = CSB, CKE0=CKE0, CKE1 = CKE1
x Rx6B[4]=1 CSA = CSA, CSB = Float, CSB = Float, MAB = Float, CKE0 = CKE0, CKE1 = CKE0
1 Rx6B[4]=0 CSA = CSA, CSB = CSB, CKE3-2 = CSA7-6 CKE5-4 = CSB7-6 CKE1 = GCKE (Global CKE) CKE0 = FENA (FET Enable)

3 Fast TLB Lookup

0 Disable..... default
1 Enable

2-0 SDRAM Operation Mode Select

000 Normal SDRAM Mode..... default
001 NOP Command Enable
010 All-Banks-Precharge Command Enable (CPU-to-DRAM cycles are converted to All-Banks-Precharge commands).
011 MSR Enable
CPU-to-DRAM cycles are converted to commands and the commands are driven on MA[14:0]. The BIOS selects an appropriate host address for each row of memory such that the right commands are generated on MA[14:0].
100 CBR Cycle Enable (if this code is selected, CAS-before-RAS refresh is used; if it is not selected, RAS-Only refresh is used)
101 Reserved
11x Reserved

Device 0 Offset 6D - DRAM Drive Strength (00h) .....RW

7 ESDRAM Memory Type
- 0 Disable .....default
- 1 Enable

6-5 Delay DRAM Read Latch
- 00 No Delay .....default
- 01 0.5 ns
- 10 1.0 ns
- 11 1.5 ns

4 Memory Data Drive (MD, MECC)
- 0 6 mA .....default
- 1 8 mA

3 SDRAM Command Drive (SRAS#, SCAS#, SWE#)
- 0 16mA .....default
- 1 24mA

2 Memory Address Drive (MA, WE#)
- 0 16mA .....default
- 1 24mA

1 CAS# Drive
- 0 8 mA .....default
- 1 12 mA

0 RAS# Drive
- 0 16mA .....default
- 1 24mA

PCI Bus Control

These registers are normally programmed once at system initialization time.

Device 0 Offset 70 - PCI Buffer Control (00h).....RW

7 CPU to PCI Post-Write
- 0 Disable .....default
- 1 Enable

6 PCI Master to DRAM Post-Write
- 0 Disable .....default
- 1 Enable

5 Reserved ..... always reads 0

4 PCI Master to DRAM Prefetch
- 0 Disable .....default
- 1 Enable

3 Enhance CPU-to-PCI Write
- 0 Normal operation .....default
- 1 Reduce 1 cycle when the CPU-to-PCI buffer becomes available after being full (PCI and AGP buses)

2 PCI Master Read Caching
- 0 Disable .....default
- 1 Enable

1 Delay Transaction
- 0 Disable .....default
- 1 Enable

0 Slave Device Stopped Idle Cycle Reduction
- 0 Normal Operation.....default
- 1 Reduce 1 PCI idle cycle when stopped by a slave device (PCI and AGP buses)

Device 0 Offset 71 - CPU to PCI Flow Control 1 (00h) . RW

7 Dynamic Burst
- 0 Disable..... default
- 1 Enable (see note under bit-3 below)

6 Byte Merge
- 0 Disable..... default
- 1 Enable

5 Reserved .....always reads 0

4 PCI I/O Cycle Post Write
- 0 Disable..... default
- 1 Enable

3 PCI Burst
- 0 Disable..... default
- 1 Enable (bit7=1 will override this option)

bit-7	bit-3	Operation
0	0	Every write goes into the write buffer and no PCI burst operations occur.
0	1	If the write transaction is a burst transaction, the information goes into the write buffer and burst transfers are later performed on the PCI bus. If the transaction is not a burst, PCI write occurs immediately (after a write buffer flush).
1	x	Every write transaction goes to the write buffer; burstable transactions will then burst on the PCI bus and non-burstable won't. This is the normal setting.

2 PCI Fast Back-to-Back Write
- 0 Disable..... default
- 1 Enable

1 Quick Frame Generation
- 0 Disable..... default
- 1 Enable

0 1 Wait State PCI Cycles
- 0 Disable..... default
- 1 Enable

Device 0 Offset 72 - CPU to PCI Flow Control 2 (00h) RWC

7 Retry Status
- 0 No retry occurred .....default
- 1 Retry occurred..... **write 1 to clear**

6 Retry Timeout Action
- 0 Retry Forever (record status only).....default
- 1 Flush buffer for write or return all 1s for read

5-4 Retry Limit
- 00 Retry 2 times .....default
- 01 Retry 16 times
- 10 Retry 4 times
- 11 Retry 64 times

3 Clear Failed Data and Continue Retry
- 0 Flush the entire post-write buffer .....default
- 1 When data is posting and master (or target) abort fails, pop the failed data if any, and keep posting

2 CPU Backoff on PCI Read Retry Failure
- 0 Disable .....default
- 1 Backoff CPU when reading data from PCI and retry fails

1 Reduce 1T for FRAME# Generation
- 0 Disable .....default
- 1 Enable

0 Reduce 1T for CPU read PCI slave
- 0 Disable .....Default
- 1 Enable

Device 0 Offset 73 - PCI Master Control 1 (00h)..... RW

7 Reserved .....always reads 0

6 PCI Master 1-Wait-State Write
- 0 Zero wait state TRDY# response..... default
- 1 One wait state TRDY# response

5 PCI Master 1-Wait-State Read
- 0 Zero wait state TRDY# response..... default
- 1 One wait state TRDY# response

4 Reserved .....always reads 0

3 Assert STOP# after PCI Master Write Timeout
- 0 Disable..... default
- 1 Enable

2 Assert STOP# after PCI Master Read Timeout
- 0 Disable..... default
- 1 Enable

1 LOCK# Function
- 0 Disable..... default
- 1 Enable

0 PCI Master Broken Timer Enable
- 0 Disable..... default
- 1 Enable. Force into arbitration when there is no FRAME# 16 PCICLK's after the grant.

Device 0 Offset 74 - PCI Master Control 2 (00h)..... RW

7 PCI Master Read Prefetch by Enhance Command
- 0 Always Prefetch..... default
- 1 Prefetch only if Enhance command

6 Reserved (Do Not Program).....default = 0

5 Reserved .....always reads 0

4 Dummy Request.....default = 0

3 PCI Delay Transaction Timeout
- 0 Disable..... default
- 1 Enable

2 Backoff CPU Immediately on CPU-to-AGP
- 0 Disable..... default
- 1 Enable

1-0 CPU/PCI Master Latency Timer Control
- 00 AGP master reloads MLT timer ..... default
- 01 AGP master falling edge reloads MLT timer
- 10 AGP master rising edge resets timer to 00 and AGP master falling edge reloads MLT timer
- 11 Reserved (do not program)

Device 0 Offset 75 - PCI Arbitration 1 (00h) .....RW

7 Arbitration Mechanism
- 0 PCI has priority .....default
- 1 Fair arbitration between PCI and CPU

6 Arbitration Mode
- 0 REQ-based (arbitrate at end of REQ#)...default
- 1 Frame-based (arbitrate at FRAME# assertion)

5-4 Latency Timer ..... read only, reads Rx0D bits 2:1

3-0 PCI Master Bus Time-Out

(force into arbitration after a period of time)
- 0000 Disable .....default
- 0001 1x32 PCICLKs
- 0010 2x32 PCICLKs
- 0011 3x32 PCICLKs
- 0100 4x32 PCICLKs
- ... ...
- 1111 15x32 PCICLKs

Device 0 Offset 76 - PCI Arbitration 2 (00h)..... RW

7 PCI CPU-to-PCI Post-Write Retry Failed
- 0 Continue retry attempt ..... default
- 1 Go to arbitration

6 CPU Latency Timer Bit-0 .....RO
- 0 CPU has at least 1 PCLK time slot when CPU has PCI bus
- 1 CPU has no time slot

5-4 Master Priority Rotation Control
- 0x Grant to CPU after every PCI master grant ....def=00
- 10 Grant to CPU after every 2 PCI master grants
- 11 Grant to CPU after every 3 PCI master grants

Setting 0x: the CPU will always be granted access after the current bus master completes, no matter how many PCI masters are requesting.

Setting 10: if other PCI masters are requesting during the current PCI master grant, the highest priority master will get the bus after the current master completes, but the CPU will be guaranteed to get the bus after that master completes.

Setting 11: if other PCI masters are requesting, the highest priority will get the bus next, then the next highest priority will get the bus, then the CPU will get the bus.

In other words, with the above settings, even if multiple PCI masters are continuously requesting the bus, the CPU is guaranteed to get access after every master grant (01), after every other master grant (10) or after every third master grant (11).

3-2 Select REQn to RQ4 mappin
- 00 REQ4
- 01 REQ0
- 10 REQ1
- 11 REQ2

1 CPU-to-PCI QW High DW Read Access to PCI Slave Allowed to be Backed Off
- 0 Disable..... default
- 1 Enable

0 Enable RQ4 as High Priority Master
- 0 Disable..... default
- 1 Enable

Device 0 Offset 77 - Chip Test Mode (00h) .....RW

7 Reserved (no function)..... always reads 0
6-0 Reserved (do not use)..... default=0

Device 0 Offset 78 - PMU Control I (00h).....RW

7 I/O Port 22 Access
0 CPU access to I/O address 22h is passed on to the PCI bus .....default
1 CPU access to I/O address 22h is processed internally
6 Suspend Refresh Type
0 CBR Refresh .....default
1 Self Refresh
5 Reserved ..... always reads 0
4 Dynamic Clock Control
0 Normal (clock is always running).....default
1 Clock to various internal functional blocks is disabled when those blocks are not being used
3 Reserved ..... always reads 0
2 GSTOP# Assertion
0 Disable (GSTOP# is always high).....default
1 Enable (GSTOP# could be low)
1 Reserved ..... always reads 0
0 Memory Clock Enable (CKE) Function
0 CKE Function Disable.....default
1 CKE Function Enable

Device 0 Offset 79 - PMU Control 2 (00h) .....RW

7 Cache Controller Module Clock Dynamic Stop
0 Disable .....default
1 Enable
6 DRAM Controller Module Clock Dynamic Stop
0 Disable .....default
1 Enable
5 AGP Controller Module Clock Dynamic Stop
0 Disable .....default
1 Enable
4 PCI Controller Module Clock Dynamic Stop
0 Disable .....default
1 Enable
3 Pseudo Power Good
0 Disable .....default
1 Enable
2 Indicate SIO Request to DRAM Controller
0 Disable .....default
1 Enable
1-0 Reserved ..... always reads 0

Device 0 Offset 7A – Miscellaneous Control 1 (00h)..... RW

7 No Time-Out Arbitration for Consecutive Frame Accesses
0 Enable ..... default
1 Disable
6-5 Reserved ..... always reads 0
4 Invalidate PCI / AGP Buffered (Cached) Read Data for CPU to PCI / AGP Accesses
0 Enable ..... default
1 Disable
3 Background PCI-to-PCI Write Cycle Mode
0 Enable ..... default
1 Disable
2-1 Reserved ..... always reads 0
0 South Bridge PCI Master Force Timeout When PCI Master Occupancy Timer Is Up
0 Disable ..... default
1 Enable

Device 0 Offset 7B – Miscellaneous Control 2 (02h)..... RW

7-2 Reserved ..... always reads 0
1 PCI Master Access PMRDY Select
0 Tail
1 Head **..... default**
0 PCI Bus Operating Freq.....strapped from MAB5#
0 33 MHz..... default
1 66 MHz

Device 0 Offset 7E – PLL Test Mode (00h) ..... RW

7-6 Reserved (status) .....RO
5-0 Reserved (do not use) ..... default=0

Device 0 Offset 7F – PLL Test Mode (00h) ..... RW

7-0 Reserved (do not use) ..... default=0

GART / Graphics Aperture Control

The function of the Graphics Address Relocation Table (GART) is to translate virtual 32-bit addresses issued by an AGP device into 4K-page based physical addresses for system memory access. In this translation, the upper 20 bits (A31-A12) are remapped, while the lower 12 address bits (A11-A0) are used unchanged.

A one-level fully associative lookup scheme is used to implement the address translation. In this scheme, the upper 20 bits of the virtual address are used to point to an entry in a page table located in system memory. Each page table entry contains the upper 20 bits of a physical address (a "physical page" address). For simplicity, each page table entry is 4 bytes. The total size of the page table depends on the GART range (called the "aperture size") which is programmable in the VT8605 / 86C370.

This scheme is shown in the figure below.

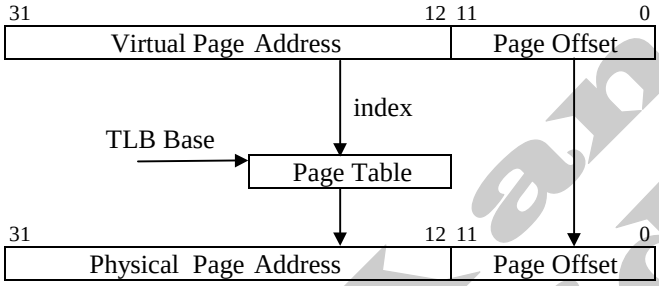


Figure 5. Graphics Aperture Address Translation

Since address translation using the above scheme requires an access to system memory, an on-chip cache (called a "Translation Lookaside Buffer" or TLB) is utilized to enhance performance. The TLB in the VT8605 / 86C370 contains 16 entries. Address "misses" in the TLB require an access of system memory to retrieve translation data. Entries in the TLB are replaced using an LRU (Least Recently Used) algorithm.

Addresses are translated only for accesses within the "Graphics Aperture" (GA). The Graphics Aperture can be any power of two in size from 1MB to 256MB (i.e., 1MB, 2MB, 4MB, 8MB, etc). The base of the Graphics Aperture can be anywhere in the system virtual address space on an address boundary determined by the aperture size (e.g., if the aperture size is 4MB, the base must be on a 4MB address boundary). The Graphics Aperture Base is defined in register offset 10 of device 0. The Graphics Aperture Size and TLB Table Base are defined in the following register group (offsets 84 and 88 respectively) along with various control bits.

Device 0 Offset 83-80 - GART/TLB Control (00000000h) RW

31-16 Reserved ..... always reads 0

15-8 Reserved (test mode status) ..... RO

7 Flush Page TLB
- 0 Disable ..... default
- 1 Enable

6-4 Reserved (always program to 0) ..... RW

3 PCI Master Address Translation for GA Access
- 0 Addresses generated by PCI Master accesses of the Graphics Aperture will not be translated default
- 1 PCI Master GA addresses will be translated

2 AGP Master Address Translation for GA Access
- 0 Addresses generated by AGP Master accesses of the Graphics Aperture will not be translated default
- 1 AGP Master GA addresses will be translated

1 CPU Address Translation for GA Access
- 0 Addresses generated by CPU accesses of the Graphics Aperture will not be translated ..... def
- 1 CPU GA addresses will be translated

0 AGP Address Translation for GA Access
- 0 Addresses generated by AGP accesses of the Graphics Aperture will not be translated ..... def
- 1 AGP GA addresses will be translated

Note: For any master access to the Graphics Aperture range, snoop will not be performed.

Device 0 Offset 84 - Graphics Aperture Size (00h) ..... RW

7-0 Graphics Aperture Size

11111111	1M	1111000	16M
11111110	2M	1110000	32M
11111100	4M	11000000	64M
11111000	8M	10000000	128M
		00000000	256M

Offset 8B-88 - GA Translation Table Base (00000000h) RW

31-12 Graphics Aperture Translation Table Base. Pointer to the base of the translation table in system memory used to map addresses in the aperture range (the pointer to the base of the "Directory" table).

11-3 Reserved ..... always reads 0

2 PCI Master Directly Accesses DRAM if in GART Range
- 0 Disable ..... default
- 1 Enable

1 Graphics Aperture Enable
- 0 Disable ..... default
- 1 Enable

Note: To disable the Graphics Aperture, set this bit to 0 and set all bits of the Graphics Aperture Size to 0. To enable the Graphics Aperture, set this bit to 1 and program the Graphics Aperture Size to the desired aperture size.

0 Reserved ..... always reads 0

AGP Control

Device 0 Offset A3-A0 - AGP Capability Identifier (00200002h) .....RO

31-24 Reserved ..... always reads 00
23-20 Major Specification Revision ..... always reads 0010
Major rev # of AGP spec that device conforms to
19-16 Minor Specification Revision ..... always reads 0000
Minor rev # of AGP spec that device conforms to
15-8 Pointer to Next Item..... always reads 00 (last item)
7-0 AGP ID .. (always reads 02 to indicate it is AGP)

Device 0 Offset A7-A4 - AGP Status (07000203h).....RO

31-24 Maximum AGP Requests ..... always reads 07†
Max # of AGP requests the device can manage (8)
† See also RxFC[1] and RxFD[2-0]
23-10 Reserved .....always reads 0s
9 Supports SideBand Addressing ..... always reads 1
8-6 Reserved .....always reads 0s
5 4G Supported .....(can be written at RxAE[5]
4 Fast Write Supported .....(can be written at RxAE[4]
3 Reserved .....always reads 0s
2 4X Rate Supported..... (can be written at RxAE[2])
1 2X Rate Supported..... (can be written at RxAC[3])
0 1X Rate Supported..... always reads 1

Device 0 Offset AB-A8 - AGP Command (00000000h) ..RW

31-24 Request Depth (reserved for target)...always reads 0s
23-10 Reserved .....always reads 0s
9 SideBand Addressing Enable
0 Disable .....default
1 Enable
8 AGP Enable
0 Disable .....default
1 Enable
7-6 Reserved .....always reads 0s
5 4G Enable
0 Disable .....default
1 Enable
4 Fast Write Enable
0 Disable .....default
1 Enable
3 Reserved .....always reads 0s
2 4X Mode Enable
0 Disable .....default
1 Enable
1 2X Mode Enable
0 Disable .....default
1 Enable
0 1X Mode Enable
0 Disable .....default
1 Enable

Device 0 Offset AC - AGP Control (00h)..... RW

7 AGP Disable.....RO
0 Disable..... default
1 Enable
This bit is latched from MAB9# at the rising edge of RESET#.
6 AGP Read Synchronization
0 Disable..... default
1 Enable
5 AGP Read Snoop DRAM Post-Write Buffer
0 Disable..... default
1 Enable
4 GREQ# Priority Becomes Higher When Arbiter is Parked at AGP Master
0 Disable..... default
1 Enable
3 2X Rate Supported (read also at RxA4[1])
0 Not supported ..... default
1 Supported
2 LPR In-Order Access (Force Fence)
0 Fence/Flush functions not guaranteed. AGP read requests (low/normal priority and high priority) may be executed before previously issued write requests. ..... default
1 Force all requests to be executed in order (automatically enables Fence/Flush functions). Low (i.e., normal) priority AGP read requests will never be executed before previously issued writes. High priority AGP read requests may still be executed prior to previously issued write requests as required.
1 AGP Arbitration Parking
0 Disable..... default
1 Enable (GGNT# remains asserted until either GREQ# de-asserts or data phase ready)
0 AGP to PCI Master or CPU to PCI Turnaround Cycle
0 2T or 3T Timing ..... default
1 1T Timing

Device 0 Offset AD – AGP Latency Timer (02h).....RW

7-5 Reserved ..... always reads 0
4 Choose First or Last Ready of DRAM
0 Last ready chosen.....default
1 First ready chosen
3-0 AGP Data Phase Latency Timer..... default = 02h

Device 0 Offset AE – AGP Miscellaneous Control (00h)RW

7-6 Reserved ..... always reads 0
5 4G Supported
0 4G not supported.....default
1 4G supported
4 Fast Write Supported
0 Fast Write not supported .....default
1 Fast Write supported
3 Reserved ..... always reads 0
2 4x Rate Supported
0 4x Rate not supported.....default
1 4x Rate supported
1-0 Reserved ..... always reads 0

Device 0 Offset B0 – AGP Pad Control / Status (8xh)....RW

7 AGP 4x Strobe VREF Control
0 STB VREF is STB# and vice versa
1 STB VREF is AGPREF **.....default**
6 AGP 4x Strobe & GD Pad Drive Strength
0 Drive strength set to compensation circuit default.....default
1 Drive strength controlled by RxB1[7-0]
5-3 AGP Compensation Circuit N Control Output .RO
2-0 AGP Compensation Circuit P Control Output .RO

Device 0 Offset B1 – AGP Drive Strength (63h).....RW

7-4 AGP Output Buffer Drive Strength N Ctrl ... def=6
3-0 AGP Output Buffer Drive Strength P Ctrl.... def=3

Device 0 Offset E0 – Miscellaneous Control (00h)..... RW

7-6 Reserved .....always reads 0
5 Enable internal graphics and AGP/CPU-to-PCI2 concurrent access
0 Disable..... default
1 Enable
3-1 Indicate which bank that Frame Buffer is loacted
000 FB located in bank 0..... default
001 FB located in bank 1
010 FB located in bank 2
011 FB located in bank 3
101 FB located in bank 4
110 Reserved
111 Reserved

0 Latch DRAM Data Using
0 Internal DRAM DCLK ..... default
1 External Feedback DRAM DCLK

Device 0 Offset F7-F0 – BIOS Scratch Registers ..... RW

7-0 No hardware function .....default = 0

Device 0 Offset F8 – DRAM Arbitration Timer (00h)... RW

7-4 AGP Timer .....default = 0
3-0 Host CPU Timer .....default = 0

Device0 Offset F9 – FB – Reserved

Device 0 Offset FC – Back Door Control 1 (00h)..... RW

7-4 Priority Timer.....default = 0
3-2 Reserved (Do Not Program) .....default = 0
1 Back-Door Max # of AGP Requests.....default = 0
0 Read of RxA7 always returns a value of 7... def
1 Read of RxA7 returns the value programmed in RxFD[2-0]
0 Back-Door Device ID Enable.....default = 0
0 Use Rx3-2 value for Rx3-2 readback..... default
1 Use RxFE-FF Back-Door Device ID for Rx3-2 read

Device 0 Offset FD – Back-DoorControl 2 (00h) ..... RW

7-5 Reserved .....always reads 0
4-0 Max # of AGP Requests .....default = 0
(see also RxA7 and RxFC[1])

Device 0 Offset FF-FE – Back-Door Device ID (0000h) RW

15-0 Back-Door Device ID.....default=00

Device 1 Register Descriptions

Device 1 Header Registers - PCI-to-PCI Bridge

All registers are located in PCI configuration space. They should be programmed using PCI configuration mechanism 1 through CF8 / CFC with bus number of 0 and function number equal to 0 and device number equal to one.

Device 1 Offset 1-0 - Vendor ID (1106h) .....RO

15-0 ID Code (reads 1106h to identify VIA Technologies)

Device 1 Offset 3-2 - Device ID (TBDh).....RO

15-0 ID Code (reads TBDh to identify the VT8605 / 86C370 PCI-to-PCI Bridge device)

Device 1 Offset 5-4 – Command (0007h) .....RW

15-10 Reserved ..... always reads 0

9 Fast Back-to-Back Cycle Enable ..... RO
- 0 Fast back-to-back transactions only allowed to the same agent .....default
- 1 Fast back-to-back transactions allowed to different agents

8 SERR# Enable..... RO
- 0 SERR# driver disabled.....default
- 1 SERR# driver enabled

(SERR# is used to report parity errors if bit-6 is set).

7 Address / Data Stepping ..... RO
- 0 Device never does stepping.....default
- 1 Device always does stepping

6 Parity Error Response.....**RW**
- 0 Ignore parity errors & continue .....default
- 1 Take normal action on detected parity errors

5 VGA Palette Snoop (Not Supported)..... RO
- 0 Treat palette accesses normally .....default
- 1 Don't respond to palette writes on PCI bus (10-bit decode of I/O addresses 3C6-3C9 hex)

4 Memory Write and Invalidate Command..... RO
- 0 Bus masters must use Mem Write .....default
- 1 Bus masters may generate Mem Write & Inval

3 Special Cycle Monitoring ..... RO
- 0 Does not monitor special cycles .....default
- 1 Monitors special cycles

2 Bus Master .....**RW**
- 0 Never behaves as a bus master
- 1 Enable to operate as a bus master on the primary interface on behalf of a master on the secondary interface .....default

1 Memory Space.....**RW**
- 0 Does not respond to memory space
- 1 Enable memory space access .....default

0 I/O Space .....**RW**
- 0 Does not respond to I/O space
- 1 Enable I/O space access .....default

Device 1 Offset 7-6 - Status (Primary Bus) (0230h).... RWC

15 Detected Parity Error .....always reads 0

14 Signaled System Error (SERR#).....always reads 0

13 Signaled Master Abort
- 0 No abort received ..... default
- 1 Transaction aborted by the master with Master-Abort (except Special Cycles) .... write 1 to clear

12 Received Target Abort
- 0 No abort received ..... default
- 1 Transaction aborted by the target with Target-Abort ..... write 1 to clear

11 Signaled Target Abort.....always reads 0

10-9 DEVSEL# Timing
- 00 Fast
- 01 Medium.....always reads 01
- 10 Slow
- 11 Reserved

8 Data Parity Error Detected .....always reads 0

7 Fast Back-to-Back Capable .....always reads 0

6 User Definable Features.....always reads 0

5 66MHz Capable.....always reads 1

4 Supports New Capability list.....always reads 1

3-0 Reserved .....always reads 0

Device 1 Offset 8 - Revision ID (00h) ..... RO

7-0 VT8605 / 86C370 Chip Revision Code (00=First Silicon)

Device 1 Offset 9 - Programming Interface (00h) ..... RO

This register is defined in different ways for each Base/Sub-Class Code value and is undefined for this type of device.

7-0 Interface Identifier .....always reads 00

Device 1 Offset A - Sub Class Code (04h).....RO

7-0 Sub Class Code .reads 04 to indicate PCI-PCI Bridge

Device 1 Offset B - Base Class Code (06h).....RO

7-0 Base Class Code.. reads 06 to indicate Bridge Device

Device 1 Offset D - Latency Timer (00h) .....RO

7-0 Reserved .....always reads 0

Device 1 Offset E - Header Type (01h) .....RO

7-0 Header Type Code.....reads 01: PCI-PCI Bridge

Device 1 Offset F - Built In Self Test (BIST) (00h) ..... RO

7 BIST Supported..... reads 0: no supported functions

6 Start Test ..... write 1 to start but writes ignored

5-4 Reserved .....always reads 0

3-0 Response Code.....0 = test completed successfully

Device 1 Offset 18 - Primary Bus Number (00h).....RW

7-0 Primary Bus Number..... default = 0

This register is read write, but internally the chip always uses bus 0 as the primary.

Device 1 Offset 19 - Secondary Bus Number (00h).....RW

7-0 Secondary Bus Number..... default = 0

Note: AGP must use these bits to convert Type 1 to Type 0.

Device 1 Offset 1A - Subordinate Bus Number (00h).....RW

7-0 Primary Bus Number..... default = 0

Note: AGP must use these bits to decide if Type 1 to Type 1 command passing is allowed.

Device 1 Offset 1B – Secondary Latency Timer (00h) ....RO

7-0 Reserved ..... always reads 0

Device 1 Offset 1C - I/O Base (f0h).....RW

7-4 I/O Base AD[15:12]..... default = 1111b

3-0 I/O Addressing Capability..... default = 0

Device 1 Offset 1D - I/O Limit (00h).....RW

7-4 I/O Limit AD[15:12] ..... default = 0

3-0 I/O Addressing Capability..... default = 0

Device 1 Offset 1F-1E - Secondary Status (0000h).....RO

15-0 Reserved ..... always reads 0

Device 1 Offset 21-20 - Memory Base (fff0h).....RW

15-4 Memory Base AD[31:20].....default = FFFh

3-0 Reserved ..... always reads 0

Device 1 Offset 23-22 - Memory Limit (Inclusive) (0000h) RW

15-4 Memory Limit AD[31:20]..... default = 0

3-0 Reserved ..... always reads 0

Device 1 Offset 25-24 - Prefetchable Memory Base (fff0h) RW

15-4 Prefetchable Memory Base AD[31:20]default = FFFh

3-0 Reserved ..... always reads 0

Device 1 Offset 27-26 - Prefetchable Memory Limit (0000h) .....RW

15-4 Prefetchable Memory Limit AD[31:20] . default = 0

3-0 Reserved ..... always reads 0

Device 1 Offset 3F-3E – PCI-to-PCI Bridge Control (0000h) ..... RW

15-4 Reserved .....always reads 0

3 VGA-Present on AGP

0 Forward VGA accesses to PCI Bus ..... default

1 Forward VGA accesses to AGP Bus

Note: VGA addresses are memory A0000-BFFFFh and I/O addresses 3B0-3BBh, 3C0-3CFh and 3D0-3DFh (10-bit decode). "Mono" text mode uses B0000-B7FFFh and "Color" Text Mode uses B8000-BFFFFh. Graphics modes use Axxxxh. Mono VGA uses I/O addresses 3Bx-3Cxh and Color VGA uses 3Cx-3Dxh. If an MDA is present, a VGA will not use the 3Bxh I/O addresses and B0000-B7FFFh memory space; if not, the VGA will use those addresses to emulate MDA modes.

2 Block / Forward ISA I/O Addresses

0 Forward all I/O accesses to the AGP bus if they are in the range defined by the I/O Base and I/O Limit registers (device 1 offset 1C-1D) .....default

1 Do not forward I/O accesses to the AGP bus that are in the 100-3FFh address range even if they are in the range defined by the I/O Base and I/O Limit registers.

1-0 Reserved .....always reads 0

Device 1 Configuration Registers - PCI-to-PCI Bridge

AGP Bus Control

Device 1 Offset 40 - CPU-to-AGP Flow Control 1 (00h)RW

7 CPU-AGP Post Write
- 0 Disable .....default
- 1 Enable

6 CPU-AGP Dynamic Burst
- 0 Disable .....default
- 1 Enable

5 CPU-AGP One Wait State Burst Write
- 0 Disable .....default
- 1 Enable

4 AGP to DRAM Prefetch
- 0 Disable .....default
- 1 Enable

3 CPU to AGP Post Write
- 0 Disable .....default
- 1 Enable

2 MDA Present on AGP
- 0 Forward MDA accesses to AGP.....default
- 1 Forward MDA accesses to PCI

Note: Forward despite IO / Memory Base / Limit

Note: MDA (Monochrome Display Adapter) addresses are memory addresses B0000h-B7FFFh and I/O addresses 3B4-3B5h, 3B8-3BAh, and 3BFh (10-bit decode). 3BC-3BE are reserved for printers.

Note: If Rx3E bit-3 is 0, this bit is a don't care (MDA accesses are forwarded to the PCI bus).

1 AGP Master Read Caching
- 0 Disable .....default
- 1 Enable

0 AGP Delay Transaction
- 0 Disable .....default
- 1 Enable

Table 5. VGA/MDA Memory/IO Redirection

3E[3] VGA Pres.	40[2] MDA Pres.	VGA is on	MDA is on	Axxxx, B8xxx Access	B0000 -B7FFF Access	3Cx, 3Dx I/O	3Bx I/O
0	-	PCI	PCI	PCI	PCI	PCI	PCI
1	0	AGP	AGP	AGP	AGP	AGP	AGP
1	1	AGP	PCI	AGP	PCI	AGP	PCI

Device 1 Offset 41 - CPU-to-AGP Flow Control 2 (00h) RW

7 Retry Status
- 0 No retry occurred..... default
- 1 Retry Occurred .....**write 1 to clear**

6 Retry Timeout Action
- 0 No action taken except to record status ..... def
- 1 Flush buffer for write or return all 1s for read

5-4 Retry Count
- 00 Retry 2, backoff CPU ..... default
- 01 Retry 4, backoff CPU
- 10 Retry 16, backoff CPU
- 11 Retry 64, backoff CPU

3 Post Write Data on Abort
- 0 Flush entire post-write buffer on target-abort or master abort..... default
- 1 Pop one data output on target-abort or master-abort

2 CPU Backoff on AGP Read Retry Timeout
- 0 Disable..... default
- 1 Enable

1-0 Reserved .....always reads 0

Device 1 Offset 42 - AGP Master Control (00h) ..... RW

7 Read Prefetch for Enhance Command
- 0 Always Perform Prefetch..... default
- 1 Prefetch only if Enhance Command

6 AGP Master One Wait State Write
- 0 Disable..... default
- 1 Enable

5 AGP Master One Wait State Read
- 0 Disable..... default
- 1 Enable

4 Extend AGP Internal Master for Efficient Handling of Dummy Request Cycles
- 0 Disable..... default
- 1 Enable

This bit is normally set to 1.

3 AGP Delay Transaction Timeout
- 0 Disable..... default
- 1 Enable

2 Prefetch Disable when Delay Transaction Occured
- 0 Normal operation..... default
- 1 Disable prefetch when doing fast response to the previous delay transaction or doing read caching

1 Reserved .....always reads 0

0 Shorten AGP Master to TRFCTL
- 0 Disable..... default
- 1 Enable

Device 1 Offset 43 - AGP Master Latency Timer (00h) RW

7-4 Host to AGP Time slot
- 0 Disable (no timer).....default
- 1 16 GCLKs
- 2 32 GCLKs
- … …
- F 128 GCLKs

3-0 AGP Master Time Slot
- 0 Disable (no timer).....default
- 1 16 GCLKs
- 2 32 GCLKs
- … …
- F 128 GCLKs

Device 1 Offset 44 – Backdoor Register Control (00h) .RW

7-1 Reserved ..... always reads 0

0 Back Door Register
- 0 Disable .....default
- 1 Enable

Device 1 Offset 45 – Fast Write Control (72h).....RW

7 Force Fast Write Cycle to be QW Aligned (if Rx45[6] = 0)
- 0 Disable .....default
- 1 Enable

6 Merge Multiple CPU Transactions Into One Fast Write Burst Transaction
- 0 Disable
- 1 Enable**.....default**

5 Merge Multiple CPU Write Cycles To Memory Offset 23-20 Into Fast Write Burst Cycles (if Rx45[6] = 0)
- 0 Disable
- 1 Enable**.....default**

4 Merge Multiple CPU Write Cycles To Prefetchable Memory Offset 27-24 Into Fast Write Burst Cycles (if Rx45[6] = 0)
- 0 Disable
- 1 Enable**.....default**

3 Reserved ..... always reads 0

2 Fast Write Burst 4T Max (No Slave Flow Control)
- 0 Disable .....default
- 1 Enable

1 Fast Write Fast Back to Back
- 0 Disable
- 1 Enable**.....default**

0 Fast Write Initial Block 1 Wait State
- 0 Disable .....default
- 1 Enable

Rx45 Bits 7-4	CPU Write Address in Mem1	CPU Write Address in Mem2	Fast Write Cycle Alignment
x1xx	-	-	QW aligned, burstable
0000	-	-	DW aligned, nonburstable
x010	0	0	n/a
0010	0	1	DW aligned, non-burstable
x010	1	-	QW aligned, burstable
x001	0	0	n/a
x001	-	1	QW aligned, burstable
0001	1	0	DW aligned, non-burstable
x011	0	0	n/a
x011	1	-	QW aligned, burstable
x011	0	1	QW aligned, burstable
1000	-	-	QW aligned, non-burstable
1010	0	1	QW aligned, non-burstable
1001	1	0	QW aligned, non-burstable

Device 1 Offset 47-46 – PCI-to-PCI Bridge Device ID .. RW

15-0 PCI-to-PCI Bridge Device ID ..... default = 0000

Device 1 Offset 80 – Capability ID (01h) ..... RO

7-0 Capability ID ..... always reads 01h

Device 1 Offset 81 – Next Pointer (00h) ..... RO

7-0 Next Pointer: Null..... always reads 00h

Device 1 Offset 82 – Power Mgmt Capabilities 1 (02h) .. RO

7-0 Power Mgmt Capabilities ..... always reads 02h

Device 1 Offset 83 – Power Mgmt Capabilities 2 (00h) .. RO

7-0 Power Mgmt Capabilities ..... always reads 00h

Device 1 Offset 84 – Power Mgmt Ctrl/Status (00h)..... RW

7-2 Reserved ..... always reads 0

1-0 Power State
- 00 D0 ..... default
- 01 -reserved-
- 10 -reserved-
- 11 D3 Hot

Device 1 Offset 85 – Power Mgmt Status (00h)..... RO

7-0 Power Mgmt Status ..... default = 00

Device 1 Offset 86 – P2P Br. Support Extensions (00h) . RO

7-0 P2P Bridge Support Extensions..... default = 00

Device 1 Offset 87 – Power Management Data (00h) ..... RO

7-0 Power Management Data..... default = 00

FUNCTIONAL DESCRIPTION - INTEGRATED SAVAGE4 GRAPHICS

Configuration Strapping

Certain VT8605 / 86C370 graphics functions have options that must be selected and fixed at reset (before the register bits controlling these functions can be programmed by software). This is accomplished via power-on configuration strapping.

The strapping pins are pulled low internally and can be individually pulled high through 10 KOhm resistors. These pull-ups and pull-downs do not affect normal operation of the pins, but they do force the pins to a definite state during reset. At the rising edge of the reset signal, this state is sampled, the result is inverted and the data loaded into the CR36, CR37 and CRB0 registers. The data is used for system configuration. The definitions of the strapping bits at the rising edge of the reset signal are shown in Table 6.

Pin Name	Pin #	CR Bit(s) Value	Description
MA2		CR36[0]	**PCI Interrupt**
			Disable INTA# claim (00H in PCI3D)
			Enable INTA# claim (01H in PCI3D)
MA3		CR36[4]	**IO Disable**
			Disable I/O access PCI04[0] ignored
			Enable I/O access via PCI04[0] = 1.
MA4		CRB0[7]	**PCI Base Address Mapping**
			Address Mapping 1 (varies by chip revision)
			Address Mapping 0 (PCI10, 14) (16M assigned to PCI0; 128M assigned to PCI14)

Table 6. Definition of Strapping Bits at the Rising Edge of the Reset Signal

Important Note: As described above, the signal levels on the strapping pins are inverted before being latched in the various strapping bit registers. Since the strapping pins all have internal pull-downs, the default values for each of the strapping bits is 1. The value latched at reset can be changed to 0 by adding an external pull-up to the appropriate pin. After reset, the strapping bits are written and read normally, i.e., there is no inversion of the register values.

PCI Configuration and Integrated AGP

PCI Configuration

The VT8605 / 86C370 graphics Vendor ID register (Index 00H) in the PCI Configuration space is hardwired to 5333H to specify S3 Incorporated as the vendor. The Device ID register is hardwired to 8A25H.

Bits 10-9 of the Status register (Index 06H) are hardwired to 01b to specify medium DEVSEL timing. The Class Code register (Index 08H) is hardwired to 30000xxH to specify that the VT8605 / 86C370 is a VGA compatible device.

There are two MMIO address mappings, as determined by the state of CRB0[7]. By default, CRB0[7] = 1, which selects Mapping 0. This uses the PCI base addresses specified by PCI10 and PCI14. 16 Mbytes of address space is claimed by PCI10 and 128 Mbytes of address space is claimed by PCI14. If the MA4 pin is strapped high at reset, a 0 is latched in CRB0[7] and selects Mapping 1. This uses base addresses PCI10 (same as Mapping 0), PCI14 (redefined from Mapping 0 to claim 16 Mbytes) and adds PCI18, PCI1C, PCI20 and PCI24, each claiming 16 Mbytes. Thus, Mapping 1 allows the address space claimed to be broken up into smaller blocks, as required by some operating systems. The Base Address 0 register (Index 10H) defaults to address 7000 0000H. This is the relocatable base address for memory-mapped I/O register accessing.

PCI04[4] is hardwired to 1 to indicate a capabilities list is available. PCI34[7-0] point to the PCI power management registers starting at offset DC. The basic power states (D0-D3) are supported as explained by the PCI Bus Power Management Interface Specification, Revision 1.0.

PCI Subsystem ID

The Subsystem ID and Subsystem Vendor ID are located in a 32-bit read only register at PCI Configuration Space Index 2C. These registers reflect the content of 4 read/write CR registers as follows:

Register	CR Space	PCI Configuration Space
Subsystem Vendor ID Low Byte	CR81	Index 2CH
Subsystem Vendor ID High Byte	CR82	Index 2DH
Subsystem ID Low Byte	CR83	Index 2EH
Subsystem ID High Byte	CR84	Index 2FH

Table 7. PCI Subsystem ID and Subsystem Vendor ID Registers

These registers allow identification of particular vendors using the same graphics chip. The following design allows the subsystem identification to be handled by software (no hardwiring).

All VT8605 / 86C370 motherboard designs will incorporate the video BIOS into the system BIOS ROM. The system BIOS must load the subsystem ID information in the VT8605 / 86C370 before any ID scanning takes place. To do this, it must turn on the VT8605 / 86C370, enable I/O accesses in the PCI configuration space, unlock the CR registers, program the subsystem ID information in the registers described above, then turn off the VT8605 / 86C370.

Integrated AGP

VT8605 / 86C370 graphics conform with the requirements of Revision 2.0 of the AGP Interface Specification. Internal AGP VT8605 / 86C370 graphics are enabled by default (CR37[6] = 1) unless another AGP graphics device is located in the AGP4X Expansion Slot. In this case, the Expansion AGP graphics are enabled by default and the internal AGP VT8605 / 86C370 graphics are disabled. A System BIOS setting permits advanced users to override the default.

Major functions supported include:

- PIPE# and 1x/2x/4x side band addressing
- Data received at 1x/2x/4x clock rate
- Fast back to back data transfers
- Early grant
- Flow control of RBF# and throttling
- Up to 32 outstanding AGP requests
- Master read for 3D textures in system memory
- Command split function

For the most part, AGP configuration is identical to PCI configuration. PCI04[4] is hardwired to 1 to indicate that VT8605 / 86C370 graphics implements a list of capabilities. PCI34[7-0] point to the location of this list, which is at offset 80H. PCI80, PCI84 and PCI88 implement the register bits required by the AGP specification. PCI88[2-0] select the data rate. PCI88[8] = 1 enables AGP bus master operations. PCI88[9] =1 enables sideband addressing. This is indicated by PCI84[9] (1 = sideband addressing supported). The state of PCI84[9] is determined by the state of CR70[7].

Display Memory

The VT8605 / 86C370 north bridge utilizes a Shared Memory Architecture (SMA) for Frame Buffer Memory. SMA allows system memory to be efficiently shared by the host CPU and the VT8605 / 86C370 north bridge graphics controller. By default, 8 Mbytes of system memory is allocated for the graphics frame buffer, but up to 32 Mbytes may be allocated depending on user preference, application requirements, and the total size of system memory. A System BIOS setting permits advanced users to override the default and select their preferred frame buffer size. When Expansion AGP graphics are enabled, the internal AGP VT8605 / 86C370 graphics are disabled and NO frame buffer memory is allocated.

Note: Frame buffer memory is allocated from system memory at bootup time. Changing the display settings to a resolution requiring additional frame buffer memory will require a system reboot to be performed.

Frame Buffer Size	CR36[7-5] Register Setting
0 Mbytes	000
2 Mbytes	001
4 Mbytes	010
8 Mbytes	011
16 Mbytes	100
32 Mbytes	101

Table 8. Supported Frame Buffer Memory Configurations

Interrupt Generation

Whatever the mode of operation (VGA or Enhanced), bit 4 of CR32 must be set to 1 to enable interrupt generation. When an enabled interrupt is generated, INTA# is pulled low unless CR36[0] = 0 (MA2 pulled high at reset), for which case no PCI interrupt line is claimed during PCI configuration.

When VT8605 / 86C370 graphics are being operated in VGA mode (CR66[0] = 0), only vertical retrace can generate an interrupt. This is enabled when CR11[5] = 0 and CR11[4] = 1. When an interrupt occurs, it is cleared by writing a 0 to CR11[4]. The interrupt must then be re-enabled by writing a 1 to the same bit. Note that the BIOS clears both bit 4 and bit 5 of CR11 during power-on, a mode set, or a reset. Thus, interrupt generation is disabled until bit 4 is set to 1.

In Enhanced mode (CR66[0] = 1 or 3D operation), interrupts can be generated by vertical retrace, command or bus FIFO overflow, command or bus FIFO empty, or by a BCI command. These interrupts are enabled and cleared and their status reported via MM8504. Serial port interrupts are controlled via MMFF08. If interrupts are used, they should be cleared before they are enabled.

Multiple interrupts can be enabled at the same time in Enhanced mode. The interrupt pin will remain asserted until all interrupt status bits are cleared.

Display Interfaces

CRT Interface

The VT8605 / 86C370 provides the following CRT interface signals:

- AR (analog red)
- AG (analog green)
- AB (analog blue)
- HSYNC (horizontal sync)
- VSYNC (vertical sync)

In addition, DDC2 monitor communications can be implemented via the serial communications port controlled by CRB1[4]-0. These bits control two-way communications over the SPCLK2 (clock) and SPDAT2 (data) lines. The operation is the same as described for the I^2C serial communications port section except that interrupts and wait states are not supported.

External TV Encoder Interface

Figure 6 shows the interface to an external Bt868/869 TV encoder (or compatible device). The TV outputs are generated whenever the clock input from the decoder is present on the TVCLK pin and CRB0[4] = 0. The encoder is controlled via the I^2C interface. TV monitor detection is also done via this interface. The TV encoder interface and the flat panel interface are multiplexed on common pins, so only one of the two (either the TV interface or the flat panel interface) can be enabled at any given time

Figure 6. External TV Encoder Interface

The VT8605 / 86C370 supports three output formats as shown in Table 9. As shown in Figure 6, P[11:0] on the encoder connect to TVD[11:0] on the VT8605 / 86C370. The CLKI pin on the encoder connects to the TVCLKR pin on the VT8605 / 86C370.

	SR35[5-4] = 00		SR35[5-4] = 01		SR35[5-4] = 10	
Pin	CLK1 Rising	CLKI Falling	CLK1 Rising	CLKI Falling	CLK1 Rising	CLKI Falling
P11	G4	R7	B7	G3	R7	G3
P10	G3	R6	B6	G2	R6	G2
P9	G2	R5	B5	G1	R5	G1
P8	B7	R4	B4	G0	R4	G0
P7	B6	R3	B3	R7	R3	B7
P6	B5	G7	B2	R6	R2	B6
P5	B4	G6	B1	R5	R1	B5
P4	B3	G5	B0	R4	R0	B4
P3	G0	R2	G7	R3	G7	B3
P2	B2	R1	G6	R2	G6	B2
P1	B1	R0	G5	R1	G5	B1
P0	B0	G1	G4	R0	G4	B0

Table 9. External TV Encoder Output Data Formats

TFT Flat Panel TMDS Interface

Figure 7 shows the hardware connections to a receiver conforming to the DVI 1.0 or VESA TMDS standards. This interface allows the VT8605 / 86C370 to drive a TFT flat panel over considerable distance and is active when SR31[4] = 1 and CRB0[3] = 0. Panel power sequencing is controlled by the receiver components.

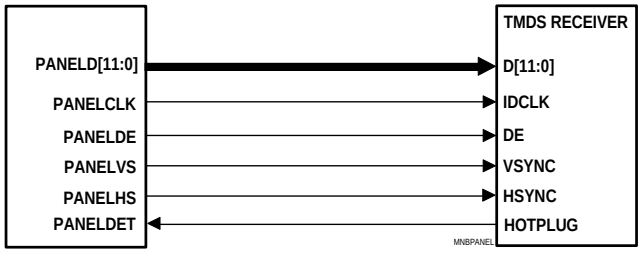


Figure 7. TMDS Interface

The VT8605 / 86C370 provides the following panel detection capability. If SR30[1] = 0 and the PANELDET pin is properly connected to a voltage source indicating the presence/absence of a panel, SR30[1] will reflect the high/low state of this input. A read of 1 indicates that a powered-up panel is connected.

For proper flat panel output with a standard VGA primary screen and the Streams Processor active, the following special register settings are required:

CR3A[4] = 1

CR67[3-2] = 01b (Streams Processor secondary and VGA primary

CR67[7-4] = desired bits/pixel mode

CR90[3] = 1 (CR0 must be programmed before this is set to 1. Setting this bit is not required for 8 bit/pixel modes)

CR90[6] = 1 (this bit must also be set to 1 for 8 bit/pixel modes)

MM8180 = 00000000H

These settings are required for correct automatic centering and expansion with Streams Processor operation.

I2C Serial Communications Port

One serial communications port is implemented in a register that can be accessed either via MMFF20 or CRA0. Bit 4 is set to 1 to enable the interface. The clock is written to bit 0 (= 0) and data to bit 1 (= 0), driving the SPCLK1 and SPDAT1 pins low respectively. The state of the SPCLK1 pin can be read via bit 2 and the state of the SPDAT1 pin can be read via bit 3. The SPCLK1 and SPDAT1 pins are tri-stated when their corresponding control bits are reset to 0, allowing other devices to drive the serial bus.

This serial port is typically used for I2C interfacing. When SPCLK1 and SPDAT1 are tri-stated, the VT8605 / 86C370 can detect an I2C start condition (SPDAT1 driven low while SPCLK1 is not driven low). This condition is generated by another I2C master that wants control of the I2C bus. If bit 19 of MMFF08 is set to 1, detection of a start condition generates an interrupt and sets bit 3 of MMFF08 to 1. If bit 24 of MMFF08 is set to 1, the VT8605 / 86C370 drives SPCLK1 low to generate I2C wait states until the Host can clear the interrupt and service the I2C bus.

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Table 10. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes
T_A	Ambient operating temperature	0	55	^oC	1
T_C	Case operating temperature	0	110	^oC	1
T_S	Storage temperature	-55	125	^oC	1
V_{IN}	Input voltage	-0.5	V_{RAIL} + 10%	Volts	1, 2
V_{OUT}	Output voltage	-0.5	V_{RAIL} + 10%	Volts	1, 2

Note 1: Stress above the conditions listed may cause permanent damage to the device. Functional operation of this device should be restricted to the conditions described under operating conditions.

Note 2. V_{RAIL} is defined as the V_{CC} level of the respective rail. The CPU interface can be 3.3V or 2.5V. Memory can be 3.3V only. PCI can be 3.3V or 5.0V. Video can be 3.3V or 5.0V. Flat Panel can be 3.3V only.

DC Characteristics

T_A = 0-70^{o}C, V_{RAIL} = V_{CC} +/- 5%, V_{CORE} = 2.5V +/- 5%, GND=0V

Table 11. DC Characteristics

Symbol	Parameter	Min	Max	Unit	Condition
V_{IL}	Input Low Voltage	-0.50	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}+0.5	V	
V_{OL}	Output Low Voltage	-	0.55	V	I_{OL}=4.0mA
V_{OH}	Output High Voltage	2.4	-	V	I_{OH}=-1.0mA
I_{IL}	Input Leakage Current	-	+/-10	uA	$0<V_{IN}<V_{CC}$
I_{OZ}	Tristate Leakage Current	-	+/-20	uA	$0.55<V_{OUT}<V_{CC}$
I_{CC}	Power Supply Current	-		mA	

AC Timing Specifications

AC timing specifications provided are based on external zero-pf capacitance load. Min/max cases are based on the following table:

Table 12. AC Timing Min / Max Conditions

Parameter	Min	Max	Unit
5.0V Power	4.75	5.25	Volts
3.3V Power	3.135	3.465	Volts
2.5V Power	2.375	2.625	Volts
Temperature	0	55	^oC

Drive strength for selected output pins is programmable. See Rx6D for details.

MECHANICAL SPECIFICATIONS

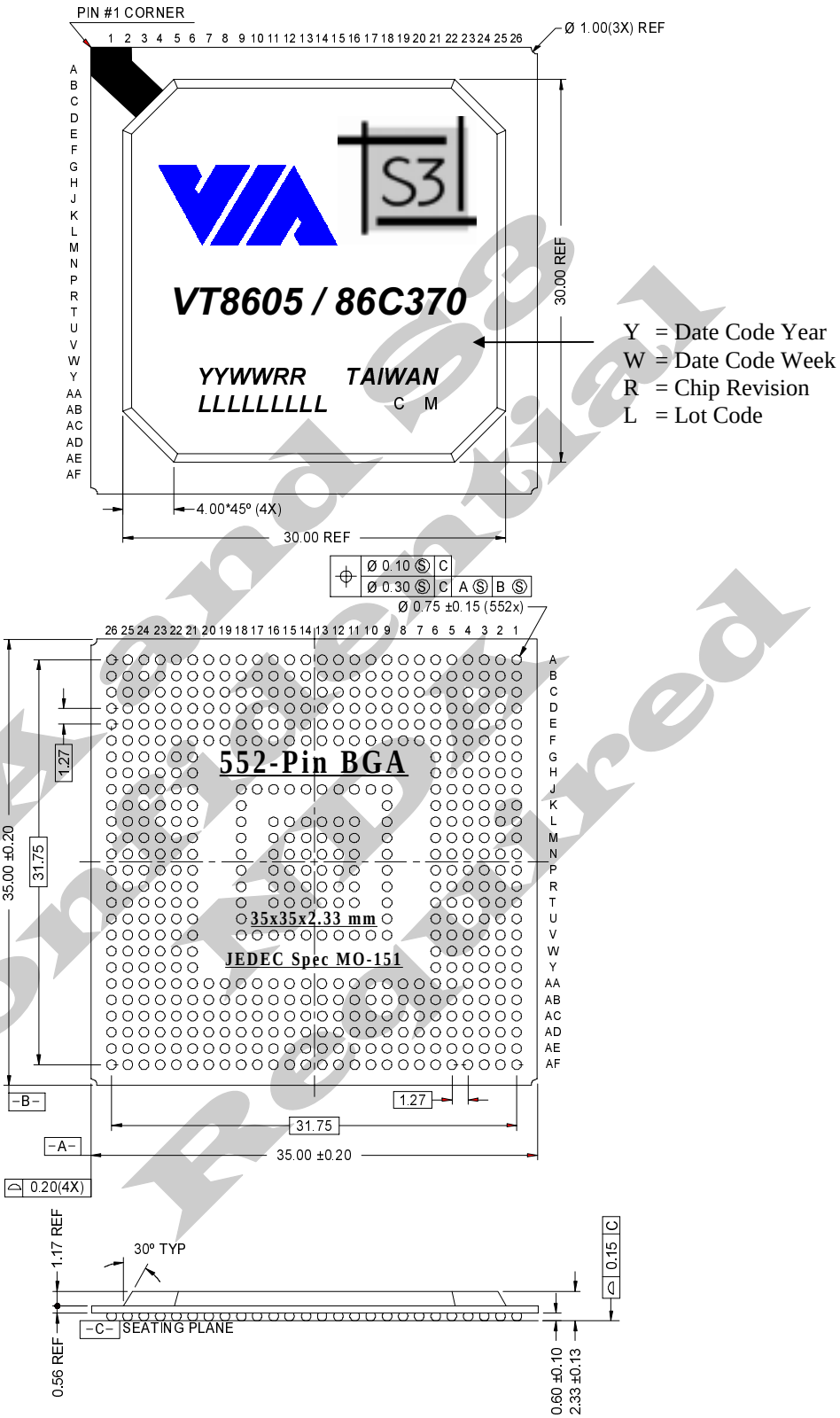


Figure 8. Mechanical Specifications - 552-Pin Ball Grid Array Package