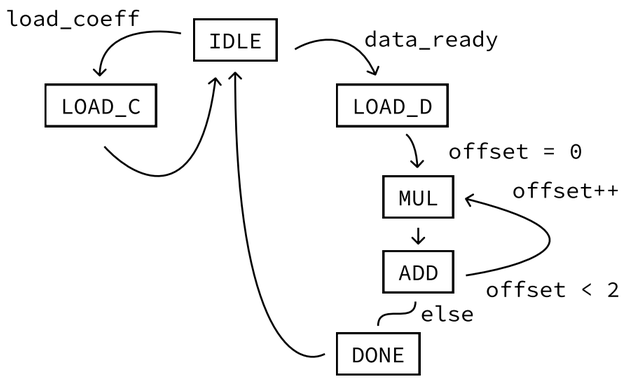
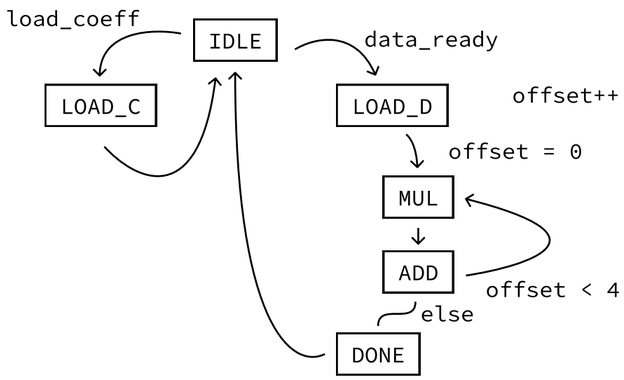
State Transition Diagram (2 sample)



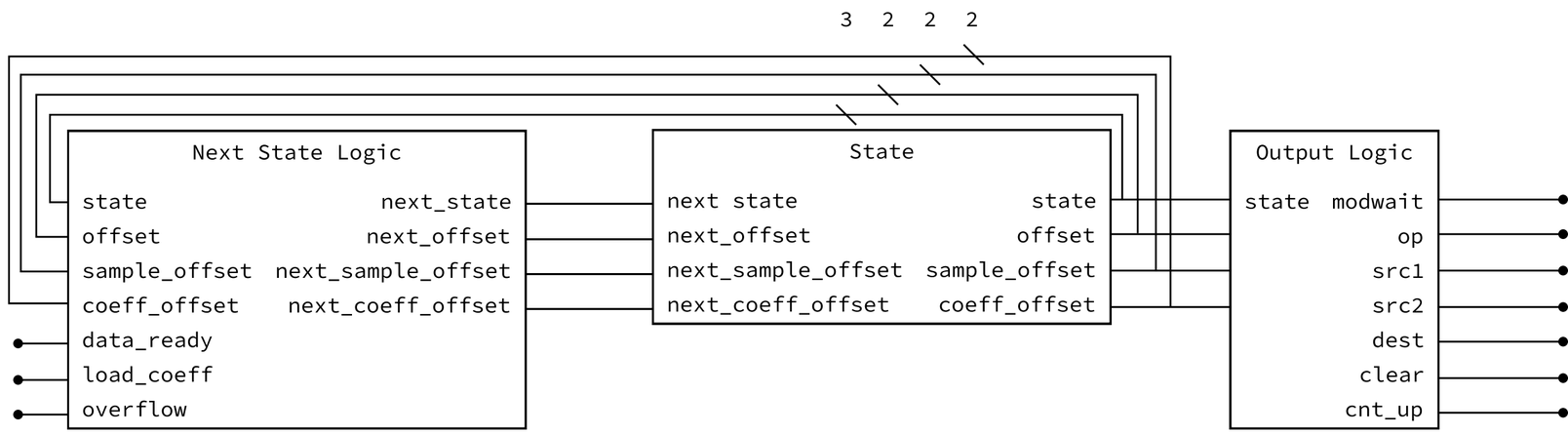
Psuedocode

```
IDLE:  next_state  <= data_ready ? LOADD :  load_coeff ? LOADC : IDLE;

EIDLE: next_state  <= data_ready ? LOADD :  load_coeff ? LOADC : EIDLE;

LOADC: next_state  <= IDLE;
       next_coeff_offset <= coeff_offset + 1;

LOADD: next_state  <= M;
       next_offset <= 0;
       next_sample_offset <= sample_offset == 0 ? 2'b11 : sample_offset - 1;
       LOAD: R[sample_offset] <= ext_in1

M:     next_state  <= overflow ? EIDLE : A;
       MUL: R[TEMP_REG] <= R[((sample_offset + offset + 1) % 4) + 1], R[offset + 5]

A:     next_state  <= overflow ? EIDLE : &offset ? DONE : M;
       next_offset <= offset + 1;
       (offset % 2 == 0 ? SUB : ADD): R[ACC_REG] <= R[TEMP_REG], R[offset == 0 ? ZERO_REG : ACC_REG]

DONE:  next_state  <= overflow ? EIDLE : IDLE;
       next_offset <= 0;
       COPY: R[0] <= R[ACC_REG]
```

State Transition Diagram (4 sample)



Controller RTL



Magnitude Schematic