Report of CS220 Assignment 2

Anushka Panda Harshit Raj Shubhan R

February 6, 2022

1 About

- About Assignment

  Name: Assignment 2
  Due on: Feb 6, 2022

- Team

  Name: Anushka Panda
  Email: apanda20@iitk.ac.in
  Roll: 200174

  Name: Harshit Raj
  Email: harshitr20@iitk.ac.in
  Roll: 200433

  Name: Shubhan R
  Email: shubhanr20@iitk.ac.in
  Roll: 200971

- About Course

  Course Code: CS220
  Name of course: Computer Organization
  Instructor: Dr. Urbi Chatterjee
  Semester: 2021-22-II

2 8 bit Carry Look-Ahead Adder

The Carry Look-Ahead Adder is an improvisation of the full-adder. The normal one bit full adder uses the below circuit.

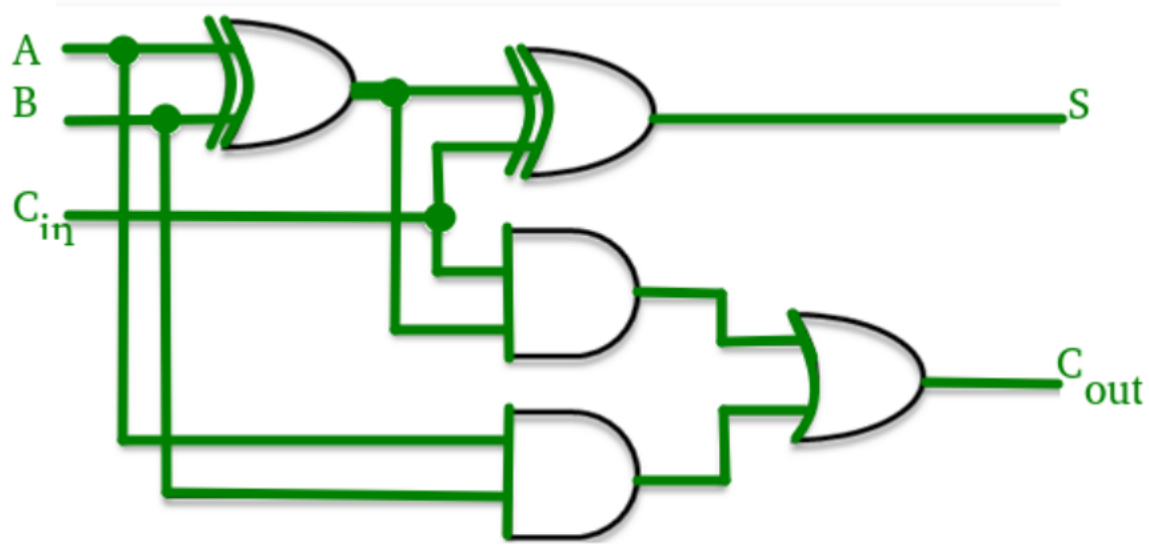

Fig 1: Normal One bit full adder

However, for multiple bit inputs, the full-adder suffers a disadvantage. In multiple bit full-adder, the C_{out} for a less significant bit serves as the C_{in} for the next most significant bit. Because of this reason, the calculation of the sum of the bits in question becomes very dependent on the availability of C_{in}, which in turn is dependent on the C_{out} for the previous bit, resulting in *significant delay* in overall calculation of S. This is where Carry-Look-Ahead adder comes in.

The main task of the carry-look-ahead adder is to calculate the sum of two n bit inputs by calculating the C_{out} for all the bits at once, which reduces delay in sum calculation significantly. Looking at the full-adder circuit diagram in detail, we see that the XOR of A and B, and the AND of A and B are being used to determine the C_{out} (along with other operations, of course).

Let,

$$P_i = A_i \oplus B_i$$

and,

$$G_i = A_i.B_i$$

where i represents the i-th bit from 0 to 7, $\oplus$ represents the XOR operation and . represents the AND operation.
Now,

$$S_i = P_i \oplus C_i$$

and

$$C_{i+1} = G_i + P_i.C_i$$

Using the above calculations, for an eight bit adder,

$$C_1 = G_0 + P_0.C_{in}$$

$$C_2 = G_1 + P_1.C_1 = G_1 + P_1.G_0 + P_1.P_0.C_{in}$$

Similarly,

$$C_3 = G_2 + P_2.G_1 + P_2.P_1.G_0 + P_2.P_1.P_0.C_{in}$$

$$\vdots$$

$$C_8 = G_7 + P_7.G_6 + P_7.P_6.G_5 \cdots + P_7.P_6.P_5.P_4.P_3.P_2.P_1.P_0.C_{in}$$

As we can see, not a single carry-out is dependent on the previous bit's carry-in, as they are all being calculated using C_{in}(the initial carry-in), and using A_i and B_i!
The diagram below shows how complicated things can get, but the efforts put in are worth the speed and efficiency of this carry-look-ahead adder.
NOTE: C_8 is just the carry-out for A_7 and B_7. It is also mentioned as C_{out} in the below circuit diagram.

2.1 Circuit Diagram

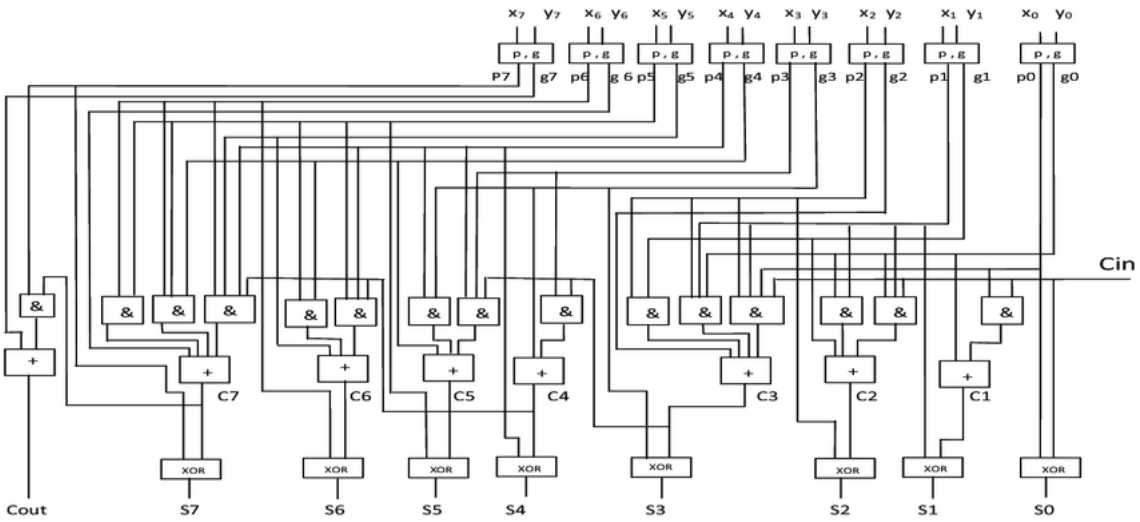

Fig 2: 8 bit Carry Look-ahead Adder

3 Johnson Counter

Johnson counter is a synchronous counter. Other names of Johnson counter are creeping counter, twisted ring counter, mobile counter and switch tail counter. In Johnson counter, the complemented output of last flip flop is connected to input of first flip flop and to implement n-bit Johnson counter we require n flip-flop. It is formed by the feedback of the output to its own input and is one of the most important types of shift register counter.

In an 8 bit Johnson counter:

- Number of used states = 16
- Number of unused states = 240

3.1 Circuit Diagram

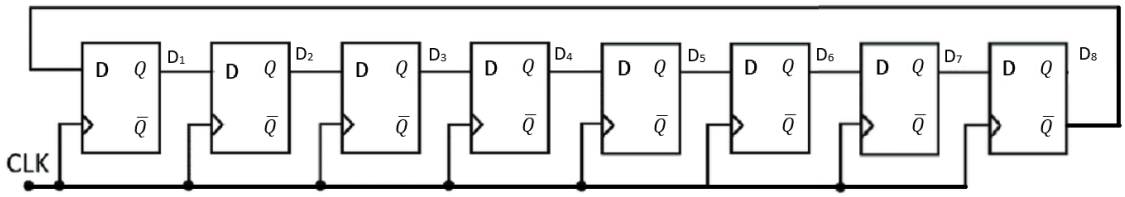

Fig 3: 8 bit Johnson Counter using D flip flops

Here, we use 8 *D flip-flops* to implement the counter. The flip-flops are connected in sequence, with input of all the flip-flops except the first one being the output of the previous flip-flop. Only for the fist flip-flop, the complement of output of last flip flop is connected.

3.2 Truth Table

Clock Input	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8
0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0
2	1	1	0	0	0	0	0	0
3	1	1	1	0	0	0	0	0
4	1	1	1	1	0	0	0	0
5	1	1	1	1	1	0	0	0
6	1	1	1	1	1	1	0	0
7	1	1	1	1	1	1	1	0
8	1	1	1	1	1	1	1	1
9	0	1	1	1	1	1	1	1
10	0	0	1	1	1	1	1	1
11	0	0	0	1	1	1	1	1
12	0	0	0	0	1	1	1	1
13	0	0	0	0	0	1	1	1
14	0	0	0	0	0	0	1	1
15	0	0	0	0	0	0	0	1
16	0	0	0	0	0	0	0	0

3.3 Advantages of Johnson Counter

Advantages of Johnson Counter are:

- It can be implemented with JK and D flip flop.
- It is a self-decoding circuit
- It is used to count data in a continuous loop.
- It has same number of flip flops but it can count twice the number of states the ring counter can count.

3.4 Disadvantages of Johnson Counter

Disadvantages of Johnson Counter are:

- It doesn't count in a binary sequence.
- More number of states remain unutilized than the number of states being utilized.
- The number of flip flops needed is one half the number of timing signals.

3.5 Applications of Johnson Counter

Applications of Johnson Counter are:

- It is used as a synchronous decade counter or divider circuit.
- It is used in hardware logic design to create complicated Finite states machine. ex: ASIC and FPGA design.
- The 3 stage Johnson counter is used as a 3 phase square wave generator which produces 1200 phase shift.
- It is also used to divide the frequency of the clock signal by varying their feedback.

4 Footnotes

- Entire code of this assignment could be found here.