1. Description

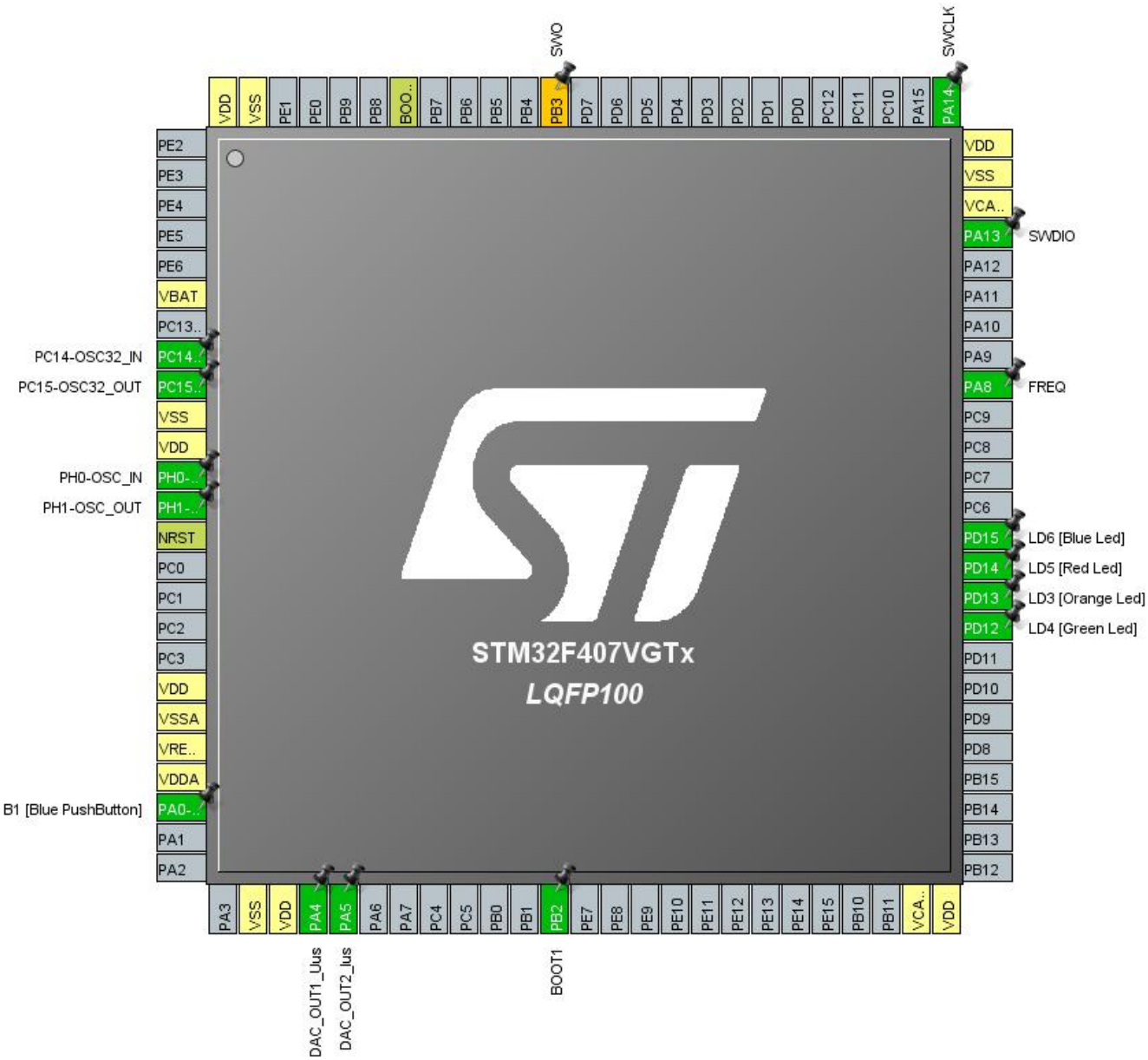
1.1. Project

Project Name	BoostWaveformGenerator
Board Name	STM32F4DISCOVERY
Generated with:	STM32CubeMX 5.0.0
Date	03/27/2019

1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F407/417
MCU name	STM32F407VGTx
MCU Package	LQFP100
MCU Pin number	100

2. Pinout Configuration

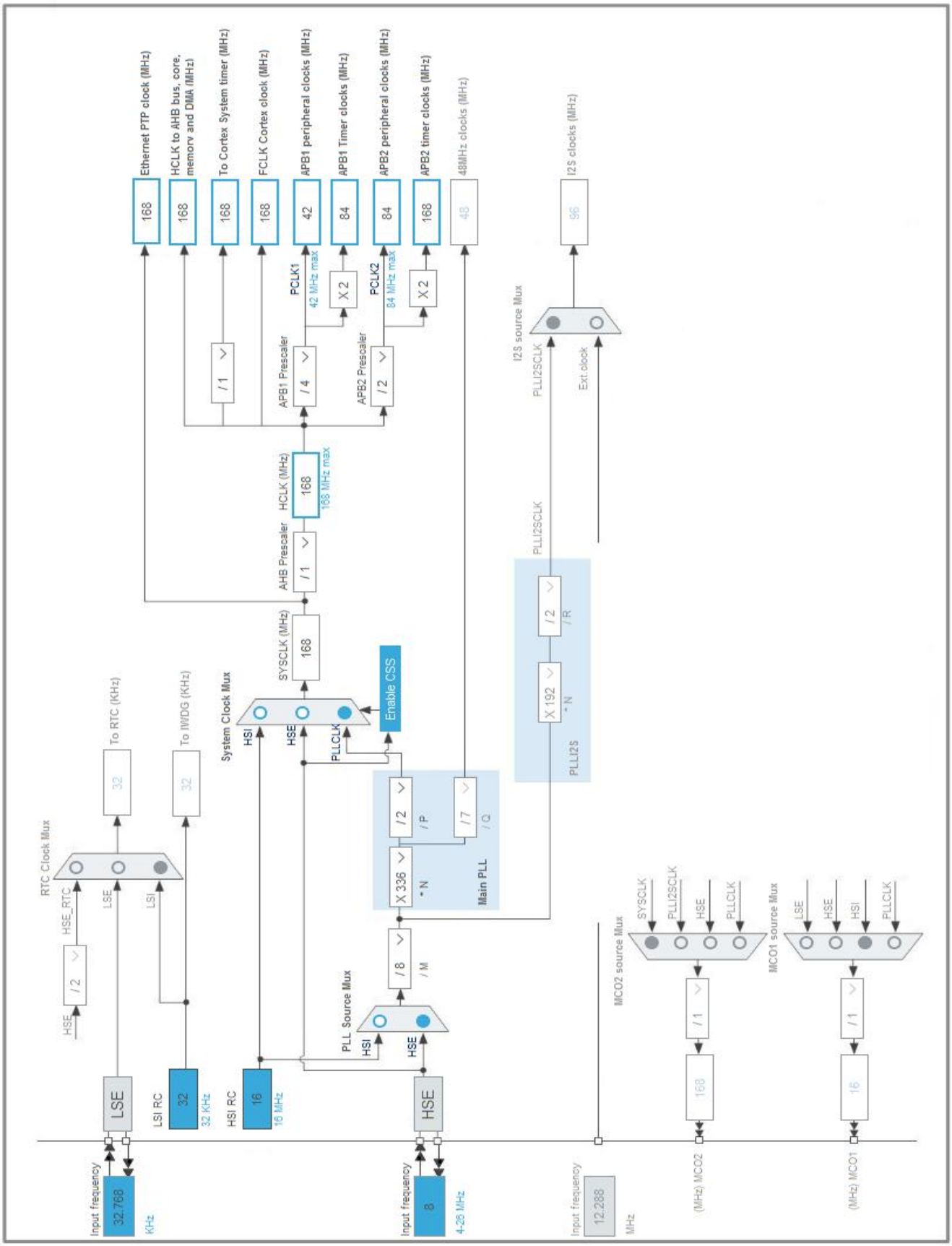


3. Pins Configuration

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
6	VBAT	Power		
8	PC14-OSC32_IN	I/O	RCC_OSC32_IN	PC14-OSC32_IN
9	PC15-OSC32_OUT	I/O	RCC_OSC32_OUT	PC15-OSC32_OUT
10	VSS	Power		
11	VDD	Power		
12	PH0-OSC_IN	I/O	RCC_OSC_IN	PH0-OSC_IN
13	PH1-OSC_OUT	I/O	RCC_OSC_OUT	PH1-OSC_OUT
14	NRST	Reset		
19	VDD	Power		
20	VSSA	Power		
21	VREF+	Power		
22	VDDA	Power		
23	PA0-WKUP	I/O	GPIO_EXTI0	B1 [Blue PushButton]
27	VSS	Power		
28	VDD	Power		
29	PA4	I/O	DAC_OUT1	DAC_OUT1_Uus
30	PA5	I/O	DAC_OUT2	DAC_OUT2_Ius
37	PB2 *	I/O	GPIO_Input	BOOT1
49	VCAP_1	Power		
50	VDD	Power		
59	PD12 *	I/O	GPIO_Output	LD4 [Green Led]
60	PD13 *	I/O	GPIO_Output	LD3 [Orange Led]
61	PD14 *	I/O	GPIO_Output	LD5 [Red Led]
62	PD15 *	I/O	GPIO_Output	LD6 [Blue Led]
67	PA8	I/O	TIM1_CH1	FREQ
72	PA13	I/O	SYS_JTMS-SWDIO	SWDIO
73	VCAP_2	Power		
74	VSS	Power		
75	VDD	Power		
76	PA14	I/O	SYS_JTCK-SWCLK	SWCLK
89	PB3 **	I/O	SYS_JTDO-SWO	SWO
94	BOOT0	Boot		
99	VSS	Power		
100	VDD	Power		

 * The pin is affected with an I/O function
** The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	BoostWaveformGenerator
Project Folder	C:\Users\gutton_b\workspace\BoostWaveformGenerator
Toolchain / IDE	TrueSTUDIO
Firmware Package Name and Version	STM32Cube FW_F4 V1.23.0

5.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	Yes

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F4
Line	STM32F407/417
MCU	STM32F407VGTx
Datasheet	022152_Rev8

6.2. Parameter Selection

Temperature	25
Vdd	3.3

7. IPs and Middleware Configuration

7.1. DAC

mode: OUT1 Configuration

mode: OUT2 Configuration

7.1.1. Parameter Settings:

DAC Out1 Settings:

Output Buffer	Enable
Trigger	None

DAC Out2 Settings:

Output Buffer	Enable
Trigger	**Timer 6 Trigger Out event ***
Wave generation mode	Disabled

7.2. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

7.2.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Enabled
Data Cache	Enabled
Flash Latency(WS)	5 WS (6 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Regulatror Voltage Scale	Power Regulator Voltage Scale 1

7.3. SYS

Debug: Serial Wire

Timebase Source: SysTick

7.4. TIM1

Channel1: PWM Generation CH1

7.4.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**2618 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	**1309 ***
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

7.5. TIM6

mode: Activated

7.5.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**TIM6_APB1_PSC ***
Counter Mode	Up

Counter Period (AutoReload Register - 16 bits value)	**TIM6_ARR_100MS ***

Trigger Output (TRGO) Parameters:

Trigger Event Selection	**Update Event ***

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
DAC	PA4	DAC_OUT1	Analog mode	No pull-up and no pull-down	n/a	DAC_OUT1_Uus
	PA5	DAC_OUT2	Analog mode	No pull-up and no pull-down	n/a	DAC_OUT2_Ius
RCC	PC14-OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	PC14-OSC32_IN
	PC15-OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	PC15-OSC32_OUT
	PH0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	PH0-OSC_IN
	PH1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	PH1-OSC_OUT
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	SWDIO
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	SWCLK
TIM1	PA8	TIM1_CH1	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	FREQ
Single Mapped Signals	PB3	SYS_JTDO-SWO	n/a	n/a	n/a	SWO
GPIO	PA0-WKUP	GPIO_EXTI0	**External Event Mode with Rising edge trigger detection ***	No pull-up and no pull-down	n/a	B1 [Blue PushButton]
	PB2	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	BOOT1
	PD12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD4 [Green Led]
	PD13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD3 [Orange Led]
	PD14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD5 [Red Led]
	PD15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD6 [Blue Led]

8.2. DMA configuration

DMA request	Stream	Direction	Priority
DAC1	DMA1_Stream5	Memory To Peripheral	Low

DAC1: DMA1_Stream5 DMA request Settings:

Mode:	**Circular ***
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

8.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
DMA1 stream5 global interrupt	true	0	0
TIM6 global interrupt, DAC1 and DAC2 underrun error interrupts	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
TIM1 break interrupt and TIM9 global interrupt	unused		
TIM1 update interrupt and TIM10 global interrupt	unused		
TIM1 trigger and commutation interrupts and TIM11 global interrupt	unused		
TIM1 capture compare interrupt	unused		
FPU global interrupt	unused		

*** User modified value**

9. Software Pack Report