UNIVERSIDAD CARLOS III DE MADRID
Computer Structure
Exam

You have **1:30 hrs** for this exam.
You may **NOT** use any handouts, lecture notes, books, calculators, nor any other external help.

Exercise 1. We want to develop a controller for a microwave oven. The controller includes a 32 bit processor, with a shared I/O and memory space address. The processor executes the MIPS32 assembly language. This processor is connected to an I/O module that controls the microwave behavior. This module has five 32-bit registers:

- Register with address 1000. This register is used to load a value that represents the countdown timer in seconds.
- Register with address 1004. When the value stored is "1", the countdown is started.
- Register with address 1008. When the countdown finishes, the value of this register changes from "0" to "1".
- Register with address 1012. This register is used to load the value corresponding to the power.
- Register with address 1016. The oven is turn on when the value stored is "1". The microwave stops when the value stored is "0".

Write a function, called `Microwave_Controller` to control the behavior. This function receives two arguments: an integer value that represents the number of seconds, and a second integer value that represents the power. The function must control the oven. The function returns the following values:

- 0, when any error has been detected, and the microwave finishes.
- -1, when the power passed to the function is less than 100 or greater than 1000. In this case, then function returns inmediatly.

a) Describe the registers used to pass the arguments.
b) Invoke the function passing two parameters: 800 W and 90 seconds.
c) Implement the function.

Solution

a) Parameters are passed in `$a0` and `$a1`. The result is returned in `$v0`.

b)

```
li   $a0,  800
li   $a1, 90
jal  Microwave_Controller
move $a0, $v0
li    $a1, 1
syscall
```

c)

```
Microwave_Controller:
                      li   $t0, 100
                      blt  $a0, $t0, end_error
                      li   $t0, 1000
```

```
                bgt  $a0, $t0, end_error
                sw   $a1, 1000      ; countdown
                sw   $a0, 1012      ; power
                li   $t0, 1
                sw   $t0, 1016      ; motor on
                sw   $t0, 1004      ; init countdown
        loop:   lw   $t1, 1008      ; read status
                beq  $t1, $0, loop
                sw   $0, 1016       ; motor off
                move $v0, $0
                jr $ra
end_error:      li $v0, -1
                jr $ra
```

Exercise 2. We want to represent integer numbers in the range -8191…8191. Reply justifying your answer:

a) What is the number of bits needed if we use one's complement?
b) What is the number of bits needed if we use sign-magnitude?

Solution

We need 14 bits. Using 14 bits the representation range in both cases is:
$-(2^{13}-1) \ldots 2^{13}-1 = -8191 \ldots 8191$

Exercise 3. Represent the value -24.50 using the IEEE 754 single precision format. Give the result in binary and hexadecimal.

Solution

$24{,}5_{(10} = 11000.1_{(2} = 1{,}10001 \times 2^4$

Sign = 1, negative number
Exponent = 4 + 127 = 131 = 10000011
Mantissa = 1000100000 .. 00000

binary => 11000000111000100000 …….00000
Hexadecimal => 0xC1C40000

Exercise 4. A 32 bit computer has a cache memory of 512 KB. The cache is 4-way associative and uses lines of 64 bits. In this computer the following code is executed:

```
int v[200];
int i;
int s;

for (i=0; i < 200; i++)
     s = s + v[i];
```

Reply, justifying your answer:

a) What is the number of lines and sets of this cache?

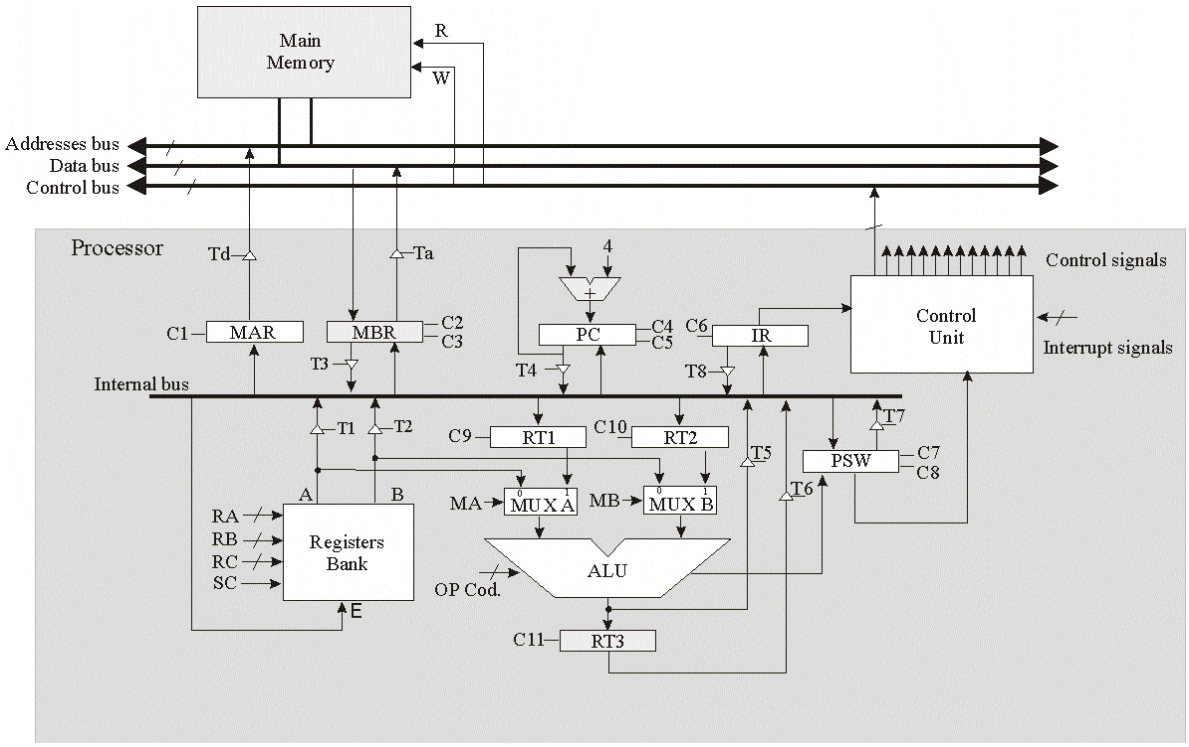
b) Is the cache is initially empty and the variables i and s are stored in registers, what is the number of access to the array `v`? What is the hit ratio obtained in the previous code?

Solution

a) The cache memory has 512 Kb = 2^{19} bytes. Each line has 64 bits = 8 bytes = 2^3 bytes. The number of lines is 2^{19} bytes / 2^3 bytes = 2^{16} lines. Each set has 4 líneas, the number of sets is = 2^{16} / 2^2 = 2^{14} sets.

b) Each integer uses 4 bytes, and then, each line can store two integers. Every two access, one is a miss, and the other one is a hit. Then the hit ratio is 50 %.

Exercise 5. Consider the following 32-bit computer. The processor has 32 registers and uses one cycle for decoding instructions. The main memory needs one cycle in reading and writing memory operations.



a) Indicate the control signals needed to execute the elemental operation: RT2 ← PC.
b) Write the sequence of elemental operations and control signals (fetch included) needed to execute the instruction `lw $t1, ($t2).`

Solution

a) We have to activate: T4 and C10

b)

cycle 0: MAR ← PC Signals: T4, C3
cycle 1: MBR ← MP Signals: Td, L, C2
PC ← PC + 4 C4

cycle 2: RI ← MBR	Signals: T3, C6
cycle 3: Decoding	
cycle 4: MAR ← $t2	Signals: RA= identifier of $t2, T1, C1
cycle 5: MBR ← MP	Signals: Td, L, C2
cycle 6: $t1 ← MBR	T3, RC = identifier de $t1, SC