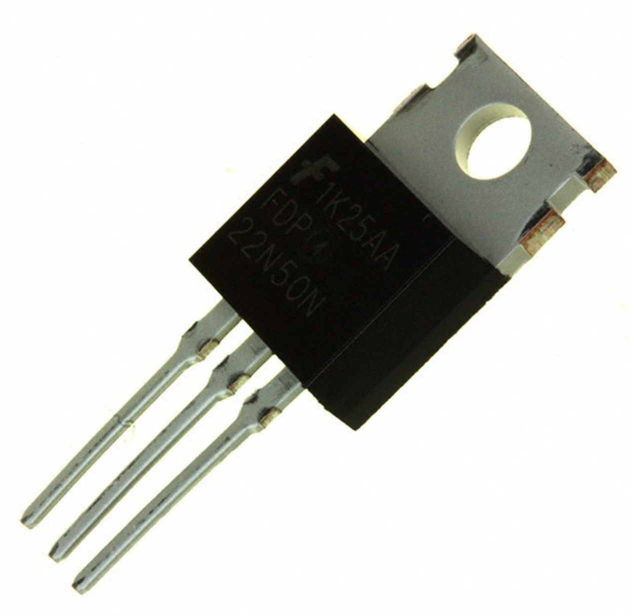
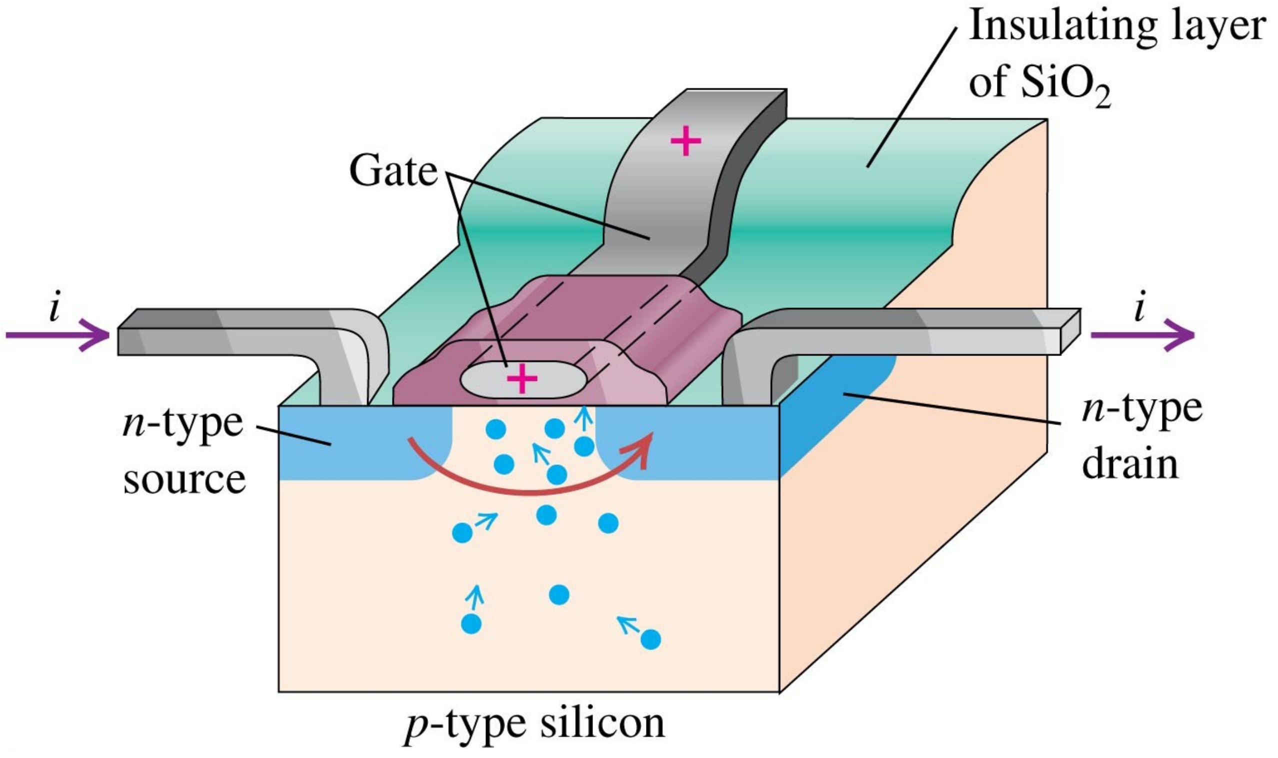
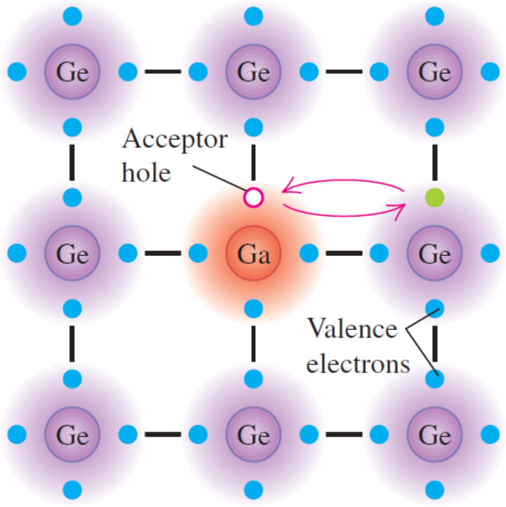
Semiconductor devices



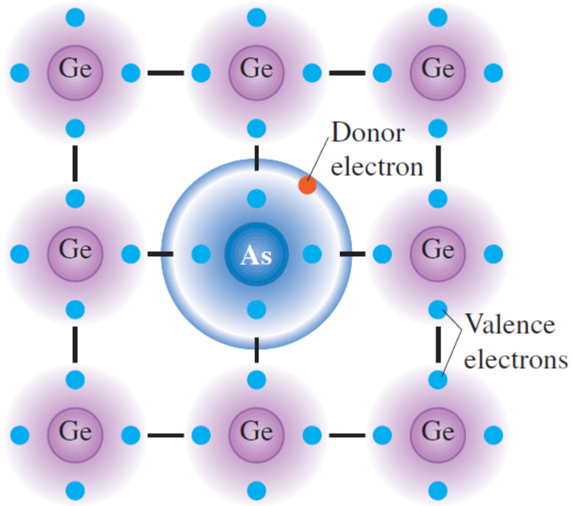


p-type and n-type semiconductors

p-type



n-type

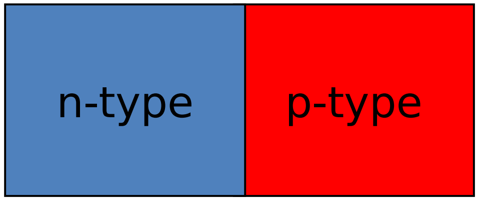


acceptor impurities
Majority carriers: holes

donor impurities
Majority carriers: electrons

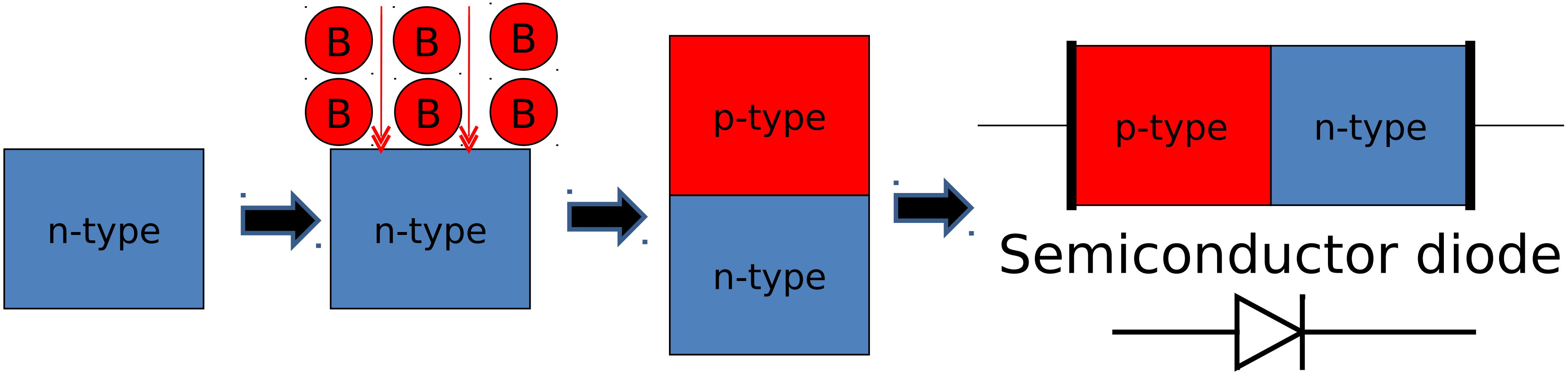
PN junction

When we join two extrinsic semiconductors, one of each type (n and p), we form a pn junction.



<u>PN JUNCTION FABRICATION:</u>

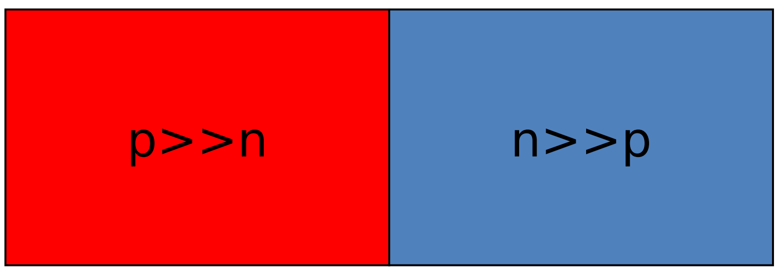
Deposition of p-type material on a “clean” single crystal of an extrinsic semiconductor (for example, n-type Si).



PN junction

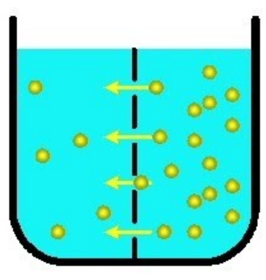
DIFFUSION THROUGH THE JUNCTION:

excess holes diffuse
to the n-type region



excess electrons diffuse
to the p-type region

similar to:

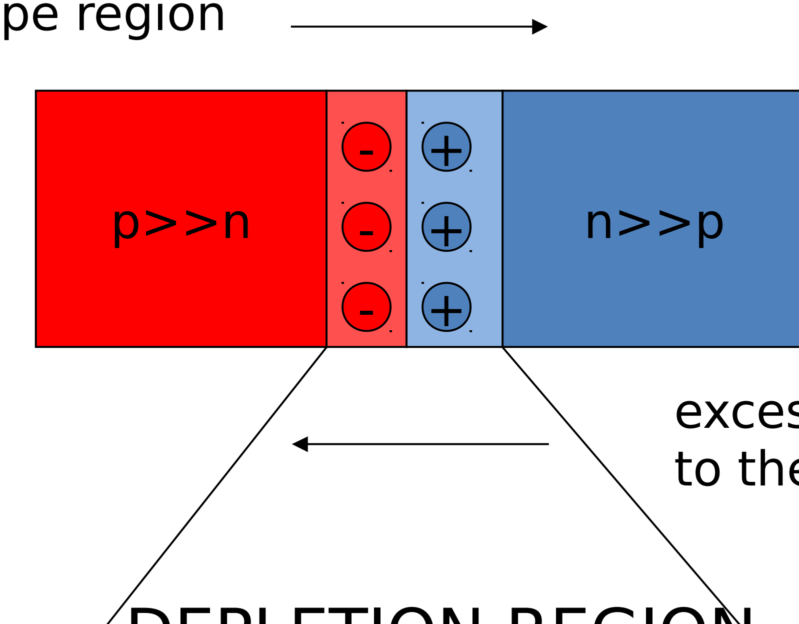


Diffusion
(Solvent moves by
concentration gradient)

PN junction

DIFFUSION THROUGH THE JUNCTION:

excess holes diffuse
to the n-type region



excess electrons diffuse
to the p-type region

DEPLETION REGION:

p~0
- negative ions from acceptor impurities

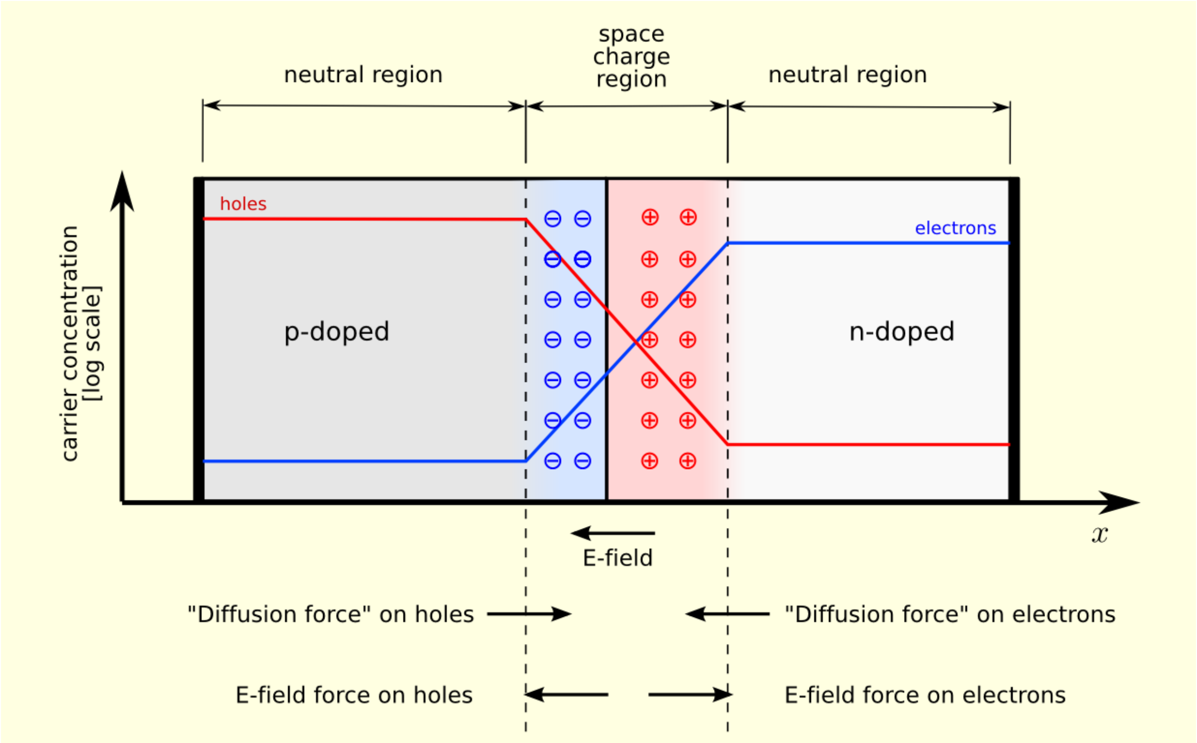
n~0
+ positive ions from donor impurities

PN junction

<u>ZERO BIAS</u>

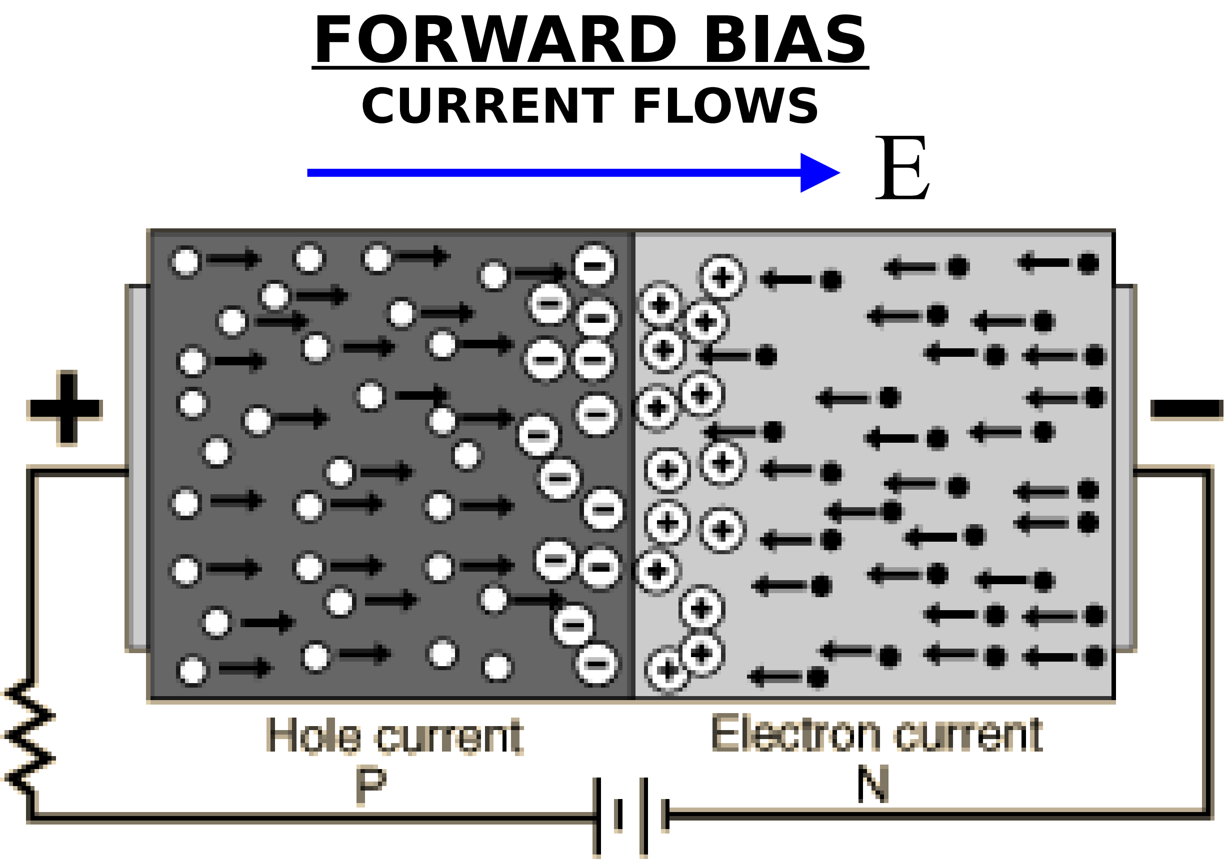
DIFFUSION STOPS, EQUILIBRIUM REACHED

Depletion region=space charge region (width ~10^{-6} m)



An electric field is created in the depletion region, with direction from the n side to the p side. (E ~10^5 V/cm). This balances diffusion, and equilibrium is reached.

PN junction

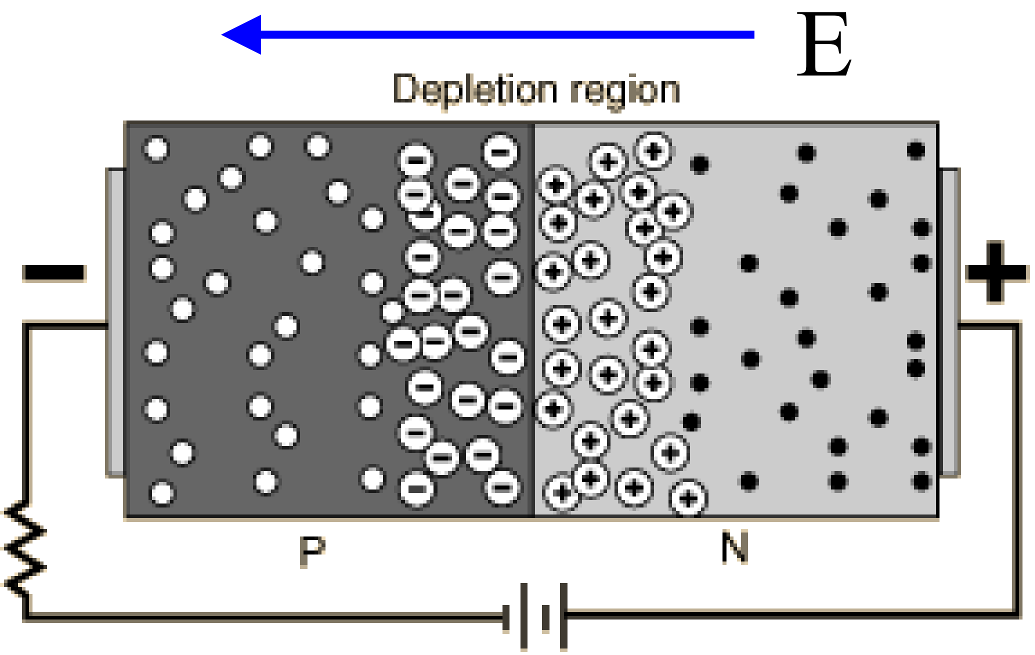


Holes and electrons are pushed towards the junction due to E (which is established on the opposite direction to the internal E). This reduces the width of the depletion region. More and more carriers will pass through the region as E increases.

PN junction

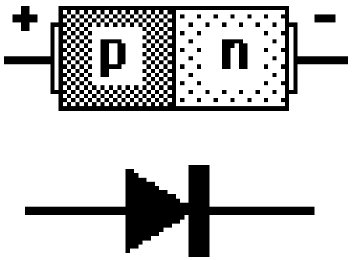
REVERSE BIAS

NEARLY NO CURRENT FLOWS

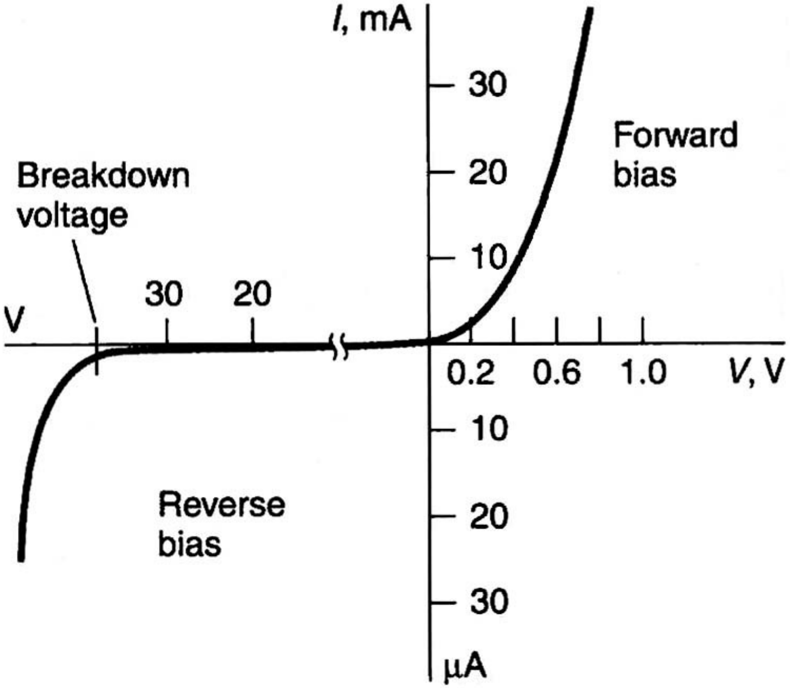


Holes and electrons are pushed away from the junction due to E (which is established on the same direction as the internal E). This increases the width of the depletion region, and nearly no current flows through the junction.

PN junction: diode



$$I = I_s \left(e^{\frac{q \cdot V_{ext}}{kT}} - 1 \right)$$



Diode: A semiconductor device which conducts electric current run in one direction only

Transistor

- Based on PN junction, but two junctions (three-layer structure → NPN or PNP).
- Three terminals instead of two.
- The voltage applied on one of the contacts (input) controls the current flowing through the other two (output).
- They work as amplifiers and switches.

Invented by John Bardeen, William Shockley and Walter Brattain in 1947, who received the Nobel Prize in 1956.

One of the most important inventions of the century.
It has revolutionised the electronic industry, allowing to have computers with very high speed and processing capacity and reduced sizes.

Transistors

- First transistors (50s) → individual BJTs (bipolar junction transistors)
- Integrated circuits (60s) → made from BJTs integrated on a Si substrate
- 80s → BJT substituted with FET (field effect transistors)

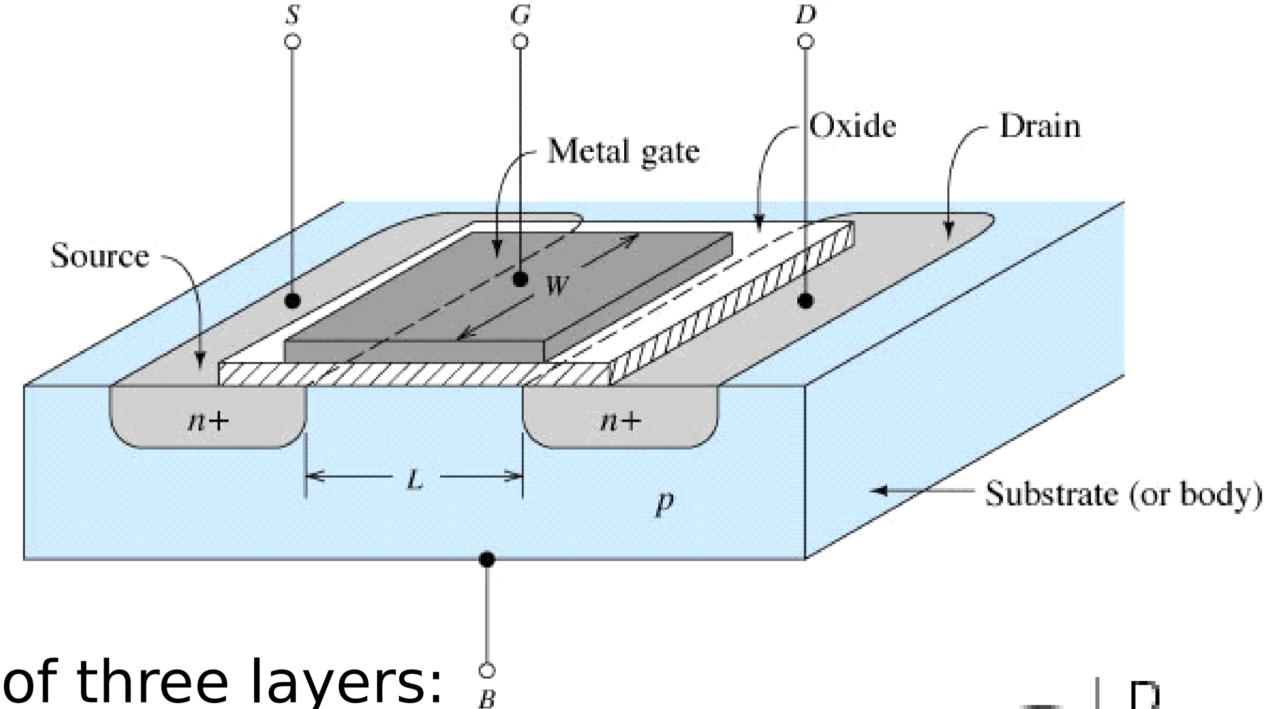
WHY?

- BJTs have a higher power consumption than FET.
- BJTs (controlled by a current) need to dissipate the heat produced by the high currents, so integrated circuits made with those cannot be as compact as the ones made with FETs.
- An advantage of the BJTs is that they have a quicker response than the FETs.

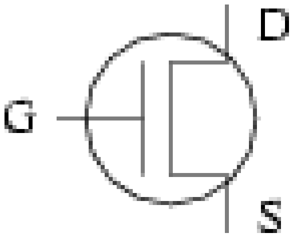
MOSFET transistor

MOSFET: METAL-OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTOR

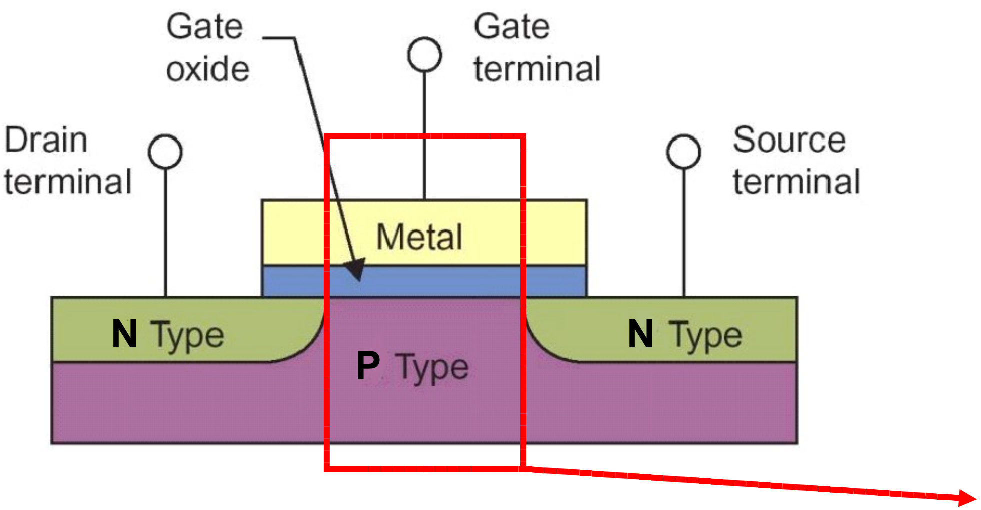
Terminals:
G→ gate
S→ source
D→ drain
B→ body

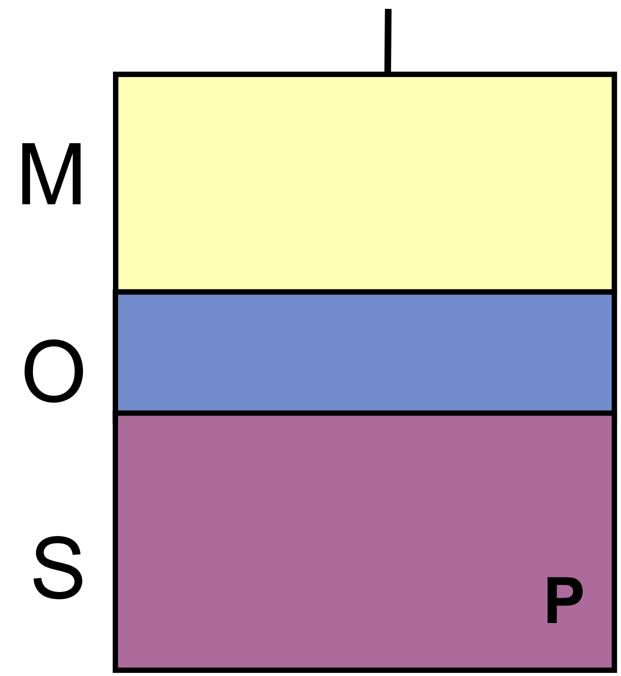


MOS structure, made of three layers:
- Metal (connected to the gate)
- Oxide (for example SiO_2), acts as an insulator
- Semiconductor



MOS structure

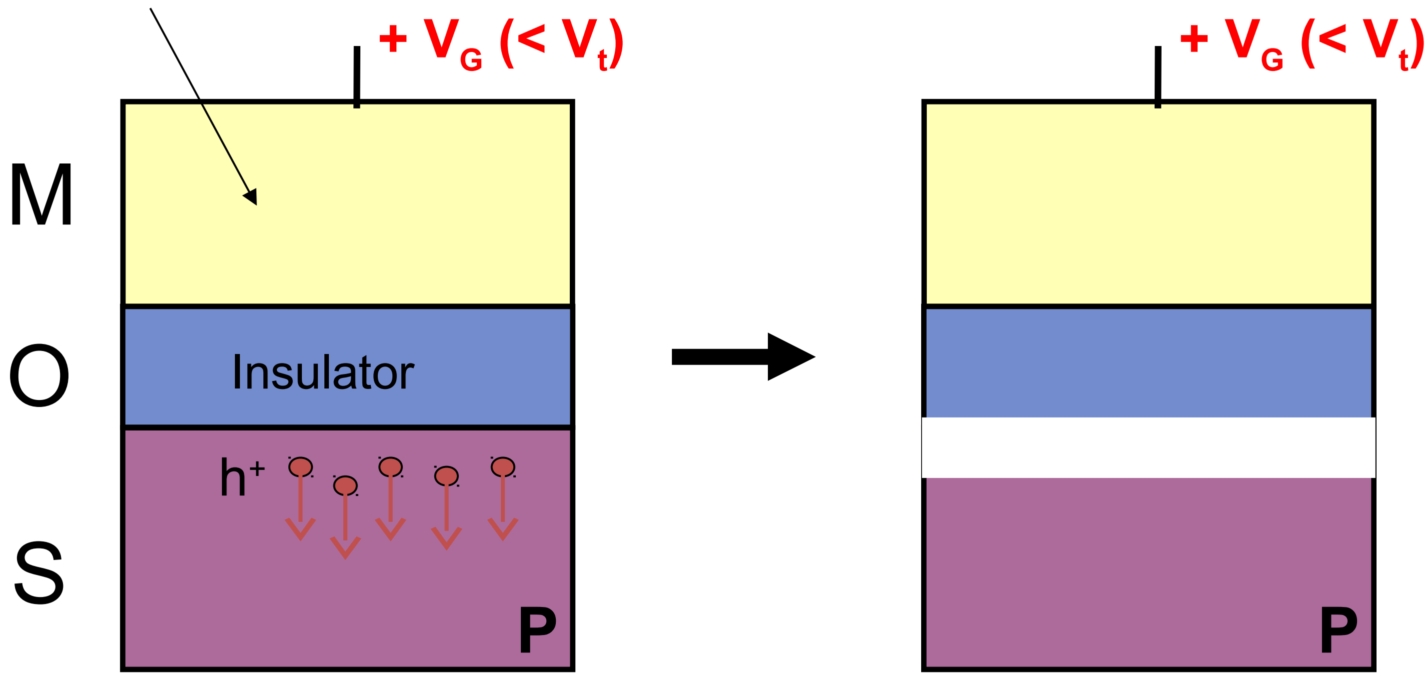




The MOS structure works as a capacitor.

MOS structure

The metal acts as the positive plate of a capacitor. A charge +Q is accumulated due to V.

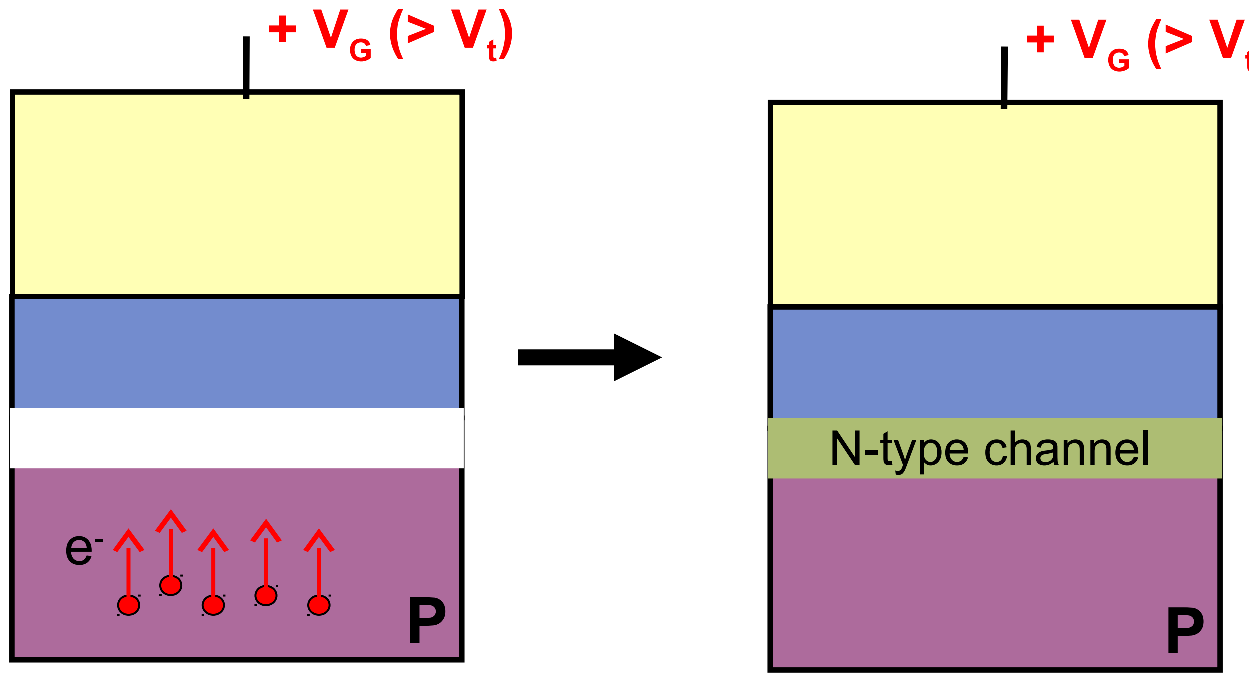


As a consequence, free holes move away from the metal...

...leaving a region depleted in free charges, and negatively charged (space charge region).

MOS structure

When V increases enough…



…free electrons flow towards the depleted region…

…creating an *inversion layer* of N-type. This layer constitutes a channel for electrons to flow between S and D.

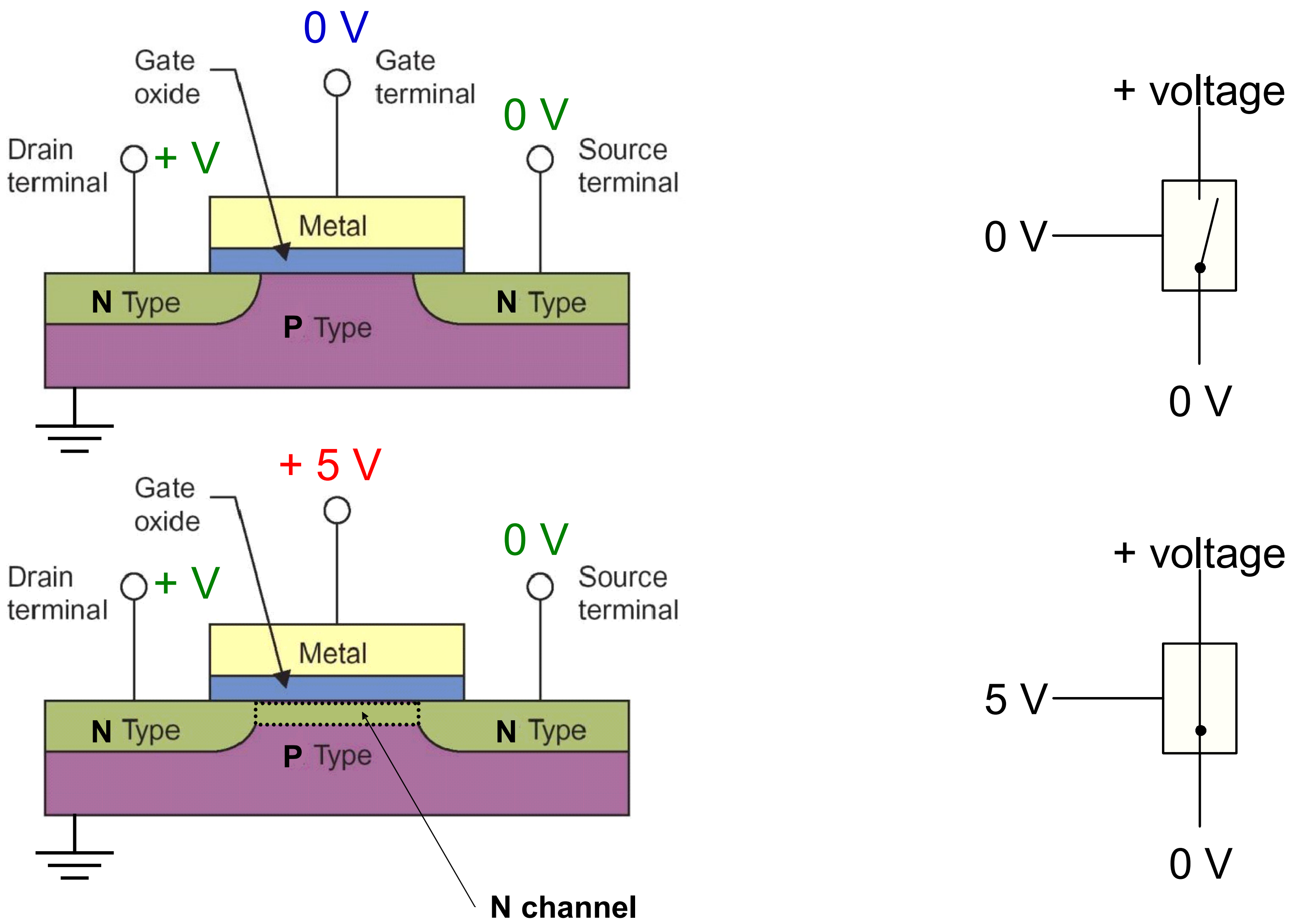
MOSFET transistor

MOS STRUCTURE

- V_t is the *threshold voltage* (typically 5 V), the one needed to invert the layer
- If $V_G < V_t$, then there is insufficient positive charge on the gate to *invert* the p-type region
- If $V_G > V_t$, then there is sufficient charge on the gate to attract electrons and invert the p-type region, creating an **n-channel** between the source and drain
  - The MOSFET is now "on"

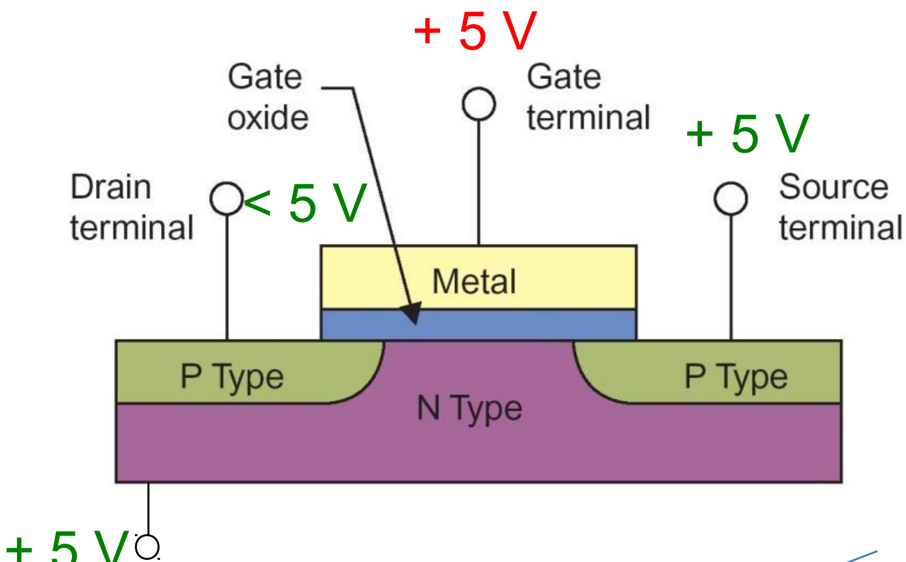
Transistor

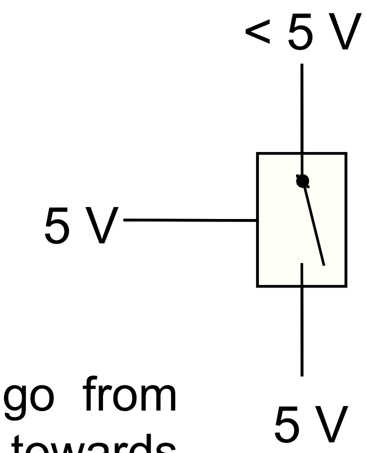
<u>THE MOSFET TRANSISTOR: N-MOSFET</u>



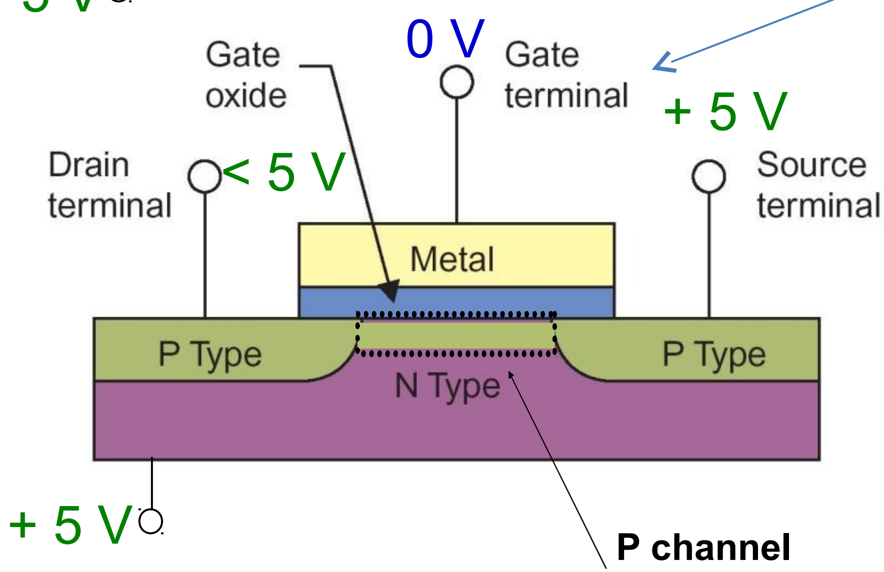
Transistor

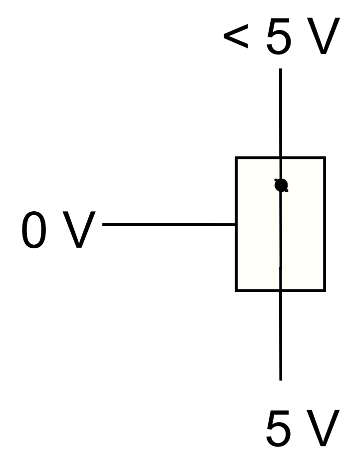
THE MOSFET TRANSISTOR: P-MOSFET



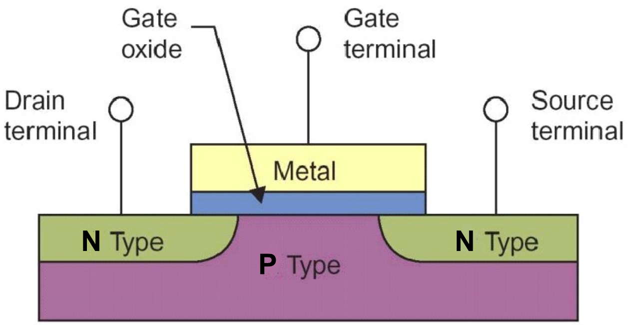


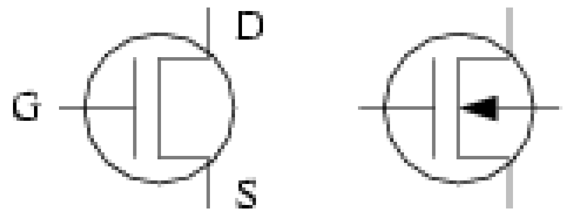
In this case, holes go from the source (V=+5V) towards the gate (V=0V), creating the p-channel.



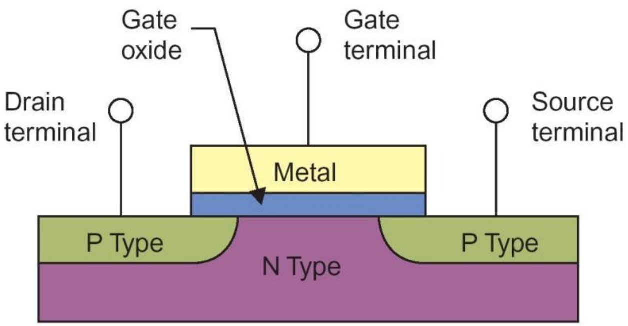


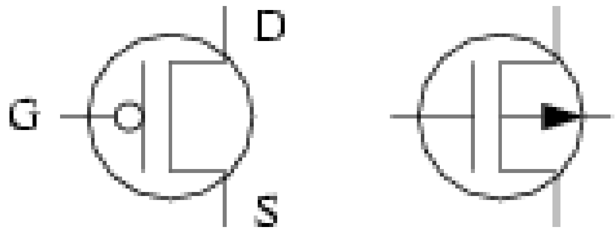
MOSFET transistor: Symbols





N-MOSFET





P-MOSFET

Complementary MOS (CMOS) logic

a pair of transistors consisting of one n-channel and one p-channel MOSFET: extremely low power consumption