MIPS 32 guide

arcos.inf.uc3m.es

Registers

Name	Number	Use
zero	0	Constant 0
at	1	Reserved for assembler
v0	2	Evaluation of expressions and function results
v1	3	Evaluation of expressions and function results
a0	4	Argument 1
a1	5	Argument 2
a2	6	Argument 3
a3	7	Argument 4
t0..t7	8..15	Temporal (no value is saved between calls)
s0..s7	16..23	Temporal (value is saved between calls)
t8, t9	24, 25	Temporal (no value is saved between calls)
k0, k1	26, 27	Reserved for the operating system kernel
gp	28	Pointer to the global area
sp	29	Stack pointer
fp	30	Stack frame pointer
ra	31	Return address, used by function calls

System calls

Service	Call code	Arguments	Results
print_int	1	$a0 = integer	
print_float	2	$f12 = real (32 bits)	
print_double	3	$f12 = real (64 bits)	
print_string	4	$a0 = string	
read_int	5		Integer ($v0)
read_float	6		Real 32-bits ($f0)
read_double	7		Real 64-bits ($f0)
read_string	8	$a0=buffer, $a1 = length	
sbrk	9	$a0 = quantity	Address ($v0)
exit	10		
print_char	11	$a0 = byte	
read_char	12		$v0 (ASCII code)

Assembly directives

.ascii string	Store the string in memory, but it does not end with NULL ('\ 0')
.asciiz string	Store the string in memory and place a NULL ('\ 0') at the end.
.byte b1, ..., bn	Stores N values in successive bytes of memory.
.data	The following data definitions that appear are stored in the data segment. It can include an argument that indicates the address from where the data will begin to be stored.
.double d1, ..., dn	Stores N real double precision values in consecutive memory addresses.
.extern label n	Declares that data stored from label occupies N bytes and that label is a global symbol. This directive allows the assembler to store data in an area of the data segment that can be accessed through the $gp register.
.float f1, ..., fn	Stores N real values of simple precision in consecutive memory positions.
.globl symbol	Declares a global symbol that can be referenced from other programs.
.half h1, ..., hn	Store N 16-bit numbers in half consecutive words.
.text	The instructions that follow this directive are placed in the code segment. It can include a parameter that indicates where the code zone begins.
.word w1, ..., wn	Stores N 32-bit elements (words) in consecutive memory locations.

Constant Handling Instructions

li Rdest, inmediate	Load immediate value
lui Rdest, inmediate	Load the 16 bits of the lower part of the immediate value in the upper part of the register. The bits of the lower part are set to 0

Data transfer instructions

move Rdest, Rsrc	Move the contents of the Rsrc register to the Rdest register.
mfhi Rdest	Move the contents of the HI register to the Rdest register.
mflo Rdest	Move the contents of the LO register to the Rdest register.
mthi Rsrc	Move the contents of the Rsrc register to the HI register.
mtlo Rsrc	Move the contents of the Rsrc register to the LO register.

Arithmetic and logical instructions

In all the following instructions, *Src2* can be both a register and an immediate value (a 16-bit integer) and in those where it puts *inm* it only accepts an immediate value

add Rdest, Rsrc1, Src2	Sum with overflow
addi Rdest, Rsrc1, inm	Add an immediate number with overflow
addu Rdest, Rsrc1, Src2	Sum without overflow
addiu Rdest, Rsrc1, inm	Add an immediate number without overflow
and Rdest, Rsrc1, Src2	AND logical operation
andi Rdest, Rsrc1, inm	AND logical operation with an immediate number
div Rsrc1, Rsrc2	Divide with overflow. Leave the quotient in the register lo and the rest in the register hi
divu Rsrc1, Rsrc2	Divide without overflow. Leave quotient in the register lo and the rest in the register hi
div Rdest, Rsrc1, Rrc2	Divide with overflow
divu Rdest, Rsrc1, Rrc2	Divide without overflow

mul Rdest, Rsrc1, Src2	Multiply without overflow
mult Rsrc1, Rsrc2	Multiply, the low part of the result is left in the lo register and the high part in the hi register
multu Rsrc1, Rsrc2	Multiply without overflow, the low part of the result goes to LO and the high part to HI
mod Rdest, Rsrc1, Rsrc2	Division module with overflow
modu Rdest, Rsrc1, Rsrc2	Division module without overflow
nop	It does not perform any operation
nor Rdest, Rsrc1, Src2	NOR Logic Operation
or Rdest, Rsrc1, Src2	OR Logic Operation
ori Rdest, Rsrc1, inm	OR Logic Operation with immediate
rem Rdest, Rsrc1, Rsrc2	Division module with overflow
rotr rdest, rsrc1, inm	Right rotation of Src2 number of bits
sll Rdest, Rsrc1, inm	Logical bit shift to the left
srl Rdest, Rsrc1, inm	Logical bit shift to the right
sra Rdest, Rsrc1, inm	Arithmetic bit shift to the right
sub Rdest, Rsrc1, Src2	Subtraction (with overflow)
subu Rdest, Rsrc1, Src2	Subtraction (without overflow)
xor Rdest, Rsrc1, Src2	XOR Logic Operation

Load instructions

la Rdest, address	Load address in Rdest (the address value, not the content)
lb Rdest, address	Load the byte of the specified address and extend the sign
lbu Rdest, address	Load the byte of the specified address, do not extend the sign
lh Rdest, address	Load 16 bits of the specified address, sign is extended
lhu Rdest, address	Load 16 bits of the specified address, no sign is extended
lw Rdest, address	Load a word from the specified address.

Storing instructions

sb Rsrc, address	Stores the lowest Rsrc byte in the indicated address.
sh Rsrc, address	Stores the low half word (16 bits) of a register in the indicated memory address.
sw Rsrc, address	Store the Rsrc in the indicated address.

Branch and jump instructions

In all the following instructions, Src2 can be a record or an immediate value. Branch instructions use a signed 16-bit offset; So you can skip 215-1 instructions forward or 215 instructions backward. The jump instructions contain a 26-bit address field.

b label	Unconditional branch to the instruction that is on label.
beq Rsrc1, Src2, label	Conditional branch if Rsrc1 is equal to Src2.
beqz Rsrc, label	Conditional branch if the Rsrc register is equal to 0.
bge Rsrc1, Src2, label	Conditional branch if the Rsrc1 register is greater than or equal to Src2 (signed).
bgeu Rsrc1, Src2, label	Conditional branch if the Rsrc1 register is greater than or equal to Src2 (unsigned).
bgez Rsrc, label	Conditional branch if the Rsrc register is greater than or equal to 0.
bgezal Rsrc, label	Conditional branch if the Rsrc register is greater than or equal to 0. Save the current address in the $ra register ($31)
bgt Rsrc1, Src2, label	Conditional branch if the Rsrc1 register is greater than Src2 (signed).
bgtu Rsrc1, Src2, label	Conditional branch if the Rsrc1 register is greater than Src2 (unsigned).
bgtz Rsrc, label	Conditional branch if Rsrc is greater than 0.
ble Rsrc1, Src2, label	Conditional branch if Rsrc1 is less than or equal to Src2 (signed).
bleu Rsrc1, Src2, label	Conditional branch if Rsrc1 is less than or equal to Src2 (unsigned).
blez Rsrc, label	Conditional branch if Rsrc is less than or equal to 0.
blt Rsrc1, Src2, label	Conditional branch if Rsrc1 is less than Src2 (signed).
bltu Rsrc1, Src2, label	Conditional branch if Rsrc1 is less than Src2 (unsigned).
bltz Rsrc, label	Conditional branch if Rsrc is less than 0.
bne Rsrc1, Src2, label	Conditional branch if Rsrc1 is not equal to Src2.
bnez Rsrc, label	Conditional branch if Rsrc is not equal to 0.
j label	Unconditional jump.
jal label	Unconditional jump, stores the current address at $ ra ($31).
jalr Rsrc	Unconditional jump, stores the current address at $ ra ($31).
jalr Rsrc1, Rsrc2	Unconditional jump, stores the current address in Rsrc1.
jr Rsrc	Unconditional jump.