Memory systems and cache memory
Proposed exercises

Exercise 1. Given the following assembly fragment:

```
            la   t1, 0x04000
            li   t2, 0
            li   t3, 0
            li   t4, 1000
            li   t5, 80
    loop1:  bgt  t3, t4, end1
            lw   t5, 0($t1)
            addi t2, t2, t5
            addi t1, t1, 4
            addi t3, t3, 1
            addi t5, t5, 4
            j    loop1
      end1:
```

It is requested:

a) Indicate in a reasoned way the number of bytes this program occupies in memory and the number of accesses.
b) what is done in memory when this program fragment is executed.
c) If the program fragment is executed in a computer that has a single 8 MB cache size and a line size of 32 bytes, indicate the number of hits and misses that occur, considering that the cache is initially empty.

Exercise 2. Consider a 32-bit computer with a cache 64 KB 4-way associative and an access time of 4 ns. The line size is 128 bytes. The time to serve a miss is 120 ns:

a) The number of lines in the cache.
b) The number of sets in the cache.
c) The size of the block being transferred in a cache miss between main memory and cache.
d) Calculate the hit rate required for an average memory access time of 20 ns.

Exercise 3. Consider a computer with the following features:

- 4 ns cache access time
- Main memory access time of 80 ns
- Time to serve a miss cache of 120 ns
- Write-through Policy

In this computer it has been observed that the rate of hits to the cache memory is 95% and that every 100 accesses, 90 are read operations. Calculate the average memory access time.

Exercise 4. Consider a computer with the following features:

A. Cache Size: 16KB with 32-byte blocks (8 words)
B. Access time: 10ns

This memory is connected through a 32-bit bus to a main memory that is capable of transferring a block of 8 words in 120 ns. Calculate the hit rate that is necessary to obtain an average access time to the memory system of 20 ns.

Exercise 5. A system with a 2-level cache is available. In the execution of a certain application, the hit ratio of the level 1 cache is 90% and the hit ratio of the level 2 cache is 95%. The application generates during its execution one million memory accesses. Indicate in a reasoned way:

a) The number of accesses generated to the level 1 cache.
b) The number of accesses generated to the level 2 cache.
c) The number of accesses generated to the main memory

Exercise 6. There is a computer with 32-bit memory addresses, which addresses the memory by bytes. The computer has a 4-way associative cache memory with a line size of 64 bytes. This cache has a size of 128 KB. The access time to the cache is 2 ns and the time necessary to treat a cache failure is 80 ns. Consider the following program fragment.

```
float v1[10000];
float v2[10000];

for (i = 0; i < 10000; i = i + 1)
      v1[i] = v1[i] + v2[i];
```

Answer:

a) The size in MB of the memory that can be addressed in this computer.
b) The number of words that can be stored in the cache memory of this computer.
c) The number of lines in the cache and the number of sets in the cache.
d) Indicate the hit ratio required for an average access time to the memory system of this computer of 10 ns.
e) Indicate in a reasoned way the hit ratio for the previous code fragment taking into account only the data accesses (consider that the variable i is stored in a register and that the cache is initially empty).

Exercise 7. A 32-bit computer has a 512 KB cache memory. This cache is a 4-way associative with lines of 128 bytes. On this computer we want to execute the following code fragment:

```
int a1[200];
int a2[200]:
int i;
int s;

for (i=0; i < 200; i++)
      s = s + a1[i] + a2[i];
```

Answer:

a) Indicate in a reasoned way the number of lines and sets of the cache.
b) If it is considered that the cache is empty and that the values of variables i and s of the previous code are stored in registers, indicate, considering only the accesses to vector a1 and a2, the hit ratio obtained when the previous code fragment is executed.

Exercise 8. A 32-bit computer has a 256 KB cache, 64-byte lines and an access time of 5 ns. The cache is 4-way associative and the LRU replacement policy is used. It is requested:

a) The number of lines and sets of this cache memory.
b) What is the size of the blocks that are transferred between the cache and the memory?
c) If the time to transfer a block between main memory and cache is 200 ns, indicate the required hit ratio, so that the average memory access time is 20 ns.

Exercise 9. There is a computer with a cache memory with a size of 64 KB for data and instructions. The line size is 64 bytes. The cache has an access time of 20 ns and a miss requires 120 ns. The cache is 2-way associative:

a) Indicate the total number of cache lines.
b) Indicate the number of sets.
c) Indicate the number of lines per set.
d) Make an draw of the cache structure.
e) Time to obtain a data in case of miss

Exercise 10. A 32-bit computer with the RISC-V instruction set, executes the following code fragment loaded from the address 0x000000

```
            li t0, 1000
            li t1, 0
            li t2, 0
loop:       addi t1, t1, 1
            addi t2, t2, 4
            beq  t1, t0, loop
```

This computer has a 4-way associative cache memory. The cache size is 32 KB and 16 bytes lines. Calculate, in a reasoned way, the miss cache ratio and theft ratio produced by the previous code fragment, assuming that it is executed without any interruption and that the cache is initially empty.

Exercise 11. Consider a 32-bit computer with an 8 KB data cache and lines of 64-byte, direct mapped policy and write-back policy. Calculate the overall miss cache ratio.

```
double a[1024], b[1024], c[1024], d[1024];
// consider that the vectors are
// arranged in memory consecutively.
for (int i = 0; i < 1024; i++)
      a[i] = b[i] + c[i] +d[i];
```

Exercise 12. Resolve Exercise 11 assuming that the cache is fully associative, with an LRU replacement policy

Exercise 13. Solve exercise 11 assuming that the cache is 2-way associative and 4 -way associative and LRU substitution policy.

Exercise 14. A 32-bit computer has a cache memory for 32 KB data and 64-byte line. The cache is 2-way associative. Consider the following two code fragment:

```
int m[512][512];
sum = 0;

for (i = 0; i < 512; i ++)
      for (j = 0; j < 512; j++)
            sum = sum + m[i][j];
```

```
int m[512][512];
sum = 0;

for (i = 0; i < 512; i ++)
      for (j = 0; j < 512; j++)
            sum = sum + m[j][i];
```

considering that the sum variable is stored in a register, calculate the hit ratio in both fragments (Note: the array is stored by rows).