Processor design and control unit
Proposed exercises

WepSIM processor

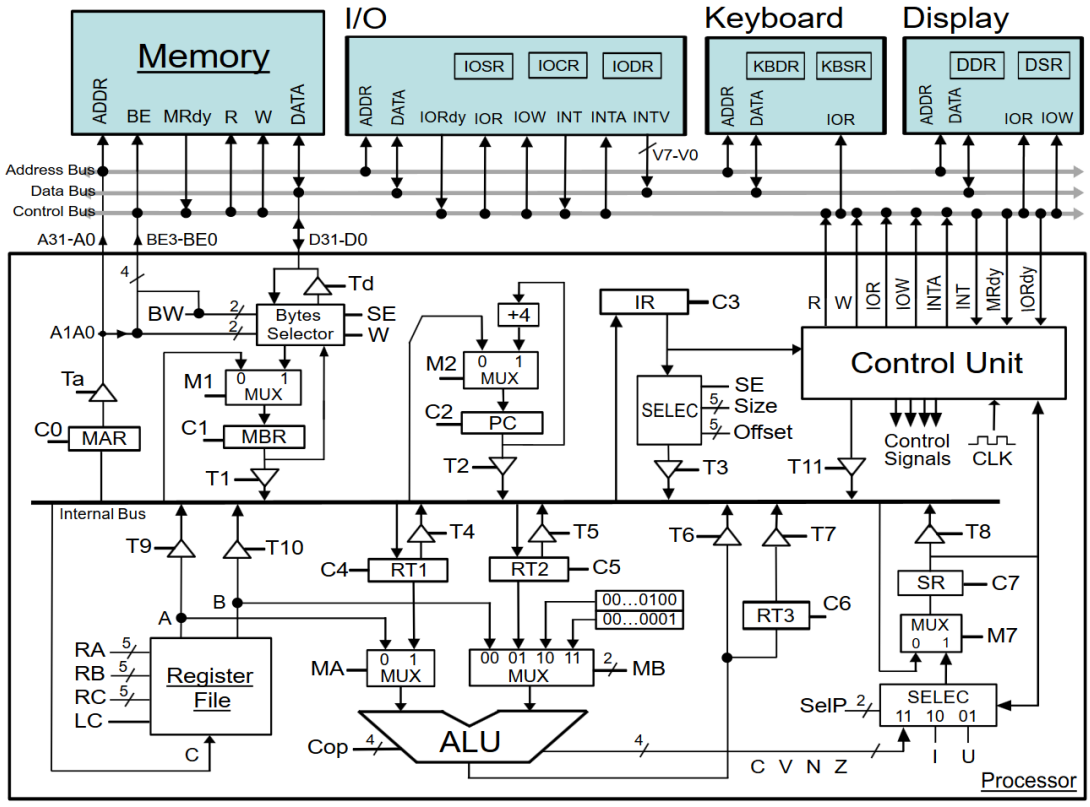


Figura 1. WepSIM processor

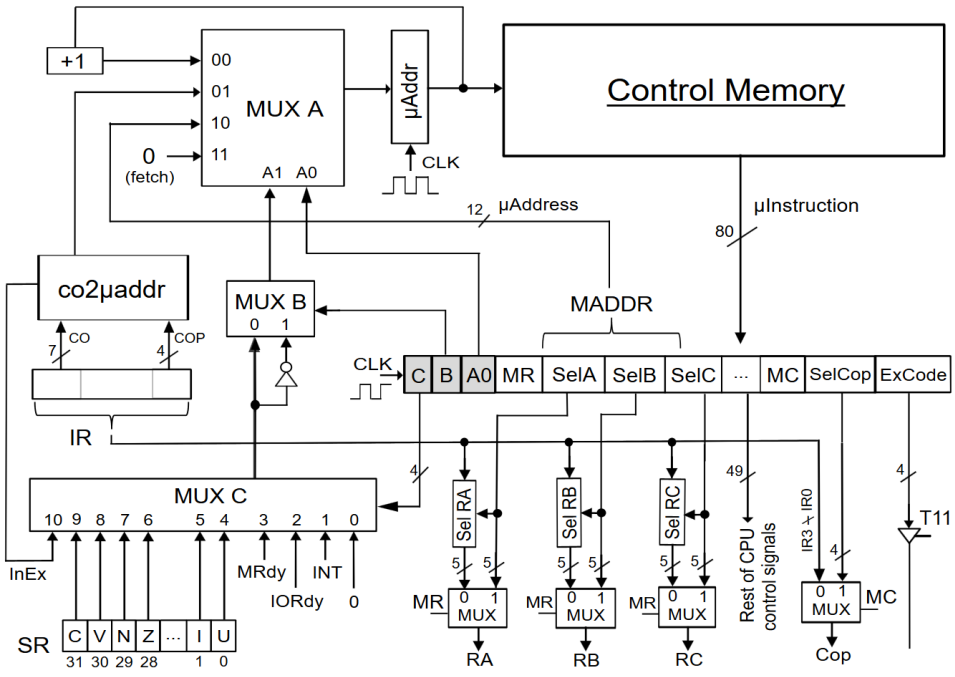


Figura 2. WepSIM Control Unit

Exercise 1. Consider a 32-bit processor with a clock frequency of 500 MHz with the structure of the WepSIM processor. The memory is addressed by bytes and requires two cycles to perform read and write operations.

Answer:

a) Indicate the elementary operations corresponding to the RISC-V32 instruction: `lw R1, n(R2)`
b) If the average number of clock cycles needed to execute an instruction is 25, calculate the average number of instructions this computer can execute in one second.

Exercise 2. Consider two computers A and B. Computer A has a clock frequency of 1 GHz and the average number of cycles per instruction is 8. Computer B has a clock frequency of 2.5 GHz and the average number of cycles per instruction is 30:

a) What does the term MIPS represent?
b) Calculate this value for computers A and B.
c) A program written in C language is available. The compiler available in the machine A obtains a program composed by 5000 machine instructions. In the second one, you get a program composed by 7000 machine instructions. In which computer will the program be executed faster, considering that all the instructions obtained are executed only once?

Exercise 3. Consider a computer with a clock frequency of 0.5 GHz and an average number of cycles per instruction of 10.:

a) What does the term MIPS represent?
b) Calculate this value for this computer.
c) What should be done if you want to get the computer to run twice as many MIPS as those obtained in question a) keeping the clock frequency?

Exercise 4. Consider a 32-bit processor with a frequency of 1 GHz with the structure of the one shown in Exercise 3. The memory is addressed by bytes and requires two cycles to perform read and write operations. If the computer is capable of executing 200 MIPS, Indicate the average number of cycles per instruction.

Exercise 5. For a processor running at 1.6 GHz and 850 MIPS, calculate the average number of cycles per instruction (CPI).

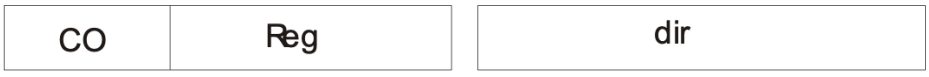
Exercise 6. Consider the processor shown in Figure 1 and the following control signals that are generated in each clock cycle (fetch not included). The rest of the signals are at 0.

C1: T3, C0, Size = 10000, Offset=00000
C2: R, Ta, BW=11
C3: R, Ta, BW=11, M1, C1
C4: RC= 00010, T1, LC

Answer:

a) The elementary operations carried out in each clock cycle.
b) Which machine instruction corresponds to the previous elementary operation?

Exercise 7. Consider the WepSIM processor. Indicate the elementary operations corresponding to the instruction SWAP R1, dir. This instruction occupies two words and its format is as follows:



This instruction exchanges the contents of the register indicated in the instruction (Reg) with the contents stored in the memory position dir.

Exercise 8. Consider a 32-bit computer, with the structure of the WepSIM processor, which 32 registers, which is connected to a memory, which is addressed by bytes and requires two cycles for reading and writing operation.

Answer:

a) Indicate the addressing modes of the following RISC-V32 instruction: `sw t1, 80(t2).`
b) Indicate the elementary operations and control signals necessary for the execution of the previous instruction.

Exercise 9. Consider a 32-bit computer, with the structure of the WepSIM processor, which 32 registers, that is connected to a memory, which is addressed by bytes and requires two cycles for reading and writing operations. Consider a hypothetical instruction: `ADD R1, address` that adds the contents of the register R1 with the contents of the memory location address and stores the result in the register R1.

Answer:

a) Indicate a possible format for the instruction, taking into account that the computer has 100 machine instructions and that 32 bit are used for the address fields.

b) Indicate the elementary operations and control signals necessary for the execution of the previous instruction.

Exercise 10. If a computer A executes a program in 10 seconds and a computer B executes a program in 15 seconds, which of the following two statements is true?

a) A is 50% faster than B
b) A is 33% faster

Exercise 11. Consider the 32-bit processor scheme shown in figure 1. Consider that the computer uses a clock cycle to perform the instruction decoding and that it is connected to a memory that allows performing a read and write operation in one cycle

This computer has the RISC-V32 instruction set:

a) Indicate the control signals required to perform the elementary operation PC ← R7, being R7 the register number 7
b) If during a clock cycle, signals T1 and C5 are activated, indicate which elementary operation is being performed.
c) Indicate elementary operations and control signals (including fetch) needed to execute the instruction addi t0, t1, 10.
d) Indicate the control signals required to perform the elementary operation RT1 ← R2, being R2 the register number 2.
e) Indicate the elementary operations and control signals (including fetch) needed to execute the hypothetical instruction addm R1, (R2). This function adds the contents of the register R1 with the contents of the memory position, which is stored in R2. The result is stored in the register R1. That is: R1 ← R1 + MP[R2]

Exercise 12. Consider the 32-bit computer, with the processor structure in Figure 1, which has a bank of 32 registers, which is connected to a memory, which is addressed by bytes and requires a cycle for reading and writing operations. The computer has a set of instructions with 98 machine instructions. The arithmetic-logical unit is capable of performing arithmetic and logical operations (adding, subtracting, multiplying, dividing, increasing, decreasing by one, etc.) The processor uses a cycle for the decoding of the instruction. Consider the following machine instruction: `swap R1, addr`. This instruction exchanges the content stored in the register R1 with the content stored in the memory address `addr`

Answer:

a) Indicate the format of the previous instruction. Note that the adds field must be able to store any valid memory address in this computer.
b) Indicate the addressing mode of the R1 and addressing fields.
c) Indicate, according to the format defined in paragraph a), the elementary operations and control signals required for the execution of the previous instruction. Also include the fetch cycle.

Exercise 13. Consider the WepSIM computer, which is connected to a memory, which is addressed by bytes and requires a cycle for reading and writing operations. The computer has a set of instructions with 98 machine instructions. The arithmetic-logic unit can perform arithmetic and logic operations (adding, subtracting, multiplying, dividing, etc.). The processor uses a cycle for the decoding of the instruction. The stack pointer register is register 29. And register 0 has its content wired to 0

Answer:

a) Indicate what is an interruption and why it occurs. Indicate two examples that cause an interruption.
b) What actions does the control unit perform during the interruption recognition cycle?
c) Indicate the elementary operations and control signals to be performed by the unit during the interrupt recognition cycle described above, assuming that the address of the interrupt processing routine is in the memory address 0.

Exercise 14. Consider the WepSIM processor, which is connected to a memory that is addressed by bytes. The stack pointer is register 29 and register 0 is wired to 0. The control unit is the one shown in figure 2. Indicate the elementary operations and control signals required to execute the following instruction, which takes up two words:

```
reset N, addr
```

The N field occupies the lower 16 bits of the first word of the instruction and the address field occupies the 32 bits of the second word of the instruction. This instruction sets to 0 the N words in memory from the dir address. That is, it sets to 0 the memory addresses: add, adds + 4, adds + 8, ... adds +N*4. If N is less than or equal to 0, the instruction does not perform any operation.

Exercise 15. Consider the processor in figure 1 and the hypothetical machine instruction: PUSHREGS R1, R2, R3. This instruction occupies a word and stores at the top of the stack three values in this order: the content of R1, the content of R2 and the content of R3, updating the stack pointer properly. Consider that the stack pointer register is register 29 of the register file and that the ALU includes an operation code that allows adding a 4 (0100) to the operand that enters the ALU from the multiplexer A. Indicate the elementary operations needed to execute this instruction.

Exercise 16. Given the processor in figure 1, specify the elementary operations and control signals needed to execute the machine instruction: adds R1, R2. This function adds the contents of the two registers R1 and R2 and leaves the result at the top of the stack (this implies making room in the stack to store the result). Assume that the number of the register R1 is 1, the register R2 is 2 and the stack pointer is 16.

Exercise 17. Given the processor in figure 1, and the instruction addm R1, adds, where R1 is a register and addr a memory address. If the addr value is 0, this instruction does nothing. Otherwise, it adds the contents of the memory position addr with the value of register R1 and stores the result in R1.

a) Indicate the format of such instruction.
b) Specify the elementary operations needed to execute this instruction, excluding the fetch.