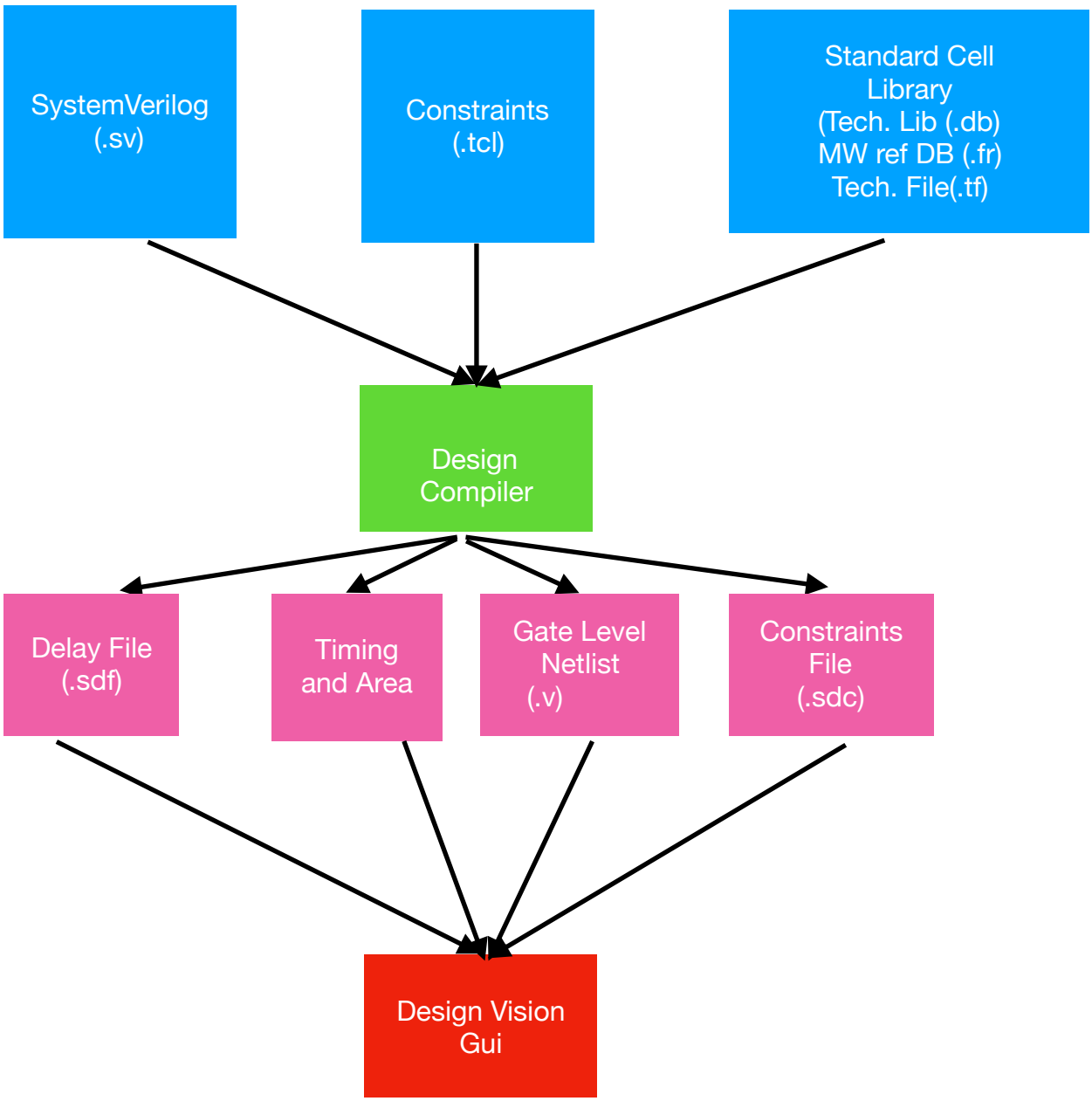
Design Compiler

A synthesis tool takes an RTL hardware description and a standard cell library as input and produces a gate- level netlist as output.

The resulting gate-level netlist is a completely structural description with standard cells only at the leaves of the design.



The Design Compiler product includes the following technologies:

- **DC Expert** optimizes designs for area, timing, and power using wire load models for delay estimation.

  Additional Features :

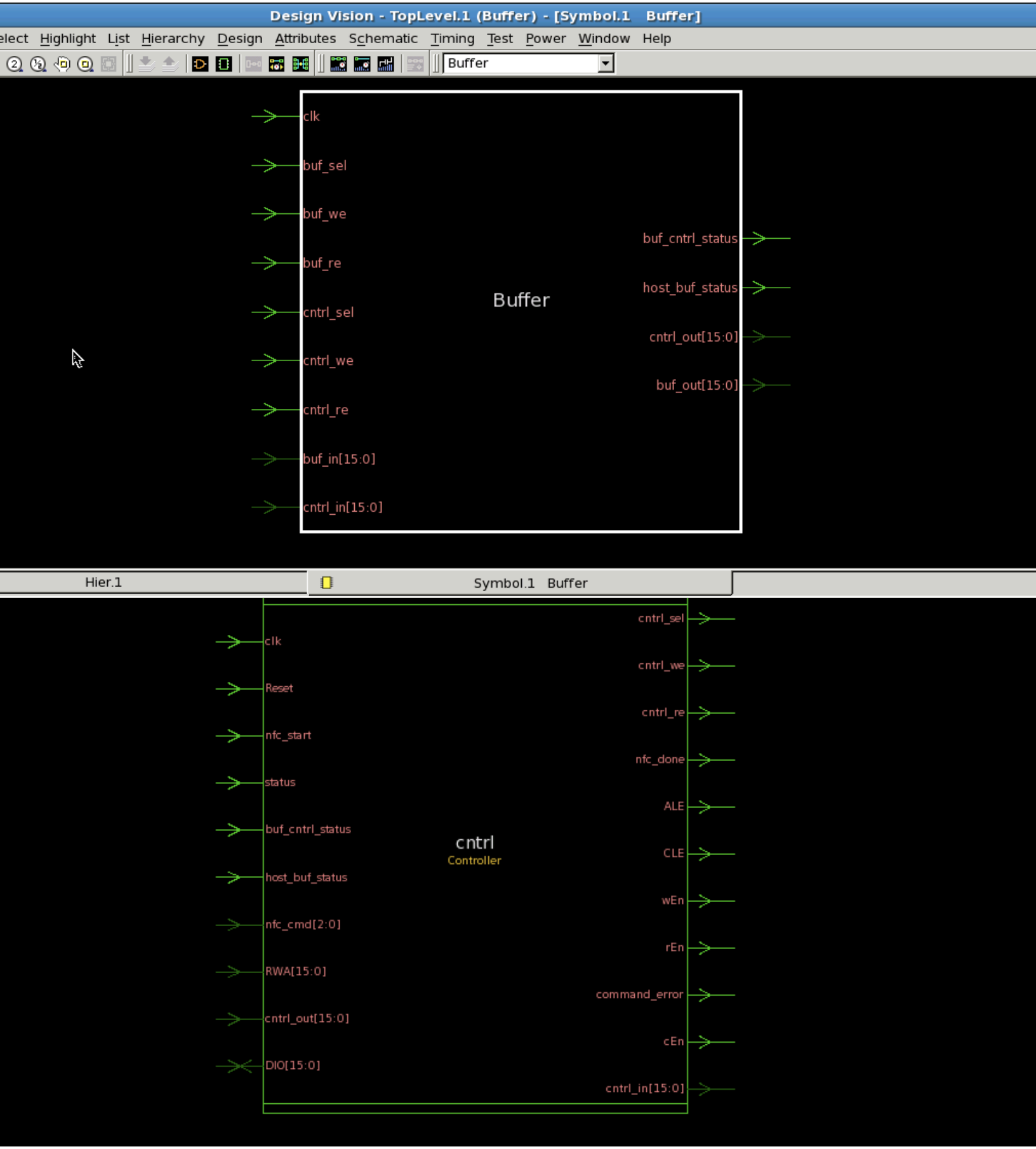
  •Hierarchical compile (top down or bottom up)
  •Full and incremental compile techniques
  •Sequential optimization for complex flip-flops and latches
  •Time borrowing for latch-based designs
  •Timing analysis
  •Command-line interface and graphical user interface.

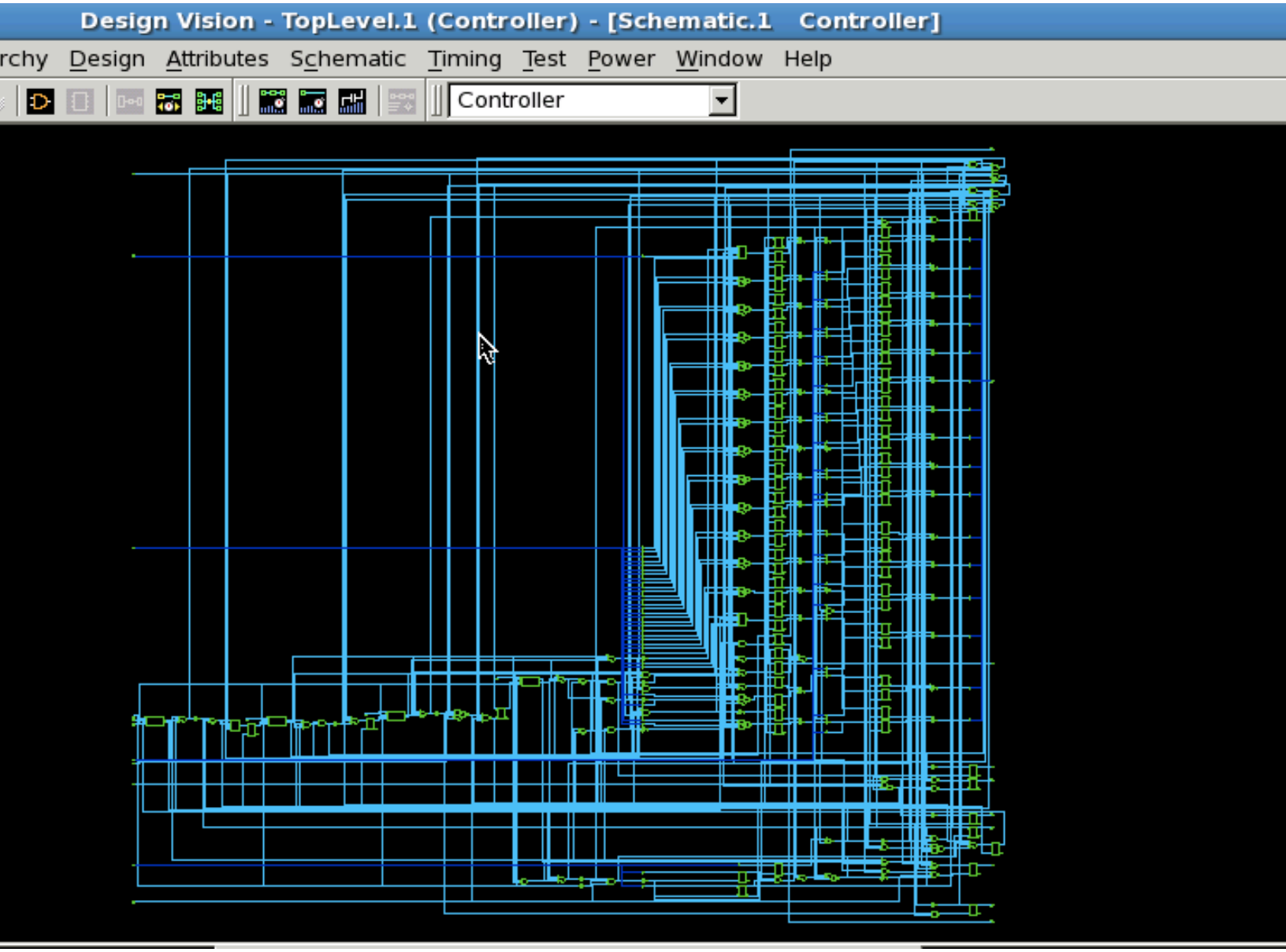
Design Vision

- Graphical user interface (GUI) for the Synopsys logic synthesis environment.
- Provides analysis tools for viewing and analyzing designs at the generic technology (GTECH) and gate level.
- When you start the tool in topographical mode, the Design Vision layout window lets you analyze physical constraints, timing, and congestion in your floorplan.
- A layout view displays floorplan constraints, critical timing paths, and congested areas in a single, flat view of the physical design.
- Thisinformation can help to guide later optimization operations in Design Compiler and other Synopsys tools.

Synthesis Script Flow

1. Configuration of ward
2. Library variables
3. Read design
4. Compile
5. Elaborate
6. Reports
7. Write design

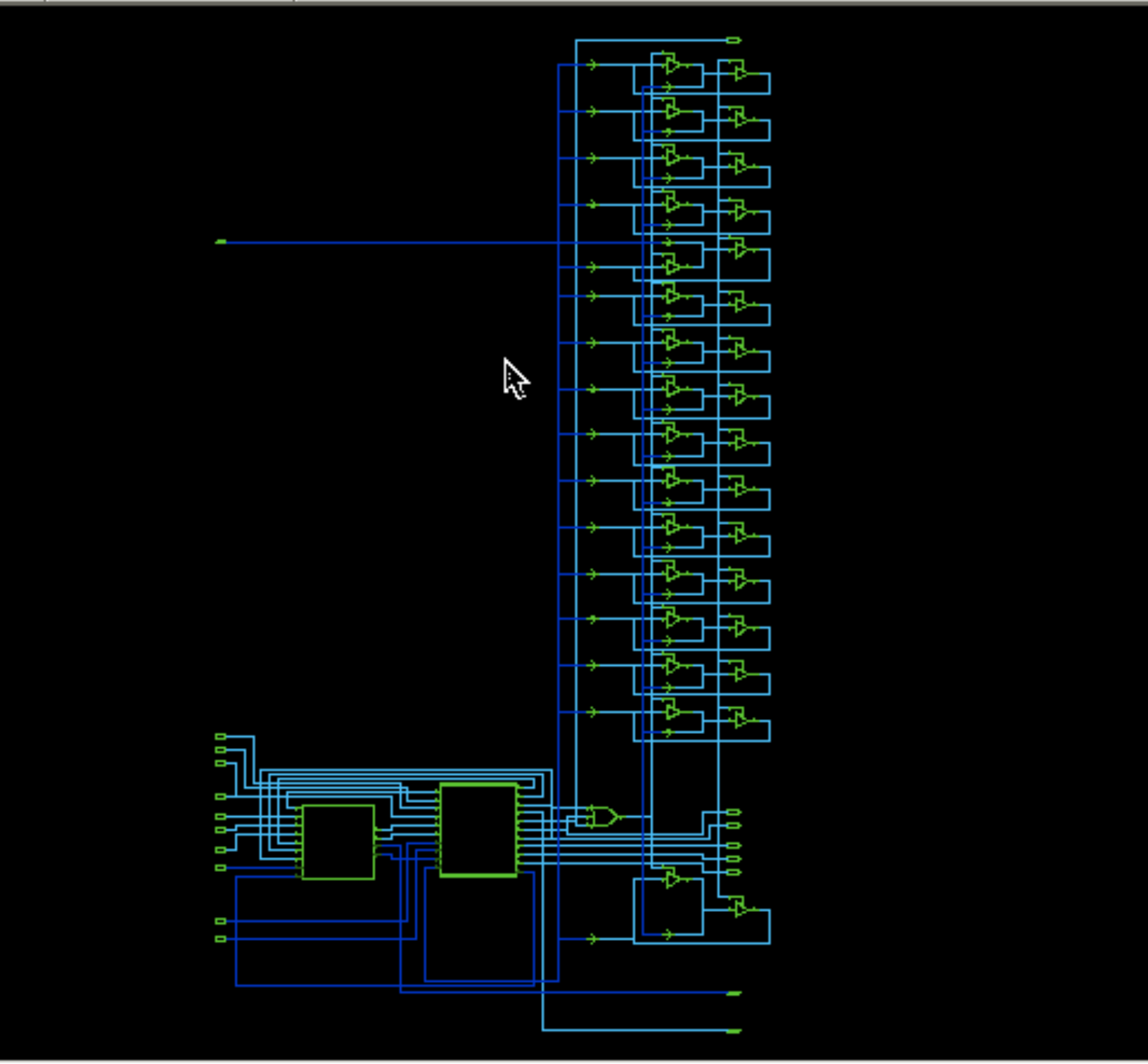

Design Vision - TopLevel.1 (Buffer) - [Symbol.1 Buffer]
elect Highlight List Hierarchy Design Attributes Schematic Timing Test Power Window Help
Buffer
clk
buf_sel
buf_we
buf_re
cntrl_sel
cntrl_we
cntrl_re
buf_in[15:0]
cntrl_in[15:0]
Buffer
buf_cntrl_status
host_buf_status
cntrl_out[15:0]
buf_out[15:0]
Hier.1
Symbol.1 Buffer
clk
Reset
nfc_start
status
buf_cntrl_status
host_buf_status
nfc_cmd[2:0]
RWA[15:0]
cntrl_out[15:0]
DIO[15:0]
cntrl
Controller
cntrl_sel
cntrl_we
cntrl_re
nfc_done
ALE
CLE
wEn
rEn
command_error
cEn
cntrl_in[15:0]

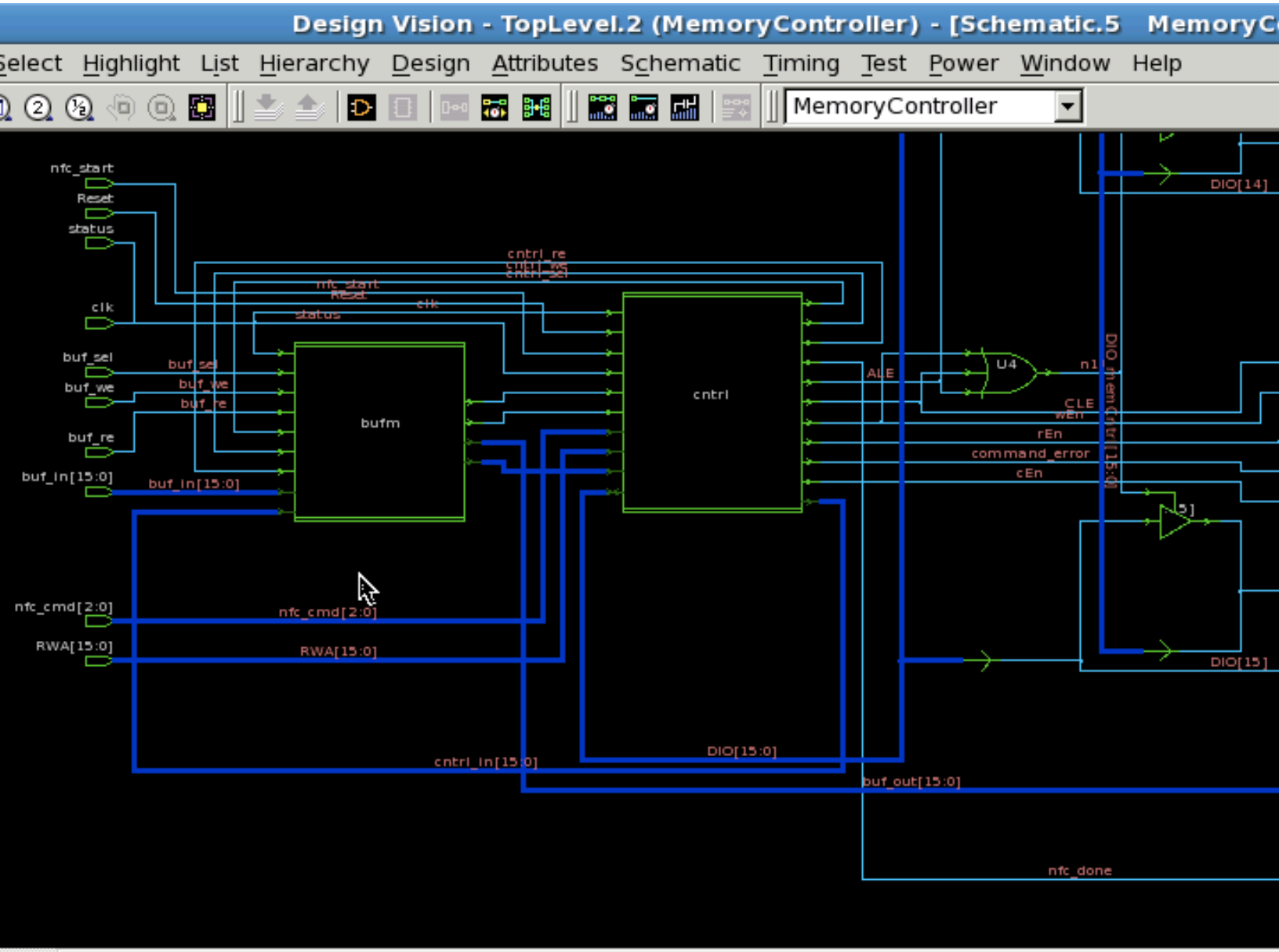

Design Vision - TopLevel.1 (Controller) - [Schematic.1 Controller]
rchy Design Attributes Schematic Timing Test Power Window Help
Controller

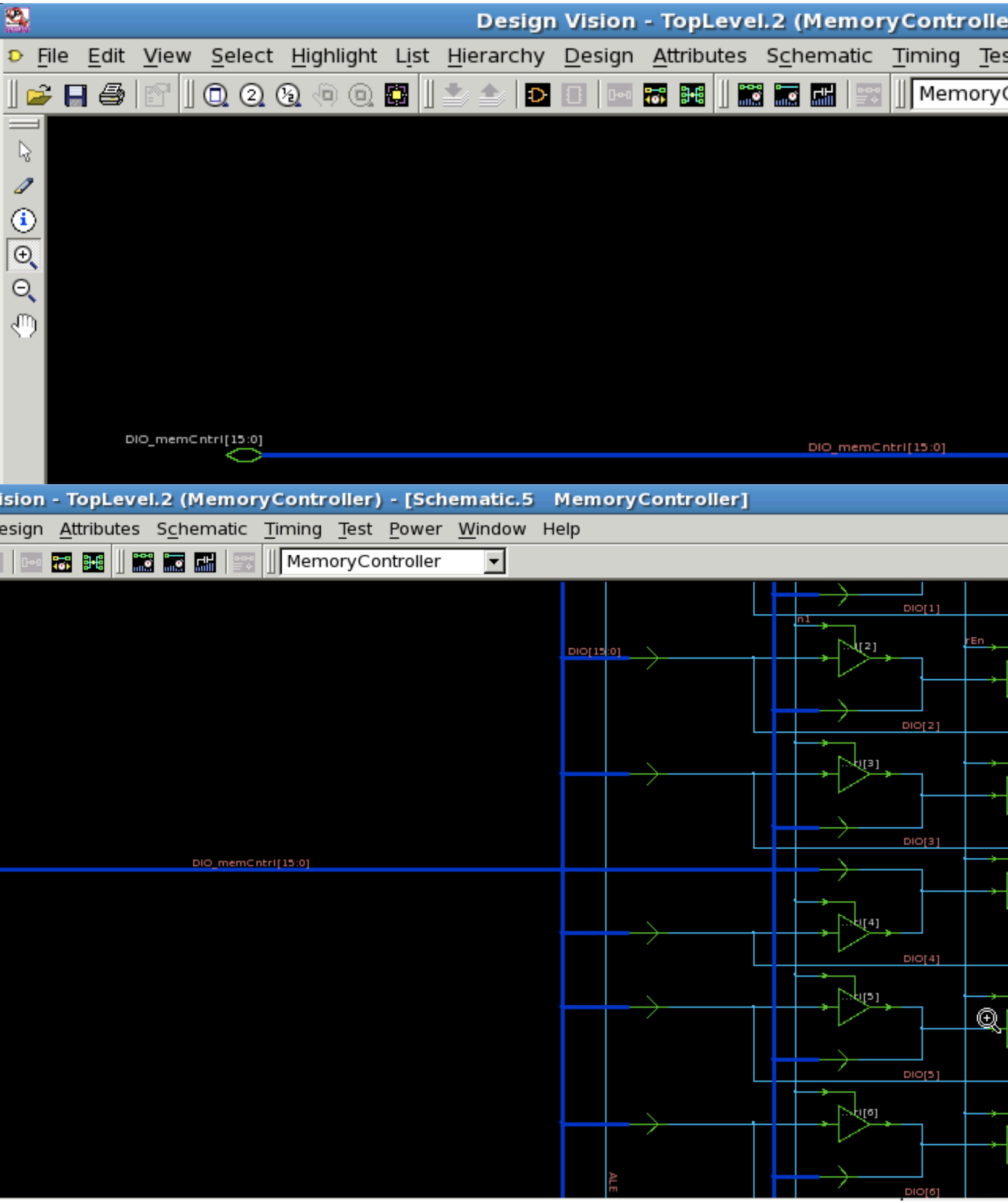
opLevel.2 (MemoryController) - [Schematic.5 MemoryController]

ributes Schematic Timing Test Power Window Help

MemoryController




Design Vision - TopLevel.2 (MemoryController) - [Schematic.5
Select Highlight List Hierarchy Design Attributes Schematic Timing Test Power Window Help
MemoryController
nfc_start
Reset
status
clk
buf_sel
buf_we
buf_re
buf_in[15:0]
bufm
cntrl
ALE
U4
CLE
wEn
rEn
command_error
cEn
DIO[14]
DIO[15]
nfc_cmd[2:0]
RWA[15:0]
cntrl_in[15:0]
DIO[15:0]
buf_out[15:0]
nfc_done


Design Vision - TopLevel.2 (MemoryControlle
File Edit View Select Highlight List Hierarchy Design Attributes Schematic Timing Tes
DIO_memCntrl[15:0]
DIO_memCntrl[15:0]
ision - TopLevel.2 (MemoryController) - [Schematic.5 MemoryController]
esign Attributes Schematic Timing Test Power Window Help
MemoryController
DIO[15:0]
DIO_memCntrl[15:0]
DIO[1]
DIO[2]
DIO[3]
DIO[4]
DIO[5]
DIO[6]
ALE