○ Tentative Specification
✓ Preliminary Specification
○ Specification Approval

Specification For SID 3.52” BW EPD

Model Name: SE0352NQ01-MNG-A0

Version:V0.1

SID	PREPARED BY	CHECKED BY	APPROVED BY
SIGNATURE	JY. Guo		
DATE	2022.04.23		

CUSTOMER APPROVAL	**SIGNATURE**	**DATE**
	Notes:	

Notes :

1、Please contact SID before assigning your product based on this module specification.

2、To improve the quality of product, and this product specification is subject to change without any notice.

REVISION RECORD

Rev No.	Rev date	Contents	Remarks
0.1	2022.04.23	First release	Preliminary

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1 General Description

SE0352NQ01-A0 is an Active Matrix Electrophoretic Display (AM EPD), with interface and a reference system design. The 3.5” active area contains 240x360 pixels. The module is a TFT-array driving electrophoretic display, with integrated circuits including gate buffer, source buffer, MCU interface, timing control logic, oscillator, DC-DC, SRAM, LUT, VCOM. Module can be used in portable electronic devices, such as Electronic Shelf Label (ESL) System.

2 Features

- 240×360pixels display
- White reflectance above 30%
- Contrast ratio above 8:1
- Ultra wide viewing angle
- Ultra low power consumption
- Pure reflective mode
- Bi-stable display
- Landscape, portrait modes
- Ultra Low current deep sleep mode
- On chip display RAM
- Waveform stored in On-chip OTP
- Serial peripheral interface available
- On-chip oscillator
- On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage
- I^{2}C signal master interface to read extemal temperature sensor

3 Application

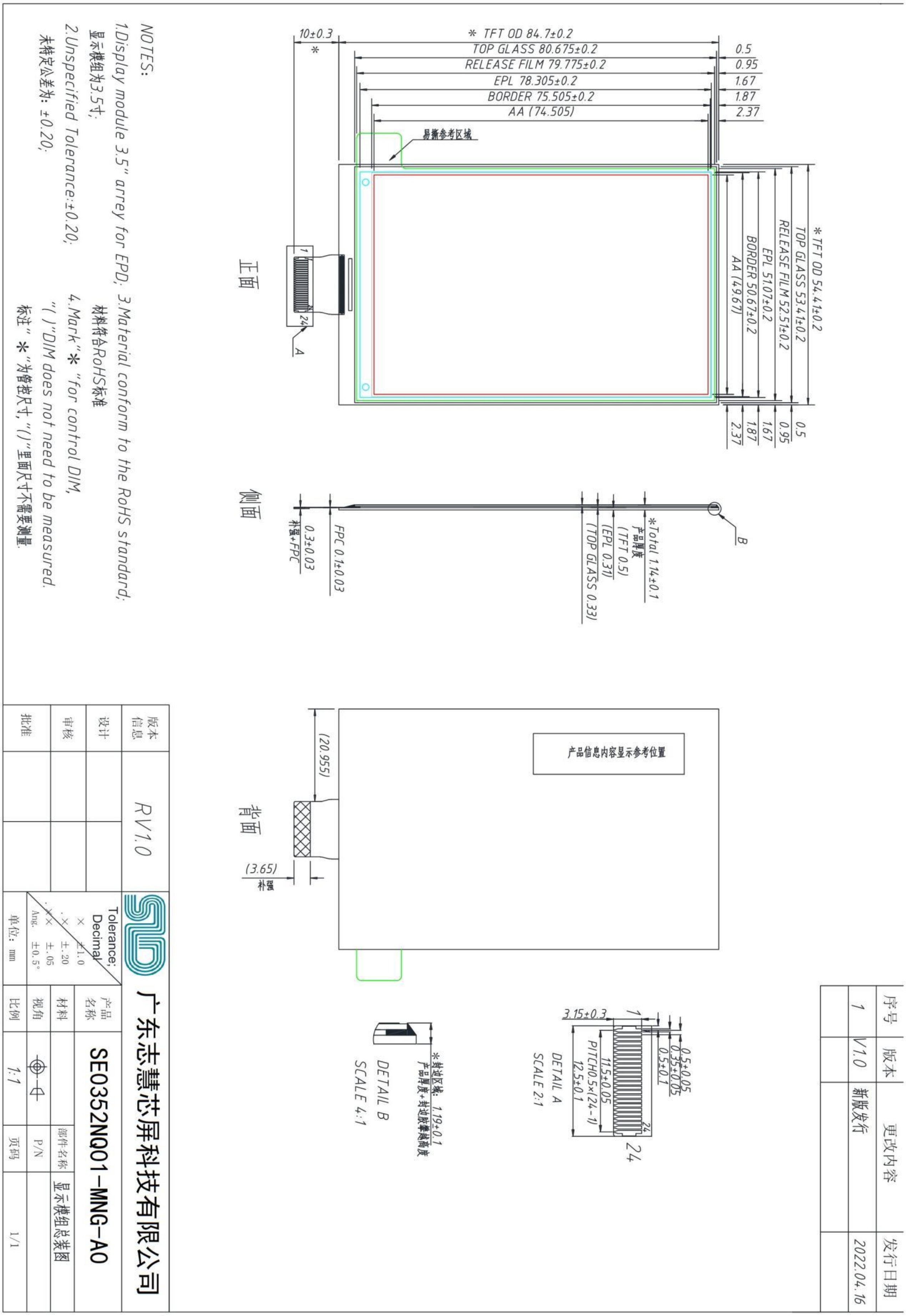
Electronic Shelf Label System or others

4 Mechanical Specification

4.1 Dimension

Parameter	Specifications	Unit
Screen Size	3.5	Inch
Display Resolution	240(H)×360(V)	Pixel
Active Area	49.67×74.51	mm
Pixel Pitch	0.207×0.207	mm
Pixel Configuration	Rectangle	
Outline Dimension	54.41(H)×84.70(V) ×1.14(D)	mm
Weight	10.75	g

4.2 Mechanical Drawing of EPD Module


10±0.3
✻ TFT OD 84.7±0.2
TOP GLASS 80.675±0.2
RELEASE FILM 79.775±0.2
EPL 78.305±0.2
BORDER 75.505±0.2
AA (74.505)
0.5
0.95
1.67
1.87
2.37
易撕参考区域
✻ TFT OD 54.41±0.2
TOP GLASS 53.41±0.2
RELEASE FILM 52.51±0.2
EPL 51.07±0.2
BORDER 50.67±0.2
AA (49.67)
正面
1
24
A
侧面
FPC 0.1±0.03
0.3±0.03
补强+FPC
✻Total 1.14±0.1
产品厚度
(TFT 0.5)
(EPL 0.31)
(TOP GLASS 0.33)
B
背面
(20.955)
(3.65)
补强
产品信息内容显示参考位置
DETAIL B
SCALE 4:1
✻封边区域: 1.19±0.1
产品厚度+封边胶水高度
DETAIL A
SCALE 2:1
3.15±0.3
0.5±0.05
0.35±0.05
0.5±0.1
11.5±0.05
PITCH0.5×(24-1)
12.5±0.1
1
24

NOTES:
1.Display module 3.5" arrey for EPD, 3.Material conform to the RoHS standard;
显示模组为3.5寸, 材料符合RoHS标准
2.Unspecified Tolerance:±0.20; 4.Mark "✻" for control DIM,
未特定公差为: ±0.20; "( )"DIM does not need to be measured.
标注 "✻"为管控尺寸, "( )"里面尺寸不需要测量.

版本信息	RV1.0
设计	
审核	
批准	

广东志慧芯屏科技有限公司

Tolerance;
Decimal
.× ±1.0
.×× ±.20
.××× ±.05
Ang. ±0.5°
单位: mm

产品名称	SE0352NQ01-MNG-A0
材料	
视角	
比例	1:1
部件名称	显示模组总装图
P/N	
页码	1/1

序号	版本	更改内容	发行日期
1	V1.0	新版发行	2022.04.16

5 Input/output Pin Assignment

No.	Name	I/O	Description	Remark
1	NC	/	Do not connect with other NC pins	
2	GDR	O	N-Channel MOSFET Gate Drive Control	
3	RESE	I	Current Sense Input for the Control Loop	
4	NC	/	Do not connect with other NC pins	
5	VDHR	C	Positive Source driving voltage 1	
6	TSCL	O	I^2C Interface to digital temperature sensor Clock pin	
7	TSDA	I/O	I^2C Interface to digital temperature sensor Data pin	
8	BS	I	Bus Interface selection pin	Note 5-4
9	BUSYN	O	Busy state output pin	Note 5-3
10	RSTN	I	Reset signal input. Active Low.	
11	D/C	I	Data /Command control pin	Note 5-2
12	CSB	I	Chip select input pin	Note 5-1
13	SCL	I	Serial Clock pin (SPI)	
14	SDA	I	Serial Data pin (SPI)	
15	VDD	P	Power Supply for interface logic pins	
16	VDD	P	Power Supply for the chip	
17	VSS	P	Ground	
18	VDDD	C	Core logic power pin VDDD can be regulated internally from VDD. A capacitorshould be connected between VDDD and VSS under all circumstances	
19	VPP	P	Power Supply for OTP Programming	
20	VSH	C	Positive Source driving voltage 2	
21	VGH	C	Positive Gate driving voltage	
22	VSL	C	Negative Source driving voltage	
23	VGL	C	Negative Gate driving voltage	
24	VCOM	C	VCOM driving voltage	

I = Input Pin, O =Output Pin, I/O = Bi-directional Pin (Input/Output), P = Power Pin, C = Capacitor Pin

Note 5-1: This pin is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CSB is pulled LOW.

Note 5-2: This pin is Data/Command control pin connecting to the MCU in 4-wire SPI mode. When the pin is pulled HIGH, the data at D1 will be interpreted as data. When the pin is pulled LOW, the data at D1 will be interpreted as command.

Note 5-3: This pin is Busy state output pin. When Busy is Low, the operation of chip should not be interrupted, command should not be sent, e.g., The chip would put Busy pin Low when

- Outputting display waveform
- Programming with OTP
- Communicating with digital temperature sensor

Note 5-4: Bus interface selection pin

BS State	MCU Interface
L	4-lines serial peripheral interface(SPI)
H	3- lines serial peripheral interface(SPI) - 9 bits SPI

6 Electrical Characteristics

6.1 Absolute Maximum Rating

Parameter	Symbol	Rating	Unit
Logic supply voltage	V_{dd}	-0.5 to +4.0	V
Logic Input voltage	V_{IN}	-0.5 to V_{dd} +0.5	V
Logic Output voltage	V_{OUT}	-0.5 to V_{dd} +0.5	V

Note: Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Panel DC Characteristics tables.

6.2 Panel DC Characteristics

The following specifications apply for: VSS=0V, VDD=3.0V, T_{OPR} =25ºC.

Parameter	Symbol	Condition	Applicable pin	Min.	Typ.	Max.	Unit
Logic supply voltage	V_{dd}	-	VDD	2.4	3.0	3.6	V
High level input voltage	V_{IH}	-	-	0.8 V_{dd}	-	-	V
Low level input voltage	V_{IL}	-	-	-	-	0.2 V_{dd}	V
High level output voltage	V_{OH}	IOH = -100uA	-	0.9 V_{dd}	-	-	V
Low level output voltage	V_{OL}	IOL = 100uA	-	-	-	0.1 V_{dd}	V
OTP Program voltage	V_{PP}	-	VPP	-	8.25	-	V
Typical power panel	P_{TYP}	-	-	-	15	150	mW
Deep sleep mode	P_{STPY}	-	-	-	3	-	uW
Typical operating current	Iopr_VDD	V_{dd} =3.0V-	-	-	5	50	mA

Sleep mode current	Islp_VDD	VDD=3.0V DC/DC OFF No clock No output load Ram data retain	VDD	-	26	--	uA
Deep sleep mode current	IdslpVDD	VDD=3.0V DC/DC OFF No clock No output loadRam data not retain	VDD	-	1	--	uA
Operation temperature range	T_{OPR}	-	-	0	-	50	°C
Operation illuminance intensity	E	indoor only	-	-	-	2000	lux
Storage temperature range	T_{STG}	-	-	-25	-	60	°C
Storage relative humidity	RHst	-	-	30	-	60	%RH

Notes: 1. The typical power is measured with following transition: from horizontal 2 gray scale pattern to vertical 2 gray scale pattern. (Figure 10-2)

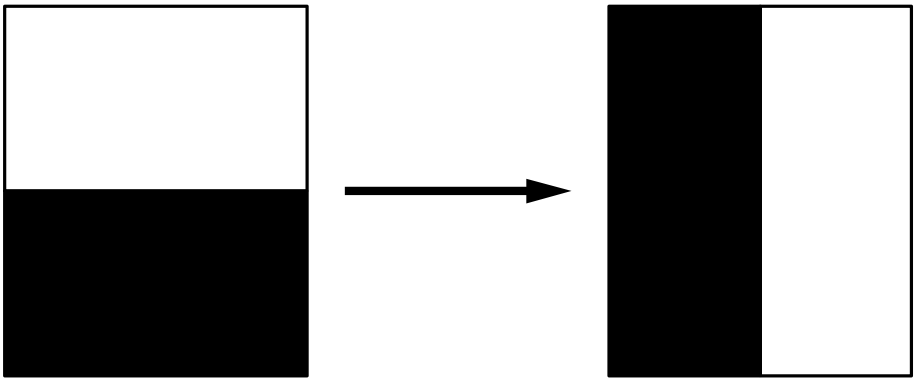


Figure 10-2 The typical power consumption measure pattern

2. The deep sleep power is the consumed power when the panel controller is in deep sleep mode.

3. The listed electrical/optical characteristics are only guaranteed under the controller & waveform providedby SID.

6.3 Panel DC Characteristics(Driver IC Internal Regulators)

The following specifications apply for: VSS=0V, VDD =3.0V, T_{OPR} =25ºC.

Parameter	Symbol	Condition	Applicable pin	Min.	Typ.	Max.	Unit
VCOM output voltage	VCOM	-	VCOM		-0.8		V

6.4 Panel AC Characteristics

6.4.1 MCU Interface Selection

MCU interface consist of 2 data/command pins and 3 control pins. The pin assignment at different interface mode is summarized in Table 10-4-1. Different MCU mode can be set by hardware selection on BS pins. The display panel only supports 4-wire SPI or 3-wire SPI interface mode.

Pin Name	**Data/Connnand Interface**		**Control Signal**		
Bus interface	**SDA**	**SCL**	**CSB**	**D/C**	**RSTN**
4-wire SPI	SDIN	SCLK	CSB	D/C	RSTN
3-wire SPI	SDIN	SCLK	CSB	L	RSTN

Table 10-4-1: MCU interface assignment under different bus interface mode

6.4.2 MCU Serial Interface (4-wire SPI)

The serial interface consists of serial clock SCLK, serial data SDIN, D/C, CSB. In 4-wire SPI mode, SCL acts as SCLK, SDA acts as SDIN.

Function	**CSB**	**D/C**	**SCLK**
Write command	L	L	↑
Write data	L	H	↑

Note: ↑ stands for rising edge of signal

Table10-4-2: Control pins of 4-wire Serial interface

SDIN is shifted into an 8-bit shift register on every rising edge of SCLK in the order of D7, D6, ... D0. D/C is sampled on every eighth clock and the data byte in the shift register is written to the Graphic Display Data RAM (RAM) or command register in the same clock.

Under serial mode, only write operations are allowed.

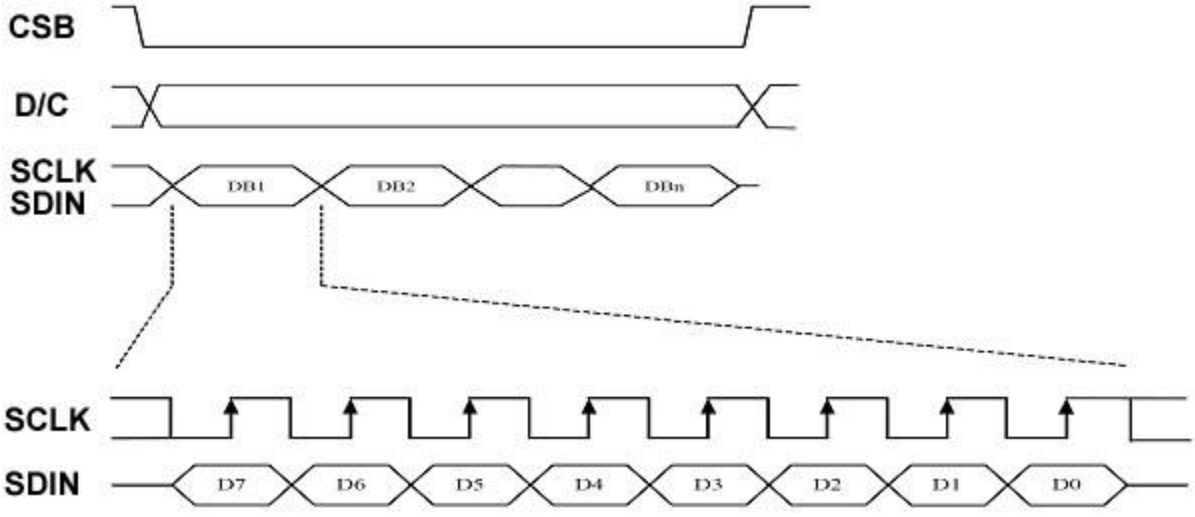


Figure 10-4-2: Write procedure in 4-wire SPI mode

6.4.3 MCU Serial Interface (3-wire SPI)

The 3-wire serial interface consists of serial clock SCLK, serial data SDIN and CSB. In 3-wire SPI mode, SCL acts as SCLK, SDA acts as SDIN.

The operation is similar to 4-wire serial interface while D/C pin is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: D/C bit, D7 to D0 bit. The D/C bit (first bit of the sequential data) will determine the following data byte in the shift register is written to the Display Data RAM (D/Cbit = 1) or the command register (D/C bit = 0).

Under serial mode, only write operations are allowed.

Function	CSB	D/C	SCLK
Write command	L	Tie	↑
Write data	L	Tie	↑

Note：↑ stands for rising edge of signal

Table 10-4-3: Control pins of 3-wire Serial interface

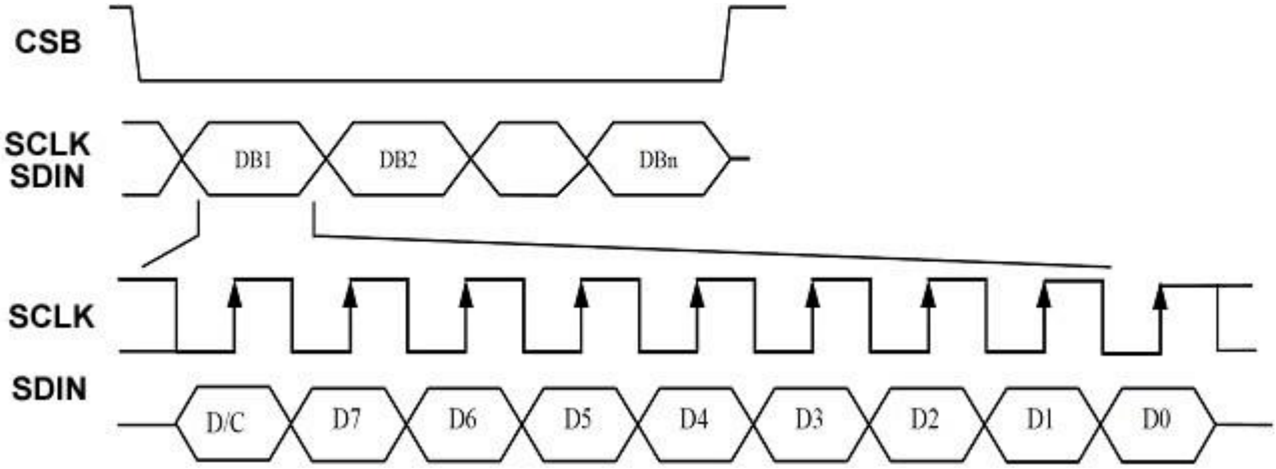


Figure 10-4-3: Write procedure in 3-wire SPI mode

6.4.4 Interface Timing

The following specifications apply for: VSS=0V, VDD =3.0V, T_{OPR} =25ºC.

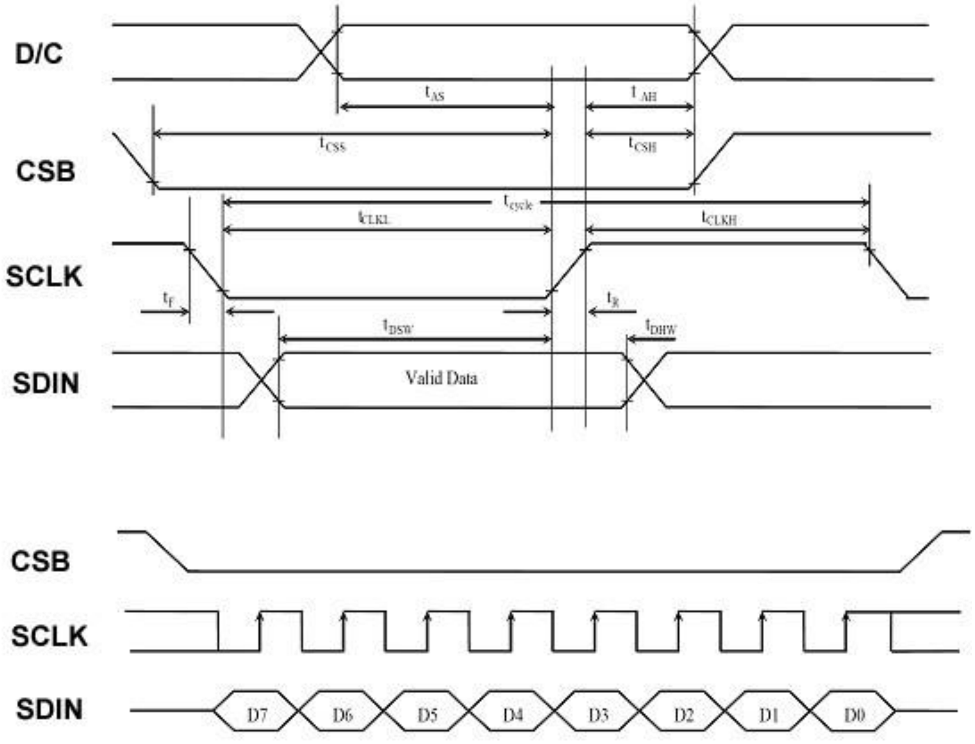

D/C
CSB
SCLK
SDIN
t_{AS}
t_{AH}
t_{CSS}
t_{CSH}
t_{cycle}
t_{CLKL}
t_{CLKH}
t_F
t_R
t_{DSW}
t_{DHW}
Valid Data
CSB
SCLK
SDIN
D7
D6
D5
D4
D3
D2
D1
D0

Figure 10-4-4: Serial interface characteristics

(V_{dd} - VSS = 2.4V to 3.3V, T_{OPR} = 25°C, CL=20pF)

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{cycle}	Clock Cycle Time	250	-	-	ns
t_{AS}	Address Setup Time	150	-	-	ns
t_{AH}	Address Hold Time	150	-	-	ns
t_{CSS}	Chip Select Setup Time	120	-	-	ns
t_{CSH}	Chip Select Hold Time	60	-	-	ns
t_{DSW}	Write Data Setup Time	50	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{CLKL}	Clock Low Time	100	-	-	ns
t_{CLKH}	Clock High Time	100	-	-	ns
t_R	Rise Time [20% ~ 80%]	-	-	15	ns
t_F	Fall Time [20% ~80%]	-	-	15	ns

Table 10-4-4: Serial Interface Timing Characteristics

7 Optical Specification

Measurements are made with that the illumination is under an angle of 45 degrees, the detection is perpendicular unless otherwise specified.

Symbol	**Parameter**	**Conditions**	**Values**			**Units**	**Notes**
			Min.	Typ.	Max		
R	White Reflectivity	White	30	35	-	%	11-1
CR	Contrast Ratio		8:1	10:1	-	-	11-2
White△L 24h	Reduce		-	≤4	-	-	-
T_{update}	Image update time	at 25 °C	-	2800	-	ms	-

Notes: 11-1. Luminance meter: Eye-One Pro Spectrophotometer.

11-2. CR=Surface Reflectance with all white pixel/Surface Reflectance with all black pixels.

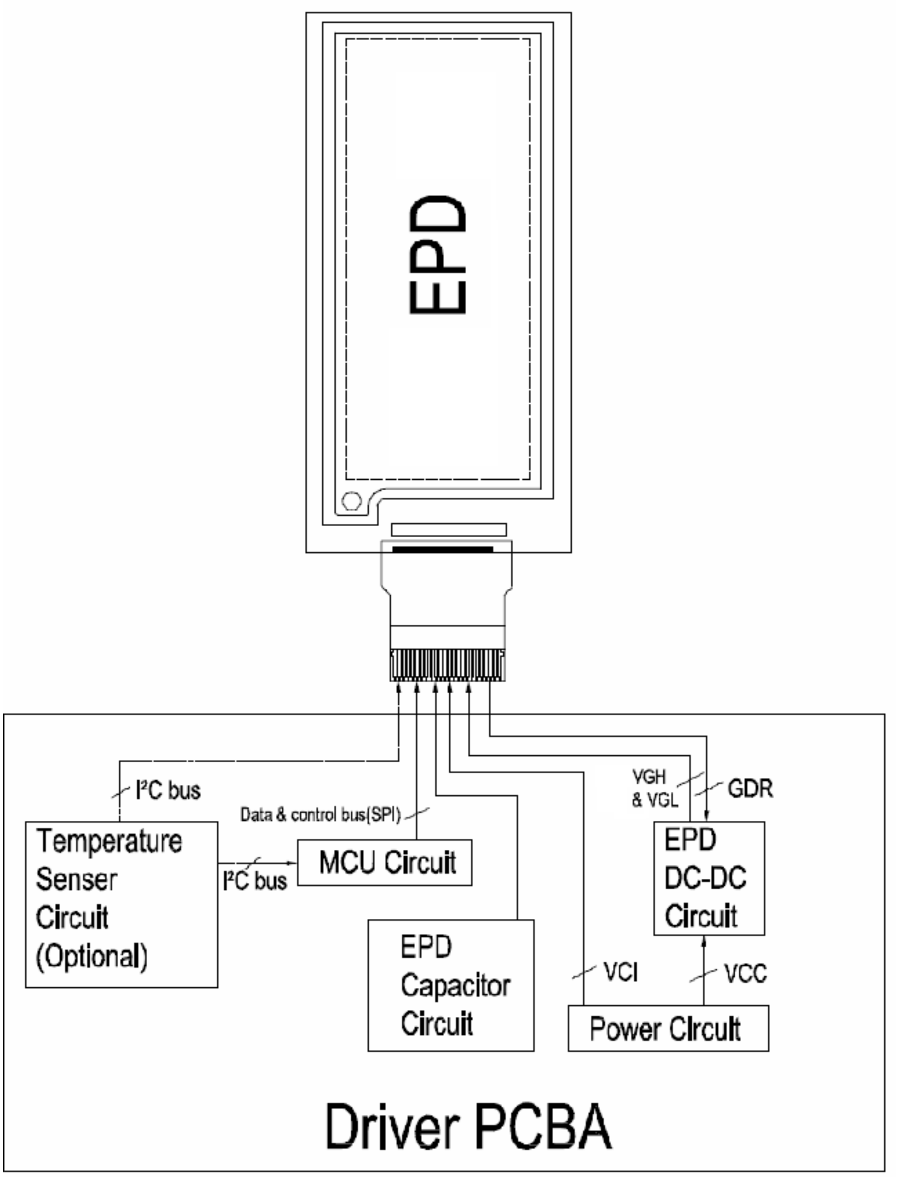
8 Handling, Safety, and Environment Requirements

1. The EPD Panel / Module is manufactured from fragile materials such as glass and plastic, and may be broken or cracked if dropped. Please handle with care. Do not apply force such as bending or twisting to the EPD panel
2. The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.
3. Do not apply pressure to the EPD panel in order to prevent damaging it
4. Do not connect or disconnect the interface connector while the EPD panel is in operation
5. Do not stack the EPD panels / Modules.
6. Keep the EPD Panel / Module in the specified environment and original packing boxes whenstorage in order to avoid scratching and keep original performance.
7. Do not disassemble or reassemble the EPD panel
8. Use a soft dry cloth without chemicals for cleaning. Please don't press hard for cleaning because the surface of the protection sheet film is very soft and without hard coating. This behavior would make dent or scratch on protection sheet
9. Please be mindful of moisture to avoid its penetration into the EPD panel, which may cause damage during operation
10. It's low temperature operation product. Please be mindful the temperature different to make frost or dew on the surface of EPD panel. Moisture may penetrate into the EPD panel because of frostor dew on surface of EPD panel, and makes EPD panel damage.
11. High temperature, high humidity, sunlight or fluorescent light may degrade the EPD panel's performance. Please do not expose the unprotected EPD panel to high temperature, high humidity, sunlight, or fluorescent for long periods of time. Please store the EPD panel in controllable environment of warehouse and original package. Without sunlight, without condensation a temperature range of 15ºC to 35ºC, and humidity from 30%RH to 60%RH.

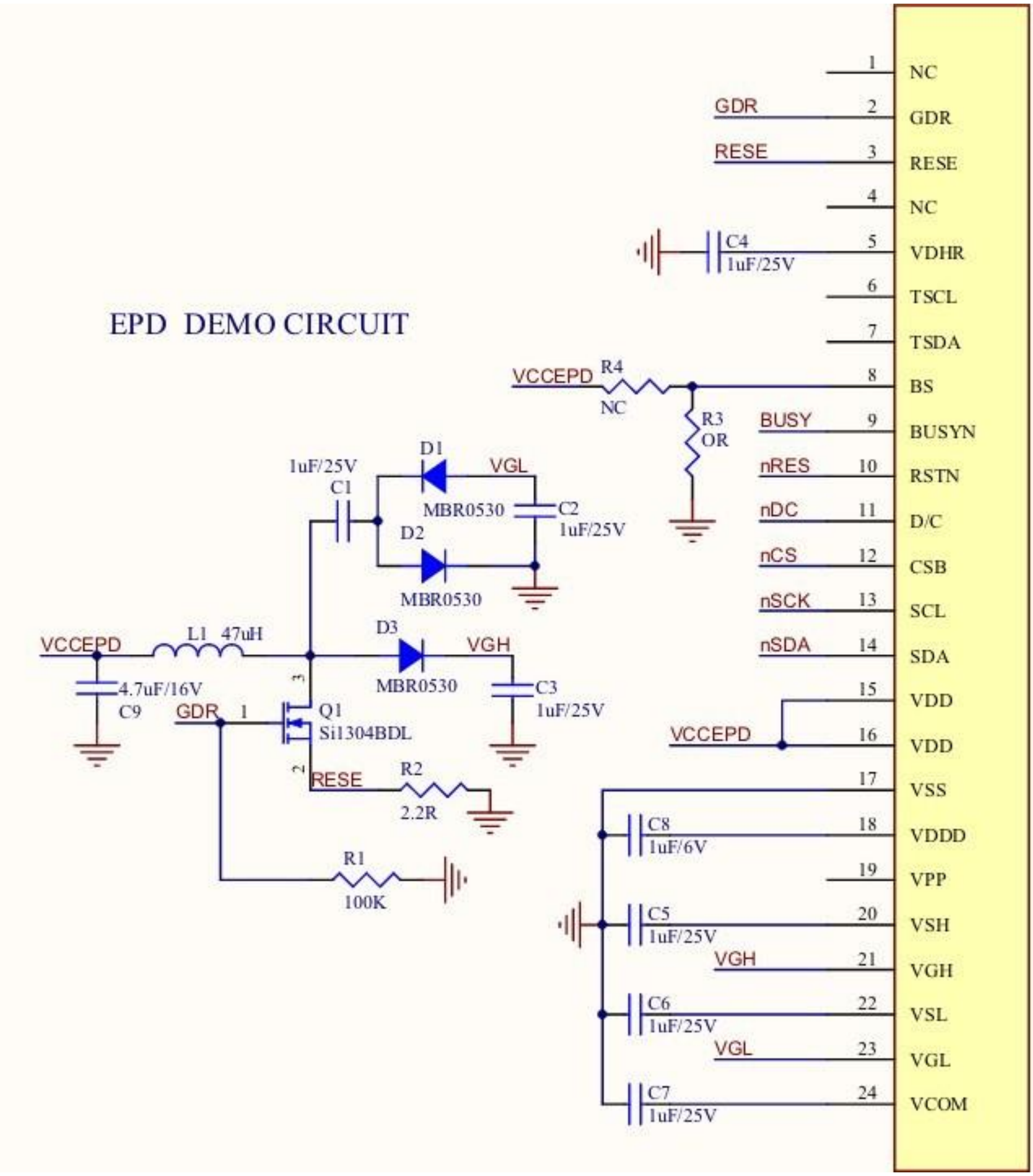
9 Reliability Test

No.	Test	Condition	Method	Remark
1	High-Temperature Operation	T = +50°C, RH = 30% for 240 hrs	IEC 60 068-2-2Bp	At the end of the test, electrical,mechanical, and optical specifications shall be satisfied.
2	Low-Temperature Operation	T = 0°C for 240 hrs	IEC 60 068-2-2Ab	At the end of the test, electrical,mechanical, and optical specifications shall be satisfied.
3	High-Temperature Storage	T = +70°C, RH=23% for 240 hrs	IEC 60 068-2-2Bp	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
4	Low-Temperature Storage	T = -25°C for 240 hrs	IEC 60 068-2-1Ab	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
5	High-Temperature, High-Humidity Operation	T = +40°C, RH = 90% for 168 hrs	IEC 60 068-2-3CA	At the end of the test, electrical,mechanical, and optical specifications shall be satisfied.
6	High Temperature, High-Humidity Storage	T = +60°C, RH=80% for 240hrs	IEC 60 068-2-3CA	At the end of the test, electrical,mechanical, and optical specifications shall be satisfied.
7	Thermal Shock	1 cycle:[-25°C 30min]→[+70 °C 30 min] : 100 cycles	IEC 60 068-2-14	At the end of the test, electrical, mechanical, and optical specifications shall be satisfied.
8	Package Vibration	1.04G, Frequency:10~500Hz Direction: X,Y,Z Duration: 1 hours in each direction	Full packedfor shipment	At the end of the test, electrical,mechanical, and optical specifications shall be satisfied.
9	Package DropImpact	Drop from height of 122 cm on concrete surface. Drop sequence:1 corner, 3edges, 6 faces One drop for each	Full packedfor shipment	At the end of the test, electrical,mechanical, and optical specifications shall be satisfied.
10	Electrostatic Effect (non-operating)	Machine model +/- 250V, 0Ω, 200pF	IEC 62179, IEC 62180	At the end of the test, electrical,mechanical, and optical specifications shall be satisfied.

10 Block Diagram


EPD
I²C bus
Data & control bus(SPI)
VGH & VGL
GDR
Temperature Senser Circuit (Optional)
I²C bus
MCU Circuit
EPD DC-DC Circuit
EPD Capacitor Circuit
VCI
VCC
Power CIrcuit
Driver PCBA

11 Typical Application Circuit with SPI Interface


EPD DEMO CIRCUIT
1 NC
2 GDR
3 RESE
4 NC
5 VDHR
6 TSCL
7 TSDA
8 BS
9 BUSYN
10 RSTN
11 D/C
12 CSB
13 SCL
14 SDA
15 VDD
16 VDD
17 VSS
18 VDDD
19 VPP
20 VSH
21 VGH
22 VSL
23 VGL
24 VCOM
GDR
RESE
C4 1uF/25V
VCCEPD
R4 NC
R3 OR
BUSY
nRES
nDC
nCS
nSCK
nSDA
1uF/25V C1
D1 MBR0530
VGL
C2 1uF/25V
D2 MBR0530
D3 MBR0530
VGH
C3 1uF/25V
VCCEPD
L1 47uH
4.7uF/16V C9
GDR 1
Q1 Si1304BDL
RESE
R2 2.2R
R1 100K
VCCEPD
C8 1uF/6V
C5 1uF/25V
VGH
C6 1uF/25V
VGL
C7 1uF/25V

12 Packaging

TBD

13 Mark and Bar Code Definition

TBD

14 Inspection Standard

14.1 Appearances Inspection Standard

14.1.1 Appearances Specification

This appearance inspection shall be applied to segment EPD modules.

14.1.2 Inspection Conditions Viewing Angle: α =±45°

Viewing Distance: 30cm±10cm Ambient Luminance: 700~1000 Lux.

Supply Voltage: Typical value described on the Electrical CharacteristicsEnvironment

Ambient Temperature: 20℃~25℃

Environment Ambient Humidity: 40~70%RHESD should be controlled within ±200V

14.1.3 Inspection Level: Level II

Sampling table: GB/T 2828.1-2012 II, unless otherwise agreed in writing.

14.1.4Acceptance Quality Level (AQL) Major Defect: 0.65 , Minor Defect: 1.5

14.1.5 Classification of Defects

Defects are classified as either a major or a minor defect defined as below.

Major Defect :It is a defect that is likely to result in failure or to reduce materially the usability of the product for the intended function.

Minor Defect :It is a defect that will not result in functioning problem with deviation classified.

14.2 Quality Criteria

14.2.1 Zone Definitions

A Zone: EPD Active Area (not including border)B

Zone: Out of Active Area

14.2.2 Appearances Criteria

As shown in the tables below. If any other items, standard values or applicable zones are required to be defined, a written agreement shall be signed, and otherwise a limited sample shall be made for reference.

Major Defects:

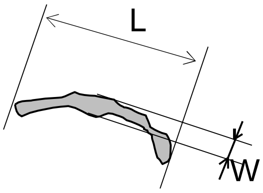
Item	Description	Classification
No Display	No display shown on screen due to malfunction	Major
Line Missing	Line missing	Major
Abnormal Display	Unusual pattern or function displayed	Major
TFT Broken	TFT broken by external force	Major

Minor Defects:

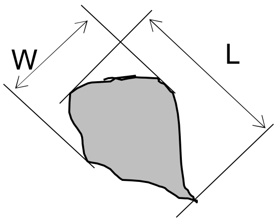
Item		Criteria	Specific Zone	
Name	Description		A Zone	B Zone
Dot defect	Spot/ Air bubble/ Foreign material in dot shape	D≤0.30mm	Ignore	Ignore
		0.30mm＜D≤0.50mm	≤5	
		D＞0.50mm	0	
Line defect	Scratch on top surface/ Foreign material in line or spiral shape	L≤1.0 mm , W≤0.15mm	Ignore	Ignore
		1.0mm＜L≤5.0mm & 0.15mm＜W≤0.5mm	≤4	
		L＞5.0mm or W＞0.5mm	0	
Chipping	Corner chip	Not affect the display, not have diffuse or comminuted cracks		
	Edge chip			
Curl	Curl for Panel	≤1.0 mm		

Remarks:

Definitions of “line” and “dot”:

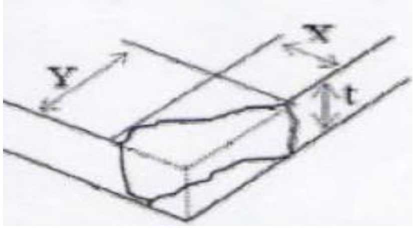


a. Line

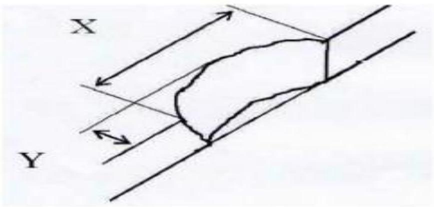


b. Dot

When L≤0.5mm or L＜4W, defined as a dot. Definitions of “Chipping”:



c. Corner chip



d. Edge chip