RTL8723BU

Single-Chip IEEE 802.11b/g/n 1T1R WLAN with Integrated Bluetooth 2.1/3.0/4.0 Controller with USB 2.0 Multi-Function Interface

DATASHEET

(CONFIDENTIAL: Development Partners Only)

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USING THIS DOCUMENT

This document is intended for the software engineer’s reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

REVISION HISTORY

Revision	Release Date	Summary
0.1	2012/08/09	Preliminary release.

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1. General Description

The Realtek RTL8723BU is a highly integrated single-chip 802.11n Wireless LAN (WLAN) USB 2.0 Multi-Function network interface controller with integrated Bluetooth 2.1/3/0/4.0 controller. It combines a WLAN MAC, a 1T1R capable WLAN baseband, and RF in s single chip. The RTL8723BU provides a complete solution for a high-performance integrated wireless and Bluetooth device. The integration provides better coordination between 802.11 and Bluetooth, and with sophisticated dynamic power control and packet traffic arbitration, RTL8723BU is able to provide the best coexistence performance.

The RTL8723BU WLAN MAC supports 802.11e for multimedia applications, 802.11i for security, and 802.11n for enhanced MAC protocol efficiency. Using packet aggregation techniques such as A-MPDU with BA and A-MSDU, protocol efficiency is significantly improved. Power saving mechanisms such as Legacy Power Save, and U-APSD, reduce the power wasted during idle time, and compensate for the extra power required to transmit OFDM.

A RTL8723BU built-in enhanced signal detector, adaptive frequency domain equalizer, and a soft-decision Viterbi decoder help to alleviate multi-path effects and mutual interference in the reception of multiple streams. Robust interference detection and suppression are provided to protect against Bluetooth, cordless phone, and microwave oven interference. The WLAN Controller supports fast receiver Automatic Gain Control (AGC) with synchronous and asynchronous control loops among antennas, antenna diversity functions, and adaptive transmit power control function to obtain better performance in the analog portions of the transceiver.

The RTL8723BU Efficient IQ-imbalance, DC offset, phase noise, frequency offset, and timing offset compensations are provided for the radio frequency front-end. Selectable digital transmit and receive FIR filters are provided to meet transmit spectrum mask requirements and to reject adjacent channel interference, respectively. RTL8723BU also integrates RF/PA/LNA/Balun/DPDT for both 802.11n and Bluetooth to reduce the number of external components.

The RTL8723BU Bluetooth controller complies with Bluetooth core specification v4.0, and supports dual mode (BR/EDR + AMP + Low Energy Controllers). It is backward compatible with previous versions including v2.1 + EDR and v3.0 + HS. For BR/EDR, it can support scatternet topology up to four active links in slave mode, and seven active links in master mode. For Low Energy, it supports multiple states and allows eight active links in master mode. Both BR/EDR and LE can operate simultaneously.

2. Features

General

- 56-pin QFN
- IEEE 802.11b/g/n 1T1R WLAN and Bluetooth single chip

Host Interface

- Complies with USB2.0 for WLAN and BT controller
- USB Multi-Function for both BT (USB function 0) and WLAN (USB function 1)
- USB LPM/ USB SS supported

WLAN Controller

- CMOS MAC, Baseband PHY, and RF in a single chip for IEEE 802.11b/g/n compatible WLAN
- Integrated Balun and DPDT
- Complete 802.11n solution for 2.4GHz band
- 72.2Mbps receive PHY rate and 72.2Mbps transmit PHY rate using 20MHz bandwidth
- 150Mbps receive PHY rate and 150Mbps transmit PHY rate using 40MHz bandwidth
- Backward compatible with 802.11b/g devices while operating in 802.11n mode
- IEEE 802.11b/g/n compatible WLAN
- IEEE 802.11e QoS Enhancement (WMM)
- IEEE 802.11i (WPA, WPA2). Open, shared key, and pair-wise key authentication services
- WAPI supported

WLAN MAC Features

- Frame aggregation for increased MAC efficiency (A-MSDU, A-MPDU)
- Low latency immediate High-Throughput Block Acknowledgement (HT-BA)
- PHY-level spoofing to enhance legacy compatibility
- Multi MACID support with Fast Channel switch
- Channel management and co-existence
- Transmit Opportunity (TXOP) Short Inter-Frame Space (SIFS) bursting for higher multimedia bandwidth
- WiFi Direct supports wireless peer to peer applications

WLAN PHY Features

- IEEE 802.11n OFDM
- One Transmit and one Receive path (1T1R)
- 20MHz and 40MHz bandwidth transmission
- Support 2.4GHz band channels
- Short Guard Interval (400ns)
- DSSS with DBPSK and DQPSK, CCKmodulation with long and short preamble

- OFDM with BPSK, QPSK, 16QAM, 64QAM modulation.
  Convolutional Coding Rate: 1/2, 2/3, 3/4, and 5/6
- Maximum data rate 54Mbps in IEEE 802.11g; and 150Mbps in IEEE 802.11n
- Switch diversity for DSSS/CCK
- Packet based hardware antenna diversity
- Selectable receiver FIR filters
- Programmable scaling in transmitter and receiver to trade quantization noise against increased probability of clipping
- Fast receiver Automatic Gain Control (AGC)
- On-chip ADC and DAC

Other Features

- Supports Wake-On-WLAN via Magic Packet and Wake-up frame
- Support S3/S4 AES/TKIP group key update
- Support Win8 Network List Offload
- Support TCP/UDP/IP checksum offload

Bluetooth Controller

- Compatible with Bluetooth v2.1 and v3.0 Systems
- Supports Bluetooth 4.0 Low Energy(BLE)
- Integrated MCU to execute Bluetooth protocol stack
- Supports all packet types in basic rate and enhanced data rate
- Supports 4 piconets in a scatternet
- Supports Secure Simple Pairing
- Supports Low Power Mode (Sniff/Sniff Sub-rating/Hold/Park)
- Enhanced BT/WIFI Coexistence Control to improve transmission quality in different profiles
- Bluetooth 4.0 Dual Mode support: Simultaneous LE and BR/EDR
- Supports multiple Low Energy states
- Support 3D Glasses application
- Support Intel Latency Tolerance Reporting (LTR)

Bluetooth Transceiver

- Fast AGC control to improve receiving dynamic range
- Supports AFH to dynamically detect channel quality to improve transmission quality
- Integrated internal Class 1, Class 2, and Class 3 PA
- Bluetooth 3.0+HS compliant
- Supports Enhanced Power Control
- Supports Bluetooth Low Energy
- Integrated 32K oscillator for power management

Peripheral Interfaces

- General Purpose Input/Output (8 pins)
- 4-wire EEPROM control interface (93C46)

- Three configurable LED pins
- Flexible XTAL frequency selection(52, 48, 40, 38.4, 27, 26, 25, 24, 20, 19.2, 17.664, 16, 14.318, 13 and 12MHz)
- Support XTAL or external clock input

3. Application Diagram

3.1. Single-Band 11n (1x1) Solution with Integrated Bluetooth Controller with Antenna Diversity

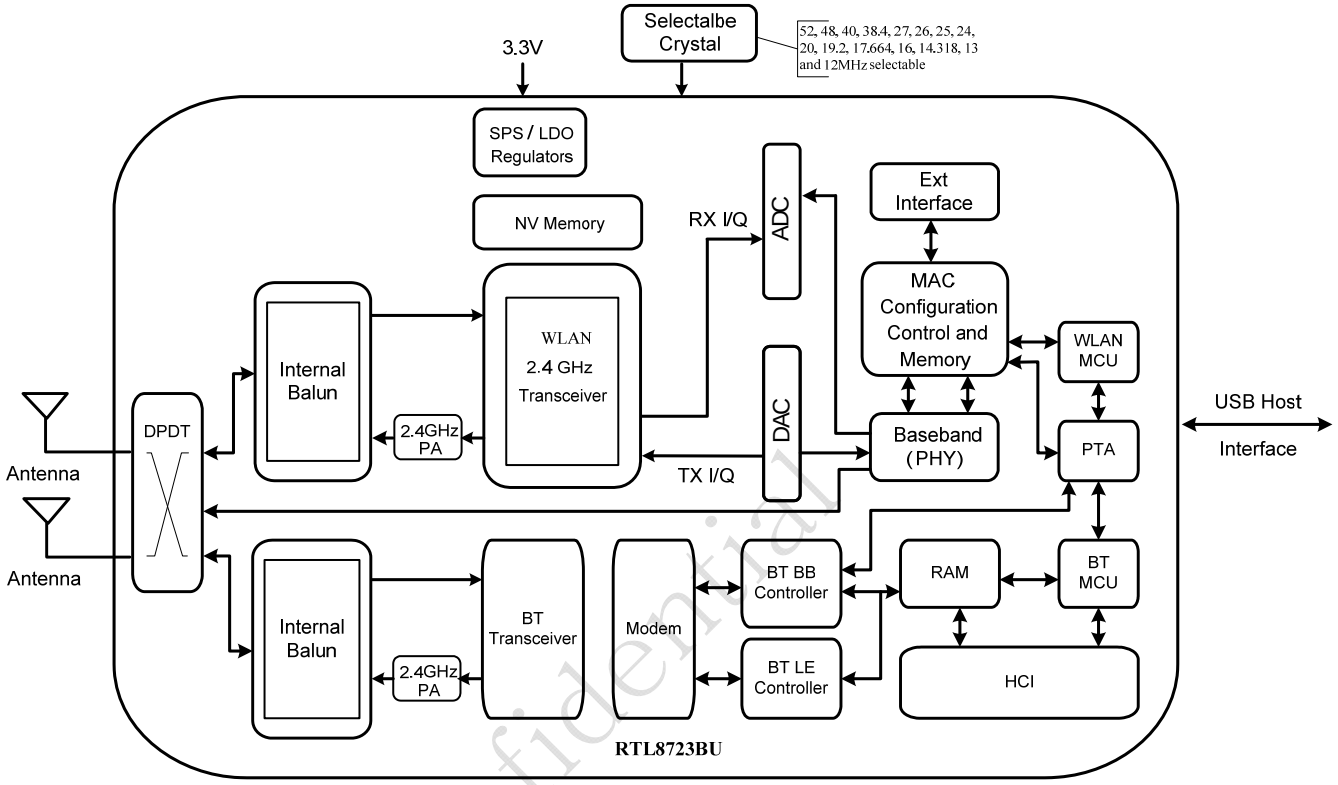


Figure 1. Single-Band 11n (1x1) and Integrated Bluetooth Controller Solution with Antenna Diversity

3.2. Single-Band 11n (1x1) Solution with Integrated Bluetooth Controller with Single Antenna

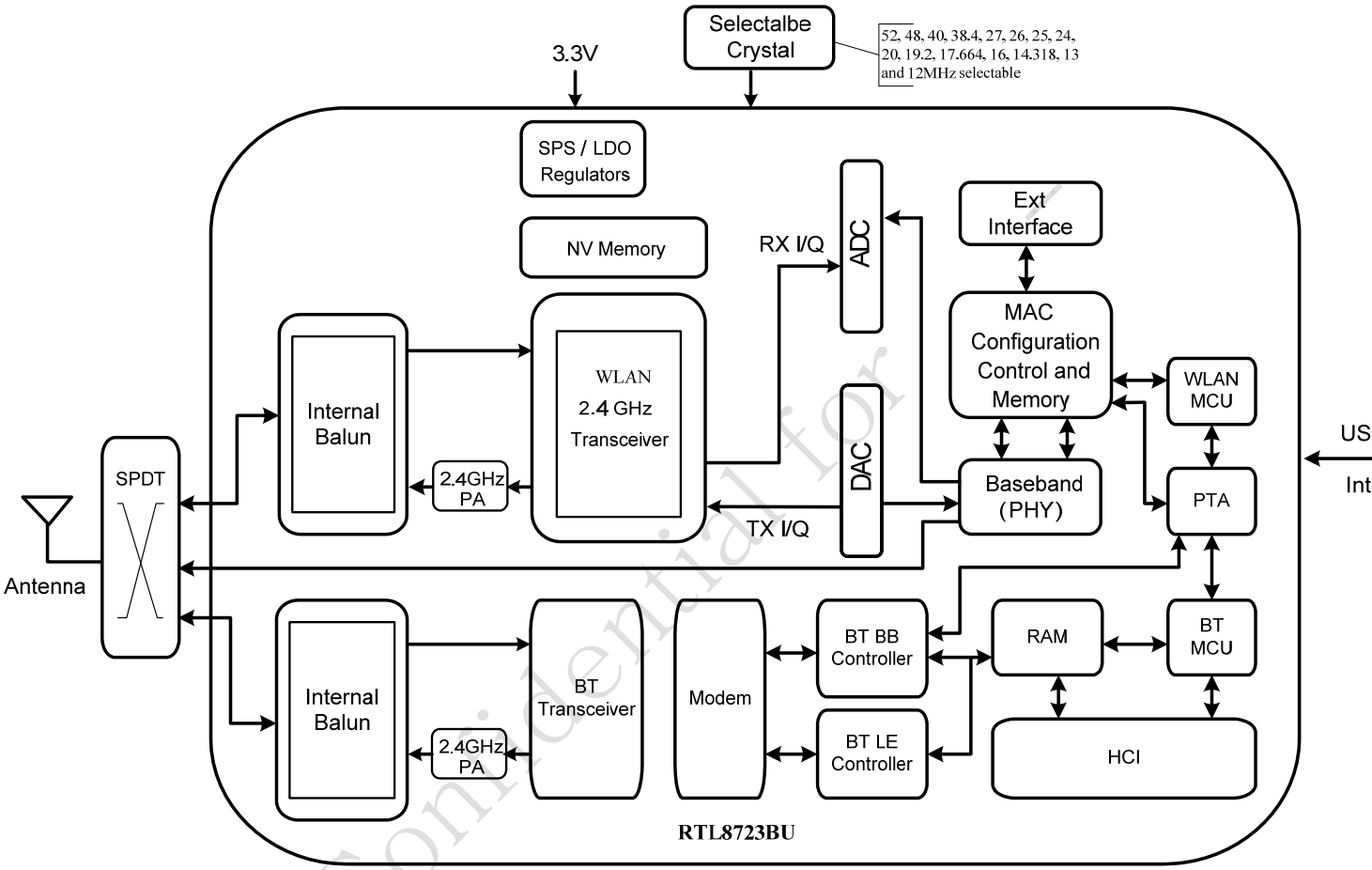


Figure 2. Single-Band 11n (1x1) and Integrated Bluetooth Controller Solution with Single Antenna

4. Pin Assignments

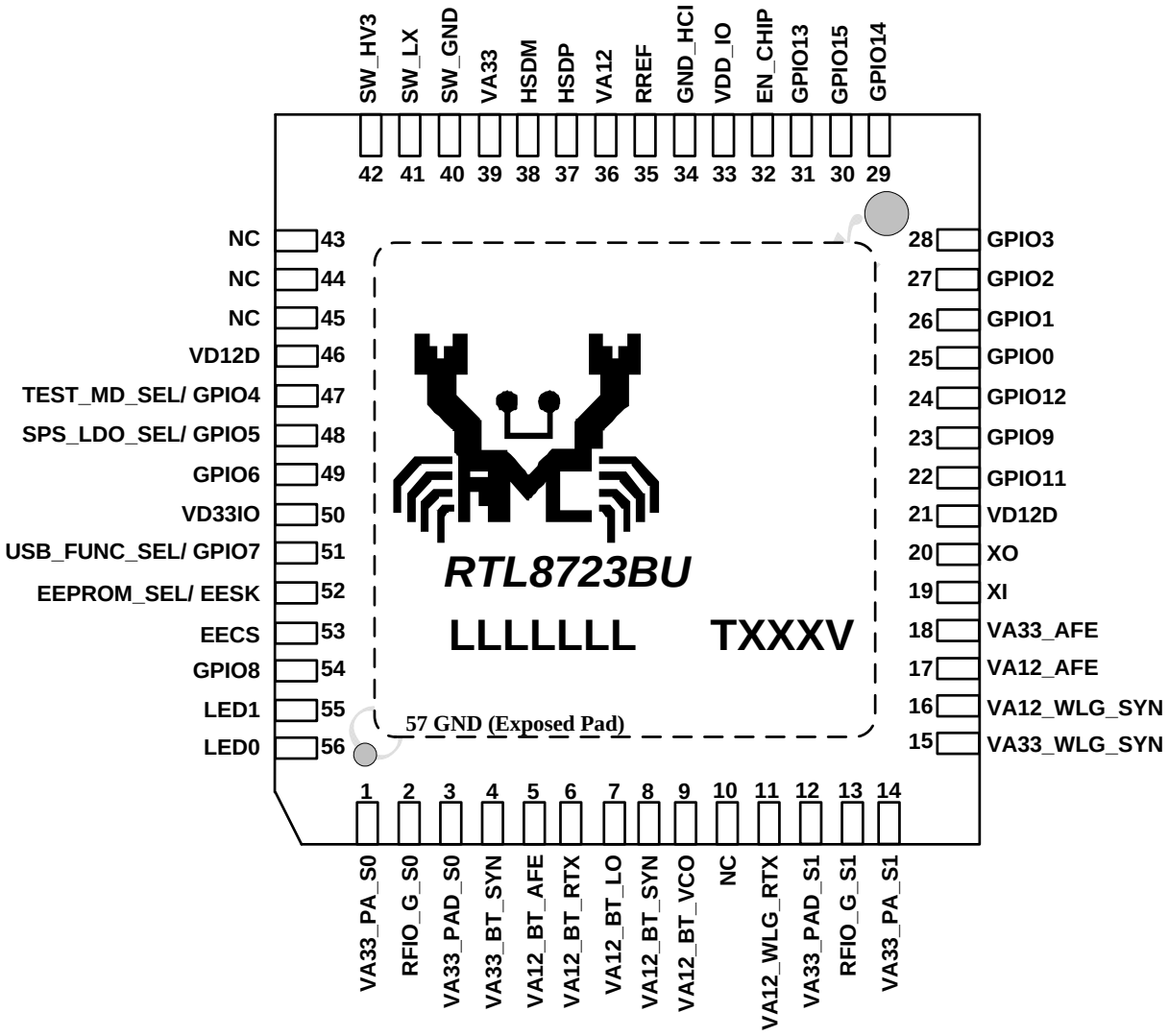


Figure 3. Pin Assignments

4.1. Package Identification

"Green" package is indicated by a 'G' in the location marked "T" in Figure 3.

5. Pin Descriptions

The following signal type codes are used in the tables:

I: Input O: Output

T/S: Tri-State bi-directional input/output pin S/T/S: Sustained Tri-State

O/D: Open Drain P: Power pin

5.1. Power On Trap Pin

Table 1. Power-On Trap Pins

Symbol	Type	Pin No	Description
TEST_MODE_SEL	I	47	Shared with GPIO4 0: Normal operation mode 1: Test/debug mode
SPS_LDO_SEL	I	48	Shared with GPIO5 0: Internal switching regulator select 1: Internal LDO select
USB_FUNC_SEL	I	51	Shared with GPIO7 0: USB 1.1 or 2.0 1: otherwise
EEPROM_SEL	I	52	Shared with EESK pin 0: Internal NV memory select 1: External EEPROM select

5.2. USB Transceiver Interface

Table 2. USB Transceiver Interface

Symbol	Type	Pin No	Description
HSDP	IO	37	High-Speed USB D+ Signal
HSDM	IO	38	High-Speed USB D- Signal

5.3. EEPROM Interface

Table 3. EEPROM Interface

Symbol	Type	Pin No	Description
EECS	O	53	External EEPROM Chip Select
EESK	O	52	External EEPROM Clock
EEDI	I	51	Shared with GPIO7. External EEPROM Data In
EEDO	O	49	Shared with GPIO6. External Data Out

5.4. PCM Interface

Table 4. PCM Interface

Symbol	Type	Pin No	Description
PCM_IN/GPIO0	I	25	PCM input shared with GPIO0
PCM_OUT/GPIO1	O	26	PCM output shared with GPIO1
PCM_SYNC/GPIO2	IO	27	PCM sync shared with GPIO2
PCM_CLK/GPIO3	IO	28	PCM clock shared with GPIO3

5.5. BT 3D Glass Interface

Table 5. BT 3D Glass Interface

Symbol	Type	Pin No	Description
3DG_SYNC_A	I	26	Shared with GPIO1. BT 3D Glass synchronization control port A.
3DG_SEL_A	I	25	Shared with GPIO0. BT 3D Glass select control port A.
3DG_SYNC_B	I	49	Shared with GPIO6. BT 3D Glass synchronization control port B.
3DG_SEL_B	I	53	Shared with EECS. BT 3D Glass select control port B.

5.6. RF Interface

Table 5. RF Interface

Symbol	Type	Pin No	Description
RFIO_G_S0	IO	2	WLAN/BT RF TX/RX signal port 0
RFIO_G_S1	IO	13	WLAN/BT RF TX/RX signal port 1
DPDT_SEL_P	O	52	Shared with EESK. Antenna Control Positive Signal
DPDT_SEL_N	O	53	Shared with EECS. Antenna Control Negative Signal

5.7. LED Interface

Table 6. LED Interface

Symbol	Type	Pin No	Description
LED0	O	56	LED Pin (Active Low)
LED1	O	55	LED Pin (Active Low)
LED2	O	54	LED Pin (Active Low), shared with GPIO8

5.8. Power Management Handshake Interface

Table 7. Power Management Handshake Interface

Symbol	Type	Pin No	Description
EN_CHIP	I	32	enable chip
BT_DIS_N/GPIO11	I	22	This Pin Can Externally Shutdown the RTL8723BU (no requirement for Extra Power Switch) when BT_DISn is pulled low This pin can also support the WLAN Radio-off function with host interface remaining connected.
WL_DIS_N/GPIO9	I	23	This Pin Can Externally Shutdown the RTL8723BU (no requirement for Extra Power Switch) when WL_DISn is pulled low This pin can also support the BT Radio-off function with host interface remaining connected.
GPIO12/WPS	I	24	This pin can be detected by WIFI controller to initiate WPS procedure
HOST_WAKE_CHIP/ GPIO13	I	31	Host wakeup chip pin
CHIP_WAKE_HOST/ GPIO14	O	29	chip wakeup host pin

5.9. Clock and Other Pins

Table 8. Clock and Other Pins

Symbol	Type	Pin No	Description
XI	I	19	40MHz OSC Input 40MHz crystal reference clock input
XO	O	20	40MHz Crystal reference clock output
SUS_CLK	I	49	Shared with GPIO6. External 32K or RTC clock input.
GPIO0	IO	25	General Purpose Input/Output Pin
GPIO1	IO	26	General Purpose Input/Output Pin
GPIO2	IO	27	General Purpose Input/Output Pin
GPIO3	IO	28	General Purpose Input/Output Pin
GPIO4	IO	47	General Purpose Input/Output Pin
GPIO5	IO	48	General Purpose Input/Output Pin
GPIO6	IO	49	General Purpose Input/Output Pin
GPIO7	IO	51	General Purpose Input/Output Pin
GPIO8	IO	54	General Purpose Input/Output Pin
GPIO9	IO	23	General Purpose Input/Output Pin
GPIO11	IO	22	General Purpose Input/Output Pin
GPIO12	IO	24	General Purpose Input/Output Pin
NC		10, 43~45,	No connection pins

5.10. Power Pins

Table 9. Power Pins

Symbol	Type	Pin No	Description
SW_LX	P	41	Switching Regulator Output
SW_HV3	P	42	Switching Regulator Input Or Linear Regulator input from 3.3V to 1.5V
VA33	P	39	3.3V for Interface Analog Circuit
VA33_PA_S0 VA33_PAD_S0 VA33_BT_SYN VA33_PAD_S1 VA33_PA_S1 VA33_WLG_SYN VA33_AFE	P	1 3, 4 ,12, 14, 15, 18	3.3V for RF Analog Circuit
VD33IO	P	50	VDD3.3V for Digital IO
VDD_IO	P	33	VDD for WAKE#, CLKREQ#, PERST#, GPIO0 to GPIO3 and GPIO9 to GPIO12 (3.3V)
VD12D	P	21, 46	VDD 1.2V Digital Circuit
VA12	P	36	1.2V for analog blocks

Symbol	Type	Pin No	Description
VA12_BT_AFE VA12_BT_RTX VA12_BT_LO VA12_BT_SYN VA12_BT_VCO	P	5 6 7 8 9	1.2V for BT RF analog circuit
VA12_WLG_RTX VA12_WLG_SYN VA12_AFE	P	11, 16, 17	1.2V for WL RF analog circuit
SW_GND	P	40	Switching Regulator Ground
GND_HCI	P	34	Ground for host interface
RREF	P	35	Precision Resistor for Bandgap

6. Electrical and Thermal Characteristics

6.1. Temperature Limit Ratings

Table 10. Temperature Limit Ratings

Parameter	Minimum	Maximum	Units
Storage Temperature	-55	+125	°C
Ambient Operating Temperature	0	70	°C
Junction Temperature	0	125	°C

6.2. DC Characteristics

6.2.1. Power Supply Characteristics

Table 11. DC Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Units
VA33, VA33_PAD_S0, VA33_PA_S0, VA33_PAD_S1 VA33_PA_S1, VA33_WLG_SYN, VA33_AFE, VD33IO, VDD_IO	3.3V Supply Voltage	3.0	3.3	3.6	V
VA12, VA12_BT, VA12_BT_SYN, VA12_WLG, VA12_WLG_SYN, VA12_AFE, VD12D	1.2V Core Supply Voltage	1.10	1.2	1.32	V
IDD33	3.3V Rating Current	-	-	600	mA

6.2.2. Digital IO Pin DC Characteristics

Table 12. 3.3V GPIO DC Characteristics

Symbol	Parameter	Minimum	Normal	Maximum	Units
V_{IH}	Input high voltage	2.0	3.3	3.6	V
V_{IL}	Input low voltage	--	0	0.9	V
V_{OH}	Output high voltage	2.97	--	3.3	V
V_{OL}	Output low voltage	0	--	0.33	V

Table 13. 2.8V GPIO DC Characteristics

Symbol	Parameter	Minimum	Normal	Maximum	Units
V_{IH}	Input high voltage	1.8	2.8	3.1	V
V_{IL}	Input low voltage	--	0	0.8	V
V_{OH}	Output high voltage	2.5	--	3.1	V
V_{OL}	Output low voltage	0	--	0.28	V

Table 14. 1.8V GPIO DC Characteristics

Symbol	Parameter	Minimum	Normal	Maximum	Units
V_{IH}	Input high voltage	1.7	1.8	2.0	V
V_{IL}	Input low voltage	--	0	0.8	V
V_{OH}	Output high voltage	1.62	--	1.8	V
V_{OL}	Output low voltage	0	--	0.18	V

7. Interface Timing Specification

7.1. USB Bus during Power On Sequence

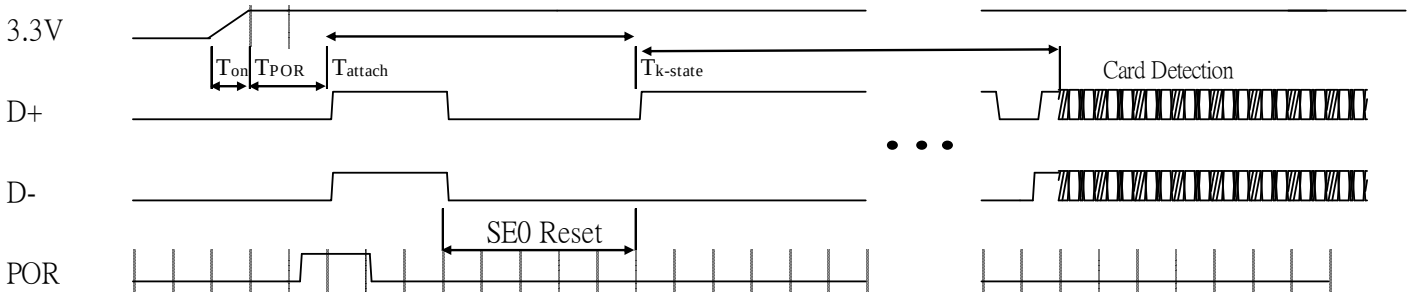


Figure 4. RTL8811AU USB Bus Power On Sequence
T_{on}: The main power ramp up duration
T_{por}: The power on reset releases and power management unit executes power on tasks
T_{attach}: USB attach state
$T_{k\text{-}state}$: the duration from resister attached to USB host starting card detection procedure

The power on flow description:
After main 3.3V ramp up, the internal power on reset is released by power ready detection circuit and the power management unit will be enabled. The power management unit enables the internal regulator and clock circuits.
The power management unit also enables the USB circuits.
USB analog circuits attach resisters to indicate the insertion of the USB device

Table 15. The typical timing range

	Unit	Min	Typical	Max
T_{on}	ms	--	1.5	5
T_{por}	ms	--	2	10
T_{attach}	ms	2	7	15
$T_{k\text{-}state}$	ms	50	250	--

7.2. PCM Interface Characteristics

The RTL8811AU supports a PCM digital audio interface that is used for transmitting digital audio/voice data to/from the Audio Codec. Features are supported as below:

- Supports Master and Slave mode
- Programmable long/short Frame Sync
- Supports 8-bit A-law/μ-law, and 13/16-bit linear PCM formats
- Supports sign-extension and zero-padding for 8-bit and 13-bit samples
- Supports padding of Audio Gain to 13-bit samples

- PCM Master Clock Output: 64, 128, 256, or 512kHz
- Supports SCO/ESCO link

7.2.1. PCM Format

FrameSync is the synchronizing function used to control the transfer of DAC_Data and ADC_Data. A Long FrameSync indicates the start of ADC_Data at the rising edge of FrameSync (Figure 5), and a Short FrameSync indicates the start of ADC_Data at the falling edge of FrameSync (Figure 6).

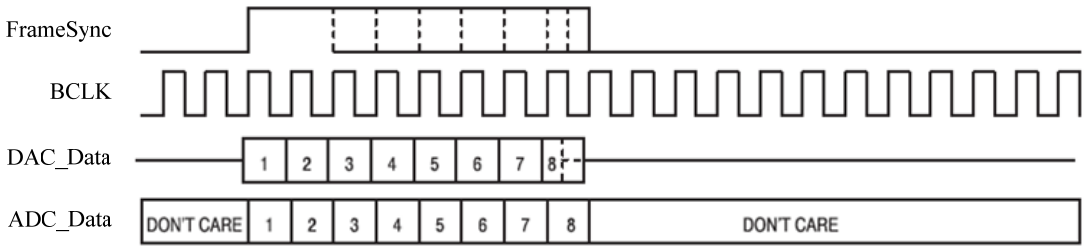


Figure 5. Long FrameSync

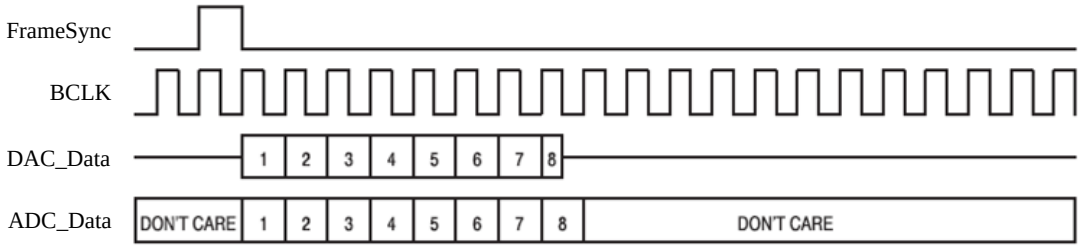


Figure 6. Short FrameSync

7.2.2. Sign Extension and Zero Padding for 8-Bit and 13-Bit Samples

For 16-bit linear PCM output, 3 or 8 unused bits may be sign extended/zero padded.

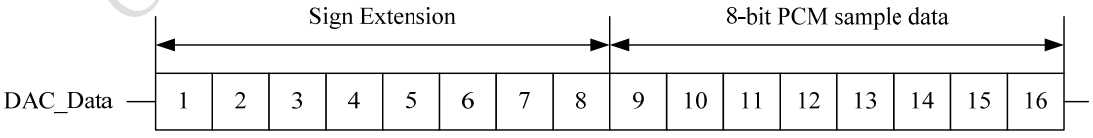


Figure 7. 16-Bit Output Data with 8-Bit PCM Sample Data and Sign Extension

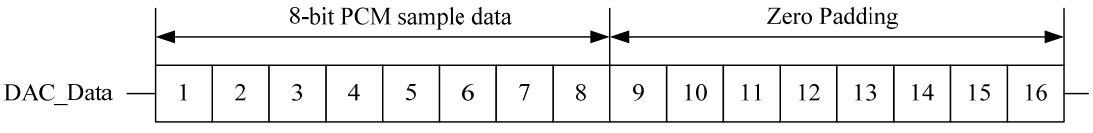


Figure 8. 16-Bit Output Data with 8-Bit PCM Sample Data and Zero Padding

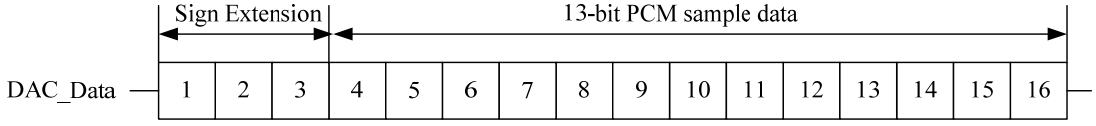


Figure 9. 16-Bit Output Data with 13-Bit PCM Sample Data and Sign Extension

For 16-bit linear PCM output, 3-bit programmable audio gain value can be padded to 13-bit sample data.

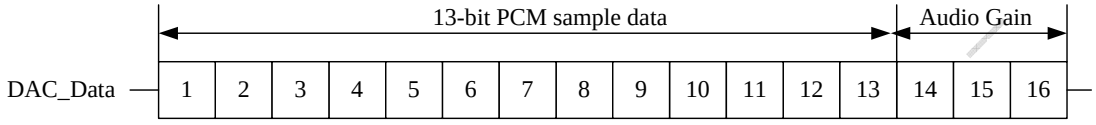


Figure 10. 16-Bit Output Data with 13-Bit PCM Sample Data and Audio Gain

7.2.3. PCM Interface Timing

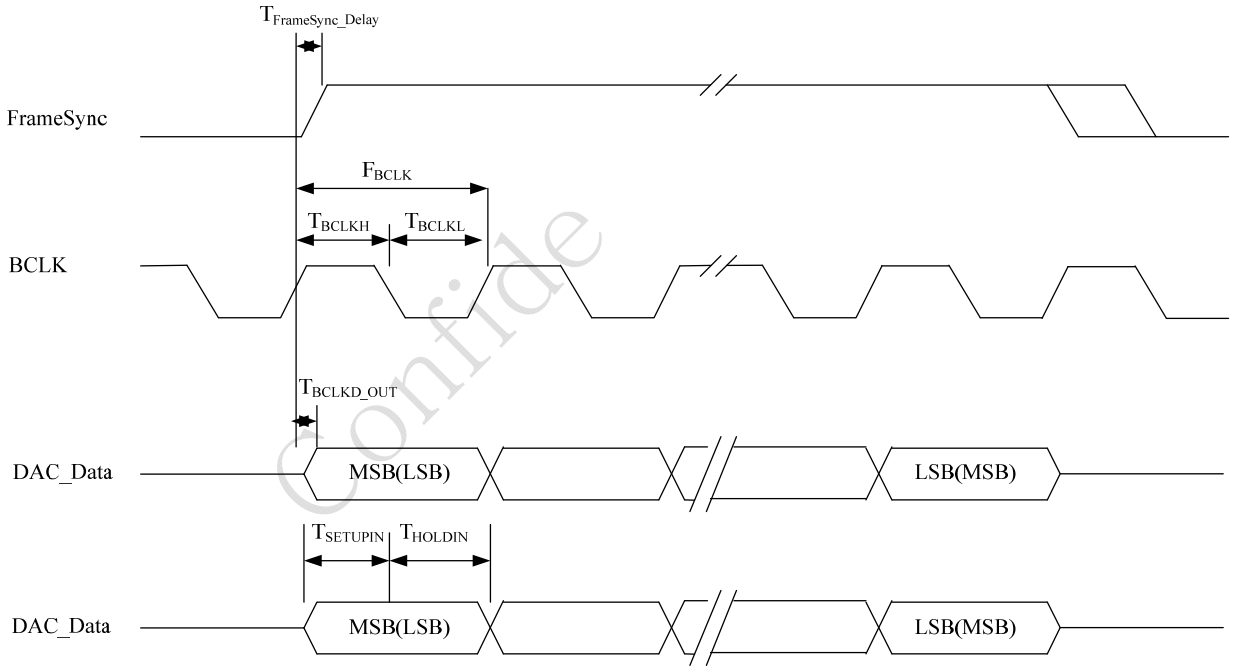
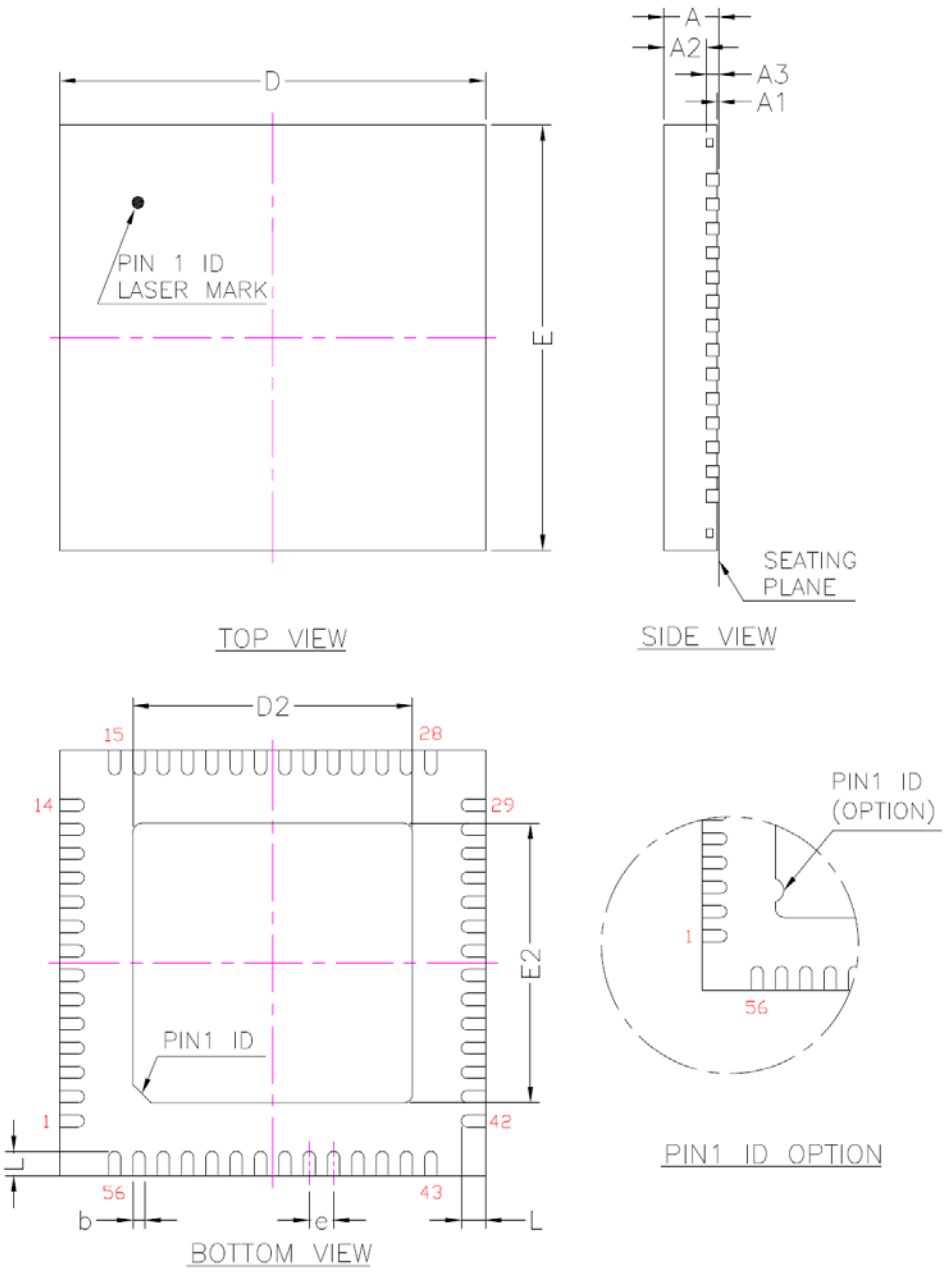


Figure 11. PCM Interface (Long FrameSync)

Figure 12. RTL8723BU PCIe and USB Bus Power On Sequence

8. Mechanical Dimensions



8.1. Mechanical Dimensions Notes

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	0.80	0.85	0.90	0.031	0.033	0.035
A_1	0.00	0.02	0.05	0.000	0.001	0.002
A_2	---	0.65	0.70	---	0.026	0.028
A_3	0.2 REF			0.008 REF		
b	0.15	0.20	0.25	0.006	0.008	0.010
D/E	7.00 BSC			0.276 BSC		
D_2/E_2	4.35	4.60	4.85	0.171	0.181	0.191
e	0.40 BSC			0.016 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020

Notes：

1. CONTROLLING DIMENSION：MILLIMETER(mm).

   REFERENCE DOCUMENTL：JEDEC MO-220.

9. Ordering Information

Table 16. Ordering Information

Part Number	Package	Status
RTL8723BU	QFN-68, 'Green' Package	To Be Available

Note: See page 7 for package identification.

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