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RTL8152B
RTL8152BN

INTEGRATED 10/100M ETHERNET CONTROLLER FOR USB APPLICATIONS

LAYOUT GUIDE

(CONFIDENTIAL: Development Partners Only)

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USING THIS DOCUMENT

This document is intended for the hardware engineer's reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

REVISION HISTORY

Revision	Release Date	Summary
1.0	2012/08/29	First release.

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1. Introduction

The Realtek RTL8152B/RTL8152BN 10/100M Ethernet controller combines an IEEE 802.3u compliant Media Access Controller (MAC), USB bus controller, and embedded memory. A linear regulator (LDO) is incorporated for reduced BOM cost.

With state-of-the-art DSP technology and mixed-mode signal technology, the RTL8152B/RTL8152BN offers high-speed transmission over CAT 5 UTP cable or CAT 3 UTP (10Mbps only) cable. Functions such as Crossover Detection and Auto-Correction, polarity correction, adaptive equalization, cross-talk cancellation, echo cancellation, timing recovery, and error correction are implemented to provide robust transmission and reception capabilities. The RTL8152B/RTL8152BN features embedded One-Time-Programmable (OTP) memory.

Advanced Configuration Power management Interface (ACPI)—power management for modern operating systems that are capable of Operating System-directed Power Management (OSPM)—is supported to achieve the most efficient power management possible. In addition to the ACPI feature, remote wake-up (including AMD Magic Packet and Microsoft Wake-Up Frame) is supported in both ACPI and APM (Advanced Power Management) environments.

The RTL8152B/RTL8152BN supports Microsoft Wake Packet Detection (WPD) to provide Wake-Up Frame information to the OS, e.g., PatternID, OriginalPacketSize, SavedPacketSize, SavedPacketOffset, etc. WPD helps prevent unwanted/unauthorized wake-up of a sleeping computer.

The RTL8152B/RTL8152BN supports 'RealWoW!' Technology which enables remote wake-up of a sleeping PC through the Internet. This feature allows PCs to reduce power consumption by remaining in low power sleeping state until needed.

Note: The 'RealWoW!' service requires registration on first time use.

The RTL8152B/RTL8152BN is fully compliant with Microsoft NDIS5, NDIS6 (IPv4, IPv6, TCP, UDP) Checksum features, and supports IEEE 802 IP Layer 2 priority encoding and IEEE 802.1Q Virtual bridged Local Area Network (VLAN). The above features contribute to lowering CPU utilization, especially benefiting performance when in operation on a network server.

The RTL8152B/RTL8152BN supports Protocol offload. It offloads some of the most common protocols to NIC hardware in order to prevent spurious wake-up and further reduce power consumption. The RTL8152B/RTL8152BN can offload ARP (IPv4) and NS (IPv6) protocols while in the D3 power saving state.

The RTL8152B/RTL8152BN supports the ECMA (European Computer Manufacturers Association) proxy for sleeping hosts standard. The standard specifies maintenance of network connectivity and presence via proxies in order to extend the sleep duration of higher-powered hosts. It handles some network tasks on behalf of the host, allowing the host to remain in sleep mode for longer periods. Required and optional behavior of an operating proxy includes generating reply packets, ignoring packets, and waking the host.

The RTL8152B/RTL8152BN supports IEEE 802.3az-2010, also known as Energy Efficient Ethernet (EEE). IEEE 802.3az operates with the IEEE 802.3 Media Access Control (MAC) Sublayer to support

operation in Low Power Idle mode. When the Ethernet network is in low link utilization, EEE allows systems on both sides of the link to save power.

The device also features USB 2.0 technology. It provides higher bandwidth and improved protocols for data exchange between the host and the device. In addition, USB 2.0 offers a more aggressive power management feature that enables selective suspend to save energy.

The RTL8152B/RTL8152BN is suitable for multiple market segments and emerging applications, such as desktop, mobile, workstation, server, communications platforms, and embedded applications.

2. Design and Layout Guide

System designers should follow basic rules in layout and placement, general termination, power supply filtering, plane partitioning, and EMI reduction in order to optimize designs that use the RTL8152B/RTL8152BN. Following these rules will greatly contribute to a properly functioning hardware system.

This guide has the following goals:

(1) Create a low-noise, power-stable environment.

(2) Reduce the degree of EMI/EMC and their influence on the RTL8152B/RTL8152BN.

(3) Simplify the task of routing signal traces.

2.1. General Guidelines

In order to achieve maximum performance using the RTL8152B/RTL8152BN, good design practices are required throughout the process. The following are some recommendations for implementing a high-performance system.

- Provide a good power source, minimizing noise from switching power supply circuits (<100mV peak-to-peak)
- Keep power and ground noise levels below 100mV peak-to-peak
- Use bulk capacitors (4.7µF~10µF) between the power and ground planes
- Use 0.1µF de-coupling capacitors to reduce high-frequency noise on the power and ground planes
- Keep de-coupling capacitors close to the RTL8152B/RTL8152BN (within 200 mils)
- Provide termination on all high-speed switching signals
- Use a smaller package for the capacitor to reduce the package inductance
- Verify that critical components such as the clock source and transformer meet application requirements

Use the following signal integrity techniques to reduce crosstalk:

- Shorter parallel routes
- Proper termination
- Provide a solid ground plane

2.2. Differential Signal Layout Guidelines

- Keep differential pairs as close as possible and route both traces as identically as possible, meaning width, length, and location
- Avoid vias and layer changes if possible
- Keep transmit and receive pairs away from each other. Run orthogonally, or separate by a ground plane if possible
- 0.1µF common mode noise filter capacitors should be placed near the RTL8152B/RTL8152BN chip
- Ninety-degree trace angles should be avoided. We recommend that the traces turn at 45° angles as shown in Figure 1. Sharp edges may add unexpected parasitic effects into the circuitry. Reducing the trace length will reduce trace inductance during quick energy bursts

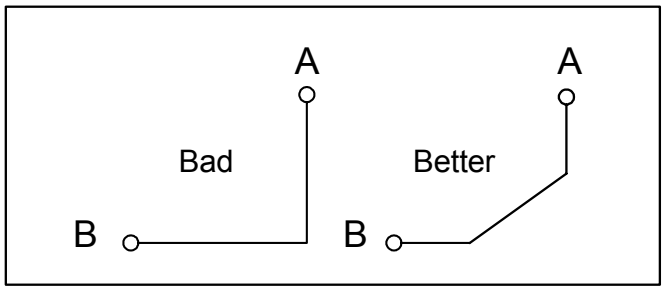

Figure 1. Signal Trace Angles

2.3. Placement

- The RTL8152B/RTL8152BN should be placed as close as possible to the magnetics (less than 12cm)

2.4. Magnetics

- The 10/100M magnetics should be placed as close as possible to the RJ-45 connector
- The magnetics device, or devices with magnetic fields, should be separated and mounted at 90 degrees to each other

2.5. Crystal/Oscillator

- The crystal should be placed away from I/O ports, important or high frequency signal traces (TX, RX, power), magnetics, and board edges
- The outer shield of the crystal requires good grounding to avoid induction of EMC/EMI
- The retaining straps of the oscillator, if any, need good grounding

2.6. Ferrite Beads and De-Coupling Capacitors

Each PCB design has its unique noise coupling behavior. Ferrite beads are used to suppress power noise. System designers are suggested to provide the option to replace the ferrite beads with 0Ω resistors. Decoupling capacitors should be placed as close as possible to the power pins, such that the distance from the IC power pin to the capacitor is less than 200 mils.

3. Signal and Trace Routing

Noise, ringing, and data lines should be controlled with proper termination. Power supply pins should be protected by proper filtering techniques. Good routing of traces can reduce propagation delay, crosstalk, and high frequency noise. It will also improve the signal quality to the receiver and reduce transmit signal losses.

- Ninety-degree trace corners should be avoided. We recommend that the traces turn at 45° angles as shown in Figure 1, page 4. Sharp edges may add unexpected parasitic effects into the circuitry. Reducing the trace length will reduce trace inductance during quick energy bursts
- The trace length and the ratio of trace width to trace height above the ground planes should be carefully considered. If running power on the trace is unavoidable, the trace width should be wider than 60 mils, and properly filtered to minimize power noise effects. The clock and other high-speed signal traces should be as short and wide as possible (compared to normal digital traces). It is better to have a ground plane under these traces. If possible, use a ground plane to surround them
- It is important to separate Digital Signals (e.g., Serial EEPROM) from Analog Signals (e.g., MDI0+/-, MDI1+/-, RSET) in order to avoid interference. If it is unavoidable to cross digital signals with analog power, do it at 90° angles

3.1. Power Trace

- The power into the RTL8152B/RTL8152BN digital power pins can be improved with de-coupling capacitors. Keep de-coupling capacitors as close as possible to the RTL8152B/RTL8152BN (within 200 mils), and keep the traces short. The vias of the de-coupling capacitor should be sufficiently large enough in diameter. All analog power pins on the RTL8152B/RTL8152BN need to be de-coupled with a capacitor
- The power signal traces (de-coupling cap traces, power traces, grounding traces) should be as short and wide as possible
- The vias of the de-coupling capacitor should be large enough in diameter
- 5V power trace width: 30 mils (minimum)
- 3.3V power trace width: 30 mils (minimum)
- 1.05V power trace width: 40 mils (minimum)
- RSET trace width is 10 mils (minimum) and is recommended to be isolated with a guard ground

3.2. MDI Signal Trace

- Traces routed from the RTL8152B/RTL8152BN to the 10/100M magnetics, and to the RJ-45 connector, should be as short as possible. The 12cm maximum length between the RTL8152B/RTL8152BN and magnetics is achievable only when there is no interference. It is also very important to keep differential pair signal traces (MDI0+/-, MDI1+/-) equal in length
- The two traces of each pair should be placed close to each other (D1) as they are differential pair signals to each other and provide a strong cancelling effect on noise. The width of D1 should be calculated to have 100ohm impedance (Figure 2). MDI impedance is 50ohm common mode, 100ohm differential mode
- There should be more than 30 mils spacing between different differential pairs to minimize cross-talk coupled from other pairs (D2 in Figure 2). In addition, Ground Plane shielding can be used to separate all two-signal pairs. However, a good layout should avoid the following situations:
  - Intersection of any two pairs of signal traces
  - Intersection of the two signal traces of the same differential pair
- To minimize impedance mismatch, do not to use vias on the differential pairs

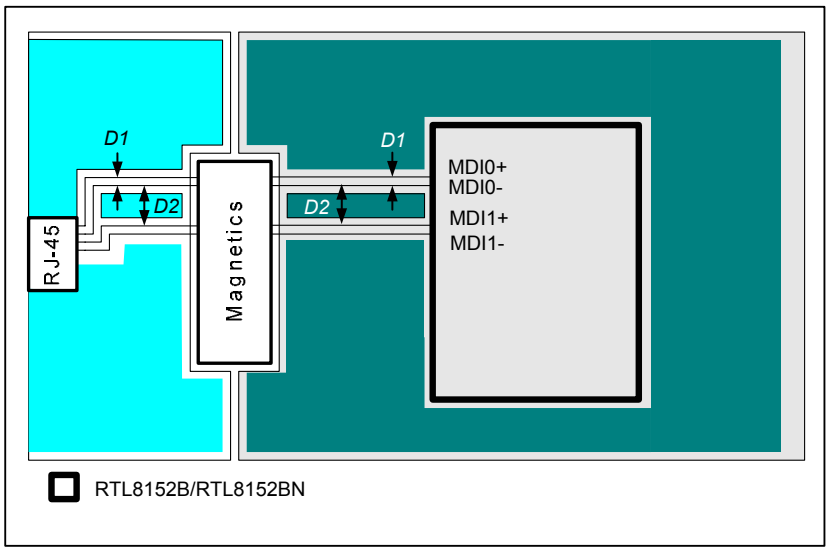

Figure 2. MDI Signal

3.3. USB Signal Trace

- The USB interface differential pair signal is U2DP/U2DM
- Differential characteristic impedance of USB signal trace is 90Ω±10% (see Figure 3, page 9)
- Differential pairs should maintain lateral routing symmetry between the two signals of a differential pair if possible
- Differential pair signals should avoid discontinuities in reference plane, such as splits and other voids
- We recommend to use a guard ground to isolate each differential pair of USB interface signals
- Maintain at least 20 mils air gap to the edge of the reference plane (guard ground) when the traces run parallel to the plane edge (see Figure 4, page 9)
- Avoid via and layer changes if possible
- Via usage per trace: No more than 2 vias is recommended
- Via size: Pad ≤ 24 mils, Finished hole ≤ 12 mils

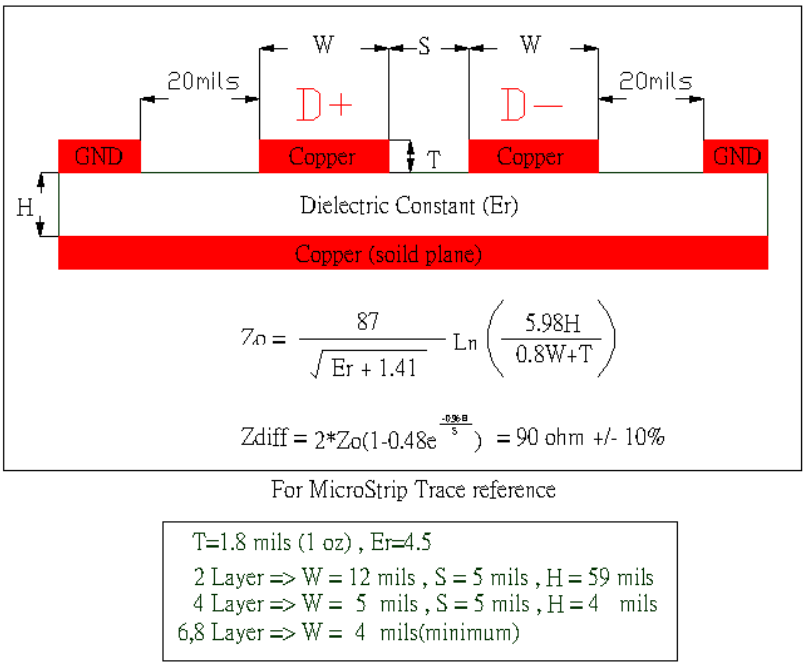

Figure 3. USB Differential Characteristic Impedance (Zdiff)

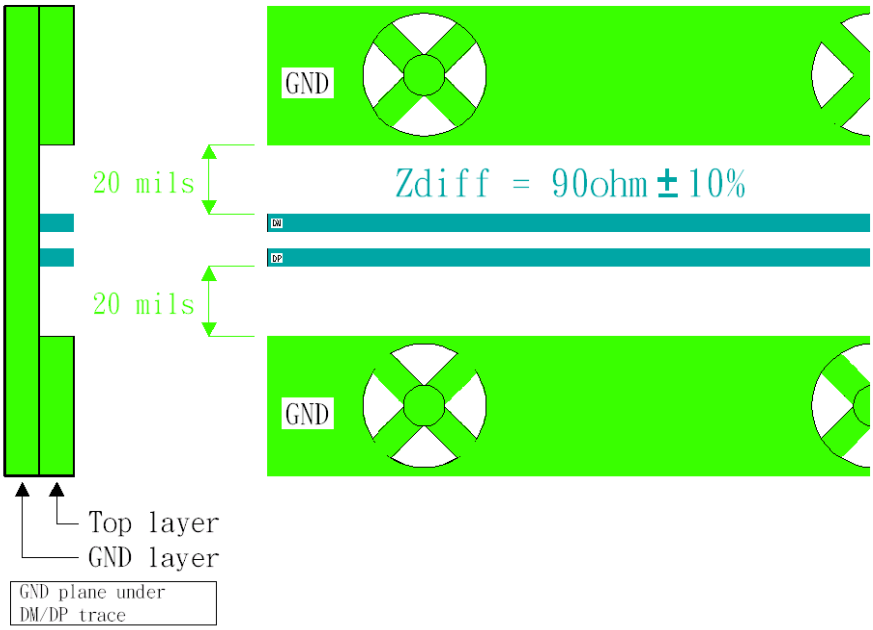

Figure 4. USB Differential Pairs

4. Ground and Power Plane Layout

4.1. Ground Plane Layout

There is only one ground plane for analog power (VDD5, AVDD33, AVDD10) and digital power (DVDD33, DVDD10, DVDD10_UPS). In the center of the IC, there is an Exposed Pad (EPAD) ground.

- RTL8152B: The size of the center EPAD ground is 2.7mm x 2.7mm. The PCB layout requires 4 vias to connect the EPAD to the lower layer ground plane (see Figure 5)
- RTL8152BN: The size of the center EPAD ground is 4.4mm x 4.4mm. The PCB layout requires 9 vias to connect the EPAD to the lower layer ground plane (see Figure 6)

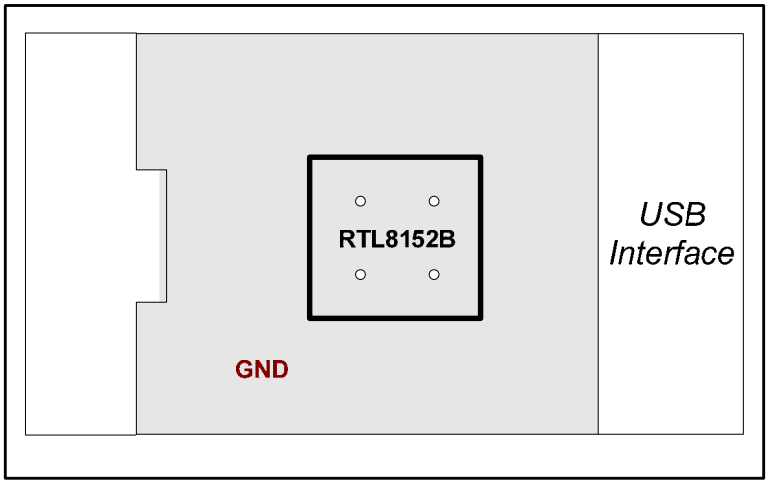

Figure 5. Ground Plane Layout-1 (RTL8152B)

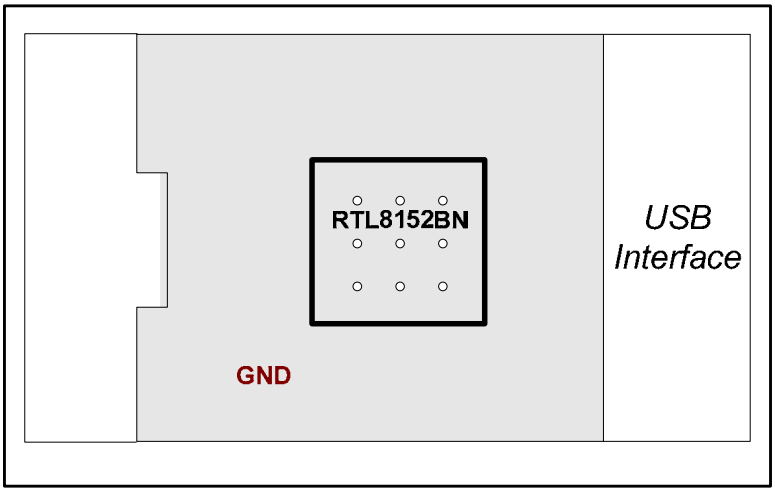

Figure 6. Ground Plane Layout-1 (RTL8152BN)

Isolated separation between Analog and Digital Ground domains is not recommended since bad ground plane partitioning could cause serious EMI emissions and degrade analog performance due to bouncing noise.

Whether there is sufficient space on the PCB for an isolated separation layout must also be taken into consideration. The key point of such a layout is to keep the analog GND return path approximately equal to the common GND. If the system designer is not comfortable doing this, just place a single ground plane with no partition.

To achieve better ground plane performance, we recommend to keep the plane as large and uniform as possible. Figure 7 illustrates a not so good (left) and a good ground plane layout (right).

Figure 7. Ground Plane Layout-2

The plane area beneath the magnetics should be left void. The void area is to keep transformer-induced noise away from the power and system ground planes (Figure 8).

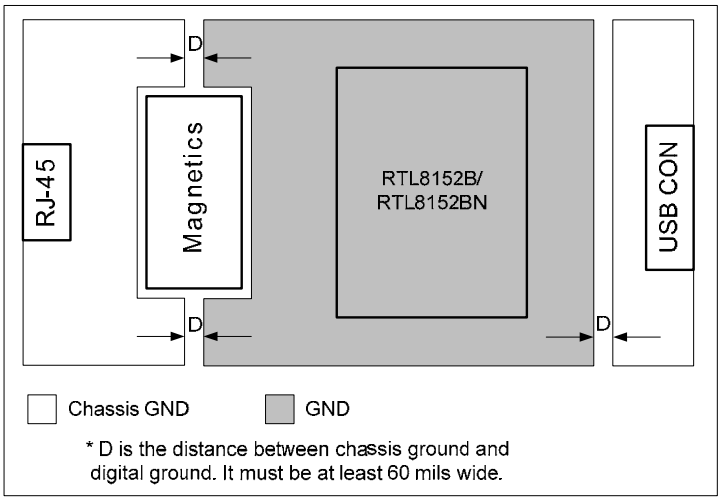

Figure 8. Ground Plane Separation

The Chassis Ground as shown in Figure 8 is known as an 'Isolated Ground'. It connects directly to the RJ-45 connector (fully shielded is recommended). In addition, 75ohm termination resistors and a 1000pF/2kV (3kV recommended) high voltage capability capacitor between the magnetics RJ-45 jack side and the Chassis GND is needed for EMI and ESD protection.

It is important to keep the gap (D in Figure 8) between Chassis GND and System GND wider than 60 mils for better isolation.

4.2. Power Plane Layout

The digital power plane should be separated from analog areas, which are extremely sensitive to noise. It is recommended to use at least a 4-layer PCB.

A low-pass filter combination of a ferrite bead and capacitors should be used to provide a clean, filtered power plane for analog consideration. It is important to avoid using unnecessary power traces to the RTL8152B/RTL8152BN. If it is unavoidable, try to keep these traces as short and wide as possible and make good use of vias.

(a) Decoupled Capacitor Example

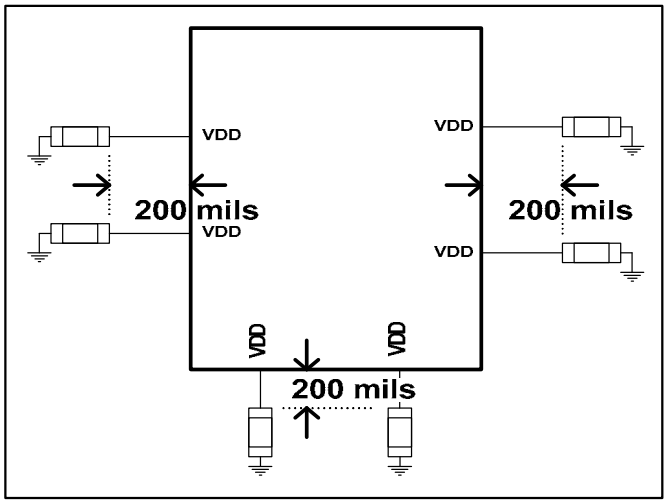

Figure 9. Decoupled Capacitor Example

(b) Use a Ferrite Bead or 0 ohm Resistor to connect Digital and Analog Power

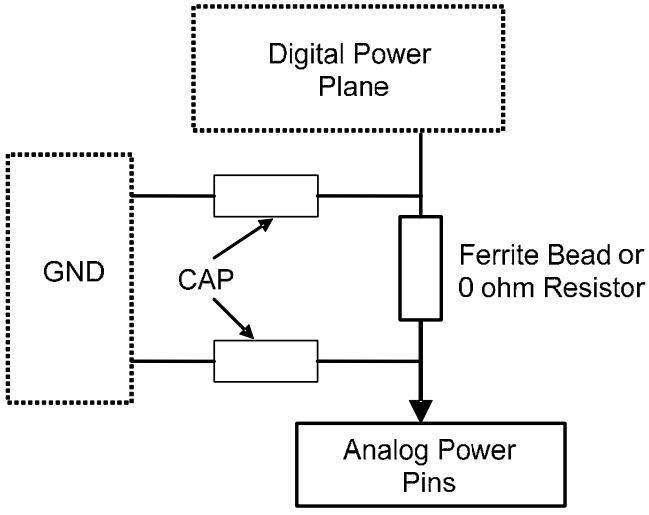

Figure 10. Power Plane

To further improve the performance of the power plane, try to keep the contact area between the RTL8152B/RTL8152BN VDD pins and power plane as large as possible rather than using small narrow traces (Figure 11).

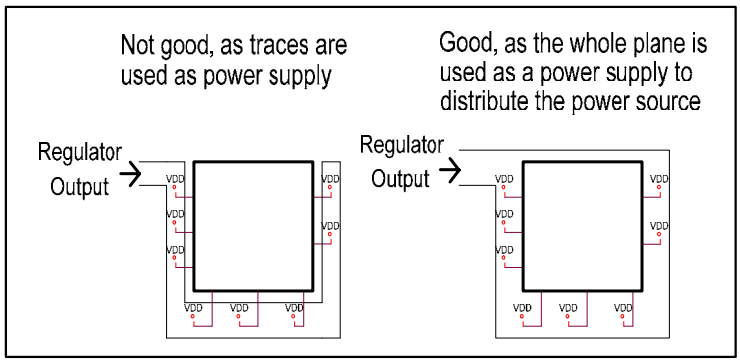

Figure 11. Power Source Distribution

- Keep power noise levels below 100mV peak-to-peak in 100M mode
- All 3.3V/1.05V decoupling capacitors shown in the reference schematic should be used in all designs
- Keep the analog power (1.05V) plane as whole and as large as possible

4.3. Four-Layer Board Plane Layout

1. Signal 1 (top layer)

2. GND

3. Power

4. Signal 2 (bottom layer)

5. Center-Tapping

- A center-tapped fine-tuned capacitor (C1 Value: 0.01µF~0.4µF) can improve EMI for single tone noise. The capacitor default is 0.01µF
- Changing the R resistor to a capacitor (Value: 0.01µF~0.4µF), and fine-tuning the connection to GND can improve EMI for single tone noise. The resistor default is 0 ohm

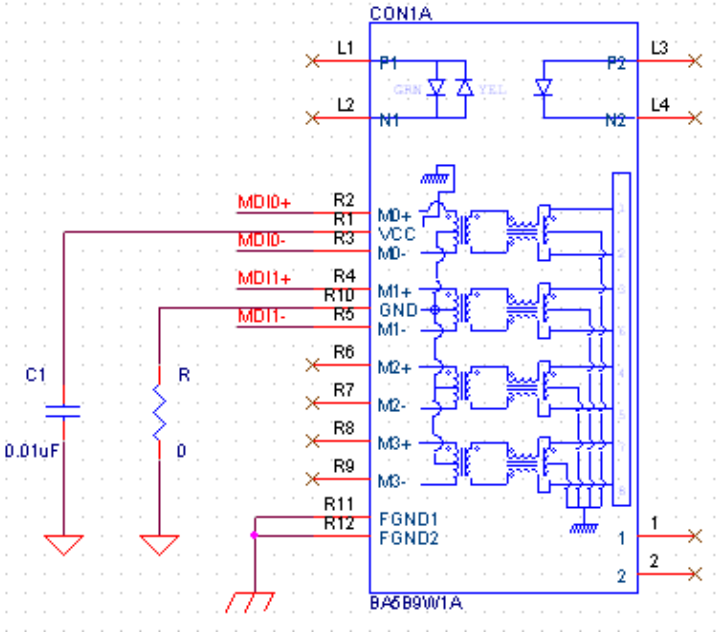

Figure 12. Center-Tapping

- When using a separate transformer, all center-tap pins MUST be aggregated (pins 7, 10; Figure 13) (C1 Value: 0.01µF~0.4µF)

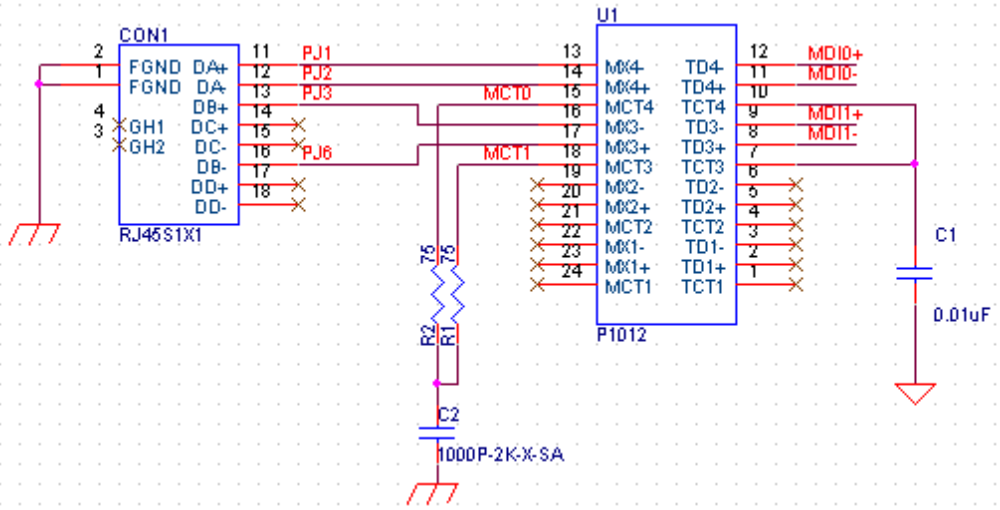

Figure 13. Separate Transformer

6. Parts Recommendations

6.1. 10/100M Magnetics

Turn Ratio TX/RX: 1:1

Primary Inductance: 350µH OCL with 8mA bias

Insertion Loss: -1.0 dB Max, 1 ~ 100MHz

Return Loss: -18dB Min @ 100Ω, 1 ~ 30MHz

-14dB Min @ 100Ω, 30 ~ 60MHz

-12dB Min @ 100Ω, 60 ~ 80MHz

Differential to Common Mode Rejection:

-40dB Min @ 1 ~ 60MHz

-30dB Min @ 60 ~ 100MHz

Hi-Pot: 1500Vrms @ 60sec

Operating Temperature: 0°C to 70°C

Recommended Magnetics: Delta LFE8423 or similar

6.2. Reference Clock

A 25MHz (within 50ppm) parallel resonant crystal can be used as the reference clock source to replace the 25MHz Oscillator. The crystal must be connected to CKXTAL1 and CKXTAL2 pins. Shunt each crystal lead to ground with a 27pF capacitor.

Parameters	Range
Frequency	25MHz
Temperature Stability	±30ppm
Duty Cycle	50%±10%
Tolerance	±50ppm
ESR	Max 30Ω
Broadband Peak-to-Peak Jitter*	MAX 200ps
Aging	5ppm/year, max.

Note: Broadband RMS=9ps; 25KHz to 25MHz RMS=3ps.

6.3. Resistors

Resistors that have tolerance requirements within 1% are strongly recommended. Refer to the provided BOM for suggested schematics.

6.4. Ferrite Bead

The ferrite bead used should be of at least 100Ω@100MHz impedance with a rated current of 300mA or higher.

6.5. RJ-45 Jack

A fully shielded RJ-45 connector should be used.

7. Surge Protection

In order to provide adequate surge protection for the RTL8152B/RTL8152BN, proper PCB design is required. The following are some recommendations for better surge protection of line-to-ground mode defined in the IEC-61000-4-5 specification.

7.1. General Guidelines

- There should be more than 30 mils spacing between different differential pairs of MDI signals. In addition, MDI signal trace routing between the magnetics and the RJ-45 connector should have clearance constraint from other traces with a minimum of 100 mils spacing
- Keep 75ohm termination resistors and high voltage capability capacitors away from other component pads (min 50 mils)
- For 75ohm termination resistors we recommend to use 0603 or larger resistors, with a maximum overload voltage specification of at least 100V
- Trace routing from the magnetics RJ-45 jack side through 75ohm termination resistors and a high voltage capability capacitor to the Chassis GND should be as wide as possible to make sure the whole discharge path is wide enough
    - The trace width should be more than 40 mils
    - Use at least 3 solder-filled blind vias (diameter ≥ 30 mils; drill size ≥ 20 mils) or a solder-filled through hole (diameter ≥ 60 mils; drill size ≥ 35 mils) if a layer change is needed

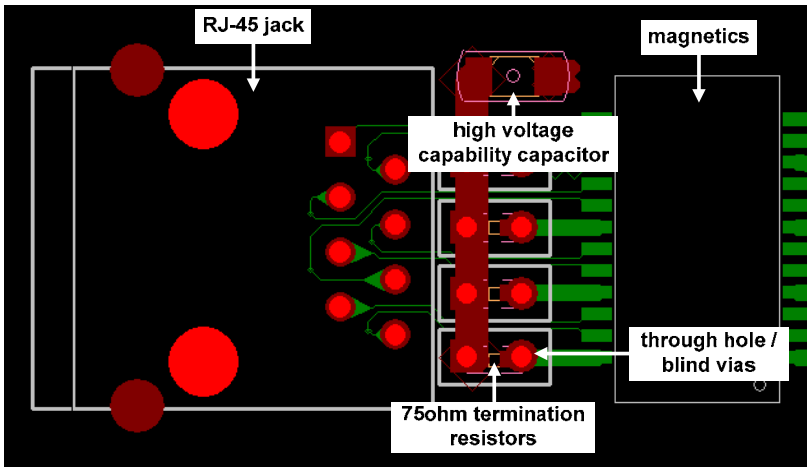

Figure 14. Trace Routing of the Magnetics RJ-45 Jack Side

- The power signal traces (power traces, ground traces) should be as short and wide as possible
- The plane area of Chassis GND should be as large as possible. We recommend to have mounting screw holes on the board that connects the Chassis GND to the chassis
- The magnetics should be placed at least 1500 mils away from the RJ-45 jack

7.2. Special Layout Technique

A low-cost PCB design technique for surge protection of line-to-ground mode developed by Realtek is the spark gap (Patent Pending), which can be implemented as a part of the component pattern of a PCB. The spark gap can produce spark discharge in a short gap and provide overvoltage protection from a surge event such as that produced by lightning transients.

- We suggest two spark gap pads that have half circles with a radius of 20 mils, and with a gap between each of 8 mils. The pads must not be covered with solder mask (copper exposure) and the gap area must be open to the air. The spark gap design is shown in Figure 15

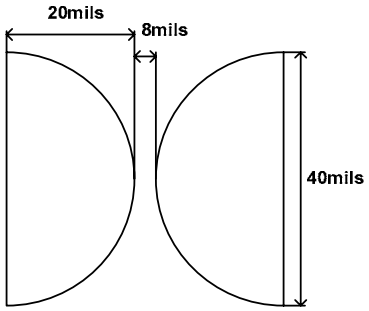

Figure 15. Spark Gap Design

- We recommend to place all spark gaps, 75ohm termination resistors, and a high voltage capability capacitor on the opposite side of the magnetics in the clear area, and keep these away from other component pads (min. of 150 mils)
- The spark gap should be located between the source of the discharge path, e.g., the center tap of RJ-45 jack side of the magnetics, and the Chassis GND. The purpose is to generate a second discharge path and help to dissipate very high amplitude and fast rising surge voltage

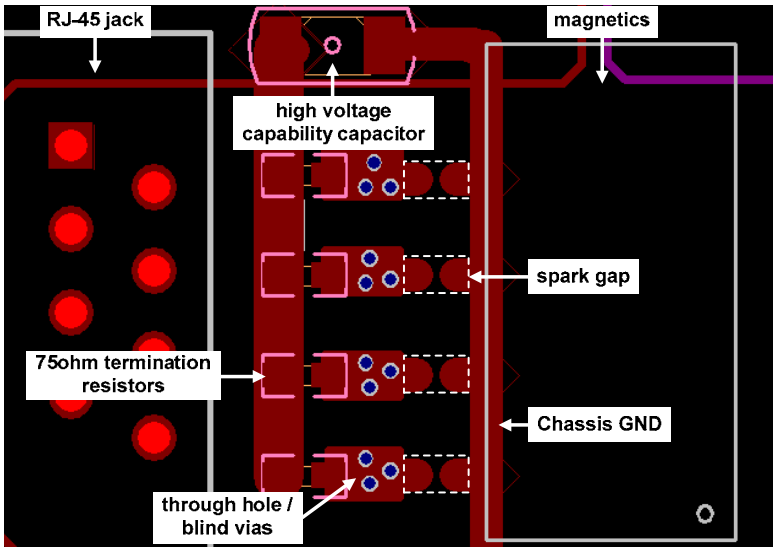

Figure 16. Spark Gap Layout

8. Special Notes

The analog GND pins must maintain a good ground return path. To do this, avoid using single-ended grounds, enlarge the analog GND plane, and try to keep the analog circuit return back to the real GND as short as possible. This is particularly important for 10/100M Ethernet applications.

- When using the oscillator as the clock source for 25MHz/48MHz, avoid connecting any capacitors to the clock circuitry
- Keep a void area of at least 100 mils from the edge of each layer (e.g., power plane, GND plane, etc.) to the PCB edge in order to minimize fringe effect and lower EMI emissions
- The RTL8152B/RTL8152BN incorporates a linear regulator (LDO). Note that the embedded LDO is designed for RTL8152B/RTL8152BN internal use only. Do not provide this power source to other devices

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