Roll Number: _____ Name _____ Group _____

THAPAR INSTITUTE OF ENGINEERING &TECHNOLOGY, PATIALA

Department of Computer Science & Engineering

Operating System (UCS303) – End Semester Examination

Date: 08/12/2023 & Time: 02:00PM ***MM: 100 & WT: 35 & MT: 180 Min***

Attempt/Answer any five COMPLETE questions and all sub-parts like (a), (b), (c) for each question at one place. Do mention Page No. of your attempt at front page of the answer sheet. *Assume missing data (if any). Show all intermediate computations properly.*

Q1. (a). Consider a system with processor uses 2–level page tables for virtual to physical address translation. Page tables for both levels are stored in the main memory. Virtual and physical addresses are both 32 bits wide. The memory is byte addressable. For virtual to physical address translation, the 10 most significant bits of the virtual address are used as index into the first level page table while the next 12 bits are used as index into the second level page table. The 10 least significant bits of the virtual address are used as offset within the page. Assume that the page table entries in both levels of page tables are 4 bytes wide. Show intermediate calculations to answer the following questions:

(i) Illustrate the translation of logical to physical address in 2–level paging with the help of a diagram. [5]

(ii) Compute the size of logical address space (LAS), physical address space (PAS), inner and outer page table size, and number of bits to represent frame number. [5]

(iii) Further, the processor has a translation look-aside buffer (TLB) to improve page table access time, with a hit rate of 90%. The TLB stores recently used virtual page numbers and the corresponding frame numbers. So if there is a hit in TLB, then the processor avoids page table access as frame numbers are available in TLB. The processor also has a physically addressed cache to improve main memory access time with a hit rate of 96%. The physically addressed cache has a copy of the corresponding frames in the main memory. So if there is a hit in the physically addressed cache, then the processor avoids main memory access as frames are available in the physically addressed cache. The main memory access time is 100 ns, cache access time is 10 ns, and TLB access time is also 5 ns. Assuming that no page faults occur, calculate the average memory access time taken to access data at a given virtual address. [5]

(b). With a suitable diagram explain the RAID 0+1 and RAID 1+0 structure. [5]

Q2. (a). Explain any five categories of viruses related to Operating systems. [5]

(b). Explain any three free-space management techniques under disk management. [5]

(c). Consider a system with fixed partitioning scheme and 4 partitions of sizes 4KB, 28KB, 16KB, and 32KB. Best fit memory allocation strategy is utilised to allocate jobs on different partitions. Assuming that we have same number of processors as the number of partitions to allow parallel processing, i.e., four process can execute simultaneously. Compute completion time of all the jobs using GANTT chart for following jobs. [10]

Job	J1	J2	J3	J4	J5	J6	J7
Memory Size	2K	14K	3K	16K	10K	25K	3K
Arrival Time	0	0	1	1	2	2	3
Burst Time	2	6	3	7	4	8	5

Q3. (a). With a suitable diagram explain thrashing and its causes? Also, explain two thrashing solutions working set model and page fault frequency with suitable diagram. [10]

(b). Consider a system with five processes that use the Priority scheduling (preemptive). The Priority algorithm schedules a new process either when the running process gets blocked on I/O, a new higher priority process arrives, or when the running process finishes its CPU burst. Assume that all I/O operations can be overlapped as much as possible, and the process first [10]

spends CPU time, followed by I/O time, and followed by CPU time again. Assume higher number indicate higher priority. The processes have different arrival and burst times, given as follows. With the help of GANTT chart, compute average waiting time of the system?

Process ID	Arrival Time	Burst Time			Priority
		CPU	I/O	CPU	
P1	0	3	4	1	8
P2	0	2	3	2	6
P3	1	1	3	3	7
P4	1	4	4	4	9
P5	6	2	2	2	4

Q4. (a). Consider a system with 3 frames allocated to a process in the main memory. The process having the page references 6, 7, 8, 9, 6, 7, 1, 6, 7, 8, 9, 1 to complete its execution. With the help of a suitable diagram (showing step-by-step execution) compute the page faults that will occur using First in First Out (FIFO), Most Frequently Used (MFU), Least Recently Used (LRU), and Optimal Page Replacement (OPR) algorithms. In case of multiple choices for page replacement, the FIFO algorithm will be used to resolve conflict. [10]

(b). Explain the Readers-Writers Problem along with its constraints and conditions. Also, write the deadlock-free solution (pseudo code) for the said problem using semaphores. [10]

Q5. (a). Consider a disk storage system with 200 cylinders numbered as 0, 1, …, 199. Cylinder number 0 starts from centre and move in an incremental fashion towards the circumference. The disk requests with following cylinder number are received by the disk controller: 55, 58, 39, 18, 90, 160, 150, 38, 184. Compute the Total Head movements and the Number of times Head changes its direction, when the following algorithms have been deployed. Currently head is positioned at cylinder 100. The initial direction of movement is towards higher cylinder numbers for SCAN and C-SCAN. Show suitable diagrams and intermediate computational steps for each case. [10]

(i) FCFS (ii) SSTF (iii) SCAN (iv) C-SCAN

(b). Consider the given code segment to analyse the three critical section conditions: mutual exclusion, bounded waiting, and progress. Pre-emption can occur while executing the given code. Assume, initial lock value is zero (lock==0) and all instructions are atomic. Show that if above mentioned synchronization conditions are satisfied or not with proper explanation. [10]

1. Load Ri, M[lock]
2. CMP Ri, 0
3. JNZ Step 1
4. Store M[lock], 1
5. CRITICAL SECTION
6. Store M[lock], 0

Where, CMP and JNZ denotes comparision and jump at non-zero intructions.

Q6. (a). Consider a disk which has 16 platters, and every platters has 2 surfaces, every surface is having 1K tracks. Each track of the disk has 1024 sectors and each of size 512 Bytes. Assume that disk has an average seek time of 60ns and rotational rate of 720RPM. Show intermediate calculations to answer the following questions: [10]

(i) What is the capacity of the disk?
(ii) What is the time taken to read 8 consecutive sectors of a track?
(iii) What is the data transfer rate of the disk?

(b). In a computer system, four files of size 11050 bytes, 4990 bytes, 5170 bytes, and 12640 bytes need to be stored. For storing these files on disk, we are using 100 byte disk blocks. For each block used to store a file, 4 bytes of bookkeeping information also needs to be stored on the disk. Consequently, the total space used to store a file is the sum of the space taken to store the file and the space taken to store the bookkeeping information for the blocks allocated for storing the file. A disk block can store either bookkeeping information for a file or data from a file, but not both. Assume that no two process and their bookkepping information stored in same block. What is the total space and total number of blocks required for storing the above mentioned files using 100 byte disk blocks? [10]