Roll Number:_____

Thapar Institute of Engineering & Technology
Department of Computer Science and Engineering
END SEMESTER EXAMINATION

B. E. **(2nd Yr. COE / CSE)**
15th December, 2022
Thursday, Time– 4:30 To 7:30 PM
Time: 3 Hours, Max Marks: 100 (weightage 35)

Course Code: UCS303
Course Name: Operating Systems
Name of Faculty: Vinay Arora, Tarunpreet Bhatia, Sachin Kansal, Shahsank Sheshar, Tanu Goyal

Attempt all Questions in sequence. Attempt/Answer all sub-parts of each question at one place. Assume missing data (if any). Show all the intermediate computations properly.

Q.1 Consider a disk storage system with 200 cylinders numbered as 0, 1, …, 199. Cylinder number 0 starts from centre and move in an incremental fashion towards circumference. The disk requests with following cylinder number are received by the disk controller: (20)

72, 134, 20, 86, 116, 16

Compute the Total Head movements and Number of times Head changes its direction, when following algorithms have been deployed. Currently head is positioned at cylinder 80. Initial direction of movement is towards higher cylinder numbers for C-LOOK and C-SCAN. Show suitable diagrams and intermediate computational steps for each case.

i. FCFS
ii. SSTF
iii. C-LOOK
iv. C-SCAN

Q.2 (a) Illustrate the translation of logical to physical address in segmentation with the help of a diagram. (5)

(b) Consider a system with single-level paging-based memory management, whose architecture allows for a 4GB virtual/logical address space for processes. The size of each logical page is 4KB. The system has 512MB of physical RAM. Assume valid-invalid bit is also attached to each entry in the page table, and memory is byte addressable. Show intermediate calculations to answer the following questions:

i. When a process starts, the content of page table gets loaded to the CPU registers from RAM (with load speed of 01 byte per 100 nsec). If a process runs for 500 msec (including the time to load the page table), what percentage of the CPU time is involved for loading the page table? (5)

ii. Assume a program of size 20400 bytes that is to be loaded in some of the available free frames numbered {6, 18, 60, 2, 35, 15, 45}. The order for occupying the frames will be 6→18→60→2→35→15→45. Convert the logical addresses 11876 and 17865 to their corresponding physical addresses. All addresses given here are in decimal and your answer should also be in decimal. (Assume that memory addresses start from 0). Also, calculate the external fragmentation in bytes (if any). (10)

Q.3 (a) With a suitable diagrammatic representation explain in detail the Dining Philosopher Problem along with its constraints and conditions. Also, write the deadlock-free solution (pseudocode) for the said problem using semaphores. (10)

(b) With a suitable diagram explain the Access Matrix and various operations (copy, owner, control, switch) that can be applied to it. (5)

(c) With a suitable diagram explain the Indexed allocation of disk space. Also, describe three ways to handle the size of index block. (5)

Q.4 (a) Consider a system with 4 frames allocated to a process in the main memory. The process having the page references 7,0,1,2,0,3,0,4,2,3,0,3,2,1,0,4 to complete its execution. With the help of a suitable diagram (showing step-by-step execution) compute the page faults that will occur using Least Recently Used (LRU) and Optimal Page Replacement (OPR) algorithms. In case of multiple choices for page replacement in OPR, the First in First out (FIFO) algorithm will be used to resolve conflict. Draw a diagram to depict Thrashing in operating systems. (10)

(b) A processor uses single-level paging for virtual to physical address translation. The page table is stored in the main memory. The processor has a translation look-aside buffer (TLB) to improve page table access time, with a hit rate of 96%. The TLB stores recently used virtual page numbers and the corresponding frame numbers. So if there is a hit in TLB, then the processor avoids page table access as frame numbers are available in TLB. The processor also has a physically addressed cache to improve main memory access time with a hit rate of 90%. The physically addressed cache has a copy of the corresponding frames in the main memory. So if there is a hit in the physically addressed cache, then the processor avoids main memory access as frames are available in the physically addressed cache. The main memory access time is 100 ns, the physically addressed cache access time is 10 ns, and the TLB access time is 4ns.

i. Draw the labelled diagram for above mentioned paging scheme. (2)

ii. Assuming that no page faults occur, calculate the average memory access time taken to access data at a given virtual address. (4)

iii. Further, 80% of the page references generate page faults which are identified by using valid/invalid bit in page table. Calculate the average memory access time taken to access data at a given virtual address if time taken to transfer page from disk to RAM is 200 ns. Assume the time taken to update TLB, cache memory, and page table is negligible and sufficient free frames are available in main memory to store the pages. (4)

Q.5 (a) In a scenario of a process execution, there exist 04 processes in a system and table given below is a snapshot for the same. Apply Round Robin (time quanta=2 units) and pre-emptive Shortest Job First/Shortest Remaining Time (SRTF) CPU scheduling algorithms on the scenario given below and compute the waiting time and turnaround time for each process in both the algorithms with the help of GANTT chart. (10)

Arrival Time	Process Name	CPU Burst Time
0	P1	3
1	P2	5
3	P3	1
6	P4	2

(b) With the help of pseudocode, describe in detail the Banker's Algorithm used by Operating System for avoiding the Deadlock condition. (10)