# Xilinx Software Development Kit (SDK) Standalone Library Documentation

## *XilFPGA (v1.1)*

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Chapter 1

# XilFPGA APIs

## Overview

The Xilfpga library provides an interface to the Linux or bare-metal users for configuring the programmable logic (PL) over PCAP from PS. The library is designed for Zynq® UltraScale+™ MPSoC to run on top of Xilinx standalone BSPs. It is tested for A53, R5 and MicroBlaze. In the most common use case, we expect users to run this library on PMU MicroBlaze with PMUFW to serve requests from Linux for bitstream programming. In its current from it supports only full bitstream download. In subsequent releases it will support other features like encrypted and authenticated bitstream loading, partial bitstream loading.

### Xilfpga library Interface modules

Xilfpga library uses the below major components to configure the PL through PS.

**Processor Configuration Access Port (PCAP) -** The processor configuration access port (PCAP) is used to configure the programmable logic (PL) through the PS.

**CSU DMA driver -** The CSU DMA driver is used to transfer the actual Bit stream file for the PS to PL after PCAP initialization.

**Xilsecure_library -** The LibXilSecure library provides APIs to access secure hardware on the Zynq® UltraScale+™ MPSoC devices. This library includes:

- SHA-3 engine hash functions
- AES for symmetric key encryption
- RSA for authentication

**Note**

- The current version of library supports only Zynq® UltraScale+™ MPSoC devices.
- The XilFPGA library is capable of loading only .bin format files into PL. The library will not support the other file formats.
- Xilsecure_library is required only for the below use cases:

- Encrypted bit-stream loading.
- Authenticated bit-stream loading

## Design Summary

Xilfpga library acts as a bridge between the user application and the PL device. It provides the required functionality to the user application for configuring the PL Device with the required bit-stream. The figure below illustrates an implementation where the Xilfpga library needs the CSU DMA driver APIs to transfer the bit-stream from the DDR to the PL region. The Xilfpga library also needs the XilSecure library APIs to support while programming the authenticated and the encrypted bitstream files.

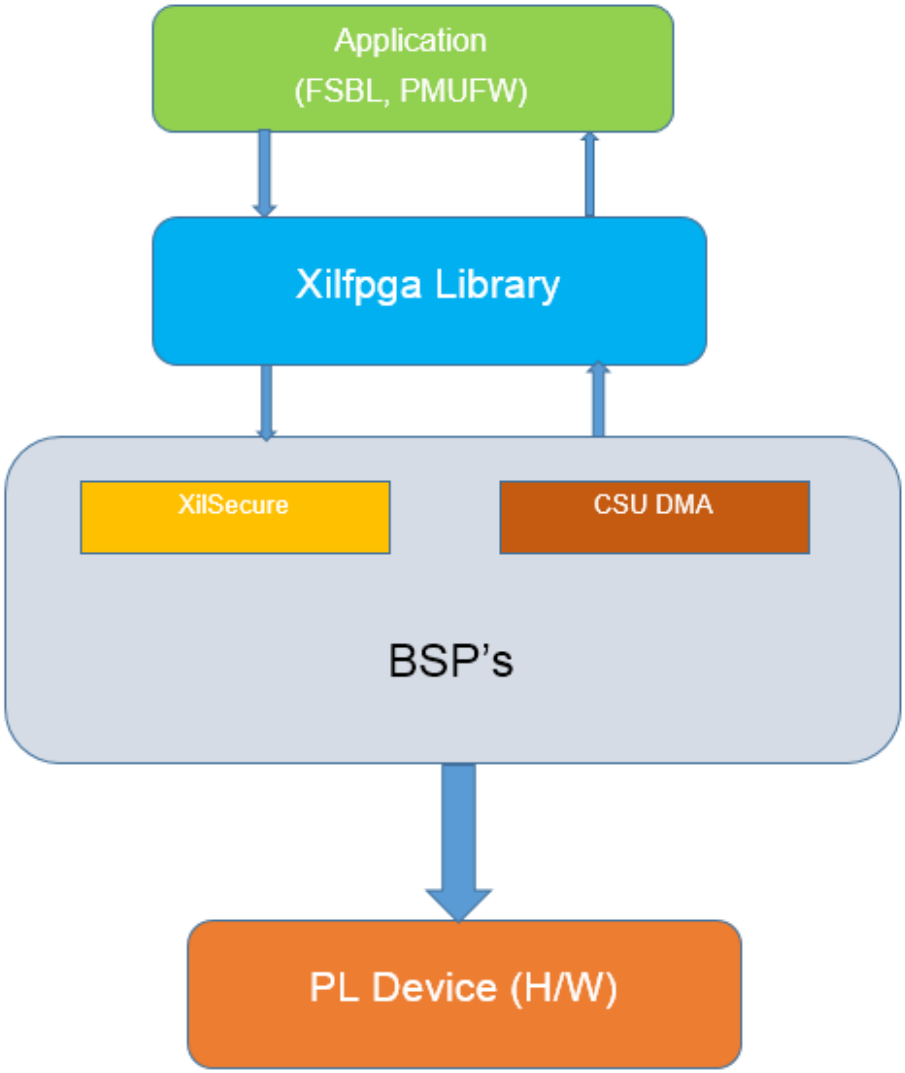


Figure 1.1: XilFPGA Design Summary

## Flow Diagram

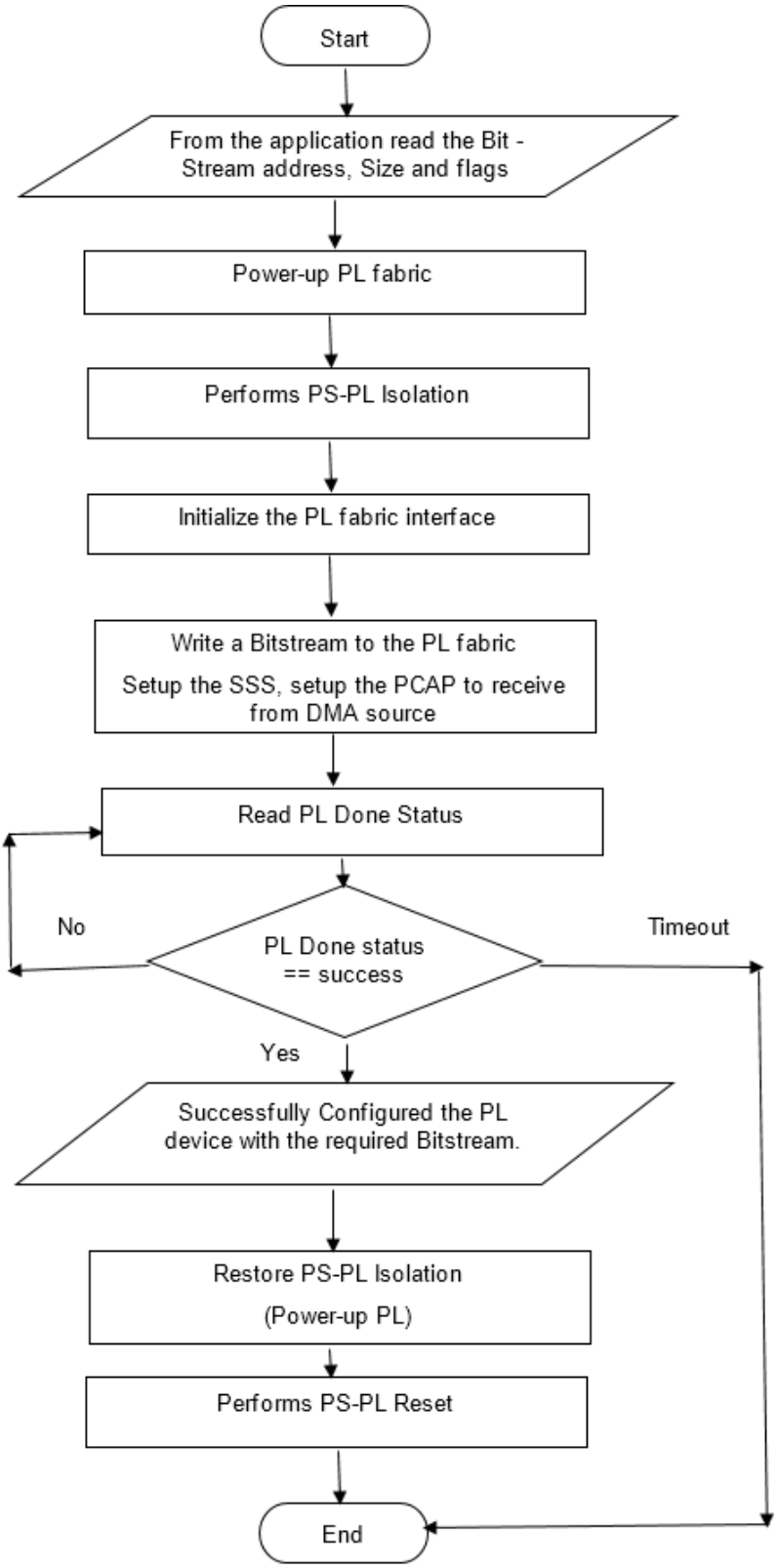


Figure 1.2: XilFPGA Library Workflow

# Setting up the Software System

To use XilFPGA in a software application, you must first compile the XilFPGA library as part of software application.

1. Launch SDK. SDK opens and prompts you to create a workspace.
2. Select **File** > **New** > **Xilinx Board Support Package**. The **New Board Support Package** wizard appears.
3. Specify a project name.
4. Select **Standalone** from the **Board Support Package OS** drop-down list. The **Board Support Package Settings** wizard appears.
5. Select the **xilfpga** library from the list of **Supported Libraries**.
6. Expand the **Overview** tree and select **xilfpga**. The configuration options for xilfpga are listed.
7. Configure the xilfpga by providing the base address of the Bit-stream file (DDR address) and the size (in bytes).
8. Click **OK**. The board support package automatically builds with xilfpga library included in it.
9. Double-click the **system.mss** file to open it in the **Editor** view.
10. Scroll-down and locate the **Libraries** section.
11. Click **Import Examples** adjacent to the xilfpga 1.1 entry.

# Functions

- u32 XFpga_PL_BitSream_Load (u32 WrAddrHigh, u32 WrAddrLow, u32 WrSize, u32 flags)
- u32 XFpga_PcapStatus (void)

# Function Documentation

## u32 XFpga_PL_BitSream_Load ( u32 *WrAddrHigh,* u32 *WrAddrLow,* u32 *WrSize,* u32 *flags* )

The API is used to load the user provided bitstream file into zynqmp PL region. This function does the following jobs:

- Power-up the PL fabric.
- Performs PL-PS Isolation.
- Initialize PCAP Interface
- Write a bitstream into the PL
- Wait for the PL Done Status.
- Restore PS-PL Isolation (Power-up PL fabric).
- Performs the PS-PL reset.

**Note**

This function contains the polling implementation to provide the PL reset wait time due to this polling implementation the function call is blocked till the time out value expires or gets the appropriate status value from the PL Done Status register.

**Parameters**

| | |
|---|---|
| *WrAddrHigh* | Higher 32-bit Linear memory space from where CSUDMA will read the data to be written to PCAP interface |
| *WrAddrLow* | Lower 32-bit Linear memory space from where CSUDMA will read the data to be written to PCAP interface |
| *WrSize* | Number of 32bit words that the DMA should write to the PCAP interface |
| *flags* | Flags are used to specify the type of bitstream file.<br>◦ BIT(0) - Bit-stream type<br>■ 0 - Full Bit-stream<br>■ 1 - Partial Bit-stream<br>◦ BIT(1) - Authentication<br>■ 1 - Enable<br>■ 0 - Disable<br>◦ BIT(2) - Encryption<br>■ 1 - Enable<br>■ 0 - Disable |

**Returns**

- Error status based on implemented functionality (SUCCESS by default).

# u32 XFpga_PcapStatus ( void )

This function provides the STATUS of PCAP interface

### Parameters

| | |
|---|---|
| *None* | |

### Returns

Status of the PCAP interface.

*Appendix A*

# Additional Resources and Legal Notices

## Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see Xilinx Support .

## Solution Centers

See the Xilinx Solution Centers for support on devices, software tools, and intellectual property at all stages of the design cycle. Topics include design assistance, advisories, and troubleshooting tips.

## Please Read: Important Legal Notices

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