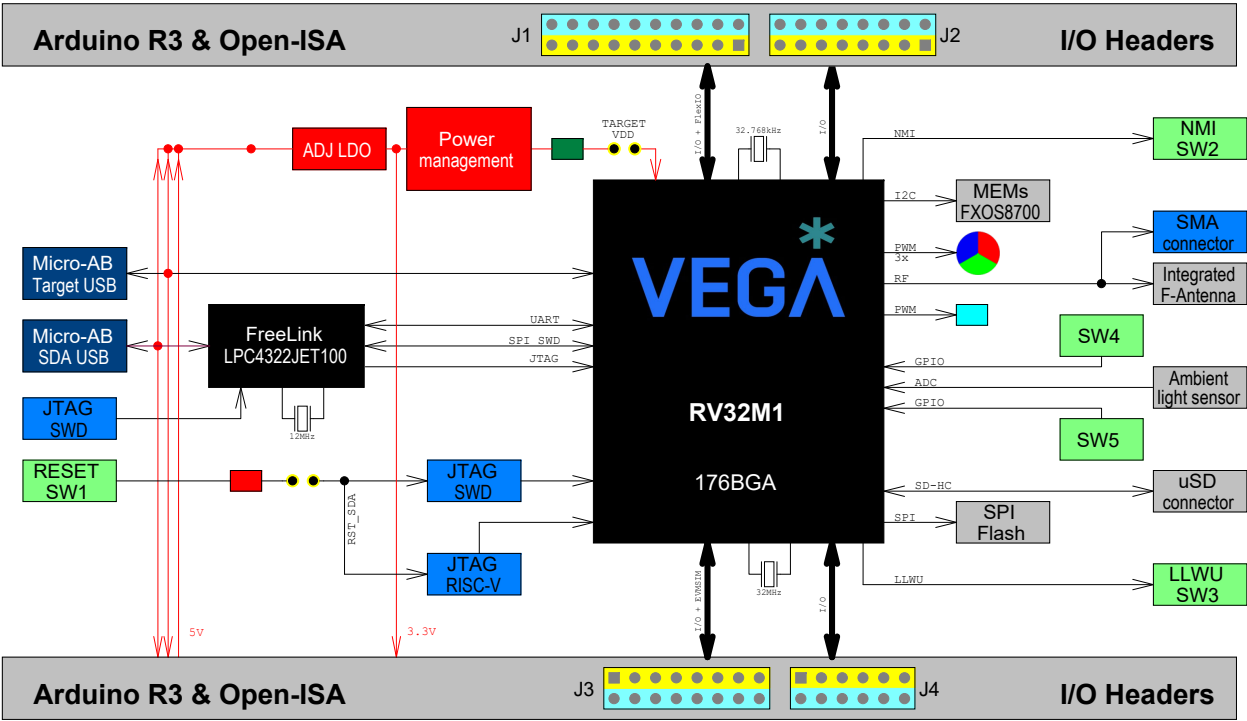


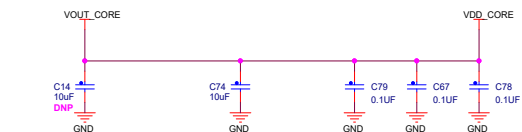
Table of Contents	
BLOCK DIAGRAM	Sheet 2
MCU INTERFACE 1	Sheet 3
MCU INTERFACE 2	Sheet 4
FREELINK INTERFACE	Sheet 5
ARDUINO HEADERS	Sheet 6
POWER MANAGEMENT	Sheet 7

RV32-VEGA-Lite

1. Unless Otherwise Specified:
All resistors are in ohms, 5%
All voltages are DC
All polarized capacitors are aluminum electrolytic
2. Interrupted lines coded with the same letter or letter combinations are electrically connected.
3. Device type number is for reference only. The number varies with the manufacturer.
4. Special signal usage:
_B Denotes - Active-Low Signal
<> or [] Denotes - Vectored Signals
Green text Denotes - Extra Notes to be considered.
5. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.

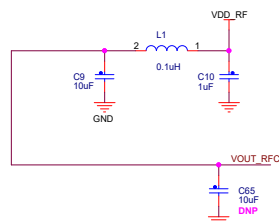
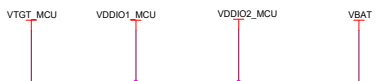


1



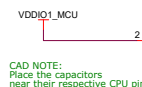
CAD NOTE: Place capacitors close to VOUT_CORE MCU pin

CAD NOTE: Place capacitors close to H9, J8 and N14 pins



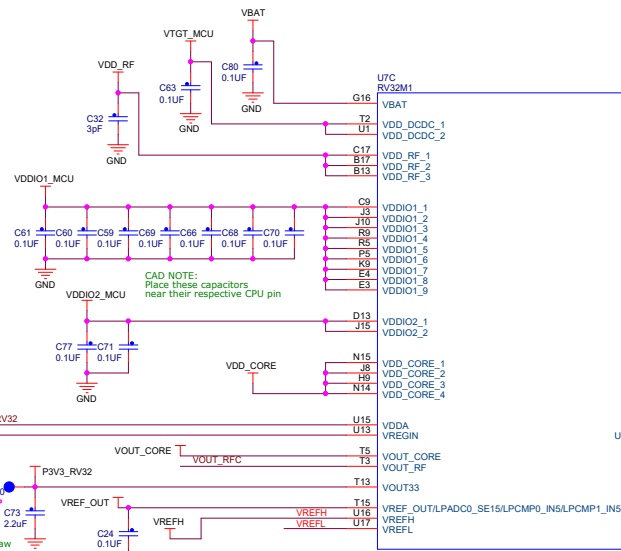
CAD NOTE: Place capacitors close to VDD_RF MCU pin

CAD NOTE: Place capacitors close to VOUT_RFC MCU pin

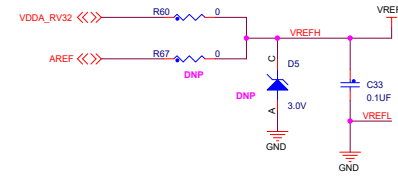


CAD NOTE: Place the capacitors near their respective CPU pin

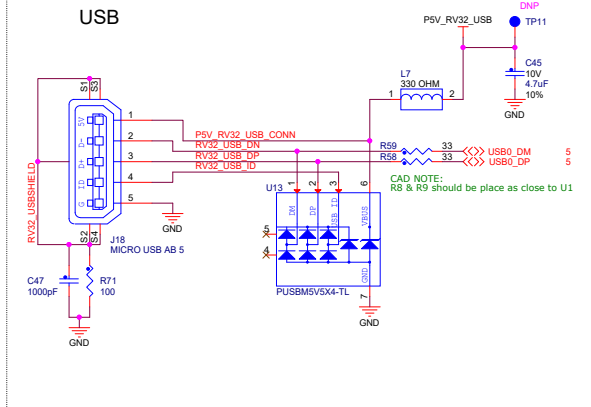
CAD NOTE: Add 20mOhm draw resistor for C4



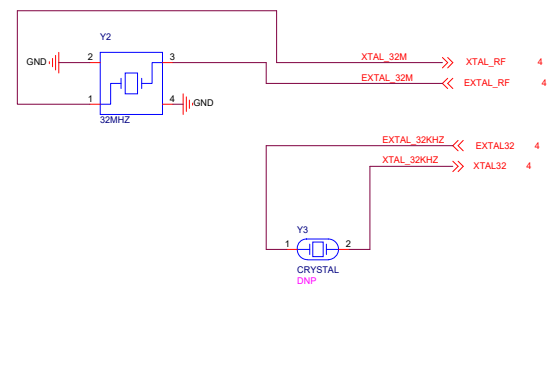
CAD NOTE: Place these capacitors near their respective CPU pin



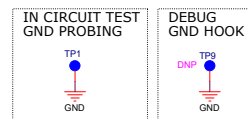
USB



Crystal



custom EMI SHIELD



CAD NOTE: TP12 should be placed on top layer.

ICAP Classification: CP: IUD: PUB: X			
Drawing Title: RV32-VEGA-Lite			
Page Title: MCU_INTERFACE_2			
Size C	Document Number SCH-45731, PDF: SPF-45731	Rev B	
Date: Tuesday, March 19, 2019	Sheet 4 of 7		

Freelink Interface

