LAPIS
SEMICONDUCTOR

ML610401/ML610402/ML610403
User's Manual

<u>NOTES</u>

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Preface

This manual describes the operation of the hardware of the 8-bit microcontroller ML610401/ML610402/ML610403.

The following manuals are also available.　Read them as necessary.

■ nX-U8/100 Core Instruction Manual
Description on the basic architecture and the each instruction of the nX-U8/100 Core.

■ MACU8 Assembler Package User's Manual
Description on the method of operating the relocatable assembler, the linker, the librarian, and the object converter and also on the specifications of the assembler language.

■ CCU8 User's Manual
Description on the method of operating the compiler.

■ CCU8 Programming Guide
Description on the method of programming.

■ CCU8 Language Reference
Description on the language specifications.

■ DTU8 Debugger User's Manual
Description on the method of operating the debugger DTU8.

■ IDEU8 User's Manual
Description on the integrated development environment IDEU8.

Notation

Classification	Notation	Description
♦ Numeric value	xxh, xxH	Indicates a hexadecimal number. x: Any value in the range of 0 to F
	xxb	Indicates a binary number; "b" may be omitted. x: A value 0 or 1
♦ Unit	word, W	1 word = 16 bits
	byte, B	1 byte = 8 bits
	nibble, N	1 nibble = 4 bits
	maga-, M	10^6
	kilo-, K	$2^{10} = 1024$
	kilo-, k	$10^3 = 1000$
	milli-, m	10^{-3}
	micro-, μ	10^{-6}
	nano-, n	10^{-9}
	second, s (lower case)	second
♦ Terminology	"H" level, "1" level	Indicates high voltage signal levels V_{IH} and V_{OH} as specified by the electrical characteristics.
	"L" level, "0" level	Indicates low voltage signal levels V_{IL} and V_{OL} as specified by the electrical characteristics.

♦ Register description

R/W: Indicates that Read/Write attribute. "R" indicates that data can be read and "W" indicates that data can be written. "R/W" indicates that data can be read or written.

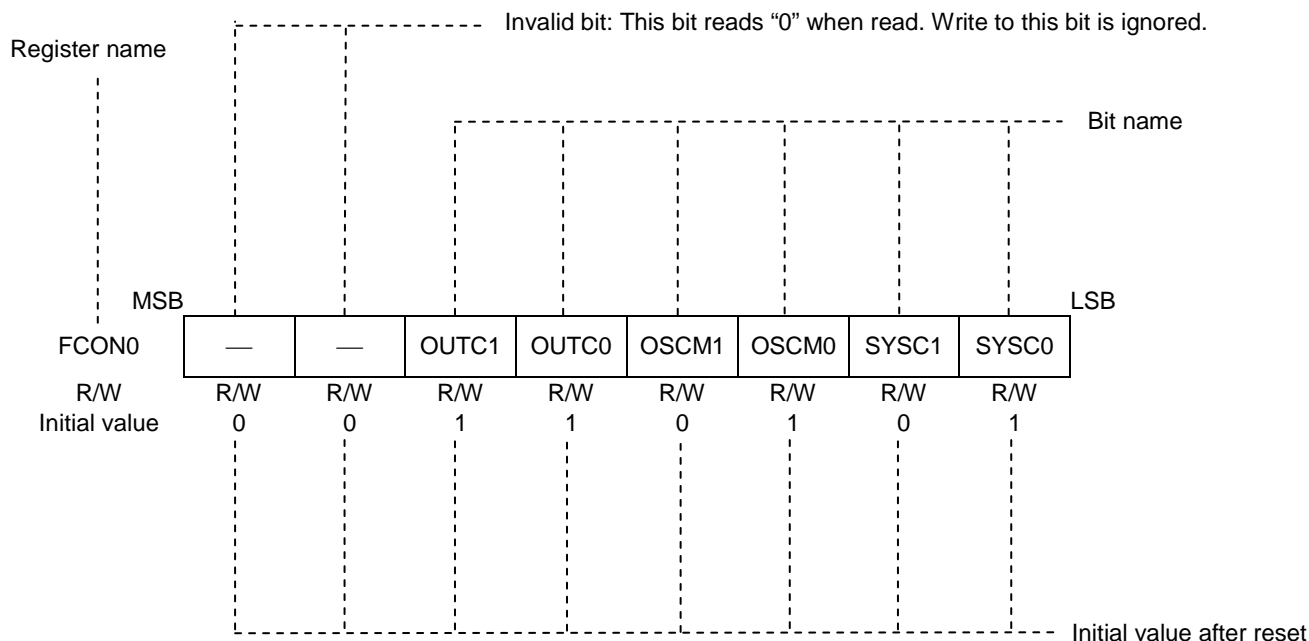# Table of Contents

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Chapter 1

Overview

1. Overview

1.1 Features

This LSI is a high performance CMOS 8-bit microcontroller equipped with an 8-bit CPU nX-U8/100 and integrated with peripheral functions such as UART, melody driver, RC oscillation type A/D converter, and LCD driver.

The CPU nX-U8/100 is capable of efficient instruction execution in 1-intruction 1-clock mode by pipe line architecture parallel processing. Additionally, it adopts the low-/high-speed dual clock system, standby mode, and process that prohibits leak current at high temperatures, and is most suitable for battery-driven applications. For industrial use, ML610401P/ML610402P/ML610403P with the extended operating ambient temperature ranging from -40°C to 85°C are available.

- CPU
  - 8-bit RISC CPU (CPU name: nX-U8/100)
  - Instruction system: 16-bit length instruction
  - Instruction set: Transfer, arithmetic operations, comparison, logic operations, multiplication/division, bit manipulations, bit logic operations, jump, conditional jump, call return stack manipulations, arithmetic shift, and so on
  - Minimum instruction execution time
    - 30.5 μs (at 32.768 kHz system clock)
    - 2 μs (at 500 kHz system clock)

- Internal memory
  - Internal 6KByte mask ROM (3K x 16 bits) (including unusable 256Byte TEST area)
  - Internal 192Byte RAM (192 x 8 bits)

- Interrupt controller
  - 1 non-maskable interrupt source:
    - Internal source: 1 (Watchdog Timer)
  - 17 maskable interrupt sources:
    - Internal source: 9 (Timer 2, Timer 3, UART0, Melody 0, RC Oscillation type A/D converter, TBC128Hz, TBC32Hz, TBC16Hz, TBC2Hz)
    - External source: 8 (P00, P01, P02, P03, P50, P51, P52, P53) *
    - *: For P50 to P53, the interrupt sources are ORed into a single interrupt request.

- Time base counter
  - Low-speed time base counter x 1 channel
    - Frequency compensation (Compensation range: Approx. -488ppm to +488ppm. Compensation accuracy: Approx. 0.48ppm)
  - High-speed time base counter x 1 channel

- Watchdog timer
  - Non-maskable interrupt and reset
  - Free running
  - Overflow period: 4 types selectable (125ms, 500ms, 2s, 8s)

- Timer
  - 8 bits x 2 channels [also available is 16-bit configuration (using Timers 2 and 3) x 1 channels]
  - Clock frequency measurement function mode (16-bit configuration only)

- Capture
  - Time base capture x 2 channels (4096 Hz to 32 Hz)

- UART
  - TXD/RXD × 1 channel
  - Bit length, parity/no parity, odd parity/even parity, 1 stop bit/2 stop bits
  - Positive logic/negative logic selectable
  - Built-in baud rate generator

- Melody driver
  - Scale: 29 types (Melody sound frequency: 508 Hz to 32.768 kHz)
  - Tone length: 63 types
  - Tempo: 15 types
  - Buzzer output mode (4 output modes, 8 frequencies, 16 duty levels)

- RC oscillation type A/D converter
  - 16-bit counter
  - Time division x 2 channels

- General-purpose port
  - Input-only port: 4 channels (including secondary functions)
  - Output-only port
    - ML610401: 12 channels (including secondary functions)
    - ML610402: 8 channels (including secondary functions)
    - ML610403: 4 channels (including secondary functions)
  - Input/output port: 18 channels (including secondary functions)

- LCD driver
  - Number of segments
    - ML610401: Up to 55 dots (select among 11 segments x 5 commons, 12 segments x 4 commons, 13 segments x 3 commons, and 14 segments x 2 commons)
    - ML610402: Up to 75 dots (select among 15 segments x 5 commons, 16 segments x 4 commons, 17 segments x 3 commons, and 18 segments x 2 commons)
    - ML610403: Up to 95 dots (select among 19 segments x 5 commons, 20 segments x 4 commons, 21 segments x 3 commons, and 22 segments x 2 commons)
  - 1/1 to 1/5 duty
  - 1/3 bias (built-in bias generation circuit)
  - Frame frequency selectable (approx. 64 Hz, 73 Hz, 85 Hz, and 102 Hz)
  - Bias voltage multiplying clock selectable (8 types)
  - LCD drive stop mode, LCD display mode, all LCDs on mode, and all LCDs off mode selectable
  - Programmable display allocation function

- Reset
  - Reset through the RESET_N pin
  - Power-on reset generation when powered on
  - Reset when oscillation stop of the low-speed clock is detected(Cancellation by a mask option is possible)
  - Reset by the WDT overflow

- Clock
  - Low-speed clock (Operation of this LSI is not guaranteed under a condition with no supply of low-speed crystal oscillation clock)
    - Crystal oscillation (32.768 kHz)
  - High-speed clock
    - Built-in RC oscillation (500 kHz)

● Power management
  - HALT mode: Suspends the instruction execution by CPU (peripheral circuits are in operating states)
  - STOP mode: Stops the low-speed oscillation and high-speed oscillation (Operations of CPU and
      peripheral circuits are stopped.)
  - High-speed clock gear: The frequency of high-speed system clock can be changed by software (1/1, 1/2,
      1/4, or 1/8 of the oscillation clock)
  - Block control function: Completely stops the operation of any function block circuit that is not used
      (resets registers and stops clock)

● Guaranteed Operation Range
  − Operating temperature: -20°C to +70°C (P version: -40°C to +85°C)
  − Operating voltage: VDD = 1.25V to 3.6V

● Product name – Supported Function

- Chip (Die) -	LCD bias		Low-speed oscillation stop detect reset	Operating temperature	Product availability
	1/2	1/3			
ML610401-xxxWA	-	Yes	Cancellation by a mask option is possible	-20°C to +70°C	Yes
ML610402-xxxWA	-	Yes	Cancellation by a mask option is possible	-20°C to +70°C	Yes
ML610403-xxxWA	-	Yes	Cancellation by a mask option is possible	-20°C to +70°C	Yes
ML610401P-xxxWA	-	Yes	Cancellation by a mask option is possible	-40°C to +85°C	Yes
ML610402P-xxxWA	-	Yes	Cancellation by a mask option is possible	-40°C to +85°C	Yes
ML610403P-xxxWA	-	Yes	Cancellation by a mask option is possible	-40°C to +85°C	Yes

-64-pin plastic TQFP -	LCD bias		Low-speed oscillation stop detect reset	Operating temperature	Product availability
	1/2	1/3			
ML610401-xxxTB	-	Yes	Cancellation by a mask option is possible	-20°C to +70°C	-
ML610402-xxxTB	-	Yes	Cancellation by a mask option is possible	-20°C to +70°C	-
ML610403-xxxTB	-	Yes	Cancellation by a mask option is possible	-20°C to +70°C	-
ML610401P-xxxTB	-	Yes	Cancellation by a mask option is possible	-40°C to +85°C	-
ML610402P-xxxTB	-	Yes	Cancellation by a mask option is possible	-40°C to +85°C	
ML610403P-xxxTB	-	Yes	Cancellation by a mask option is possible	-40°C to +85°C	-

xxx: ROM code number
P: Wide range temperature version (P version)
WA: Chip (Die)
TB: TQFP

1.2 Configuration of Functional Blocks

1.2.1   Block Diagram of ML610401/ML610402/ML610403
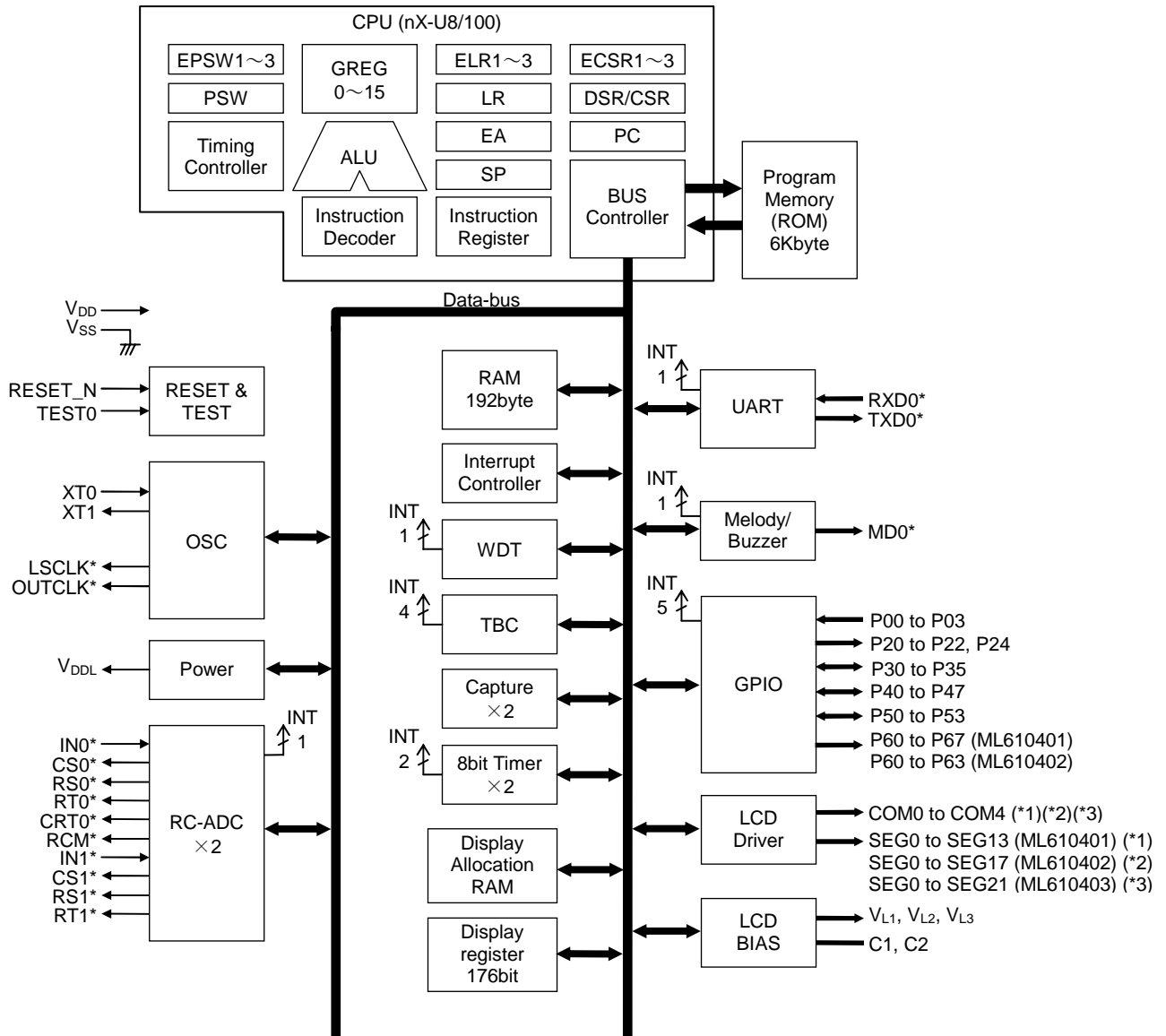
* Secondary function

"*1": Select among 11 segments x 5 commons, 12 segments x 4 commons, 13 segments x 3 commons, and 14 segments x 2 commons with the register

"*2": Select among 15 segments x 5 commons, 16 segments x 4 commons, 17 segments x 3 commons, and 18 segments x 2 commons with the register

"*3": Select among 19 segments x 5 commons, 20 segments x 4 commons, 21 segments x 3 commons, and 22 segments x 2 commons with the register

Figure 1-1   Block Diagram of ML610401/2/3

1.3 Pins

1.3.1   Pin Layout

1.3.1.1 Pin Layout of ML610401 TQFP Package

<p style="text-align:center; color:red; font-size:2em;">Not available</p>

Figure 1-2   Pin Layout of ML610401 Package

1.3.1.2 Pin Layout of ML610402 TQFP Package

Not available

Figure 1-3   Pin Layout of ML610402 Package

1.3.1.3 Pin Layout of ML610403 TQFP Package

Not available

Figure 1-4   Pin Layout of ML610403 Package

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1.3.1.4 Pin Layout of ML610401 Chip
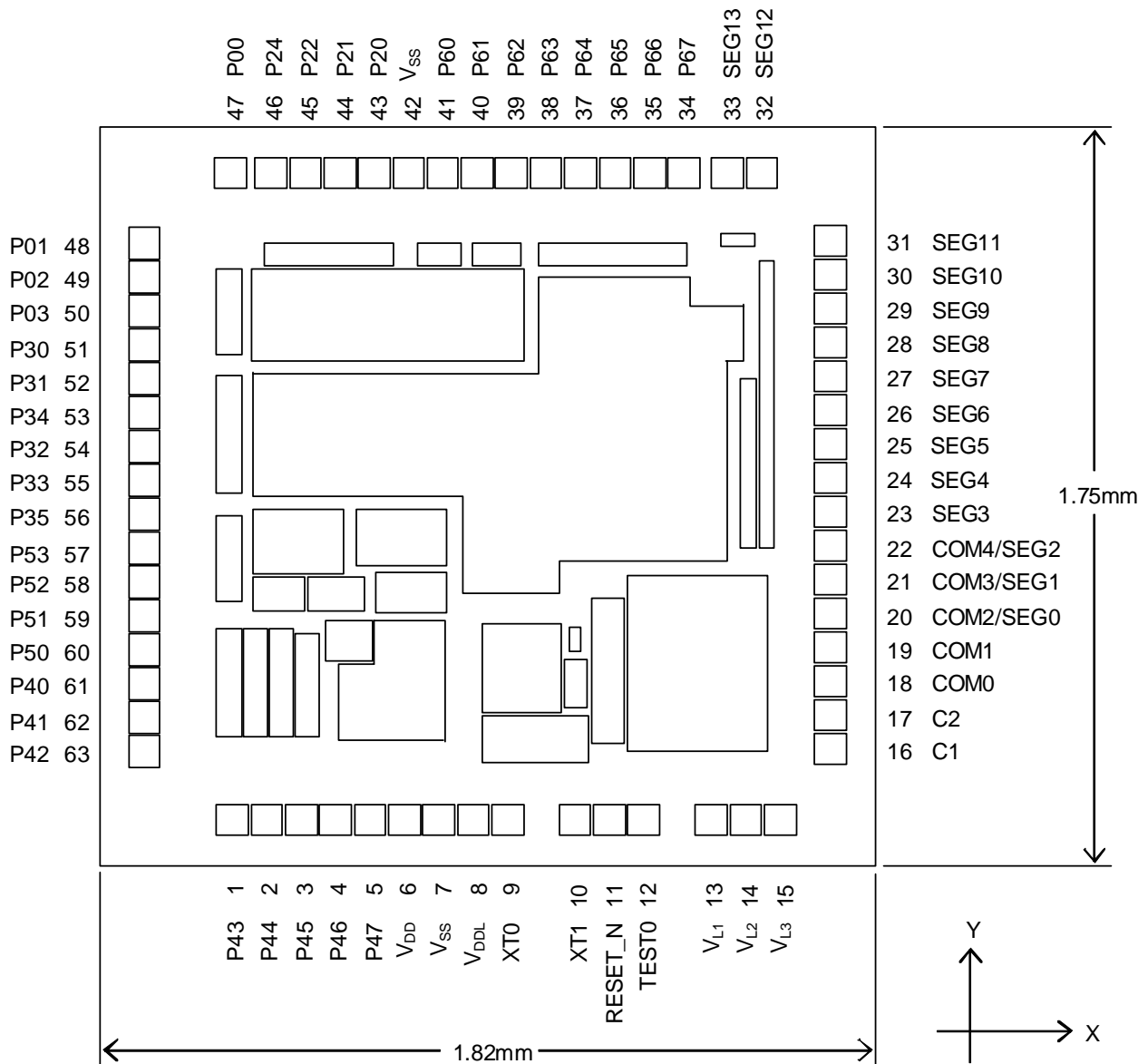
Note:
The assignment of the pads P30 to P35 are not in order.

Chip size: 1.82 mm × 1.75 mm
PAD count: 63 pins
Minimum PAD pitch: 80 μm
PAD aperture: 70 μm × 70 μm
Chip thickness: 350 μm
Voltage of the rear side of chip: VSS level.

Figure 1-5   Dimensions of ML610401 Chip

1.3.1.5 Pin Layout of ML610402 Chip
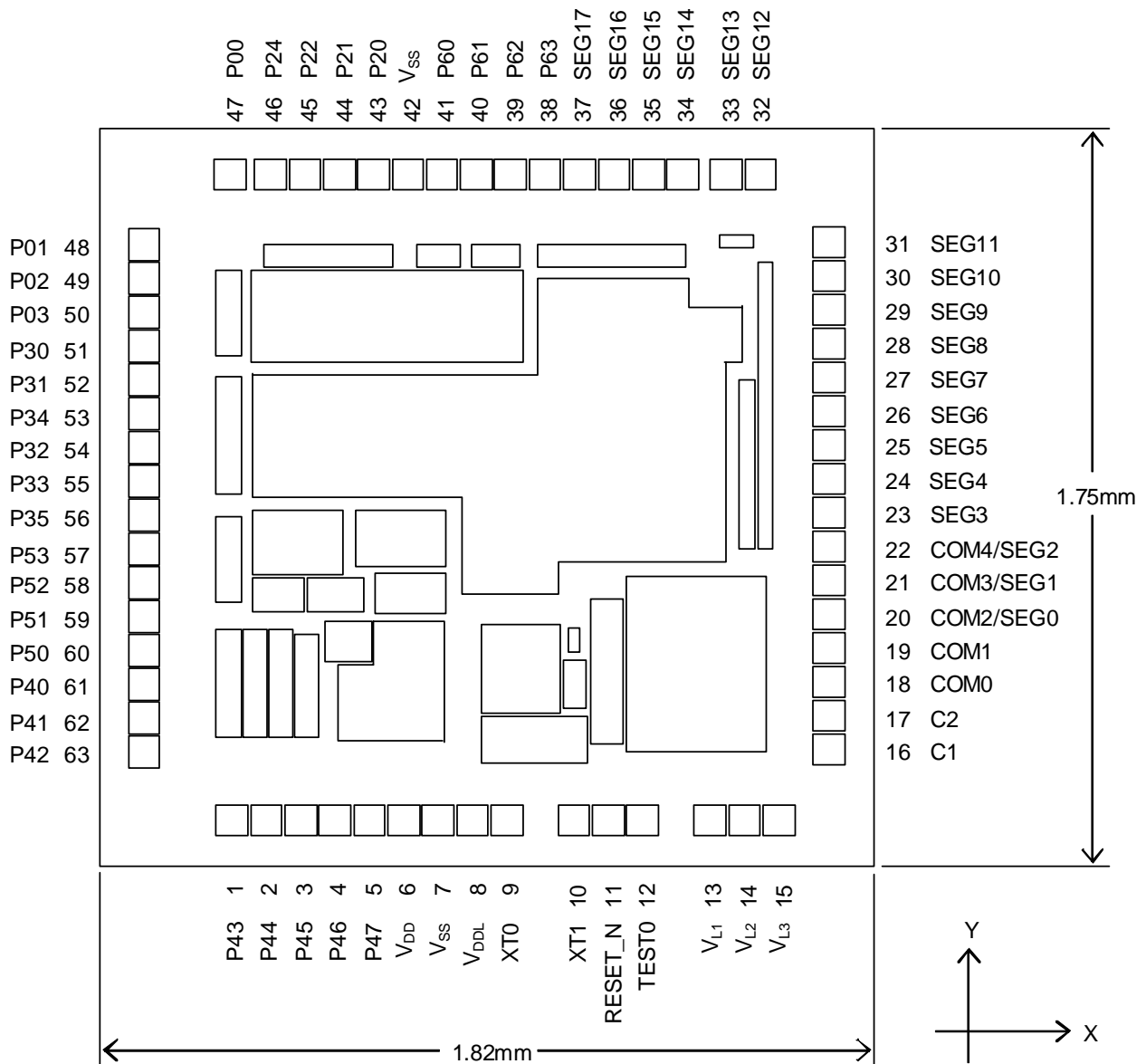
Note:
The assignment of the pads P30 to P35 are not in order.

Chip size: 1.82 mm × 1.75 mm
PAD count: 63 pins
Minimum PAD pitch: 80 μm
PAD aperture: 70 μm × 70 μm
Chip thickness: 350 μm
Voltage of the rear side of chip: VSS level.

Figure 1-6   Dimensions of ML610402 Chip

1.3.1.6 Pin Layout of ML610403 Chip
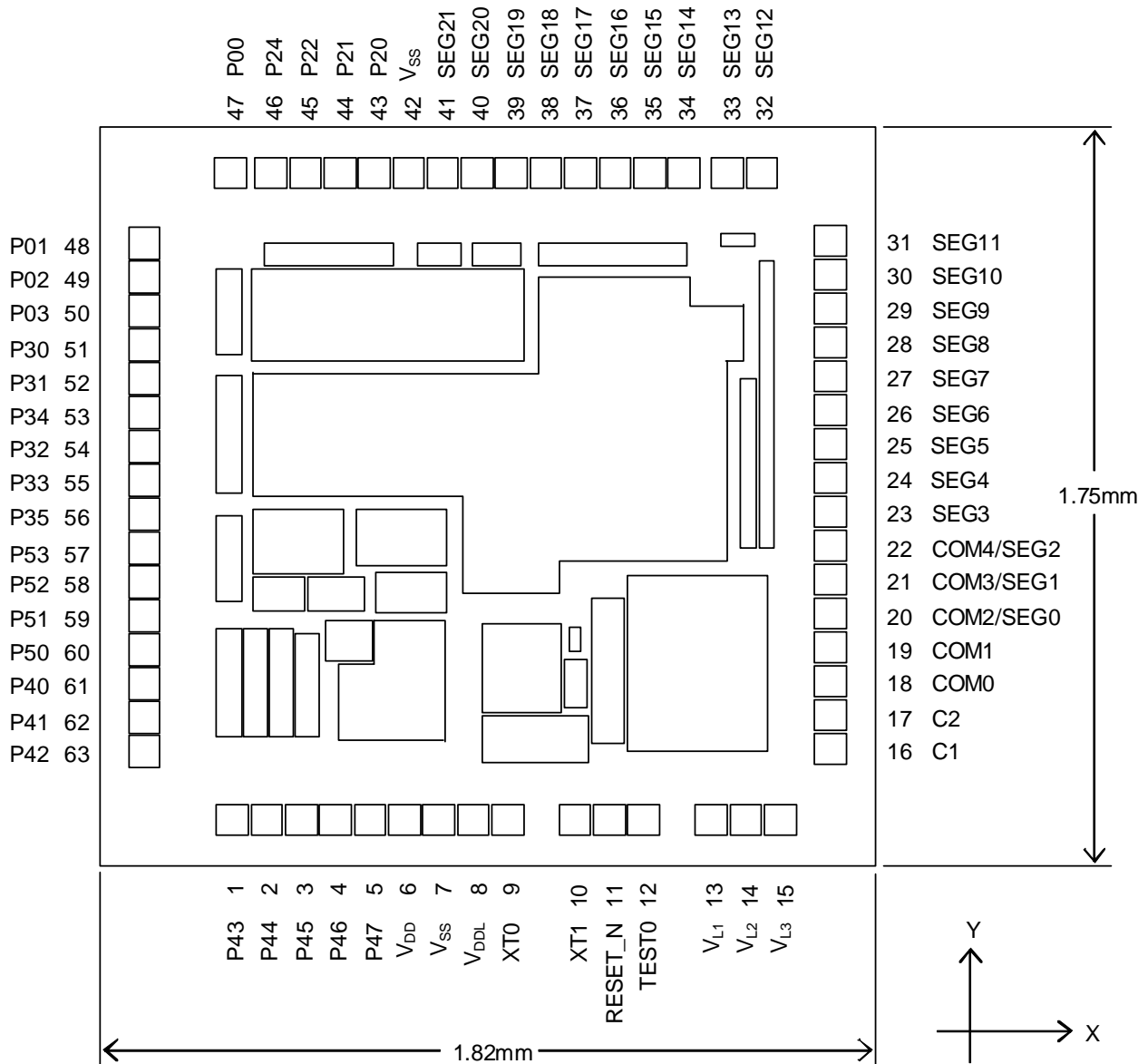
Note:
The assignment of the pads P30 to P35 are not in order.

Chip size: 1.82 mm ×1.75 mm
PAD count: 63 pins
Minimum PAD pitch: 80 μm
PAD aperture: 70 μm × 70 μm
Chip thickness: 350 μm
Voltage of the rear side of chip: VSS level.

Figure 1-7   Dimensions of ML610403 Chip

1.3.1.7 Pad Coordinates of ML610401/ML610402/ML610403 Chip

Table 1-1 Pad Coordinates of ML610401/ML610402/ML610403

Chip Center: X=0,Y=0

PAD No.	Pad Name	ML610401/2/3 X (μm)	ML610401/2/3 Y (μm)	PAD No.	Pad Name	ML610401/2/3 X (μm)	ML610401/2/3 Y (μm)
1	P43	-598	-769	35	P66 [*1] / SEG15 [*2][*3]	375	769
2	P44	-518	-769				
3	P45	-438	-769	36	P65 [*1] / SEG16 [*2][*3]	295	769
4	P46	-358	-769				
5	P47	-278	-769	37	P64 [*1] / SEG17 [*2][*3]	215	769
6	V_{DD}	-198	-769				
7	V_{SS}	-118	-769	38	P63 [*1][*2] / SEG18 [*3]	135	769
8	V_{DDL}	-38	-769				
9	XT0	42	-769	39	P62 [*1][*2] / SEG19 [*3]	55	769
10	XT1	202	-769				
11	RESET_N	282	-769	40	P61 [*1][*2] / SEG20 [*3]	-25	769
12	TEST0	362	-769				
13	VL1	522	-769	41	P60 [*1][*2] / SEG21 [*3]	-105	769
14	VL2	602	-769				
15	VL3	682	-769	42	V_{SS}	-185	769
16	C1	804	-600	43	P20	-265	769
17	C2	804	-520	44	P21	-345	769
18	COM0	804	-440	45	P22	-425	769
19	COM1	804	-360	46	P24	-505	769
20	COM2/SEG0	804	-280	47	P00	-605	769
21	COM3/SEG1	804	-200	48	P01	-804	600
22	COM4/SEG2	804	-120	49	P02	-804	520
23	SEG3	804	-40	50	P03	-804	440
24	SEG4	804	40	51	P30	-804	360
25	SEG5	804	120	52	P31	-804	280
26	SEG6	804	200	53	P34	-804	200
27	SEG7	804	280	54	P32	-804	120
28	SEG8	804	360	55	P33	-804	40
29	SEG9	804	440	56	P35	-804	-40
30	SEG10	804	520	57	P53	-804	-120
31	SEG11	804	600	58	P52	-804	-200
32	SEG12	645	769	59	P51	-804	-280
33	SEG13	565	769	60	P50	-804	-360
34	P67 [*1] / SEG14 [*2][*3]	455	769	61	P40	-804	-440
				62	P41	-804	-520
				63	P42	-804	-600

[*1] Pad for ML610401. [*2] Pad for ML610402. [*3] Pad for ML610403.

1.3.2　List of Pins

PIN No.	PAD No.	Primary function			Secondary function		
		Pin name	I/O	Function	Pin name	I/O	Function
7,43	7,42	Vss	—	Negative power supply pin	—	—	—
6	6	V_{DD}	—	Positive power supply pin	—	—	—
8	8	V_{DDL}	—	Power supply pin for internal logic (internally generated)	—	—	—
14	13	VL1	—	Power supply pin for LCD bias (internally generated or connected to positive power supply pin)[*1]	—	—	—
15	14	V_{L2}	—	Power supply pin for LCD bias (internally generated or connected to positive power supply pin)[*1]	—	—	—
16	15	V_{L3}	—	Power supply pin for LCD bias (internally generated)	—	—	—
17	16	C1	—	Capacitor connection pin for LCD bias generation	—	—	—
18	17	C2	—	Capacitor connection pin for LCD bias generation	—	—	—
13	12	TEST0	I	Test pin	—	—	—
12	11	RESET_N	I	Reset input pin	—	—	—
10	9	XT0	I	Low-speed clock oscillation pin	—	—	—
11	10	XT1	O	Low-speed clock oscillation pin	—	—	—
48	47	P00/EXI0/ CAP0	I	Input port, External interrupt, Capture 0 input	—	—	—
49	48	P01/EXI1/ CAP1	I	Input port, External interrupt, Capture 1 input	—	—	—
50	49	P02/EXI2/ RXD0	I	Input port, External interrupt, UART0 data input	—	—	—
51	50	P03/EXI3	I	Input port, External interrupt	—	—	—
44	43	P20/LED0	O	Output port	LSCLK	O	Low-speed clock output
45	44	P21/LED1	O	Output port	OUTCLK	O	High-speed clock output
46	45	P22/LED2	O	Output port	MD0	O	Melody 0 output
47	46	P24/LED4	O	Output port	—	—	—
52	51	P30	I/O	Input/output port	IN0	I	RC type ADC0 oscillation input pin
53	52	P31	I/O	Input/output port	CS0	O	RC type ADC0 reference capacitor connection pin
54	53	P34	I/O	Input/output port	RCT0	O	RC type ADC0 resistor/capacitor sensor connection pin
55	54	P32	I/O	Input/output port	RS0	O	RC type ADC0 reference resistor connection pin
56	55	P33	I/O	Input/output port	RT0	O	RC type ADC0 measurement resistor sensor connection pin
57	56	P35	I/O	Input/output port	RCM	O	RC type ADC oscillation monitor pin
62	61	P40	I/O	Input/output port	—	—	—
63	62	P41	I/O	Input/output port	—	—	—
64	63	P42	I/O	Input/output port	RXD0	I	UART data input
1	1	P43	I/O	Input/output port	TXD0	O	UART data output
2	2	P44/T2CK	I/O	Input/output port, Timer 2 external clock input	IN1	I	RC type ADC1 oscillation input pin
3	3	P45/T3CK	I/O	Input/output port, Timer 3 external clock input	CS1	O	RC type ADC1 reference capacitor connection pin
4	4	P46	I/O	Input/output port	RS1	O	RC type ADC1 reference resistor connection pin
5	5	P47	I/O	Input/output port	RT1	O	RC type ADC1 measurement resistor sensor connection pin

PIN No.	PAD No.	Primary function			Secondary function		
		Pin name	I/O	Function	Pin name	I/O	Function
61	60	P50/EXI8	I/O	Input/output port, External interrupt	MD0	O	Melody 0 output
60	59	P51/EXI8	I/O	Input/output port, External interrupt	—	—	—
59	58	P52/EXI8	I/O	Input/output port, External interrupt	—	—	—
58	57	P53/EXI8	I/O	Input/output port, External interrupt	—	—	—
19	18	COM0	O	LCD common pin	—	—	—
20	19	COM1	O	LCD common pin	—	—	—
21	20	COM2/ SEG0	O	LCD common/segment pin	—	—	—
22	21	COM3/ SEG1	O	LCD common/segment pin	—	—	—
23	22	COM4/ SEG2	O	LCD common/segment pin	—	—	—
24	23	SEG3	O	LCD segment pin	—	—	—
25	24	SEG4	O	LCD segment pin	—	—	—
26	25	SEG5	O	LCD segment pin	—	—	—
27	26	SEG6	O	LCD segment pin	—	—	—
28	27	SEG7	O	LCD segment pin	—	—	—
29	28	SEG8	O	LCD segment pin	—	—	—
30	29	SEG9	O	LCD segment pin	—	—	—
31	30	SEG10	O	LCD segment pin	—	—	—
32	31	SEG11	O	LCD segment pin	—	—	—
33	32	SEG12	O	LCD segment pin	—	—	—
34	33	SEG13	O	LCD segment pin	—	—	—
35	34	P67[*4]	O	Output port	—	—	—
		SEG14[*5]	O	LCD segment pin	—	—	—
36	35	P66[*4]	O	Output port	—	—	—
		SEG15[*5]	O	LCD segment pin	—	—	—
37	36	P65[*4]	O	Output port	—	—	—
		SEG16[*5]	O	LCD segment pin	—	—	—
38	37	P64[*4]	O	Output port	—	—	—
		SEG17[*5]	O	LCD segment pin	—	—	—
39	38	P63[*2]	O	Output port	—	—	—
		SEG18[*3]	O	LCD segment pin	—	—	—
40	39	P62[*2]	O	Output port	—	—	—
		SEG19[*3]	O	LCD segment pin	—	—	—
41	40	P61[*2]	O	Output port	—	—	—
		SEG20[*3]	O	LCD segment pin	—	—	—
42	41	P60[*2]	O	Output port	—	—	—
		SEG21[*3]	O	LCD segment pin	—	—	—

[*1] Internally generated, or connect to either positive power supply pin (V_{DD}) or power supply pin for internal logic (V_{DDL}). For details, see "Chapter 20   LCD Drivers."
[*2] Pin for ML610401/ML610402.
[*3] Pin for ML610403.
[*4] Pin for ML610401.
[*5] Pin for ML610402/ML610403.

1.3.3 Pin Descriptions

Pin name	I/O	Description	Primary/ Secondary	Logic
System				
RESET_N	I	Reset input pin. When this pin is set to a "L" level, system reset mode is set and the internal section is initialized. When this pin is set to a "H" level subsequently, program execution starts. A pull-up resistor is internally connected.	—	Negative
XT0	I	Crystal connection pin for low-speed clock. A 32.768 kHz crystal resonator is connected to this pin. Capacitors C_{DL} and C_{GL} are connected across this pin and V_{SS}. (see appendix C measuring circuit 1)	—	—
XT1	O		—	—
LSCLK	O	Low-speed clock output. Assigned to the secondary function of the P20 pin.	Secondary	—
OUTCLK	O	High-speed clock output pin. This pin is used as the secondary function of the P21 pin.	Secondary	—
General-purpose input port				
P00 to P03	I	General-purpose input port.	Primary	Positive
General-purpose output port				
P20 to P22, P24	O	General-purpose output port. This cannot be used as the general output port when used as the secondary function.	Primary	Positive
General-purpose input/output port				
P30 to P35	I/O	General-purpose input/output port. This cannot be used as the general input/output port when used as the secondary function.	Primary	Positive
P40 to P47	I/O	General-purpose input/output port. This cannot be used as the general input/output port when used as the secondary function.	Primary	Positive
P50 to P53	I/O	General-purpose input/output port. This cannot be used as the general input/output port when used as the secondary function.	Primary	Positive
P60 to P63	O	General-purpose output port. Incorporated only into ML610401/ML610402, and not into ML610403.	Primary	Positive
P64 to P67	O	General-purpose output port. Incorporated only into ML610401, and not into ML610402/ML610403.	Primary	Positive

Pin name	I/O	Description	Primary/ Secondary	Logic
UART				
TXD0	O	UART data output pin. This pin is used as the secondary function of the P43 pin.	Secondary	Positive
RXD0	I	UART data input pin. This pin is used as the secondary function of the P42 or the primary function of the P02 pin.	Primary/ Secondary	Positive
External interrupt				
EXI0-3	I	External maskable interrupt input pins. Interrupt enable and edge selection can be performed for each bit by software. These pins are used as the primary functions of the P00 to P03 pins.	Primary	Positive/ negative
EXI8	I	External maskable interrupt input pins. Interrupt enable and edge selection can be performed for each bit by software. Assigned to the primary function of the P50 to P53 pins.	Primary	Positive/ negative
Capture				
CAP0	I	Capture trigger input pins. The value of the time base counter is captured in the register synchronously with the interrupt edge selected by software. These pins are used as the primary functions of the P00 pin(CAP0) and P01 pin(CAP1).	Primary	Positive/ negative
CAP1	I		Primary	Positive/ negative
Timer				
T2CK	I	External clock input pin used for Timer 2. This pin is used as the primary function of the P04 pin and P44 pin.	Primary	—
T3CK	I	External clock input pin used for Timer 3. This pin is used as the primary function of the P45 pin.	Primary	—
Melody				
MD0	O	Melody/buzzer signal output pin. This pin is used as the secondary function of the P22 and P50 pins.	Secondary	Positive/ negative
LED drive				
LED0 to LED2, LED4	O	N-channel open drain output pins to drive LED. This pin is used as the primary function of the P20 to P22 and P24 pins.	Primary	Positive /negative

Pin name	I/O	Description	Primary/ Secondary/ Tertiary	Logic
RC oscillation type A/D converter				
IN0	I	Channel 0 oscillation input pin. This pin is used as the secondary function of the P30 pin.	Secondary	—
CS0	O	Channel 0 reference capacitor connection pin. This pin is used as the secondary function of the P31 pin.	Secondary	—
RCT0	O	Resistor/capacitor sensor connection pin of Channel 0 for measurement. This pin is used as the secondary function of the P34 pin.	Secondary	—
RS0	O	This pin is used as the secondary function of the P32 pin which is the reference resistor connection pin of Channel 0.	Secondary	—
RT0	O	Resistor sensor connection pin of Channel 0 for measurement. This pin is used as the secondary function of the P33 pin.	Secondary	—
RCM	O	RC oscillation monitor pin. This pin is used as the secondary function of the P35 pin.	Secondary	—
IN1	I	Oscillation input pin of Channel 1. This pin is used as the secondary function of the P44 pin.	Secondary	—
CS1	O	Reference capacitor connection pin of Channel 1. This pin is used as the secondary function of the P45 pin.	Secondary	—
RS1	O	Reference resistor connection pin of Channel 1. This pin is used as the secondary function of the P46 pin.	Secondary	—
RT1	O	Resistor sensor connection pin for measurement of Channel 1. This pin is used as the secondary function of the P47 pin.	Secondary	—
LCD drive signal				
COM0 to COM4	O	Common output pins. COM2, COM3, and COM4 can be switched to SEG0, SEG1, and SEG2, respectively, through the register setting. To change the setting, switch between COM4 and SEG2 for one pin and switch between COM3, COM4 and SEG1, SEG2 for two pins.	—	—
SEG0 to SEG13	O	Segment output pin. The SEG0, SEG1, and SEG2 pins are for switching the register setting with the COM2, COM3, and COM4.	—	—
SEG14 to SEG17	O	Segment output pin. Incorporated into ML610402/ML610403, not into ML610401.	—	—
SEG18 to SEG21	O	Segment output pin. Incorporated into ML610403, not into ML610401/ML610402.		
LCD driver power supply				
V_{L1}	—	Power supply pin for LCD bias (internally generated) or power supply connection pin. Depending on LCD Bias setting and V_{DD} voltage level, V_{DD} or V_{DDL} or capacitor is connected. For details of the connection method, see "appendix C measuring circuit 1."	—	—
V_{L2}	—		—	—
V_{L3}	—		—	—
C1	—	Power supply pins for LCD bias (internally generated). Capacitor C_{12} (see measuring circuit 1) is connected between C1 and C2.	—	—
C2	—		—	—

Pin name	I/O	Description	Primary/ Secondary/ Tertiary	Logic
Test				
TEST0	I/O	Pin for testing. A pull-down resistor is internally connected.	—	Positive
Power supply				
V_{SS}	—	Negative power supply pin.	—	—
V_{DD}	—	Positive power supply pin.	—	—
V_{DDL}	—	Positive power supply pin (internally generated) for internal logic. Capacitors C_{L0} and C_{L1} (see measuring circuit 1) are connected between this pin and V_{SS}.	—	—

1.3.4 Handling of Unused Pins

Table 1-2 shows methods of terminating the unused pins.

Table 1-2   Termination of Unused Pins

Pin	Recommended pin handling
V_{PP}	Open
V_{L1}	Open
V_{L2}	Open
V_{L3}	Open
C1, C2	Open
RESET_N	Open
TEST0	Open
TEST1_N	Open
P00 to P03	V_{DD} or V_{SS}
P20 to P22, P24	Open
P30 to P35	Open
P40 to P47	Open
P50 to P53	Open
P60 to P67	Open
COM0 to COM 4	Open
SEG0 to SEG 21	Open

Note:
It is recommended to set the unused input ports and input/output ports to the inputs with pull-down resistors/pull-up resistors or the output mode since the supply current may become excessively large if the pins are left open in the high impedance input setting.

CPU and Memory Space

2.　CPU and Memory Space

2.1　Overview

This LSI includes 8-bit CPU nX-U8/100 and the memory model is SMALL model.
For details of the CPU nX-U8/100, see "nX-U8/100 Core Instruction Manual".

2.2　Program Memory Space

The program memory space is used to store program codes, table data (ROM window), or vector tables.
The program codes have a length of 16 bits and are specified by a 16-bit program counter (PC).
The ROM window area data has a length of 8 bits and can be used as table data.
The vector table, which has 16-bit long data, can be used as reset vectors, hardware interrupt vectors, and software interrupt vectors.
The program memory space consists of one segment and has 6-Kbyte (3-Kword) capacity.
Figure 2-1 shows the configuration of the program memory space.

PC	
0000H	Vector Table Area or Program Code
00FFH	ROM Window Area
0100H	
	Program Code Area or ROM Window Area
16FFH	
1700H	
	Unused Area
3CFFH	
3D00H	Test Data Area
3DFFH	
3E00H	Unused Area
3FFFH	
	8bit
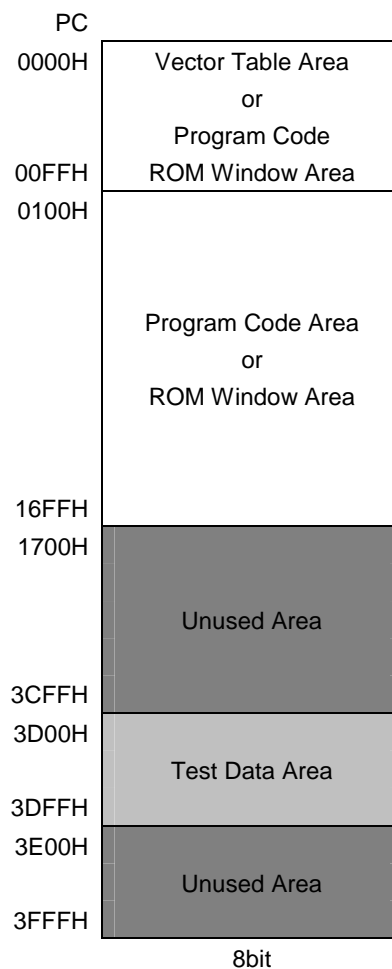
Figure 2-1　Configuration of Program Memory Space

Note:
・ The 256 bytes (128 words) from 3D00H to 3DFFH are the test data area. From 3DE8H to 3DFFH, set the Mask ROM version mode data programmed by using the Mask ROM version emulation function of ML610Q407. For the Mask ROM version emulation function, see "ML610Q407 user's manual : Chapter 25 Mask ROM Version Emulation Function".
・ Set "0FFH" data (BRK instruction) in the unused area of the program memory space.

2.3 Data Memory Space

The data memory space of this LSI consists of the ROM window area, 192Byte RAM area, and SFR area of Segment 0.
The data memory has the 8-bit length and is specified by the addressing specified by each instruction.

Figure 2-2 shows the configuration of the data memory space.
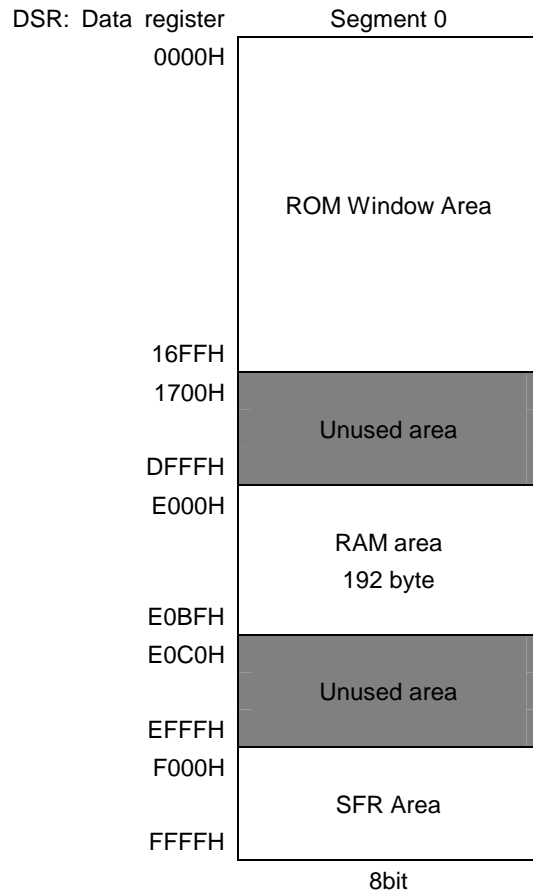
Figure 2-2   Configuration of Data Memory Space

Note:
・The contents of the RAM area are undefined at system reset. Initialize this area by software.

2.4　Instruction Length

The length of an instruction is 16 bits.

2.5　Data Type

The data types supported include byte (8 bits) and word (16 bits).

2.6 Description of Registers

2.6.1   List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F000H	Data segment register	DSR	—	R/W	8	00H

2.6.2   Data Segment Register (DSR)

Address: 0F000H
Access: R/W
Access size: 8-bit
Initial value: 00H

	7	6	5	4	3	2	1	0
DSR	—	—	—	—	DSR3	DSR2	DSR1	DSR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

DSR is a special function register (SFR) to retain a data segment.
Always use this register with the initial state (0). For details of DSR, see "nX-U8/100 Core Instruction Manual".

[Description of Bits]
- **DSR3-DSR0** (bits 3 to 0)

DSR3	DSR2	DSR1	DSR0	Description
0	0	0	0	Initial value
In other than above				Prohibited

Reset Function

3.   Reset Function

3.1 Overview

This LSI has the five reset functions shown below. If any of the five reset conditions is satisfied, this LSI enters system reset mode.

- Reset by the RESET_N pin
- Reset by power-on detection
- Reset by the low-speed oscillation stop detection (Cancellation by a mask option is possible)
- Reset by the 2nd watchdog timer (WDT) overflow
- Software reset by execution of the BRK instruction

3.1.1   Features

- The RESET_N pin has an internal pull-up resistor
- The low-speed oscillation stop detection time is 19 ms (typ.)
- 250 ms, 1 sec, 4 sec, or 16 sec can be selected as the watchdog timer (WDT) overflow period
- Built-in reset status register (RSTAT) indicating the reset generation causes
- Only the CPU is reset by the BRK instruction (neither the RAM area nor the SFR area are reset).

3.1.2   Configuration

Figure 3-1 shows the configuration of the reset generation circuit.
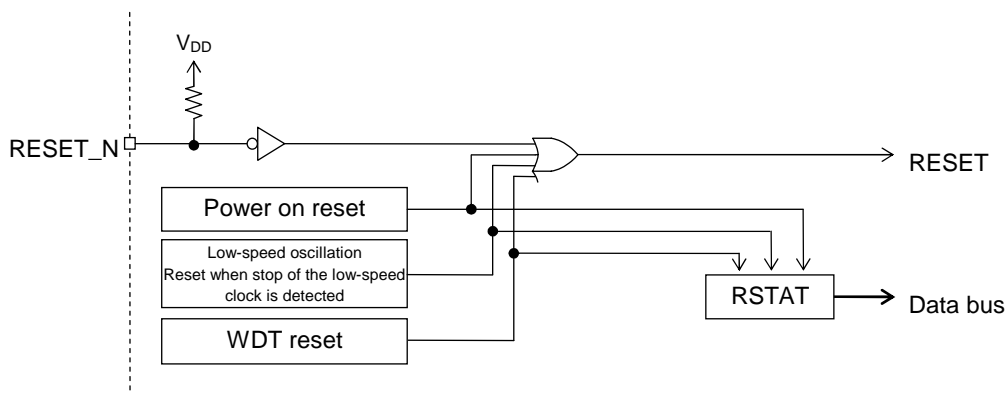
RSTAT   : Reset status register

Figure 3-1   Configuration of Reset Generation Circuit

3.1.3   List of Pins

Pin name	Input/output	Function
RESET_N	I	Reset input pin

3.2 Description of Registers

3.2.1　List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F001H	Reset status register	RSTAT	—	R/W	8	—

3.2.2　Reset Status Register (RSTAT)

Address: 0F001H
Access: R/W
Access size: 8-bit
Initial value: Undefined

	7	6	5	4	3	2	1	0
RSTAT	—	—	—	—	—	WDTR	XSTR	POR
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	X	1

RSTAT is a special function register (SFR) that indicates the causes by which the reset is generated.
At the occurrence of reset, the contents of RSTAT are not initialized, while the bit indicating the cause of the reset is set to "1". When checking the reset cause using this function, perform write operation to RSTAT in advance and initialize the contents of RSTAT to "00H".

[Description of Bits]
- **POR** (bit 0)
  The POR bit is a flag that indicates that the power-on reset is generated. This bit is set to "1" when powered on.

POR	Description
0	Power-on reset not generated
1	Power-on reset generated

- **XSTR** (bit 1)
  The XSTR bit is a flag that indicates the generation of low-speed oscillation stop detect reset. When low-speed oscillation stops for the period specified by the low-speed oscillation stop detection time (T_{STOP}) or more, this bit is set to "1". When the low-speed oscillation stop detection reset is disabled by a mask option, it always returns the value "0". For the Mask-Option, see Chapter 22, "Mask Option".

XSTR	Description
0	Low-speed oscillation stop detect reset not occurred
1	Low-speed oscillation stop detect reset occurred

- **WDTR** (bit 2)
  The WSDTR is a flag that indicates that the watchdog timer reset is generated. This bit is set to "1" when the reset by overflow of the watchdog timer is generated.

WDTR	Description
0	Watchdog timer reset not occurred
1	Watchdog timer reset occurred

Note:
No flag is provided that indicates the occurrence of reset by the RESET_N pin.

3.3 Description of Operation

3.3.1   Operation of System Reset Mode

System reset has the highest priority among all the processings and any other processing being executed up to then is cancelled.
The system reset mode is set by any of the following causes.

- Reset by the RESET_N pin
- Reset by power-on detection
- Reset by the low-speed oscillation stop detection (Cancellation by a mask option is possible)
- Reset by watchdog timer (WDT) overflow
- Software reset by the BRK instruction (only the CPU is reset)

In system reset mode, the following processing is performed.

(1) The power circuit is initialized. However, it is not initialized by the reset by the BRK instruction execution. For the details of the power circuit, refer to Chapter 21, "Power Circuit".
(2) All the special function registers (SFRs) whose initial value is not undefined are initialized. However, the initialization is not performed by software reset due to execution of the BRK instruction. See Appendix A "Registers" for the initial values of the SFRs.
(3) CPU is initialized.
-     All the registers in CPU are initialized.
-     The contents of addresses 0000H and 0001H in the program memory are set to the stack pointer (SP).
-     The contents of addresses 0002H and 0003H in the program memory are set to the program counter (PC). However, when the interrupt level (ELEEVL) of the program status word (PSW) at reset by the BRK instruction is 1 or lower, the contents of addresses 0004H and 0005H of the program memory are set in the program counter (PC). For the BRK instruction, see "nX-U8/100 Core Instruction Manual".

Note:
In system reset mode, the contents of data memory and those of any SFR whose initial value is undefined are not initialized and are undefined. Initialize them by software.
In system reset mode by the BRK instruction, no special function register (SFR) that has a fixed initial value is initialized either. Therefore initialize such an SFR by software.

MCU Control Function

4. MCU Control Function

4.1 Overview

The operating states of this LSI are classified into the following 4 modes including system reset mode:

(1) System reset mode
(2) Program run mode
(3) HALT Mode
(4) STOP mode

For system reset mode, see Chapter 3, "Reset Function".

4.1.1   Features

- HALT mode, where the CPU stops operating and only the peripheral circuit is operating
- STOP mode, where both low-speed oscillation and high-speed oscillation stop
- Stop code acceptor function, which controls transition to STOP mode
- Block control function, which power downs the circuits of unused peripherals (reset registers and stop clock supplies)

4.1.2   Configuration

Figure 4-1 shows an operating state transition diagram.
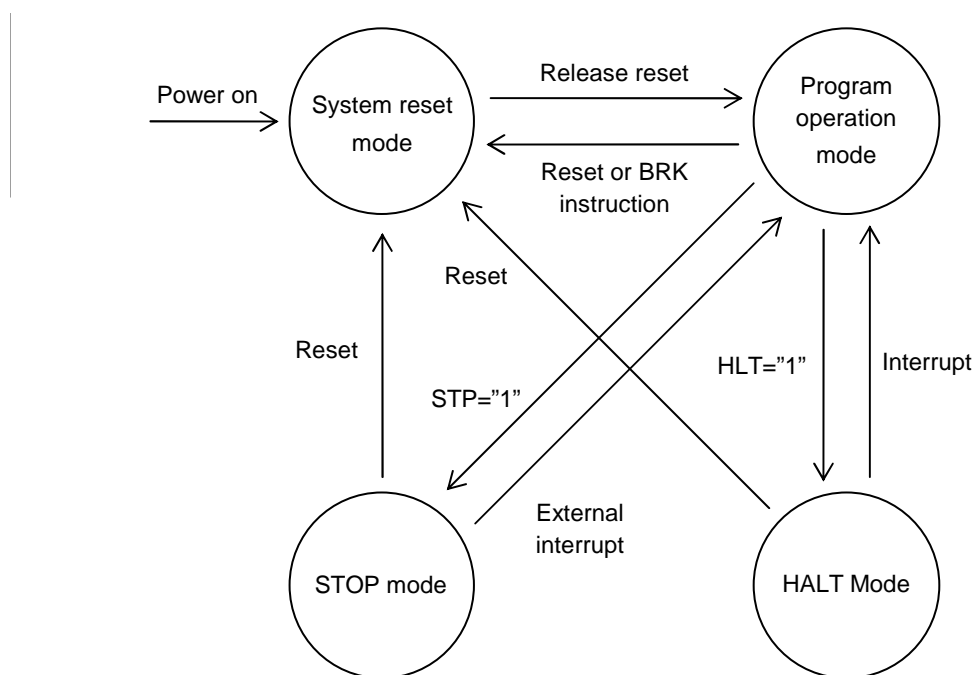
Figure 4-1   Operating State Transition Diagram

4.2 Description of Registers

4.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F008H	Stop code acceptor	STPACP	—	W	8	—
0F009H	Standby control register	SBYCON	—	W	8	00H
0F028H	Block control register 0	BLKCON0	—	R/W	8	00H
0F029H	Block control register 1	BLKCON1	—	R/W	8	00H
0F02AH	Block control register 2	BLKCON2	—	R/W	8	00H
0F02BH	Block control register 3	BLKCON3	—	R/W	8	00H
0F02CH	Block control register 4	BLKCON4	—	R/W	8	00H

4.2.2   Stop Code Acceptor (STPACP)

Address: 0F008H
Access: W
Access size: 8-bit
Initial value:—(Undefined)

	7	6	5	4	3	2	1	0
STPACP	—	—	—	—	—	—	—	—
	W	W	W	W	W	W	W	W
Initial value	-	-	-	-	-	-	-	-

STPACP is a write-only special function register (SFR) that is used for setting a STOP mode.
When STPACP is read, "00H" is read.
When data is written to STPACP in the order of "5nH"(n: an arbitrary value) and "0AnH"(n: an arbitrary value), the stop code acceptor is enabled. When the STP bit of the standby control register (SBYCON) is set to "1" in this state, the mode is changed to the STOP mode. When the STOP mode is set, the STOP code acceptor is disabled.
When another instruction is executed between the instruction that writes "5nH" to STPACP and the instruction that writes "0AnH", the stop code acceptor is enabled after "0AnH" is written. However, if data other than "0AnH" is written to STPACP after "5nH" is written, the "5nH" write processing becomes invalid so that data must be written again starting from "5nH".
During a system reset, the stop code acceptor is disabled.

Note:
   The STOP code acceptor cannot be enabled on the condition of that both any interrupt enable flag and the corresponding interrupt request flag are "1"(An interrupt request occurrence with resetting MIE flag will have the condition).

4.2.3 Standby Control Register (SBYCON)

Address: 0F009H
Access: W
Access size: 8-bit
Initial value: 00H

	7	6	5	4	3	2	1	0
SBYCON	—	—	—	—	—	—	STP	HLT
	W	W	W	W	W	W	W	W
Initial value	0	0	0	0	0	0	0	0

SBYCON is a special function register (SFR) to control operating mode of MCU.

[Description of Bits]

- **STP** (bit 1)
  The STP bit is used for setting the STOP mode. When the STP bit is set to "1" with the stop code adapter enabled by using STPACP, the mode is changed to the STOP mode. When any of the P00 to P03 interrupt requests enabled by the Interrupt Enable Register 1 (IE1) occurs or an external 8 interrupt request enabled by the Interrupt Enable Register 2 (IE2) occurs, the STP becomes "0" and the operation returns to the program run mode.

- **HLT** (bit 0)
  The HALT bit is used for setting a HALT mode. When the HALT bit is set to "1", the mode is changed to the HALT mode. When the WDT interrupt request or enabled (the interrupt enable flag is "1") interrupt request is issued, the HALT bit is set to "1" and the mode is returned to program run mode.

STP	HLT	Description
0	0	Program run mode (initial value)
0	1	HALT Mode
1	0	STOP mode
1	1	Prohibited

Note:
  The mode cannot be changed to HALT mode or STOP mode on the condition of that both any interrupt enable flag and the corresponding interrupt request flag are "1"(An interrupt request occurrence with resetting MIE flag will have the condition).
  When a maskable interrupt source (interrupt with enable bit) occurs while the MIE flag of the program status word (PSW) in the nX-U8/100 core is "0", the STOP mode and the HALT mode are simply released and interrupt processing is not performed. For details of PSW, see "nX-U8/100 Core Instruction Manual".

4.2.4   Block Control Register 0 (BLKCON0)

Address: 0F028H
Access: R/W
Access size: 8-bit
Initial value: 00H

	7	6	5	4	3	2	1	0
BLKCON0	—	—	—	—	DTM3	DTM2	—	—
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

BLKCON0 is a special function register (SFR) to control each block operation.

[Description of Bits]

- **DTM2** (bit 2)
  The DTM2 bit is used to control Timer 2 operation.

DTM2	Description
0	Enable operating Timer 2 (initial value)
1	Disable operating Timer 2

- **DTM3** (bit 3)
  The DTM3 bit is used to control Timer 3 operation.

DTM3	Description
0	Enable operating Timer 3 (initial value)
1	Disable operating Timer 3

Note:
•When any flag is set to "1" (disable operation), the function of the applicable block is reset (all registers are initialized) and the clock supply to such block stops. When this flag is set to "1", the writing to all registers in the applicable block becomes invalid, and thus the reading from such register becomes the initial value. When using the function of the applicable block, ensure to reset the applicable flag of this block control register to "0" (enable operation).
•See Chapter 9, "Timers" for detail about operation of Timer 0, Timer 1, Timer 2 and Timer 3.

4.2.5   Block Control Register 1 (BLKCON1)

Address: 0F029H
Access: R/W
Access size: 8-bit
Initial value: 00H

	7	6	5	4	3	2	1	0
BLKCON1	—	DCAPR	—	—	—	—	—	—
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

BLKCON1 is a special function register (SFR) to control each block operation.

[Description of Bits]

- **DCAPR** (bit 6)
  The DCAPR bit is used to control Capture operation.

DCAPR	Description
0	Enable operating Capture (initial value)
1	Disable operating Capture

Note:
•When any flag is set to "1" (disable operation), the function of the applicable block is reset (all registers are initialized) and the clock supply to such block stops. When this flag is set to "1", the writing to all registers in the applicable block becomes invalid, and thus the reading from such register becomes the initial value. When using the function of the applicable block, ensure to reset the applicable flag of this block control register to "0" (enable operation).
•See Chapter 8, "Capture" for detail about operation of Capture.

4.2.6   Block Control Register 2 (BLKCON2)

Address: 0F02AH
Access: R/W
Access size: 8-bit
Initial value: 00H

	7	6	5	4	3	2	1	0
BLKCON2	—	—	—	—	—	DUA0	—	—
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

BLKCON2 is a special function register (SFR) to control each block operation.

[Description of Bits]

- **DUA0** (bit 2)
  The DUA0 bit is used to control UART operation.

DUA0	Description
0	Enable operating UART (initial value)
1	Disable operating UART

Note:
•When any flag is set to "1" (disable operation), the function of the applicable block is reset (all registers are initialized) and the clock supply to such block stops. When this flag is set to "1", the writing to all registers in the applicable block becomes invalid, and thus the reading from such register becomes the initial value. When using the function of the applicable block, ensure to reset the applicable flag of this block control register to "0" (enable operation).
•See Chapter 11, "UART" for detail about operation of UART.

4.2.7   Block Control Register 3 (BLKCON3)

Address: 0F02BH
Access: R/W
Access size: 8-bit
Initial value: 00H

	7	6	5	4	3	2	1	0
BLKCON3	—	—	—	—	—	—	—	DMD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

BLKCON3 is a special function register (SFR) to control each block operation.

[Description of Bits]
- **DMD0** (bit 0)
  The DMD0 bit is used to control the Melody Driver 0 operation.

DMD0	Description
0	Enable operating Melody/Buzzer (initial value)
1	Disable operating Melody/Buzzer

Note:
•When any flag is set to "1" (disable operation), the function of the applicable block is reset (all registers are initialized) and the clock supply to such block stops. When this flag is set to "1", the writing to all registers in the applicable block becomes invalid, and thus the reading from such register becomes the initial value. When using the function of the applicable block, ensure to reset the applicable flag of this block control register to "0" (enable operation).
•See Chapter 18, "Melody Driver" for detail about operation of Melody/Buzzer.

4.2.8   Block Control Register 4 (BLKCON4)

Address: 0F02CH
Access: R/W
Access size: 8-bit
Initial value: 00H

	7	6	5	4	3	2	1	0
BLKCON4	—	DLCD	—	—	—	—	DRAD	—
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

BLKCON4 is a special function register (SFR) to control each block operation.

[Description of Bits]

- **DRAD** (bit 1)
  The DRAD bit is used to control the RC oscillation type A/D converter operation.

DRAD	Description
0	Enable operating RC oscillation type A/D converter (initial value)
1	Disable operating RC oscillation type A/D converter

- **DLCD** (bit 6)
  The DLCD bit is used to control LCD driver operation.

DLCD	Description
0	Enable operating LCD driver (initial value)
1	Disable operating LCD driver

Note:
•When any flag is set to "1" (disable operation), the function of the applicable block is reset (all registers are initialized) and the clock supply to such block stops. When this flag is set to "1", the writing to all registers in the applicable block becomes invalid, and thus the reading from such register becomes the initial value. When using the function of the applicable block, ensure to reset the applicable flag of this block control register to "0" (enable operation).
•See Chapter 20, "LCD Driver" for detail about operation of LCD driver.
•See Chapter 19, "RC Oscillation Type A/D Converter" for detail about operation of RC oscillation type A/D converter.

4.3 Description of Operation

4.3.1   Program Run Mode

The program run mode is the state where the CPU executes instructions sequentially.
At power-on reset, RESET_N pin reset, low-speed oscillation stop detect reset, or WDT overflow reset, the CPU executes instructions from the addresses that are set in addresses 0002H and 0003H of program memory (ROM) after the system reset mode is released.
At reset by the BRK instruction, the CPU executes instructions from the addresses that are set in the addresses 0004H and 0005H of the program memory after the system reset mode is released. However, when the value of the interrupt level bit (ELEVEL) of the program status word (PSW) is 02H or higher at execution of the BRK instruction (after the occurrence of the WDT interrupt), the CPU executes instructions from the addresses that are set in the addresses 0002H and 0003H. For details of the BRK instruction and PSW, see the "nX-U8/100 Core Instruction Manual" and for the reset function, see Chapter 3, "Reset Function".

4.3.2   HALT Mode

The HALT mode is the state where the CPU interrupts execution of instructions and only the peripheral circuits are running.
When the HLT bit of the standby control register (SBYCON) is set to "1", the HALT mode is set.
When a WDT interrupt request, or an interrupt request enabled by an interrupt enable register (IE1–IE7) is issued, the HLT bit is set to "0" on the falling edge of the next system clock (SYSCLK) and the HALT mode is returned to the program run mode released.
Figure 4-2 shows the operation waveforms in HALT mode.
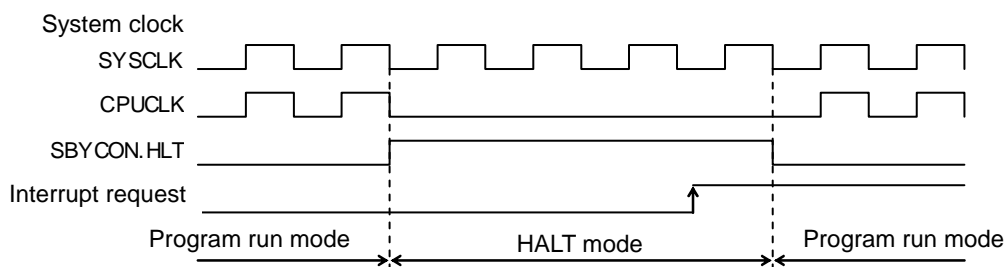
Figure 4-2   Operation Waveforms in HALT Mode

Note:
Since up to two instructions are executed during the period between HALT mode release and a transition to interrupt processing, place two NOP instructions next to the instruction that sets the HLT bit to "1".

4.3.3   STOP mode

The STOP mode is the state where low-speed oscillation and high-speed oscillation stop and the CPU and peripheral circuits stop the operation.

When the stop code acceptor is enabled by writing "5nH"(n: an arbitrary value) and "0AnH"(n: an arbitrary value) to the stop code acceptor (STPACP) sequentially and the STP bit of the standby control register (SBYCON) is set to "1", the STOP mode is entered. When the STOP mode is set, the STOP code acceptor is disabled.

When any of the P00 to P03 interrupt requests or an external 8 interrupt request occurs with the interrupt enabled (the interrupt enable flag is "1"), the STOP mode is released, and the mode is returned to the program run mode.

4.3.3.1 STOP Mode When CPU Operates with Low-Speed Clock

When the stop code acceptor is in the enabled state and the STP bit of SBYCON is set to "1", the STOP mode is entered, stopping low-speed oscillation and high-speed oscillation.

When any of the P00 to P03 interrupt request or an external 8 interrupt request occurs with the interrupt enabled (interrupt enabled flag is "1") state, the STP bit becomes "0" and the low-speed oscillation resumes. If the high-speed clock was oscillating before the STOP mode is entered, the high-speed oscillation restarts. When the high-speed clock was not oscillating before the STOP mode is entered, high-speed oscillation does not start.

When an interrupt request occurs, the STOP mode is released after the elapse of the low-speed oscillation start time (T_{XTL}) and the low-speed clock (LSCLK) oscillation stabilization time (8192-pulse count), the mode is returned to the program run mode, and the low-speed clock (LSCLK) restarts supply to the peripheral circuits. If the high-speed clock already started oscillation at this time, the high-speed clocks (OSCLK and HSCLK) also restart supply to the peripheral circuits.

For the low-speed oscillation start time (T_{XTL}), see Appendix C, "Electrical Characteristics".

Figure 4-3 shows the operation waveforms in STOP mode when CPU operates with the low-speed clock.
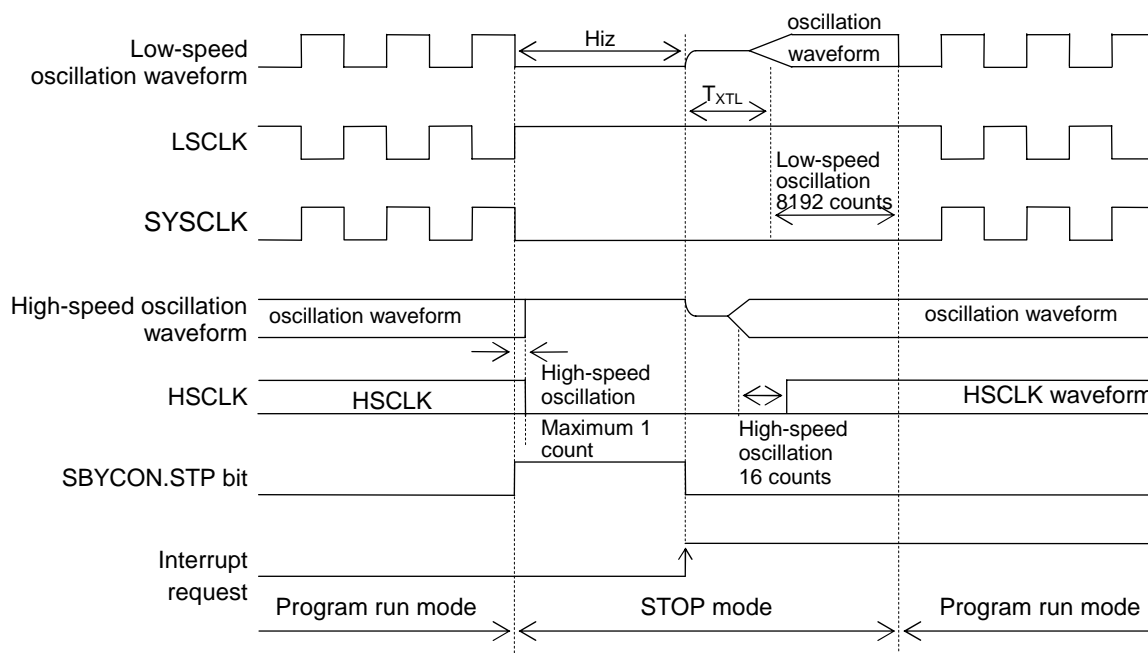
Figure 4-3   Operation Waveforms in STOP Mode When CPU Operates with Low-Speed Clock

4.3.3.2 STOP Mode When CPU Operates with High-Speed Clock

When the CPU is operating with the high-speed clock and the STP bit of SBYCON is set to "1" with the stop code acceptor enabled, the STOP mode is entered and high-speed oscillation and low-speed oscillation stop.

When any of the P00 to P03 interrupt request or an external 8 interrupt request occurs with the interrupt enabled (interrupt enabled flag is "1") state, the STP bit becomes "0" and the high-speed and low-speed oscillation resumes. When an interrupt request is issued, the STOP mode is released after the elapse of the high-speed oscillation start time (T_{RC}) and the high-speed clock (OSCLK) oscillation stabilization time (16-pulse count), the mode is returned to the program run mode, and the high-speed clocks (OSCLK and HSCLK) restart supply to the peripheral circuits.

The low-speed clock (LSCLK) restarts supply to the peripheral circuits after the elapse of the low-speed oscillation start time (T_{XTL}) and low-speed clock (LSCLK) oscillation stabilization time (8192 count).

For the high-speed oscillation start time (T_{XTH}) and low-speed oscillation start time (T_{XTL}), see the "Electrical Characteristics" Section in Appendix C.

Figure 4-4 shows the operation waveforms in STOP mode when CPU operates with the high-speed clock.
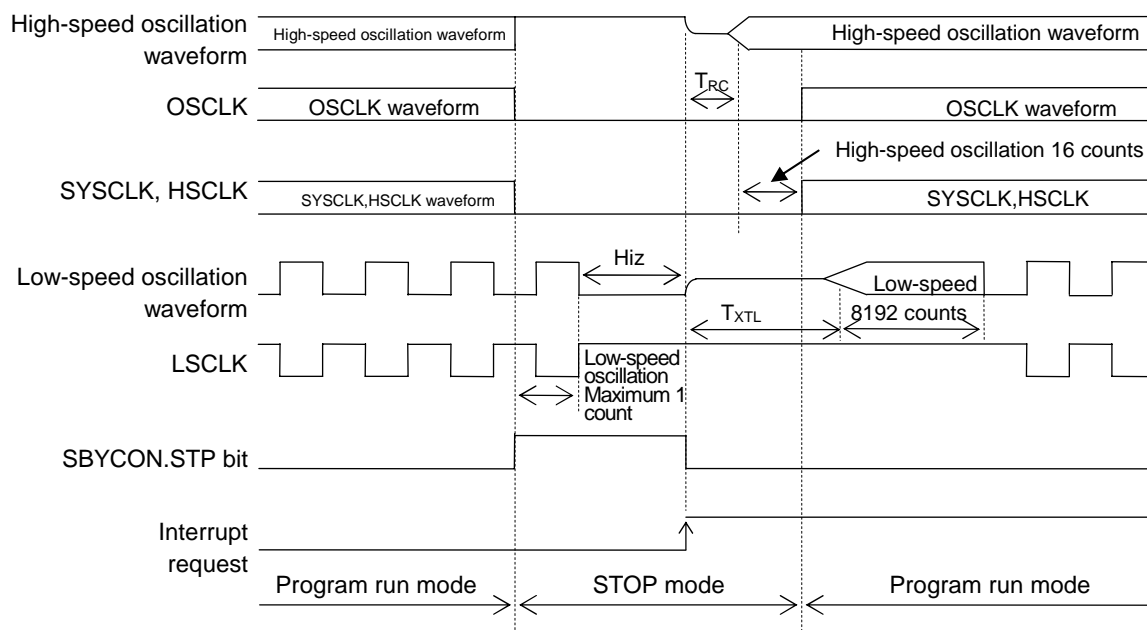
Figure 4-4   Operation Waveforms in STOP Mode When CPU Operates with High-Speed Clock

Note:
   Since up to two instructions are executed during the period between STOP mode release and a transition to interrupt processing, place two NOP instructions next to the instruction that sets the STP bit to "1".

4.3.4   Note on Return Operation from STOP/HALT Mode

The operation of returning from the STOP mode and HALT mode varies according to the interrupt level (ELEVEL) of the program status word (PSW), master interrupt enable flag (MIE), the contents of the interrupt enable register (IE0 to IE3), and whether the interrupt is a non-maskable interrupt or a maskable interrupt.
For details of PSW and the IE and IRQ registers, see "nX-U8/100 Core Instruction Manual" and Chapter 5, "Interrupt", respectively.

Table 4-1 and Table 4-2 show the return operations from STOP/HALT mode.

Table 4-1   Return Operation from STOP/HALT Mode (Non-Maskable Interrupt)

ELEVEL	MIE	IEn.m	IRQn.m	Return operation from STOP/HALT mode
*	*	—	0	Not returned from STOP/HALT mode.
3	*	—	1	After the mode is returned from STOP/HALT mode, the program operation restarts from the instruction following the instruction that sets the STP/HLT bit to "1". The program operation does not go to the interrupt routine.
0,1,2	*	—	1	After the mode is returned from the STOP/HALT mode, program operation restarts from the instruction following the instruction that sets the STP/HLT bit to "1", then goes to the interrupt routine.

Table 4-2   Return Operation from STOP/HALT Mode (Maskable Interrupt)

ELEVEL	MIE	IEn.m	IRQn.m	Return operation from STOP/HALT mode
*	*	*	0	Not returned from STOP/HALT mode.
*	*	0	1	
*	0	1	1	After the mode is returned from STOP/HALT mode, the program operation restarts from the instruction following the instruction that sets the STP/HLT bit to "1". The program operation does not go to the interrupt routine.
2,3	1	1	1	
0,1	1	1	1	After the mode is returned from the STOP/HALT mode, program operation restarts from the instruction following the instruction that sets the STP/HLT bit to "1", then goes to the interrupt routine.

Note:
   •If the ELEVEL bit is 0H, it indicates that the CPU is performing neither non-maskable interrupt processing nor maskable interrupt processing nor software interrupt processing.
   •If the ELEVEL bit is 1H, it indicates that the CPU is performing maskable interrupt processing or software interrupt processing. (ELEVEL is set during interrupt transition cycle.)
   •If the ELEVEL bit is 2H, it indicates that the CPU is performing non-maskable interrupt processing. (ELEVEL is set during interrupt transition cycle.)
   •If the ELEVEL bit is 3H, it indicates that the CPU is performing interrupt processing specific to the emulator. This setting is not allowed in normal applications.

4.3.5   Block Control Function

This LSI has a block control function, which resets and completely turns operating circuits of unused peripherals off to make even more reducing current consumption.

For each block control register, the initial value of each flag is "0", meaning the operation of each block is enabled. When any flag is set to "1" (Disable Operating), the function of the applicable block is reset and the clock supply to this block is stopped. When this flag is set to "1", the writing to all registers in the applicable block becomes invalid, and thus the reading from such register becomes the initial value. When using the function of the applicable block, ensure to reset the applicable flag of this block control register to "0" (enable operation).

・   BLKCON0 register: Controls (enables/disables) the operation of the Timers 2 and 3 circuits.
・   BLKCON1 register: Controls (enables/disables) the operation of the capture circuits.
・   BLKCON2 register: Controls (enables/disables) the operation of the UART0 circuits.
・   BLKCON3 register: Controls (disables/enables) the operation of the melody driver 0 circuit.
・   BLKCON4 register: Controls (disables/enables) the operation of the LCD driver and RC oscillation type A/D converter circuits.

Interrupts

5.   Interrupts

5.1 Overview

This LSI has 15 interrupt sources (External interrupts: 5 sources, Internal interrupts: 10 sources) and a software interrupt (SWI).
For details of each interrupt, see the following chapters:
Chapter 7, "Time Base Counter"
Chapter 9, "Timer"
Chapter 10, "Watchdog Timer"
Chapter 11, "UART"
Chapter 12, "Port 0"
Chapter 16, "Port 5"
Chapter 18, "Melody Driver"
Chapter 19, "RC Oscillation Type A/D Converter"

5.1.1   Features

- Non-maskable interrupt source: 1 (Internal sources: 1)
- Maskable interrupt sources: 14 (Internal sources: 9, External sources: 5)
- Software interrupt (SWI): maximum 64 sources
- External interrupts allow edge selection and sampling selection

5.2 Description of Registers

5.2.1   List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F011H	Interrupt enable register 1	IE1	—	R/W	8	00H
0F012H	Interrupt enable register 2	IE2	—	R/W	8	00H
0F014H	Interrupt enable register 4	IE4	—	R/W	8	00H
0F015H	Interrupt enable register 5	IE5	—	R/W	8	00H
0F016H	Interrupt enable register 6	IE6	—	R/W	8	00H
0F017H	Interrupt enable register 7	IE7	—	R/W	8	00H
0F018H	Interrupt request register 0	IRQ0	—	R/W	8	00H
0F019H	Interrupt request register 1	IRQ1	—	R/W	8	00H
0F01AH	Interrupt request register 2	IRQ2	—	R/W	8	00H
0F01CH	Interrupt request register 4	IRQ4	—	R/W	8	00H
0F01DH	Interrupt request register 5	IRQ5	—	R/W	8	00H
0F01EH	Interrupt request register 6	IRQ6	—	R/W	8	00H
0F01FH	Interrupt request register 7	IRQ7	—	R/W	8	00H

5.2.2   Interrupt Enable Register 1 (IE1)

Address: 0F011H
Access: R/W
Access size: 8-bit
Initial value: 00H

	7	6	5	4	3	2	1	0
IE1	—	—	—	—	EP03	EP02	EP01	EP00
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

IE1 is a special function register (SFR) to control enable/disable for each interrupt request.
When an interrupt is accepted, the master interrupt enable flag (MIE) is set to "0", but the corresponding flag of IE1 is not reset.

[Description of Bits]

- **EP00** (bit 0)
  EP00 is the enable flag for the input port P00 pin interrupt (P00INT).

EP00	Description
0	Disabled (initial value)
1	Enabled

- **EP01** (bit 1)
  EP01 is the enable flag for the input port P01 pin interrupt (P01INT).

EP01	Description
0	Disabled (initial value)
1	Enabled

- **EP02** (bit 2)
  EP02 is the enable flag for the input port P02 pin interrupt (P02INT).

EP02	Description
0	Disabled (initial value)
1	Enabled

- **EP03** (bit 3)
  EP03 is the enable flag for the input port P03 pin interrupt (P03INT).

EP03	Description
0	Disabled (initial value)
1	Enabled

5.2.3   Interrupt Enable Register 2 (IE2)

Address: 0F012H
Access: R/W
Access size: 8-bit
Initial value: 00H

	7	6	5	4	3	2	1	0
IE2	—	—	—	—	EP5	—	—	—
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

IE2 is a special function register (SFR) to control enable/disable for each interrupt request.
When an interrupt is accepted, the master interrupt enable flag (MIE) is set to "0", but the corresponding flag of IE2 is not reset.

[Description of Bits]
- **EP5** (bit 5)
  EP5 is the enable flag for the external 8 interrupt (P5INT).

EP5	Description
0	Disabled (initial value)
1	Enabled

5.2.4　Interrupt Enable Register 4 (IE4)

Address: 0F014H
Access: R/W
Access size: 8-bit
Initial value: 00H

	7	6	5	4	3	2	1	0
IE4	—	—	ERAD	—	—	EMD0	—	EUA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

IE4 is a special function register (SFR) to control enable/disable for each interrupt request.
When an interrupt is accepted, the master interrupt enable flag (MIE) is set to "0", but the corresponding flag of IE4 is not reset.

[Description of Bits]

- **EUA0** (bit 0)
  EUA0 is the enable flag for the UART0 interrupt (UA0INT).

EUA0	Description
0	Disabled (initial value)
1	Enabled

- **EMD0** (bit 2)
  EMD0 is the enable flag for the melody 0 interrupt (MD0INT).

EMD0	Description
0	Disabled (initial value)
1	Enabled

- **ERAD** (bit 5)
  ERAD is the enable flag for the RC oscillation type A/D converter interrupt (RADINT).

ERA0	Description
0	Disabled (initial value)
1	Enabled

5.2.5   Interrupt Enable Register 5 (IE5)

Address: 0F015H
Access: R/W
Access size: 8-bit
Initial value: 00H

	7	6	5	4	3	2	1	0
IE5	—	—	ETM3	ETM2	—	—	—	—
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

IE5 is a special function register (SFR) to control enable/disable for each interrupt request.
When an interrupt is accepted, the master interrupt enable flag (MIE) is set to "0", but the corresponding flag of IE5 is not reset.

[Description of Bits]

- **ETM2** (bit 4)
  ETM2 is the enable flag for the timer 2 interrupt (TM2INT).

ETM2	Description
0	Disabled (initial value)
1	Enabled

- **ETM3** (bit 5)
  ETM3 is the enable flag for the timer 3 interrupt (TM3INT).

ETM3	Description
0	Disabled (initial value)
1	Enabled

5.2.6　Interrupt Enable Register 6 (IE6)

Address: 0F016H
Access: R/W
Access size: 8-bit
Initial value: 00H

	7	6	5	4	3	2	1	0
IE6	E32H	—	E128H	—	—	—	—	—
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

IE6 is a special function register (SFR) to control enable/disable for each interrupt request.
When an interrupt is accepted, the master interrupt enable flag (MIE) is set to "0", but the corresponding flag of IE6 is not reset.

[Description of Bits]

- **E128H** (bit 5)
  E128H is the enable flag for the time base counter 128 Hz interrupt (T128HINT).

E128H	Description
0	Disabled (initial value)
1	Enabled

- **E32H** (bit 7)
  E32H is the enable flag for the time base counter 32 Hz interrupt (T32HINT).

E32H	Description
0	Disabled (initial value)
1	Enabled

5.2.7   Interrupt Enable Register 7 (IE7)

Address: 0F017H
Access: R/W
Access size: 8-bit
Initial value: 00H

	7	6	5	4	3	2	1	0
IE7	—	—	—	—	E2H	—	—	E16H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

IE7 is a special function register (SFR) to control enable/disable for each interrupt request.
When an interrupt is accepted, the master interrupt enable flag (MIE) is set to "0", but the corresponding flag of IE7 is not reset.

[Description of Bits]
- **E16H** (bit 0)
  E16H is the enable flag for the time base counter 16 Hz interrupt (T16HINT).

E16H	Description
0	Disabled (initial value)
1	Enabled

- **E2H** (bit 3)
  E2H is the enable flag for the time base counter 2 Hz interrupt (T2HINT).

E2H	Description
0	Disabled (initial value)
1	Enabled

5.2.8   Interrupt Request Register 0 (IRQ0)

Address: 0F018H
Access: R/W
Access size: 8-bit
Initial value: 00H

	7	6	5	4	3	2	1	0
IRQ0	—	—	—	—	—	—	—	QWDT
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

IRQ0 is a special function register (SFR) to request an interrupt for each interrupt source.
The watchdog timer interrupt (WDTINT) is a non-maskable interrupt that do not depend on MIE. In this case, an interrupt is requested to the CPU regardless of the value of the Mask Interrupt Enable flag (MIE).
Each IRQ0 request flag is set to "1" regardless of the MIE value when an interrupt is generated. By setting the IRQ0 request flag to "1" by software, an interrupt can be generated.
The corresponding flag of IRQ0 is set to "0" by hardware when the interrupt request is accepted by the CPU.

[Description of Bits]
- **QWDT** (bit 0)
  QWDT is the request flag for the watchdog timer interrupt (WDTINT).

QWDT	Description
0	No request (initial value)
1	Request

Note:
    When an interrupt is generated by the write instruction to the interrupt request register (IRQ0), the interrupt shift cycle starts after the next 1 instruction is executed.

5.2.9　Interrupt Request Register 1 (IRQ1)

Address: 0F019H
Access: R/W
Access size: 8-bit
Initial value: 00H

	7	6	5	4	3	2	1	0
IRQ1	—	—	—	—	QP03	QP02	QP01	QP00
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

IRQ1 is a special function register (SFR) to request an interrupt for each interrupt source.
Each IRQ1 request flag is set to "1" regardless of the IE1 and MIE values when an interrupt is generated. In this case, an interrupt is requested to the CPU when the related flag of the interrupt enable register (IE1) is set to "1" and the master interrupt enable flag (MIE) is set to "1".
By setting the IRQ1 request flag to "1" by software, an interrupt can be generated.
The corresponding flag of IRQ1 is set to "0" by hardware when the interrupt request is accepted by the CPU.

[Description of Bits]

- **QP00** (bit 0)

  QP00 is the request flag for the input port P00 pin interrupt (P00INT).

QP00	Description
0	No request (initial value)
1	Request

- **QP01** (bit 1)

  QP01 is the request flag for the input port P01 pin interrupt (P01INT).

QP01	Description
0	No request (initial value)
1	Request

- **QP02** (bit 2)

  QP02 is the request flag for the input port P02 pin interrupt (P02INT).

QP02	Description
0	No request (initial value)
1	Request

- **QP03** (bit 3)

  QP03 is the request flag for the input port P03 pin interrupt (P03INT).

QP03	Description
0	No request (initial value)
1	Request

Note:
　When an interrupt is generated by the write instruction to the interrupt request register (IRQ1) or to the interrupt enable register (IE1), the interrupt shift cycle starts after the next 1 instruction is executed.

5.2.10　Interrupt Request Register 2 (IRQ2)

Address: 0F01AH
Access: R/W
Access size: 8-bit
Initial value: 00H

	7	6	5	4	3	2	1	0
IRQ2	—	—	—	—	QP5	—	—	—
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

IRQ2 is a special function register (SFR) to request an interrupt for each interrupt source.
Each IRQ2 request flag is set to "1" regardless of the IE2 and MIE values when an interrupt is generated. In this case, an interrupt is requested to the CPU when the related flag of the interrupt enable register (IE2) is set to "1" and the master interrupt enable flag (MIE) is set to "1".
By setting the IRQ2 request flag to "1" by software, an interrupt can be generated.
The corresponding flag of IRQ2 is set to "0" by hardware when the interrupt request is accepted by the CPU.

[Description of Bits]
- **QP5** (bit 3)
  QP5 is the request flag for the external 8 interrupt (P5INT).

QP5	Description
0	No request (initial value)
1	Request

Note:
　When an interrupt is generated by the write instruction to the interrupt request register (IRQ2) or to the interrupt enable register (IE2), the interrupt shift cycle starts after the next 1 instruction is executed.

5.2.11 Interrupt Request Register 4 (IRQ4)

Address: 0F01CH
Access: R/W
Access size: 8-bit
Initial value: 00H

	7	6	5	4	3	2	1	0
IRQ4	—	—	QRAD	—	—	QMD0	—	QUA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

IRQ4 is a special function register (SFR) to request an interrupt for each interrupt source.
Each IRQ4 request flag is set to "1" regardless of the IE4 and MIE values when an interrupt is generated. In this case, an interrupt is requested to the CPU when the related flag of the interrupt enable register (IE4) is set to "1" and the master interrupt enable flag (MIE) is set to "1".
By setting the IRQ4 request flag to "1" by software, an interrupt can be generated.
The corresponding flag of IRQ4 is set to "0" by hardware when the interrupt request is accepted by the CPU.

[Description of Bits]

- **QUA0** (bit 0)
  QUA0 is the request flag for the UART0 interrupt (UA0INT).

QUA0	Description
0	No request (initial value)
1	Request

- **QMD0** (bit 2)
  QMD0 is the request flag for the melody 0 interrupt (MD0INT).

QMD0	Description
0	No request (initial value)
1	Request

- **QRA0** (bit 5)
  QRA0 is the request flag for the RC oscillation type A/D converter interrupt (RADINT).

QRA0	Description
0	No request (initial value)
1	Request

Note:
When an interrupt is generated by the write instruction to the interrupt request register (IRQ4) or to the interrupt enable register (IE4), the interrupt shift cycle starts after the next 1 instruction is executed.

5.2.12 Interrupt Request Register 5 (IRQ5)

Address: 0F01DH
Access: R/W
Access size: 8-bit
Initial value: 00H

	7	6	5	4	3	2	1	0
IRQ5	—	—	QTM3	QTM2	—	—	—	—
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

IRQ5 is a special function register (SFR) to request an interrupt for each interrupt source.
Each IRQ5 request flag is set to "1" regardless of the IE5 and MIE values when an interrupt is generated. In this case, an interrupt is requested to the CPU when the related flag of the interrupt enable register (IE5) is set to "1" and the master interrupt enable flag (MIE) is set to "1".
By setting the IRQ5 request flag to "1" by software, an interrupt can be generated.
The corresponding flag of IRQ5 is set to "0" by hardware when the interrupt request is accepted by the CPU.

[Description of Bits]
- **QTM2** (bit 4)
   QTM2 is the request flag for the timer 2 interrupt (TM2INT).

QTM2	Description
0	No request (initial value)
1	Request

- **QTM3 (bit 5)**
   QTM3 is the request flag for the timer 3 interrupt (TM3INT).

QTM3	Description
0	No request (initial value)
1	Request

Note:
   When an interrupt is generated by the write instruction to the interrupt request register (IRQ5) or to the interrupt enable register (IE5), the interrupt shift cycle starts after the next 1 instruction is executed.

5.2.13　Interrupt Request Register 6 (IRQ6)

Address: 0F01EH
Access: R/W
Access size: 8-bit
Initial value: 00H

	7	6	5	4	3	2	1	0
IRQ6	Q32H	—	Q128H	—	—	—	—	—
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

IRQ6 is a special function register (SFR) to request an interrupt for each interrupt source.
Each IRQ6 request flag is set to "1" regardless of the IE6 and MIE values when an interrupt is generated. In this case, an interrupt is requested to the CPU when the related flag of the interrupt enable register (IE6) is set to "1" and the master interrupt enable flag (MIE) is set to "1".
By setting the IRQ6 request flag to "1" by software, an interrupt can be generated.
The corresponding flag of IRQ6 is set to "0" by hardware when the interrupt request is accepted by the CPU.

[Description of Bits]
- **Q128H** (bit 5)
   Q128H is the request flag for the time base counter 128 Hz interrupt (T128HINT).

Q128H	Description
0	No request (initial value)
1	Request

- **Q32H** (bit 7)
   Q32H is the request flag for the time base counter 32 Hz interrupt (T32HINT).

Q32H	Description
0	No request (initial value)
1	Request

Note:
　When an interrupt is generated by the write instruction to the interrupt request register (IRQ6) or to the interrupt enable register (IE6), the interrupt shift cycle starts after the next 1 instruction is executed.

5.2.14 Interrupt Request Register 7 (IRQ7)

Address: 0F01FH
Access: R/W
Access size: 8-bit
Initial value: 00H

	7	6	5	4	3	2	1	0
IRQ7	—	—	—	—	Q2H	—	—	Q16H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

IRQ7 is a special function register (SFR) to request an interrupt for each interrupt source.
Each IRQ7 request flag is set to "1" regardless of the IE7 and MIE values when an interrupt is generated. In this case, an interrupt is requested to the CPU when the related flag of the interrupt enable register (IE7) is set to "1" and the master interrupt enable flag (MIE) is set to "1".
By setting the IRQ7 request flag to "1" by software, an interrupt can be generated.
The corresponding flag of IRQ7 is set to "0" by hardware when the interrupt request is accepted by the CPU.

[Description of Bits]
- **Q16H** (bit 0)
   Q16H is the request flag for the time base counter 8 Hz interrupt (T8HINT).

Q16H	Description
0	No request (initial value)
1	Request

- **Q2H** (bit 3)
   Q2H is the request flag for the time base counter 2 Hz interrupt (T2HINT).

Q2H	Description
0	No request (initial value)
1	Request

Note:
   When an interrupt is generated by the write instruction to the interrupt request register (IRQ7) or to the interrupt enable register (IE7), the interrupt shift cycle starts after the next 1 instruction is executed.

5.3 Description of Operation

With the exception of the watchdog timer interrupt (WDTINT), interrupt enable/disable for 14 sources is controlled by the master interrupt enable flag (MIE) and the individual interrupt enable registers (IE1 to 7). WDTINT is a non-maskable interrupt.

When the interrupt conditions are satisfied, the CPU calls a branching destination address from the vector table determined for each interrupt source and the interrupt shift cycle starts to branch to the interrupt processing routine. Table 5-1 lists the interrupt sources.

Table 5-1   Interrupt Sources

Priority	Interrupt source	Symbol	Vector table address
1	Watchdog timer interrupt	WDTINT	0008H
2	P00 interrupt	P00INT	0010H
3	P01 interrupt	P01INT	0012H
4	P02 interrupt	P02INT	0014H
5	P03 interrupt	P03INT	0016H
6	External 8 interrupt	P5INT	0026H
7	UART 0 interrupt	UA0INT	0040H
8	Melody 0 interrupt	MD0INT	0044H
9	RC oscillation type A/D converter interrupt	RADINT	004AH
10	Timer 2 interrupt	TM2INT	0058H
11	Timer 3 interrupt	TM3INT	005AH
12	TBC128Hz interrupt	T128HINT	006AH
13	TBC32Hz interrupt	T32HINT	006EH
14	TBC16Hz interrupt	T16HINT	0070H
15	TBC2Hz interrupt	T2HINT	0076H

Note:
- When multiple interrupts are generated concurrently, the interrupts are serviced according to this priority and processing of low-priority interrupts is pending.
- Please define vector tables for all unused interrupts for fail safe.

5.3.1　Maskable Interrupt Processing

When an interrupt is generated with the MIE flag set to "1", the following processing is executed by hardware and the processing of program shifts to the interrupt destination.

(1)　Transfer the program counter (PC) to ELR1
(2)　Transfer CSR to ECSR1
(3)　Transfer PSW to EPSW1
(4)　Set the MIE flag to "0"
(5)　Set the ELEVEL field to "1"
(6)　Load the interrupt start address into PC

5.3.2　Non-Maskable Interrupt Processing

When an interrupt is generated regardless of the state of MIE flag, the following processing is performed by hardware and the processing of program shifts to the interrupt destination.

(1)　Transfer PC to ELR2
(2)　Transfer CSR to ECSR2
(3)　Transfer PSW to EPSW2
(4)　Set the ELEVEL field to "2"
(5)　Load the interrupt start address into PC

5.3.3　Software Interrupt Processing

A software interrupt is generated as required within an application program. When the SWI instruction is performed within the program, a software interrupt is generated, the following processing is performed by hardware, and the processing program shifts to the interrupt destination. The vector table is specified by the SWI instruction.

(1)　Transfer PC to ELR1
(2)　Transfer CSR to ECSR1
(3)　Transfer PSW to EPSW1
(4)　Set the MIE flag to "0"
(5)　Set the ELEVEL field to "1"
(6)　Load the interrupt start address into PC

Reference:
For the MIE flag, Program Counter (PC), CSR, PSW, and ELEVEL, see "nX-U8/100 Core Instruction Manual".

5.3.4 Notes on Interrupt Routine

Notes are different in programming depending on whether a subroutine is called or not by the program in executing an interrupt routine, whether multiple interrupts are enabled or disabled, and whether such interrupts are maskable or non-maskable.

Status A: Maskable interrupt is being processed

A-1: When a subroutine is not called by the program in executing an interrupt routine
   A-1-1: When multiple interrupts are disabled
     •Processing immediately after the start of interrupt routine execution
      No specific notes.
     •Processing at the end of interrupt routine execution
      Specify the RTI instruction to return the contents of the ELR register to the PC and those of the EPSW register to PSW.
   A-1-2: When multiple interrupts are enabled
     •Processing immediately after the start of interrupt routine execution
      Specify "PUSH   ELR, EPSW" to save the interrupt return address and the PSW status in the stack.
     •Processing at the end of interrupt routine execution
      Specify "POP   PC, PSW" instead of the RTI instruction to return the contents of the stack to PC and PSW.

Example of description: Status A-1-1

```
Intrpt_A-1-1;     ; A-1-1 state

 DI               ; Disable interrupt

  :
  :
  :
 RTI              ; Return PC from ELR
                  ; Return PSW form
                  EPSW
                  ; End
```

Example of description: Status A-1-2

```
Intrpt_A-1-2;        ; Start
  PUSH               ; Save ELR and EPSW at
ELR,EPSW             the beginning

  EI                 ; Enable interrupt
  :
  :
  :
  :
  :
  POP   PC,PSW       ; Return PC from the stack
                     ; Return PSW from the stack
                     ; End
```

A-2: When a subroutine is called by the program in executing an interrupt routine
  A-2-1: When multiple interrupts are disabled
    •Processing immediately after the start of interrupt routine execution
      Specify the "PUSH LR" instruction to save the subroutine return address in the stack.
    •Processing at the end of interrupt routine execution
      Specify "POP LR" immediately before the RTI instruction to return from the interrupt processing after returning the subroutine return address to LR.
  A-2-2: When multiple interrupts are enabled
    •Processing immediately after the start of interrupt routine execution
      Specify "PUSH   LR, ELR, EPSW" to save the interrupt return address, the subroutine return address, and the EPSW status in the stack.
    •Processing at the end of interrupt routine execution
      Specify "POP PC, PSW, LR" instead of the RTI instruction to return the saved data of the interrupt return address to PC, the saved data of EPSW to PSW, and the saved data of LR to LR.

Example of description: Status A-2-2

```
Intrpt_A-2-2;              ; Start
  PUSH                    ; Save ELR, EPSW, and LR
ELR,EPSW,LR               at the beginning


  EI                      ; Enable interrupt
  :
  :
  :


  BL Sub_1                ; Call subroutine Sub_1
  :
  POP   PC,PSW,LR         ; Return PC from the stack
                          ; Return PSW from the stack
                          ; Return LR from the stack
                          ; End
```

```
Sub_1;          ;
DI              ; Disable interrupt
 :
 :
 :
RT              ; Return PC from LR
                ; End of subroutine
```
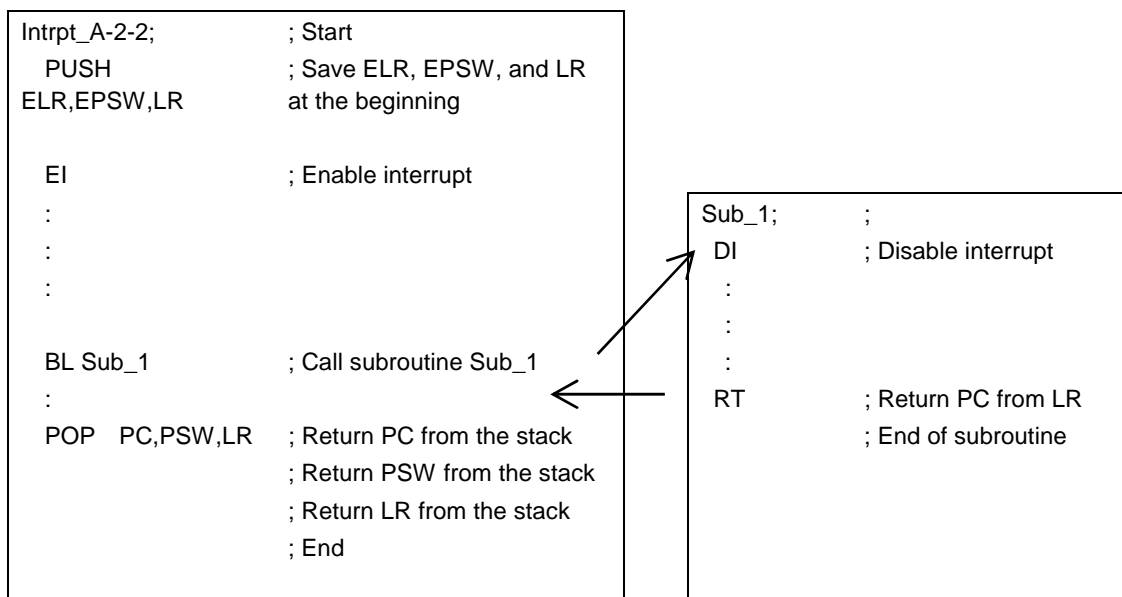
Status B: Non-maskable interrupt is being processed

B-1: When a subroutine is not called in an interrupt routine
   •Processing immediately after the start of interrupt routine execution
      Specify "PUSH   ELR, EPSW" to save the interrupt return address and the PSW status in the stack.
   •Interrupt routine execution end processing
      Specify "POP PSW, PC" to return the contents of the stack to PC and PSW.

   Example of description: Status B-1

Intrpt_B-1:	; Start the interrupt routine
PUSH ELR,EPSW	; Save ELR and EPSW at the beginning
:	
:	
POP PSW,PC	; Return PC from the stack
	; Return PSW from the stack
	; Return LR from the stack
	; End the interrupt routine

B-2: When a subroutine is called in an interrupt routine
   •IProcessing immediately after the start of interrupt routine
      Specify "PUSH   ELR, LR, EPSW" to save the interrupt return address, the subroutine return address, and the EPSW status in the stack.
   •Interrupt routine end processing
      Specify "POP PSW, PC, LR" to return the saved data of the interrupt return address to PC, the saved data of EPSW to PSW, and the saved data of LR to LR.

   Example of description: Status B-2

Intrpt_B-2:	; Start			
PUSH ELR,EPSW,LR	; Save ELR, EPSW, and LR at the beginning			
:			Sub_1:	;
:			:	
BL Sub_1	; Call subroutine Sub_1		:	
:			RT	; Return PC from LR
POP PSW,PC,LR	; Return PC from the stack			; End of subroutine
	; Return PSW from the stack			
	; Return LR from the stack			
	; End			
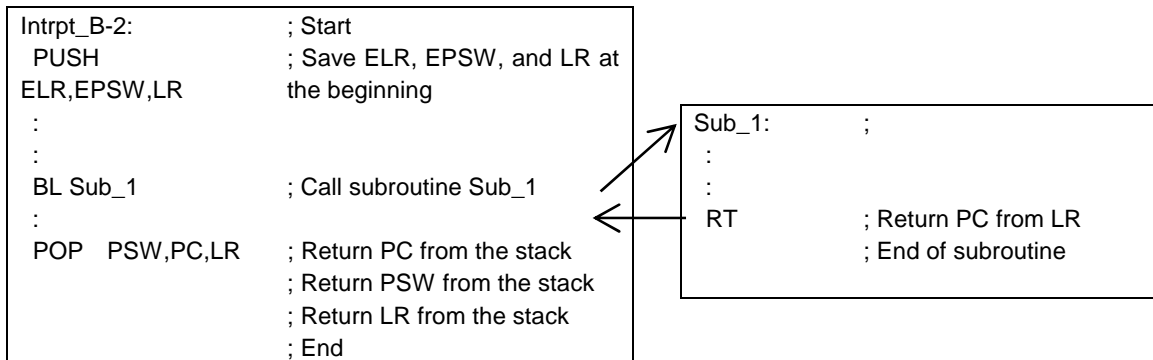
5.3.5   Interrupt Disable State

Even if the interrupt conditions are satisfied, an interrupt may not be accepted depending on the operating state. This is called an interrupt disabled state. See below for the interrupt disabled state and the handling of interrupts in this state.

Interrupt disabled state 1:Between the interrupt shift cycle and the instruction at the beginning of the interrupt routine
When the interrupt conditions are satisfied in this section, an interrupt is generated immediately following the execution of the instruction at the beginning of the interrupt routine corresponding to the interrupt that has already been enabled.

Interrupt disabled state 2:Between the DSR prefix instruction and the next instruction
When the interrupt conditions are satisfied in this section, an interrupt is generated immediately after execution of the instruction following the DSR prefix instruction.

For the DSR prefix instruction, see "nX-U8/100 Core Instruction Manual".

Clock Generation Circuit

6.   Clock Generation Circuit

6.1 Overview

The clock generation circuit generates and provides a low-speed clock (LSCLK), the low-speed double clock (LSCLK x 2), a high-speed clock (HSCLK), a system clock (SYSCLK), and a high-speed output clock (OUTCLK). LSCLK, LSCLK x 2, and HSCLK are time base clocks for the peripheral circuits, SYSCLK is a basic operation clock of CPU, and OUTCLK is a clock that is output from a port.
For the OUTCLK output port, see Chapter 13, "Port 2".
For the STOP mode described in this chapter, see Chapter 4, "MCU Control Function."

6.1.1   Features

- Low-Speed Clock Generation Circuit:
  - 32.768kHz crystal oscillation
  - Capable of using the 32.768kHz double clock LSCLK x 2 (64kHz) for some peripherals
- High-speed clock generation circuit
  - 500kHz RC oscillation

6.1.2   Configuration

Figure 6-1 shows the configuration of the clock generation circuit.

FCON0 : Frequency control register 0
FCON1 : Frequency control register 1
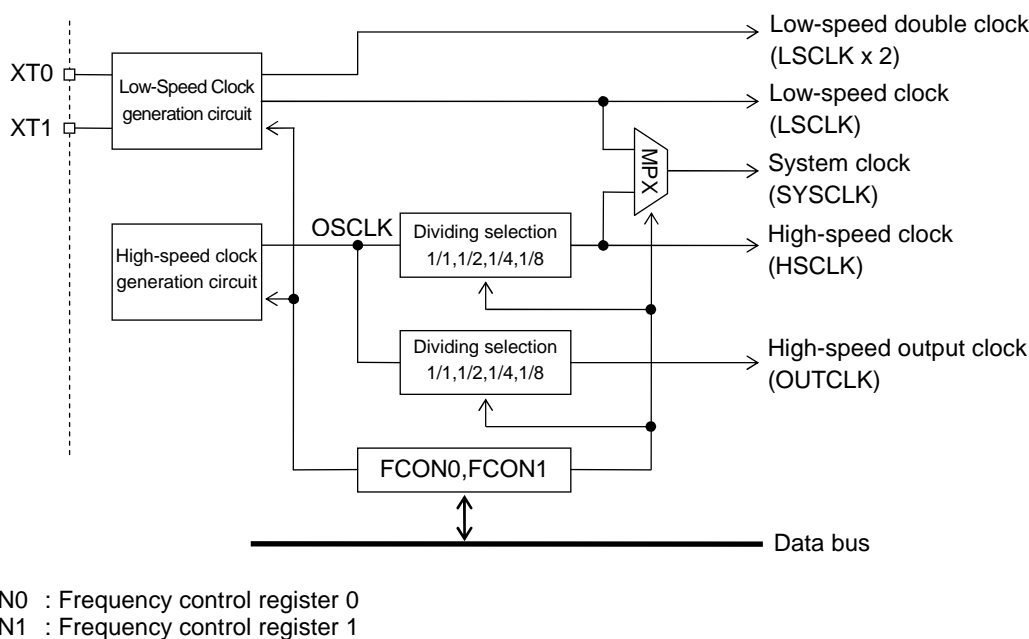
Figure 6-1   Configuration of Clock Generation Circuit

Note:
This LSI starts operation with the low-speed clock after power-on or a system reset. At initialization by software, set the FCON0 or FCON1 register to switch the clock to a required one. Operation of this LSI is not guaranteed under a condition where a low-speed clock is not supplied.

6.1.3   List of Pins

Pin name	Input/output	Function
XT0	I	Pin for connecting a crystal for low-speed clock.
XT1	O	Pin for connecting a crystal for low-speed clock.

6.2 Description of Registers

6.2.1   List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F002H	Frequency control register 0	FCON0	FCON	R/W	8/16	33H
0F003H	Frequency control register 1	FCON1		R/W	8	00H

6.2.2 Frequency Control Register 0 (FCON0)

Address: 0F002H
Access: R/W
Access size: 8/16 bit
Initial value: 33H

	7	6	5	4	3	2	1	0
FCON0	—	—	OUTC1	OUTC0	—	—	SYSC1	SYSC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	1	1	0	0	1	1

FCON0 is a special function register (SFR) to control the high-speed clock generation circuit and to select system clock.

[Description of Bits]
- **SYSC1, SYSC0** (bits 1, 0)
  The SYSC1 and SYSC0 bits are used to select the frequency of the high-speed clock (HSCLK) used for system clock and peripheral circuits (including high-speed time base counter). OSCLK, 1/2OSCLK, 1/4OSCLK, or 1/8OSCLK can be selected. The maximum operating frequency guaranteed for the system clock (SYSCLK) of this LSI is 500 kHz.
  At system reset, 1/8OSCLK is selected.

SYSC1	SYSC0	Description
0	0	OSCLK
0	1	1/2OSCLK
1	0	1/4OSCLK
1	1	1/8OSCLK (initial value)

- **OUTC1, OUTC0** (bits 5, 4)
  The OUTC1 and OUTC0 bits are used to select the frequency of the high-speed output clock which is output when the secondary function of the port is used. OSCLK, 1/2OSCLK, 1/4OSCLK, or 1/8OSCLK can be selected.
  At system reset, 1/8OSCLK is selected.

OUTC1	OUTC0	Description
0	0	OSCLK
0	1	1/2OSCLK
1	0	1/4OSCLK
1	1	1/8OSCLK (initial value)

6.2.3 Frequency Control Register 1 (FCON1)

Address: 0F003H
Access: R/W
Access size: 8-bit
Initial value: 00H

	7	6	5	4	3	2	1	0
FCON1	—	—	—	—	—	ENMLT	ENOSC	SYSCLK
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

FCON1 is a special function register (SFR) to control the high-speed clock generation circuit and to select system clock.

[Description of Bits]
- **SYSCLK** (bit 0)
  The SYSCLK bit is used to select system clock. It allows selection of the low-speed clock (LSCLK) or HSCLK (1/nOSCLK: n = 1, 2, 4, 8) selected by using the high-speed clock frequency select bit (SYSC1, 0) of FCON0. When the oscillation of high-speed clock is stopped (ENOSC bit = "0"), the SYSCLK bit is fixed to "0" and the low-speed clock (LSCLK) is selected for system clock.

SYSCLK	Description
0	LSCLK (initial value)
1	HSCLK

- **ENOSC** (bit 1)
  The ENOSC bit is used to select enable/disable of the oscillation of the high-speed clock oscillator circuit.

ENOSC	Description
0	Stops high-speed oscillation (initial value)
1	Enables high-speed oscillation

- **ENMLT** (bit 2)
  The ENMLT bit is used to select enable/disable of the operation of the low-speed double clock (LSCLK x 2).

ENMLT	Description
0	Disables low-speed double clock operation (initial value)
1	Enables low-speed double clock operation

6.3 Description of Operation

6.3.1 Low-Speed Clock

6.3.1.1 Low-Speed Clock Generation Circuit

Figure 6-2 shows the circuit configuration of the low-speed clock generation circuit.
For the low-speed clock generation circuit, externally provide a 32.768kHz crystal oscillator and capacitors (C_{GL} and C_{DL}).
In the STOP mode, Low-speed clock and Low-speed double clock oscillation are stopped.
When the ENMLT bit of FCON1 is set to "1", the low-speed double clock (LSCLK x 2) starts operation.
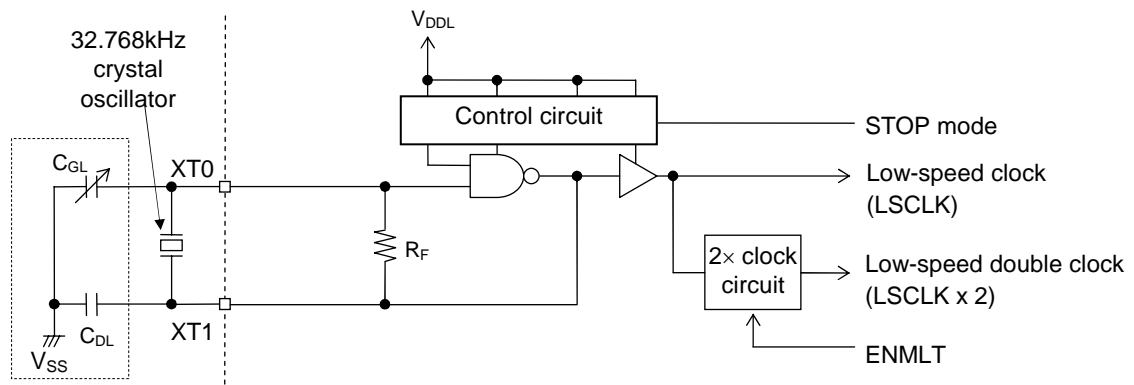
Figure 6-2   Circuit Configuration of 32.768 kHz Crystal Oscillation Mode

Note:
  Install a crystal as close to the LSI as possible and make sure that signals causing noise and power supply wiring are not near the crystal and its wiring.
  Note that oscillation may stop due to condensation.

6.3.1.2 Operation of Low-Speed Clock Generation Circuit

The low-speed clock generation circuit is activated by the occurrence of power ON reset.

After the power-on, it waits for the low-speed oscillation start time (T_{XTL}) and the low-speed clock (LSCLK) oscillation stabilization time (8192 counts). Then, the mode moves to the program run mode, the CPU starts operation, and at the same time the low-speed clock (LSCLK) is supplied to the peripheral circuits.

The low-speed clock generation circuit stops oscillation when it shifts to the STOP mode by software. When oscillation is resumed by releasing of the STOP mode by external interrupt, LSCLK is supplied to the peripheral circuits after the elapse of the low-speed oscillation start period (T_{XTL}) and low-speed clock (LSCLK) oscillation stabilization time (8192 counts). For STOP mode, see Chapter 4, "MCU Control Function".

Figure 6-3 shows the waveforms of the low-speed clock generation circuit. For the low-speed oscillation start time (T_{XTL}), see Appendix C, "Electrical Characteristics".
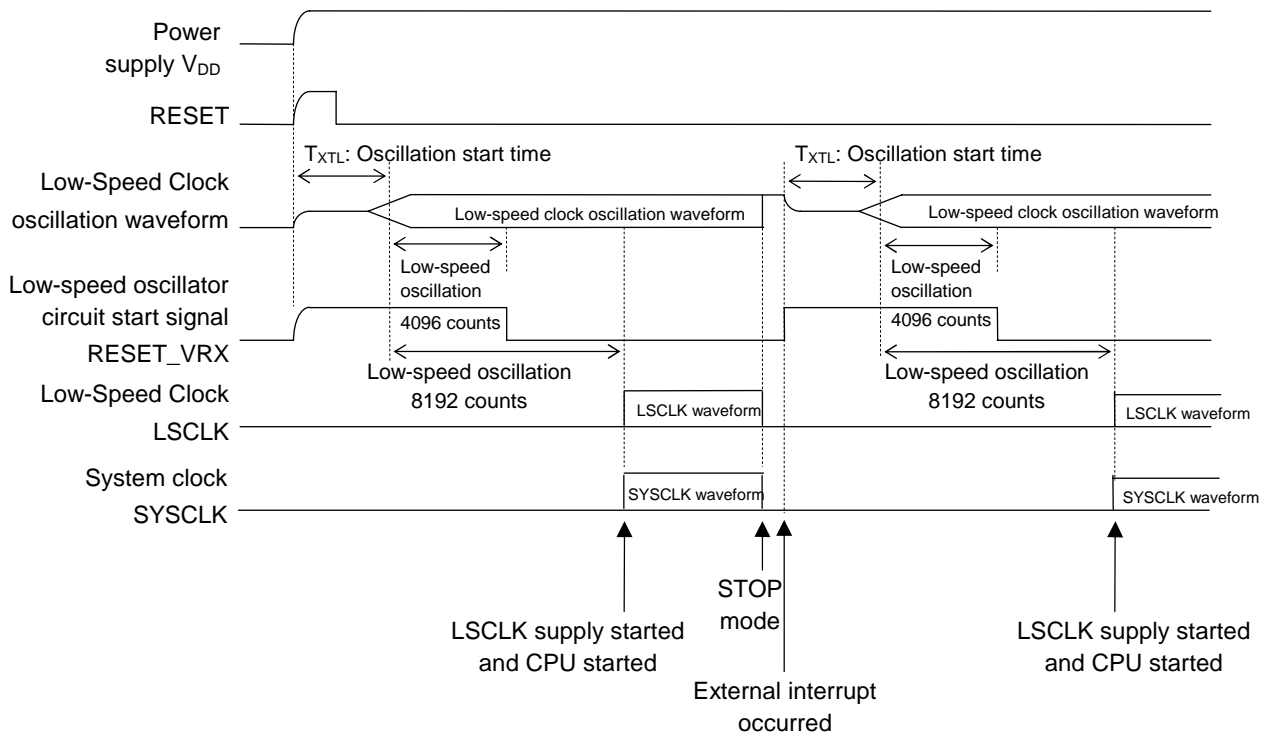
Figure 6-3　Operation of Low-Speed Clock Generation Circuit

Note:

After the power supply is turned on, CPU starts operation with the low-speed clock. After the STOP mode is released, the CPU starts operation with the low-speed clock (SYSCLK bit = "0") or high-speed clock (SYSCLK bit = "1") depending on the FCON1's SYSCLK bit.

6.3.2   High-speed clock

The high-speed clock is supplied from the 500kHz RC oscillator circuit.

6.3.2.1 High-Speed Clock Circuit

After the oscillation is enabled (ENOSC set to "1"), the high-speed clock (OSCLK) supply starts in 16 counts of the RC oscillation clock.
Figure 6-4 shows the high-speed clock circuit configuration.
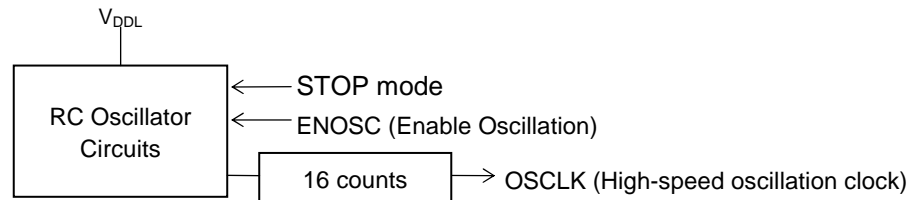
Figure 6-4   High-Speed Clock Circuit Configuration

Note:
•After the system reset mode is cleared, the OSCLK becomes the oscillation stopped state because the initial ENOSC value is "0". In the oscillation enabled (ENOSC set to "1") state, the OSCLK supply starts in 16 counts after the stop mode is released.

6.3.2.2 Operation of High-Speed Clock Generation Circuit

The high-speed clock generation circuit allows the start/stop control of oscillation by using the frequency control registers 0 and 1 (FCON0 and FCON1).

Oscillation can be started by setting the ENOSC bit of FCON1 to "1" after selecting a high-speed oscillation frequency with FCON0. After the start of oscillation, HSCLK starts supply of a clock to the peripheral circuits following the elapse of the high-speed oscillation start period (T_{RC}) and the oscillation stabilization time of the high-speed oscillation clock (OSCLK).

The high-speed clock generation circuit stops oscillation when it shifts to the STOP mode by software. When the STOP mode is released by external interrupt, HSCLK supplies clocks to peripheral circuits following the elapse of the high-speed oscillation start period (T_{RC}) and the oscillation stabilization time of the high-speed clock (OSCLK). The oscillation stabilization time is for 16 clocks.

Figure 6-5 shows the waveforms of the high-speed clock generation circuit.
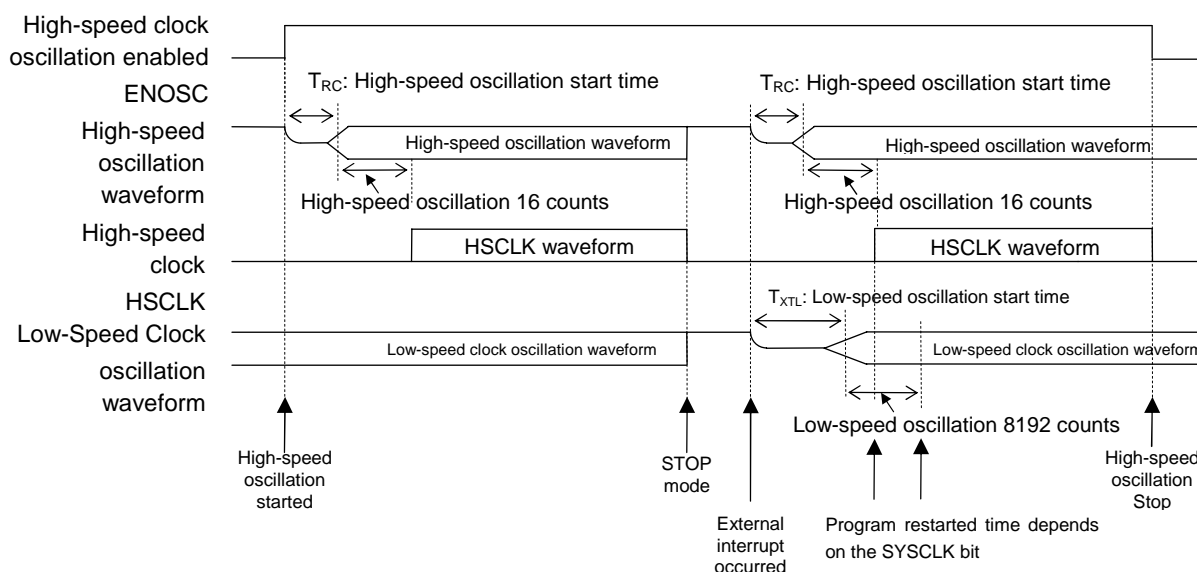
Figure 6-5   Operation of High-Speed Clock Generation Circuit

6.3.3   Switching of System Clock

The system clock can be switched between high-speed clock (HSCLK) and low-speed clock (LSCLK) by using the frequency control registers (FCON0, FCON1).
Figure 6-6 shows the flow chart of system clock switching processing (HSCLK to LSCLK) and Figure 6-7 shows the flow chart of system clock switching processing (LSCLK to HSCLK).
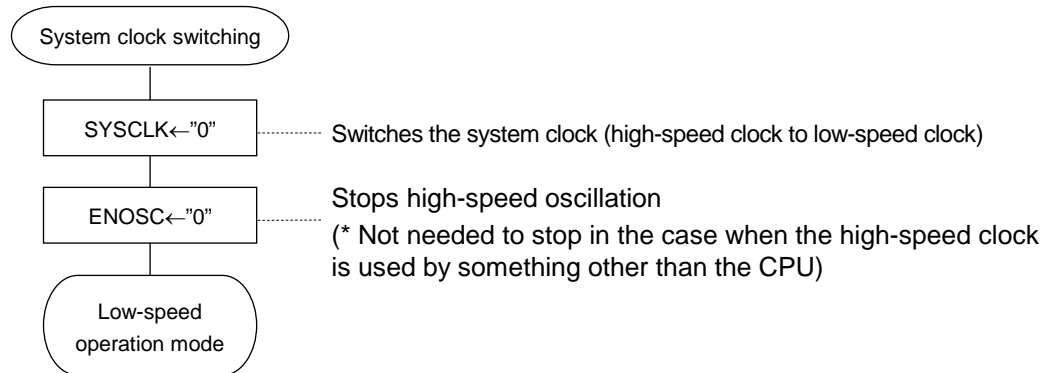
Figure 6-6   Flow of System Clock Switching Processing (HSCLK to LSCLK)

Note:
Immediately after the recovery from the STOP mode, if the system clock is switched from HSCLK to LSCLK, the CPU becomes inactive until LSCLK starts clock supply to the peripheral circuits. Therefore, It is recommended to switch to LSCLK after confirming that the LSCLK is oscillating by checking that the time base counter interrupt request bit (Q128H) is "1".
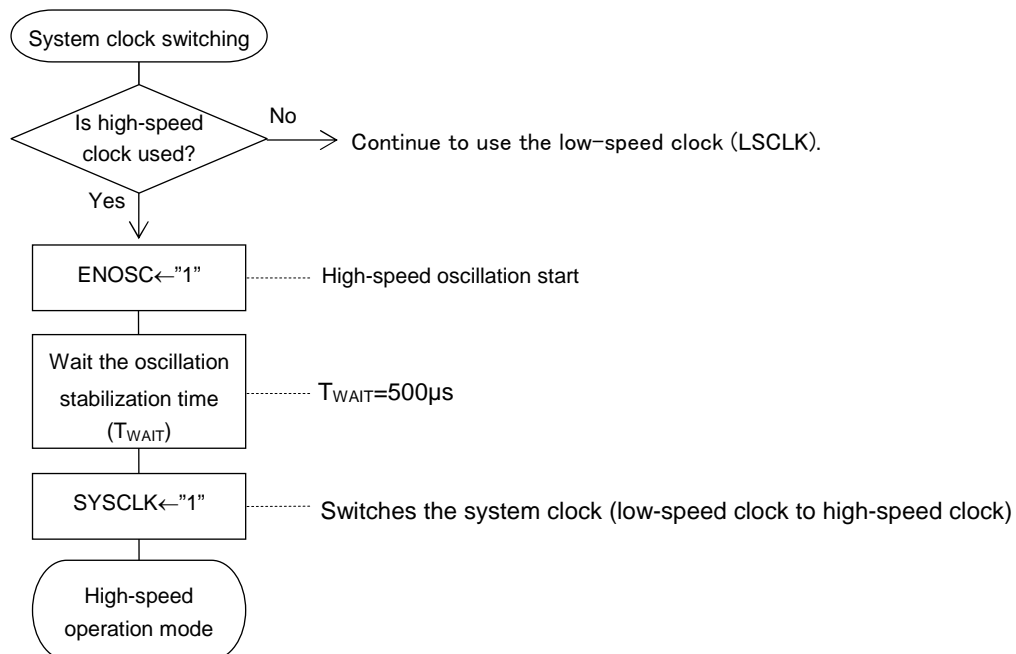
Figure 6-7   Flow of System Clock Switching Processing (LSCLK to HSCLK)

Note:
If the system clock is switched from a low-speed clock to a high-speed clock before the high-speed clock (HSCLK) starts oscillation, the CPU becomes inactive until HSCLK starts clock supply to the peripheral circuits.

6.4 Specifying Port Registers

To enable the clock output function, each related port register bit needs to be set. See Chapter 13, "Port 2" for detail about the port registers.

6.4.1   Functioning P21 (OUTCLK) as the high-speed clock output

Set P21MD bit (P2MOD register bit 1) to "1" for specifying the high-speed clock output as the secondary function of P21.

Register name	P2MOD register (Address: 0F214H)							
Bit	7	6	5	4	3	2	**1**	0
Bit name	-	-	-	-	-	P22MD	**P21MD**	P20MD
Setting value	-	-	-	-	-	*	**1**	*

Set the P21C1 bit (P2CON1 register bit 1) to "1" and the P21C0 bit (P2CON0 register bit 1) to "1" for specifying the state mode of the P21 pin to CMOS output.

Register name	P2CON1 register (Address: 0F213H)							
Bit	7	6	5	4	3	2	**1**	0
Bit name	-	-	-	-	-	P22C1	**P21C1**	P20C1
Setting value	-	-	-	-	-	*	**1**	*

Register name	P2CON0 register (Address: 0F212H)							
Bit	7	6	5	4	3	2	**1**	0
Bit name	-	-	-	-	-	P22C0	**P21C0**	P20C0
Setting value	-	-	-	-	-	*	**1**	*

The P21D bit (P2D register bit 1) data can either be "0" or "1".

Register name	P2D register (Address: 0F210H)							
Bit	7	6	5	4	3	2	**1**	0
Bit name	-	-	-	-	-	P22D	**P21D**	P20D
Setting value	-	-	-	-	-	*	******	*

- : Bit that does not exist
* : Bit not related to the high-speed clock function
** : Don't care

Note:
P21 (Port 2) is an output-only port and does not have the register to select the data direction(input or output).

6.4.2   Functioning P20 (LSCLK) as the low-speed clock output

Set P20MD bit (P2MOD register bit 0) to "1" for specifying the low-speed clock output as the secondary function of P22.

Register name	P2MOD register (Address: 0F214H)							
Bit	7	6	5	4	3	2	1	**0**
Bit name	-	-	-	-	-	P22MD	P21MD	**P20MD**
Setting value	-	-	-	-	-	*	*	**1**

Set the P20C1 bit (P2CON1 register bit 0) to "1" and the P20C0 bit (P2CON0 register bit 0) to "1" for selecting the P20 pin state mode to CMOS output.

Register name	P2CON1 register (Address: 0F213H)							
Bit	7	6	5	4	3	2	1	**0**
Bit name	-	-	-	-	-	P22C1	P21C1	**P20C1**
Setting value	-	-	-	-	-	*	*	**1**

Register name	P2CON0 register (Address: 0F212H)							
Bit	7	6	5	4	3	2	1	**0**
Bit name	-	-	-	-	-	P22C0	P21C0	**P20C0**
Setting value	-	-	-	-	-	*	*	**1**

Data of P20D bit (P2D register bit 0) does not affect to the low speed clock output function, so don't care the data for the function.

Register name	P2D register (Address: 0F210H)							
Bit	7	6	5	4	3	2	1	**0**
Bit name	-	-	-	-	-	P22D	P21D	**P20D**
Setting value	-	-	-	-	-	*	*	******

- : Bit that does not exist
* : Bit not related to the low-speed clock function
** : Don't care

Note:
P20 (Port 2) is an output-only port and does not have the register to select the data direction(input or output).

Time Base Counter

7. Time Base Counter

7.1 Overview

This LSI includes a low-speed time base counter (LTBC) and a high-speed time base counter (HTBC) that generate base clocks for peripheral circuits. By using the time base counter, it is possible to generate events periodically.
For input clocks, see Chapter 6, "Clock Generation Circuit". For interrupt permission, interrupt request flags, etc., described in this chapter, see Chapter 5, "Interrupt".

7.1.1 Features

- LTBC generates T32KHZ to T1HZ signals by dividing the low-speed clock (LSCLK) frequency.
- LTBC allows frequency adjustment (Adjustment range: Approx. -488ppm to +488ppm. Adjustment accuracy: Approx. 0.48ppm) by using the low-speed time base counter frequency adjustment registers (LTBADJH and LTBADJL).
- HTBC generates HTB1 to HTB32 signals by dividing the high-speed clock (HSCLK) frequency.
- Capable of generating 128Hz , 32Hz , 16Hz , and 2Hz interrupts.

7.1.2 Configuration

Figure 7-1 and Figure 7-2 show the configuration of a low-speed time base counter and a high-speed time base counter, respectively.

LTBR　　　: Low-speed time base counter register
LTBADJL　: Low-speed time base counter frequency adjustment register
LTBADJH　: Low-speed time base counter frequency adjustment register
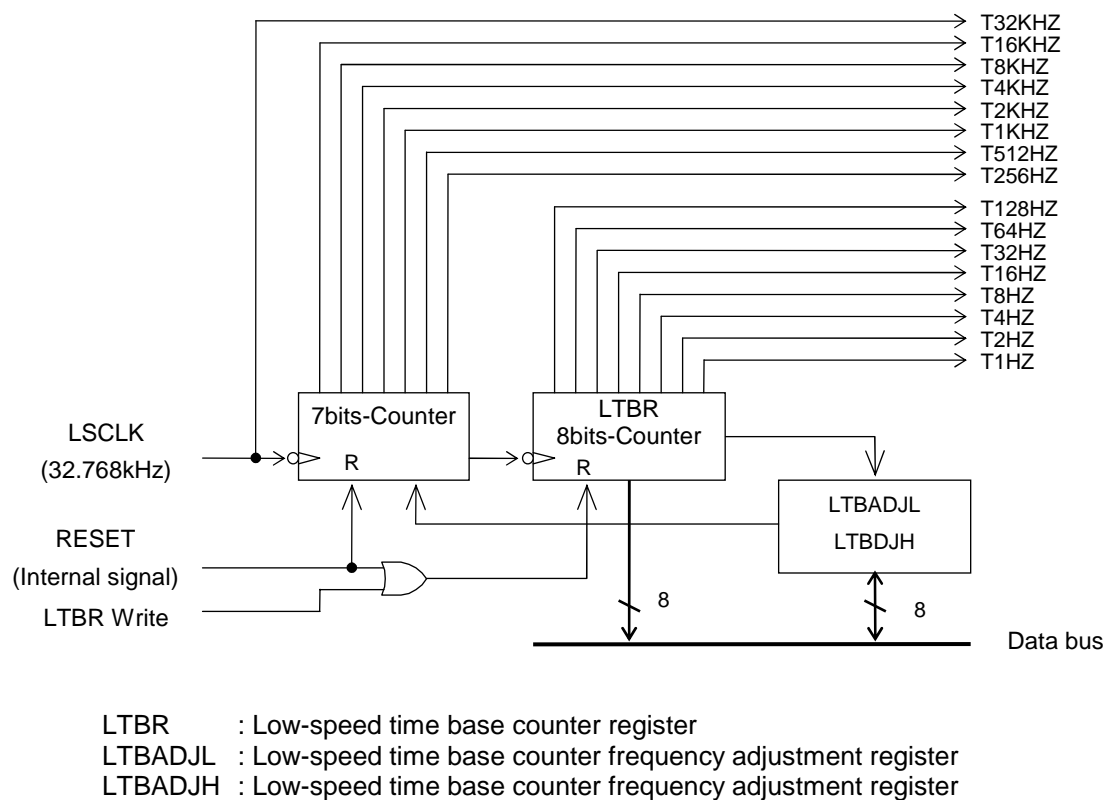
Figure 7-1　Configuration of Low-Speed Time Base Counter (LTBC)
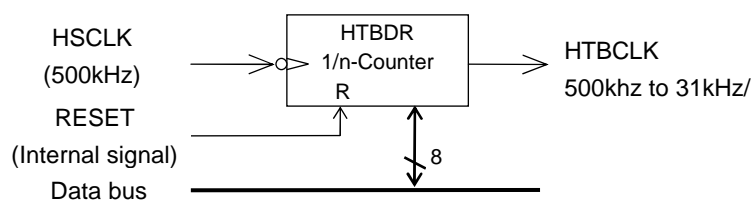
HTBDR : High-speed time base counter frequency divide register

Figure 7-2　Configuration of High-Speed Time Base Counter

Note:
The frequency of HSCLK changes according to specified data in SYSC1 and SYSC0 bits of Frequency control register 0 (FCON0).

7.2 Description of Registers

7.2.1   List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F00AH	Low-speed time base counter register	LTBR	–	R/W	8	00H
0F00BH	High-speed time base counter frequency divide register	HTBDR	–	R/W	8	00H
0F00CH	Low-speed time base counter frequency adjustment register L	LTBADJL	LTBADJ	R/W	8/16	00H
0F00DH	Low-speed time base counter frequency adjustment register H	LTBADJH		R/W	8	00H

7.2.2   Low-Speed Time Base Counter Register (LTBR)

Address: 0F00AH
Access: R/W
Access size: 8-bit
Initial value: 00H

	7	6	5	4	3	2	1	0
LTBR	T1HZ	T2HZ	T4HZ	T8HZ	T16HZ	T32HZ	T64HZ	T128HZ
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

LTBR is a special function register (SFR) to read the T128HZ to T1HZ outputs of the low-speed time base counter. The T128HZ-T1HZ outputs are set to "0" when write operation is performed for LTBR. Write data is invalid.

Note:
A TBC interrupt (128Hz interrupt, 32Hz interrupt, 16Hz interrupt, or 2Hz interrupt) may occur depending on the LTBR write timing. Take this into consideration when programming your software by referring to "Figure 7-4   Interrupt Timing and Reset Timing by Writing to LTBR."

7.2.3 High-Speed Time Base Counter Divide Register (HTBDR)

Address: 0F00BH
Access: R/W
Access size: 8-bit
Initial value: 00H

	7	6	5	4	3	2	1	0
HTBDR	–	–	–	–	HTD3	HTD2	HTD1	HTD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

HTBDR is a special function register (SFR) to set the dividing ratio of the 4-bit, 1/n counter.

[Description of Bits]
- **HTD3-HTD0** (bits 3-0)
  The HTD3-HTD0 bits are used to set the dividing ratio of the 4-bit, 1/n counter. The frequency divide ratios selectable include 1/1 to 1/16.

HTD3	HTD2	HTD1	HTD0	Description	
				Dividing ratio	Frequency of HTBCLK (*1)
0	0	0	0	1/16 (initial value)	31kHz
0	0	0	1	1/15	33kHz
0	0	1	0	1/14	36kHz
0	0	1	1	1/13	38kHz
0	1	0	0	1/12	42kHz
0	1	0	1	1/11	45kHz
0	1	1	0	1/10	50kHz
0	1	1	1	1/9	56kHz
1	0	0	0	1/8	63kHz
1	0	0	1	1/7	71kHz
1	0	1	0	1/6	83kHz
1	0	1	1	1/5	100kHz
1	1	0	0	1/4	125kHz
1	1	0	1	1/3	167kHz
1	1	1	0	1/2	250kHz
1	1	1	1	1/1	500kHz

*1: Indicates the frequency when the high-speed oscillation clock, HSCLK, is 500 kHz.

7.2.4   Low-Speed Time Base Counter Frequency Adjustment Registers L and H (LTBADJL, LTBADJH)

Address: 0F00CH
Access: R/W
Access size: 8/16 bit
Initial value: 00H

	7	6	5	4	3	2	1	0
LTBADJL	LADJ7	LADJ6	LADJ5	LADJ4	LADJ3	LADJ2	LADJ1	LADJ0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F00DH
Access: R/W
Access size: 8-bit
Initial value: 00H

	7	6	5	4	3	2	1	0
LTBADJH	—	—	—	—	—	LADJS	LADJ9	LADJ8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

LTBADJL and LTBADJH are special function registers (SFRs) to set the frequency adjustment values of the low-speed time base clock.

[Description of Bits]
- **LADJS, LADJ9 to LADJ8** (bits 2 to 0) **LADJ7-LADJ0** (bits 7 to 0)
  The LADJS and LADJ9 to LADJ0 bits are used to adjust frequency.
  Adjustment range: approximately -488ppm to +488ppm, Adjustment accuracy: approximately 0.48ppm is possible. See Section 7.3.3, "Low-Speed Time Base Counter Frequency Adjustment Function" for the correspondence between the frequency adjustment values (LTBADJH, LTBADJL) and adjustment ratio.

7.3 Description of Operation

7.3.1 Low-speed Time Base Counter

The low-speed time base counter (LTBC) starts counting from 0000H on the LSCLK falling edge after system reset. The T128HZ, T32HZ, T16HZ, and T2HZ outputs of LTBC are used as time base interrupts and an interrupt is requested on the falling edge of each output. Each of LTBC outputs is also used as an operation clock for peripheral circuits.
The output data of T128HZ to T1HZ of LTBC can be read from the low-speed time base counter register (LTBR). When reading the data, read LTBR twice and check that the two values coincide to prevent reading of undefined data during counting.
Figure 7-3 shows an example of program to read LTBR.

```
        LEA     offset LTBR      ; EA  LTBR address
MARK:
        L       R0,    [EA]      ; 1st read
        L       R1,    [EA]      ; 2nd read
;
        CMP     R0,    R1        ; Comparison for LTBR
        BNE     MARK             ; To MARK when the values do not coincide
;
           :
```

Figure 7-3   Programming Example for Reading LTBR

LTBR is reset when write operation is performed and the T128HZ to T1HZ outputs are set to "0". Write data is invalid. Since an interrupt occurs if a falling edge occurs in the T128Hz to T2HZ outputs during writing to LTBR, take care in software programming.
Figure 7-4 shows interrupt generation timing and reset timing of the time base counter output by writing to LTBR.
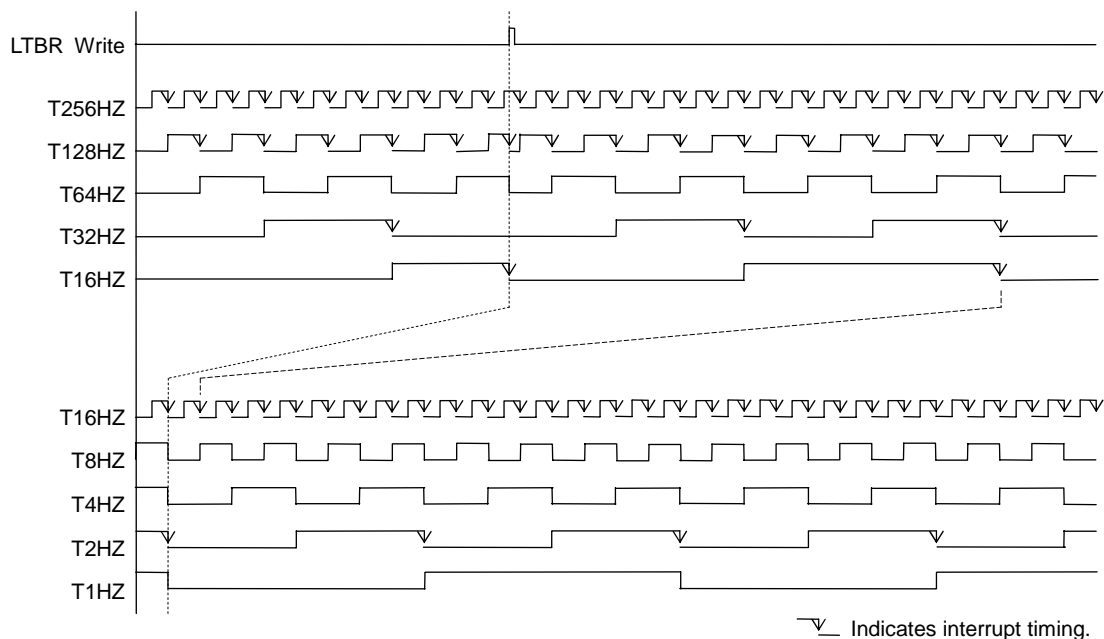
Figure 7-4   Interrupt Timing and Reset Timing by Writing to LTBR

7.3.2   High-Speed Time Base Counter

The high-speed time base counter is configured as a 4-bit 1/n counter (n = 1 to 16).
In the 4-bit 1/n counter, the divided clock (1/16 x HSCLK to 1/1 x HSCLK) selected by the high-speed time base counter divide register (HTBDR) is generated as HTBCLK. HTBCLK is used as a timer and also as an operation clock of PWM.
Figure 7-5 shows the output waveform of HTBCLK.
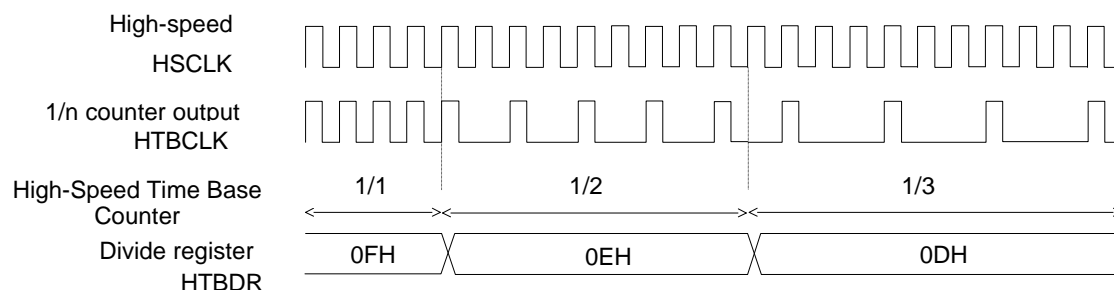
Figure 7-5   Output Waveform of HTBCLK

7.3.3   Low-Speed Time Base Counter Frequency Adjustment Function

Frequency adjustment (Adjustment range: Approx. -488ppm to +488ppm. Adjustment accuracy: Approx. 0.48ppm) is possible for outputs of T8KHZ to T1HZ of LTBC by using the low-speed time base counter frequency adjust registers (LTBADJH and LTBADJL).
Table7-1 shows correspondence between the frequency adjustment values (LTBADJH, LTBADJL) and adjustment ratio.

Table 7-1   Correspondence between Frequency Adjustment Values (LTBADJH, LTBADJL) and Adjustment Ratio

LADJ10 - 0											Hexadecimal	Frequency adjustment ratio (ppm)
0	1	1	1	1	1	1	1	1	1	1	3FFH	+487.80
0	1	1	1	1	1	1	1	1	1	0	3FEH	+487.33
:	:	:	:	:	:	:	:	:	:	:		:
0	0	0	0	0	0	0	0	0	1	1	003H	+1.43
0	0	0	0	0	0	0	0	0	1	0	002H	+0.95
0	0	0	0	0	0	0	0	0	0	1	001H	+0.48
0	0	0	0	0	0	0	0	0	0	0	000H	0
1	1	1	1	1	1	1	1	1	1	1	7FFH	-0.48
1	1	1	1	1	1	1	1	1	1	0	7FEH	-0.95
:	:	:	:	:	:	:	:	:	:	:		:
1	0	0	0	0	0	0	0	0	0	1	401H	-487.80
1	0	0	0	0	0	0	0	0	0	0	400H	-488.28

The adjustment values (LADJ10 to LADJ0) to be set in LTBADJH and LTBADJL can be obtained by using the following equations:

Adjustment value= Frequency adjustment ratio x 2097152 (decimal)
= Frequency adjustment ratio x 200000h (hexadecimal)

Example 1: When adjusting +15.0ppm (when the clock loses)
Adjustment value= +15.0ppm x 2097152 (decimal)
= $+15.0\times10^{-6}\times2097152$
= +31.45728 (decimal)
≑ 01Fh (hexadecimal)

Example 2: When adjusting −25.5ppm (when the clock gains)
Adjustment value= −25.5ppm x 2097152 (decimal)
= $−25.5\times10{-6}\times2097152$
= −53.477376 (decimal)
≑ 7CCh (hexadecimal)

Note:
The low-speed clock (LSCLK) and the outputs of T32KHZ and T16KHZ of LTBC are not adjusted by the frequency adjust function.
The frequency adjustment accuracy does not guarantee the accuracy including the frequency variation of the crystal oscillation (32.768kHz) due to temperature variations.

7.3.4 A signal generation for 16-bit timer 2-3 frequency measurement mode

A signal (437C) used for 16-bit timer 2-3 frequency measurement mode is generated from the output clock of the low-speed time base counter. See Chapter 9, "Timer" for more detail about the frequency measurement mode.
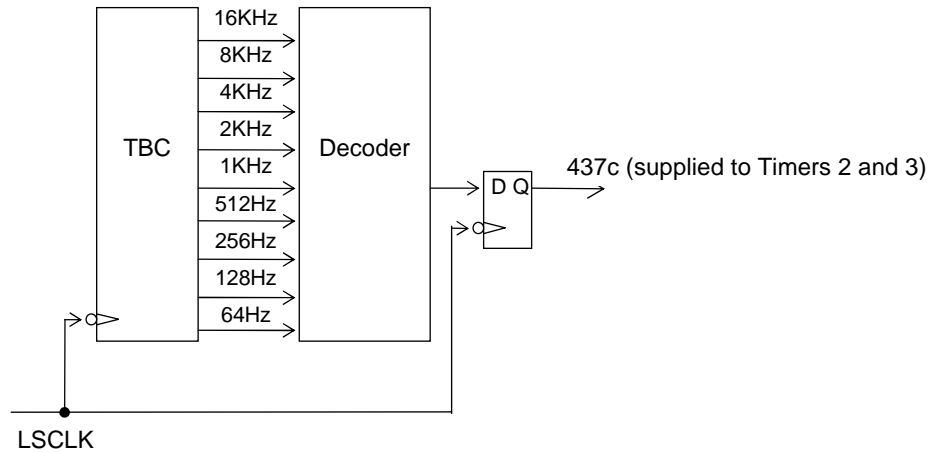
Figure 7-6　Configuration of Frequency Measurement Mode Clock (437c) Generation Circuit

Capture

8. Capture

8.1 Overview

This LSI has two channels of capture circuits that capture the T4KHZ to T32HZ signals of the low-speed time base counter (LTBC) to the capture data register at the occurrence of P00 and P01 interrupts. The circuits capture timings at which each interrupt occurred, based on the time from the time base counter. It can also read out the T4KHZ to T32HZ signals of the low-speed time base counter (LTBC) at any timing.
For the external interrupt (P00INT, P01INT) from the P00 or P01 pin, see Chapter 5, "Interrupt" and Chapter 12, "Port 0".

8.1.1 Features

- Time base capture x 2 channels (4096Hz to 32Hz)

8.1.2 Configuration

Figure 8-1 shows the configuration of the capture circuit.


```
CAPCON    : Capture control register
CAPSTAT : Capture status register
CAPR0     : Capture data register 0
CAPR1     : Capture data register 1
CAPTB     : Capture time base data register
```

Figure 8-1　Configuration of Capture Circuit

8.1.3 List of Pins

Pin name	I/O	Function
P00/CAP0	I	Capture 0 input pin Used as the secondary function of the P00 pin.
P01/CAP1	I	Capture 1 input pin Used as the secondary function of the P01 pin.

8.2 Description of Registers

8.2.1   List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F090H	Capture control register	CAPCON	—	R/W	8	00H
0F091H	Capture status register	CAPSTAT	—	R	8	00H
0F092H	Capture data register 0	CAPR0	—	R/W	8	00H
0F093H	Capture data register 1	CAPR1	—	R/W	8	00H
0F094H	Capture time base data register	CAPTB	—	R	8	Undefined

8.2.2   Capture Control Register (CAPCON)

Address: 0F090H
Access: R/W
Access size: 8-bit
Initial value: 00H

	7	6	5	4	3	2	1	0
CAPCON	—	—	—	—	—	—	ECAP1	ECAP0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

CAPCON is a special function register (SFR) to control the capture circuit.

[Description of Bits]
- **ECAP0** (bit 0)
  The ECAP0 bit is used to start or stop the operation of capture 0.

ECAP0	Description
0	Stops the capture 0 operation. (initial value)
1	Starts the capture 0 operation.

- **ECAP1** (bit 1)
  The ECAP1 bit is used to start or stop the operation of capture 1.

ECAP1	Description
0	Stops the capture 1 operation. (initial value)
1	Starts the capture 1 operation.

8.2.3 Capture Status Register (CAPSTAT)

Address: 0F091H
Access: R
Access size: 8-bit
Initial value: 00H

	7	6	5	4	3	2	1	0
CAPSTAT	—	—	—	—	—	—	CAPF1	CAPF0
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

CAPSTAT is a read-only, special function register (SFR) to indicate a state of the capture circuit.

[Description of Bits]
- **CAPF0** (bit 0)
  The CAPF0 bit is the flag to indicate whether data is captured in capture data register 0 (CARP0) or not. When the CAPF0 bit is set to "1", it indicates that data is captured in capture data register 0 (CAPR0).
  When the CAPF0 bit is set to "1", the next capture operation is stopped. So perform the write operation to capture data register 0 (CAPR0) to clear the CAPF0 bit to "0".

CAPF0	Description
0	No capture 0 latch (initial value)
1	Capture 0 latch

- **CAPF1** (bit 1)
  The CAPF1 bit is the flag to indicate whether data is captured in capture data register 0 (CARP1) or not. When the CAPF0 bit is set to "1", it indicates that data is captured in capture data register 0 (CAPR1).
  When the CAPF1 bit is set to "1", the next capture operation is stopped. So perform the write operation to capture data register 1 (CAPR1) to clear the CAPF0 bit to "0".

CAPF1	Description
0	No capture 1 latch (initial value)
1	Capture 1 latch

8.2.4 Capture Data Register 0 (CAPR0)

Address: 0F092H
Access: R/W
Access size: 8-bit
Initial value: 00H

	7	6	5	4	3	2	1	0
CAPR0	CP07	CP06	CP05	CP04	CP03	CP02	CP01	CP00
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

CAPR0 is a register in which capture data is stored.
The T4KHZ to T32HZ signals of the low-speed time base counter (LTBC) are captured when the P00 interrupt request is generated with the CAPF0 flag (bit 0 of the CAPSTAT register) set to "0".
Writing to CAPR0 sets the CAPF0 flag of CAPSTAT to "0". The value of CAPR0 does not change even if data is written to it.

8.2.5   Capture Data Register 1 (CAPR1)

Address: 0F093H
Access: R/W
Access size: 8-bit
Initial value: 00H

	7	6	5	4	3	2	1	0
CAPR1	CP17	CP16	CP15	CP14	CP13	CP12	CP11	CP10
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

CAPR1 is a register in which capture data is stored.
The T4KHZ to T32HZ signals of the low-speed time base counter (LTBC) are captured when the P01 interrupt request is generated with the CAPF1 flag (bit 1 of the CAPSTAT register) set to "0".
Writing to CAPR1 sets the CAPF1 flag of CAPSTAT to "0". The value of CAPR1 does not change even if data is written to it.

8.2.6   Capture Time Base Data Register (CAPTB)

Address: 0F094H
Access: R
Access size: 8-bit
Initial value: Undefined

	7	6	5	4	3	2	1	0
CAPTB	CPTB7	CPTB6	CPTB5	CPTB4	CPTB3	CPTB2	CPTB1	CPTB0
R	R	R	R	R	R	R	R	R
Initial value	X	X	X	X	X	X	X	X

CAPTB is a special function register (SFR) to read the T4KHZ to T32HZ outputs of the low-speed time base counter (LTBC). The initial value varies depending on the state of the T4KHZ to T32HZ outputs of the low-speed time base counter (LTBC) at the timing when this register is read. When reading the data, read this register twice and check that the two values coincide to prevent reading of undefined data during counting.

8.3 Description of Operation

The capture circuit starts the capture operation by setting the ECAP0 or ECAP1 bit of the capture control register (CAPCON).

When the input trigger from the P00 or P01 pin selected by the external interrupt control register 0 or 1 (EXICON0 or EXICON1) is generated and the P00 or P01 interrupt request flag (QP00 or QP01) is set to "1", the T4KHZ to T32HZ signals of the low-speed time base counter (LTBC) are captured in the capture data register 0 or 1 (CAPR0 or CAPR1) on the next low-speed clock (LSCLK) falling edge and the at the same time, the capture flag (CAPF0 or CAPF1) of the capture status register (CAPSTAT) is set to "1".

When the capture flag (CAPF0, CAPF1) is "1", the following capture operation stops.

The value, once captured by software into the capture data register 0 or 1 (CAPR0, CAPR1), is read to the CPU. Then, in preparation for the next capture operation, the writing operation is performed to the applicable capture data register 0 or 1 (CAPR0, CAPR1)(write data is meaningless), the capture flag (CAPF0, CAPF1) is cleared to "0", then the next P00 or P01 interrupt is waited.

Figure 8-2 shows the timing of the capture operation.
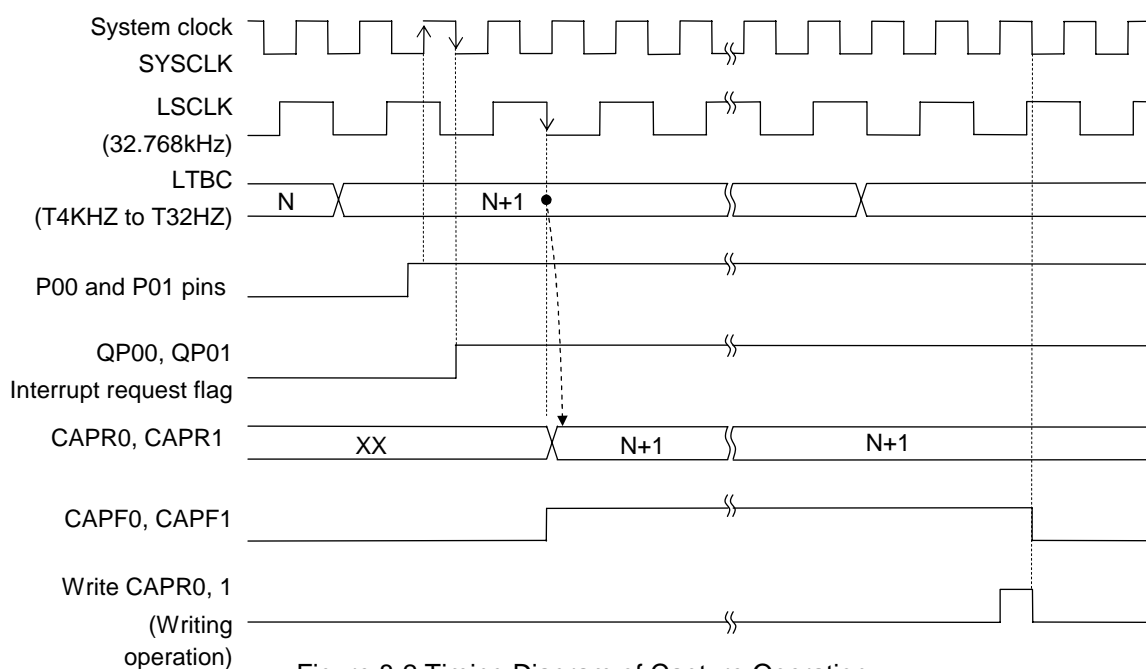
Figure 8-2 Timing Diagram of Capture Operation

Note:
When CPU is operating on the high-speed clock (HSCLK), check that the capture flag (CAPF0, CAPF1) is set to "1" after the P00 or P01 interrupt request is generated and then read capture data register 0 or 1 (CAPR0, CAPR1).

Timer

9. Timer

9.1 Overview

This LSI includes 2 channels of 8-bit timers.

9.1.1 Features

- The timer interrupt (TMnINT) is generated when the values of timer counter register (TMnC, n=2 to 3) and timer data register (TMnD) coincide.
- A timer configured by combining or timer 2 and timer 3 can be used as a 16-bit timer.
- For the timer clock, the low-speed clock (LSCLK), high-speed time base clock (HTBCLK), or external clock can be selected.
- A 16bit-timer has clock frequency measurement mode, which can count HTBCLK and generates the timer interrupt (TM3INT) when the count ends.

9.1.2 Configuration

Figure 9-1 shows the configuration of the timers.

TMnCON0   : Timer control register 0
TMnCON1   : Timer control register 1
TMmD, TMnD : Timer data register
TMmC, TMnC : Timer counter register

(a) In 8-bit Timer Mode (Timers 2 to 3)

(b) In 16-bit Timer Mode (Timers 2 to 3)

(c) Frequency measurement mode with 16 bit timer (Timer2 to 3)

Figure 9-1   Timer Configuration

9.1.3   List of Pins

Pin name	I/O	Function
P44/T2CK	I	External clock input pin 8bit timer mode : used for timer2 16bit timer mode : used for timer2 to timer3.
P45/T3CK	I	External clock input pin 8bit timer mode : used for timer3

9.2 Description of Registers

9.2.1   List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F038H	Timer 2 data register	TM2D	TM2DC	R/W	8/16	0FFH
0F039H	Timer 2 counter register	TM2C		R/W	8	00H
0F03AH	Timer 2 control register 0	TM2CON0	TM2CON	R/W	8/16	0A0H
0F03BH	Timer 2 control register 1	TM2CON1		R/W	8	00H
0F03CH	Timer 3 data register	TM3D	TM3DC	R/W	8/16	0FFH
0F03DH	Timer 3 counter register	TM3C		R/W	8	00H
0F03EH	Timer 3 control register 0	TM3CON0	TM3CON	R/W	8/16	00H
0F03FH	Timer 3 control register 1	TM3CON1		R/W	8	00H

9.2.2 Timer 2 Data Register (TM2D)

Address: 0F038H
Access: R/W
Access size: 8-bit
Initial value: 0FFH

	7	6	5	4	3	2	1	0
TM2D	T2D7	T2D6	T2D5	T2D4	T2D3	T2D2	T2D1	T2D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	1	1	1	1	1

TM2D is a special function register (SFR) to set the value to be compared with the value of the timer 2 counter register (TM2C).

Note:
    Set TM2D when the timer stops(When T2STAT bit of TM2CON1 register is "0").
    When "00H" is written in TM2D, TM2D is set to "01H".

9.2.3　Timer 3 Data Register (TM3D)

Address: 0F03CH
Access: R/W
Access size: 8-bit
Initial value: 0FFH

	7	6	5	4	3	2	1	0
TM3D	T3D7	T3D6	T3D5	T3D4	T3D3	T3D2	T3D1	T3D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	1	1	1	1	1

TM3D is a special function register (SFR) to set the value to be compared with the value of the timer 3 counter register (TM3C).

Note:
　　Set TM3D when the timer stops(When T3STAT bit of TM3CON1 register is "0").
　　When "00H" is written in TM3D, TM3D is set to "01H".

9.2.4　Timer 2 Counter Register (TM2C)

Address: 0F039H
Access: R/W
Access size: 8-bit
Initial value: 00H

	7	6	5	4	3	2	1	0
TM2C	T2C7	T2C6	T2C5	T2C4	T2C3	T2C2	T2C1	T2C0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

TM2C is a special function register (SFR) that functions as an 8-bit binary counter.
When write operation to TM2C is performed, TM2C is set to "00H". The data that is written is meaningless.
In 16-bit timer mode and 16-bit timer frequency measurement mode, if write operation is performed to either the low-order TM2C or high-order TM3C, both the low order and the high order are set to "0000H".

During timer operation, the TM2C content may not be read depending on the conditions of the timer clock and the system clock.
Table 9-1 shows whether a TM2C read is enabled or disabled during timer operation for each condition of the timer clock and system clock.

Table 9-1　TM2C Read Enable/Disable during Timer Operation

Timer clock TM2CK	System clock SYSCLK	TM2C read enable/disable
LSCLK	LSCLK	Read enabled.
LSCLK	HSCLK	Read enabled. However, to prevent the reading of undefined data during incremental counting, read TM2C twice and check that the results match.
HTBCLK	LSCLK	Read disabled.
HTBCLK	HSCLK	Read enabled.
External clock	LSCLK	Read disabled.
External clock	HSCLK	Read disabled.

9.2.5 Timer 3 Counter Register (TM3C)

Address: 0F03DH
Access: R/W
Access size: 8-bit
Initial value: 00H

	7	6	5	4	3	2	1	0
TM3C	T3C7	T3C6	T3C5	T3C4	T3C3	T3C2	T3C1	T3C0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

TM3C is a special function register (SFR) that functions as an 8-bit binary counter.
When write operation to TM3C is performed, TM3C is set to "00H". The data that is written is meaningless.
In 16-bit timer mode and 16-bit timer frequency measurement mode, if write operation is performed to either the low-order TM2C or high-order TM3C, both the low order and the high order are set to "0000H".
When reading TM3C in 16-bit timer mode, be sure to read TM2C first since the count value of TM3C is stored in the TM3C latch when TM2C is read.

During timer operation, the TM3C content may not be read depending on the conditions of the timer clock and the system clock.
Table 9-2 shows whether a TM3C read is enabled or disabled during timer operation for each condition of the timer clock and system clock.

Table 9-2　TM3C Read Enable/Disable during Timer Operation

Timer clock TM3CK	System clock SYSCLK	TM3C read enable/disable
LSCLK	LSCLK	Read enabled.
LSCLK	HSCLK	Read enabled. However, to prevent the reading of undefined data during incremental counting, read TM3C twice and check that the results match.
HTBCLK	LSCLK	Read disabled.
HTBCLK	HSCLK	Read enabled.
External clock	LSCLK	Read disabled.
External clock	HSCLK	

9.2.6 Timer 2 Control Register 0 (TM2CON0)

Address: 0F03AH
Access: R/W
Access size: 8-bit
Initial value: 0A0H

	7	6	5	4	3	2	1	0
TM2CON0	T2FMA7	T2FMA6	T2FMA5	T2FMA4	T23MFM	T23M16	T2CS1	T2CS0
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Initial value	1	0	1	0	0	0	0	0

TM2CON0 is a special function register (SFR) to control the Timer 2.
Rewrite TM2CON0 while the timer 2 is stopped (T2STAT of the TM2CON1 register is "0").

[Description of Bits]

- **T2CS1, T2CS0** (bits 1, 0)
  The T2CS1 and T2CS0 bits are used for selecting the operation clock of timer 2. LSCLK, HTBCLK, or the
  external clock (P44/T2CK) can be selected by these bits.

T2CS1	T2CS0	Description
0	0	LSCLK (initial value)
0	1	HTBCLK
1	0	Prohibited
1	1	External clock (P44/T2CK)

- **T23MFM, T23M16** (bit 3, 2)
  The T23MFM bit and T23M16 bit is used for selecting the operating mode of timer 2 and timer 3..
  In 8-bit timer mode, each of timer 0 and timer 1 operates independently as a 8-bit timer.
  In 16-bit timer mode, timer 2 and timer 3 are connected and they operate as a 16-bit timer.
  In 16-bit timer mode, timer 3 is incremented by a timer 2 overflow signal.
  A timer 2 interrupt (TM2INT) is not generated.
  In 16-bit timer frequency measurement mode, timer 2 and timer 3 are connected and they operate as a 16-bit
  clock counter to measure the frequency.
  A timer 2 interrupt (TM2INT) is not generated.

T23MFM	T23M16	Description
0	0	8-bit timer mode (initial value)
0	1	16-bit timer mode
1	0	Prohibited
1	1	16-bit timer frequency measurement mode

- **T2FMA7 to T2FMA4** (bit 7 to 4)
  T2FMA7 to T2FMA4 are read-only registers that show whether the frequency measurement function is provided.

T2FMA7	T2FMA6	T2FMA5	T2FMA4	Description
1	0	1	0	The frequency measurement mode is available

9.2.7　Timer 3 Control Register 0 (TM3CON0)

Address: 0F03EH
Access: R/W
Access size: 8-bit
Initial value: 00H

	7	6	5	4	3	2	1	0
TM3CON0	—	—	—	—	—	—	T3CS1	T3CS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

TM3CON0 is a special function register (SFR) to control the Timer 3.
Rewrite TM3CON0 while the timer 3 is stopped (T3STAT of the TM3CON1 register is "0").

[Description of Bits]
- **T3CS1, T3CS0** (bits 1, 0)
  The T3CS1 and T3CS0 bits are used for selecting the operation clock of timer 3. LSCLK, HTBCLK, or the external clock (P45/T3CK) can be selected by these bits.
  In cases where the 16-bit timer mode has been selected by setting T23M16 of TM2CON to "1", the values of T3CS1 and T3CS0 are invalid.

T3CS1	T3CS0	Description
0	0	LSCLK (initial value)
0	1	HTBCLK
1	0	Prohibited
1	1	External clock (P45/T3CK)

9.2.8　Timer 2 Control Register 1 (TM2CON1)

Address: 0F03BH
Access: R/W
Access size: 8-bit
Initial value: 00H

	7	6	5	4	3	2	1	0
TM2CON1	T2STAT	—	—	—	—	—	—	T2RUN
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

TM2CON1 is a special function register (SFR) to control the Timer 2.

[Description of Bits]

- **T2RUN** (bit 0)
  The T2RUN bit is used for controlling stop/start of timer 2.
  Setting the T2RUN bit can force cancel the counting in the 16-bit timer frequency measurement mode.
  In that case, TM3INT does not occur.

T2RUN	Description
0	In timer mode: Stops counting.　　In frequency measurement mode: Stops measurement
1	In timer mode: Starts counting.　　In frequency measurement mode: Starts measurement

- **T2STAT** (bit 7)
  The T2STAT bit is used for indicating "counting stopped"/"counting in progress" of timer 2.

T2STAT	Description
0	In timer mode: Count halted.　　In frequency measurement mode: Measurement halted
1	In timer mode: Counting in progress.　　In frequency measurement mode: Measuring

9.2.9 Timer 3 Control Register 1 (TM3CON1)

Address: 0F03FH
Access: R/W
Access size: 8-bit
Initial value: 00H

	7	6	5	4	3	2	1	0
TM3CON1	T3STAT	—	—	—	—	—	—	T3RUN
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

TM3CON1 is a special function register (SFR) to control the Timer 3.

[Description of Bits]

- **T3RUN** (bit 0)

  The T3RUN bit is used for controlling counting stop/start of timer 3.

  In 16-bit timer mode and 16-bit timer frequency measurement mode, be sure to set this bit to "0". Regardless of the T3RUN value, the Timer 3 counts up
  by the Timer 2 overflow signal.

  In 16-bit timer frequency measurement mode, be sure to set this bit to "0" also.

T3RUN	Description
0	Stops counting.
1	Starts counting.

- **T3STAT** (bit 7)

  The T3STAT bit is used for indicating "counting stopped"/"counting in progress" of timer 3.

  In 16-bit timer mode and 16-bit timer frequency measurement mode, this bit will return "0".

T3STAT	Description
0	Counting stopped.
1	Counting in progress.

9.3 Description of Operation

9.3.1   Timer mode operation

The timer counters (TMnC) are set to an operating state (TnSTAT are set to "1") on the first falling edge of the timer clocks (TMnCK) that are selected by the Timer 2 to 3 control register 0 (TMnCON0) when the TnRUN bits of timer 2 to 3 control register 1 (TMnCON1) are set to "1" and increment the count value on the 2nd falling.

When the count value of TM2 to TM3C and the timer 2 to 3 data register (TMnD) coincide, timer 2 to 3 interrupt (TMnINT) occurs on the next timer clock falling edge, TMnC are reset to "00H" and incremental counting continues.

When the TnRUN bits are set to "0", TMnC stop counting after counting once the falling of the timer clock (TMnCK). Confirm that TMnC has been stopped by checking that the TnSTAT bit of the Timer 2–3 control register 1 (TMnCON1) is "0".
When the TnRUN bits are set to "1" again, TMn restart incremental counting from the previous values.
To initialize TMnC to "00H", perform write operation in TMnC.

The timer interrupt period (T_{TMI}) is expressed by the following equation.

$$T_{TMI} = \frac{TMnD + 1}{TMnCK\ (Hz)} \qquad (n=2\sim3)$$

TMnD: Timer 2 to 3 data register (TMnD) setting value (01H to 0FFH)
TMnCK: Clock frequency selected by the Timer 2 to 3 control register 0 (TMnCON0)

After the TnRUN bits are set to "1", timers are synchronized by the timer clock and counting starts so that an error of a maximum of 1 clock period occurs until the first timer interrupt. The timer interrupt periods from the second time are constant.
Figure 9-2 shows the operation timing diagram of Timer 2 to 3.
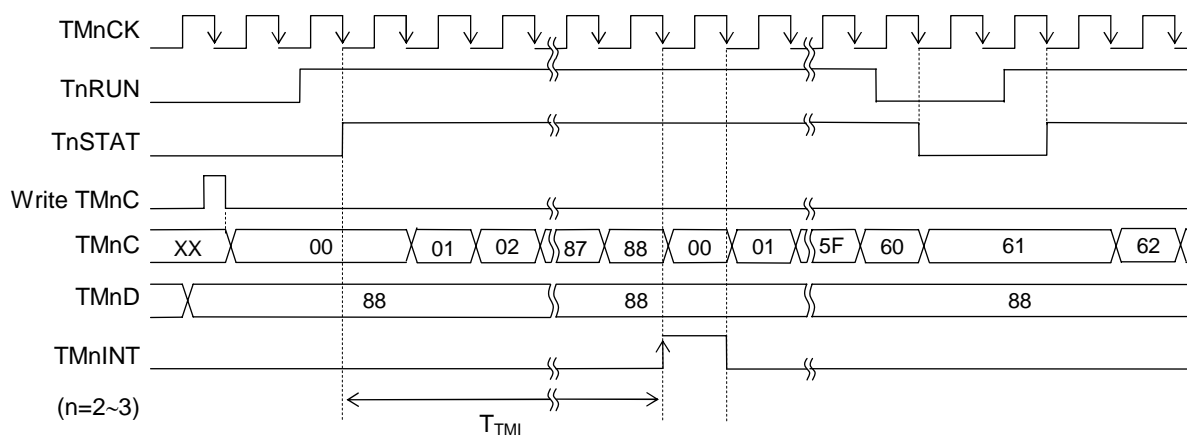
Figure 9-2   Operation Timing Diagram of Timer 2 to 3

Note:
  Even if "0" is written to the TnRUN bits, counting operation continues up to the falling edge (the timer 2 to 3 status flag (TnSTA) is in a "1" state) of the next timer clock pulse. Therefore, the timer 2 to 3 interrupt (TMnINT) may occur.

9.3.2 16-bit timer frequency measurement mode operation

The frequency measurement mode in 16-bit timer 2&3, is used to count the frequency of RC oscillation clock which typically has temperature variation and production tolerance.

Using the frequency measurement mode can make better accuracy for timer function.
− Reading the count data, calculating and setting it to a timer data register, can make more accurate timing in normal timer mode.

Figure 9-3 shows the operation timing in frequency measurement mode.
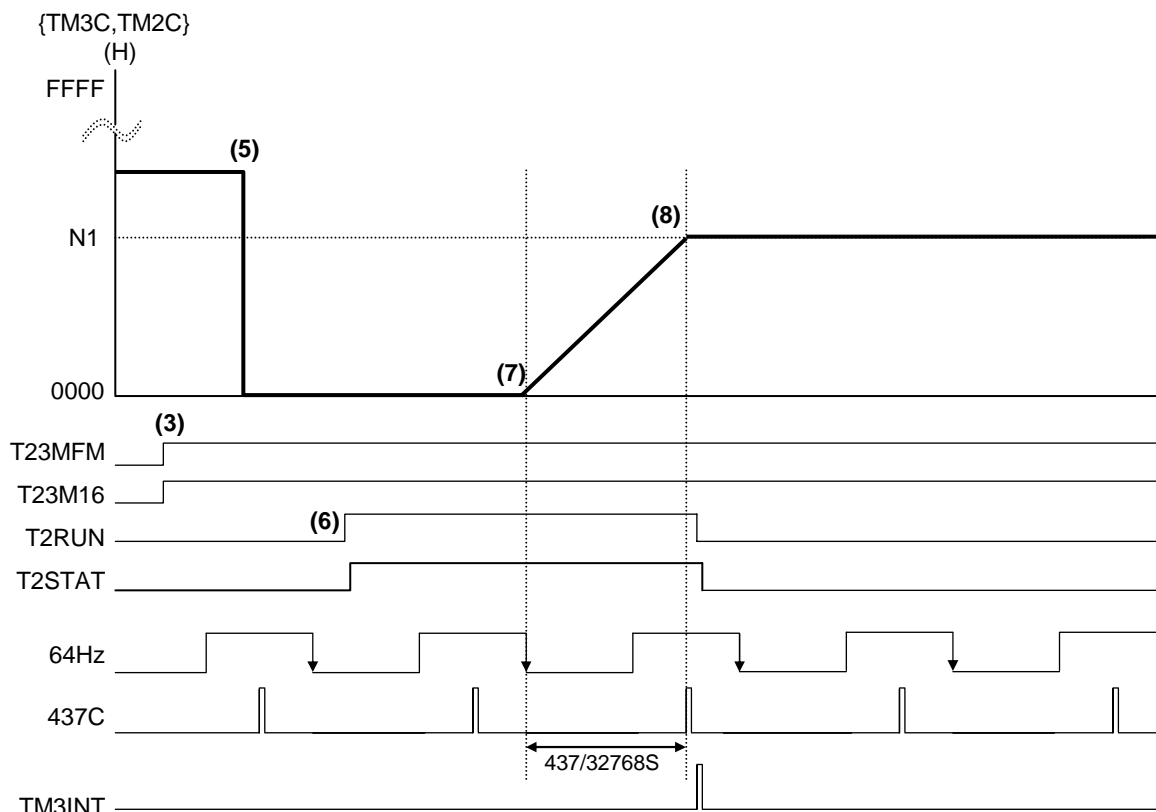
Figure 9-3   Operation Timing in frequency measurement mode

(1) High-speed clock (HSCLK, HTBCLK) has to be in oscillating state by controlling with FCONn registers. And also select 1/1 divide ratio of the high-speed time base counter by setting HTBDR (High-speed Time Base counter Divide Register) register to 0FH.

(2) Reset both T2RUN bit (bit0 of TM2CON1 register) and T3RUN bit (bit0 of TM3CON1 register) to "0" to stop the timer. And then, check both T2STAT bit (bit7 of TM2CON1 register) and T3STAT bit (bit7 of TM3CON1 register) are "0" for making certain the timer stops.

(3) Set T23MFM bit (bit3 of TM2CON0 register) to "1" (Frequency measurement mode), set T23M16 bit (bit2 of TM2CON0 register) to "1" (16bit mode) and set T2CS1-0 bits(bit1/0 of TM2CON0 register) to "01"(HTBCLK mode).

(4) Set "FFH" to both TM2D register and TM3D register.

(5) Clear both TM2C register and TM3C register to "00H".

(6) Set T2RUN bit (bit0 of TM2CON1 register) to "1" to start counting the timer.

(7) When (T23MFM bit == "1") and (TM23M16 bit == "1") and (T2RUN bit == "1"),
     the count up starts with the falling of the 64Hz clock signal.

(8) The count-up stops at the falling edge of the next timer clock (HTBCLK) after 437C signal becomes "1".
Also, at the same time, T2RUN bit and T2STAT bit become "0" and the interrupt signal TM3INT activates.
The 437C signal is the pulse signal that rises in 437/32768 seconds after the falling of the 64Hz signal.

(9) After checking T2STAT bit or TM3INT interrupt occurs, read out the data (N1) of TM2C register and TM3C register.

For example of utilizing N1, 9600Hz timer interrupt is generated.

Assuming a low-accuracy high-speed clock (HTBCLK) is exactly 600kHz, then the count value N1 is:
$$N1 = 600000 \times 437 / 32768$$
$$= 8001 \text{ (Decimal)}$$
$$= 1F41 \text{ (Hexadecimal)}$$
$$= 0001\ 1111\ 0\underline{100\ 0001} \text{ (Binary)}$$

Because 437/32768 seconds are equivalent to 128 clocks at 9600 Hz (more precisely, 9598 Hz),
dividing the count value NI by 128 provides the frequency ratio (N2) between the HTBCLK and 9600 Hz.
Because $128 = 2^7$, this calculation can be solved by truncating the right-hand seven digits of N1 (Binary), that is:
$$N2 = 8001\text{(Decimal)} / 128 \text{ (Decimal)}$$
$$= 0001\ 1111\ 0 \text{ (Binary)}$$
$$= 3E \text{ (Hexadecimal)}$$
$$= 62 \text{ (Decimal)}$$

This indicates that 9600Hz is about 62 times the cycle of HTBCLK.
Therefore, for an operation in the timer mode where the timer data register is set to
3EH – 1 = 3DH to overflow the counter every 62 counts of the HTBCLK clock,
the TMnINT interrupt signal cycle tTMnINT is:
$$tTMnINT = 1 / 600000 \times 62 = 0.10333\text{ms}(9677\text{Hz})$$

9.3.3　16-bit timer frequency measurement mode application for setting uart baud-rate

For example, when the target baud-rate is 9600bps and the clock is HSCLK(500kHz), the UART0 baud-rate register (UA0BRTH, UA0BRTL) should be set as:
UA0BRTH, UA0BRTL = 500000/9600 – 1 = 51 (decimal) = 33 (hexadecimal) (See Section 11.3.2.)

However, actual 500kHz RC oscillation clock has temperature variation and production tolerance, the calculation by using the fixed value of 500kHz cannot make accurate baud-rate. To compensate it, count the frequency in the frequency measurement mode to set the baud-rate again before operating UART communication.

After finishing the clock count in the frequency measurement mode, assuming HTBCLK is 451kHz, data of TM2C register and TM3C register will be:
$N1 = 451000 \times 437 / 32768$
= 6014 (Decimal)
= 177E (Hexadecimal)
= 1011101111110 (Binary)
As (437 / 32768) sec is equivalent to 128 clocks at 9600Hz (more precisely, 9598Hz), a division of the count (N1) by 128 equals frequency ratio (N2) between the frequency of HTBCLK and 9600Hz. For the calculation, the accuracy of baud-rate depends on truncating (1) or rounding (2) the data.

UART0 baud rate registers H and L are:
UA0BRTH, UA0BRTL = (frequency ratio between HTBCLK clock and baud rate) - 1 = (N1/128)-1 = N2 -1
(See Section 11.3.2.)

① Round data in calculation
N1 = 1011101111110 (binary)
N2 = 101111 (binary) = 47 (decimal) = 2F (hexadecimal)
Set N2-1 (= 2E) to UA0BRTH and UA0BRTL registers. In this case, the actual baud-rate will be 9595.744681.. [bps], so the accuracy = ((9595.744681/9600) -1)* 100= -0.04..[%].

② Truncate data in calculation (the accuracy of baud-rate becomes worse)
N1 = 1011101111110 (binary)
N2 = 101110 (binary) = 46 (decimal) = 2E (hexadecimal)
Set N2-1 (= 2D) to UA0BRTH and UA0BRTL registers. In this case, the actual baud-rate will be 9804.347826.. [bps], so the accuracy = ((9804.347826/9600) -1)* 100= 2.12..[%].

Table 9-5 shows the baud rate and accuracy (theoretical) when the baud rate clock is set to 500KHz.

Table 9-5　Baud Rate and Accuracy (theoretical) for Baud Rate Clock Set to 500KHz

Baud-rate[bps]	Data setting to UA0BRTH register and UA0BRTH register	Theoretical accuracy
300	Round off {N1/4 (2bit right-shift) } - (minus) 1.	~ ±2%
600	Round off {N1/8 (3bit right-shift) } - (minus) 1.	
1200	Round off {N1/16 (4bit right-shift) } - (minus) 1.	
2400	Round off {N1/32 (5bit right-shift) } - (minus) 1.	
4800	Round off {N1/64 (6bit right-shift) } - (minus) 1.	
9600	Round off {N1/128 (7bit right-shift) } - (minus) 1.	
19200	Round off {N1/256 (8bit right-shift) } - (minus) 1.	±2% ~ 2.5%
38400	Round off {N1/512 (9bit right-shift) } - (minus) 1.	±2.5% ~

9.4 Operating Timers by External Clock Inputs

When the external clock is selected as the operation clock for the Timer 2 (8-bit timer mode), operate it by inputting the clock with the P44 set to the 1st function. When the external clock is selected as the operation clock for the Timer 3 (8-bit timer mode), operate it by inputting the clock with the P45 set to the 1st function.
When the external clock is selected as the operation clock for the Timers 1 and 2 set to the 16-bit timer mode, operate them by inputting the clock with the P44 set to the 1st function.
Set the external clock frequency to a value below the operating frequency (fop) in "Appendix C Electrical Characteristics."

9.4.1   Operating Timer 2 (8-Bit Timer Mode) by External Clock (P44/T2CK)

Set the P44MD1 bit (P4MOD1 register's bit 4) to "0" and the P44MD0 bit (P4MOD0 register's bit 4) to "0" for specifying the P44 to the 1st function.

Register name	P4MOD1 register (Address: 0F225H)							
Bit	7	6	5	**4**	3	2	1	0
Bit name	P47MD1	P46MD1	P45MD1	**P44MD1**	P43MD1	P42MD1	P41MD1	P40MD1
Setting value	*	*	*	**0**	*	*	*	*

Register name	P4MOD0 register (Address: 0F224H)							
Bit	7	6	5	**4**	3	2	1	0
Bit name	P47MD0	P46MD0	P45MD0	**P44MD0**	P43MD0	P42MD0	P41MD0	P40MD0
Setting value	*	*	*	**0**	*	*	*	*

Set the P44DIR bit (P4DIR register's bit 4) to "1" for specifying the state mode of the P44 pin to input.

Register name	P4DIR register (Address: 0F221H)							
Bit	7	6	5	**4**	3	2	1	0
Bit name	P47DIR	P46DIR	P45DIR	**P44DIR**	P43DIR	P42DIR	P41DIR	P40DIR
Setting value	*	*	*	**1**	*	*	*	*

Select the external clock(P44/T2CK) and timer2 (8-bit mode) in the TM2CON0 register, and input the operation clock for the Timer 2 from the P44 pin.

9.4.2 Operating Timer 3 (8-Bit Timer Mode) by External Clock (P45/T3CK)

Set the P45MD1 bit (P4MOD1 register's bit 5) to "0" and the P45MD0 bit (P4MOD0 register's bit 5) to "0" for specifying the P45 to the 1st function.

Register name	P4MOD1 register (Address: 0F225H)							
Bit	7	6	5	4	3	2	1	0
Bit name	P47MD1	P46MD1	**P45MD1**	P44MD1	P43MD1	P42MD1	P41MD1	P40MD1
Setting value	*	*	**0**	*	*	*	*	*

Register name	P4MOD0 register (Address: 0F224H)							
Bit	7	6	5	4	3	2	1	0
Bit name	P47MD0	P46MD0	**P45MD0**	P44MD0	P43MD0	P42MD0	P41MD0	P40MD0
Setting value	*	*	**0**	*	*	*	*	*

Set the P45DIR bit (P4DIR register's bit 5) to "1" for specifying the state mode of the P45 pin to input.

Register name	P4DIR register (Address: 0F221H)							
Bit	7	6	5	4	3	2	1	0
Bit name	P47DIR	P46DIR	**P45DIR**	P44DIR	P43DIR	P42DIR	P41DIR	P40DIR
Setting value	*	*	**1**	*	*	*	*	*

Select the external clock (P45/T3CK) and timer3 (8-bit mode) in the TM3CON0 register, and input the operation clock for the Timer 3 from the P45 pin.

9.4.3 Operating Timer 2 and Timer 3 (16-Bit Timer Mode) by External Clock (P44/T2CK)

Set the P44MD1 bit (P4MOD1 register's bit 4) to "0" and the P44MD0 bit (P4MOD0 register's bit 4) to "0" for specifying the P44 to the 1st function.

Register name	P4MOD1 register (Address: 0F225H)							
Bit	7	6	5	**4**	3	2	1	0
Bit name	P47MD1	P46MD1	P45MD1	**P44MD1**	P43MD1	P42MD1	P41MD1	P40MD1
Setting value	*	*	*	**0**	*	*	*	*

Register name	P4MOD0 register (Address: 0F224H)							
Bit	7	6	5	**4**	3	2	1	0
Bit name	P47MD0	P46MD0	P45MD0	**P44MD0**	P43MD0	P42MD0	P41MD0	P40MD0
Setting value	*	*	*	**0**	*	*	*	*

Set the P44DIR bit (P4DIR register's bit 4) to "1" for specifying the state mode of the P44 pin to input.

Register name	P4DIR register (Address: 0F221H)							
Bit	7	6	5	**4**	3	2	1	0
Bit name	P47DIR	P46DIR	P45DIR	**P44DIR**	P43DIR	P42DIR	P41DIR	P40DIR
Setting value	*	*	*	**1**	*	*	*	*

Select the external clock (P44/T2CK) and Timers 2 and 3 (16-bit mode) in the TM2CON0 register, and input the operation clock for the Timers 2 and 3 (16-bit mode) from the P44 pin.

Watchdog Timer

10. Watchdog Timer

10.1 Overview

This LSI incorporates a watchdog timer (WDT) that operates at a system reset unconditionally (free-run operation) in order to detect an undefined state of the MCU and return from that state.

If the WDT counter overflows due to the failure of clearing of the WDT counter within the WDT overflow period, the watchdog timer requests a WDT interrupt (non-maskable interrupt). When the second overflow occurs, the watchdog timer generates a WDT reset signal and shifts the mode to a system reset mode.

For interrupts see Chapter 5, "Interrupt," and for WDT interrupt see Chapter 3, "Reset Function".

10.1.1　Features

- Free running (cannot be stopped)
- One of four types of overflow periods (125ms, 500ms, 2s, and 8s) selectable by software
- Non-maskable interrupt request generated by the first overflow
- WDT reset generated by the second overflow

10.1.2　Configuration

Figure 10-1 shows the configuration of the watchdog timer.

WDTCON　: Watchdog timer control register
WDTMOD　: Watchdog timer mode register

Figure 10-1　Configuration of Watchdog Timer

10.2 Description of Registers

10.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F00EH	Watchdog timer control register	WDTCON	—	R/W	8	00H
0F00FH	Watchdog timer mode register	WDTMOD	—	R/W	8	02H

10.2.2 Watchdog Timer Control Register (WDTCON)

Address: 0F00EH
Access: W
Access size: 8-bit
Initial value: 00H

	7	6	5	4	3	2	1	0
WDTCON	d7	d6	d5	d4	d3	d2	d1	WDP/d0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

WDTCON is a special function register (SFR) to clear the WDT counter.
When WDTCON is read, the value of the internal pointer (WDP) is read from bit 0.

[Description of Bits]
- **WDP/d0** (bit 0)
  The value of the internal pointer (WDP) is read from this bit. The WDP is reset to "0" at the system reset or WDT counter overflow and is inverted every writing to WDTCON.

- **d7-d0** (bits 7-0)
  This bit is used to write data to clear the WDT counter. The WDT counter can be cleared by writing "5AH" with the internal pointer (WDP) is "0", then writing "0A5H" with the WDP "1".

Note:
When a WDT interrupt (WDTINT) occurs due to the first overflow of the WDT counter, the WDT counter and internal pointer (WDP) are initialized for a half-clock period (about 15us) of low-speed clock. Because of this, writing to WDTCON will be disabled and the WDP will not be inverted during this period. In the case that you clear the WDT while the system clock is at high speed when a WDT interrupt occurs, make sure that the WDP is inverted by writing to WDTCON and the writing is successfully done. See "10.3.1 Process example for a case watchdog timer is not used" for a program example.

10.2.3 Watchdog Timer Mode Register (WDTMOD)

Address: 0F00FH
Access: W
Access size: 8-bit
Initial value: 02H

	7	6	5	4	3	2	1	0
WDTMOD	—	—	—	—	—	—	WDT1	WDT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	1	0

WDTMOD is a special function register to set the overflow period of the WDT counter.

[Description of Bits]
- **WDT1-0** (bits 1-0)
  These bits are used to select an overflow period of the watchdog timer.
  The WDT1 and WDT0 bits set an overflow period (T_{WOV}) of the WDT counter. One of 125ms, 500ms, 2s, and 8s can be selected.

WDT1	WDT0	Description
0	0	125ms
0	1	500ms
1	0	2s (initial value)
1	1	8s

10.3 Description of Operation

The WDT counter starts counting after the system reset has been released and the low-speed clock oscillation start..
The WDT counter can be cleared by writing "5AH" with the internal pointer (WDP) is "0", then writing "0A5H" with the WDP "1".
The WDP is reset to "0" at the system reset or WDT counter overflow and is inverted every writing to WDTCON.
When the WDT counter cannot be cleared within the WDT counter overflow period (T_{WOV}), a watchdog timer interrupt (WDTINT) occurs. If the WDT counter is not cleared even by the software processing performed following the watchdog timer interrupt and overflow occurs again, WDT reset occurs and the mode shifts to a system reset mode.
For the overflow period (T_{WOV}) of the WDT counter, one of 125ms, 500ms, 2s, and 8s can be selected by the watchdog mode register (WDTMOD).
Clear the WDT counter within the clear period of the WDT counter (T_{WCL}) shown in Table 10-1.

Table 10-1   Clear Period of WDT Counter

WDT1	WDT0	T_{WOV}	T_{WCL}
0	0	125ms	Approxi. 121ms
0	1	500ms	Approx. 496 ms
1	0	2000ms	Approx. 1996 ms
1	1	8000ms	Approx. 7996 ms

Figure 10-2 shows an example of watchdog timer operation.
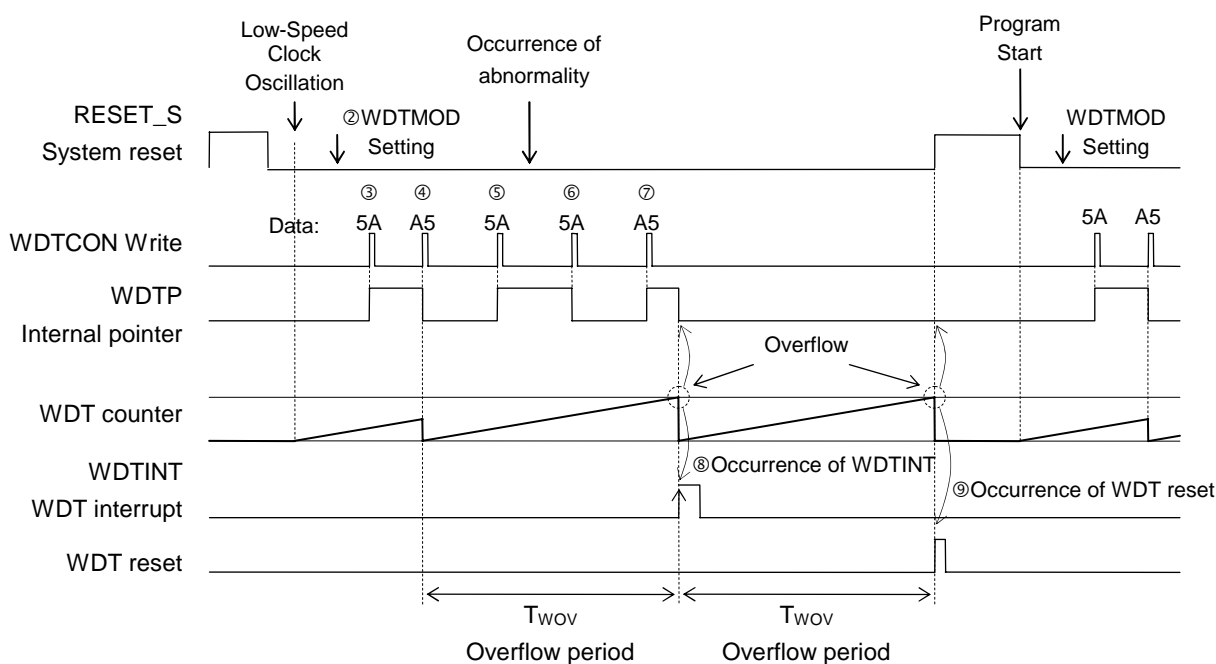
Figure 10-2   Example of Watchdog Timer Operation

① The WDT counter starts counting after the system reset has been released and the low-speed clock oscillation start.

② The overflow period of the WDT counter (T_{WOV}) is set to WDTMOD.

③ "5AH" is written to WDTCON. (Internal pointer 0 to 1)

④ "0A5H" is written to WDTCON and the WDT counter is cleared. (Internal pointer 1 to 0)

⑤ "5AH" is written to WDTCON. (Internal pointer 0 to 1)

⑥ When "5AH" is written to WDTCON after the occurrence of abnormality, it cannot be accepted as the internal pointer is set to "1". (Internal pointer 1 to 0)

⑦ Although "0A5H" is written to WDTCON, the WDT counter is not cleared since the internal pointer is "0" and the writing of "5AH" is not accepted in ⑥. (Internal pointer 0 to 1)

⑧ The WDT counter overflows and a watchdog timer interrupt request (WDTINT) is generated. At this time, the WDT counter and the internal pointer (WDP) are initialized for a half-clock period (about 15.26us) of low-speed clock. (Internal pointer 1 to 0)

⑨ If the WDT counter is not cleared even by the software processing performed following a watchdog timer interrupt and the WDT counter overflows again, WDT reset occurs and the mode is shifted to a system reset mode.

Note:
・In STOP mode, the watchdog timer operation also stops. In HALT mode, the watchdog timer operation does not stop. When the WDT interrupt occurs, the HALT mode is released.
・The watchdog timer cannot detect all the abnormal operations. Even if the CPU loses control, the watchdog timer cannot detect the abnormality in the operation state in which the WDT counter is cleared.

10.3.1 Process example for a case watchdog timer is not used

The WDT counter is a free-run counter that starts counting whenever the low-speed clock (LSCLK) starts oscillation after a system reset is cancelled. Because an overflow of the WDT counter causes non-maskable interrupt or system reset, the WDT counter needs to be cleared even if the WDT function is not used as a fail-safe.
See the following program example that clears the WDT counter in a WDT interrupt routine.

Program example:

```
__DI();                 // Disable multiple interrupts
do
{
WDTCON = 0x5a;
} while(WDP != 1)
WDTCON = 0xa5;
__EI();
```

UART

11. UART

11.1 Overview

This LSI includes 1 channel of UART (Universal Asynchronous Receiver Transmitter) which is an asynchronous serial interface.
For the input clock, see Chapter 6, "Clock Generation Circuit".
The use of UART requires setting of the secondary functions of Port 4. For the secondary functions of Port 4, see Chapter 15, "Port 4".

11.1.1 Features

- 5-bit/6-bit/7-bit/8-bit data length selectable.
- Odd parity, even parity, or no parity selectable.
- 1 stop bit or 2 stop bits selectable.
- Provided with parity error flag, overrun error flag, framing error flag, and transmit buffer status flag.
- Positive logic or negative logic selectable as communication logic.
- LSB first or MSB first selectable as a communication direction.
- Communication speed: Settable within the range of 200bps to 38400bps.
- Built-in baud rate generator.

11.1.2 Configuration

Figure 11-1 shows the configuration of the UART.

UA0BUF	: UART0 transmit/receive buffer
UA0BRTH,L	: UART0 baud rate H and L are:
UA0CON	: UART0 control register
UA0MOD0,1	: UART0 mode registers 0 and 1
UA0STAT	: UART0 status register
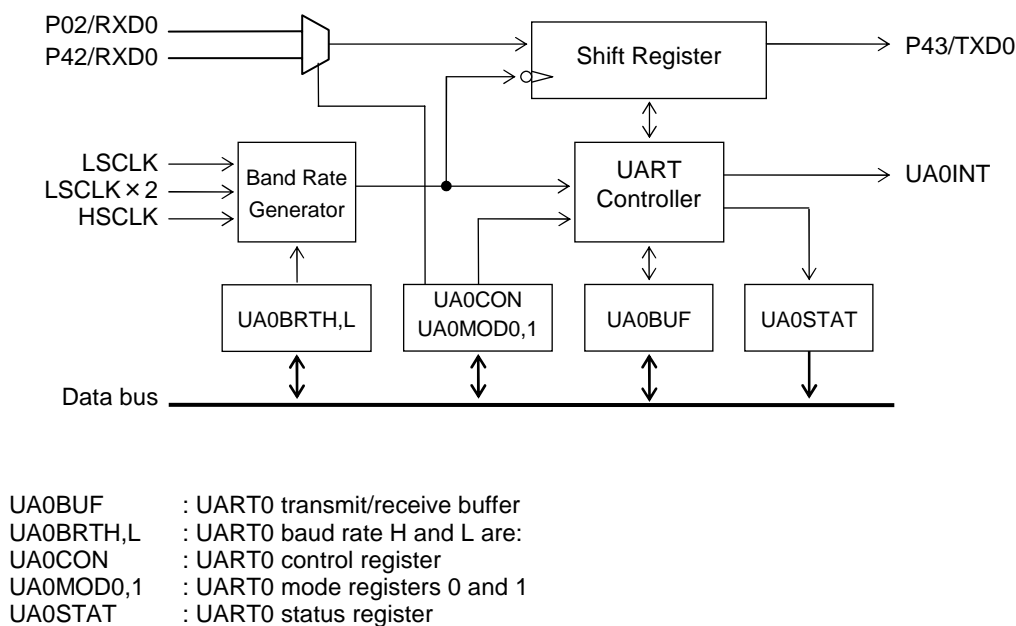
Figure 11-1   Configuration of UART

11.1.3 List of Pins

Pin name	I/O	Function
P02/RXD0	I	UART0 data input pin Used for the primary function of the P02 pin.
P42/RXD0	I	UART0 data input pin Used for the secondary function of the P42 pin.
P43/TXD0	O	UART0 data output pin Used for the secondary function of the P43 pin.

11.2 Description of Registers

11.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F290H	UART0 transmit/receive buffer	UA0BUF	—	R/W	8	00H
0F291H	UART0 control register	UA0CON	—	R/W	8	00H
0F292H	UART0 mode register 0	UA0MOD0	UA0MOD	R/W	8/16	00H
0F293H	UART0 mode register 1	UA0MOD1		R/W	8	00H
0F294H	UART0 baud rate register L	UA0BRTL	UA0BRT	R/W	8/16	0FFH
0F295H	UART0 baud rate register H	UA0BRTH		R/W	8	0FH
0F296H	UART0 status register	UA0STAT	—	R/W	8	00H

11.2.2　UART0 Transmit/Receive Buffer (UA0BUF)

Address: 0F290H
Access: R/W
Access size: 8-bit
Initial value: 00H

	7	6	5	4	3	2	1	0
UA0BUF	U0B7	U0B6	U0B5	U0B4	U0B3	U0B2	U0B1	U0B0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

UA0BUF is a special function register (SFR) to store the transmitted/received data of the UART.
In transmit mode, write transmission data to UA0BUF. To transmit the data consecutively, confirm the U0FUL flag of the UART0 status register (UA0STAT) becomes "0", then write the next transmitted data to the UA0BUF. Any value written to UA0BUF can be read.
In receive mode, since data received at termination of reception is stored in UA0BUF, read the contents of UABUF using the UART0 interrupt at termination of reception. At continuous reception, BA0BUF is updated whenever reception terminates. Any write to BA0BUF is disabled in receive mode.
The bits, which are not required when any of the 5- to 8-bit data length is selected, become invalid in transmit mode and are set to "0" in receive mode.

Note:
　　For operation in transmit mode, be sure to set the transmit mode (UA0MOD0 and UA0MOD1) before setting the
　　transmitted data in UA0BUF.

11.2.3　UART0 Control Register (UA0CON)

Address: 0F291H
Access: R/W
Access size: 8-bit
Initial value: 00H

	7	6	5	4	3	2	1	0
UA0CON	—	—	—	—	—	—	—	U0EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

UA0CON is a special function register (SFR) to start/stop communication of the UART.

[Description of Bits]

- **U0EN** (bit 0)
  The U0EN bit is used to specify the UART communication operation start. When U0EN is set to "1", UART communication starts. In transmit mode, this bit is automatically set to "0" at termination of transmission. In receive mode, receive operation is continued. To terminate reception, set the bit to "0" by software.

U0EN	Description
0	Stops communication. (Initial value)
1	Starts communication

11.2.4　UART0 Mode Register 0 (UA0MOD0)

Address: 0F292H
Access: R/W
Access size: 8/16 bit
Initial value: 00H

	7	6	5	4	3	2	1	0
UA0MOD0	−	−	U0RSS	U0RSEL	−	U0CK1	U0CK0	U0IO
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

UA0MOD0 is a special function register (SFR) to set the transfer mode of the UART.

[Description of Bits]
- **U0IO** (bit 0)
  The U0IO bit is used to select transmit or receive mode.

U0IO	Description
0	Transmit mode (initial value)
1	Receive mode

- **U0CK1, U0CK0** (bits 2, 1)
  The U0CK1 and U0CK0 bits are used to select the clock to be input to the baud rate generator of the UART.

U0CK1	U0CK0	Description
0	0	LSCLK (initial value)
0	1	LSCLK × 2
1	∗	HSCLK

- **U0RSEL** (bit 4)
  The U0RSEL bit is used to select the received data input pin for the UART.

U0RSEL	Description
0	Selects the P02 pin. (Initial value)
1	Selects the P42 pin.

- **U0RSS** (bit 5)
  U0RSS is the bit that selects the UART received data input sampling timing.

U0RSS	Description
0	Value set in the UA0BRTH and UA0BRTL registers/2 (initial value)
1	Value set in the UA0BRTH and UA0BRTL registers/2-1

Note:
　•Always set the UA0MOD0 register while communication is stopped, and do not rewrite it during communication.
　•When specifying LSCLK X 2 for the clock, enable the operation of the low-speed double clock by setting bit 2 (ENMLT) of the frequency control register 1 (FCON1) to "1".
　•When selecting the P42 pin as the received data input pin, it is necessary to configure settings for the Port 4 secondary functions. For the secondary functions of Port 4, see Chapter 15, "Port 4".

11.2.5　UART0 Mode Register 1 (UA0MOD1)

Address: 0F293H
Access: R/W
Access size: 8/16 bit
Initial value: 00H

	7	6	5	4	3	2	1	0
UA0MOD1	–	U0DIR	U0NEG	U0STP	U0PT1	U0PT0	U0LG1	U0LG0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

UA0MOD1 is a special function register (SFR) to set the transfer mode of the UART.

[Description of Bits]
- **U0LG1, U0LG0** (bits 1, 0)
  The U0LG1 and U0LG0 bits are used to specify the data length in the communication of the UART.

U0LG1	U0LG0	Description
0	0	8-bit length (initial value)
0	1	7-bit length
1	0	6-bit length
1	1	5-bit length

- **U0PT1, U0PT0** (bits 3, 2)
  The U0PT1 and U0PT0 bits are used to select "even parity", odd parity", or "no parity" in the communication of the UART.

U0PT1	U0PT0	Description
0	0	Even parity (initial value)
0	1	Odd parity
1	*	No parity bit

- **U0STP** (bit 4)
  The U0STP bit is used to select the stop bit length in the communication of the UART.

U0STP	Description
0	1 stop bit (initial value)
1	2 stop bits

- **U0NEG** (bit 5)
  The U0NEG bit is used to select positive logic or negative logic in the communication of the UART.

U0NEG	Description
0	Positive logic (initial value)
1	Negative logic

- **U0DIR** (bit 6)
  The U0DIR bit is used to select LSB first or MSB first in the communication of the UART.

U0DIR	Description
0	LSB first (initial value)
1	MSB first

Note:
   Always set the UA0MOD1 register while communication is stopped, and do not rewrite it during communication.

11.2.6 UART0 Baud Rate Registers L, H (UA0BRTL, UA0BRTH)

Address: 0F294H
Access: R/W
Access size: 8/16 bit
Initial value: 0FFH

	7	6	5	4	3	2	1	0
UA0BRTL	U0BR7	U0BR6	U0BR5	U0BR4	U0BR3	U0BR2	U0BR1	U0BR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	1	1	1	1	1

Address: 0F295H
Access: R/W
Access size: 8-bit
Initial value: 0FH

	7	6	5	4	3	2	1	0
UA0BRTH	—	—	—	—	U0BR11	U0BR10	U0BR9	U0BR8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	1	1	1	1

UA0BRTL and UA0BRTH are special function registers (SFRs) to set the count value of the baud rate generator which generates baud rate clocks.
For the relationship between the count value of the baud rate generator and baud rate, see Section 11.3.2, "Baud Rate".

Note:
    Always set the UA0BRTL and UA0BRTH registers while communication is stopped, and do not rewrite them during communication.

11.2.7 UART0 Status Register (UA0STAT)

Address: 0F296H
Access: R/W
Access size: 8-bit
Initial value: 00H

	7	6	5	4	3	2	1	0
UA0STAT	–	–	–	–	U0FUL	U0PER	U0OER	U0FER
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

UA0STAT is a special function register (SFR) to indicate the state of transmit or receive operation of the UART.
When any data is written to UA0STAT, all the flags are initialized to "0".

[Description of Bits]
- **U0FER** (bit 0)
  The U0FER bit is used to indicate occurrence of a framing error of the UART.
  When an error occurs in the start or stop bit, the U0FER bit is set to "1". This bit is updated each time reception is completed.
  The U0FER bit is fixed to "0" in transmit mode.

U0FER	Description
0	No framing error (initial value)
1	With framing error

- **U0OER** (bit 1)
  The U0OER bit is used to indicate occurrence of an overrun error of the UART.
  If the received data in the transmit/receive buffer (UA0BUF) is received again before it is read, this bit is set to "1". Even if reception is stopped by the U0EN bit and then reception is restarted, this bit is set to "1" if the previously received data is not read. Therefore, make sure that data is always read from the transmit/receive buffer even if the data is not required.
  The U0OER bit is fixed to "0" in transmit mode.

U0OER	Description
0	No overrun error (initial value)
1	Overrun error

- **U0PER** (bit 2)
  The U0PER bit is used to indicate occurrence of a parity error of the UART.
  When the parity of the received data and the parity bit attached to the data do not coincide, this bit is set to "1".
  U0PER is updated whenever data is received.
  The U0PER bit is fixed to "0" in transmit mode.

U0PER	Description
0	No parity error (initial value)
1	Parity error

- **U0FUL** (bit 3)

    The U0FUL bit is used to indicate the state of the transmit/receive buffer of the UART.

    When the transmitted data is written in UA0BUF in transmit mode, this bit is set to "1" and when this transmitted data is transferred to the shift register, this bit is set to "0". To transmit the data consecutively, confirm the U0FUL flag becomes "0", then write the next transmitted data to the UA0BUF.

    The U0FUL bit is fixed to "0" in receive mode.

U0FUL	Description
0	There is no data in the transmit/receive buffer. (Initial value)
1	There is data in the transmit/receive buffer.

11.3 Description of Operation

11.3.1　Transfer Data Format

In the transfer data format, one frame contains a start bit, a data bit, a parity bit, and a stop bit. In this format, 5 to 8 bits can be selected as data bit. For the parity bit, "with parity bit", "without parity bit", "even parity", or "odd parity" can be selected. For the stop bit, "1 stop bit" or "2 stop bits" are available and for the transfer direction, "LSB first" or "MSB first" are available for selection. For serial input/output logic, positive logic or negative logic can be selected.
All these options are set with the UART0 mode register (UA0MOD1).
Figure 11-2 and Figure 11-3 show the positive logic input/output format and negative logic input/output format, respectively.
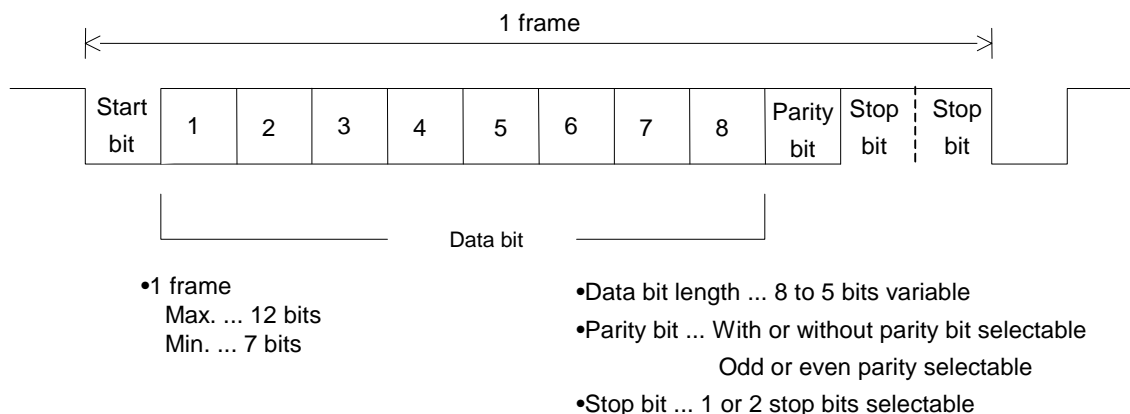
Figure 11-2　Positive Logic Input/Output Format
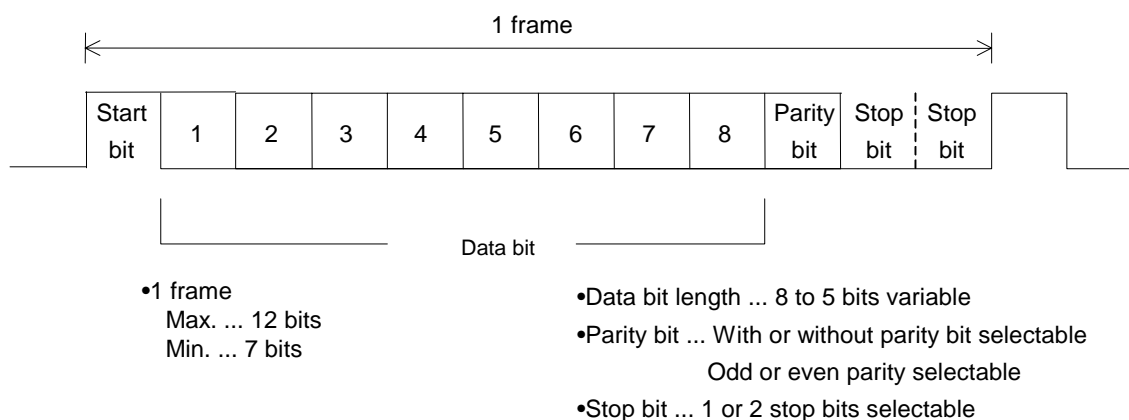
Figure 11-3　Negative Logic Input/Output Format

11.3.2 Baud rate

Baud rates are generated by the baud generator.

The baud rate generator generates a baud rate by counting the clock selected by the baud rate clock selection bits (U0CK1, U0CK0) of the UART0 mode register 0 (UA0MOD0). The count value of the baud rate generator can be set by writing it in the UART0 baud rate register H or L (UA0BRTH, UA0BRTL). The maximum count is 4096.

The setting values of UA0BRTH and UA0BRTL are expressed by the following equation.

$$\text{UA0BRTH, L} = \frac{\text{Clock frequency (Hz)}}{\text{Baud rate (bps)}} - 1$$

Table 11-2 lists the count values for typical baud rates.

Table 11-2   Count Values for Typical Baud Rates

Baud rate	Baud rate generator Clock selection			Baud rate generator counter value				Error [%]
	Baud rate Clock	U0CK1	U0CK0	Count value	Period of one bit	UA0BRTH	UA0BRTL	
1200bps	32.768kHz	0	0	27	Approximately 824us	00H	1AH	1.1
2400bps	32.768kHz	0	0	14	Approximately 427us	00H	0DH	-2.5
	65.536kHz	0	1	27	Approximately 412us	00H	1AH	1.1
4800bps	32.768kHz	0	0	7	Approximately 214us	00H	06H	-2.5
	65.536kHz	0	1	14	Approximately 214us	00H	0DH	-2.5
	500kHz	1	∗	104	Approximately 208us	00H	67H	0.2
9600bps	65.536kHz	0	1	7	Approximately 107us	00H	06H	-2.5
	500kHz	1	∗	52	Approximately 104us	00H	33H	0.2
19200bps	500kHz	1	∗	26	Approximately 52us	00H	01BH	0.2
38400bps	500kHz	1	∗	13	Approximately 26us	00H	00CH	0.2

Note:

When using 65.536KHz (LSCLK X 2) for the baud rate generator input clock, enable the operation of the low-speed double clock by setting bit 2 (ENMLT) of the frequency control register 1 (FCON1) to "1".

When the baud rate clock generator input clock selection is set to 500kHz, an error of 500kHz±25% may occur. To set the baud rate with accuracy, set the baud rate generator counter value by referring to the frequency measurement modes for Timers 2 and 3 (Sections 9.3.3).

11.3.3 Transmitted Data Direction

Figure 11-4 shows the relationship between the transmit/receive buffer and the transmitted/received data.

Data length: 8 bits

LSB reception $\longrightarrow$ | U0B7 | U0B6 | U0B5 | U0B4 | U0B3 | U0B2 | U0B1 | U0B0 | $\longrightarrow$ LSB reception
MSB reception $\longleftarrow$ | | | | | | | | | $\longleftarrow$ MSB reception

Data length: 7 bits

LSB reception $\longrightarrow$ | U0B6 | U0B5 | U0B4 | U0B3 | U0B2 | U0B1 | U0B0 | $\longrightarrow$ LSB reception
MSB reception $\longleftarrow$ | | | | | | | | $\longleftarrow$ MSB reception

U0B7 is "0" at completion of

Data length: 6 bits

LSB reception $\longrightarrow$ | U0B5 | U0B4 | U0B3 | U0B2 | U0B1 | U0B0 | $\longrightarrow$ LSB reception
MSB reception $\longleftarrow$ | | | | | | | $\longleftarrow$ MSB reception

U0B7 and U0B6 are "0" at completion

Data length: 5 bits

LSB reception $\longrightarrow$ | U0B4 | U0B3 | U0B2 | U0B1 | U0B0 | $\longrightarrow$ LSB reception
MSB reception $\longleftarrow$ | | | | | | $\longleftarrow$ MSB reception

U0B7, U0B6, and U0B5 are "0" at
completion of reception.

Figure 11-4 Relationship between Transmit/Receive Buffer and Transmitted/Received Data

Note:
  When the TXD0 pin is set to serve the secondary function output in receive mode, "H" level is output from the TXD0 output.

11.3.4 Transmit Operation

Transmission is started by setting the U0IO bit of the UART0 mode register 0 (UA0MOD0) to "0" to select transmit mode and setting the U0EN bit of the UART0 control register (UA0CON) to "1".
Figure 11-5 shows the operation timing for transmission.

When the U0EN bit is set to "1" (①), the baud rate generator generates an internal transfer clock of the baud rate set and starts transmission.
The start bit is output to the TXD0 pin by the falling edge of the internal transfer clock (②). Subsequently, the transmitted data, a parity bit, and a stop bit are output.
When the start bit is output (②), a UART0 interrupt is requested. In the UART0 interrupt routine, the next data to be transmitted is written to the transmit/receive buffer (UA0BUF).
When the next data to be transmitted is written to the transmit/receive buffer (UA0OBUF), the transmit buffer status flag (U0FUL) is set to "1" (③) and a UART0 interrupt is requested on the falling edge of the internal transfer clock (④) after transmission of the stop bit. If the UART0 interrupt routine is terminated without writing the next data to the transmit/receive buffer, the U0FUL bit is not set to "1" (⑤) and transmission continues up to the transmission of the stop bit, then the U0EN bit is reset to "0" and a UART0 interrupt is requested.
The valid period for the next transmit data to be written to the transmit/receive buffer is from the generation of an interrupt to the termination of stop bit transmission. (⑥)
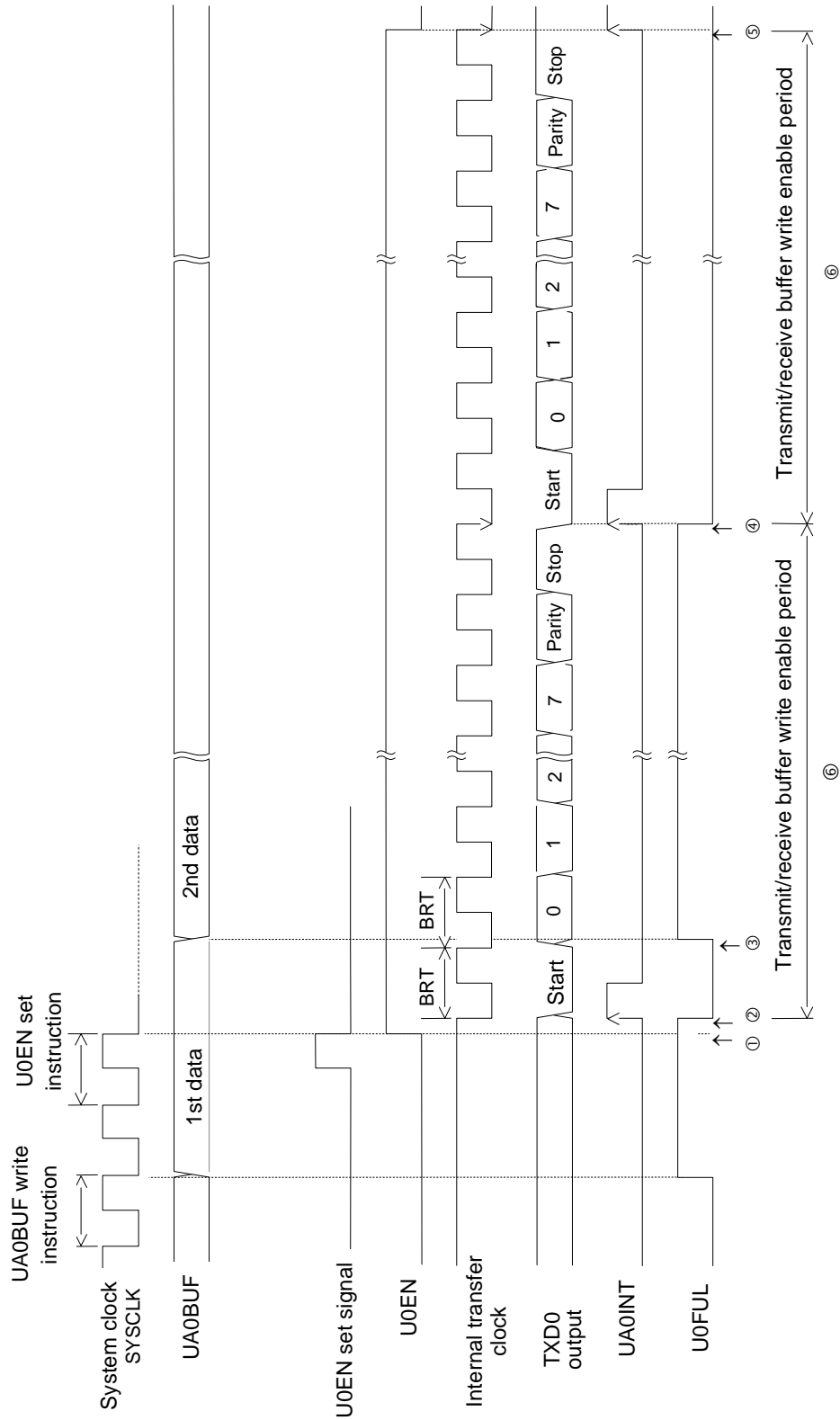
Figure 11-5　Operation Timing in Transmission

11.3.5 Receive Operation

Select the received data pin using the U0RSEL bit of the UART0UART0 mode register 0 (UA0MOD0). Select the receive mode by setting the U0IO bit of the UART0 mode register 0 (UA0MOD0) to "1". Then, set the U0EN bit of the UART0 control register (UA0CON) to "1" to start receiving data.
Figure 11-6 shows the operation timing for reception.

When receive operation starts, the LSI checks the data sent to the input pin RXD0 and waits for the arrival of a start bit. When detecting a start bit (①), the LSI generates the internal transfer clock of the baud rate set with the start bit detect point as a reference and performs receive operation.
The shift register shifts in the data input to RXD on the rising edge of the internal transfer clock. The data and parity bit are shifted into the shift register and 5- to 8- bit received data is transferred to the transmit/receive buffer (UA0BUF) concurrently with the fall of the internal transfer clock of ③.
The LSI requests a UART0 interrupt on the rising edge of the internal transfer clock subsequent to the internal transfer clock by which the received data was fetched (④) and checks for a stop bit error and a parity bit error. When an error is detected, the LSI sets the corresponding bit of the UART0 status register (UA0STAT) to "1".

Parity error   : S0PER ＝"1"
Overrun error   : S0OER ＝"1"
Framing error   : S0FER ＝"1"

As shown in Figure 11-6, the rise of the internal transfer clock is set so that it may fall into the middle of the bit interval of the received data.
Reception continues until the U0EN bit is reset to "0" by the program. When the U0EN bit is reset to "0" during reception, the received data may be destroyed. When the U0EN bit is reset to "0" during the "U0EN reset enable period" in Figure 11-6, the received data is protected.
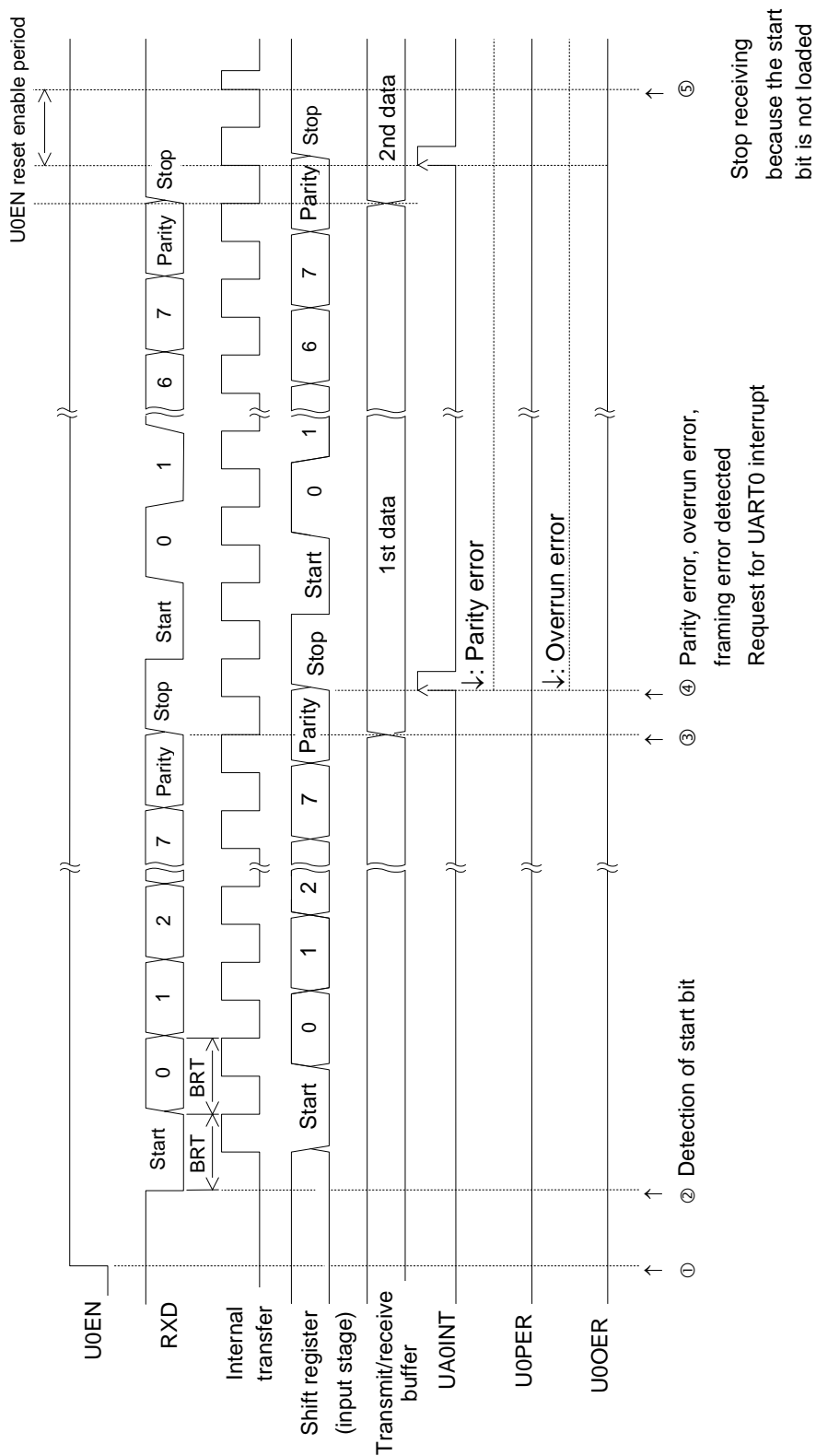
Figure 11-6   Operation Timing in Reception

11.3.5.1 Detection of Start Bit

The Start bit is sampled using the baud rate generator clock (LSCLK, LSCLK x 2, HSCLK) selected by the U0CK1 and U0CK0 bits of the UARTn mode register 0 (UA0MOD0). Therefore, the start bit detection may be delayed for one cycle of the baud rate generate clock at the maximum.
Figure 11-7 shows the start bit detection timing.
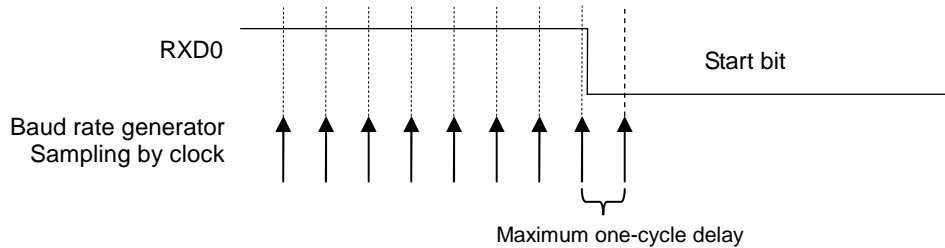
Figure 11-7   Start Bit Detection Timing (Positive Logic)

11.3.5.2 Sampling Timing

When the Start bit is detected, the received data that was input to the RXD0 is sampled almost at the center of the baud rate, then loaded to the shift register.
The loading sampling timing of this shift register can be adjusted for one clock of the baud rate generator clock, using the U0RSS bit of the UART0 mode register 0 (UA0MOD0).
Figure 11-8 shows the relationship between the U0RSS bit and the sampling timing.
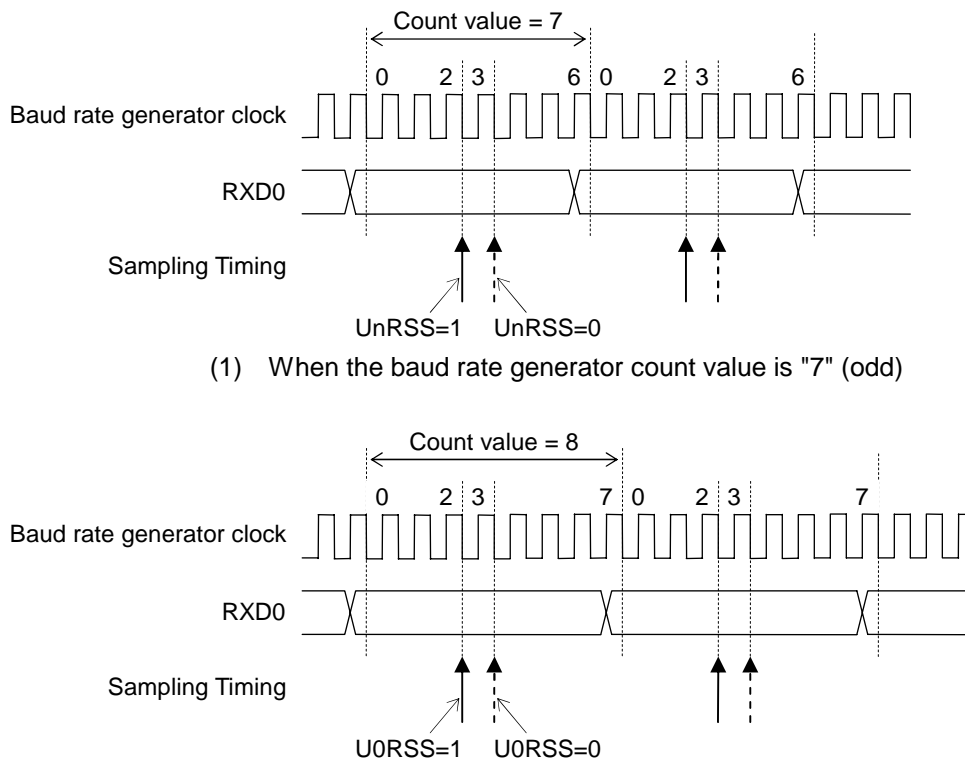
(1)   When the baud rate generator count value is "7" (odd)

(2)   When the baud rate generator count value is "8" (even)

Figure 11-8   Relationship between UORSS Bit and Sampling Timing

11.3.5.3 Receive Margin

If there is an error between the sender baud rate and the baud rate generated by the baud rate generator of this LSI, the error accumulates until the last stop bit loading in one frame, decreasing the receive margin. This receive margin needs to be fully considered, particularly when the baud rate generator clock uses a lower frequency such as LSCLK and LSCLK x 2 to realize a higher bit rate (e.g., 4800bps, 9600bps).

Figure 11-9 shows the baud rate errors and receive margin waveforms.
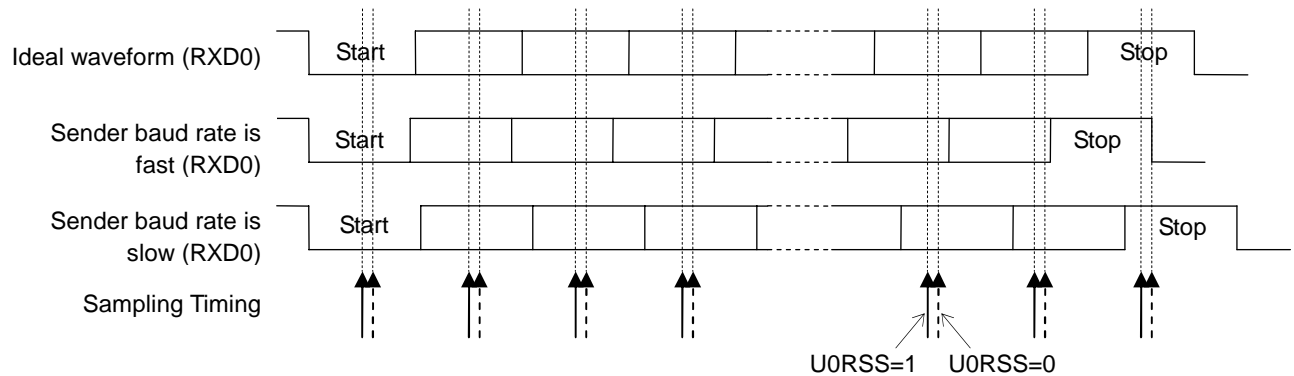
Figure 11-9   Baud Rate Error and Receive Margin

Note:

In system designing, ensure a sufficient receive margin considering the baud rate difference between sender and receiver, start bit detection delay, distortion in receive data, and influence of noise.

11.4 Specifying port registers

To enable the UART function, the applicable bit of each related port register needs to be set. See Chapter 12, "Port 0" and Chapter 15, "Port 4" for detail about the port registers.

11.4.1 Functioning P43(TXD0) and P42(RXD0) as the UART

Set P43MD1-P42MD1 bits(bit3-bit2 of P4MOD1 register) to "0" and set P43MD0-P42MD0(bit3-bit2 of P4MOD0 register) to "1", for specifying the UART as the secondary function of P43 and P42.

Register name	P4MOD1 register (Address: 0F225H)							
Bit	7	6	5	4	3	2	1	0
Bit name	P47MD1	P46MD1	P45MD1	P44MD1	**P43MD1**	**P42MD1**	P41MD1	P40MD1
Setting value	*	*	*	*	**0**	**0**	*	*

Register name	P4MOD0 register (Address: 0F224H)							
Bit	7	6	5	4	3	2	1	0
Bit name	P47MD0	P46MD0	P45MD0	P44MD0	**P43MD0**	**P42MD0**	P41MD0	P40MD0
Setting value	*	*	*	*	**1**	**1**	*	*

Set the P43C1 bit (P4CON1 register's bit 3) to "1", the P43C0 bit (P4CON0 register's bit 3) to "1", and the P43DIR bit (P4DIR register's bit 3) to "0" for specifying the state mode of the P43 pin to CMOS output.
Set P42DIR bit (bit2 of P4DIR register) to "1" for specifying the P42 as an input pin.
The set value ($) is arbitrary for the P42C1 and P42C0 bits. Select an arbitrary input mode depending on the state of the external circuit to which the P42 pin is connected.

Register name	P4CON1 register (Address: 0F223H)							
Bit	7	6	5	4	3	2	1	0
Bit name	P47C1	P46C1	P45C1	P44C1	**P43C1**	**P42C1**	P41C1	P40C1
Setting value	*	*	*	*	**1**	**$**	*	*

Register name	P4CON0 register (Address: 0F222H)							
Bit	7	6	5	4	3	2	1	0
Bit name	P47C0	P46C0	P45C0	P44C0	**P43C0**	**P42C0**	P41C0	P40C0
Setting value	*	*	*	*	**1**	**$**	*	*

Register name	P4DIR register (Address: 0F221H)							
Bit	7	6	5	4	3	2	1	0
Bit name	P47DIR	P46DIR	P45DIR	P44DIR	**P43DIR**	**P42DIR**	P41DIR	P40DIR
Setting value	*	*	*	*	**0**	**1**	*	*

The P43D to P42D bits (P4D register bits 3 to 2) data can either be "0" or "1" (not need to be set).

Register name	P4D register (Address: 0F220H)							
Bit	7	6	5	4	3	2	1	0
Bit name	P47D	P46D	P45D	P44D	**P43D**	**P42D**	P41D	P40D
Setting value	*	*	*	*	******	******	*	*

* : Bit not related to the UART function
** : Don't care $: Optional

[Note:]
The receive pin (RXD) is selected by U0RSEL bit (bit4 of UA0MOD0 register). The initial value "0" selects the P02 and the value "1" selects the P43.

11.4.2 Functioning P43(TXD0) and P02(RXD0) as the UART

Set P43MD1 bit (bit3 of P4MOD1 register) to "0" and set P43MD0(bit3 of P4MOD0 register) to "1", for specifying the UART as the secondary function of P43.

Register name	P4MOD1 register (Address: 0F225H)							
Bit	7	6	5	4	**3**	2	1	0
Bit name	P47MD1	P46MD1	P45MD1	P44MD1	**P43MD1**	P42MD1	P41MD1	P40MD1
Setting value	*	*	*	*	**0**	$	*	*

Register name	P4MOD0 register (Address: 0F224H)							
Bit	7	6	5	4	**3**	2	1	0
Bit name	P47MD0	P46MD0	P45MD0	P44MD0	**P43MD0**	P42MD0	P41MD0	P40MD0
Setting value	*	*	*	*	**1**	$	*	*

Set the P43C1 bit (P4CON1 register's bit 3) to "1", the P43C0 bit (P4CON0 register's bit 3) to "1", and the P43DIR bit (P4DIR register's bit 3) to "0" for specifying the state mode of the P43 pin to CMOS output.

Register name	P4CON1 register (Address: 0F223H)							
Bit	7	6	5	4	**3**	2	1	0
Bit name	P47C1	P46C1	P45C1	P44C1	**P43C1**	P42C1	P41C1	P40C1
Setting value	*	*	*	*	**1**	*	*	*

Register name	P4CON0 register (Address: 0F222H)							
Bit	7	6	5	4	**3**	2	1	0
Bit name	P47C0	P46C0	P45C0	P44C0	**P43C0**	P42C0	P41C0	P40C0
Setting value	*	*	*	*	**1**	*	*	*

Register name	P4DIR register (Address: 0F221H)							
Bit	7	6	5	4	**3**	2	1	0
Bit name	P47DIR	P46DIR	P45DIR	P44DIR	**P43DIR**	P42DIR	P41DIR	P40DIR
Setting value	*	*	*	*	**0**	*	*	*

The P43D bit (P4D register bit 3) data can either be "0" or "1" (not need to be set).

Register name	P4D register (Address: 0F220H)							
Bit	7	6	5	4	**3**	2	1	0
Bit name	P47D	P46D	P45D	P44D	**P43D**	P42D	P41D	P40D
Setting value	*	*	*	*	****	*	*	*

The P02 pin is an input-only pin and does not need input/output selection by the register. The set value ($) is arbitrary for the P02C1 and P02C0 bits. Select an arbitrary input mode depending on the state of the external circuit to which the P02 pin is connected.

Register name	P0CON1 register (Address: 0F207H)							
Bit	7	6	5	4	3	**2**	1	0
Bit name	-	-	-	-	P03C1	**P02C1**	P01C1	P00C1
Setting value	-	-	-	-	*	**$**	*	*

Register name	P0CON0 register (Address: 0F206H)							
Bit	7	6	5	4	3	**2**	1	0
Bit name	-	-	-	-	P03C0	**P02C0**	P01C0	P00C0
Setting value	-	-	-	-	*	**$**	*	*

The P02D bit (P0D register bit 2) data can either be "0" or "1" (not need to be set).

Register name	P0D register (Address: 0F204H)							
Bit	7	6	5	4	3	**2**	1	0
Bit name	-	-	-	-	P03D	**P02D**	P01D	P00D
Setting value	-	-	-	-	*	**	*	*

- : Bit that does not exist
* : Bit not related to the UART function
** : Don't care　　　　　　　　　　$: Optional

Note:
•The receive pin (RXD) is selected by U0RSEL bit (bit4 of UA0MOD0 register). The initial value "0" selects the P02 and the value "1" selects the P43.
•Even if the P42 pin is selected as RXD0 by the P42MD1, P42MD0, P42C1, P42C0, and P42IDR bits, the P02 pin will be selected as RXD0 when the U0RSEL bit of the UA0MOD0 register is "0".
•P02(Port 0) is an input-only port, does not have registers that can select data direction(input or output) or mode(primary or secondary function).

Port 0

12. Port 0

12.1 Overview

This LSI includes the 4-bit, input-only Port 0 (P00 to P03).

12.1.1 Features

- All bits support a maskable interrupt function.
- Allows selection of interrupt disabled mode, falling-edge interrupt mode, rising-edge interrupt mode, or both-edge interrupt mode for each bit.
- Allows selection of with/without interrupt sampling for each bit. (Sampling frequency: T16KHZ)
- Allows selection of high-impedance input mode, input mode with a pull-down resistor, or input mode with a pull-up resistor for each bit.
- The P00 and P01 pins can be used as the trigger input pins of the capture circuit and the P02 pin can be used as the RXD0 input pin of UART0.

12.1.2 Configuration

Figure 12-1 shows the configuration of Port 0.

P0D   : Port 0 data register
P0CON0   : Port 0 control register 0
P0CON1   : Port 0 control register 1
EXICON0 : External interrupt control register 0
EXICON1 : External interrupt control register 1
EXICON2 : External interrupt control register 2
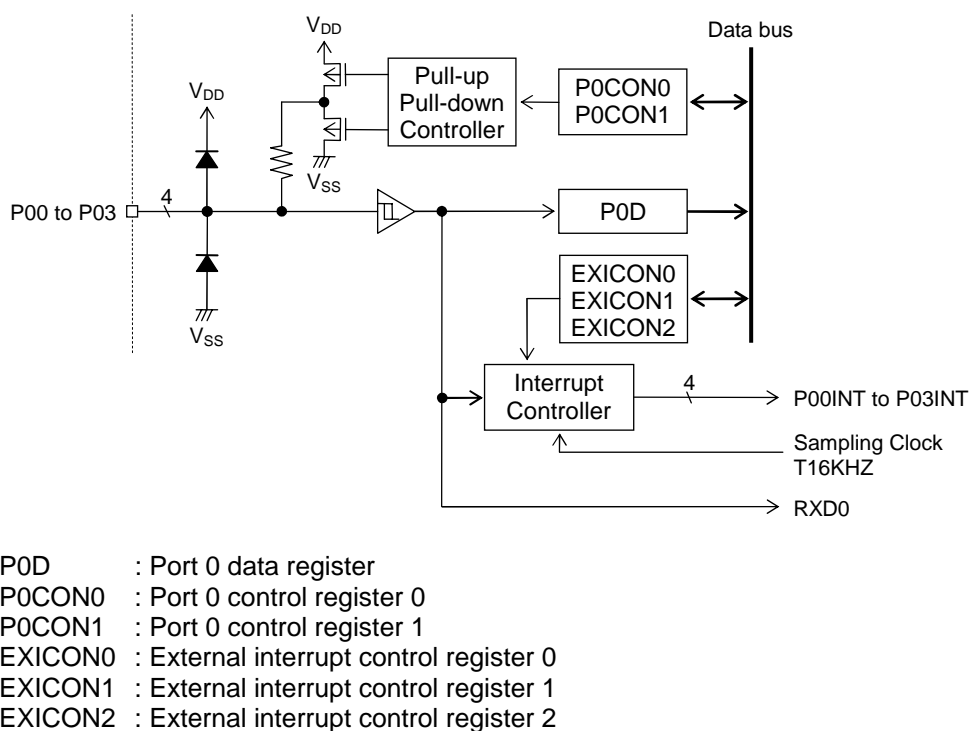
Figure 12-1   Configuration of Port 0

12.1.3 List of Pins

Pin name	I/O	Function
P00/EXI0/CAP0	I	Input port, External 0 interrupt, Capture 0 trigger signal input
P01/EXI1/CAP1	I	Input port, External 1 interrupt, Capture 1 trigger signal input
P02/EXI2/RXD0	I	Input port, External 2 interrupt, UART0 data input (RXD0)
P03/EXI3	I	Input port, External 3 interrupt

12.2 Description of Registers

12.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F204H	Port 0 data register	P0D	—	R	8	Depends on pin state
0F206H	Port 0 control register 0	P0CON0	P0CON	R/W	8/16	00H
0F207H	Port 0 control register 1	P0CON1		R/W	8	00H
0F020H	External interrupt control register 0	EXICON0	—	R/W	8	00H
0F021H	External interrupt control register 1	EXICON1	—	R/W	8	00H
0F022H	External interrupt control register 2	EXICON2	—	R/W	8	00H

12.2.2 Port 0 Data Register (P0D)

Address: 0F204H
Access: R
Access size: 8-bit
Initial value: Depends on pin state

	7	6	5	4	3	2	1	0
P0D	—	—	—	—	P03D	P02D	P01D	P00D
	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	x	x	x	x

P0D is a special function register (SFR) to only read the pin level of Port 0.

[Description of Bits]
- **P03D to P00D** (bits 3 to 0)
  The P03D to P00D bits are used to read the pin level of Port 0.

P03D	Description
0	P03 pin input: "L" level
1	P03 pin input: "H" level

P02D	Description
0	P02 pin input: "L" level
1	P02 pin input: "H" level

P01D	Description
0	P01 pin input: "L" level
1	P01 pin input: "H" level

P00D	Description
0	P00 pin input: "L" level
1	P00 pin input: "H" level

12.2.3　Port 0 Control Registers 0, 1 (P0CON0, P0CON1)

Address: 0F206H
Access: R/W
Access size: 8/16 bit
Initial value: 00H

	7	6	5	4	3	2	1	0
P0CON0	—	—	—	—	P03C0	P02C0	P01C0	P00C0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F207H
Access: R/W
Access size: 8-bit
Initial value: 00H

	7	6	5	4	3	2	1	0
P0CON1	—	—	—	—	P03C1	P02C1	P01C1	P00C1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P0CON0 and P0CON1 are special function registers (SFRs) to select the input mode of Port 0.

[Description of Bits]
- P03C0 to P00C0, P03C1 to P00C1 (bits 3 to 0)
  The P03C0 to P00C0 bits and the P03C1 to P00C1 bits are used to select high-impedance input mode, input mode with a pull-down resistor, or input mode with a pull-up resistor. The P0nC0 bit and the P0nC1 bit determine the input mode of P0n (Example: When P02C0 = "0" and P02C1 = "1", P02 is in input mode with a pull-up resistor).

P03C1-P00C1	P03C0-P00C0	Description
0	0	High-impedance input mode (initial value)
0	1	Input mode with a pull-down resistor
1	0	Input mode with a pull-up resistor
1	1	High-impedance input mode

12.2.4 External Interrupt Control Registers 0, 1 (EXICON0, EXICON1)

Address: 0F020H
Access: R/W
Access size: 8-bit
Initial value: 00H

	7	6	5	4	3	2	1	0
EXICON0	—	—	—	—	P03E0	P02E0	P01E0	P00E0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F021H
Access: R/W
Access size: 8-bit
Initial value: 00H

	7	6	5	4	3	2	1	0
EXICON1	—	—	—	—	P03E1	P02E1	P01E1	P00E1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

EXICON0 and EXICON1 are special function registers (SFRs) to select an interrupt edge of Port 0.

[Description of Bits]
- **P03E0 to P00E0**, **P03E1 to P00E1** (bits 3 to 0)
  The P03E0 to P00E0 bits and the P03E1 to P00E1 bits are used to select interrupt disabled mode, falling-edge interrupt mode, rising-edge interrupt mode, or both-edge interrupt mode. The P0nE0 bit and the P0nE1 bit determine the interrupt mode of P0n (Example: When P02E0 = "0" and P02E1 = "1", P02 is in rising-edge interrupt mode).

P03E1-P00E1	P03E0-P00E0	Description
0	0	Interrupt disabled (initial value)
0	1	Falling-edge interrupt mode
1	0	Rising-edge interrupt mode
1	1	Both-edge interrupt mode

12.2.5 External Interrupt Control Register 2 (EXICON2)

Address: 0F022H
Access: R/W
Access size: 8-bit
Initial value: 00H

	7	6	5	4	3	2	1	0
EXICON2	—	—	—	—	P03SM	P02SM	P01SM	P00SM
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

EXICON2 is a special function register (SFR) to select whether the Port 0 interrupt is with sampling or without sampling.

[Description of Bits]
- **P03SM to P00SM** (bits 3 to 0)
  The P03SM to P00SM bits are used to select detection of signal edge for Port 0 interrupts with or without sampling. The sampling clock is T16KHZ of the low-speed time base counter (LTBC).

P03SM	Description
0	Detects the input signal edge for a P03 interrupt without sampling (initial value).
1	Detects the input signal edge for a P00 interrupt with sampling.

P02SM	Description
0	Detects the input signal edge for a P02 interrupt without sampling (initial value).
1	Detects the input signal edge for a P00 interrupt with sampling.

P01SM	Description
0	Detects the input signal edge for a P01 interrupt without sampling (initial value).
1	Detects the input signal edge for a P00 interrupt with sampling.

P00SM	Description
0	Detects the input signal edge for a P00 interrupt without sampling (initial value).
1	Detects the input signal edge for a P00 interrupt with sampling.

Note:
In STOP mode, since the 16 kHz sampling clock stops, no sampling is performed regardless of the values set in P00SM to P03SM.

12.3 Description of Operation

For each pin of Port 0, the setting of the Port 0 control registers 0 and 1 (P0CON0 and P0CON1) allows selection of high-impedance input mode, input mode with a pull-down resistor, or input mode with a pull-up resistor. High-impedance input mode is selected at system reset.
The pin level of Port 0 can be read by reading the Port 0 data register (P0D).

12.3.1 External Interrupt / Secondary Function

The Port 0 pins (P00, P01, P02, P03) can be used for P00 to P03 interrupts (P00INT to P03INT). The P00 to P03 interrupts are maskable and interrupt enable or disable can be selected. For interrupts, see Chapter 5, "Interrupt." The P00 and P01 pins can be used as the trigger input to the capture circuit, the P02 pin as the RXD0 input to the UART0.
For the capture function, see Chapter 8, "Capture." For the UART function, see Chapter 11, "UART."

12.3.2 Interrupt Request

When an interrupt edge selected with the external interrupt control register 0, 1, or 2 (EXICON0, EXICON1, or EXICON2) occurs at a Port 0 pin, any of the maskable P00 to P03 interrupts (P00INT to P03INT) occurs.
Figure 12-2 shows the P00 to P03 interrupt generation timing in rising-edge interrupt mode, in falling-edge interrupt mode, and in both-edge interrupt mode without sampling and the P00 to P03 interrupt generation timing in rising-edge interrupt mode with sampling.
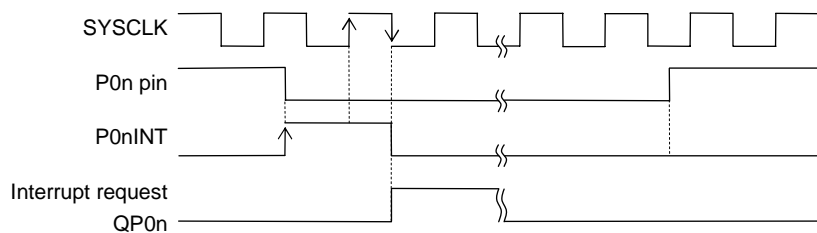
(a) When Falling-Edge Interrupt Mode without Sampling is Selected
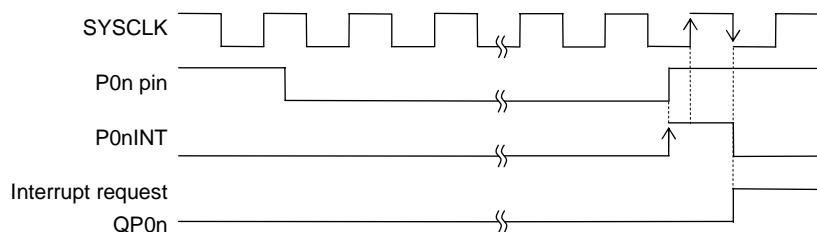
(b) When Rising-Edge Interrupt Mode without Sampling is Selected
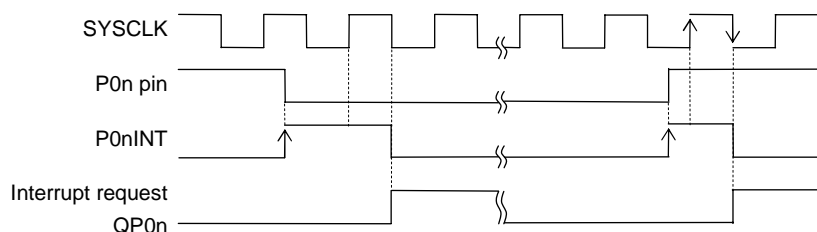
(c) When Both-Edge Interrupt Mode without Sampling is Selected
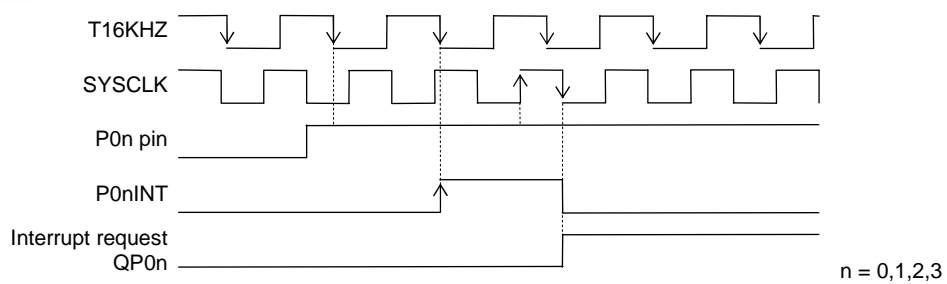
(d) When Rising-Edge Interrupt Mode with Sampling is Selected

Figure 12-2   P00 to P03 Interrupts Generation Timing

Port 2

13. Port 2

13.1 Overview

This LSI includes 4-bit Port 2 (P20 to P22, and P24) dedicated to output.
Port 2 can output low-speed clock (LSCLK), high-speed clock (OUTCLK) , and melody waveform as a secondary function. For the clock output, see Chapter 6, "Clock Generation Circuit." For the Melody 0 (MD0) output, see Chapter 18, "Melody Driver."

13.1.1 Features

- Allows direct LED drive.
- Allows selection of high-impedance output mode, P-channel open drain output mode, N-channel open drain output mode, or CMOS output mode for each bit.
- Allows output of low-speed clock (LSCLK), high-speed clock (OUTCLK), and Melody 0 (MD0) waveform (PWM0) as a secondary function.

13.1.2 Configuration

Figure 13-1 shows the configuration of Port 2.
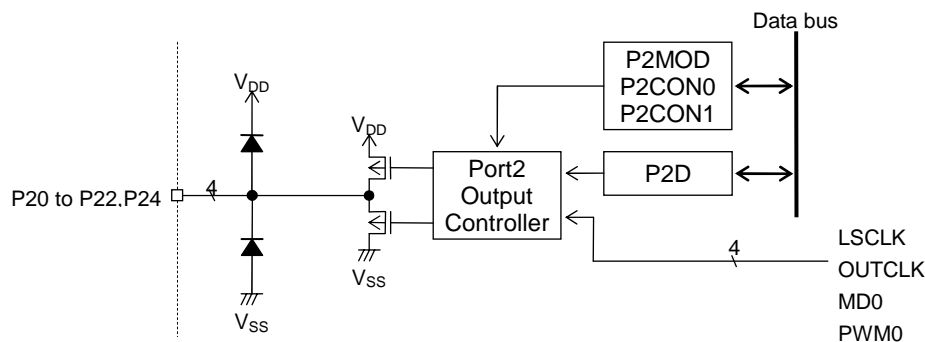
P2D   : Port 2 data register
P2CON0   : Port 2 control register 0
P2CON1   : Port 2 control register 1
P2MOD   : Port 2 mode register

Figure 13-1   Configuration of Port 2

13.1.3 List of Pins

Pin name	I/O	Primary function	Secondary function
P20/LED0/LSCLK	O	Output port	Low-speed clock output (LSCLK)
P21/LED1/OUTCLK	O	Output port	High-speed clock output (OUTCLK)
P22/LED2/MD0	O	Output port	Melody 0 output (MD0)
P24/LED4	O	Output port	—

13.2 Description of Registers

13.2.1　List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F210H	Port 2 data register	P2D	—	R/W	8	00H
0F212H	Port 2 control register 0	P2CON0	P2CON	R/W	8/16	00H
0F213H	Port 2 control register 1	P2CON1		R/W	8	00H
0F214H	Port 2 mode register	P2MOD	—	R/W	8	00H

13.2.2 Port 2 Data Register (P2D)

Address: 0F210H
Access: R/W
Access size: 8-bit
Initial value: 00H

	7	6	5	4	3	2	1	0
P2D	—	—	—	P24D	—	P22D	P21D	P20D
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P2D is a special function register (SFR) to set the output value of the Port 2. The value of this register is output to Port 2. The value written to P2D is readable.

[Description of Bits]
- **P24D** (bits 4 to 0)
  The P24D and P22D to P20D bits are used to set the output value of the Port 2 pin.

P24D	Description
0	Output level of the P24 pin: "L"
1	Output level of the P24 pin: "H"

P22D	Description
0	Output level of the P22 pin: "L"
1	Output level of the P22 pin: "H"

P21D	Description
0	Output level of the P21 pin: "L"
1	Output level of the P21 pin: "H"

P20D	Description
0	Output level of the P20 pin: "L"
1	Output level of the P20 pin: "H"

13.2.3 Port 2 Control Registers 0, 1 (P2CON0, P2CON1)

Address: 0F212H
Access: R/W
Access size: 8/16 bit
Initial value: 00H

	7	6	5	4	3	2	1	0
P2CON0	—	—	—	P24C0	—	P22C0	P21C0	P20C0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F213H
Access: R/W
Access size: 8-bit
Initial value: 00H

	7	6	5	4	3	2	1	0
P2CON1	—	—	—	P24C1	—	P22C1	P21C1	P20C1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P2CON0 and P2CON1 are special function registers (SFRs) to select the output state of the output pin Port 2.

[Description of Bits]
- **P24C0, P22C0 to P20C0, P24C1, P22C1 to P20C1** (bits 4 and 2 to 0)
  The P24C0, P22C0 to P20C0, P24C1, and P22C1 to P20C1 bits are used to select high-impedance output mode,
  P-channel open drain output mode, N-channel open drain output mode, or CMOS output mode.
  To directly drive LEDs, select N-channel open drain output mode.

P24C1	**P24C0**	Description
0	0	P24 pin: In high-impedance output mode (initial value)
0	1	P24 pin: In P-channel open drain output mode
1	0	P24 pin: In N-channel open drain output mode
1	1	P24 pin: In CMOS output mode

P22C1	**P22C0**	Description
0	0	P22 pin: In high-impedance output mode (initial value)
0	1	P22 pin: In P-channel open drain output mode
1	0	P22 pin: In N-channel open drain output mode
1	1	P22 pin: In CMOS output mode

P21C1	**P21C0**	Description
0	0	P21 pin: In high-impedance output mode (initial value)
0	1	P21 pin: In P-channel open drain output mode
1	0	P21 pin: In N-channel open drain output mode
1	1	P21 pin: In CMOS output mode

P20C1	**P20C0**	Description
0	0	P20 pin: In high-impedance output mode (initial value)
0	1	P20 pin: In P-channel open drain output mode
1	0	P20 pin: In N-channel open drain output mode
1	1	P20 pin: In CMOS output mode

13.2.4　Port 2 Mode Register (P2MOD)

Address: 0F214H
Access: R/W
Access size: 8-bit
Initial value: 00H

	7	6	5	4	3	2	1	0
P2MOD	—	—	—	—	—	P22MD	P21MD	P20MD
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P2MOD is a special function register (SFR) to select the primary function or the secondary function of Port 2.

[Description of Bits]

- **P22MD** (bit 2)
  The P22MD bit is used to select the primary function or the secondary function of the P22 pin.

P22MD	Description
0	General-purpose output port function (initial value)
1	Melody 0 (MD0) output function

- **P21MD** (bit 1)
  The P21MD bit is used to select the primary function or the secondary function of the P21 pin.

P21MD	Description
0	General-purpose output port function (initial value)
1	High-speed clock (OUTCLK) output function

- **P20MD** (bit 0)
  The P20MD bit is used to select the primary function or the secondary function of the P20 pin.

P20MD	Description
0	General-purpose output port function (initial value)
1	Low-speed clock (LSCLK) output function

Note:
- Secondary function is not settable for P24 pin.
- P2 (Port 2) is an output-only pin and does not have the register to select the data direction(input or output).
- The output characteristics of the P2 pins (P20, P21, and P22) are VOL1 and VOH1 (described in "Appendix C Electrical Characteristics") when each bit (P20MD, P21MD, and P22MD) of the corresponding P2MOD register is "1" (melody is selected as the secondary function) and are VOL2 and VOH2 when each bit is "0".

13.3 Description of Operation

13.3.1   Output Port Function

For each pin of Port 2, any one of high-impedance output mode, P-channel open drain output mode, N-channel open drain output mode, and CMOS output mode can be selected by setting the Port 2 control registers 0 and 1 (P2CON0 and P2CON1). At a system reset, high-impedance output mode is selected as the initial state.
Depending of the value set in the Port 2 data register (P2D), a "L" level or "H" level signal is output to each pin of Port 2.

13.3.2   Secondary Function

Low-speed clock (LSCLK) output, High-speed clock (OUTCLK) output, and melody 0 (MD0) output are assigned to Port 2 as a secondary function. The secondary function can be used by setting the P22MD to P20MD bits of the Port 2 mode register (P2MOD) to "1".

Port 3

14. Port 3

14.1 Overview

This LSI includes Port 3 (P30 to P35), which is a 6-bit input/output port.
Furthermore, the oscillation pins (IN0, CS0, RS0, RT0, RCT0, and RCM) for the RC-ADC (Channel 0) are provided as the secondary function mode.
For the RC-ADC, see Chapter 19, "RC Oscillation Type A/D Converter".

14.1.1 Features

- Allows selection of high-impedance output, P-channel open drain output, N-channel open drain output, or CMOS output for each bit in output mode.
- Allows selection of high-impedance input, input with a pull-down resistor, or input with a pull-up resistor for each bit in input mode.
- The oscillation pins (IN0, CS0, RS0, RT0, RCT0, and RCM) for the RC-ADC (Channel 0) are available as the secondary function mode.

14.1.2 Configuration

Figure 14-1 shows the configuration of Port 3.


```
P3D     : Port 3 data register
P3DIR   : Port 3 direction register
P3CON0  : Port 3 control register 0
P3CON1  : Port 3 control register 1
P3MOD0  : Port 3 mode register 0
```

Figure 14-1　Configuration of Port 3

14.1.3 List of Pins

Pin name	I/O	Primary function	Secondary function
P30/IN0	I/O	Input/output port	Oscillation waveform input pin for RC-ADC0
P31/CS0	I/O	Input/output port	Reference capacitor connection pin for RC-ADC0
P32/RS0	I/O	Input/output port	Reference resistor connection pin for RC-ADC0
P33/RT0	I/O	Input/output port	Resistor sensor connection pin for measurement for RC-ADC0
P34/RCT0	I/O	Input/output port	Resistor/capacitor sensor connection pin for measurement for RC-ADC0
P35/RCM	I/O	Input/output port	RC oscillation monitor pin for RC-ADC

14.2 Description of Registers

14.2.1　List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F218H	Port 3 data register	P3D	—	R/W	8	00H
0F219H	Port 3 direction register	P3DIR	—	R/W	8	00H
0F21AH	Port 3 control register 0	P3CON0	P3CON	R/W	8/16	00H
0F21BH	Port 3 control register 1	P3CON1		R/W	8	00H
0F21CH	Port 3 mode register 0	P3MOD0	—	R/W	8	00H

14.2.2 Port 3 Data Register (P3D)

Address: 0F218H
Access: R/W
Access size: 8-bit
Initial value: 00H

	7	6	5	4	3	2	1	0
P3D	—	—	P35D	P34D	P33D	P32D	P31D	P30D
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P3D is a special function register (SFR) to set the value to be output to the Port 3 pin or to read the input level of the Port 3. In output mode, the value of this register is output to the Port 3 pin. The value written to P3D is readable.
In input mode, the input level of the Port 3 pin is read when P3D is read. Output mode or input mode is selected by using the port direction register (P3DIR) described later.

[Description of Bits]
- **P35D to P30D** (bits 5 to 0)
  The P35D to P30D bits are used to set the output value of the Port 3 pin in output mode and to read the pin level of the Port 3 pin in input mode.

P35D	Description
0	Output or input level of the P35 pin: ”L”
1	Output or input level of the P35 pin: ”H”

P34D	Description
0	Output or input level of the P34 pin: ”L”
1	Output or input level of the P34 pin: ”H”

P33D	Description
0	Output or input level of the P33 pin: ”L”
1	Output or input level of the P33 pin: ”H”

P32D	Description
0	Output or input level of the P32 pin: ”L”
1	Output or input level of the P32 pin: ”H”

P31D	Description
0	Output or input level of the P31 pin: ”L”
1	Output or input level of the P31 pin: ”H”

P30D	Description
0	Output or input level of the P30 pin: ”L”
1	Output or input level of the P30 pin: ”H”

14.2.3 Port 3 Direction Register (P3DIR)

Address: 0F219H
Access: R/W
Access size: 8-bit
Initial value: 00H

	7	6	5	4	3	2	1	0
P3DIR	—	—	P35DIR	P34DIR	P33DIR	P32DIR	P31DIR	P30DIR
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P3DIR is a special function register (SFR) to select the input/output mode of Port 3.

[Description of Bits]
- **P35DIR to P30DIR** (bits 5 to 0)
  P35DIR to P30DIR are the bits for setting the input/output direction of the Port 3 pins.

P35DIR	Description
0	P35 pin: Output (initial value)
1	P35 pin: Input

P34DIR	Description
0	P34 pin: Output (initial value)
1	P34 pin: Input

P33DIR	Description
0	P33 pin: Output (initial value)
1	P33 pin: Input

P32DIR	Description
0	P32 pin: Output (initial value)
1	P32 pin: Input

P31DIR	Description
0	P31 pin: Output (initial value)
1	P31 pin: Input

P30DIR	Description
0	P30 pin: Output (initial value)
1	P30 pin: Input

14.2.4 Port 3 Control Registers 0, 1 (P3CON0, P3CON1)

Address: 0F21AH
Access: R/W
Access size: 8/16 bit
Initial value: 00H

	7	6	5	4	3	2	1	0
P3CON0	—	—	P35C0	P34C0	P33C0	P32C0	P31C0	P30C0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F21BH
Access: R/W
Access size: 8-bit
Initial value: 00H

	7	6	5	4	3	2	1	0
P3CON1	—	—	P35C1	P34C1	P33C1	P32C1	P31C1	P30C1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P3CON0 and P3CON1 are special function registers (SFRs) to select input/output state of the Port 3 pin. The input/output state is different between input mode and output mode. Input or output is selected by using the P3DIR register.

[Description of Bits]
- **P35C1 to P30C1, P35C0 to P30C0** (bits 5 to 0)
  P35C1 to P30C1 and P35C0 to P30C0 are the bit bits for selecting the high-impedance output, P-channel open drain output, N-channel open drain output, or CMOS output in output mode and for selecting the high-impedance input, input with a pull-down resistor, or input with a pull-up resistor in input mode.

Setting of P35 pin		When output mode is selected (P35DIR bit = "0")	When input mode is selected (P35DIR bit = "1")
P35C1	**P35C0**	Description	
0	0	P35 pin: High-impedance output (initial value)	P35 pin: High-impedance input
0	1	P35 pin: P-channel open drain output	P35 pin: Input with a pull-down resistor
1	0	P35 pin: N-channel open drain output	P35 pin: Input with a pull-up resistor
1	1	P35 pin: CMOS output	P35 pin: High-impedance input

Setting of P34 pin		When output mode is selected (P34DIR bit = "0")	When input mode is selected (P34DIR bit = "1")
P34C1	**P34C0**	Description	
0	0	P34 pin: High-impedance output (initial value)	P34 pin: High-impedance input
0	1	P34 pin: P-channel open drain output	P34 pin: Input with a pull-down resistor
1	0	P34 pin: N-channel open drain output	P34 pin: Input with a pull-up resistor
1	1	P34 pin: CMOS output	P34 pin: High-impedance input

Setting of P33 pin		When output mode is selected (P33DIR bit = "0")	When input mode is selected (P33DIR bit = "1")
P33C1	**P33C0**	Description	
0	0	P33 pin: High-impedance output (initial value)	P33 pin: High-impedance input
0	1	P33 pin: P-channel open drain output	P33 pin: Input with a pull-down resistor
1	0	P33 pin: N-channel open drain output	P33 pin: Input with a pull-up resistor
1	1	P33 pin: CMOS output	P33 pin: High-impedance input

Setting of P32 pin		When output mode is selected (P32DIR bit = "0")	When input mode is selected (P32DIR bit = "1")
P32C1	**P32C0**	Description	
0	0	P32 pin: High-impedance output (initial value)	P32 pin: High-impedance input
0	1	P32 pin: P-channel open drain output	P32 pin: Input with a pull-down resistor
1	0	P32 pin: N-channel open drain output	P32 pin: Input with a pull-up resistor
1	1	P32 pin: CMOS output	P32 pin: High-impedance input

Setting of P31 pin		When output mode is selected (P31DIR bit = "0")	When input mode is selected (P31DIR bit = "1")
P31C1	**P31C0**	Description	
0	0	P31 pin: High-impedance output (initial value)	P31 pin: High-impedance input
0	1	P31 pin: P-channel open drain output	P31 pin: Input with a pull-down resistor
1	0	P31 pin: N-channel open drain output	P31 pin: Input with a pull-up resistor
1	1	P31 pin: CMOS output	P31 pin: High-impedance input

Setting of P30 pin		When output mode is selected (P30DIR bit = "0")	When input mode is selected (P30DIR bit = "1")
P30C1	**P30C0**	Description	
0	0	P30 pin: High-impedance output (initial value)	P30 pin: High-impedance input
0	1	P30 pin: P-channel open drain output	P30 pin: Input with a pull-down resistor
1	0	P30 pin: N-channel open drain output	P30 pin: Input with a pull-up resistor
1	1	P30 pin: CMOS output	P30 pin: High-impedance input

14.2.5 Port 3 Mode Register 0 (P3MOD0)

Address: 0F21CH
Access: R/W
Access size: 8/16 bit
Initial value: 00H

	7	6	5	4	3	2	1	0
P3MOD0	—	—	P35MD0	P34MD0	P33MD0	P32MD0	P31MD0	P30MD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P3MOD0 is a special function register (SFR) to select the primary function or the secondary function of Port 3.

[Description of Bits]

- **P35MD0** (bit 5)
  The P35MD0 bit is used to select the primary or secondary function of the P35 pin.

P35MD0	Description
0	General-purpose input/output mode (initial value)
1	RC oscillation monitor pin for RC-ADC

- **P34MD0** (bit 4)
  The P34MD0 bit is used to select the primary function or the secondary function of the P34 pin.

P34MD0	Description
0	General-purpose input/output mode (initial value)
1	Resistor/capacitor sensor connection pin for measurement for RC-ADC (channel 0)

- **P33MD0** (bit 3)
  The P33MD0 bit is used to select the primary or secondary function of the P33 pin.

P33MD0	Description
0	General-purpose input/output mode (initial value)
1	Resistor/capacitor sensor connection pin for measurement for RC-ADC (channel 0)

- **P32MD0** (bit 2)
  The P32MD0 bit is used to select the primary or secondary function of the P32 pin.

P32MD0	Description
0	General-purpose input/output mode (initial value)
1	Reference resistor connection pin for RC-ADC (channel 0)

- **P31MD0** (bit 1)
  The P31MD0 bit is used to select the primary or secondary function of the P31 pin.

P31MD0	Description
0	General-purpose input/output mode (initial value)
1	Reference capacitor connection pin for RC-ADC (channel 0)

- **P30MD0** (bit 0)

   The P30MD0 bit is used to select the primary or secondary function of the P30 pin.

P30MD0	Description
0	General-purpose input/output mode (initial value)
1	RC oscillation waveform input pin for RC-ADC (channel 0)

Note:

   When using the RC-ADC as the secondary function, set the P3DIR, P3CON0, and P3CON1 registers to bring each
   pin state to high-impedance input (same for when using the RC oscillation monitor function).
   Pull-up or Pull-down input makes drawing the current.

14.3 Description of Operation

14.3.1 Input/Output Port Functions

For each pin of Port 3, either output or input is selected by setting the Port 3 direction register (P3DIR).
In output mode, high-impedance output mode, P-channel open drain output mode, N-channel open drain output mode, or CMOS output mode can be selected by setting the Port 3 control registers 0 and 1 (P3CON0 and P3CON1).
In input mode, high-impedance input mode, input mode with a pull-down resistor, or input mode with a pull-up resistor can be selected by setting the Port 3 control registers 0 and 1 (P3CON0 and P3CON1).
At a system reset, high-impedance output mode is selected as the initial state.
In output mode, "L" or "H" level is output to each pin of Port 3 depending on the value set by the Port 3 data register (P3D).
In input mode, the input level of each pin of Port 3 can be read from the Port 3 data register (P3D).

14.3.2 Secondary Function

The secondary function is assigned to Port 3 as the RC-ADC (channel 0) oscillation pins (IN0, CS0, RS0, RT0, CRT0, RCM). Each of them can be used as the secondary function by setting the P35MD0 to P30MD0 bits of the port 3 mode register (P3MOD0).

Note:
·All the Port 3 pins except P35/RCM are configured as pins dedicated to the RC-ADC function during A/D conversion. Therefore, if there is any unused pin, that pin cannot be used as its primary function during A/D conversion. For the RC-ADC, see Chapter 19, "RC Oscillation Type A/D Converter".

Port 4

15. Port 4

15.1 Overview

This LSI includes Port 4 (P40 to P47) which is an 8-bit input/output port.
The port 4 can be used as an oscillation pin (IN1, CS1, RS1 and RT1) for the UART and RC-ADC (channel 1) as a secondary function.
For the UART, see Chapter 11, "UART." For the RC-ADC, see Chapter 19, "RC Oscillation Type A/D Converter."

15.1.1 Features

- Allows selection of high-impedance output, P-channel open drain output, N-channel open drain output, or CMOS output for each bit in output mode.
- Allows selection of high-impedance input, input with a pull-down resistor, or input with a pull-up resistor for each bit in input mode.
- The P44 pin can be used as the external clock input pin for the Timer 2. The P45 pin can be used as the external clock input pin for the Timer 3.
- The UART pins (RXD0, TXD0) and RC-ADC (channel 1) oscillation pins (IN1, CS1, RS1, RT1) can be used as the secondary functions.

15.1.2 Configuration

Figure 15-1 shows the configuration of Port 4.


```
P4D      : Port 4 data register
P4DIR    : Port 4 direction register
P4CON0   : Port 4 control register 0
P4CON1   : Port 4 control register 1
P4MOD0   : Port 4 mode register 0
P4MOD1   : Port 4 mode register 1
```

Figure 15-1   Configuration of Port 4

15.1.3 List of Pins

Pin name	I/O	Primary function	Secondary function
P40	I/O	Input/output port	—
P41	I/O	Input/output port	—
P42/RXD0	I/O	Input/output port	UART0 data input pin
P43/TXD0	I/O	Input/output port	UART0 data output pin
P44/ T2CK /IN1	I/O	Input/output port, Timer2 external clock input	RC oscillation waveform input pin for RC-ADC1
P45/ T3CK /CS1	I/O	Input/output port, Timer3 external clock input	Reference capacitor connection pin for RC-ADC1
P46/RS1	I/O	Input/output port	Reference resistor connection pin for RC-ADC1
P47/RT1	I/O	Input/output port	Resistor sensor connection pin for measurement for RC-ADC1

15.2 Description of Registers

15.2.1　List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F220H	Port 4 data register	P4D	—	R/W	8	00H
0F221H	Port 4 direction register	P4DIR	—	R/W	8	00H
0F222H	Port 4 control register 0	P4CON0	P4CON	R/W	8/16	00H
0F223H	Port 4 control register 1	P4CON1		R/W	8	00H
0F224H	Port 4 mode register 0	P4MOD0	—	R/W	8/16	00H
0F225H	Port 4 mode register 1	P4MOD1	—	R/W	8	00H

15.2.2 Port 4 Data Register (P4D)

Address: 0F220H
Access: R/W
Access size: 8-bit
Initial value: 00H

	7	6	5	4	3	2	1	0
P4D	P47D	P46D	P45D	P44D	P43D	P42D	P41D	P40D
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P4D is a special function register (SFR) to set the value to be output to the Port 4 pin or to read the input level of the Port 4. In output mode, the value of this register is output to the Port 4 pin. The value written to P4D is readable.
In input mode, the input level of the Port 4 pin is read when P4D is read. Output mode or input mode is selected by using the port direction register (P4DIR) described later.

[Description of Bits]
- **P47D to P40D** (bits 7 to 0)
  The P47D to P40D bits are used to set the output value of the Port 4 pin in output mode and to read the pin level of the Port 4 pin in input mode.

P47D	Description
0	Output or input level of the P47 pin: "L"
1	Output or input level of the P47 pin: "H"

P46D	Description
0	Output or input level of the P46 pin: "L"
1	Output or input level of the P46 pin: "H"

P45D	Description
0	Output or input level of the P45 pin: "L"
1	Output or input level of the P45 pin: "H"

P44D	Description
0	Output or input level of the P44 pin: "L"
1	Output or input level of the P44 pin: "H"

P43D	Description
0	Output or input level of the P43 pin: "L"
1	Output or input level of the P43 pin: "H"

P42D	Description
0	Output or input level of the P42 pin: "L"
1	Output or input level of the P42 pin: "H"

P41D	Description
0	Output or input level of the P41 pin: "L"
1	Output or input level of the P41 pin: "H"

P40D	Description
0	Output or input level of the P40 pin: "L"
1	Output or input level of the P40 pin: "H"

15.2.3   Port 4 Direction Register (P4DIR)

Address: 0F221H
Access: R/W
Access size: 8-bit
Initial value: 00H

	7	6	5	4	3	2	1	0
P4DIR	P47DIR	P46DIR	P45DIR	P44DIR	P43DIR	P42DIR	P41DIR	P40DIR
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P4DIR is a special function register (SFR) to select the input/output mode of Port 4.

[Description of Bits]
- **P47DIR to P40DIR** (bits 7 to 0)
  P47DIR to P40DIR are the bits for selecting the input/output mode of the Port 4 pins.

P47DIR	Description
0	P47 pin: Output (initial value)
1	P47 pin: Input

P46DIR	Description
0	P46 pin: Output (initial value)
1	P46 pin: Input

P45DIR	Description
0	P45 pin: Output (initial value)
1	P45 pin: Input

P44DIR	Description
0	P44 pin: Output (initial value)
1	P44 pin: Input

P43DIR	Description
0	P43 pin: Output (initial value)
1	P43 pin: Input

P42DIR	Description
0	P42 pin: Output (initial value)
1	P42 pin: Input

P41DIR	Description
0	P41 pin: Output (initial value)
1	P41 pin: Input

P40DIR	Description
0	P40 pin: Output (initial value)
1	P40 pin: Input

15.2.4 Port 4 Control Registers 0, 1 (P4CON0, P4CON1)

Address: 0F222H
Access: R/W
Access size: 8/16 bit
Initial value: 00H

	7	6	5	4	3	2	1	0
P4CON0	P47C0	P46C0	P45C0	P44C0	P43C0	P42C0	P41C0	P40C0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F223H
Access: R/W
Access size: 8-bit
Initial value: 00H

	7	6	5	4	3	2	1	0
P4CON1	P47C1	P46C1	P45C1	P44C1	P43C1	P42C1	P41C1	P40C1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P4CON0 and P4CON1 are special function registers (SFRs) to select input/output state of the Port 4 pin. The input/output state is different between input mode and output mode. Input or output is selected by using the P4DIR register.

[Description of Bits]
- **P47C1 to P40C1, P47C0 to P40C0** (bits 7 to 0)
  P47C1 to P40C1 and P47C0 to P40C0 are the bits for selecting the high-impedance output, P-channel open drain output, N-channel open drain output, or CMOS output in output mode and for selecting the high-impedance input, input with a pull-down resistor, or input with a pull-up resistor in input mode.

Setting of P47 pin		When output mode is selected (P47DIR bit = "0")	When input mode is selected (P47DIR bit = "1")
P47C1	**P47C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P46 pin		When output mode is selected (P46DIR bit = "0")	When input mode is selected (P46DIR bit = "1")
P46C1	**P46C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P45 pin		When output mode is selected (P45DIR bit = "0")	When input mode is selected (P45DIR bit = "1")
P45C1	**P45C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P44 pin		When output mode is selected (P44DIR bit = "0")	When input mode is selected (P44DIR bit = "1")
P44C1	**P44C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P43 pin		When output mode is selected (P43DIR bit = "0")	When input mode is selected (P43DIR bit = "1")
P43C1	**P43C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P42 pin		When output mode is selected (P42DIR bit = "0")	When input mode is selected (P42DIR bit = "1")
P42C1	**P42C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P41 pin		When output mode is selected (P41DIR bit = "0")	When input mode is selected (P41DIR bit = "1")
P41C1	**P41C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P40 pin		When output mode is selected (P40DIR bit = "0")	When input mode is selected (P40DIR bit = "1")
P40C1	**P40C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

15.2.5 Port 4 Mode Registers 0, 1 (P4MOD0, P4MOD1)

Address: 0F224H
Access: R/W
Access size: 8/16 bit
Initial value: 00H

	7	6	5	4	3	2	1	0
P4MOD0	P47MD0	P46MD0	P45MD0	P44MD0	P43MD0	P42MD0	—	—
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F225H
Access: R/W
Access size: 8-bit
Initial value: 00H

	7	6	5	4	3	2	1	0
P4MOD1	P47MD1	P46MD1	P45MD1	P44MD1	P43MD1	P42MD1	—	—
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P4MOD0 and P4MOD1 are special function registers (SFRs) to select the primary or secondary function of Port 4.

[Description of Bits]
- **P47MD1, P47MD0** (bit 7)
  The P47MD1 and P47MD0 bits are used to select the primary or secondary function of the P47 pin.

P47MD1	P47MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	Resistor sensor connection pin for measurement for RC-ADC (channel 1)
1	0	Prohibited
1	1	Prohibited

- **P46MD1, P46MD0** (bit 6)
  The P46MD1 and P46MD0 bits are used to select the primary or secondary function of the P46 pin.

P46MD1	P46MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	Reference resistor connection pin for RC-ADC (channel 1)
1	0	Prohibited
1	1	Prohibited

- **P45MD1, P45MD0** (bit 5)
  The P45MD1 and P45MD0 bits are used to select the primary or secondary function of the P45 pin.

P45MD1	P45MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	Reference capacitor connection pin for RC-ADC (channel 1)
1	0	Prohibited
1	1	Prohibited

- **P44MD1, P44MD0** (bit 4)
  The P44MD1 and P44MD0 bits are used to select the primary or secondary function of the P44 pin.

P44MD1	P44MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	RC oscillation waveform input pin for RC-AD (channel 1)
1	0	Prohibited
1	1	Prohibited

- **P43MD1, P43MD0** (bit 3)
  The P43MD1 and P43MD0 bits are used to select the primary, secondary, or tertiary function of the P43 pin.

P43MD1	P43MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	UART0 data output pin
1	0	Prohibited
1	1	Prohibited

- **P42MD1, P42MD0** (bit 2)
  The P42MD1 and P42MD0 bits are used to select the primary, secondary, or tertiary function of the P42 pin.

P42MD1	P42MD0	Description
0	0	General-purpose input/output mode (initial value)
0	1	UART0 data input pin
1	0	Prohibited
1	1	Prohibited

Note:
  When the pin is set to "Prohibited" and the output mode is selected (by the Port 4 control register), the Port 4 output pin state is fixed as follows regardless of the data of the port data register P4D:

  When high-impedance output is selected: Output pin is high-impedance
  When P-channel open drain output is selected: Output pin is high-impedance
  When N-channel open drain output is selected: Output pin is fixed to "L"
  When CMOS output is selected: Output pin is fixed to "L"

  When using the RC-ADC as the secondary function, set the P4DIR, P4CON0, and P4CON1 registers to bring each pin state to high-impedance input. Pull-up or Pull-down input makes drawing the current.

15.3 Description of Operation

15.3.1   Input/Output Port Functions

For each pin of Port 4, either output or input is selected by setting the Port 4 direction register (P4DIR).
In output mode, high-impedance output mode, P-channel open drain output mode, N-channel open drain output mode, or CMOS output mode can be selected by setting the Port 4 control registers 0 and 1 (P4CON0 and P4CON1).
In input mode, high-impedance input mode, input mode with a pull-down resistor, or input mode with a pull-up resistor can be selected by setting the Port 4 control registers 0 and 1 (P4CON0 and P4CON1).
At a system reset, high-impedance output mode is selected as the initial state.
In output mode, "L" or "H" level is output to each pin of Port 4 depending on the value set by the Port 4 data register (P4D).
In input mode, the input level of each pin of Port 4 can be read from the Port 4 data register (P4D).

15.3.2   Secondary Functions

The secondary functions are assigned to Port 4 as the UART0 pins (RXD0, TXD0) and RC-ADC (channel 1) oscillation pins (IN1, CS1, RS1, RT1). These pins can be used in a secondary function mode by setting the P47MD0 to P42MD0 bits and the P47MD1 to P42MD1 bits of the Port 4 mode registers (P4MOD0, P4MOD1).

Note:
The P44 to P47 pins of Port 4 are configured as pins dedicated to the RC-ADC function during A/D conversion.
Therefore, if any of them is unused, it cannot be used as the primary function (or as the port). For the RC-ADC, see Chapter 19, "RC Oscillation Type A/D Converter".

Port 5

16. Port 5

16.1 Overview

This LSI includes Port 5 (P50 to P57) which is an 8-bit input/output port.

16.1.1 Features

- Allows selection of N-channel open drain output or CMOS output for each bit in the output mode.
- Allows selection of high-impedance input or input with a pull-down/pull-up resistor for each bit in the input mode.
- Allows selection of interrupt disabled or interrupt enabled for each bit in the input mode.
- The Melody 0 (MD0) is available as the secondary and tertiary function.

16.1.2 Configuration

Figure 16-1 shows the configuration of Port 5.
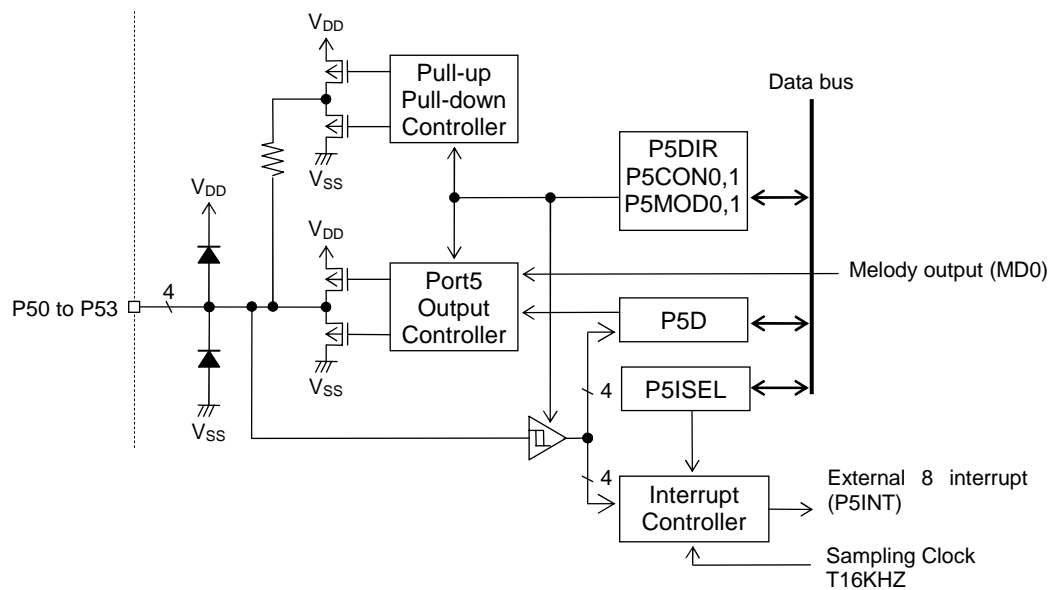
P5D   : Port 5 data register
P5DIR   : Port 5 direction register
P5CON0   : Port 5 control register 0
P5CON1   : Port 5 control register 1
P5MOD0   : Port 5 mode register 0
P5MOD1   : Port 5 mode register 1
P5ISEL   : Port 5 interrupt mode register

Figure 16-1   Configuration of Port 5

16.1.3 List of Pins

Pin name	Input/output	Primary function	Secondary Function
P50/EXI8/MD0	I/O	Input/output port, External 8 interrupt	Melody 0 output
P51/EXI8	I/O	Input/output port, External 8 interrupt	—
P52/EXI8	I/O	Input/output port, External 8 interrupt	—
P53/EXI8	I/O	Input/output port, External 8 interrupt	—

16.2 Description of Registers

16.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F228H	Port 5 data register	P5D	—	R/W	8	0FH
0F229H	Port 5 direction register	P5DIR	—	R/W	8	00H
0F22AH	Port 5 control register 0	P5CON0	P5CON	R/W	8/16	00H
0F22BH	Port 5 control register 1	P5CON1		R/W	8	00H
0F22CH	Port 5 mode register 0	P5MOD0	P5MOD	R/W	8/16	00H
0F22DH	Port 5 mode register 1	P5MOD1		R/W	8	00H
0F22EH	Port 5 interrupt mode register	P5ISEL	—	R/W	8	00H

16.2.2 Port 5 Data Register (P5D)

Address: 0F228H
Access: R/W
Access size: 8-bit
Initial value: 0FH

	7	6	5	4	3	2	1	0
P5D	—	—	—	—	P53D	P52D	P51D	P50D
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	1	1	1	1

P5D is a special function register (SFR) to set the value to be output to the Port 5 pin or to read the input level of the Port 5. In output mode, the value of this register is output to the Port 5 pin. The value written to P5D is readable.
In input mode, the input level of the Port 5 pin is read when P5D is read. Output mode or input mode is selected by using the port direction register (P5DIR) described later.

[Description of Bits]
- **P53D to P50D** (bit 3 to 0)
  The P53D to P50D bits are used to set the output value of the Port 5 pin in output mode and to read the pin level of the Port 5 pin in input mode.

P53D	Description
0	Output or input level of the P53 pin: "L"
1	Output or input level of the P53 pin: "H"

P52D	Description
0	Output or input level of the P52 pin: "L"
1	Output or input level of the P52 pin: "H"

P51D	Description
0	Output or input level of the P51 pin: "L"
1	Output or input level of the P51 pin: "H"

P50D	Description
0	Output or input level of the P50 pin: "L"
1	Output or input level of the P50 pin: "H"

16.2.3   Port 5 Direction Register (P5DIR)

Address: 0F229H
Access: R/W
Access size: 8-bit
Initial value: 00H

	7	6	5	4	3	2	1	0
P5DIR	—	—	—	—	P53DIR	P52DIR	P51DIR	P50DIR
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P5DIR is a special function register (SFR) to select the input/output mode of Port 5.

[Description of Bits]
- **P53DIR to P50DIR** (bit 3 to 0)
  The P53DIR to P50DIR pins are used to set the input/output direction of the Port 5 pin.

P53DIR	Description
0	P53 pin: Output (initial value)
1	P53 pin: Input

P52DIR	Description
0	P52 pin: Output (initial value)
1	P52 pin: Input

P51DIR	Description
0	P51 pin: Output (initial value)
1	P51 pin: Input

P50DIR	Description
0	P50 pin: Output (initial value)
1	P50 pin: Input

16.2.4 Port 5 Control Registers 0 and 1 (P5CON0 and P5CON1)

Address: 0F22AH
Access: R/W
Access size: 8/16 bit
Initial value: 00H

	7	6	5	4	3	2	1	0
P5CON0	—	—	—	—	P53C0	P52C0	P51C0	P50C0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F22BH
Access: R/W
Access size: 8-bit
Initial value: 00H

	7	6	5	4	3	2	1	0
P5CON1	—	—	—	—	—	—	—	P5UD
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P5CON0 and P5CON1 are special function registers (SFRs) to select input/output state of the Port 5 pin. The input/output state is different between input mode and output mode. Input or output is selected by using the P5DIR register.

[Description of Bits]
- **P53C0 to P50C0** (bit 3 to 0)
  P53C0 to P50C0 are the bits that select N-channel open drain output or CMOS output in the output mode, and high-impedance input or input with a pull-down or pull-up resistor in the input mode.

Setting of P53 pin	When output mode is selected (P53DIR bit = "0")	When input mode is selected (P53DIR bit = "1")
P53C0	Description	
0	N-channel open drain output (initial value)	Input with a pull-down or pull-up resistor
1	CMOS output	High-impedance input

Setting of P52 pin	When output mode is selected (P52DIR bit = "0")	When input mode is selected (P52DIR bit = "1")
P52C0	Description	
0	N-channel open drain output (initial value)	Input with a pull-down or pull-up resistor
1	CMOS output	High-impedance input

Setting of P51 pin	When output mode is selected (P51DIR bit = "0")	When input mode is selected (P51DIR bit = "1")
P51C0	Description	
0	N-channel open drain output (initial value)	Input with a pull-down or pull-up resistor
1	CMOS output	High-impedance input

Setting of P50 pin	When output mode is selected (P50DIR bit = "0")	When input mode is selected (P50DIR bit = "1")
P50C0	Description	
0	N-channel open drain output (initial value)	Input with a pull-down or pull-up resistor
1	CMOS output	High-impedance input

- **P5UD** (bit 0)

  P5UD is the bit that selects input with a pull-up resistor or input with a pull-down resistor when the input with a pull-down or pull-up resistor is selected.

Setting of each port 5 pin	When the input with a pull-down or pull-up resistor mode is selected (P5nDIR bit = "1", P5nC0 = "0") (n = 0,1,2,3)
P5UD	Description
0	Input with a pull-up resistor (initial value)
1	Input with a pull-down resistor

16.2.5 Port 5 Mode Register 0 (P5MOD0 and P5MOD1)

Address: 0F22CH
Access: R/W
Access size: 8/16-bit
Initial value: 00H

	7	6	5	4	3	2	1	0
P5MOD0	—	—	—	—	—	—	—	P50MD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F22DH
Access: R/W
Access size: 8-bit
Initial value: 00H

	7	6	5	4	3	2	1	0
P5MOD1	—	—	—	—	—	—	—	P50MD1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P5MOD0 and P5MOD1 are special function registers (SFRs) to select the primary function or the secondary function of Port 5.

[Description of Bits]
- **P50MD1, P50MD0** (bit 0)
  The P50MD1 and P50MD0 bit is used to select the primary or secondary function of the P50 pin.

P50MD1	**P50MD0**	Description
0	0	General-purpose input/output mode (initial value)
0	1	Melody 0 output
1	0	Prohibited
1	1	Prohibited

Note:
When the pin is set to "Prohibited" and the output mode is selected (by the Port 5 control register), the Port 5 output pin state is fixed as follows regardless of the data of the port data register P5D:

When N-channel open drain output is selected: Output pin is fixed to "L"
When CMOS output is selected: Output pin is fixed to "L"

Secondary function is not settable for the pins P51 to P53.

16.2.6 Port 5 Interrupt Mode Register (P5ISEL)

Address: 0F22EH
Access: R/W
Access size: 8-bit
Initial value: 00H

	7	6	5	4	3	2	1	0
P5ISEL	—	—	—	—	P53IS	P52IS	P51IS	P50IS
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P5ISEL is a special function register (SFR) to select the pin used for the external 8 interrupt (P5INT).

[Description of Bits]
- **P53IS to P50IS** (bit 3 to 0)
  P53IS to P50IS are the bits that select to disable or enable the interrupt of each pin on the Port 5.

P53IS	Description
0	P53 external interrupt disabled (initial value)
1	P53 external interrupt enabled

P52IS	Description
0	P52 external interrupt disabled (initial value)
1	P52 external interrupt enabled

P51IS	Description
0	P51 external interrupt disabled (initial value)
1	P51 external interrupt enabled

P50IS	Description
0	P50 external interrupt disabled (initial value)
1	P50 external interrupt enabled

16.3 Description of Operation

16.3.1 Input/Output Port Functions

For each pin of Port 5, either output or input is selected by setting the Port 5 direction register (P5DIR).
In the output mode, set the Port 5 control register 0 (P5CON0) to select either N-channel open drain output mode or CMOS output mode.
In the input mode, set the Port 5 control registers 0 and 1 (P5CON0 and P5CON1) to select any of high-impedance input mode, input mode with a pull-down resistor, or input mode with a pull-up resistor.
At the system reset, N-channel open drain output mode is selected as the initial state.
In output mode, the "L" or "H" level is output to each pin of Port 5 depending on the value set by the Port 5 data register (P5D).
In input mode, the input level of each pin of Port 5 is read from the Port 5 data register (P5D).

16.3.2 Secondary Functions

The Port 5 is assigned with the pins for Melody 0 (MD0) output as the secondary function. Each of them can be used as the secondary function by setting the P50MD1 and P50MD0 bits of the port mode register 1(P5MOD1) and 0 (P5MOD0).

16.3.3 External Interrupt

Each pin of the port 5 (P50 to P53) can be used as an external 8 interrupt (P5INT) and disabling/enabling the interrupt can be set individually. For details of interrupts, see Chapter 5, "Interrupts".

16.3.4 Interrupt Request

The maskable external 8 interrupt (P5INT) occurs when each of the Port 5 pins has an interrupt edge.
Figure 16-2 shows the external 8 interrupt (P5INT) generation timing in case P5UD bit of P5CON1 register is "1".
Figure 16-3 shows the external 8 interrupt (P5INT) generation timing in case P5UD bit of P5CON1 register is "0".

Note:
    - The external 8 interrupt (P5INT) is fixed to both-edge interrupt with sampling.
    In STOP mode, since the 16 kHz sampling clock stops, no sampling is performed.
    - Depending on the P5n pin state, the External 8 Interrupt Request flag (IRQ2's bit 3) may be set to "1" when the
    P5ISEL setting is changed. Therefore, change the P5ISEL setting when the Master Interrupt Enable (MIE) flag is "0",
    then reset the External 8 Interrupt Request flag to "0" by software before setting the MIE to "1". For interrupts, see
    Chapter 5, "Interrupts."
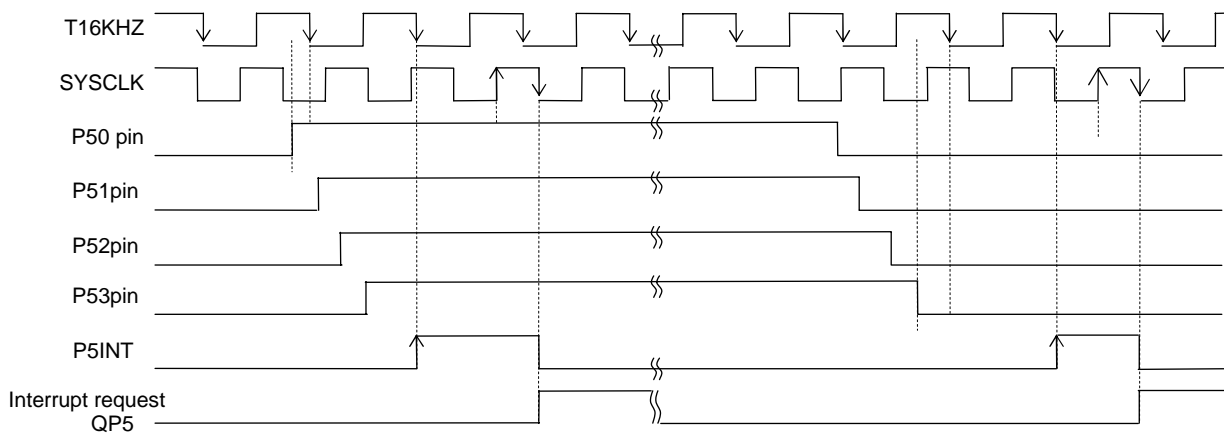
With sampling, both-edge interrupt

Figure 16-2   External 8 Interrupt Generation Timing (P5UD = 1)
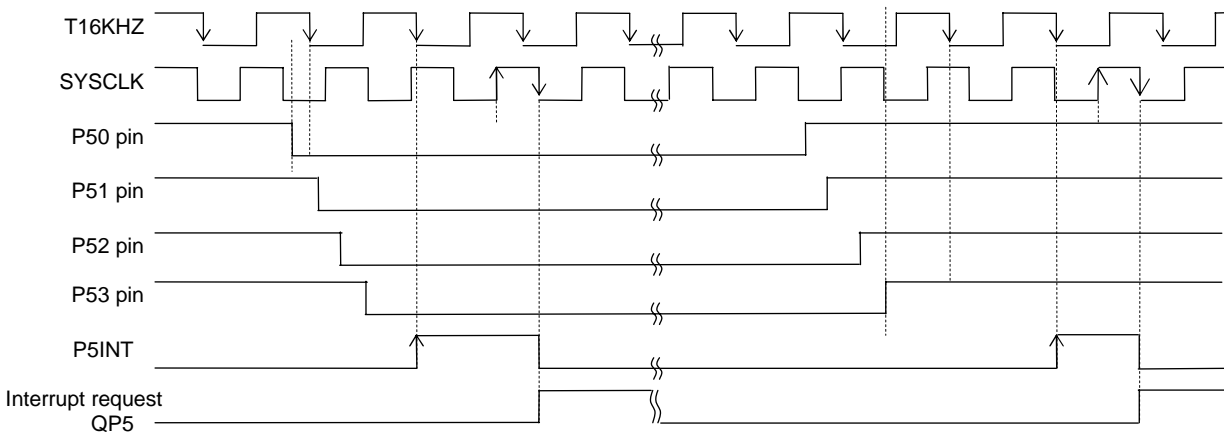
With sampling, both-edge interrupt

Figure 16-3   External 8 Interrupt Generation Timing (P5UD = 0)

Port 6

17. Port 6

17.1 Overview

ML610401	Includes Port 6 (P60 to P67) which is an 8-bit output port.
ML610402	Includes Port 6 (P60 to P63) which is a 4-bit output port.
ML610403	This function is not included.

17.1.1　Features

- Allows selection of N-channel open drain output or CMOS output for each bit.

17.1.2　Configuration

Figure 17-1 shows the configuration of Port 6.

P6D 　　: Port 6 data register
P6CON0 　: Port 6 control register 0
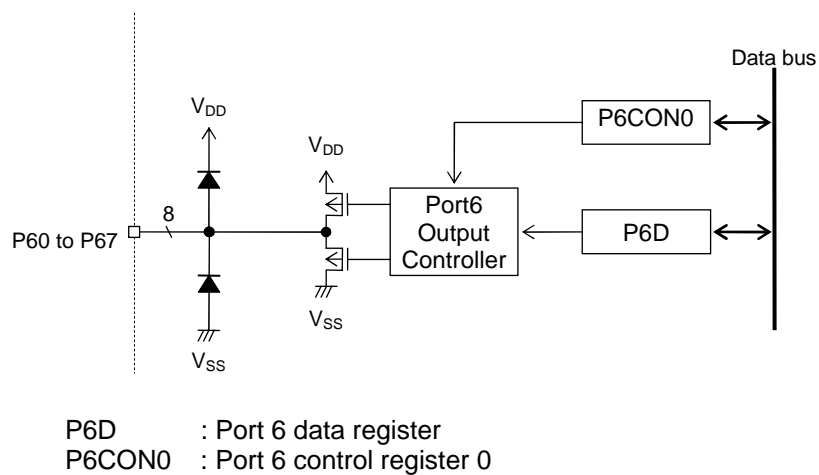
Figure 17-1　Configuration of Port 6

17.1.3　List of Pins

Pin name	Input/Output	Function
P60	O	Output port
P61	O	Output port
P62	O	Output port
P63	O	Output port
P64	O	Output port
P65	O	Output port
P66	O	Output port
P67	O	Output port

17.2 Description of Registers

17.2.1 List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F230H	Port 6 data register	P6D	—	R/W	8	0FFH
0F232H	Port 6 control register 0	P6CON0	—	R/W	8	00H

17.2.2 Port 6 Data Register (P6D)

Address: 0F230H
Access: R/W
Access size: 8-bit
Initial value: 0FFH

	7	6	5	4	3	2	1	0
P6D	P67D	P66D	P65D	P64D	P63D	P62D	P61D	P60D
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	1	1	1	1	1

P6D is a special function register (SFR) to set the output value of the Port 6 pins. The value of this register is output to Port 6. The value written to P6D is readable.
For ML610402, P67D to P64D always returns the value "0".
ML610403 does not have this register.

[Description of Bits]
- **P67D to P60D** (bit 7 to 0)
  The P67D to P60D bits are used to set the output value of the Port 6 pins.

P67D	Description
0	Output level of the P67 pin: "L"
1	Output level of the P67 pin: "H"

P66D	Description
0	Output level of the P66 pin: "L"
1	Output level of the P66 pin: "H"

P65D	Description
0	Output level of the P65 pin: "L"
1	Output level of the P65 pin: "H"

P64D	Description
0	Output level of the P64 pin: "L"
1	Output level of the P64 pin: "H"

P63D	Description
0	Output level of the P63 pin: "L"
1	Output level of the P63 pin: "H"

P62D	Description
0	Output level of the P62 pin: "L"
1	Output level of the P62 pin: "H"

P61D	Description
0	Output level of the P61 pin: "L"
1	Output level of the P61 pin: "H"

P60D	Description
0	Output level of the P60 pin: "L"
1	Output level of the P60 pin: "H"

17.2.3 Port 6 Control Register 0 (P6CON0)

Address: 0F232H
Access: R/W
Access size: 8-bit
Initial value: 00H

	7	6	5	4	3	2	1	0
P6CON0	P67C0	P66C0	P65C0	P64C0	P63C0	P62C0	P61C0	P60C0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P6CON0 is a special function registers (SFR) to select output state of the Port 6 pin.
For ML610402, P67C0 to P64C0 always returns the value "0".
ML610403 does not have this register.

[Description of Bits]
- **P67C0 to P60C0** (bit 7 to 0)
  P67C0 to P60C0 are the bits that select either N-channel open drain output or CMOS output.

P67C0	Description
0	N-channel open drain output (initial value)
1	CMOS output

P66C0	Description
0	N-channel open drain output (initial value)
1	CMOS output

P65C0	Description
0	N-channel open drain output (initial value)
1	CMOS output

P64C0	Description
0	N-channel open drain output (initial value)
1	CMOS output

P63C0	Description
0	N-channel open drain output (initial value)
1	CMOS output

P62C0	Description
0	N-channel open drain output (initial value)
1	CMOS output

P61C0	Description
0	N-channel open drain output (initial value)
1	CMOS output

P60C0	Description
0	N-channel open drain output (initial value)
1	CMOS output

17.3 Description of Operation

17.3.1 Output Port Function

For each of the Port 6 pins, N-channel open drain output mode or CMOS output mode can be selected by setting the Port 6 control register 0 (P6CON0).
At the system reset, N-channel open drain output mode is selected as the initial state.
Depending on the value set in the Port 6 data register (P6D), a "L" level or "H" level signal is output to each pin of Port 6.

Melody Driver

18. Melody Driver

18.1 Overview

This LSI includes one channel of the melody driver.
To use the melody driver, the secondary function of Port 2 or Port 5 should be set. For the secondary function of Port 2, see Chapter 13, "Port 2". For the secondary function of Port 5, see Chapter 16, "Port 5".For the clock to be used in this block, see Chapter 6, "Clock Generation Circuit".

18.1.1 Features

- In melody output mode, 29 scales (melody audio frequency: 508Hz to 32.768kHz), 63 tone lengths, and 15 tempos) are available.
- In buzzer output mode, 4 output modes, 8 frequencies, and 15 duties can be set.

18.1.2 Configuration

Figure 18-1 shows the configuration of the melody driver.
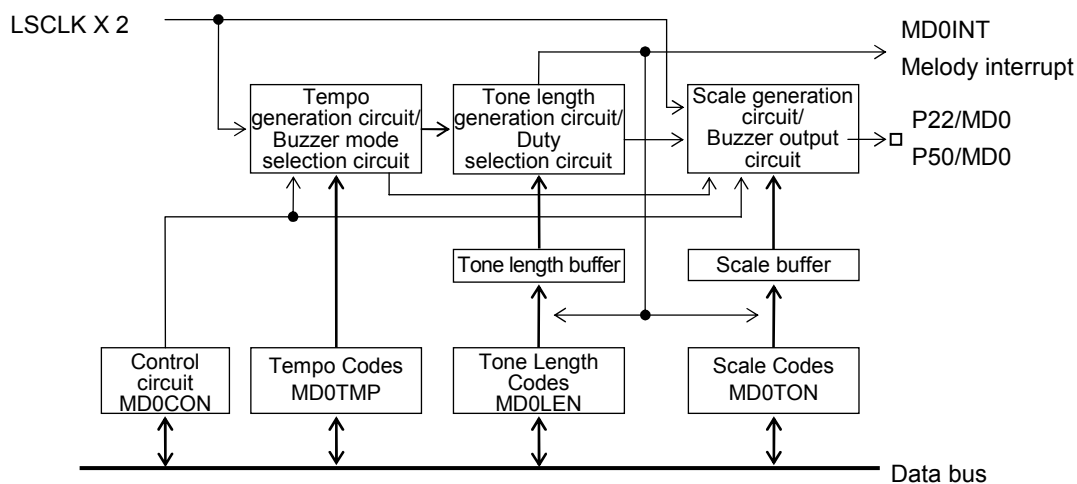
MD0CON   : Melody 0 control register
MD0TMP   : Melody 0 tempo code register
MD0TON   : Melody 0 scale code register
MD0LEN   : Melody 0 tone length code register

Figure 18-1   Configuration of Melody Driver

18.1.3 List of Pins

Pin name	I/O	Function
P22/MD0	O	Melody 0 signal output pin Used as the secondary function of the P22 pin.
P50/MD0	O	Melody 0 signal output pin Used for the secondary function of the P50 pin.

18.2 Description of Registers

18.2.1   List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F2C0H	Melody 0 control register	MD0CON	—	R/W	8	00H
0F2C1H	Melody 0 tempo code register	MD0TMP	—	R/W	8	00H
0F2C2H	Melody 0 scale code register	MD0TON	MD0TL	R/W	8/16	00H
0F2C3H	Melody 0 tone length code register	MD0LEN		R/W	8	00H

18.2.2 Melody 0 Control Register (MD0CON)

Address: 0F2C0H
Access: R/W
Access size: 8-bit
Initial value: 00H

	7	6	5	4	3	2	1	0
MD0CON	—	—	—	—	—	—	BZMD	M0RUN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

MD0CON is a special function register (SFR) to control the melody and the buzzer.

[Description of Bits]
- **BZMD** (bit 1)
  The BZMD bit is used to select melody mode or buzzer mode.

BZMD	Description
0	Melody mode (initial value)
1	Buzzer mode

- **M0RUN** (bit 0)
  The M0RUN bit is used to control start/stop of the MD0 output.

M0RUN	Description
0	Stops MD0 output. (Initial value)
1	Starts MD0 output.

Note:
   For melody output, use the low-speed double clock (LSCLK x 2).
   Enable the low-speed double clock by setting bit 2 (ENMLT) of frequency control register 1 (FCON1) to "1" and
   then start melody output by setting M0RUN to "1".

18.2.3 Melody 0 Tempo Code Register (MD0TMP)

Address: 0F2C1H
Access: R/W
Access size: 8-bit
Initial value: 00H

	7	6	5	4	3	2	1	0
MD0TMP	—	—	—	—	M0TM3	M0TM2	M0TM1	M0TM0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

MD0TMP is a special function register (SFR) to set the tempo code of a melody when melody mode is selected and the output mode of a buzzer sound waveform when buzzer mode is selected.

[Description of Bits]
- **M0TM3, M0TM2, M0TM1, M0TM0** (bits 3-0)

When melody mode is selected (BZMD bit = "0")				
M0TM3	**M0TM2**	**M0TM1**	**M0TM0**	Description
0	0	0	0	♪ = 480 (initial value)
0	0	0	1	♪ =480
0	0	1	0	♪ =320
0	0	1	1	♪ =240
0	1	0	0	♪ =192
0	1	0	1	♪ =160
0	1	1	0	♪ ≅137
0	1	1	1	♪ =120
1	0	0	0	♪ ≅107
1	0	0	1	♪ =96
1	0	1	0	♪ ≅87
1	0	1	1	♪ =80
1	1	0	0	♪ ≅74
1	1	0	1	♪ ≅69
1	1	1	0	♪ =64
1	1	1	1	♪ =60

When buzzer mode is selected (BZMD bit = "1")				
M0TM3	**M0TM2**	**M0TM1**	**M0TM0**	Description
*	*	0	0	Intermittent sound 1 output (initial value)
*	*	0	1	Intermittent sound 2 output
*	*	1	0	Single sound output
*	*	1	1	Continuous sound output

18.2.4   Melody 0 Scale Code Register (MD0TON)

Address: 0F2C2H
Access: R/W
Access size: 8-bit
Initial value: 00H

	7	6	5	4	3	2	1	0
MD0TON	—	M0TN6	M0TN5	M0TN4	M0TN3	M0TN2	M0TN1	M0TN0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

MD0TON is a special function register (SFR) to set the scale code of a melody when melody mode is selected and a buzzer output frequency when buzzer mode is selected.

[Description of Bits]
- **M0TN6, M0TN5, M0TN4, M0TN3, M0TN2, M0TN1, M0TN0** (bits 6-0)

When melody mode is selected (BZMD bit = "0")	
M0TN6~0	Description
	Sets the corresponding scale code.

For scale codes, see Section 18.3.4, "Scale Codes".

When buzzer mode is selected (BZMD bit = "1")				
M0TN6~3	M0TN2	M0TN1	M0TN0	Description
*	0	0	0	4.096 kHz (initial value)
*	0	0	1	2.048kHz
*	0	1	0	1.365kHz
*	0	1	1	1.024kHz
*	1	0	0	819Hz
*	1	0	1	683Hz
*	1	1	0	585Hz
*	1	1	1	512Hz

Note: In buzzer mode, the M0TN6 to M0TN3 bits are not used (Don't care).

18.2.5 Melody 0 Tone Length Code Register (MD0LEN)

Address: 0F2C3H
Access: R/W
Access size: 8-bit
Initial value: 00H

	7	6	5	4	3	2	1	0
MD0LEN	—	—	M0LN5	M0LN4	M0LN3	M0LN2	M0LN1	M0LN0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

MD0LEN is a special function register (SFR) to set the tone length code of a melody when melody mode is selected and buzzer output duty when buzzer mode is selected.

[Description of Bits]
- **M0LN5, M0LN4, M0LN3, M0LN2, M0LN1, M0LN0** (bits 5-0)

When melody mode is selected (BZMD bit = "0")	
M0LN5~0	Description
	Sets the corresponding tone length code.

For tone length codes, see Section 18.3.3, "Tone Length Codes".

When buzzer mode is selected (BZMD bit = "1")					
M0LN5~4	**M0LN3**	**M0LN2**	**M0LN1**	**M0LN0**	Description
*	0	0	0	0	1/16 DUTY (initial value)
*	0	0	0	1	1/16DUTY
*	0	0	1	0	2/16DUTY
*	0	0	1	1	3/16DUTY
*	0	1	0	0	4/16DUTY
*	0	1	0	1	5/16DUTY
*	0	1	1	0	6/16DUTY
*	0	1	1	1	7/16DUTY
*	1	0	0	0	8/16DUTY
*	1	0	0	1	9/16DUTY
*	1	0	1	0	10/16DUTY
*	1	0	1	1	11/16DUTY
*	1	1	0	0	12/16DUTY
*	1	1	0	1	13/16DUTY
*	1	1	1	0	14/16DUTY
*	1	1	1	1	15/16DUTY

Note: In buzzer mode, the M0LN5 to M0LN4 bits are not used (Don't care).

18.3 Description of Operation

18.3.1 Operation of Melody Output

Melody is output in the following procedure.
(1) Select melody mode by setting the BZMD bit of the melody 0 control register (MD0CON) to "0".
(2) Set a melody tempo in the melody 0 tempo code register (MD0TMP).
(3) Set a tone length code in the melody 0 tone length code register (MD0LEN).
(4) Set a scale code in the melody 0 scale code register (MD0TON).
(5) Set bit 2 (ENMLT) of the frequency control register 1(FCON1) to "1" to enable the low-speed double clock.
(6) When the M0RUN bit of the melody 0 control register (MD0CON) is set to "1", the tone length code and scale code are transferred to the tone length buffer and scale buffer and melody output is started from the MD0 pin. At the same time, a melody 0 interrupt (MD0INT) is requested. When an interrupt occurs and program is passed to the interrupt routine, the interrupt request flag is cleared.

The melody 0 signal output pin (MD0) is assigned as the secondary function of Port 2 or Port 5. For the secondary function of Port 2 or Port 5, see Chapter 13, "Port 2" or Chapter 16, "Port 5".

In the software processing after melody 0 interrupt, the tone length code and the scale code of the note that are output next are set to MD0LEN and MD0TON, respectively. When there is no next note to be output, rest data "00H" is set in MD0TON, the M0RUN bit is set to "0" by the software processing after the next melody 0 interrupt, and melody output is terminated.

By setting the M0RUN bit to "0", melody can be terminated forcibly during melody output.
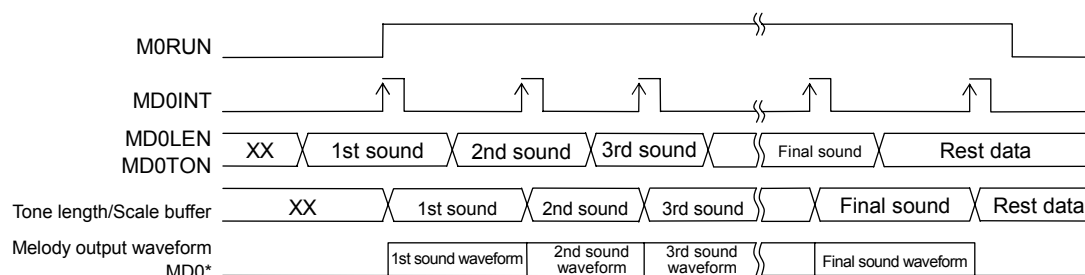
Figure 18-2 shows the operation waveform of the melody driver.

Figure 18-2   Operation Waveform of Melody Driver

18.3.2 Tempo Codes

A tempo code is set in the melody 0 tempo code register (MD0TEM).

Table 18-1 shows the correspondence between tempos (number of counts for one minute) and tempo codes.

The tempo when all the bits are set to "0" is equal to the shortest tone length (the tempo when the only M0TP0 bit is set to "1").

Table 18-1   Correspondence between Tempos and Tempo Codes

Tempo	Tempo code (MD0TMP)				
	M0TP3	M0TP2	M0TP1	M0TP0	M0TP3~0
♩ = 480	0	0	0	0	0H
♩ = 480	0	0	0	1	1H
♩ = 320	0	0	1	0	2H
♩ = 240	0	0	1	1	3H
♩ = 192	0	1	0	0	4H
♩ = 160	0	1	0	1	5H
♩ ≅ 137	0	1	1	0	6H
♩ = 120	0	1	1	1	7H
♩ ≅ 107	1	0	0	0	8H
♩ = 96	1	0	0	1	9H
♩ ≅ 87	1	0	1	0	AH
♩ = 80	1	0	1	1	BH
♩ ≅ 74	1	1	0	0	CH
♩ ≅ 69	1	1	0	1	DH
♩ = 64	1	1	1	0	EH
♩ = 60	1	1	1	1	FH

18.3.3 Tone Length Codes

A tone length code is set in the melody 0 tone length code register (MD0LEN).
Table 18-2 shows the correspondence between tone lengths and tone length codes.
The tone length when all the bits are set to "0" is equal to the shortest tone length (the tone length when the only M0LN0 bit is set to "1").

Table 18-2   Correspondence between Tone Lengths and Tone Length Codes

Tone length	Tone length code (MD0LEN)						
	M0LN5	M0LN4	M0LN3	M0LN2	M0LN1	M0LN1	M0LN5~0
♩	1	1	1	1	1	1	3FH
♩.	1	0	1	1	1	1	2FH
♩	0	1	1	1	1	1	1FH
♪.	0	1	0	1	1	1	17H
♪	0	0	1	1	1	1	0FH
♪.	0	0	1	0	1	1	0BH
♪	0	0	0	1	1	1	07H
♪.	0	0	0	1	0	1	05H
♪	0	0	0	0	1	1	03H
♪	0	0	0	0	1	0	02H
♪	0	0	0	0	0	1	01H

The tone length set by a tone length code and a tempo code is expressed by the following equation.

Tone length = 1.953125 x (TP + 1) x (LN + 1) ms where TP is an integer of 1 to 15, and LN is an integer of 1 to 63.

The bit correspondence between TP and tempo codes is expressed by the following equation.

$TP = 2^3 M0TP3 + 2^2 M0TP2 + 2^1 M0TP1 + 2^0 M0TP0$

The bit correspondence between LN and tone length codes is expressed by the following equation.

$LN = 2^5 M0LN5 + 2^4 M0LN4 + 2^3 M0LN3 + 2^2 M0LN2 + 2^1 M0LN1 + 2^0 M0LN0$

18.3.4 Scale Codes

A scale code is set in the melody 0 scale code register (MD0TON).
In the melody driver, a frequency that can be output is expressed by the following equation.

$$\frac{65536}{(\,TN + 1\,)}\ \ Hz \quad \text{(where TN is an integer of 4 to 127.)}$$

The bit correspondence between TN and scale codes is expressed by the following equation.

$$TN = 2^6 M0TN6 + 2^5 M0TN5 + 2^4 M0TN4 + 2^3 M0TN3 + 2^2 M0TN2 + 2^1 M0TN1 + 2^0 M0TN0$$

Table 18-3 shows the correspondence between scales and scale codes.
When the M0TN6 to M0TN2 bits are set to "0", scale becomes a rest. The rest length is set by the tone length code (MD0LEN).

Table 18-3　Correspondence between Scales and Scale Codes

Scale	Frequency (Hz)	Scale code (MD0TON)							
		M0TN6	M0TN5	M0TN4	M0TN3	M0TN2	M0TN1	M0TN0	M0TN6~0
C^1	529	1	1	1	1	0	1	1	7BH
Cis^1	560	1	1	1	0	1	0	0	74H
D^1	590	1	1	0	1	1	1	0	6EH
Dis^1	624	1	1	0	1	0	0	0	68H
E^1	662	1	1	0	0	0	1	0	62H
F^1	705	1	0	1	1	1	0	0	5CH
Fis^1	745	1	0	1	0	1	1	1	57H
G^1	790	1	0	1	0	0	1	0	52H
Gis^1	840	1	0	0	1	1	0	1	4DH
A^1	886	1	0	0	1	0	0	1	49H
Ais^1	936	1	0	0	0	1	0	1	45H
B^1	993	1	0	0	0	0	0	1	41H
C^2	1057	0	1	1	1	1	0	1	3DH
Cis^2	1111	0	1	1	1	0	1	0	3AH
D^2	1192	0	1	1	0	1	1	0	36H
Dis^2	1260	0	1	1	0	0	1	1	33H
E^2	1338	0	1	1	0	0	0	0	30H
F^2	1394	0	1	0	1	1	1	0	2EH
Fis^2	1490	0	1	0	1	0	1	1	2BH
G^2	1560	0	1	0	1	0	0	1	29H
Gis^2	1680	0	1	0	0	1	1	0	26H
A^2	1771	0	1	0	0	1	0	0	24H
Ais^2	1872	0	1	0	0	0	1	0	22H
B^2	1986	0	1	0	0	0	0	0	20H
C^3	2114	0	0	1	1	1	1	0	1EH
D^3	2341	0	0	1	1	0	1	1	1BH
Dis^3	2521	0	0	1	1	0	0	1	19H
E^3	2621	0	0	1	1	0	0	0	18H
Fis^3	2979	0	0	1	0	1	0	1	15H

18.3.5 Example of Using Melody Circuit

Figure 18-3 shows an example of a melody notation, and Table 18-4 shows note codes of melody examples.

Figure 18-3   Example of Melody Notation

Table 18-4   Note Codes of Melody Examples

Note		Note code													Hexadecimal
		MD0LEN						MD0TON							
		5	4	3	2	1	0	6	5	4	3	2	1	0	
	G^2	1	0	1	1	1	1	0	1	0	1	0	0	0	2F28H
	D^2	0	0	1	1	1	1	0	1	1	0	1	0	1	0F35H
	G^2	0	0	1	1	1	1	0	1	0	1	0	0	0	0F28H
	—	0	0	0	1	1	1	0	0	0	0	0	0	0	0700H
	D^2	0	0	0	1	1	1	0	1	1	0	1	0	1	0735H
	G^2	0	0	1	1	1	1	0	1	0	1	0	0	0	0F28H
	—	0	0	0	1	1	1	0	0	0	0	0	0	0	0700H
	A^2	0	0	0	1	1	1	0	1	0	0	0	1	1	0723H
	B^2	1	1	1	1	1	1	0	0	1	1	1	1	1	3F1FH
	G^2	1	1	1	1	1	1	0	1	0	1	0	0	0	3F28H

18.3.6 Operations of Buzzer Output

A buzzer sound is output in the following procedure.
(1) Select a buzzer mode by setting the BZMD bit of the melody 0 control register (MD0CON) to "1".
(2) Select a buzzer output mode using the melody 0 tempo code register (MD0TMP).
(3) Select a duty of the High level width of the buzzer output waveform using the melody 0 tone length code register (MD0LEN).
(4) Set the buzzer output frequency in the melody 0 scale code register (MD0TON).
(5)Set bit 2 (ENMLT) of the frequency control register 1(FCON1) to "1" to enable the low-speed double clock.
(6) When the M0RUN bit of the melody 0 control register (MD0CON) is set to "1", the waveform equivalent to the buzzer sound that is set from the MD0 pin is output.
Figure 18-4 shows the output waveform of each buzzer output mode.

(1/4) Intermittent sound 1 output waveform

(2/4) Intermittent sound 2 output waveform

(3/4) Single sound output waveform

(4/4) Continuous sound output waveform
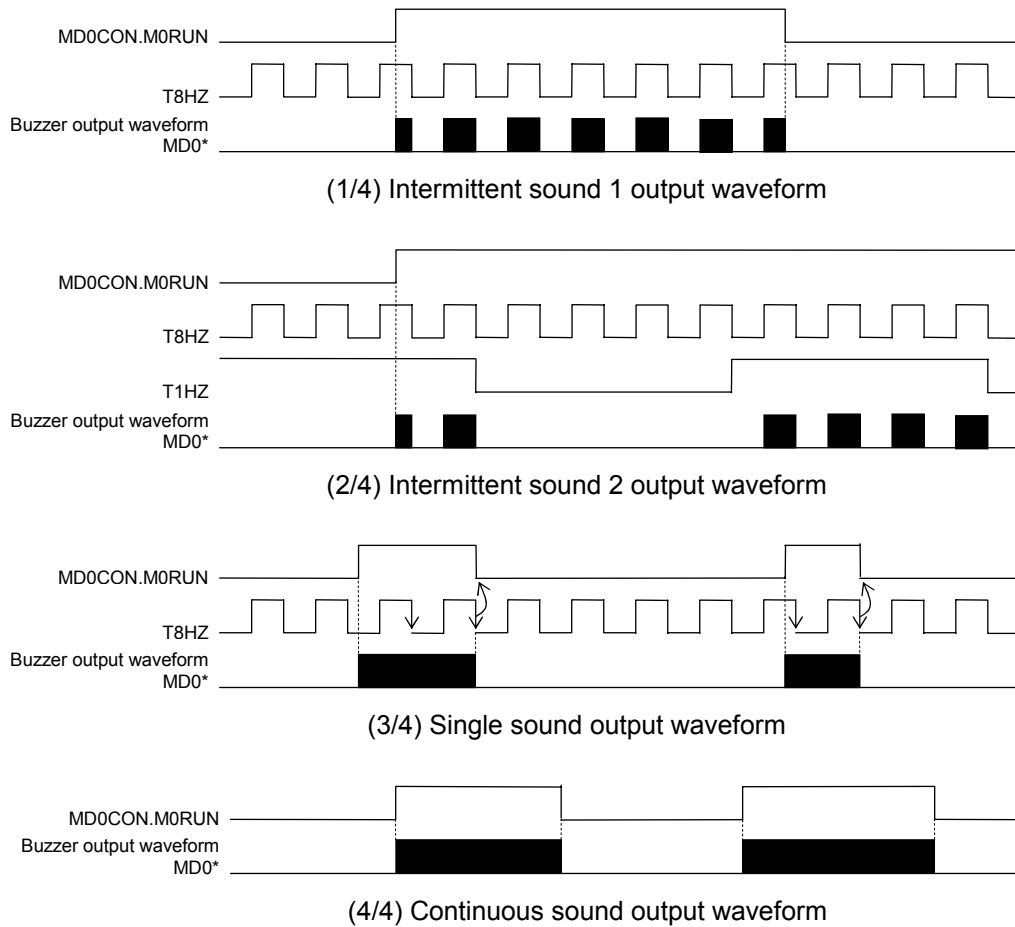
Figure 18-4   Output Waveform of Each Buzzer Output Mode

18.4 Specifying Port Registers

To enable the melody or buzzer function, the applicable bit of each related port register needs to be set. See the following chapters for details of each register function: "Chapter 13 Port 2" for secondary function settings of the port 2 and "Chapter 16 Port 5" for secondary function settings of the port 5.

18.4.1   Functioning P22 Pin (MD0: Output) as the Melody or Buzzer Output

Set the P22MD bit (P2MOD register bit 2) to "1" for selecting the melody or buzzer output as the secondary function of the P22.

Register name	P2MOD register (Address: 0F214H)							
Bit	7	6	5	4	3	**2**	1	0
Bit name	-	-	-	-	-	**P22MD**	P21MD	P20MD
Setting value	-	-	-	-	-	**1**	*	*

Set the P22C1 bit (P2CON1 register bit 2) to "1" and the P22C0 bit (P2CON0 register bit 2) to "1" for selecting the P22 pin state mode to CMOS output.

Register name	P2CON1 register (Address: 0F213H)							
Bit	7	6	5	4	3	**2**	1	0
Bit name	-	-	-	-	-	**P22C1**	P21C1	P20C1
Setting value	-	-	-	-	-	**1**	*	*

Register name	P2CON0 register (Address: 0F212H)							
Bit	7	6	5	4	3	**2**	1	0
Bit name	-	-	-	-	-	**P22C0**	P21C0	P20C0
Setting value	-	-	-	-	-	**1**	*	*

Data of P22D bit (bit2 of P2D register) does not affect to the melody or buzzer function, so don't care the data for the function.

Register name	P2D register (Address: 0F210H)							
Bit	7	6	5	4	3	**2**	1	0
Bit name	-	-	-	-	-	**P22D**	P21D	P20D
Setting value	-	-	-	-	-	******	*	*

\- : Bit that does not exist
* : Bit not related to the Melody function
** : Don't care

Note:
● P2 (Port 2) is an output-only pin and does not have the register to select the data direction(input or output).
● The P22 pin output characteristics are VOL1 and VOH1 (described in Appendix C, "Electrical Characteristics")
   when the P22MD bit is "1"
   (melody/buzzer is selected as the secondary function), and VOL2 and VOH2 when the bit is "0".

18.4.2 Functioning P50 Pin (MD0: Output) as the Melody or Buzzer Output

Set the P50MD1 bit (P5MOD1 register bit 0) to "0" and the P50MD0 bit (P5MOD0 register bit 0) to "1" for selecting the melody or buzzer output as the secondary function of the P50.

Register name	P5MOD1 register (address: 0F22DH)							
Bit	7	6	5	4	3	2	1	**0**
Bit name	-	P56MD1	P55MD1	P54MD1	-	P52MD1	P51MD1	**P50MD1**
Setting value	-	*	*	*	*	*	*	**1**

Register name	P5MOD0 register (address: 0F22CH)							
Bit	7	6	5	4	3	2	1	**0**
Bit name	-	P56MD0	P55MD0	P54MD0	-	P52MD0	P51MD0	**P50MD0**
Setting value	-	*	*	*	*	*	*	**1**

Set the the P50C0 bit (P5CON0 register bit 0) to "1" for selecting the P50 pin state mode to CMOS output. Set the P50DIR bit (P5DIR register bit 0) to "0" for selecting the P50 as an output pin. The P5UD bit (P5CON1 register bit 0) data can either be "0" or "1".

Register name	P5CON1 register (address: 0F22BH)							
Bit	7	6	5	4	3	2	1	**0**
Bit name	-	-	-	-	-	-	-	**P5UD**
Setting value	-	-	-	-	-	-	-	*

Register name	P5CON0 register (address: 0F22AH)							
Bit	7	6	5	4	3	2	1	**0**
Bit name	P57C0	P56C0	P55C0	P54C0	P53C0	P52C0	P51C0	**P50C0**
Setting value	*	*	*	*	*	*	*	**1**

Register name	P5DIR register (address: 0F229H)							
Bit	7	6	5	4	3	2	1	**0**
Bit name	P57DIR	P56DIR	P55DIR	P54DIR	P53DIR	P52DIR	P51DIR	**P50DIR**
Setting value	*	*	*	*	*	*	*	**0**

The P50D bit (P5D register bit 0) data can either be "0" or "1".

Register name	P5D register (address: 0F228H)							
Bit	7	6	5	4	3	2	1	**0**
Bit name	P57D	P56D	P55D	P54D	P53D	P52D	P51D	**P50D**
Setting value	-	-	-	-	*	*	*	**

- : Bit that does not exist
* : Bit not related to the Melody function
** : Don't care

RC Oscillation Type A/D Converter

19. RC Oscillation Type A/D Converter

19.1 Overview

This LSI has a built-in 2-channel RC oscillation type A/D converter (RC-ADC).
The RC-ADC converts resistance values or capacitance values to digital values by counting the oscillator clock whose frequency changes according to the resistor or capacitor connected to the RC oscillator circuits. By using a thermistor or humidity sensor as a resistor, a thermometer or hygrometer can be formed.
In addition, a different sensor for each of the two channels of RC-ADC's RC oscillator circuit can be used to broaden RC-ADC applications; for example, the converter can be used for expansion of measurement range or measurement at two points.
For input clocks, see Chapter 6, "Clock Generation Circuit".

19.1.1 Features

- 2-channel system by time division

19.1.2 Configuration

The RC-ADC consists of two RC oscillator circuits to form two channels, Counter A (RADCA0 and RADCA1) and Counter B (RADCB0 and RADCB1) as 16-bit binary counters, and an RC-ADC control circuit (RADCON, RADMOD). Figure 19-1 shows the configuration of the RC-ADC.

RADMOD　　　: RC-ADC mode register
RADCON　　　: RC-ADC control register
RADCA0~1　　: RC-ADC Counter A register
RADCB0~1　　: RC-ADC Counter B register
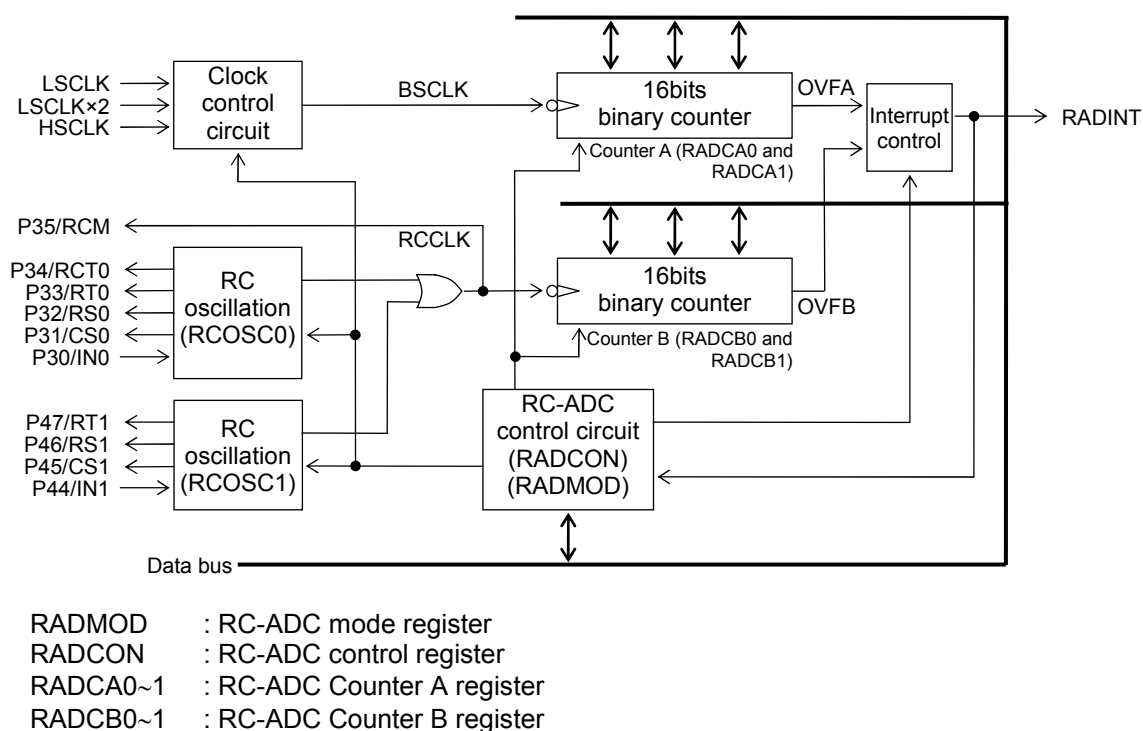
Figure 19-1　Configuration of RC-ADC

19.1.3 List of Pins

Pin name	I/O	Function
P30/IN0	I	Channel 0 oscillation input pin. Used for the secondary function of the P30 pin.
P31/CS0	O	Channel 0 reference capacitor connection pin. Used for the secondary function of the P31 pin.
P32/RS0	O	Channel 0 reference resistor connection pin. Used for the secondary function of the P32 pin.
P33/RT0	O	Pin for connection with a resistive sensor for measurement on Channel 0. Used for the secondary function of the P33 pin.
P34/RCT0	O	Pin for connection with a resistive/capacitive sensor for measurement on Channel 0. Used for the secondary function of the P34 pin.
P35/RCM	O	RC oscillation monitor pin. Used for the secondary function of the P35 pin.
P44/IN1	I	Channel 1 oscillation input pin. Used for the secondary function of the P44 pin.
P45/CS1	O	Channel 1 reference capacitor connection pin. Used for the secondary function of the P45 pin.
P46/RS1	O	Channel 1 reference resistor connection pin. Used for the secondary function of the P46 pin.
P47/RT1	O	Pin for connection with a resistive sensor for measurement on Channel 1. Used for the secondary function of the P47 pin.

19.2 Description of Registers

19.2.1 List of Registers

Address	Name	Symbol(Byte)	Symbol (Word)	R/W	Size	Initial value
0F300H	RC-ADC Counter A register 0	RADCA0	—	R/W	8	00H
0F301H	RC-ADC Counter A register 1	RADCA1	—	R/W	8	00H
0F304H	RC-ADC Counter B register 0	RADCB0	—	R/W	8	00H
0F305H	RC-ADC Counter B register 1	RADCB1	—	R/W	8	00H
0F308H	RC-ADC mode register	RADMOD	—	R/W	8	00H
0F309H	RC-ADC control register	RADCON	—	R/W	8	00H

19.2.2 RC-ADC Counter A Registers (RADCA0–1)

Address: 0F300H
Access: R/W
Access size: 8-bit
Initial value: 00H

	7	6	5	4	3	2	1	0
RADCA0	RAA7	RAA6	RAA5	RAA4	RAA3	RAA2	RAA1	RAA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F301H
Access: R/W
Access size: 8-bit
Initial value: 00H

	7	6	5	4	3	2	1	0
RADCA1	RAA15	RAA14	RAA13	RAA12	RAA11	RAA10	RAA9	RAA8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

RADCA0 and RADCA1 are special function registers (SFRs) for reading from and writing to the Counter A of the RC-ADC. RADCA0 and RADCA1 are 16-bit binary counters.

Note:
  After writing data into the RC-ADC counter A register, be sure to read it to check that the data has been written correctly.
  When A/D conversion starts after data is written, the value that has been written is read during A/D conversion (RARUN = 1).
  When A/D conversion terminates (RARUN = 0), the count value is read.

19.2.3 RC-ADC Counter B Registers (RADCB0–1)

Address: 0F304H
Access: R/W
Access size: 8-bit
Initial value: 00H

	7	6	5	4	3	2	1	0
RADCB0	RAB7	RAB6	RAB5	RAB4	RAB3	RAB2	RAB1	RAB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Address: 0F305H
Access: R/W
Access size: 8-bit
Initial value: 00H

	7	6	5	4	3	2	1	0
RADCB1	RAB15	RAB14	RAB13	RAB12	RAB11	RAB10	RAB9	RAB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

RADCB0 and RADCB1 are special function registers (SFRs) for reading from and writing to the Counter B of the RC-ADC. RADCB0 and RADCB1 are 16-bit binary counters.

Note:
After writing data into the RC-ADC counter B register, be sure to read it to check that the data has been written correctly.
When A/D conversion starts after data is written, the value that has been written is read during A/D conversion (RARUN = 1).
When A/D conversion terminates (RARUN = 0), the count value is read.

19.2.4 RC-ADC Mode Register (RADMOD)

Address: 0F308H
Access: R/W
Access size: 8-bit
Initial value: 00H

	7	6	5	4	3	2	1	0
RADMOD	RACK2	RACK1	RACK0	RADI	OM3	OM2	OM1	OM0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

RADMOD is a special function register (SFR) used to select the A/D conversion mode of the RC-ADC.

[Description of Bits]
- **OM3-0** (bits 3 to 0)
  The OM3–0 bits are used to select an oscillation mode for the RC oscillator circuits.

OM3	OM2	OM1	OM0	Description
0	0	0	0	IN0 pin external clock input mode (initial value)
0	0	0	1	RS0-CS0 oscillation mode
0	0	1	0	RT0–CS0 oscillation mode
0	0	1	1	RT_{0-1}–CS0 oscillation mode
0	1	0	0	RS0–CT0 oscillation mode
0	1	0	1	RS1–CS1 oscillation mode
0	1	1	0	RT1–CS1 oscillation mode
0	1	1	1	IN1 pin external clock input mode
1	*	*	*	Prohibited

- **RADI** (bit 4)
  The RADI bit is used to choose whether to generate the RC-ADC interrupt request signal (RADINT) by an overflow at Counter A or Counter B.

RADI	Description
0	Generates an interrupt request by Counter A overflow (initial value).
1	Generates an interrupt request by Counter B overflow.

- **RACK2-0** (bits 7 to 5)
  The RACK2 to RACK0 bits are used to select the base clock of Counter A (BSCLK).

RACK2	RACK1	RACK0	Description
0	0	0	LSCLK (initial value)
0	0	1	LSCLK×2
0	1	0	HSCLK
0	1	1	1/2HSCLK
1	0	0	1/4HSCLK
1	0	1	1/8HSCLK
1	1	*	Setting prohibited (no clock is supplied)

Note:
When specifying LSCLK x 2 for the base clock, enable the operation of the low-speed double clock by setting bit 2 (ENMLT) of the frequency control register 1 (FCON1) to "1".

19.2.5 RC-ADC Control Register (RADCON)

Address: 0F309H
Access: R/W
Access size: 8-bit
Initial value: 00H

	7	6	5	4	3	2	1	0
RADCON	—	—	—	—	—	—	—	RARUN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

RADCON is a special function register (SFR) used to control A/D conversion operation of the RC-ADC.

[Description of Bits]

- **RARUN** (bit 0)
  The RARUN bit is used to start A/D conversion of the RC-ADC. When RARUN is set to "1", A/D conversion starts. If Counter A or Counter B overflows with RARUN set to "1", the bit is automatically reset to "0". RARUN is set to "0" at system reset.

RARUN	Description
0	Stops A/D conversion (initial value).
1	Starts A/D conversion.

Note:
　　When A/D conversion is stopped by resetting the RARUN to "0", the RC-ADC does not perform properly without the following procedures.
　　1) Set the "DRAD" bit of the Block Control Register 4 (BLKCON4) to "1" , in order to disable the RC-ADC.
　　2) Reset the "DRAD" bit of the Block Control Register 4 (BLKCON4) to "0" , in order to enable the RC-ADC.
　　3) Set up the RC-ADC again by following the required procedures, then restart.

19.3 Description of Operation

Counter A (RADCA0 and RADCA1) is a 16-bit binary counter for counting the base clock (BSCLK), which is used as the standard of time. Counter A can count up to 0FFFFH.

Counter B (RADCB0 to RADCB1) is a 16-bit binary counter for counting the oscillator clock (RCCLK) of the RC oscillator circuits. Counter B can count up to 0FFFFH.

Counters A and B are provided with overflow flags (OVFA and OVFB, respectively). Each overflow output results in generation of an RC-ADC interrupt request signal (RADINT). Use the RADI bit of the RC-AC mode register (RADMOD) to select whether to generate an overflow interrupt by an overflow on Counter A or Counter B: setting RADI to "0" specifies Counter A overflow and setting it to "1" specifies Counter B overflow.

The RARUN bit of the RC-AD control register (RADCON) is used to start or stop RC-ADC conversion operation. When RARUN is set to "0", the oscillator circuits stop, so that counting will not be performed. When RARUN is set to "1", RC oscillation starts, when the RC oscillator clock (RCCLK) and the base clock (BSCLK) start counting through Counter B and Counter A.

The RC oscillation section has a total of eight types of oscillation modes based on the two oscillator circuits of RCOSC0 and RCOSC1, and mode selection is made by the RC-ADC mode register (RADMOD).

P30–34, P44–47, and P35 must be configured as their secondary function input or output when using 1) the RC oscillator circuit RCOSC0, 2) the RC oscillator circuit RCOSC1, and 3) the RC monitor pin (RCM) that outputs RC oscillation waveforms, respectively. For the RC oscillator circuit configuration, see "19.1.2 Configuration." For the secondary functions of Port 3, see Chapter 14, "Port 3." For the secondary functions of Port 4, see Chapter 15, "Port 4."

19.3.1 RC Oscillator Circuits

RC-ADC performs A/D conversion by converting the oscillation frequency ratio between a reference resistor (or capacitor) and a resistive sensor (or capacitive sensor) such as a thermistor to digital data.

By making RC oscillation occur both on the reference side and on the sensor side with the reference capacitor the error factor that the RS oscillator circuit itself is eliminated, thereby making it possible to perform the A/D conversion of the characteristics of the sensor itself.

Also, by calculating the ratio between the oscillation frequency on the reference side and that on the sensor side and then calculating the correlation between the calculated ratio and temperatures that the sensor characteristics have in advance, a temperature can be obtained based on that calculated ratio.

Table 19-1 lists the eight types of oscillation modes, one of which is selected by the RC-ADC mode register (RADMOD) OM3–0 bits.

Table 19-1   Oscillation Modes from Which Selection Is Made by OM3–0 Bits

Mode No.	RADMOD				RCOSC0 output pin				RCOSC1 output pin			Mode	
	OM3	OM2	OM1	OM0	RS0	RT0	CRT0	CS0	RS1	RT1	CS1		
0	0	0	0	0	Z	Z	Z	Z	Z	Z	Z	IN0 external clock input mode	
1	0	0	0	1	1/0	Z	Z	0/1	Z	Z	Z	RS0–CS0 oscillation	RCOSC0 oscillation mode
2	0	0	1	0	Z	1/0	Z	0/1	Z	Z	Z	RT0–CS0 oscillation	
3	0	0	1	1	Z	Z	1/0	0/1	Z	Z	Z	RT$_{0-1}$–CS0 oscillation	
4	0	1	0	0	1/0	Z	0/1	Z	Z	Z	Z	RS0–CT0 oscillation	
5	0	1	0	1	Z	Z	Z	Z	1/0	Z	0/1	RS1–CS1 oscillation	RCOSC1 oscillation mode
6	0	1	1	0	Z	Z	Z	Z	Z	1/0	0/1	RT1–CS1 oscillation	
7	0	1	1	1	Z	Z	Z	Z	Z	Z	Z	IN1 external clock input mode	
8	1	*	*	*	Z	Z	Z	Z	Z	Z	Z	(Prohibited)	

Note)　*　　　　　: Indicates arbitrary.
　　　　Z　　　　: Indicates high-impedance output.
　　　　1/0, 0/1　: Indicates active output.
　　　　(Prohibited)　: The oscillator clock is not supplied even by setting the RARUN bit to "1" or by starting A/D conversion.

In Table 19-1, mode No.0 and mode No.7 are modes where external clocks to be input to the IN0 or IN1 pin are used for measurement with the RC oscillator circuit stopped.

As shown in Table 19-1, the two oscillator circuits, RCOSC0 and RCOSC1, are so specified that they cannot operate concurrently in order to prevent interference in oscillation from occurring when they oscillate concurrently.

The relationship between an oscillation frequency f_{RCCLK} and an RC constant is expressed by the following equation:

$$\frac{1}{f_{RCCLK}} \quad = \quad t_{RCCLK} \quad = \quad k_{RCCLK} \cdot R \cdot C$$

where t_{RCCLK} is the period of the oscillator clock, k_{RCCLK} the proportional constant, and R x C the product of capacitances CS, CT, (CS+CVR) and (CT+CVR) and resistances RS and RT. The value of k_{RCCLK} slightly changes depending on the value of the supply voltage VDD, RI, R, or C.

Table 19-2 lists the typical k_{RCCLK} values.

Table 19-2   Typical Values of the Proportional Constant k_{RCCLK} of RC Oscillator Circuits

V_{DD} (V)	CSn, CTn (pF)	CVRn(pF)	RSn, RTn (kΩ)	k_{RCCLK} (Typ.)
3	560	820	10	1.26
	560	820	100	1.24
	560	820	15	1.25
	560	820	105	1.24
1.5	560	820	15	1.26
	560	820	105	1.22

Note)   n=0,1,0-1

Note:

Out of the Port 3 and Port 4 pins, pins that are to be used for the RC-ADC function must be configured as secondary function input or output using the mode register (P3MOD0, P4MOD0, P4MOD1) of the corresponding port.

All the Port 3 pins except P35/RCM (see Section 19.1.3, "List of Pins") are configured as pins dedicated to the RC-ADC function during A/D conversion. Therefore, all the Port 3 pins except P35 cannot be used as their primary functions in oscillation mode No. 0, 1, 2, 3 or 4, which is selected by the RADMOD register. In the same way, the P44 to P47 pins of Port 4 cannot be used as their primary functions in oscillation mode No. 5, 6 or 7.

Figures 19-2 to 24-5 show the oscillator circuit configurations, the modes of oscillation for each configuration, and the OM3–0 bit settings.

OM3	OM2	OM1	OM0	oscillation mode
0	0	0	1	Oscillates with the reference resistor RS0 and CS0
0	0	1	0	Oscillates with the sensor RT0 and CS0
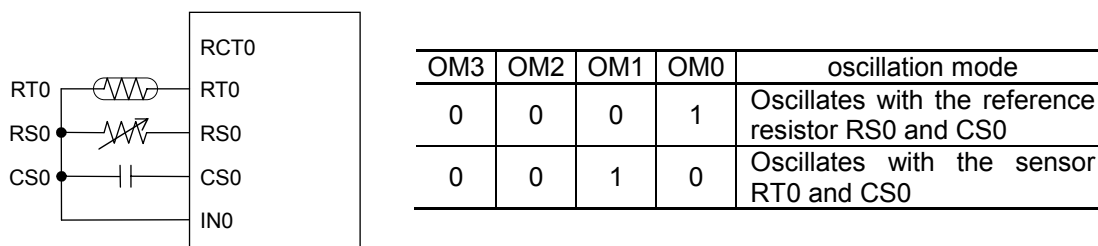
Figure 19-2   When RCOSC0 Is Used for Measurement with One Resistive Sensor

Note:

The unused pin RCT0 shown in Figure 19-2 is configured as a pin dedicated to the RC-ADC function during A/D conversion; therefore, during A/D conversion, RCT0 cannot be used as a primary function port (P34).
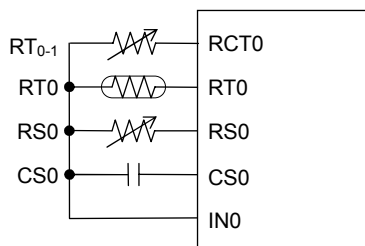
OM3	OM2	OM1	OM0	oscillation mode
0	0	0	1	Oscillates with the reference resistor RS0 and CS0
0	0	1	0	Oscillates with the sensor RT0 and CS0
0	0	1	1	Oscillates with the reference resistor RT_{0-1} and CS0

Figure 19-3   When RCOSC0 Is Used for Measurement with One Resistive Sensor
(Two points are adjusted with two reference resistors)
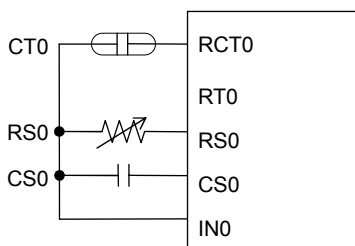
OM3	OM2	OM1	OM0	oscillation mode
0	0	0	1	Oscillates with the reference resistor RS0 and CS0
0	1	0	0	Oscillates with the sensor RS0 and CT0

Figure 19-4   When RCOSC0 Is Used for Measurement with One Capacitive Sensor

Note:
The unused pin RT0 shown in Figure 19-4 is configured as a pin dedicated to the RC-ADC function during A/D conversion; therefore, during A/D conversion, RT0 cannot be used as a primary function port (P33).
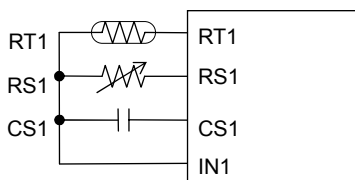
OM3	OM2	OM1	OM0	oscillation mode
0	1	0	1	Oscillates with the reference resistor RS1 and CS1
0	1	1	0	Oscillates with the sensor RT1 and CS1

Figure 19-5   When RCOSC1 Is Used for Measurement with One Resistive Sensor

19.3.2 Counter A/Counter B Reference Modes

There are the following two modes of RC-ADC conversion operation:

•Counter A reference mode (RADMOD RADI = "0")

   In this mode, a gate time is determined by Counter A and the base clock (BSCLK), which is used as the time reference, then the RC oscillator clock (RCCLK) is counted by Counter B within the gate time to make the content of Counter B the A/D conversion value.

   The A/D conversion value is proportional to RC oscillation frequency.

•Counter B reference mode (RADMOD RADI = "1")

   In this mode, a gate time is determined by Counter B and the RC oscillator clock (RCCLK), and the base clock (BSCLK), which is used as the time reference, is counted by Counter A within the gate time to make the content of Counter A the A/D conversion value.

   The /D conversion value is inversely proportional to RC oscillation frequency.

(1) Operation in Counter A reference mode

Figure 19-6 shows the operation timing in Counter A reference mode.
Following is an example of operation procedure in Counter A reference mode:

① Preset to Counter A (RADCA1 and RADCA0) the value obtained by subtracting the count value "nA0" from the maximum value + 1 (10000H). The product of the count value "nA0" and the BSCLK clock cycle indicates the gate time.

② Preset "0000H" to Counter B (RADCB1 and RADCB0).

③ Set the OM3–OM0 bits of RADMOD to desired oscillation mode. (See Table 19-1.)

④ Set the RADI bit of RADMOD to "0" to specify generating of an interrupt request signal by Counter A overflow.

⑤ Set the RARUN bit of RADCON to "1" to start A/D conversion.

Counter A starts counting of the base clock (BSCLK) when RARUN is set to "1" and the RCON signal (signal synchronized with the fall of the base clock) is set to "1". When Counter A overflows, the RARUN bit is automatically reset to "0" (⑥) and counting is terminated. At the same time, an RC-ADC interrupt request (RADIN) occurs (⑦).

When the RCON signal is set to "1", the RC oscillator circuit starts operation and Counter B starts counting of the RC oscillator clock (RCCLK). When the RARUN bit is reset to "0" due to overflow of Counter A, RC oscillation stops and Counter B stops counting.

The final count value "nB0" of Counter B is the RCCLK count value during the gate time "nA0 x t_{BSCLK}" and is expressed by the following expression:

$$nB0 \quad \cong \quad nA0 \cdot \frac{t_{BSCLK}}{t_{RCCLK}} \quad \propto \quad f_{RCCLK}$$

where t_{BSCLK} indicates the BSCLK period and t_{RCCLK} the RCCLK period. That is, "nB0" is a value proportional to the RC oscillation frequency f_{RCCLK}.
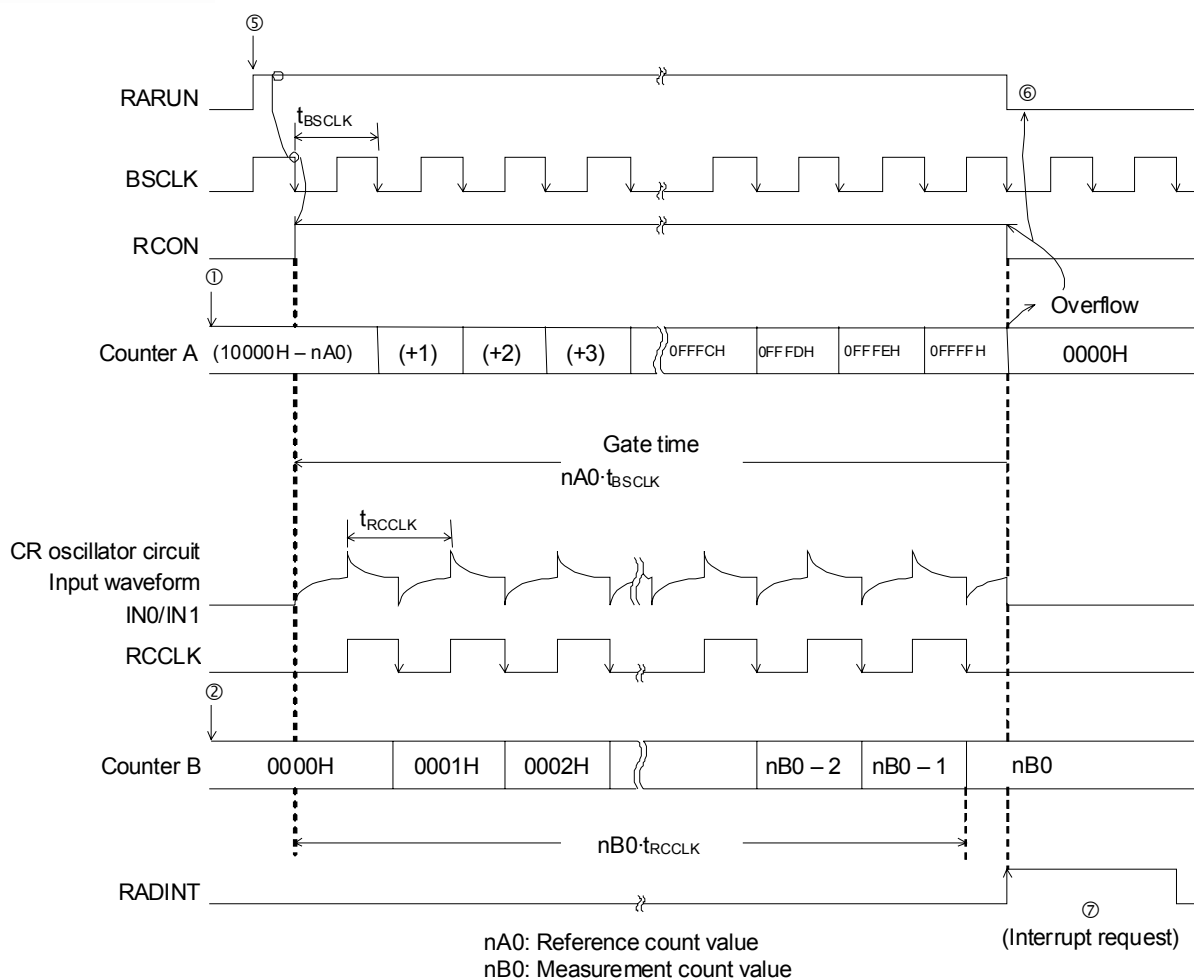
Figure 19-6   Operation Timing in Counter A Reference Mode

(2) Operation in Counter B reference mode

Figure 19-7 shows the operation timing in Counter B reference mode.
Following is an example of operation procedure in Counter B reference mode:

① Preset to Counter B (RADCB1 and RADCB0) the value obtained by subtracting the count value "nB1" from the maximum value + 1 (10000H). The product of the count value "nB1" and the RCCLK clock cycle indicates the gate time.
② Preset "0000H" to Counter A (RADCA1 and RADCA0).
③ Set the OM3–OM0 bits of RADMOD to desired oscillation mode. (See Table 19-1.)
④ Set the RADI bit of RADMOD to "1" to specify generating of an interrupt request signal by Counter B overflow.
⑤ Set the RARUN bit of RADCON to "1" to start A/D conversion.

When the RARUN bit is set to "1" and the RCON signal (signal synchronized with the fall of the base clock) is set to"1", the RC oscillator circuit starts operation and Counter B starts counting of the RC oscillator clock (RCCLK). When Counter B overflows, the RARUN bit is automatically reset (⑥) and conversion operation terminates. At the same time, an RC-ADC interrupt request (RADINT) occurs. (⑦)

When the RCON signal is set to "1", Counter A starts counting of the base clock (BSCLK). When the RARUN bit is reset due to overflow of Counter B, Counter A stops counting.
The final count "nA1" of Counter A is the CLK count value during the gate time "nB1 x t_{RCCLK}" and is expressed by the following expression:

$$nA1 \cong nB1 \cdot \frac{t_{RCCLK}}{t_{BSCLK}} \propto \frac{1}{f_{RCCLK}}$$

That is, "nA1" is a value inversely proportional to the RC oscillation frequency f_{RCCLK}.
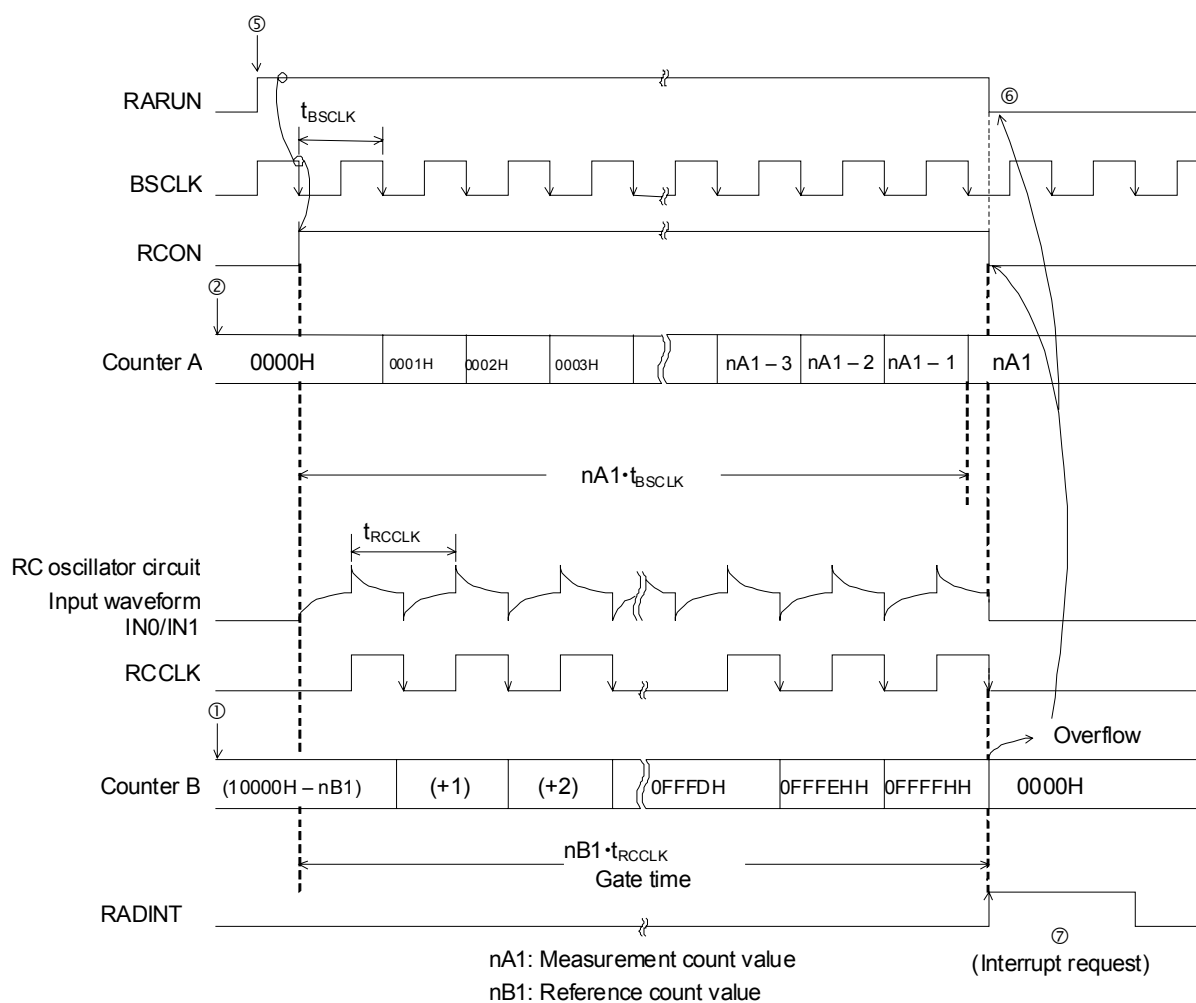
Figure 19-7   Operation Timing in Counter B Reference Mode

19.3.3 Example of Use of RC Oscillation Type A/D Converter

This section describes the method of performing A/D conversion for sensor values in Counter A and B reference modes by taking temperature measurement by a thermistor as an example.
Figure 19-8 shows the circuit configuration of 1-thermistor RC oscillator circuit using RCOSC0.
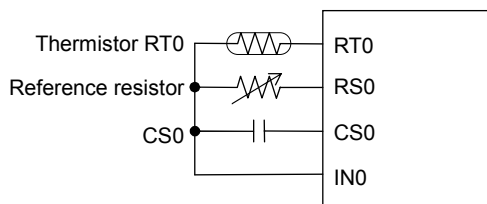
Figure 19-8   Configuration of 1-Thermistor RC Oscillator Circuit Using RCOSC0

Figure 19-9 shows the temperature characteristics of the thermistor resistance RT0.
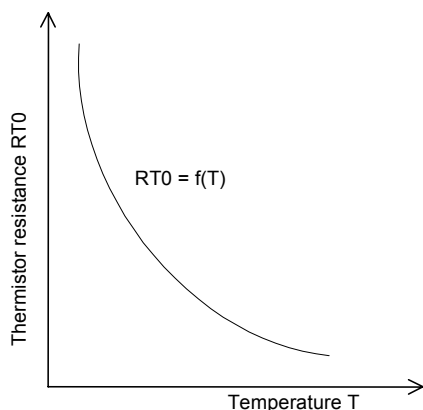
Figure 19-9   Temperature Characteristics of   Figure 19-10   A/D Conversion
Thermistor Characteristics   (Ideal characteristics when nT0 is proportional to RT0)

RT0 is expressed as a function of temperature T by the following equation:

$$RT0 \quad = \quad f(T)$$

Figure 19-10 shows the ideal characteristics of A/D conversion with the assumption that RT0 is an analog quantity. In the ideal characteristics, the A/D conversion value nT0 will purely depend on RT0 only. Assuming that nT0 is proportional to RT0, let proportional constant be K, then nT0 has the following relationship with temperature T:

$$nT0 \quad = \quad K{\cdot}RT0 \quad = \quad K{\cdot}f(T) \quad ... \text{Expression A}$$

Therefore, temperature T can be expressed as a digital value by performing the conversion processing that accords with the characteristics shown in Figure 19-9 for nT0 by software.

To convert from an RT0 value to a digital value, the ratio is used between a) the oscillation frequency by the thermistor connected to the RT0 pin and the capacitor connected to the CS0 pin and b) the oscillation frequency by the reference resistor (which ideally should have no temperature characteristics) connected to the RS0 pin and the capacitor connected to the CS0 pin. This is for making the conditions other than resistance equal to eliminate the error factor in oscillation characteristics.
As shown in Figures 19-9 and 19-11, the RT0 value depends on temperature T and the RS0 value is assumed to be constant regardless of temperature T. It is ideal if the characteristics of the oscillation frequency f_{OSC} to temperature T using these resistances will be like the solid lines in Figures 19-12 and 19-13; however, in reality, it would appear that they will be like the dotted lines due to error factors such as IC temperature characteristics.
Since the condition of f_{RCCLK} (RT0) and that of f_{RCCLK} (RS0) are the same except for the resistances, the error ratios are almost the same; therefore, errors can almost be eliminated by using the ratio between f_{RCCLK} (RT0) and f_{RCCLK} (RS0).

The ratio between f_{RCCLK} (RT0) and f_{RCCLK} (RS0) is equivalent to the above-mentioned A/D conversion value nT0 that should ideally depend only on RT0.
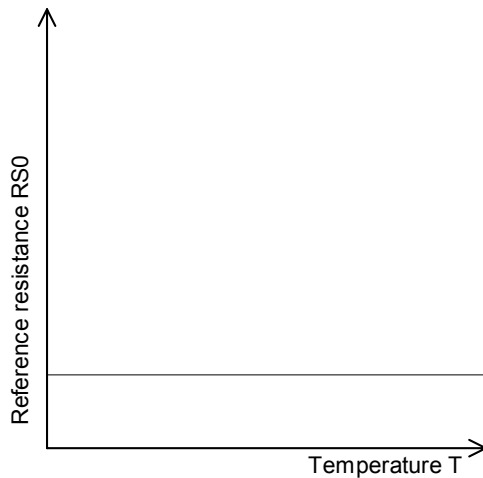
Figure 19-11   Temperature Characteristics of Reference Resistor
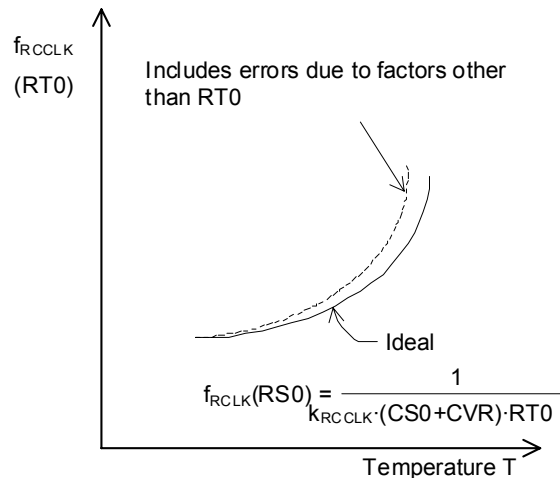
Figure 19-12   Oscillation Characteristics of Thermistor

$$f_{RCLK}(RS0) = \frac{1}{k_{RCCLK} \cdot (CS0 + CVR) \cdot RT0}$$

$$f_{RCCLK}(RS0) = \frac{1}{k_{RCCLK} \cdot (CS0 + CVR) \cdot RS0}$$
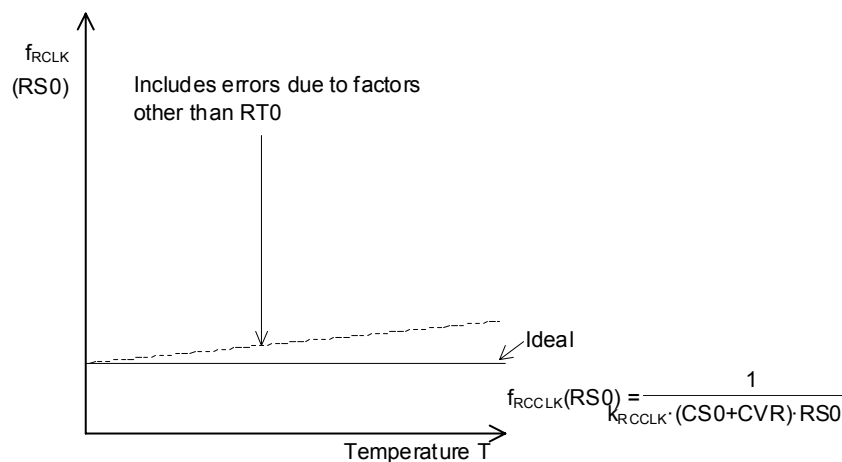
Figure 19-13   Oscillation Characteristics of Reference Resistor

Figure 19-14 shows, as an example of method, a timing chart of one cycle of conversion from analog value RT0 to a digital value, that is, A/D conversion.

Basically, one A/D conversion cycle must consist of two steps, as shown in Figure 19-14. The reason for requiring two steps is that the reference resistor and the thermistor must first be oscillated separately and then the ratio between the oscillation frequencies of them is used, as described above.

In the example below, operation for these two steps is performed using the following combination:

•First step = RC oscillation with RS0 in Counter A reference mode
•Second step = RC oscillation with RT0 in Counter B reference mode

Besides this, there would be several possible A/D conversion methods.

In the above method, the operation time (gate time) for the second step fluctuates depending on the value of thermistor RT0. To avoid the fluctuation of the operation time, using a method that uses the following combination is recommended:

•First step = RC oscillation with RS0 in Counter B reference mode
•Second step = RC oscillation with RT0 in Counter A reference mode

A/D conversion procedure is explained below by taking Figure 19-14 as an example.
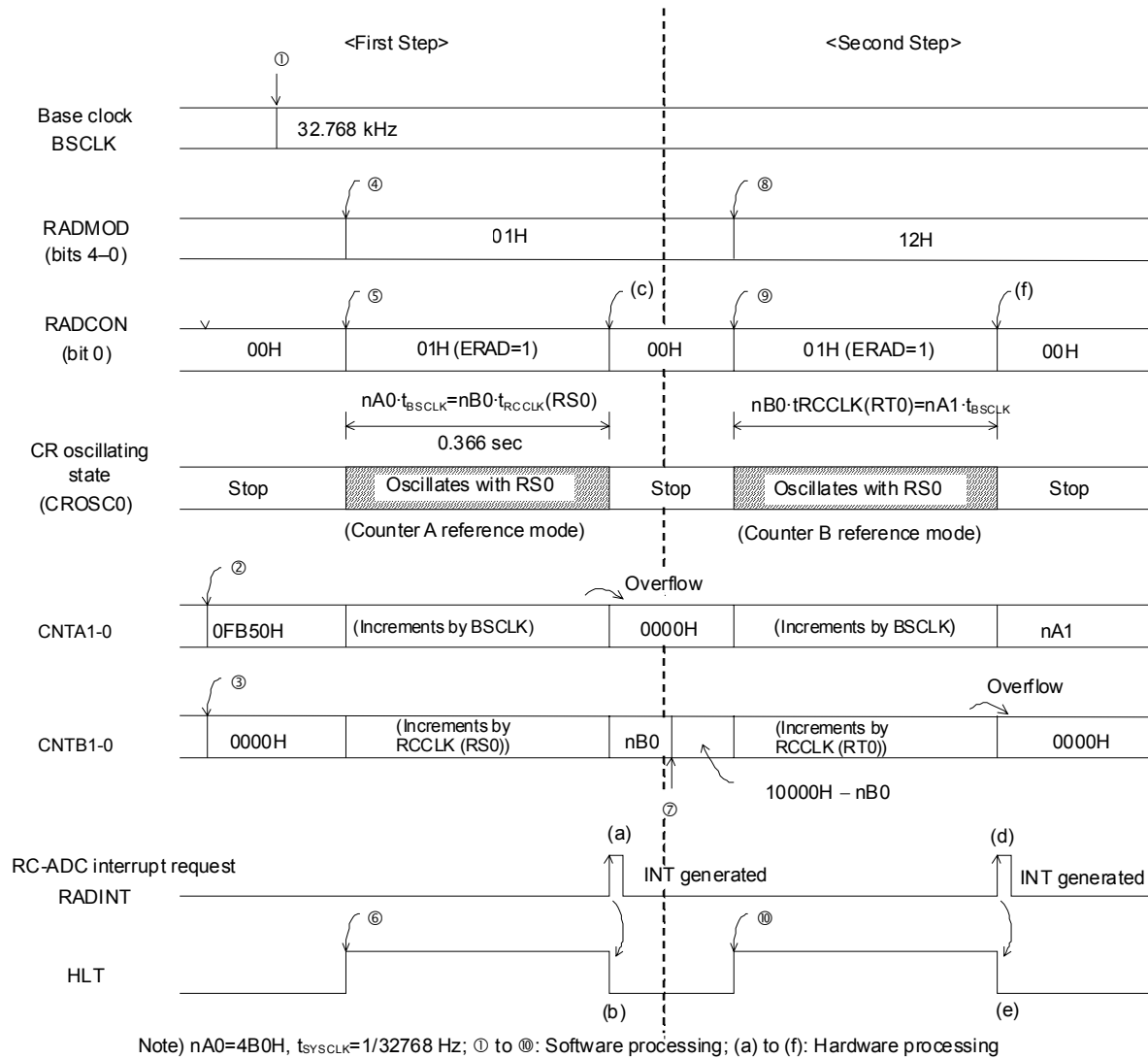
Figure 19-14   Timing Chart for 1 Cycle of A/D Conversion (Example)

<First step>

① Set the base clock to 32.768 kHz. (Write "00H" in FCON0.)
② Preset "10000H – nA0" in Counter A.
③ Preset "0000H" in Counter B.
④ Write "01H" in RADMOD to select Counter A reference mode and the oscillation mode that uses reference resistance RS0.
⑤ Write "01H" in RADCON to start A/D conversion operation.
⑥ Write "1" in the HLT bit of SBYCON to set the device to HALT mode.

Note:
  In this example, nA0 is set to 4B0H because the gate time "nA0 x t_{BSCLK}" in oscillation mode with reference resistor RS0 is set to 0.366 second. The value of nA0 is related to how much the margin of the quantization error of the A/D conversion is: the greater the nA0 value is, the smaller the margin of error becomes.
  To reduce noise contamination to the RC oscillator circuit caused by CPU operation, it is recommended to constantly put the device into HALT mode during operation of RC oscillation.

From this point of time, the RC oscillator circuit (RCOSC0) continues oscillation for about 0.366 second with the reference resistance RS0. Then, when Counter A overflows, the RADINT signal is set to "1" and an RC-ADC interrupt

request is generated. (Section (a)). Also, the generation of interrupt request releases HALT mode (section (b)) and at the same time, A/D conversion operation stops. (Section (c), RARUN bit = "0"). At this time, Counter A is set to "0000H". The content of Counter B at this time is expressed by the following expression:

$$nB0 \quad = \quad nA0 \bullet \quad \frac{t_{BSCLK}}{t_{RCCLK}(RS0)} \quad \quad ... \text{ Expression B}$$

That completes the operations in First Step.

<Second step>

①   Calculate "10000H – nB0" from the content of Counter B "nB0" and set the obtained value in Counter B.
At this point, Counter A needs to be cleared; however, no processing is required since the counter is already set to "0000H".
②   Write "12H" in RADMOD to select Counter B reference mode and the oscillation mode that uses thermistor RT0.
③   Write "01H" in RADCON to start A/D conversion operation.
④   Write "1" in the HLT bit of SBYCON to set the device to HALT mode.

The RC oscillator circuit (RCOSC0) oscillates with thermistor RT0 from this point until Counter B overflows. This period is equal to the product of "nB0" obtained in the First Step and the oscillation period t_{RCCLK} (RT0) using RT0.
When Counter B overflows, the RADINT signal is set to "1" and an RC-ADC interrupt request is generated. (Section (d)). Also, the generation of interrupt request releases HALT mode (section (e)) and at the same time, A/D conversion operation stops. (Section (f), RARUN bit = "0").
This completes the operations in Second Step.

The content of Counter A at this time becomes the A/D conversion value nA1, which is expressed by the following expression:

$$nA1 \quad = \quad nB0 \bullet \quad \frac{t_{RCCLK}(RT0)}{t_{BSCLK}} \quad \quad ... \text{ Expression C}$$

From expressions B and C, nA1 is expressed by the following expression:

$$nA1 \quad = \quad nA0 \bullet \quad \frac{t_{RCCLK}(RT0)}{t_{RCCLK}(RS0)} \quad \quad ... \text{ Expression D}$$

where t_{RCCLK} (RS0) is the oscillator clock period by reference resistor RS0 and t_{RCCLK} (RT0) the oscillator clock period by thermistor RT0.
Since the oscillation period is expressed by "$t_{RCCLK} = k_{RCCLK} \times R \times C$", t_{RCCLK} (RS0) and t_{RCCLK} (RT0) are expressed by the following expressions:

$$t_{RCCLK} (RS0) \quad = \quad k_{RCCLK} \bullet (CS0+CVR) \bullet RS0$$
$$... \text{ Expression E}$$
$$t_{RCCLK} (RT0) \quad = \quad k_{RCCLK} \bullet (CS0+CVR) \bullet RT0$$

When expression E is substituted for expression D, nA1 will be:

$$nA1 \quad = \quad nA0 \bullet \quad \frac{RT0}{RS0}$$

Since "nA0" ("4B0H" in this example) and RS0 are constants whose values are fixed, "nA1" is a digital value proportional to RT0. This very "nA1" corresponds to "nT0" in expression A.

That concludes the description of the A/D conversion method using a thermistor. "nA1" that has been obtained must further be converted to a value such as a temperature indication value for thermometer by program according to the temperature-to-resistance characteristics of the thermistor.

19.3.4 Monitoring RC Oscillation

The RC oscillator clock (RCCLK) can be output using the secondary function of the P35 pin of Port 3. See Chapter 14, "Port 3," for the details of the secondary function of P35.

Monitoring RC oscillation is useful for checking the characteristics of the RC oscillator circuit. That is, the relationship between a sensor, such as a thermistor, and the oscillation frequency can be measured. For instance, the coefficient for conversion from the above-described nA1 value to a temperature indication value can be obtained by checking the relationship between the ambient temperature of a thermistor-incorporated RC oscillator circuit, the oscillation frequency with thermistor RT0, and the oscillation frequency with reference resistor RS0.

Note:
P35 (RCM) is a monitor pin for oscillation clock. The Channel 0 and Channel 1 share the monitor pin.
Please use P35 (RCM) for the evaluation purpose and disable the output while operating in an actual application to minimize the noise.

19.4 Specifying Port Registers

To enable the RC-ADC function, the applicable bit of each related port register needs to be set. See Chapter 14, "Port 3" and Chapter 15, "Port 4" for detail about the port registers.

19.4.1   Functioning P35(RCM), P34(RCT0), P33(RT0), P32(RS0), P31(CS0) and P30(IN0) as the RC-ADC(Ch0)

Set P35MD0-P30MD0(bit5-bit0 of P3MOD0 register) to "1", for specifying the RC-ADC as the secondary function of P35, P34, P33, P32, P31 and P30.

Register name	P3MOD0 register (Address: 0F21CH)							
Bit	7	6	5	4	3	2	1	0
Bit name	P37MD0	P36MD0	**P35MD0**	**P34MD0**	**P33MD0**	**P32MD0**	**P31MD0**	**P30MD0**
Setting value	-	-	1	1	1	1	1	1

Set the P34C1 to P30C1 bits (P3CON1 register bits 4 to 0) to "0", the P34C0 to P30C0 bits (P3CON0 register bits 4 to 0) to "0", and the P34DIR to P30DIR bits (P3DIR register bits 4 to 0) to "1" for selecting the state mode of the P34, P33, P32, P31, and P30 to high-impedance input. The P34C1-P30C1 bit and P34C0-P30C0 bit can be set to all "1" instead of all "0" to select the high-impedance inputs.
Set the P35C1 bit (P3CON1 register bit 5) to "1", the P35C0 bit (P3CON0 register bit 5) to "1", and the P35DIR bit (P3DIR register bit 5) to "0" for selecting the P35 state mode to CMOS output.

Register name	P3CON1 register (Address: 0F21BH)							
Bit	7	6	5	4	3	2	1	0
Bit name	P37C1	P36C1	**P35C1**	**P34C1**	**P33C1**	**P32C1**	**P31C1**	**P30C1**
Setting value	-	-	1	0	0	0	0	0

Register name	P3CON0 register (Address: 0F21AH)							
Bit	7	6	5	4	3	2	1	0
Bit name	P37C0	P36C0	**P35C0**	**P34C0**	**P33C0**	**P32C0**	**P31C0**	**P30C0**
Setting value	-	-	1	0	0	0	0	0

Register name	P3DIR register (Address: 0F219H)							
Bit	7	6	5	4	3	2	1	0
Bit name	P37DIR	P36DIR	**P35DIR**	**P34DIR**	**P33DIR**	**P32DIR**	**P31DIR**	**P30DIR**
Setting value	-	-	0	1	1	1	1	1

Data of P35D-P30D bits (bit5-0 of P3D register) do not affect to the RC-ADC function, so don't care the data for the function.

Register name	P3D register (Address: 0F218H)							
Bit	7	6	5	4	3	2	1	0
Bit name	P37D	P36D	**P35D**	**P34D**	**P33D**	**P32D**	**P31D**	**P30D**
Setting value	-	-	**	**	**	**	**	**

- : Bit that does not exist

* : Bit not related to the RC-ADC function
** : Don't care

19.4.2   Functioning P47(RT1), P46(RS1), P45(CS1) and P44(IN1) as the RC-ADC(Ch1)

Set P47MD1-P44MD1 bits(bit7-bit4 of P4MOD1 register) to "0" and set P47MD0-P44MD0(bit7-bit4 of P4MOD0 register) to "1", for specifying the RC-ADC as the secondary function of P47, P46, P45 and P44.

Register name	P4MOD1 register (Address: 0F225H)							
Bit	7	6	5	4	3	2	1	0
Bit name	**P47MD1**	**P46MD1**	**P45MD1**	**P44MD1**	P43MD1	P42MD1	P41MD1	P40MD1
Setting value	**0**	**0**	**0**	**0**	*	*	*	*

Register name	P4MOD0 register (Address: 0F224H)							
Bit	7	6	5	4	3	2	1	0
Bit name	**P47MD0**	**P46MD0**	**P45MD0**	**P44MD0**	P43MD0	P42MD0	P41MD0	P40MD0
Setting value	**1**	**1**	**1**	**1**	*	*	*	*

Set the P47C1 to P44C1 bits (P4CON1 register bits 7 to 4) to "0", the P47C0 to P44C0 bits (P4CON0 register bits 7 to 4) to "0", and the P47DIR to P44DIR bits (P4DIR register bits 7 to 4) to "1" for selecting the state mode of the P47, P46, P45, and P44 to high-impedance input. The P47C1-P44C1 bit and P47C0-P44C0 bit can be set to all "1" instead of all "0" to select the high-impedance inputs.

Register name	P4CON1 register (Address: 0F223H)							
Bit	7	6	5	4	3	2	1	0
Bit name	**P47C1**	**P46C1**	**P45C1**	**P44C1**	P43C1	P42C1	P41C1	P40C1
Setting value	**0**	**0**	**0**	**0**	*	*	*	*

Register name	P4CON0 register (Address: 0F222H)							
Bit	7	6	5	4	3	2	1	0
Bit name	**P47C0**	**P46C0**	**P45C0**	**P44C0**	P43C0	P42C0	P41C0	P40C0
Setting value	**0**	**0**	**0**	**0**	*	*	*	*

Register name	P4DIR register (Address: 0F221H)							
Bit	7	6	5	4	3	2	1	0
Bit name	**P47DIR**	**P46DIR**	**P45DIR**	**P44DIR**	P43DIR	P42DIR	P41DIR	P40DIR
Setting value	**1**	**1**	**1**	**1**	*	*	*	*

Data of P47D-P44D bits (bit7-4 of P4D register) do not affect to the RC-ADC function, so don't care the data for the function.

Register name	P4D register (Address: 0F220H)							
Bit	7	6	5	4	3	2	1	0
Bit name	P47D	P46D	P45D	P44D	P43D	P42D	P41D	P40D
Setting value	**	**	**	**	*	*	*	*

* : Bit not related to the RC-ADC function
** : Don't care

Note:
Status of output pins P31-P34 and P45-P47 changes according to the RC oscillation mode specified by OM0-OM3 bit of
RADMOD register.

LCD Drivers

20. LCD Driver

20.1 Overview

This LSI includes LCD drivers that display the contents that are set in the display register.
For the ML610407/8/9, the numbers of commons and segments and the maximum number of dots are as shown in Table 20-1.

Table 20-1   Numbers of Commons/Segments and Maximum Number of Dots for ML610401/2/3

Product name (ML610...)	401	402	403
Number of commons/segments (changeable by software)	2com-14seg	2com-18seg	2com-22seg
	3com-13seg	3com-17seg	3com-21seg
	4com-12seg	4com-16seg	4com-20seg
	5com-11seg	5com-15seg	5com-19seg
Maximum number of dots	55	75	95

The LCD display function consists of four blocks as shown in Figure 20-1:
1. Display registers
2. Display allocation
3. Display control
4. Driver
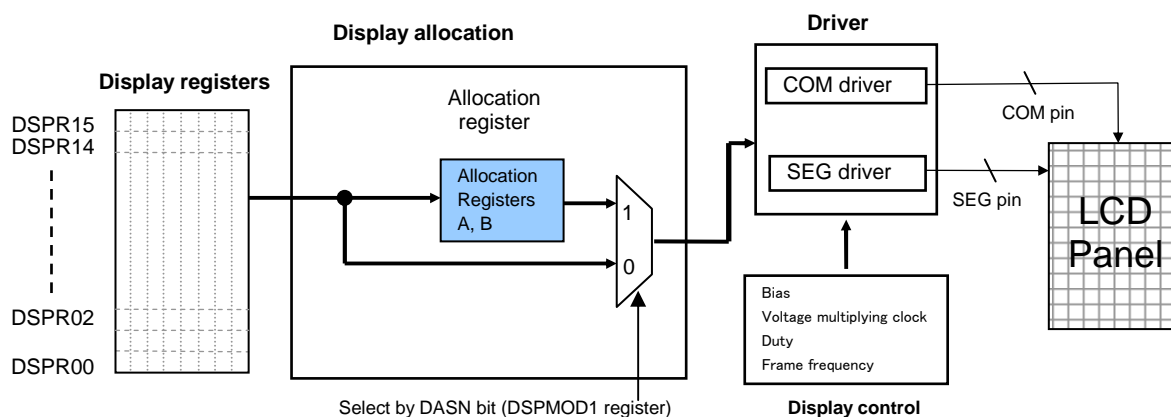
Figure 20-1   Configuration of LCD Display Function

The display registers are used to store the contents to be displayed as bit patterns.
The bit pattern storage method depends on the specification of the LCD panel to be used (display pattern and assignment of the COM pin and SEG pin) and the setting of the display allocation circuit.

The display allocation block controls mapping of the display register for the LCD common/segment.
Using the display allocation registers A and B or not using them is selectable. When using them (Set DASN bit of DSPMOD1 register to "1"), the segment mapping of the display register can be specified in bit units by programming according to the contents of display allocation registers A and B. Therefore, the display register array can be changed in flexible and simplify the software process for display (This function is defined as the programmable display allocation function in the User's Manual). Also, the data specified to the registers A and B can be easily prepared by using LAPIS semiconductor LCD allocation Tool.
When the display allocation registers A and B are not used (set the DSPMOD1 register's DASN bit to "0"), the display content is controlled only with the display registers.

The display control circuit generates LCD drive waveforms according to the characteristics of the LCD.
A bias, a bias voltage multiplying clock, a duty, and a frame frequency suitable for the LCD panel can be selected.

A) When not using Programmable display allocation function (DASN bit of DSPMOD1 register is "0")
Suitable for the dot matrix type LCD panel whose common/segment array is approximated to the bit array of the display register.
Figure 20-2 shows an example of the correlation between the display registers and the dot matrix type LCD image.
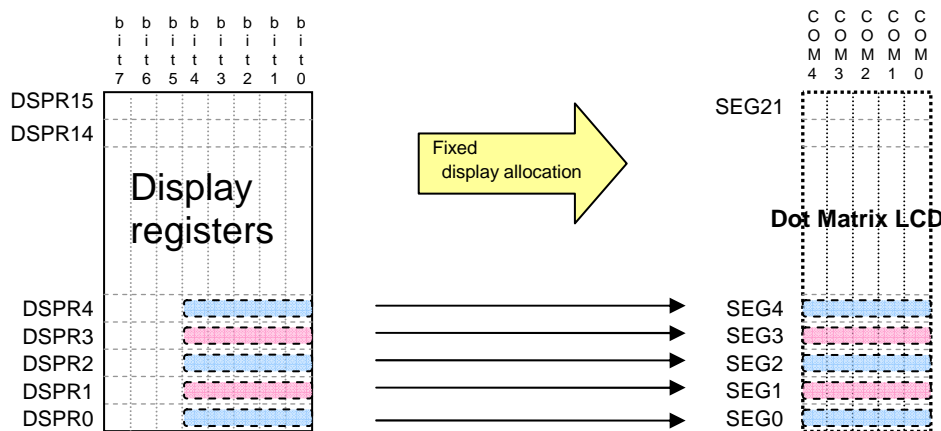
Figure 20-2   Example of Correlation between Display Registers and Dot Matrix Type LCD Image

B) When using Programmable display allocation function (DASN bit of DSPMOD1 register is "1")
The programmable display allocation function is suitable for the LCD panel of segment type or character type whose common/segment array is restricted by the design or wiring. The display allocation registers A and B can be used to programmatically specify the display register bit-by-bit. This allows the display registers to be arrayed flexibly and thus makes the display processing in the software easier. The content of the display allocation register A (DSmCn) specifies the addresses of the display registers (DSPR00 to 15) to be output to the common "n" of the segment "m." The content of the display allocation register B (DSmCnB) specifies the bits of the display registers (DSPR00 to 15) to be output to the common "n" of the segment "m."
Figure 20-3 shows an example of the correlation between the display registers and the dot matrix type LCD image when the programmable display allocation is used.

DSPR	bit	Symbol on panel	COM	SEG
…	…	…	…	…
DSPR4	6	4G	1	7
…	…	…	…	..
DSPR0	2	0C	3	0
DSPR0	1	0B	4	0
DSPR0	0	0A	4	1
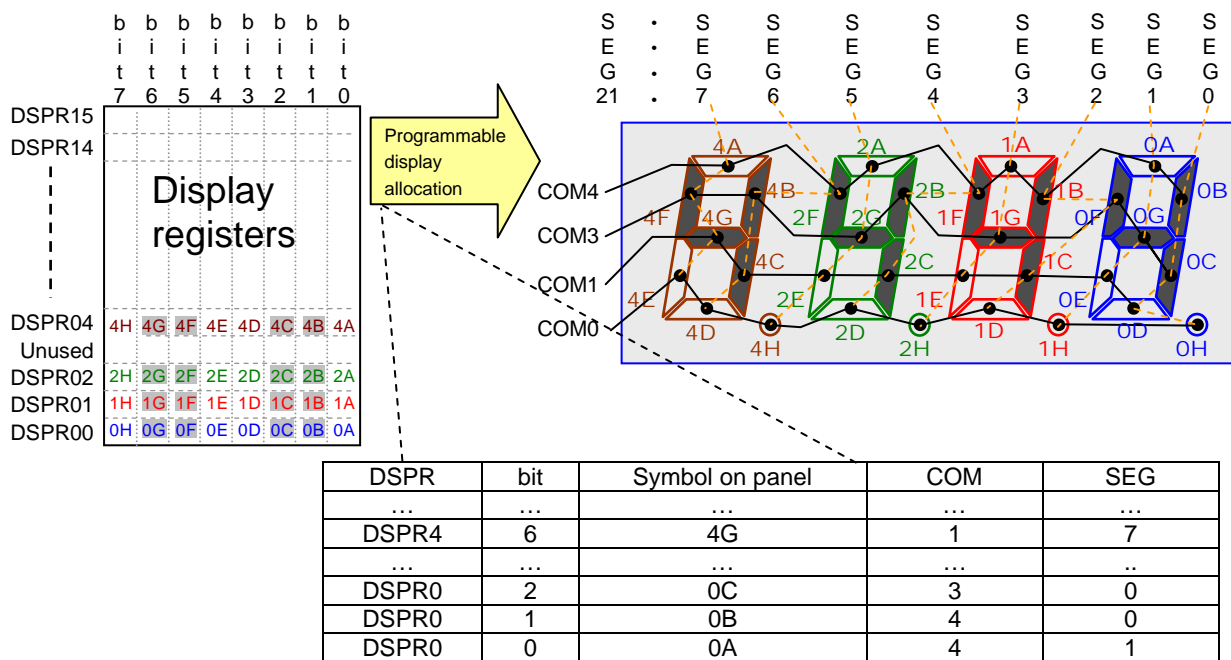
Figure 20-3   An example of correlation between display registers and segment type LCD

20.1.1 Features

The LCD drivers are applicable to various types of LCD panels.

- ML610403: 95 dots max. (19 segments x 5 commons)
- ML610402: 70 dots max. (15 segments x 5 commons)
- ML610401: 55 dots max. (11 segments x 5 commons)
- 1/1 to 1/5 duty
- 1/3 bias (built-in bias generation circuit)
- Frame frequency selectable (4 types)
- Bias voltage multiplying clock selectable (8 types)
- Programmable display allocation function

The programmable display allocation function facilitates software display processing. By using "ALL LCDs on mode" and "ALL LCDs off mode", LCD panel inspection processing software can be easily created.

20.1.2 Configuration of the LCD Drivers

Figure 20-4 shows the configuration of the LCD drivers and the bias generation circuit.

BIASCON   : Bias circuit control register
DSPMOD0   : Display mode register 0
DSPMOD1   : Display mode register 1
DSPCON   : Display control register
DSmCn   : Allocation register (m = 0 to 21, n = 0 to 4)
DSPR00 - DSPR15 : Display registers
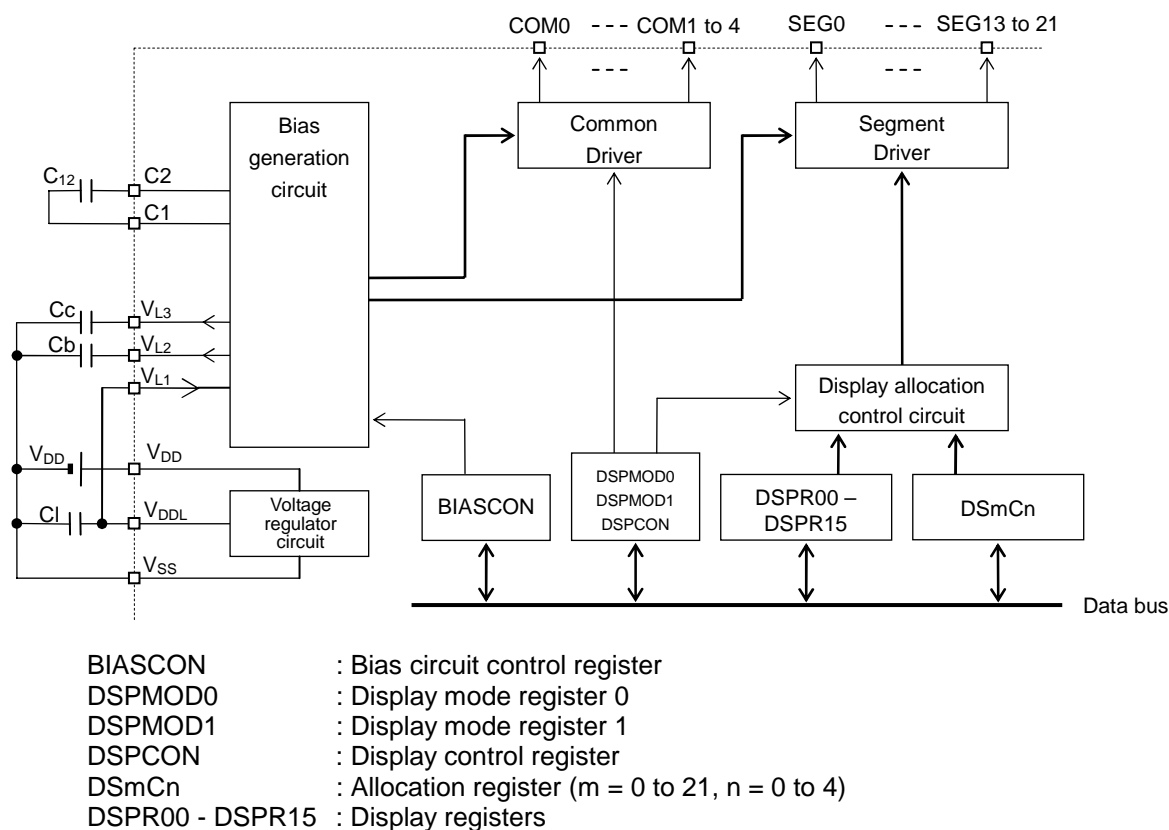
Figure 20-4   Configuration of LCD Drivers and Bias Generation Circuit

20.1.3 Configuration of the Bias Generation Circuit

The bias generation circuit generates LCD drive voltages (V_{L1} to V_{L3}) by multiplying the power supply voltage (V_{DD}) or the voltage (V_{DDL}) generated by the voltage regulator circuit with the capacitor (C_{12}).
When a system reset starts the bias generation circuit operation stops.
Figure 20-5-1 shows the configuration of the bias generation circuit.

VDD = 1.6 to 3.6V, without LCD regulator

VDD = 2.4 to 3.6V, without LCD regulator

VDD = 1.25 to 3.6V, with LCD regulator
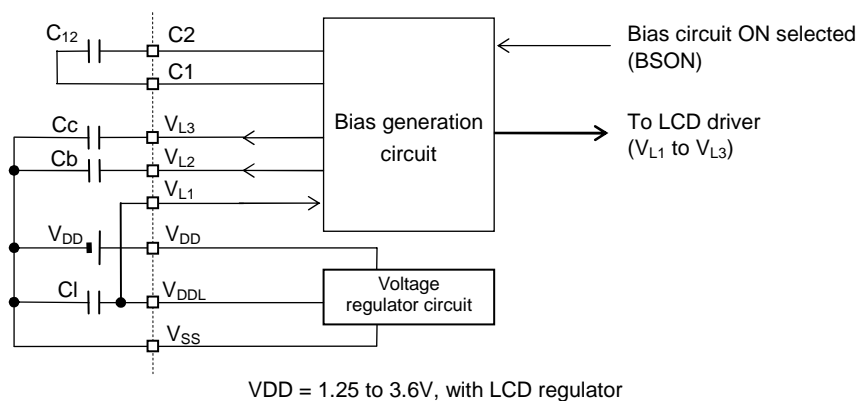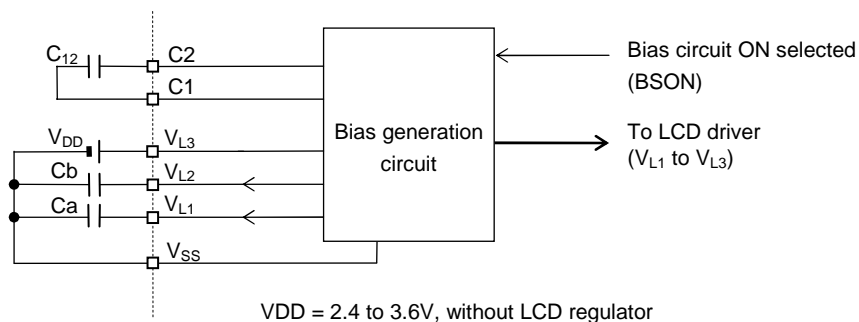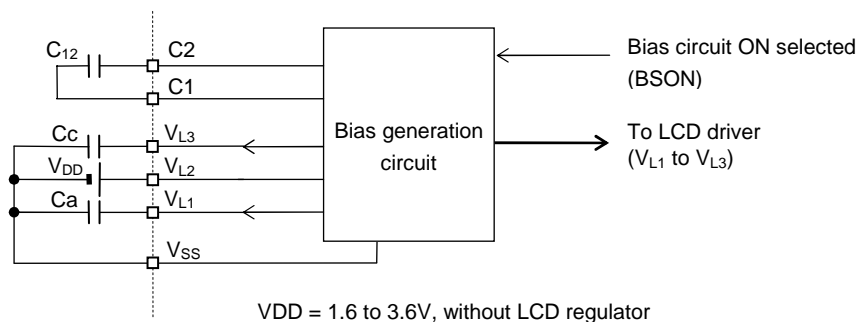
Figure 20-5-1   Configuration of Bias Generation Circuit (1/3 Bias)

20.1.4 List of Pins

Pin name	Input/output	Function	ML610401	ML610402	ML610403
V_{L1}	—	Power supply pin for LCD bias (internally generated)	●	●	●
V_{L2}	—	Power supply pin for LCD bias (internally generated)	●	●	●
V_{L3}	—	Power supply pin for LCD bias (internally generated)	●	●	●
C1	—	Capacitor connection pin for LCD bias generation	●	●	●
C2	—	Capacitor connection pin for LCD bias generation	●	●	●
COM0	O	LCD common pin	●	●	●
COM1	O	LCD common pin	●	●	●
COM2/SEG0	O	LCD common/segment pin	●	●	●
COM3/SEG1	O	LCD common/segment pin	●	●	●
COM4/SEG2	O	LCD common/segment pin	●	●	●
SEG3	O	LCD segment pin	●	●	●
SEG4	O	LCD segment pin	●	●	●
SEG5	O	LCD segment pin	●	●	●
SEG6	O	LCD segment pin	●	●	●
SEG7	O	LCD segment pin	●	●	●
SEG8	O	LCD segment pin	●	●	●
SEG9	O	LCD segment pin	●	●	●
SEG10	O	LCD segment pin	●	●	●
SEG11	O	LCD segment pin	●	●	●
SEG12	O	LCD segment pin	●	●	●
SEG13	O	LCD segment pin	●	●	●
SEG14	O	LCD segment pin		●	●
SEG15	O	LCD segment pin		●	●
SEG16	O	LCD segment pin		●	●
SEG17	O	LCD segment pin		●	●
SEG18	O	LCD segment pin			●
SEG19	O	LCD segment pin			●
SEG20	O	LCD segment pin			●
SEG21	O	LCD segment pin			●

20.2 Description of Registers

20.2.1   List of Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F0F0H	Bias circuit control register	BIASCON	—	R/W	8	38H
0F0F2H	Display mode register 0	DSPMOD0	DSPMOD	R/W	8/16	00H
0F0F3H	Display mode register 1	DSPMOD1		R/W	8	00H
0F0F4H	Display control register	DSPCON	—	R/W	8	00H
0F100H ～0F115H	Display register 00 to Display register 15	DSPR00 ～DSPR15	—	R/W	8	Undefined
0F400H ～0F415H	Display allocation register A	DS0C0A ～DS21C0A	—	R/W	8	Undefined
0F440H ～0F455H		DS0C1A ～DS21C1A	—	R/W	8	Undefined
0F480H ～0F495H		DS0C2A ～DS21C2A	—	R/W	8	Undefined
0F4C0H ～0F4D5H		DS0C3A ～DS21C3A	—	R/W	8	Undefined
0F500H ～0F515H		DS0C4A ～DS21C4A	—	R/W	8	Undefined
0F600H ～0F615H	Display allocation register B	DS0C0B ～DS21C0B	—	R/W	8	Undefined
0F640H ～0F655H		DS0C1B ～DS21C1B	—	R/W	8	Undefined
0F680H ～0F695H		DS0C2B ～DS21C2B	—	R/W	8	Undefined
0F6C0H ～0F6D5H		DS0C3B ～DS21C3B	—	R/W	8	Undefined
0F700H ～0F715H		DS0C4B ～DS21C4B	—	R/W	8	Undefined

20.2.2 Bias Circuit Control Register 0 (BIASCON)

Address: 0F0F0H
Access: R/W
Access size: 8-bit
Initial value: 38H

	7	6	5	4	3	2	1	0
BIASCON	—	—	BSEL1	BSEL0	BSN2	BSN1	BSN0	—
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	1	1	1	0	0	0

BIASCON is a special function register (SFR) to control the bias generation circuit.

[Description of Bits]
- **BSN2 to BSN0** (bit 3 to 1)
  The BSN2 to BSN0 bits are used to select a clock for multiplying the bias voltage in the bias generation circuit.
  LSCLK to 1/128LSCLK can be selected.

BSN2	BSN1	BSN0	Description
0	0	0	1/1 LSCLK (32kHz)
0	0	1	1/2 LSCLK (16kHz)
0	1	0	1/4 LSCLK (8kHz)
0	1	1	1/8 LSCLK (4kHz)
1	0	0	1/16 LSCLK (2 kHz) (initial value)
1	0	1	1/32 LSCLK (1kHz)
1	1	0	1/64 LSCLK (512Hz)
1	1	1	1/128 LSCLK (256Hz)

- **BSEL1-BSEL0** (bit 5, 4)
  The BSEL bit is used to set the bias in the bias generation circuit.
  1/3 bias can be selected.

BSEL1	BSEL0	Description
0	0	1/3 bias
0	1	Setting prohibited
1	0	Setting prohibited
1	1	Setting prohibited (initial value)

20.2.3 Display Mode Register 0 (DSPMOD0)

Address: 0F0F2H
Access: R/W
Access size: 8/16 bit
Initial value: 00H

	7	6	5	4	3	2	1	0
DSPMOD0	—	FRM1	FRM0	—	—	DUTY2	DUTY1	DUTY0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

DSPMOD0 is a special function register (SFR) to control the display mode of the LCD drivers.

[Description of Bits]
- **DUTY2 to DUTY0** (bit 2 to 0)
  The DUTY2 to DUTY0 bits are used to specify the duty in 5 steps (1/1 to 1/5). The numbers of commons/segments are determined according to the duty setting.

Product (ML610...)			Common to all products	401	402	403
DUTY2	**DUTY1**	**DUTY0**	Duty	Number of commons/segments		
0	0	0	1/1 duty (initial value)	2c-14s	2c-18s	2c-22s
0	0	1	1/2 duty	2c-14s	2c-18s	2c-22s
0	1	0	1/3 duty	3c-13s	3c-17s	3c-21s
0	1	1	1/4 duty	4c-12s	4c-16s	4c-20s
1	*	*	1/5 duty	5c-11s	5c-15s	5c-19s

- **FRM1-FRM0** (bit 6, 5)
  The FRM1 to FRM0 bits are used to select a frame frequency of the LCD drivers.
  The reference frequency of a frame frequency (LLSCLK = 32.768 kHz) is selectable from 64 Hz, 73 Hz, 85 Hz, or 102 Hz.

FRM1	FRM0	Description
0	0	Reference frequency: 64 Hz (initial value)
0	1	Reference frequency: 73 Hz
1	0	Reference frequency: 85 Hz
1	1	Reference frequency: 102 Hz

The frame frequency for each duty is listed in Table 20-2.

Table 20-2   Frame Frequency for Each Duty

Duty	Frame frequency [Hz]			
	Reference frequency 64Hz	Reference frequency: 73 Hz	Reference frequency: 85 Hz	Reference frequency: 102 Hz
1/1 duty	64.00	73.14	85.33	102.40
1/2 duty	64.00	73.14	85.33	102.40
1/3 duty	64.25	73.31	85.33	103.04
1/4 duty	64.00	73.14	85.33	102.40
1/5 duty	64.25	73.64	86.23	102.40

20.2.4 Display Mode Register 1 (DSPMOD1)

Address: 0F0F3H
Access: R/W
Access size: 8-bit
Initial value: 00H

	7	6	5	4	3	2	1	0
DSPMOD1	—	—	—	—	—	DASN	—	—
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

DSPMOD1 is a special function register (SFR) to control the display mode of the LCD drivers.
Use DSPMOD1 to select to use or unuse the programmable display allocation function for the display registers.

[Description of Bits]

- **DASN** (bit 2)
  The DASN bit is used to control the operation of the programmable display allocation function.
  See Sections 20.2.7, 20.2.8, and 20.3.3.

DASN	Description
0	Not use Programmable display allocation function (initial value)
1	Use Programmable display allocation function

20.2.5 Display Control Register (DSPCON)

Address: 0F0F4H
Access: R/W
Access size: 8-bit
Initial value: 00H

	7	6	5	4	3	2	1	0
DSPCON	—	—	—	—	—	—	LMD1	LMD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

DSPCON is a special function register (SFR) to control the LCD drivers.

[Description of Bits]

- **LMD1-LMD0** (bit 1, 0)
    The LMD1 and LMD0 bits are used to select an LCD display mode.
    LCD stop mode, all LCDs off mode, LCD display mode, and all LCDs on mode can be selected.
    In LCD stop mode, V_{ss} level is output to all the common drivers and segment drivers. The charge and discharge current to and from the display panel can be stopped.
    In all LCDs off mode, off waveform is output to all the segment drivers irrespective of the contents of the display registers.
    In LCD display mode, the contents of the display registers are output to each segment driver.
    In all LCDs on mode, on waveform is output to all the segment drivers irrespective of the contents of the display registers.

LMD1	LMD0	Description
0	0	LCD stop mode (initial value)
0	1	All LCDs off mode
1	0	LCD display mode
1	1	All LCDs on mode

20.2.6 Display Allocation Register A (DS0C0A to DS21C4A)

Address: 0F400H to 0F415H, 0F440H to 0F455H, 0F480H to 0F495H, 0F4C0H to 0F4D5H, 0F500H to 0F515H
Access: R/W
Access size: 8-bit
Initial value: Undefined

	7	6	5	4	3	2	1	0
DSmCnA	—	—	—	a4	a3	a2	a1	a0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	x	x	x	x	x

DSmCnA (m= 0 to 21, n = 0 to 4) are special function registers (SFRs) that are used for the programmable display allocation function.
Each valid bit of DSmCnA becomes undefined at system reset.
Table 20-3 shows a list of the display allocation register A.

[Description of Bits]
- **a4 to a0** (bit 4 to 0)
  The a4 to a0 bits of DSmCnA (m = 0 to 21, n = 0 to 4) are used to set the low 8 bits of the address of display register (DSPR00 to 15) which is output to common n of segment m.
  Set DSmCnA when the DASN bit of the display mode register 1 (DSPMOD1) is "0". When the DASN bit is "1", access from the CPU is invalid.

Table 20-3　Display Allocation Register A

Segment	Common	Register name	Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
SEG0	COM0	DS0C0A	0F400H	—	—	—	a4	a3	a2	a1	a0	R/W
SEG1	COM0	DS1C0A	0F401H	—	—	—	a4	a3	a2	a1	a0	R/W
SEG2	COM0	DS2C0A	0F402H	—	—	—	a4	a3	a2	a1	a0	R/W
SEG3	COM0	DS3C0A	0F403H	—	—	—	a4	a3	a2	a1	a0	R/W
:	:	:	:	:	:	:	:	:	:	:	:	:
SEG21	COM0	DS21C0A	0F415H	—	—	—	a4	a3	a2	a1	a0	R/W
SEG0	COM1	DS0C1A	0F440H	—	—	—	a4	a3	a2	a1	a0	R/W
:	:	:	:	:	:	:	:	:	:	:	:	:
SEG21	COM1	DS21C1A	0F455H	—	—	—	a4	a3	a2	a1	a0	R/W
SEG0	COM2	DS0C2A	0F480H	—	—	—	a4	a3	a2	a1	a0	R/W
:	:	:	:	:	:	:	:	:	:	:	:	:
SEG21	COM2	DS21C2A	0F495H	—	—	—	a4	a3	a2	a1	a0	R/W
SEG0	COM3	DS0C3A	0F4C0H	—	—	—	a4	a3	a2	a1	a0	R/W
:	:	:	:	:	:	:	:	:	:	:	:	:
SEG21	COM3	DS21C3A	0F4D5H	—	—	—	a4	a3	a2	a1	a0	R/W
SEG0	COM4	DS0C4A	0F500H	—	—	—	a4	a3	a2	a1	a0	R/W
:	:	:	:	:	:	:	:	:	:	:	:	:
SEG21	COM4	DS21C4A	0F515H	—	—	—	a4	a3	a2	a1	a0	R/W

20.2.7 Display Allocation Register B (DS0C0B to DS21C4B)

Address: 0F600H to 0F615H, 0F640H to 0F655H, 0F680H to 0F695H, 0F6C0H to 0F6D5H, 0F700H to 0F715H
Access: R/W
Access size: 8-bit
Initial value: Undefined

	7	6	5	4	3	2	1	0
DSmCnB	—	—	—	—	—	b2	b1	b0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	x	x	x

DSmCnB (m= 0 to 21, n = 0 to 4) are special function registers (SFRs) to store segment allocation data.
Each valid bit of DSmCnB becomes undefined at system reset.
Table 20-4 shows a list of the display allocation register B.

[Description of Bits]
- **b2 to b0** (bit 2 to 0)
  The b2 to b0 bits of DSmCnB (m = 0 to 21, n = 0 to 4) are used to set the bits of the display registers (DSPR00 to 15) that are output to common n of segment m.
  Set DSmCnB when the DASN bit of the display control register 0 (DSPCON0) is "0".
  When the DASN bit is "1", access from the CPU is invalid.

b2	b1	b0	Description
0	0	0	Selects bit 0
0	0	1	Selects bit 1
0	1	0	Selects bit 2
0	1	1	Selects bit 3
1	0	0	Selects bit 4
1	0	1	Selects bit 5
1	1	0	Selects bit 6
1	1	1	Selects bit 7

Table 20-4 Display Allocation Register B

Segment	Common	Register name	Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
SEG0	COM0	DS0C0B	0F600H	—	—	—	—	—	b2	b1	b0	R/W
SEG1	COM0	DS1C0B	0F601H	—	—	—	—	—	b2	b1	b0	R/W
SEG2	COM0	DS2C0B	0F602H	—	—	—	—	—	b2	b1	b0	R/W
SEG3	COM0	DS3C0B	0F603H	—	—	—	—	—	b2	b1	b0	R/W
:	:	:	:	:	:	:	:	:	:	:	:	:
SEG21	COM0	DS21C0B	0F615H	—	—	—	—	—	b2	b1	b0	R/W
SEG0	COM1	DS0C1B	0F640H	—	—	—	—	—	b2	b1	b0	R/W
:	:	:	:	:	:	:	:	:	:	:	:	:
SEG21	COM1	DS21C1B	0F655H	—	—	—	—	—	b2	b1	b0	R/W
SEG0	COM2	DS0C2B	0F680H	—	—	—	—	—	b2	b1	b0	R/W
:	:	:	:	:	:	:	:	:	:	:	:	:
SEG21	COM2	DS21C2B	0F695H	—	—	—	—	—	b2	b1	b0	R/W
SEG0	COM3	DS0C3B	0F6C0H	—	—	—	—	—	b2	b1	b0	R/W
:	:	:	:	:	:	:	:	:	:	:	:	:
SEG21	COM3	DS21C3B	0F6D5H	—	—	—	—	—	b2	b1	b0	R/W
SEG0	COM4	DS0C4B	0F700H	—	—	—	—	—	b2	b1	b0	R/W
:	:	:	:	:	:	:	:	:	:	:	:	:
SEG21	COM4	DS21C4B	0F715H	—	—	—	—	—	b2	b1	b0	R/W

20.2.8 Display Registers (DSPR00 to DSPR15)

Address: 0F100H to 0F115H
Access: R/W
Access size: 8-bit
Initial value: Undefined

	7	6	5	4	3	2	1	0
DSPRxx	c7	c6	c5	c4	c3	c2	c1	c0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	x	x	x	x	x	x	x	x

DSPRxx (xx = 00 to 15) are special function registers (SFRs) to store display data.
Each valid bit of DSPRxx becomes undefined at system reset.
The display registers that are not used for LCD display can be used for data memories.
Set data in DSPRxx before setting LCD display mode.
The c4 to c0 values are used when the programmable display allocation function is not used.

[Description of Bits]
- **c7 to c0** (bit 7 to 0)
  The c7 to c0 bits are used to set display data.

c7~c0	Description
0	off waveform
1	on waveform

Table 20-5 List of Display Registers

Register name	Address	Corresponding segment	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
DSPR00	0F100H	SEG0	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR01	0F101H	SEG1	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR02	0F102H	SEG2	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR03	0F103H	SEG3	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR04	0F104H	SEG4	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR05	0F105H	SEG5	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR06	0F106H	SEG6	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR07	0F107H	SEG7	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR08	0F108H	SEG8	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR09	0F109H	SEG9	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR0A	0F10AH	SEG10	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR0B	0F10BH	SEG11	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR0C	0F10CH	SEG12	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR0D	0F10DH	SEG13	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR0E	0F10EH	SEG14	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR0F	0F10FH	SEG15	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR10	0F110H	SEG16	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR11	0F111H	SEG17	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR12	0F112H	SEG18	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR13	0F113H	SEG19	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR14	0F114H	SEG20	c7	c6	c5	c4	c3	c2	c1	c0	R/W
DSPR15	0F115H	SEG21	c7	c6	c5	c4	c3	c2	c1	c0	R/W
Unused	0F116H to 0F13FH	-	-	-	-	-	-	-	-	-	-

20.3 Description of Operation

20.3.1   Operation of LCD Drivers and Bias Generation Circuit

Figure 20-6 shows the operation of the LCD drivers and the bias generation circuit.
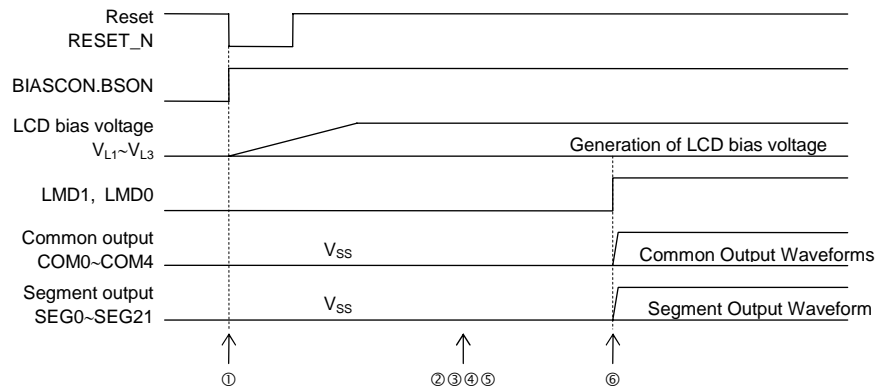
Figure 20-6   Operation of LCD Drivers and Bias Generation Circuit

① System reset causes the bias generation circuit and the LCD drivers to stop operation and V_{SS} level to be output to each of the common and segment pins.

② By using the bias circuit control register (BIASCON), select 1/3 bias and select the bias voltage multiplying clock.

③ When the programmable display allocation function is used, set LCD allocation data in the display allocation registers (DS0C0 to DS21C4).

④ Set a frame frequency and a duty by using the display mode register 0 (DSPMOD0). When using the programmable display allocation function, set the DSPMOD1 register's DASN bit to"1". When not using the programmable display allocation function, set the DSPMOD1 register's DASN bit to"0".

⑤ Set display data in the display registers (DSPR00 to DSPR15).

⑥ On the display control register (DSPCON), set the LMD1 and LMD0 bits to the display mode. (Display waveform is output to each segment pin.)

20.3.2 Segment Mapping When the Programmable Display Allocation Function is Not Used

The following shows the segment map of the display registers (DSPR00 to 15) when the programmable display allocation function is not used (DSPMOD1 register's DASN bit = "0"):

SEG21	SEG20	-----	SEG1	SEG0	
DSPR15[4]	DSPR14[4]		DSPR01[4]	DSPR00[4]	← COM4
DSPR15[3]	DSPR14[3]	-----	DSPR01[3]	DSPR00[3]	← COM3
DSPR15[2]	DSPR14[2]	-----	DSPR01[2]	DSPR00[2]	← COM2
DSPR15[1]	DSPR14[1]	-----	DSPR01[1]	DSPR00[1]	← COM1
DSPR15[0]	DSPR14[0]	-----	DSPR01[0]	DSPR00[0]	← COM0

For ML610403

SEG17	SEG16	-----	SEG1	SEG0	
DSPR11[4]	DSPR10[4]		DSPR01[4]	DSPR00[4]	← COM4
DSPR11[3]	DSPR10[3]	-----	DSPR01[3]	DSPR00[3]	← COM3
DSPR11[2]	DSPR10[2]	-----	DSPR01[2]	DSPR00[2]	← COM2
DSPR11[1]	DSPR10[1]	-----	DSPR01[1]	DSPR00[1]	← COM1
DSPR11[0]	DSPR10[0]	-----	DSPR01[0]	DSPR00[0]	← COM0

For ML610402

SEG13	SEG12	-----	SEG1	SEG0	
DSPR0D[4]	DSPR0C[4]		DSPR01[4]	DSPR00[4]	← COM4
DSPR0D[3]	DSPR0C[3]	-----	DSPR01[3]	DSPR00[3]	← COM3
DSPR0D2]	DSPR0C[2]	-----	DSPR01[2]	DSPR00[2]	← COM2
DSPR0D[1]	DSPR0C[1]	-----	DSPR01[1]	DSPR00[1]	← COM1
DSPR0D[0]	DSPR0C[0]	-----	DSPR01[0]	DSPR00[0]	← COM0

For ML610401

Figure 20-7   Segment Map Configuration Diagram

20.3.3 Segment Mapping When the Programmable Display Allocation Function is Used

When the programmable display allocation function is used (DASN bit of DSPMOD1 register is "1"), the segment map of the display registers (DSPR00 to 15) can be programmatically changed using the display allocation registers (DSmCn: m = 0 to 21, n = 0 to 4).
Figure 20-8 shows the configuration when using the programmable display allocation function.
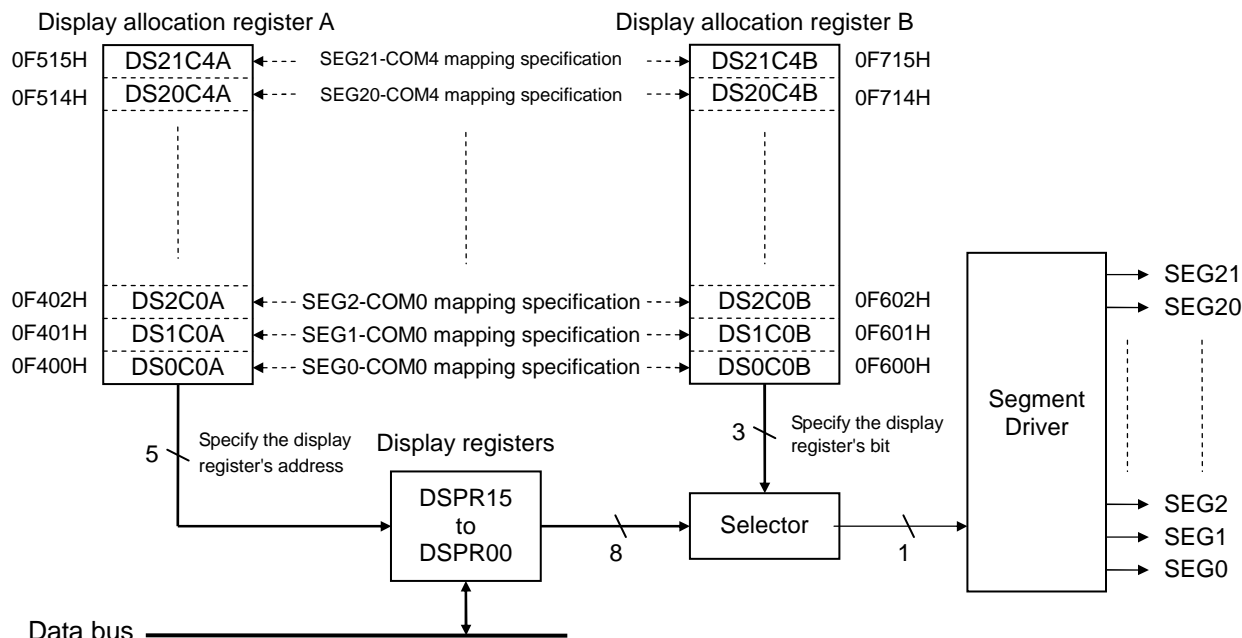
Figure 20-8   Configuration When Using the Programmable Display Allocation Function

In the display allocation register A (DSmCnA: m = 0 to 21, n = 0 to 4), set the address (00H to 15H) of the display register (DSPR00 to DSPR15) that is output to the common n of the segment n. In display allocation register B (DSmCnB: m = 0 to 21, n = 0 to 4), set the bits of the display register (DSPR00 to DSPR15) that is output to the common n of the segment m.
For instance, to display bit 6 of display register 13 (DSPR13) to the common 3 of the segment 6, set as follows.
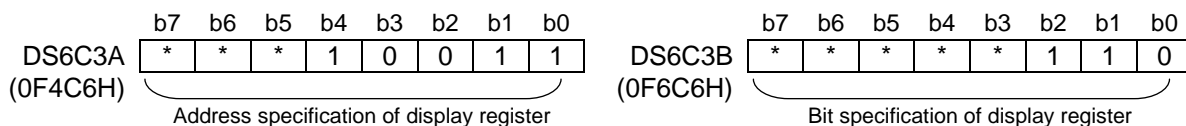
"*" indicates an arbitrary value.

[Note]
- Set display allocation data to display allocation registers when the DASN bit of display mode register 1 (DSPMOD1) is "0". When the DASN bit is "1", access from the CPU is invalid.

20.3.4   Common Output Waveforms

Figure 20-9 shows the common output waveform at 1/5 duty (5 commons) and 1/3 bias.
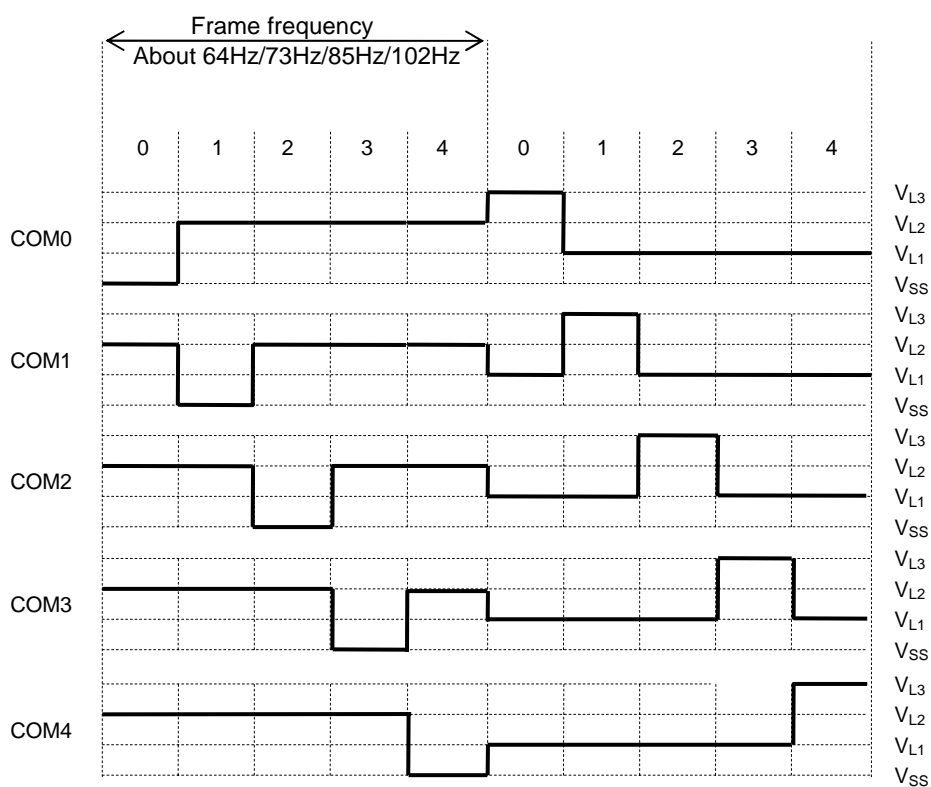
Figure 20-9   Common Output Waveform at 1/5 Duty (5 Commons) and 1/3 Bias

20.3.5 Segment Output Waveform

Figure 20-10 shows the segment output waveform at 1/5 duty (5 commons) and 1/3 bias.
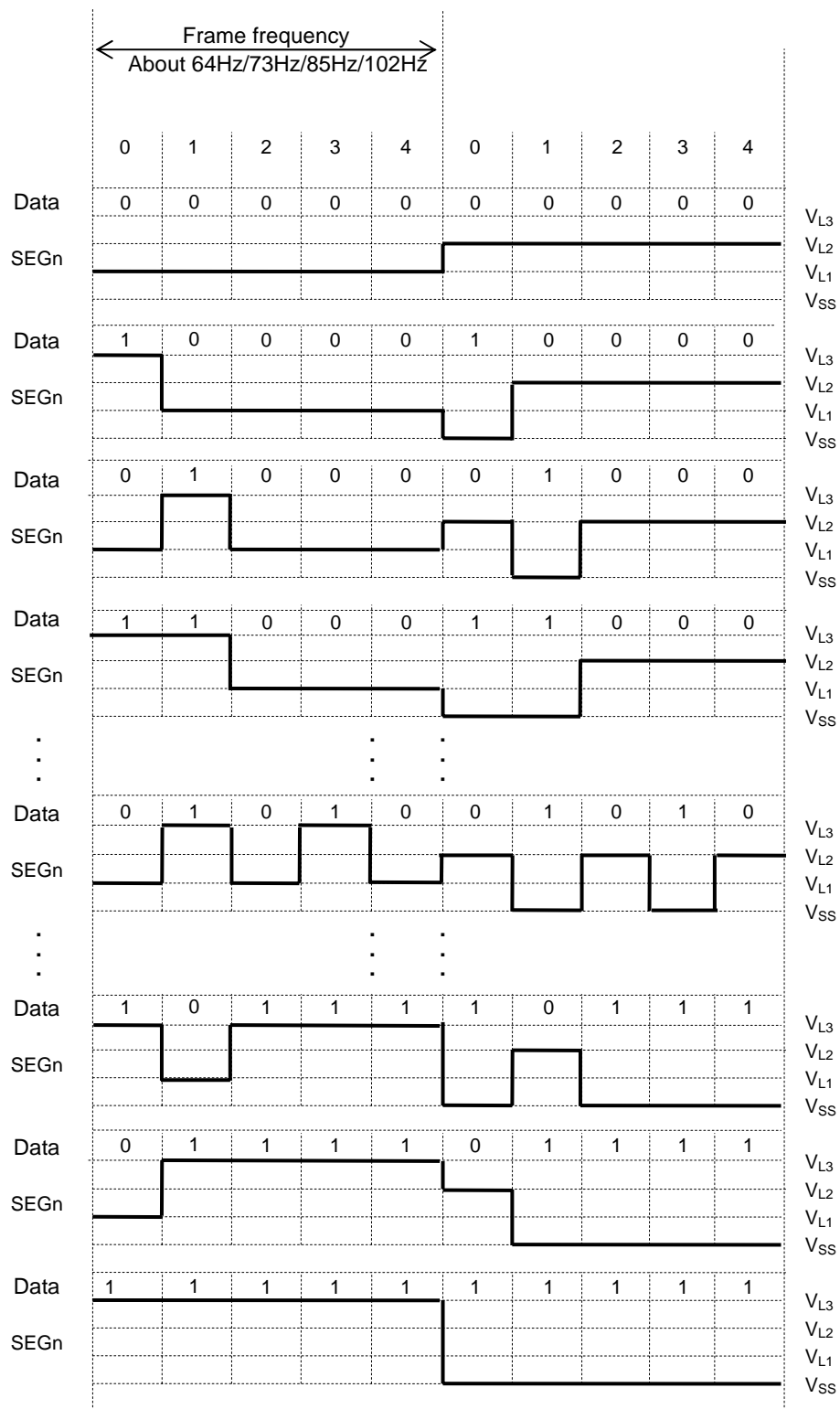
Figure 20-10   Segment Output Waveform at 1/5 Duty (5 Commons) and 1/3 Bias

Power Supply Circuit

21. Power Supply Circuit

21.1 Overview

This LSI includes a voltage regulator circuit for internal logic (VRL).
The VRL outputs the operating voltage, V_{DDL}, of the internal logic circuit, program memory, RAM, low-speed oscillation, etc.
For the circuit configuration of the power supplies for LCD (V_{L1} to V_{L3}), see Chapter 20, "LCD Driver".

21.1.1 Features

- The VRL outputs the operating voltage, V_{DDL}, of the internal logic circuit, program memory, RAM, low-speed oscillation, etc.

21.1.2 Configuration

Figure 21-1 shows the configuration of the power supply circuit.
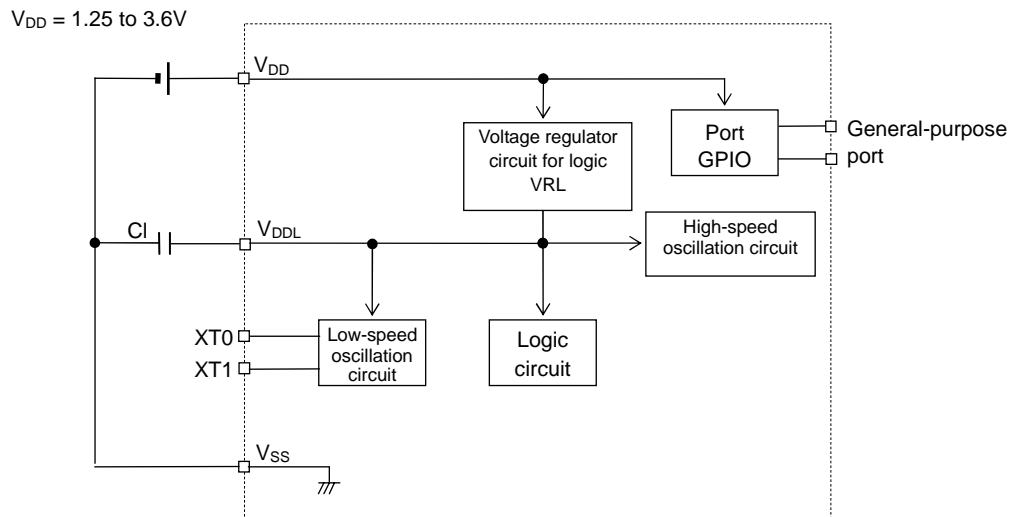
Figure 21-1 Configuration of Power Supply Circuit

21.1.3 List of Pins

Pin name	I/O	Function
V_{DDL}	—	Positive power supply pin for the internal logic circuits The V_{DDL} voltage becomes approximately 1.2 V at a system reset.

Mask Option

22. Mask Option

22.1 Overview

In this LSI, the low-speed oscillation stop detection enable/disable is selected as a mask option.
The low-speed oscillation stop detection enable/disable is decided by the test area data of the program memory space when the LSI is manufactured.
For the Mask-Option, see Chapter 3, "Reset Function".
For the test area data of the program memory space, see Chapter 2, "CPU and Memory Space".
For the Mask ROM version emulation function, see "ML610Q407 user's manual : Chapter 25 Mask ROM Version Emulation Function".

22.1.1 Features

- The low-speed oscillation stop detection enable/disable is selected as a mask option.

Appendixes

Appendix A   Registers

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F000H	Data segment register	DSR	—	R/W	8	00H
0F001H	Reset status register	RSTAT	—	R/W	8	Undefined
0F002H	Frequency control register 0	FCON0	FCON	R/W	8/16	33H
0F003H	Frequency control register 1	FCON1		R/W	8	00H
0F008H	Stop code acceptor	STPACP	—	W	8	Undefined
0F009H	Standby control register	SBYCON	—	W	8	00H
0F00AH	Low-speed time base counter register	LTBR	—	R/W	8	00H
0F00BH	High-speed time base counter frequency divide register	HTBDR	—	R/W	8	00H
0F00CH	Low-speed time base counter frequency adjustment register L	LTBADJL	LTBADJ	R/W	8/16	00H
0F00DH	Low-speed time base counter frequency adjustment register H	LTBADJH		R/W	8	00H
0F00EH	Watchdog timer control register	WDTCON	—	R/W	8	00H
0F00FH	Watchdog timer mode register	WDTMOD	—	R/W	8	02H
0F011H	Interrupt enable register 1	IE1	—	R/W	8	00H
0F012H	Interrupt enable register 2	IE2	—	R/W	8	00H
0F014H	Interrupt enable register 4	IE4	—	R/W	8	00H
0F015H	Interrupt enable register 5	IE5	—	R/W	8	00H
0F016H	Interrupt enable register 6	IE6	—	R/W	8	00H
0F017H	Interrupt enable register 7	IE7	—	R/W	8	00H
0F018H	Interrupt request register 0	IRQ0	—	R/W	8	00H
0F019H	Interrupt request register 1	IRQ1	—	R/W	8	00H
0F01AH	Interrupt request register 2	IRQ2	—	R/W	8	00H
0F01CH	Interrupt request register 4	IRQ4	—	R/W	8	00H
0F01DH	Interrupt request register 5	IRQ5	—	R/W	8	00H
0F01EH	Interrupt request register 6	IRQ6	—	R/W	8	00H
0F01FH	Interrupt request register 7	IRQ7	—	R/W	8	00H
0F020H	External interrupt control register 0	EXICON0	—	R/W	8	00H
0F021H	External interrupt control register 1	EXICON1	—	R/W	8	00H
0F022H	External interrupt control register 2	EXICON2	—	R/W	8	00H
0F028H	Block control register 0	BLKCON0	—	R/W	8	00H
0F029H	Block control register 1	BLKCON1	—	R/W	8	00H
0F02AH	Block control register 2	BLKCON2	—	R/W	8	00H
0F02BH	Block control register 3	BLKCON3	—	R/W	8	00H
0F02CH	Block control register 4	BLKCON4	—	R/W	8	00H
0F038H	Timer 2 data register	TM2D	TM2DC	R/W	8/16	0FFH
0F039H	Timer 2 counter register	TM2C		R/W	8	00H
0F03AH	Timer 2 control register 0	TM2CON0	TM2CON	R/W	8/16	00H
0F03BH	Timer 2 control register 1	TM2CON1		R/W	8	00H
0F03CH	Timer 3 data register	TM3D	TM3DC	R/W	8/16	0FFH
0F03DH	Timer 3 counter register	TM3C		R/W	8	00H
0F03EH	Timer 3 control register 0	TM3CON0	TM3CON	R/W	8/16	00H
0F03FH	Timer 3 control register 1	TM3CON1		R/W	8	00H
0F090H	Capture control register	CAPCON	—	R/W	8	00H

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F091H	Capture status register	CAPSTAT	—	R	8	00H
0F092H	Capture data register 0	CAPR0	—	R/W	8	00H
0F093H	Capture data register 1	CAPR1	—	R/W	8	00H
0F094H	Capture time base data register	CAPTB	—	R	8	Undefined
0F0F0H	Bias circuit control register	BIASCON	—	R/W	8	38H
0F0F2H	Display mode register 0	DSPMOD0	DSPMOD	R/W	8/16	00H
0F0F3H	Display mode register 1	DSPMOD1		R/W	8	00H
0F0F4H	Display control register	DSPCON	—	R/W	8	00H
0F100H	Display register 00	DSPR00	—	R/W	8	Undefined
0F101H	Display register 01	DSPR01	—	R/W	8	Undefined
0F102H	Display register 02	DSPR02	—	R/W	8	Undefined
0F103H	Display register 03	DSPR03	—	R/W	8	Undefined
0F104H	Display register 04	DSPR04	—	R/W	8	Undefined
0F105H	Display register 05	DSPR05	—	R/W	8	Undefined
0F106H	Display register 06	DSPR06	—	R/W	8	Undefined
0F107H	Display register 07	DSPR07	—	R/W	8	Undefined
0F108H	Display register 08	DSPR08	—	R/W	8	Undefined
0F109H	Display register 09	DSPR09	—	R/W	8	Undefined
0F10AH	Display register 0A	DSPR0A	—	R/W	8	Undefined
0F10BH	Display register 0B	DSPR0B	—	R/W	8	Undefined
0F10CH	Display register 0C	DSPR0C	—	R/W	8	Undefined
0F10DH	Display register 0D	DSPR0D	—	R/W	8	Undefined
0F10EH	Display register 0E	DSPR0E	—	R/W	8	Undefined
0F10FH	Display register 0F	DSPR0F	—	R/W	8	Undefined
0F110H	Display register 10	DSPR10	—	R/W	8	Undefined
0F111H	Display register 11	DSPR11	—	R/W	8	Undefined
0F112H	Display register 12	DSPR12	—	R/W	8	Undefined
0F113H	Display register 13	DSPR13	—	R/W	8	Undefined
0F114H	Display register 14	DSPR14	—	R/W	8	Undefined
0F115H	Display register 15	DSPR15	—	R/W	8	Undefined
0F204H	Port 0 data register	P0D	—	R	8	Undefined
0F206H	Port 0 control register 0	P0CON0	P0CON	R/W	8/16	00H
0F207H	Port 0 control register 1	P0CON1		R/W	8	00H
0F210H	Port 2 data register	P2D	—	R/W	8	00H
0F212H	Port 2 control register 0	P2CON0	P2CON	R/W	8/16	00H
0F213H	Port 2 control register 1	P2CON1		R/W	8	00H
0F214H	Port 2 mode register	P2MOD	—	R/W	8	00H
0F218H	Port 3 data register	P3D	—	R/W	8	00H
0F219H	Port 3 direction register	P3DIR	—	R/W	8	00H
0F21AH	Port 3 control register 0	P3CON0	P3CON	R/W	8/16	00H
0F21BH	Port 3 control register 1	P3CON1		R/W	8	00H
0F21CH	Port 3 mode register 0	P3MOD0	—	R/W	8	00H
0F220H	Port 4 data register	P4D	—	R/W	8	00H
0F221H	Port 4 direction register	P4DIR	—	R/W	8	00H
0F222H	Port 4 control register 0	P4CON0	P4CON	R/W	8/16	00H
0F223H	Port 4 control register 1	P4CON1		R/W	8	00H
0F224H	Port 4 mode register 0	P4MOD0	P4MOD	R/W	8/16	00H
0F225H	Port 4 mode register 1	P4MOD1		R/W	8	00H

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F228H	Port 5 data register	P5D	—	R/W	8	FFH
0F229H	Port 5 direction register	P5DIR	—	R/W	8	00H
0F22AH	Port 5 control register 0	P5CON0	P5CON	R/W	8/16	00H
0F22BH	Port 5 control register 1	P5CON1		R/W	8	00H
0F22CH	Port 5 mode register 0	P5MOD0	P5MOD	R/W	8/16	00H
0F22DH	Port 5 mode register 1	P5MOD1		R/W	8	00H
0F22EH	Port 5 interrupt mode register	P5ISEL	—	R/W	8	00H
0F230H	Port 6 data register [*1]	P6D	—	R/W	8	FFH[*2] 0FH[*3]
0F232H	Port 6 control register 0 [*1]	P6CON0	—	R/W	8	00H
0F290H	UART0 transmit/receive buffer	UA0BUF	—	R/W	8	00H
0F291H	UART0 control register	UA0CON	—	R/W	8	00H
0F292H	UART0 mode register 0	UA0MOD0	UA0MOD	R/W	8/16	00H
0F293H	UART0 mode register 1	UA0MOD1		R/W	8	00H
0F294H	UART0 baud rate register L	UA0BRTL	UA0BRT	R/W	8/16	0FFH
0F295H	UART0 baud rate register H	UA0BRTH		R/W	8	0FH
0F296H	UART0 status register	UA0STAT	—	R/W	8	00H
0F2C0H	Melody 0 control register	MD0CON	—	R/W	8	00H
0F2C1H	Melody 0 tempo code register	MD0TMP	—	R/W	8	00H
0F2C2H	Melody 0 scale code register	MD0TON	MD0TL	R/W	8/16	00H
0F2C3H	Melody 0 tone length code register	MD0LEN		R/W	8	00H
0F300H	RC-ADC Counter A register 0	RADCA0	—	R/W	8	00H
0F301H	RC-ADC Counter A register 1	RADCA1	—	R/W	8	00H
0F304H	RC-ADC Counter B register 0	RADCB0	—	R/W	8	00H
0F305H	RC-ADC Counter B register 1	RADCB1	—	R/W	8	00H
0F308H	RC-ADC mode register	RADMOD	—	R/W	8	00H
0F309H	RC-ADC control register	RADCON	—	R/W	8	00H
0F400H	Display allocation register A	DS0C0A	—	R/W	8	Undefined
0F401H	Display allocation register A	DS1C0A	—	R/W	8	Undefined
0F402H	Display allocation register A	DS2C0A	—	R/W	8	Undefined
0F403H	Display allocation register A	DS3C0A	—	R/W	8	Undefined
0F404H	Display allocation register A	DS4C0A	—	R/W	8	Undefined
0F405H	Display allocation register A	DS5C0A	—	R/W	8	Undefined
0F406H	Display allocation register A	DS6C0A	—	R/W	8	Undefined
0F407H	Display allocation register A	DS7C0A	—	R/W	8	Undefined
0F408H	Display allocation register A	DS8C0A	—	R/W	8	Undefined
0F409H	Display allocation register A	DS9C0A	—	R/W	8	Undefined
0F40AH	Display allocation register A	DS10C0A	—	R/W	8	Undefined
0F40BH	Display allocation register A	DS11C0A	—	R/W	8	Undefined
0F40CH	Display allocation register A	DS12C0A	—	R/W	8	Undefined
0F40DH	Display allocation register A	DS13C0A	—	R/W	8	Undefined
0F40EH	Display allocation register A	DS14C0A	—	R/W	8	Undefined
0F40FH	Display allocation register A	DS15C0A	—	R/W	8	Undefined
0F410H	Display allocation register A	DS16C0A	—	R/W	8	Undefined
0F411H	Display allocation register A	DS17C0A	—	R/W	8	Undefined
0F412H	Display allocation register A	DS18C0A	—	R/W	8	Undefined
0F413H	Display allocation register A	DS19C0A	—	R/W	8	Undefined
0F414H	Display allocation register A	DS20C0A	—	R/W	8	Undefined

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F415H	Display allocation register A	DS21C0A	—	R/W	8	Undefined
0F440H	Display allocation register A	DS0C1A	—	R/W	8	Undefined
0F441H	Display allocation register A	DS1C1A	—	R/W	8	Undefined
0F442H	Display allocation register A	DS2C1A	—	R/W	8	Undefined
0F443H	Display allocation register A	DS3C1A	—	R/W	8	Undefined
0F444H	Display allocation register A	DS4C1A	—	R/W	8	Undefined
0F445H	Display allocation register A	DS5C1A	—	R/W	8	Undefined
0F446H	Display allocation register A	DS6C1A	—	R/W	8	Undefined
0F447H	Display allocation register A	DS7C1A	—	R/W	8	Undefined
0F448H	Display allocation register A	DS8C1A	—	R/W	8	Undefined
0F449H	Display allocation register A	DS9C1A	—	R/W	8	Undefined
0F44AH	Display allocation register A	DS10C1A	—	R/W	8	Undefined
0F44BH	Display allocation register A	DS11C1A	—	R/W	8	Undefined
0F44CH	Display allocation register A	DS12C1A	—	R/W	8	Undefined
0F44DH	Display allocation register A	DS13C1A	—	R/W	8	Undefined
0F44EH	Display allocation register A	DS14C1A	—	R/W	8	Undefined
0F44FH	Display allocation register A	DS15C1A	—	R/W	8	Undefined
0F450H	Display allocation register A	DS16C1A	—	R/W	8	Undefined
0F451H	Display allocation register A	DS17C1A	—	R/W	8	Undefined
0F452H	Display allocation register A	DS18C1A	—	R/W	8	Undefined
0F453H	Display allocation register A	DS19C1A	—	R/W	8	Undefined
0F454H	Display allocation register A	DS20C1A	—	R/W	8	Undefined
0F455H	Display allocation register A	DS21C1A	—	R/W	8	Undefined
0F480H	Display allocation register A	DS0C2A	—	R/W	8	Undefined
0F481H	Display allocation register A	DS1C2A	—	R/W	8	Undefined
0F482H	Display allocation register A	DS2C2A	—	R/W	8	Undefined
0F483H	Display allocation register A	DS3C2A	—	R/W	8	Undefined
0F484H	Display allocation register A	DS4C2A	—	R/W	8	Undefined
0F485H	Display allocation register A	DS5C2A	—	R/W	8	Undefined
0F486H	Display allocation register A	DS6C2A	—	R/W	8	Undefined
0F487H	Display allocation register A	DS7C2A	—	R/W	8	Undefined
0F488H	Display allocation register A	DS8C2A	—	R/W	8	Undefined
0F489H	Display allocation register A	DS9C2A	—	R/W	8	Undefined
0F48AH	Display allocation register A	DS10C2A	—	R/W	8	Undefined
0F48BH	Display allocation register A	DS11C2A	—	R/W	8	Undefined
0F48CH	Display allocation register A	DS12C2A	—	R/W	8	Undefined
0F48DH	Display allocation register A	DS13C2A	—	R/W	8	Undefined
0F48EH	Display allocation register A	DS14C2A	—	R/W	8	Undefined
0F48FH	Display allocation register A	DS15C2A	—	R/W	8	Undefined
0F490H	Display allocation register A	DS16C2A	—	R/W	8	Undefined
0F491H	Display allocation register A	DS17C2A	—	R/W	8	Undefined
0F492H	Display allocation register A	DS18C2A	—	R/W	8	Undefined
0F493H	Display allocation register A	DS19C2A	—	R/W	8	Undefined
0F494H	Display allocation register A	DS20C2A	—	R/W	8	Undefined
0F495H	Display allocation register A	DS21C2A	—	R/W	8	Undefined
0F4C0H	Display allocation register A	DS0C3A	—	R/W	8	Undefined
0F4C1H	Display allocation register A	DS1C3A	—	R/W	8	Undefined
0F4C2H	Display allocation register A	DS2C3A	—	R/W	8	Undefined

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F4C3H	Display allocation register A	DS3C3A	—	R/W	8	Undefined
0F4C4H	Display allocation register A	DS4C3A	—	R/W	8	Undefined
0F4C5H	Display allocation register A	DS5C3A	—	R/W	8	Undefined
0F4C6H	Display allocation register A	DS6C3A	—	R/W	8	Undefined
0F4C7H	Display allocation register A	DS7C3A	—	R/W	8	Undefined
0F4C8H	Display allocation register A	DS8C3A	—	R/W	8	Undefined
0F4C9H	Display allocation register A	DS9C3A	—	R/W	8	Undefined
0F4CAH	Display allocation register A	DS10C3A	—	R/W	8	Undefined
0F4CBH	Display allocation register A	DS11C3A	—	R/W	8	Undefined
0F4CCH	Display allocation register A	DS12C3A	—	R/W	8	Undefined
0F4CDH	Display allocation register A	DS13C3A	—	R/W	8	Undefined
0F4CEH	Display allocation register A	DS14C3A	—	R/W	8	Undefined
0F4CFH	Display allocation register A	DS15C3A	—	R/W	8	Undefined
0F4D0H	Display allocation register A	DS16C3A	—	R/W	8	Undefined
0F4D1H	Display allocation register A	DS17C3A	—	R/W	8	Undefined
0F4D2H	Display allocation register A	DS18C3A	—	R/W	8	Undefined
0F4D3H	Display allocation register A	DS19C3A	—	R/W	8	Undefined
0F4D4H	Display allocation register A	DS20C3A	—	R/W	8	Undefined
0F4D5H	Display allocation register A	DS21C3A	—	R/W	8	Undefined
0F500H	Display allocation register A	DS0C4A	—	R/W	8	Undefined
0F501H	Display allocation register A	DS1C4A	—	R/W	8	Undefined
0F502H	Display allocation register A	DS2C4A	—	R/W	8	Undefined
0F503H	Display allocation register A	DS3C4A	—	R/W	8	Undefined
0F504H	Display allocation register A	DS4C4A	—	R/W	8	Undefined
0F505H	Display allocation register A	DS5C4A	—	R/W	8	Undefined
0F506H	Display allocation register A	DS6C4A	—	R/W	8	Undefined
0F507H	Display allocation register A	DS7C4A	—	R/W	8	Undefined
0F508H	Display allocation register A	DS8C4A	—	R/W	8	Undefined
0F509H	Display allocation register A	DS9C4A	—	R/W	8	Undefined
0F50AH	Display allocation register A	DS10C4A	—	R/W	8	Undefined
0F50BH	Display allocation register A	DS11C4A	—	R/W	8	Undefined
0F50CH	Display allocation register A	DS12C4A	—	R/W	8	Undefined
0F50DH	Display allocation register A	DS13C4A	—	R/W	8	Undefined
0F50EH	Display allocation register A	DS14C4A	—	R/W	8	Undefined
0F50FH	Display allocation register A	DS15C4A	—	R/W	8	Undefined
0F510H	Display allocation register A	DS16C4A	—	R/W	8	Undefined
0F511H	Display allocation register A	DS17C4A	—	R/W	8	Undefined
0F512H	Display allocation register A	DS18C4A	—	R/W	8	Undefined
0F513H	Display allocation register A	DS19C4A	—	R/W	8	Undefined
0F514H	Display allocation register A	DS20C4A	—	R/W	8	Undefined
0F515H	Display allocation register A	DS21C4A	—	R/W	8	Undefined
0F600H	Display allocation register B	DS0C0B	—	R/W	8	Undefined
0F601H	Display allocation register B	DS1C0B	—	R/W	8	Undefined
0F602H	Display allocation register B	DS2C0B	—	R/W	8	Undefined
0F603H	Display allocation register B	DS3C0B	—	R/W	8	Undefined
0F604H	Display allocation register B	DS4C0B	—	R/W	8	Undefined
0F605H	Display allocation register B	DS5C0B	—	R/W	8	Undefined
0F606H	Display allocation register B	DS6C0B	—	R/W	8	Undefined

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F607H	Display allocation register B	DS7C0B	—	R/W	8	Undefined
0F608H	Display allocation register B	DS8C0B	—	R/W	8	Undefined
0F609H	Display allocation register B	DS9C0B	—	R/W	8	Undefined
0F60AH	Display allocation register B	DS10C0B	—	R/W	8	Undefined
0F60BH	Display allocation register B	DS11C0B	—	R/W	8	Undefined
0F60CH	Display allocation register B	DS12C0B	—	R/W	8	Undefined
0F60DH	Display allocation register B	DS13C0B	—	R/W	8	Undefined
0F60EH	Display allocation register B	DS14C0B	—	R/W	8	Undefined
0F60FH	Display allocation register B	DS15C0B	—	R/W	8	Undefined
0F610H	Display allocation register B	DS16C0B	—	R/W	8	Undefined
0F611H	Display allocation register B	DS17C0B	—	R/W	8	Undefined
0F612H	Display allocation register B	DS18C0B	—	R/W	8	Undefined
0F613H	Display allocation register B	DS19C0B	—	R/W	8	Undefined
0F614H	Display allocation register B	DS20C0B	—	R/W	8	Undefined
0F615H	Display allocation register B	DS21C0B	—	R/W	8	Undefined
0F640H	Display allocation register B	DS0C1B	—	R/W	8	Undefined
0F641H	Display allocation register B	DS1C1B	—	R/W	8	Undefined
0F642H	Display allocation register B	DS2C1B	—	R/W	8	Undefined
0F643H	Display allocation register B	DS3C1B	—	R/W	8	Undefined
0F644H	Display allocation register B	DS4C1B	—	R/W	8	Undefined
0F645H	Display allocation register B	DS5C1B	—	R/W	8	Undefined
0F646H	Display allocation register B	DS6C1B	—	R/W	8	Undefined
0F647H	Display allocation register B	DS7C1B	—	R/W	8	Undefined
0F648H	Display allocation register B	DS8C1B	—	R/W	8	Undefined
0F649H	Display allocation register B	DS9C1B	—	R/W	8	Undefined
0F64AH	Display allocation register B	DS10C1B	—	R/W	8	Undefined
0F64BH	Display allocation register B	DS11C1B	—	R/W	8	Undefined
0F64CH	Display allocation register B	DS12C1B	—	R/W	8	Undefined
0F64DH	Display allocation register B	DS13C1B	—	R/W	8	Undefined
0F64EH	Display allocation register B	DS14C1B	—	R/W	8	Undefined
0F64FH	Display allocation register B	DS15C1B	—	R/W	8	Undefined
0F650H	Display allocation register B	DS16C1B	—	R/W	8	Undefined
0F651H	Display allocation register B	DS17C1B	—	R/W	8	Undefined
0F652H	Display allocation register B	DS18C1B	—	R/W	8	Undefined
0F653H	Display allocation register B	DS19C1B	—	R/W	8	Undefined
0F654H	Display allocation register B	DS20C1B	—	R/W	8	Undefined
0F655H	Display allocation register B	DS21C1B	—	R/W	8	Undefined
0F680H	Display allocation register B	DS0C2B	—	R/W	8	Undefined
0F681H	Display allocation register B	DS1C2B	—	R/W	8	Undefined
0F682H	Display allocation register B	DS2C2B	—	R/W	8	Undefined
0F683H	Display allocation register B	DS3C2B	—	R/W	8	Undefined
0F684H	Display allocation register B	DS4C2B	—	R/W	8	Undefined
0F685H	Display allocation register B	DS5C2B	—	R/W	8	Undefined
0F686H	Display allocation register B	DS6C2B	—	R/W	8	Undefined
0F687H	Display allocation register B	DS7C2B	—	R/W	8	Redefined
0F688H	Display allocation register B	DS8C2B	—	R/W	8	Undefined
0F689H	Display allocation register B	DS9C2B	—	R/W	8	Undefined
0F68AH	Display allocation register B	DS10C2B	—	R/W	8	Undefined

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F68BH	Display allocation register B	DS11C2B	—	R/W	8	Undefined
0F68CH	Display allocation register B	DS12C2B	—	R/W	8	Undefined
0F68DH	Display allocation register B	DS13C2B	—	R/W	8	Undefined
0F68EH	Display allocation register B	DS14C2B	—	R/W	8	Undefined
0F68FH	Display allocation register B	DS15C2B	—	R/W	8	Undefined
0F690H	Display allocation register B	DS16C2B	—	R/W	8	Undefined
0F691H	Display allocation register B	DS17C2B	—	R/W	8	Undefined
0F692H	Display allocation register B	DS18C2B	—	R/W	8	Undefined
0F693H	Display allocation register B	DS19C2B	—	R/W	8	Undefined
0F694H	Display allocation register B	DS20C2B	—	R/W	8	Undefined
0F695H	Display allocation register B	DS21C2B	—	R/W	8	Undefined
0F6C0H	Display allocation register B	DS0C3B	—	R/W	8	Undefined
0F6C1H	Display allocation register B	DS1C3B	—	R/W	8	Undefined
0F6C2H	Display allocation register B	DS2C3B	—	R/W	8	Undefined
0F6C3H	Display allocation register B	DS3C3B	—	R/W	8	Undefined
0F6C4H	Display allocation register B	DS4C3B	—	R/W	8	Undefined
0F6C5H	Display allocation register B	DS5C3B	—	R/W	8	Undefined
0F6C6H	Display allocation register B	DS6C3B	—	R/W	8	Undefined
0F6C7H	Display allocation register B	DS7C3B	—	R/W	8	Undefined
0F6C8H	Display allocation register B	DS8C3B	—	R/W	8	Undefined
0F6C9H	Display allocation register B	DS9C3B	—	R/W	8	Undefined
0F6CAH	Display allocation register B	DS10C3B	—	R/W	8	Undefined
0F6CBH	Display allocation register B	DS11C3B	—	R/W	8	Undefined
0F6CCH	Display allocation register B	DS12C3B	—	R/W	8	Undefined
0F6CDH	Display allocation register B	DS13C3B	—	R/W	8	Undefined
0F6CEH	Display allocation register B	DS14C3B	—	R/W	8	Undefined
0F6CFH	Display allocation register B	DS15C3B	—	R/W	8	Undefined
0F6D0H	Display allocation register B	DS16C3B	—	R/W	8	Undefined
0F6D1H	Display allocation register B	DS17C3B	—	R/W	8	Undefined
0F6D2H	Display allocation register B	DS18C3B	—	R/W	8	Undefined
0F6D3H	Display allocation register B	DS19C3B	—	R/W	8	Undefined
0F6D4H	Display allocation register B	DS20C3B	—	R/W	8	Undefined
0F6D5H	Display allocation register B	DS21C3B	—	R/W	8	Undefined
0F700H	Display allocation register B	DS0C4B	—	R/W	8	Undefined
0F701H	Display allocation register B	DS1C4B	—	R/W	8	Undefined
0F702H	Display allocation register B	DS2C4B	—	R/W	8	Undefined
0F703H	Display allocation register B	DS3C4B	—	R/W	8	Undefined
0F704H	Display allocation register B	DS4C4B	—	R/W	8	Undefined
0F705H	Display allocation register B	DS5C4B	—	R/W	8	Undefined
0F706H	Display allocation register B	DS6C4B	—	R/W	8	Undefined
0F707H	Display allocation register B	DS7C4B	—	R/W	8	Undefined
0F708H	Display allocation register B	DS8C4B	—	R/W	8	Undefined
0F709H	Display allocation register B	DS9C4B	—	R/W	8	Undefined
0F70AH	Display allocation register B	DS10C4B	—	R/W	8	Undefined
0F70BH	Display allocation register B	DS11C4B	—	R/W	8	Redefined
0F70CH	Display allocation register B	DS12C4B	—	R/W	8	Undefined
0F70DH	Display allocation register B	DS13C4B	—	R/W	8	Unfefined
0F70EH	Display allocation register B	DS14C4B	—	R/W	8	Undefined

Address	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value
0F70FH	Display allocation register B	DS15C4B	—	R/W	8	Undefined
0F710H	Display allocation register B	DS16C4B	—	R/W	8	Undefined
0F711H	Display allocation register B	DS17C4B	—	R/W	8	Undefined
0F712H	Display allocation register B	DS18C4B	—	R/W	8	Undefined
0F713H	Display allocation register B	DS19C4B	—	R/W	8	Undefined
0F714H	Display allocation register B	DS20C4B	—	R/W	8	Undefined
0F715H	Display allocation register B	DS21C4B	—	R/W	8	Undefined

[*1] ML610401 and ML610402 have this register, but ML610403 does not have it.
[*2] Initial value for ML610401
[*3] Initial value for ML610402

Appendix B　Package Dimensions

Not available

Appendix C   Electrical Characteristics

● Absolute Maximum Ratings

(V$_{SS}$= 0V)

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage 1	V$_{DD}$	Ta=25°C	-0.3 to +4.6	V
Power supply voltage 2	V$_{DDL}$	Ta=25°C	-0.3 to +3.6	V
Power supply voltage 3	V$_{L1}$	Ta=25°C	-0.3 to +2.0	V
Power supply voltage 4	V$_{L2}$	Ta=25°C	-0.3 to +4.0	V
Power supply voltage 5	V$_{L3}$	Ta=25°C	-0.3 to +6.0	V
Input voltage	V$_{IN}$	Ta=25°C	-0.3 to V$_{DD}$+0.3	V
Output voltage	V$_{OUT}$	Ta=25°C	-0.3 to V$_{DD}$+0.3	V
output current 1	I$_{OUT1}$	Port 3 to 6, Ta=25°C	-12 to +11	mA
Output current 2	I$_{OUT2}$	Port 2, Ta=25°C	-12 to +20	mA
Power dissipation	PD	Ta=25°C	0.9	W
Storage temperature	T$_{STG}$	—	-55 to +150	°C

● Recommended Operation Condition

(V$_{SS}$= 0V)

Parameter	Symbol	Condition	Range	Unit
Operating temperature	T$_{OP}$	without P version	-20 to +70	°C
		P version	-40 to +85	
Operating voltage	V$_{DD}$	f$_{OP}$=30k to 625kHz	1.25 to 3.6	V
Operating frequency (CPU)	f$_{OP}$	V$_{DD}$=1.25 to 3.6V	30k to 625k	Hz
V$_{DD}$ pin external capacitance	C$_V$	—	1.0±30% to 2.2±30%[*1]	μF
V$_{DDL}$ pin external capacitance	C$_L$	—	0.47±30% to 2.2±30%[*2]	μF
V$_{L1, 2, or 3}$ pin external capacitance	C$_{a,b,c}$	—	0.1±30%	μF
Pin-to-pin (C1 to C2) external capacitance	C$_{12}$	—	0.47±30%	μF

[*1]: Please select C$_V$ as to be larger than C$_L$ or same as C$_L$.
[*2]: When the load of V$_{DD}$ is small and the power rise time is too short, it may happen that the power-on reset is not generated. In this case, please select larger capacitance value for C$_L$.

● Clock Generation Circuit Operating Conditions

(V$_{SS}$ = 0V)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Low-speed crystal oscillation frequency	f$_{XTL}$	—	—	32.768k	—	Hz
Recommended equivalent series resistance value of low-speed crystal oscillation	R$_L$	—	—	—	40k	Ω
Low-speed crystal oscillation external capacitor	C$_{DL}$/C$_{GL}$	C$_L$=6pF of crystal oscillation	—	12	—	pF
		C$_L$=9pF of crystal oscillation	—	18	—	
		C$_L$=12pF of crystal oscillation	—	24	—	

●DC Characteristics (1/5)

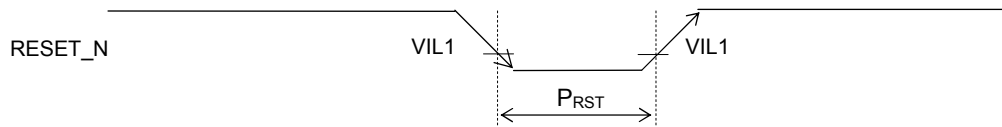(V_{DD}=1.25 to 3.6V, V_{SS}=0V, Ta=-20 to +70°C, Ta=-40 to +85°C for P version, unless otherwise specified)

Parameter	Symbol	Condition			Rating			Unit	Measurement circuit
					Min.	Typ.	Max.		
500kHz RC oscillation frequency	f_{RC}	V_{DD}=1.25 to 3.6V	Ta=25°C		Typ. -10%	500	Typ. +10%	kHz	1
			*3		Typ. -25%	500	Typ. +25%	kHz	
Low-speed crystal oscillation start time*2	T_{XTL}	—			—	0.6	2	s	
500kHz RC oscillation start time	T_{RC}	—			—	—	3	μs	
Low-speed oscillation stop detect time*1	T_{STOP}	—			12	16.4	41	ms	
Reset pulse width	P_{RST}	—			200	—	—	μs	
Reset noise elimination pulse width	P_{NRST}	—			—	—	0.3		
Power-on reset generated power rise time	T_{POR}	—			—	—	10	ms	

*1: When low-speed crystal oscillation stops for a duration more than the low-speed oscillation stop detect time, the system is reset to shift to system reset mode.
*2: 32.768kHz crystal resonator DT-26 (Load capacitance 6pF) (made by KDS:DAISHINKU CORP.) is used ($C_{GL}=C_{DL}$=6pF).
*3: Recommended operating temperature (Ta=-20 to 70°C, Ta=-40 to 85°C for P version)

Reset pulse width (P_{RST})

Power-on reset activation power rise time (T_{POR})

● DC Characteristics (2/5)

(V_{DD}=1.25 to 3.6V, V_{SS}=0V, Ta=-20 to +70°C, Ta=-40 to +85°C for P version, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measurement circuit
			Min.	Typ.	Max.		
V_{DDL} voltage	V_{DDL}	fop=30k to 625kHz	1.1	1.2	1.3	V	1
V_{DDL} temperature deviation [1]	ΔV_{DDL}	V_{DD}=3.0V	—	-1	—	mV/°C	
V_{DDL} voltage dependency [1]	ΔV_{DDL}	—	—	5	20	mV/V	

[1]: The maximum V_{DDL} voltage becomes the V_{DD} voltage level when the V_{DDL} voltage determined by the temperature and voltage deviations mathematically exceeds the V_{DD} voltage.

● DC Characteristics (3/5)

(V_{DD}=3.0V, V_{SS}=0V, Ta=-20 to +70°C, Ta=-40 to +85°C for P version, unless otherwise specified)

Parameter	Symbol	Condition		Rating			Unit	Measurement circuit
				Min.	Typ.	Max.		
Supply current 1	IDD1	CPU: In STOP state. Low-speed/High-speed 500kHz oscillation: stopped.	Ta=25°C	—	0.3	0.8	μA	1
			*5	—	—	3		
Supply current 2	IDD2	CPU: In HALT state. (LTBC, WDT: Operating)*3*4. High-speed 500kHz oscillation: Stopped. LCD/BIAS circuits: Operating.*6	Ta=25°C	—	0.9	1.8	μA	
			*5	—	—	4		
Supply current 3	IDD3	CPU: In 32.768kHz operating state.*1*3 High-speed 500kHz oscillation: Stopped, LCD/BIAS circuits: Operating.*2	Ta=25°C	—	3	6	μA	
			*5	—	—	9		
Supply current 4	IDD4	CPU: In 500kHz RC operating state. LCD/BIAS circuits: Operating.*2	Ta=25°C	—	50	70	μA	
			*5	—	—	80		

*1: When the CPU operating rate is 100% (no HALT state).
*2: All SEGs: off waveform, No LCD panel load, 1/3 bias, 1/3 duty, Frame frequency: Approx. 64 Hz, Bias voltage multiplying clock: 1/128 LSCLK (256Hz)
*3 : 32.768KHz crystal resonator DT-26 (Load capacitance 6pF) (made by KDS:DAISHINKU CORP.) is used (C_{GL}=C_{DL}=6pF)
*4 : Significant bits of BLKCON0 to BLKCON4 registers except DLCD bit on BLKCON4 are all "1".
*5 : Recommended operating temperature (Ta=-20 to 70°C, Ta=-40 to 85°C for P version)
*6 : LCD Stop mode, 1/3 bias, Bias voltage multiplying clock: 1/128 LSCLK (256Hz)

●DC Characteristics (4/5)

(V_{DD}=1.25 to 3.6V, V_{SS}=0V, Ta=-20 to +70°C, Ta=-40 to +85°C for P version, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measurement circuit
			Min.	Typ.	Max.		
Output voltage 1 (P20 to P22, P24 (N-channel open drain output mode is not selected)) (P30 to P35) (P40 to P47) (P50 to P53) (P60 to P63) [1][2] (P64 to P67) [1]	VOH1	IOH1=-0.5mA, V_{DD}=1.8 to 3.6V	V_{DD} -0.5	—	—	V	2
		IOH1=-0.03mA, V_{DD}=1.25 to 3.6V	V_{DD} -0.3	—	—		
	VOL1	IOL1=+0.5mA, V_{DD}=1.8 to 3.6V	—	—	0.5		
		IOL1=+0.1mA, V_{DD}=1.25 to 3.6V	—	—	0.3		
Output voltage 2 (P20 to P22, P24 (N-channel open drain output mode is selected))	VOL2	IOL2=+5mA, V_{DD}=1.8 to 3.6V	—	—	0.5		
Output voltage 3 (COM0 to 4) (SEG0 to 13) [1] (SEG0 to 17) [2] (SEG0 to 21) [3]	VOH3	IOH3=-0.05mA, VL1=1.2V	V_{L3} -0.2	—	—		
	VOMH3	IOMH3=+0.05mA, VL1=1.2V	—	—	V_{L2} +0.2		
	VOMH3S	IOMH3S=-0.05mA, VL1=1.2V	V_{L2} -0.2	—	—		
	VOML3	IOML3=+0.05mA, VL1=1.2V	—	—	V_{L1} +0.2		
	VOML3S	IOML3S=-0.05mA, VL1=1.2V	V_{L1} -0.2	—	—		
	VOL3	IOL3=+0.05mA, VL1=1.2V	—	—	0.2		
Output leakage (P20 to P22,P24) (P30 to P35) (P40 to P47) (P50 to P53) (P60 to P63) [1][2] (P64 to P67) [1]	IOOH	VOH=V_{DD} (in high-impedance state)	—	—	1	μA	3
	IOOL	VOL=V_{SS} (in high-impedance state)	-1	—	—		
Input current 1 (RESET_N)	IIH1	VIH1=V_{DD}	—	—	1	μA	4
	IIL1	VIL1=V_{SS}	-600	-300	-2		
Input current 2 (TEST0)	IIH2	VIH2=V_{DD}	2	—	600		
	IIL2	VIL2=V_{SS}	-1	—	—		
Input current 3 (P00 to P03) (P30 to P35) (P40 to P47) (P50 to P53)	IIH3	VIH3=V_{DD}, V_{DD}=1.8 to 3.6V (when pulled-down)	2	30	200		
		VIH3=V_{DD}, V_{DD}=1.25 to 3.6V (when pulled-down)	0.01	30	200		
	IIL3	VIL3=V_{SS}, V_{DD}=1.8 to 3.6V (when pulled-up)	-200	-30	-2		
		VIL3=V_{SS}, V_{DD}=1.25 to 3.6V (when pulled-up)	-200	-30	-0.01		
	IIH3Z	VIH3=V_{DD} (in high-impedance state)	—	—	1		
	IIL3Z	VIL3=V_{SS} (in high-impedance state)	-1	—	—		

[1]: Characteristics for ML610401.
[2]: Characteristics for ML610402.
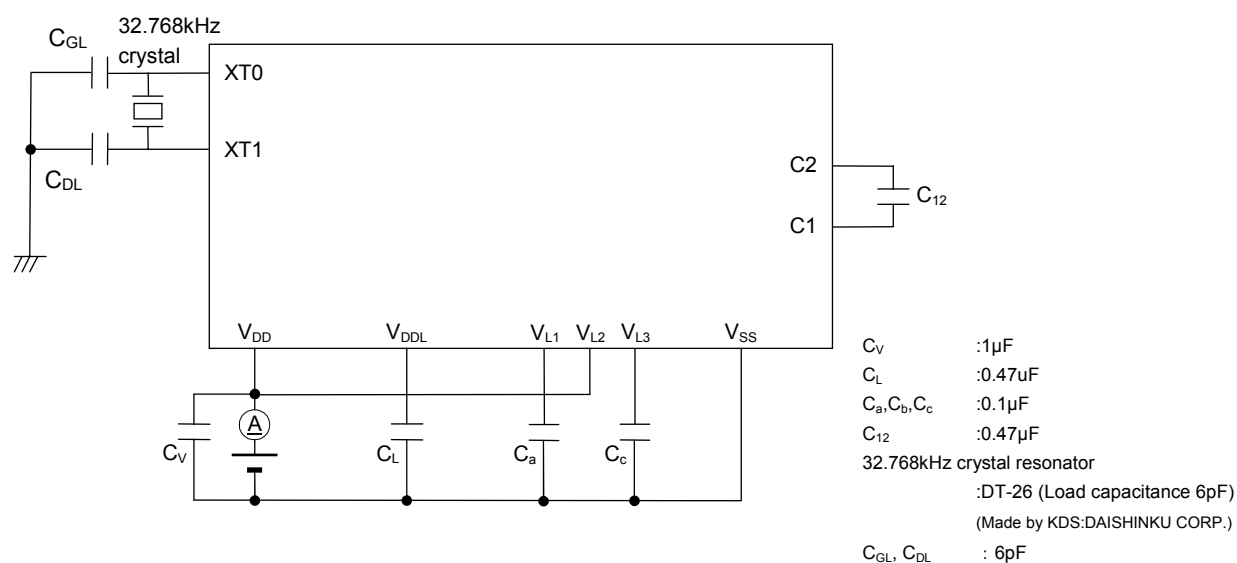[3]: Characteristics for ML610403.

●DC Characteristics (5/5)

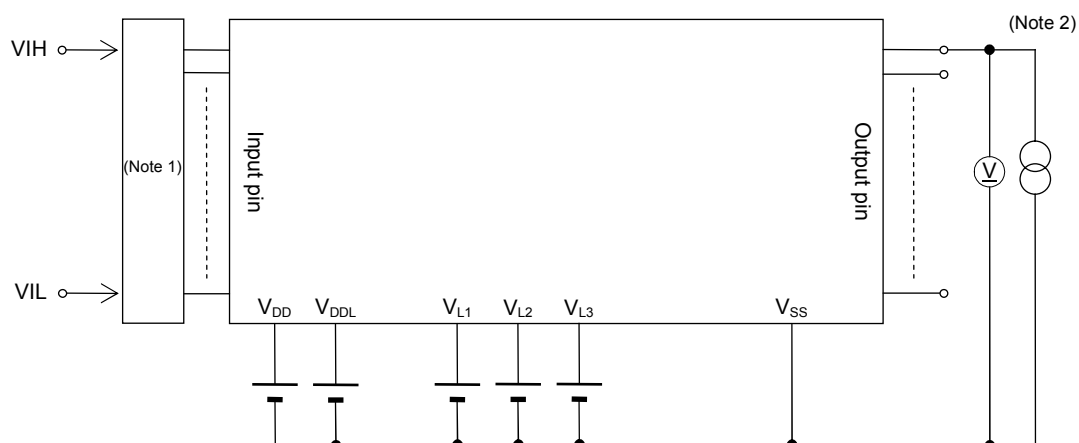(V_{DD}=1.25 to 3.6V, V_{SS}=0V, Ta=-20 to +70°C, Ta=-40 to +85°C for P version, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measurement circuit
			Min.	Typ.	Max.		
Input voltage 1 (RESET_N) (TEST0) (P00 to P03) (P30 to P35) (P40 to P47) (P50 to P53)	VIH1	—	0.7 ×V_{DD}	—	V_{DD}	V	5
	VIL1	V_{DD}=1.8 to 3.6V	0	—	0.3 ×V_{DD}		
		V_{DD}=1.25 to 3.6V	0	—	0.2 ×V_{DD}		
Input pin capacitance (P00 to P03) (P30 to P35) (P40 to P47) (P50 to P53)	CIN	f=10kHz V_{rms}=50mV Ta=25°C	—	—	5	pF	—

● Measuring circuit

Measuring circuit 1

C_V : 1μF
C_L : 0.47uF
C_a, C_b, C_c : 0.1μF
C_{12} : 0.47μF
32.768kHz crystal resonator
 : DT-26 (Load capacitance 6pF)
 (Made by KDS:DAISHINKU CORP.)
C_{GL}, C_{DL} : 6pF

Measuring circuit 2

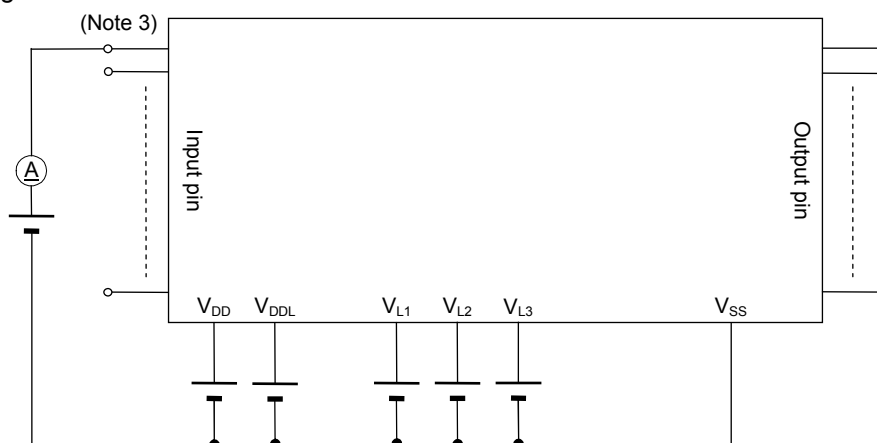(Note 1) Input logic circuit to determine the specified measuring conditions.
(Note 2) Repeats for the specified output pin
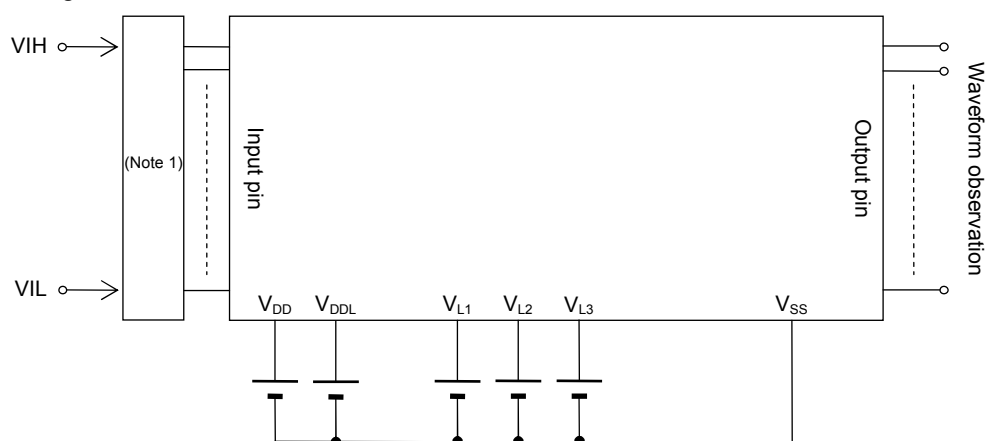
Measuring circuit 3
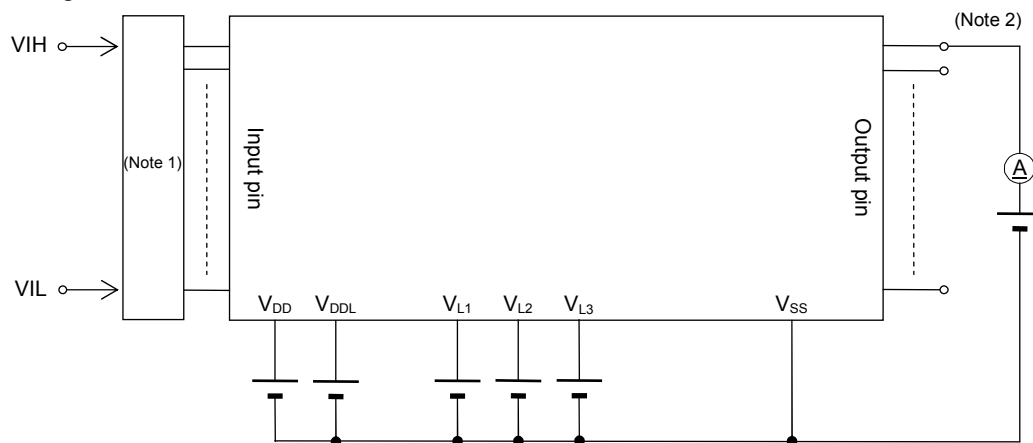
(Note 1) Input logic circuit to determine the specified measuring conditions.
(Note 2) Repeats for the specified output pin

Measuring circuit 4

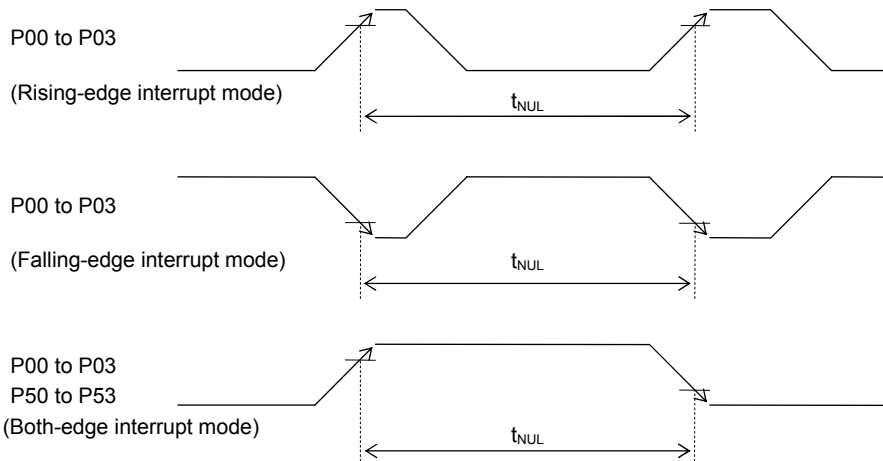(Note 3) Repeats for the specified input pin

Measuring circuit 5

(Note 1) Input logic circuit to determine the specified measuring conditions.

● AC Characteristics (External Interrupt)

(V_{DD}=1.25 to 3.6V, V_{SS}=0V, Ta=-20 to +70°C, Ta=-40 to +85°C for P version, unless otherwise specified)

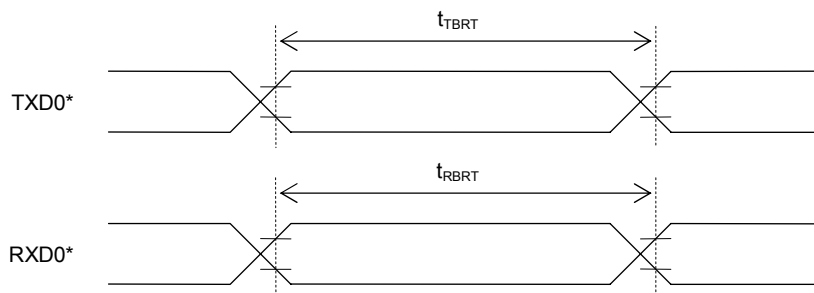| Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
External interrupt disable period	T_{NUL}	Interrupt: Enabled (MIE = 1), CPU: NOP operation System clock: 32.768kHz	76.8	—	106.8	μs

P00 to P03

(Rising-edge interrupt mode)

P00 to P03

(Falling-edge interrupt mode)

P00 to P03
P50 to P53
(Both-edge interrupt mode)

● AC Characteristics (UART)

(V_{DD}=1.25 to 3.6V, V_{SS}=0V, Ta=-20 to +70°C, Ta=-40 to +85°C for P version, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Transmit baud rate	t_{TBRT}	—	—	BRT[1]	—	s
Receive baud rate	t_{RBRT}	—	BRT[1] -3%	BRT[1]	BRT[1] +3%	s

[1]: Baud rate period (including the error of the clock frequency selected) set with the UART baud rate register (UA0BRTL,H) and the UART mode register 0 (UA0MOD0).

TXD0*

RXD0*

*: Indicates the secondary function of the port.

● AC CHARACTERISTICS (RC Oscillation A/D Converter)
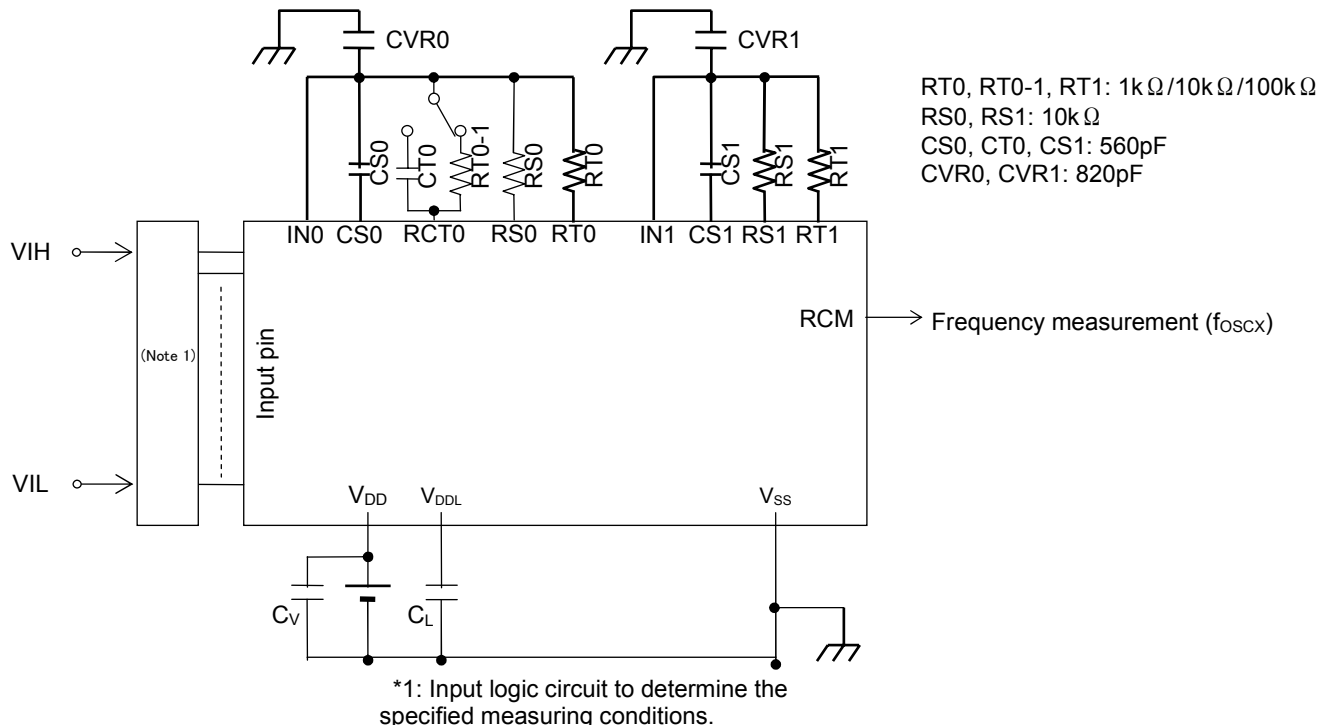
Condition for V_{DD}=1.8 to 3.6V

(V_{DD}=1.8 to 3.6V, V_{SS}=0V, Ta=-20 to +70°C, Ta=-40 to +85°C for P version, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Oscillation resistor	RS0,RS1,RT0, RT0-1,RT1	CS0, CT0, CS1≥740pF	1	—	—	kΩ
Oscillation frequency V_{DD} = 3.0V	f_{OSC1}	Resistor for oscillation=1kΩ	457.3	525.2	575.1	kHz
	f_{OSC2}	Resistor for oscillation=10kΩ	53.48	58.18	62.43	kHz
	f_{OSC3}	Resistor for oscillation=100kΩ	5.43	5.89	6.32	kHz
RS to RT oscillation frequency ratio [1] V_{DD} = 3.0V	Kf1	RT0, RT0-1, RT1=1kΩ	7.972	9.028	9.782	—
	Kf2	RT0, RT0-1, RT1=10kΩ	0.981	1	1.019	—
	Kf3	RT0, RT0-1, RT1=100kΩ	0.099	0.101	0.104	—

[1]: Kfx is the ratio of the oscillation frequency by the sensor resistor to the oscillation frequency by the reference resistor on the same conditions.

$$ Kfx = \frac{f_{OSCx}(RT0\text{-}CS0 \text{ oscillation})}{f_{OSCx}(RS0\text{-}CS0 \text{ oscillation})}, \quad \frac{f_{OSCx}(RT0\text{-}1\text{-}CS0 \text{ oscillation})}{f_{OSCx}(RS0\text{-}CS0 \text{ oscillation})}, \quad \frac{f_{OSCx}(RT1\text{-}CS1 \text{ oscillation})}{f_{OSCx}(RS1\text{-}CS1 \text{ oscillation})} $$

(x = 1, 2, 3)

RT0, RT0-1, RT1: 1kΩ/10kΩ/100kΩ
RS0, RS1: 10kΩ
CS0, CT0, CS1: 560pF
CVR0, CVR1: 820pF

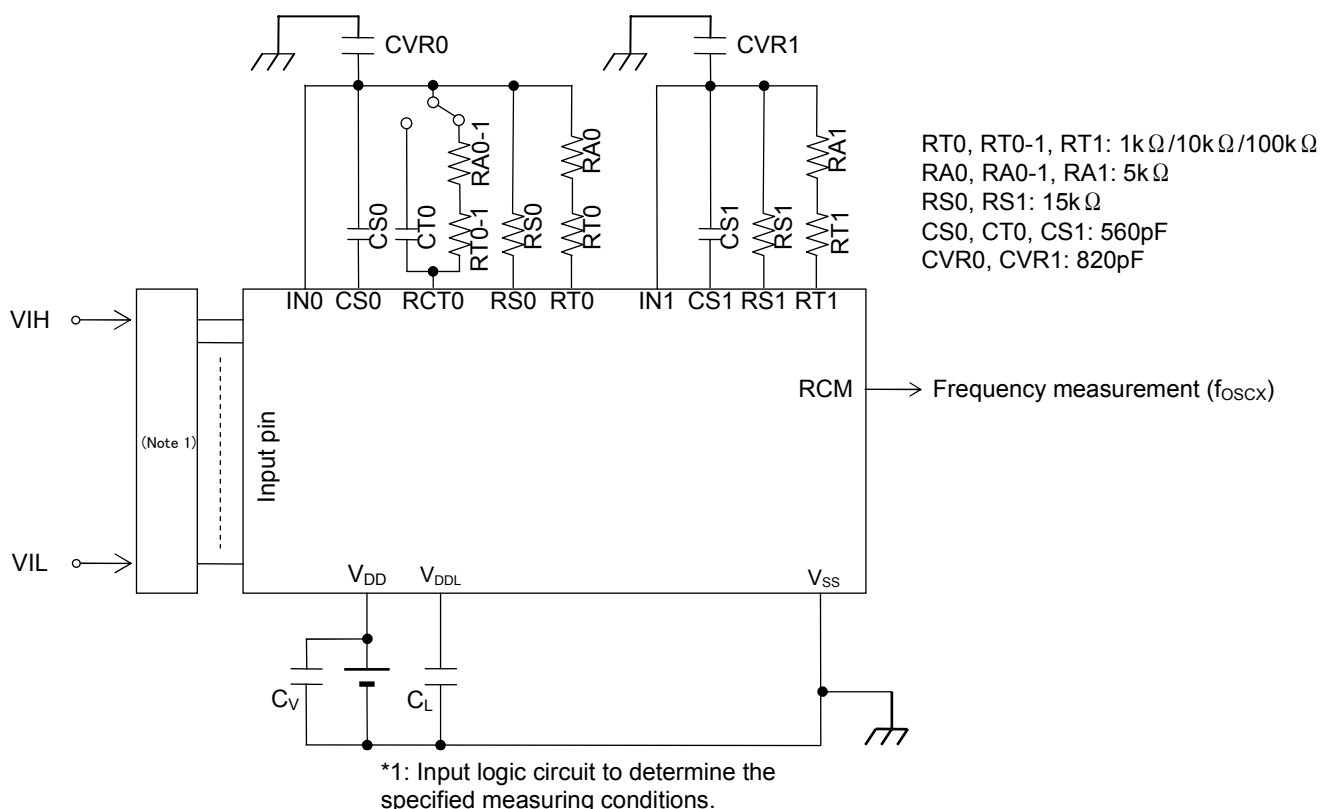*1: Input logic circuit to determine the specified measuring conditions.

Condition for V_{DD}=1.25 to 3.6V

(V_{DD}=1.25 to 3.6V, V_{SS}=0V, Ta=-20 to +70°C, Ta=-40 to +85°C for P version, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Oscillation resistor	RS0,RS1,RT0, RT0-1,RT1	CS0, CT0, CS1≥740pF	1	—	—	kΩ
Oscillation frequency V_{DD} = 1.5V	f_{OSC1}	Resistor for oscillation=6kΩ	81.93	93.16	101.2	kHz
	f_{OSC2}	Resistor for oscillation=15kΩ	35.32	38.75	41.48	kHz
	f_{OSC3}	Resistor for oscillation=105kΩ	5.22	5.65	6.03	kHz
RS to RT oscillation frequency ratio [*1] V_{DD} = 1.5V	Kf1	RT0, RT0-1, RT1=1kΩ	2.139	2.381	2.632	—
	Kf2	RT0, RT0-1, RT1=10kΩ	0.973	1	1.028	—
	Kf3	RT0, RT0-1, RT1=100kΩ	0.142	0.147	0.152	—
Oscillation frequency V_{DD} = 3.0V	f_{OSC1}	Resistor for oscillation=6kΩ	85.28	94.58	103.3	kHz
	f_{OSC2}	Resistor for oscillation=15kΩ	35.72	38.87	41.78	kHz
	f_{OSC3}	Resistor for oscillation=105kΩ	5.189	5.622	6.012	kHz
RS to RT oscillation frequency ratio [*1] V_{DD} = 3.0V	Kf1	RT0, RT0-1, RT1=1kΩ	2.227	2.432	2.626	—
	Kf2	RT0, RT0-1, RT1=10kΩ	0.982	1	1.018	—
	Kf3	RT0, RT0-1, RT1=100kΩ	0.141	0.145	0.149	—

[*1]: Kfx is the ratio of the oscillation frequency by the sensor resistor to the oscillation frequency by the reference resistor on the same conditions.

$$Kfx = \frac{f_{OSCx}(RT0\text{-}CS0\ oscillation)}{f_{OSCx}(RS0\text{-}CS0\ oscillation)}, \quad \frac{f_{OSCx}(RT0\text{-}1\text{-}CS0\ oscillation)}{f_{OSCx}(RS0\text{-}CS0\ oscillation)}, \quad \frac{f_{OSCx}(RT1\text{-}CS1\ oscillation)}{f_{OSCx}(RS1\text{-}CS1\ oscillation)}$$
(x = 1, 2, 3)

RT0, RT0-1, RT1: 1kΩ/10kΩ/100kΩ
RA0, RA0-1, RA1: 5kΩ
RS0, RS1: 15kΩ
CS0, CT0, CS1: 560pF
CVR0, CVR1: 820pF

*1: Input logic circuit to determine the specified measuring conditions.

Note:

·Please have the shortest layout for the common node (wiring patterns which are connected to the external capacitors, resistors and IN0/IN1 pin), including CVR0/CVR1. Especially, do not have long wiring between IN0/IN1 and RS0/RS1. The coupling capacitance on the wires may occur incorrect A/D conversion. Also, please do not have signals which may be a source of noise around the node.

·When RT0/RT1 (Thermistor and etc.) requires long wiring due to the restricted placement, please have V_{SS}(GND) trace next to the signal.

·Please make wiring to components (capacitor, resistor, and so on) necessary for objective measurement. Wiring to reserved components may affect to the A/D conversion operation by noise the components itself may have.

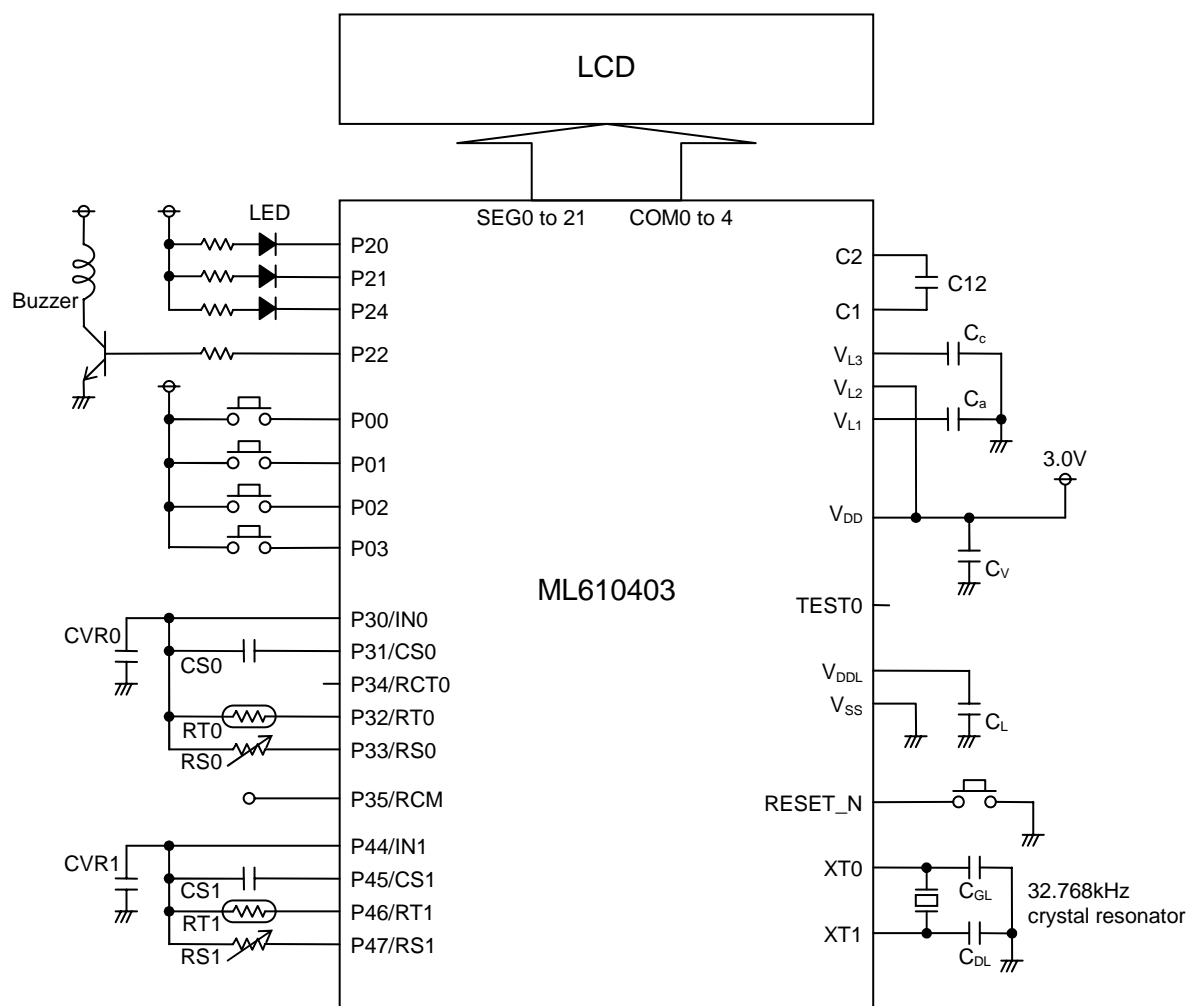# Appendix D   Application Circuit Example

Figure D-1   ML610403 Application Circuit Diagram

Appendix E   Check List

This Check List has notes to prevent commonly-made programming mistakes and frequently overlooked or misunderstood hardware features of the MCU. Check each note listed up chapter by chapter while coding the program or evaluating it using the MCU.

Chapter 1 Overview
•About unused pins

[   ] Please confirm how to handle the unused pins(Refer to Section 1.3.4 in the user's manual).

Chapter 2 CPU and Memory Space
•Program Memory size

[   ] 5,888 Byte (0:0000H to 0:16FFH)

•Data RAM size

[   ] 192 Byte (0:E000H to 0:E0BFH)

•Unused area

[   ] Please fill test area 0:3D00H to 0:3DFFH with BRK instruction code "0FFH" (Refer to a startup file "S61040XSW.asm" for programming in the source code).

[   ] For fail safe in your system, please fill unused program memory area (your program code does not use) with BRK instruction code "0FFH".

•RAM initialization

[   ] The hardware reset does not initialize RAM. Please initialize RAM by the software.

Chapter 3 Reset
•Reset activation pulse width

[   ] Minimum 200us (Refer to Appendix C-2 in the user's manual)

•Power-on reset occurrence power rise time

[   ] Maximum 10ms (Refer to Appendix C-2 in the user's manual)

•Reset status flag

[   ] No flag is provided that indicates the occurrence of reset by the RESET_N pin (Refer to section 3.2.2. in the user's manual).

•BRK instruction reset

[   ] In system reset by the BRK instruction, no special function register (SFR) is initialized either. Therefore initialize the SFRs by your software (see Section 3.3.1 in the User's Manual).

Chapter 4 MCU Control Function
•STOP mode

[   ] When the MIE flag is "0", the stop code acceptor (STPACP) cannot be enabled under the condition where both the interrupt enable and request flags become "1" (Refer to Sections 4.2.2 and 4.2.3 in the user's manual).

[   ] Place two NOP instructions next to the instruction that sets the STP bit to "1" (Refer to Section 4.3.3. in the user's manual).

•HALT mode

[   ] Place two NOP instructions next to the instruction that sets the HLT bit to "1" (Refer to Section 4.3.2. in the user's manual).

•BLKCON register

[   ] BLKCON registers enable or disable corresponsive each peripheral (Refer to Section 4.2.4 - 4.2.8. in the user's manual).

[   ] When certain bits of block control registers are set to "1", corresponding peripherals are reset (all registers are reset) and operating clocks for the peripherals stop.

Chapter 5 Interrupts
•Unused interrupt vector table

[   ] Please define all unused interrupt vector tables for fail safe.

•Non-maskable interrupt

[   ] The watchdog timer interrupt (WDTINT) is a non-maskable interrupt that does not depend on MIE flag (Refer to Sections 5.2.8. and 5.3 in the User's Manual).

Chapter 6 Clock Generation Circuit
•Initial System clock
[   ] At power up or system reset, the 32.768kHz crystal oscillation clock oscillates to be supplied to CPU as the system clock.
•Switching high-speed clock operation mode to low-speed clock operation mode
[   ] When switching the high-speed clock to the low-speed clock after the recovery from the STOP mode, make sure the low-speed clock is oscillating checking to see the low-speed time base counter's Q128H bit becomes "1".
•Port secondary function setting
[   ] Specify the secondary function for the port 2 when driving a clock to the pin(Refer to Section 6.4 in the user's manual).

Chapter 7 TBC (Time Base Counter)
•HTBCLK
[   ] When using the HTBCLK for a timer, set an arbitrary dividing ratio in the high-speed side time base counter frequency divide register (HTBDR register) (see Section 7.2.3. in the User's Manual).
•How to read LTBC
[   ] Read consecutively LTBC(Low-speed Time Base Counter) twice until the last data coincides the previous data to prevent reading of uncertain data while counting up the clock (Refer to Section 7.3.1 in the user's manual).

Chapter 9 Timer
•How to read the timer counter registers
[   ] Check notes for reading the timer counter registers while counting up (Refer to Sections 9.2.4 to 9.2.5 in the user's manual).

Chapter 10 WDT
•Overflow period
Clear WDT during the selected overflow period:
[   ] 125ms,   [   ] 500ms,   [   ] 2s,   [   ] 8s
•WDP
[   ] Check the WDP content before writing to the WDTCON register, then determine writing whether "5AH" or "0A5H" (Refer to Section 10.2.2. in the user's manual).

Chapter 11 UART
•Pins used
[   ] Use P02(RXD0) and P43(TXD0),   or   [   ] P42(RXD0) and P43(TXD0).
[   ] Select the P02 or P42 for RXD0 by specifying U0RSEL bit of UA0MOD0 register.
•Port secondary function setting
[   ] Specify the secondary Function for the port(Refer to Section 11.4 in the user's manual).

Chapters 12 to 17 Port
•Pin Handling
[   ] Don't leave Hi-impedance Input ports in floating state.
•Port secondary Function
[   ] Specify properly PnCON0/1 and PnMOD0/1 registers for each port.

Chapter 18 Melody Driver
•Enabling the LSCLK x 2
[   ] Set ENMLT bit of FCON1 register to "1" to enable the low-speed double clock (LSCLK x 2) before stating the melody or buzzer outputs.
•Port secondary function setting
[   ] Specify the secondary Function for the port(Refer to Section 18.4 in the user's manual).

Chapter 19 RC oscillation type A/D converter
•counter register
[   ] Reading the counter register A or B during the A/D conversion, returns the data written before starting the A/D conversion.
•Oscillation monitor pin
[   ] P35/RCM pin is a monitor pin for oscillation clock. The channel 0(P34-P30) and channel 1(P47-P44) share the monitor pin.
[   ] Please use P35/RCM for the evaluation purpose and disable the output while operating in an actual application to minimize the noise.
•Port secondary function setting
[   ] Specify the secondary Function for the port(Refer to Section 19.4 in the user's manual).
[   ] All the Port 3 pins except P35/RCM are configured as pins dedicated to the RC-ADC function during A/D conversion(Refer to Section 19.3.1. in the user's manual).

Chapter 20 LCD driver
•Bias
[   ] 1/3 bias
•Duty
[   ] 1/1 to 1/5 Duty
•COM/SEG
[   ] ML610401: 2COM x 14SEG
[   ] ML610401: 3COM x 13SEG
[   ] ML610401: 4COM x 12SEG
[   ] ML610401: 5COM x 11SEG

[   ] ML610402: 2COM x 18SEG
[   ] ML610402: 3COM x 17SEG
[   ] ML610402: 4COM x 16SEG
[   ] ML610402: 5COM x 15SEG

[   ] ML610403: 2COM x 22SEG
[   ] ML610403: 3COM x 21SEG
[   ] ML610403: 4COM x 20SEG
[   ] ML610403: 5COM x 19SEG

•External capacitor
(1/3 bias, V_{DD} = 1.6 to 3.6V, LCD without regulator)
[   ] Ca = 0.1uF (for V_{L1} pin), [   ] Cc = 0.1uF (for V_{L3} pin)
[   ] C12 = 0.47uF (for C1 pin to C2 pin)
(1/3 bias, V_{DD} = 2.4 to 3.6V, LCD without regulator)
[   ] Ca = 0.1uF (for V_{L1} pin), [   ] Cb = 0.1uF (for V_{L2} pin)
[   ] C12 = 0.47uF (for C1 pin to C2 pin)
(1/3 bias, V_{DD} = 1.2 to 3.6V, LCD with regulator)
[   ] Cb = 0.1uF (for V_{L2} pin), [   ] Cc = 0.1uF (for V_{L3} pin)
[   ] C12 = 0.47uF (for C1 pin to C2 pin)

Chapter 21 Power Supply Circuit
•External capacitor
[   ] C_V = 1.0uF to 2.2uF (for V_{DD} pin)
[   ] C_L = 0.47uF to 2.2uF (for V_{DDL} pin)

Appendix A SFR (Specific Function Registers)
•Initial value
[   ] Please confirm there are some SFRs have undefined initial value at reset (Refer to Appendix A in the user's manual).

Appendix C Electrical Characteristics
•Operating temperature
[   ] -20°C to +70°C
[   ] -40°C to +85°C
•Operating voltage vs Operating frequency
[   ] Please confirm the operating conditions.
    [   ] +1.25V to +3.6V (32.768kHz: Low-speed crystal oscillation clock operation)
    [   ] +1.25V to +3.6V (32.768kHz to 500kHz: Low-speed crystal oscillation clock or built-in RC oscillation clock)

Revision History

Revision History

| Document No. | Date | Page | | Description |
		Previous Edition	Current Edition	
FEUL610403-01	Dec.6, 2010	–	–	Final edition 1.0
FEUL610403-02	Oct.30, 2012	1-3	1-3	Change the package sample part s number
		6-1	6-1	Correct comment in chapter 6.1.1 Features
		C-1, E-3	C-1, E-3	Add recommended V_{DD} pin external capacitance and add the notes about the capacitance value
		C-1, E-3	C-1, E-3	Change V_{DDL} pin external capacitance and add the notes about the capacitance value
FEUL610403-03	Apr.18,2014	All	All	Change header and footer
		1-3	1-4	Change from "Shipment" to " Product name – Supported Function "
		1-2 20-3 20-4 20-5 20-8 20-18 E-3	1-2 20-3 20-4 20-7 20-17 E-3	Delete the description of LCD drivers 1/2 bias supported version
		19-7	19-7	Add notes of the case that RC-ADC is stopped by software during A / D conversion.
		C-2	C-2	Correct minimum time of Power-on reset generated power rise time
		1-3 1-5 1-6 1-7 B-1	1-4 1-6 1-7 1-8 B-1	Delete package products
FEUL610403-04	May.23,2014	-	C-1	Add Clock Generation Circuit Operating Conditions
		C-2	C-2	Change "RESET" to " Reset pulse width (P_{RST})" and " Power-on reset activation power rise time (T_{POR})".
		C-2	C-2	Correct minimum time of Power-on reset generated power rise time
		C-2	C-2	Correct the C_{GL}'s value and the C_{DL}'s value of DC CHARACTERISTICS (1/5)'s note No.2