Brian Crafton

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Education

- **Georgia Institute of Technology** — Atlanta, GA
  Ph,D. Computer Engineering — *May 2022*
  MS. Computer Engineering — *May 2019*
  Advanced Computer Architecture, CAD - Synthesis, CAD - PD, VLSI, Neuromorhpic Computing
- **Northeastern University** — Boston, MA
  Bachelor of Science in Computer Engineering; GPA: 3.7 — *Aug 2013 - May 2017*
  Compilers, Operating Systems, Nanofab, VLSI, Parallel Programming, Algorithms 1, 2, & 3

Experience

- **ICSRL, Georgia Institute of Technology** — Atlanta, GA
  Research Assistant — *May 2018 -*
  - **Emerging Device Circuits**: Worked with device collaborators to create circuit simulations using FeFETs and memristors
  - **Spiking Networks**: Developed models from experimental data for ferroelectric neurons and synapses implementing STDP to solve learning problems
  - **Memristive Neural Network**: Designed memristive neural network to solve MNIST
  - **Local Learning**: Using variation of feedback alignment algorithm to allow deep networks to learn locally
- **GTCAD, Georgia Institute of Technology** — Atlanta, GA
  Research Assistant — *Aug 2017 - May 2018*
  - **Compiler**: Developed frontend for modeling protocols. Syntax eventually translated to an abstract syntax tree and finally turned into a finite state machine
  - **Algorithms**: Implemented merging algorithms to combine two protocols to automatically generate a finite state machine for a hardware translator
  - **Full Flow**: Implemented a full flow to translate the high level syntax into Verilog and finally go down to netlist and layout
- **AMD** — Boxborough MA
  Engineer Coop — *May-Aug 2017, July-Dec 2016*
  - **Performance Verification**: Lead performance verification. Debugged bottlenecks and proposed solutions
  - **Cache**: Debugged cache bottleneck and offered tradeoffs of different models (size and eviction policy)
  - **Functional Verification**: Implemented tests at block level. Set register values and drive random and constant stimulus. Debugged RTL failures and proposed solutions
  - **Subblock Testbench**: Implemented and owned subblock test bench. Stressed cache and compression blocks
  - **Tools**: Implemented Python tools to automate verification techniques
- **Northeastern University** — Boston, MA
  Research Assistant — *May-July 2016*
  - **Bench Marks**: Implemented and modified OpenCL benchmarks for floating point research
  - **Analysis**: Ran benchmarks on different hardware platforms, collected and analyzed results
- **Basis Science, Intel** — San Francisco CA
  Engineer Coop — *July-Dec 2015*
  - **Drivers**: Sensor and flash memory drivers in embedded C
  - **Tools**: Test and data generation for learning algorithms
- **EMC** — Franklin MA
  Engineer Coop — *July-Dec 2014*

Publications

- Z. Wang, B. Crafton, T. Tomas-Gomez, X. Ruijuan, A. Luo, Z. Krivokapic, L. Martin, S. Datta, A. Raychowdhury, and A. Khan. Experimental demonstration of ferroelectric spiking neurons for unsupervised clustering. In ElectronDevices Meeting (IEDM), 2018 IEEE International. IEEE, 2018
- Bayati, Mahsa, Brian Crafton, Miriam Leeser, Yijia Gu, and Thomas Wahl. Identifying Volatile Numeric Expressions in OpenCL Applications.

Projects

- **Compiler - Assembler - Processor**: Out of order, superscalar processor with branch prediction in Verilog. Compiler, assembler, test bench, and emulator.
- **Memory Simulator**: DRAM and cache memory simulator for the processor project
- **Parallel Neural Network**: Parallel programming project. Written in C, MPI, OpenMP.
- **Wireless Speakers**: Lead of senior capstone design. Synchronized wireless speakers.
- **Data Structures**: C implementation of 15 popular data structures

Programming Skills

- **Programming**: C, C++, Python
- **HDL**: Verilog, System Verilog
- **Technologies**: Debugger, Oscilloscope, Git, Perforce, Simulation, Synthesis, Place and Route tools