TEXAS INSTRUMENTS

**TMP102**

ZHCSIX4H –AUGUST 2007 –REVISED DECEMBER 2018

# 采用 SOT563 封装、具有 SMBus 和双线制串行接口的 TMP102 低功耗数字温度传感器

## 1 特性

- SOT563 封装 (1.6mm × 1.6mm) 相较于 SOT-23，尺寸缩小了 68%
- 未经校准时的精度：
  – –25°C 至 85°C 范围内为 2.0°C（最大值）
  – –40°C 至 125°C 范围内为 3.0°C（最大值）
- 低静态电流：
  – 激活时 10µA（最大值）
  – 关断时 1µA（最大值）
- 电源电压范围：1.4V 至 3.6V
- 分辨率：12 位
- 数字输出：兼容 SMBus、双线制和 I²C 接口
- NIST 可追溯

## 2 应用

- 便携式和电池供电类 应用
- 电源温度监控
- 计算机外设过热保护
- 笔记本电脑
- 电池管理
- 办公机器
- 恒温器控制
- 机电设备温度
- 通用温度测量：
  – 工业控制
  – 测试设备
  – 医疗仪表

## 3 说明

TMP102 器件是一款数字温度传感器，非常适用于作为需要高精度的 NTC/PTC 热敏电阻的替代品。该器件在未经校准或无外部组件信号调节的情况下可提供的精度为 ±0.5°C。器件温度传感器为高度线性化产品，无需复杂计算或查表即可得知温度。片上 12 位 ADC 具备最低 0.0625°C 的分辨率。

1.6mm × 1.6mm 的 SOT563 封装相较于 SOT-23 封装，尺寸缩小了 68%。TMP102 器件 具备 SMBus™、两线制和 I²C 接口兼容性，最多允许四个器件位于一条总线上。此外，该器件还 具备 SMBus 报警功能。器件的额定工作电压范围是 1.4V 至 3.6V，整个工作范围内最大静态电流为 10µA。

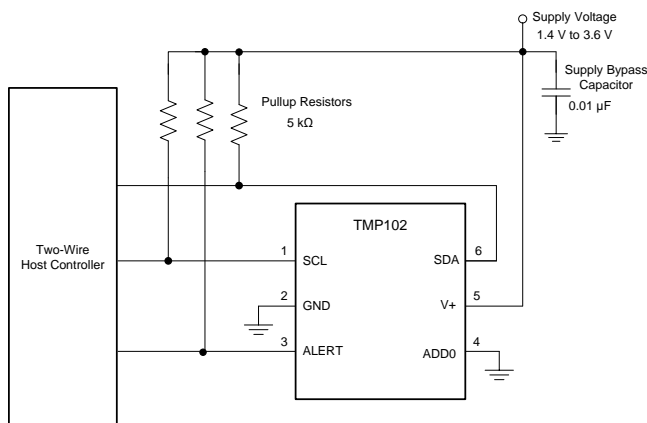TMP102 器件适用于在各种通信、计算机、消费类产品、环境、工业和仪表 应用中进行扩展温度测量。器件的额定工作温度范围为 –40°C 至 125°C。

TMP102 生产单元已经过 100% 的传感器测试，具有 NIST 可追溯的特点，并已借助 NIST 可追溯的设备使用 ISO/IEC 17025 标准认可的校准要求进行验证。
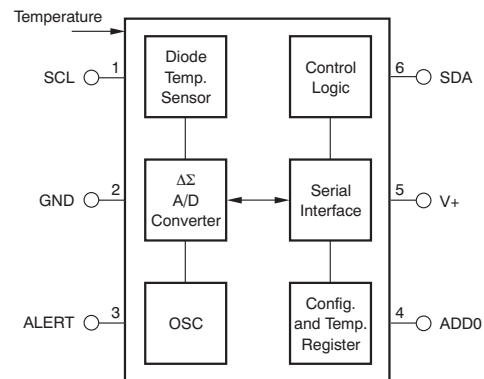
### 器件信息[1]

| 器件型号 | 封装 | 封装尺寸（标称值） |
| --- | --- | --- |
| TMP102 | SOT563 (6) | 1.60mm x 1.20mm |

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

### 简化电路原理图



### 方框图

English Data Sheet: SBOS397

<h1 style="text-align:center">目录</h1>

## 4  修订历史记录

注：之前版本的页码可能与当前版本有所不同。

**Changes from Revision G (September 2018) to Revision H**     **Page**

- Changed *Absolute Maximum Ratings* for voltage at SCL, SDA and ADD0 pin ... 4
- Changed *Absolute Maximum Ratings* for voltage at ALERT pin ... 4

**Changes from Revision F (September 2018) to Revision G**     **Page**

- Changed input voltage maximum value from: 3.6 V to: 4 V ... 4
- Changed output voltage maximum value from: 3.6 V to: ((V+) + 0.5) and ≤ 4 V ... 4
- Changed Junction-to-ambient thermal resistance from 200 °C/W to 210.3 °C/W ... 5
- Changed Junction-to-case (top) thermal resistance from 73.7 °C/W to 105.0 °C/W ... 5
- Changed Junction-to-board thermal resistance from 34.4 °C/W to 87.5 °C/W ... 5
- Changed Junction-to-top characterization parameter from 3.1 °C/W to 6.1 °C/W ... 5
- Changed Junction-to-board characterization parameter from 34.2 °C/W to 87.0 °C/W ... 5
- 添加了*接收文档更新通知* 部分 ... 24

**Changes from Revision E (April 2015) to Revision F**     **Page**

- 添加了 TI 设计 ... 1
- 添加 NIST 特性 要点 ... 1
- *说明* 部分的最后添加了一个段落 ... 1

**Changes from Revision D (December 2014) to Revision E**     **Page**

- Changed the MAX value for the Supply voltage from 3.6 to 4 in the *Absolute Maximum Ratings* table ... 4
- Changed MIN, TYP, and MAX values for the Temperature Accuracy (temperature error) parameter ... 5
- Changed the frequency from 2.85 to 3.4 MHz in the POWER SUPPLY section of the *Electrical Characteristics* table ... 6
- Changed the Temperature Error vs Temperature graph in the *Typical Characteristics* section ... 7

**Changes from Revision C (October 2012) to Revision D**                                                     **Page**

**Changes from Revision B (October 2008) to Revision C**                                                     **Page**

# 5 Pin Configuration and Functions

**DRL Package**
**6-Pin SOT563**
**Top View**

```
        ┌─────────┐
 SCL  1 │  ───    │ 6  SDA
        │   C     │
 GND  2 │   B     │ 5  V+
        │   Z     │
ALERT 3 │         │ 4  ADD0
        └─────────┘
```
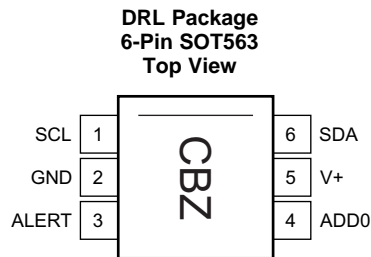
**Pin Functions**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| 1 | SCL | I | Serial clock. Open-drain output; requires a pullup resistor. |
| 2 | GND | — | Ground |
| 3 | ALERT | O | Overtemperature alert. Open-drain output; requires a pullup resistor. |
| 4 | ADD0 | I | Address select. Connect to GND or V+ |
| 5 | V+ | I | Supply voltage, 1.4 V to 3.6 V |
| 6 | SDA | I/O | Serial data. Open-drain output; requires a pullup resistor. |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

| | MIN | MAX | UNIT |
|---|---|---|---|
| Supply Voltage | | 4 | V |
| Voltage at SCL, SDA and ADD0[2] | −0.5 | 4 | V |
| Voltage at ALERT | | ((V+) + 0.3) and ≤ 4 | V |
| Operating temperature | −55 | 150 | °C |
| Junction temperature | | 150 | °C |
| Storage temperature, $T_{stg}$ | −60 | 150 | °C |

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.
(2) Input voltage rating applies to all TMP102 input voltages.

## 6.2 Handling Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1] | ±2000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101[2] | ±1000 | |
| | | Machine model (MM) | ±200 | |

(1) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|  |  | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| V+ | Supply voltage | 1.4 | 3.3 | 3.6 | V |
| $T_A$ | Operating free-air temperature | −40 | | 125 | °C |

## 6.4 Thermal Information

| | THERMAL METRIC[1] | TMP102 | UNIT |
|---|---|---|---|
| | | DRL (SOT563) | |
| | | 6 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 210.3 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 105.0 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 87.5 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 6.1 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 87.0 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

## 6.5 Electrical Characteristics

At $T_A$ = 25°C and $V_S$ = 1.4 to 3.6 V, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **TEMPERATURE INPUT** | | | | | | |
| Range | | | −40 | | 125 | °C |
| Accuracy (temperature error) | | −25°C to 85°C | | ±0.5 | ±2 | °C |
| | | −40°C to 125°C | | ±1 | ±3 | |
| vs supply | | | | 0.2 | 0.5 | °C/V |
| Resolution | | | | 0.0625 | | °C |
| **DIGITAL INPUT/OUTPUT** | | | | | | |
| Input capacitance | | | | 3 | | pF |
| $V_{IH}$ | Input logic high | | 0.7 × (V+) | | 3.6 | V |
| $V_{IL}$ | Input logic low | | −0.5 | | 0.3 × (V+) | V |
| $I_{IN}$ | Input current | 0 < $V_{IN}$ < 3.6 V | | | 1 | µA |
| $V_{OL}$ | Output logic | SDA | V+ > 2 V, $I_{OL}$ = 3 mA | 0 | | 0.4 | V |
| | | | V+ < 2 V, $I_{OL}$ = 3 mA | 0 | | 0.2 × (V+) | |
| | | ALERT | V+ > 2 V, $I_{OL}$ = 3 mA | 0 | | 0.4 | |
| | | | V+ < 2 V, $I_{OL}$ = 3 mA | 0 | | 0.2 × (V+) | |
| Resolution | | | | 12 | | Bit |
| Conversion time | | | | 26 | 35 | ms |
| Conversion modes | | CR1 = 0, CR0 = 0 | | 0.25 | | Conv/s |
| | | CR1 = 0, CR0 = 1 | | 1 | | |
| | | CR1 = 1, CR0 = 0 (default) | | 4 | | |
| | | CR1 = 1, CR0 = 1 | | 8 | | |
| Timeout time | | | | 30 | 40 | ms |

## Electrical Characteristics (continued)

At $T_A$ = 25°C and $V_S$ = 1.4 to 3.6 V, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **POWER SUPPLY** | | | | | | |
| | Operating supply range | | +1.4 | | +3.6 | V |
| $I_Q$ | Average quiescent current | Serial bus inactive, CR1 = 1, CR0 = 0 (default) | | 7 | 10 | µA |
| | | Serial bus active, SCL frequency = 400 kHz | | 15 | | |
| | | Serial bus active, SCL frequency = 3.4 MHz | | 85 | | |
| $I_{SD}$ | Shutdown current | Serial bus inactive | | 0.5 | 1 | µA |
| | | Serial bus active, SCL frequency = 400 kHz | | 10 | | |
| | | Serial bus active, SCL frequency = 3.4 MHz | | 80 | | |
| **TEMPERATURE** | | | | | | |
| | Specified range | | –40 | | 125 | °C |
| | Operating range | | –55 | | 150 | °C |

## 6.6 Timing Requirements

See the *Timing Diagrams* section for additional information.

| | | | FAST MODE | | | HIGH-SPEED MODE | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $f_{(SCL)}$ | SCL operating frequency | V+ | 0.001 | | 0.4 | 0.001 | | 2.85 | MHz |
| $t_{(BUF)}$ | Bus-free time between STOP and START condition | See Figure 7 | 600 | | | 160 | | | ns |
| $t_{(HDSTA)}$ | Hold time after repeated START condition. After this period, the first clock is generated. | | 600 | | | 160 | | | ns |
| $t_{(SUSTA)}$ | repeated start condition setup time | | 600 | | | 160 | | | ns |
| $t_{(SUSTO)}$ | STOP condition setup time | | 600 | | | 160 | | | ns |
| $t_{(HDDAT)}$ | Data hold time | | 100 | | 900 | 25 | | 105 | ns |
| $t_{(SUDAT)}$ | Data setup time | | 100 | | | 25 | | | ns |
| $t_{(LOW)}$ | SCL-clock low period | V+ , see Figure 7 | 1300 | | | 210 | | | ns |
| $t_{(HIGH)}$ | SCL-clock high period | See Figure 7 | 600 | | | 60 | | | ns |
| $t_{FD}$ | Data fall time | See Figure 7 | | | 300 | | | 80 | ns |
| $t_{RD}$ | Data rise time | See Figure 7 | | | 300 | | | | ns |
| | | SCLK ≤ 100 kHz, see Figure 7 | | | 1000 | | | | ns |
| $t_{FC}$ | Clock fall time | See Figure 7 | | | 300 | | | 40 | ns |
| $t_{RC}$ | Clock rise time | See Figure 7 | | | 300 | | | 40 | ns |

## 6.7 Typical Characteristics

At $T_A$ = 25°C and V+ = 3.3 V, unless otherwise noted.
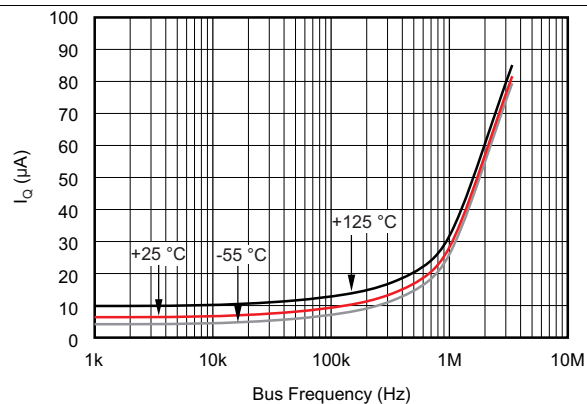


Four conversions per second
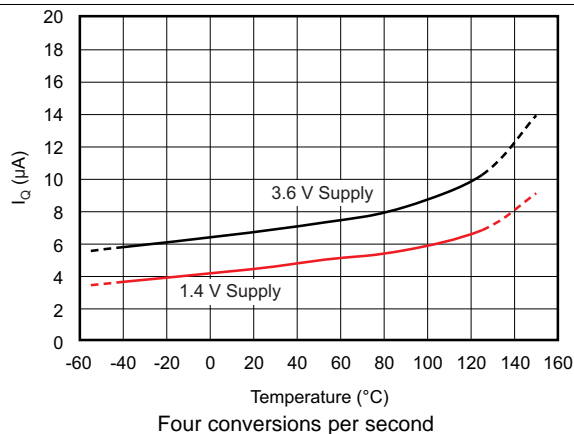
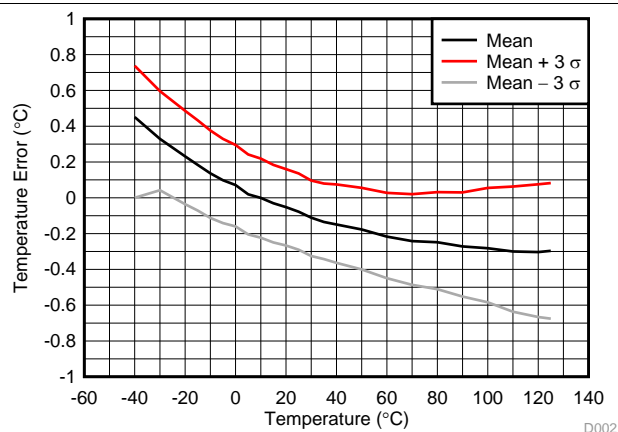**Figure 1. Average Quiescent Current vs Temperature**
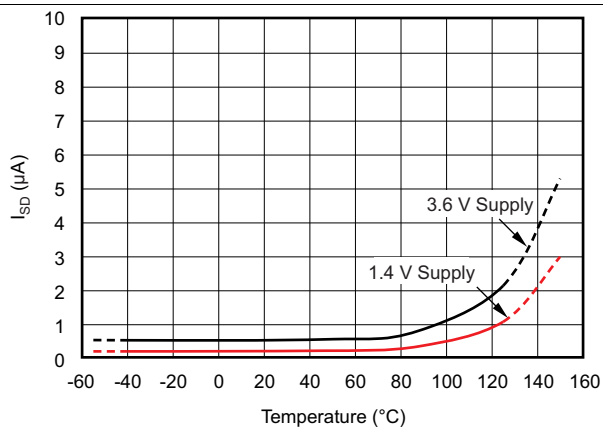


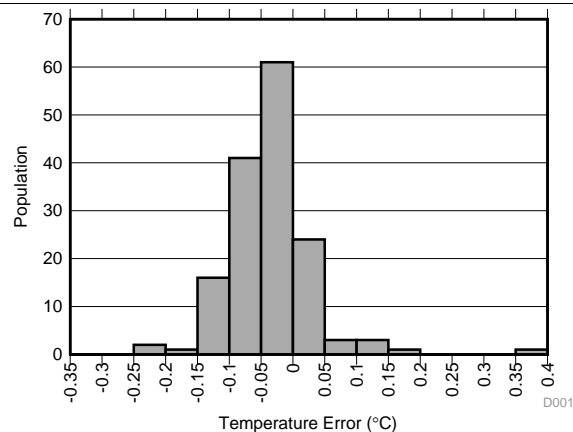**Figure 2. Shutdown Current vs Temperature**
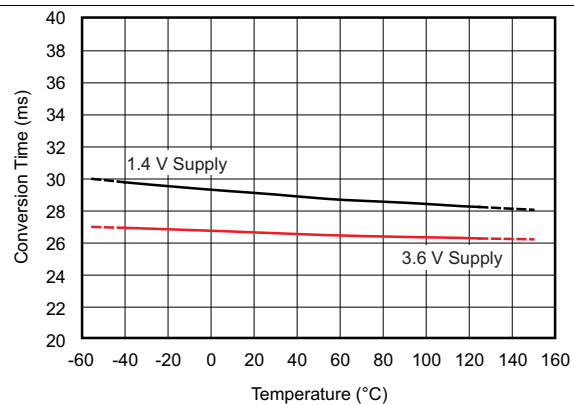


**Figure 3. Conversion Time vs Temperature**



**Figure 4. Quiescent Current vs Bus Frequency
(Temperature at 3.3-V Supply)**



**Figure 5. Temperature Error vs Temperature**



**Figure 6. Temperature Error at 25°C**

# 7 Detailed Description

## 7.1 Overview

The TMP102 device is a digital temperature sensor that is optimal for thermal-management and thermal-protection applications. The TMP102 device is two-wire, SMBus and I²C interface-compatible. The device is specified over an operating temperature range of –40°C to 125°C. See *Functional Block Diagram* for a block diagram of the TMP102 device.
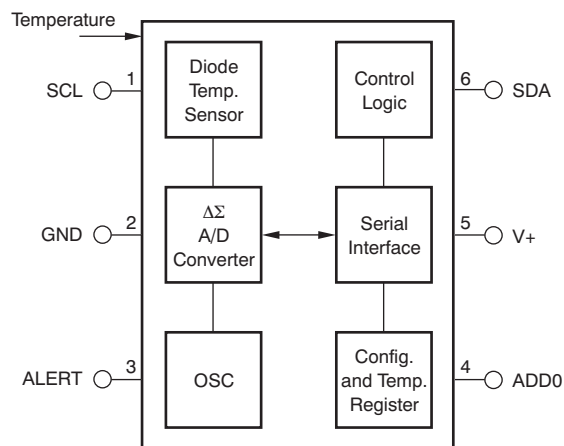
The temperature sensor in the TMP102 device is the chip itself. Thermal paths run through the package leads as well as the plastic package. The package leads provide the primary thermal path because of the lower thermal resistance of the metal.

An alternative version of the TMP102 device is available. The TMP112 device has highest accuracy, the same micro-package, and is pin-to-pin compatible.

**Table 1. Advantages of TMP112 versus TMP102**

| DEVICE | COMPATIBLE INTERFACES | PACKAGE | SUPPLY CURRENT | SUPPLY VOLTAGE (MIN) | SUPPLY VOLTAGE (MAX) | RESOLUTION | LOCAL SENSOR ACCURACY (MAX) | SPECIFIED CALIBRATION DRIFT SLOPE |
|---|---|---|---|---|---|---|---|---|
| TMP112 | I²C SMBus | SOT563 1.2 × 1.6 × 0.6 | 10 µA | 1.4 V | 3.6 V | 12 bit 0.0625°C | 0.5°C: (0°C to 65°C) 1°C: (-40°C to 125°C) | Yes |
| TMP102 | I²C SMBus | SOT563 1.2 × 1.6 × 0.6 | 10 µA | 1.4 V | 3.6 V | 12 bit 0.0625°C | 2°C: (25°C to 85°C) 3°C: (-40°C to 125°C) | No |

## 7.2 Functional Block Diagram



## 7.3 Feature Description

### 7.3.1 Digital Temperature Output

The digital output from each temperature measurement is stored in the read-only temperature register. The temperature register of the TMP102 device is configured as a 12-bit, read-only register (configuration register EM bit = 0, see the *Extended Mode (EM)* section), or as a 13-bit, read-only register (configuration register EM bit = 1) that stores the output of the most recent conversion. Two bytes must be read to obtain data and are listed in Table 8 and Table 9. Byte 1 is the most significant byte (MSB), followed by byte 2, the least significant byte (LSB). The first 12 bits (13 bits in extended mode) are used to indicate temperature. The least significant byte does not have to be read if that information is not needed. The data format for temperature is summarized in Table 2 and Table 3. One LSB equals 0.0625°C. Negative numbers are represented in binary twos-complement format. Following power-up or reset, the temperature register reads 0°C until the first conversion is complete. Bit D0 of byte 2 indicates normal mode (EM bit = 0) or extended mode (EM bit = 1) , and can be used to distinguish between the two temperature register data formats. The unused bits in the temperature register always read 0.

## Feature Description (continued)

**Table 2. 12-Bit Temperature Data Format[1]**

| TEMPERATURE (°C) | DIGITAL OUTPUT (BINARY) | HEX |
|---|---|---|
| 128 | 0111 1111 1111 | 7FF |
| 127.9375 | 0111 1111 1111 | 7FF |
| 100 | 0110 0100 0000 | 640 |
| 80 | 0101 0000 0000 | 500 |
| 75 | 0100 1011 0000 | 4B0 |
| 50 | 0011 0010 0000 | 320 |
| 25 | 0001 1001 0000 | 190 |
| 0.25 | 0000 0000 0100 | 004 |
| 0 | 0000 0000 0000 | 000 |
| −0.25 | 1111 1111 1100 | FFC |
| −25 | 1110 0111 0000 | E70 |
| −55 | 1100 1001 0000 | C90 |

(1) The resolution for the Temp ADC in Internal Temperature mode is 0.0625°C/count.

Table 2 does not list all temperatures. Use the following rules to obtain the digital data format for a given temperature or the temperature for a given digital data format.

To convert positive temperatures to a digital data format:
1. Divide the temperature by the resolution
2. Convert the result to binary code with a 12-bit, left-justified format, and MSB = 0 to denote a positive sign.

   Example: (50°C) / (0.0625°C / LSB) = 800 = 320h = 0011 0010 0000

To convert a positive digital data format to temperature:
1. Convert the 12-bit, left-justified binary temperature result, with the MSB = 0 to denote a positive sign, to a decimal number.
2. Multiply the decimal number by the resolution to obtain the positive temperature.

   Example: 0011 0010 0000 = 320h = 800 × (0.0625°C / LSB) = 50°C

To convert negative temperatures to a digital data format:
1. Divide the absolute value of the temperature by the resolution, and convert the result to binary code with a 12-bit, left-justified format.
2. Generate the twos complement of the result by complementing the binary number and adding one. Denote a negative number with MSB = 1.

   Example: (|−25°C|) / (0.0625°C / LSB) = 400 = 190h = 0001 1001 0000

   Two's complement format: 1110 0110 1111 + 1 = 1110 0111 0000

To convert a negative digital data format to temperature:
1. Generate the twos compliment of the 12-bit, left-justified binary number of the temperature result (with MSB = 1, denoting negative temperature result) by complementing the binary number and adding one. This represents the binary number of the absolute value of the temperature.
2. Convert to decimal number and multiply by the resolution to get the absolute temperature, then multiply by −1 for the negative sign.

   Example: 1110 0111 0000 has twos compliment of 0001 1001 0000 = 0001 1000 1111 + 1

   Convert to temperature: 0001 1001 0000 = 190h = 400; 400 × (0.0625°C / LSB) = 25°C = (|−25°C|); (|−25°C|) × (−1) = −25°C

**Table 3. 13-Bit Temperature Data Format**

| TEMPERATURE (°C) | DIGITAL OUTPUT (BINARY) | HEX |
|---|---|---|
| 150 | 0 1001 0110 0000 | 0960 |
| 128 | 0 1000 0000 0000 | 0800 |
| 127.9375 | 0 0111 1111 1111 | 07FF |
| 100 | 0 0110 0100 0000 | 0640 |
| 80 | 0 0101 0000 0000 | 0500 |
| 75 | 0 0100 1011 0000 | 04B0 |
| 50 | 0 0011 0010 0000 | 0320 |
| 25 | 0 0001 1001 0000 | 0190 |
| 0.25 | 0 0000 0000 0100 | 0004 |
| 0 | 0 0000 0000 0000 | 0000 |
| −0.25 | 1 1111 1111 1100 | 1FFC |
| −25 | 1 1110 0111 0000 | 1E70 |
| −55 | 1 1100 1001 0000 | 1C90 |

### 7.3.2 Serial Interface

The TMP102 device operates as a slave device only on the two-wire bus and SMBus. Connections to the bus are made through the open-drain I/O lines, SDA and SCL. The SDA and SCL pins feature integrated spike suppression filters and Schmitt triggers to minimize the effects of input spikes and bus noise. The TMP102 device supports the transmission protocol for both fast (1 kHz to 400 kHz) and high-speed (1 kHz to 2.85 MHz) modes. All data bytes are transmitted MSB first.

### 7.3.3 Bus Overview

The device that initiates the transfer is called a *master*, and the devices controlled by the master are called *slaves*. The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions.

To address a specific device, a START condition is initiated, indicated by pulling the data-line (SDA) from a high to low logic level when SCL is high. All slaves on the bus shift in the slave address byte on the rising edge of the clock, with the last bit indicating whether a read or write operation is intended. During the ninth clock pulse, the slave being addressed responds to the master by generating an acknowledge and by pulling SDA pin low.

A data transfer is then initiated and sent over eight clock pulses followed by an acknowledge bit. During the data transfer the SDA pin must remain stable when SCL is high, because any change in SDA pin when SCL pin is high is interpreted as a START signal or STOP signal.

When all data have been transferred, the master generates a STOP condition indicated by pulling SDA pin from low to high, when the SCL pin is high.

### 7.3.4 Serial Bus Address

To communicate with the TMP102, the master must first address slave devices via a slave address byte. The slave address byte consists of seven address bits, and a direction bit indicating the intent of executing a read or write operation.

The TMP102 features an address pin to allow up to four devices to be addressed on a single bus. Table 4 describes the pin logic levels used to properly connect up to four devices.

**Table 4. Address Pin and Slave Addresses**

| DEVICE TWO-WIRE ADDRESS | A0 PIN CONNECTION |
|---|---|
| 1001000 | Ground |
| 1001001 | V+ |
| 1001010 | SDA |
| 1001011 | SCL |

### 7.3.5  Writing and Reading Operation

Accessing a particular register on the TMP102 device is accomplished by writing the appropriate value to the pointer register. The value for the pointer register is the first byte transferred after the slave address byte with the R/$\overline{\text{W}}$ bit low. Every write operation to the TMP102 device requires a value for the pointer register (see Figure 8).

When reading from the TMP102 device, the last value stored in the pointer register by a write operation determines which register is read by a read operation. To change the register pointer for a read operation, a new value must be written to the pointer register. This action is accomplished by issuing a slave address byte with the R/$\overline{\text{W}}$ bit low, followed by the pointer register byte. No additional data are required. The master then generates a START condition and sends the slave address byte with the R/$\overline{\text{W}}$ bit high to initiate the read command. See Figure 7 for details of this sequence. If repeated reads from the same register are desired, continually sending the Pointer Register bytes is not necessary because the TMP102 remembers the Pointer Register value until it is changed by the next write operation.

Register bytes are sent with the most significant byte first, followed by the least significant byte.

### 7.3.6  Slave Mode Operations

The TMP102 can operate as a slave receiver or slave transmitter. As a slave device, the TMP102 never drives the SCL line.

#### 7.3.6.1  Slave Receiver Mode

The first byte transmitted by the master is the slave address, with the R/$\overline{\text{W}}$ bit low. The TMP102 then acknowledges reception of a valid address. The next byte transmitted by the master is the pointer register. The TMP102 then acknowledges reception of the pointer register byte. The next byte or bytes are written to the register addressed by the pointer register. The TMP102 acknowledges reception of each data byte. The master can terminate data transfer by generating a START or STOP condition..

#### 7.3.6.2  Slave Transmitter Mode

The first byte transmitted by the master is the slave address, with the R/$\overline{\text{W}}$ bit high. The slave acknowledges reception of a valid slave address. The next byte is transmitted by the slave and is the most significant byte of the register indicated by the pointer register. The master acknowledges reception of the data byte. The next byte transmitted by the slave is the least significant byte. The master acknowledges reception of the data byte. The master terminates data transfer by generating a *Not-Acknowledge* on reception of any data byte, or generating a START or STOP condition.

### 7.3.7  SMBus Alert Function

The TMP102 device supports the SMBus alert function. When the TMP102 device operates in Interrupt Mode (TM = 1), the ALERT pin can be connected as an SMBus alert signal. When a master senses that an ALERT condition is present on the ALERT line, the master sends an SMBus alert command (0001 1001) to the bus. If the ALERT pin is active, the device acknowledges the SMBus alert command and responds by returning the slave address on the SDA line. The eighth bit (LSB) of the slave address byte indicates if the ALERT condition was caused by the temperature exceeding $T_{HIGH}$ or falling below $T_{LOW}$. For POL = 0, the LSB is low if the temperature is greater than or equal to $T_{HIGH}$; this bit is high if the temperature is less than $T_{LOW}$. The polarity of this bit is inverted if POL = 1. See Figure 10 for details of this sequence.

If multiple devices on the bus respond to the SMBus alert command, arbitration during the slave address portion of the SMBus alert command determines which device clears the ALERT status. The device with the lowest two-wire address wins the arbitration. If the TMP102 device wins the arbitration, its ALERT pin inactivates at the completion of the SMBus alert command. If the TMP102 device loses the arbitration, its ALERT pin remains active.

### 7.3.8 General Call

The TMP102 device responds to a two-wire general call address (000 0000) if the eighth bit is 0. The device acknowledges the general call address and responds to commands in the second byte. If the second byte is 0000 0110, the TMP102 device internal registers are reset to power-up values. The TMP102 device does not support the general address acquire command.

### 7.3.9 High-Speed (HS) Mode

In order for the two-wire bus to operate at frequencies above 400 kHz, the master device must issue an HS-Mode master code (0000 1xxx) as the first byte after a START condition to switch the bus to high-speed operation. The TMP102 device does not acknowledge this byte, but switches the input filters on SDA and SCL and the output filters on SDA to operate in HS-mode, allowing transfers of up to 2.85 MHz. After the HS-Mode master code has been issued, the master transmits a two-wire slave address to initiate a data transfer operation. The bus continues to operate in HS-Mode until a STOP condition occurs on the bus. Upon receiving the STOP condition, the TMP102 device switches the input and output filters back to fast-mode operation..

### 7.3.10 Timeout Function

The TMP102 device resets the serial interface if SCL is held low for 30 ms (typ) between a start and stop condition. The TMP102 device releases the SDA line if the SCL pin is pulled low and waits for a start condition from the host controller. To avoid activating the time-out function, maintaining a communication speed of at least 1 kHz for SCL operating frequency is necessary..

### 7.3.11 Timing Diagrams

The TMP102 device is two-wire, SMBus, and $I^2C$-interface compatible. Figure 7, Figure 8, Figure 9, and Figure 10 list the various operations on the TMP102 device. Parameters for Figure 7 are defined in the *Timing Requirements* table. The bus definitions are defined as follows:
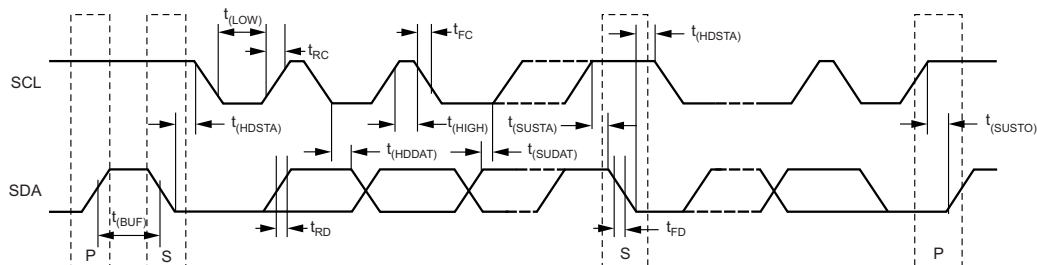
**Acknowledge** Each receiving device, when addressed, is obliged to generate an acknowledge bit. A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the Acknowledge clock pulse. Setup and hold times must be taken into account. On a master receive, the termination of the data transfer can be signaled by the master generating a *not-acknowledge* (1) on the last byte that has been transmitted by the slave.

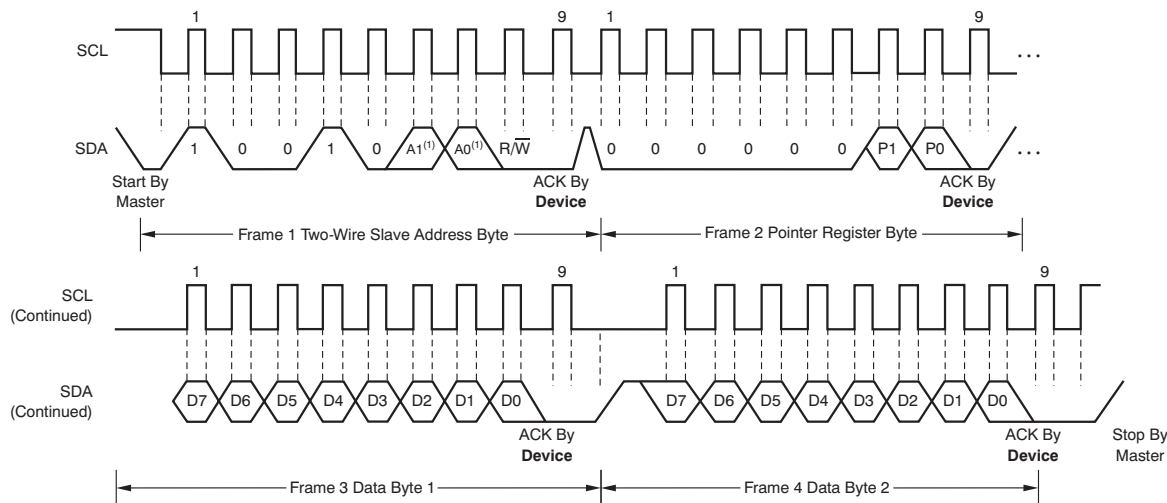**Bus Idle** Both SDA and SCL lines remain high.

**Data Transfer** The number of data bytes transferred between a START and a STOP condition is not limited and is determined by the master device. The TMP102 device can also be used for single byte updates. To update only the MS byte, terminate the communication by issuing a START or STOP communication on the bus.

**Start Data Transfer** A change in the state of the SDA line, from high to low, when the SCL line is high, defines a START condition. Each data transfer is initiated with a START condition.

**Stop Data Transfer** A change in the state of the SDA line from low to high when the SCL line is high defines a STOP condition. Each data transfer is terminated with a repeated START or STOP condition.



**Figure 7. Two-Wire Timing Diagram**

NOTE: (1) The value of A0 and A1 are determined by the ADD0 pin.

**Figure 8. Two-Wire Timing Diagram for Write Word Format**



NOTE: (1) The value of A0 and A1 are determined by the ADD0 pin.
(2) Master should leave SDA high to terminate a single-byte read operation.
(3) Master should leave SDA high to terminate a two-byte read operation.
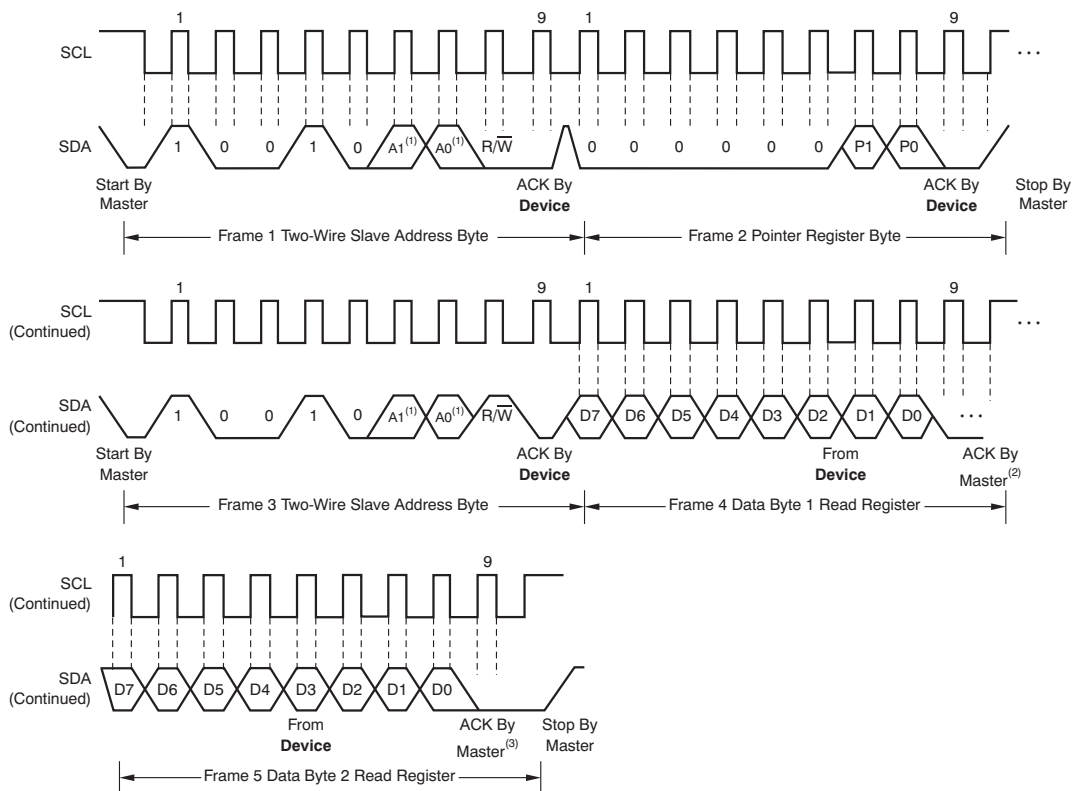
**Figure 9. Two-Wire Timing Diagram for Read Word Format**

NOTE: (1) The value of A0 and A1 are determined by the ADD0 pin.
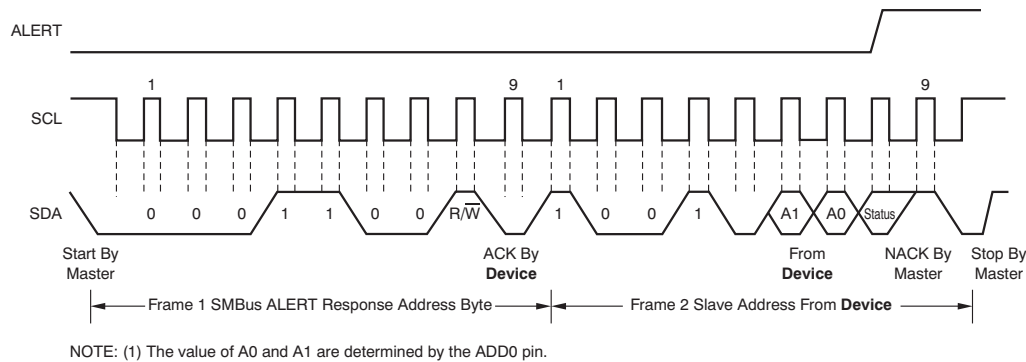
**Figure 10. Timing Diagram for SMBus Alert**

## 7.4 Device Functional Modes

### 7.4.1 Continuos-Conversion Mode

The default mode of the TMP102 device is continuos conversion mode. During continuos-conversion mode, the ADC performs continuos temperature conversions and stores each results to the temperature register, overwriting the result from the previous conversion. The conversion rate bits, CR1 and CR0, configure the TMP102 device for conversion rates of 0.25 Hz, 1 Hz, 4 Hz, or 8 Hz. The default rate is 4 Hz. The TMP102 device has a typical conversion time of 26 ms. To achieve different conversion rates, the TMP102 device makes a conversion and then powers down to wait for the appropriate delay set by CR1 and CR0. Table 5 lists the settings for CR1 and CR0.

**Table 5. Conversion Rate Settings**

| CR1 | CR0 | CONVERSION RATE |
|-----|-----|-----------------|
| 0 | 0 | 0.25 Hz |
| 0 | 1 | 1 Hz |
| 1 | 0 | 4 Hz (default) |
| 1 | 1 | 8 Hz |

After power-up or general-call reset, the TMP102 immediately starts a conversion, as shown in Figure 11. The first result is available after 26 ms (typical). The active quiescent current during conversion is 40 μA (typical at +27°C). The quiescent current during delay is 2.2 μA (typical at +27°C).
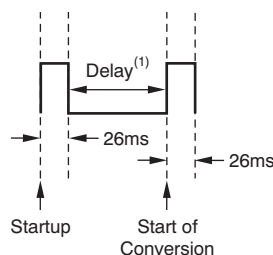


(1)  Delay is set by CR1 and CR0.

**Figure 11. Conversion Start**

### 7.4.2 Extended Mode (EM)

The Extended-Mode bit configures the device for Normal mode operation (EM = 0) or Extended mode operation (EM = 1). In Normal mode, the Temperature Register and high- and low-limit registers use a 12-bit data format. Normal mode is used to make the TMP102 device compatible with the TMP75 device.

Extended mode (EM = 1) allows measurement of temperatures above 128°C by configuring the Temperature Register, and high- and low-limit registers for 13-bit data format.

### 7.4.3 Shutdown Mode (SD)

The Shutdown-mode bit saves maximum power by shutting down all device circuitry other than the serial interface, reducing current consumption to typically less than 0.5 μA. Shutdown mode enables when the SD bit is 1; the device shuts down when current conversion is completed. When SD is equal to 0, the device maintains a continuous conversion state.

### 7.4.4 One-Shot/Conversion Ready (OS)

The TMP102 device features a one-shot temperature measurement mode. When the device is in Shutdown Mode, writing a 1 to the OS bit starts a single temperature conversion. During the conversion, the OS bit reads '0'. The device returns to the shutdown state at the completion of the single conversion. After the conversion, the OS bit reads 1. This feature reduces power consumption in the TMP102 device when continuous temperature monitoring is not required.

As a result of the short conversion time, the TMP102 device achieves a higher conversion rate. A single conversion typically takes 26 ms and a read can take place in less than 20 μs. When using One-Shot Mode, 30 or more conversions per second are possible.

### 7.4.5 Thermostat Mode (TM)

The thermostat-mode bit indicates to the device whether to operate in comparator mode (TM = 0) or Interrupt mode (TM = 1).

#### 7.4.5.1 Comparator Mode (TM = 0)

In Comparator mode (TM = 0), the Alert pin is activated when the temperature equals or exceeds the value in the $T_{(HIGH)}$ register and remains active until the temperature falls below the value in the $T_{(LOW)}$ register. For more information on the comparator mode, see the *High- and Low-Limit Registers* section.

#### 7.4.5.2 Interrupt Mode (TM = 1)

In Interrupt mode (TM = 1), the Alert pin is activated when the temperature exceeds $T_{(HIGH)}$ or goes below $T_{(LOW)}$ registers. The Alert pin is cleared when the host controller reads the temperature register. For more information on the interrupt mode, see the *High- and Low-Limit Registers* section.

## 7.5 Programming

### 7.5.1 Pointer Register

Figure 12 illustrates the internal register structure of the TMP102 device. The 8-bit Pointer Register of the device is used to address a given data register. The Pointer Register uses the two least-significant bytes (LSBs) (see Table 15 and Table 16) to identify which of the data registers must respond to a read or write command. Table 6 identifies the bits of the Pointer Register byte. During a write command, P2 through P7 must always be '0'. Table 7 describes the pointer address of the registers available in the TMP102 device. The power-up reset value of P1 and P0 is 00. By default, the TMP102 device reads the temperature on power up.

## Programming (continued)
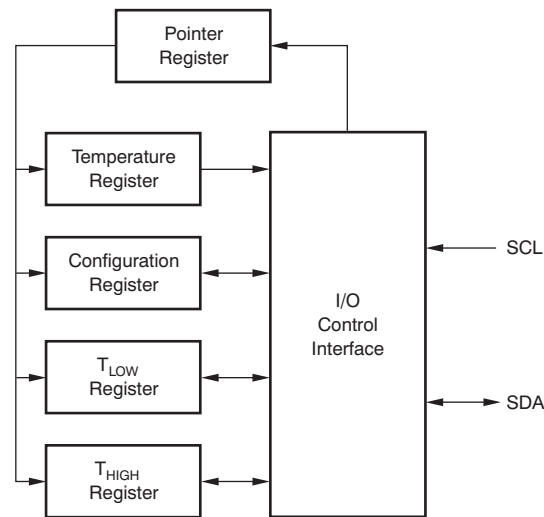


**Figure 12. Internal Register Structure**

**Table 6. Pointer Register Byte**

| P7 | P6 | P5 | P4 | P3 | P2 | P1 | P0 |
|----|----|----|----|----|----|----|----|
| 0 | 0 | 0 | 0 | 0 | 0 | Register Bits | |

**Table 7. Pointer Addresses**

| P1 | P0 | REGISTER |
|----|----|----------|
| 0 | 0 | Temperature Register (Read Only) |
| 0 | 1 | Configuration Register (Read/Write) |
| 1 | 0 | $T_{LOW}$ Register (Read/Write) |
| 1 | 1 | $T_{HIGH}$ Register (Read/Write) |

### 7.5.2 Temperature Register

The Temperature Register of the TMP102 is configured as a 12-bit, read-only register (Configuration Register EM bit = 0, see the *Extended Mode* section), or as a 13-bit, read-only register (Configuration Register EM bit = 1) that stores the output of the most recent conversion. Two bytes must be read to obtain data, and are described in Table 8 and Table 9. Note that byte 1 is the most significant byte, followed by byte 2, the least significant byte. The first 12 bits (13 bits in Extended mode) are used to indicate temperature. The least significant byte does not have to be read if that information is not needed.

**Table 8. Byte 1 of Temperature Register[1]**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
| T11 | T10 | T9 | T8 | T7 | T6 | T5 | T4 |
| (T12) | (T11) | (T10) | (T9) | (T8) | (T7) | (T6) | (T5) |

(1) Extended mode 13-bit configuration shown in parenthesis.

**Table 9. Byte 2 of Temperature Register[1]**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
| T3 | T2 | T1 | T0 | 0 | 0 | 0 | 0 |
| (T4) | (T3) | (T2) | (T1) | (T0) | (0) | (0) | (1) |

(1)   Extended mode 13-bit configuration shown in parenthesis.

### 7.5.3   Configuration Register

The Configuration Register is a 16-bit read/write register used to store bits that control the operational modes of the temperature sensor. Read/write operations are performed MSB first. Table 10 and Table 11 list the format and the power-up or reset value of the configuration register. For compatibility, Table 10 and Table 11 correspond to the configuration register in the TMP75 device and TMP275 device (for more information see the device data sheets, SBOS288 and SBOS363, respectively). All registers are updated byte by byte.

**Table 10. Byte 1 of Configuration and Power-Up or Reset Format**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
| OS | R1 | R0 | F1 | F0 | POL | TM | SD |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

**Table 11. Byte 2 of Configuration and Power-Up or Reset Format**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
| CR1 | CR0 | AL | EM | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |

#### 7.5.3.1   Shutdown Mode (SD)

The Shutdown-mode bit saves maximum power by shutting down all device circuitry other than the serial interface, reducing current consumption to typically less than 0.5 $\mu$A. Shutdown mode enables when the SD bit is 1; the device shuts down when current conversion is completed. When SD is equal to 0, the device maintains a continuous conversion state

#### 7.5.3.2   Thermostat Mode (TM)

The Thermostat mode bit indicates to the device whether to operate in Comparator mode (TM = 0) or Interrupt mode (TM = 1). For more information on comparator and interrupt modes, see the *High- and Low-Limit Registers* section.

#### 7.5.3.3   Polarity (POL)

The polarity bit allows the user to adjust the polarity of the ALERT pin output. If the POL bit is set to 0 (default), the ALERT pin becomes active low. When the POL bit is set to 1, the ALERT pin becomes active high and the state of the ALERT pin is inverted. The operation of the ALERT pin in various modes is illustrated in Figure 13.
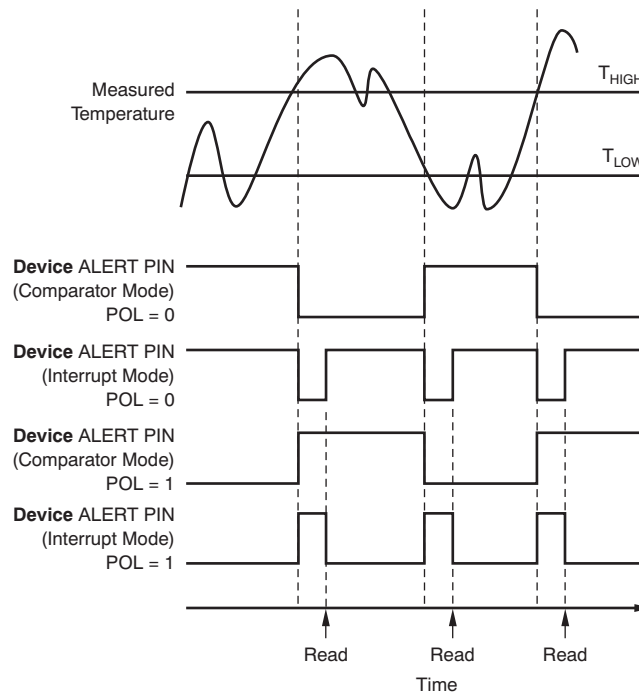
**Figure 13. Output Transfer Function Diagrams**

### 7.5.3.4 Fault Queue (F1/F0)

A fault condition exists when the measured temperature exceeds the user-defined limits set in the $T_{HIGH}$ and $T_{LOW}$ registers. Additionally, the number of fault conditions required to generate an alert may be programmed using the fault queue. The fault queue is provided to prevent a false alert as a result of environmental noise. The fault queue requires consecutive fault measurements in order to trigger the alert function. Table 12 defines the number of measured faults that may be programmed to trigger an alert condition in the device. For $T_{HIGH}$ and $T_{LOW}$ register format and byte order, see the *High- and Low-Limit Registers* section.

**Table 12. TMP102 Fault Settings**

| F1 | F0 | CONSECUTIVE FAULTS |
|----|----|--------------------|
| 0 | 0 | 1 |
| 0 | 1 | 2 |
| 1 | 0 | 4 |
| 1 | 1 | 6 |

### 7.5.3.5 Converter Resolution (R1/R0)

The converter resolution bits, R1 and R0, are read-only bits. The TMP102 converter resolution is set at device start-up to 11 which sets the temperature register to a 12 bit-resolution.

### 7.5.3.6 One-Shot (OS)

When the device is in Shutdown Mode, writing a 1 to the OS bit starts a single temperature conversion. During the conversion, the OS bit reads '0'. The device returns to the shutdown state at the completion of the single conversion. For more information on the one-shot conversion mode, see the *One-Shot/Conversion Ready (OS)* section.

### 7.5.3.7 EM Bit

The Extended-Mode bit configures the device for Normal Mode operation (EM = 0) or Extended Mode operation (EM = 1). In normal mode, the temperature register, high-limit register, and low-limit register use a 12-bit data format. For more information on the extended mode, see the *Extended Mode (EM)* section.

### 7.5.3.8 Alert (AL Bit)

The AL bit is a read-only function. Reading the AL bit provides information about the comparator mode status. The state of the POL bit inverts the polarity of data returned from the AL bit. When the POL bit equals 0, the AL bit reads as 1 until the temperature equals or exceeds $T_{(HIGH)}$ for the programmed number of consecutive faults, causing the AL bit to read as 0. The AL bit continues to read as 0 until the temperature falls below $T_{(LOW)}$ for the programmed number of consecutive faults, when it again reads as 1. The status of the TM bit does not affect the status of the AL bit..

### 7.5.3.9 Conversion Rate (CR)

The conversion rate bits, CR1 and CR0, configure the TMP102 device for conversion rates of 0.25 Hz, 1 Hz, 4 Hz, or 8 Hz. The default rate is 4 Hz. For more information on the conversion rate bits, see Table 5.

### 7.5.4 High- and Low-Limit Registers

The temperature limits are stored in the $T_{(LOW)}$ and $T_{(HIGH)}$ registers in the same format as the temperature result, and their values are compared to the temperature result on every conversion. The outcome of the comparison drives the behavior of the ALERT pin, which operates as a comparator output or an interrupt, and is set by the TM bit in the configuration register.

In Comparator mode (TM = 0), the ALERT pin becomes active when the temperature equals or exceeds the value in $T_{HIGH}$ and generates a consecutive number of faults according to fault bits F1 and F0. The ALERT pin remains active until the temperature falls below the indicated $T_{LOW}$ value for the same number of faults.

In Interrupt mode (TM = 1), the ALERT pin becomes active when the temperature equals or exceeds the value in $T_{HIGH}$ for a consecutive number of fault conditions (as shown in Table 5). The ALERT pin remains active until a read operation of any register occurs, or the device successfully responds to the SMBus Alert Response address. The ALERT pin will also be cleared if the device is placed in Shutdown mode. When the ALERT pin is cleared, it becomes active again only when temperature falls below $T_{LOW}$, and remains active until cleared by a read operation of any register or a successful response to the SMBus Alert Response address. When the ALERT pin is cleared, the above cycle repeats, with the ALERT pin becoming active when the temperature equals or exceeds $T_{HIGH}$. The ALERT pin can also be cleared by resetting the device with the General Call Reset command. This action also clears the state of the internal registers in the device, returning the device to Comparator mode (TM = 0).

Both operational modes are represented in Figure 13. Table 13 through Table 16 describe the format for the $T_{HIGH}$ and $T_{LOW}$ registers. Note that the most significant byte is sent first, followed by the least significant byte. Power-up reset values for $T_{HIGH}$ and $T_{LOW}$ are: $T_{HIGH}$ = +80°C and $T_{LOW}$ = +75°C. The format of the data for $T_{HIGH}$ and $T_{LOW}$ is the same as for the Temperature Register.

**Table 13. Byte 1 Temperature Register $_{HIGH}$[1]**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
| H11 | H10 | H9 | H8 | H7 | H6 | H5 | H4 |
| (H12) | (H11) | (H10) | (H9) | (H8) | (H7) | (H6) | (H5) |

(1)    Extended mode 13-bit configuration shown in parenthesis.

**Table 14. Byte 2 Temperature Register $_{HIGH}$**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
| H3 | H2 | H1 | H0 | 0 | 0 | 0 | 0 |
| (H4) | (H3) | (H2) | (H1) | (H0) | (0) | (0) | (0) |

**Table 15. Byte 1 Temperature Register $_{LOW}$[1]**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
| L11 | L10 | L9 | L8 | L7 | L6 | L5 | L4 |
| (L12) | (L11) | (L10) | (L9) | (L8) | (L7) | (L6) | (L5) |

(1)    Extended mode 13-bit configuration shown in parenthesis.

#### Table 16. Byte 2 Temperature Register LOW

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|:--:|:--:|:--:|:--:|:--:|:--:|:--:|:--:|
| L3 | L2 | L1 | L0 | 0 | 0 | 0 | 0 |
| (L4) | (L3) | (L2) | (L1) | (L0) | (0) | (0) | (0) |

# 8 Application and Implementation

## 8.1 Application Information

The TMP102 device is used to measure the PCB temperature of the board location where the device is mounted. The programmable address options allow up to four locations on the board to be monitored on a single serial bus.

## 8.2 Typical Application
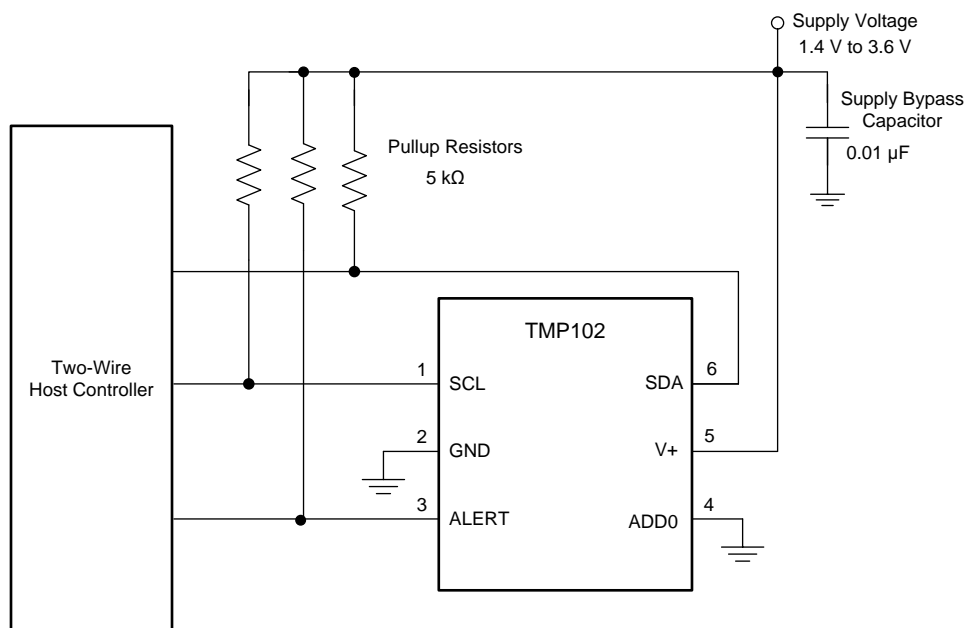


**Figure 14. Typical Connections**

### 8.2.1 Design Requirements

The TMP102 device requires pullup resistors on the SCL, SDA, and ALERT pins. The recommended value for the pullup resistors is 5-kΩ. In some applications the pullup resistor can be lower or higher than 5 kΩ but must not exceed 3 mA of current on any of those pins. A 0.01-μF bypass capacitor on the supply is recommended as shown in Figure 14. The SCL and SDA lines can be pulled up to a supply that is equal to or higher than V+ through the pullup resistors. To configure one of four different addresses on the bus, connect the ADD0 pin to either the GND, V+, SDA, or SCL pin.

### 8.2.2 Detailed Design Procedure

Place the TMP102 device in close proximity to the heat source that must be monitored, with a proper layout for good thermal coupling. This placement ensures that temperature changes are captured within the shortest possible time interval. To maintain accuracy in applications that require air or surface temperature measurement, care must be taken to isolate the package and leads from ambient air temperature. A thermally-conductive adhesive is helpful in achieving accurate surface temperature measurement.

## Typical Application (continued)

The TMP102 device is a very low-power device and generates very low noise on the supply bus. Applying an RC filter to the V+ pin of the TMP102 device can further reduce any noise that the TMP102 device might propagate to other components. $R_{(F)}$ in Figure 15 must be less than 5 kΩ and $C_{(F)}$ must be greater than 10 nF.
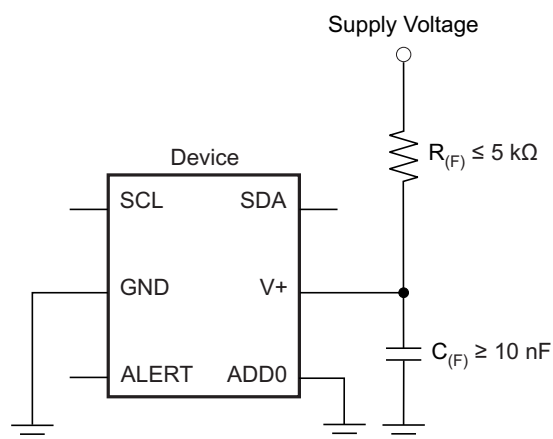


**Figure 15.  Noise Reduction Techniques**

### 8.2.3  Application Curve

Figure 16 shows the step response of the TMP102 device to a submersion in an oil bath of 100ºC from room temperature (27ºC). The time-constant, or the time for the output to reach 63% of the input step, is 0.8 s. The time-constant result depends on the printed circuit board (PCB) that the TMP102 device is mounted. For this test, the TMP102 device was soldered to a two-layer PCB that measured 0.375 inch × 0.437 inch.
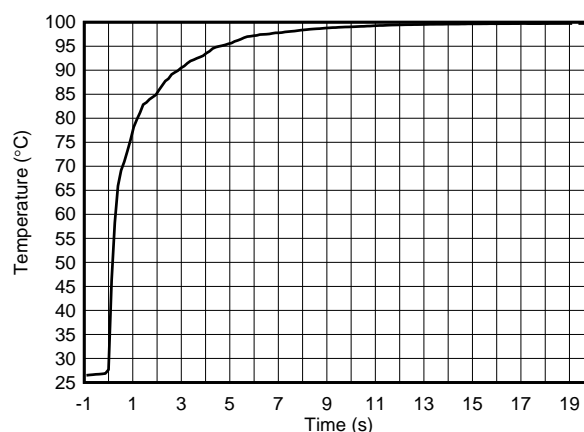


**Figure 16. Temperature Step Response**

# 9 Power Supply Recommendations

The TMP102 device operates with power supply in the range of 1.4 to 3.6 V. The device is optimized for operation at 3.3-V supply but can measure temperature accurately in the full supply range.

A power-supply bypass capacitor is required for proper operation. Place this capacitor as close as possible to the supply and ground pins of the device. A typical value for this supply bypass capacitor is 0.01 μF. Applications with noisy or high-impedance power supplies may require additional decoupling capacitors to reject power-supply noise.

# 10 Layout

## 10.1 Layout Guidelines

Place the power-supply bypass capacitor as close as possible to the supply and ground pins. The recommended value of this bypass capacitor is 0.01 μF. Additional decoupling capacitance can be added to compensate for noisy or high-impedance power supplies. Pull up the open-drain output pins (SDA , SCL and ALERT) through 5-kΩ pullup resistors.
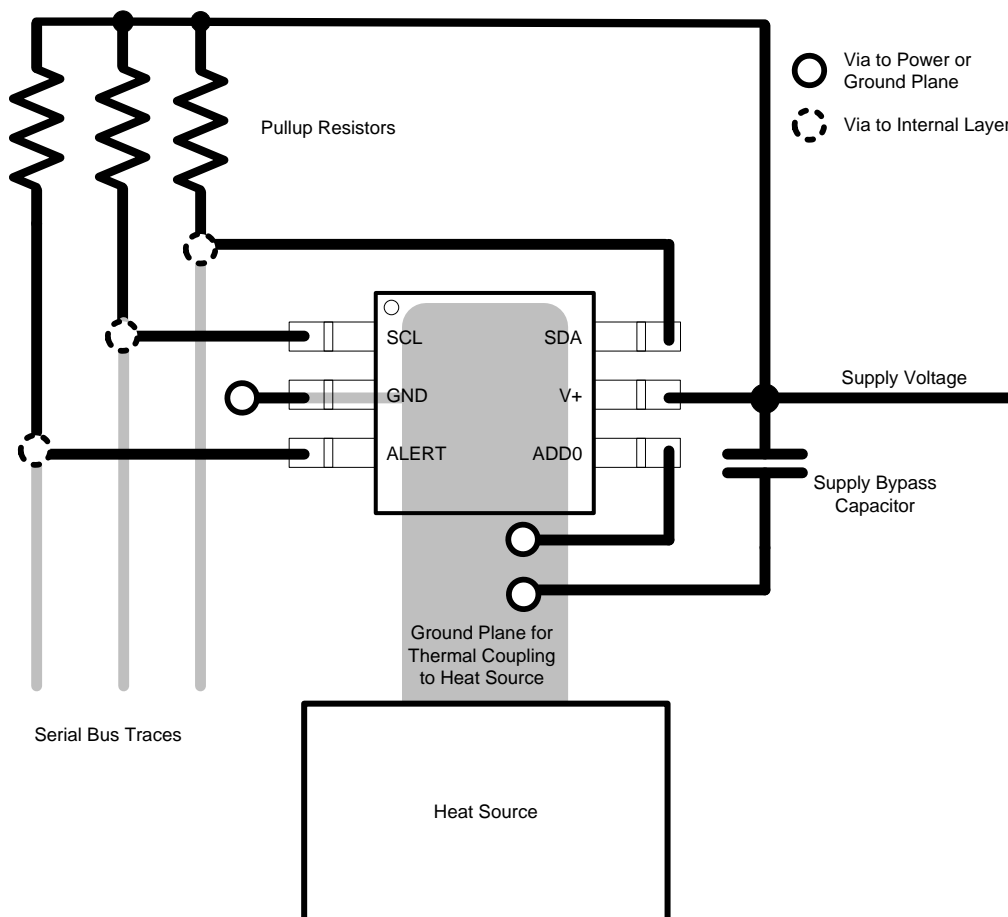
## 10.2 Layout Example



**Figure 17. TMP102 Layout Example**

## 11 器件和文档支持

### 11.1 文档支持

#### 11.1.1 相关文档

请参阅如下相关文档：

- TMP175、TMP75 产品说明书，SBOS288
- TMP275 产品说明书，SBOS363
- *具有触觉反馈的电容触控式汽车 LED 座舱顶灯*设计指南

### 11.2 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 11.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商"按照原样"提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

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### 11.5 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

### 11.6 术语表

SLYZ022 — *TI 术语表。*

这份术语表列出并解释术语、缩写和定义。

## 12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TMP102AIDRLR | ACTIVE | SOT-5X3 | DRL | 6 | 4000 | RoHS & Green | NIPDAU \| NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | CBZ | Samples |
| TMP102AIDRLRG4 | LIFEBUY | SOT-5X3 | DRL | 6 | 4000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CBZ | |
| TMP102AIDRLT | LIFEBUY | SOT-5X3 | DRL | 6 | 250 | RoHS & Green | NIPDAU \| NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | CBZ | |
| TMP102AIDRLTG4 | LIFEBUY | SOT-5X3 | DRL | 6 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CBZ | |

**(1)** The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

**(2) RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF TMP102 :**

● Automotive : TMP102-Q1

NOTE: Qualified Version Definitions:

     ● Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

# PACKAGE MATERIALS INFORMATION

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

**TAPE DIMENSIONS**



| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**
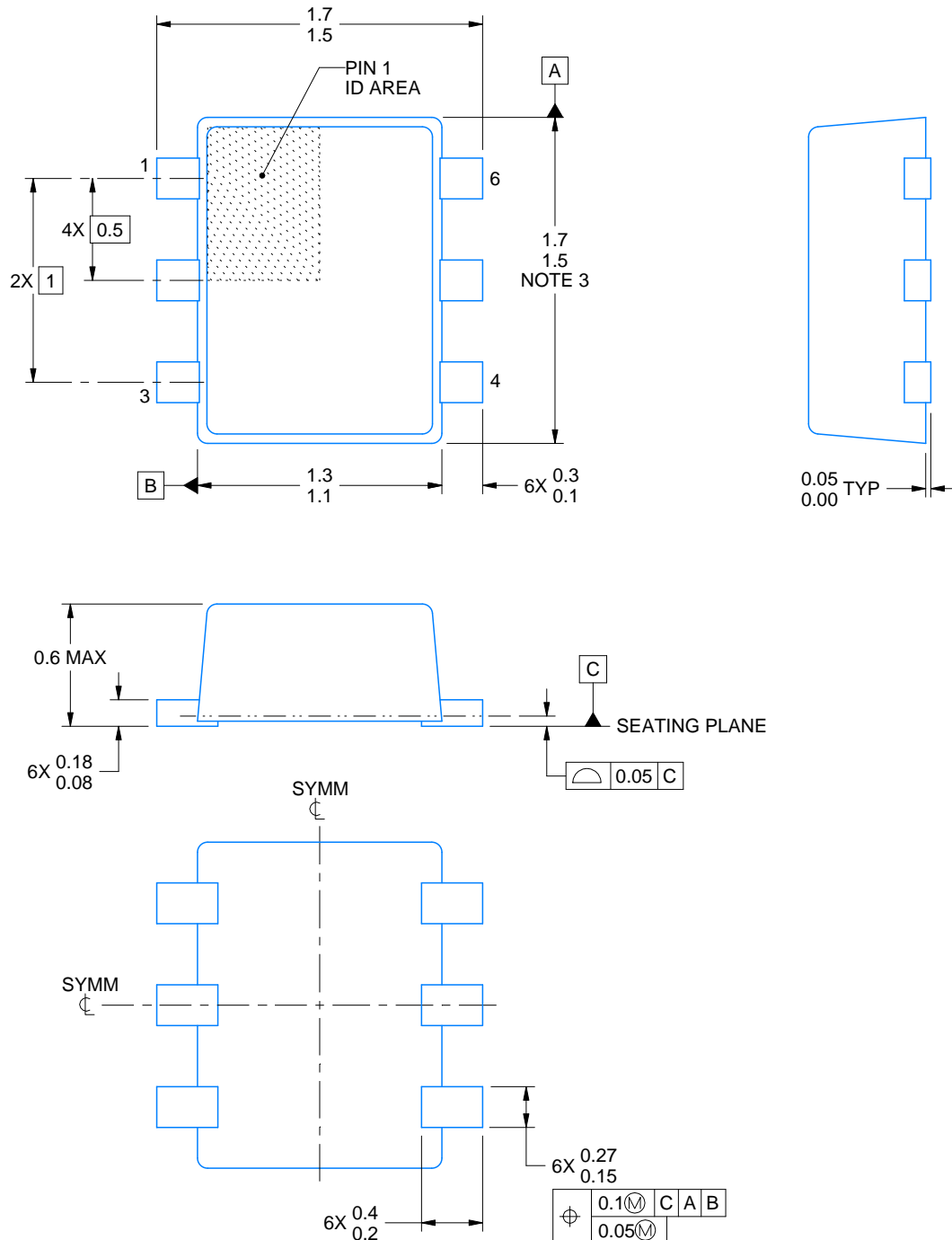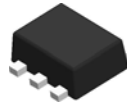


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------|-------------|----------------|------|-----|-------------------|-------------------|---------|---------|---------|---------|--------|---------------|
| TMP102AIDRLR | SOT-5X3 | DRL | 6 | 4000 | 180.0 | 8.4 | 2.0 | 1.8 | 0.75 | 4.0 | 8.0 | Q3 |
| TMP102AIDRLR | SOT-5X3 | DRL | 6 | 4000 | 180.0 | 8.4 | 1.98 | 1.78 | 0.69 | 4.0 | 8.0 | Q3 |
| TMP102AIDRLT | SOT-5X3 | DRL | 6 | 250 | 180.0 | 8.4 | 1.98 | 1.78 | 0.69 | 4.0 | 8.0 | Q3 |
| TMP102AIDRLT | SOT-5X3 | DRL | 6 | 250 | 180.0 | 8.4 | 2.0 | 1.8 | 0.75 | 4.0 | 8.0 | Q3 |

# PACKAGE MATERIALS INFORMATION

**TAPE AND REEL BOX DIMENSIONS**



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TMP102AIDRLR | SOT-5X3 | DRL | 6 | 4000 | 210.0 | 185.0 | 35.0 |
| TMP102AIDRLR | SOT-5X3 | DRL | 6 | 4000 | 202.0 | 201.0 | 28.0 |
| TMP102AIDRLT | SOT-5X3 | DRL | 6 | 250 | 202.0 | 201.0 | 28.0 |
| TMP102AIDRLT | SOT-5X3 | DRL | 6 | 250 | 210.0 | 185.0 | 35.0 |

PIN 1
ID AREA

1.7
1.5

A

1
4X 0.5

2X 1

3

1.7
1.5
NOTE 3

6

4

B

1.3
1.1

6X 0.3
0.1

0.05
0.00 TYP

0.6 MAX

C

SEATING PLANE

6X 0.18
0.08

0.05 C

SYMM

SYMM

6X 0.27
0.15

6X 0.4
0.2

⊕ | 0.1 Ⓜ | C | A | B
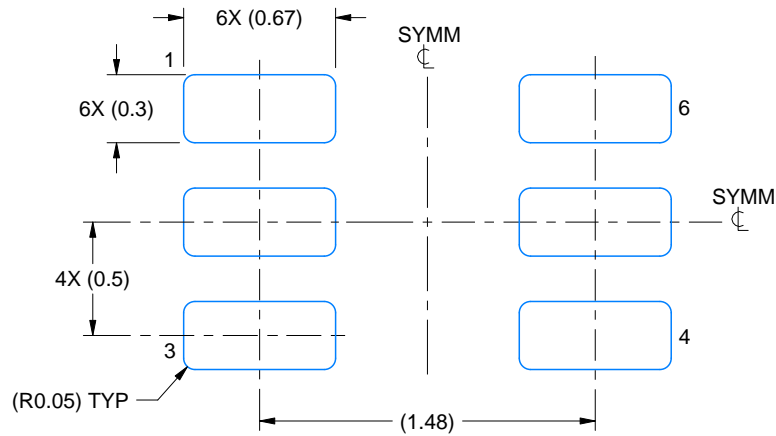0.05 Ⓜ

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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
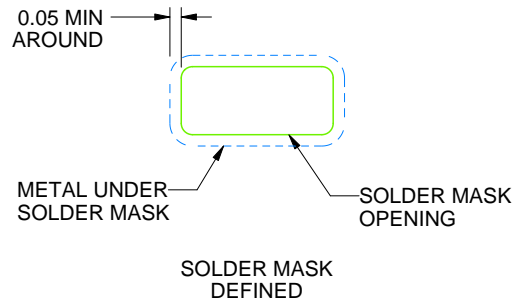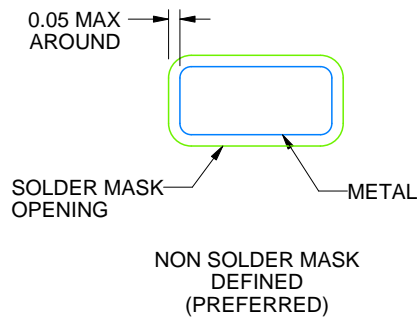4. Reference JEDEC registration MO-293 Variation UAAD

6X (0.67)

SYMM
℄

1

6X (0.3)

6

SYMM
℄

4X (0.5)

3

(R0.05) TYP

4

(1.48)

**LAND PATTERN EXAMPLE**
SCALE:30X

0.05 MAX
AROUND

SOLDER MASK
OPENING

METAL

**NON SOLDER MASK
DEFINED
(PREFERRED)**

0.05 MIN
AROUND

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

**SOLDER MASK
DEFINED**

**SOLDERMASK DETAILS**

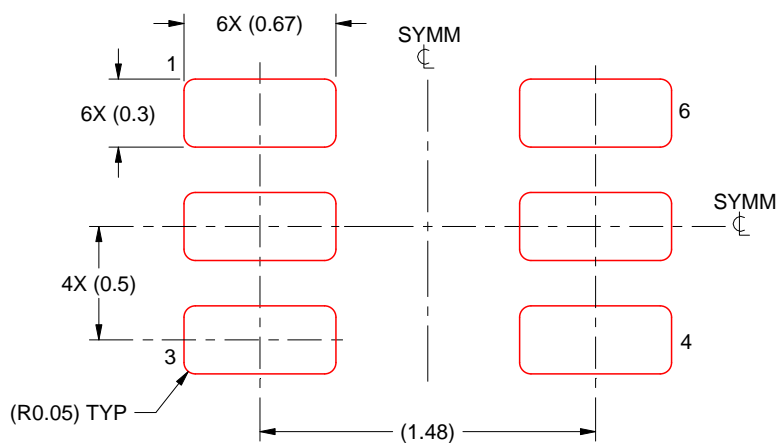4223266/C   12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.

6X (0.67)

1

6X (0.3)

6

SYMM

4X (0.5)

SYMM

3

4

(R0.05) TYP

(1.48)

SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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