

# 具有 PowerPath 的 BQ2407x 独立型 1 节电池、1.5A 线性电池充电器

## 1 特性

- 完全符合 USB 充电器标准
  - 最大输入电流可选 100mA 和 500mA
  - 100mA 最大电流限制可确保充电符合 USB-IF 标准
  - 基于输入的动态电源管理 ( $V_{IN}$ -DPM), 用于保护免受不良 USB 电源损害
- 28V 输入额定值, 具有过压保护功能
- 集成动态电源路径管理 (DPPM) 功能可同时独立进行系统供电和对电池充电
- 借助电流监控输出 (ISET) 功能可支持高达 1.5A 的充电电流
- 针对墙上适配器的高达 1.5A 的可编程输入电流限制
- 系统输出跟踪电池电压 (bq24072)
- 可编程终端电流 (bq24074)
- 通过 SYSOFF 输入实现的电池断开功能 (bq24075、bq24079)
- 可编程预充电和快速充电安全计时器
- 反向电流、短路和热保护
- NTC 热敏电阻输入
- 专有启动序列可限制浪涌电流
- 具有充电中/充电完成和电源正常状态指示

## 2 应用

- 智能手机
- 便携式媒体播放器
- 便携式导航设备
- 低功耗手持设备

## 3 说明

BQ2407x 系列器件是集成型锂离子线性充电器和系统电源路径管理器件, 适用于空间受限的便携式应用。这类器件通过 USB 端口或交流适配器运行, 最高支持 1.5A 的充电电流。它们在输入电压范围内具有输入电压保护功能, 因此支持非稳压适配器。BQ2407x 的 USB 输入电流限制精度和启动序列使得这款器件能够符合 USB-IF 浪涌电流规范。此外, 输入动态电源管理 ( $V_{IN}$ -DPM) 可防止充电器损毁错误配置的 USB 电源。

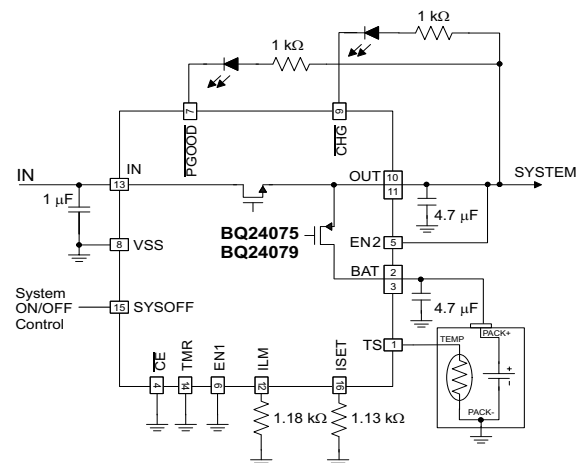
BQ2407x 具有 动态电源路径管理 (DPPM) 功能, 可在系统供电的同时独立为电池充电。当输入电流限制引起系统输出降至 DPPM 阈值时, DPPM 电路将减少充电电流; 因此, 可在系统负载供电时随时监测充电电流。这个特性减少了电池上充放电周期的数量, 可实现充电正常终止并使得系统能够在由有缺陷或者不完整的电池组供电的情况下运行。

器件信息(1)

器件型号	封装	封装尺寸 (标称值)
BQ24072	VQFN (16)	3.00mm x 3.00mm
BQ24073		
BQ24074		
BQ24075		
BQ24079		

(1) 如需了解所有可用封装, 请参阅产品说明书末尾的可订购产品附录。

典型应用电路



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## 4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

<b>Changes from Revision L (June 2018) to Revision M</b>	<b>Page</b>
• 更改了文档标题.....	<b>1</b>
• Changed the <i>Device Comparison Table</i> .....	<b>5</b>
• Deleted the <i>Dissipation Ratings</i> table.....	<b>10</b>
• Changed $V_{IN-LOW}$ To $V_{IN-DPM}$ in the <i>Functional Block Diagram</i> .....	<b>16</b>
• Changed text From: "the DPPM loop or the $V_{IN-LOW}$ loop." To: "the DPPM loop or the $V_{IN-DPM}$ loop." in the <i>Battery Charging</i> section.....	<b>23</b>
• Changed text From: "input voltage has fallen to $V_{IN-LOW}$ " To: "input voltage has fallen to $V_{IN-DPM}$ " in the <i>Dynamic Charge Timers (TMR Input)</i> section .....	<b>26</b>
• Changed <a href="#">Equation 11</a> .....	<b>39</b>

<b>Changes from Revision K (March 2015) to Revision L</b>	<b>Page</b>
• Deleted MARKINGS from the <i>Device Comparison Table</i> .....	<b>5</b>
• Added the RGT0016B and RGT0016C package information to the <i>Device Comparison Table</i> .....	<b>5</b>
• Changed the Pinout images and descriptions .....	<b>6</b>
• Change description of the $\overline{CE}$ pin From: "Connect $\overline{CE}$ to a high logic level to place the battery charger in standby mode. In standby mode,..." To: "Connect $\overline{CE}$ to a high logic level to disable battery charging. OUT is active and battery supplement mode is still available." .....	<b>7</b>
• "Changed text in the third paragraph of the <i>Power On</i> section From: When $V_{OUT}$ is above $V_{SC}$ ,..." To: "When $V_{OUT}$ is above $V_{Q(SC1)}$ ,..." .....	<b>17</b>
• Changed text From: "The valid resistor range is 590 $\Omega$ to 5.9 k $\Omega$ ." To: "The valid resistor range is 590 $\Omega$ to 8.9 k $\Omega$ ." in the <i>Battery Charging</i> section .....	<b>23</b>
• Changed From: $V_{IN(DT)}$ To: $V_{BAT} + V_{IN(DT)}$ in <a href="#">Table 2</a> .....	<b>26</b>
• Changed $I_{NTC}$ To: $I_{TS}$ in <a href="#">Figure 24</a> .....	<b>28</b>

<b>Changes from Revision J (January 2015) to Revision K</b>	<b>Page</b>
<ul style="list-style-type: none"> <li>Deleted package type code from Device Comparison Table. See the POA at the end of the data sheet. ....</li> <li>Changed <math>I_{CHG}</math> Battery fast charge current range MIN specification from "150 mA" to "100 mA" .....</li> </ul>	5 11
<b>Changes from Revision I (January 2014) to Revision J</b>	<b>Page</b>
<ul style="list-style-type: none"> <li>已添加 ESD 额定值 表, 特性 说明 部分、器件功能模式、应用和实施 部分、电源相关建议 部分、布局 部分、器件和文档支持 部分以及机械、封装和可订购信息 部分 .....</li> </ul>	1
<b>Changes from Revision H (December 2013) to Revision I</b>	<b>Page</b>
<ul style="list-style-type: none"> <li>Changed resistor value from "3 k<math>\Omega</math>" to "8.9 k<math>\Omega</math>" in the Pin Functions table ISET Description paragraph.....</li> <li>Changed <math>R_{ISET}</math> spec MAX value from "3000" to "8900" in the Recommended Operating Conditions table. ....</li> <li>Changed resistor value from "3 k<math>\Omega</math>" to "5.9 k<math>\Omega</math>" in the <i>Battery Charging</i> section paragraph. ....</li> </ul>	7 8 23
<b>Changes from Revision G (July 2011) to Revision H</b>	<b>Page</b>
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<b>Changes from Revision F (September 2010) to Revision G</b>	<b>Page</b>
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<b>Changes from Revision E (August 2010) to Revision F</b>	<b>Page</b>
<ul style="list-style-type: none"> <li>Changed 10 x 45 s/k<math>\Omega</math> to 10 x 48 s/k<math>\Omega</math> under section Program 6.25hour.....(TMR) .....</li> </ul>	32
<b>Changes from Revision D (June 2009) to Revision E</b>	<b>Page</b>
<ul style="list-style-type: none"> <li>Changed globally RT1 and RT2 to Rs and Rp.....</li> <li>Added equations 2 and 3 plus explanations and table.....</li> </ul>	27 27
<b>Changes from Revision C (March 2009) to Revision D</b>	<b>Page</b>
<ul style="list-style-type: none"> <li>已添加 器件型号 bq24079。 .....</li> </ul>	1
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<ul style="list-style-type: none"> <li>Changed Maximum input current factor values. ....</li> </ul>	10
<b>Changes from Revision A (December 2008) to Revision B</b>	<b>Page</b>
<ul style="list-style-type: none"> <li>Changed <math>V_{BAT(REG)}</math> max value From 4.24 V To: 4.23 V .....</li> </ul>	11

**Changes from Original (September 2008) to Revision A**
**Page**

• 已更改 器件 特性添加了 AEC-Q100 信息 .....	1
• 已更改 “说明”。 .....	1
• 已更改 典型应用电路 .....	1
• Changed description of $\overline{\text{CHG}}$ pin.....	7
• Changed SYSOFF Description.....	7
• Added <a href="#">Figure 34</a> through <a href="#">Figure 1</a> . .....	12
• Changed DETAILED FUNCTIONAL DESCRIPTION section. ....	15
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• Changed text in section - STATUS INDICATORS ( $\overline{\text{PGOOD}}$ , $\overline{\text{CHG}}$ ) .....	26
• Changed Table - $\overline{\text{CHG}}$ STATUS INDICATOR.....	26
• Changed <a href="#">Equation 8</a> and <a href="#">Equation 9</a> .....	27
• Changed APPLICATION CIRCUITS section.....	31
• Added Using BQ24075 to Disconnect the Battery from the System, <a href="#">Figure 42</a> .....	36
• Changed section - Half-Wave Adaptors .....	37

## 5 说明（续）

此外，该系列充电器可提供经稳压的系统输入，即使在电池完全放电的情况下，也可使系统在连接电源后实现瞬间开启。当适配器无法提供峰值系统电流时，电源路径管理架构还允许使用电池来补充系统电流，进而支持使用更小的适配器。

电池充电过程分为三个阶段：预充电、恒流充电和恒压充电。在所有的充电阶段，一个内部控制环路监测 IC 结温并且如果超过此内部温度阈值则减少充电电流。充电器功率级和充电电流感应功能完全集成在了一起。该充电器具高精度电流和电压调节环路、充电状态显示和充电终止功能。输入电流限制和充电电流可使用外部电阻编程设定。

## 6 Device Comparison Table

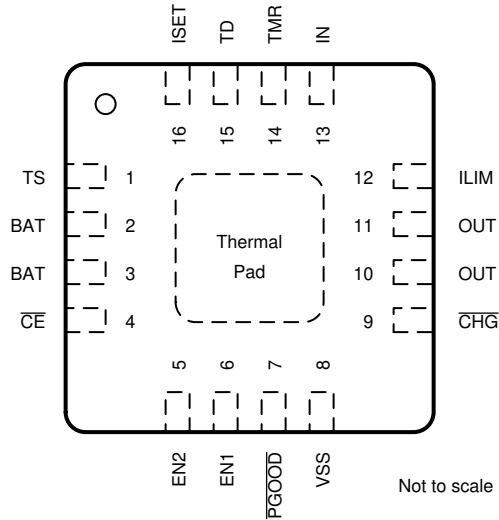
Part NO. <sup>(1) (2)</sup>	V <sub>OV</sub> P	V <sub>BAT(REG)</sub>	V <sub>OUT(REG)</sub>	V <sub>DPPM</sub>	TS Method	Optional Function	Package
BQ24072	6.6 V	4.2 V	V <sub>BAT</sub> + 225 mV	V <sub>O(REG)</sub> – 100 mV	Current Based	TD	RGT0016B
BQ24073	6.6 V	4.2 V	4.4 V	V <sub>O(REG)</sub> – 100 mV		TD	
BQ24074	10.5 V	4.2 V	4.4 V	V <sub>O(REG)</sub> – 100 mV		ITERM	
BQ24075	6.6 V	4.2 V	5.5 V	4.3 V		SYSOFF	
BQ24076	6.6 V	4.4 V	V <sub>BAT</sub> + 225 mV	V <sub>O(REG)</sub> – 100 mV		SYSOFF	
BQ24078	6.6 V	4.35 V	V <sub>BAT</sub> + 225 mV	V <sub>O(REG)</sub> – 100 mV		SYSOFF	
BQ24079	6.6 V	4.1 V	5.5 V	4.3 V		SYSOFF	
BQ24072T	6.6 V	4.2 V	V <sub>BAT</sub> + 225 mV	V <sub>O(REG)</sub> – 100 mV	Voltage Based	TD	
BQ24075T	6.6 V	4.2 V	5.5 V	4.3 V		SYSOFF	
BQ24079T	v	6.6 V	5.5 V	4.3 V		v	

(1) For all available packages, see the orderable addendum at the end of the datasheet

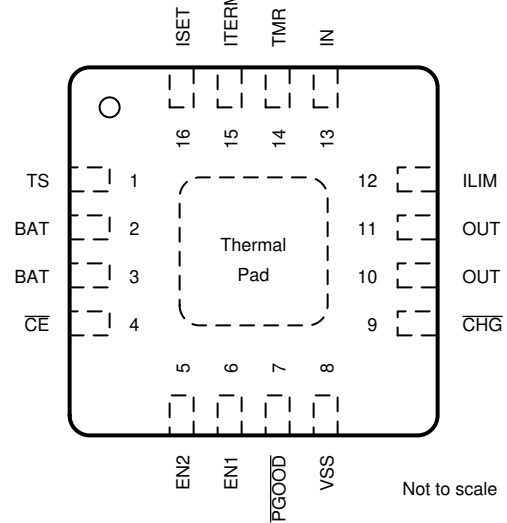
(2) This product is RoHS compatible, including a lead concentration that does not exceed 0.1% of total product weight, and is suitable for use in specified lead-free soldering processes. In addition, this product uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

## 7 Pin Configuration and Functions

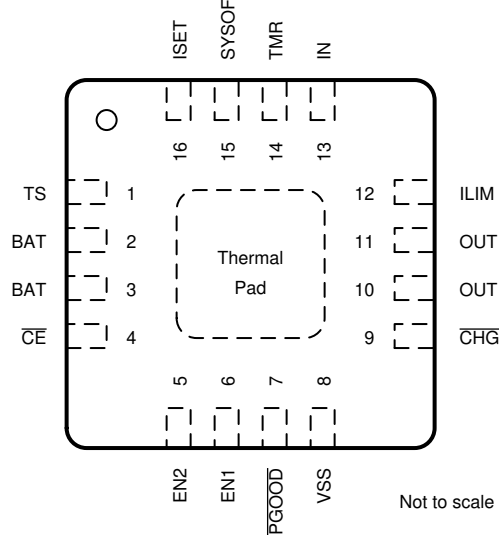
**BQ24072, BQ24073 RGT0016B Package  
16 Pins  
Top View**



**BQ24074 RGT0016B Package  
16 Pins  
Top View**



**BQ24075 RGT0016C Package, BQ24079 RGT0016B Package  
16 Pins  
Top View**



## Pin Functions

PIN				I/O	DESCRIPTION
NAME	'72, '73	'74	'75, '79		
BAT	2, 3	2, 3	2, 3	I/O	Charger Power Stage Output and Battery Voltage Sense Input. Connect BAT to the positive terminal of the battery. Bypass BAT to VSS with a 4.7-μF to 47-μF ceramic capacitor.
$\overline{CE}$	4	4	4	I	Charge Enable Active-Low Input. Connect $\overline{CE}$ to a high logic level to disable battery charging. OUT is active and battery supplement mode is still available. Connect $\overline{CE}$ to a low logic level to enable the battery charger. $\overline{CE}$ is internally pulled down with approximately 285 kΩ. Do not leave $\overline{CE}$ unconnected to ensure proper operation.
$\overline{CHG}$	9	9	9	O	Open-Drain Charging Status Indication Output. $\overline{CHG}$ pulls to VSS when the battery is charging. $\overline{CHG}$ is high impedance when charging is complete and when charger is disabled. Connect $\overline{CHG}$ to the desired logic voltage rail using a 1kΩ-100kΩ resistor, or use with an LED for visual indication.
EN1	6	6	6	I	Input Current Limit Configuration Inputs. Use EN1 and EN2 control the maximum input current and enable USB compliance. See <a href="#">Table 1</a> for the description of the operation states. EN1 and EN2 are internally pulled down with ≈285 kΩ. Do not leave EN1 or EN2 unconnected to ensure proper operation.
EN2	5	5	5	I	
ILIM	12	12	12	I	Adjustable Current Limit Programming Input. Connect a 1100-Ω to 8-kΩ resistor from ILIM to VSS to program the maximum input current (EN2=1, EN1=0). The input current includes the system load and the battery charge current. Leaving ILIM unconnected disables all charging.
IN	13	13	13	I	Input Power Connection. Connect IN to the external DC supply (AC adapter or USB port). The input operating range is 4.35 V to 6.6 V (BQ24072, BQ24073, BQ24075, and BQ24079) or 4.35 V to 10.5 V (BQ23074). The input can accept voltages up to 26 V without damage but operation is suspended. Connect bypass capacitor 1 μF to 10 μF to VSS.
ISET	16	16	16	I/O	Fast Charge Current Programming Input. Connect a 590-Ω to 8.9-kΩ resistor from ISET to VSS to program the fast charge current level. Charging is disabled if ISET is left unconnected. While charging, the voltage at ISET reflects the actual charging current and can be used to monitor charge current. See <a href="#">Charge Current Translator</a> for more details.
ITERM	–	15	–	I	Termination Current Programming Input. Connect a 0-Ω to 15-kΩ resistor from ITERM to VSS to program the termination current. Leave ITERM unconnected to set the termination current to the default 10% termination threshold.
OUT	10, 11	10, 11	10, 11	O	System Supply Output. OUT provides a regulated output when the input is below the OVP threshold and above the regulation voltage. When the input is out of the operation range, OUT is connected to V <sub>BAT</sub> except when SYSOFF is high (BQ24075 and BQ24079 only). Connect OUT to the system load. Bypass OUT to VSS with a 4.7-μF to 47-μF ceramic capacitor.
$\overline{PGOOD}$	7	7	7	O	Open-drain Power Good Status Indication Output. $\overline{PGOOD}$ pulls to VSS when a valid input source is detected. $\overline{PGOOD}$ is high-impedance when the input power is not within specified limits. Connect $\overline{PGOOD}$ to the desired logic voltage rail using a 1-kΩ to 100-kΩ resistor, or use with an LED for visual indication.
SYSOFF	–	–	15	I	System Enable Input. Connect SYSOFF high to turn off the FET connecting the battery to the system output. When an adapter is connected, charging is also disabled. Connect SYSOFF low for normal operation. SYSOFF is internally pulled up to V <sub>BAT</sub> through a large resistor (approximately 5 MΩ). Do not leave SYSOFF unconnected to ensure proper operation.
TD	15	–	–	I	Termination Disable Input. Connect TD high to disable charger termination. Connect TD to VSS to enable charger termination. TD is checked during startup only and cannot be changed during operation. See the TD section in this datasheet for a description of the behavior when termination is disabled. TD is internally pulled down to VSS with approximately 285 kΩ. Do not leave TD unconnected to ensure proper operation.
Thermal Pad	—	—	—	–	There is an internal electrical connection between the exposed thermal pad and the VSS pin of the device. The thermal pad must be connected to the same potential as the VSS pin on the printed circuit board. Do not use the thermal pad as the primary ground input for the device. VSS pin must be connected to ground at all times.
TMR	14	14	14	I	Timer Programming Input. TMR controls the pre-charge and fast-charge safety timers. Connect TMR to VSS to disable all safety timers. Connect a 18-kΩ to 72-kΩ resistor between TMR and VSS to program the timers a desired length. Leave TMR unconnected to set the timers to the default values.
TS	1	1	1	I	External NTC Thermistor Input. Connect the TS input to the NTC thermistor in the battery pack. TS monitors a 10kΩ NTC thermistor. For applications that do not use the TS function, connect a 10-kΩ fixed resistor from TS to VSS to maintain a valid voltage level on TS.
VSS	8	8	8	–	Ground. Connect to the thermal pad and to the ground rail of the circuit.

**Table 1. EN1/EN2 Settings**

EN2	EN1	MAXIMUM INPUT CURRENT INTO IN PIN
0	0	100 mA. USB100 mode
0	1	500 mA. USB500 mode
1	0	Set by an external resistor from ILIM to VSS
1	1	Standby (USB suspend mode)

## 8 Specifications

### 8.1 Absolute Maximum Ratings<sup>(1)</sup>

over the 0°C to 125°C operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V <sub>I</sub>	Input Voltage			
	IN (with respect to VSS)	–0.3	28	V
	BAT (with respect to VSS)	–0.3	5	V
	OUT, EN1, EN2, $\overline{\text{CE}}$ , TS, ISET, $\overline{\text{PGOOD}}$ , CHG, ILIM, TMR, ITERM, SYSOFF, TD (with respect to VSS)	–0.3	7	V
I <sub>I</sub>	Input Current		1.6	A
I <sub>O</sub>	Output Current (Continuous)		5	A
	BAT (Discharge mode)		5	A
	BAT (Charging mode)		1.5 <sup>(2)</sup>	A
	Output Sink Current		15	mA
T <sub>J</sub>	Junction temperature	–40	150	°C
T <sub>stg</sub>	Storage temperature	–65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to the network ground terminal unless otherwise noted.
- (2) The IC operational charging life is reduced to 20,000 hours, when charging at 1.5A and 125°C. The thermal regulation feature reduces charge current if the IC's junction temperature reaches 125°C; thus without a good thermal design the maximum programmed charge current may not be reached.

### 8.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge		
	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 8.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V <sub>I</sub>	IN voltage range		4.35	26	V
	IN operating voltage range	'72, '73, '75, '79	4.35	6.4	V
		'74	4.35	10.2	
I <sub>IN</sub>	Input current, IN pin			1.5	A
I <sub>OUT</sub>	Current, OUT pin			4.5	A
I <sub>BAT</sub>	Current, BAT pin (Discharging)			4.5	A
I <sub>CHG</sub>	Current, BAT pin (Charging)			1.5 <sup>(1)</sup>	A
T <sub>J</sub>	Junction Temperature		–40	125	°C
R <sub>ILIM</sub>	Maximum input current programming resistor		1100	8000	Ω
R <sub>ISET</sub>	Fast-charge current programming resistor <sup>(2)</sup>		590	8900	Ω
R <sub>ITERM</sub>	Termination current programming resistor		0	15	kΩ
R <sub>TMR</sub>	Timer programming resistor		18	72	kΩ

- (1) The IC operational charging life is reduced to 20,000 hours, when charging at 1.5A and 125°C. The thermal regulation feature reduces charge current if the IC's junction temperature reaches 125°C; thus without a good thermal design the maximum programmed charge current may not be reached.
- (2) Use a 1% tolerance resistor for R<sub>ISET</sub> to avoid issues with the R<sub>ISET</sub> short test when using the maximum charge current setting.



## 8.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		BQ2407x	UNIT
		RGT	
		16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	44.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	54.2	
$R_{\theta JB}$	Junction-to-board thermal resistance	17.2	
$\Psi_{JT}$	Junction-to-top characterization parameter	1.0	
$\Psi_{JB}$	Junction-to-board characterization parameter	17.1	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.8	

(1) For more information about traditional and new thermal metrics, see the [Semiconductor IC Package Thermal Metrics](#) application report.

## 8.5 Electrical Characteristics

Over junction temperature range ( $0^{\circ} \leq T_J \leq 125^{\circ}\text{C}$ ) and the recommended supply voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>INPUT</b>						
UVLO	Undervoltage lock-out	$V_{IN}: 0\text{ V} \rightarrow 4\text{ V}$	3.2	3.3	3.4	V
$V_{hys}$	Hysteresis on UVLO	$V_{IN}: 4\text{ V} \rightarrow 0\text{ V}$	200		300	mV
$V_{IN(DT)}$	Input power detection threshold	Input power detected when $V_{IN} > V_{BAT} + V_{IN(DT)}$ $V_{BAT} = 3.6\text{ V}$ , $V_{IN}: 3.5\text{ V} \rightarrow 4\text{ V}$	55	80	130	mV
$V_{hys}$	Hysteresis on $V_{IN(DT)}$	$V_{BAT} = 3.6\text{ V}$ , $V_{IN}: 4\text{ V} \rightarrow 3.5\text{ V}$	20			mV
$t_{DGL(PGOOD)}$	Deglintch time, input power detected status	Time measured from $V_{IN}: 0\text{ V} \rightarrow 5\text{ V}$ 1 $\mu\text{s}$ rise-time to $PGOOD = LO$		1.2		ms
$V_{OVP}$	Input overvoltage protection threshold	$V_{IN}: 5\text{ V} \rightarrow 7\text{ V}$	('72, '73, '75, '79)		6.4	V
		$V_{IN}: 5\text{ V} \rightarrow 11\text{ V}$	('74)		10.2	
$V_{hys}$	Hysteresis on OVP	$V_{IN}: 7\text{ V} \rightarrow 5\text{ V}$	('72, '73, '75, '79)		110	mV
		$V_{IN}: 11\text{ V} \rightarrow 5\text{ V}$	('74)		175	
$t_{DGL(OVP)}$	Input overvoltage blanking time (OVP fault deglitch)			50		$\mu\text{s}$
$t_{REC}$	Input overvoltage recovery time	Time measured from $V_{IN}: 11\text{ V} \rightarrow 5\text{ V}$ with 1 $\mu\text{s}$ fall-time to $PGOOD = LO$		1.2		ms
<b>ILIM, ISET SHORT-CIRCUIT DETECTION (CHECKED DURING STARTUP)</b>						
$I_{SC}$	Current source	$V_{IN} > UVLO$ and $V_{IN} > V_{BAT} + V_{IN(DT)}$		1.3		mA
$V_{SC}$		$V_{IN} > UVLO$ and $V_{IN} > V_{BAT} + V_{IN(DT)}$		520		mV
<b>QUIESCENT CURRENT</b>						
$I_{BAT(PDWN)}$	Sleep current into BAT pin	$\overline{CE} = LO$ or HI, input power not detected, No load on OUT pin, $T_J = 85^{\circ}\text{C}$			6.5	$\mu\text{A}$
$I_{IN}$	Standby current into IN pin	EN1= HI, EN2=HI, $V_{IN} = 6\text{ V}$ , $T_J = 85^{\circ}\text{C}$			50	$\mu\text{A}$
		EN1= HI, EN2=HI, $V_{IN} = 10\text{ V}$ , $T_J = 85^{\circ}\text{C}$			200	
$I_{CC}$	Active supply current, IN pin	$\overline{CE} = LO$ , $V_{IN} = 6\text{ V}$ , no load on OUT pin, $V_{BAT} > V_{BAT(REG)}$ , (EN1, EN2) $\neq$ (HI, HI)			1.5	mA
<b>POWER PATH</b>						
$V_{DO(IN-OUT)}$	$V_{IN} - V_{OUT}$	$V_{IN} = 4.3\text{ V}$ , $I_{IN} = 1\text{ A}$ , $V_{BAT} = 4.2\text{ V}$		300	475	mV
$V_{DO(BAT-OUT)}$	$V_{BAT} - V_{OUT}$	$I_{OUT} = 1\text{ A}$ , $V_{IN} = 0\text{ V}$ , $V_{BAT} > 3\text{ V}$		50	100	mV
$V_{O(REG)}$	OUT pin voltage regulation (BQ24072)	$V_{IN} > V_{OUT} + V_{DO(IN-OUT)}$ , $V_{BAT} < 3.2\text{ V}$	3.3	3.4	3.5	V
		$V_{IN} > V_{OUT} + V_{DO(IN-OUT)}$ , $V_{BAT} \geq 3.2\text{ V}$	$V_{BAT} + 150\text{mV}$	$V_{BAT} + 225\text{mV}$	$V_{BAT} + 270\text{mV}$	
	OUT pin voltage regulation (BQ24073, BQ24074)	$V_{IN} > V_{OUT} + V_{DO(IN-OUT)}$	4.3	4.4	4.5	
	OUT pin voltage regulation (BQ24075, BQ24079)	$V_{IN} > V_{OUT} + V_{DO(IN-OUT)}$	5.4	5.5	5.6	
$I_{IN(max)}$	Maximum input current	EN1 = LO, EN2 = LO	90	95	100	mA
		EN1 = HI, EN2 = LO	450	475	500	
		EN2 = HI, EN1 = LO	$K_{ILIM}/R_{ILIM}$			
$K_{ILIM}$	Maximum input current factor	$I_{LIM} = 500\text{ mA}$ to 1.5 A	1500	1610	1720	A $\Omega$
		$I_{LIM} = 200\text{ mA}$ to 500 mA	1330	1525	1720	
$I_{IN(max)}$	Programmable input current limit range	EN2 = HI, EN1 = LO, $R_{ILIM} = 8\text{ k}\Omega$ to 1.1 k $\Omega$	200		1500	mA
$V_{IN-DPM}$	Input voltage threshold when input current is reduced	EN2 = LO, EN1 = X	4.35	4.5	4.63	V
$V_{DPPM}$	Output voltage threshold when charging current is reduced	('72, '73, '74) ('75, '79)	$V_{O(REG)} - 180\text{mV}$	$V_{O(REG)} - 100\text{mV}$	$V_{O(REG)} - 30\text{mV}$	V
			4.2	4.3	4.4	V
$V_{BSUP1}$	Enter battery supplement mode	$V_{BAT} = 3.6\text{ V}$ , $R_{ILIM} = 1.5\text{ k}\Omega$ , $R_{LOAD} = 10\text{ }\Omega \rightarrow 2\text{ }\Omega$		$V_{OUT} \leq V_{BAT} - 40\text{mV}$		V
$V_{BSUP2}$	Exit battery supplement mode	$V_{BAT} = 3.6\text{ V}$ , $R_{ILIM} = 1.5\text{ k}\Omega$ , $R_{LOAD} = 2\text{ }\Omega \rightarrow 10\text{ }\Omega$		$V_{OUT} \geq V_{BAT} - 20\text{mV}$		V
$V_{O(SC1)}$	Output short-circuit detection threshold, power-on	$V_{IN} > V_{UVLO}$ and $V_{IN} > V_{BAT} + V_{IN(DT)}$	0.8	0.9	1	V
$V_{O(SC2)}$	Output short-circuit detection threshold, supplement mode $V_{BAT} - V_{OUT} > V_{O(SC2)}$ indicates short-circuit	$V_{IN} > V_{UVLO}$ and $V_{IN} > V_{BAT} + V_{IN(DT)}$	200	250	300	mV
$t_{DGL(SC2)}$	Deglitch time, supplement mode short circuit			250		$\mu\text{s}$
$t_{REC(SC2)}$	Recovery time, supplement mode short circuit			60		ms

## Electrical Characteristics (continued)

Over junction temperature range ( $0^{\circ} \leq T_J \leq 125^{\circ}\text{C}$ ) and the recommended supply voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>BATTERY CHARGER</b>						
$I_{BAT}$	Source current for BAT pin short-circuit detection	$V_{BAT} = 1.5\text{ V}$	4	7.5	11	mA
$V_{BAT(SC)}$	BAT pin short-circuit detection threshold	$V_{BAT}$ rising	1.6	1.8	2	V
$V_{BAT(REG)}$	Battery charge voltage	( '72, '73, '74, '75) ( '79)	4.16 4.059	4.20 4.100	4.23 4.141	V
$V_{LOWV}$	Pre-charge to fast-charge transition threshold	$V_{IN} > V_{UVLO}$ and $V_{IN} > V_{BAT} + V_{IN(DT)}$	2.9	3	3.1	V
$t_{DGL1(LOWV)}$	Deglintch time on pre-charge to fast-charge transition			25		ms
$t_{DGL2(LOWV)}$	Deglintch time on fast-charge to pre-charge transition			25		ms
$I_{CHG}$	Battery fast charge current range	$V_{BAT(REG)} > V_{BAT} > V_{LOWV}$ , $V_{IN} = 5\text{ V}$ $\overline{CE} = LO$ , $EN1 = LO$ , $EN2 = HI$	100		1500	mA
	Battery fast charge current	$\overline{CE} = LO$ , $EN1 = LO$ , $EN2 = HI$ , $V_{BAT} > V_{LOWV}$ , $V_{IN} = 5\text{ V}$ , $I_{IN(max)} > I_{CHG}$ , no load on OUT pin, thermal loop and DPPM loop not active		$K_{ISET}/R_{ISET}$		A
$K_{ISET}$	Fast charge current factor		797	890	975	AΩ
$I_{PRECHG}$	Pre-charge current			$K_{PRECHG}/R_{ISET}$		A
$K_{PRECHG}$	Pre-charge current factor		70	88	106	AΩ
$I_{TERM}$	Termination comparator detection threshold (internally set)	$\overline{CE} = LO$ , $(EN1, EN2) \neq (LO, LO)$ , $V_{BAT} > V_{RCH}$ , $t < t_{MAXCH}$ , $V_{IN} = 5\text{ V}$ , DPPM loop and thermal loop not active	$0.09 \times I_{CHG}$	$0.1 \times I_{CHG}$	$0.11 \times I_{CHG}$	A
		$\overline{CE} = LO$ , $(EN1, EN2) = (LO, LO)$ , $V_{BAT} > V_{RCH}$ , $t < t_{MAXCH}$ , $V_{IN} = 5\text{ V}$ , DPPM loop and thermal loop not active	$0.027 \times I_{CHG}$	$0.033 \times I_{CHG}$	$0.040 \times I_{CHG}$	
$I_{BIAS(ITERM)}$	Current for external termination-setting resistor	$V_{IN} > V_{UVLO}$ and $V_{IN} > V_{BAT} + V_{IN(DT)}$	72	75	78	μA
$I_{TERM}$	Termination current threshold (externally set) (BQ24074)			$K_{ITERM} \times R_{ITERM} / R_{ISET}$		A
$K_{ITERM}$	K Factor for termination detection threshold (externally set) (BQ24074)	USB500 or ISET mode( $EN1, EN2 \neq (LO, LO)$ ) $\overline{CE} = LO$ , $V_{BAT} > V_{RCH}$ , $t < t_{MAXCH}$ , $V_{IN} = 5\text{ V}$ , DPPM loop and thermal loop not active	0.0225	0.0300	0.0375	A
		USB100 mode ( $EN1, EN2 = (LO, LO)$ ), $\overline{CE} = LO$ , $V_{BAT} > V_{RCH}$ , $t < t_{MAXCH}$ , $V_{IN} = 5\text{ V}$ , DPPM loop and thermal loop not active	0.008	0.0100	0.012	
$t_{DGL(TERM)}$	Deglintch time, termination detected			25		ms
$V_{RCH}$	Recharge detection threshold	$V_{IN} > V_{UVLO}$ and $V_{IN} > V_{BAT} + V_{IN(DT)}$	$V_{BAT(REG)} - 140\text{mV}$	$V_{BAT(REG)} - 100\text{mV}$	$V_{BAT(REG)} - 60\text{mV}$	V
$t_{DGL(RCH)}$	Deglintch time, recharge threshold detected			62.5		ms
$t_{DGL(NO-IN)}$	Delay time, input power loss to OUT LDO turn-off	$V_{BAT} = 3.6\text{ V}$ . Time measured from $V_{IN}$ : $5\text{ V} \rightarrow 3\text{ V}$ 1 μs fall-time		20		ms
$I_{BAT(DET)}$	Sink current for battery detection	$V_{BAT} = 2.5\text{ V}$	5	7.5	10	mA
$t_{DET}$	Battery detection timer	BAT high or low		250		ms
<b>BATTERY CHARGING TIMERS</b>						
$t_{PRECHG}$	Pre-charge safety timer value	TMR = floating	1440	1800	2160	s
$t_{MAXCHG}$	Charge safety timer value	TMR = floating	14400	18000	21600	s
$t_{PRECHG}$	Pre-charge safety timer value	$18\text{ k}\Omega < R_{TMR} < 72\text{ k}\Omega$		$R_{TMR} \times K_{TMR}$		s
$t_{MAXCHG}$	Charge safety timer value	$18\text{ k}\Omega < R_{TMR} < 72\text{ k}\Omega$		$10 \times R_{TMR} \times K_{TMR}$		s
$K_{TMR}$	Timer factor		36	48	60	s/kΩ
<b>BATTERY-PACK NTC MONITOR<sup>(1)</sup></b>						
$I_{NTC}$	NTC bias current	$V_{IN} > V_{UVLO}$ and $V_{IN} > V_{BAT} + V_{IN(DT)}$	72	75	78	μA
$V_{HOT}$	High temperature trip point	Battery charging, $V_{TS}$ Falling	270	300	330	mV
$V_{HYS(HOT)}$	Hysteresis on high trip point	Battery charging, $V_{TS}$ Rising from $V_{HOT}$		30		mV
$V_{COLD}$	Low temperature trip point	Battery charging, $V_{TS}$ Rising	2000	2100	2200	mV
$V_{HYS(COLD)}$	Hysteresis on low trip point	Battery charging, $V_{TS}$ Falling from $V_{COLD}$		300		mV
$t_{DGL(TS)}$	Deglintch time, pack temperature fault detection	TS fault detected to charger disable		50		ms
$V_{DIS(TS)}$	TS function disable threshold (BQ24072, BQ24073)	TS unconnected		$V_{IN} - 200\text{mV}$		V
<b>THERMAL REGULATION</b>						
$T_{J(REG)}$	Temperature regulation limit			125		°C
$T_{J(OFF)}$	Thermal shutdown temperature	$T_J$ Rising		155		°C
$T_{J(OFF-HYS)}$	Thermal shutdown hysteresis			20		°C

(1) These numbers set trip points of  $0^{\circ}\text{C}$  and  $50^{\circ}\text{C}$  while charging, with  $3^{\circ}\text{C}$  hysteresis on the trip points, with a Vishay Type 2 curve NTC with an R25 of  $10\text{ k}\Omega$ .

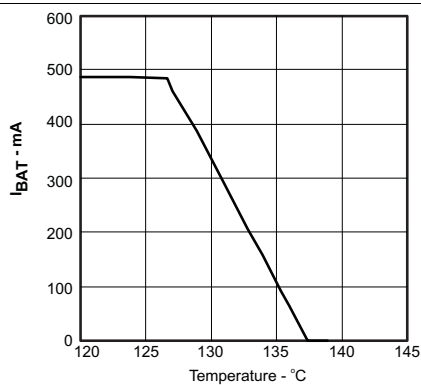
## Electrical Characteristics (continued)

Over junction temperature range ( $0^{\circ} \leq T_J \leq 125^{\circ}\text{C}$ ) and the recommended supply voltage range (unless otherwise noted)

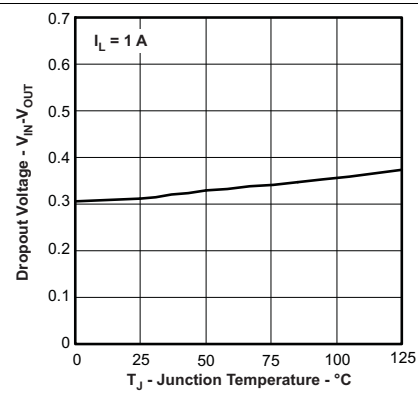
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOGIC LEVELS ON EN1, EN2, $\overline{\text{CE}}$ , SYSOFF, TD						
V <sub>IL</sub>	Logic LOW input voltage		0		0.4	V
V <sub>IH</sub>	Logic HIGH input voltage		1.4		6	V
I <sub>IL</sub>	Input sink current	V <sub>IL</sub> = 0 V			1	μA
I <sub>IH</sub>	Input source current	V <sub>IH</sub> = 1.4 V			10	μA
LOGIC LEVELS ON $\overline{\text{PGOOD}}$ , $\overline{\text{CHG}}$						
V <sub>OL</sub>	Output LOW voltage	I <sub>SINK</sub> = 5 mA			0.4	V

## 8.6 Typical Characteristics

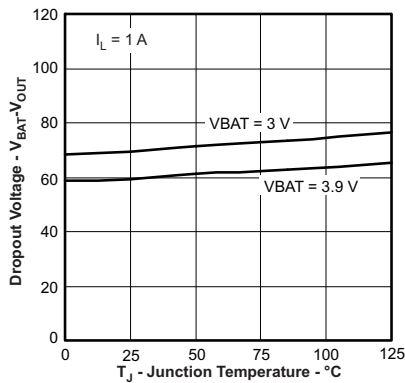
$V_{IN} = 6\text{ V}$ ,  $EN1=1$ ,  $EN2=0$ , BQ24073 application circuit,  $T_A = 25^{\circ}\text{C}$ , unless otherwise noted.



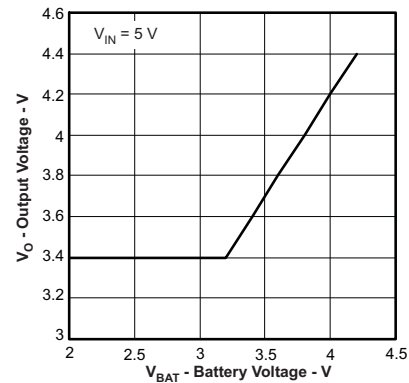
**Figure 1. Thermal Regulation**



**Figure 2. Dropout Voltage vs Temperature**



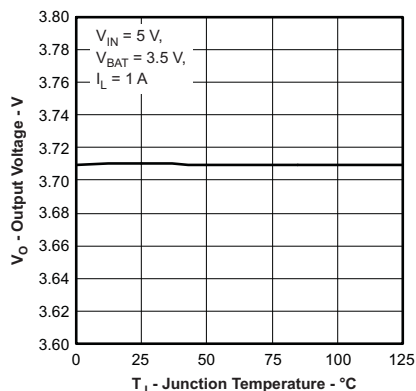
**Figure 3. Dropout Voltage vs Temperature  
No Input Supply**



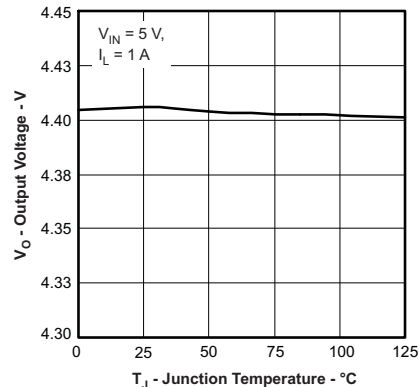
**Figure 4. BQ24072  
Output Regulation Voltage vs Battery Voltage**

## Typical Characteristics (continued)

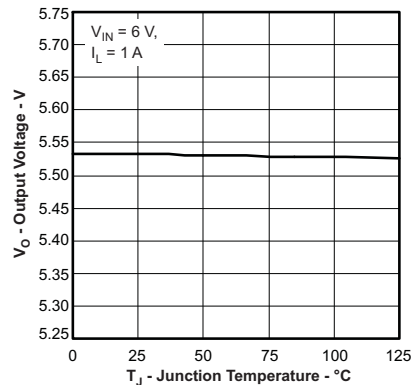
$V_{IN} = 6\text{ V}$ ,  $EN1=1$ ,  $EN2=0$ , BQ24073 application circuit,  $T_A = 25^\circ\text{C}$ , unless otherwise noted.



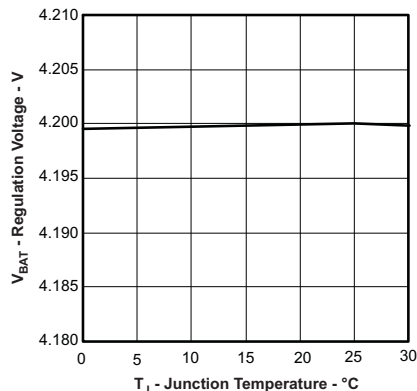
**Figure 5. BQ24072**  
Output Regulation Voltage vs Temperature



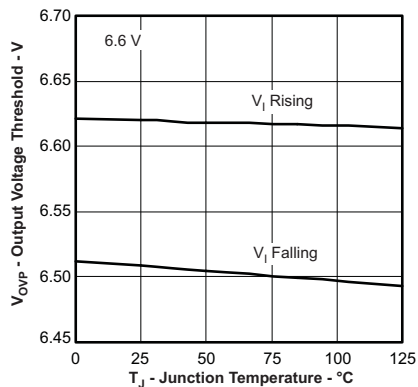
**Figure 6. BQ24073/ 74**  
Output Regulation Voltage vs Temperature



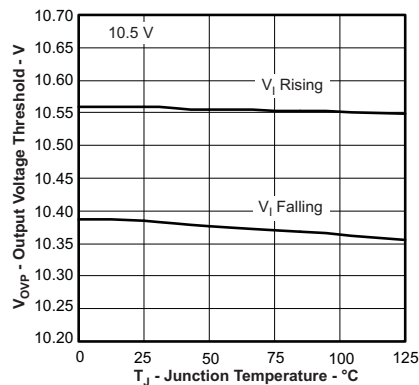
**Figure 7. BQ24075, BQ24079**  
Output Regulation Voltage vs Temperature



**Figure 8. BAT Regulation Voltage vs Temperature**



**Figure 9. BQ24072/ 73/ 75/ 79**  
Overvoltage Protection Threshold vs Temperature



**Figure 10. BQ24074 Overvoltage Protection Threshold vs Temperature**

## Typical Characteristics (continued)

$V_{IN} = 6\text{ V}$ ,  $EN1=1$ ,  $EN2=0$ , BQ24073 application circuit,  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

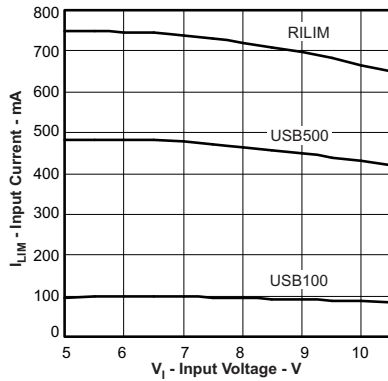


Figure 11. BQ24074 Input Current Limit vs Input Voltage

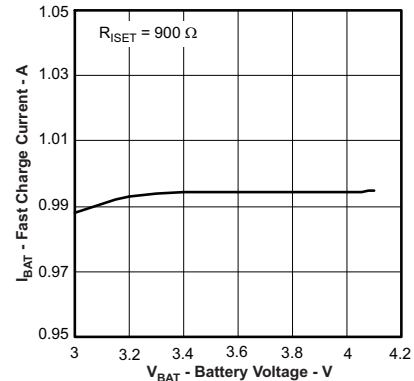


Figure 12. Fastcharge Current vs Battery Voltage

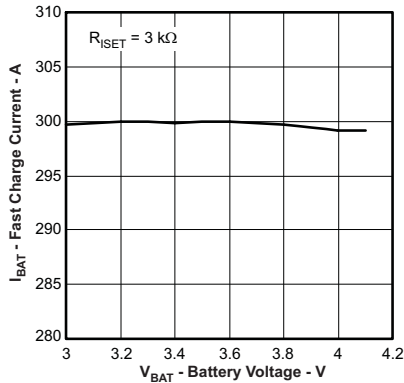


Figure 13. Fastcharge Current vs Battery Voltage

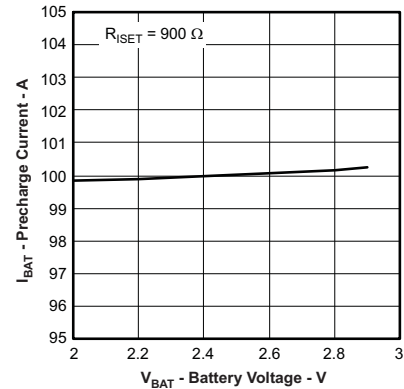


Figure 14. Precharge Current vs Battery Voltage

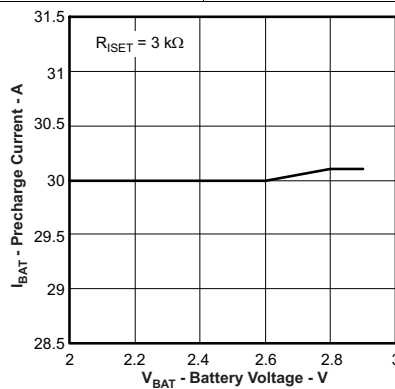


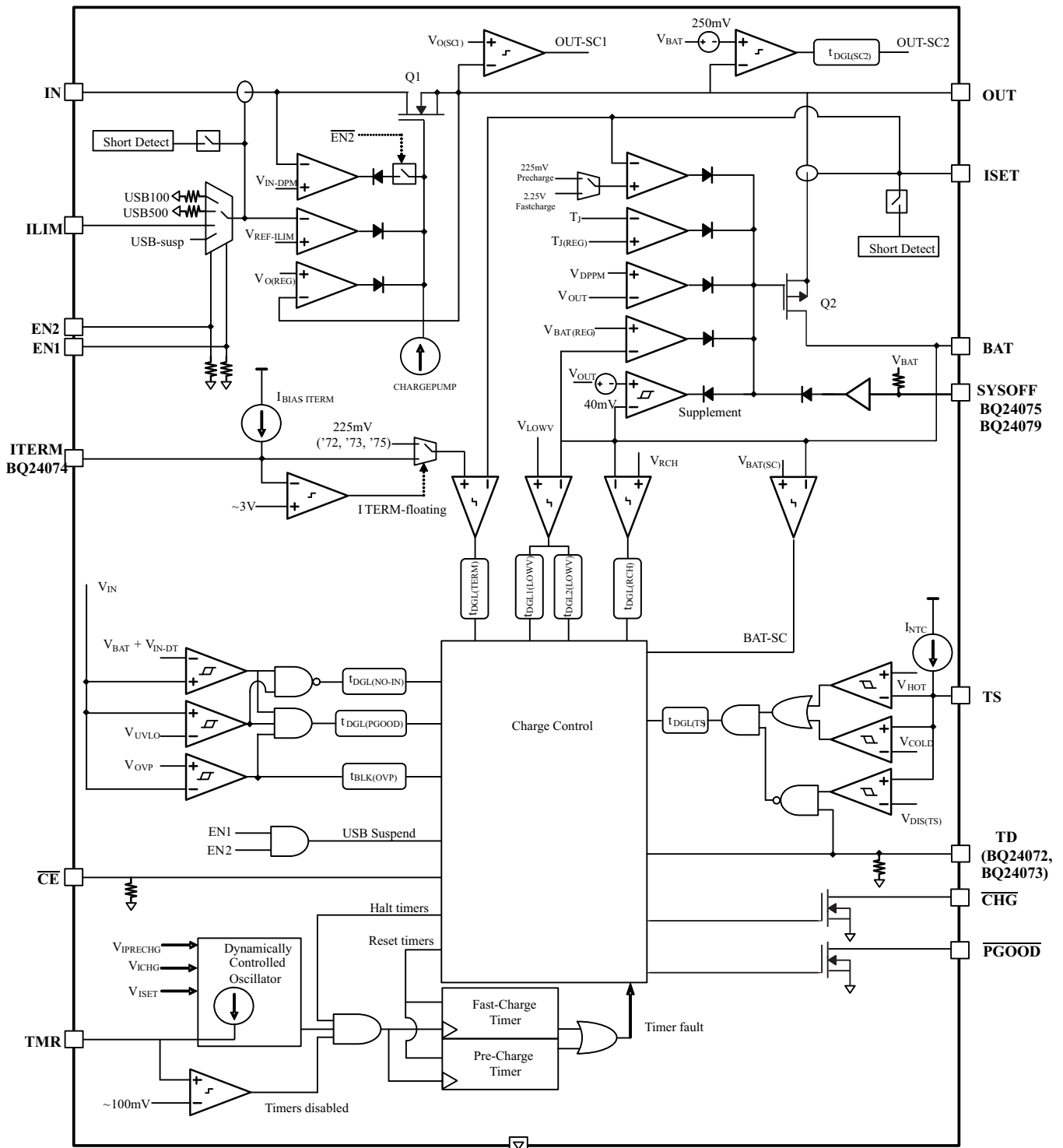
Figure 15. Precharge Current vs Battery Voltage

## 9 Detailed Description

### 9.1 Overview

The BQ2407x devices are integrated Li-Ion linear chargers and system power path management devices targeted at space-limited portable applications. The device powers the system while simultaneously and independently charging the battery. This feature reduces the number of charge and discharge cycles on the battery, allows for proper charge termination and enables the system to run with a defective or absent battery pack. This feature also allows instant system turn-on even with a totally discharged battery. The input power source for charging the battery and running the system can be an AC adapter or a USB port. The devices feature Dynamic Power Path Management (DPPM), which shares the source current between the system and battery charging, and automatically reduces the charging current if the system load increases. When charging from a USB port, the input dynamic power management ( $V_{IN-DPM}$ ) circuit reduces the input current if the input voltage falls below a threshold, thus preventing the USB port from crashing. The power-path architecture also permits the battery to supplement the system current requirements when the adapter cannot deliver the peak system currents.

## 9.2 Functional Block Diagram





## 9.3 Feature Description

### 9.3.1 Undervoltage Lockout (UVLO)

The BQ2407X family remains in power down mode when the input voltage at the IN pin is below the undervoltage threshold (UVLO).

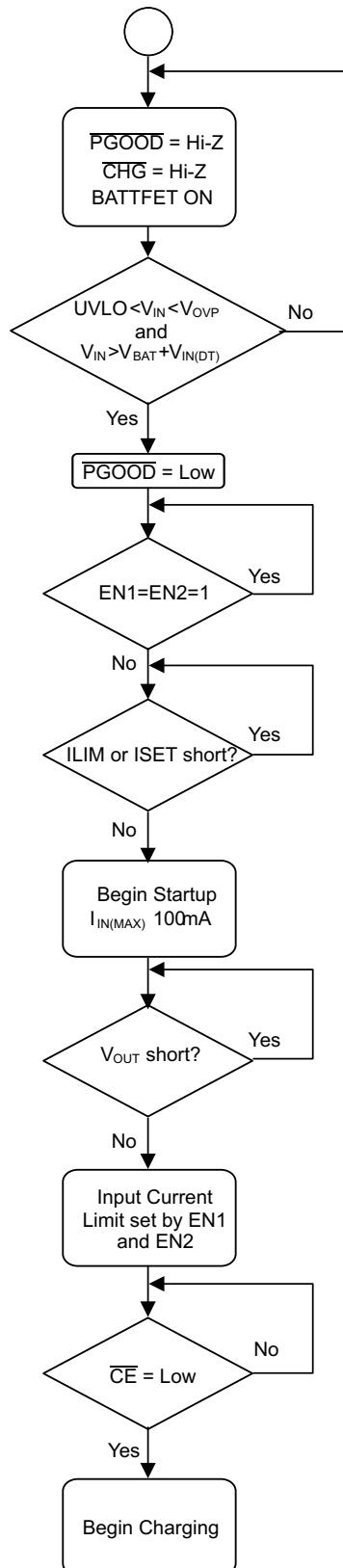
During the power down mode the host commands at the control inputs ( $\overline{CE}$ , EN1 and EN2) are ignored. The Q1 FET connected between IN and OUT pins is off, and the status outputs  $\overline{CHG}$  and  $\overline{PGOOD}$  are high impedance. The Q2 FET that connects BAT to OUT is ON. (If SYSOFF is high, Q2 is off). During power down mode, the  $V_{OUT(SC2)}$  circuitry is active and monitors for overload conditions on OUT.

### 9.3.2 Power On

When  $V_{IN}$  exceeds the UVLO threshold, the BQ2407x powers up. While  $V_{IN}$  is below  $V_{BAT} + V_{IN(DT)}$ , the host commands at the control inputs ( $\overline{CE}$ , EN1 and EN2) are ignored. The Q1 FET connected between IN and OUT pins is off, and the status outputs  $\overline{CHG}$  and  $\overline{PGOOD}$  are high impedance. The Q2 FET that connects BAT to OUT is ON. (If SYSOFF is high, Q2 is off). During this mode, the  $V_{OUT(SC2)}$  circuitry is active and monitors for overload conditions on OUT.

Once  $V_{IN}$  rises above  $V_{BAT} + V_{IN(DT)}$ ,  $\overline{PGOOD}$  is driven low to indicate the valid power status and the  $\overline{CE}$ , EN1, and EN2 inputs are read. The device enters standby mode if (EN1 = EN2 = HI) or if an input overvoltage condition occurs. In standby mode, Q1 is OFF and Q2 is ON so OUT is connected to the battery input. (If SYSOFF is high, FET Q2 is off). During this mode, the  $V_{OUT(SC2)}$  circuitry is active and monitors for overload conditions on OUT.

When the input voltage at IN is within the valid range:  $V_{IN} > UVLO$  **AND**  $V_{IN} > V_{BAT} + V_{IN(DT)}$  **AND**  $V_{IN} < V_{OVP}$ , and the EN1 and EN2 pins indicate that the USB suspend mode is not enabled [(EN1, EN2)  $\neq$  (HI, HI)] all internal timers and other circuit blocks are activated. The device then checks for short-circuits at the ISET and ILIM pins. If no short conditions exists, the device switches on the input FET Q1 with a 100mA current limit to checks for a short circuit at OUT. When  $V_{OUT}$  is above  $V_{O(SC1)}$ , the FET Q1 switches to the current limit threshold set by EN1, EN2 and  $R_{ILIM}$  and the device enters into the normal operation. During normal operation, the system is powered by the input source (Q1 is regulating), and the device continuously monitors the status of  $\overline{CE}$ , EN1 and EN2 as well as the input voltage conditions.

**Feature Description (continued)**

**Figure 16. Startup Flow Diagram**

## Feature Description (continued)

### 9.3.3 Overvoltage Protection (OVP)

The BQ2407x accepts inputs up to 28 V without damage. Additionally, an overvoltage protection (OVP) circuit is implemented that shuts off the internal LDO and discontinues charging when  $V_{IN} > V_{OVP}$  for a period long than  $t_{DGL(OVP)}$ . When in OVP, the system output (OUT) is connected to the battery and PGOOD is high impedance. Once the OVP condition is removed, a new power on sequence starts (see [Power On](#)). The safety timers are reset and a new charge cycle will be indicated by the CHG output.

### 9.3.4 Dynamic Power-Path Management

The BQ2407x features an OUT output that powers the external load connected to the battery. This output is active whenever a source is connected to IN or BAT. The following sections discuss the behavior of OUT with a source connected to IN to charge the battery and a battery source only.

#### 9.3.4.1 Input Source Connected (ADAPTER or USB)

With a source connected, the dynamic power-path management (DPPM) circuitry of the BQ2407x monitors the input current continuously. The OUT output for the BQ24073/ 74/ 75/ 79 is regulated to a fixed voltage ( $V_{O(REG)}$ ). For the BQ24072, OUT is regulated to 200 mV above the voltage at BAT. When the BAT voltage falls below 3.2 V, OUT is clamped to 3.4 V. This allows for proper startup of the system load even with a discharged battery. The current into IN is shared between charging the battery and powering the system load at OUT. The BQ2407x has internal selectable current limits of 100 mA (USB100) and 500 mA (USB500) for charging from USB ports, as well as a resistor-programmable input current limit.

The BQ2407x is USB IF compliant for the inrush current testing. The USB specification allows up to 10  $\mu$ F to be hard started, which establishes 50  $\mu$ C as the maximum inrush charge value when exceeding 100 mA. The input current limit for the BQ2407x prevents the input current from exceeding this limit, even with system capacitances greater than 10  $\mu$ F. The input capacitance to the device must be selected small enough to prevent a violation (<10  $\mu$ F), as this current is not limited. [Figure 17](#) demonstrates the start-up of the BQ2407x and compares it to the USB-IF specification.

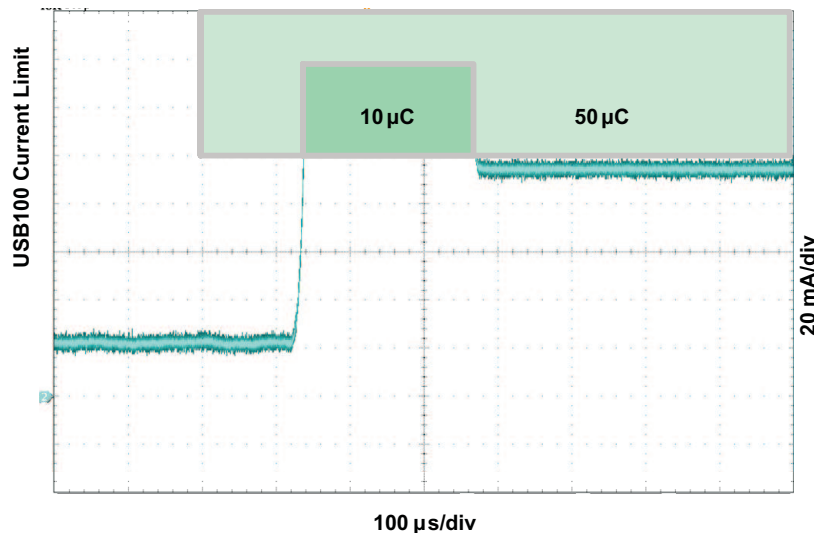


Figure 17. USB-IF Inrush Current Test

The input current limit selection is controlled by the state of the EN1 and EN2 pins as shown in the *EN1/EN2 Settings* table in [Pin Configuration and Functions](#). When using the resistor-programmable current limit, the input current limit is set by the value of the resistor connected from the ILIM pin to VSS, and is given by the equation:

$$I_{IN-MAX} = K_{ILIM}/R_{ILIM} \quad (1)$$

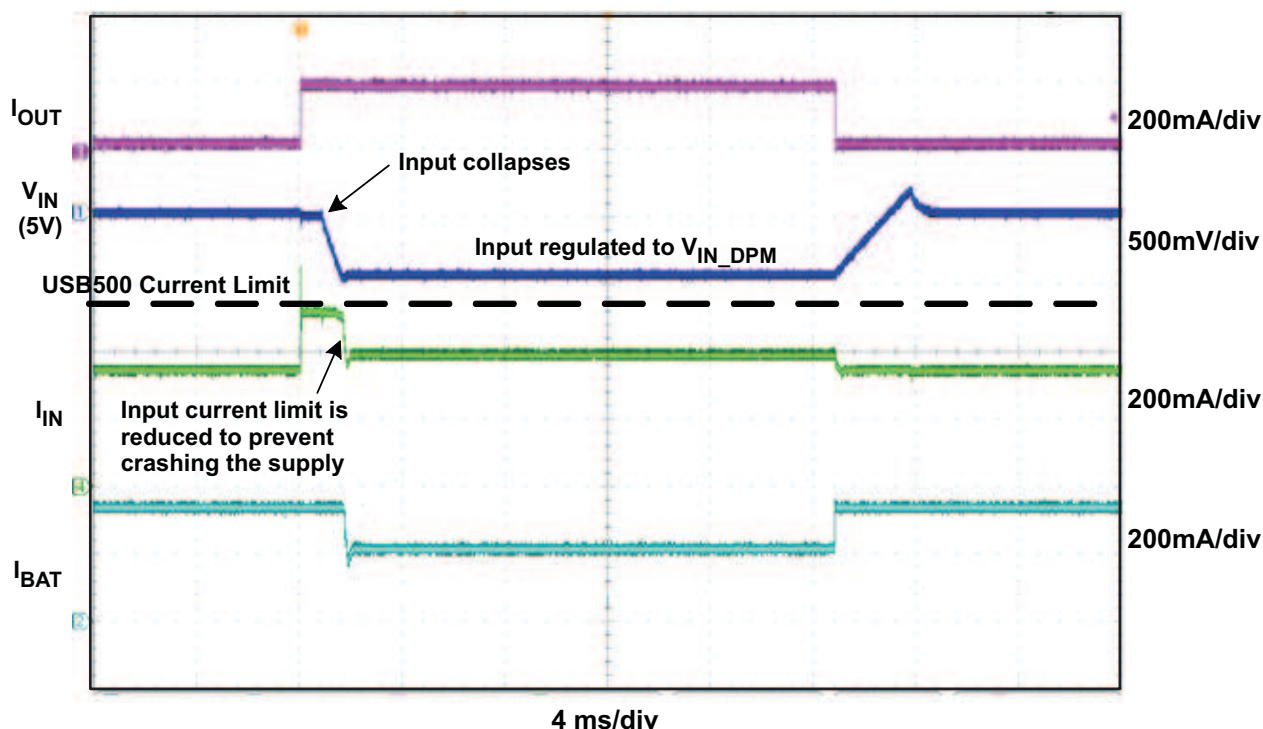
The input current limit is adjustable up to 1.5 A. The valid resistor range is 1.1 k $\Omega$  to 8 k $\Omega$ .

## Feature Description (continued)

When the IN source is connected, priority is given to the system load. The DPPM and Battery Supplement modes are used to maintain the system load. Figure 19 and Figure 20 illustrate examples of the DPPM and supplement modes. These modes are explained in detail in the following sections.

### 9.3.4.1.1 Input DPM Mode ( $V_{IN\_DPM}$ )

The BQ2407x utilizes the  $V_{IN\_DPM}$  mode for operation from current-limited USB ports. When EN1 and EN2 are configured for USB100 (EN2=0, EN1=0) or USB500 (EN2=0, EN1=1) modes, the input voltage is monitored. If  $V_{IN}$  falls to  $V_{IN\_DPM}$ , the input current limit is reduced to prevent the input voltage from falling further. This prevents the BQ2407x from crashing poorly designed or incorrectly configured USB sources. Figure 18 shows the  $V_{IN\_DPM}$  behavior to a current limited source. In this figure, the input source has a 400-mA current limit and the device is in USB500 mode (EN1=1, EN2=0).



**Figure 18.  $V_{IN\_DPM}$  Waveform**

### 9.3.4.1.2 DPPM Mode

When the sum of the charging and system load currents exceeds the maximum input current (programmed with EN1, EN2, and ILIM pins), the voltage at OUT decreases. Once the voltage on the OUT pin falls to  $V_{DPPM}$ , the BQ2407x enters DPPM mode. In this mode, the charging current is reduced as the OUT current increases in order to maintain the system output. Battery termination is disabled while in DPPM mode.

### 9.3.4.1.3 Battery Supplement Mode

While in DPPM mode, if the charging current falls to zero and the system load current increases beyond the programmed input current limit, the voltage at OUT reduces further. When the OUT voltage drops below the  $V_{BSUP1}$  threshold, the battery supplements the system load. The battery stops supplementing the system load when the voltage at OUT rises above the  $V_{BSUP2}$  threshold.

During supplement mode, the battery supplement current is not regulated (BAT-FET is fully on), however there is a short circuit protection circuit built in. Figure 35 demonstrates supplement mode. If during battery supplement mode, the voltage at OUT drops  $V_{O(SC2)}$  below the BAT voltage, the OUT output is turned off if the overload exists after  $t_{DGL(SC2)}$ . The short circuit recovery timer then starts counting. After  $t_{REC(SC2)}$ , OUT turns on and attempts to restart. If the short circuit remains, OUT is turned off and the counter restarts. Battery termination is disabled while in supplement mode.

## Feature Description (continued)

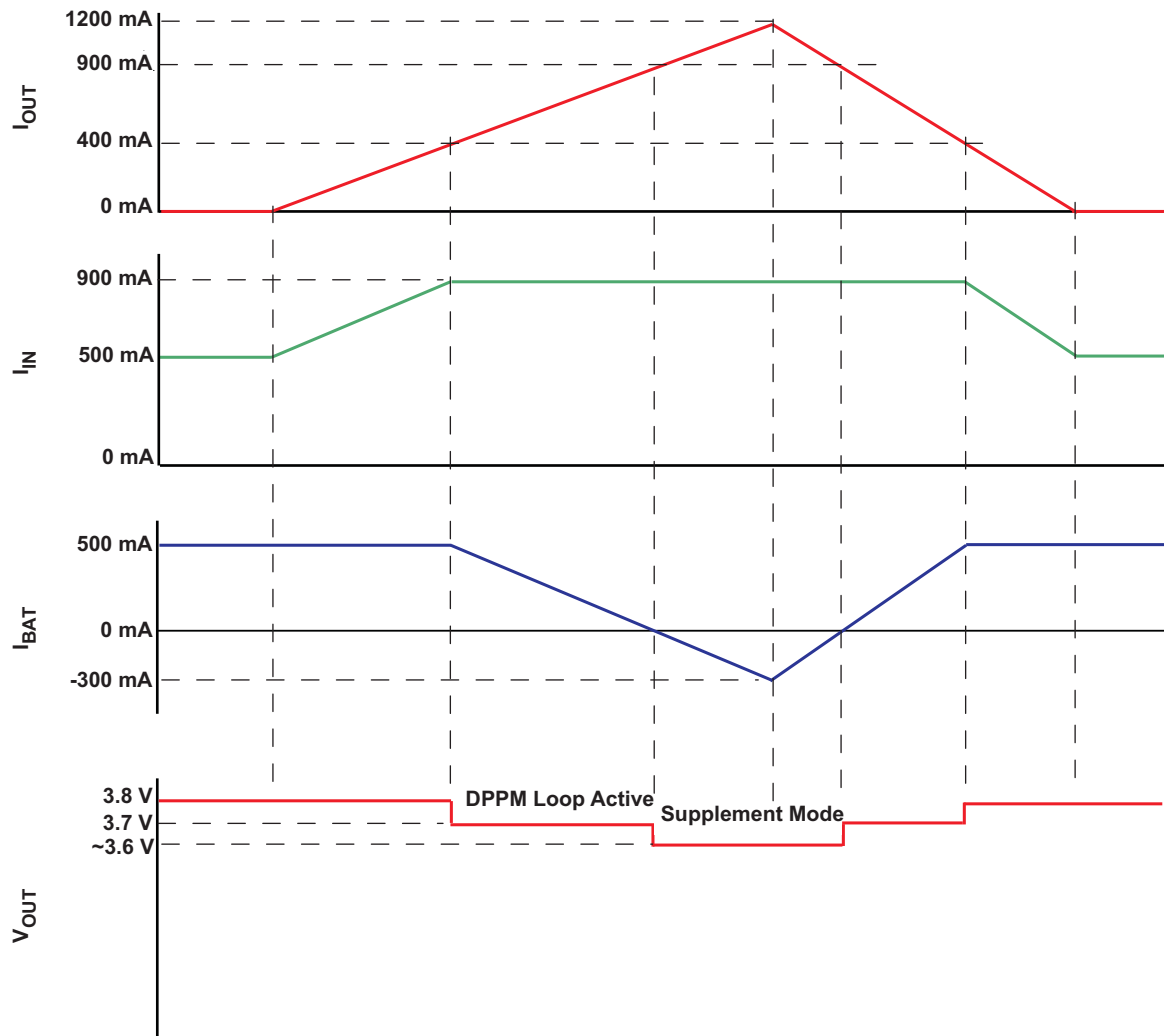


Figure 19. BQ24072 DPM and Battery Supplement Modes ( $V_{OREG} = V_{BAT} + 225 \text{ mV}$ ,  $V_{BAT} = 3.6 \text{ V}$ )

## Feature Description (continued)

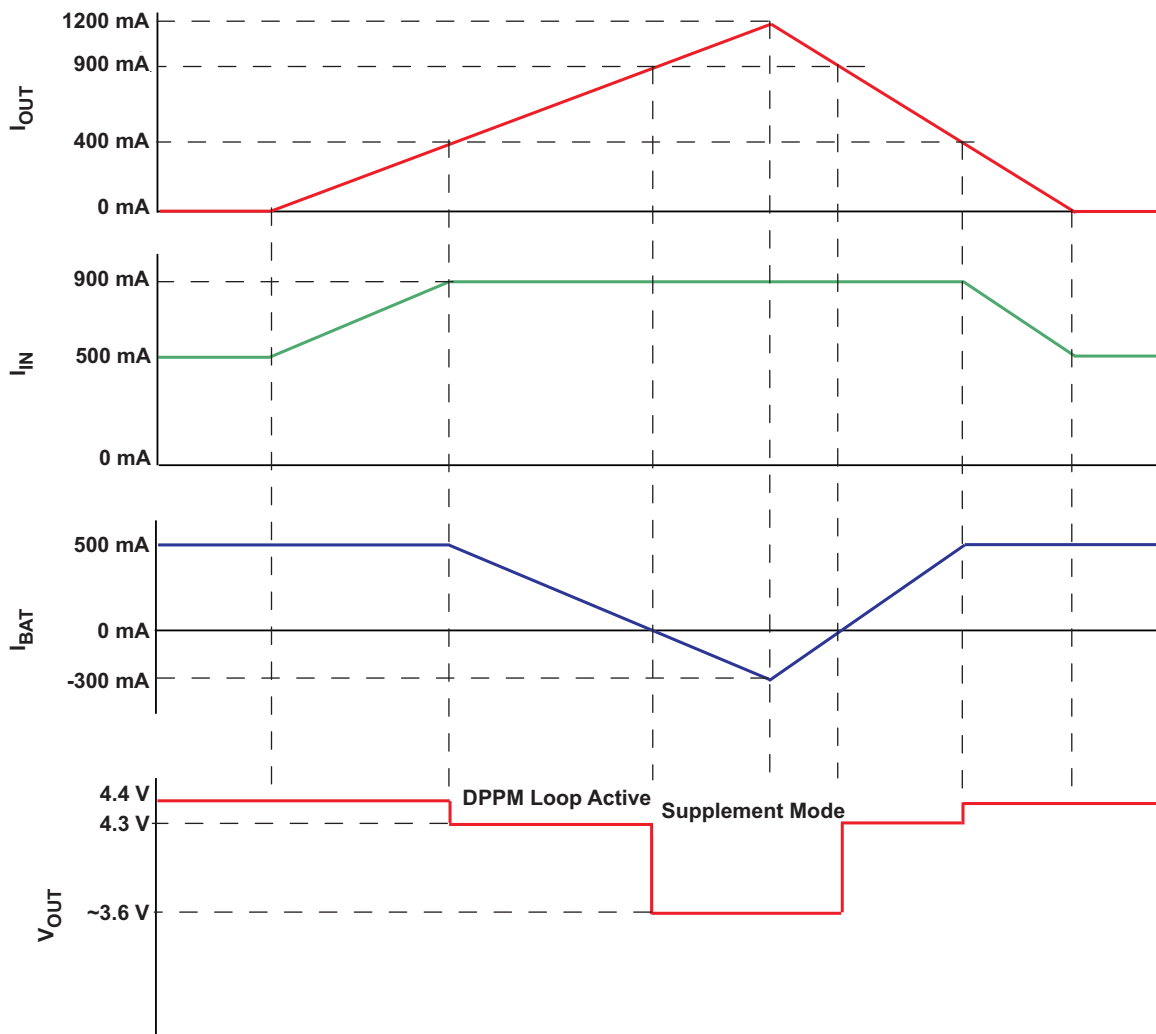


Figure 20. BQ24073 DPPM and Battery Supplement Modes ( $V_{OREG} = 4.4 \text{ V}$ ,  $V_{BAT} = 3.6 \text{ V}$ )

### 9.3.4.2 Input Source Not Connected

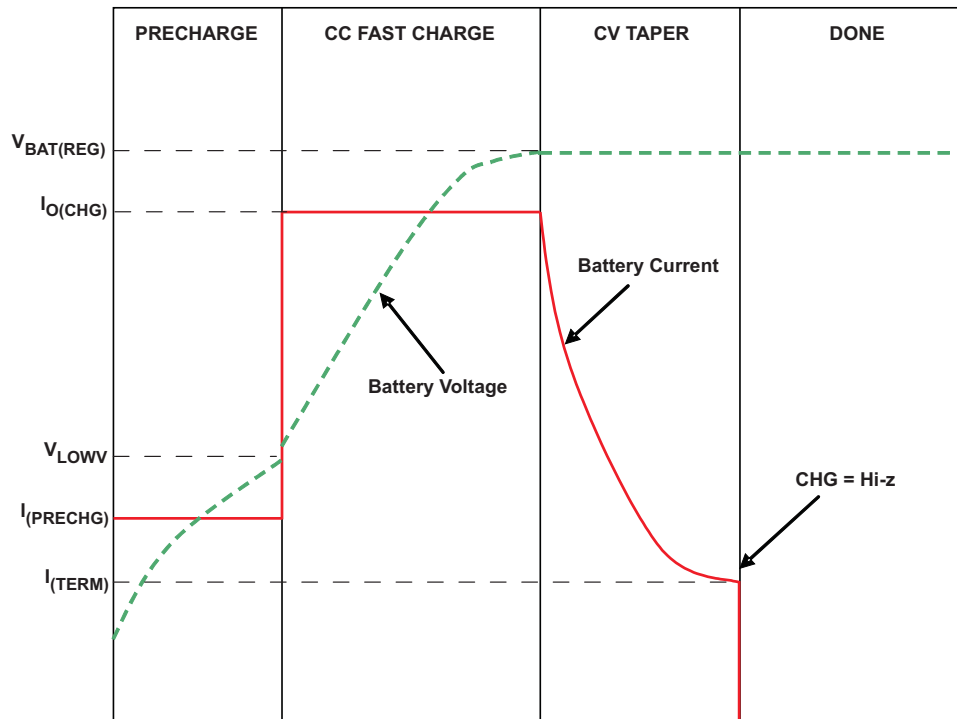
When no source is connected to the IN input, OUT is powered strictly from the battery. During this mode the current into OUT is not regulated, similar to *Battery Supplement Mode*, however the short circuit circuitry is active. If the OUT voltage falls below the BAT voltage by 250 mV for longer than  $t_{DGL(SC2)}$ , OUT is turned off. The short circuit recovery timer then starts counting. After  $t_{REC(SC2)}$ , OUT turns on and attempts to restart. If the short circuit remains, OUT is turned off and the counter restarts. This ON/OFF cycle continues until the overload condition is removed.

### 9.3.5 Battery Charging

Set  $\overline{CE}$  low to initiate battery charging. First, the device checks for a short-circuit on the BAT pin by sourcing  $I_{BAT(SC)}$  to the battery and monitoring the voltage. When the BAT voltage exceeds  $V_{BAT(SC)}$ , the battery charging continues. The battery is charged in three phases: conditioning pre-charge, constant current fast charge (current regulation) and a constant voltage tapering (voltage regulation). In all charge phases, an internal control loop monitors the IC junction temperature and reduces the charge current if an internal temperature threshold is exceeded.

Figure 21 illustrates a normal Li-Ion charge cycle using the BQ2407x:

## Feature Description (continued)



**Figure 21. Typical Charge Cycle**

In the pre-charge phase, the battery is charged at with the pre-charge current ( $I_{PRECHG}$ ). Once the battery voltage crosses the  $V_{LOWV}$  threshold, the battery is charged with the fast-charge current ( $I_{CHG}$ ). As the battery voltage reaches  $V_{BAT(REG)}$ , the battery is held at a constant voltage of  $V_{BAT(REG)}$  and the charge current tapers off as the battery approaches full charge. When the battery current reaches  $I_{TERM}$ , the  $\overline{CHG}$  pin indicates *charging done* by going high-impedance.

Note that termination detection is disabled whenever the charge rate is reduced because of the actions of the thermal loop, the DPPM loop or the  $V_{IN-DPM}$  loop.

The value of the fast-charge current is set by the resistor connected from the ISET pin to VSS, and is given by the equation:

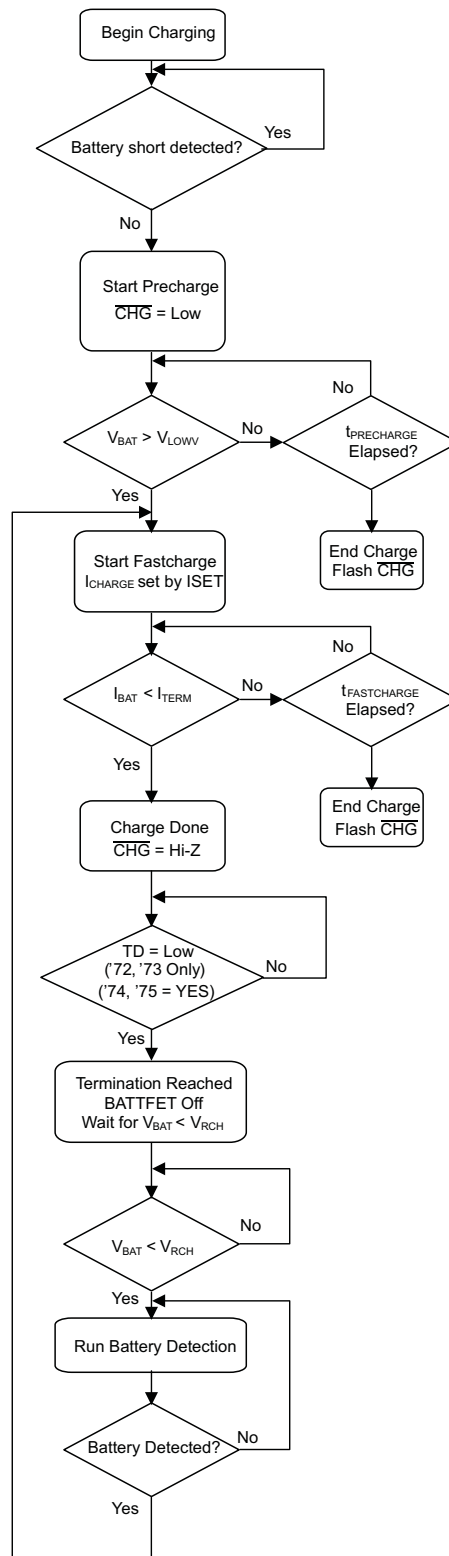
$$I_{CHG} = K_{ISET}/R_{ISET} \quad (2)$$

The charge current limit is adjustable up to 1.5 A. The valid resistor range is 590  $\Omega$  to 8.9 k $\Omega$ . If  $I_{CHG}$  is programmed as greater than the input current limit, the battery will not charge at the rate of  $I_{CHG}$ , but at the slower rate of  $I_{IN(MAX)}$  (minus the load current on the OUT pin, if any). In this case, the charger timers will be proportionately slowed down.

### 9.3.5.1 Charge Current Translator

When the charger is enabled, internal circuits generate a current proportional to the charge current at the ISET input. The current out of ISET is 1/400 ( $\pm 10\%$ ) of the charge current. This current, when applied to the external charge current programming resistor,  $R_{ISET}$ , generates an analog voltage that can be monitored by an external host to calculate the current sourced from BAT.

$$V_{ISET} = I_{CHARGE} / 400 \times R_{ISET} \quad (3)$$

**Feature Description (continued)**

**Figure 22. Battery Charging Flow Diagram**



## Feature Description (continued)

### 9.3.5.2 Adjustable Termination Threshold (ITERM Input, BQ24074)

The termination current threshold in the BQ24074 is user-programmable. Set the termination current by connecting a resistor from ITERM to VSS. For USB100 mode (EN1 = EN2 = Low), the termination current value is calculated as:

$$I_{TERM} = 0.01 \times R_{ITERM} / R_{ISET} \quad (4)$$

In the other input current limit modes (EN1 ≠ EN2), the termination current value is calculated as:

$$I_{TERM} = 0.03 \times R_{ITERM} / R_{ISET} \quad (5)$$

The termination current is programmable up to 50% of the fastcharge current. The R<sub>ITERM</sub> resistor must be less than 15 kΩ. Leave ITERM unconnected to select the default internally set termination current.

### 9.3.5.3 Termination Disable (TD Input, BQ24072, BQ24073)

The BQ24072 and BQ24073 contain a TD input that allows termination to be enabled/ disabled. Connect TD to a logic high to disable charge termination. When termination is disabled, the device goes through the pre-charge, fast-charge and CV phases, then remains in the CV phase. During the CV phase, the charger maintains the output voltage at BAT equal to V<sub>BAT(REG)</sub>, and charging current does not terminate. The charge current is set by I<sub>CHG</sub> or I<sub>INmax</sub>, whichever is less. Battery detection is not performed. The  $\overline{CHG}$  output is high impedance once the current falls below I<sub>TERM</sub> and does not go low until the input power or  $\overline{CE}$  are toggled. When termination is disabled, the pre-charge and fast-charge safety timers are also disabled. Battery pack temperature sensing (TS pin functionality) is disabled if the TD pin is high and the TS pin is unconnected or pulled up to V<sub>IN</sub>.

### 9.3.5.4 Battery Detection and Recharge

The BQ2407x automatically detects if a battery is connected or removed. Once a charge cycle is complete, the battery voltage is monitored. When the battery voltage falls below V<sub>RCH</sub>, the battery detection routine is run. During battery detection, current (I<sub>BAT(DET)</sub>) is pulled from the battery for a duration t<sub>DET</sub> to see if the voltage on BAT falls below V<sub>LOWV</sub>. If not, charging begins. If it does, then it indicates that the battery is missing or the protector is open. Next, the precharge current is applied for t<sub>DET</sub> to close the protector if possible. If V<sub>BAT</sub> < V<sub>RCH</sub>, then the protector closed and charging is initiated. If V<sub>BAT</sub> > V<sub>RCH</sub>, then the battery is determined to be missing and the detection routine continues.

### 9.3.5.5 Battery Disconnect (SYSOFF Input, BQ24075, BQ24079)

The BQ24075 and BQ24079 feature a SYSOFF input that allows the user to turn the FET Q2 off and disconnect the battery from the OUT pin. This is useful for disconnecting the system load from the battery, factory programming where the battery is not installed or for host side impedance track fuel gauging, such as bq27500, where the battery open circuit voltage level must be detected before the battery charges or discharges. The /CHG output remains low when SYSOFF is high. Connect SYSOFF to VSS, to turn Q2 on for normal operation. SYSOFF is internally pulled to VBAT through ~5 MΩ resistor.

### 9.3.5.6 Dynamic Charge Timers (TMR Input)

The BQ2407x devices contain internal safety timers for the pre-charge and fast-charge phases to prevent potential damage to the battery and the system. The timers begin at the start of the respective charge cycles. The timer values are programmed by connecting a resistor from TMR to VSS. The resistor value is calculated using the following equation:

$$t_{PRECHG} = K_{TMR} \times R_{TMR} \quad (6)$$

$$t_{MAXCHG} = 10 \times K_{TMR} \times R_{TMR} \quad (7)$$

Leave TMR unconnected to select the internal default timers. Disable the timers by connecting TMR to VSS.

Reset the timers by toggling the CE pin, or by toggling EN1, EN2 pin to put the device in and out of USB suspend mode (EN1 = HI, EN2 = HI).

Note that timers are suspended when the device is in thermal shutdown, and the timers are slowed proportionally to the charge current when the device enters thermal regulation. For the BQ24072 and BQ24073, the timers are disabled when TD is connected to a high logic level.

During the fast charge phase, several events increase the timer durations.

## Feature Description (continued)

- The system load current activates the DPPM loop which reduces the available charging current
- The input current is reduced because the input voltage has fallen to  $V_{IN-DPM}$
- The device has entered thermal regulation because the IC junction temperature has exceeded  $T_{J(REG)}$

During each of these events, the internal timers are slowed down proportionately to the reduction in charging current. For example, if the charging current is reduced by half for two minutes, the timer clock is reduced to half the frequency and the counter counts half as fast resulting in only one minute of "counting" time.

If the pre charge timer expires before the battery voltage reaches  $V_{LOWV}$ , the BQ2407x indicates a fault condition. Additionally, if the battery current does not fall to  $I_{TERM}$  before the fast charge timer expires, a fault is indicated. The  $\overline{CHG}$  output flashes at approximately 2 Hz to indicate a fault condition. The fault condition is cleared by toggling  $\overline{CE}$  or the input power, entering/ exiting USB suspend mode, or an OVP event.

### 9.3.5.7 Status Indicators ( $\overline{PGOOD}$ , $\overline{CHG}$ )

The BQ2407x contains two open-drain outputs that signal its status. The  $\overline{PGOOD}$  output signals when a valid input source is connected.  $\overline{PGOOD}$  is low when  $(V_{BAT} + V_{IN(DT)}) < V_{IN} < V_{OVP}$ . When the input voltage is outside of this range,  $\overline{PGOOD}$  is high impedance.

The charge cycle after power-up,  $\overline{CE}$  going low, or exiting OVP is indicated with the  $\overline{CHG}$  pin on (low - LED on), whereas all refresh (subsequent) charges will result in the  $\overline{CHG}$  pin off (open - LED off). In addition, the  $\overline{CHG}$  signals timer faults by flashing at approximately 2 Hz.

**Table 2.  $\overline{PGOOD}$  Status Indicator**

INPUT STATE	$\overline{PGOOD}$ OUTPUT
$V_{IN} < V_{UVLO}$	High-impedance
$V_{UVLO} < V_{IN} < V_{BAT} + V_{IN(DT)}$	High-impedance
$V_{BAT} + V_{IN(DT)} < V_{IN} < V_{OVP}$	Low
$V_{IN} > V_{OVP}$	High-impedance

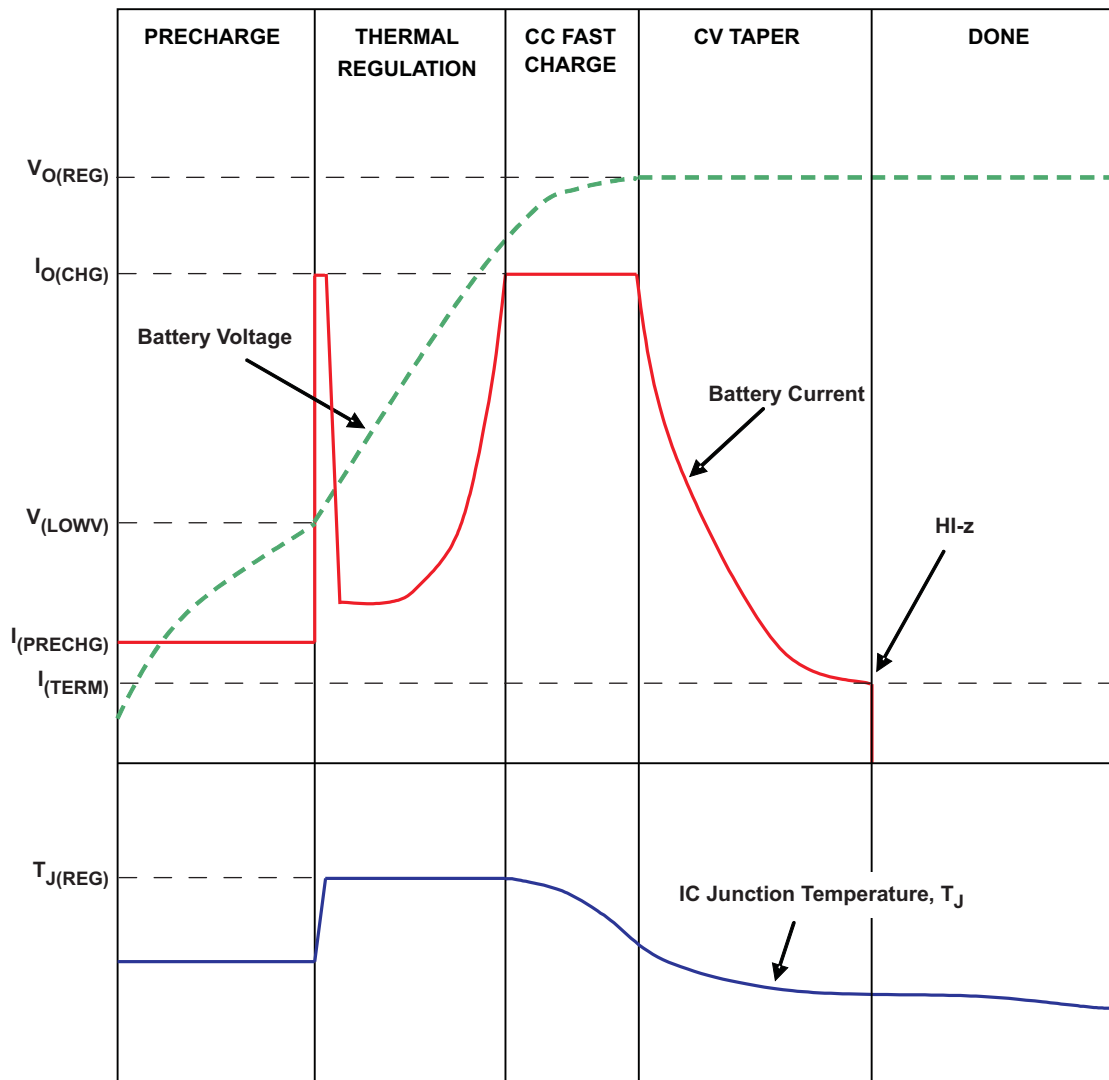
**Table 3.  $\overline{CHG}$  Status Indicator**

CHARGE STATE	$\overline{CHG}$ OUTPUT
Charging	Low (for first charge cycle)
Charging suspended by thermal loop	
Safety timers expired	Flashing at 2 Hz
Charging done	High-impedance
Recharging after termination	
IC disabled or no valid input power	
Battery absent	

### 9.3.5.8 Thermal Regulation and Thermal Shutdown

The BQ2407x contain a thermal regulation loop that monitors the die temperature. If the temperature exceeds  $T_{J(REG)}$ , the device automatically reduces the charging current to prevent the die temperature from increasing further. In some cases, the die temperature continues to rise despite the operation of the thermal loop, particularly under high  $V_{IN}$  and heavy OUT system load conditions. Under these conditions, if the die temperature increases to  $T_{J(OFF)}$ , the input FET Q1 is turned OFF. FET Q2 is turned ON to ensure that the battery still powers the load on OUT. Once the device die temperature cools by  $T_{J(OFF-HYS)}$ , the input FET Q1 is turned on and the device returns to thermal regulation. Continuous overtemperature conditions result in a "hiccup" mode. During thermal regulation, the safety timers are slowed down proportionately to the reduction in current limit.

Note that this feature monitors the die temperature of the BQ2407x. This is not synonymous with ambient temperature. Self heating exists due to the power dissipated in the IC because of the linear nature of the battery charging algorithm and the LDO associated with OUT. A modified charge cycle with the thermal loop active is shown in [Figure 23](#). Battery termination is disabled during thermal regulation.



**Figure 23. Charge Cycle Modified by Thermal Loop**

### 9.3.6 Battery Pack Temperature Monitoring

The BQ2407x features an external battery pack temperature monitoring input. The TS input connects to the NTC thermistor in the battery pack to monitor battery temperature and prevent dangerous over-temperature conditions. During charging,  $I_{NTC}$  is sourced to TS and the voltage at TS is continuously monitored. If, at any time, the voltage at TS is outside of the operating range ( $V_{COLD}$  to  $V_{HOT}$ ), charging is suspended. The timers maintain their values but suspend counting. When the voltage measured at TS returns to within the operation window, charging is resumed and the timers continue counting. When charging is suspended due to a battery pack temperature fault, the CHG pin remains low and continues to indicate charging.

For the BQ24072 and BQ24073, battery pack temperature sensing is disabled when termination is disabled ( $TD = High$ ) and the voltage at TS is greater than  $V_{DIS(TS)}$ . For applications that do not require the TS monitoring function, connect a 10-k $\Omega$  resistor from TS to VSS to set the TS voltage at a valid level and maintain charging.

The allowed temperature range for 103AT-2 type thermistor is 0°C to 50°C. However, the user may increase the range by adding two external resistors. See Figure 24 for the circuit details. The values for  $R_s$  and  $R_p$  are calculated using the following equations:

$$R_s = \frac{-(R_{TH} + R_{TC}) \pm \sqrt{(R_{TH} + R_{TC})^2 - 4 \left\{ R_{TH} \times R_{TC} + \frac{V_H \times V_C}{(V_H - V_C) \times I_{TS}} \times (R_{TC} - R_{TH}) \right\}}}{2} \quad (8)$$

$$R_p = \frac{V_H \times (R_{TH} + R_s)}{I_{TS} \times (R_{TH} + R_s) - V_H}$$

where

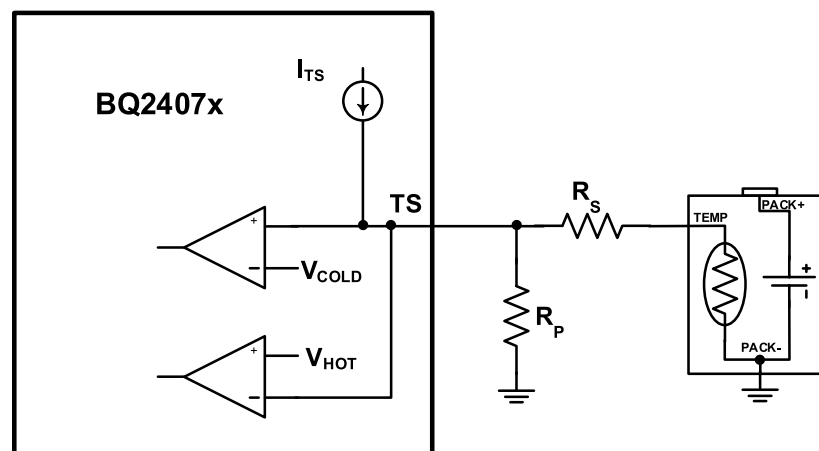
- $R_{TH}$ : Thermistor Hot Trip Value found in thermistor data sheet
  - $R_{TC}$ : Thermistor Cold Trip Value found in thermistor data sheet
  - $V_H$ : IC's Hot Trip Threshold = 0.3 V nominal
  - $V_C$ : IC's Cold Trip Threshold = 2.1 V nominal
  - $I_{TS}$ : IC's Output Current Bias = 75  $\mu$ A nominal
  - NTC Thermistor Semitec 103AT-4
- (9)

$R_s$  and  $R_p$  1% values were chosen closest to calculated values in [Table 4](#).

**Table 4. Calculated Values**

Cold Temp Resistance and Trip Threshold; $\Omega$ ( $^{\circ}$ C)	Hot Temp Resistance and Trip Threshold; $\Omega$ ( $^{\circ}$ C)	External Bias Resistor, $R_s$ ( $\Omega$ )	External Bias Resistor, $R_p$ ( $\Omega$ )
28000 (–0.6)	4000 (51)	0	$\infty$
28480 (–1)	3536 (55)	487	845000
28480 (–1)	3021 (60)	1000	549000
33890 (–5)	4026 (51)	76.8	158000
33890 (–5)	3536 (55)	576	150000
33890 (–5)	3021 (60)	1100	140000

RHOT and RCOLD are the thermistor resistance at the desired hot and cold temperatures, respectively. The temperature window cannot be tightened more than using only the thermistor connected to TS, it can only be extended.



**Figure 24. Extended TS Pin Thresholds**

## 9.4 Device Functional Modes

### 9.4.1 Sleep Mode

When the input is between UVLO and  $V_{IN(DT)}$ , the device enters sleep mode. After entering sleep mode for >20 mS the internal FET connection between the IN and OUT pin is disabled and pulling the input to ground will not discharge the battery, other than the leakage on the BAT pin. If one has a full 1000-mAhr battery and the leakage is 10  $\mu$ A, then it would take 1000 mAhr / 10  $\mu$ A = 100000 hours (11.4 years) to discharge the battery. The self-discharge of the battery is typically five times higher than this.

### 9.4.2 Explanation of Deglitch Times and Comparator Hysteresis

#### NOTE

Figure 25 to Figure 29 are not to scale.

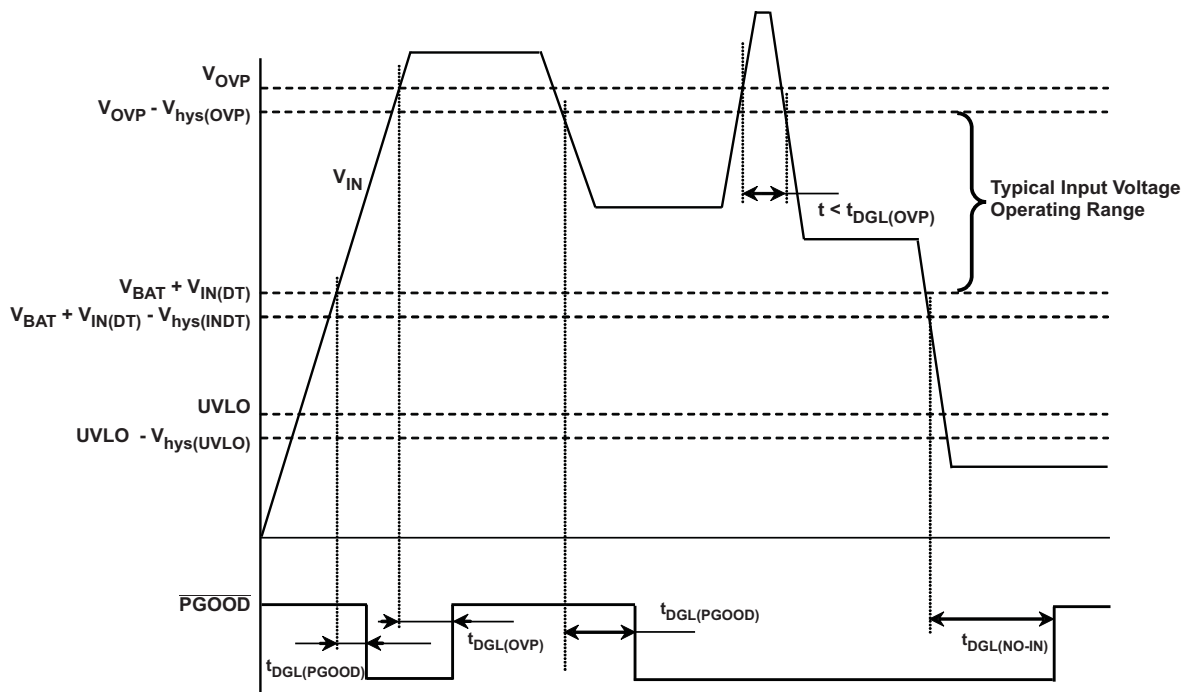


Figure 25. Power-Up, Power-Down, Power Good Indication

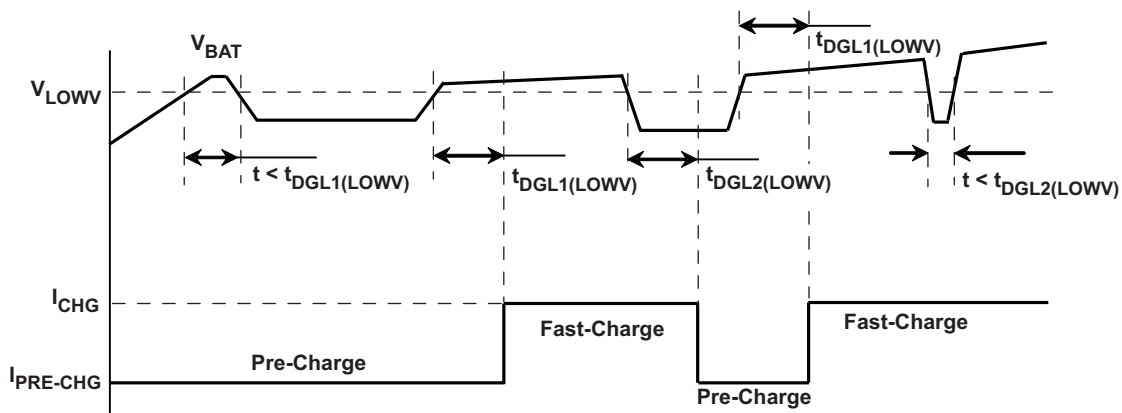
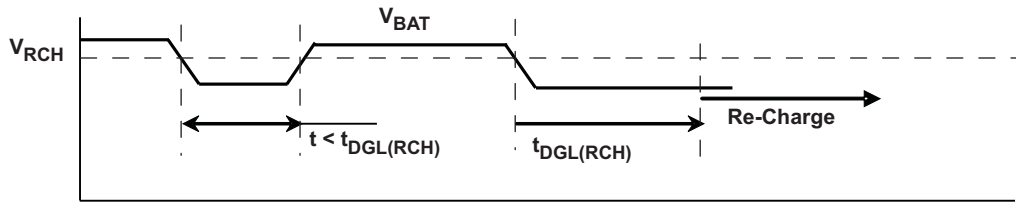
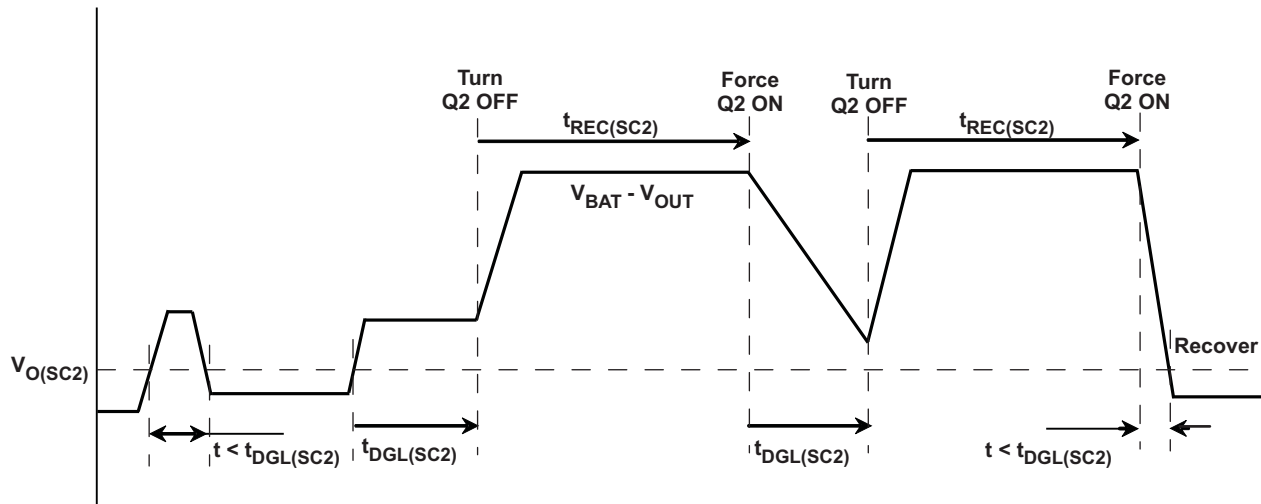


Figure 26. Precharge to Fast-Charge, Fast- to Pre-Charge Transition –  $t_{DGL1(LOWV)}$ ,  $t_{DGL2(LOWV)}$

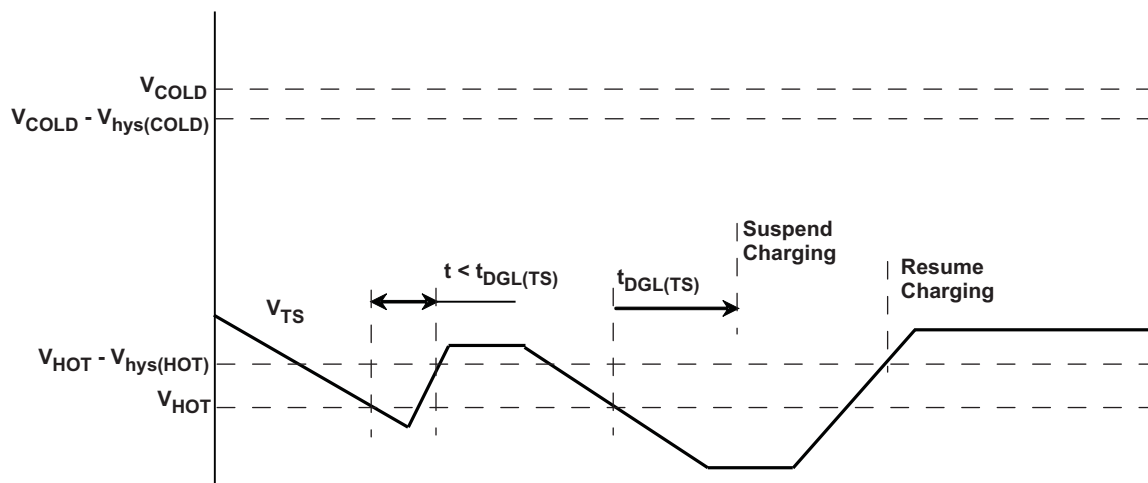
## Device Functional Modes (continued)



**Figure 27. Recharge –  $t_{DGL(RCH)}$**



**Figure 28. OUT Short-Circuit – Supplement Mode**



**Figure 29. Battery Pack Temperature Sensing – TS Pin. Battery Temperature Increasing**

## 10 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

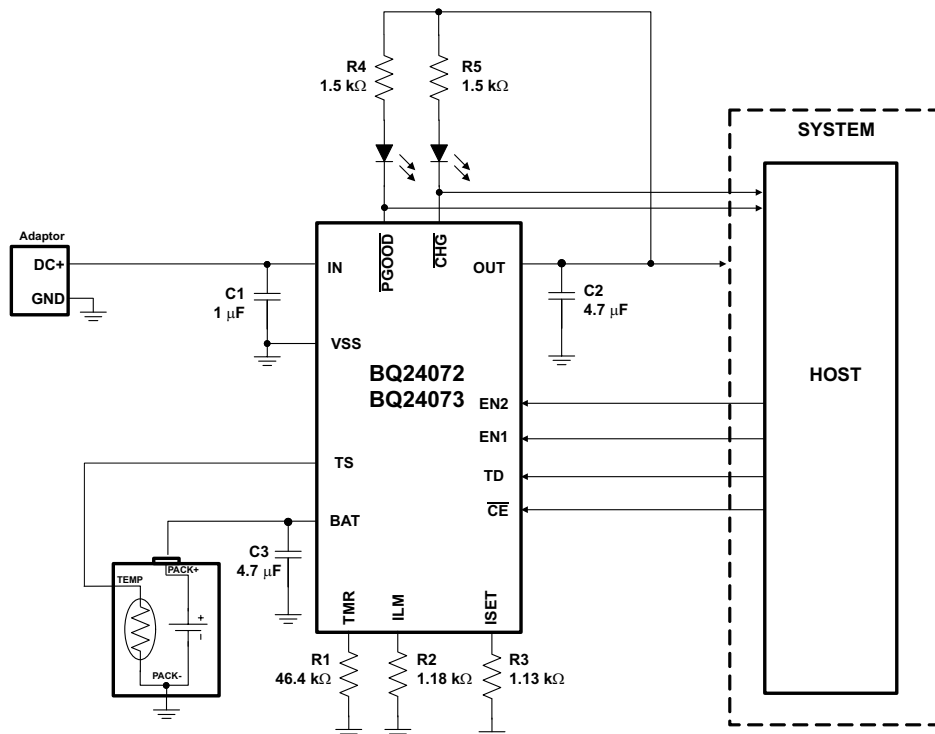
### 10.1 Application Information

The BQ2407x devices power the system while simultaneously and independently charging the battery. The input power source for charging the battery and running the system can be an AC adapter or a USB port. The devices feature dynamic power-path management (DPPM), which shares the source current between the system and battery charging and automatically reduces the charging current if the system load increases. When charging from a USB port, the input dynamic power management (VIN-DPM) circuit reduces the input current limit if the input voltage falls below a threshold, preventing the USB port from crashing. The power-path architecture also permits the battery to supplement the system current requirements when the adapter cannot deliver the peak system currents.

The BQ2407x is configurable to be host controlled for selecting different input current limits based on the input source connected, or a fully stand alone device for applications that do not support multiple types of input sources.

### 10.2 Typical Application

$V_{IN} = UVLO$  to  $V_{OVP}$ ,  $I_{FASTCHG} = 800$  mA,  $I_{IN(MAX)} = 1.3$  A, Battery Temperature Charge Range =  $0^{\circ}\text{C}$  to  $50^{\circ}\text{C}$ , 6.25-hour Fastcharge Safety Timer



**Figure 30. Using BQ24072/ BQ24073 in a Host-Controlled Charger Application**

## Typical Application (continued)

### 10.2.1 Design Requirements

- Supply voltage = 5 V
- Fast charge current of approximately 800 mA; ISET - pin 16
- Input Current Limit = 1.3 A; ILIM - pin 12
- Termination Current Threshold = 110 mA; ITERM – pin 15 (BQ24074 only)
- Safety timer duration, Fast-Charge = 6.25 hours; TMR – pin 14
- TS – Battery Temperature Sense = 10 kΩ NTC (103AT-2)

### 10.2.2 Detailed Design Procedure

#### 10.2.2.1 BQ2407x Charger Design Example

See [Figure 30](#) to [Figure 42](#) for Schematics of the Design Example.

##### 10.2.2.1.1 Termination Disable (TD) (BQ24072, BQ24073 only)

Connect TD high to disable termination. Connect TD low to enable termination.

##### 10.2.2.1.2 System ON/OFF (SYSOFF) (BQ24075 or BQ24079 only)

Connect SYSOFF high to disconnect the battery from the system load. Connect SYSOFF low for normal operation

#### 10.2.2.2 Calculations

##### 10.2.2.2.1 Program the Fast Charge Current (ISET):

$$R_{ISET} = K_{ISET} / I_{CHG}$$

$K_{ISET} = 890 \text{ A}\Omega$  from the electrical characteristics table.

$$R_{ISET} = 890 \text{ A}\Omega / 0.8 \text{ A} = 1.1125 \text{ k}\Omega$$

Select the closest standard value, which for this case is 1.13 kΩ. Connect this resistor between ISET (pin 16) and  $V_{SS}$ .

##### 10.2.2.2.2 Program the Input Current Limit (ILIM)

$$R_{ILIM} = K_{ILIM} / I_{L\_MAX}$$

$K_{ILIM} = 1550 \text{ A}\Omega$  from the electrical characteristics table.

$$R_{ISET} = 1550 \text{ A}\Omega / 1.3 \text{ A} = 1.192 \text{ k}\Omega$$

Select the closest standard value, which for this case is 1.18 kΩ. Connect this resistor between ILIM (pin 12) and  $V_{SS}$ .

##### 10.2.2.2.3 Program the Termination Current Threshold ( $I_{TERM}$ ) (BQ24074 only)

$$R_{ITERM} = I_{TERM} \times R_{ISET} / 0.030$$

$R_{ISET} = 1.13 \text{ k}\Omega$  from the above calculation.

$$R_{ITERM} = 110 \text{ mA} \times 1.13 \text{ k}\Omega / 0.030 = 4.143 \text{ k}\Omega$$

Select the closest standard value, which for this case is 4.12 kΩ. Connect this resistor between ITERM (pin 15) and  $V_{SS}$ . Note that when in USB100 mode ( $EN1 = EN2 = V_{SS}$ ), the termination threshold is 1/3 of the normal threshold.

##### 10.2.2.2.4 Program 6.25-hour Fast-Charge Safety Timer (TMR)

$$R_{TMR} = t_{MAXCHG} / (10 \times K_{TMR})$$

$K_{TMR} = 48 \text{ s/k}\Omega$  from the electrical characteristics table.

$$R_{TMR} = (6.25 \text{ hr} \times 3600 \text{ s/hr}) / (10 \times 48 \text{ s/k}\Omega) = 46.8 \text{ k}\Omega$$

Select the closest standard value, which for this case is 46.4 kΩ. Connect this resistor between TMR (pin 2) and  $V_{SS}$ .



## Typical Application (continued)

### 10.2.2.3 TS Function

Use a 10-k $\Omega$  NTC thermistor in the battery pack (103AT-2). For applications that do not require the TS monitoring function, connect a 10-k $\Omega$  resistor from TS to VSS to set the TS voltage at a valid level and maintain charging.

### 10.2.2.4 $\overline{CHG}$ and $\overline{PGOOD}$

LED Status: Connect a 1.5-k $\Omega$  resistor in series with a LED between OUT and  $\overline{CHG}$  to indicate charging status. Connect a 1.5-k $\Omega$  resistor in series with a LED between OUT and  $\overline{PGOOD}$  to indicate when a valid input source is connected.

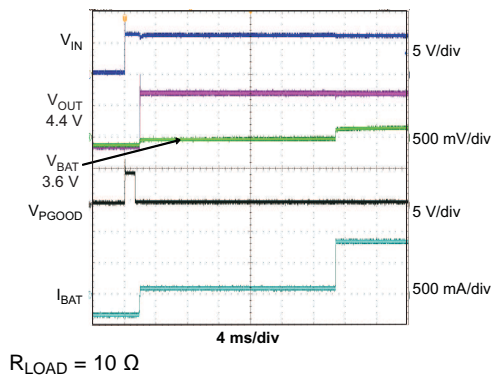
Processor Monitoring Status: Connect a pullup resistor (on the order of 100 k $\Omega$ ) between the power rail of the processor and  $\overline{CHG}$  and  $\overline{PGOOD}$ .

### 10.2.2.5 Selecting IN, OUT, and BAT Pin Capacitors

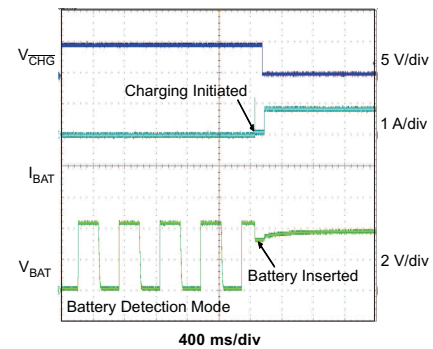
In most applications, all that is needed is a high-frequency decoupling capacitor (ceramic) on the power pin, input, output and battery pins. Using the values shown on the application diagram, is recommended. After evaluation of these voltage signals with real system operational conditions, one can determine if capacitance values can be adjusted toward the minimum recommended values (DC load application) or higher values for fast high amplitude pulsed load applications. Note if designed high input voltage sources (bad adaptors or wrong adaptors), the capacitor needs to be rated appropriately. Ceramic capacitors are tested to 2x their rated values so a 16-V capacitor may be adequate for a 30-V transient (verify tested rating with capacitor manufacturer).

## Typical Application (continued)

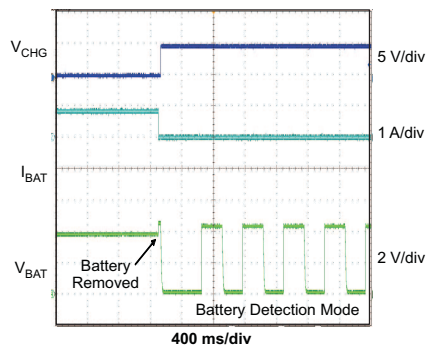
### 10.2.3 Application Curves



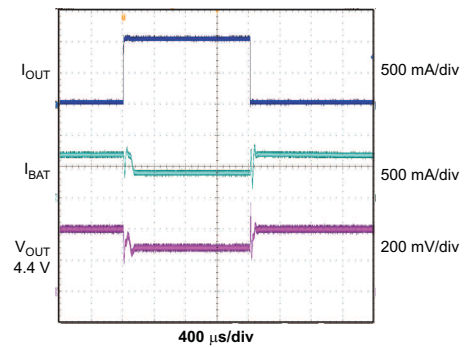
**Figure 31. Adapter Plug-In  
Battery Connected**



**Figure 32. Battery Detection  
Battery Inserted**

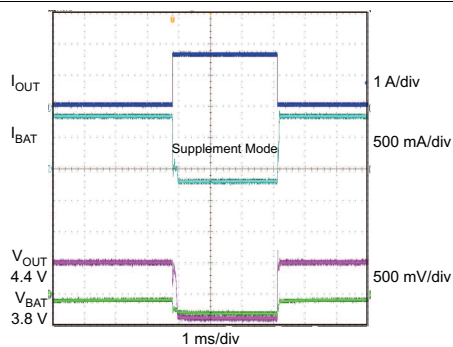


**Figure 33. Battery Detection  
Battery Removed**

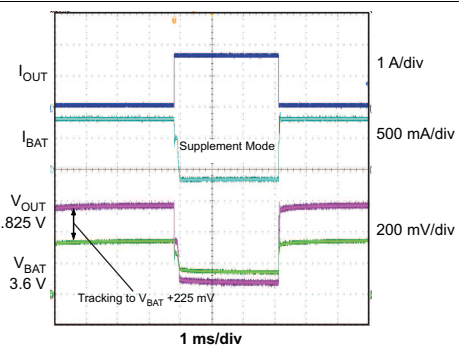


$R_{LOAD} = 20\ \Omega$  to  $9\ \Omega$

**Figure 34. Entering and Exiting DPPM Mode**

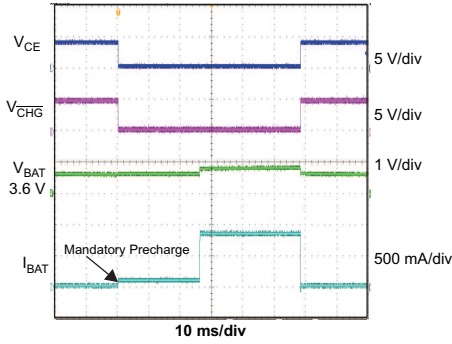


**Figure 35. Entering and Exiting Battery Supplement Mode  
BQ24074**

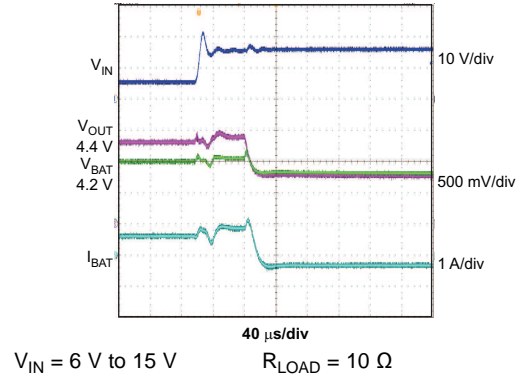


**Figure 36. Entering and Exiting Battery Supplement Mode  
BQ24072**

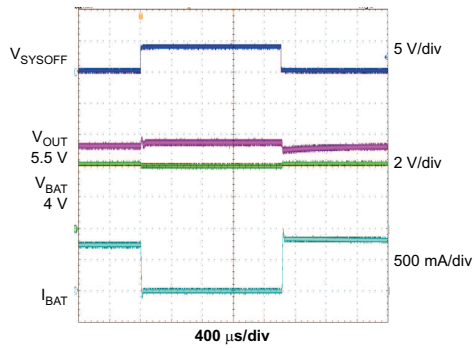
## Typical Application (continued)



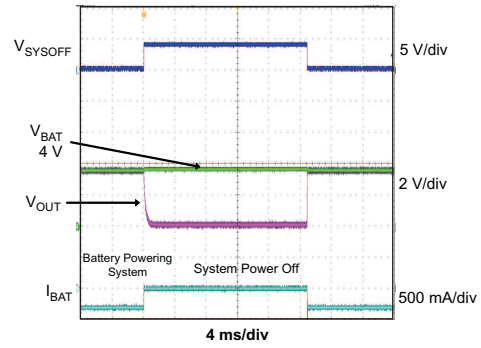
**Figure 37. Charger ON/OFF Using  $\overline{CE}$**



**Figure 38. OVP Fault**



**Figure 39. System ON/OFF With Input Connected**  
 $V_{IN} = 6\text{ V}$   
**BQ24075, BQ24079**



**Figure 40. System ON/OFF With Input Not Connected**  
 $V_{IN} = 0\text{ V}$   
**BQ24075, BQ24079**

## 10.3 System Examples

### 10.3.1 Standalone Charger

$V_{IN}$  = UVLO to  $V_{OVP}$ ,  $I_{FASTCHG}$  = 800 mA,  $I_{IN(MAX)}$  = 1.3 A,  $I_{TERM}$  = 110 mA, Battery Temperature Charge Range = 0°C to 50°C, Safety Timers disabled.

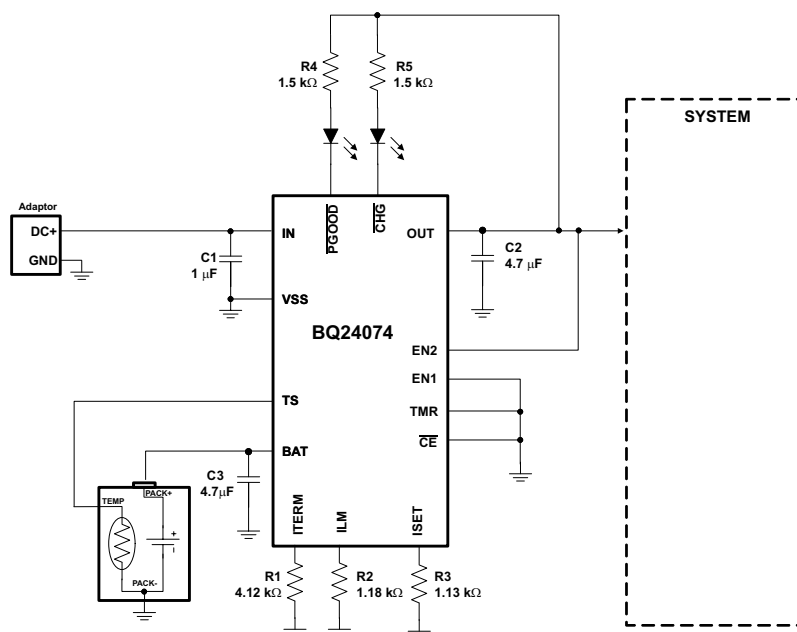


Figure 41. Using BQ24074 in a Standalone Charger Application

### 10.3.2 Disconnecting the Battery From the System

$V_{IN}$  = UVLO to  $V_{OVP}$ ,  $I_{FASTCHG}$  = 800 mA,  $I_{IN(MAX)}$  = 1.3 A, Battery Temperature Charge Range = 0°C to 50°C, 6.25 hour Fastcharge Safety Timer.

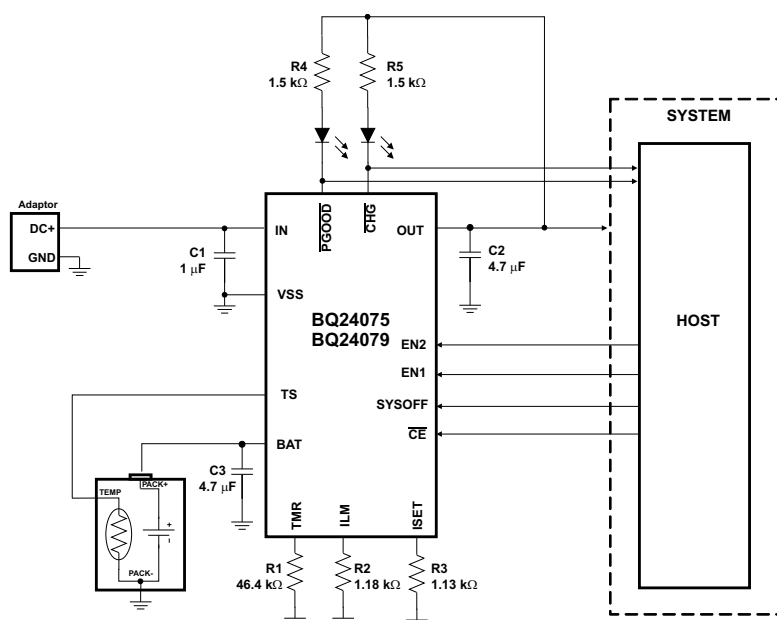


Figure 42. Using BQ24075 or BQ24079 to Disconnect the Battery From the System

## 11 Power Supply Recommendations

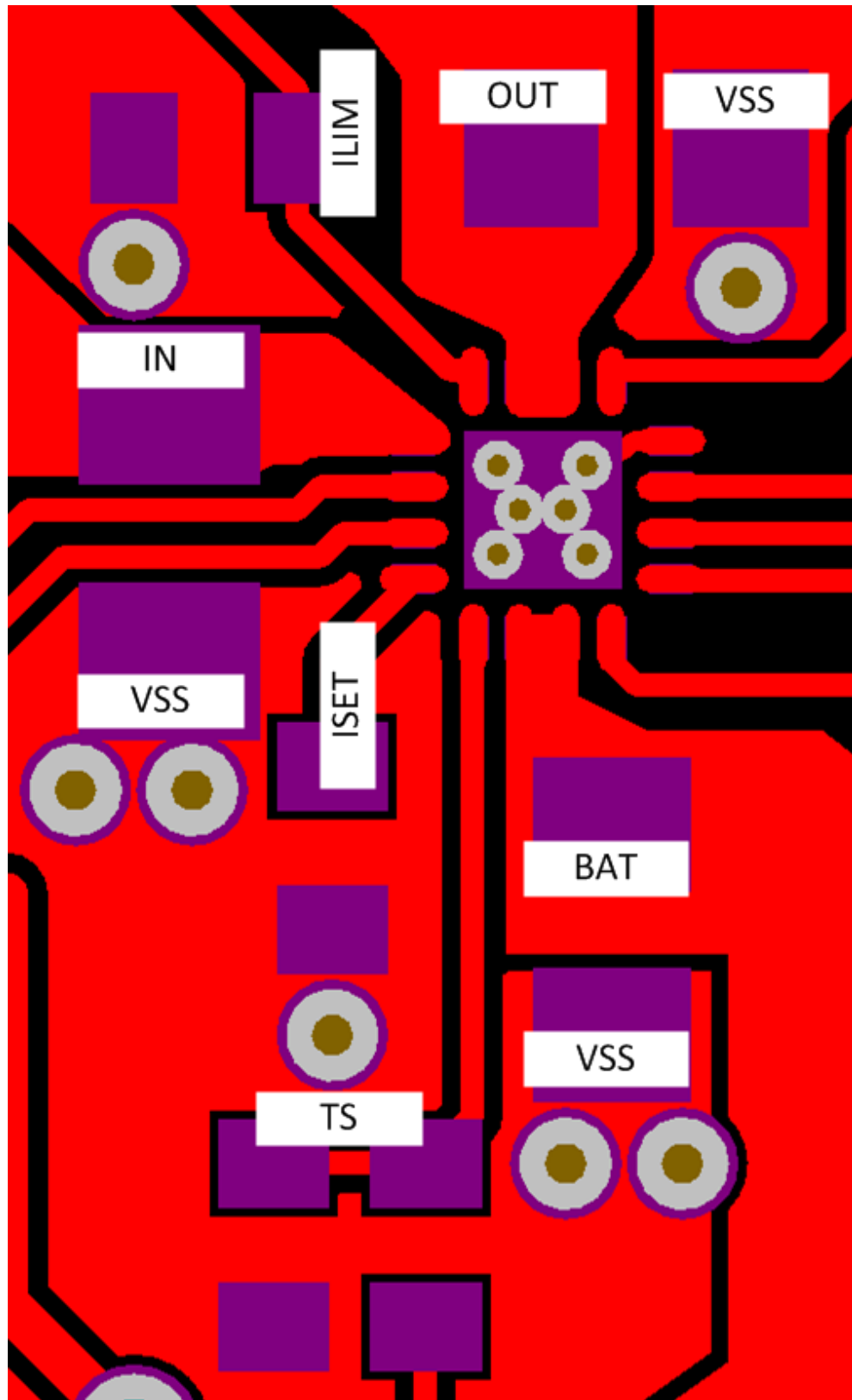
Some adapters implement a half rectifier topology, which causes the adapter output voltage to fall below the battery voltage during part of the cycle. To enable operation with adapters under those conditions, the BQ2407x family keeps the charger on for at least 20 msec (typical) after the input power puts the part in sleep mode. This feature enables use of external adapters using 50 Hz networks. The input must not drop below the UVLO voltage for the charger to work properly. Thus, the battery voltage should be above the UVLO to help prevent the input from dropping out. Additional input capacitance may be needed.

## 12 Layout

### 12.1 Layout Guidelines

- To obtain optimal performance, the decoupling capacitor from IN to GND (thermal pad) and the output filter capacitors from OUT to GND (thermal pad) should be placed as close as possible to the BQ2407x, with short trace runs to both IN, OUT and GND (thermal pad).
- All low-current GND connections should be kept separate from the high-current charge or discharge paths from the battery. Use a single-point ground technique incorporating both the small signal ground path and the power ground path.
- The high current charge paths into IN pin and from the OUT pin must be sized appropriately for the maximum charge current in order to avoid voltage drops in these traces
- The BQ2407x family is packaged in a thermally enhanced MLP package. The package includes a thermal pad to provide an effective thermal contact between the IC and the printed circuit board (PCB); this thermal pad is also the main ground connection for the device. Connect the thermal pad to the PCB ground connection. Full PCB design guidelines for this package are provided in *QFN/SON PCB Attachment Application Note* ([SLUA271](#)).

## 12.2 Layout Example



**Figure 43. Layout Schematic**

## 12.3 Thermal Considerations

The BQ24072/3/4/5 family is packaged in a thermally enhanced MLP package. The package includes a thermal pad to provide an effective thermal contact between the IC and the printed circuit board (PCB). The power pad should be directly connected to the  $V_{SS}$  pin. Full PCB design guidelines for this package are provided in *QFN/SON PCB Attachment Application Note (SLUA271)*. The most common measure of package thermal performance is thermal impedance ( $\theta_{JA}$ ) measured (or modeled) from the chip junction to the air surrounding the package surface (ambient). The mathematical expression for  $\theta_{JA}$  is:

$$\theta_{JA} = (T_J - T) / P$$

where

- $T_J$  = chip junction temperature
- $T$  = ambient temperature
- $P$  = device power dissipation

(10)

Factors that can influence the measurement and calculation of  $\theta_{JA}$  include:

- Whether or not the device is board mounted
- Trace size, composition, thickness, and geometry
- Orientation of the device (horizontal or vertical)
- Volume of the ambient air surrounding the device under test and airflow
- Whether other surfaces are in close proximity to the device being tested

Due to the charge profile of Li-Ion batteries the maximum power dissipation is typically seen at the beginning of the charge cycle when the battery voltage is at its lowest. Typically after fast charge begins the pack voltage increases to  $\approx 3.4$  V within the first 2 minutes. The thermal time constant of the assembly typically takes a few minutes to heat up so when doing maximum power dissipation calculations, 3.4 V is a good minimum voltage to use. This is verified, with the system and a fully discharged battery, by plotting temperature on the bottom of the PCB under the IC (pad should have multiple vias), the charge current and the battery voltage as a function of time. The fast charge current will start to taper off if the part goes into thermal regulation.

The device power dissipation,  $P$ , is a function of the charge rate and the voltage drop across the internal PowerFET. It can be calculated from the following equation when a battery pack is being charged :

$$P = [V_{(IN)} - V_{(OUT)}] \times [I_{(OUT)} + I_{(BAT)}] + [V_{(OUT)} - V_{(BAT)}] \times I_{(BAT)} \quad (11)$$

The thermal loop feature reduces the charge current to limit excessive IC junction temperature. It is recommended that the design not run in thermal regulation for typical operating conditions (nominal input voltage and nominal ambient temperatures) and use the feature for non typical situations such as hot environments or higher than normal input source voltage. With that said, the IC will still perform as described, if the thermal loop is always active.

## 13 器件和文档支持

### 13.1 器件支持

#### 13.1.1 第三方产品免责声明

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### 13.2 相关链接

下表列出了快速访问链接。类别包括技术文档、支持与社区资源、工具和软件，以及申请样片或购买产品的快速链接。

表 5. 相关链接

器件	产品文件夹	样片与购买	技术文档	工具与软件	支持和社区
bq24072	<a href="#">单击此处</a>	<a href="#">单击此处</a>	<a href="#">单击此处</a>	<a href="#">单击此处</a>	<a href="#">单击此处</a>
bq24073	<a href="#">单击此处</a>	<a href="#">单击此处</a>	<a href="#">单击此处</a>	<a href="#">单击此处</a>	<a href="#">单击此处</a>
bq24074	<a href="#">单击此处</a>	<a href="#">单击此处</a>	<a href="#">单击此处</a>	<a href="#">单击此处</a>	<a href="#">单击此处</a>
bq24075	<a href="#">单击此处</a>	<a href="#">单击此处</a>	<a href="#">单击此处</a>	<a href="#">单击此处</a>	<a href="#">单击此处</a>
bq24079	<a href="#">单击此处</a>	<a href="#">单击此处</a>	<a href="#">单击此处</a>	<a href="#">单击此处</a>	<a href="#">单击此处</a>

### 13.3 接收文档更新通知

要接收文档更新通知，请导航至 [TI.com.cn](http://TI.com.cn) 上的器件产品文件夹。单击右上角的 [通知我](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 13.4 社区资源

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**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 13.7 Glossary

**SLYZ022** — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 14 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。



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## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ24072RGTR	ACTIVE	VQFN	RGT	16	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CKP	<a href="#">Samples</a>
BQ24072RGTT	ACTIVE	VQFN	RGT	16	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CKP	<a href="#">Samples</a>
BQ24073RGTR	ACTIVE	VQFN	RGT	16	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CKQ	<a href="#">Samples</a>
BQ24073RGTT	ACTIVE	VQFN	RGT	16	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CKQ	<a href="#">Samples</a>
BQ24073RGTTG4	ACTIVE	VQFN	RGT	16	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CKQ	<a href="#">Samples</a>
BQ24074RGTR	ACTIVE	VQFN	RGT	16	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	(BZF, NXK)	<a href="#">Samples</a>
BQ24074RGTRG4	ACTIVE	VQFN	RGT	16	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	(BZF, NXK)	<a href="#">Samples</a>
BQ24074RGTT	ACTIVE	VQFN	RGT	16	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	(BZF, NXK)	<a href="#">Samples</a>
BQ24075RGTR	ACTIVE	VQFN	RGT	16	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CDU	<a href="#">Samples</a>
BQ24075RGTT	ACTIVE	VQFN	RGT	16	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CDU	<a href="#">Samples</a>
BQ24079RGTR	ACTIVE	VQFN	RGT	16	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ODI	<a href="#">Samples</a>
BQ24079RGTT	ACTIVE	VQFN	RGT	16	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ODI	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

---

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of  $\leq 1000$ ppm threshold. Antimony trioxide based flame retardants must also meet the  $\leq 1000$ ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

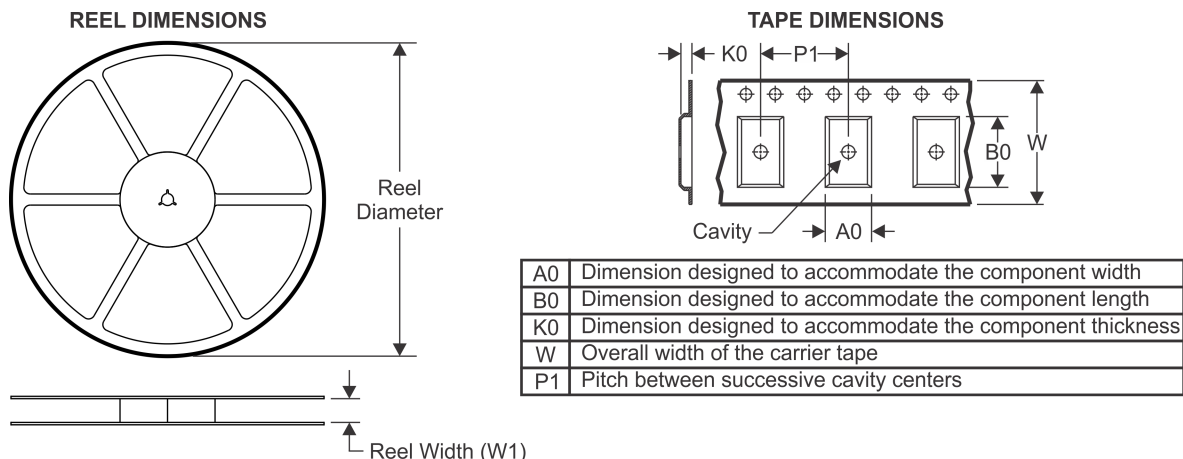
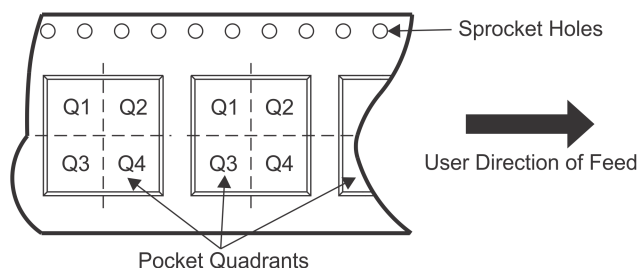
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ24072RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ24072RGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ24073RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ24073RGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ24074RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ24074RGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ24075RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ24075RGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ24079RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ24079RGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ24072RGTR	VQFN	RGT	16	3000	367.0	367.0	35.0
BQ24072RGTT	VQFN	RGT	16	250	210.0	185.0	35.0
BQ24073RGTR	VQFN	RGT	16	3000	367.0	367.0	35.0
BQ24073RGTT	VQFN	RGT	16	250	210.0	185.0	35.0
BQ24074RGTR	VQFN	RGT	16	3000	367.0	367.0	35.0
BQ24074RGTT	VQFN	RGT	16	250	210.0	185.0	35.0
BQ24075RGTR	VQFN	RGT	16	3000	367.0	367.0	35.0
BQ24075RGTT	VQFN	RGT	16	250	210.0	185.0	35.0
BQ24079RGTR	VQFN	RGT	16	3000	367.0	367.0	35.0
BQ24079RGTT	VQFN	RGT	16	250	210.0	185.0	35.0

**RGT 16**

**GENERIC PACKAGE VIEW**

**VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

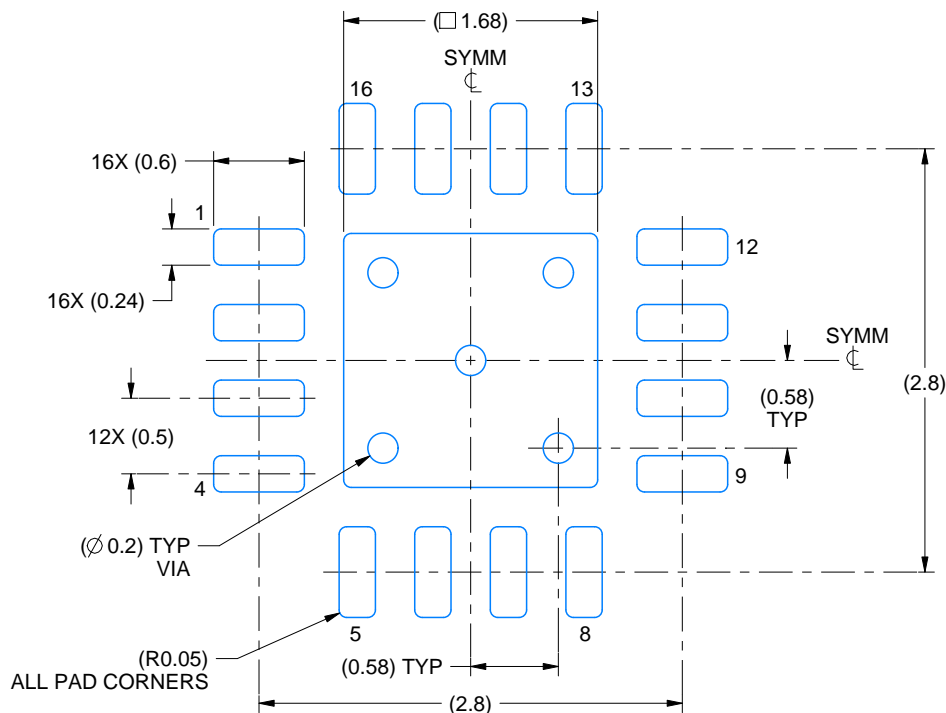
4203495/1



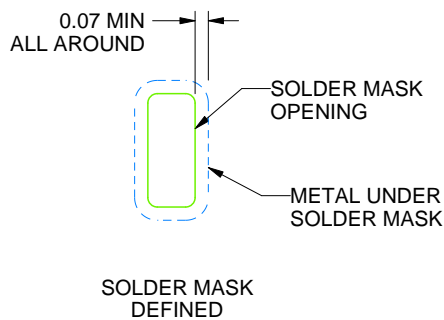
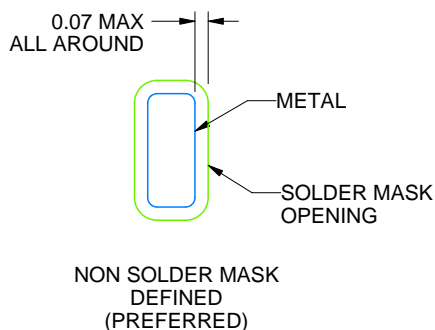
**RGT0016C**

## VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
SCALE:20X



## SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

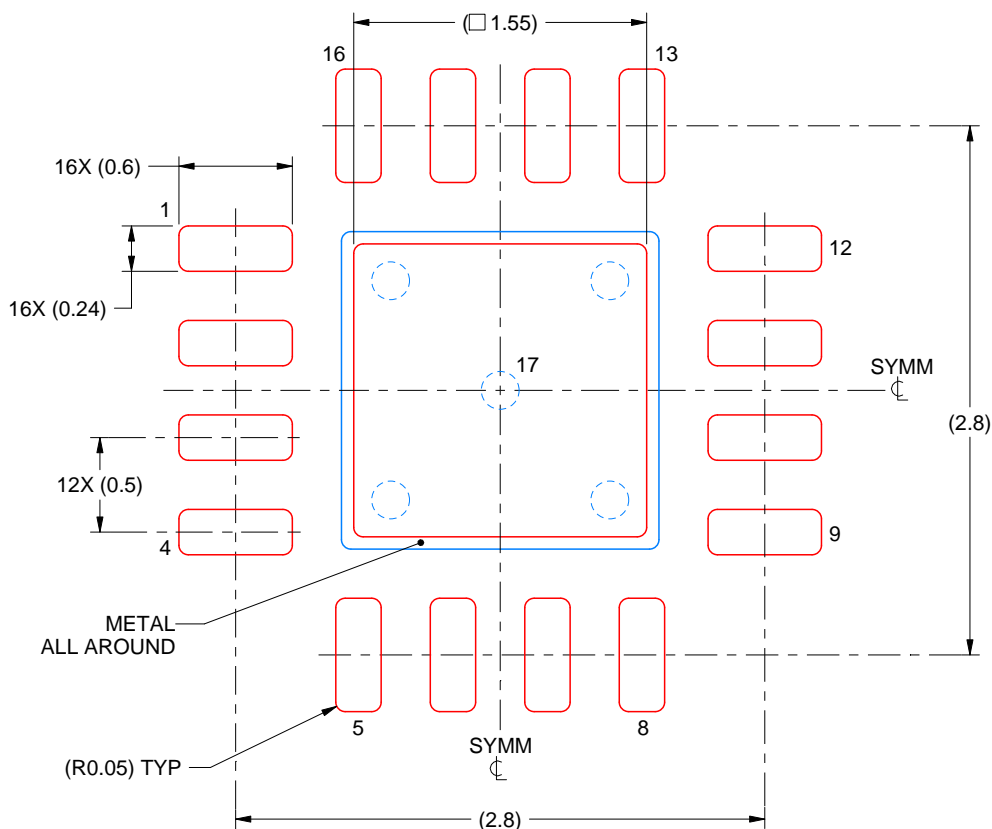


# EXAMPLE STENCIL DESIGN

RGT0016C

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE**  
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:  
 85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
 SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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