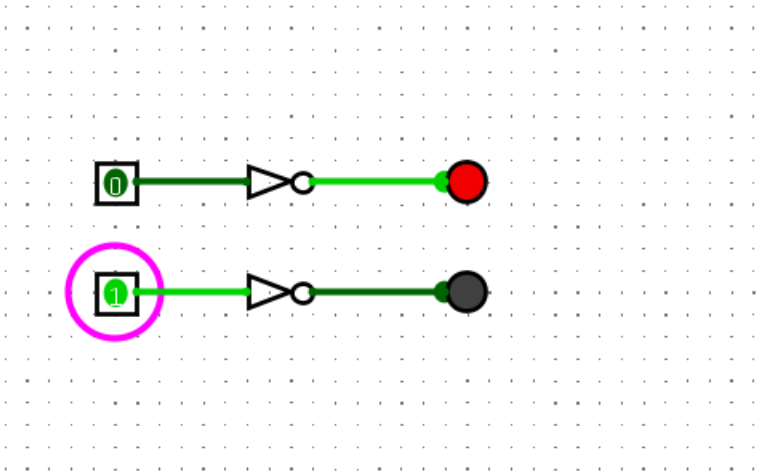
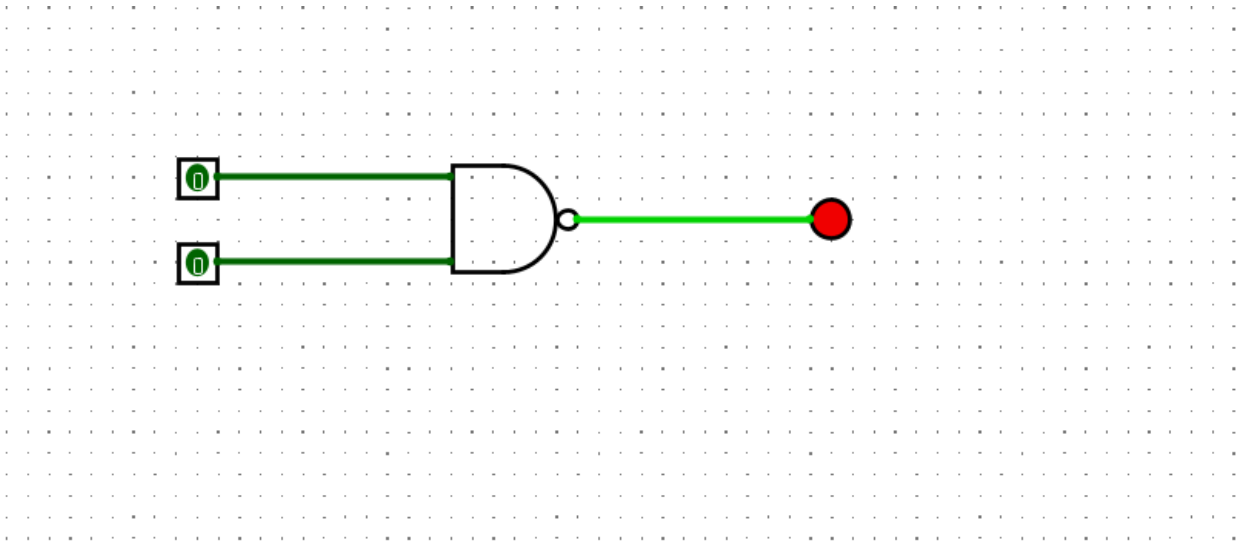
Lab 01 -Nguyen Manh Duc -103792724

Not gate



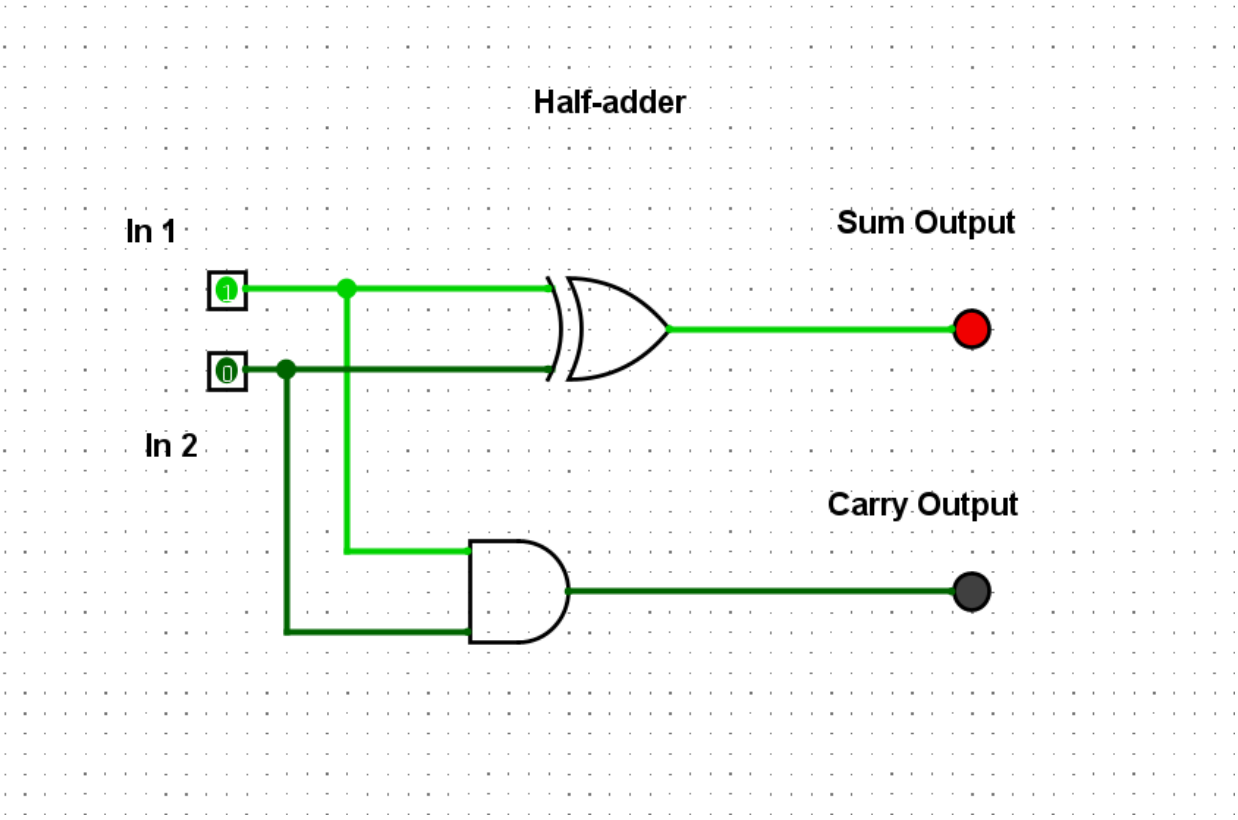
Pin	Output
0	1
1	0

NAND gate



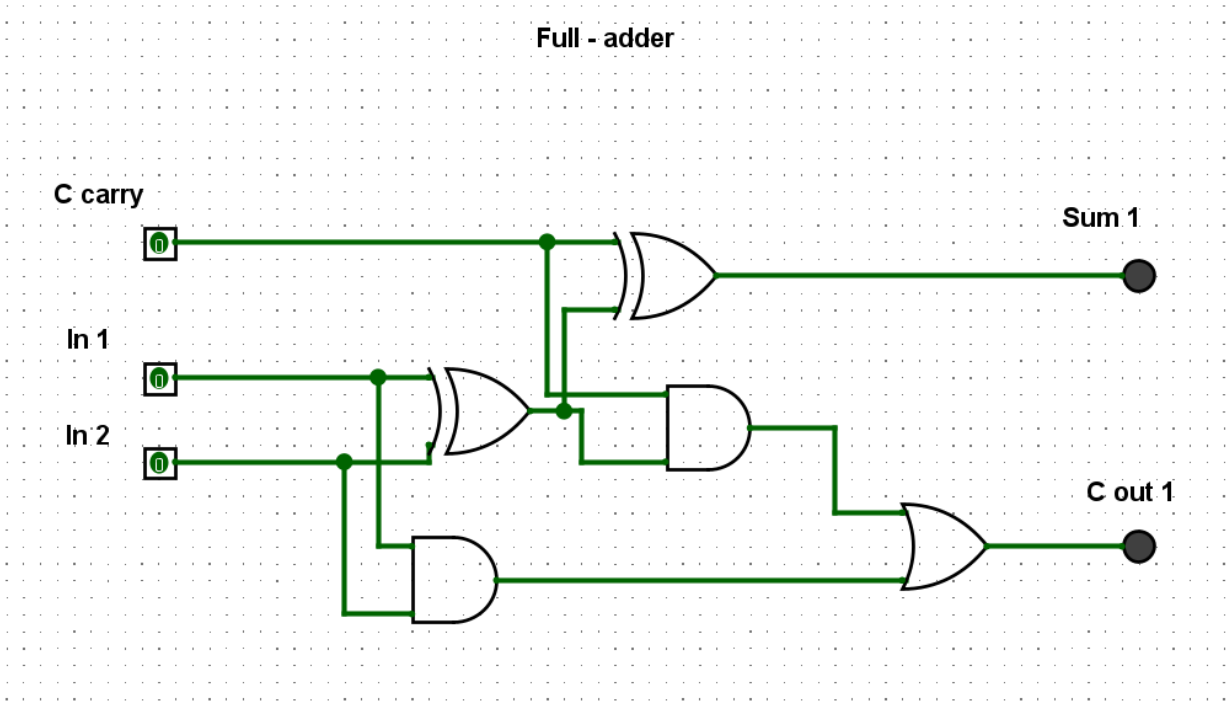
Pin 1	Pin 2	Output
0	0	**1**
0	1	**1**
1	0	**1**
1	1	**0**

Half-adder



Input 1	Input 2	Sum Output	Carry output
0	0	0	0
1	0	1	0
0	1	1	0
1	1	0	1

Full-adder



Input 1	Input 2	Carry In	**Sum Output**	**Carry Output**
0	0	0	**0**	**0**
0	1	0	**1**	**0**
1	0	0	**1**	**0**
1	1	0	**0**	**1**
0	0	1	**1**	**0**
0	1	1	**0**	**1**
1	0	1	**0**	**1**
1	1	1	**1**	**1**