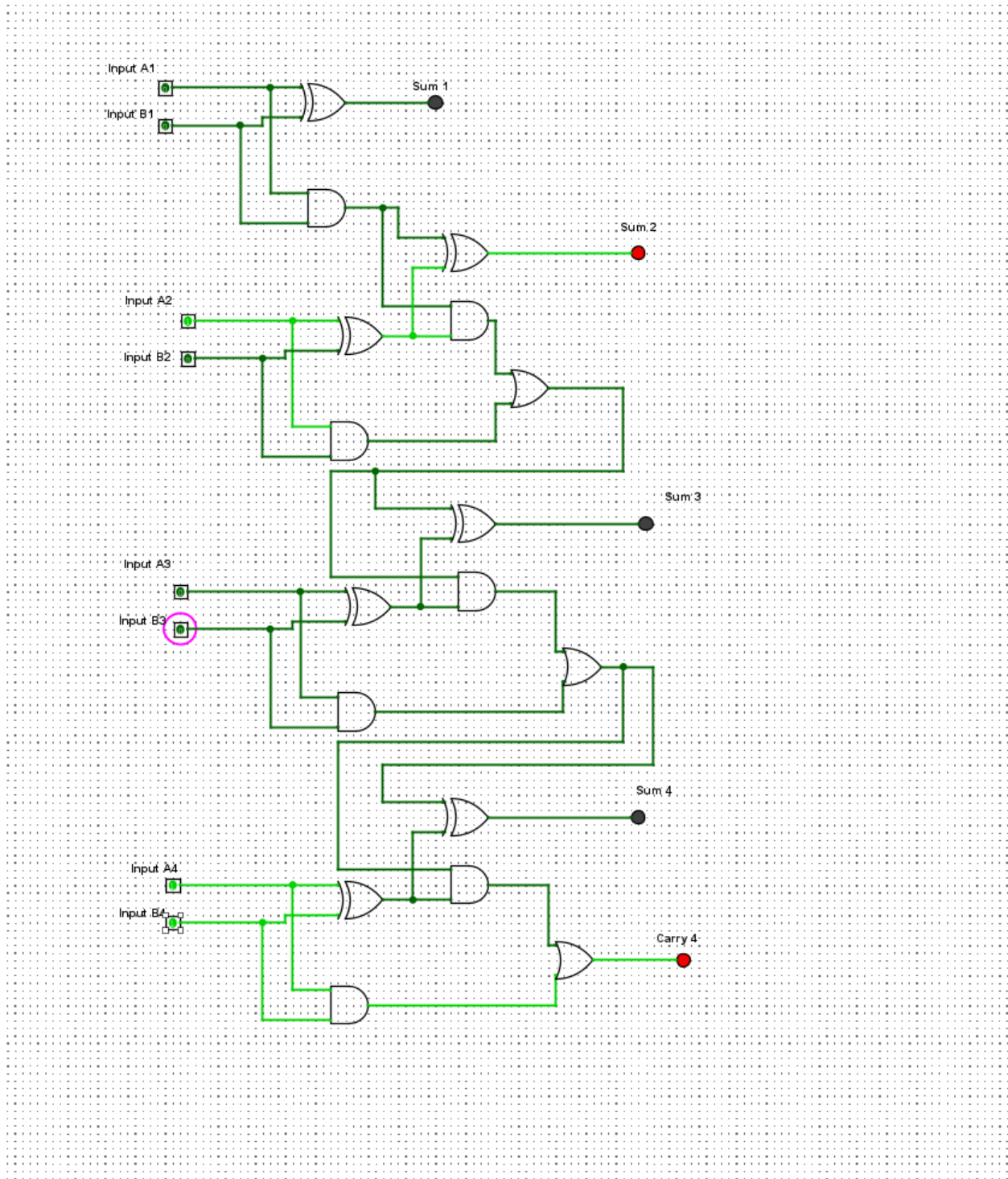
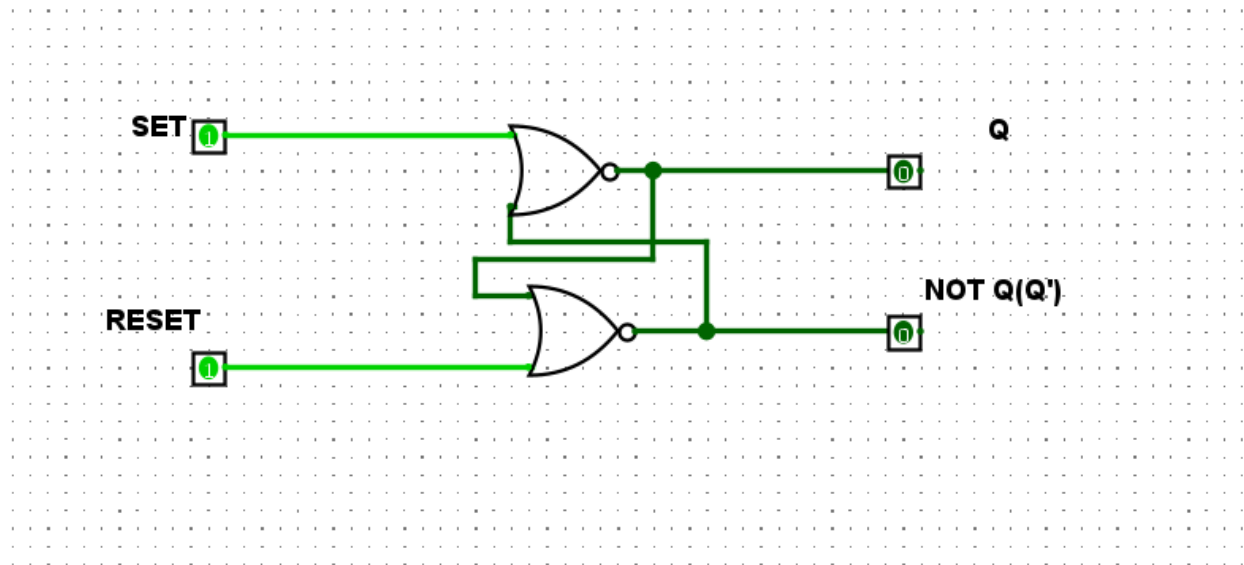


4 Bit Adder



Input A	Input B	Output
0101	0000	0101
0101	0001	0110
0101	0010	0111
0101	0011	1000
0101	0100	1001
0101	0101	1010
0101	0110	1011
0101	0111	1100
0101	1000	1101
0101	1001	1110
0101	1010	1111
0101	1011	0000
0101	1100	0001
0101	1101	0010
0101	1110	0011
0101	1111	0100

Storing bits with Flip Flops



Set	Reset	Q	Not Q(Q')
1	0	0	1
1	1	0	0
0	1	1	0
1	1	0	0

Describe in a sentence, the behaviour of the circuit when one of the inputs is 1 (but not both) and why this is useful for digital circuit design.

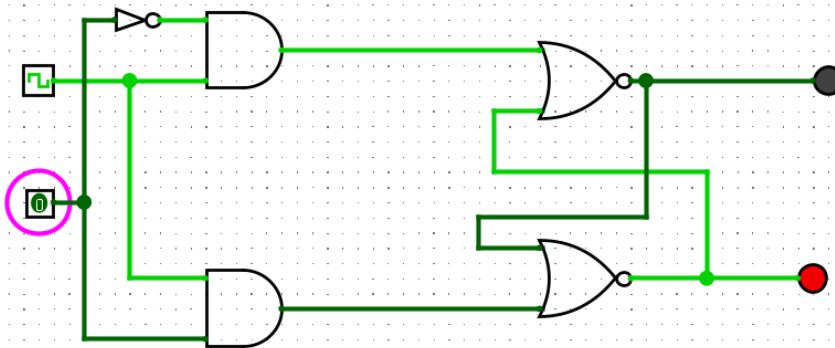
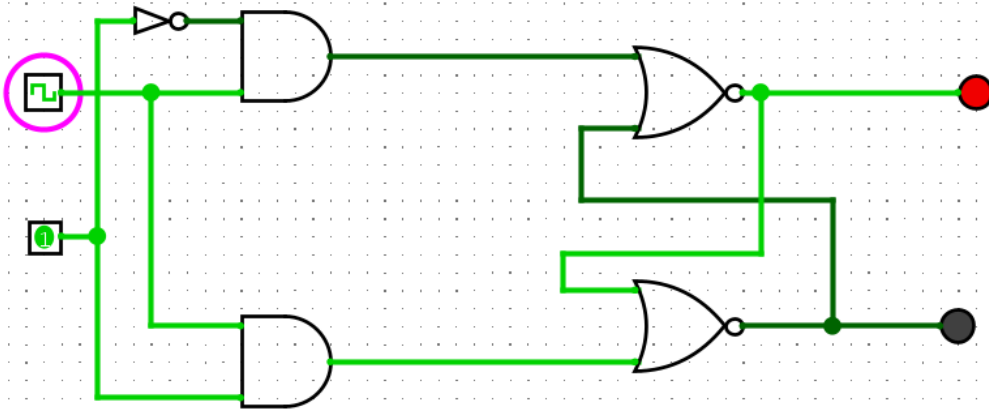
The RS Flip Flop is made from coupled NOR gates which were crossed on the diagram above. If we open the Set (1) and close the Reset (0), it will set the Q (1) and Q' (0). By contrast, if we open the Reset (1) and close the Reset (0), it will set the Not Q or Q' (1) and Q (0), the Q will be reset.

What do you notice about the two times you set both inputs to 1. Briefly explain what is happening here and why this is an issue for digital circuit design?

When we set both inputs Set (1) and Reset (1), the outputs are both 0 and the RS Flip Flop will be gone to the undefined state.

This is an issue for the digital circuit design because the rule of the flip flop is that the outputs need to support and supplement each other. By that reason, it infringes the rule by being set like that

D Flip Flops



Clock	Data	Q	Not Q(Q')
0	0	0	0
0	1	0	0
1	1	0	1
1	0	1	0

Briefly explain the behaviour of a D Flip Flop and how it is useful for digital circuit design.

The D Flip-Flop has only one input Data with the Clock to control the signal. Q is set to be reversed as D and Not Q or Q' is set to be the same as D when the clock goes active.

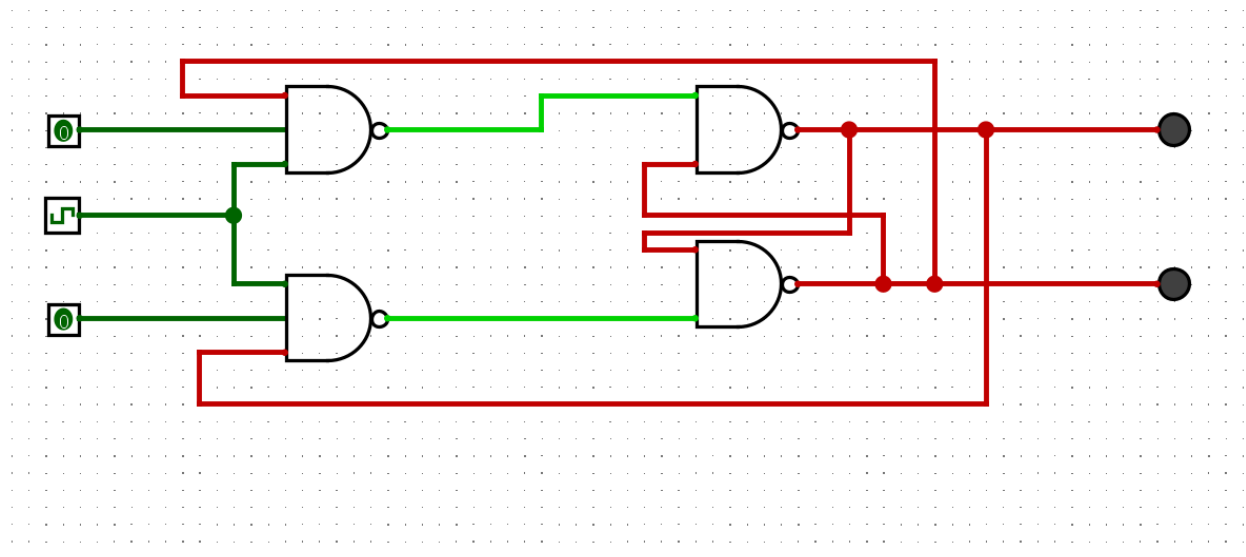
What is the role of the clock?

How does it impact the changing of state of Q and Q'? The role of the clock which integrated inside the diagram above is the ability to control the signal..

Why is it generally preferred over the R-S Flip Flop?

The first reason make the D Flip Flop is preferred over the R S Flip Flop is that D Flip Flops can assist in synchronizing the data, in condition that those need to be clocked.

JK Flip Flops



J	K	Q(When clocked)	Q'(When clocked)
0	0	No charge	
1	0	1	0
0	1	0	1
1	1	Toggle	

How can a J-K Flip Flop be made to behave like a D Flip Flop?

J-K Flip Flop was made behave like a D Flip Flop by the way that it adds one more Input which connects with (NAND Gate) and the clock, and delete the essential additional component (NOT GATE)

How can a J-K Flip Flop be made to behave like a toggle (T Flip Flop)?

When both the J Input and K Input is 1, the J-K Flip Flop behave like a Toggle – T Flip Flop.