FPGA Emulation

Hsi-Pin Ma

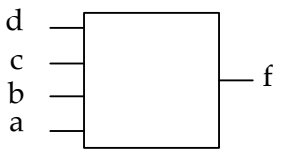
http://lms.nthu.edu.tw/course/38127
Department of Electrical Engineering
National Tsing Hua University

Notes from Lab1

- Always 'SAVE' before next step
- Select the right file for the next step
  - For simulation
  - For implementation
- Do not use specific names for files and directories
  - Leading with number,
  - Names with space,
  - Names in Chinese

Example: Prime Detector (1/2)

- Spec 1
  - A circuit outputs a 1 when its four-bit input represents a prime number in binary
  - f(d,c,b,a)=1 if $dcba_2$ is a prime



- Truth table 2

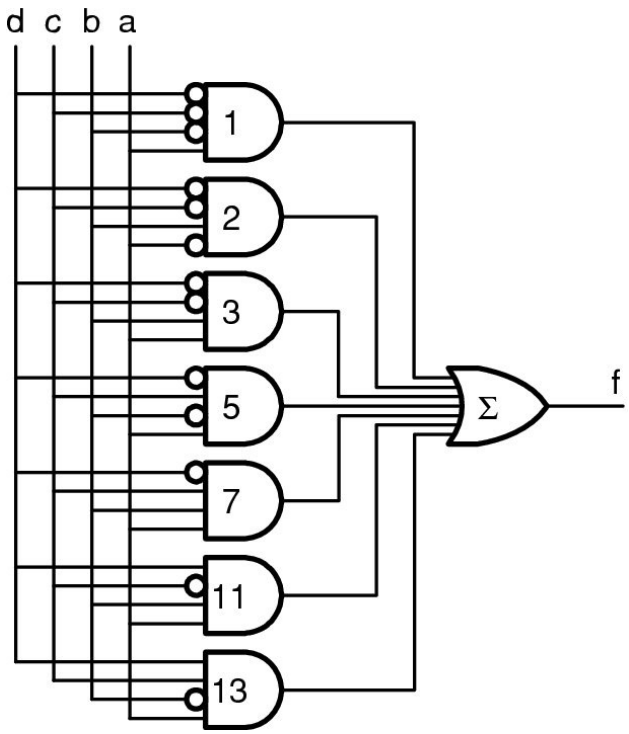
No	dcba	f
0	0000	0
1	0001	1
2	0010	1
3	0011	1
4	0100	0
5	0101	1
6	0110	0
7	0111	1
8	1000	0
9	1001	0
10	1010	0
11	1011	1
12	1100	0
13	1101	1
14	1110	0
15	1111	0

abbreviated truth table

No	dcba	f
1	0001	1
2	0010	1
3	0011	1
5	0101	1
7	0111	1
11	1011	1
13	1101	1
Otherwise		0

Example: Prime Detector (2/2)

- Normal form 2
  - $f(d,c,b,a) = d'c'b'a + d'c'ba' + d'c'ba + d'cb'a + d'cba + dc'ba + dcb'a$
- Sum of minterms
  - $f(d,c,b,a) = \sum m(1,2,3,5,7,11,13)$



Verilog Module v1 (assign)

$$f(d,c,b,a) = d'a + d'c'b + cb'a + c'ba$$

- Use simple assignment "assign"

```
module prime(isprime, a, b, c, d);
output isprime;
input a,b,c,d;

assign isprime= ((~d)&a) | ((~d)&(~c)&b) | (c&(~b)&a) | ((~c)&b&a));

endmodule
```

Verilog Module v2 (case)

let in[3:0]=dcba (bus)

```
module prime(isprime, in);
output isprime;  //true if input is prime
input [3:0] in;  //4-bit input
reg isprime;  //for signal to be assigned in always block

always @*
  case (in)
    1,2,3,5,7,11,13: isprime = 1'b1;
    default: isprime = 1'b0;
  endcase

endmodule
```

Verilog Module v3 (casex)

```
module prime(isprime, in);
output isprime;  //true if input is prime
input [3:0] in;  //4-bit input
reg isprime;  //for signal to be assigned in always block

always @*
  casex (in)
    4'b0xx1: isprime = 1'b1;
    4'b001x: isprime = 1'b1;
    4'bx011: isprime = 1'b1;
    4'bx101: isprime = 1'b1;
    default: isprime = 1'b0;
  endcase
endmodule
```

- **allow don't-cares**
- **priority assignment**

Verilog Module v4 (Structural Description)

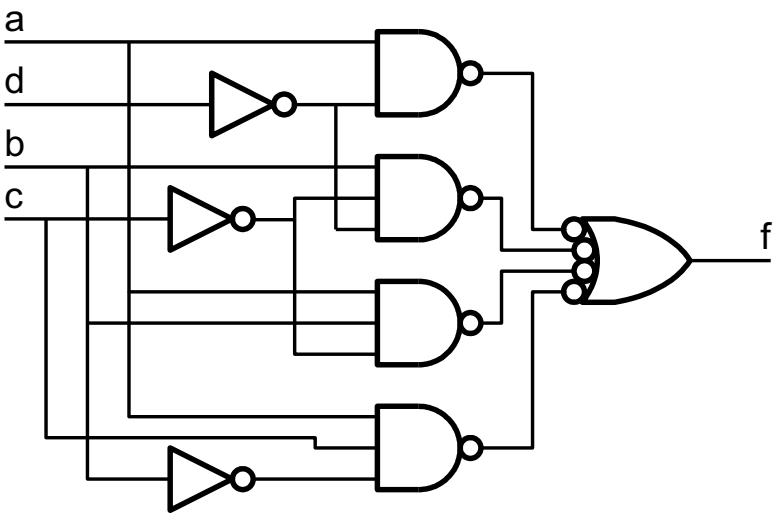
- Structural gate-level description

```
module prime(isprime, in);
output isprime;  //true if input is prime
input [3:0] in;  //4-bit input

and and1(a1,in[0],~in[3]);
and and2(a2,in[1],~in[2],~in[3]);
and and3(a3,in[0],~in[1],in[2]);
and and4(a4,in[0],in[1],~in[2]);
or or1(isprime,a1,a2,a3,a4);

endmodule
```

a1 a2 a3 a4

$$f(d,c,b,a) = d'a + d'c'b + cb'a + c'ba$$

let in[3:0]=dcba



Testbench

```
module test_prime;
wire isprime;
reg [3:0] in;

// instantiate module to test
prime U0(.isprime(isprime),.in(in));

initial
begin
  in=0;  // set to initial value
  repeat (16)  // loop 16 times
  begin
    #100    // delay for 100 time unit
    $display("in = %2d isprime = %1b", in, isprime);
    in = in +1;  // increment input
  end
 end
endmodule
```

1-digit + 1-digit Decimal Adder

Specification

- Addition of 2 decimal digits in BCD
  - $\{C_o,S\}=A+B+C_i$
  - 1 • $S=S_3S_2S_1S_0$, $A=A_3A_2A_1A_0$, $B=B_3B_2B_1B_0$
  - A digit in BCD cannot exceed 9, add 6 (0110) for final correction.

1 0		1 0 0 0 0
8_{10}	A	1000_2
9_{10}	B	1001_2
17_{10}	KZ	10001_2
		0110_2
		00010111_2

2 3

binary coded results

if >9, add 6

BCD coded results

Decimal symbol	BCD digit
0	0000
1	0001
2	0010
3	0011
4	0100
5	0101
6	0110
7	0111
8	1000
9	1001

Version 1 Implementation

2 3

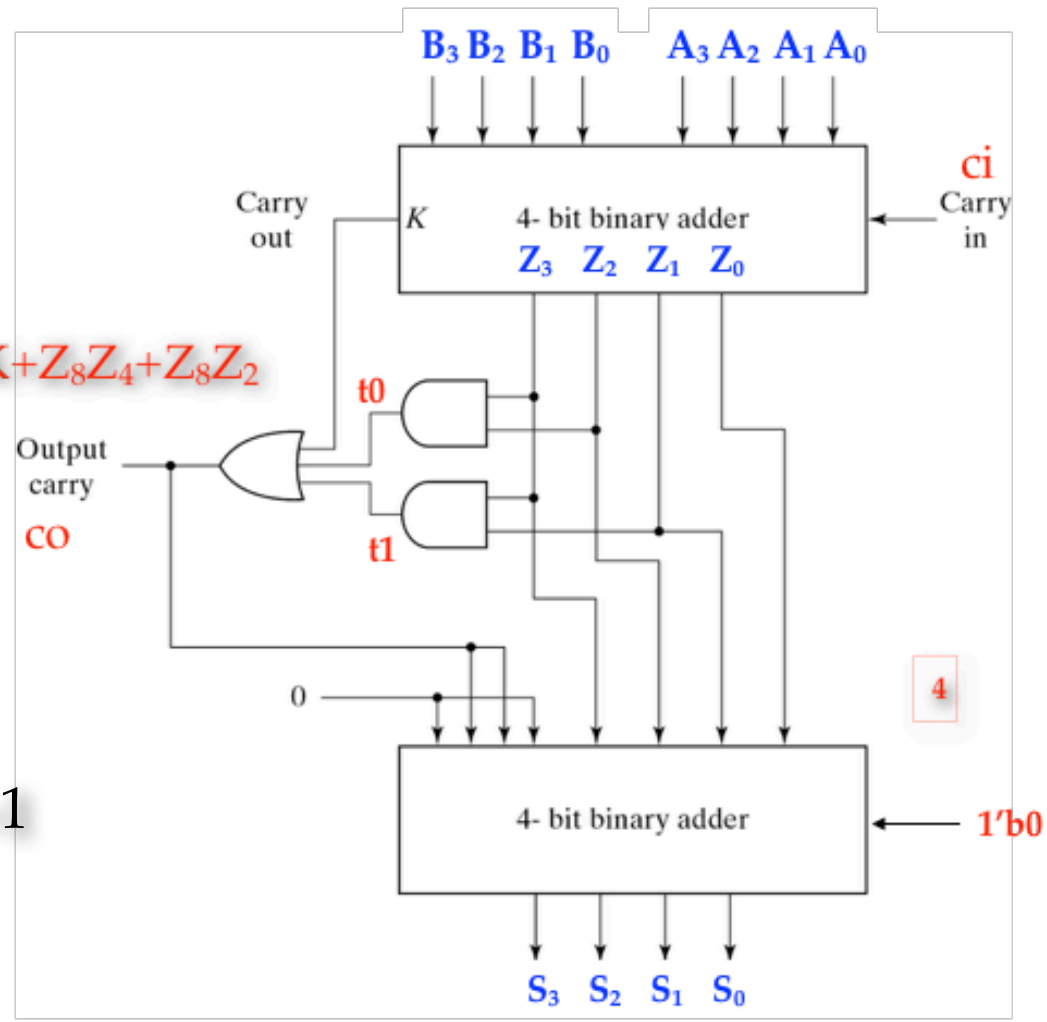
Z_3	Z_2	Z_1	Z_0
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1

Z_3Z_2

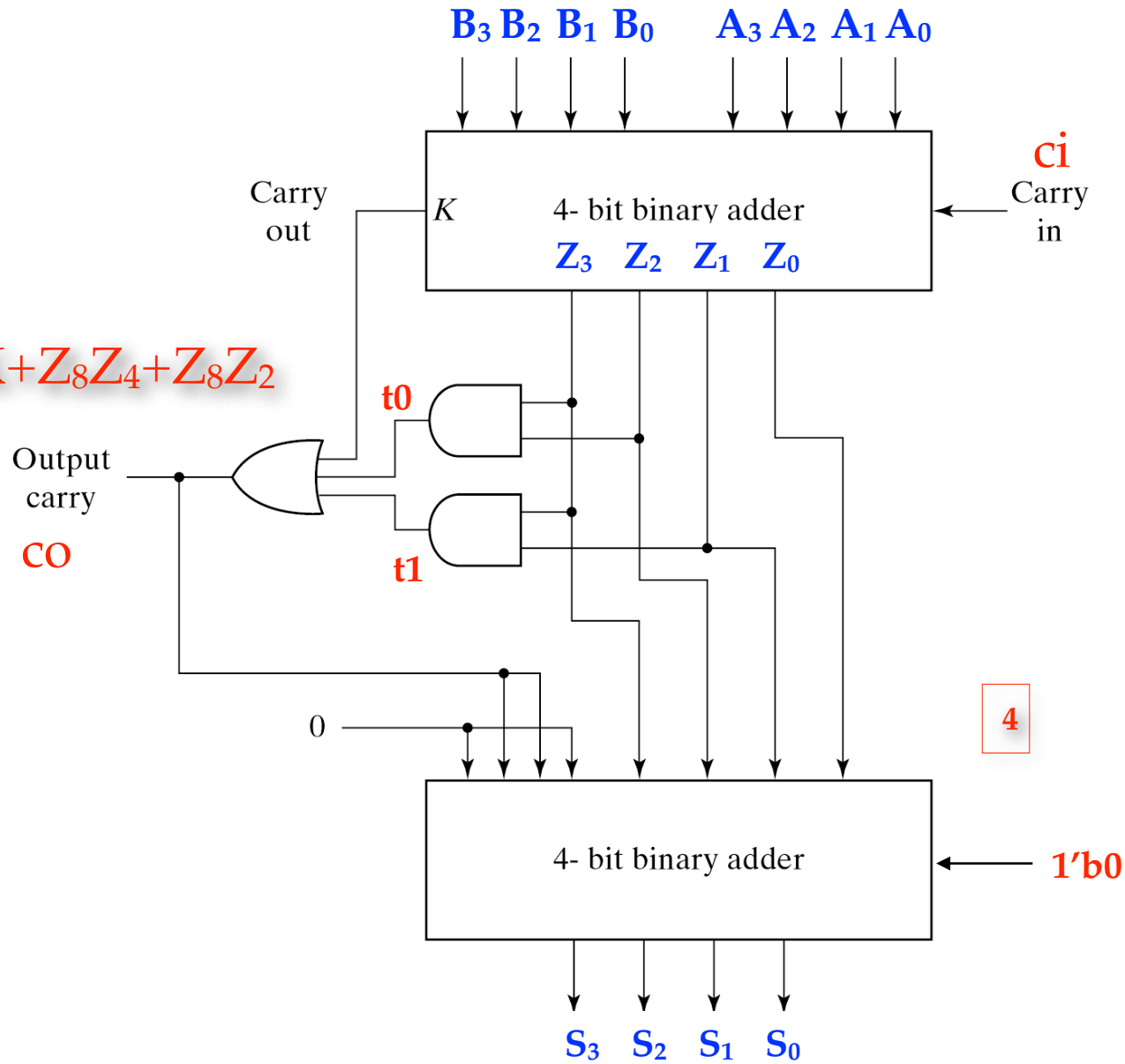
Z_3Z_1

co=1

3 $C_{out}=K+Z_8Z_4+Z_8Z_2$



Version 1 Implementation



3 $C_{out}=K+Z_8Z_4+Z_8Z_2$

Version 1 Implementation

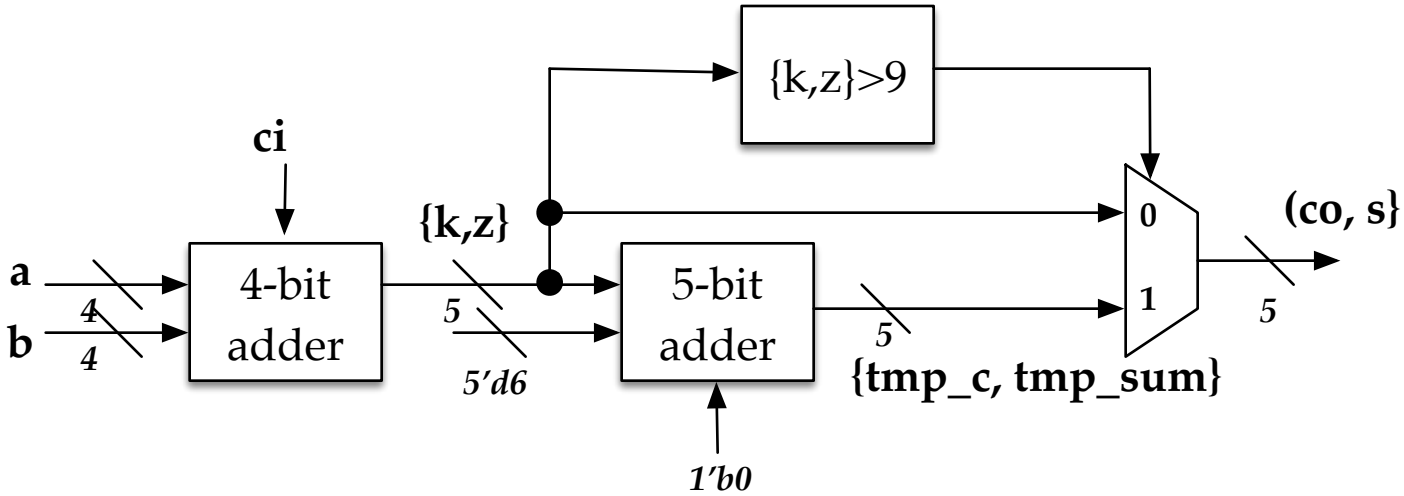
```
module add4(k, z, a, b, ci);
output  k;
output [3:0] z;
input [3:0] a, b;
input ci;

assign {k,z} = a + b + ci;

endmodule
```

```
module decadd(co, s, z, a, b, ci);
output  co;
output [3:0] s;
input [3:0] a, b;
input ci;

wire [3:0] z;
wire k;
wire [1:0] t;

add4 U0(.k(k). .z(z), .a(a), .b(b), .ci(ci));

assign t[0] = z[3] & z[2];
assign t[1] = z[3] & z[1];
assign co = k | t[1] | t[0]

add4 U1(.k(). .z(s), .a(z), .b({1'b0, co, co, 1'b0}), .ci(1'b0));

endmodule
```

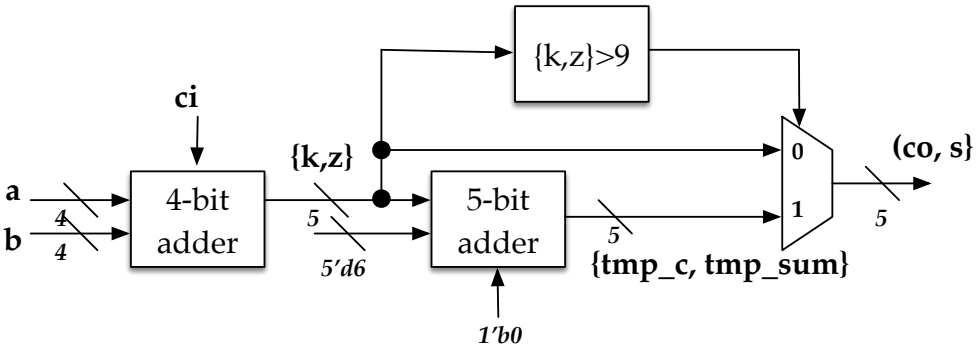
you can leave some *output* port unassigned

Version 2

10		10000	
8_{10}	A	1000_2	
9_{10}	B	1001_2	
17_{10}	KZ	10001_2	binary coded results
		0110_2	if >9, add 6
		00010111_2	BCD coded results



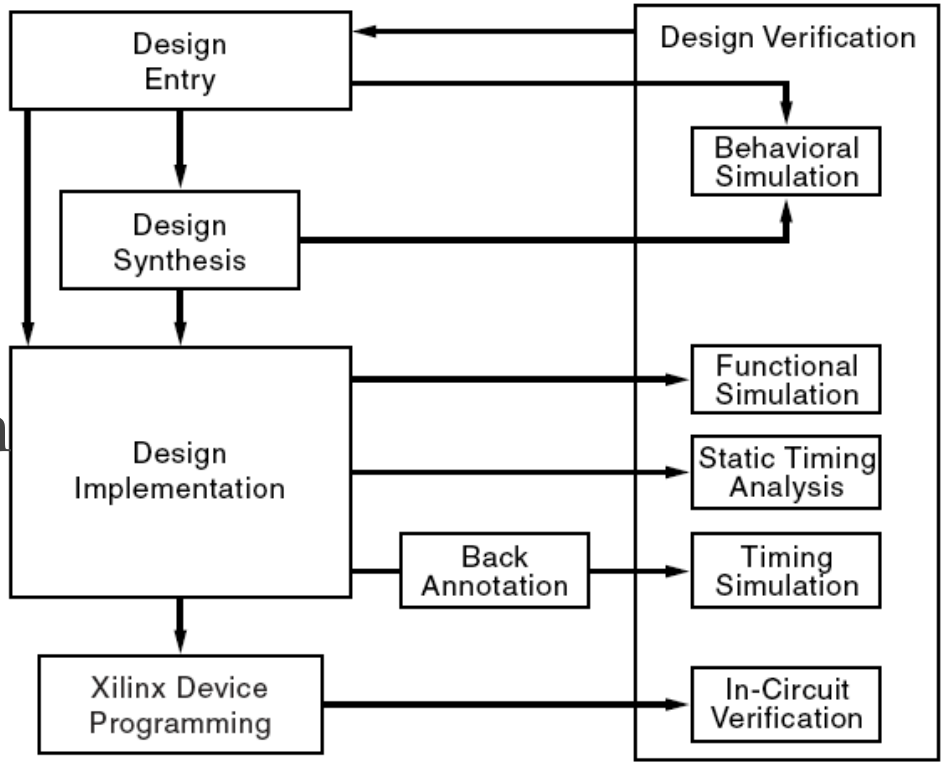
Version 2




```
module decadd(s,co,a,b,ci);
output reg [3:0] s;
output reg co;
input [3:0] a,b;
input ci;

wire [3:0] z, tmp_sum; // temp sum
wire k, tmp_c; // temp carryout

assign {k, z} = a + b + ci;
assign {tmp_c, tmp_sum} = {k, z} + 5'd6;

always @*
  if ({k, z}>5'd9)
    {co, s} = {tmp_c, tmp_sum};
  else
    {co, s} = {k, z};

endmodule
```

Design Flow

- General design flow
  - Design construction
  - Behavioral simulation
  - Design implementation
  - Timing simulation
- HDL-based design Flow



Important Notes

- **Draw schematic first** and then construct Verilog codes.
- Verilog RTL coding philosophy is not the same as C programming
  - Every Verilog RTL construct has its own logic mapping (for synthesis)
  - You should have the logics (draw schematic) first and then the RTL codes
  - You have to write **synthesizable** RTL codes

Digilent Basys 3 Demo Board

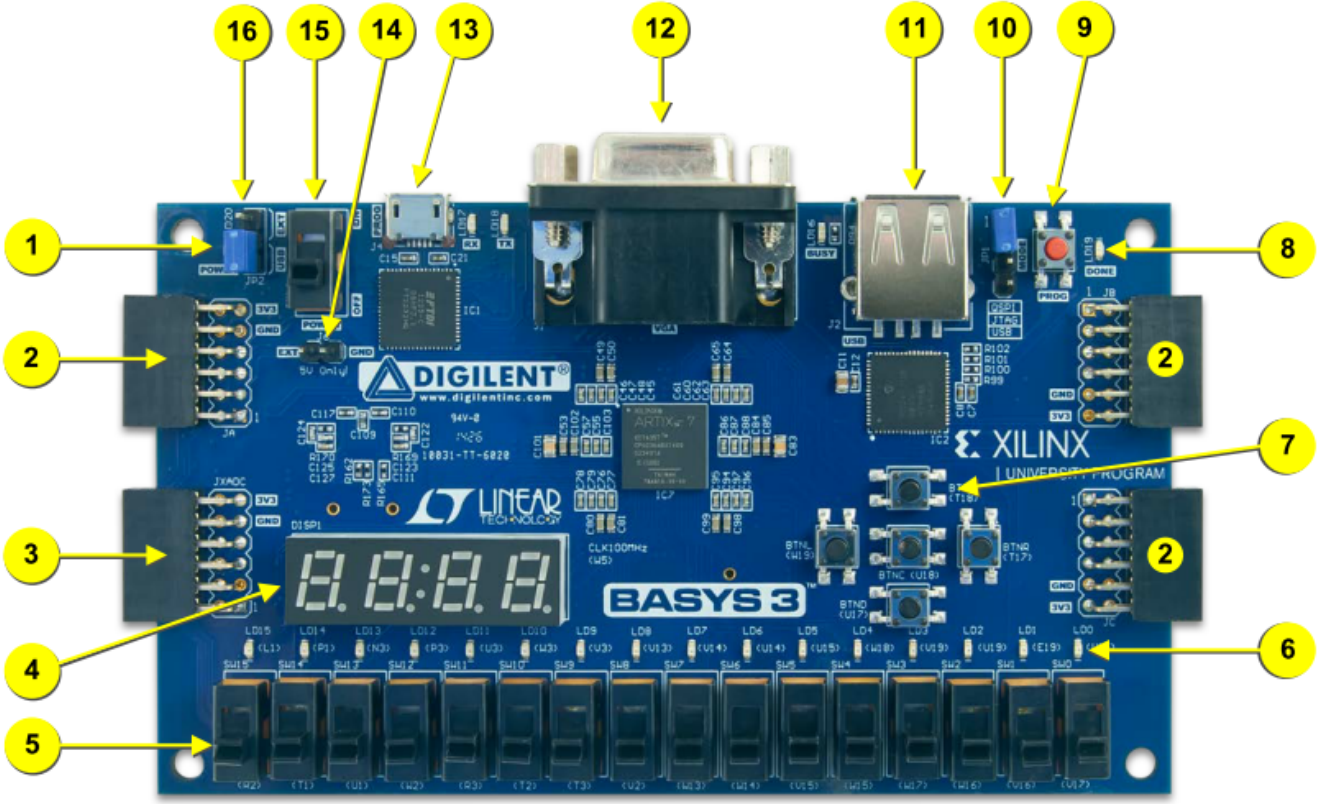


Figure 1. Basys3 FPGA board with callouts.

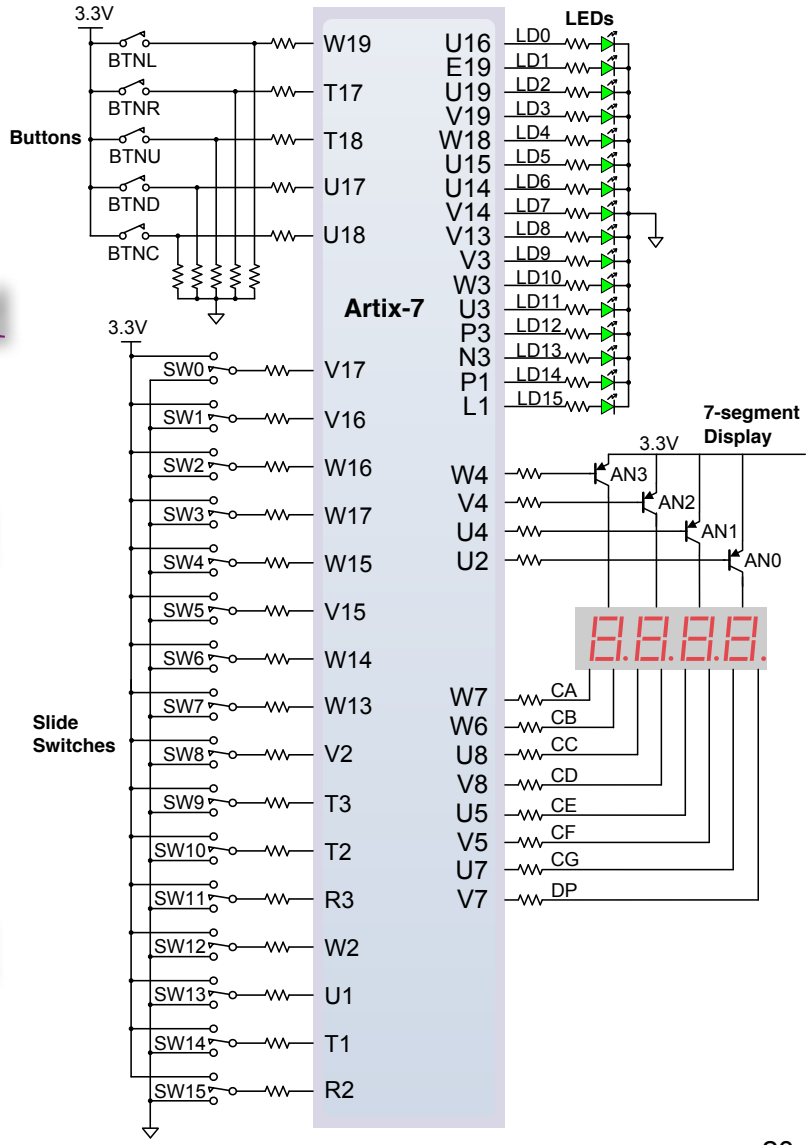
Callout	Component Description
1	Power good LED
2	Pmod connector(s)
3	Analog signal Pmod connector (XADC)
4	Four digit 7-segment display
5	Slide switches (16)
6	LEDs (16)
7	Pushbuttons (5)
8	FPGA programming done LED
9	FPGA configuration reset button
10	Programming mode jumper
11	USB host connector
12	VGA connector
13	Shared UART/ JTAG USB port
14	External power connector
15	Power Switch
16	Power Select Jumper

https://reference.digilentinc.com/reference/programmable-logic/basys-3/start?redirect=1

Check Basys 3 board reference manual for details

Input/Output Connections

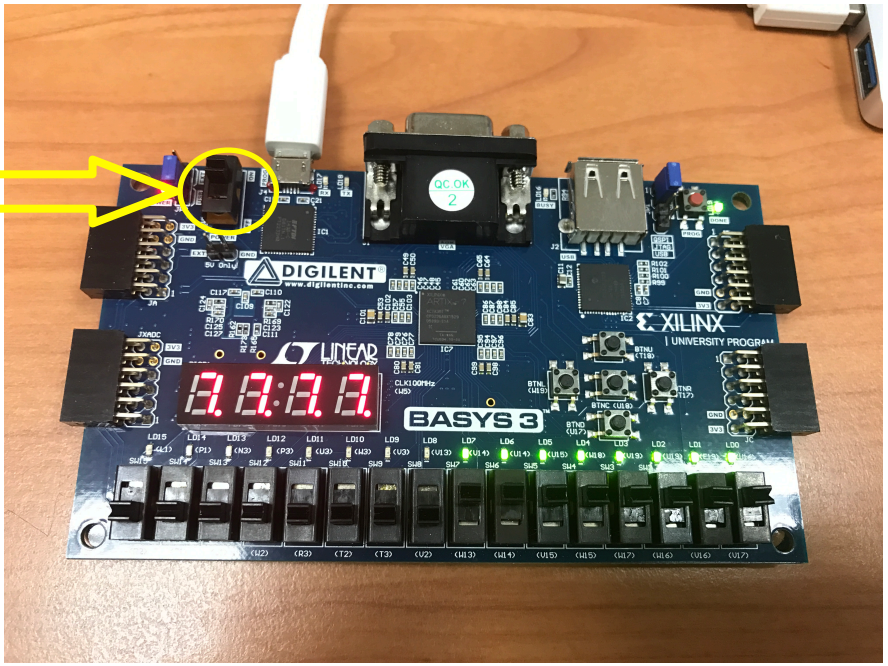
- LEDs are pre-wired **HIGH** active control
- 7-Seg Display are pre-wired **LOW** active control
- Push buttons are pre-wired **LOW** when they are at rest
- DIP switches generate **HIGH** when tuned up and generate **LOW** when tuned down



Test Your FPGA Board (1/3)

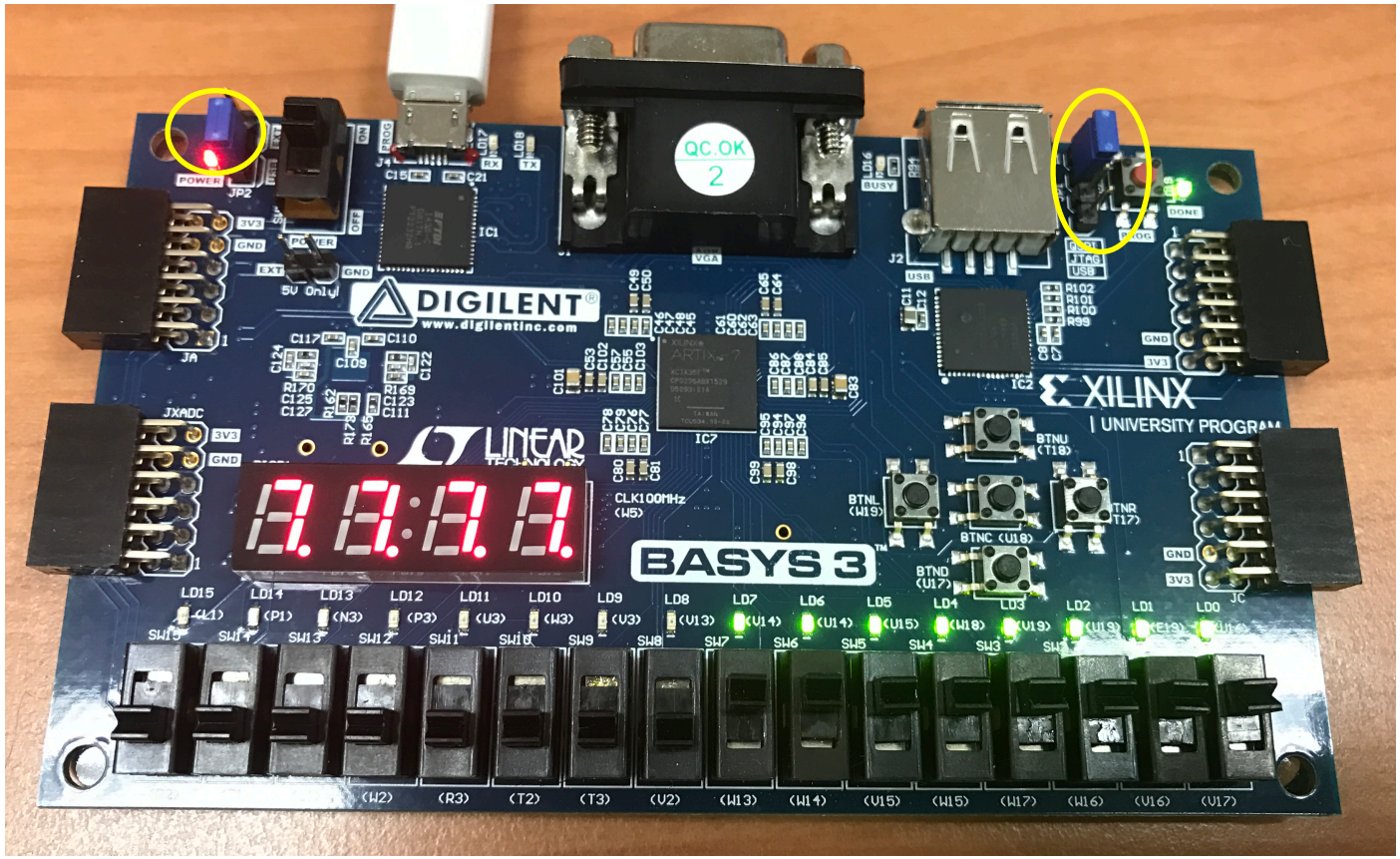
- Connect the demo board to PC and also the power supply

- 所有的線接好再開電源
- 關閉電源後再拔所有的線
- 勿用導體接觸針腳
- 插座別插反了
- 避免長時間開機



Test Your FPGA Board (2/3)

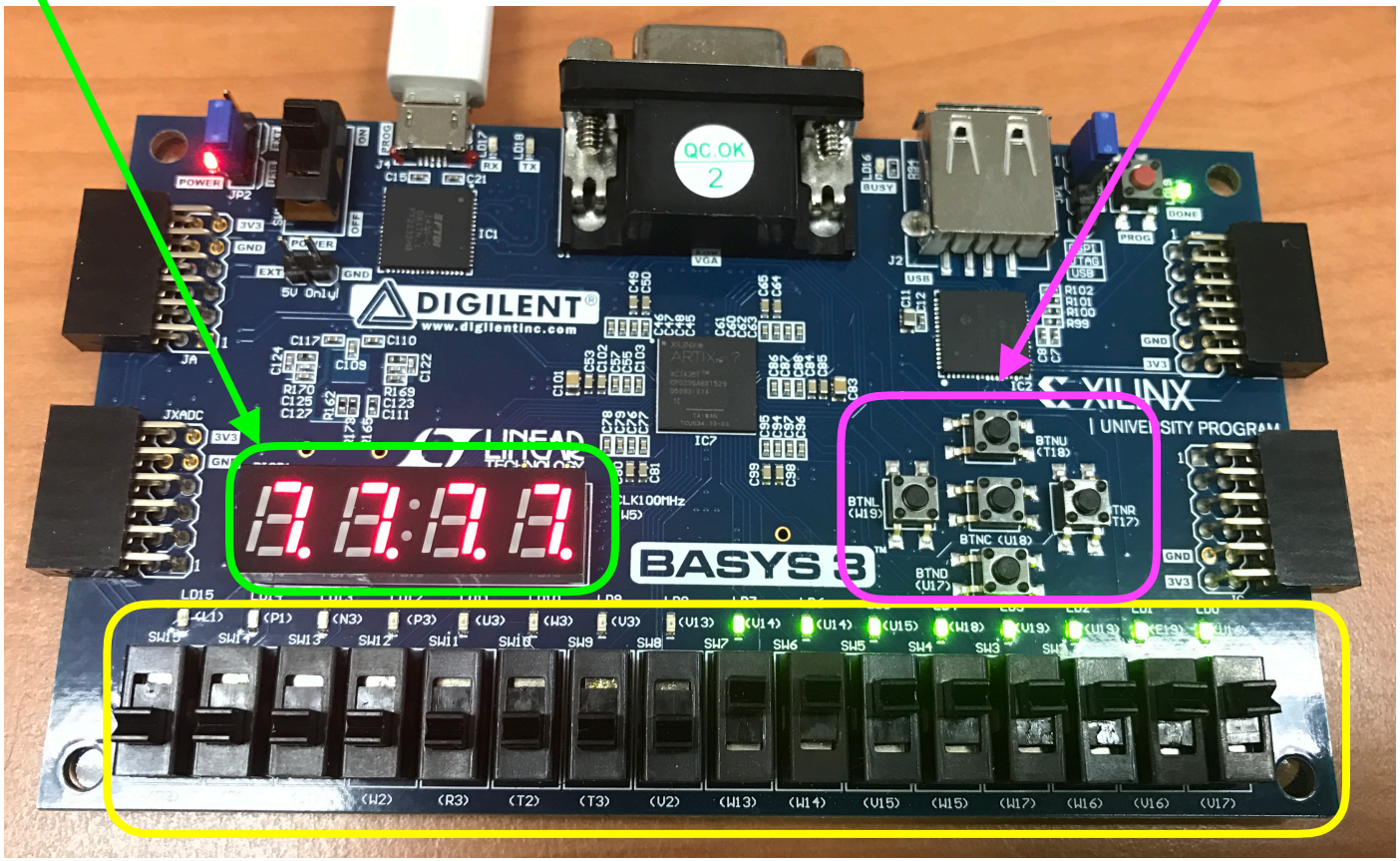
- Don't move or remove the jumpers



Test Your FPGA Board (3/3)

BCD counts on 7-Seg Displays continuously

Push buttons control the 7-Seg display



DIP Switch control the LEDs

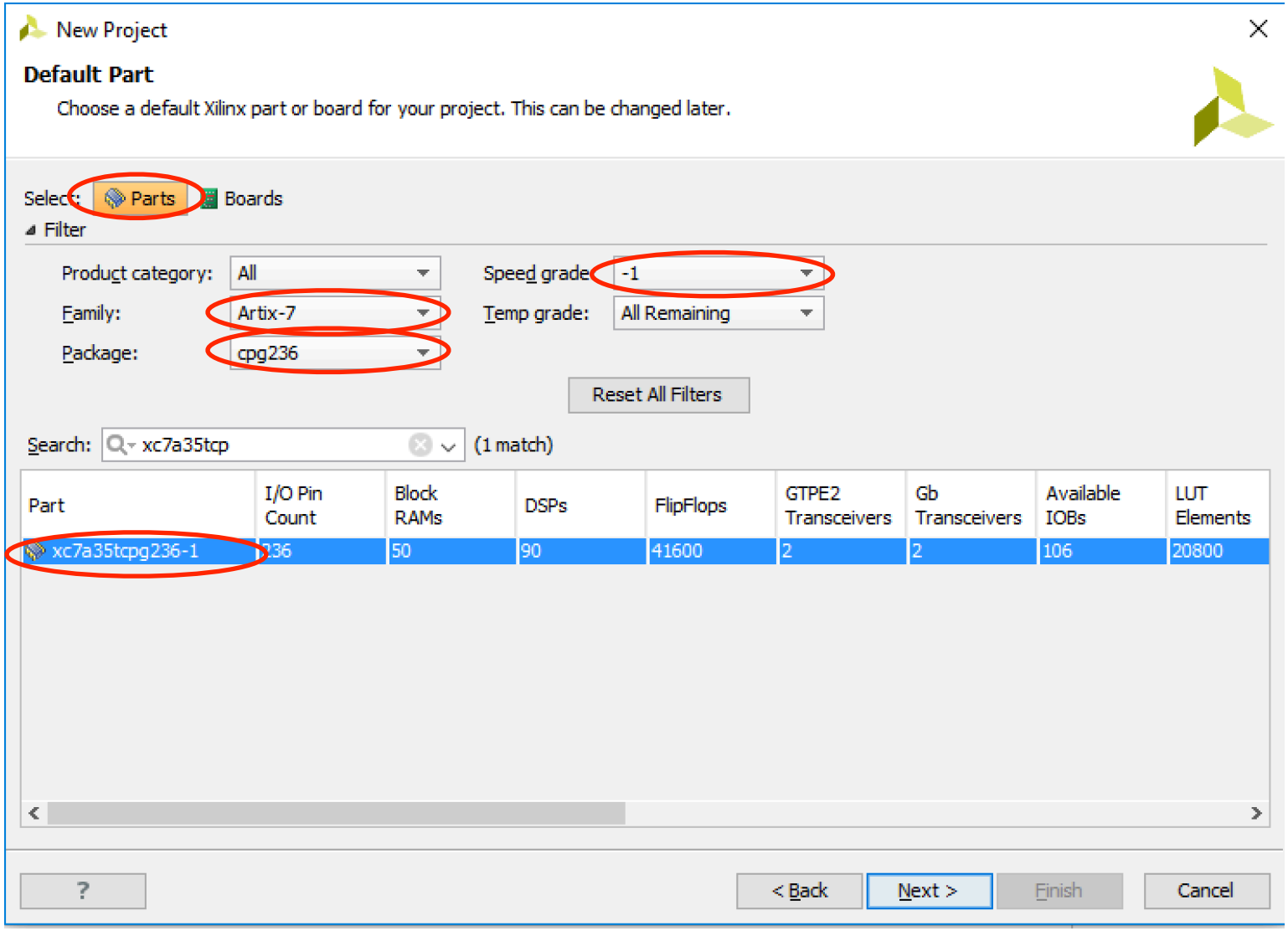
FPGA Emulation Using Xilinx Vivado

Design Flow

- Design Source Preparation
  - Design modules (.v)
  - Design constraints (I/O pin assignments) (.xdc)
- Design Simulation
  - testbench (.v)
- Design Synthesis and Implementation

Create New Project (2/3)

Continue from previous unit slides



I/O Pins Assignment (1/4)

smux - [C:/Users/hsipin/LD/smux/smux.xpr] - Vivado 2016.2

File Edit Flow Tools Window Layout View Help

Flow Navigator

- Project Manager
  - Project Settings
  - Add Sources
  - Language Templates
  - IP Catalog
- IP Integrator
  - Create Block Design
  - Open Block Design
  - Generate Block Design
- Simulation
  - Simulation Settings
  - Run Simulation
- RTL Analysis
  - Elaboration Settings
  - Open Elaborated Design
- Synthesis
  - Synthesis Settings
  - Run Synthesis
  - Open Synthesized Design
- Implementation
  - Implementation Settings
  - Run Implementation
  - Open Implemented Design
- Program and Debug
  - Bitstream Settings
  - Generate Bitstream

Project Manager - smux

Sources: Design Sources (1) — smux (smux.v); Constraints — constrs_1; Simulation Sources (1) — sim_1 (1)

Synthesis Completed

Synthesis successfully completed.

Next

- Run Implementation
- Open Synthesized Design
- View Reports

Don't show this dialog again

OK Cancel

Implementation

Status: Not started
Messages: No errors or warnings
Part: xc7a35tcpg236-1
Strategy: Vivado Implementation Defaults
Incremental compile: None

DRC Violations

Timing

Design Runs

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Failed Routes	LUT	FF	BRAM	URAM	DSP	Start
synth_1	constrs_1	Running synth_design...												2/15/17 12:44 PM
impl_1	constrs_1	Not started												

Tcl Console | Messages | Log | Reports | Design Runs

double click

I/O Pins Assignment (2/4)

Remember to save your assignment

smux - [C:/Users/hsipin/LD/smux/smux.xpr] - Vivado 2016.2

File Edit Flow Tools Window Layout View Help

1 I/O Planning

3

Flow Navigator

Project Manager
- Project Settings
- Add Sources
- Language Templates
- IP Catalog

IP Integrator
- Create Block Design
- Open Block Design
- Generate Block Design

Simulation
- Simulation Settings
- Run Simulation

RTL Analysis
- Elaboration Settings
- Open Elaborated Design

Synthesis
- Synthesis Settings
- Run Synthesis
- Synthesized Design
  - Constraints Wizard
  - Edit Timing Constrain
  - Set Up Debug
  - Report Timing Summa
  - Report Clock Networ
  - Report Clock Interac
  - Report Methodology
  - Report DRC

DEVONthink

Synthesized Design * - xc7a35tcpg236-1 (active)

Device Constraints
- Internal VREF
  - 0.6V
  - 0.675V
  - 0.75V
  - 0.9V
- NONE (4)
  - I/O Bank 14
  - I/O Bank 16
  - I/O Bank 34
  - I/O Bank 35

Sources | Netlist | Device Constraints

I/O Port Properties
sel
Name: sel
General | Properties | Configure | Power
Properties | Clock Regions

Package

Save Constraints 4

Select a target file to write new constraints to. Choosing an existing file will update that file with the new constraints.

Create a new file — **type the constraint file name**

File type: XDC
File name: smux.xdc
File location: <Local to Project>

Select an existing file
<select a target file>

OK Cancel

I/O Ports

Name	Direction	Neg Diff Pair	Package Pin	Fixed	Bank	I/O Std	Vcco	Vref	Drive Strength	Slew Type	Pull
All ports (4)											
Scalar ports (4)											
a	IN		V17	☑	14	LVCMOS33*	3.300				NONE
b	IN		V16	☑	14	LVCMOS33*	3.300				NONE
out	OUT		U16	☑	14	LVCMOS33*	3.300		12	SLOW	NONE
sel	IN		W16	☑	14	default (LVCMOS18)	1.800				NONE

2

LVCMOS18
LVCMOS25
LVCMOS33
LVTTL
MOBILE_DDR
PCI33_3
SSTL135
SSTL135_R

change to LVCMOS33

Tcl Console | Messages | Log | Reports | Design Runs | Package Pins | I/O Ports

I/O Port: sel

I/O Pins Assignment (3/4)

smux - [C:/Users/hsipin/LD/smux/smux.xpr] - Vivado 2016.2

File Edit Flow Tools Window Layout View Help

Synthesis Out-of-date more info

Flow Navigator

- Project Manager
  - Project Settings
  - Add Sources
  - Language Templates
  - IP Catalog
- IP Integrator
  - Create Block Design
  - Open Block Design
  - Generate Block Design
- Simulation
  - Simulation Settings
  - Run Simulation
- RTL Analysis
  - Elaboration Settings
  - Open Elaborated Design
- Synthesis
  - Synthesis Settings
  - Run Synthesis
  - Synthesized Design
    - Constraints Wizard
    - Edit Timing Constrain
    - Set Up Debug
    - Report Timing Summa
    - Report Clock Networ
    - Report Clock Interac
    - Report Methodology
    - Report DRC

Synthesized Design - xc7a35tcpg236-1 (active)

Device Constraints

Internal VREF
- 0.6V
- 0.675V
- 0.75V
- 0.9V
- NONE (4)
  - I/O Bank 14
  - I/O Bank 16
  - I/O Bank 34
  - I/O Bank 35

Sources | Netlist | Device Constraints

I/O Port Properties

sel

Name: sel

General | Properties | Configure | Power

Properties | Clock Regions

Package | Device

Confirm Close

OK to close 'Synthesized Design'?

Don't show this dialog again

OK | Cancel

I/O Ports

Name	Direction	Neg Diff Pair	Package Pin	Fixed	Bank	I/O Std	Vcco	Vref	Drive Strength	Slew Type	Pull
All ports (4)											
Scalar ports (4)											
a	IN		V17	☑	14	LVCMOS33*	3.300				NONE
b	IN		V16	☑	14	LVCMOS33*	3.300				NONE
out	OUT		U16	☑	14	LVCMOS33*	3.300		12	SLOW	NONE
sel	IN		W16	☑	14	LVCMOS33*	3.300				NONE

Tcl Console | Messages | Log | Reports | Design Runs | Package Pins | I/O Ports

DEVONthink

I/O Pins Assignment (4/4)

smux - [C:/Users/hsipin/LD/smux/smux.xpr] - Vivado 2016.2

File Edit Flow Tools Window Layout View Help

Synthesis Out-of-date more info

Project Manager - smux

Sources

- Design Sources (1)
  - smux (smux.v)
- Constraints (1)
  - constrs_1 (1)
    - smux.xdc (target)
- Simulation Sources (1)
  - sim_1 (1)

Hierarchy | Libraries | Compile Order

Source File Properties

smux.xdc

Enabled

Location: C:/Users/hsipin/LD/smux/smux.srcs/constrs_1/new

Type: XDC

General | Properties

Project Summary | smux.xdc *

C:/Users/hsipin/LD/smux/smux.srcs/constrs_1/new/smux.xdc

```
set_property PACKAGE_PIN V17 [get_ports a]
set_property IOSTANDARD LVCMOS33 [get_ports a]
set_property PACKAGE_PIN V16 [get_ports b]
set_property IOSTANDARD LVCMOS33 [get_ports b]
set_property PACKAGE_PIN U16 [get_ports out]
set_property IOSTANDARD LVCMOS33 [get_ports out]
set_property PACKAGE_PIN W16 [get_ports sel]
set_property IOSTANDARD LVCMOS33 [get_ports sel]
```

Or you can create the file directly and then added by "Add Sources" (constraints)

Design Runs

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Failed Routes	LUT	FF	BRAM	URAM	DSP	Start
synth_1	constrs_1	Synthesis Out-of-date							1	0	0	0	0	2/15/17 12:44 PI
impl_1	constrs_1	Not started												

Tcl Console | Messages | Log | Reports | Design Runs

9:0 Insert XDC

Synthesis and Implementation (1/6)

smux - [C:/Users/hsipin/LD/smux/smux.xpr] - Vivado 2016.2

File Edit Flow Tools Window Layout View Help

Synthesis Out-of-date more info

Flow Navigator
- Project Manager
  - Project Settings
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  - Open Elaborated Design
- Synthesis
  - Synthesis Settings
  - Run Synthesis
  - Open Synthesized Design
- Implementation
  - Implementation Settings
  - Run Implementation
  - Open Implemented Design
- Program and Debug
  - Bitstream Settings
  - Generate Bitstream
  - Open Hardware Manager

Project Manager - smux

Sources
- Design Sources (1)
  - smux (smux.v)
- Constraints (1)
  - constrs_1 (1)
    - smux.xdc (target)
- Simulation Sources (1)
  - sim_1 (1)

Hierarchy Libraries Compile

Source File Properties
smux.xdc
Enabled
Location: C:/Users/hsipi
Type: XDC
General Properties

Project Summary | smux.xdc

C:/Users/hsipin/LD/smux/smux.srcs/constrs_1/new/smux.xdc

```
1 set_property PACKAGE_PIN V17 [get_ports a]
2 set_property IOSTANDARD LVCMOS33 [get_ports a]
3 set_property PACKAGE_PIN V16 [get_ports b]
4 set_property IOSTANDARD LVCMOS33 [get_ports b]
5 set_property PACKAGE_PIN U16 [get_ports out]
6 set_property IOSTANDARD LVCMOS33 [get_ports out]
7 set_property PACKAGE_PIN W16 [get_ports sel]
8 set_property IOSTANDARD LVCMOS33 [get_ports sel]
```

Synthesis is Out-of-date

Synthesis is out-of-date. OK to launch synthesis and implementation first? 'Generate Bitstream' will automatically start when synthesis and implementation completes.

If this window pops up, press "Yes"

Don't show this dialog again

Yes No Cancel

Design Runs

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Failed Routes	LUT	FF	BRAM	URAM	DSP	Start
synth_1	constrs_1	Synthesis Out-of-date							1	0	0	0	0	2/15/17 12:44 PI
impl_1	constrs_1	Not started												

double click

Tcl Console Messages Log Reports Design Runs

Generate a programming file after implementation

Synthesis and Implementation (2/6)

implementation progress information

smux - [C:/Users/hsipin/LD/smux/smux.xpr] - Vivado 2016.2

File Edit Flow Tools Window Layout View Help

Search commands

Running synth_design Cancel

Flow Navigator

Project Manager

Project Settings
Add Sources
Language Templates
IP Catalog

IP Integrator
Create Block Design
Open Block Design
Generate Block Design

Simulation
Simulation Settings
Run Simulation

RTL Analysis
Elaboration Settings
Open Elaborated Design

Synthesis
Synthesis Settings
Run Synthesis
Open Synthesized Design

Implementation
Implementation Settings
Run Implementation
Open Implemented Design

Program and Debug
Bitstream Settings
Generate Bitstream
Open Hardware Manager

Project Manager - smux

Sources

Design Sources (1)
smux (smux.v)
Constraints (1)
constrs_1 (1)
smux.xdc (target)
Simulation Sources (1)
sim_1 (1)

Hierarchy Libraries Compile Order

Source File Properties

smux.xdc

Enabled
Location: C:/Users/hsipin/LD/smux/smux.srcs/constrs_1/new
Type: XDC

General Properties

Project Summary smux.xdc

C:/Users/hsipin/LD/smux/smux.srcs/constrs_1/new/smux.xdc

```
1 set_property PACKAGE_PIN V17 [get_ports a]
2 set_property IOSTANDARD LVCMOS33 [get_ports a]
3 set_property PACKAGE_PIN V16 [get_ports b]
4 set_property IOSTANDARD LVCMOS33 [get_ports b]
5 set_property PACKAGE_PIN U16 [get_ports out]
6 set_property IOSTANDARD LVCMOS33 [get_ports out]
7 set_property PACKAGE_PIN W16 [get_ports sel]
8 set_property IOSTANDARD LVCMOS33 [get_ports sel]
```

Design Runs

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Failed Routes	LUT	FF	BRAM	URAM	DSP	Start
synth_1	constrs_1	Running synth_design...												2/15/17 1:05 PI
impl_1	constrs_1	Queued...												

Tcl Console Messages Log Reports Design Runs

DEVONthink

Synthesis and Implementation (3/6)

smux - [C:/Users/hsipin/LD/smux/smux.xpr] - Vivado 2016.2

File Edit Flow Tools Window Layout View Help

1 Power on the FPGA board

write_bitstream Complete

Flow Navigator
- Project Manager
  - Project Settings
  - Add Sources
  - Language Templates
  - IP Catalog
- IP Integrator
  - Create Block Design
  - Open Block Design
  - Generate Block Design
- Simulation
  - Simulation Settings
  - Run Simulation
- RTL Analysis
  - Elaboration Settings
  - Open Elaborated Design
- Synthesis
  - Synthesis Settings
  - Run Synthesis
  - Open Synthesized Design
- Implementation
  - Implementation Settings
  - Run Implementation
  - Open Implemented Design
- Program and Debug
  - Bitstream Settings
  - Generate Bitstream
  - Open Hardware Manager

Project Manager - smux

Sources
- Design Sources (1)
  - smux (smux.v)
- Constraints (1)
  - constrs_1 (1)
    - smux.xdc (target)
- Simulation Sources (1)
  - sim_1 (1)

Hierarchy | Libraries | Compile Order

Project Summary | smux.xdc

C:/Users/hsipin/LD/smux/smux.srcs/constrs_1/new/smux.xdc

```
1 set_property PACKAGE_PIN V17 [get_ports a]
2 set_property IOSTANDARD LVCMOS33 [get_ports a]
3 set_property PACKAGE_PIN V16 [get_ports b]
4 set_property IOSTANDARD LVCMOS33 [get_ports b]
5 set_property PACKAGE_PIN U16 [get_ports out]
6 set_property IOSTANDARD LVCMOS33 [get_ports out]
   PIN W16 [get_ports sel]
   ARD LVCMOS33 [get_ports sel]
```

Source File Properties

smux.xdc

Enabled

Location: C:/Users/hsipin/LD/smux/smux.srcs/

Type: XDC

General | Properties

Bitstream Generation Completed

Bitstream Generation successfully completed.

Next

2

- Open Implemented Design
- View Reports
- Open Hardware Manager
- Generate Memory Configuration File

Don't show this dialog again

OK | Cancel

Design Runs

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Failed Routes	LUT	FF	BRAM	URAM	DSP	Start
synth_1	constrs_1	synth_design Complete!							1	0	0	0	0	2/15/17 1
impl_1	constrs_1	write_bitstream Complete!	NA	NA	NA	NA	NA	0	1	0	0	0	0	2/15/17 1

After synthesis and implementation

Tcl Console | Messages | Log | Reports | Design Runs

Synthesis and Implementation (4/6)

smux - [C:/Users/hsipin/LD/smux/smux.xpr] - Vivado 2016.2

File Edit Flow Tools Window Layout View Help

Default Layout | Dashboard

Sharing Screenshot
A link to your screenshot has been copied to your clipboard.
Close

Flow Navigator

- Project Manager
  - Project Settings
  - Add Sources
  - Language Templates
  - IP Catalog
- IP Integrator
  - Create Block Design
  - Open Block Design
  - Generate Block Design
- Simulation
  - Simulation Settings
  - Run Simulation
- RTL Analysis
  - Elaboration Settings
  - Open Elaborated Design
- Synthesis
  - Synthesis Settings
  - Run Synthesis
  - Open Synthesized Design
- Implementation
  - Implementation Settings
  - Run Implementation
  - Open Implemented Design
- Program and Debug
  - Bitstream Settings
  - Generate Bitstream
  - Hardware Manager

Hardware Manager - unconnected

No hardware target is open. Open target

Auto Connect
Recent Targets
Available Targets on Server
Open New Target...

Hardware

No content

Properties

Select an object to see properties

.xdc

ers/hsipin/LD/smux/smux.srcs/constrs_1/new/smux.xdc

```
t_property PACKAGE_PIN V17 [get_ports a]
t_property IOSTANDARD LVCMOS33 [get_ports a]
3 set_property PACKAGE_PIN V16 [get_ports b]
4 set_property IOSTANDARD LVCMOS33 [get_ports b]
5 set_property PACKAGE_PIN U16 [get_ports out]
6 set_property IOSTANDARD LVCMOS33 [get_ports out]
7 set_property PACKAGE_PIN W16 [get_ports sel]
8 set_property IOSTANDARD LVCMOS33 [get_ports sel]
```

Tcl Console

```
reset_run synth_1
launch_runs impl_1 -to_step write_bitstream
[Wed Feb 15 13:05:07 2017] Launched synth_1...
Run output will be captured here: C:/Users/hsipin/LD/smux/smux.runs/synth_1/runme.log
[Wed Feb 15 13:05:07 2017] Launched impl_1...
Run output will be captured here: C:/Users/hsipin/LD/smux/smux.runs/impl_1/runme.log
open_hw
```

Type a Tcl command here

Tcl Console | Messages | Serial I/O Links | Serial I/O Scans

DEVONthink

Synthesis and Implementation (5/6)

smux - [C:/Users/hsipin/LD/smux/smux.xpr] - Vivado 2016.2

File Edit Flow Tools Window Layout View Help

Default Layout | Dashboard | write_bitstream Complete

Flow Navigator

- Project Manager
  - Project Settings
  - Add Sources
  - Language Templates
  - IP Catalog
- IP Integrator
  - Create Block Design
  - Open Block Design
  - Generate Block Design
- Simulation
  - Simulation Settings
  - Run Simulation
- RTL Analysis
  - Elaboration Settings
  - Open Elaborated Design
- Synthesis
  - Synthesis Settings
  - Run Synthesis
  - Open Synthesized Design
- Implementation
  - Implementation Settings
  - Run Implementation
  - Open Implemented Design
- Program and Debug
  - Bitstream Settings
  - Generate Bitstream
  - Hardware Manager

Hardware Manager - localhost/xilinx_tcf/Digilent/210183A28121A

There are no debug cores. Program device Refresh device

Hardware: xc7a35t_0

Name	Status
localhost (1)	Connected
xilinx_tcf/Digilent/210183A28121A (1)	Open
xc7a35t_0 (1)	Programmed
XADC (System Monitor)	

smux.xdc

C:/Users/hsipin/LD/smux/smux.srcs/constrs_1/new/smux.xdc

```
1 set_property PACKAGE_PIN V17 [get_ports a]
2 set_property IOSTANDARD LVCMOS33 [get_ports a]
3 set_property PACKAGE_PIN V16 [get_ports b]
4 set_property IOSTANDARD LVCMOS33 [get_ports b]
5 set_property PACKAGE_PIN U16 [get_ports out]
6 set_property IOSTANDARD LVCMOS33 [get_ports out]
7 set_property PACKAGE_PIN W16 [get_ports sel]
8 set_property IOSTANDARD LVCMOS33 [get_ports sel]
```

Program Device

Select a bitstream programming file and download it to your hardware device. You can optionally select a debug probes file that corresponds to the debug cores contained in the bitstream programming file.

Bitstream file: C:/Users/hsipin/LD/smux/smux.runs/impl_1/smux.bit

Debug probes file:

☑ Enable end of startup check

Program | Cancel

Tcl Console

```
current_hw_device
refresh_hw_device
INFO: [Labtools 27-1434] Device xc7a35t (JTAG device index = 0) is programmed with a design that has no supported debug core(s) in it.
WARNING: [Labtools 27-3123] The debug hub core was not detected at User Scan Chain 1 or 3.
Resolution:
1. Make sure the clock connected to the debug hub (dbg_hub) core is a free running clock and is active OR
2. Manually launch hw_server with -e "set xsdb-user-bscan <C_USER_SCAN_CHAIN scan_chain_number>" to detect the debug hub at User Scan Chain
```

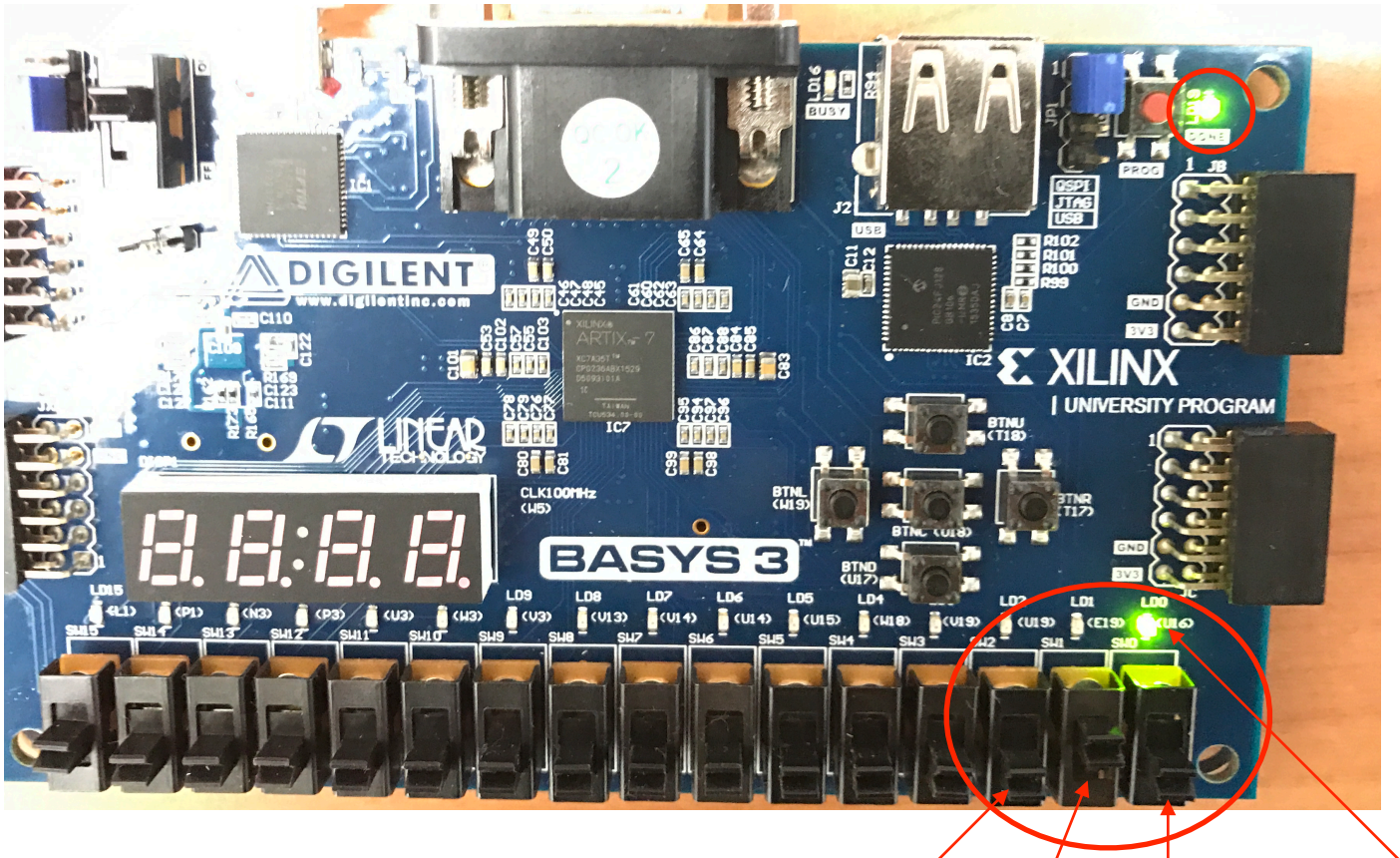
Type a Tcl command here

Tcl Console | Messages | Serial I/O Links | Serial I/O Scans

xc7a35t_0

Synthesis and Implementation (6/6)

Program Finished



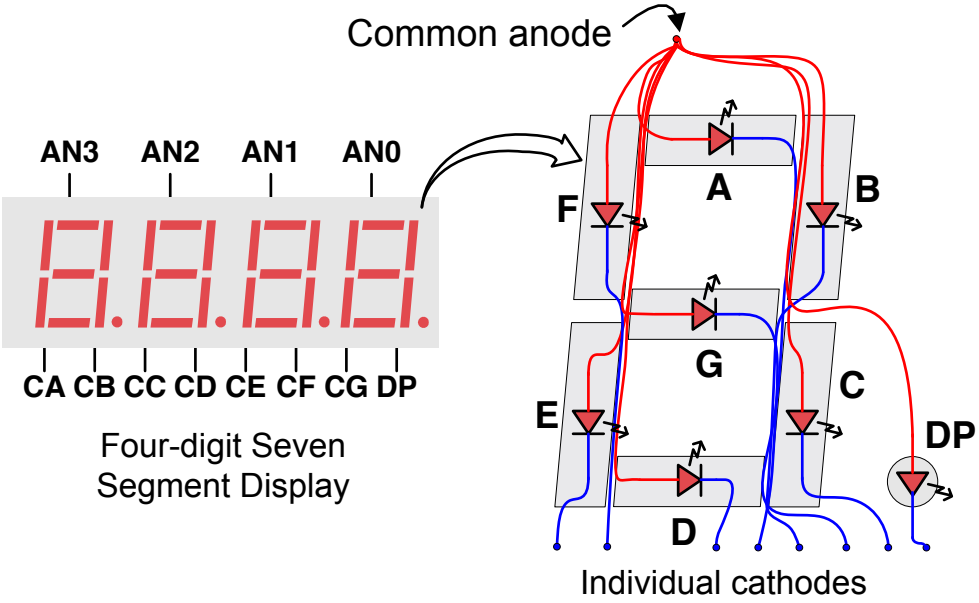
sel=0, b=1, a=0 ==> out=1

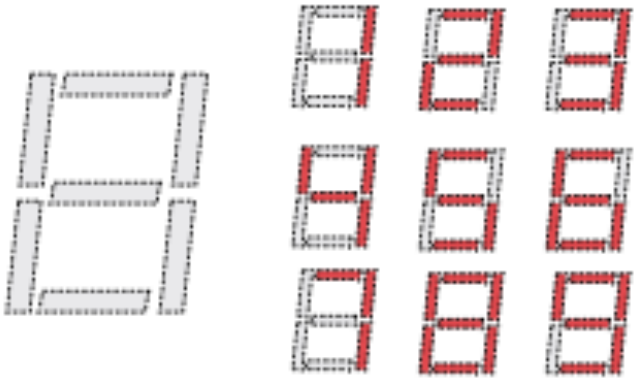
Some Notes

- Sometimes, the database of the design will be corrupted, and any changes will not take effect or your board behaves weird.
  - Open a new project with fresh source files.
- Look into the 'Errors' or 'Warnings' windows to debug your design.
- If you finish your lab at dorm and want to bring it to the lab for demo
  - DO NOT copy the entire directory to the lab and use the same directory for demo
    - Just copying the .v and .xdc files to the lab is sufficient.
    - Use 'New Project' in the lab and open the existing source files to re-implement your design for demo

7-Segment Display (1/2)

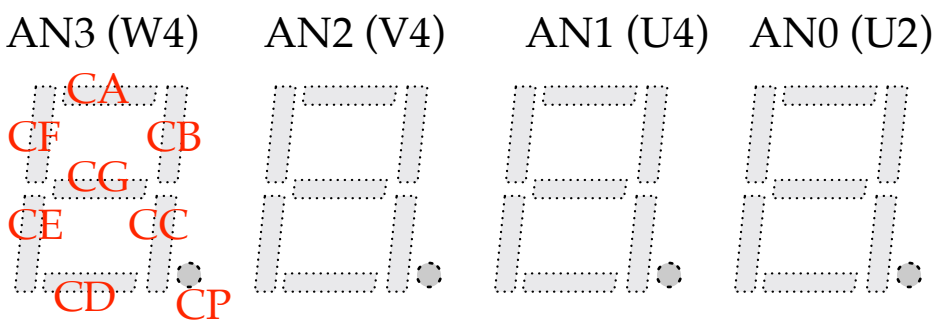
- The anodes of segments forming each digit on all four displays are connected to the same FPGA pin (AN3, AN2, AN1, AN0) (common anode)





7-Segment Display (2/2)

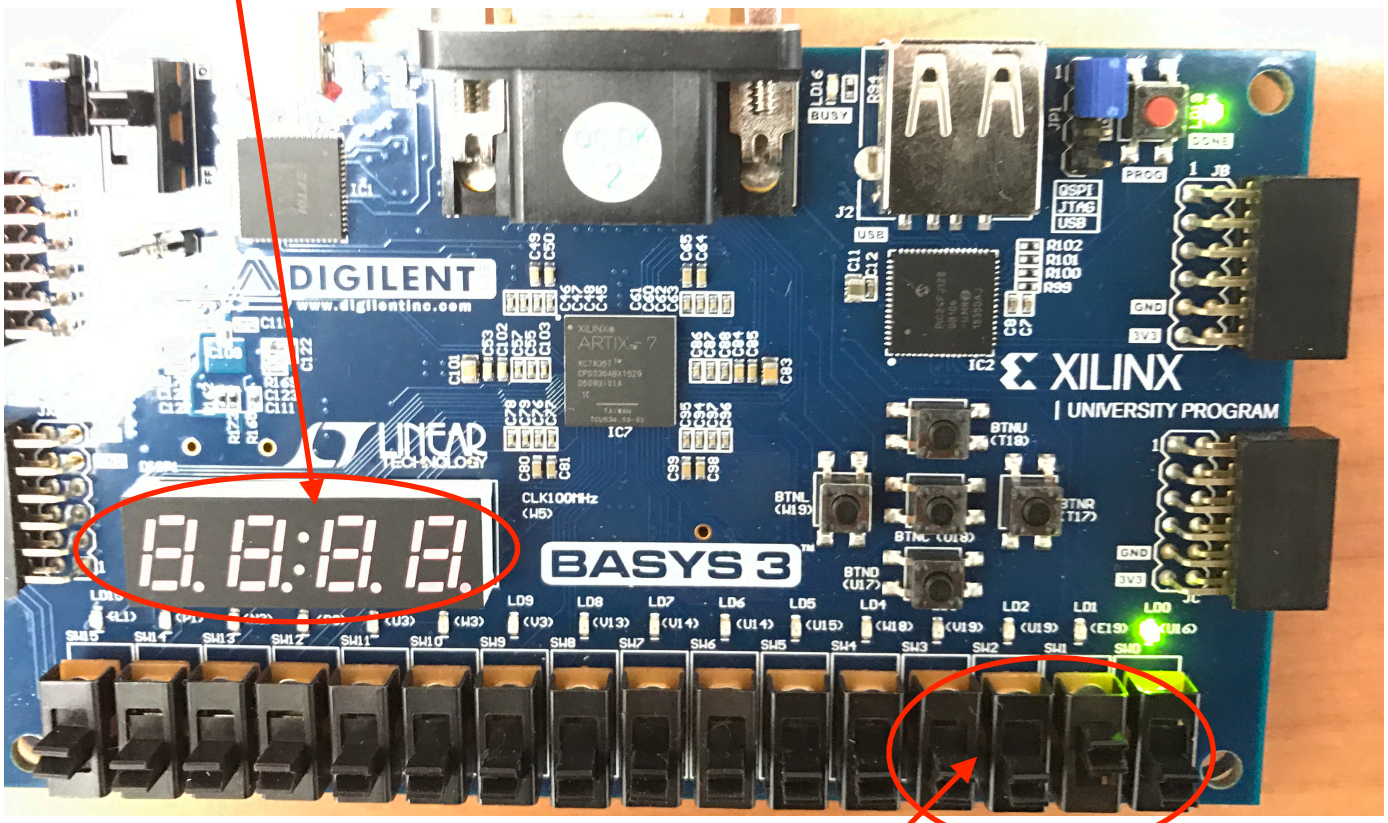
- 8 pins to control each 7-segment display
  - Including the point
- 4 pins (W4,V4,U4,U2) to choose which 7-seg to display
- Device is low activated



Symbol	CA	CB	CC	CD	CE	CF	CG	CP
FPGA Pin	W7	W6	U8	V8	U5	V5	U7	V7

Example

All 4 digits of 7-Seg Display show same number (BCD number output)

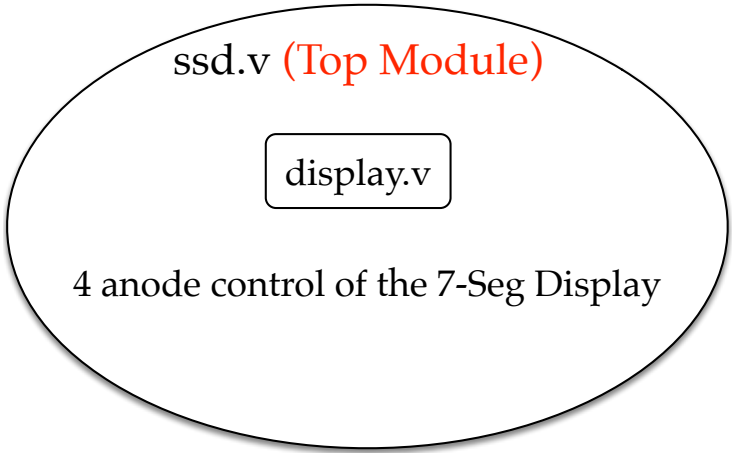


MSB

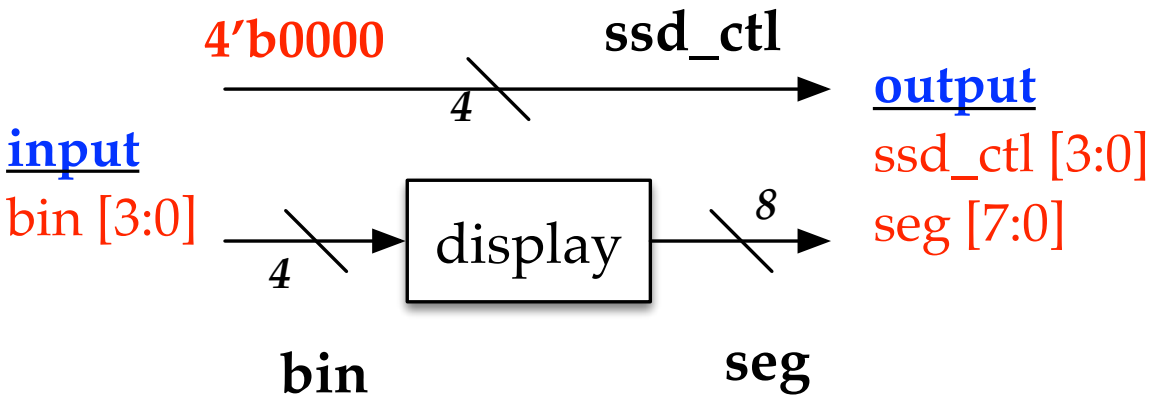
binary input: bin[3:0]

Block Diagram for 7-Seg Display

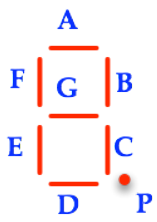
System Hierarchy



Block Diagram



A BCD to Seven-Segment Display Decoder




```
// define segment codes
`define SS_0 8'b00000011
`define SS_1 8'b10011111
`define SS_2 8'b00100101
`define SS_3 8'b00001101
`define SS_4 8'b10011001
`define SS_5 8'b01001001
`define SS_6 8'b01000001
`define SS_7 8'b00011111
`define SS_8 8'b00000001
`define SS_9 8'b00001001
```

```
module display(segs, bin);
output [7:0] segs;
input [3:0] bin;
reg [7:0] segs;

always @*
  case (bin)
    4'd0: segs = `SS_0;
    4'd1: segs = `SS_1;
    4'd2: segs = `SS_2;
    4'd3: segs = `SS_3;
    4'd4: segs = `SS_4;
    4'd5: segs = `SS_5;
    4'd6: segs = `SS_6;
    4'd7: segs = `SS_7;
    4'd8: segs = `SS_8;
    4'd9: segs = `SS_9;
    default: segs = 8'b0000000;
  endcase
endmodule
```

Top Module (ssd.v)

```
module ssd(seg, bin, ssd_ctl);
output [3:0] ssd_ctl;
output [7:0] seg;
input [3:0] bin;

display U0(.segs(seg),.bin(bin));

assign ssd_ctl = 4'b0000;

endmodule
```

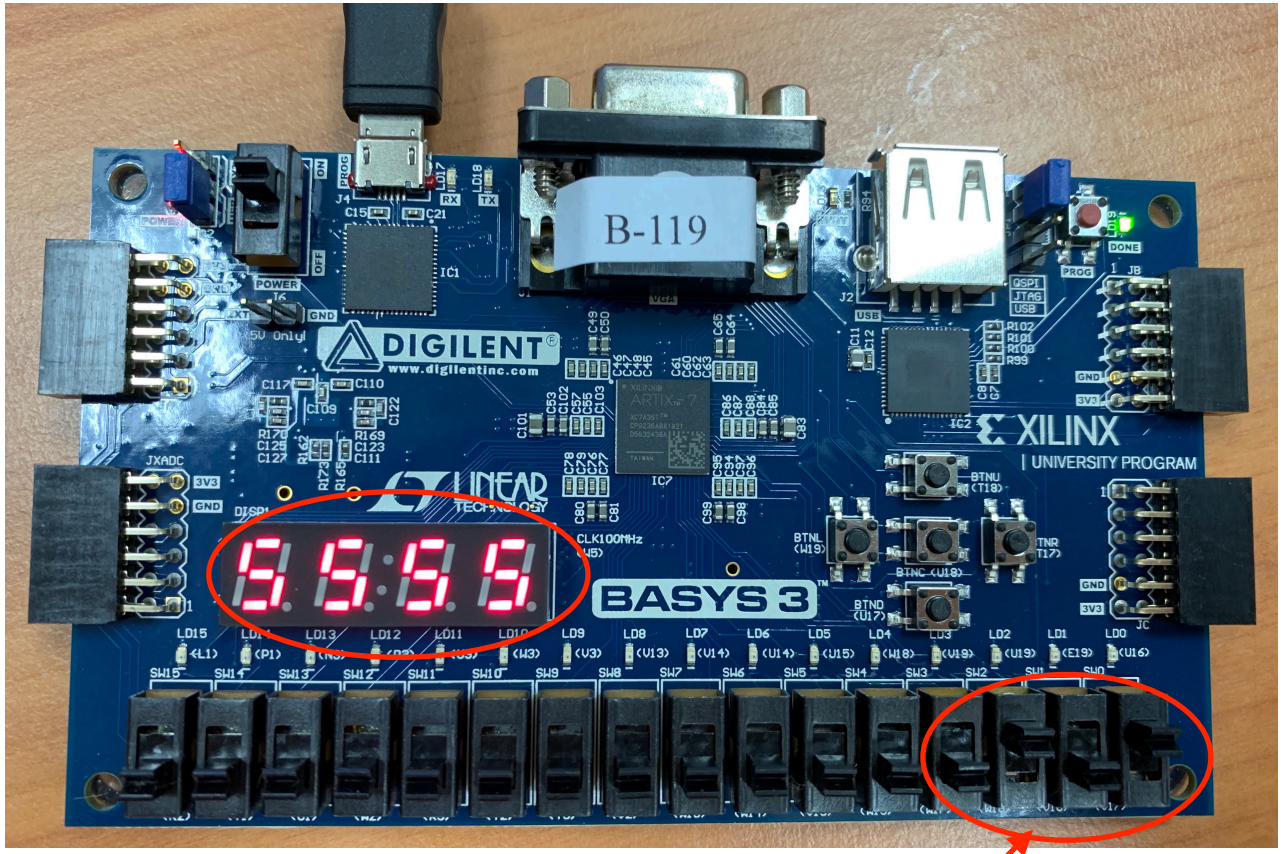
ssd.xdc (1/2)

```
# Four anode control signals
set_property PACKAGE_PIN W4 [get_ports {ssd_ctl[3]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {ssd_ctl[3]}]
set_property PACKAGE_PIN V4 [get_ports {ssd_ctl[2]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {ssd_ctl[2]}]
set_property PACKAGE_PIN U4 [get_ports {ssd_ctl[1]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {ssd_ctl[1]}]
set_property PACKAGE_PIN U2 [get_ports {ssd_ctl[0]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {ssd_ctl[0]}]

#8 common segment controls
set_property PACKAGE_PIN W7 [get_ports {seg[7]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {seg[7]}]
set_property PACKAGE_PIN W6 [get_ports {seg[6]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {seg[6]}]
set_property PACKAGE_PIN U8 [get_ports {seg[5]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {seg[5]}]
set_property PACKAGE_PIN V8 [get_ports {seg[4]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {seg[4]}]
```

ssd.xdc (2/2)

```
set_property PACKAGE_PIN U5 [get_ports {seg[3]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {seg[3]}]
set_property PACKAGE_PIN V5 [get_ports {seg[2]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {seg[2]}]
set_property PACKAGE_PIN U7 [get_ports {seg[1]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {seg[1]}]
set_property PACKAGE_PIN V7 [get_ports {seg[0]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {seg[0]}]

#4-bit binary input
set_property PACKAGE_PIN W17 [get_ports {bin[3]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {bin[3]}]
set_property PACKAGE_PIN W16 [get_ports {bin[2]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {bin[2]}]
set_property PACKAGE_PIN V16 [get_ports {bin[1]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {bin[1]}]
set_property PACKAGE_PIN V17 [get_ports {bin[0]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {bin[0]}]
```

Example



binary input: 0101