LAB01

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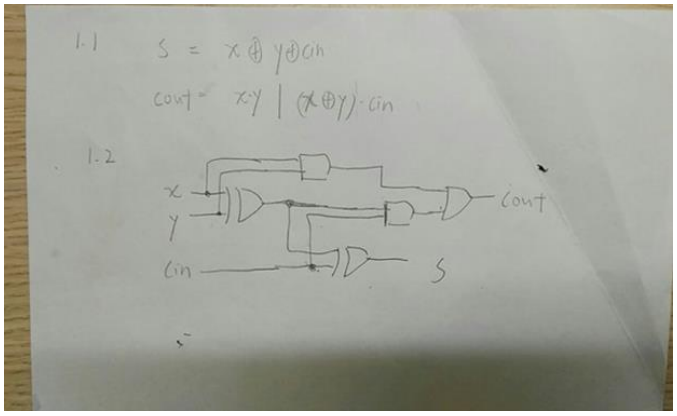
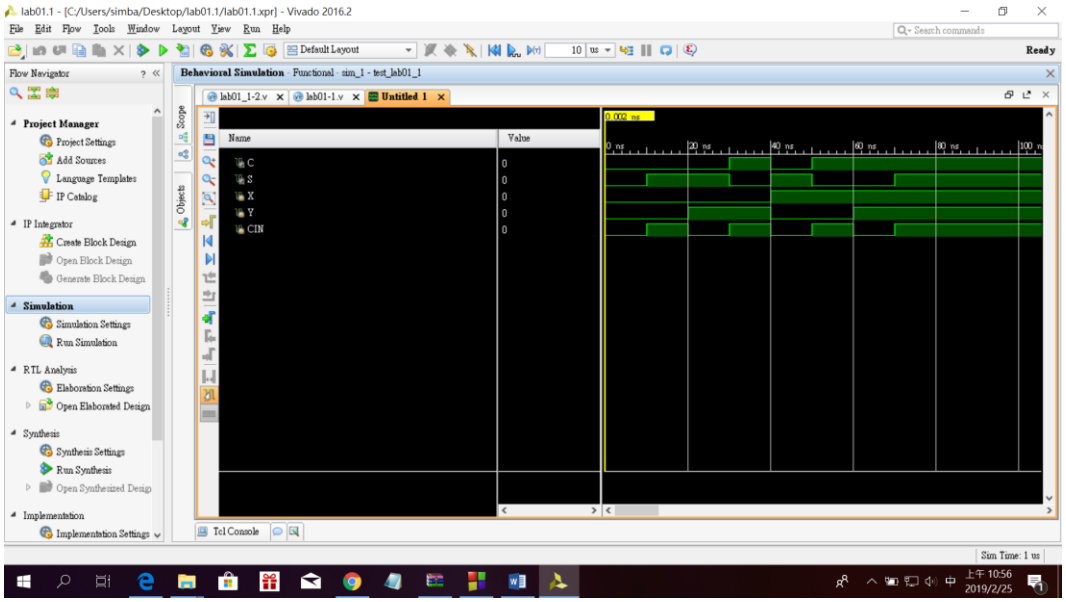
1. Input x, y, cin; output s, cout

   Diagram:



   Logic equation : s = x ^ y ^ cin cout = xy + (x^y)cin

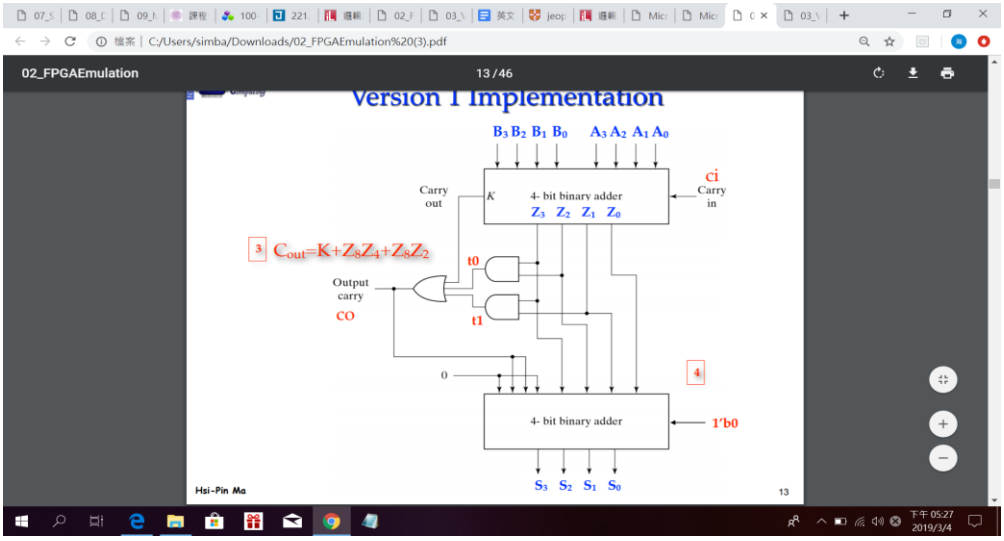
   Disscussion:



   由波形圖得知 {cout, s} = x + y + cin;

2. Input [3:0]a, [3:0]b, cin; output cout, s;

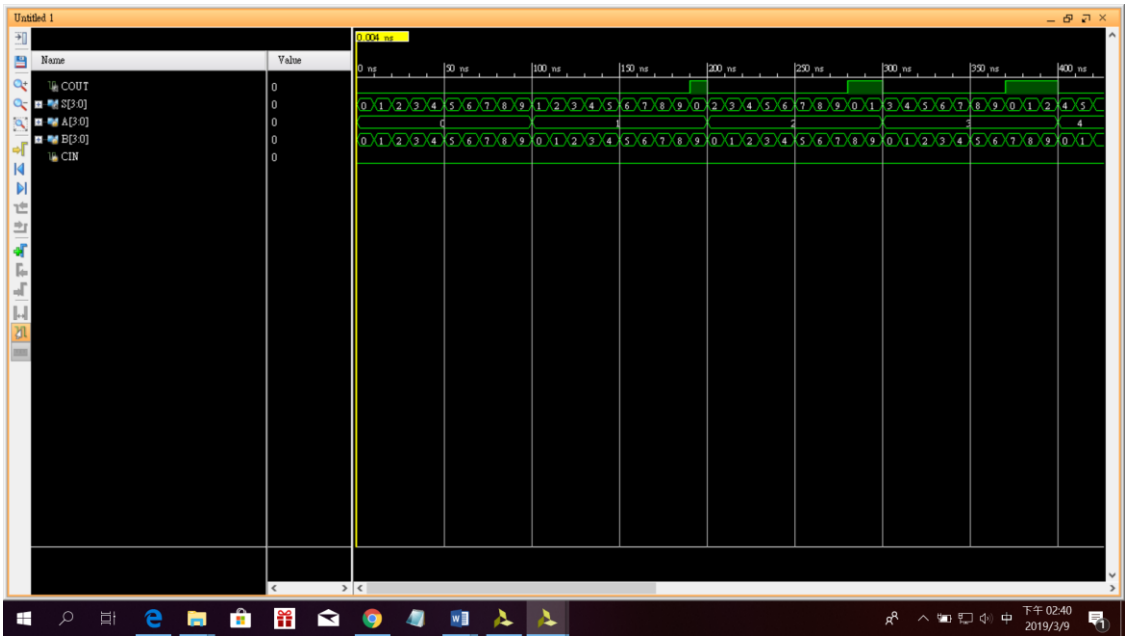
   Diagram:



Logic equation:

```
always @* begin
        if (a + b + cin > 9) begin
            cout = 1;
            s = a + b + cin + 6;
        end
        else begin
            cout = 0;
            s = a + b + cin;
        end
    end
```

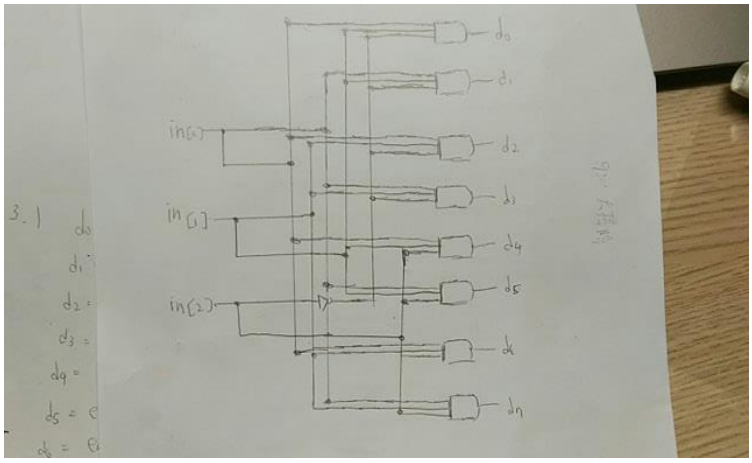
Discussion:



由波形圖得知 cout = 1; if (a + b + cin) > 9;

3. Input en, [2:0]in, [7:0]d; output [7:0]d

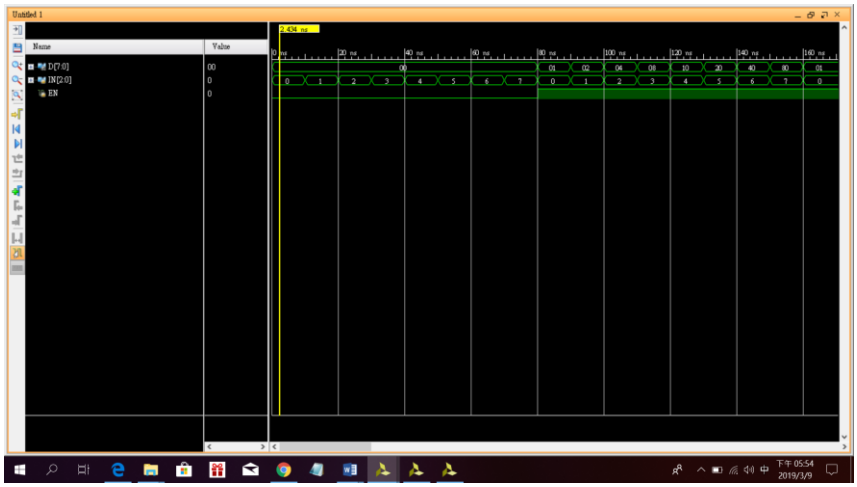
Diagram:



Logic equation:

```
assign d[0] = ~in[2] & ~in[1] & ~in[0] & en;
assign d[1] = ~in[2] & ~in[1] & in[0] & en;
assign d[2] = ~in[2] & in[1] & ~in[0] & en;
assign d[3] = ~in[2] & in[1] & in[0] & en;
assign d[4] = in[2] & ~in[1] & ~in[0] & en;
assign d[5] = in[2] & ~in[1] & in[0] & en;
assign d[6] = in[2] & in[1] & ~in[0] & en;
assign d[7] = in[2] & in[1] & in[0] & en;
```

Discussion:



Conclusion:

其實我以前上邏輯設計時候都不會打 verilog，一有 verilog 的作業我就交不出來，所以這次靠自己摸索蠻多東西的，像是 if, else 只能寫在 always 裡，還有 always 裡等號左邊要用 reg 宣告，然後除了 input, output 以外的東西都用 wire 或 reg 宣告，另外我還學會在 testbench 裡用 repeat，以前一直沒有很會用。