

計結 CH4 Part 1

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1.

(1) $(00c6ba23)_{16} = (\underline{\text{00000000}} \mid \underline{\text{000}} \mid \underline{\text{0101}} \mid \underline{\text{10100010001}})_2$

imm[11:5] RS2 IS1 func3 ↓ opcode
 ↓
 imm[4:0]

\Rightarrow sd $x_{12}, z_0(x_{13}) \Rightarrow$ ALU function 為 add

(2) 0X4000fffd4

(3) RegWrite = 0, ALUSrc = 1, MemWrite = 1, MemRead = 0, MemToReg = 0

(4) ALU 的 input 為 x_{13} 和 z_0 .

2.

(1) $70 + 250 + 170 + 25 + 200 + 170 + 25 = 910$

(2) $70 + 250 + 170 + 25 + 200 + 250 + 25 + 170 = 1160 \text{ (ps)}$

(3) $70 + 250 + 170 + 25 + 200 + 250 = 965 \text{ (ps)}$

(4) $70 + 250 + 170 + 25 + 200 + 5 + 25 = 745 \text{ (ps)}$

(5) $70 + 250 + 170 + 25 + 200 + 170 + 25 = 910 \text{ (ps)}$

(6) 1160 (ps)

3.

(1) new clock period = $1160 + (180 - 170) \times 2 = 1180 \text{ (ps)}$

$1180 \times (1 - 0.36 \times 0.12) = 1129.024 \text{ (ps)} \quad \text{--- new CPU time}$

Performance $\propto \frac{1}{\text{CPU time}} \Rightarrow \frac{1160}{1129.024} = 1.03$

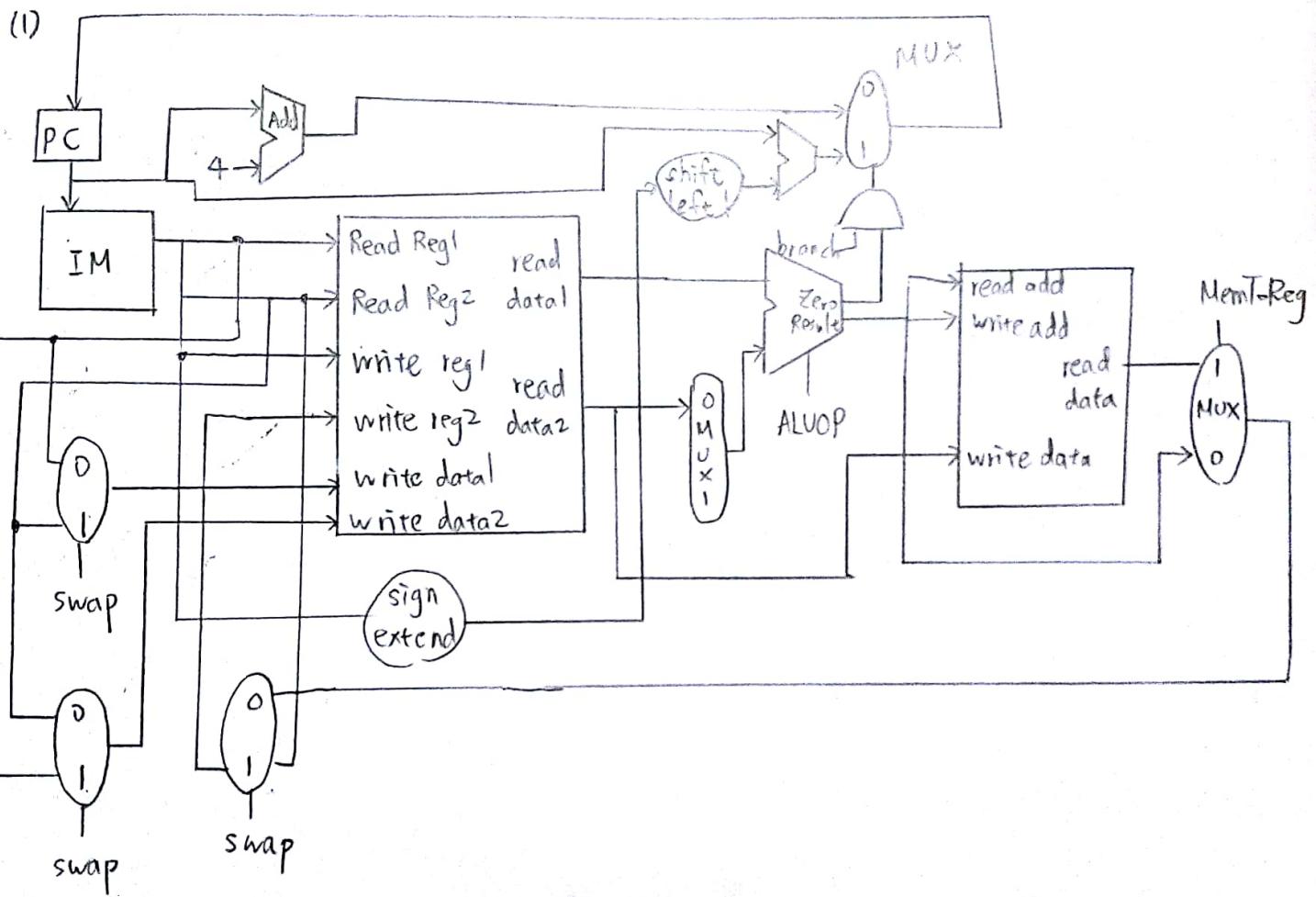
\Rightarrow new processor 的 performance 為先前的 1.03 倍。

$$(2) 1000 + 400 + 100 + 2000 + 10 \times 3 + 30 \times 2 + 1 + 100 + 5 + 500 = 4196 \rightarrow \text{new}$$

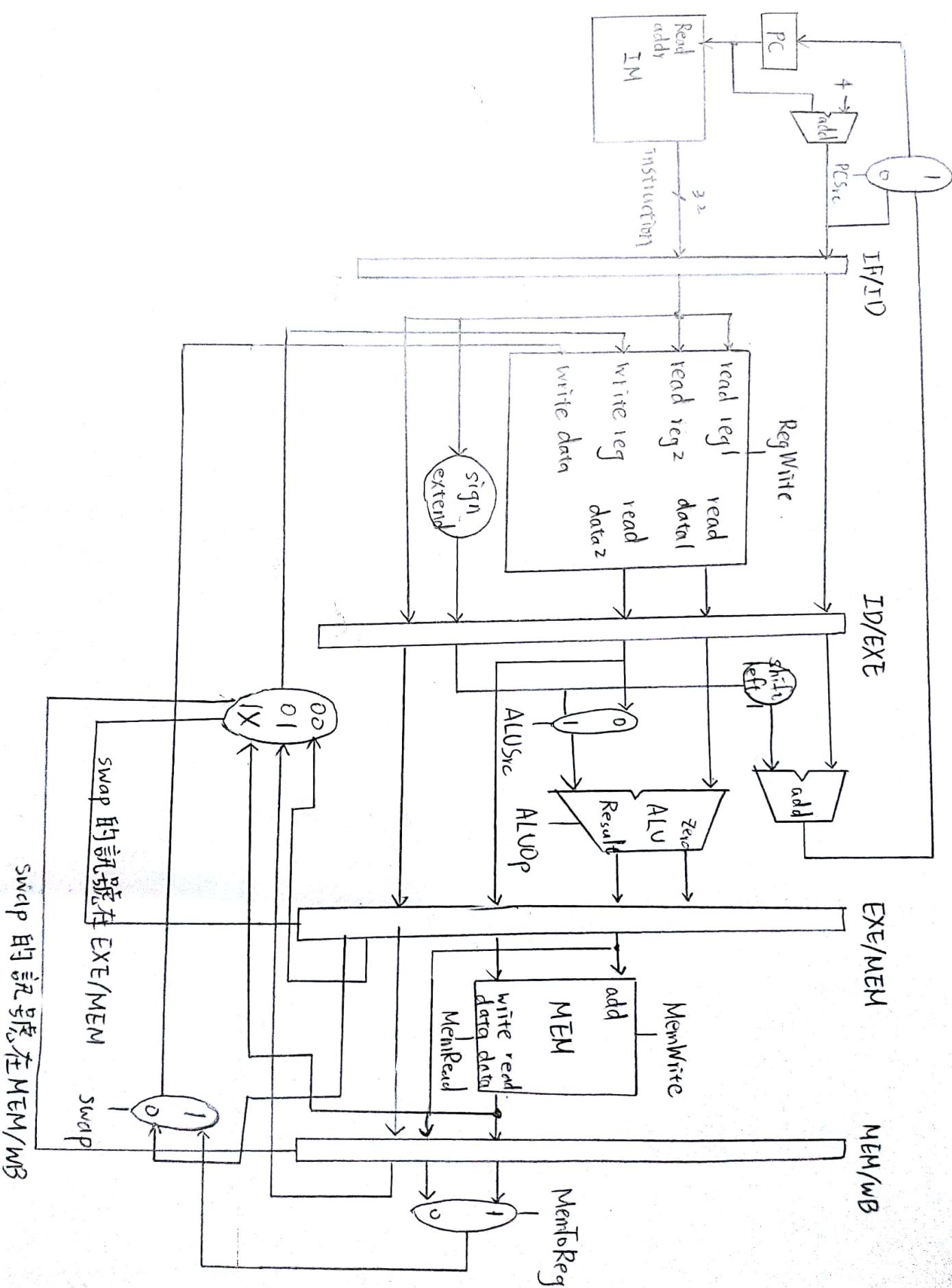
$$\text{old} = \text{new} - 200 = 3996$$

$$\frac{4196}{3996} = 1.05 \Rightarrow \text{新版的價格為舊版的 } 1.05 \text{ 倍。}$$

4.



(2)



5.

(1) 350 (ps).

(2) ID, 300 (ps).

$$(3) 20\% + 15\% = 35\%$$

6. addi x11, x12, 5

nop

nop

add x13, x11, x12

addi x14, x11, 15

nop

add x15, x13, x12

7.

(1) 設有 forwarding 的 processor 有 n 個 instruction

→ 沒有 " " " 1.1n "

$$\text{performance} \propto \frac{1}{\text{CPU time}}$$

$$\Rightarrow \frac{\text{performance without forwarding}}{\text{performance with forwarding}} = \frac{300 \times n}{250 \times 1.1n} = 1.09$$

$$(2) \frac{300 \times n}{250 \times p n} < 1 \Rightarrow p > 1.2 \Rightarrow \text{percentage of nop} > 0.2 = 20\%$$

8.

	clock cycle											
	1	2	3	4	5	6	7	8	9	10.	11	12
sd x29, 12(x16)	IF	ID	EX	MEM	WB							
ld x29, 8(x16)		IF	ID	EX	MEM	WB						
sub x17, x15, x14			IF	ID	EX	MEM	WB					
bez x17, label				IF	ID	**	**	EX	MEM	WB		
add x15, x11, x14					IF	**	**	ID	EX	MEM	WB	
sub x15, x30, x14						**	**	IF	ID	EX	MEM	WB

9. (1)

clock cycle

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
ld x10, 0(x13)	IF	ID	EXE	MEM	WB										
ld x11, 8(x13)	IF	ID	EXE	MEM	WB										
add x12, x10, x11	IF	ID	**	EXE	MEM	WB									
addi x13, x13, -16	IF	ID	**	EXE	MEM	WB									
bnez x12, LOOP	**	IF	ID	EXE	MEM	WB									
ld x10, 0(x13)	IF	ID	EXE	MEM	WB										
add x12, x10, x11	IF	ID	EXE	MEM	WB										
addi x13, x13, -16	IF	ID	**	EXE	MEM	WB									
bnez x12, LOOP	**	IF	ID	EXE	MEM	WB									

stage 7, 8, 9, 10, 13, 14, 15, 16 are the stages without useful work.

(2) 無。

10.

(1)

① add x11, x12, x13

nop

nop

, add x14, x11, x15

add x5, x6, x7

② add x11, x12, x13

add x14, x11, x15

add x5, x6, x7

③ add x11, x12, x13

nop

add x14, x11, x15

add x5, x6, x7

④ add x11, x12, x13

add x14, x11, x15

add x5, x6, x7

(2)

① ld x11, o(x12)

nop

nop

add x15, x11, x13

add x5, x6, x7

② ld x11, o(x12)

nop

nop

add x15, x11, x13

add x5, x6, x7

③ ld x11, o(x12)

nop

add x15, x11, x13

add x5, x6, x7

④ ld x11, o(x12)

nop

add x15, x11, x13

add x5, x6, x7

(3)

① add x_{11}, x_{12}, x_{13}
add x_5, x_6, x_7
nop
add x_{14}, x_{11}, x_{12}

② add x_{11}, x_{12}, x_{13}
add x_5, x_6, x_7
nop
add x_{14}, x_{11}, x_{12}

③ add x_{11}, x_{12}, x_{13}
add x_5, x_6, x_7
add x_{14}, x_{11}, x_{12}

④ add x_{11}, x_{12}, x_{13}
add x_5, x_6, x_7
add x_{14}, x_{11}, x_{12}

(4)

① Id $x_{11}, o(x_{12})$
add x_5, x_6, x_7
nop
add x_{14}, x_{11}, x_{13}

② Id $x_{11}, o(x_{12})$
add x_5, x_6, x_7
nop
add x_{14}, x_{11}, x_{13}

③ Id $x_{11}, o(x_{12})$
add x_5, x_6, x_7
add x_{14}, x_{11}, x_{13}

(5)

① add x₁₁, x₁₂, x₁₃

nop

nop

add x₅, x₁₁, x₁₅

add x₁₆, x₁₁, x₁₂

② add x₁₁, x₁₂, x₁₃

add x₅, x₁₁, x₁₅

add x₁₆, x₁₁, x₁₂

③ add x₁₁, x₁₂, x₁₃

nop

add x₅, x₁₁, x₁₅

add x₁₆, x₁₁, x₁₂

④ add x₁₁, x₁₂, x₁₃

add x₅, x₁₁, x₁₅

add x₁₆, x₁₁, x₁₂

		clock		cycle						
		1	2	3	4	5	6	7	8	9
add	x_{15}, x_{12}, x_{11}	IF	ID	EXE	MEM	WB				
ld	$x_{13}, 4(x_{15})$		IF	ID	EX	MEM	WB			
ld	$x_{12}, 0(x_2)$			IF	ID	EXE	MEM	WB		
or	x_{13}, x_{15}, x_{13}				IF	ID	EXE	MEM	WB	
sd	$x_{13}, 0(x_{15})$					IF	ID	EXE	MEM	WB
forward A		X	X	0	2	1	0	0	X	X
forward B		X	X	0	0	1	2	2	X	X