

Lab 1: Verilog HDL

Objective

- ✓ Review fundamental logic components.
- ✓ Introduce Verilog HDL modeling and verification.

Prerequisite

- ✓ Fundamentals of logic gates and Verilog HDL.

Experiments

- 1 Design and verify a 4-bit binary-to-Gray-code converter (input: $abcd$, output: $wxyz$, a and w are the MSB).
 - 1.1 Derive the Boolean function/logic equation.
 - 1.2 Draw the related logic diagram.
 - 1.3 Construct the Verilog RTL code for the converter and use a testbench to simulate the logic behavior for verification.
- 2 Design a signed 4-bit binary adder/subtractor with input a ($a_3a_2a_1a_0$), b ($b_3b_2b_1b_0$), m as the operator control (0 for addition and 1 for subtraction); output s ($s_3s_2s_1s_0$), v as overflow indicator.
 - 2.1 Derive the Boolean function/logic equation.
 - 2.2 Draw the related logic diagram.
 - 2.3 Construct the Verilog RTL code for the function and use a given testbench to simulate the logic behavior for verification.
- 3 (Bonus) For two 3-bit signed numbers a ($a_2a_1a_0$) and b ($b_2b_1b_0$), build a logic circuit to output o ($o_2o_1o_0$) as the larger number and use a given testbench for verification.