Digital IC Design

Exercise 3
Sequential circuits

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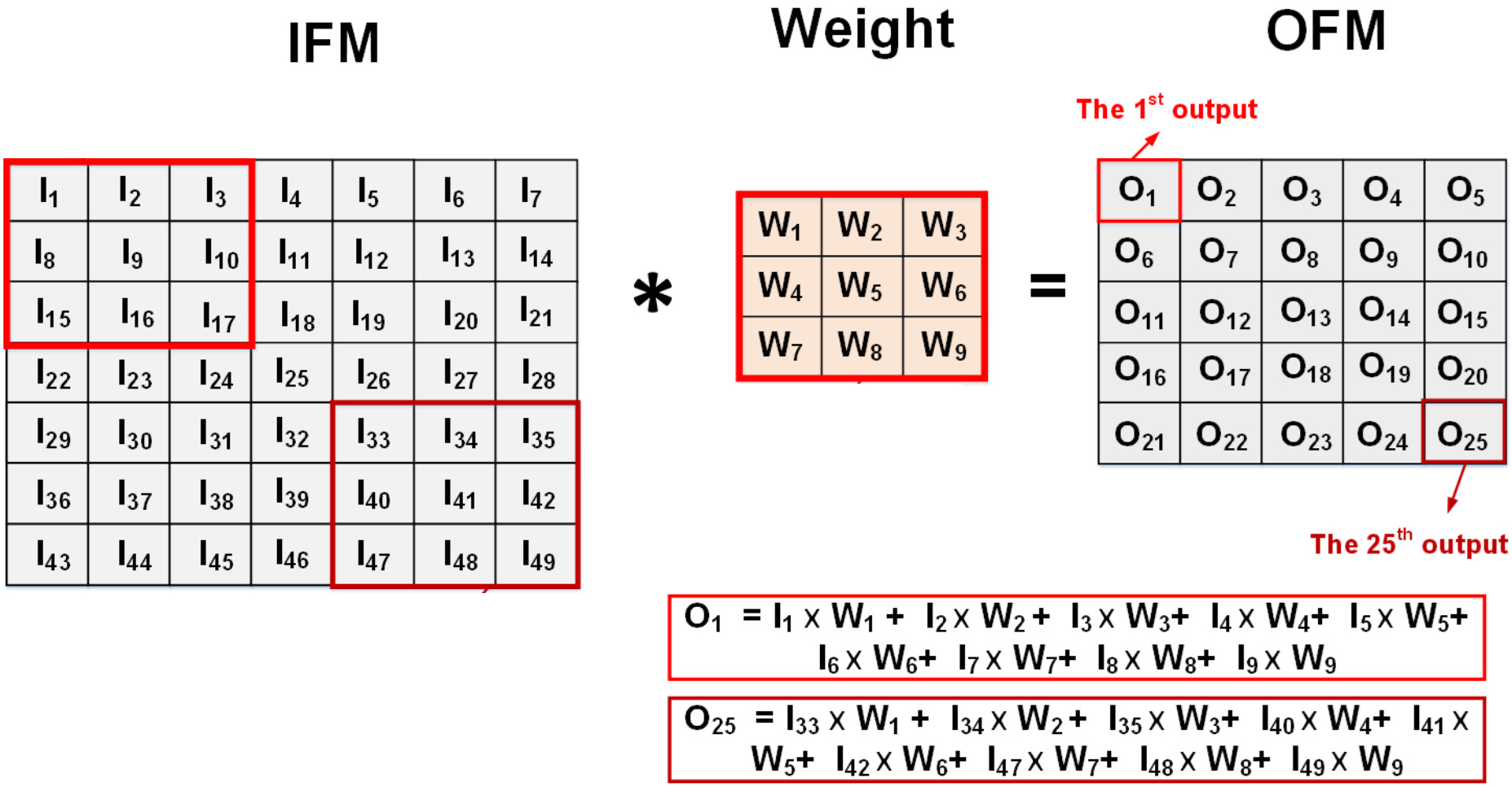
Introduction of 3x3 Convolution



$$O_1 = I_1 \times W_1 + I_2 \times W_2 + I_3 \times W_3 + I_4 \times W_4 + I_5 \times W_5 + I_6 \times W_6 + I_7 \times W_7 + I_8 \times W_8 + I_9 \times W_9$$

$$O_{25} = I_{33} \times W_1 + I_{34} \times W_2 + I_{35} \times W_3 + I_{40} \times W_4 + I_{41} \times W_5 + I_{42} \times W_6 + I_{47} \times W_7 + I_{48} \times W_8 + I_{49} \times W_9$$

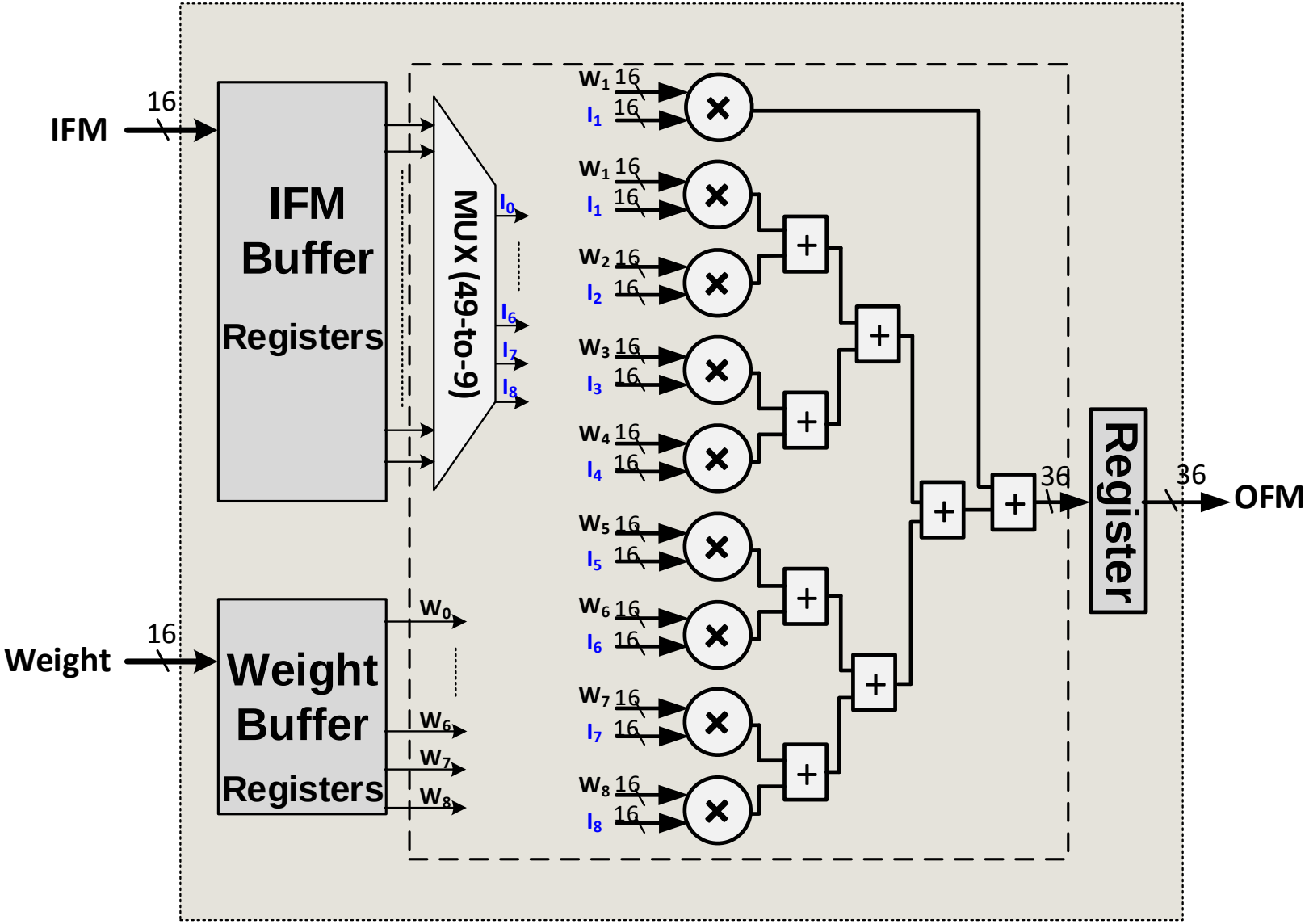
Timing/Area Analysis of Sequential Circuits [30%]

- Use Verilog to implement 3x3 convolution kernel
  - Implement the kernels **without** pipeline techniques.
    - 2 input buffers (defined by TA) and 9 Multiplier(16bit) & 1 Adder tree
    - **Measure the area and throughput**
    - **You can change the clock period** (.tcl & pattern)
  - The function of this kernel should be correct
    - Verify the kernels in gate level simulation using the pattern provided by TA.

For the .tcl file, you can only modify:
(1)clock period
(2)design_name & search_path

Example: Block Diagram of 3x3 Convolution

- 3x3 Convolution kernel without pipeline



Timing/Area Analysis of Sequential Circuits [30%]

- Use Verilog to implement 3x3 convolution kernel
  - Implement the kernels using pipeline techniques.
    - 2 input buffers (defined by TA) and 9 Multiplier(16bit) & 1 Adder tree
    - **Measure the area and throughput**
    - **You can change the clock period** (.tcl & pattern)
  - The frequency of the kernel should faster than **1.25GHz**
  - The function of these two kernels should be correct
    - Verify the kernels in gate level simulation using the pattern provided by TA.

For the .tcl file, you can only modify:
(1)clock period
(2)design_name & search_path

Optimize the Sequential Circuits [40%]

- Design a 3x3 convolution kernel
  - **Optimize the area efficiency (Throughput/Area)**
    - You can change the clock period (.tcl & pattern)
    - You can modify buffers, Mux, Multipliers, etc.
      - **Area efficiency > 550 GOPS/mm^2 [get 40 point]**
      - **Area efficiency > 400 GOPS/mm^2 [get 30 point]**
      - **Area efficiency > 350 GOPS/mm^2[get 50 point]**
      - **Area efficiency > 250 GOPS/mm^2[get 10 point]**
  - Plot the block diagram of the designed kernel
  - Verify the designs in gate level simulation using the pattern provided by TA.
  - Throughput (OPS) = (Operations/operating time)
    - Operations: (number of 16-bit multiplies during the operating time) x 2
    - Operating time: form positive edge of in_valid to negative edge of out_valid

For the .tcl file, you can only modify:
(1)clock period
(2)design_name & search_path

Specifications for 3x3 convolution kernels

- Signals:

Input signals	Bit width	Description
clk	1	Positive edge trigger clock
rst_n	1	Asynchronous active-low reset.
in_valid	1	When High, **In_IFMs** are valid
Weight_valid	1	When High, **In_Weights** are valid
In_IFM	16	Input feature map**, give in 49 cycles**
In_Weight	16	Weights**, give in 9 cycle**
Output signals	Bit width	Description
Out_valid	1	High when out is valid, then Patten will check Out_OFM. **(It should maintain 25 cycles)**
Out_OFM	36	The answers of the 3x3 convolution. **(It should maintain 25 cycles)**

- Settings:
  - In_IFM & In_Weight should be received by registers.
  - The output ports should be set as registers.

Submission of Exerice-3

- Please upload the following files
  - Due day: PM 11:55 on 11/13
  - Report.pdf
  - Convolution_without_pipeline.v
  - Convolution_with_pipeline.v
  - Convolution_optimize.v
  - Synthesis_clk_period.txt

(Please describe the clock periods, you chose to synthesis in the report, in the “Synthesis_clk_period.txt”. TA will use the clock period to run and check your design correct or not.)