數位積體電路

Lab4

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4-1 Minimal Energy-Delay Product

實驗流程:

1. 透過 **irun TESTBED.v -define RTL -debug -notimingchecks -loadpli1 debpli:novas_pli_boot** 指令進行驗證，確認功能無誤。

2. 透過 **dc_shell-t -f syn.tcl | tee syn.log** 進行合成

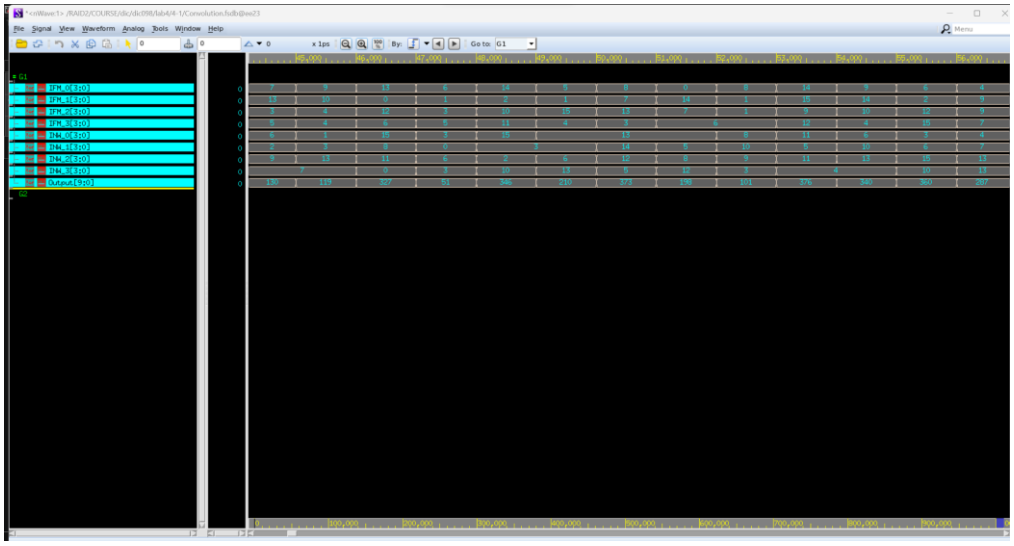
```
Operating Conditions: PVT_0P7V_25C   Library: asap7sc7p5t_INVBUF_RVT_TT_0830201
Wire Load Model Mode: top

  Startpoint: INW_3[2] (input port)
  Endpoint: Output[8] (output port)
  Path Group: default
  Path Type: max

  Point                                                   Incr       Path
  -----------------------------------------------------------------------------
  input external delay                                    0.00       0.00 f
  INW_3[2] (in)                                           0.00       0.00 f
  mult_19_4/b[2] (Convolution_DW_mult_uns_0)              0.00       0.00 f
  mult_19_4/U116/Y (NAND2xp33_ASAP7_75t_R)               20.81      20.81 r
  mult_19_4/U114/Y (NOR2xp33_ASAP7_75t_R)                30.77      51.58 f
  mult_19_4/U39/SN (FAx1_ASAP7_75t_R)                    61.57     113.15 f
  mult_19_4/U95/Y (XNOR2xp5_ASAP7_75t_R)                 28.23     141.37 r
  mult_19_4/U92/Y (NAND2xp33_ASAP7_75t_R)                12.63     154.01 f
  mult_19_4/U91/Y (NAND2xp33_ASAP7_75t_R)                25.12     179.12 r
  mult_19_4/U87/Y (NAND2xp33_ASAP7_75t_R)                14.50     193.62 f
  mult_19_4/U86/Y (NAND2xp33_ASAP7_75t_R)                25.11     218.74 r
  mult_19_4/U82/Y (NAND2xp33_ASAP7_75t_R)                14.50     233.23 f
  mult_19_4/U81/Y (NAND2xp33_ASAP7_75t_R)                25.11     258.34 r
  mult_19_4/U78/Y (XOR2xp5_ASAP7_75t_R)                  39.48     297.82 r
  mult_19_4/product[6] (Convolution_DW_mult_uns_0)        0.00     297.82 r
  add_1_root_add_0_root_add_19_3/B[6] (Convolution_DW01_add_2)
                                                          0.00     297.82 r
  add_1_root_add_0_root_add_19_3/U1_6/SN (FAx1_ASAP7_75t_R)
                                                         40.86     338.68 r
  add_1_root_add_0_root_add_19_3/U11/Y (INVx1_ASAP7_75t_R)
                                                         17.87     356.55 f
  add_1_root_add_0_root_add_19_3/SUM[6] (Convolution_DW01_add_2)
                                                          0.00     356.55 f
  add_0_root_add_0_root_add_19_3/B[6] (Convolution_DW01_add_0)
                                                          0.00     356.55 f
  add_0_root_add_0_root_add_19_3/U1_6/CON (FAx1_ASAP7_75t_R)
                                                         22.90     379.45 r
  add_0_root_add_0_root_add_19_3/U4/Y (INVx1_ASAP7_75t_R)
                                                         15.27     394.72 f
  add_0_root_add_0_root_add_19_3/U1_7/CON (FAx1_ASAP7_75t_R)
                                                         20.30     415.02 r
  add_0_root_add_0_root_add_19_3/U3/Y (INVx1_ASAP7_75t_R)
                                                         15.27     430.29 f
  add_0_root_add_0_root_add_19_3/U1_8/SN (FAx1_ASAP7_75t_R)
                                                         37.50     467.79 f
  add_0_root_add_0_root_add_19_3/U11/Y (INVx1_ASAP7_75t_R)
                                                          8.03     475.82 r
  add_0_root_add_0_root_add_19_3/SUM[8] (Convolution_DW01_add_0)
                                                          0.00     475.82 r
  Output[8] (out)                                         0.00     475.82 r
  data arrival time                                                475.82

  max_delay                                             500.00     500.00
  output external delay                                   0.00     500.00
  data required time                                               500.00
  -----------------------------------------------------------------------------
  data required time                                               500.00
  data arrival time                                               -475.82
  -----------------------------------------------------------------------------
  slack (MET)                                                      24.18
```

Report/timing

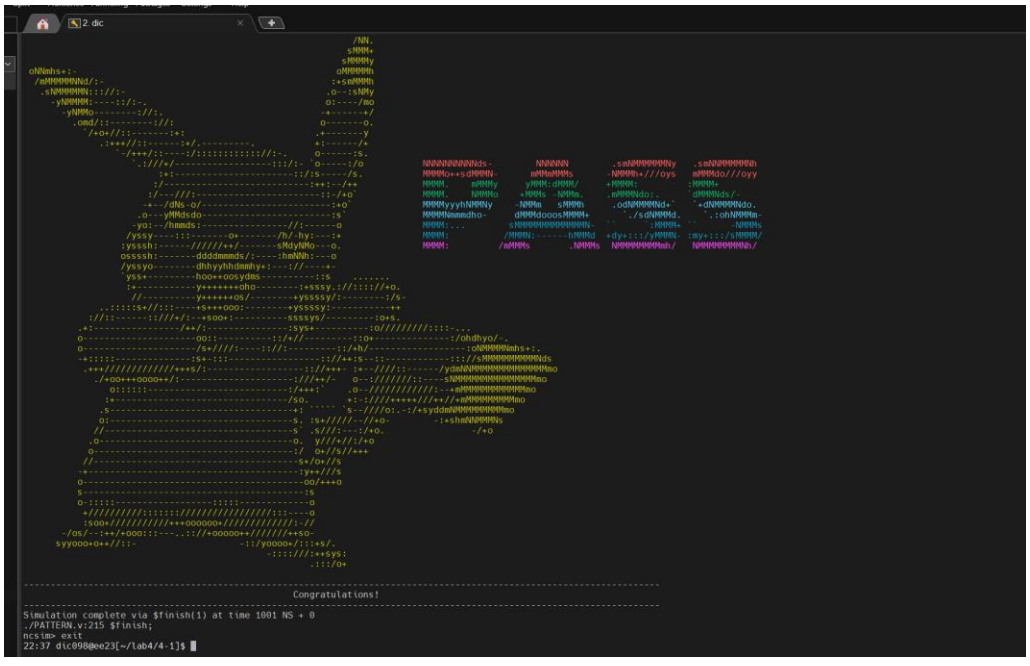
```
****************************************
Report : area
Design : Convolution
Version: T-2022.03
Date   : Mon Dec  4 22:19:59 2023
****************************************

Library(s) Used:

    asap7sc7p5t_SIMPLE_RVT_TT_08302018 (File: /RAID2/COURSE/dic/dic098/ASAP7_PDKandLIB_v1p6/ASAP7_PDKandLIB_v1p6/lib_release_191006/asap7_7p5t_library/rev25/LIB/NLDM/asap7sc7p5t_SIMPLE_RVT_TT_08302018.db)
    asap7sc7p5t_INVBUF_RVT_TT_08302018 (File: /RAID2/COURSE/dic/dic098/ASAP7_PDKandLIB_v1p6/ASAP7_PDKandLIB_v1p6/lib_release_191006/asap7_7p5t_library/rev25/LIB/NLDM/asap7sc7p5t_INVBUF_RVT_TT_08302018.db)

Number of ports:                          203
Number of nets:                           509
Number of cells:                          308
Number of combinational cells:            301
Number of sequential cells:                 0
Number of macros/black boxes:               0
Number of buf/inv:                         64
Number of references:                       8

Combinational area:             426.435838
Buf/Inv area:                    44.789761
Noncombinational area:            0.000000
Macro/Black Box area:             0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                426.435838
Total area:                 undefined
1
```

Report/area

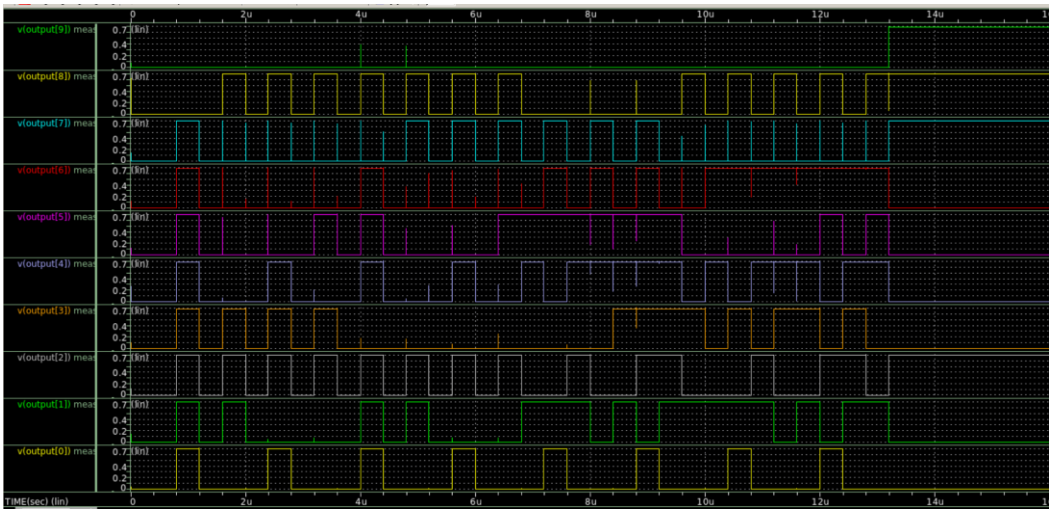
3. 透過 nWave 查看波型是否正確



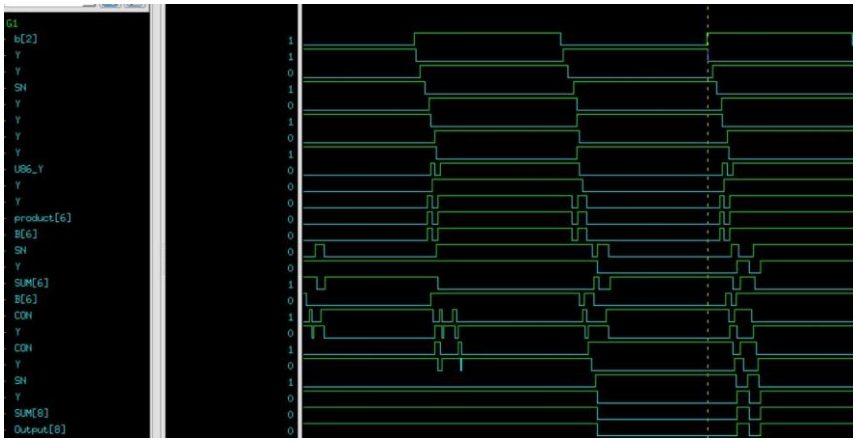
4. 進行 GATE level 驗證，透過 **irun TESTBED.v -define GATE -debug -v asap7sc7p5t_SIMPLE_RVT_TT_08302018.v asap7sc7p5t_SEQ_RVT_TT_08302018.v asap7sc7p5t_INVBUF_RVT_TT_08302018.v -nontcglitch -loadpli1 debpli:novas_pli_boot** 指令進行驗證



5. 透過 verilog2spice 轉換成.sp 檔案，並且查看波形來驗證功能是否正確



實驗結果:

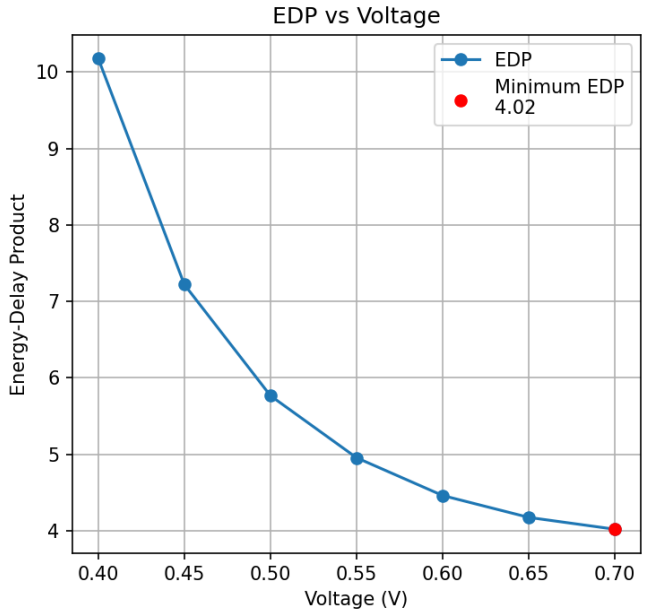


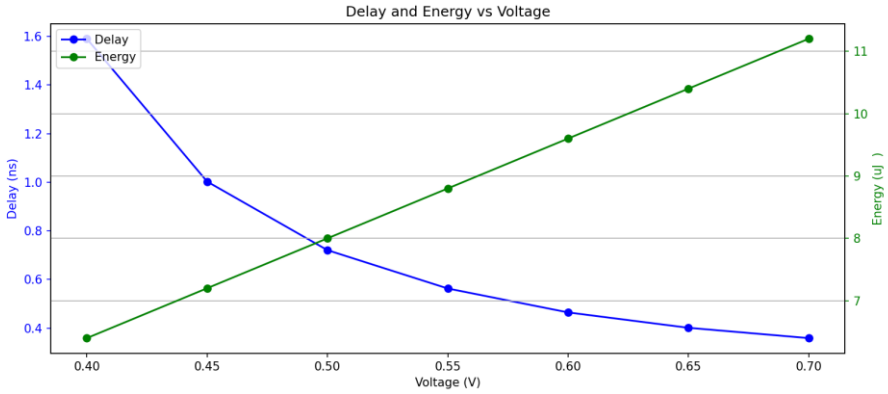
Worst Case delay:

當 Pattern 從 0000 0000 0000 0000 0011 1011 0011 1111 變成

1111 1111 1111 1111 0011 1011 0011 1011 會有 Worst Case delay

```
Find delay ('358.9131', 'p')
Find delay ('401.3902', 'p')
Find delay ('464.6374', 'p')
Find delay ('563.0217', 'p')
Find delay ('720.7155', 'p')
Find delay ('1.0027', 'n')
Find delay ('1.5900', 'n')
Find energy ('11.2000', 'u')
Find energy ('10.4000', 'u')
Find energy ('9.6000', 'u')
Find energy ('8.8000', 'u')
Find energy ('8.0000', 'u')
Find energy ('7.2000', 'u')
Find energy ('6.4000', 'u')
Find power ('210.9779', 'n')
Find power ('176.8539', 'n')
Find power ('147.9913', 'n')
Find power ('122.5796', 'n')
Find power ('100.1675', 'n')
Find power ('79.6209', 'n')
Find power ('61.4935', 'n')
Voltage = 0.7 V, Delay = 0.3589131 ns, Energy = 11.2 uJ, Power = 0.2109779 uW, EDP = 4.019826719999999
Voltage = 0.65 V, Delay = 0.4013902 ns, Energy = 10.4 uJ, Power = 0.1768539 uW, EDP = 4.17445808
Voltage = 0.6 V, Delay = 0.46463740000000003 ns, Energy = 9.6 uJ, Power = 0.1479913 uW, EDP = 4.46051904
Voltage = 0.55 V, Delay = 0.5630217000000001 ns, Energy = 8.8 uJ, Power = 0.1225796 uW, EDP = 4.954590960000001
Voltage = 0.5 V, Delay = 0.7207155000000001 ns, Energy = 8.0 uJ, Power = 0.1001675 uW, EDP = 5.7657240000000005
Voltage = 0.45 V, Delay = 1.0027 ns, Energy = 7.2 uJ, Power = 0.07962090000000001 uW, EDP = 7.21944
Voltage = 0.4 V, Delay = 1.59 ns, Energy = 6.4 uJ, Power = 0.0614935 uW, EDP = 10.176000000000002
```





討論:

從上面的實驗結果中，我們可以看到當電壓為0.7的時候，可以獲得最小的energy-delay product，而從其他實驗結果中，我們也可以觀察到，當電壓的值逐漸變小後，電路的energy會逐漸上升，也證明了能量的公式(1)，當電壓上升，所消耗的能量也會跟著上升，我們也可以看到，當電壓下降後，電路的延遲會跟著上升，因為電路操作在低電壓的模式下，驅動能力會跟著減弱，導致電路的響應速度變慢，造成延遲上升。

透過這個實驗讓我了解到，當我們在設計電路時，我們必須要去做取捨，根據我們電路的需求，是以性能為優先，還是功耗為優先，確定了這些因素後，我們才能夠去設計合適的電路。

$$E = C_L V_{DD}^2 P_{0\to1} + t_{sc} V_{DD} I_{peak} P_{0\to1} + V_{DD} I_{leakage}$$

(1)能量公式

4-2 Minimal Delay

實驗流程:

1. 透過 **01_run_Synthesis** 合成

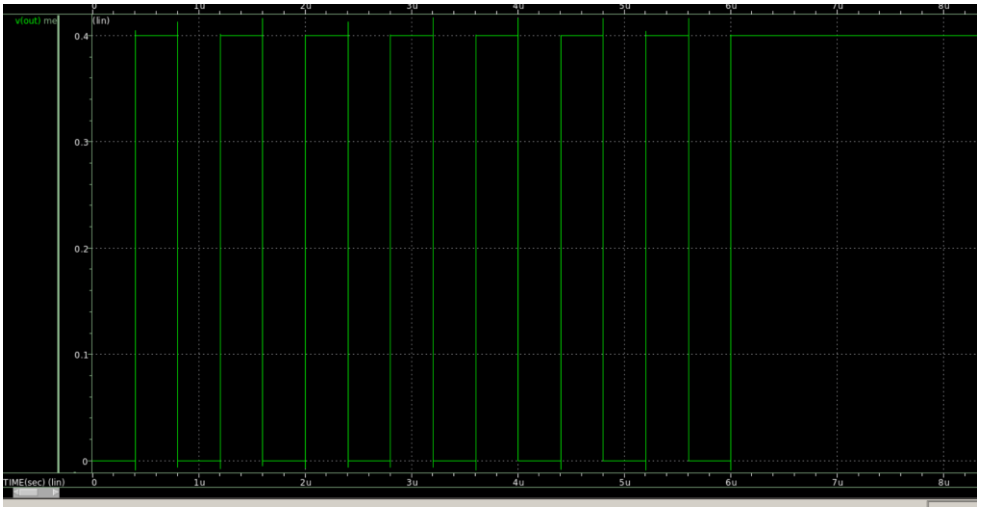
```
Design : Comparator
Version: T-2022.03
Date   : Wed Dec  6 03:20:59 2023
****************************************

Library(s) Used:

    asap7sc7p5t_SIMPLE_RVT_TT_08302018 (File: /RAID2/COURSE/dic/dic098/ASAP7_PDKandLIB_v1p6/ASAP7_PDKandLIB_v1p6/lib_release_191006/asap7_
7p5t_library/rev25/LIB/NLDM/asap7sc7p5t_SIMPLE_RVT_TT_08302018.db)

Number of ports:                          129
Number of nets:                           210
Number of cells:                           82
Number of combinational cells:             82
Number of sequential cells:                 0
Number of macros/black boxes:               0
Number of buf/inv:                          0
Number of references:                       6

Combinational area:               161.663038
Buf/Inv area:                       0.000000
Noncombinational area:              0.000000
Macro/Black Box area:               0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                  161.663038
Total area:                 undefined
1
```

Report/timing

```
  Startpoint: B[47] (input port)
  Endpoint: Out (output port)
  Path Group: default
  Path Type: max

  Point                                    Incr       Path
  -----------------------------------------------------------
  input external delay                     0.00       0.00 r
  B[47] (in)                               0.00       0.00 r
  U79/Y (XNOR2xp5_ASAP7_75t_R)            14.28      14.28 r
  U87/Y (NAND4xp25_ASAP7_75t_R)           18.47      32.74 f
  U74/Y (NOR5xp2_ASAP7_75t_R)             26.10      58.84 r
  U83/Y (NAND4xp25_ASAP7_75t_R)           21.97      80.81 f
  U10/Y (NOR5xp2_ASAP7_75t_R)             17.38      98.19 r
  Out (out)                                0.00      98.19 r
  data arrival time                                  98.19

  max_delay                              280.00     280.00
  output external delay                    0.00     280.00
  data required time                                280.00
  -----------------------------------------------------------
  data required time                                280.00
  data arrival time                                 -98.19
  -----------------------------------------------------------
  slack (MET)                                       181.81


1
```

Report/area

2. 透過 verilog2spice 轉換成.sp 檔案，並且查看波型驗證功能是否正確



實驗結果:

- Minimize the Delay

```
****** transient analysis tnom=  25.000 temp=  25.000 ******
delay=   2.0069n  targ= 404.5069n   trig= 402.5000n
tr=    1.5441n  targ= 405.3895n   trig= 403.8454n
tf= 134.6870p  targ= 803.5908n   trig= 803.4561n
power=  14.8175n  from=   0.             to=   8.7500u
```

未優化前

```
****** transient analysis tnom=  25.000 temp=  25.000 ******
delay= 436.7641p  targ= 200.4868n   trig= 200.0500n
tr= 245.3715p  targ= 200.6364n   trig= 200.3911n
tf=  22.9225p  targ= 400.1722n   trig= 400.1493n
power= 116.6198n  from=   0.             to=   8.7500u
```

優化後

討論:

在優化前我觀察到了電路的tr太大，代表電路的驅動能力較弱，信號上升慢，因此我在輸出端加了一個BUFX3_ASAP7_75T_R(1)，透過增加這個buffer，可以減少電路的負載電容，一旦負載電容減小，同樣電壓的情況下，對電容的充電速度就快，信號上升緣也會因此變得陡峭，因此透過這種方式，不但可以提高電路的驅動能力，也可以有效的降低電路的延遲，並且在查看每個cell的基本特性後，我發現NOR的延遲相較於NAND來的較大，因此，我透過NAND來實現NOR閘(2)，並且在wire loading的部分，都加上一個buffer(3)，來降低電路的延遲。

```
XU10 VSS VDD  n1 n2 n3 n4 n5 OUT_buf NOR5xp2_ASAP7_75t_R
X_BUF1 VSS VDD OUT_buf OUT BUFX4F_ASAP7_75T_R
```

(1)示意圖

```
.subckt NOR5 VSS VDD A B C D E out
    X1 VSS VDD A INV_A INVX1_ASAP7_75T_R
    X2 VSS VDD B INV_B INVX1_ASAP7_75T_R
    X3 VSS VDD C INV_C INVX1_ASAP7_75T_R
    X4 VSS VDD D INV_D INVX1_ASAP7_75T_R
    X5 VSS VDD E INV_E INVX1_ASAP7_75T_R
    X6 VSS VDD INV_A INV_B INV_C INV_D INV_E y NAND5XP2_ASAP7_75T_R
    X7 VSS VDD Y OUT INVX1_ASAP7_75T_R
.ENDS

.subckt NOR4 VSS VDD A B C D  out
    X1 VSS VDD A INV_A INVX1_ASAP7_75T_R
    X2 VSS VDD B INV_B INVX1_ASAP7_75T_R
    X3 VSS VDD C INV_C INVX1_ASAP7_75T_R
    X4 VSS VDD D INV_D INVX1_ASAP7_75T_R
    X6 VSS VDD INV_A INV_B INV_C INV_D Y NAND4XP25_ASAP7_75T_R
    X7 VSS VDD Y OUT INVX1_ASAP7_75T_R
.ENDS
```

(2)示意圖

```
X_wire_buf54 VSS VDD n43_buf n43 BUFX3_ASAP7_75T_R
X_wire_buf55 VSS VDD n68_buf n68 BUFX3_ASAP7_75T_R
X_wire_buf56 VSS VDD n67_buf n67 BUFX3_ASAP7_75T_R
X_wire_buf57 VSS VDD n66_buf n66 BUFX3_ASAP7_75T_R
X_wire_buf58 VSS VDD n65_buf n65 BUFX3_ASAP7_75T_R
X_wire_buf59 VSS VDD n72_buf n72 BUFX3_ASAP7_75T_R
X_wire_buf60 VSS VDD n71_buf n71 BUFX3_ASAP7_75T_R
X_wire_buf61 VSS VDD n70_buf n70 BUFX3_ASAP7_75T_R
X_wire_buf62 VSS VDD n69_buf n69 BUFX3_ASAP7_75T_R
X_wire_buf63 VSS VDD n42_buf n42 BUFX3_ASAP7_75T_R
X_wire_buf64 VSS VDD n77_buf n77 BUFX3_ASAP7_75T_R
X_wire_buf65 VSS VDD n76_buf n76 BUFX3_ASAP7_75T_R
X_wire_buf66 VSS VDD n75_buf n75 BUFX3_ASAP7_75T_R
X_wire_buf67 VSS VDD n74_buf n74 BUFX3_ASAP7_75T_R
X_wire_buf68 VSS VDD n81_buf n81 BUFX3_ASAP7_75T_R
X_wire_buf69 VSS VDD n80_buf n80 BUFX3_ASAP7_75T_R
X_wire_buf70 VSS VDD n79_buf n79 BUFX3_ASAP7_75T_R
X_wire_buf71 VSS VDD n78_buf n78 BUFX3_ASAP7_75T_R
X_wire_buf72 VSS VDD n1_buf n1 BUFX3_ASAP7_75T_R
X_wire_buf73 VSS VDD n55_buf n55 BUFX3_ASAP7_75T_R
X_wire_buf74 VSS VDD n46_buf n46 BUFX3_ASAP7_75T_R
X_wire_buf75 VSS VDD n64_buf n64 BUFX3_ASAP7_75T_R
X_wire_buf76 VSS VDD n73_buf n73 BUFX3_ASAP7_75T_R
X_wire_buf77 VSS VDD n10_buf n10 BUFX3_ASAP7_75T_R
X_wire_buf78 VSS VDD n19_buf n19 BUFX3_ASAP7_75T_R
X_wire_buf79 VSS VDD n28_buf n28 BUFX3_ASAP7_75T_R
```

(3)示意圖

- Measure the PPA at 0.4v and 0.7v of minimized and synthesized comparator,and analyze (Time unit :50ns)

優化前

```
****** transient analysis tnom=  25.000 temp=  25.000 ******
delay=   2.1510n  targ= 202.1795n   trig= 200.0286n
tr=   1.0020n  targ= 202.7417n   trig= 201.7398n
tf=  96.0354p  targ= 400.5302n   trig= 400.4342n
power=  64.1285n  from=   0.             to=   5.0000u
```

Supply voltage = 0.4v

```
****** transient analysis tnom=  25.000 temp=  25.000 ******
delay= 436.7641p  targ= 200.4868n   trig= 200.0500n
tr= 245.3715p  targ= 200.6364n   trig= 200.3911n
tf=  22.9225p  targ= 400.1722n   trig= 400.1493n
power= 196.1962n  from=   0.             to=   5.0000u
```

Supply voltage = 0.7v

優化後

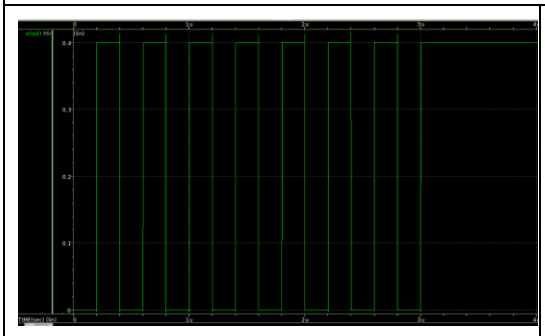
```
****** transient analysis tnom=  25.000 temp=  25.000 ******
delay=   1.0699n  targ= 201.0984n   trig= 200.0286n
tr=  72.9524p  targ= 201.1400n   trig= 201.0671n
tf=  58.8090p  targ= 400.5873n   trig= 400.5285n
power= 135.4356n  from=   0.             to=   5.0000u
```

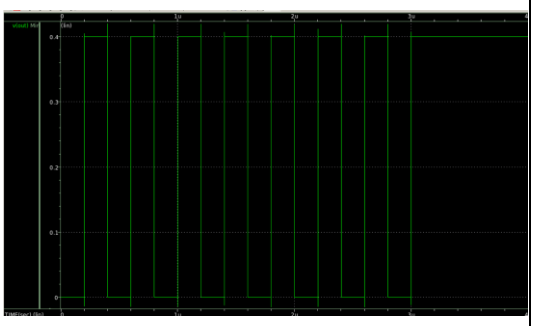
Supply voltage = 0.4v

```
****** transient analysis tnom=  25.000 temp=  25.000 ******
delay= 231.9564p  targ= 200.2820n   trig= 200.0500n
tr=  19.0087p  targ= 200.2933n   trig= 200.2743n
tf=  16.0866p  targ= 400.1860n   trig= 400.1699n
power= 429.7520n  from=   0.             to=   5.0000u
```

Supply voltage = 0.7v

功能驗證





優化前 | 優化後

PPA

優化前

	Power (W)	Performance (latency)	Area(um^2)
0.7V	0.196e-6	436.7641ps	161.66
0.4V	0.064e-6	2.1510ns	161.66

優化後

	Power (W)	Performance (latency)	Area(um^2)
0.7V	0.429e-6	231.956ps	315.87
0.4V	0.135e-6	1.0699ns	315.87

討論:

透過在不同的 Supply voltage 下，測量 PPA，我們可以觀察到當電壓上升，電路的 Power 也會隨之上升，根據 Power 公式，我們也可以推測出此結論，雖然 Power 上升，但帶來的好處是，電路的 Performance 也會提高，而因為電路在不同的 Supply voltage 功能皆正常，因此所使用的都是同一個，Area 因此不會變，而從這個實驗我們也可以知道，如果要增加電路的性能，Power 勢必會跟著上升，在 Power 跟 Performance 之間做取捨，是設計電路很重要的一個觀念。