數位積體電路

Lab5

智能系統所 312581006 張宸瑋

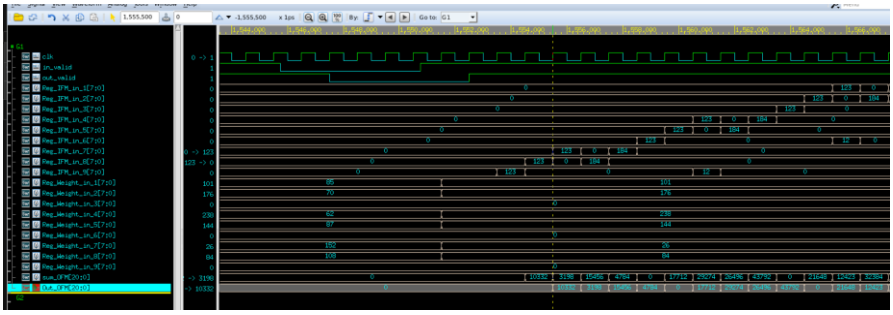
5-1 Sequential circuits

Implement a 3x3 convolution kernel without clock gating.

- Area ≤**5,100 $\mu m2$**
- Clock period≤**1ns**

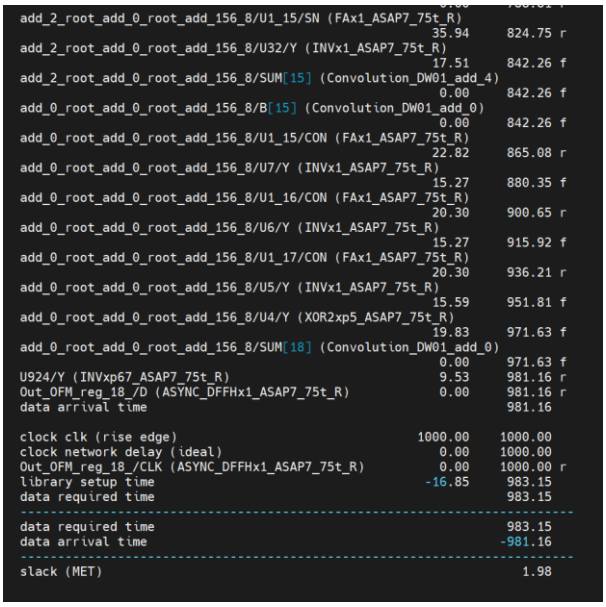
實驗流程:

1. 透過**irun TESTBED.v -define RTL -debug -notimingchecks -loadpli1 debpli:novas_pli_boot**指令進行驗證，確認功能無誤。



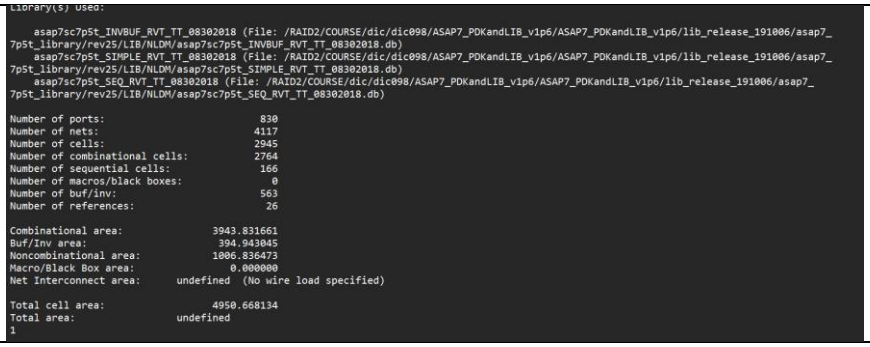
透過 nWave 查看波型是否正確

2. 透過 **dc_shell-t -f syn.tcl | tee syn.log** 進行合成



```
add_2_root_add_0_root_add_156_8/U1_15/SN (FAx1_ASAP7_75t_R)
                                                        35.94     824.75 r
add_2_root_add_0_root_add_156_8/U32/Y (INVx1_ASAP7_75t_R)
                                                        17.51     842.26 f
add_2_root_add_0_root_add_156_8/SUM[15] (Convolution_DW01_add_4)
                                                         0.00     842.26 f
add_0_root_add_0_root_add_156_8/B[15] (Convolution_DW01_add_0)
                                                         0.00     842.26 f
add_0_root_add_0_root_add_156_8/U1_15/CON (FAx1_ASAP7_75t_R)
                                                        22.82     865.08 r
add_0_root_add_0_root_add_156_8/U7/Y (INVx1_ASAP7_75t_R)
                                                        15.27     880.35 f
add_0_root_add_0_root_add_156_8/U1_16/CON (FAx1_ASAP7_75t_R)
                                                        20.30     900.65 r
add_0_root_add_0_root_add_156_8/U6/Y (INVx1_ASAP7_75t_R)
                                                        15.27     915.92 f
add_0_root_add_0_root_add_156_8/U1_17/CON (FAx1_ASAP7_75t_R)
                                                        20.30     936.21 r
add_0_root_add_0_root_add_156_8/U5/Y (INVx1_ASAP7_75t_R)
                                                        15.59     951.81 f
add_0_root_add_0_root_add_156_8/U4/Y (XOR2xp5_ASAP7_75t_R)
                                                        19.83     971.63 f
add_0_root_add_0_root_add_156_8/SUM[18] (Convolution_DW01_add_0)
                                                         0.00     971.63 f
U924/Y (INVxp67_ASAP7_75t_R)                             9.53     981.16 r
Out_OFM_reg_18_/D (ASYNC_DFFHx1_ASAP7_75t_R)             0.00     981.16 r
data arrival time                                                 981.16

clock clk (rise edge)                                 1000.00    1000.00
clock network delay (ideal)                              0.00    1000.00
Out_OFM_reg_18_/CLK (ASYNC_DFFHx1_ASAP7_75t_R)           0.00    1000.00 r
library setup time                                     -16.85     983.15
data required time                                                983.15
-------------------------------------------------------------------------
data required time                                                983.15
data arrival time                                                -981.16
-------------------------------------------------------------------------
slack (MET)                                                         1.98
```

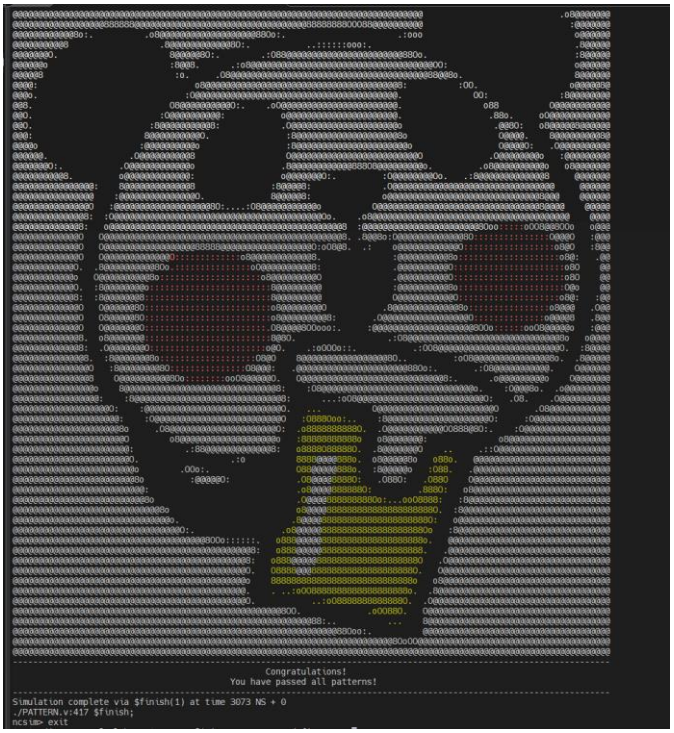
Report/timing



```
Library(s) Used:

    asap7sc7p5t_INVBUF_RVT_TT_08302018 (File: /RAID2/COURSE/dic/dic098/ASAP7_PDKandLIB_v1p6/ASAP7_PDKandLIB_v1p6/lib_release_191006/asap7_
7p5t_library/rev25/LIB/NLDM/asap7sc7p5t_INVBUF_RVT_TT_08302018.db)
    asap7sc7p5t_SIMPLE_RVT_TT_08302018 (File: /RAID2/COURSE/dic/dic098/ASAP7_PDKandLIB_v1p6/ASAP7_PDKandLIB_v1p6/lib_release_191006/asap7_
7p5t_library/rev25/LIB/NLDM/asap7sc7p5t_SIMPLE_RVT_TT_08302018.db)
    asap7sc7p5t_SEQ_RVT_TT_08302018 (File: /RAID2/COURSE/dic/dic098/ASAP7_PDKandLIB_v1p6/ASAP7_PDKandLIB_v1p6/lib_release_191006/asap7_
7p5t_library/rev25/LIB/NLDM/asap7sc7p5t_SEQ_RVT_TT_08302018.db)

Number of ports:                          830
Number of nets:                          4117
Number of cells:                         2945
Number of combinational cells:           2764
Number of sequential cells:               166
Number of macros/black boxes:               0
Number of buf/inv:                        563
Number of references:                      26

Combinational area:              3943.831661
Buf/Inv area:                     394.943045
Noncombinational area:           1006.836473
Macro/Black Box area:               0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                 4950.668134
Total area:                 undefined
1
```

Report/area

3. 進行 GATE level 驗證，透過 **irun TESTBED.v -define GATE -debug -v asap7sc7p5t_SIMPLE_RVT_TT_08302018.v asap7sc7p5t_SEQ_RVT_TT_08302018.v asap7sc7p5t_INVBUF_RVT_TT_08302018.v -nontcglitch -loadpli1 debpli:novas_pli_boot** 指令進行驗證



5-2 Power Analysis of sequential circuits

Use the pattern provided by TA to generate the waveform under gate-level simulation, and measure the power consumption of 3x3 convolution kernel using PrimePower

1. 透過PrimePower測量5-1的3*3 convolution的power

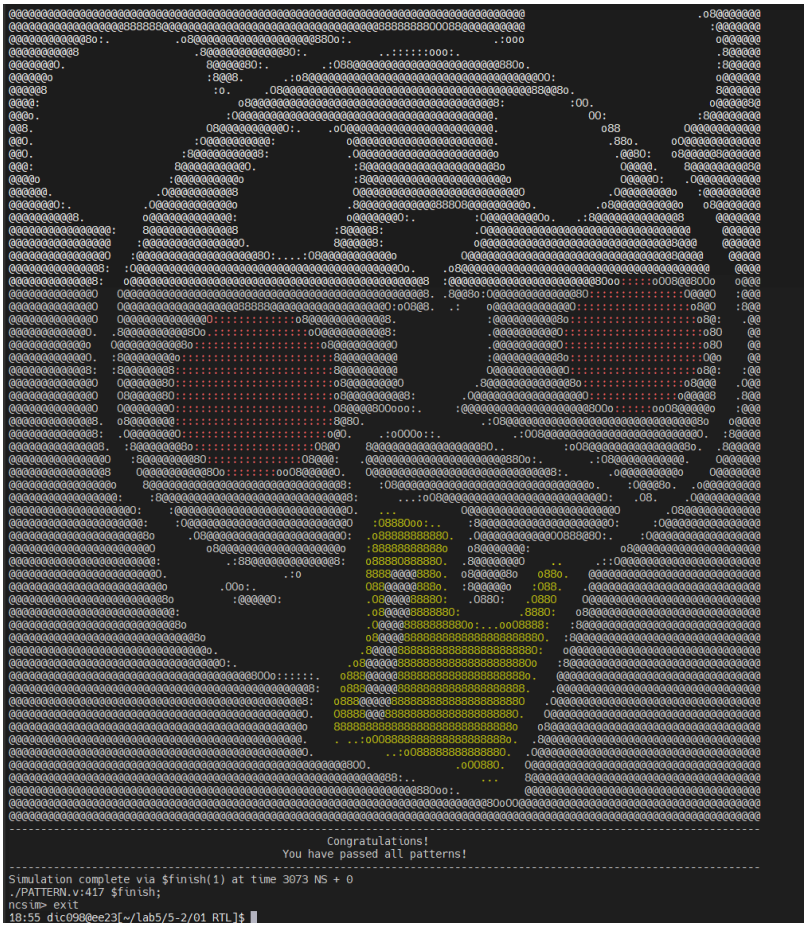
```
Date    : Mon Dec 25 18:49:30 2023
****************************************


  Attributes
  ----------
      i  -  Including register clock pin internal power
      u  -  User defined power group

                          Internal  Switching  Leakage    Total
Power Group               Power     Power      Power      Power   (     %)  Attrs
--------------------------------------------------------------------------------
clock_network               0.0000    0.0000     0.0000     0.0000 ( 0.00%)
register                 2.145e-04 1.553e-06 4.796e-08 2.161e-04 (85.76%)  i
combinational            1.427e-05 2.138e-05 2.268e-07 3.587e-05 (14.24%)
sequential                  0.0000    0.0000     0.0000     0.0000 ( 0.00%)
memory                      0.0000    0.0000     0.0000     0.0000 ( 0.00%)
io_pad                      0.0000    0.0000     0.0000     0.0000 ( 0.00%)
black_box                   0.0000    0.0000     0.0000     0.0000 ( 0.00%)

  Net Switching Power  = 2.293e-05   ( 9.10%)
  Cell Internal Power  = 2.287e-04   (90.79%)
  Cell Leakage Power   = 2.748e-07   ( 0.11%)
    Intrinsic Leakage  = 2.748e-07
    Gate Leakage       =    0.0000
                         ---------
Total Power            = 2.519e-04  (100.00%)

X Transition Power     = -1.260e-08
Glitching Power        =    0.0000

Peak Power             = 6.391e-04
Peak Time              =      1169

1
exitInformation: Defining new variable 'DESIGN'. (CMD-041)
Information: Defining new variable 'synthetic_library'. (CMD-041)

Timing updates: 1 (1 implicit, 0 explicit) (0 incremental, 1 full, 0 logical)
Noise updates: 0 (0 implicit, 0 explicit) (0 incremental, 0 full)
Maximum memory usage for this session: 1276.82 MB
CPU usage for this session: 6 seconds
Elapsed time for this session: 15 seconds
Diagnostics summary: 2 errors, 7904 warnings, 15 informationals

Thank you for using pt_shell!
18:49 dic098@ee23[~/lab5/5-2]$
```

2. **Power reduction using a data-driven clock gating technique**

Based on the gating cell: ICGx3_ASAP7_75t_R

- Power ≤**150 μW**
- Pattern CANNOT be modified

2.1 透過**irun TESTBED.v -define RTL -debug -notimingchecks -loadpli1 debpli:novas_pli_boot**指令進行驗證，確認功能無誤。



2.2 透過**dc_shell-t -f syn.tcl | tee syn.log**進行合成

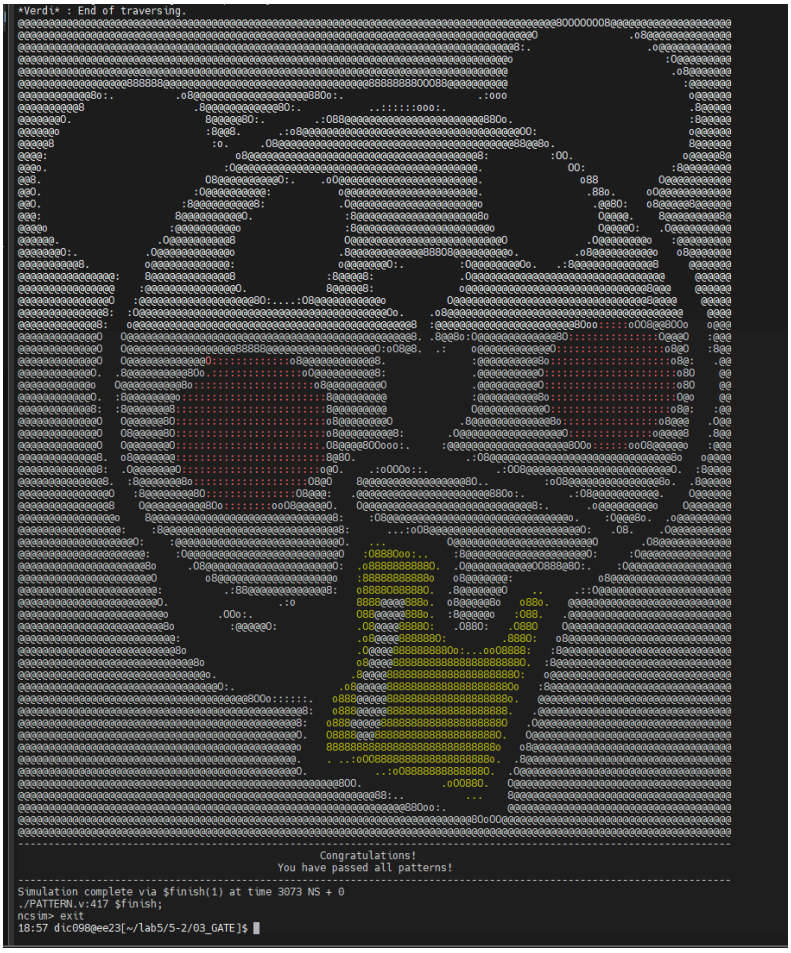
```
  add_0_root_add_0_root_add_169_8/U1_17/CON (FAx1_ASAP7_75t_R)
                                                          20.30     913.25 r
  add_0_root_add_0_root_add_169_8/U7/Y (INVx1_ASAP7_75t_R)
                                                          14.70     927.95 f
  add_0_root_add_0_root_add_169_8/U4/Y (NAND2xp33_ASAP7_75t_R)
                                                          14.04     941.99 r
  add_0_root_add_0_root_add_169_8/U5/Y (INVxp67_ASAP7_75t_R)
                                                           9.13     951.12 f
  add_0_root_add_0_root_add_169_8/SUM[19] (Convolution_DW01_add_0)
                                                           0.00     951.12 f
  U161/Y (OR2x2_ASAP7_75t_R)                              21.19     972.31 f
  U159/Y (NAND2xp5_ASAP7_75t_R)                           10.04     982.35 r
  Reg_Out_OFM_reg[19]/D (ASYNC_DFFHx1_ASAP7_75t_R)         0.00     982.35 r
  data arrival time                                                 982.35

  clock clk (rise edge)                                 1000.00    1000.00
  clock network delay (ideal)                              0.00    1000.00
  Reg_Out_OFM_reg[19]/CLK (ASYNC_DFFHx1_ASAP7_75t_R)       0.00    1000.00 r
  library setup time                                     -17.05     982.95
  data required time                                                982.95
  ---------------------------------------------------------------------------
  data required time                                                982.95
  data arrival time                                                -982.35
  ---------------------------------------------------------------------------
  slack (MET)                                                       0.60


1
```

Report/timing

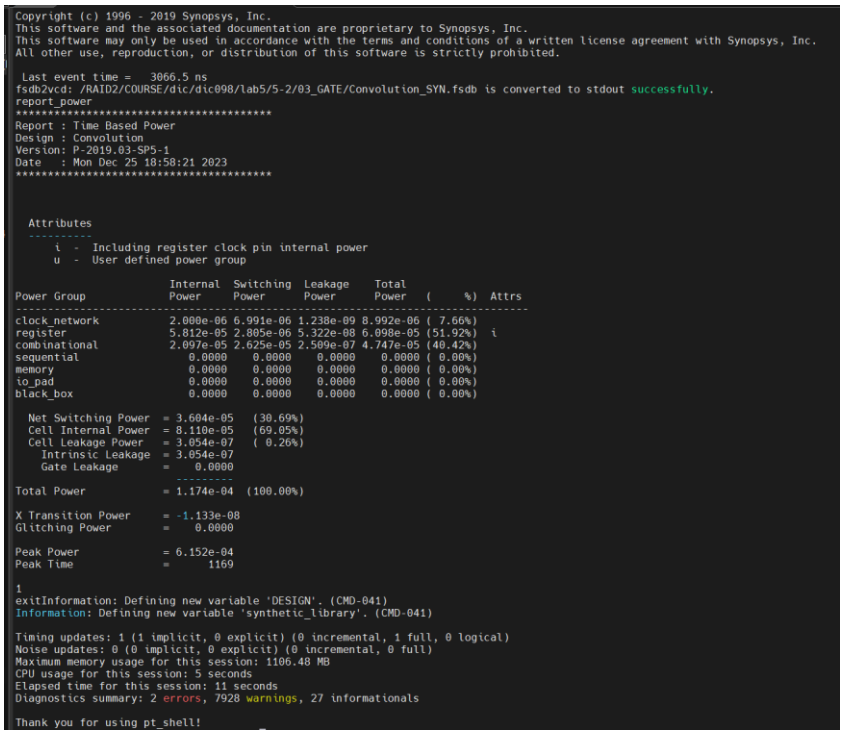
```
Library(s) Used:

    asap7sc7p5t_INVBUF_RVT_TT_08302018 (File: /RAID2/COURSE/dic/dic098/ASAP7_PDKandLIB_v1p6/ASAP7_PDKandLIB_v1p6/lib_release_191006/asap7_
7p5t_library/rev25/LIB/NLDM/asap7sc7p5t_INVBUF_RVT_TT_08302018.db)
    asap7sc7p5t_SIMPLE_RVT_TT_08302018 (File: /RAID2/COURSE/dic/dic098/ASAP7_PDKandLIB_v1p6/ASAP7_PDKandLIB_v1p6/lib_release_191006/asap7_
7p5t_library/rev25/LIB/NLDM/asap7sc7p5t_SIMPLE_RVT_TT_08302018.db)
    asap7sc7p5t_SEQ_RVT_TT_08302018 (File: /RAID2/COURSE/dic/dic098/ASAP7_PDKandLIB_v1p6/ASAP7_PDKandLIB_v1p6/lib_release_191006/asap7_
7p5t_library/rev25/LIB/NLDM/asap7sc7p5t_SEQ_RVT_TT_08302018.db)

Number of ports:                          830
Number of nets:                          4328
Number of cells:                         3153
Number of combinational cells:           2961
Number of sequential cells:               177
Number of macros/black boxes:               0
Number of buf/inv:                        646
Number of references:                      37

Combinational area:              4168.480304
Buf/Inv area:                     458.628486
Noncombinational area:           1062.357112
Macro/Black Box area:               0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                 5230.837416
Total area:                 undefined
1
```

Report/area

2.3 進行GATE level驗證，透過**irun TESTBED.v -define GATE -debug -v asap7sc7p5t_SIMPLE_RVT_TT_08302018.v asap7sc7p5t_SEQ_RVT_TT_08302018.v asap7sc7p5t_INVBUF_RVT_TT_08302018.v -nontcglitch -loadpli1 debpli:novas_pli_boot**指令進行驗證



2.4 透過PrimePower測量power



3. Compare and analyze the area and critical path

討論:

在這次的實驗中，我在三個地方加入了clock gating，分別是當input的值都等於0時，會把輸入訊號送到輸入訊號暫存的地方gate住，以及當weight_valid以及out_valid還沒等於1的時候也都會gate住，透過這樣的操作，我們在面積增加不多的情況下，power的消耗減少了一倍，因此在不需要使用到訊號時，將不會用到的訊號的clk關閉，能夠在不需要增加太多面積的情況下，大幅度的優化我們的訊號。

在critical path方面，我認為加了clock gating 僅是將電路處於閒置狀態時，將clock關閉，理論上不會影響到critical path，但是從報告的分析上來看，critical path卻改變了，我認為可能是因為我們加入的clock gating的邏輯，並沒有影響到critical path，但是卻增加了其他路徑的延遲，導致兩者的critical path不一樣。