Digital IC Design

Exercise 4
Voltage scaling

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4-1 Minimal Energy-Delay Product [60%]

- Synthesize the 2x2 convolution kernel provided by TA based on ASAP 7nm standard cells then convert the .v to .sp for voltage scaling and power measurement
  - No constraints of throughput and latency
  - Function should be correct
    - Please provide the waveform in report
  - Input patterns
    - You can generate the patterns (.vec) by high level language
    - The number of patterns should be more than 20
    - The patterns should cover the worst case delay
- Analyze and Plot EDP-voltage figure.
- Find out the minimal **energy-delay product** of the 2x2 convolution kernel by voltage scaling

4-2 Minimal Delay[40%]

- Minimize the **delay** of a 64-bit comparator.
  - Synthesize the comparator provided by TA based on ASAP 7nm standard cells then convert the .v to .sp for measurement.
  - Minimize the Delay (from a_0 first rising (0.2v) to output first rising(0.2v)) **[20%]**
    - You can based on the cell lib, asap7sc7p5t_SIMPLE_RVT.sp & asap7sc7p5t_INVBUF_RVT.sp , do the netlist ECO (add cells / change the cells).
    - The T_r and T_f of output should **less than 100ps**
    - Function should be correct
    - Input pattern is provided by TA
      - You can modify the input frequency but not values
    - Setting:
      - **Supply voltage = 0.4v**
      - **Output loading: 5f capacitance**
      - **Wire loading: 3f capacitance**
      - Add Input buffer for all input signals
    - Score
      - delay < 1.5ns[20%]
      - delay < 1.7ns [15%]
      - delay < 2.0ns[10%]
      - delay < 2.3ns [5%]
  - Measure the PPA at 0.4v and 0.7v of minimized and synthesized comparator and analyze **[20%]**

Submission of Exerice-4

- Please upload the following files on E3
  - Due day: PM 11:55 on 12/11
  - Ex-4_Student ID.tar
    - Report.pdf
    - 2x2_Conv.sp
    - Pattern_2x2_Conv.vec
    - Minimized_Comparator.sp