

Digital IC Design

Final Team Project:

**32-Row x 1-Column Digital
Computation-in-Memory Macro
for Matrix-Vector Multiplications**

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Specification of Digital CIM Macro

■ Spec:

◆ Inputs (I_1, I_2, \dots, I_{32}):

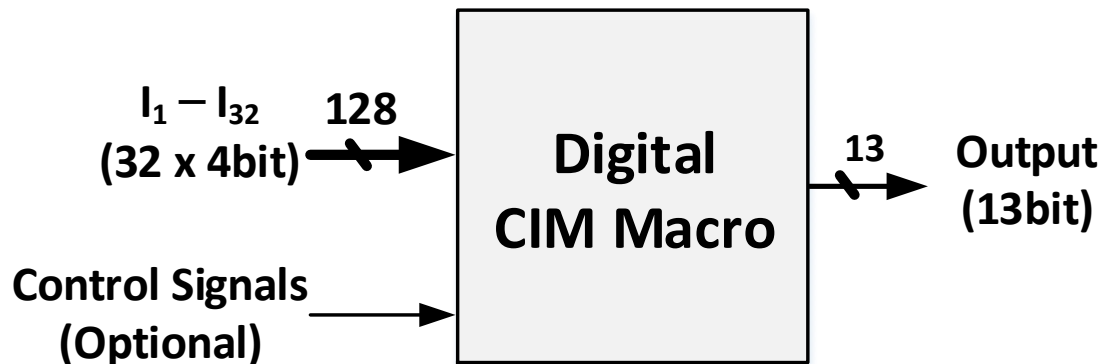
- $I_1 - I_{32}$ are 4bits
- You can add any extra control signals for your design

◆ Weights(W_1, W_2, \dots, W_{32}):

- $W_1 - W_{32}$ are 4bits
- Weights are pre-stored in latches or Flip-flops

◆ Output (O):

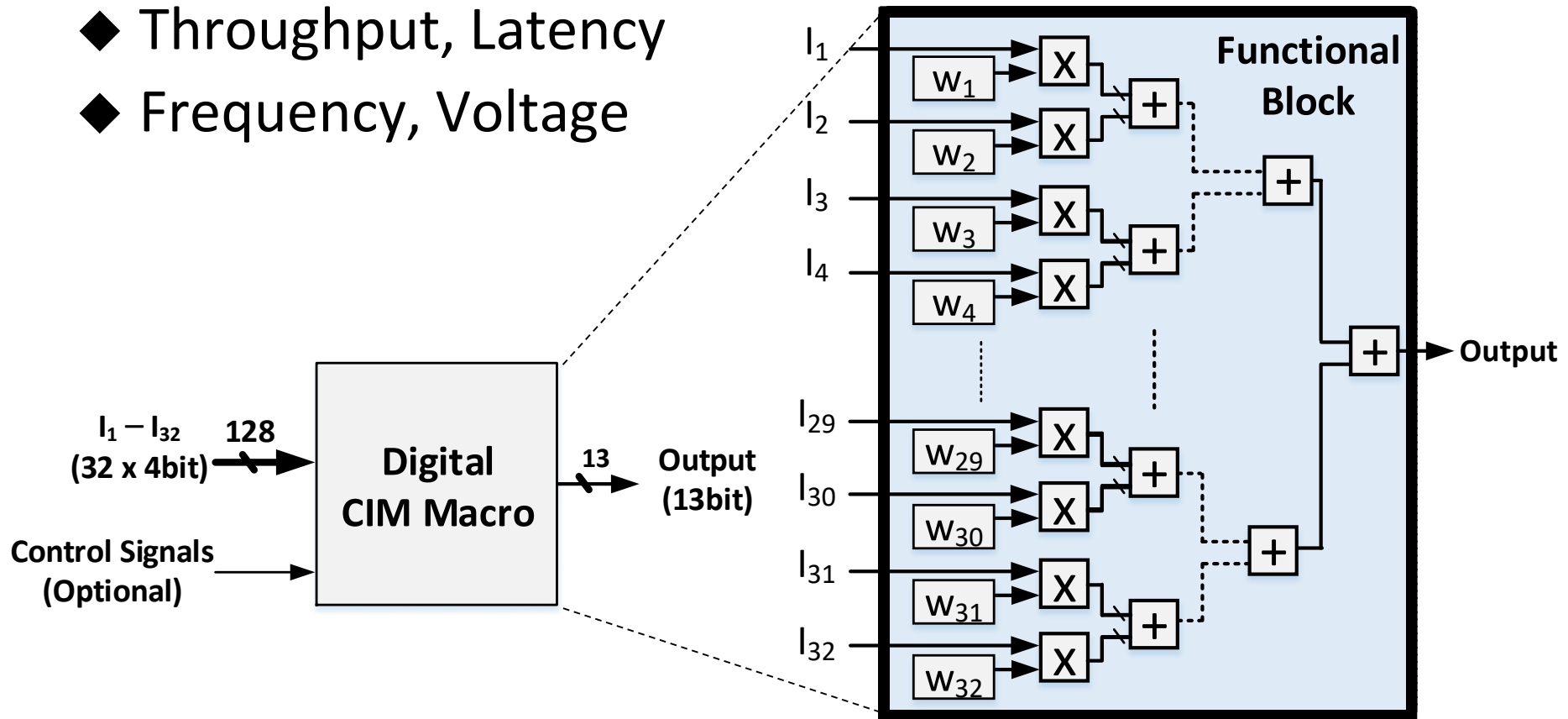
- 13 bits
- $O = (I_1 \times W_1) + (I_2 \times W_2) + \dots (I_{32} \times W_{32})$



Function of this Digital CIM Macro

■ The specification can be modified by yourself,

- ◆ Input format
- ◆ Throughput, Latency
- ◆ Frequency, Voltage

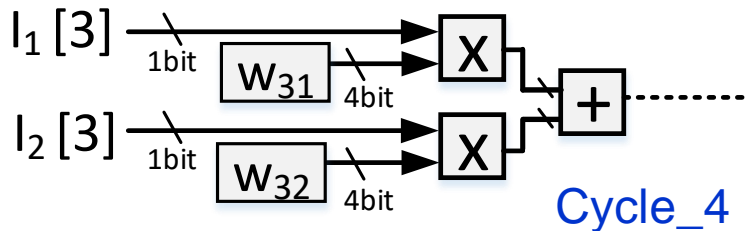
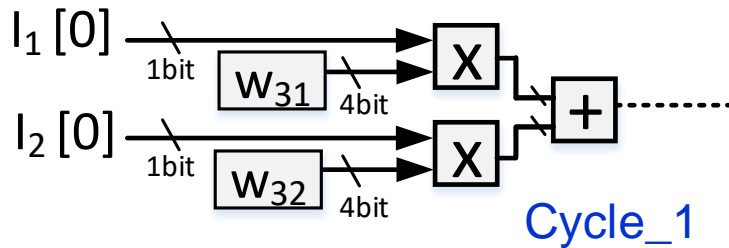


$$Output = (I_1 \times W_1) + (I_2 \times W_2) + \dots (I_{32} \times W_{32})$$

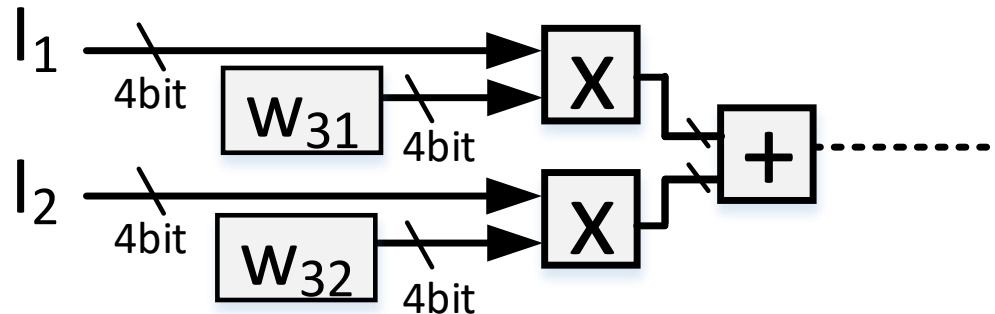
Example of Serial Input or Parallel Input

■ Example

◆ Serial input



◆ Parallel input



Goal: Achieve better PPA of digital CIM

- Measure the PPA of Digital CIM macro
 - ◆ Throughputs (GOPS)
 - ◆ Energy efficiency (TOPS/W)
 - ◆ Area efficiency (TOPS/mm²)
 - Based on number of transistor counts or equivalent NAND2 gates as the area