

數位積體電路

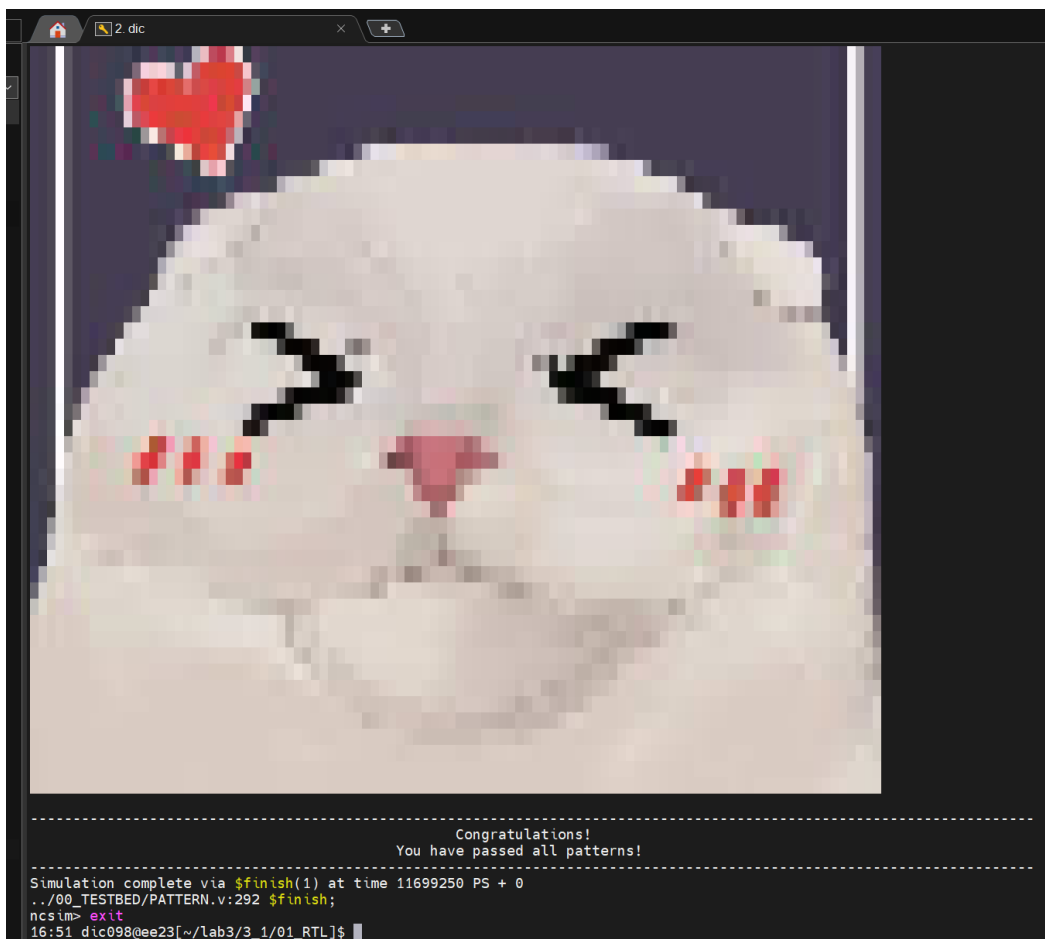
Lab3

智能系統所 312581006 張宸瑋

3-1 Implement the kernels **without** pipeline techniques.

```
16:45 dic098@ee23[~]$ cd /RAID2/COURSE/dic/dic098/lab3/3_1/01_RTL/  
16:45 dic098@ee23[~/lab3/3_1/01_RTL]$ ./01_run
```

驗證指令



確認功能正確

```
2.dic
Thank you...
16:54 dic098@ee23[~/lab3/3_1/02_SYN]$ ./01_run_Synthesis

Design Compiler Graphical
DC Ultra (TM)
DFTMAX (TM)
Power Compiler (TM)
DesignWare (R)
DC Expert (TM)
Design Vision (TM)
HDL Compiler (TM)
VHDL Compiler (TM)
DFT Compiler
Design Compiler(R)

Version T-2022.03 for linux64 - Feb 22, 2022

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Initializing...
#
# Synopsys Synthesis Scripts (Design Vision dctl mode)
#
# Set Libraries
=====
set search_path { /RAID2/COURSE/dic/dic098/ASAP7_PDKandLIB_vip6/ASAP7_PDKandLIB_vip6/lib_release_191006/asap7_7p5t_library/rev25/LIB/NLDM/ ../01_RTL }
/RAID2/COURSE/dic/dic098/ASAP7_PDKandLIB_vip6/ASAP7_PDKandLIB_vip6/lib_release_191006/asap7_7p5t_library/rev25/LIB/NLDM/ ../01_RTL
set link_library {dw_foundation.sldb }
dw_foundation.sldb
set synthetic_library {dw_foundation.sldb asap7sc7p5t_A0_RVT_TT_08302018.db asap7sc7p5t_OA_RVT_TT_08302018.db asap7sc7p5t_INBUF_RVT_TT_08302018.db asap7sc7p5t_SEO_RVT_TT_08302018.db asap7sc7p5t_SIMPLE_RVT_TT_08302018.db}
b asap7sc7p5t_SIMPLE_RVT_TT_08302018.db asap7sc7p5t_A0_RVT_TT_08302018.db asap7sc7p5t_OA_RVT_TT_08302018.db asap7sc7p5t_INBUF_RVT_TT_08302018.db asap7sc7p5t_SEO_RVT_TT_08302018.db
T_TT_08302018.db asap7sc7p5t_A0_RVT_TT_08302018.db asap7sc7p5t_OA_RVT_TT_08302018.db asap7sc7p5t_INBUF_RVT_TT_08302018.db asap7sc7p5t_SEO_RVT_TT_08302018.db
set target_library {asap7sc7p5t_INBUF_RVT_TT_08302018.db asap7sc7p5t_SIMPLE_RVT_TT_08302018.db asap7sc7p5t_SEO_RVT_TT_08302018.db }
asap7sc7p5t_INBUF_RVT_TT_08302018.db asap7sc7p5t_SIMPLE_RVT_TT_08302018.db asap7sc7p5t_SEO_RVT_TT_08302018.db
=====
# Global Parameters
=====
term by subscribing to the professional edition here: https://mobaxterm.mobatek.net
```

進行合成

```
2.dic
add_1_root_add_0_root_add_160_8/U393/Y (XNOR2x1_ASAP7_75t_R) 21.41 1289.60 r
add_1_root_add_0_root_add_160_8/SUM[31] (Convolution_without_pipeline_DW01_add_27) 22.99 1312.59 r
add_0_root_add_0_root_add_160_8/B[31] (Convolution_without_pipeline_DW01_add_20) 0.00 1312.59 r
add_0_root_add_0_root_add_160_8/U454/Y (NOR2x1p5_ASAP7_75t_R) 0.00 1312.59 r
add_0_root_add_0_root_add_160_8/U778/Y (NOR2x1p5_ASAP7_75t_R) 15.37 1327.96 f
add_0_root_add_0_root_add_160_8/U776/Y (NAND2x1p5_ASAP7_75t_R) 14.65 1342.62 r
add_0_root_add_0_root_add_160_8/U775/Y (OR2x2_ASAP7_75t_R) 10.69 1353.30 f
add_0_root_add_0_root_add_160_8/U777/Y (NAND2xp5_ASAP7_75t_R) 22.93 1376.23 f
add_0_root_add_0_root_add_160_8/U780/Y (NOR2x1_ASAP7_75t_R) 11.25 1387.48 r
add_0_root_add_0_root_add_160_8/U781/Y (NAND2x1p5_ASAP7_75t_R) 14.31 1401.79 f
add_0_root_add_0_root_add_160_8/U788/Y (AND2x2_ASAP7_75t_R) 15.35 1417.14 r
add_0_root_add_0_root_add_160_8/U476/Y (NOR2x1_ASAP7_75t_R) 21.10 1438.24 r
add_0_root_add_0_root_add_160_8/U774/Y (XOR2xp5_ASAP7_75t_R) 9.00 1447.25 f
add_0_root_add_0_root_add_160_8/SUM[33] (Convolution_without_pipeline_DW01_add_20) 19.08 1466.33 f
U30031/Y (NAND2xp5_ASAP7_75t_R) 0.00 1466.33 f
Out_0FM_reg_33 /D (ASYNCDFFHx1_ASAP7_75t_R) 11.37 1477.69 r
data arrival time 0.00 1477.69 r
clock clk (rise edge) 1500.00 1500.00
clock network delay (ideal) 0.00 1500.00
Out_0FM_reg_33 /CLK (ASYNCDFFHx1_ASAP7_75t_R) 0.00 1500.00 r
library setup time -22.04 1477.96
data required time 1477.96
data required time 1477.96
data arrival time -1477.69
slack (MET) 0.26

1
exit

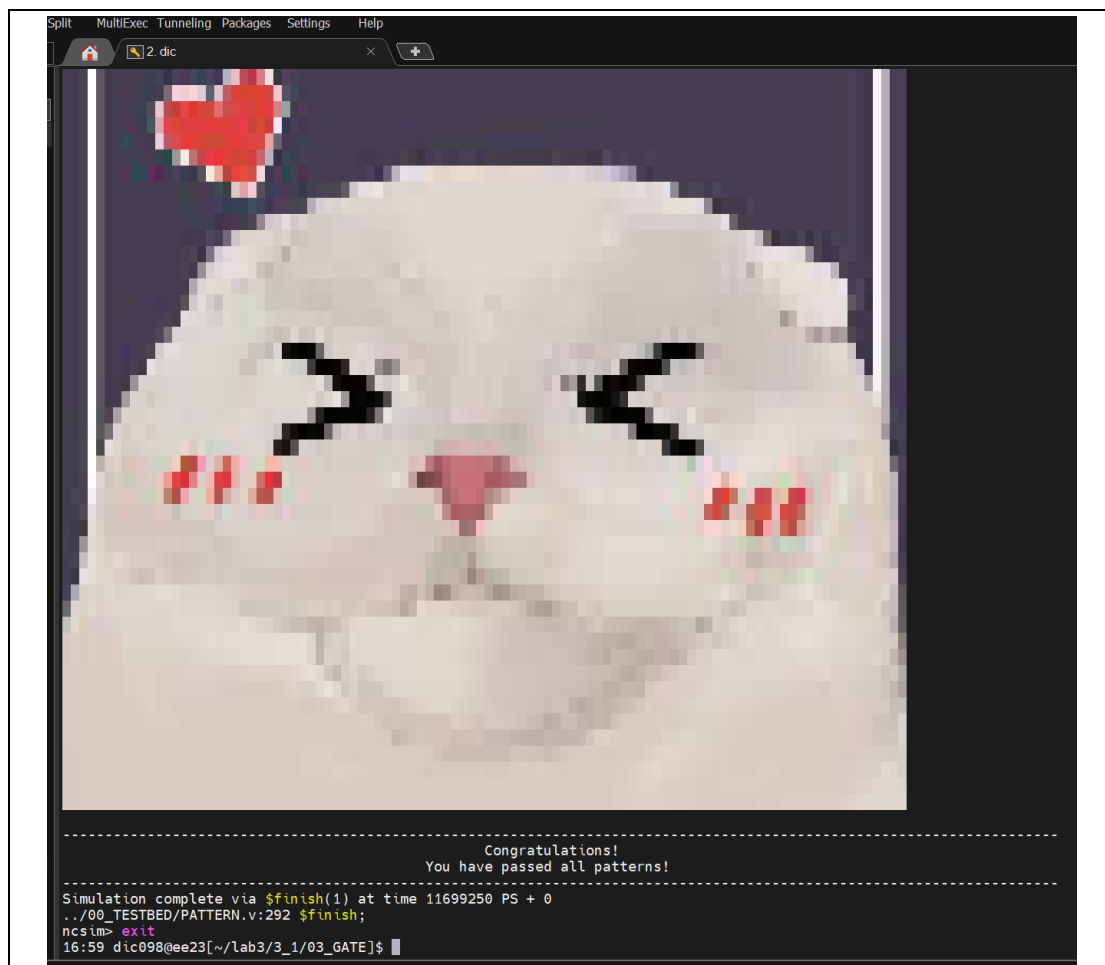
Memory usage for this session 300 Mbytes.
Memory usage for this session including child processes 300 Mbytes.
CPU usage for this session 113 seconds ( 0.03 hours ).
Elapsed time for this session 118 seconds ( 0.03 hours ).

Thank you...
16:57 dic098@ee23[~/lab3/3_1/02_SYN]$
```

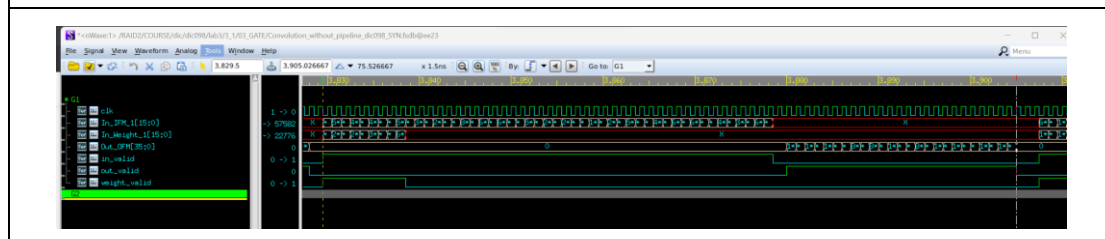
確認合成結果是否正確

```
Split MultiExec Tunneling Packages Settings Help
2 dic
16:58 dic098@ee23[~/lab3/3_1/03_GATE]$ chmod 777 09_clean_up
16:59 dic098@ee23[~/lab3/3_1/03_GATE]$ ./09_clean_up
16:59 dic098@ee23[~/lab3/3_1/03_GATE]$ ./01_run_Gate
irun(64): 15.20-s084: (c) Copyright 1995-2020 Cadence Design Systems, Inc.
file: ../00_TESTBED/TESTBED.v
module worklib.PATTERN:v
  errors: 0, warnings: 0
module worklib.Convolution_without_pipeline:v
  errors: 0, warnings: 0
module worklib.Convolution_without_pipeline_DW_div_uns_7:v
  errors: 0, warnings: 0
module worklib.Convolution_without_pipeline_DW01_add_52:v
  errors: 0, warnings: 0
module worklib.Convolution_without_pipeline_DW01_add_51:v
  errors: 0, warnings: 0
module worklib.Convolution_without_pipeline_DW_mult_uns_41:v
  errors: 0, warnings: 0
module worklib.Convolution_without_pipeline_DW_mult_uns_40:v
  errors: 0, warnings: 0
module worklib.Convolution_without_pipeline_DW_mult_uns_39:v
  errors: 0, warnings: 0
module worklib.Convolution_without_pipeline_DW01_add_49:v
  errors: 0, warnings: 0
module worklib.Convolution_without_pipeline_DW01_add_48:v
  errors: 0, warnings: 0
module worklib.Convolution_without_pipeline_DW_mult_uns_36:v
  errors: 0, warnings: 0
module worklib.Convolution_without_pipeline_DW_mult_uns_28:v
  errors: 0, warnings: 0
module worklib.Convolution_without_pipeline_DW_mult_uns_27:v
  errors: 0, warnings: 0
module worklib.Convolution_without_pipeline_DW01_add_29:v
  errors: 0, warnings: 0
module worklib.Convolution_without_pipeline_DW01_add_27:v
  errors: 0, warnings: 0
module worklib.Convolution_without_pipeline_DW01_add_20:v
  errors: 0, warnings: 0
module worklib.Convolution_without_pipeline_DW01_add_24:v
  errors: 0, warnings: 0
module worklib.Convolution_without_pipeline_DW_mult_uns_11:v
  errors: 0, warnings: 0
module worklib.Convolution_without_pipeline_DW_mult_uns_13:v
  errors: 0, warnings: 0
module worklib.Convolution_without_pipeline_DW_mult_uns_12:v
  errors: 0, warnings: 0
module worklib.TESTBED:v
  errors: 0, warnings: 0
file: asap7sc7p5t_SEQ_RWT_TT_08302018.v
module worklib.ASTNC_DFFHX1_ASAP7_75t_R:v
  errors: 0, warnings: 0
module worklib.DFFHONx1_ASAP7_75t_R:v
  errors: 0, warnings: 0
module worklib.DFFHONx2_ASAP7_75t_R:v
  errors: 0, warnings: 0
module worklib.DFFHONx3_ASAP7_75t_R:v
```

Gate level 驗證



確認 Gate level 功能正確



Measure Operation time

```

檔案 編輯 檢視
asap7sc7p5t_INVBUFF_RVT_TT_08302018 (File: /RAID2/COURSE/dic/dic098/ASAP7_PDKandLIB_v1p6/ASAP7_PDKandLIB_v1p6/lib_release_191006/asap7_7p5t_library/rev25/LIB/NLDM/asap7sc7p5t_INVBUFF_RVT_TT_08302018.db)
asap7sc7p5t_SIMPLE_RVT_TT_08302018 (File: /RAID2/COURSE/dic/dic098/ASAP7_PDKandLIB_v1p6/ASAP7_PDKandLIB_v1p6/lib_release_191006/asap7_7p5t_library/rev25/LIB/NLDM/asap7sc7p5t_SIMPLE_RVT_TT_08302018.db)
asap7sc7p5t_SEQ_RVT_TT_08302018 (File: /RAID2/COURSE/dic/dic098/ASAP7_PDKandLIB_v1p6/ASAP7_PDKandLIB_v1p6/lib_release_191006/asap7_7p5t_library/rev25/LIB/NLDM/asap7sc7p5t_SEQ_RVT_TT_08302018.db)

Number of ports:          1539
Number of nets:           30738
Number of cells:          28170
Number of combinational cells: 27125
Number of sequential cells: 1027
Number of macros/black boxes: 0
Number of buf/inv:        2674
Number of references:      57

Combinational area:       32807.332846
Buf/Inv area:             1996.643542
Noncombinational area:    6229.042520
Macro/Black Box area:     0.000000
Net Interconnect area:    undefined (No wire load specified)

Total cell area:          39036.375366
Total area:               undefined
1

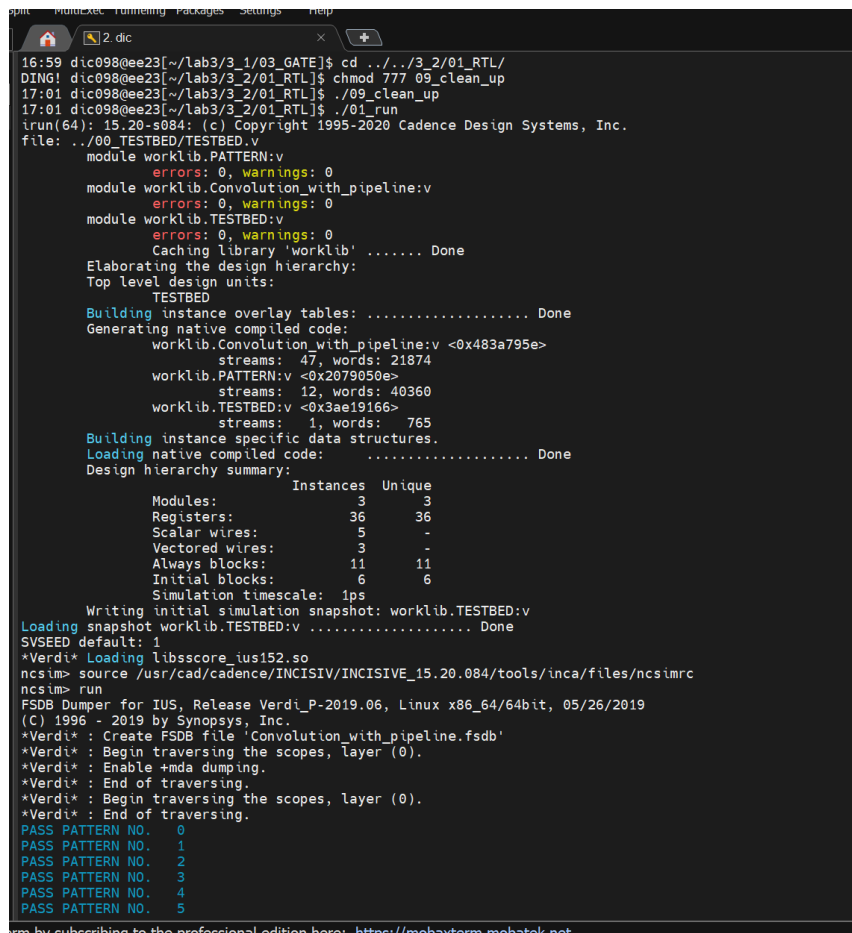
```

Area

Throughput(OPS) = Operations / operating time =

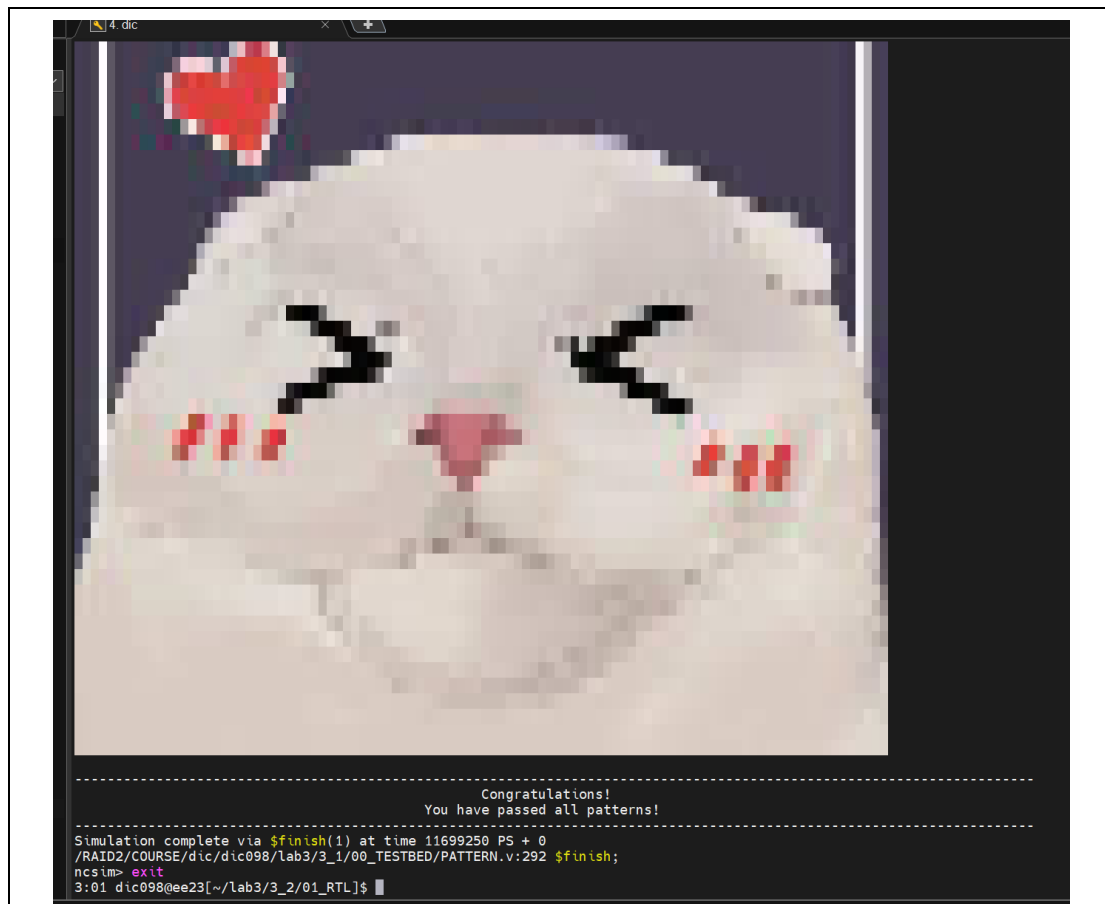
$$\frac{450}{(3905.02-3829.5)*1.5*10^{-9}} = 3.972457627 \text{ (GOPS)}$$

3-2 Implement the kernels **with** pipeline techniques.



```
16:59 dic098@ee23[~/lab3/3 1/03_GATE]$ cd ../../3 2/01_RTL/
DING! dic098@ee23[~/lab3/3 2/01_RTL]$ chmod 777 09_clean_up
17:01 dic098@ee23[~/lab3/3 2/01_RTL]$ ./09_clean_up
17:01 dic098@ee23[~/lab3/3 2/01_RTL]$ ./01_run
irun(64): 15.20-s084: (c) Copyright 1995-2020 Cadence Design Systems, Inc.
file: ../00_TESTBED/TESTBED.v
module worklib.PATTERN:v
  errors: 0, warnings: 0
module worklib.Convolution_with_pipeline:v
  errors: 0, warnings: 0
module worklib.TESTBED:v
  errors: 0, warnings: 0
  Caching library 'worklib' ..... Done
Elaborating the design hierarchy:
Top level design units:
  TESTBED
Building instance overlay tables: ..... Done
Generating native compiled code:
  worklib.Convolution_with_pipeline:v <0x483a795e>
    streams: 47, words: 21874
  worklib.PATTERN:v <0x2079050e>
    streams: 12, words: 40360
  worklib.TESTBED:v <0x3ae19166>
    streams: 1, words: 765
Building instance specific data structures.
Loading native compiled code: ..... Done
Design hierarchy summary:
  Instances Unique
  Modules:      3      3
  Registers:    36     36
  Scalar wires: 5      -
  Vectored wires: 3      -
  Always blocks: 11     11
  Initial blocks: 6      6
  Simulation timescale: 1ps
Writing initial simulation snapshot: worklib.TESTBED:v
Loading snapshot worklib.TESTBED:v ..... Done
SVSEED default: 1
*Verdi* Loading libsscore_ius152.so
ncsim> source /usr/cad/cadence/INCISIV/INCISIVE_15.20.084/tools/inca/files/ncsimrc
ncsim> run
FSDB Dumper for IUS, Release Verdi_P-2019.06, Linux x86_64/64bit, 05/26/2019
(C) 1996 - 2019 by Synopsys, Inc.
*Verdi* : Create FSDB file 'Convolution_with_pipeline.fsdb'
*Verdi* : Begin traversing the scopes, Layer (0).
*Verdi* : Enable +mda dumping.
*Verdi* : End of traversing.
*Verdi* : Begin traversing the scopes, layer (0).
*Verdi* : End of traversing.
PASS PATTERN NO. 0
PASS PATTERN NO. 1
PASS PATTERN NO. 2
PASS PATTERN NO. 3
PASS PATTERN NO. 4
PASS PATTERN NO. 5
```

驗證指令



確認功能是否正確

```
gdb MultiExec Tunneling Packages Settings Help X server
[2] dc
17:03 dic098@ee23[~/lab3/3_2/02_SYN] 01_run_Synthesis
01_run_Synthesis: Command not found.
17:04 dic098@ee23[~/lab3/3_2/02_SYN] ./01_run_Synthesis

Design Compiler Graphical
DC Ultra (TM)
DFTMAX (TM)
Power Compiler (TM)
DesignWare (S)
DC Expert (TM)
Design Vision (TM)
HDL Compiler (TM)
VHDL Compiler (TM)
DFT Compiler
Design Compiler(R)

Version T-2022.03 for Linux64 - Feb 22, 2022

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Inclusivity and Diversity" (Refer to article 000036315 at
https://solvnetplus.synopsys.com)

Initializing...
#####
# Synopsys Synthesis Scripts (Design Vision dctl mode)
#
#####
# Set Libraries
#####
set search_path ( /RAID2/COURSE/dic/dic098/ASAP7_POKandLIB_vip6/ASAP7_POKandLIB_vip6/lib_release_191006/asap7_7p5t_library/rev25/LIB/NLDM/ ../01_RTL )
set link_library { dw_foundation.slib }
dw_foundation.slib -
set synthetic_library { dw_foundation.slib asap7c7p5t_AD_RVT_TT_08302018.db asap7c7p5t_OA_RVT_TT_08302018.db asap7c7p5t_INVBUF_RVT_TT_08302018.db asap7c7p5t_SEQ_RVT_TT_08302018
b asap7c7p5t_SIMPLE_RVT_TT_08302018.db asap7c7p5t_AD_RVT_TT_08302018.db asap7c7p5t_OA_RVT_TT_08302018.db asap7c7p5t_INVBUF_RVT_TT_08302018.db asap7c7p5t_SEQ_RVT_TT_08302018.db asap7c7p5t_SIMPLE
_TT_08302018.db asap7c7p5t_AD_RVT_TT_08302018.db asap7c7p5t_OA_RVT_TT_08302018.db asap7c7p5t_INVBUF_RVT_TT_08302018.db asap7c7p5t_SEQ_RVT_TT_08302018.db asap7c7p5t_SIMPLE
set target_library { asap7c7p5t_INVBUF_RVT_TT_08302018.db asap7c7p5t_SIMPLE_RVT_TT_08302018.db asap7c7p5t_SEQ_RVT_TT_08302018.db }
asap7c7p5t_INVBUF_RVT_TT_08302018.db asap7c7p5t_SIMPLE_RVT_TT_08302018.db asap7c7p5t_SEQ_RVT_TT_08302018.db
#####
# Global Parameters
#####
```

進行合成

```
2. dic
mult_165/U1403/Y (HB1xp67_ASAP7_75t_R) 31.69 286.34 f
mult_165/U1786/Y (OR2x2_ASAP7_75t_R) 26.53 312.87 f
mult_165/U2104/Y (OR2x2_ASAP7_75t_R) 22.66 335.53 f
mult_165/U1474/Y (NAND2x1p5_ASAP7_75t_R) 13.25 348.78 r
mult_165/U553/SN (FAX1_ASAP7_75t_R) 65.33 414.12 f
mult_165/U549/CON (FAX1_ASAP7_75t_R) 41.78 455.89 r
mult_165/U549/SN (FAX1_ASAP7_75t_R) 25.32 481.22 f
mult_165/U548/SN (FAX1_ASAP7_75t_R) 44.74 525.95 f
mult_165/U2166/Y (INVx1_ASAP7_75t_R) 17.15 543.11 r
mult_165/U1593/Y (NOR2x1_ASAP7_75t_R) 14.24 557.34 f
mult_165/U2265/Y (NOR2x1_ASAP7_75t_R) 12.25 569.59 r
mult_165/U286/Y (NOR2x1_ASAP7_75t_R) 10.17 579.76 f
mult_165/U1869/Y (OR2x2_ASAP7_75t_R) 23.58 603.35 f
mult_165/U1466/Y (NAND2x1p5_ASAP7_75t_R) 10.23 613.58 r
mult_165/U1454/Y (NOR2x1p5_ASAP7_75t_R) 12.25 625.83 f
mult_165/U1437/Y (INVx3_ASAP7_75t_R) 10.85 636.68 r
mult_165/U1298/Y (NAND2x2_ASAP7_75t_R) 9.49 646.17 f
mult_165/U1438/Y (NAND2x2_ASAP7_75t_R) 19.00 665.17 r
mult_165/U1972/Y (AND2x2_ASAP7_75t_R) 26.10 691.27 r
mult_165/U1473/Y (NOR2x1p5_ASAP7_75t_R) 9.28 700.55 f
mult_165/U1981/Y (OR2x2_ASAP7_75t_R) 23.88 724.42 f
mult_165/U1525/Y (NAND2x1p5_ASAP7_75t_R) 8.85 733.27 r
mult_165/U1856/Y (XNOR2xp5_ASAP7_75t_R) 13.17 746.44 f
mult_165/product[22] (Convolution_with_pipeline_DW_mult_uns_9) 0.00 746.44 f
U16020/Y (INVx1_ASAP7_75t_R) 8.71 755.15 r
U23755/Y (NAND2xp5_ASAP7_75t_R) 8.01 763.17 f
U23758/Y (NAND2xp5_ASAP7_75t_R) 18.88 782.04 r
pipeline_out_reg_0_22_/D (ASYNC_DFFHx1_ASAP7_75t_R) 0.00 782.04 r
data arrival time 782.04
clock clk (rise edge) 800.00 800.00
clock network delay (ideal) 0.00 800.00
pipeline_out_reg_0_22_/CLK (ASYNC_DFFHx1_ASAP7_75t_R) 0.00 800.00 r
library setup time -17.93 782.07
data required time 782.07
-----
data required time 782.07
data arrival time -782.04
-----
slack (MET) 0.02

1
exit


Memory usage for this session 308 Mbytes.
Memory usage for this session including child processes 308 Mbytes.
CPU usage for this session 75 seconds ( 0.02 hours ).
Elapsed time for this session 79 seconds ( 0.02 hours ).

Thank you...
17:05 dic098@eee23[~/lab3/3_2/02_SYN]$
```

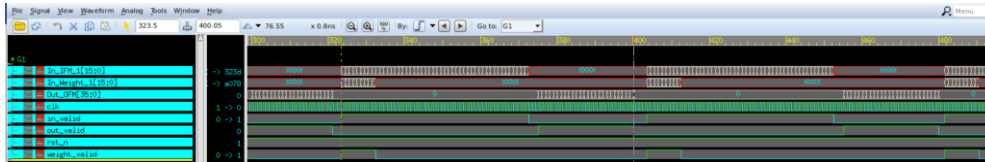
確認合成結果是否正確


```
Split MultiExec Tunneling Packages Settings Help
2 dic
17:05 dic098@ee23[~/lab3/3_2/02_SYN]$ cd ../03_GATE/
17:06 dic098@ee23[~/lab3/3_2/03_GATE]$ chmod 777 09_clean_up
17:06 dic098@ee23[~/lab3/3_2/03_GATE]$ ./09_clean_up
17:06 dic098@ee23[~/lab3/3_2/03_GATE]$ ./01_run_Gate
irun(64): 15.20-8084: (c) Copyright 1995-2020 Cadence Design Systems, Inc.
file: ../00_TESTBED/TESTBED.v
  module worklib.PATTERN:v
    errors: 0, warnings: 0
  module worklib.Convolution_with_pipeline:v
    errors: 0, warnings: 0
  module worklib.Convolution_with_pipeline_DW01_add_42:v
    errors: 0, warnings: 0
  module worklib.Convolution_with_pipeline_DW01_add_32:v
    errors: 0, warnings: 0
  module worklib.Convolution_with_pipeline_DW01_add_25:v
    errors: 0, warnings: 0
  module worklib.Convolution_with_pipeline_DW01_add_20:v
    errors: 0, warnings: 0
  module worklib.Convolution_with_pipeline_DW01_add_19:v
    errors: 0, warnings: 0
  module worklib.Convolution_with_pipeline_DW01_add_21:v
    errors: 0, warnings: 0
  module worklib.Convolution_with_pipeline_DW01_add_22:v
    errors: 0, warnings: 0
  module worklib.Convolution_with_pipeline_DW01_add_24:v
    errors: 0, warnings: 0
  module worklib.Convolution_with_pipeline_DW_mult_uns_9:v
    errors: 0, warnings: 0
  module worklib.Convolution_with_pipeline_DW_mult_uns_17:v
    errors: 0, warnings: 0
  module worklib.Convolution_with_pipeline_DW_mult_uns_16:v
    errors: 0, warnings: 0
  module worklib.Convolution_with_pipeline_DW_mult_uns_15:v
    errors: 0, warnings: 0
  module worklib.Convolution_with_pipeline_DW_mult_uns_14:v
    errors: 0, warnings: 0
  module worklib.Convolution_with_pipeline_DW_mult_uns_13:v
    errors: 0, warnings: 0
  module worklib.Convolution_with_pipeline_DW_mult_uns_12:v
    errors: 0, warnings: 0
  module worklib.Convolution_with_pipeline_DW_mult_uns_11:v
    errors: 0, warnings: 0
  module worklib.Convolution_with_pipeline_DW_mult_uns_10:v
    errors: 0, warnings: 0
  module worklib.Convolution_with_pipeline_DW_div_uns_0:v
    errors: 0, warnings: 0
  module worklib.TESTBED:v
    errors: 0, warnings: 0
file: asap7sc7p5t_SEQ_RV7_TT_08302018.v
  module worklib.ASYNC_DFFHx1_ASAP7_75t_R:v
    errors: 0, warnings: 0
  module worklib.DFFHQNx1_ASAP7_75t_R:v
    errors: 0, warnings: 0
  module worklib.DFFHQNx2_ASAP7_75t_R:v
    errors: 0, warnings: 0
```

Gate level 驗證

```
Split MultiExec Tunneling Packages Settings Help
2 dic

-----
Congratulations!
You have passed all patterns!
-----
Simulation complete via $finish(1) at time 11849250 PS + 0
/RAID2/COURSE/dic/dic098/lab3/3_1/00_TESTBED/PATTERN.v:292 $finish;
ncsim> exit
17:07 dic098@ee23[~/lab3/3_2/03_GATE]$
```

確認 Gate level 功能正確



Measure Operation time

```

檔案 編輯 檢視
asap7sc7p5t_INVBUF_RVT_TT_08302018 (File: /RAID2/COURSE/dic/dic098/ASAP7_PDKandLIB_v1p6/ASAP7_PDKandLIB_v1p6/lib_release_191006/asap7_7p5t_library/rev25/LIB/NLDM/asap7sc7p5t_INVBUF_RVT_TT_08302018.db)
asap7sc7p5t_SIMPLE_RVT_TT_08302018 (File: /RAID2/COURSE/dic/dic098/ASAP7_PDKandLIB_v1p6/ASAP7_PDKandLIB_v1p6/lib_release_191006/asap7_7p5t_library/rev25/LIB/NLDM/asap7sc7p5t_SIMPLE_RVT_TT_08302018.db)
asap7sc7p5t_SEQ_RVT_TT_08302018 (File: /RAID2/COURSE/dic/dic098/ASAP7_PDKandLIB_v1p6/ASAP7_PDKandLIB_v1p6/lib_release_191006/asap7_7p5t_library/rev25/LIB/NLDM/asap7sc7p5t_SEQ_RVT_TT_08302018.db)

Number of ports:          1539
Number of nets:           34189
Number of cells:          31789
Number of combinational cells: 30456
Number of sequential cells: 1315
Number of macros/black boxes: 0
Number of buf/inv:        3441
Number of references:      64

Combinational area:       35346.818982
Buf/Inv area:             2552.316509
Noncombinational area:    7975.843148
Macro/Black Box area:     0.000000
Net Interconnect area:    undefined (No wire load specified)

Total cell area:          43322.662130
Total area:               undefined
1

```

AREA

Throughput(OPS) = Operations / operating time =

$$\frac{450}{(400.05 - 323.05) \times 0.8 \times 10^{-9}} = 7.30519481 \text{ (GOPS)}$$