數位積體電路

Lab2

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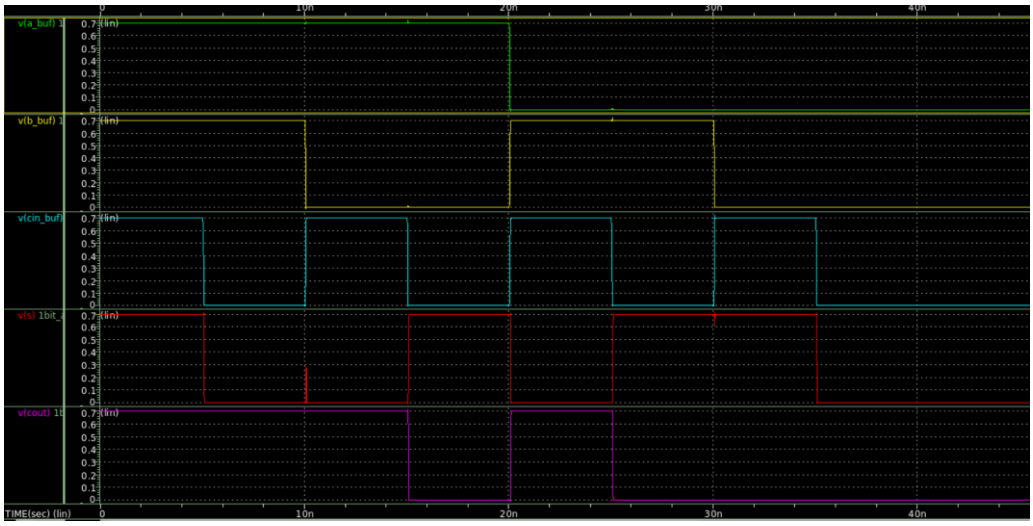
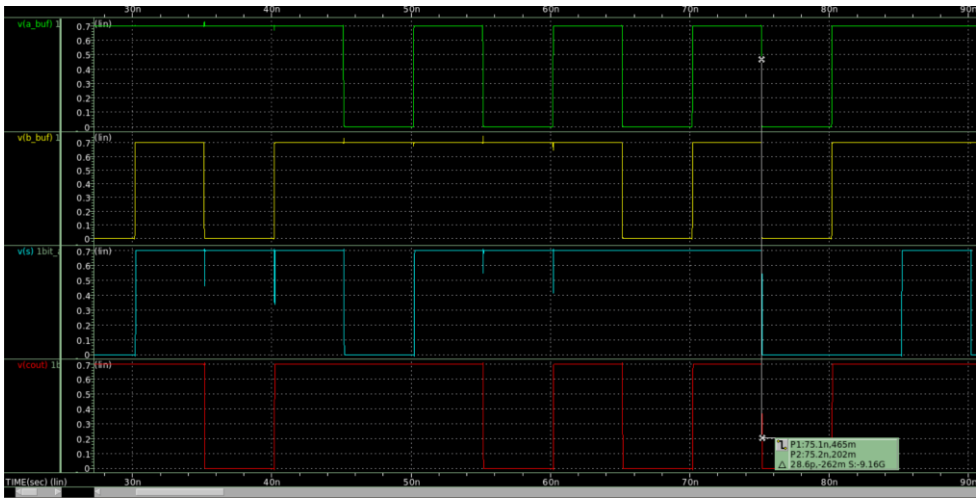
2-1: 1-bit Full Adder standard cell



波形圖(測資: pattern_adder_1_bits.vec

```
****** transient analysis tnom=  25.000 temp=  25.000 ******
power= 208.1137n  from=   0.             to=  80.0000n

          ***** job concluded
```

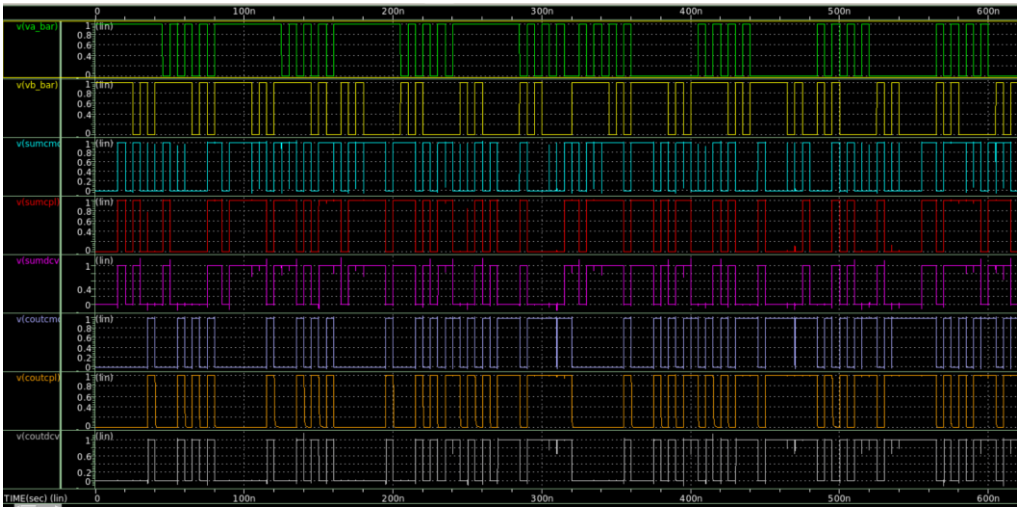
Power



Worst case delay: 28.6p

透過 worst case delay 的分析，我們可以找出 critical path 為 A 或 B 到 S 的路徑

2-2: Different logic family of 1-bit Full Adders



波形圖

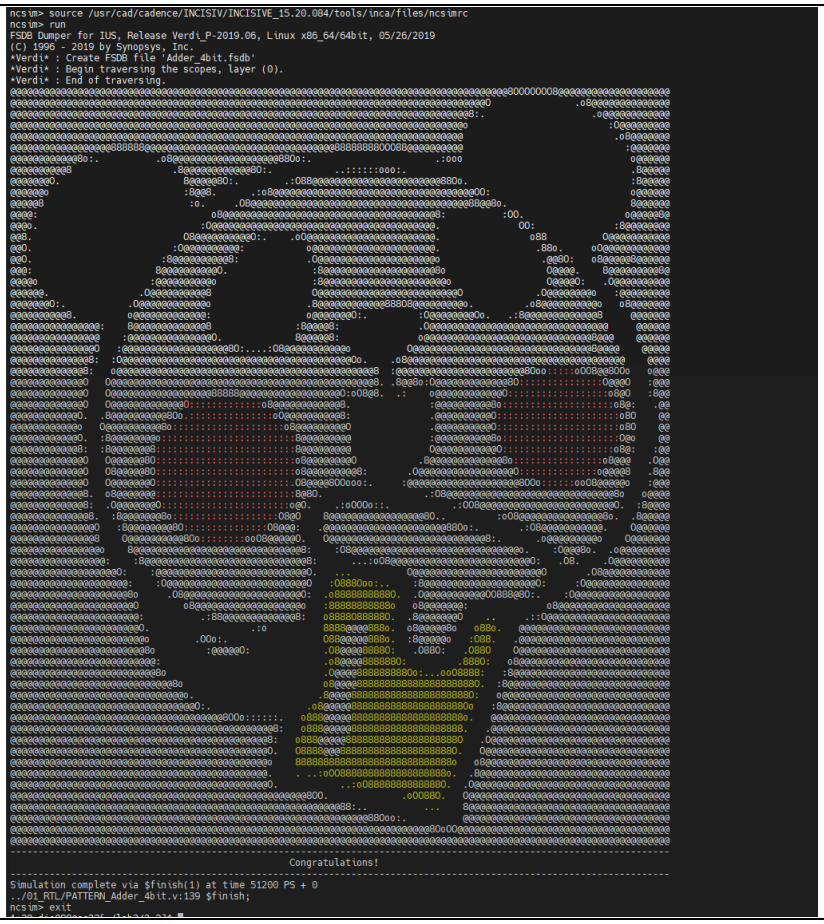
Power	
CMOS power	****** transient analysis tnom= 25.000 temp= 25.000 ****** power= 311.4605n from= 0. to= 40.0000n
CPL-type power	****** transient analysis tnom= 25.000 temp= 25.000 ****** fa_1bit= 3.5648u from= 0. to= 40.0000n
DCVS-type power	****** transient analysis tnom= 25.000 temp= 25.000 ****** power= 565.7391n from= 0. to= 40.0000n
PPA measurment	
CMOS	****** Circuit Statistics ****** # nodes = 30 # elements = 58 # resistors = 0 # capacitors = 2 # inductors = 0 # mutual_inds = 0 # vccs = 0 # vcvs = 0 # cccs = 0 # ccvs = 0 # volt_srcs = 1 # curr_srcs = 0 # diodes = 0 # bjts = 0 # jfets = 0 # mosfets = 52 # U elements = 0 # T elements = 0 # W elements = 0 # B elements = 0 # S elements = 0 # P elements = 0 # va device = 0 # vector_srcs = 3 # N elements = 0
CPL-type	****** Circuit Statistics ****** # nodes = 28 # elements = 50 # resistors = 0 # capacitors = 2 # inductors = 0 # mutual_inds = 0 # vccs = 0 # vcvs = 0 # cccs = 0 # ccvs = 0 # volt_srcs = 1 # curr_srcs = 0 # diodes = 0 # bjts = 0 # jfets = 0 # mosfets = 44 # U elements = 0 # T elements = 0 # W elements = 0 # B elements = 0 # S elements = 0 # P elements = 0 # va device = 0 # vector_srcs = 3 # N elements = 0

DCVS-type	****** Circuit Statistics ****** # nodes = 31 # elements = 56 # resistors = 0 # capacitors = 2 # inductors = 0 # mutual_inds = 0 # vccs = 0 # vcvs = 0 # cccs = 0 # ccvs = 0 # volt_srcs = 1 # curr_srcs = 0 # diodes = 0 # bjts = 0 # jfets = 0 # mosfets = 50 # U elements = 0 # T elements = 0 # W elements = 0 # B elements = 0 # S elements = 0 # P elements = 0 # va device = 0 # vector_srcs = 3 # N elements = 0

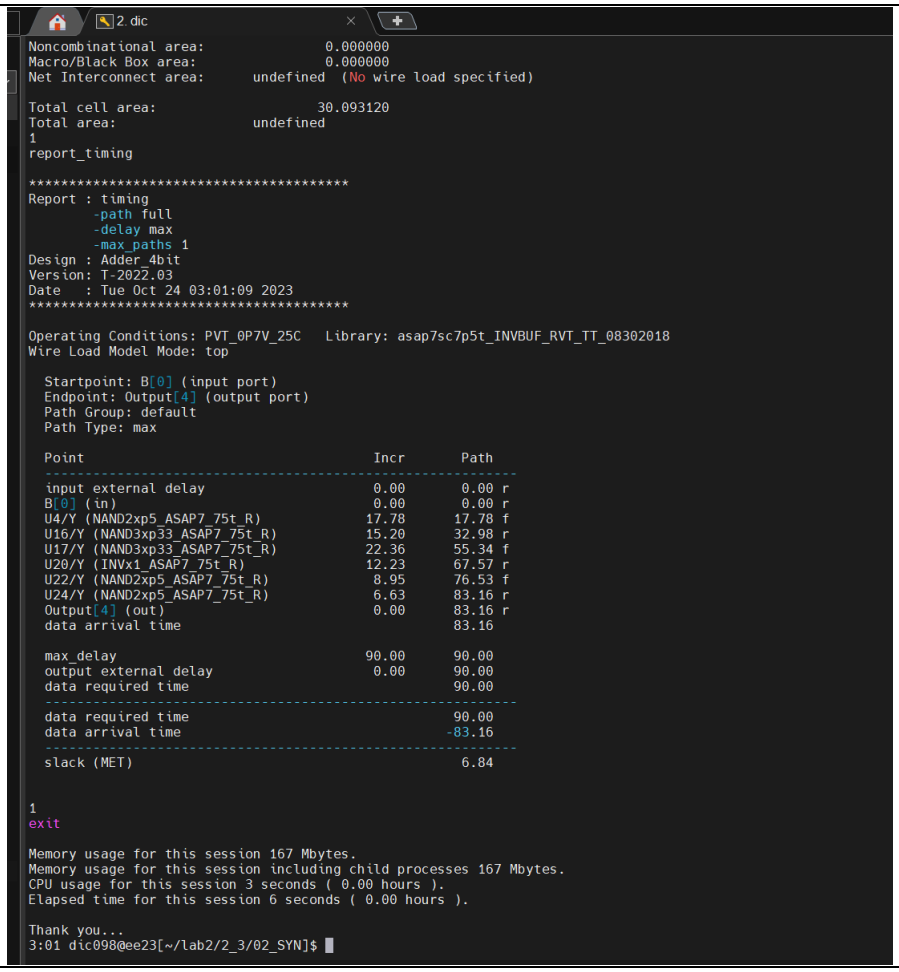
分析:

在這裡我們可以看到 CMOS 的電晶體數量理論上會是比較多的，而實際測試結果也是如此，而消耗功率也較少，而 CPL 的電晶體數量也是三者最少的，但功率消耗有點多，推測可能是因為某些情況消耗一下恆定電流，而 DCVS 的電晶體數量居中，消耗的功率也是。

2-3: Design a 4-Bit Adder

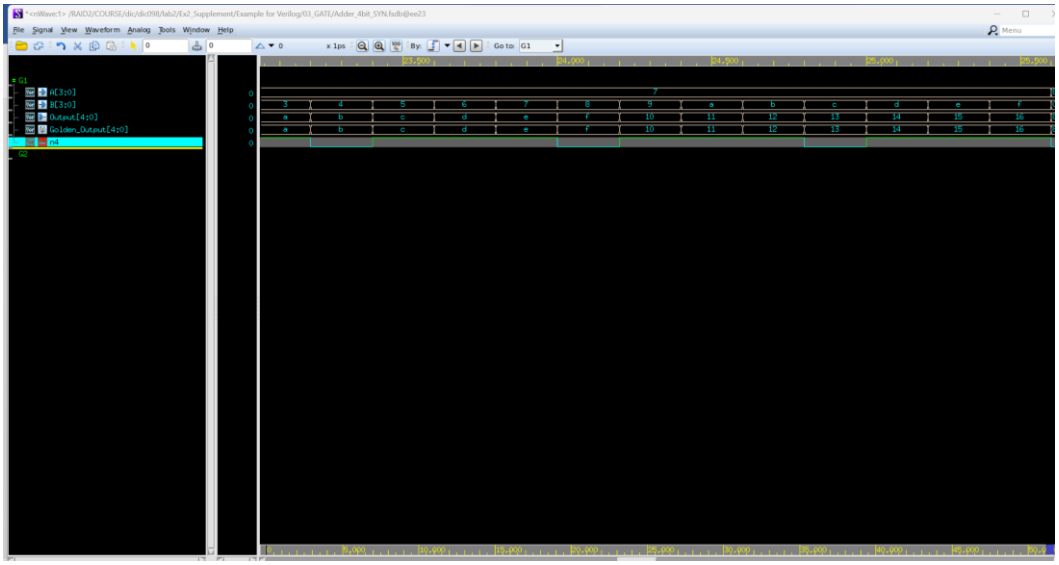


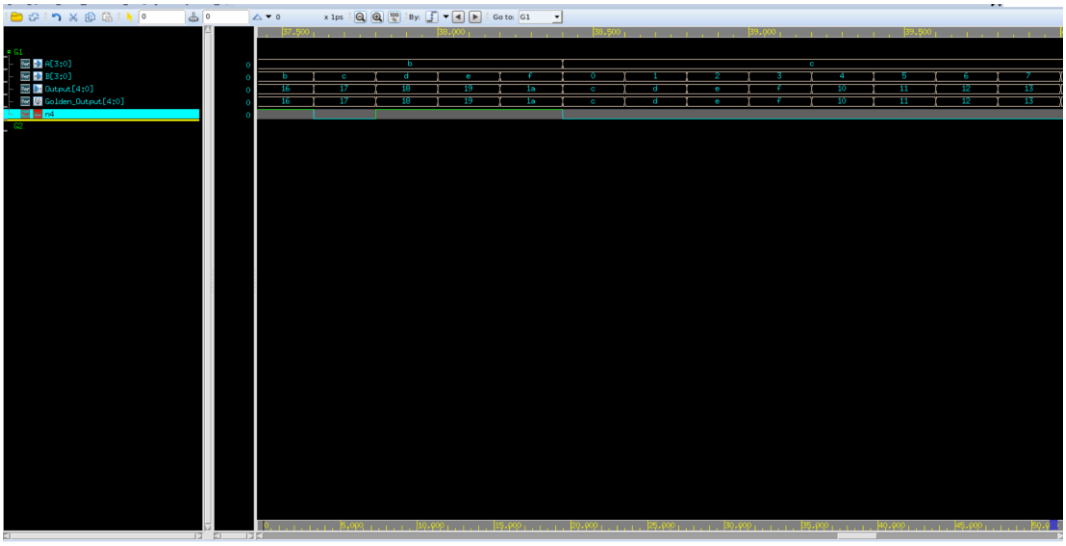
一開始先透過 01_run 中的指令，來驗證 behavior level，成功後會跑出如上的結果圖



確定功能沒問題之後，透過dc_shell-t -f syn.tcl | tee syn.log，這句command做合成，轉換成gate level

接著進行gate level的驗證





接著透過nWave，再次確認功能無誤

```
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : Adder_4bit
Version: T-2022.03
Date   : Tue Oct 24 03:01:09 2023
****************************************

Operating Conditions: PVT_0P7V_25C   Library: asap7sc7p5t_INVBUF_RVT_TT_08302018
Wire Load Model Mode: top

  Startpoint: B[0] (input port)
  Endpoint: Output[4] (output port)
  Path Group: default
  Path Type: max

  Point                                    Incr       Path
  -----------------------------------------------------------
  input external delay                     0.00       0.00 r
  B[0] (in)                                0.00       0.00 r
  U4/Y (NAND2xp5_ASAP7_75t_R)             17.78      17.78 f
  U16/Y (NAND3xp33_ASAP7_75t_R)           15.20      32.98 r
  U17/Y (NAND3xp33_ASAP7_75t_R)           22.36      55.34 f
  U20/Y (INVx1_ASAP7_75t_R)               12.23      67.57 r
  U22/Y (NAND2xp5_ASAP7_75t_R)             8.95      76.53 f
  U24/Y (NAND2xp5_ASAP7_75t_R)             6.63      83.16 r
  Output[4] (out)                          0.00      83.16 r
  data arrival time                                  83.16

  max_delay                               90.00      90.00
  output external delay                    0.00      90.00
  data required time                                 90.00
  -----------------------------------------------------------
  data required time                                 90.00
  data arrival time                                 -83.16
  -----------------------------------------------------------
  slack (MET)                                         6.84
```

critical path是b[0]的rising 到Output[4]的rising，總共花費83.16ps。

2-4: CMOS Logics for 4-Bit Adder

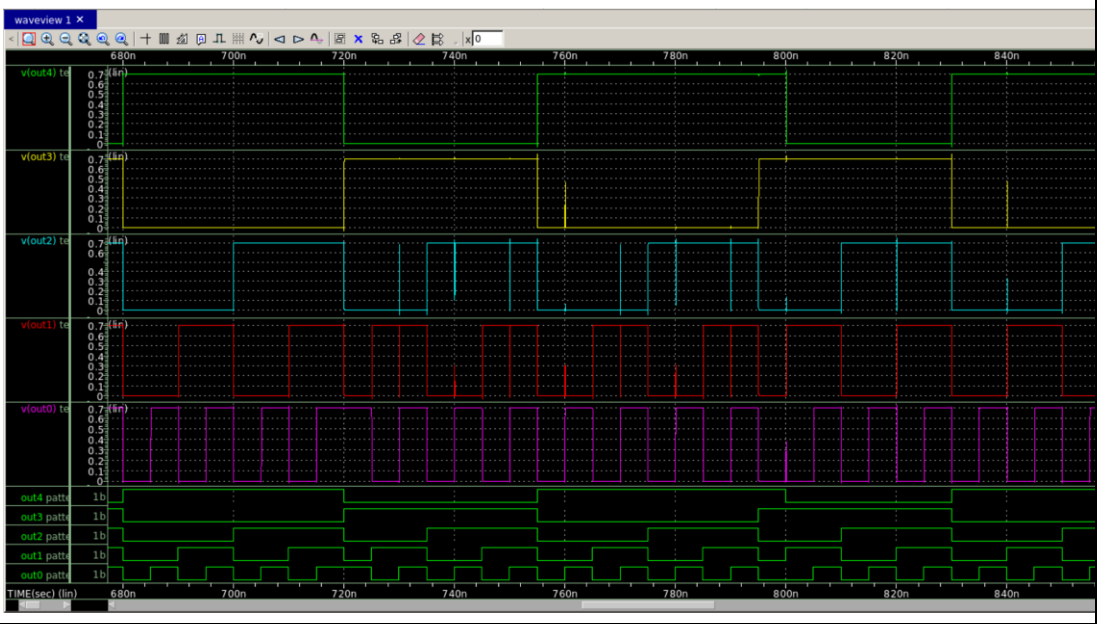
```
////////////////////////////////////////////////////////////
// Created by: Synopsys DC Expert(TM) in wire load mode
// Version   : T-2022.03
// Date      : Tue Oct 24 03:01:09 2023
////////////////////////////////////////////////////////////


module Adder_4bit ( A, B, Output );
  input [3:0] A;
  input [3:0] B;
  output [4:0] Output;
  wire   n4, n5, n6, n7, n8, n9, n10, n11, n12, n13, n14, n15, n16, n17, n18,
         n19, n20;

  XOR2xp5_ASAP7_75t_R U3 ( .A(A[0]), .B(B[0]), .Y(Output[0]) );
  NAND2xp5_ASAP7_75t_R U4 ( .A(B[0]), .B(A[0]), .Y(n11) );
  FAx1_ASAP7_75t_R U5 ( .A(B[1]), .B(A[1]), .CI(n11), .SN(Output[1]) );
  XNOR2xp5_ASAP7_75t_R U6 ( .A(B[2]), .B(A[2]), .Y(n6) );
  NAND2xp5_ASAP7_75t_R U7 ( .A(B[1]), .B(A[1]), .Y(n9) );
  NAND2xp5_ASAP7_75t_R U8 ( .A(n11), .B(n9), .Y(n4) );
  OR2x2_ASAP7_75t_R U9 ( .A(B[1]), .B(A[1]), .Y(n7) );
  NAND2xp5_ASAP7_75t_R U10 ( .A(n4), .B(n7), .Y(n5) );
  XOR2xp5_ASAP7_75t_R U11 ( .A(n6), .B(n5), .Y(Output[2]) );
  INVx1_ASAP7_75t_R U12 ( .A(n7), .Y(n8) );
  NAND2xp5_ASAP7_75t_R U13 ( .A(B[2]), .B(A[2]), .Y(n10) );
  NAND2xp5_ASAP7_75t_R U14 ( .A(n8), .B(n10), .Y(n14) );
  OR2x2_ASAP7_75t_R U15 ( .A(B[2]), .B(A[2]), .Y(n13) );
  NAND3xp33_ASAP7_75t_R U16 ( .A(n11), .B(n10), .C(n9), .Y(n12) );
  NAND3xp33_ASAP7_75t_R U17 ( .A(n14), .B(n13), .C(n12), .Y(n16) );
  XNOR2xp5_ASAP7_75t_R U18 ( .A(B[3]), .B(A[3]), .Y(n15) );
  XOR2xp5_ASAP7_75t_R U19 ( .A(n16), .B(n15), .Y(Output[3]) );
  INVx1_ASAP7_75t_R U20 ( .A(n16), .Y(n18) );
  OR2x2_ASAP7_75t_R U21 ( .A(B[3]), .B(A[3]), .Y(n17) );
  NAND2xp5_ASAP7_75t_R U22 ( .A(n18), .B(n17), .Y(n20) );
  NAND2xp5_ASAP7_75t_R U23 ( .A(B[3]), .B(A[3]), .Y(n19) );
  NAND2xp5_ASAP7_75t_R U24 ( .A(n20), .B(n19), .Y(Output[4]) );
endmodule
```

verilog gate level netlist

```
.SUBCKT Adder_4bit VSS VDD  A[3] A[2] A[1] A[0] B[3] B[2] B[1] B[0] Output[4] Output[3] Output[2] Output[1] Output[0]
XU3 A[0] B[0] VDD VSS Output[0] XOR2xp5_ASAP7_75t_R
XU4 B[0] A[0] VDD VSS n11 NAND2xp5_ASAP7_75t_R
XU5 B[1] A[1] n11 A0  Output[1] VDD VSS FAx1_ASAP7_75t_R
XU6 B[2] A[2] VDD VSS n6 XNOR2xp5_ASAP7_75t_R
XU7 B[1] A[1] VDD VSS n9 NAND2xp5_ASAP7_75t_R
XU8 n11 n9 VDD VSS n4 NAND2xp5_ASAP7_75t_R
XU9 B[1] A[1] VDD VSS n7 OR2x2_ASAP7_75t_R
XU10 n4 n7 VDD VSS n5 NAND2xp5_ASAP7_75t_R
XU11 n6 n5 VDD VSS Output[2] XOR2xp5_ASAP7_75t_R
XU12 n7 VDD VSS n8  INVx1_ASAP7_75t_R
XU13 B[2] A[2] VDD VSS n10 NAND2xp5_ASAP7_75t_R
XU14 n8 n10 VDD VSS n14 NAND2xp5_ASAP7_75t_R
XU15 B[2] A[2] VDD VSS n13 OR2x2_ASAP7_75t_R
XU16 n11 n10 n9 VDD VSS n12 NAND3xp33_ASAP7_75t_R
XU17 n14 n13 n12 VDD VSS n16 NAND3xp33_ASAP7_75t_R
XU18 B[3] A[3] VDD VSS n15 XNOR2xp5_ASAP7_75t_R
XU19 n16 n15 VDD VSS Output[3] XOR2xp5_ASAP7_75t_R
XU20 n16 VDD VSS n18  INVx1_ASAP7_75t_R
XU21 B[3] A[3] VDD VSS n17 OR2x2_ASAP7_75t_R
XU22 n18 n17 VDD VSS n20 NAND2xp5_ASAP7_75t_R
XU23 B[3] A[3] VDD VSS n19 NAND2xp5_ASAP7_75t_R
XU24 n20 n19 VDD VSS Output[4] NAND2xp5_ASAP7_75t_R
.ENDS
```

HSPICE netlist

透過助教提供的檔案，將 verilog gate level netlist 轉換成 HSPICE netlist（這裡用助教提供的.py 檔案好像不行，跟用的 cdl 腳位對不太起來，我是後來自己手動改才成功的。



透過 waveview 查看波行書出是否正確

```
****** transient analysis tnom=  25.000 temp=  25.000 ******
power=    2.1529n  from=    0.             to=    1.5000u

          ***** job concluded
```

Power

Worst case delay
當 a=0010、b=0100 -> a=1100、b=0111 會有 Worst case delay: 98.43ps
討論: 這裡透過窮舉所有可能 pattern 的方式，來找出 Worst case delay，首先透過 worst_case_delay.py 檔案，生成所有可能的.vec 檔案，以及對應的.sp 檔案，並且全部編譯，透過 python 來將所有測量出來的 delay 值比較，找出最大值。 分析: 這裡因為我用的是窮舉法，所以生成的資料非常多，也非常耗時，但我相信一定有可以減少 pattern 生成的方式，希望之後有空可以回來思考一下。