Digital IC Design

Exercise 5
Clock gating

Professor Po-Tsang Huang

International College of Semiconductor Technology
National Yang Ming Chiao Tung University

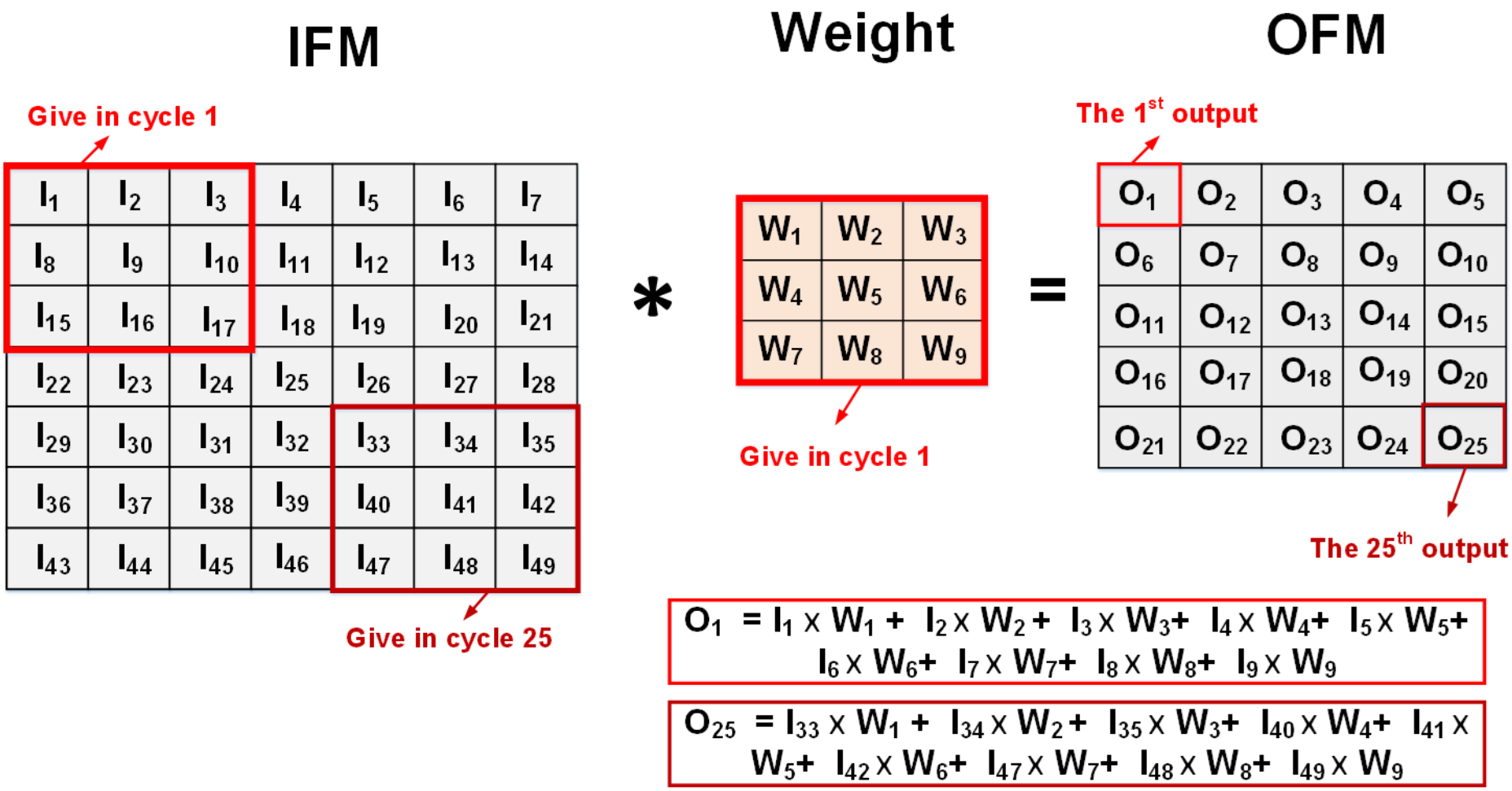
Sequential circuits

- Implement a 3x3 convolution kernel without clock gating. [20%]
  - Area $\leq$ **5,100** $\boldsymbol{\mu m^2}$
  - Clock period $\leq$ **1 ns**
- Use the .tcl file provided by TA to synthesis your designs.
  - You can only modify the search path & clock period
- Verify the design in gate level simulation using the pattern provided by TA.

Power Analysis of sequential circuits

- Use the pattern provided by TA to generate the waveform under gate-level simulation, and measure the power consumption of 3x3 convolution kernel using PrimePower [20%]
  - **Power reduction using a data-driven clock gating technique**[40%]
    - Based on the gating cell: ICGx3_ASAP7_75t_R
    - Power $\leq$ **150** $\boldsymbol{\mu W}$
    - Pattern CANNOT be modified
- Compare and analyze the area and critical path[20%]
  - w/o and w/ clock gating
  - The synthesis clock periods should be **1 ns**

Introduction of 3x3 Convolution

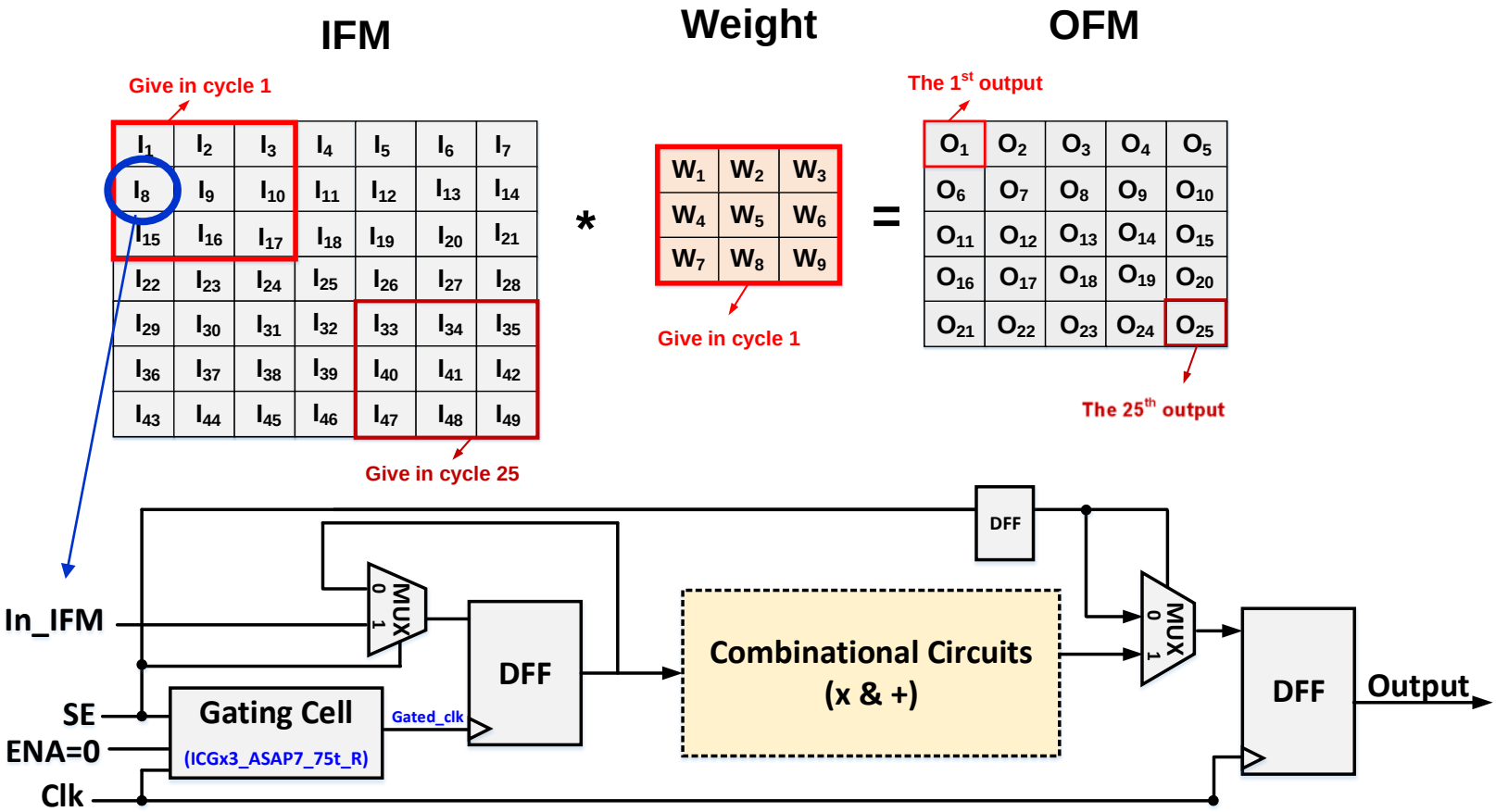


$$O_1 = I_1 \times W_1 + I_2 \times W_2 + I_3 \times W_3 + I_4 \times W_4 + I_5 \times W_5 + I_6 \times W_6 + I_7 \times W_7 + I_8 \times W_8 + I_9 \times W_9$$

$$O_{25} = I_{33} \times W_1 + I_{34} \times W_2 + I_{35} \times W_3 + I_{40} \times W_4 + I_{41} \times W_5 + I_{42} \times W_6 + I_{47} \times W_7 + I_{48} \times W_8 + I_{49} \times W_9$$

Clock gating

- Example
  - In_IFM = 0 → SE = 0
  - In_IFM != 0 → SE = 1



Specifications for 3x3 convolution kernel

- Signals:

Input signals	Bit width	Description
clk	1	Positive edge trigger clock
rst_n	1	Asynchronous active-low reset.
in_valid	1	When High, **In_IFMs** are valid
Weight_valid	1	When High, **In_Weights** are valid
In_IFM_1-9	8	Input feature map **(9 signals), give in 25 cycles**
In_Weight_1-9	8	Weights **(9 signals), give in one cycle**
Output signals	Bit width	Description
Out_valid	1	High when out is valid, then Patten will check Out_OFM. **(It should maintain 25 cycles)**
Out_OFM	21	The answers of the 3x3 convolution. **(It should maintain 25 cycles)**

- Settings:
  - **In_IFMs & In_Weights should be received by registers.**
  - **The output ports should be set as registers.**

Submission of Exerice-5

- Please upload the following files
  - Due day: PM 11:55 on 12/25
  - Naming rule:
    - Ex_5_student_ID.tar(.rar / .zip)
      - 3x3_Convolution.v
      - 3x3_Convolution_clock_gating.v
      - Report.pdf