Digital IC Design

Exercise 5
Supplement

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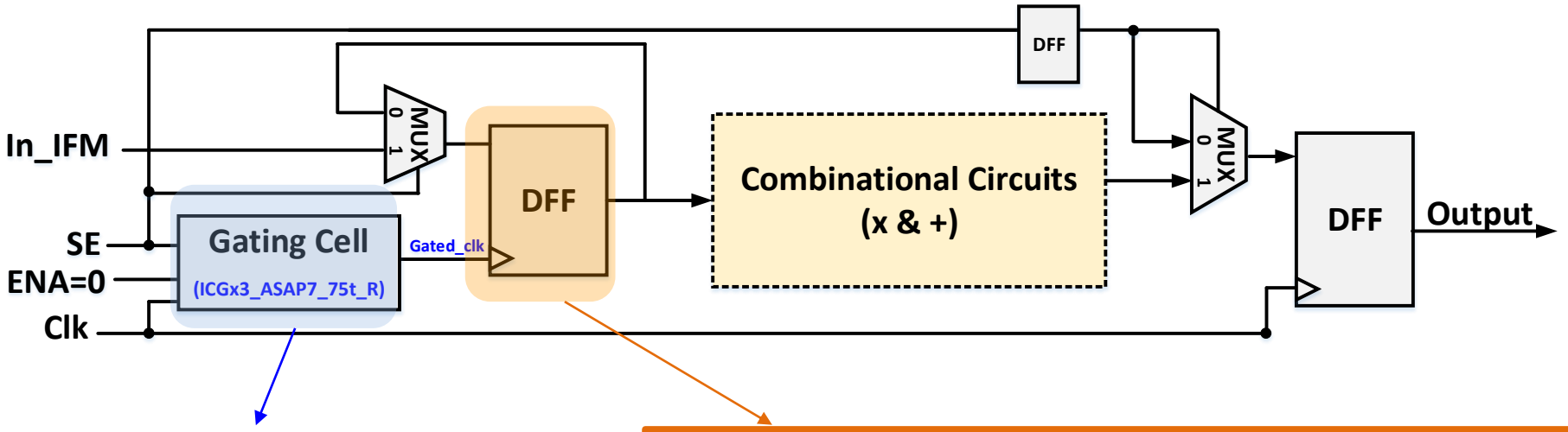
Clock gating

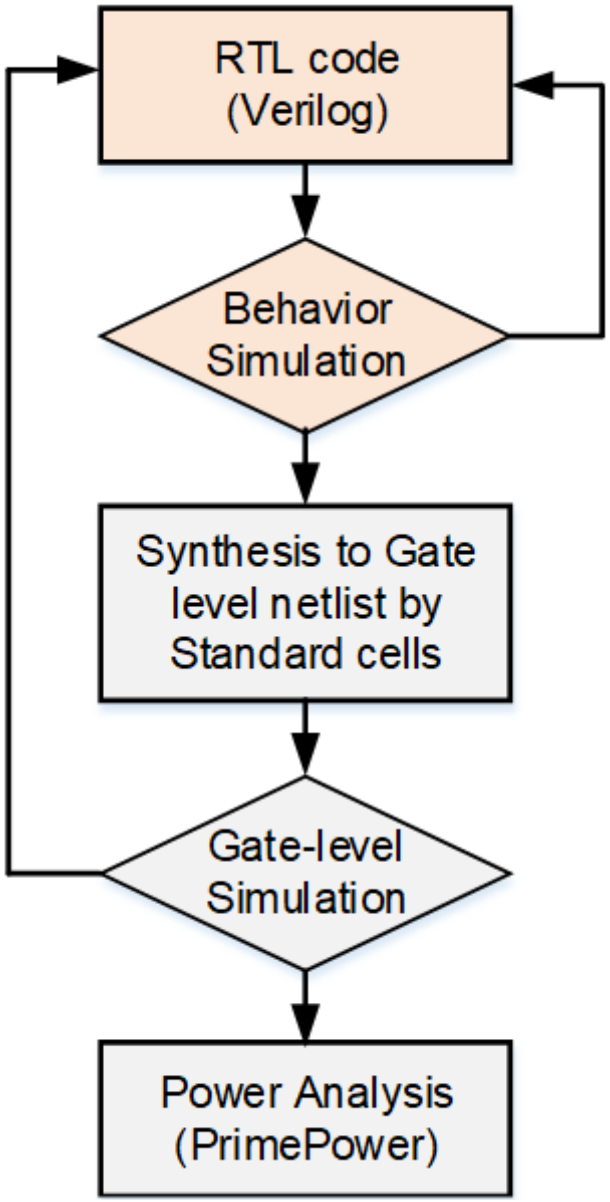
- Example code




```
// Clock Gating cells
ICGx3_ASAP7_75t_R GATED_CG_U0(
    // Input signals
    .CLK(clk),
    .ENA(0),
    .SE(Enable_1),
    // Output signals
    .GCLK(clk_gate_1)
);
```

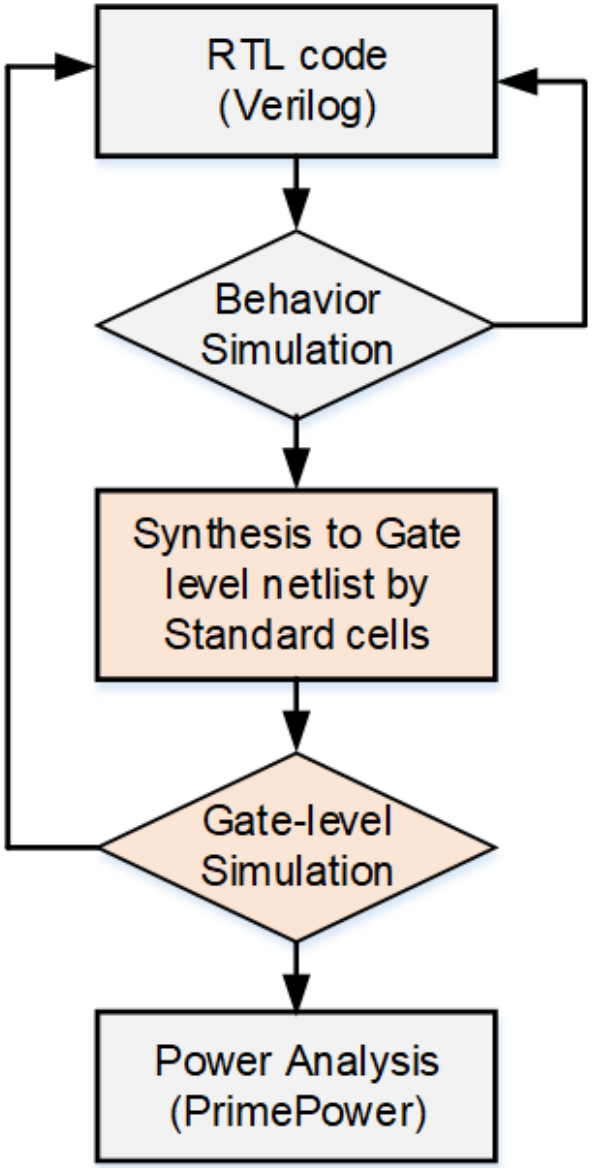
```
// Use the gated clk to trigger DFF
always @(posedge clk_gate_1 or negedge rst_n) begin
    if(!rst_n)begin
        Reg <= 0;
    end
    else if(Enable_1)begin
        Reg <= in_put;
    end
    else begin
        Reg <= Reg;
    end
end
```

Construct 3x3 convolution kernel



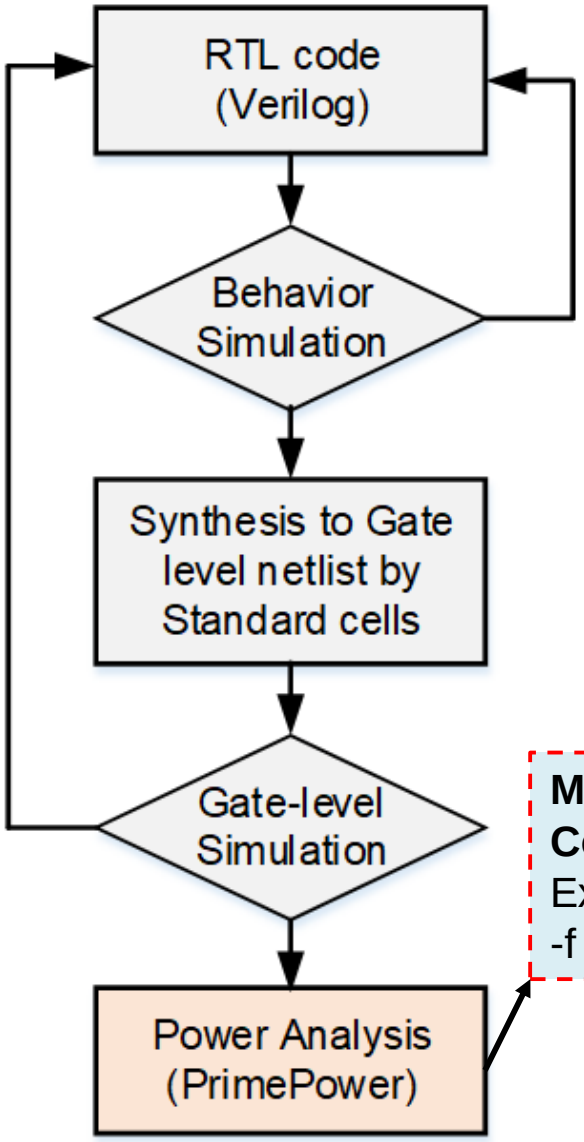
- In this exercise, you need to design the 3x3 convolution kernels
- Use the Pattern provided by TA to verify your design.

Synthesis and verify 3x3 convolution kernel



- Synthesis the 3x3 convolution kernel.
- Run the gate level simulation of 3x3 convolution kernels to verify your design and generate the **.fsdb for power measurement.**

Measure power of 3x3 convolution kernel



- Use the PrimePower to measure the power of 3x3 convolution kernels

Measure power (PrimePower)
Command:
Export SYNOPSYS_LC_ROOT=SYNOPSYS_LC_ROOTpt_shell -f ptpx.tcl | tee CORE_power.log