Verilog Lab 測驗

班級: 資工二乙

姓名: 蒲品憶

學號: 10927207

Counter

```
Ln#
 1  module Counter_sel( a, b, sel, clk, rst ,dout ) ;
 2  input clk, rst ;
 3  input[1:0] sel ;
 4  input[2:0] a, b ;
 5  output reg[3:0] dout;
 6
 7
 8  always@(posedge clk) begin
 9
10     if ( rst == 0 )
11        dout <= 4'b0000 ;
12
13     else
14
15        if ( sel == 2'b01 )
16          dout <= dout + 4'b0001 ;
17
18        else if ( sel == 2'b00 )
19          dout <= dout ;
20
21        else if ( sel == 2'b10 )
22          dout <=  { 1'b0, a } + { 1'b0, b } ;
23
24 end
25 endmodule
26
27
```

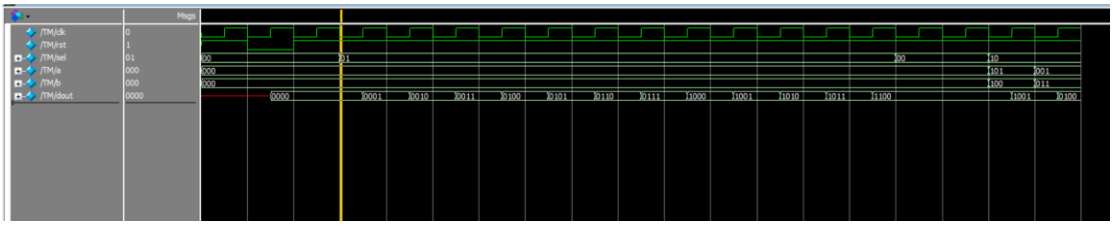
TM

```
 1  module TM;
 2
 3  reg clk, rst ;
 4  reg[1:0] sel ;
 5  reg[2:0] a, b;
 6  wire [3:0] dout;
 7
 8
 9  parameter      t = 200;
10  parameter      th= 100;
11
12  Counter_sel    U_Counter_sel  ( .a(a), .b(b), .sel(sel), .clk(clk), .rst(rst), .dout(dout) );
13
14  always #th  clk=~clk;
15  initial  begin
16    rst = 1 ;
17    sel = 2'b00 ;
18    clk = 0 ;
19    a = 3'b000 ;
20    b = 3'b000 ;
21
22    #t rst = 0;
23    #t rst = 1;
24
25    #t sel = 2'b01 ;
26
27    #(t*12)sel = 2'b00 ;
28
29
30    #(t*2) sel = 2'b10 ;
31    a = 3'b101 ;
32    b = 3'b100 ;
33    #t
34    a = 3'b001 ;
35    b = 3'b011 ;
36
37    #t $stop;
38   end
39  endmodule
40
41
```

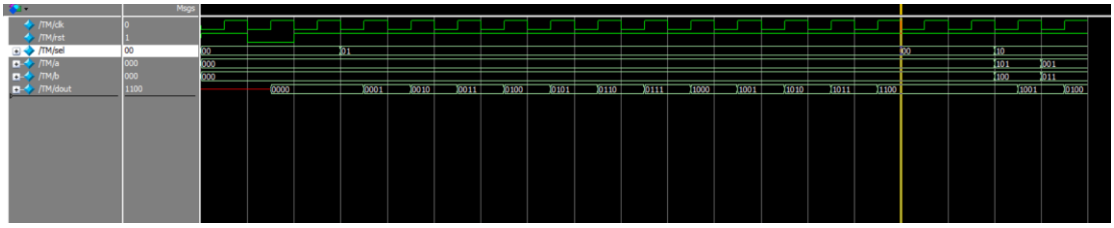
Wave

當 rst = 0 時 dout = 0

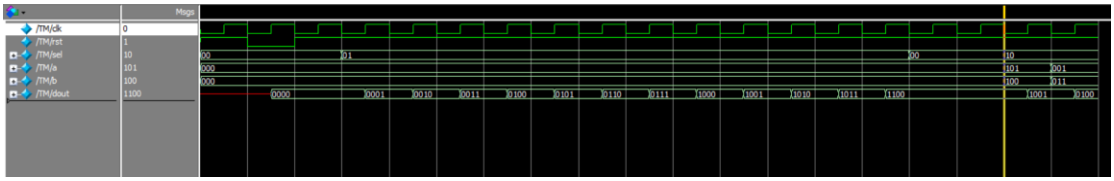
當 rst = 1 時



sel = 01 , dout = dout + 1



sel = 00 , dout = dout



sel = 10, dout = { 1’b0, a } + { 1’b0,. b }

pwd

```
VSIM 5> pwd
# D:/Lab/Lab_test_10927207
```