UM-SJTU Joint Institute

VE470

Homework 2

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1 Q1

1.1 1

It has a read after write data hazard on reg x1. As there is no forwarding the total cycle will be 9.

	1	2	3	4	5	6	7	8	9
lw	IF	D	EX	M	WB				
add		IF	D	D	D	D	EX	M	WB

1.2 2

With a forwarding RD from data memory to EX directly, it only takes 7 cycles. The forwarding still need the hazard control unit to detect and stall until the result can be correctly read. DISADVANTAGE????

	1	2	3	4	5	6	7	8	9
lw	IF	D	EX	M	WB				
add		IF	D	D	D	D	EX	M	WB

2 Q2

2.1 1

$$\begin{aligned} extra &= 25\% \times (1 - 45\%) \times 2 \\ &= 0.275 \end{aligned} \tag{1}$$

2.2 2

$$\begin{aligned} extra &= 25\% \times (1 - 55\%) \times 2 \\ &= 0.225 \end{aligned} \tag{2}$$

2.3 3

$$\begin{aligned} extra &= 25\% \times (1 - 85\%) \times 2 \\ &= 0.075 \end{aligned} \tag{3}$$

2.4 4

$$\begin{aligned} speedup &= \frac{1 + 0.075}{1 + 0.075/2} \\ &= 1.0361 \end{aligned} \tag{4}$$

2.5 5

$$\begin{aligned} 80\% + 20\% \times accuracy &= 85\% \\ accuracy &= 25\% \end{aligned} \tag{5}$$

3 Q3

Pipeline is instruction processing separated into different stages where each stage does its own function and there can be multiple instructions processed in different stages at the same time.

Superpipeline is like pipeline but divided into further substages. It allows multiple instructions to be executed in a single stage by using substages.

Supersaclar is having multiple pipelines running to execute the instructions. The most important thing for superscalar is to avoid instruction dependencies.

4 Q4

addi x11, x12, 5 nop nop add x13, x11, x12 addi x14, x11, 15 nop add x15, x13, x12

5 Q5

5.1 1

The structural hazard here is that the instructions can't be fetched when memory data operation instructions like sd and ld are executed in MEM stage.

	1	2	3	4	5	6	7	8	9	10	11	12
sd x29, 12(x16)	IF	ID	EX	MEM	WB							
ld x29, 8(x16)		IF	ID	EX	MEM	WB						
sub x17, x15, x14			IF	ID	EX	MEM	WB					
beqz x17, label				stall	stall	IF	ID	EX				
add x15, x11, x14							IF	ID	EX	MEM	WB	
sub x15, x30, x14								IF	ID	EX	MEM	WB

5.2 2

No. This is because the structural hazard will always affect the instruction fetch when a memory data operation is processing in the MEM stage. Unless the memory data operations are put at the end of the program, they will cause a stall every time it is called no matter what kind of instructions that is fetching.