UM-SJTU Joint Institute

VE470

Homework 3

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1 Q1

1.1 1

Assume there are bypass from EX/MEM to EX and from MEM/WB to EX. For each pipeline, it will have 8 bypass paths, 2 targetting at each pipeline. In total there will be 32 bypass paths. Each bypass path will have 2 wires as they need to be connected to two mux in EX stage, so there will be 64 wires. There will be 2 mux for each pipeline, so 8 mux in total. There will be additionally 8 inputs to select from bypasses.

1.2 2

Assume there are bypass from EX/MEM to EX and from MEM/WB to EX. For each pipeline, it will have 4 bypass paths, 2 targetting at each pipeline in the cluster. In total there will be 16 bypass paths. Each bypass path will have 2 wires as they need to be connected to two mux in EX stage, so there will be 32 wires. There will be 2 mux for each pipeline, so 8 mux in total. There will be additionally 4 inputs to select from bypasses.

2 Q2

2.1 1

Write-read

- L3 - L2
- L4 - L2
- L4 - L3
- L5 - L4

Write-write

- L2 - L1
- L5 - L1
- L5 - L2

Read-write

- L4 - L1
- L4 - L2
- L5 - L1
- L5 - L2

	DST			DST			DST			DST			DST			DST			Instructions	
L1	R1			R5															R5 = 100	
L2	R1	R2	R4				R6	R2	R4										R6 = R2 + R4	
L3	R2	R4								R7	R4								R7 = R4	
L4	R4	R1	R3										R8	R6	R3				R8 = R6 + R3	
L5	R1	R1														R9	R6		R9 = R6 + 30	
	Init			L1			L2			L3			L4			L5			Final	
	Map		Free list	Map		Free list	Map		Free list	Map		Free list	Map		Free list	Map		Free list	Map	Free list
	R1		R5	R1	R5		R1	R6		R1	R6		R1	R6		R1	R9		R1	R9	
	R2		R6	R2		R6	R2			R2	R7		R2	R7		R2	R7		R2	R7	
	R3		R7	R3		R7	R3		R7	R3			R3			R3			R3	R3	
	R4		R8	R4		R8	R4		R8	R4		R8	R4	R8		R4	R8		R4	R8	
			R9			R9			R9			R9			R9			R9			R9
			R10			R10			R10			R10			R10			R10			R10

2.2 2

3 Q3

1. VLIM depends heavily on compilers to fit instructions into a long instruction to solve interdependence. The compiler need to be smart enough to prevent hazard from happening.

2. When encounter instructions that can't be combined into a VLIW, i.e. some instructions can't be processed parallel, NOP will be inserted into the VLIW, reducing the number of instructions that can be processed parallel.

4 Q4

Assume there are bypass from EX/MEM to EX and from MEM/WB to EX.
See attached.

5 Q5

5.1 1

When x1 and x5 are not ready (1 - 2 and 4 can't be issued), x2 or x6 doesn't have the same value as x3 (5 can be issued), and x2 and x8 have the same value (3 can't be issued), then instruction 5 will be executed before others.

5.2 2

It's not possible. This is because instruction 4 depends on the value of x6 and x6 can only be obtained after instruction 3 is executed.