UM-SJTU Joint Institute

VE470

Homework 3

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1 Q1

1.1 1

Assume there are bypass from EX/MEM to EX and from MEM/WB to EX. For each pipeline, it will have 8 bypass paths, 2 targetting at each pipeline. In total there will be 32 bypass paths. Each bypass path will have 2 wires as they need to be connected to two mux in EX stage, so there will be 64 wires. There will be 2 mux for each pipeline, so 8 mux in total. There will be additionally 8 inputs to select from bypasses.

1.2 2

Assume there are bypass from EX/MEM to EX and from MEM/WB to EX. For each pipeline, it will have 4 bypass paths, 2 targetting at each pipeline in the cluster. In total there will be 16 bypass paths. Each bypass path will have 2 wires as they need to be connected to two mux in EX stage, so there will be 32 wires. There will be 2 mux for each pipeline, so 8 mux in total. There will be additionally 4 inputs to select from bypasses.

2 Q2

2.1 1

Write-read

- L3 - L2
- L4 - L2
- L4 - L3
- L5 - L4

Write-write

- L2 - L1
- L5 - L1
- L5 - L2

Read-write

- L4 - L1
- L4 - L2
- L5 - L1
- L5 - L2

	DST			DST			DST			DST			DST			DST			Instructions	
L1	R1			R5															R5 = 100	
L2	R1	R2	R4				R6	R2	R4										R6 = R2 + R4	
L3	R2	R4								R7	R4								R7 = R4	
L4	R4	R1	R3										R8	R6	R3				R8 = R6 + R3	
L5	R1	R1														R9	R6		R9 = R6 + 30	
	Init			L1			L2			L3			L4			L5			Final	
	Map		Free list	Map		Free list	Map		Free list	Map		Free list	Map		Free list	Map		Free list	Map	Free list
	R1		R5	R1	R5		R1	R6		R1	R6		R1	R6		R1	R9		R1	R9	
	R2		R6	R2		R6	R2			R2	R7		R2	R7		R2	R7		R2	R7	
	R3		R7	R3		R7	R3		R7	R3			R3			R3			R3	R3	
	R4		R8	R4		R8	R4		R8	R4		R8	R4	R8		R4	R8		R4	R8	
			R9			R9			R9			R9			R9			R9			R9
			R10			R10			R10			R10			R10			R10			R10

2.2 2

3 Q3

1. VLIM depends heavily on compilers to fit instructions into a long instruction to solve interdependence. The compiler need to be smart enough to prevent hazard from happening.

2. When encounter instructions that can't be combined into a VLIW, i.e. some instructions can't be processed parallel, NOP will be inserted into the VLIW, reducing the number of instructions that can be processed parallel.

4 Q4

Assume there are bypass from EX/MEM to EX and from MEM/WB to EX.
See attached.

5 Q5

5.1 1

When x1 and x5 are not ready (1 - 2 and 4 can't be issued), x2 or x6 doesn't have the same value as x3 (5 can be issued), and x2 and x8 have the same value (3 can't be issued), then instruction 5 will be executed before others.

5.2 2

It's not possible. This is because instruction 4 depends on the value of x6 and x6 can only be obtained after instruction 3 is executed.

	C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	C11	C12	C13
ld [r1] → r3	F	Di	I	RR	X	M1	M2	W	C					
mult r3*r2 → r4	F	Di				I	RR	X	X1	X2	W	C		
add r2+r5 → r4		F	Di	I	RR	X	W					C		
or r4^r6 → r7		F	Di		I	RR	X	W					C	
sub r7-3 → r8			F	Di		I	RR	X	W				C	
ld [r9] → r7			F	Di	I	RR	X	M1	M2	W				C
Ready Table														
p1	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES
p2	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	F	F	F
p3	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	F	F
p4	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	F	F
p5	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES
p6	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES
p7	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES
p8	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES
p9	YES	YES	YES	YES	YES	YES	YES	YES	F	F	F	F	F	F
p10	NO	NO	NO	NO	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES
p11	NO	NO	NO	NO	NO	NO	NO	YES	YES	YES	YES	F	F	F
p12	F	NO	NO	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES
p13	F	NO	NO	NO	YES	YES	YES	YES	YES	YES	YES	YES	YES	F
p14	F	F	NO	NO	NO	YES	YES	YES	YES	YES	YES	YES	YES	YES
p15	F	F	NO	NO	NO	NO	YES	YES	YES	YES	YES	YES	YES	YES

C1	Instruction	src1	R	src2	R	dst	Bday		Map Table			ROB		
	ld	p8	Y	N	Y	p10	0		r1	p8		ld	p9	
	mult	p10	N	p7	Y	p11	0		r2	p7		mult	p2	
									r3	p10				
									r4	p11				
									r5	p5				
									r6	p1				
									r7	p4				
									r8	p3				
									r9	p6				

C2	Instruction	src1	R	src2	R	dst	Bday		Map Table			ROB		
									r1	p8		ld	p9	
	mult	p10	N	p7	Y	p11	0		r2	p7		mult	p2	
	add	p7	Y	p5	Y	p12	1		r3	p10		add	p11	
	or	p12	N	p1	Y	p13	1		r4	p12		or	p4	
									r5	p5				
									r6	p1				
									r7	p13				
									r8	p3				
									r9	p6				

C3	Instruction	src1	R	src2	R	dst	Bday		Map Table			ROB		
									r1	p8		ld	p9	

	mult	p10	N	p7	Y	p11	0		r2	p7		mult	p2	
									r3	p10		add	p11	
	or	p12	Y	p1	Y	p13	1		r4	p11		or	p4	
	sub	p13	N	N	Y	p14	2		r5	p5		sub	p3	
	ld	p6	Y	N	Y	p15	2		r6	p1		ld	p13	
									r7	p15				
									r8	p14				
									r9	p6				

C4	Instruction	src1	R	src2	R	dst	Bday					ROB		
												ld	p9	
	mult	p10	Y	p7	Y	p11	0					mult	p2	
												add	p11	
												or	p4	
	sub	p13	Y	N	Y	p14	2					sub	p3	
												ld	p13	

C5	Instruction	src1	R	src2	R	dst	Bday							

C6												ROB		
												ld	p9	
												mult	p2	
												add	p11	DONE
												or	p4	
												sub	p3	
												ld	p13	

C7												ROB		
												ld	p9	DONE
												mult	p2	
												add	p11	DONE
												or	p4	DONE
												sub	p3	
												ld	p13	

C8												ROB		
												mult	p2	
												add	p11	DONE
												or	p4	DONE
												sub	p3	DONE
												ld	p13	

C9												ROB		
												mult	p2	
												add	p11	DONE
												or	p4	DONE
												sub	p3	DONE
												ld	p15	DONE

C10												ROB		
												mult	p2	DONE
												add	p11	DONE
												or	p4	DONE
												sub	p3	DONE
												ld	p15	DONE

C11												ROB		
												or	p4	DONE
												sub	p3	DONE
												ld	p15	DONE

C12												ROB		
												ld	p15	DONE

C13												ROB		