UM-SJTU Joint Institute

VE470

Homework 1

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1 Q1

1. We are at the end of Dennard scaling and have reaches the end of Moore's Law and Amdahl's Law. The efficiency of the performance is reaching a bottle neck and need to have some breakthrough on architecture. There are many to do in the field of computer architecture.

2. High level languages that abstract hardware designs make hardware design much easier, which allow computer architects to put more effort in innovation.

3. The trend of open source hardware can allow computer architects to base their design on open source cores, which enable them to do more top level designs and optimization.

4. ECAD tools enable computer architects to do agile hardware development, resulting in faster generation renovation.

2 Q2

1. Efficient usage of RAM as for same function, CISC uses less instructions and thus less interaction with the memory.

2. CISC reduce compiler's work. RISC need complier to be interpret programs to more lines of instructions.

3 Q3

benchmarks	Loads	Stores	Branches	Jumps	ALU	Original clock cycles	ALU Improved clock cycles	ALU Speed up	Branch Improved clock cycles	Branch Speed up
	28	6	18	2	46	460	414	1.111111111	422	1.090047393
	20	7	11	1	54	418	364	1.148351648	395	1.058227848
	17	23	20	4	36	453	417	1.086330935	409	1.107579462
	21	12	14	2	50	448	398	1.125628141	418	1.071770335
	33	14	5	2	45	474	429	1.104895105	462	1.025974026
	28	9	17	0	46	465	419	1.109785203	431	1.078886311
	16	6	29	0	48	434	386	1.124352332	376	1.154255319
mcf	35	11	24	1	29	480	451	**1.064301552**	431	**1.113689095**
	23	15	17	7	31	426	395	1.078481013	385	1.106493506
	24	14	15	7	39	451	412	1.094660194	414	1.089371981
sjeng	19	7	15	3	56	442	386	**1.14507772**	409	**1.080684597**
	30	8	27	3	31	461	430	1.072093023	404	1.141089109
					AVG	**451**	**408.4166667**	**1.104264436**	**413**	**1.092009685**
					AVG CPI	**4.51**	**4.084166667**		**4.13**	

From these benchmarks, it can be seen that ALU improvement works better under sjeng benchmark but worse in mcf benchmark. As sjeng relies heavily on ALU operations, 56%, it would be better to look at all benchmarks and do average. From the result, it can be seen that ALU speedup has a slighter larger value for speed up ratio over all benchmarks. It would be better to implement the ALU speed up.

4 Q4

Set the percentage of enhanced mode to be $x\%$, then the overall speed up will be $1/(x\%/2.5 + (1 - x\%))$. Therefore we solve the equation:

$$\frac{1}{x\%/2.5 + (1 - x\%)} = 1.1$$

, which gives:

$$x \approx 15.1515$$

This means around 15% of the program must be run in enhanced mode.

5 Q5

5.1 1

PDP $= P_{avg} * t = 105 * 1/(2.7 * 10^9) = 3.88 * 10^{-8} J$
EDP $= PDP * t = 3.88 * 10^{-8} * 1/(2.7 * 10^9) = 1.44 * 10^{-17} JS$
EDDP $= EDP * t = 1.44 * 10^{-17} * 1/(2.7 * 10^9) = 5.33 * 10^{-27} JS^2$

5.2 2

As dynamic power is 3/4 of the total power, when total power is $105W$, the dynamic power is $105 * 3/4 = 78.75W$.

As $P_{dynamic} = \alpha f C_L V_{DD}^2$, we have:

$$\alpha C_L V_{DD}^2 = 78.75/2.7 = 29.17W/GHz$$

Therefore, when dynamic power is $130W$:

$$f_{max} = \frac{P_{dynamic}}{\alpha C_L V_{DD}^2} = \frac{130}{29.17} = 4.46GHz$$

6 Q6

Cost of die is given $Costofwafer/Diesperwafer/Dieyield$.
Dies per wafer can be calculated:

$$\begin{aligned} Dies\ per\ wafer &= \frac{Wafer\ area}{Die\ area} - \frac{\pi * Wafer\ diameter}{\sqrt{2 * Die\ area}} \\ &= \frac{\pi 21^2}{2.4} - \frac{\pi * 42}{\sqrt{2 * 2.4}} \approx 517 \end{aligned} \tag{1}$$

Die yield can be calculated:

$$\begin{aligned} Die\ yield &= \frac{Wafer\ yield}{(1 + Defects\ per\ unit\ area * Die\ area)^{\alpha}} \\ &= \frac{0.99}{(1 + 0.016 * 2.4)^{10}} \\ &= 0.68 \end{aligned} \tag{2}$$

Therefore, we cost of die can be calculated:

$$\begin{aligned} Cost\ of\ die &= \frac{\$9000}{517 * 0.68} \\ &= \$25.60 \end{aligned} \tag{3}$$

7 Q7

According to formula:

$$\begin{aligned} S_{opt} &= \sqrt{\frac{(1-b)T}{bC}} \\ &= \sqrt{\frac{(1-0.2) * (700 * 10^6)^{-1} * (1+0.05)}{0.2 * 500 * 10^{-12}}} \\ &\approx 3.46 \end{aligned} \tag{4}$$

Therefore, the approximated optimized stage is 3.

The new clock frequency can be calculated:

$$\begin{aligned} f &= \frac{1}{T/S + C} \\ &= \frac{1}{(700 * 10^6)^{-1} * (1+0.05)/3 + 500 * 10^{-12}} \\ &= 1GHz \end{aligned} \tag{5}$$

The throughput can be calculated by:

$$\begin{aligned} throughput &= performance * f \\ &= \frac{f}{1 + (S-1)b} \\ &= \frac{1 * 10^9}{1 + (5-1)0.2} \\ &= 5.55 * 10^8 \end{aligned} \tag{6}$$

8 Q8

1. 1 - 7 RAW
2. 2 - 4 RAW
3. 2 - 5 WAW
4. 2 - 6 WAR
5. 3 - 4 RAW
6. 3 - 6 WAR
7. 4 - 5 RAW
8. 4 - 5 WAR

9 Q9

More registers doesn't means it is better. Here are the reasons:

1. More registers makes the cache larger, which is more expensive.
2. More registers can cause a slightly more time to look up the value, which can be a lot when many instructions are run.
3. More registers will lead to an extended address size, meaning the length of the instruction will be longer, which can cause trouble.