COL215 Hardware Assignment 2 Report
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!!!!!!!!!!!!!!!!!!!!!!Working of the Stopwatch!!!!!!!!!!!!!!!!!!!!!!!!!!

1. The reset is a master input, no input works while reset is in motion.
2. The inputs signals only work only on a rising edge of inputs(accompolished through process 1 of module a2).
3. Continue only works after pause signal. While start can also be used to start the stopwatch after a pause signal.
4.!!!!!!! Important , Sometimes due to the functionality of triggering of inputs on rising edges only , the inputs may not work(with a probability 1/11,due to signal change being registered in the time window when it was rising edge of system clock was being registered).
5. Don't override the stopwatch with signals, it is non beneficial to the hardware. The basys 3 board is a delicate machine and can be damaged by the carelessness of one.
6. The stopwatch will automatically reset after reaching 10 minutes and continue running afterwards. This specification can be changed by adding a line of code in the 2nd module of a2.

Design decisions for the hardware--

The components are mapped in the Stopwatch module.

The code consists of 2 components A1 and a2:

1. a2 , the counter which gives changing 4 digits of the seven segment display

There are 3 processes in this module.

***The first process changes the enable_watch signal based on the info whether the portsignals start, pause, reset, continue have changed to'1' from the assigned signals starter,pauser, continuer, reseter , the last time they were assigned, that is the last rising edge of the system clock. The process also changes a signal pause_continue to make thecontinue port signal work only when pause_continue = '1', and hence continue port cannot start the stopwatch after a reset.

*** The second process uses a counter k to count to 10^7 period of the 10ns seconds clock,effectively counting to 0.1s .It then changes value of n4 which denotes the 4th digit of 7 segment display until it counts to 9, at which 1s has already been counted and n4 is changed to 0 via n4 = n4+1 mod 10 functionality. An if statement starting the counting of n3 every time 1s passes or n4 has reached the value 9 in previous iteration and is just going to change is implemented. Similiar use of if else statements provide us with n1, n2, n3 ,n4 respectively being the 4 digits of seven segment display in integer signal format.

***The third process is a encoder which converts the decimals n1 to n4 to binary outputs i1 to i16 which

are required in the A1 component as inputs for display of 4 digit seven segment display. This is done through drawing a encoder table and repeated use of if -else statements.

2. A1 , the bit decoder which provides all the outputs depending on i1 to i16 from a2 module.

There are 3 processes in this module.

*** The Timing circuit

We have the access to a clock input port(clk) in the basys 3 board which we can use to measure time for our timing circuit. It has a period of 10 nanoseconds. We define a process with the sensitivity list containing the clk clock and measure a time of 1 ms with the help of a counter i, which is a signal of the type integer, instantiated at the initial value of 0. The counter i increments every rising edge of the clock using the rising_edge function and every time the counter reaches the value of 400000, the counter is reset to 0. Every 100000 iterations of I; a, b, c, d which correspond to outputs of the anode signals are maintained at values with only one of them being '0'(0 is active in basys 3 board) at the same time, the other having the value

of '1'. Correspondingly the selection inputs s0 and s1 of the multiplexer circuit mentioned in the next component is also maintained to work the corresponding cathode signals.

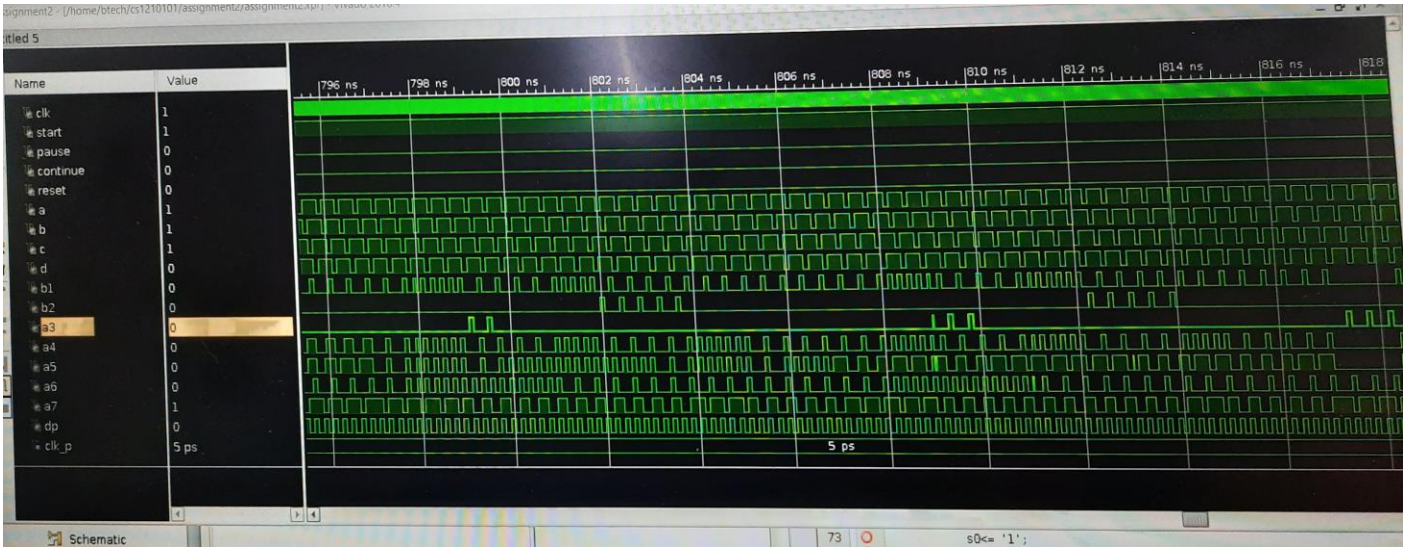
*** Multiplexer circuit

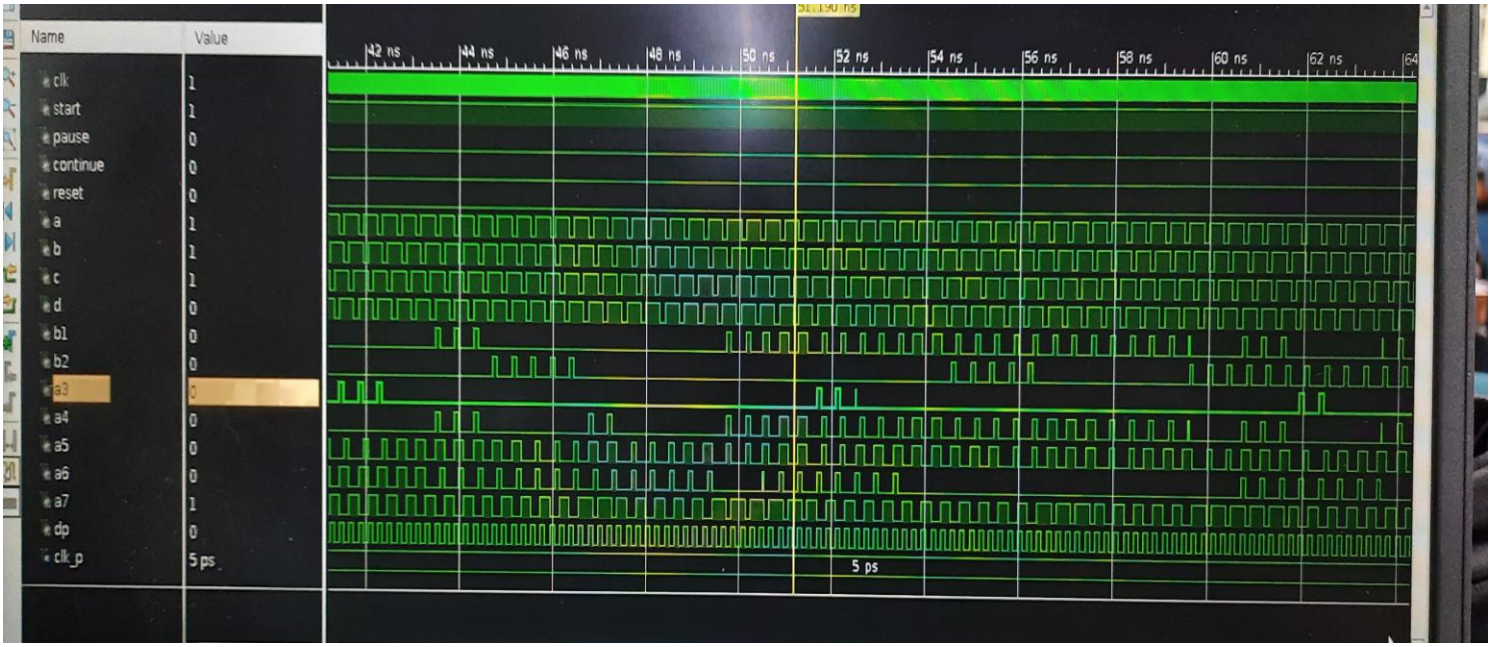
The multiplexer circuit uses the bits s0 and s1 from the timing circuit to find what bits should be used in the 7-bit decoder to find the 7 corresponding signals to the cathode for every active anode. The multiplexer logic is used 4 times in a process, which has s0, s1 and the inputs i1 to i16 in the sensitivity list. Every 0.6 ms when s0 or s1 is updated, the signals u0 to u3, the outputs of each multiplexer logic is the output. The multiplexer logic has the inputs i1 to i16 in and operation of 4 different and operation combinations of s0, s1 and their complements.

*** The 7-bit decoder

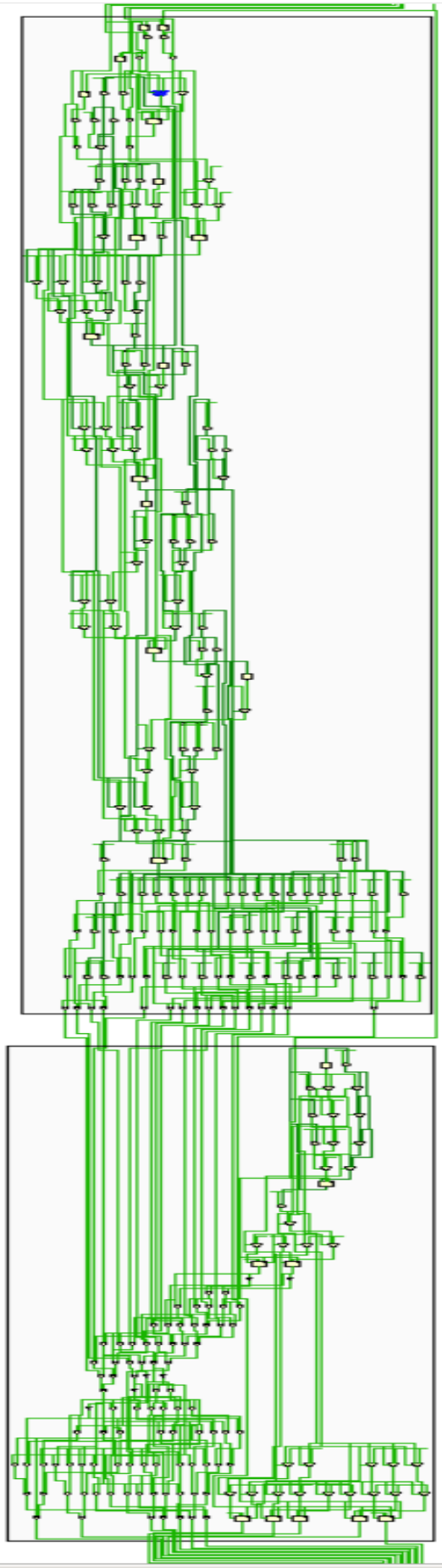
In the 7-bit decoder, logic is used to obtain 7 bits to obtain 16 different combinations pertaining to the 16 different hexadecimal digits. The seven-bit decoder takes the values u0 to u3 which are obtained through the multiplexer circuit, they also change every 0.6 ms courtesy to the multiplexer being run over s0, s1 which are obtained from the timing circuit. The cathodes are operative when it is driven low, instead of high just like the anodes, so it can be a common mistake while designing the code.

Simulation Snapshots





Block Diagram



Synthesis Report

| Tool Version : Vivado v.2016.4 (lin64) Build 1756540 Mon Jan 23 19:11:19 MST 2017
| Date : Sun Oct 30 13:03:21 2022
| Host : dhd running 64-bit Ubuntu 20.04.3 LTS
| Command : report_utilization -file Stopwatch_utilization_synth.rpt -pb Stopwatch_utilization_synth.pb
| Design : Stopwatch
| Device : 7a35tcpg236-1
| Design State : Synthesized

Utilization Design Information

Table of Contents

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1. Slice Logic

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	756	0	20800	3.63
LUT as Logic	756	0	20800	3.63
LUT as Memory	0	0	9600	0.00
Slice Registers	91	0	41600	0.22
Register as Flip Flop	91	0	41600	0.22
Register as Latch	0	0	41600	0.00
F7 Muxes	0	0	16300	0.00
F8 Muxes	0	0	8150	0.00

* Warning! The Final LUT count, after physical optimizations and full implementation, is typically lower. Run opt_design after synthesis, if not already completed, for a more realistic count.

1.1 Summary of Registers by Type

Total	Clock Enable	Synchronous	Asynchronous
0	_	-	-
0	_	-	Set
0	_	-	Reset
0	_	Set	-
0	_	Reset	-
0	Yes	-	-
0	Yes	-	Set
0	Yes	-	Reset

| 3 | Yes | Set | - |
| 88 | Yes | Reset | - |
+-------+--------------+-------------+--------------+

2. Memory

+----------------+------+-------+-----------+-------+
| Site Type | Used | Fixed | Available | Util% |
+----------------+------+-------+-----------+-------+
Block RAM Tile	0	0	50	0.00
RAMB36/FIFO*	0	0	50	0.00
RAMB18	0	0	100	0.00
+----------------+------+-------+-----------+-------+
* Note: Each Block RAM Tile only has one FIFO logic available and therefore can accommodate only one FIFO36E1 or one FIFO18E1. However, if a FIFO18E1 occupies a Block RAM Tile, that tile can still accommodate a RAMB18E1

3. DSP

+-----------+------+-------+-----------+-------+
| Site Type | Used | Fixed | Available | Util% |
+-----------+------+-------+-----------+-------+
| DSPs | 0 | 0 | 90 | 0.00 |
+-----------+------+-------+-----------+-------+

4. IO and GT Specific

+-----------------------------+------+-------+-----------+-------+
| Site Type | Used | Fixed | Available | Util% |
+-----------------------------+------+-------+-----------+-------+
Bonded IOB	17	0	106	16.04
Bonded IPADs	0	0	10	0.00
Bonded OPADs	0	0	4	0.00
PHY_CONTROL	0	0	5	0.00
PHASER_REF	0	0	5	0.00
OUT_FIFO	0	0	20	0.00
IN_FIFO	0	0	20	0.00
IDELAYCTRL	0	0	5	0.00
IBUFDS	0	0	104	0.00
GTPE2_CHANNEL	0	0	2	0.00
PHASER_OUT/PHASER_OUT_PHY	0	0	20	0.00
PHASER_IN/PHASER_IN_PHY	0	0	20	0.00
IDELAYE2/IDELAYE2_FINEDELAY	0	0	250	0.00
IBUFDS_GTE2	0	0	2	0.00
ILOGIC	0	0	106	0.00
OLOGIC	0	0	106	0.00
+-----------------------------+------+-------+-----------+-------+

5. Clocking

+------------+------+-------+-----------+-------+
| Site Type | Used | Fixed | Available | Util% |
+------------+------+-------+-----------+-------+
| BUFGCTRL | 1 | 0 | 32 | 3.13 |

BUFIO	0	0	20	0.00
MMCME2_ADV	0	0	5	0.00
PLLE2_ADV	0	0	5	0.00
BUFMRCE	0	0	10	0.00
BUFHCE	0	0	72	0.00
BUFR	0	0	20	0.00

6. Specific Feature

Site Type	Used	Fixed	Available	Util%
BSCANE2	0	0	4	0.00
CAPTUREE2	0	0	1	0.00
DNA_PORT	0	0	1	0.00
EFUSE_USR	0	0	1	0.00
FRAME_ECCE2	0	0	1	0.00
ICAPE2	0	0	2	0.00
PCIE_2_1	0	0	1	0.00
STARTUPE2	0	0	1	0.00
XADC	0	0	1	0.00

7. Primitives

Ref Name	Used	Functional Category
LUT6	275	LUT
LUT2	216	LUT
CARRY4	159	CarryLogic
LUT4	119	LUT
LUT5	111	LUT
FDRE	88	Flop & Latch
LUT3	85	LUT
LUT1	74	LUT
OBUF	12	IO
IBUF	5	IO
FDSE	3	Flop & Latch
BUFG	1	Clock

8. Black Boxes

Ref Name	Used

9. Instantiated Netlists

Ref Name	Used