CPE 322 **EXAM 2** **Name** Solution

Spring Semester 2022

Work should be performed systematically and neatly with the final answer being underlined. This exam is closed book, closed notes, closed neighbor. Allowable items on desk include: exam, supplied Verilog Reference Handout, pencils/pens, and simple calculators that do not have internet access. All other items must be removed from student's desk. Students have approximately 90 minutes (1 1/2 hours) to complete this exam. Best wishes!

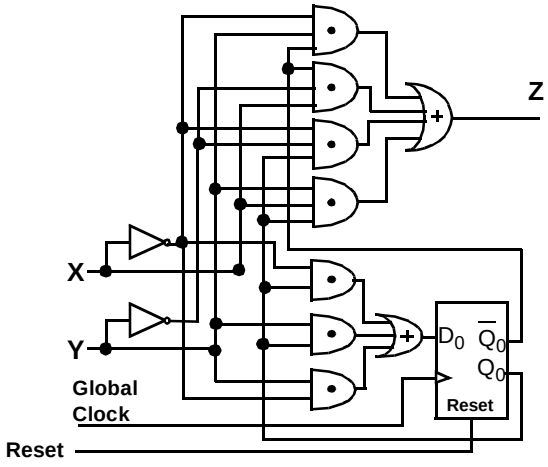
1. [34 points total] A sequential network is implemented using discrete components as shown below. The manufacturers minimum and maximum gate propagation delays are shown in the table below.

Gate Type	Minimum Delay	Maximum Delay
Inverter	1ns	2 ns
2-Input AND Gate	2ns	3 ns
3-Input AND Gate	3 ns	4 ns
3-Input OR Gate	3 ns	5 ns
4-Input OR Gate	3 ns	6 ns

The manufacturers timing parameters for the rising edge D-flip-flop is shown in the table below:

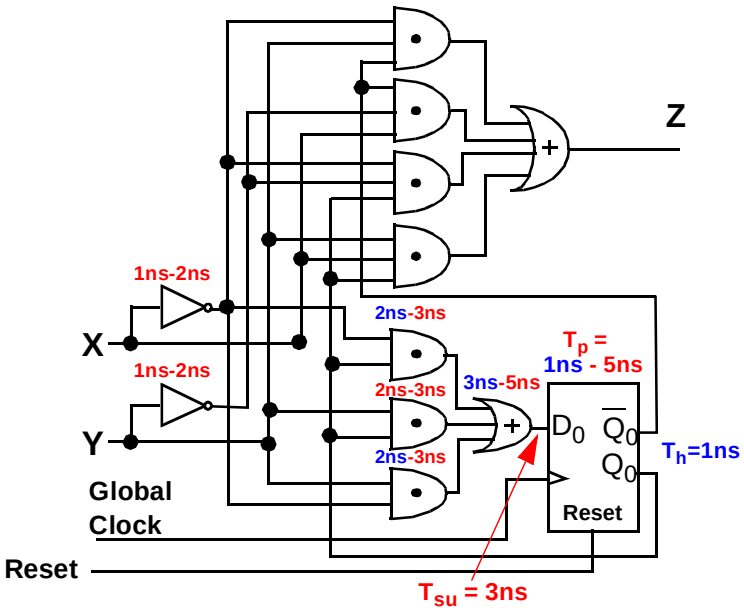
D-Flip-Flop Parameter	Timing Delay
Propagation Delay, Tp (clock to output)	1 ns Minimum 5 ns Maximum
Setup Time	3 ns
Hold Time	1 ns

External logic has been designed so that both inputs *X* and *Y* can only change their values on the falling edge of the 50% duty cycle clock



Gate Type	Min Delay	Max Delay
Inverter	1ns	2 ns
2-Input AND Gate	2ns	3 ns
3-Input AND Gate	3 ns	4 ns
3-Input OR Gate	3 ns	5 ns
4-Input OR Gate	3 ns	6 ns

D-Flip-Flop	Timing Delay
Tp (clock to output)	1 ns Min 5 ns Max
Setup Time	3 ns
Hold Time	1 ns



a) [10 points/34 points] Determine if the flip/flop hold times are met. Show all steps. If the hold times are not met describe changes in the circuit where that would fix the problem.

Case 1: Flip-Flop Output to Flip-Flop Input Hold Time Analysis

Tc_{min} = 2ns + 3ns = 5ns, $min(T_p)$ = 1ns, T_h = 1ns

shortest delay path from Q_0 back to D_0

$T_h \leq Tc_{min} + min(T_p)$ → 1ns ≤ 5ns + 1ns → 1ns ≤ 6ns

Which is True for FF to FF path Hold time is met

Case 2: Design Input to Flip-Flop Input Hold Time Analysis

Tcy_{min} = 2ns + 3ns = 5ns, T_h = 1ns,

shortest delay path from inputs X or Y to flip-flop's D_0. Note: shortest path is from input Y into bottom AND gate bypassing the inverter

$T_h \leq Tcy_{min}$ → 1ns ≤ 5ns

Which is also True for Input to FF path Hold time is met

b) [18 points/34 points] Determine the maximum clock frequency that this circuit could be driven while still meeting all specified timing constraints. Show all steps.

Case 1: Flip-Flop Output to Flip-Flop Input Analysis

Tc_{max} = 3ns + 5ns = 8ns, $max(T_p)$ = 5ns, T_{su} = 3ns

$min(T_{cycle})_{case\ 1} = max(T_p) + Tc_{max} + T_{su}$ = 5ns + 8ns + 3ns = 16ns

Case 2: Design Input to Flip-Flop Input Analysis

Tcx_{max} = 2ns + 3ns + 5ns = 10ns, T_{su} = 3ns

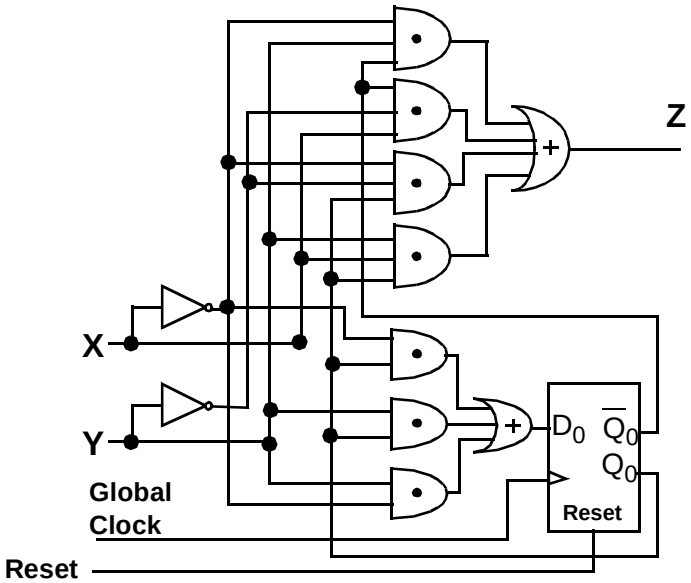
$1/2\ min(T_{cycle})_{case\ 2} = Tcx_{max} + T_{su}$ = 10ns + 3ns = 13ns → $min(T_{cycle})_{case\ 2}$ = 26ns

longest $min(T_{cycle})$

$F_{max} = 1/min(T_{cycle})_{case\ 2}$ = 1/26ns = 38.46 Mhz

Gate Type	Min Delay	Max Delay
Inverter	1ns	2 ns
2-Input AND Gate	2ns	3 ns
3-Input AND Gate	3 ns	4 ns
3-Input OR Gate	3 ns	5 ns
4-Input OR Gate	3 ns	6 ns

D-Flip-Flop	Timing Delay
Tp (clock to output)	1 ns Min 5 ns Max
Setup Time	3 ns
Hold Time	1 ns



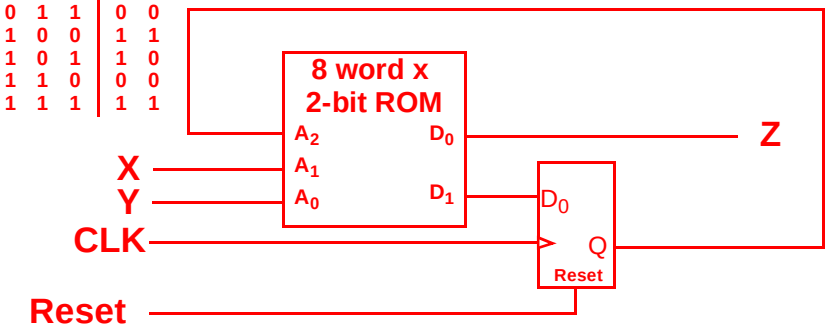
c) [6 points/34 points] Could the maximum clock frequency be increased by changing the duty cycle (i.e. changing the proportion of the time the clock is at a logic 1)? Explain your answer fully.

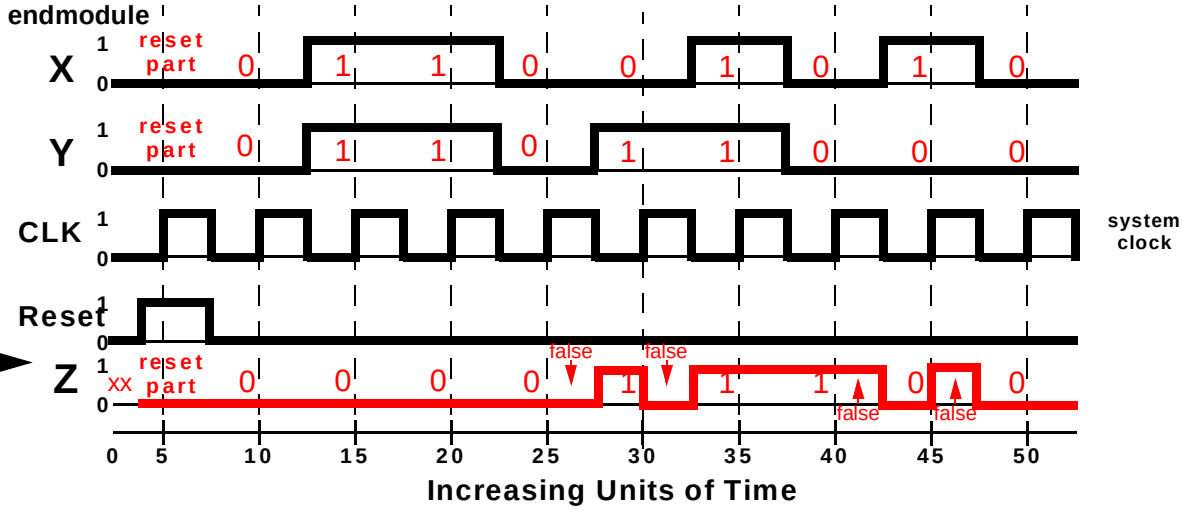
2. [33 points] Complete the following timing diagram for the Finite State Machine represented by the Verilog Model that is shown below. The signals X, Y, are inputs and Z is the output. In your diagram assume that all propagation delays are negligible (i.e. zero).

```
module FSM (input X, Y, Reset, CLK, output reg Z);

  reg [1:0] ROM [0:7];
  reg Q=1'bx,Din;

  initial
    begin
      ROM[0]=2'b00;
      ROM[1]=2'b11;
      ROM[2]=2'b01;
      ROM[3]=2'b00;
      ROM[4]=2'b11;
      ROM[5]=2'b10;
      ROM[6]=2'b00;
      ROM[7]=2'b11;
    end

  always @ (Q,X,Y)
    {Din,Z} = ROM[{Q,X,Y}];

  always @(posedge CLK, posedge Reset)
    if (Reset) Q = 0;
    else Q = Din;
endmodule
```

ROM Table

Address A_2	A_1	A_0	Data D_1	D_0
0	0	0	0	0
0	0	1	1	1
0	1	0	0	1
0	1	1	0	0
1	0	0	1	1
1	0	1	1	0
1	1	0	0	0
1	1	1	1	1





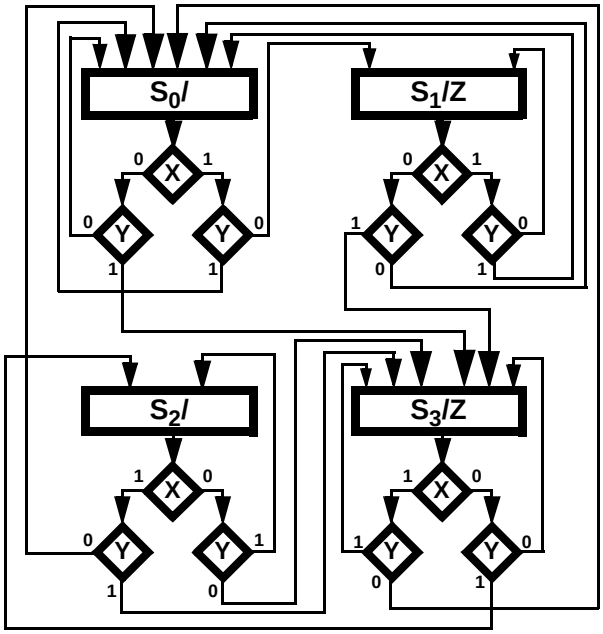
What general class of sequential network does this logic circuit represent?
Meally

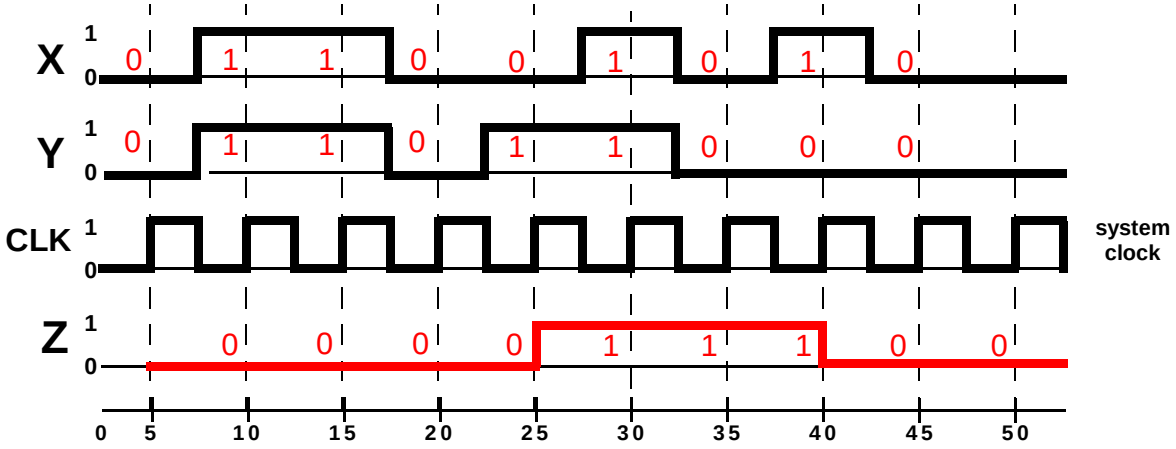
Write down the input sequence for X and Y
X=0,1,1,0,0,1,0,1,0
Y=0,1,1,0,1,1,0,0,0
Write down the output sequence for Z.
Z=0,0,0,0,1,1,1,0,0

Are there any 'false' outputs on the timing diagram? If so clearly identify them.
Yes, they are labeled on the timing diagram

3.> [33 points] Complete the following timing diagram for the Finite State Machine represented by the Algorithmic State Machine (State Chart) shown below. The signals X, Y, are inputs and Z is the output. In your diagram assume that all propagation delays through the gates and flip-flops are negligible (i.e. zero). Also assume that at time zero the Finite State Machine is placed in state S_0 and that transitions between states respond to the rising edge of the system clock.

Inputs:
X, Y
Output:
Z





Increasing Units of Time

What class of sequential network does this logic circuit represent?
Moore

Write down the input sequence for X and Y
X=0,1,1,0,0,1,0,1,0
Y=0,1,1,0,1,1,0,0,0
Write down the output sequence for Z.
Z=0,0,0,0,1,1,1,0,0

Are there any 'false' outputs on the timing diagram? If so clearly identify them.
No there are no false outputs because the ASM diagram only had outputs assigned to the states which made it a Moore FSM class sequential network.