EE 316: Electrical Circuits and Electronic Design Laboratory.

Lab 07

Characteristics of FETs.

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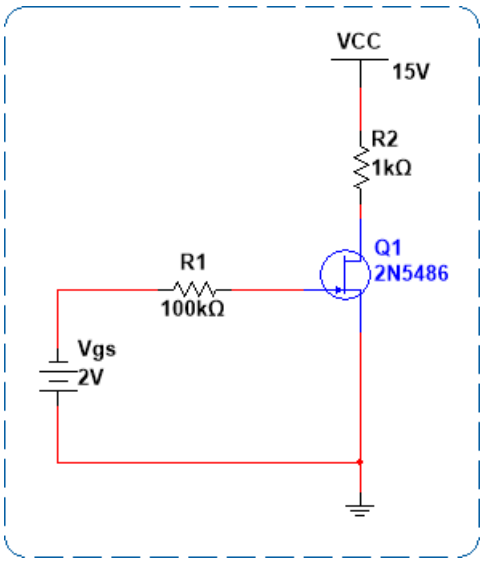
Date of Experiment: 10/10/22.

INTRODUCTION:

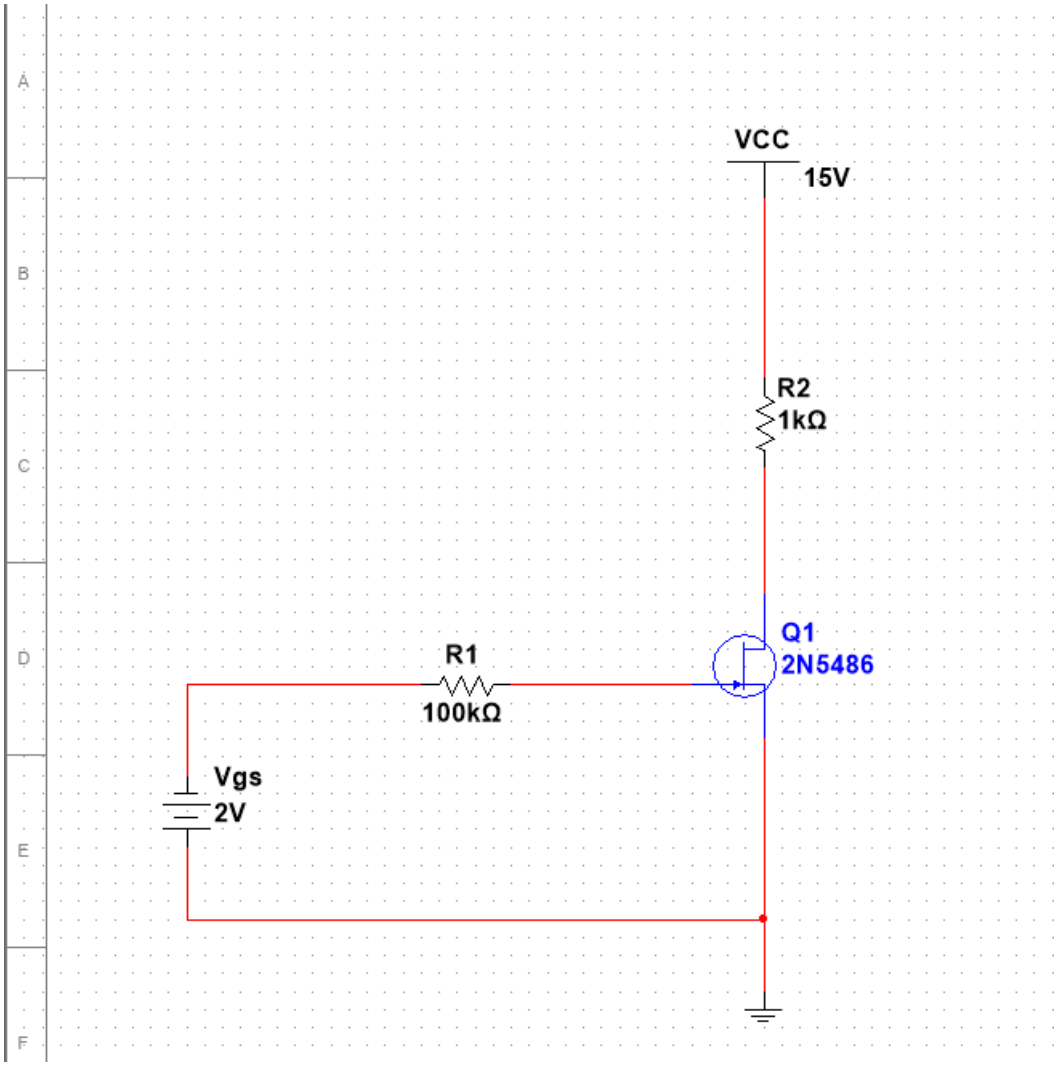
The laboratory was an introduction to Field Effect Transistors (FETs) that include added components of a gate to a BJT. The first step of this lab was to design and simulate a JFET circuit to analyze the current flowing through a resistor to the drain gate of a 2N5486 JFET. The second part of this lab was to design the same circuit in hardware, and in both cases, find the pinch voltage.

PART A:

The first part of the lab was to design and simulate the circuit shown below:

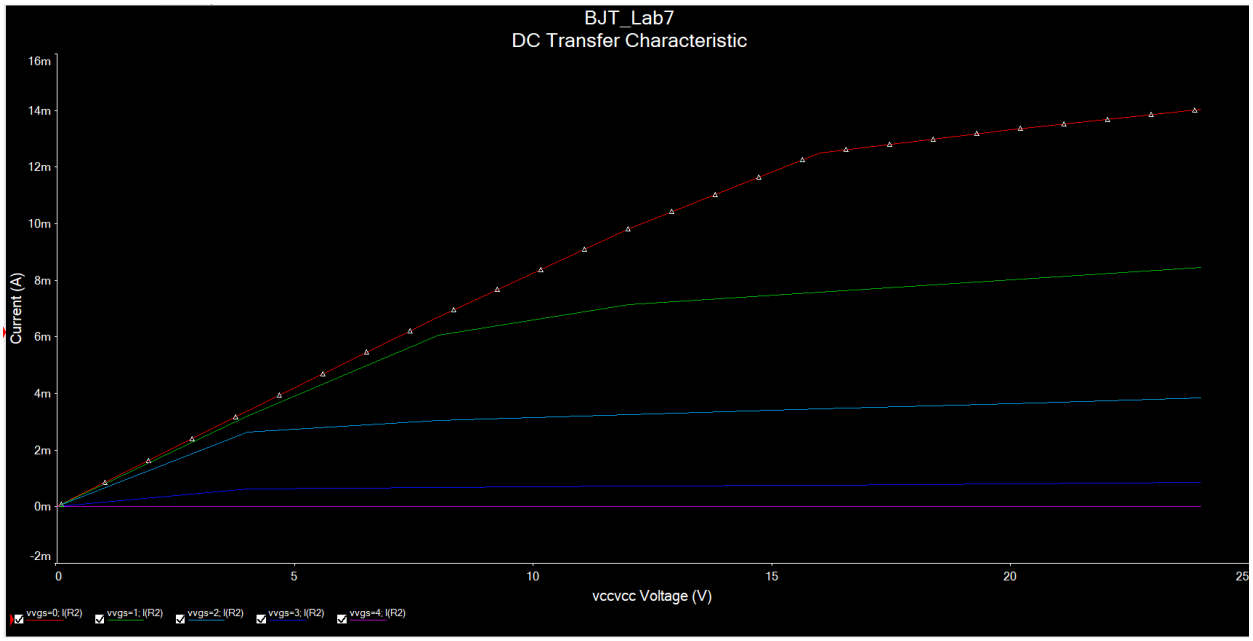


The circuit was completed in Multisim as shown:



To simulate the circuit and read the current flowing through the drain at different voltage inputs through the gate, we had to run a DC sweep and export the results in a spreadsheet. Table 9.1 of the lab is not copied below, however, the screenshots of the Excel spreadsheet containing data from the DC sweep for table 9.1 is included. The sweep was completed with the configurations suggested in the lab manual. (Source 1 to Vcc – range 0-24, increment of 4, Source 2 to Vgs – range 0-4, increment of 1). Output was selected as the current of the drain, which is IR2.

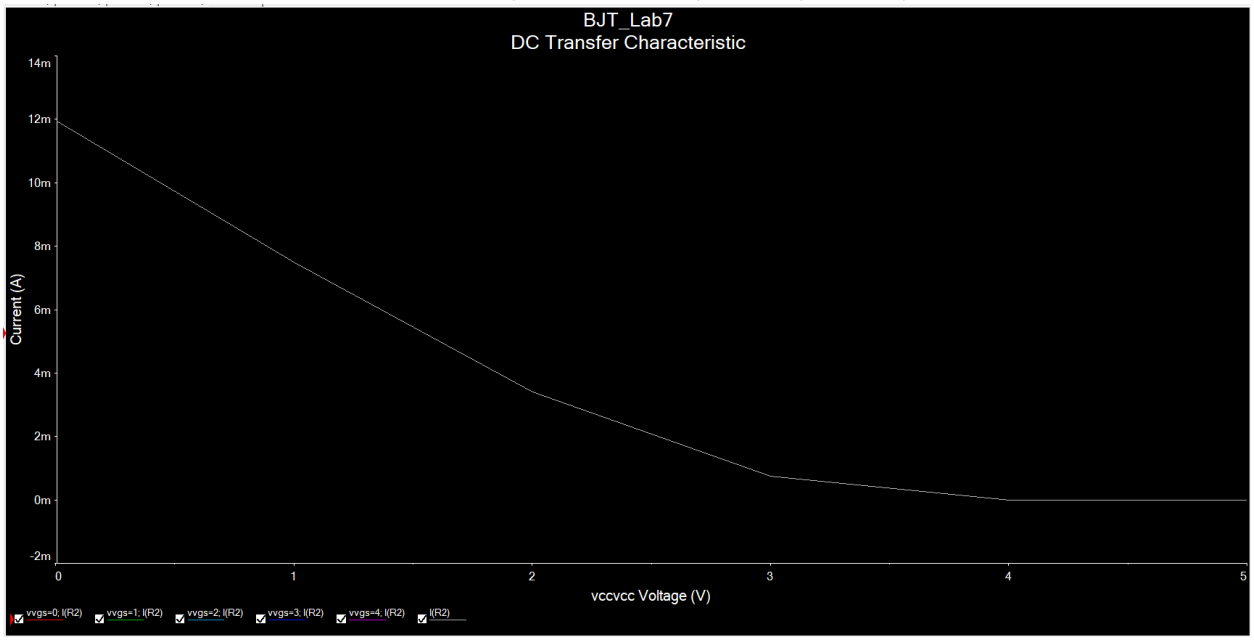
Graph for Simulation analysis through DC sweep.



X--Trace 1	Y--Trace 1::[vvgs=0; I(R2)]	Y--Trace 2::[vvgs=1; I(R2)]	Y--Trace 3::[vvgs=2; I(R2)]	Y--Trace 4::[vvgs=3; I(R2)]	Y--Trace 5::[vvgs=4; I(R2)]
0	3.18678E-28	1.81941E-13	5.03655E-13	1.25629E-12	4.0002E-12
4	0.003392602	0.00319051	0.002645968	0.000629837	1.60003E-11
8	0.006695054	0.006059131	0.003047641	0.000674825	2.80003E-11
12	0.00983171	0.007153226	0.003248315	0.000719291	4.00004E-11
16	0.012490756	0.007588259	0.00344661	0.000763642	5.20004E-11
20	0.013317774	0.008020865	0.003644428	0.00080794	6.40005E-11
24	0.014033169	0.008451922	0.003841784	0.000852186	7.60005E-11
			Converted to mA.		
	3.187E-25	1.819E-10	5.037E-10	1.256E-09	4.00E-09
	3.39	3.19	2.65	0.63	1.60E-08
	6.70	6.06	3.05	0.67	2.80E-08
	9.83	7.15	3.25	0.72	4.00E-08
	12.49	7.59	3.45	0.76	5.20E-08
	13.32	8.02	3.64	0.81	6.40E-08
	14.03	8.45	3.84	0.85	7.60E-08

The next part of the simulation was to set the Vcc value to a constant of 15V, and use one source with the DC sweep, the graph and Spreadsheet data is shown below, the data in the spreadsheet corresponds to Table 9.2 in the lab manual:

X--Trace 6::[I(R2)]	Y--Trace 6::[I(R2)]		id (mA)
0	0.011929881		11.93
1	0.007480155		7.48
2	0.003397037		3.40
3	0.000752171		0.75
4	4.90004E-11		4.9E-08
5	5.00004E-11		5E-08

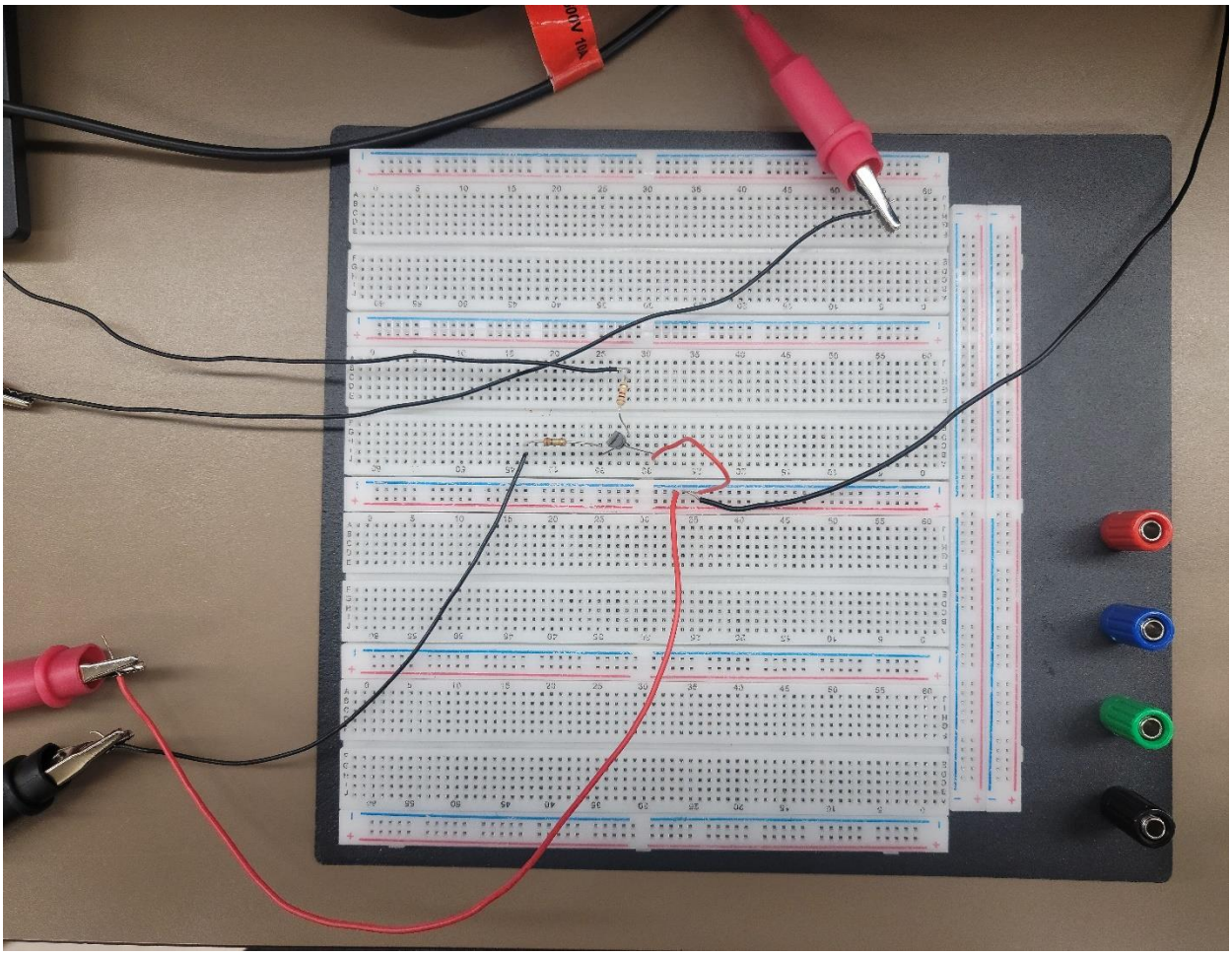


The pinch-off voltage in the digital setup is between 2V to 6V according to the datasheet for the 2N5486 JFET we used.

Gate Source Cutoff Voltage (V_{DS} = 15 Vdc, I_D = 10 nAdc)	2N5484 2N5486	$V_{GS(off)}$	−0.3 −2.0	— —	−3.0 −6.0	Vdc

PART B:

The next part of this laboratory was to design the JFET circuit using hardware components. The setup was completed as shown below:



As already mentioned, the analysis involved reading current values as we adjusted the voltage flowing through the gate. The results of the experiment are recorded in Tables 9.1 and 9.2 below.

Table 9.1 – Experimental.

Drain Characteristic (NPN 2N5486)					
Vcc = Vds	**Vgs = 0**	**Vgs = -1**	**Vgs = -2**	**Vgs = -3**	**Vgs = -4**
	Id	**Id**	**Id**	**Id**	**Id**
0	-0.00mA	-0.00mA	-0.00	-0.00	-0.001
4	3.67mA	3.499	3.26	2.36	0.303
8	7.25mA	6.897	5.92	2.81	0.378
12	10.75mA	9.837	6.82	2.98	0.427
16	13.94mA	11.24	7.02	3.09	0.467
20	16.43mA	11.55	7.03	3.15	0.503
24	16.67mA	11.28	7.06	3.20	0.541

Table 9.2 - Experimental

Vds = 15V						
Vgs	**0**	**-1**	**-2**	**-3**	**-4**	**-5**
Id	13.17mA	11.03	7.01	3.09	0.47	0.00

I was able to determine that the pinch-off voltage is roughly 4.8V in the experimental setup.

CONCLUSION:

There was a very big difference of data values between the digital simulation and experimental analysis. Although, for the first table, some of the values were in the same range, most of them are completely different in comparison. This might be due to margins of error in the experimental setup that may be caused by other hardware-related factors. It may also be that the simulation data is less accurate than experimental data. At this point, I am unable to determine why there is such a big difference in recorded data.