EE 316: Electrical Circuits and Electronic Design Laboratory.

Lab Final

Characteristics of FETs.

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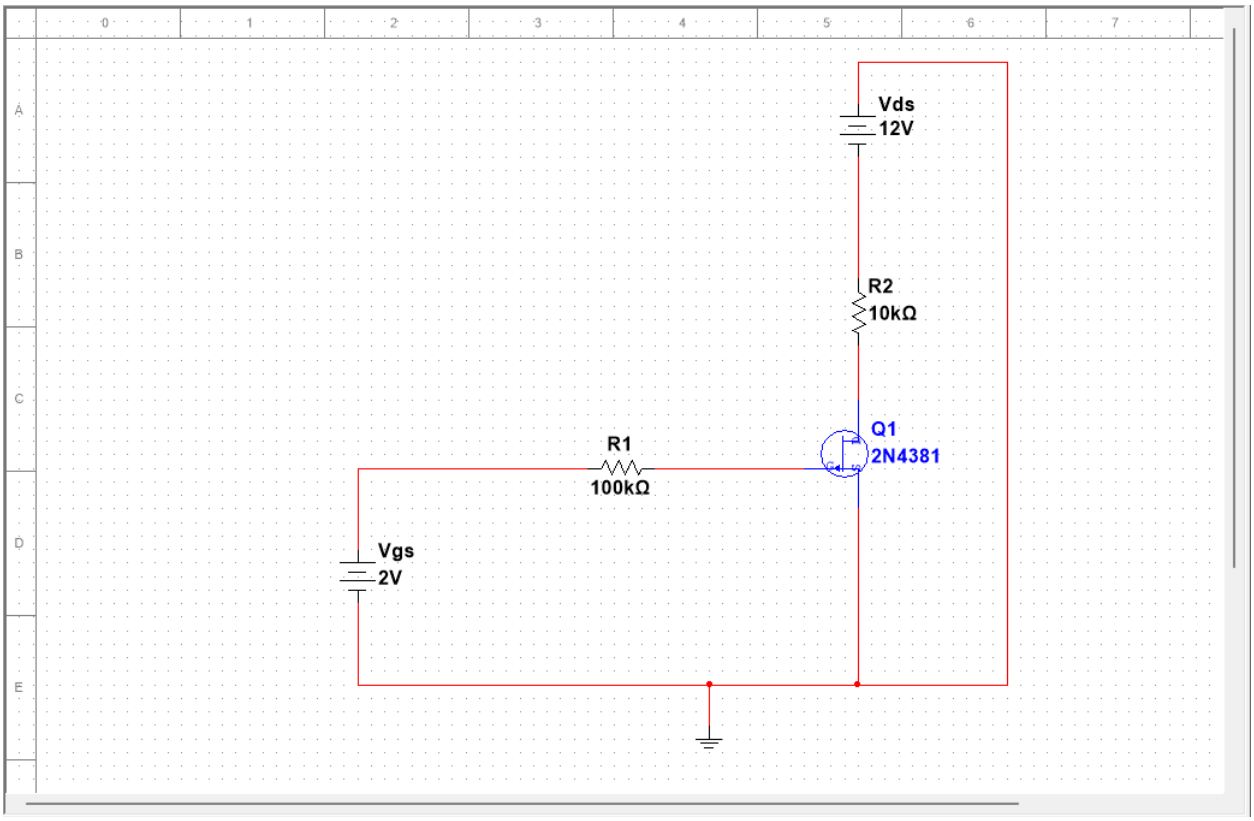
Date of Experiment: 11/28/22.

INTRODUCTION:

For this lab, I picked a transistor that is not available in the Multisim database, so for the simulation, I used the 2N4381 transistor. This lab was similar to Lab 7, where we tested the characteristics of FETs, but this report is not quite comprehensive because of the challenges faced during the design and analysis procedures.

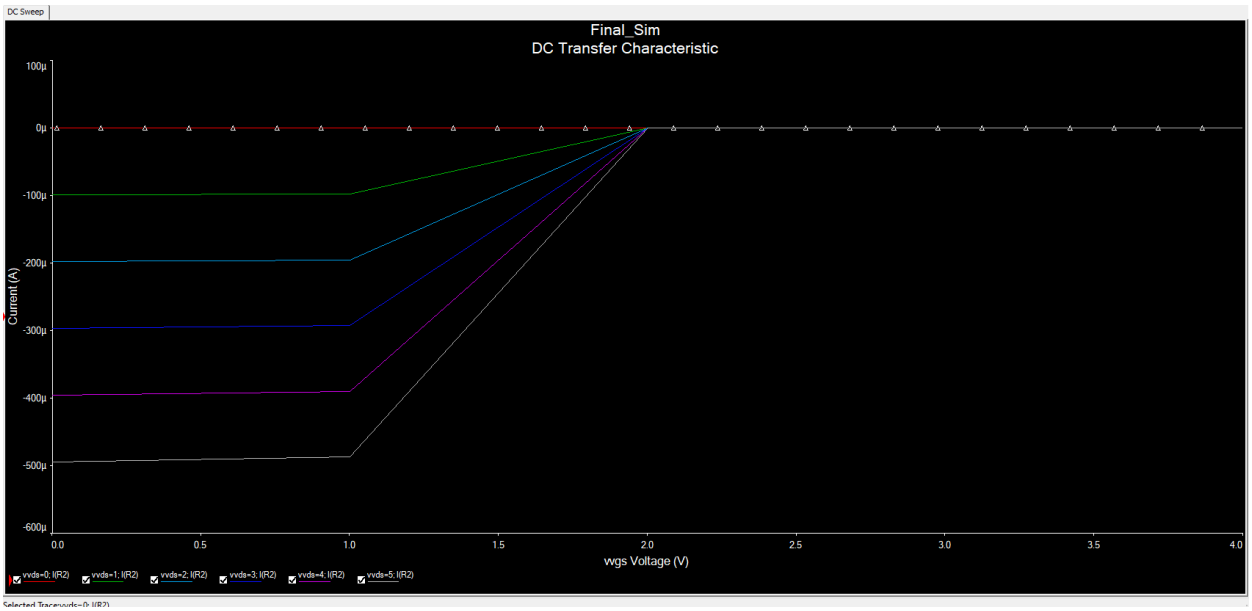
PART 1:

The following simulation circuit was completed in Multisim:



After running simulation in DC sweep, we got the following data and graphs:

X--Trace 1	Y--Trace 1::[vvds=0; I(R2)]	X--Ti	Y--Trace 2::[vvds=1; I(	X--Trace 3	Y--Trace 3::[vvds=2; I	X--Trace 4	Y--Trace 4::[vvds=3; I	X--Trace 5	Y--Trace 5::[vvds=4; I	X--Trace 6	Y--Trace 6::[vvds=5; I(R2)]
0	2.03E-30	0	-9.89E-05	0	-0.0002	0	-0.0003	0	-0.0004	0	-0.00049
1	-9.88E-14	1	-9.77E-05	1	-0.0002	1	-0.00029	1	-0.00039	1	-0.00049
2	-5.92E-12	2	-9.51E-12	2	-1.3E-11	2	-1.7E-11	2	-2E-11	2	-2.3E-11
3	-7.47E-12	3	-1.1E-11	3	-1.4E-11	3	-1.8E-11	3	-2.1E-11	3	-2.5E-11
4	-8.95E-12	4	-1.24E-11	4	-1.6E-11	4	-1.9E-11	4	-2.3E-11	4	-2.6E-11



It is worth mentioning, that after several attempts, I was unable to get a proper transfer characteristics graph. My output looked like an inverted graph of transfer characteristics.

PART 2:

For the second part of this lab, I assembled the components into a breadboard (I have looked at my media gallery and perhaps due to exam pressure I forgot to take a photo of the breadboard assembly). However, I received the following data outputs:

Drain Characteristic (NPN 2N4381)					
Vcc = Vds	**Vgs = 0**	**Vgs = -1**	**Vgs = -2**	**Vgs = -3**	**Vgs = -4**
	Id	**Id**	**Id**	**Id**	**Id**
0	-0.00mA	-0.00mA	-0.00	-0.00	-0.001
4	-3.288mA	-3.352mA	-3.329	-3.326	-3.329
8	-7.299mA	-7.268	-7.334	-7.274	-7.314
12	-11.279mA	-11.300	-11.312	-11.248	-11.346
16	-15.325mA	-15.307	-15.400	-15.301	-15.317
20	-19.421mA	-19.433	-19.403	-19.438	-19.512
24	-23.592mA	-23.595	-23.629	-23.637	-23.655

As in the case of the digital simulation, my data was not convincing, but we also never used the transistor that I picked from the tray for the test, so I was a bit confused by the setup. I also changed my Vds to 15V and got the following, almost similar output value:

Vds = 15V						
Vgs	**0**	**-1**	**-2**	**-3**	**-4**	**-5**
Id (mA)	-14.302	-14.311	-14.313	-14.311	-14.312	-14.314

I ran out of time for this lab final, so I was unfortunately unable to properly design the necessary circuits, but I had gotten a grasp of how to configure NPN transistors from the previous Lab, and hopefully this exam is not a reflection of limited understanding. I think the characteristics were well tested in my previous lab exercise.