3E1203

3E1203

B.Tech. III Sem. (Main) Examination, April/May - 2022

Artificial Intelligence & Data Science

3AID3-04 Digital Electronics

AID, CAI, CS, IT

Time : 3 Hours **Maximum Marks : 70**

Instructions to Candidates:

*Attempt **all ten** questions from **Part A**. All five questions from **Part B** and **three** questions out of **Five** questions from **Part C***

Schematic diagrams must be shown wherever necessary. Any data missing suitably be assumed and stated clearly. Units of quantities used/calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No.205)

PART - A

(Answer should be given up to 25 words only) **(10×2=20)**

(All questions are compulsory)

1. Prove the following Boolean identities using the laws of Boolean algebra: $(A + B)(A + C) = A + BC$.
2. Draw the symbol and truth table for XOR gate and NAND gate?
3. State and prove Demorgan's laws.
4. Why totem pole outputs cannot be connected together.
5. State advantages and disadvantages of TTL.
6. Define combinational logic. Explain the design procedure for combinational circuits.
7. What is edge - triggered flip - flop? Explain the flip-flop excitation tables for RS FF.
8. Define race around condition.
9. Define sequential circuit.
10. Give the comparison between synchronous and Asynchronous counters.

PART - B

(Analytical/Problem solving questions) (5×4=20)

(Attempt all five questions)

1. Verify that the following operations are commutative but not associative
   i. NAND
   ii. NOR
2. Write the expression for Boolean function $F(A,B,C) = \sum m(1,4,5,6,7)$ in standard POS form.
3. What are the advantages of CMOS logic? Explain CMOS inverter with the help of a neat circuit diagram.
4. Implement the following function using a 3 line to 8 line decoder.

   $S(A,B,C) = \sum m(1,2,4,7)$

   $C(A,B,C) = \sum m(3,5,6,7)$
5. Design a mod - 12 Synchronous up counter.

PART - C

(Descriptive/Analytical/Problem solving/Design questions) (3×10=30)

(Attempt any three questions)

1. a. Realize all gates by using :
      i. NAND gate.
      ii. NOR gate.
   b. Prove that :
      i. [AB(C+BD)+AB]C = BC.
      ii. (A+B) (A+B) = AB + AB.
2. Minimize the logic function $Y(A,B,C,D) = \sum m(0,1,2,3,5,7,8,9,11,14)$. Use Karnaugh map. Draw logic circuit for the simplified function.
3. What is meant by Wired - AND connectin of digital ICs? What are its advantages and disadvantages? Draw a circuit of TTL gates with Wired - AND connection and explain its operation.
4. Design a 8 to 1 multiplexer by using the four variable function given by $F(A,B,C,D) = \sum m(0,1,3,4,8,9,15)$.
5. Using D - Flip flops and waveforms explain the working of a 4-bit SISO shift register.