Qn. Set Code-7 (SOT)

Semester: 4th
Programme: B.Tech
Branch: CSE, IT, CSCE, CSSE

SPRING END SEMESTER EXAMINATION-2024

4th Semester B.Tech

COMPUTER ORGANISATION & ARCHITECTURE

CS21002 / CS 2006

(For 2022 & Previous Admitted Batches)

Time: 2 Hours 30 Minutes | Full Marks: 50

Answer any FIVE questions.
Question paper consists of two SECTIONS i.e. A and B.
Section A is compulsory.
Attempt any Four question from Sections B.
The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable and all parts of a question should be answered at one place only.

SECTION-A

1. Answer the following questions: [1 × 10]

(a) What is the function of MAR, IR registers?

(b) Consider a register R1 contains a value 10101010 and R2 contains 11110000.What will be the value of carry and overflow flags after the execution of the instruction?

ADD R1, R2 // R2 is the destination.

(c) How many 64 X 8 RAM chips are needed to provide a memory capacity of 2048 bytes?

(d) The represent $-(18)_{10}$ into IEEE - 754 single precision floating point representation.

(e) *Hardwired Control Unit is relatively inflexible.* Justify the statement.

(f) Write the assembly code to evaluate the following arithmetic expression: X = A / (B - C)

Using a stack organized computer with zero-address operation instructions.

(g) Draw the circuit schematic of DRAM cell and explain the cause of leakage.

(h) Differentiate between micro program counter and program counter.

(i) What is the hit ratio of the cache memory if cache memory access time is 50ns, main memory access time is 25ns and average access time is 62ns?

(j) Differentiate between Memory mapped I/O and I/O mapped I/O.

SECTION-B

2. (a) Discuss the factors that affect the performance of the computer. If a 8GHz computer takes 7 clock cycles for ALU instructions, 11 clock cycles for branch instructions and 6 clock cycles for data transfer instructions. Find the total time taken by the computer to execute the program that consists of 10 ALU instructions, 5 branch instructions and 5 data transfer instructions. [5]

(b) Explain the Relative Auto Increment and Decrement addressing modes. The content of the top of memory stack is 2452. The content of SP is 1258.A two byte call subroutine instruction is located in memory address 1456 followed by address field of 5490 at location 1457. What are the content of PC, SP and top of stack; [5]

i. After call instruction execution

ii. After return from subroutine

3. (a) Write the sequence of control steps required for the instructions given below in single bus CPU organization: [5]

I1: MOV R2, (R3) and I2: Branch<0 L1

(b) A hardwired CPU uses 10 control signals S1 to S10, at various time steps T1 to T5, to implement 4 instructions I1to I4 as shown below: [5]

	T1	T2	T3	T4	T5
I1	S1,S3,S5	S2,S4,S6	S1, S7	S10	S3.S8
I2	S1,S3,S5	S8,S9,S10	S5,S6, S7	S6	S10
I3	S1,S3,S5	S7, S8,S10	S2, S6, S9	S10	S1,S3
I4	S1,S3,S5	S2, S6, S7	S5, S10	S6, S9	S10

Draw the logic circuit for generating control signals S5 and S10 respectively? Why constant 4 in MUX is still present in three bus architecture, though incrementer is present?

4. (a) Explain about the different types of locality of references. [5]

A cache consists of a total of 256 blocks. The main memory contains 16384 blocks, each consisting of 64 words. How many bits are there in each of the TAG, BLOCK and WORD field in case of direct mapping? How many bits are there in each of the TAG, SET, and WORD field in case of 4-way set-associative mapping?

(b) Difference between SRAM and DRAM. Organize a 2MX32 memory module using 512KX8 static memory chip. [5]

5. (a) Write the floating point presentation in memory according to IEEE standard with diagram. Divide the following using Non-restoring division algorithm 14 ÷ 5. [5]

(b) Write the steps for multiplication according to Booth algorithm with the example to multiply 9 with -4. [5]

6. (a) Explain the importance of interrupt vector in I/O Processing. What is daisy chain method for handling simultaneous interrupt request? [5]

(b) The address bus of a computer has 16 address lines $A_{15\text{-}0}$. If the address assigned to one device is $(7CA4)_{16}$ and the address decoder for the device ignores the lines A_8 and A_9, what are all the addresses to which the device will respond? Distinguish between cycle stealing and burst mode data transfer in DMA. [5]

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