ABV-Indian Institute of Information Technology & Management Gwalior

Minor Exam, February 2024

Digital Electronics (EE-103)

Full Marks: 40 Time: 2 Hours

Read the instruction carefully: Don't write anything in the question paper, if found, strict action will be taken against you. Calculator or any digital gadgets are not allowed. Assume the assumptions if it is required.

1. (a) If X=1, find the value of Z in the logical expression.
   $[X+Z\{Y'+(Z'+XY')\}]\{X'+Z'(X+Y)\}=1$
   (b) The BCD equivalent of $(56)_{10}$
   (c) What is the exact number of Bytes in a 32K Bytes and 64M Bytes.
   (d) Non-weighed codes are .....
   (e) Which of the following gate(s) can be used as an inverter?
   (i) NAND (ii) AND (iii) NOR (iv) X-NOR (v) all of them (vi) None (5)

2. (a) Divide 11001 by 110 up to fraction of five digits if required.
   (b) Subtract 11001 from 1010 using 2's complement method step by step.
   (c) The following statement is true or false; justify the answer from Boolean algebra.
   (A (XOR) B (XOR) C)' = (A (XNOR) B (XNOR) C)
   (d) Reduce the expression using Boolean algebra- AB'C+B+A'C
   (e) Realize the half subtractor with step-by-step expression using Boolean algebra with minimum number of NAND gate and make the circuit diagram for the same. (10)

3. Reduce the following expression using k-map and implement them in minimum number of logic using SOP and POS and realize the expression with minimum number of NAND and NOR Gates. (Assume complement's input are also available during design of circuit diagram)
   $F(A,B,C,D)=\Sigma(9, 10, 12) + d(3,5,6,7,11,13,14,15)$ (8)

4. The inputs of a computer circuit are the 4 bits of the binary number $A_3A_2A_1A_0$. The circuit with minimum hardware requirement is required to produce a 1 if any of the following conditions hold.
   (a) The MSB is a '1' and other bits are a '0'.
   (b) A_2 is a '1' and other bits are a '0'.
   (c) All the four bits are a '0'.
   (d) A_0 is a '1' and other bits are a '0'. (5)

5. Realize the following function $f(A,B,C) = \Sigma(3,5,6,7)$ using minimum size and minimum number of MUX. (5)

6. (i) Write the truth table and realize the full adder using minimum size and minimum number of MUX.
   (ii) Write the truth table and realize the full subtractor using decoder(s). (7)