2023BEG-012

ABV-Indian Institute of Information Technology & Management Gwalior

Major Examination, November 2024

Analog Electronics (EE-204)

Full Marks: 50 Time: 3 Hours

Assume the assumptions if it is required. Assume the devices are in saturation as required.

1. (i) Make the CV characteristics of MOSFET and define the cut-off, linear and saturation region with incorporating all parasitic capacitance. Make a circuit diagram to use the MOSFET as a capacitance.
   (ii) Make the circuit diagram of common source, common gate and common drain topology. Write the difference in table form between common source, common gate and common drain topology in terms of input impedance and output impedance. (3+3)

2. Calculate the gain of the following circuits (Fig. 1 to Fig. 5) with $\lambda = 0$ for Fig. 1, Fig. 4 and Fig. 5 and $\lambda \neq 0$ for Fig. 2 & 3. (10)

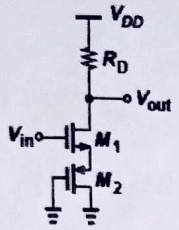

Fig. 1.

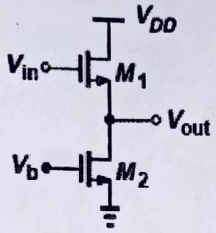

Fig. 2.

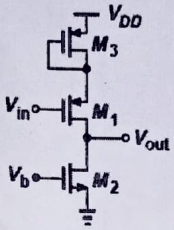

Fig. 3.

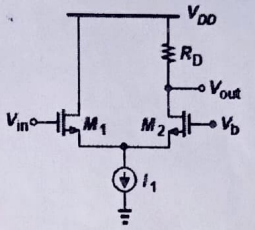

Fig. 4

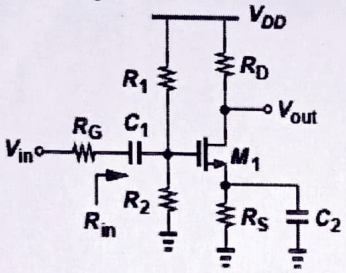

Fig. 5

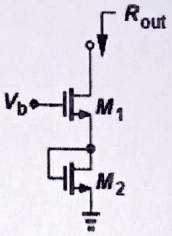

Fig. 6

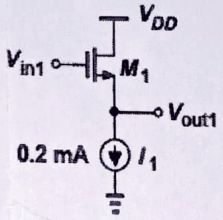

Fig. 7

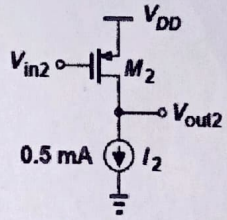

Fig. 8

3. Calculate the output impedance using small signal model for the circuit shown in Fig. 6. (4)
4. Design a current mirror that produces I_1 and I_2 to circuits shown in Fig. 7 and Fig. 8, from a single current source (I_{ref}) of 0.3 mA reference. (4)
5. (i) Make a cascode amplifier by using the N-FET and calculate the gain. What is the advantage of cascode amplifier when compared to common source amplifier.
   (ii) Calculate the I_{COPY} in the circuit shown in Fig. 9. (3+3)

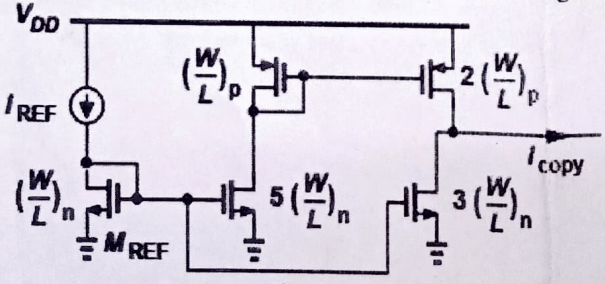

Fig. 9

6. (i) Make a common source amplifier with a load of P-FET in saturation. What will be W/L ratio of load MOSFET and driver MOSFET to achieve the voltage gain of 10. Assume the $\mu_n = 2 \times \mu_p$ and same Tox.

(ii) Make the small signal model for a circuit used in question 6 (i) at high frequency and calculate the voltage gain at high frequency with incorporating the pole(s) and zero(s). (5+5)

7. (i) Make the differential amplifier circuit with resistance as a load (R_L) and consider the output V_{out1} and V_{out2} at drain terminal of each N-FET and an input of $V_{IN/2}$ is applied at gate terminal in one N-FET and $-V_{IN/2}$ is applied at gate terminal in another N-FET. A current source (I_{REF}) with internal resistance of r_o is connected to the source terminal of N-FETs. Calculate the voltage gain of the circuit. Why the source terminal of N-FET is considered as AC virtual ground during AC analysis. Justify it within two lines.

   (ii) Make the circuit for the following.

   1. Make the circuit diagram of common source amplifier with AC input signal is connected at gate terminal of p-FET and load will be n-FET in saturation (diode connected n-FET).
   2. Make the circuit diagram of common source amplifier with AC input signal is connected at gate terminal of n-FET and load will be n-FET in saturation (diode connected n-FET). (6+4)