Reg.No. [redacted]

24042

Velammal College of Engineering and Technology

Viraganoor, Madurai – 625 009
(Autonomous)

B.E./B.Tech. End Semester Examinations November 2024

Third Semester | **Regulation 2021**
Time : 3 Hours | **Max. Marks 100**

21EC201 – Digital Principles and System design
(Common to CSE, ECE and IT branches)

Answer ALL Questions
PART-A (10 x 2 = 20 Marks)

1. Convert the $(11011.011)_2$ to hexadecimal number.
2. Find the Complement of the given expression $\bar{A}B + C\bar{D}$.
3. Draw a logic diagram for Full adder using two half adders.
4. List out the applications of multiplexer.
5. Distinguish between synchronous sequential circuits and asynchronous sequential circuits.
6. Give the design steps for synchronous sequential circuit.
7. List the steps for the design of asynchronous sequential circuit?
8. How can the hazards in combinational circuit be removed?
9. Define FPGA.
10. Determine the number of address lines required for 512 bytes of memory and for a 2kB memory.

Part – B (5 x 13 = 65 Marks)

11. a) Construct the expression, f = Σm (1,4,6,9,10,11,14,15) using K-map to obtain minimum SOP & minimum POS forms and implement it using logic gates.

OR

b) (a)Prove if $\bar{A}B + C\bar{D} = 0, then\ AB + \bar{C}(\bar{A} + \bar{D}) = AB + BD + \bar{B}\bar{D} + \bar{A}\bar{C}D$

(b)Obtain the canonical sum of product form of the function $Y = A + \bar{B}C$ (8 + 5 Marks)

12. a) Design a combinational circuits to compare the 4 bit binary numbers A and B and to generate the outputs A<B, A=B, A>B. Write its truth table and draw the logic diagram.

OR

b) (i)Design a combinational logic using a suitable multiplexer to realize the following Boolean expression $F(A,B,C,D)=AD' +B'C+BC'D'$ (6 + 7 Marks)

(ii)Illustrate the Boolean function $F(A,B,C,D)=\sum m(0,1,3,4,12,14,15)$ using 8 : 1 MUX

13. a) Design a synchronous counter using JK flip flops to count the following sequence: 1-3-15-5-8-2-0-12-6-9.

OR

b) Design a synchronous counter using D flip flops for the given sequence: 000, 001, 010, 011, 100, 101, 110, 111, 000.

14. a) Design a negative edge triggered T flip flop. The circuit has 2 inputs, T(toggle) and C (Clock) and outputs Q and Q'. The output state is complemented if T=1 and the clock changes from 1 to 0. Otherwise under any other input condition, the output Q remains unchanged.

OR

b) Interpret the following Boolean functions using a Hazard free realization

i) $F(W,X,Y,Z)=\Sigma m(0,1,5,6,7,9,11)$ (7 + 6 Marks)

ii) $F(A,B,C,D) = \Sigma m(0,2,6,7,8,10,12)$, Implement the functions using AOI logic.

15. a) Implement:$F_1(A,B,C) = \sum(3,5,6,7)$; $F_2(A,B,C) = \sum(0,2,4,7)$ using PLA.

OR

b) Explain RAM organization and explain how read and write operation is performed in RAM.

Part – C (1 x 15=15 Marks)

16. a) Illustrate a Decade Synchronous Counter using JK flip flop. Draw the timing diagram.

OR

b) Design an asynchronous sequential circuit with two input D and G and with one output Z. Whenever G is '1', input D is transferred to Z. When G is 0, the output does not change for any change in D. Use SR latch for implementation of the circuit.