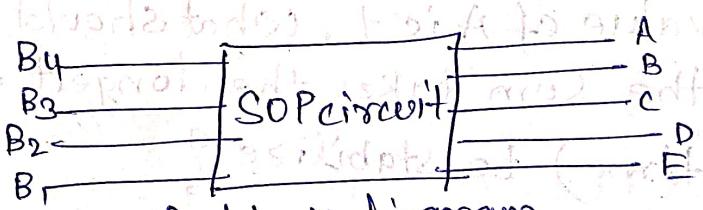
Q.1

Decimal	4 bit binary				BCD output				
	B_4	B_3	B_2	B_1	A	B	C	D	E
0	0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	0	1
2	0	0	1	0	0	0	0	1	0
3	0	0	1	1	0	0	0	1	1
4	0	1	0	0	0	0	1	0	0
5	0	1	0	1	0	0	1	0	1
6	0	1	1	0	0	0	1	1	0
7	0	1	1	1	0	0	1	1	1
8	1	0	0	0	0	1	0	0	0
9	1	0	0	1	0	1	0	0	1
10	1	0	1	0	1	0	0	0	0
11	1	0	1	1	1	0	0	0	1
12	1	1	0	0	1	0	0	1	0
13	1	1	0	1	1	0	0	1	1
14	1	1	1	0	1	0	1	0	0
15	1	1	1	1	1	0	1	0	1



b) block diagram

Ans 2 We consider the last full adder for worst case delay

- Time after which output carry bit becomes available from the last full adder.

= Total no of full adders X carry propogation delay of full adder

= Total no of full adder X {propogation delay of AND gate + propogation delay of OR gate}

= 16 X {15 ns + 10 ns}

= 16 X 25 ns = **400 ns** Ans

- Time after which output Sum bit becomes available from the last full adder

= Time taken for its carry in to become available + Sum propogation delay of full adder

= {Total no of full adder before last full adder * carry propogation delay of full adder} + propogation delay of XOR gate

= {15 x (15ns + 10ns)} + 20ns

= 395ns

Ans.3 if the decimal value of A is 1, what should be the value of B, so that the Sum takes the longest latency (i.e the most time) to stabilize ?

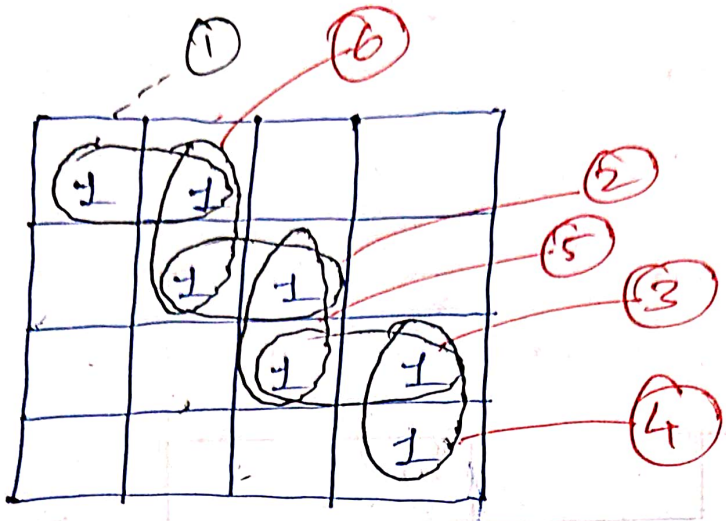
A = 1 (binary : 0000 0001)

- So to maximize latency, we want the carry to propogate through all 8 bits, from MSB to LSB.

So the full B = 1111 1111 → which is -1 in two's complement.

- In 2's compliment, the MSB represents the sign : 0 for +ve and 1 for -ve.
- To find the decimal value of a negative number in 2's compliment, you first need to find the 2's compliment of the given number. Find the 2's compliment of the binary number and then convert to decimal. If the original number's MSB was 1, add a -ve sign.

Ans:4



No of implicants = 7

PI = (1, 2, 3, 4, 5, 6)

EPI = (1, 4)

SPI = (2, 3, 5, 6)

$F = (1) + (2) + (3) + (4)$

OR

$F = (1) + (5) + (6) + (4)$

No of implicants = 7

No of prime implicants (PI) = 6

No of Essential (PI) = 2 (EPI)

No of Redundant PI = 2 (RPI)

No of Selective PI (SPI) = 4

Ans:5

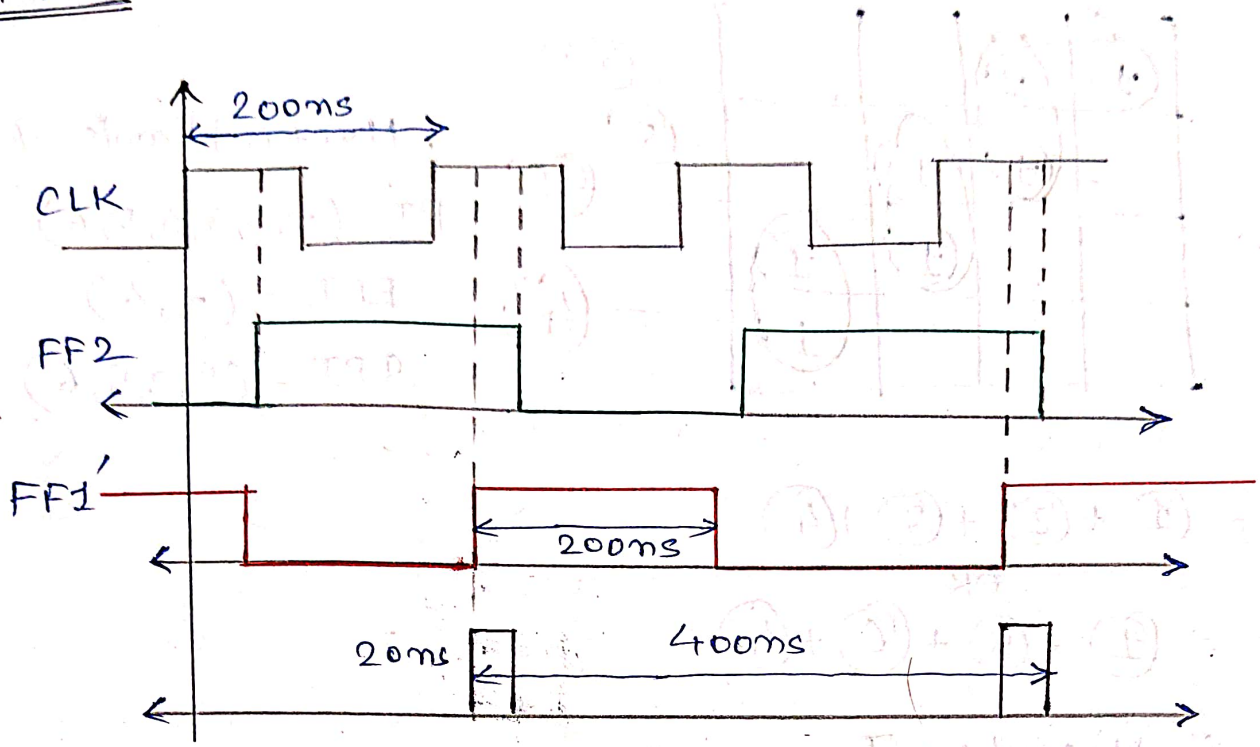
X	Y	Z_n	D	Z_{n+1}
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	1	1
1	0	0	0	0
1	0	1	0	0
1	1	0	1	1
1	1	1	0	0

J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

$X = K$ & $Y = J$

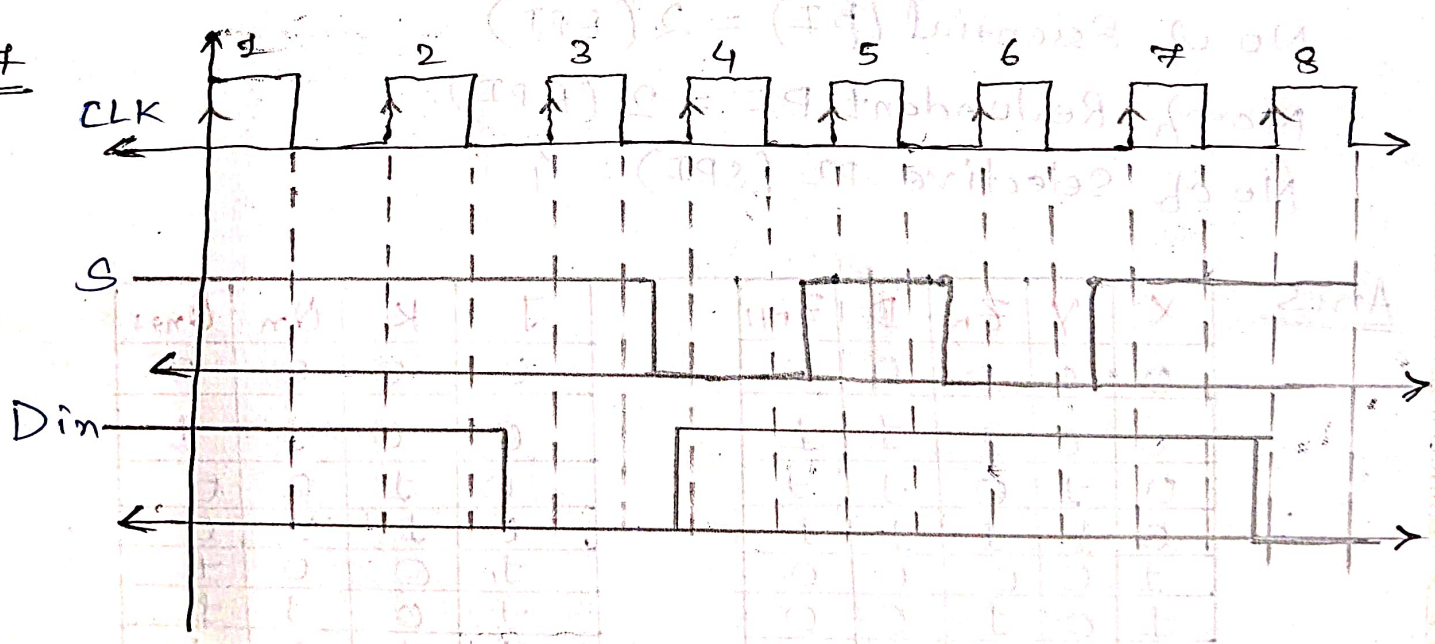
$D = X'Z_n + YZ_n'$

Ans.6



Duty cycle = 5%

Ans.7



Ans.7 (table)

$Y = (Q_2' \oplus 1 \oplus 0)'$

	Signals			Inputs			OUTPUTS			
CLK	DIN	S		D2	D1	Do	Q2	Q1	Q0	Y
1	1	1		1	0	0	1	0	0	1
2	1	1		1	1	0	1	1	0	1
3	0	1		0	1	1	0	1	1	0
4	1	0		0	1	1	0	1	1	0
5	1	1		1	0	1	1	0	1	1
6	1	0								
7	1	1								
8	0	1								