Electronics and Communication Engineering Department
National Institute of Technology Kurukshetra
Digital Design ECPC34

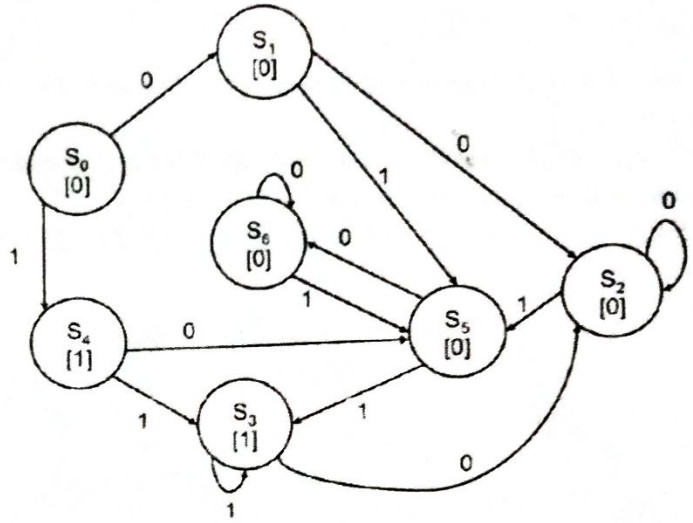
Max. Marka: 50

Time : 3 Hours

Attempt any Five questions

Q.1 Consider the function $F(A,B,C,D)=\sum m(0,2,8,9,10,15)+\sum d(3,4,5,11)$
Use a K-map to write a minimized sum-of-products for F.
Use 8:1 multiplexer and a minimum of additional logic to draw a circuit diagram for F. [5,5]

Q.2 For the state diagram of FSM given below, use Implication Chart method to reduce the number of states. Draw the minimized FSM equivalent to the given FSM [10]



Q.3 A Mealy finite state machine has one input (X) and one output (Z). After each reset, an output Z=l occurs every time an input sequence of 000 or 101 is observed and an output of Z=O occurs whenever any other input sequence is observed. (Sequences may overlap.) [4,2,4]

a) Draw a state diagram for this Mealy machine and give a name to each state (Hint: 5 states suffice)
b) Describe an encoding for each state of this Mealy machine using the "almost" one-hot encoding in which one state is encoded as all 0's. Name each bit of that encoding
c) Write out the sum-of-products expressions for the state transitions and the output of your FSM design.

Q.4 a) Give a expression for the logical function realized by the CMOS circuit in the figure below?
b) Draw circuit diagram of 3-state TTL Buffer
c) Draw diagrams to show logic 1 and logic 0 levels of TTL and CMOS Logic families
d) What are typical Fan-In and Fan-Out values for TTL and CMOS Logic families. What is the procedure to compute Fan-In and Fan-Out. [2.5x4]

(a) Draw the circuit using CMOS transistor for boolean expression $Y = \overline{A+B}$

Q.5 a) Design a combinational circuit whose inputs are two 8-bit unsigned binary integers, X and Y, and a control signal MIN/MAX. The output of the circuit is an 8-bit unsigned binary integer Z such that Z = min(X,Y) if MIN/MAX = 1, and Z = max(X,Y) if MIN/MAX = 0.

b) Write Boolean expressions for outputs A > B and A < B where A and B are inputs of 4-bit comparator [6,4]

OR

Q.5 Write logic equations for an 8-input (I1-I7) priority encoder. Input I7 has the highest priority. Outputs A2–A0 contain the number of the highest-priority asserted input, if any. The IDLE output is asserted if no inputs are asserted.

Obtain the Minimized Function F in POS Form where $F(P,Q,R,S) = \sum m(0,1,2,3,6,8,9,14)$ [5.5]

Q.6 a) Show using the diagram and explain rise time and fall time and propagation delay of CMOS inverter

b) Define Setup and Hold time of Flip-Flop. What happens if they are violated ?

c) Covert the following as directed. [2,2,6]

(4 2 A 5 6. F 1)16 = (?)8; (AF5.2C)16 = (?)4 ; (567.23)8 = (?)16