End-Term Examination
(CBCS)(SUBJECTIVE TYPE)(OffLine)
Course Name:<B.TECH ECE>, Semester:<4>
(May, 2024)

Subject Code: BEC-204 | **Subject: Digital System Design**

Time :3 Hours | Maximum Marks :60

Note:Q. 1 is compulsory. Attempt one question each from the Units I, II, III & IV.

Q1		(2.5*8=20)	
	(a) What are the various Delay Mechanisms in VHDL?		
	(b) What is the role of Library and Entity in VHDL?		
	(c) What is a transition matrix and how is it related to a state Diagram.		
	(d) In the design of digital circuits, what factors should be considered when choosing between pulse mode and fundamental mode of operation.		
	(e)) What is the role of Design for testability in VHDL Designing?		
	(f) List the capabilities and limitations of FSM in digital logic design.		
	(g) Differentiate between ROM, PLA and PAL.		
	(h) What are Finite State Machines? Give some applications of the same.		
	UNIT-I		
Q2	Write the VHDL code for full Subtractor and 4x1 MUX in Data Flow and Behavioral modeling.	(10)	
Q3	Explain the role of test benches in VHDL Design. What are the data types and data objects in VHDL.	(10)	
	UNIT-II		
Q4	Define the concept of secondary state assignment. Describe the steps involved in realizing a state table from a verbal description and provide an example to illustrate your explanation.	(10)	
Q5	(a) Draw the state diagram and state table for D, T, S-R and J-K flip flop. (b) Explain the method (steps) which is used to reduce the flow tables of completely and incompletely specified sequential machines?	(5) (5)	
	UNIT-III		
Q6	What are the race and hazard problems that occur in the asynchronous sequential machines and how can they be mitigated through circuit design techniques.	(10)	
Q7	Differentiate between Mealy and Moore model machines. Draw a state diagram, state table and transition table for a sequence 1010 (non-overlap) by using Mealy model.	(10)	
	UNIT-IV		
Q8	What is RTL synthesis in VHDL and how is it different from behavioral synthesis? What is the role of simulation tools in the EDA process?	(10)	
Q9	(a) Differentiate between FPGA and CPLD logic devices. (b) Design full adder using PLA and PAL logic devices.	(5) (5)	