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Final Examination

Analog Integrated Circuit Design (EC2008)

Instructions: Solve all questions, Draw neat/sketches/circuit diagram,
All Calculations to three decimal places accuracy

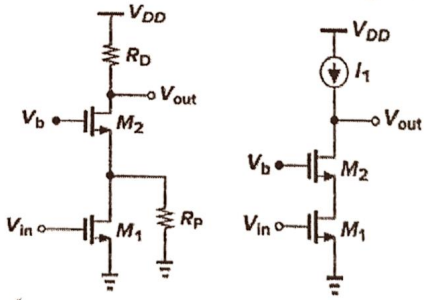
PNV

Max. Marks: 75
Duration: 3 Hours

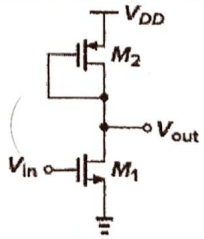
Q1. Write "T" for true and "F" for false in your answer sheet. **10**

a) A MOSFET can operate as a small signal register when its gate and drain are shorted.
b) A MOS device operating in deep triode region behaves as resister and therefore can be used as a load in CG state.
c) In common source stage to achieve a high voltage gain with limited supply voltage, the load impedance must be as large as possible.
d) If R_S equal to infinity, voltage gain of source follower is equal to one.
e) The cascade transistor shields the input device from voltage variation at the output.
f) A differential pair achieves the same gain as CS stage at same cost.
g) A common mode rejection ratio is the ratio of differential gain to common mode gain.
h) Current mirror circuit can be used to amplify the signal.
i) MOSFET can be ideal current source in triode region.
j) The value of $|A_{CM}|$ represents that, even with perfect symmetry the output signal is corrupted by input variation.

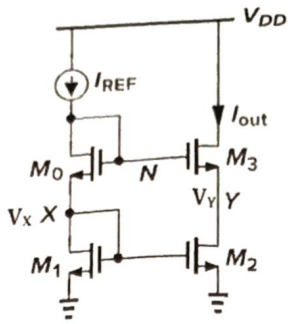
Q2. (a) Calculate the exact voltage gain of the circuit shown in figures below if $\lambda = 0$. **5**



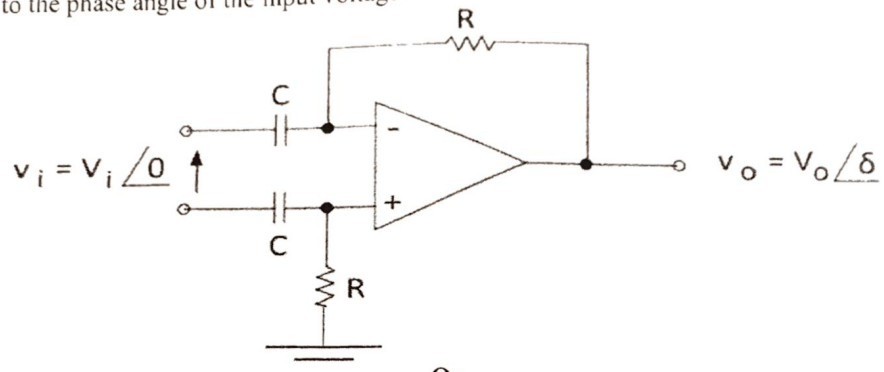
(b) In order to achieve high gain in CS stage with diode connected PMOS device "we need a strong n-MOS input device and a weak load device" is this true? Derive gain equation. What is the sever limitation of this stage diode connected load? Explain with example considering a gain of 10. **6**



(c) In the given Figure, sketch V_X and V_X as a function of I_{REF}. If I_{REF} requires 0.5 V to operate as a current source, what is its maximum value? **4**



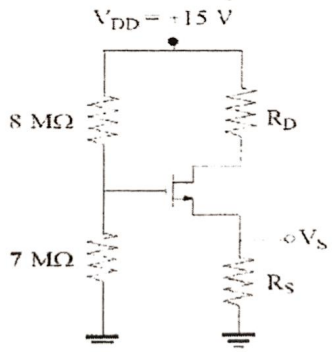
Q3.a Consider the circuit shown in the figure. In this circuit R=1KΩ, and C=1μF. The input voltage is sinusoidal with a frequency of 50Hz, represented as a phasor with magnitude Vi and phase angle 0 radian as shown in the figure. The output voltage is represented as a phasor with magnitude V0 and phase angle δ radian. What is the value of the output phase angle δ (in radian) relative to the phase angle of the input voltage? 5



Or

Q3. (a) Draw the circuit diagram of a monostable multivibrator using an operational amplifier (op-amp), describe its operation, and derive the expression for the time period of the circuit.

(b) In the circuit shown, MOSFET is operating into the saturation region. The characteristic of MOSFET is given by $I_D = {}^1/_2\,(V_{GS} - 1)^2$ mA, where V_{GS} in V. if Vs=5V, then value of Rs in KΩ. 5



Q4. (a) In the circuit of given figure, then drive the expression for V_X and V_Y if $V_{in1} \neq -V_{in2}$ and λ ≠ 0 by using the half circuit concept.

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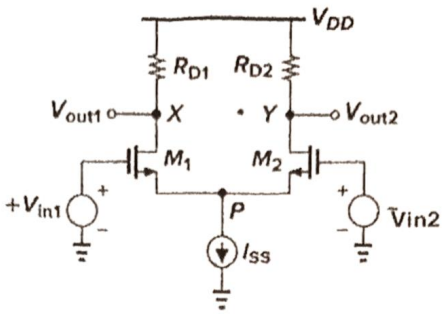
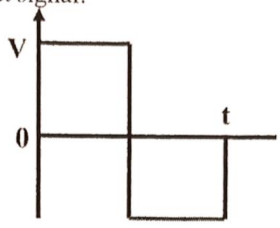
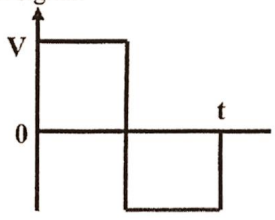


(b) Draw a neat circuit diagram for a differentiator and explain its operation with derivation and what is the limitations of this circuit and describe how these limitations can be minimized. What is the output of the differentiator for following input signal: **8**

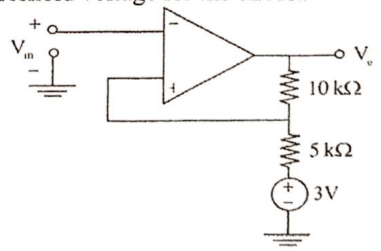


(c) Draw a neat circuit diagram for a integrator and explain its operation with derivation and what is the limitations of this circuit and describe how these limitations can be minimized. What is the output of the differentiator for following input signal: **7**



Q5 What is largest sine wave output voltage (in Volts) possible for frequency f=1MHz when an op-amp has a slew rate is 10V/μs. **5**

Q6. (a) For operational amplifier circuit shown below, the output saturation voltage is $\pm 15V$,then calculate the upper and lower threshold voltage for the circuit. **5**



(b) Explain the following terms **10**

1. Input offset voltage.
2. Input bias current.
3. Thermal drift and error budget.
4. SVRR
5. CMRR