Short Syllabus

BECE102L Digital Systems Design (3-0-0-3)

Digital Logic - Boolean algebra, Gate level minimization; Verilog HDL – Data flow modelling, Test bench; Design of combinational logic circuits – Full Adder, Full Subtractor, Multiplexers, Modeling of Combinational logic circuits using Verilog HDL; Design of Data path circuits - N-bit Parallel Adder/Subtractor; Design of Sequential logic circuits – Shift Registers, state table and state diagrams; Design of FSM - Modeling of FSM using Verilog HDL; Programmable Logic devices - FPGA Generic architecture.

Course Code	Course Title	L	T	P	C
BECE102L	Digital Systems Design	3	0	0	3
Pre-requisite	Nil	Syllabus version			
		1.0			

Course Objectives

1. Provide an understanding of Boolean algebra and logic functions.
2. Develop the knowledge of combinational and sequential logic circuit design.
3. Design and model the data path circuits for digital systems.
4. Establish a strong understanding of programmable logic.
5. Enable the student to design and model the logic circuits using Verilog HDL.

Course Outcome

At the end of the course the student will be able to

1. Optimize the logic functions using and Boolean principles and K-map.
2. Model the Combinational and Sequential logic circuits using Verilog HDL.
3. Design the various combinational logic circuits and data path circuits.
4. Analyze and apply the design aspects of sequential logic circuits.
5. Analyze and apply the design aspects of Finite state machines.
6. Examine the basic architectures of programmable logic devices.

Module:1	Digital Logic	8 hours

Boolean Algebra: Basic definitions, Axiomatic definition of Boolean Algebra, Basic Theorems and Properties of Boolean Algebra, Boolean Functions, Canonical and Standard Forms, Simplification of Boolean functions. Gate-Level Minimization: The Map Method (K-map up to 4 variable), Product of Sums and Sum of Products Simplification, NAND and NOR Implementation. Logic Families: Digital Logic Gates, TTL and CMOS logic families.

Module:2	Verilog HDL	5 hours

Lexical Conventions, Ports and Modules, Operators, Dataflow Modelling, Gate Level Modelling, Behavioural Modeling, Test Bench.

Module:3	Design of Combinational Logic Circuits	8 hours

Design Procedure, Half Adder, Full Adder, Half Subtractor, Full Subtractor, Decoders, Encoders, Multiplexers, De-multiplexers, Parity generator and checker, Applications of Decoder, Multiplexer and De-multiplexer. Modeling of Combinational logic circuits using Verilog HDL.

Module:4	Design of data path circuits	6 hours

N-bit Parallel Adder/Subtractor, Carry Look Ahead Adder, Unsigned Array Multiplier, Booth Multiplier, 4-Bit Magnitude comparator. Modeling of data path circuits using Verilog HDL.

Module:5	Design of Sequential Logic Circuits	8 hours

Latches, Flip-Flops - SR, D, JK & T, Buffer Registers, Shift Registers - SISO, SIPO, PISO, PIPO, Design of synchronous sequential circuits: state table and state diagrams, Design of counters: Modulo-n, Johnson, Ring, Up/Down, Asynchronous counter. Modeling of sequential logic circuits using Verilog HDL.

Module:6	Design of FSM	4 hours

Finite state Machine(FSM):Mealy FSM and Moore FSM , Design Example : Sequence detection, Modeling of FSM using Verilog HDL.

Module:7	Programmable Logic Devices	4 hours

Types of Programmable Logic Devices: PLA, PAL, CPLD, FPGA Generic Architecture.

Module:8	**Contemporary issues**			**2 hours**
			Total Lecture hours:	**45 hours**
Textbook(s)				
1.	M. Morris Mano and Michael D. Ciletti, Digital Design: With an Introduction to the Verilog HDL and System Verilog, 2018, 6th Edition, Pearson Pvt. Ltd.			
Reference Books				
1.	Ming-Bo Lin, Digital Systems Design and Practice: Using Verilog HDL and FPGAs, 2015, 2nd Edition, Create Space Independent Publishing Platform.			
2.	Samir Palnitkar, Verilog HDL: A Guide to Digital Design and Synthesis, 2009, 2nd edition, Prentice Hall of India Pvt. Ltd.			
3.	Stephen Brown and ZvonkoVranesic, Fundamentals of Digital Logic with Verilog Design, 2013, 3rd Edition, McGraw-Hill Higher Education.			
Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and Final Assessment Test				
Recommended by Board of Studies		14-05-2022		
Approved by Academic Council		No. 66	Date	16-06-2022