2023BEE012

ABV-Indian Institute of Information Technology & Management, Gwalior

End Sem Examination

Sub: CoA(CS-202) **Date:** Nov 26, 2024 **Class:** BCS+BEE Sem III

Time: 3 hours **Max. Marks:** 40

Note: Attempt **all** questions in **sequence**. Calculators are **allowed**.

1. What is the difference between a label and an operand in Assembly Language? [3]
2. Give flowchart for the first pass of assembler? [3]
3. A digital computer supports 2-address and 1-address instructions. The size of instruction is 16-bits and address size is 6-bits. If these are 12 2-address instructions then minimum and maximum number of 1-address instructions supported is respectively? [2+2]
4. An instruction is stored at location 500 with its address field at location 501.The address field has the value 400. A processor register R1 contains the number 200. Evaluate the effective address if the addressing mode of the instruction is (i) direct (ii) register indirect (iii) index with R1 as index register [3]
5. An instruction of size 4 Bytes is stored in memory. Which is a branch instruction and it uses PC relative mode. The target for this instruction is stored on address 560. The relative address field of instruction contains value 230. Determine the value of program counter (PC) before the fetch of this instruction. (Assume all the numbers are in decimal). [3]
6. Briefly describe the hardware organization of associative memory. Also discuss the read and write operation for the associative memory. [3+2]
7. How many 128 x 8 RAM chips are needed to provide a memory capacity of 2048 bytes? [2]
8. Assume a memory access to main memory on a cache "miss" takes 30 ns and a memory access to the cache on a cache "hit" takes 3 ns. If 80% of the processor's memory requests result in a cache "hit", what is the average memory access time? [2]
9. Below is a sequence of four binary memory addresses with 16 address bits in the order they are used to reference memory. Assume that the cache is initially empty. For each reference, write down the tag and index bits and indicate whether that reference is a hit or a miss.

   0010 1101 1011 0011

   0000 0110 1111 1100

   0010 1101 1011 1000

   1010 1010 1010 1011 [4]

10. A computer has an 8 GByte memory with 64 bit word sizes. Each block of memory stores 16 words. The computer has a direct-mapped cache of 128 blocks. The computer uses word level addressing. What is the address format? If we change the cache to a 4-way set associative cache, what is the new address format? [2+2]

11. Consider a 4 stage pipeline processor. The number of cycles needed by the four instructions I1, I2, I3 and I4 in stages S1, S2, S3 and S4 is shown below-

	S1	S2	S3	S4
I1	2	1	1	1
I2	1	3	2	2
I3	2	1	1	3
I4	1	2	2	2

What is the number of cycles needed to execute the following loop?

for(i=1 to 2) { I1; I2; I3; I4; } [3]

12. There are 2 designs D1 and D2 for a synchronous pipeline processor. D1 has 5 stage pipeline with execution time of 3 ns, 2 ns, 4 ns, 2 ns and 3 ns. While the design D2 has 8 pipeline stages each with 2 ns execution time. How much time can be saved using design D2 over design D1 for executing 100 instructions? [4]