WALCHAND COLLEGE OF ENGINEERING

(Government Aided Autonomous Institute)
Visharambag, Sangli – 416415

Second Year B.Tech. Computer Science and Engineering
Supplementary ODD SEMESTER, AY 2022-23
Computer Organization and Architecture (6CS204)

Supplementary

PRN: _____

Date: Wednesday, 01/11/2023 Time : 02.00 pm to 05.00 pm

Max Marks: **100**

IMP: Verify that you have received question papers with correct course code, branch etc.

Instructions
a) All questions are compulsory.
b) Writing question number on answer book is compulsory otherwise answers may not be assess
c) Assume suitable data wherever necessary.
d) Figures to the right of question text indicate full marks.
e) Mobile phones, smart gadgets and programmable calculators are strictly prohibited.
f) Except PRN anything else writing on question paper is not allowed.
g) Exchange/Sharing of stationery, calculator etc. not allowed.

Figure on the right of marks indicates course outcomes (Only for faculty use)

		Mar
	Answer the following (*ONE Mark each*)	**20**
a)	Capacity of One Segment in 8086 is ..... kB. A) 16 B) 32 C) 64 D) 128	
b)	Effective Address is ..... Bit value in 8086 A) 16 B) 32 C) 64 D) 128	
c)	Following Addressing Mode is NOT there for 8085 A) Register B) Direct C) Immediate D) Based Indexed	
d)	Segment Register for Source Operand in ***MOV AL, [BX]*** instruction is ..... A) CS B) SS C) DS D) ES	
e)	***RAR*** Instruction affects ..... Flag. A) Sign B) Zero C) Carry D) Auxiliary Carry	
f)	Following is ***Non-Maskable*** *Interrupt* for 8085. A) INTR B) TRAP C) RST 7.5 D) RST 6.5	
g)	After ***TRAP*** *Interrupt* is received, the Program Counter becomes ..... A) 0000H B) 0024H C) 0030H D) 003CH	
h)	Addressing Mode for Source Operand in ***MOV AL, [BX]*** is ..... A) Immediate B) Direct C) Relative D) Register Indirect	
i)	Addressing Mode for Source Operand in ***MOV AL, (BX+SI]*** is ..... A) Immediate B) Direct C) Relative D) Based Indexed	
j)	Addressing Mode for Source Operand in ***MOV AL, [8000H]*** is ..... A) Immediate B) Direct C) Relative D) Based Indexed	
k)	Addressing Mode for Source Operand in ***MOV AL, BL*** is ..... A) Immediate B) Direct C) Relative D) Register	

l) Addressing Mode for Source Operand in ***MOV AL, [SI]*** is .....
A) Immediate B) Direct C) Indexed D) Relative

m) Addressing Mode for Source Operand in ***MOV AL, [BP+DI]*** is .....
A) Immediate B) Direct C) Relative D) Based Indexed

n) After RESET, the ***CS*** Register in 8086 becomes.....
A) 0000H B) FFFFH C) F000H D) Undefined

o) After RESET, the ***SS*** Register in 8086 becomes.....
A) 0000H B) FFFFH C) F000H D) Undefined

p) After RESET, the ***IP*** Register in 8086 becomes.....
A) 0000H B) FFFFH C) F000H D) Undefined

q) After RESET, the ***SP*** Register in 8086 becomes.....
A) 0000H B) FFFFH C) F000H D) Undefined

r) Following is ***Non-Vectored Interrupt*** for 8085.
A) INTR B) TRAP C) RST 7.5 D) RST 6.5

s) After RESET, the ***PC*** Register in 8085 becomes.....
A) 0000H B) FFFFH C) F000H D) Undefined

t) After RESET, the ***SP*** Register in 8085 becomes.....
A) 0000H B) FFFFH C) F000H D) Undefined

Q 2 Explain following 8085 Instructions in detail. (*Including Number of Bytes, Number of Machine Cycles and working of Instruction*)

a) STA 5000H	**b) LHLD 8000H**	**c) ORA C**	**d) DCR M**
e) LDAX B	**f) PUSH H**	**g) POP D**	**h) INX H**
i) MOV M, C	**j) CALL 7000H**	**k) STAX D**	**l) LXI H, 1122H**
m) CMP M	**n) JNC 6000H**	**o) DAD D**	

Q 3 Explain following 8086 Instructions in brief.

a) MOV [BX], AL	**b) MUL BL**	**c) DIV BX**	**d) MOV [BX+DI], AL**
e) AND AL, BL	**f) LOOP**	**g) INC DX**	**h) MOV AL, [4000H]**
i) MOVSB	**j) POP AX**		

Q 4 a) Write an 8085 Assembly Language Program to arrange an array of ***8*** bytes starting from ***8100H*** in ascending order.

b) Write an 8085 Assembly Language Program to add two 8-Bit Numbers stored at ***8000H*** and ***8001H*** and store result of addition at ***8002H*** & ***8003H***.

c) Write an 8085 Assembly Language Program to transfer a Block of *5* Bytes from ***8000H*** onwards to ***9000H*** onwards. 4

d) Write an 8085 Assembly Language Program to multiply two 8-Bit Numbers stored in Memory at ***8000H & 8001H*** and store the result of the multiplication ***8002H & 8003H***. 5

e) State any four differences between 8085 and 8086 Processors. 4

Write Short Notes on the following with suitable Diagram wherever necessary. (***Not more than 25 - 30 Lines***) 16

a) Integer & Floating Point Representation of Numbers

b) Internal Architecture of 8085

c) 8086 Processor Architecture and Features

d) ARM Processor Architecture

..... End of question paper .....