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WALCHAND COLLEGE OF ENGINEERING

(Government Aided Autonomous Institute)
Vishrambag, Sangli – 416415

First YearB.Tech. Group B (Civil, Mech, ELE)
ESE ,ODD SEMESTER,AY 2022-23
Basic Electronics Engineering (6EN101)

ESE

PRN: _____

ay & Date: Wednesday, 01/03/2023 Time: 10.30 am to 12.30 pm

Max Marks: **50**

IMP: Verify that you have received question papers with correct course code, branch etc.

nstructions
a) All questions are compulsory.
b) Writing question number on answer book is compulsory otherwise answers may not be assessed.
c) Assume suitable data wherever necessary.
d) Figures to the right of question text indicate full marks.
e) Mobile phones, smart gadgets and programmable calculators are strictly prohibited.
f) Except PRN anything else writing on question paper is not allowed.
g) Exchange/Sharing of stationery, calculator etc. not allowed.

ext on the right of marks indicates course outcomes (Only for faculty use) Marks

1 Answer ***ANY TEN (10)*** of the following. (***ONE Mark each***) C

i) In a Combinational Circuit, the Output at any time depends on .....
A) Only Present Inputs B) Only Past Outputs
C) Both Present Inputs and Past Outputs D) None of these

ii) Gain of Voltage Follower Configuration of Operational Amplifier is .....
A) Exactly equal to 1 B) Somewhat less than 1 C) Somewhat more than 1
D) None of these

iii) An ideal Operational Amplifier amplifies ..... of two input voltages.
A) difference B) sum C) product D) None of these

iv) "Forbidden" State is there for the following Flip-Flops.
A) Only R-S B) Only J-K C) Only D D) D & J-K

v) Transistor operates in ..... region when it works as an Amplifier. **10**
A) Active B) Cut-Off C) Saturation D) None of these

vi) "Toggle" State is there for the following Flip-Flops.
A) Only R-S B) Only J-K C) Only D D) D & J-K

vii) The differential-mode gain for an Operational Amplifier is .....
A) very high B) very low C) always unity D) About 50

viii) D Flip-Flop has got following States.
A) Toggle B) Forbidden C) Toggle & Forbidden D) None of these

ix) In a Sequential Circuit, the Output at any time depends on .....
A) Only Present Inputs B) Only Past Outputs
C) Both Present Inputs and Past Outputs D) None of these

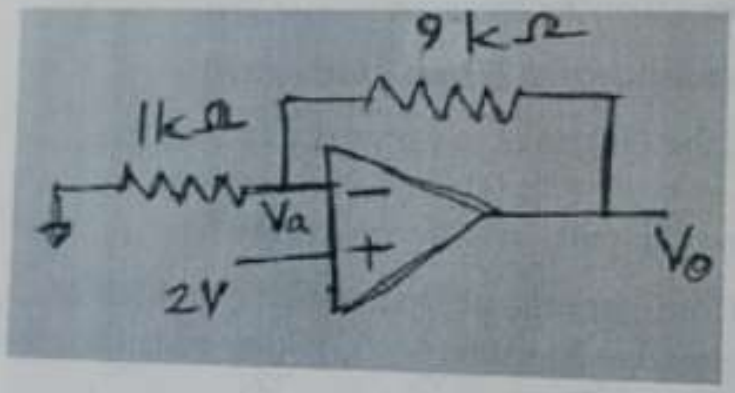
x) The common-mode gain for an Operational Amplifier is .....
A) very high B) very low C) always unity D) About 50

xi) Which of the following is correct statement?
A) Combinational and Sequential Circuits both have Feedback
B) Combinational and Sequential Circuits both have NO Feedback
C) Combinational Circuits have Feedback & Sequential Circuits have NO Feedback
D) Sequential Circuits have Feedback & Combinational Circuits have NO Feedback

xii) Which of the following is correct statement?
A) All Flip-Flops in Synchronous Counters run on Common Clock
B) All Flip-Flops in Asynchronous Counters run on Common Clock
C) All Flip-Flops in Synchronous Counters run on Separate Clock
D) None of these

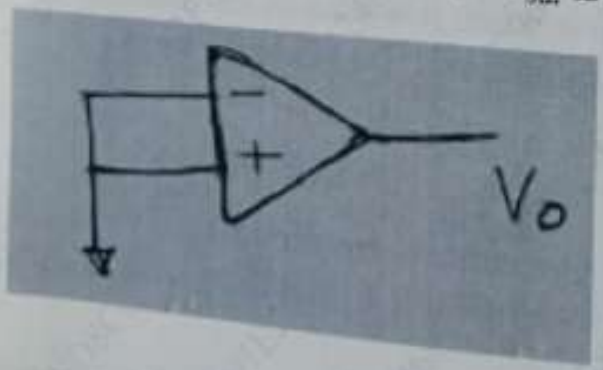
Q2 Answer ***ANY <u>THIRTEEN (13)</u>*** of the following. (***ONE** Mark each*)

i) What will be the Output Voltage V_o in volts for the following circuit if $+/- V_{cc}$ *is* ***+/- 15 volts*** *and* $+/- V_{sat}$ *is* ***+/- 14 volts***.

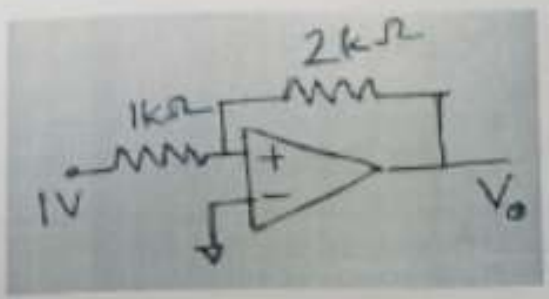


ii) What will be the Output Voltage V_o in volts for the circuit for Q 2(i) above if $+/- V_{cc}$ *is* ***+/- 25 volts*** *and* $+/- V_{sat}$ *is* ***+/- 24 volts***.

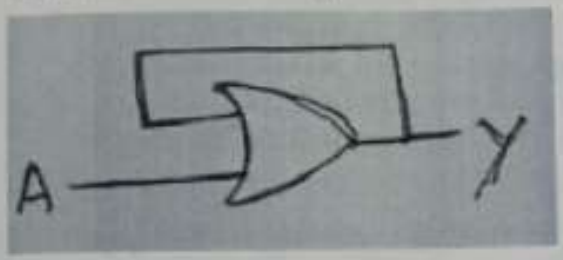
iii) What will be the Output Voltage V_o in volts for the following circuit if $+/- V_{cc}$ *is* ***+/- 15 volts*** *and* $+/- V_{sat}$ *is* ***+/- 14 volts***.



iv) What will be the Output Voltage V_o in volts for the following circuit if $+/- V_{cc}$ *is* ***+/- 15 volts*** *and* $+/- V_{sat}$ *is* ***+/- 14 volts***.



v) What will be Output ***Y*** for the following Sequential Circuit if $A = 1$?



vi) What will be Output ***Y*** for Sequential Circuit in Q 2(v) above if $A = 0$?

vii) For J-K Flip-Flop, we certainly get Output $Q = 1$when J = ... & K = ...

viii) For designing a *MOD-3 UP Counter* how many Flip-Flops are required?

ix) Zener Diode is normally used in …….. Bias mode.

x) For Half Adder when Inputs are $A = 1$ & $B = 1$,Outputs are S =... & C = ...

xi) For designing *MOD-7 DOWN Counter* how many Flip-Flops are needed?

xii) For J-K Flip-Flop, Outputs *toggle* when J = ... & K = ...

xiii) For J-K Flip-Flop, Outputs *maintain last state* when J = ... & K = ...

xiv) For R-S Flip-Flop, Outputs *maintain last state* when R = ... & S = ...

xv) For Half Adder when Inputs are **A = 1** & **B = 0**,Outputs are S=... & C= ...

With a neat Diagram explain the working of following Circuits. (***ANY SIX***)

i) Half Wave Rectifier

ii) Zener Regulator

iii) Astable Multivibrator using 555

iv) RC Phase Shift Oscillator

v) Op-Amp based Voltage Regulator

vi) Common Emitter Amplifier

vii) Unity Gain Buffer (Voltage Follower)

viii) Inverting *Adder*

Q4 Draw a neat Diagram and derive the expression for Output Voltage V_o in terms of Input Voltage V_i of the following circuits using Operational Amplifier.

i) Non-inverting Amplifier *ii)* Inverting Amplifier

Q5 Write Short Notes on the following. (***NOT more than 7-8 Lines each***)

i) Photodiode *ii)* NMOS

..... End of question paper.....