# Walchand College of Engineering, Sangli

*(Government Aided Autonomous Institute)*

**AY 2024 -25**

**Course Information**

| | |
|---|---|
| **Programme** | B. Tech. (Electronics Engineering) |
| **Class, Semester** | Second Year (Electronics Engineering), Sem. III |
| **Course Code** | 7MA204 |
| **Course Name** | Mathematics for Electronics Engineers |
| **Desired Requisites:** | Engineering Mathematics I and Engineering Mathematics II |

| **Teaching Scheme** | | **Examination Scheme (Marks)** | | | |
|---|---|---|---|---|---|
| **Lecture** | 3 Hrs/week | **MSE** | **ISE** | **ESE** | **Total** |
| **Tutorial** | - | 30 | 20 | 50 | 100 |
| | | **Credits: 3** | | | |

**Course Objectives**

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|---|---|
| **1** | To develop Mathematical skills and enhance thinking power of students. |
| **2** | To introduce fundamental concepts of Mathematics and their applications in engineering fields |

**Course Outcomes (CO) with Bloom's Taxonomy Level**

At the end of the course, the students will be able to,

| **CO** | **Course Outcome Statements** | **Bloom's Taxonomy Level** | **Bloom's Taxonomy Descriptor** |
|---|---|---|---|
| **CO1** | **Understand** the solution of Nonlinear Partial differential equation | II | Understanding |
| **CO2** | **Understand** the Fourier transform and its properties | II | Understanding |
| **CO3** | **Construct** Fourier series for any periodic function by Euler's Formulae | III | Applying |
| **CO4** | **Apply** the Method of Laplace transforms to solve initial-value problems for linear differential equations with constant coefficients. | III | Applying |
| **CO5** | **Use** of basic knowledge of Z- transform to solve the problem in Signal system | III | Applying |
| **CO6** | **Apply** Various probability distribution to find the probabilities. | III | Applying |

| **Module** | **Module Contents** | **Hours** |
|---|---|---|
| I | **Laplace Transform and Its Applications**<br>Definition, Transform of Standard functions, Properties, Transform of derivative and Integral, Inverse Laplace Transform, Convolution Theorem, Applications to solve linear differential equation | 7 |
| II | **Fourier Series**<br>Periodic functions , Dirichlet's conditions, Definition , Determination of Fourier coefficients (Euler's formulae), Expansion of functions, Even and odd functions, Change of Interval and functions having arbitrary period, Half range | 7 |

| | | |
|---|---|---|
| | Fourier sine and cosine series. | |
| III | **Partial differential equations and its Application**<br>Introduction, Four Standard Forms: (i) $f(p,q)=0$<br>$(ii)\ f(z,p,q)=0, (iii) f_1(x,p)=f_2(y,q)$ (iv) Lagrange's equation application to one dimensional Heat equation. | 6 |
| IV | **Fourier Transform**<br>Definition, Fourier Sine and Cosine Integral, Fourier sine and Cosine transform, Inverse Fourier sine and Cosine transform, Properties, Parseval's Identity. | 6 |
| V | **Z-Transform**<br>Definition, Z- transform of standard functions, Properties of Z-transform, inverse Z transform, Application to difference equation | 6 |
| VI | **Probability Distribution**<br>Random variable, discrete random variable, continuous random variable, probability mass function, probability density function, Poisson distribution, Normal Distribution, Exponential Distribution. | 7 |

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|---|---|
| | |
| **Textbooks** | |
| 1 | Advanced Engineering Mathematics, Erwin Kreyszig, John Wiley& Sons,Inc,10th Edition,2017. |
| 2 | A Text Book Of Applied Mathematics, Vol I and II , P.N. and J.N. Wartikar, Vidyarthi Griha Prakashan, Pune, 2010. |
| | |
| **References** | |
| 1 | Higher Engineering Mathematics, B.V.Ramanna., Tata McGraw Hill Education Pvt. Ltd, 1st Edition 2007. |
| 2 | Advanced Engineering Mathematics , H.K. Dass, S. Chand and company Ltd., 1st Edition 1988. |
| 3 | An Introduction to probability and Statistics, V.K Rohatgi, Wiley Publication, 2nd Edition 2008 |
| 4 | Higher Engineering Maths, B.S.Grewal, Khanna Publication, 44th Edition, 2017. |
| | |
| **Useful Links** | |
| 1 | https://www.youtube.com/watch?v=lkAvgVUvYvY |
| 2 | https://www.youtube.com/watch?v=c9NibpoQjDk |
| 3 | |
| 4 | |

| **CO-PO Mapping** | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | **Programme Outcomes (PO)** | | | | | | | | | | | | **PSO** | |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 1 | 2 |
| **CO1** | 2 | | | | | | | | | | | | | |
| **CO2** | 2 | | | | | | | | | | | | | |
| **CO3** | 2 | | | | | | | | | | | | | |
| **CO4** | 2 | | | | | | | | | | | | | |
| **CO5** | 2 | | | | | | | | | | | | | |
| **CO6** | 2 | | | | | | | | | | | | | |
| The strength of mapping is to be written as 1: Low, 2: Medium, 3: High<br>Each CO of the course must map to at least one PO. | | | | | | | | | | | | | | |

| Assessment |
| --- |
| The assessment is based on MSE, ISE and ESE.<br>MSE shall be typically on modules 1 to 3.<br>ISE shall be taken throughout the semester in the form of teacher's assessment. Mode of assessment can be field visit, assignments etc. and is expected to map at least one higher order PO.<br>ESE shall be on all modules with around 40% weightage on modules 1 to 3 and 60% weightage on modules 4 to 6.<br>For passing a theory course, Min. 40% marks in (MSE+ISE+ESE) are needed and Min. 40% marks in ESE are needed. (ESE shall be a separate head of passing) |

# Walchand College of Engineering, Sangli

*(Government Aided Autonomous Institute)*

**AY 2024-25**

**Course Information**

| | |
|---|---|
| **Programme** | B. Tech. (Electronics Engineering) |
| **Class, Semester** | Second Year B. Tech., Sem.-III |
| **Course Code** | 7EN201 |
| **Course Name** | Circuit Theory |
| **Desired Requisites:** | Engineering Mathematics, Basic Electrical Engineering |

| **Teaching Scheme** | | **Examination Scheme (Marks)** | | | |
|---|---|---|---|---|---|
| **Lecture** | 3 Hrs/week | **MSE** | **ISE** | **ESE** | **Total** |
| **Tutorial** | - | 30 | 20 | 50 | 100 |
| | | **Credits: 3** | | | |

**Course Objectives**

| | |
|---|---|
| **1.** | On completion of the course, students should be sufficiently familiar with the theoretical structure, formal representation, computational methods, notation, and vocabulary of linear models to be able to apply them to the analysis and design of digital and analog communications and control systems. The students will be able to perform signal analysis with reference to spectrum analysis of deterministic signals. |

**Course Outcomes (CO) with Bloom's Taxonomy Level**

At the end of the course, the students will be able to,

| | | |
|---|---|---|
| **CO1** | Work with basic fundamentals, theorems used in circuit's analysis | Understanding |
| **CO2** | Carry out transient and steady state analysis of different circuits | Analyzing |
| **CO3** | Do analysis and synthesis of circuit characteristics | Evaluating |
| **CO4** | Design a circuit and network | Creating |

| **Module** | **Module Contents** | **Hours** |
|---|---|---|
| I | **Network Analysis Diode Circuits:** Review of fundamentals of circuit components ,complex numbers and phasors in circuits, applications to networks, graphs and trees, node and mesh analysis, matrix representations dual and inverse networks, admittance and impedance, state variable analysis, T-II transformations, bridged-T and lattice networks, Network Theorems: Superposition, Millman, Norton, Thevenin, Maximum power transfer, AC and DC analysis | **8** |
| II | **Transient Response of Circuits:** RL and RC circuits, switching conditions, RLC circuits, Review of Laplace transform, important theorems and properties, application analysis of circuits in time domain, transfer function, Initial Conditions and Solutions to networks | **8** |
| III | **Sinusoidal Steady State Analysis:** The Sinusoidal Forcing Function, Phasor Concept, Average and Effective values of Voltage and Current, Instantaneous and Average Power, Complex Power, Steady State Analysis Using Mesh and Nodal Analysis, Application of Network Theorems to AC Circuits | **6** |

| | | |
|---|---|---|
| V | **Resonance and Magnetically Coupled Circuits:**<br>Series resonance, impedance and phase angle of series resonant circuit, voltage and current in series resonant circuit, effect of resistance on frequency response curve, bandwidth, selectivity and quality factor. Parallel resonance, resonant frequency for tank circuit, and variation of impedance with frequency factor of parallel resonant circuit, reactance curves. Magnetic coupled circuits: Mutual inductance, coefficient of coupling, single tuned and double tuned circuits | **6** |
| V | **Two Port Networks:**<br>Open and short circuit parameters, transmission parameters, hybrid parameters, matrix form of input output relations, interaction of two four terminal networks, unsymmetrical networks, propagation functions, lattice networks, balanced and unbalanced networks, bisection theorem | **8** |
| VI | **Network Functions:**<br>Concept of complex frequency network functions for one port and two port network, poles and zeros of network functions, restrictions on poles and zeros location for driving point function and transfer function. Time domain behavior from poles and zero plot, stability of active network, Characteristics of RLC and LC high pass, low pass, band pass and band stop filter. | **6** |

| **Textbooks** | |
|---|---|
| 1 | Van Valkenburg, "Network Analysis", PHI publication, 3rd Edition, 1983. |
| 2 | Leonard S. Bobrow, "Fundamentals of Electrical Engineering". |
| **References** | |
| 1 | L.P. Huelsman, "Basic Circuit Theory", PHI Publication, 3rd Edition, 2009. |
| 2 | C. K. Alexander, M. N. O. Sadiku, "Electrical Circuits", Tata McGraw-Hill, 2008. |
| 3 | Ravish R Singh, "Network Analysis and Synthesis", Tata McGraw-Hill, 2013 |
| 4 | |
| **Useful Links** | |
| 1 | |

**CO-PO Mapping**

| | Programme Outcomes (PO) | | | | | | | | | | | | PSO | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 1 | 2 |
| **CO1** | 1 | 1 | | | | | | | | | | | | |
| **CO2** | | 1 | 2 | | | | | | | | | | | |
| **CO3** | | 1 | | 2 | | | | | | | | | 3 | |
| **CO4** | | | 1 | 2 | | | | | | | | | 3 | |

The strength of mapping is to be written as 1: Low, 2: Medium, 3: High
Each CO of the course must map to at least one PO.

**Assessment**

The assessment is based on MSE, ISE and ESE.
MSE shall be typically on modules 1 to 3.
ISE shall be taken throughout the semester in the form of teacher's assessment. Mode of assessment can be field visit, assignments etc. and is expected to map at least one higher order PO.
ESE shall be on all modules with around 40% weightage on modules 1 to 3 and 60% weightage on modules 4 to 6.
For passing a theory course, Min. 40% marks in (MSE+ISE+ESE) are needed and Min. 40% marks in ESE are needed. (ESE shall be a separate head of passing)

# Walchand College of Engineering, Sangli

*(Government Aided Autonomous Institute)*

**AY 2024-25**

**Course Information**

| | |
|---|---|
| **Programme** | B. Tech. (Electronics Engineering) |
| **Class, Semester** | Second Year B. Tech., Sem,-III |
| **Course Code** | 7EN202 |
| **Course Name** | Electronic Circuit Analysis and Design |
| **Desired Requisites:** | Analog Electronics |

| **Teaching Scheme** | | **Examination Scheme (Marks)** | | | |
|---|---|---|---|---|---|
| **Lecture** | 3 Hrs/week | **MSE** | **ISE** | **ESE** | **Total** |
| **Tutorial** | - | 30 | 20 | 50 | 100 |
| | | **Credits: 3** | | | |

**Course Objectives**

| | |
|---|---|
| **1** | To **explain** the working of electronic circuits: small signal amplifiers using BJT and MOSFETs, feedback amplifiers and voltage regulators. |
| **2** | To **illustrate** the small signal models used for analysis of electronic circuits. |
| **3** | To **explain** the working of oscillators and multivibrators. |
| **4** | To **illustrate** the methods of designing the electronic circuits using discrete components. |

**Course Outcomes (CO) with Bloom's Taxonomy Level**

At the end of the course, the students will be able to,

| | | |
|---|---|---|
| **CO1** | **Apply** the fundamentals of circuit theory to calculate AC/DC conditions of amplifiers. | Applying |
| **CO2** | **Analyze** the performance of electronic circuits (amplifiers) using small signal models such as hybrid-$\pi$, $r_e$ and $h$-parameter model. | Analyzing |
| **CO3** | **Evaluate** the performance power amplifiers, feedback amplifiers, oscillators and multivibrators. | Evaluating |
| **CO4** | **Design** the electronic circuits (amplifiers) for given specifications using discrete components such as BJT, FET and MOSFET. | Creating |

| **Module** | **Module Contents** | **Hours** |
|---|---|---|
| I | **Small Signal Amplifiers:** Biasing Methods for BJT, JFET and MOSFET amplifiers, DC and AC load line analysis, small signal hybrid-$\pi$ model, small signal equivalent circuit, analysis of common emitter (CE), common collector (emitter follower) amplifier and common base (CB) amplifier; analysis of common emitter (CS), common drain (source follower) amplifier and common gate (CG) amplifier. | **10** |
| II | **Power Amplifiers:** Classification of power amplifiers: class-A, class-B, class-AB, class-C power amplifiers; transformer-coupled amplifiers, class-AB push-pull complementary output stage. | **6** |
| III | **Frequency Response of Amplifiers:** Amplifier frequency response, square wave testing, effect of coupling, bypass, junction and stray capacitances, Low frequency and high frequency response of common emitter (CE) and common source (CS) amplifiers considering high frequency models of BJT and MOSFET. | **5** |

| | | |
|---|---|---|
| IV | **Feedback Amplifiers:**<br>Multistage amplifiers, Darlington pair, feedback concept, amplifiers with negative feedback, effects of negative feedback, four basic feedback topologies; Oscillators: basic principle of oscillation, Phase-Shift oscillator | **7** |
| V | **Oscillators and Multivibrators:**<br>Principle of Positive feedback, Barkhausen criteria for oscillation, RC and LC oscillators; Multivibrators: Astable, Monostable and Bistable Multivibrator, Schmitt trigger circuit. | **8** |
| VI | **Voltage Regulators:**<br>Series and shunt voltage regulators, design of Zener diode voltage regulator. | **4** |

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| **Textbooks** | |
| 1 | D. A. Neamen, "Electronic Circuit Design and Analysis", 3rd Edition, McGraw Hill Education (India) Private Limited, New Delhi, 2007. |
| 2 | D. A. Neamen, "*Microelectronics: Circuit Analysis and Design*", 4th Edition, McGraw Hill Education (India) Private Limited, New Delhi, 2021. |
| 3 | A. S. Sedra and K. C. Smith, "Microelectronic Circuits", 5th Edition, Oxford University Press, 2004. |
| 4 | Allen Mottershead, "*Electronic Devices and Cir*cuits", 2nd Edition, PHI, 1979. |
| | |
| **References** | |
| 1 | R. Boylestad and L. Nashelsky, "*Electronic Devices and Circuit Theory*", 9th Edition, PHI, 2009. |
| 2 | Millman and Halkias, "*Electronic devices and Circuits: An Introduction*", 1st Edition, Tata McGraw Hill, 1991. |
| 3 | Jacob Millman, Herbert Taub, "Pulse, Digital and Switching Waveforms", 2nd Edition, Tata McGraw –Hill Publishing Company Ltd., New Delhi, 2007. |
| | |
| **Useful Links** | |
| 1 | https://nptel.ac.in/courses/108105158 |
| 2 | https://nptel.ac.in/courses/117101106 |
| 3 | https://nptel.ac.in/courses/108101091 |

**CO-PO Mapping**

| | Programme Outcomes (PO) | | | | | | | | | | | | PSO | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 1 | 2 |
| **CO1** | 2 | 3 | | | | | | | | | | | | 2 |
| **CO2** | 2 | 3 | | | | | | | | | | | | 2 |
| **CO3** | | 3 | 3 | | | | | | | | | | | 2 |
| **CO4** | | | 3 | | | | | | | | | | | 2 |

The strength of mapping is to be written as 1: Low, 2: Medium, 3: High
Each CO of the course must map to at least one PO.

**Assessment**

The assessment is based on MSE, ISE and ESE.
MSE shall be typically on modules 1 to 3.
ISE shall be taken throughout the semester in the form of teacher's assessment. Mode of assessment can be field visit, assignments etc. and is expected to map at least one higher order PO.
ESE shall be on all modules with around 40% weightage on modules 1 to 3 and 60% weightage on modules 4 to 6.
For passing a theory course, Min. 40% marks in (MSE+ISE+ESE) are needed and Min. 40% marks in ESE are needed. (ESE shall be a separate head of passing)

# Walchand College of Engineering, Sangli

*(Government Aided Autonomous Institute)*

**AY 2022-23**

**Course Information**

| | |
|---|---|
| **Programme** | B. Tech. (Electronics Engineering) |
| **Class, Semester** | Second Year B. Tech., Sem. III |
| **Course Code** | 7EN203 |
| **Course Name** | Digital System and Microprocessor |
| **Desired Requisites:** | Digital Electronics |

| **Teaching Scheme** | | **Examination Scheme (Marks)** | | | |
|---|---|---|---|---|---|
| **Lecture** | 3 Hrs/week | **MSE** | **ISE** | **ESE** | **Total** |
| **Tutorial** | | 30 | 20 | 50 | 100 |
| | | **Credits: 3** | | | |

**Course Objectives**

| | |
|---|---|
| **1** | To develop the fundamental concepts in digital design. |
| **2** | To make differences between combinational and sequential circuits evident to students. |
| **3** | To motivate students learn implementation of digital circuits using HDL and PLD. |
| **4** | To teach students to develop digital design using VHDL code |

**Course Outcomes (CO) with Bloom's Taxonomy Level**

At the end of the course, the students will be able to,

| | | |
|---|---|---|
| **CO1** | Differentiate between combinational and sequential circuits | Compare |
| **CO2** | Design medium scale combinational and sequential digital circuits | Construct |
| **CO3** | Utilize the architecture and organization of microprocessors with instruction set to design assembly language programs | Apply |
| **CO4** | Differentiate between PAL, PLA, PLD and their architecture. | Compare |

| **Module** | **Module Contents** | **Hours** |
|---|---|---|
| I | **Combinational Logic:** Review of Digital circuits, Code converter, Quine: Mc-cluskey method for logic minimization, Designs using MUX and Demux, Priority Encoder, Priority decoder, Parity Generator and Checker, Carry look ahead adder, ALU , tristate buffers, Hazards,. Hazard removal, | 8 |
| II | **Sequential Logic:** Characteristics equations of F/F,Conversion of any FF to any other FF, , Switch Denouncing, Counters. | 6 |
| III | **Shift register**: shift resistor, Bidirectional shift resistor, universal shift register, Johnson counter, universal shift resistor, Ring Counter. twisted ring counters, Timing parameters. Clock Skew, Clock jitter, Meta stability | 8 |
| IV | **Finite state machines:** State diagram, State assignment, Clocked Synchronous State Machines Design using J-K, D, T FF, State reduction | 8 |
| V | **a)Programmable Logic Devices**: Design Using PLA & PAL, CPLD architectures **b) Logic Families:** TTL,CMOS, and their characteristics | 3 |
| VI | **Microprocessors:** CPU organization, Introduction to 8-bit microprocessor architecture, internal architecture, assembly language programming, instructions. | 6 |

**Textbooks**

| | |
|---|---|
| 1 | "Digital Design", John F. Wakerly,Pearson Education Publication, |
| 2 | "Fundamentals of Digital Circuits", Anand Kumar, PHI, 2ndEdition, 2016. |
| 3 | "Digital Electronics" Mandal S.K , 1st Ediction. Mc-Graw-Hill |
| 4 | "VHDL-Programming by Example" Douglas Perry TMH, 4th Edition |

| | |
|---|---|
| 5 | "Microprocessor Architecture, Programming and Applications with the 8085 " Ramesh Gaonkar, Penram 6th Edition |
| | |
| **References** | |
| 1 | "Modern Digital Design", R..P.Jain, Mc-Graw-Hill |
| 2 | "Digital Logic and Computer Design", Morris Manno, PHI |
| 3 | |
| 4 | |
| | |
| **Useful Links** | |
| 1 | https://nptel.ac.in/courses/108/105/108105113 |
| 2 | https://nptel.ac.in/courses/117/106/117106086 |
| 3 | |
| 4 | |

| **CO-PO Mapping** | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | **Programme Outcomes (PO)** | | | | | | | | | | | | **PSO** | |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 1 | 2 |
| **CO1** | 1 | 1 | | | | | | | | | | | | |
| **CO2** | | 1 | 1 | 2 | | | | | | | | | | 2 |
| **CO3** | | | 1 | 2 | | | | | | | | | | 2 |
| **CO4** | 2 | 2 | | | | | | | | | | | | |
| The strength of mapping is to be written as 1: Low, 2: Medium, 3: High<br>Each CO of the course must map to at least one PO. | | | | | | | | | | | | | | |

| **Assessment** |
|---|
| The assessment is based on MSE, ISE and ESE.<br>MSE shall be typically on modules 1 to 3.<br>ISE shall be taken throughout the semester in the form of teacher's assessment. Mode of assessment can be field visit, assignments etc. and is expected to map at least one higher order PO.<br>ESE shall be on all modules with around 40% weightage on modules 1 to 3 and 60% weightage on modules 4 to 6.<br>For passing a theory course, Min. 40% marks in (MSE+ISE+ESE) are needed and Min. 40% marks in ESE are needed. (ESE shall be a separate head of passing) |

# Walchand College of Engineering, Sangli

*(Government Aided Autonomous Institute)*

**AY 2024-25**

**Course Information**

| | |
|---|---|
| **Programme** | B. Tech. (Electronics Engineering) |
| **Class, Semester** | Second Year B. Tech., Sem. III |
| **Course Code** | 7EN204 |
| **Course Name** | Electronic Instrumentation |
| **Desired Requisites:** | - |

| **Teaching Scheme** | | **Examination Scheme (Marks)** | | | |
|---|---|---|---|---|---|
| **Lecture** | 2 Hrs/week | **MSE** | **ISE** | **ESE** | **Total** |
| **Tutorial** | - | 30 | 20 | 50 | 100 |
| | | **Credits: 2** | | | |

**Course Objectives**

| | |
|---|---|
| **1** | Get an adequate knowledge about selecting particular sensing elements for the measurement of physical parameters. |
| **2** | Discuss the design, calibration and characteristics of various measuring systems/ instruments. |
| **3** | |
| **4** | |

**Course Outcomes (CO) with Bloom's Taxonomy Level**

At the end of the course, the students will be able to,

| | | |
|---|---|---|
| **CO1** | Identify various types of electronic instrument suitable for specific measurement. | Understand |
| **CO2** | Demonstrate different types of signal generators, oscilloscopes, analysers and their construction and operation. | Apply |
| **CO3** | Describe various errors present in measuring instruments. | Understand |
| **CO4** | Analyze the working principle, selection criteria and applications of various transducers used in measurement systems. | Analyze |

| **Module** | **Module Contents** | **Hours** |
|---|---|---|
| I | **Instrumentation of an Engineering System**<br>Instrumentation of an Engineering System: Role of Sensors and Actuators, Human Sensory System, Mechatronic Engineering, Control System Architectures, Instrumentation Process. Component Interconnection and Signal Conditioning: Signal Modification and Conditioning, Impedance Matching Methods, Data Acquisition Hardware, Bridge Circuits, Linearizing Devices, Signal-Modification Hardware. | 4 |
| II | **Performance Specification and Instrument Rating Parameters**<br>Performance Specification, Time-Domain Specifications, Frequency-Domain Specifications, Linearity, Instrument Ratings, Bandwidth Analysis, Aliasing Distortion Due to Signal Sampling, Instrument Error Considerations, Estimation from Measurements, Sensing and Estimation, Least-Squares Estimation. | 4 |
| III | **Analog Sensors and Transducers**<br>Sensors and Transducers, Sensors for Electromechanical Applications, Potentiometer, Variable-Inductance Transducers, Permanent-Magnet and Eddy Current Transducers, Variable-Capacitance Transducers., Piezoelectric Sensors, Strain Gauges, Torque Sensors, Gyroscopic Sensors, Thermo-Fluid Sensors. | 4 |

| | | |
|---|---|---|
| IV | **Digital and Innovative Sensing**<br>Innovative Sensor Technologies, Shaft Encoders, Incremental Optical Encoder, Motion Sensing by Encoder, Encoder Data Acquisition and Processing, Absolute Optical Encoders, Encoder Error, Optical Sensors, Lasers, and Cameras, Miscellaneous Sensor Technologies, Tactile Sensing, MEMS Sensors, Sensor Fusion, Wireless Sensors | 4 |
| V | **Special Oscilloscopes**<br>Delayed Time Base oscilloscopes, Analog storage oscilloscopes, Sampling oscilloscopes, Digital storage oscilloscopes, DSO Applications | 4 |
| VI | **Waveform Analyzing Instruments**<br>Spectrum Analyzer , Digital Spectrum Analyzer | 4 |
| | | |
| **Textbooks** | | |
| 1 | B. P. Lathi and Jeff Kennedy, "Modern Digital and Analog Communication Systems", Third edition, Oxford University Press, 1998, ISBN: 12345678 | |
| 2 | Straus, Joseph Nathan, "Elements of Communication", Third edition, Prentice Hall, 2011, ISBN: 12345678 | |
| 3 | | |
| 4 | | |
| | | |
| **References** | | |
| 1 | Pawlak, Andrzej M.,Sensors and actuators in mechatronics : design and applications, CRC Press, Taylor & Francis Group, 2007. | |
| 2 | Ranganathan S.," Transducer Engineering", Allied Publishers (P) Ltd., 2003 | |
| 3 | | |
| 4 | | |
| | | |
| **Useful Links** | | |
| 1 | | |

**CO-PO Mapping**

| | Programme Outcomes (PO) | | | | | | | | | | | | PSO | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 1 | 2 |
| **CO1** | | | 2 | | | | | | | | | | 2 | |
| **CO2** | | 2 | 3 | | | | | | | | | | | |
| **CO3** | | | 2 | | | | | | | | | | 2 | |
| **CO4** | | | 3 | | | | | | | | | | 3 | |

The strength of mapping is to be written as 1: Low, 2: Medium, 3: High
Each CO of the course must map to at least one PO.

**Assessment**

The assessment is based on MSE, ISE and ESE.
MSE shall be typically on modules 1 to 3.
ISE shall be taken throughout the semester in the form of teacher's assessment. Mode of assessment can be field visit, assignments etc. and is expected to map at least one higher order PO.
ESE shall be on all modules with around 40% weightage on modules 1 to 3 and 60% weightage on modules 4 to 6.
For passing a theory course, Min. 40% marks in (MSE+ISE+ESE) are needed and Min. 40% marks in ESE are needed. (ESE shall be a separate head of passing)

# Walchand College of Engineering, Sangli

*(Government Aided Autonomous Institute)*

**AY 2024-25**

**Course Information**

| | |
|---|---|
| **Programme** | B. Tech. (Electronics Engineering) |
| **Class, Semester** | Second Year B. Tech., Sem.-III |
| **Course Code** | 7EN251 |
| **Course Name** | Electronic Circuit Analysis and Design Lab |
| **Desired Requisites:** | Analog Electronics Lab |

| **Teaching Scheme** | | **Examination Scheme (Marks)** | | | |
|---|---|---|---|---|---|
| **Practical** | 2 Hrs/ Week | **LA1** | **LA2** | **Lab ESE** | **Total** |
| **Interaction** | - | 30 | 30 | 40 | 100 |
| | | **Credits: 1** | | | |

**Course Objectives**

| | |
|---|---|
| **1** | To **explain** the working of electronic circuits like rectifiers, amplifiers (voltage and current), power amplifiers and feedback amplifiers using BJT, FET and MOSFETs. |
| **2** | To **illustrate** the methods of designing the electronic circuits using discrete components. |
| **3** | To **explain** the practical ways of **measuring** AC and DC parameters of electronic circuits like amplifiers, feedback amplifiers for their performance analysis. |
| **4** | To **explain** the working of voltage regulators |

**Course Outcomes (CO) with Bloom's Taxonomy Level**

At the end of the course, the students will be able to,

| | | |
|---|---|---|
| **CO1** | **Demonstrate** the working of electronic circuits: small signal amplifiers built using BJT, JFET and MOSFET, feedback amplifiers and voltage regulators. | Applying |
| **CO2** | **Test** and **analyse** the performance of amplifiers built using BJT, JFET and MOSFET. | Analysing |
| **CO3** | **Evaluate** the performance of small signal, power and feedback amplifiers. | Evaluating |
| **CO4** | **Design** the electronic circuits (amplifiers) for given specifications using discrete components such as BJT, FET and MOSFET. | Creating |

**List of Experiments / Lab Activities/Topics**

**List of Topics(Applicable for Interaction mode ):**

**List of Lab Activities: (Minimum 08 experiments)**

1. Design and analysis of single stage common emitter BJT amplifier. Plot the frequency response of amplifier.
2. Design and analysis of common collector (emitter follower) amplifier.
3. Design and analysis of common source JFET amplifier.
4. Design and analysis of common source MOSFET amplifier.
5. Design and analysis of common drain (source follower) MOSFET amplifier.
6. Study of performance of Darlington pair.
7. Design and analysis of two stage BJT amplifier with negative feedback.
8. Design and analysis of class-A power amplifier using BJT/MOSFET.
9. Design and analysis of class-AB power amplifier.
10. Analyse the performance RC Phase-Shift Oscillator.
11. Analyse the performance astable multivibrator.
12. Design and analysis of Zener diode voltage regulator.
13. Design and analysis of series pass voltage regulator.

**Textbooks**

| | |
|---|---|
| 1 | D. A. Neamen, "*Electronic Circuit Design and Analysis*", 3rd Edition, McGraw Hill Education (India) Private Limited, New Delhi, 2007. |
| 2 | A. S. Sedra and K. C. Smith, "*Microelectronic Circuits*", 5th Edition, Oxford University Press, 2004. |
| 3 | Allen Mottershed , "*Electronic Devices and Cir*cuits", 2nd Edition, PHI, 1979. |
| 4 | D. A. Neamen, "*Microelectronics: Circuit Analysis and Design*", 4th Edition, McGraw Hill Education (India) Private Limited, New Delhi, 2021. |
| | |
| **References** | |
| 1 | R. Boylestad and L. Nashelsky, "*Electronic Devices and Circuit Theory*", 9th Edition, PHI, 2009. |
| 2 | Millman and Halkias, "*Electronic devices and Circuits*", 1st Edition, Tata McGraw Hill, 1991. |
| 3 | Gerald E. Williams, "*Practical Transistor Circuit Design and Analysis*", 1st Edition, Tata McGraw Hill, New Delhi, 1973. |
| 4 | |
| | |
| **Useful Links** | |
| 1 | https://nptel.ac.in/courses/122106025 |
| 2 | https://nptel.ac.in/courses/108105158 |
| 3 | https://nptel.ac.in/courses/117101106 |
| 4 | |

**CO-PO Mapping**

| | Programme Outcomes (PO) | | | | | | | | | | | | PSO | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 1 | 2 |
| **CO1** | 2 | | | | | | | | | 3 | | | | 2 |
| **CO2** | | | | 2 | | | | | | | | | | 2 |
| **CO3** | | | | | 2 | | | | | | | | | 2 |
| **CO4** | | | | 2 | | | | | | | | | | 2 |

The strength of mapping is to be written as 1,2,3; where, 1: Low, 2: Medium, 3: High
Each CO of the course must map to at least one PO, and preferably to only one PO.

**Assessment**

There are three components of lab assessment, LA1, LA2 and Lab ESE.
IMP: Lab ESE is a separate head of passing.(min 40 %), LA1+LA2 should be min 40%

| Assessment | Based on | Conducted by | Typical Schedule | Marks |
|---|---|---|---|---|
| LA1 | Lab activities, attendance, journal | Lab Course Faculty | During Week 1 to Week 8<br>Marks Submission at the end of Week 8 | 30 |
| LA2 | Lab activities, attendance, journal | Lab Course Faculty | During Week 9 to Week 16<br>Marks Submission at the end of Week 16 | 30 |
| Lab ESE | Lab activities, journal/ performance | Lab Course Faculty and External Examiner as applicable | During Week 18 to Week 19<br>Marks Submission at the end of Week 19 | 40 |

Week 1 indicates starting week of a semester. Lab activities/Lab performance shall include performing experiments, mini-project, presentations, drawings, programming, and other suitable activities, as per the nature and requirement of the lab course. The experimental lab shall have typically 8-10 experiments and related activities if any.

# Walchand College of Engineering, Sangli

*(Government Aided Autonomous Institute)*

**AY 2022-23**

**Course Information**

| | |
|---|---|
| **Programme** | B.Tech. (Electronics Engineering) |
| **Class, Semester** | Second Year B. Tech., Sem III |
| **Course Code** | 7EN252 |
| **Course Name** | Digital System and Microprocessor Lab |
| **Desired Requisites:** | Digital Electronics Lab |

| **Teaching Scheme** | | **Examination Scheme (Marks)** | | | |
|---|---|---|---|---|---|
| **Practical** | 2 Hrs/ Week | **LA1** | **LA2** | **Lab ESE** | **Total** |
| **Interaction** | | 30 | 30 | 40 | 100 |
| | | **Credits: 1** | | | |

**Course Objectives**

| | |
|---|---|
| **1** | To explain the importance of the HDL for Digital Design |
| **2** | To demonstrate the complete flow of EDA tool for implementing digital designs |
| **3** | To explain the concepts involved in simulation and synthesis of digital circuits using EDA tool |

**Course Outcomes (CO) with Bloom's Taxonomy Level**

At the end of the course, the students will be able to,

| | | |
|---|---|---|
| **CO1** | Able to write & debug the VHDL code / Assembly language program | Understand |
| **CO2** | Able to implement on kits or on simulator. | Apply |

**List of Experiments / Lab Activities/Topics**

**List of Topics(Applicable for Interaction mode ):**

**List of Experiments:**

1. Experiment 1: Introduction to Xilinx with sample experiment
2. Experiment 2: 1 bit full adder using 1 bit half adder as a component
3. Experiment 3: 4 bit full adder using 1 bit full adder as a component
4. Experiment 4: 1 bit full adder using 8:1 multiplexer as component
5. Experiment 5: 1 bit full adder using 1:8 demux as component
6. Experiment 6: Implementation of 4:1 mux using 2:1 mux as a component
7. Experiment 7: Implementation of demultiplexer IC 74138
8. Experiment 8: 4 bit comparator
9. Experiment 9: Implementation of flip flops
10. Experiment 10: UP counter and DOWN counter
11. Experiment 11: MODN counter
12. Experiment 12: UP-DOWN counter
13. Experiment 13: Shift registers
14. Experiment 14: Universal shift register
15. Experiment 15: Parallel loading shift register
16. Experiment 16: Sequence detector
17. Experiment 17: Creation of project in Quartus-II & download
18. Experiment 18 to 20: Assembly language program

**Textbooks**

| | |
|---|---|
| 1 | John F. Wakerly, "Digital Design", Pearson Education Publication, 5th edition, 2018. |
| 2 | Anand Kumar, "Fundamentals of Digital Circuits", PHI, 2ndEdition, 2009 |

| | |
|---|---|
| 3 | Mandal S.K , “Digital Electronics” Mc-Graw-Hill, 1stEdiction., 2009 |
| 4 | Douglas Perry, “VHDL-Programming by Example” TMH, 4th Edition, 2012 |
| 5 | “Microprocessor Architecture, Programming and Applications with the 8085 ” Ramesh Gaonkar, Penram 6th Edition |
| | |
| **References** | |
| 1 | R.P.Jain, “Modern Digital Design”, Mc-Graw-Hill, 4th edition, 2010 |
| 2 | Morris Manno, “Digital Logic and Computer Design”, Prentice-Hall India, 1st edition 2011 |
| 3 | |
| 4 | |
| | |
| **Useful Links** | |
| 1 | https://nptel.ac.in/courses/108/105/108105113 |
| 2 | https://nptel.ac.in/courses/117/106/117106086 |
| 3 | |
| 4 | |

**CO-PO Mapping**

| | Programme Outcomes (PO) | | | | | | | | | | | | PSO | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 1 | 2 |
| **CO1** | 2 | 2 | | 2 | 2 | | | | | | | | | 1 |
| **CO2** | | 1 | 1 | | | | | | | | | | | 1 |
| | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | |

The strength of mapping is to be written as 1,2,3; where, 1: Low, 2: Medium, 3: High
Each CO of the course must map to at least one PO, and preferably to only one PO.

**Assessment**

There are three components of lab assessment, LA1, LA2 and Lab ESE.
IMP: Lab ESE is a separate head of passing.(min 40 %), LA1+LA2 should be min 40%

| Assessment | Based on | Conducted by | Typical Schedule | Marks |
|---|---|---|---|---|
| LA1 | Lab activities, attendance, journal | Lab Course Faculty | During Week 1 to Week 8<br>Marks Submission at the end of Week 8 | 30 |
| LA2 | Lab activities, attendance, journal | Lab Course Faculty | During Week 9 to Week 16<br>Marks Submission at the end of Week 16 | 30 |
| Lab ESE | Lab activities, journal/ performance | Lab Course Faculty and External Examiner as applicable | During Week 18 to Week 19<br>Marks Submission at the end of Week 19 | 40 |

Week 1 indicates starting week of a semester. Lab activities/Lab performance shall include performing experiments, mini-project, presentations, drawings, programming, and other suitable activities, as per the nature and requirement of the lab course. The experimental lab shall have typically 8-10 experiments and related activities if any.

# Walchand College of Engineering, Sangli

*(Government Aided Autonomous Institute)*

**AY 2024-25**

**Course Information**

| | |
|---|---|
| **Programme** | B. Tech. (Electronics Engineering) |
| **Class, Semester** | Second Year B. Tech., Sem. III |
| **Course Code** | 7EN253 |
| **Course Name** | Data Structure and Algorithms Lab |
| **Desired Requisites:** | Programming basics, C programming |

| **Teaching Scheme** | | **Examination Scheme (Marks)** | | | |
|---|---|---|---|---|---|
| **Practical** | 2 Hrs/ Week | **LA1** | **LA2** | **Lab ESE** | **Total** |
| **Lecture** | 1 Hrs/ Week | 30 | 30 | 40 | 100 |
| | | **Credits: 1** | | | |

**Course Objectives**

| | |
|---|---|
| **1** | To make the students understand different linear data structures and ADTs |
| **2** | To implement data structures by static and dynamic ways as per requirement |
| **3** | To apply different algorithms of searching and sorting techniques |
| **4** | To compare algorithms performance on basis of time complexities |

**Course Outcomes (CO) with Bloom's Taxonomy Level**

At the end of the course, the students will be able to,

| | | |
|---|---|---|
| **CO1** | **Demonstrate need of** different data structures and need of searching and sorting techniques. | Understand |
| **CO2** | **Implement** data structures stack and queue with different approaches | Apply |
| **CO3** | **Implement** searching and sorting algorithms. | Apply |
| **CO4** | **Examine** the complexity of data structures, searching and sorting algorithms | Analyze |

**List of Experiments / Lab Activities/Topics**

**List of Topics to be covered :**

1. Data structures and its need
2. Different types of data structures
3. Static and dynamic approach for implementation of data structures
4. Algorithmic complexity and its significance
5. Need of searching techniques and its types
6. Need of sorting techniques and its types
7. Applications of data structures
8. Implementation of data structures
9. Implement searching algorithms with its complexity comparison
10. Implement sorting algorithms with its complexity comparison
11. Introduction to Graph theory and its applications

| List of Lab Activities: |
|---|
| 1. Programs to revise arrays, structures and pointers<br>2. Program to implement static stack<br>3. Program to implement static queue<br>4. Program to implement singly linked list<br>5. Different operations on singly linked list<br>6. Program to implement dynamic Stack<br>7. Program to implement dynamic queue<br>8. Programs to sort the data with algorithm complexity measure<br>9. Sequential search with algorithm complexity measure<br>10. Binary search with algorithm complexity measure |

| | Textbooks |
|---|---|
| 1 | Richard F. Gilberg, Behrouz A. Forouzan, "Data Structures A pseudo code approach with C". |
| 2 | Horowitz, Sahni, "Fundamentals of Data structures in C", 2nd edition, 2008 |
| 3 | S. Lipschutz, “Data Structures,Schaum's” Outlines Series, Tata McGraw-Hill, 2013 |
| 4 | Ellis Horowitz, S. Sahni, D. Mehta, “Fundamentals of Data Structures in C++”, Galgotia Book Source, New Delhi, 2008 |

| | References |
|---|---|
| 1 | N. B. Venkateshwarlu, E. V. Prasad, “C and Data Structures”, S. Chand and Company, 2010 |
| 2 | Yashavant Kanetkar, “Understanding pointers in C”, BPB Publication, 4th Edition, 2009 |
| 3 | Thomas H. Cormen, Charles E. Leiserson,,”Introduction to Algorithms”, PHI publications , 3rd Edition |
| 4 | |

| | Useful Links |
|---|---|
| 1 | http://www.nptelvideos.in/2012/11/data-structures-and-algorithms.html |
| 2 | https://www.coursera.org/learn/data-structures |
| 3 | http://vlabs.iitb.ac.in/vlabs-dev/labs/mit_bootcamp/dslab/index.php |
| 4 | https://nptel.ac.in/courses/106/106/106106130/ |

| CO-PO Mapping | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Programme Outcomes (PO) | | | | | | | | | | | | PSO | |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 1 | 2 |
| **CO1** | 3 | | | | | | | | | | | | | |
| **CO2** | | 2 | | | | | | | | | | | | 2 |
| **CO3** | | 2 | | | | | | | | | | | | 2 |
| **CO4** | | | 2 | | | | | | 2 | | | | | |
| The strength of mapping is to be written as 1,2,3; where, 1: Low, 2: Medium, 3: High<br>Each CO of the course must map to at least one PO, and preferably to only one PO. | | | | | | | | | | | | | | |

| Assessment | | | | |
|---|---|---|---|---|
| There are three components of lab assessment, LA1, LA2 and Lab ESE.<br>IMP: Lab ESE is a separate head of passing.(min 40 %), LA1+LA2 should be min 40% | | | | |
| **Assessment** | **Based on** | **Conducted by** | **Typical Schedule** | **Marks** |
| LA1 | Lab activities, attendance, journal | Lab Course Faculty | During Week 1 to Week 8<br>Marks Submission at the end of Week 8 | 30 |
| LA2 | Lab activities, attendance, journal | Lab Course Faculty | During Week 9 to Week 16<br>Marks Submission at the end of Week 16 | 30 |
| Lab ESE | Lab activities, journal/ performance | Lab Course Faculty and External Examiner as applicable | During Week 18 to Week 19<br>Marks Submission at the end of Week 19 | 40 |
| Week 1 indicates starting week of a semester. Lab activities/Lab performance shall include performing experiments, mini-project, presentations, drawings, programming, and other suitable activities, as per the nature and requirement of the lab course. The experimental lab shall have typically 8-10 experiments and related activities if any. | | | | |

# Walchand College of Engineering, Sangli

*(Government Aided Autonomous Institute)*

**AY 2024-25**

**Course Information**

| | |
|---|---|
| **Programme** | B.Tech. (Information Technology) |
| **Class, Semester** | Second Year B. Tech., Sem III |
| **Course Code** | 7IK201 |
| **Course Name** | Introduction to Ancient Indian Technology |
| **Desired Requisites:** | General curiosity, maturity expected from adult student. |

| **Teaching Scheme** | | **Examination Scheme (Marks)** | | | |
|---|---|---|---|---|---|
| Lecture | 02 Hrs/week | MSE | ISE | ESE | Total |
| Tutorial | 0 Hrs/week | 30 | 20 | 50 | 100 |
| | | **Credits: 2** | | | |

**Course Objectives**

| | |
|---|---|
| 1 | The course is designed for undergraduate students, interested in learning about the ancient Indian technology which is the hallmark of glorious Indian civilization. |
| 2 | The objective is to emphasize on nature centric aspects of ancient Indian technologies that can be adopted in modern time. |
| 3 | The course is to expose the students to ancient science and technologies which can be adopted for modern technological development. |

**Course Outcomes (CO) with Bloom's Taxonomy Level**

At the end of the course, the students will be able to,

| **CO** | **Course Outcome Statement/s** | **Bloom's Taxonomy Level** | **Bloom's Taxonomy Descriptor** |
|---|---|---|---|
| **CO1** | Name the ancient Indian technological achivments | 1 | Remenbering |
| **CO2** | Comprehend the concept of Indian traditional knowledge and its relevance | 2 | Understanding |
| **CO3** | Explain the Indian contribution to the world at large | 2 | Understanding |
| **CO4** | Judge the ancient Indian technology. | 5 | Evaluating |

| **Module** | **Module Contents** | **Hours** |
|---|---|---|
| I | Introduction: Why are ancient Indian science and technology relevant today? What is science? How is it different from technology? . | 4 |
| II | Philosophy of ancient Indian technology, how is different from modern technology? Ancient Indian Scientific methods. Glimpses of ancient Indian science and technology?. | 4 |
| III | Material technology in ancient India : Mining, Metals and Metallurgy, Iron Making and craftsmanship, Wootz Steel Technology | 5 |
| IV | Extraction of Zinc in ancient India, Glass making, Bead making Techniques, Ceramic Technology. | 4 |
| V | Water Harvesting Technology, Irrigation Systems. Town planning, Building construction, Sanitation from ancient India period. | 5 |
| VI | Agriculture and Textile Technology in context of ancient India i.e Bharat. | 4 |

| Textbooks | |
|---|---|
| 1 | Transcript of the NPTEL course available at https://archive.nptel.ac.in/courses/101/104/101104065/. Title of the course "Introduction To Ancient Indian Technology" by Prof. D.P. Mishra Department of Aerospace Engineering, IIT Kanpur |
| | |

| References | |
|---|---|
| 1 | The NPTEL course available at https://archive.nptel.ac.in/courses/101/104/101104065/. Title of the course "Introduction To Ancient Indian Technology" by Prof. D.P. Mishra Department of Aerospace Engineering, IIT Kanpur |
| | |

| Useful Links | |
|---|---|
| 1 | https://archive.nptel.ac.in/courses/101/104/101104065/ |
| | |

**CO-PO Mapping**

| | Programme Outcomes (PO) | | | | | | | | | | | | PSO | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 1 | 2 |
| **CO1** | 2 | | | | | 1 | | | | | | | | |
| **CO2** | 1 | | | | | 2 | | | | | | 1 | | |
| **CO3** | 1 | | | | | 2 | | | 1 | | | | | |

The strength of mapping is to be written as 1: Low, 2: Medium, 3: High
Each CO of the course must map to at least one PO.

**Assessment**

The assessment is based on MSE, ISE and ESE.
MSE shall be typically on modules 1 to 3.
ISE shall be taken throughout the semester in the form of teacher's assessment. Mode of assessment can be Tests, assignments, oral, seminar etc. and is expected to map at least one higher order PO.
ESE shall be on all modules with around 30 - 40% weightage on modules 1 to 3 and 60 - 70% weightage on modules 4 to 6.
For passing a theory course, Min. 40% marks in (MSE+ISE+ESE) are needed and Min. 40% marks in ESE are needed. (ESE shall be a separate head of passing)