3E1203

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3E1203

B. Tech. III - Sem. (Main / Back) Exam., February - 2023

Artificial Intelligence & Data Science

3AID3 – 04 Digital Electronics

AID, CAI, CS, IT

Time: 3 Hours **Maximum Marks: 70**

Instructions to Candidates:

Attempt all ten questions from Part A, five questions out of seven questions from Part B and three questions out of five from Part C.

Schematic diagrams must be shown wherever necessary. Any data you feel missing may suitably be assumed and stated clearly. Units of quantities used /calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. NIL 2. NIL

PART – A

(Answer should be given up to 25 words only) **[10×2=20]**

All questions are compulsory

Q.1 Write the difference between Latch and Flip-flop.

Q.2 Explain the Excess-3 code.

Q.3 Convert the following numbers –

(i) $(250.5)_{10} = (\ )_2$

(ii) $(101110.01)_2 = (\ )_8$

Q.4 What is Master Slave Flip-flop?

Q.5 What is the operation of SR Flip-flop?

Q.6 Simplify the following expression Y = (A+B)' (A'+B')'.

Q.7 Compare Combinational and Sequential circuits.

Q.8 Which gates are called universal gates? What are its advantages?

Q.9 Mention the expressions for difference and borrow of Full Subtractor.

Q.10 Explain De Morgan's law.

PART – B

(Analytical/Problem solving questions) **[5×4=20]**

Attempt all five questions

Q.1 Implement BCD to 7-segment decoder and cathode type using 4:16 decoder.

Q.2 What is Digital System? Write the characteristics of digital systems.

Q.3 Explain the Half Adder. Implement the full adder using two half adders.

Q.4 What is a shift register? Explain the working of 4-bit universal shift register.

Q.5 Implement the following Boolean function using 8:1 multiplexer $F(A,B,C,D) = \Sigma m (0, 1, 2, 5, 7, 8, 9, 14, 15)$.

Q.6 Discuss the following concerns with Logic Families and Semiconductor Memories -
- (i) Noise margin
- (ii) Propagation delay
- (iii) Fan-in, fan-out

Q.7 Design an octal to binary encoder.

PART – C

(Descriptive/Analytical/Problem Solving/Design Questions) **[3×10=30]**

Attempt any three questions

Q.1 Design of a synchronous BCD Up-Down counter using FFs.

Q.2 Write a short note -
- (i) Encoder
- (ii) Decoder
- (iii) Multiplexer

Q.3 Simplify the Boolean expression using K-map and implement using NAND gates $F(A,B,C,D) = \Sigma m(0, 2, 3, 8, 10, 11, 12, 14)$

Q.4 Write about the following -
- (i) Transistor-transistor Logic (TTL)
- (ii) Emitter-coupled Logic (ECL)
- (iii) CMOS Logic

Q.5 Draw and explain the following using a truth table and logic diagrams -
- (i) J-K Flip-flop
- (ii) D-Flip-flop
- (iii) T-Flip-flop
