ABV-Indian Institute of Information Technology & Management Gwalior

Major Exam, April 2024 Digital Electronics (EE-103)

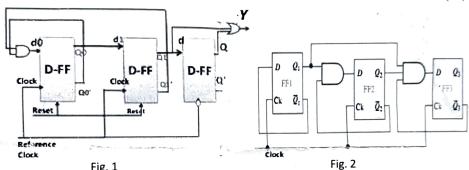
Full Marks: 60

Time: 3 Hours

(5)

Read the instruction carefully: Don't write anything in the question paper, if found, strict action will be taken against you. Calculators non't write anything in the question paper, if found, strict action will be taken against you. be taken against you. Calculator or any digital gadgets are not allowed. Assume the assumptions if it is required. Make the timing waveform with reference to clock.

- 1. Explain the race around condition in four NAND gates based JK Latch. There are two input pins, two output pins and two intermediate nodes J, K, Q, Q', X and Y respectively. Make the table for X, Y, Q and Q' to indicate the change of each node value with change of τ upto 6τ time to explain the race around condition. Assume X, Y, Q and Q' are at '0', '0', '1' and '0' respectively for t<0.
- 2. In the following Fig. 1, two flip-flops are positive edge trigger and one flip-flop is negative edge trigger. Make the timing wave form for Q0, Q1, Q and Y with minimum 8 clock cycle.



- 3. Consider the synchronous counter shown in Fig. 2 and Draw the timing waveform of Q1, Q2, (6)and Q3 with respect to clock.
- 4. Implement the SR flip-flop with the help of D flip-flop. (8)
- 5. Design a type D counter that goes through state 0, 1, 2, 4, 0, ... The undesired (unused) states must always go to (000) on the next clock cycle with minimum number of resources.
- There are two 2x1 MUX and CLK is used as select line. Make the timing waveform for the input, output with respect to clock of the circuit as shown in Fig. 3. What is the functionality of the given block. 1010001

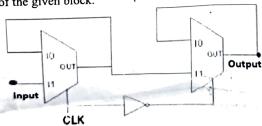


Fig. 3

- 7. Implement the Full subtractor using 2x1 MUX and minimum number of resources.
- Make the circuit and timing diagram for serial-in serial-out shift register to transfer the (5)sequence 101000) How many clock cycle will it take?
- 9. The inputs of a computer circuit are the 4 bits of the binary number A₃A₂A₁A₀. The circuit is required to produce a 1 if and only if any of the following conditions hold.
 - (5)(a) The MSB is a '1'. (b) A2 is a '1'.