(Please write your Enrollment Number) Enrollment No. 02701022022

End-Term Examination
(CBCS)(SUBJECTIVE TYPE)(OffLine)
Course Name: B.Tech ECE, Semester:3rd
(November-December, 2023)

Subject Code: BEC-207	Subject: Digital Electronics
Time :3 Hours	Maximum Marks :60

Note:Q. 1 is compulsory. Attempt one question each from the Units I, II, III & IV.

Q1		**(2.5*8 =20)**	
	(a) Design a Master Slave JK flip- flop with 9 NAND gates.		
	(b) Excess – 3 code is a self-complementary code, Justify		
	(c) Simplify: $Y=\bar{A}C(\overline{\bar{A}BD}) + \bar{A}B\bar{C}\bar{D} + A\bar{B}C$		
	(d) Convert the following expression in canonical POS form. $Y = (A + B)(\bar{B} + C)$		
	(e) Differentiate between ROM, PAL and PLA with help of internal circuitry.		
	(f) State the Excitation Table for JK flip-flop and T flip-flop		
	(g) Draw the logic diagram of 2-to-4 line decoder using NOR gates. Draw the truth table.		
	(h) Compare between the CMOS and TTL logic families		
	UNIT-I		
Q2	Use K-Maps to minimize and express the function in SOP and POS form. Implement both expressions using NAND gates only. $F = \sum m(0, 1, 2, 6, 7, 10, 12, 15) + \sum d(3, 8, 13, 14)$	**(10)**	
Q3	(a) The 74154 is a 4-to-16 decoder. The outputs are active low and there are two gate control signals, $\overline{G1}$ and $\overline{G2}$. The decoder is enabled when $\overline{G1}$ and $\overline{G2}$ are both equal to 0. Realize the following functions using 74154 and logic gates $F_1(W, X, Y, Z) = \sum m(1, 9, 12, 15)$ $F_2(w, X, Y, Z) = \sum m(0, 1, 2, 3, 4, 5, 7, 8, 10, 11, 12, 13)$ (b) An equality detector gives the output Y = 1, if both the inputs A and B are either 1 or 0 (i) Construct the truth table (ii) Write the Boolean expression of Y (iii) Implement the circuit using NAND gates only	**(5+5)**	
	UNIT-II		
Q4	(a) Construct a 3-bit Ring Counter using the JK flip flops. Show the working with the waveforms w.r.t clock pulses. (b) With the help of appropriate waveforms, explain the functioning of MOD-8 Down Ripple Counter using negative edge triggered flip flops.	**(5+5)**	

Q5	(a) Determine the output state of a 4-bit SIPO shift register after 3 clock pulses if the serial in terminal is held HIGH and the initial contents of the shift register is 1001. (b) Design a self-correcting synchronous counter with the following binary sequence: 0, 1, 3, 5, 7 and repeat using T flip-flops.	(4+6)	
	UNIT-III		
Q6	(a) What is a flip flop? How is an SR flip flop realized employing (i) NOR gates (ii) NAND gates (b) Implement an 8:1 MUX using two 4:1 MUX(s) use block diagrams.	(6+4)	
Q7	(a) A 5-bit DAC produces $V_0 = 1.4$ V for a digital input of 00111. Find (i) its % resolution, (ii) step size (ΔV), (iii) V_0 for digital input of 11000 and (iv) full scale analog voltage (b)State the various performance characteristics of ADC.	(8+2)	
	UNIT-IV		
Q8	A combinational circuit is defined by the following function. $F_1 (ABC) = \sum m (4, 5, 7)$ $F_2 (ABC) = \sum m (3, 5, 7)$ Implement this circuit with a PLA having 3 inputs, 3 product terms and 2 outputs.	(10)	
Q9	Write a short Note on (i) Content Addressable Memory (ii) Dual-Slope ADC **OR** Successive-Approximation ADC	(5+5)	