Update on Ara

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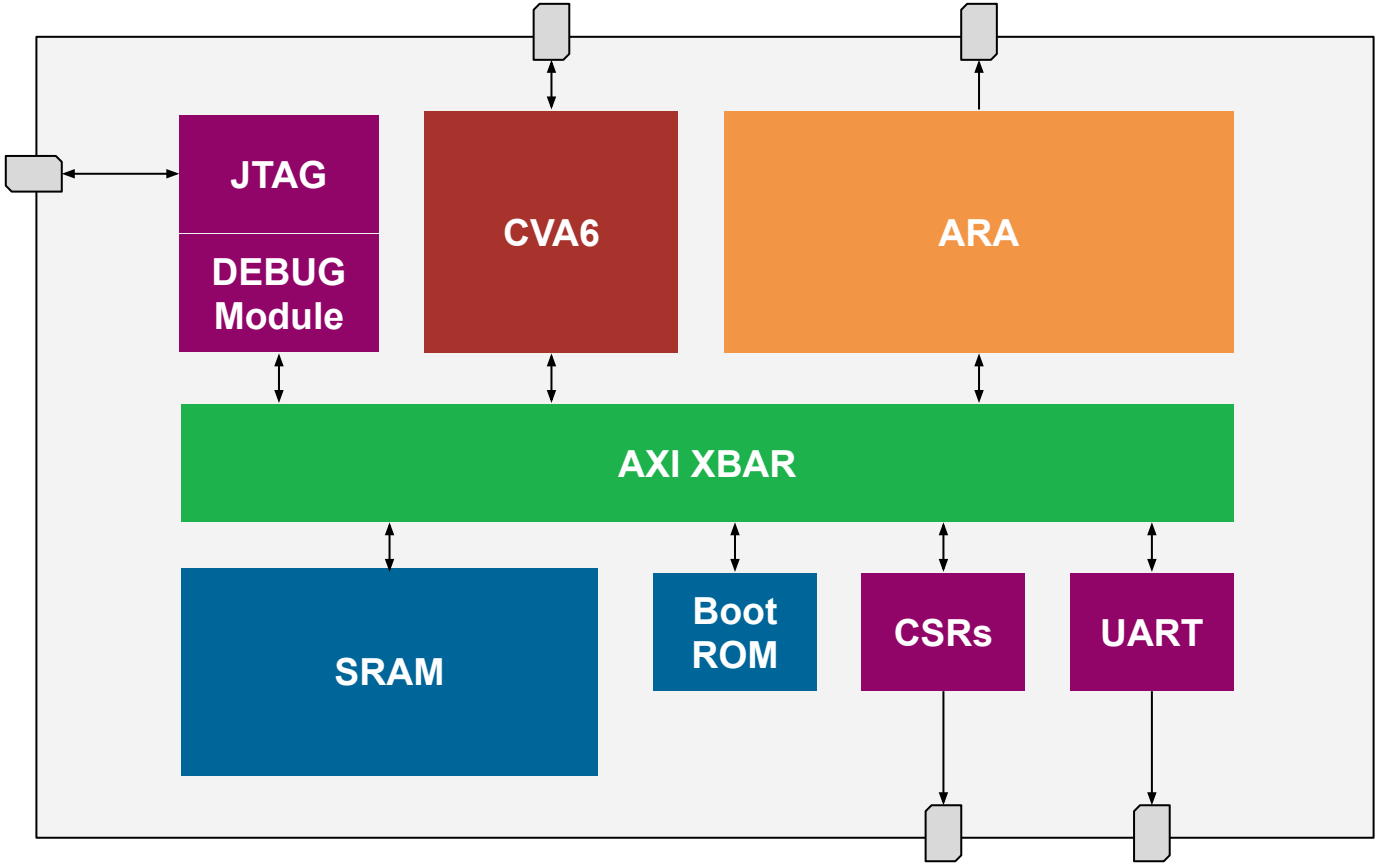
Yun Chip

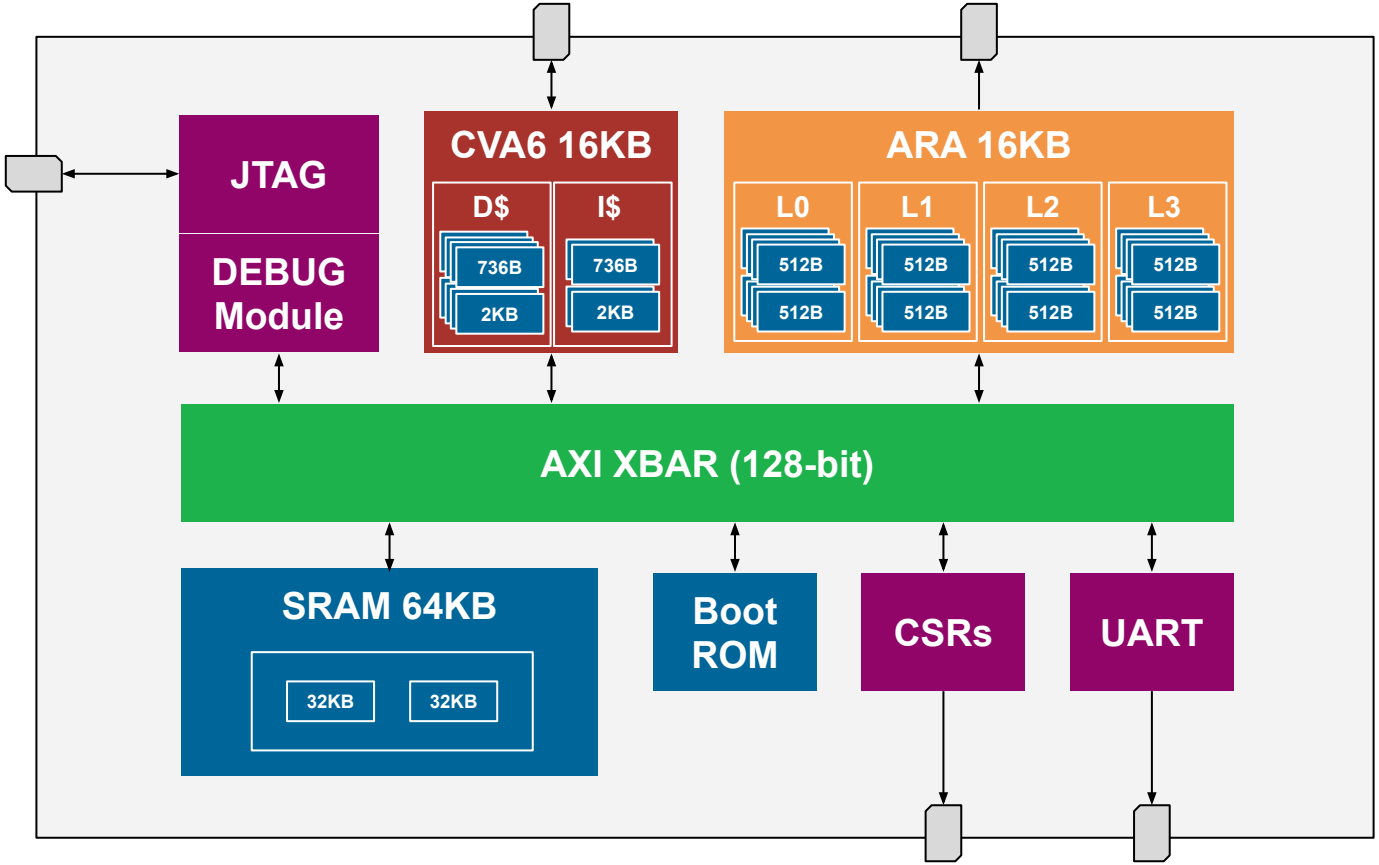
The first Tapeout of Ara (tsmc65)

- Ara (RISC-V vector accelerator)
- Ariane
- JTAG + Debug Module
- 64 KiB SRAM
- BootROM
- UART (tx only)
- CSRs
- Status from Ara, Ariane, CSRs

Yun - Architectural Overview



Yun - Detailed Overview

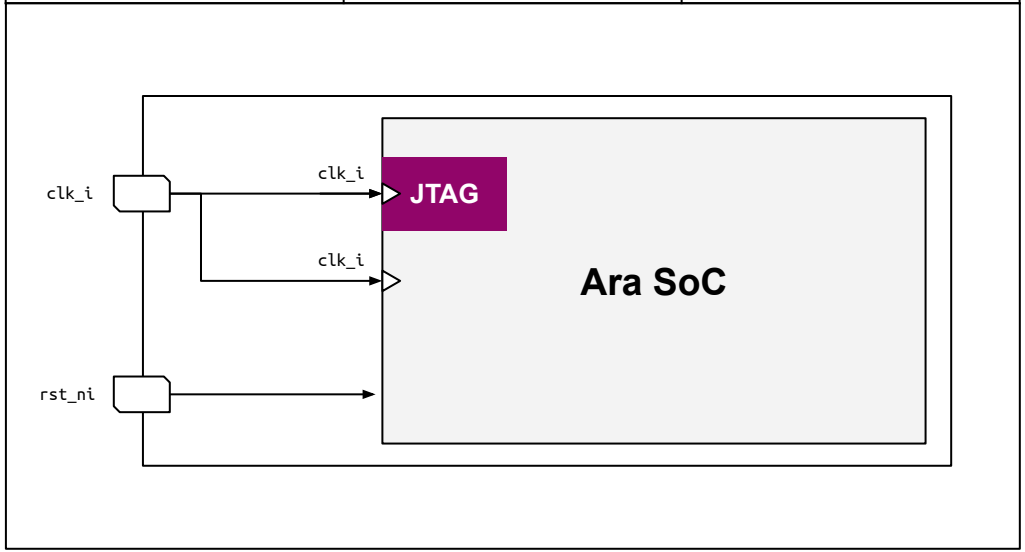


Yun - Clock Domain

YUN

- **Single clock domain**
- **Target frequency:** 250 MHz
- **Two views**:
  - Functional
  - Test (scan chain)

Frequency (MHz)	**Functional view**	**Test view**
clk_i	250	50



Yun - Verification Strategy (RTL + Post Synthesis)

- **Ariane stuck** at `wfi in the BootROM`
- **Load program** binary **through JTAG** into SRAM
- When loading is over, Debug Module **fires** an **interrupt**
  - **Alternatively**: **external wake-up** for Ariane (dedicated PIN)
- **Ariane jumps to** the SRAM **program**

- Several debug **probes**:
  - Is **Ariane idle**?
  - Is **Ara idle**?
  - Are **Ara** internal **sub-modules idle**? (VLU, VSU, VSLD, VALU, VMFPU, ...)
- **Delimitate kernel** with dedicated PIN toggling (**special CSR bit**)
- Dedicated **PIN** to detect **EOC** (End Of Computation)
- Dedicated **PIN** to read the **return value**

- **UART TX** to implement printf