

Update on Ara

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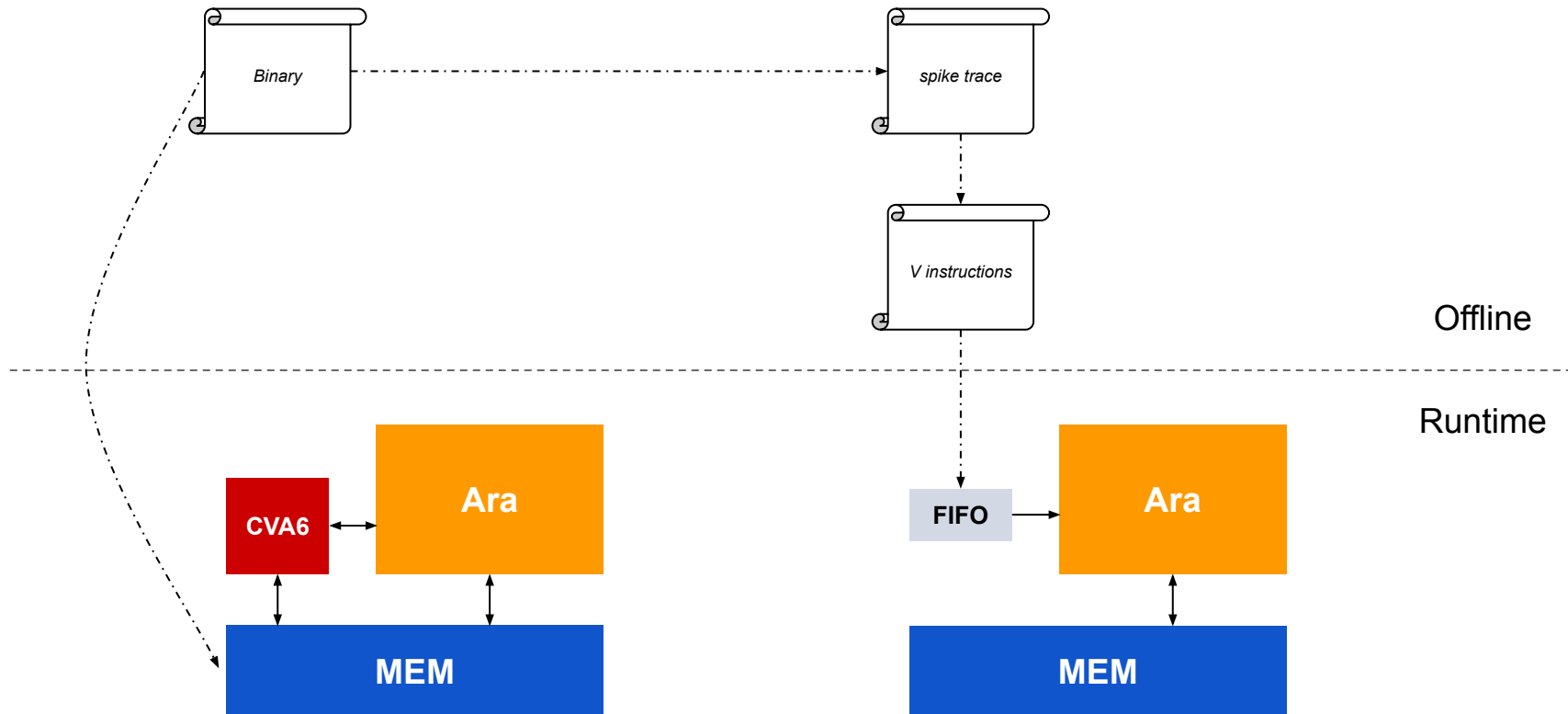
Summary

- **SW** optimization
 - Ideal dispatcher
 - Bug fixes
- **HW** optimization
 - Timing

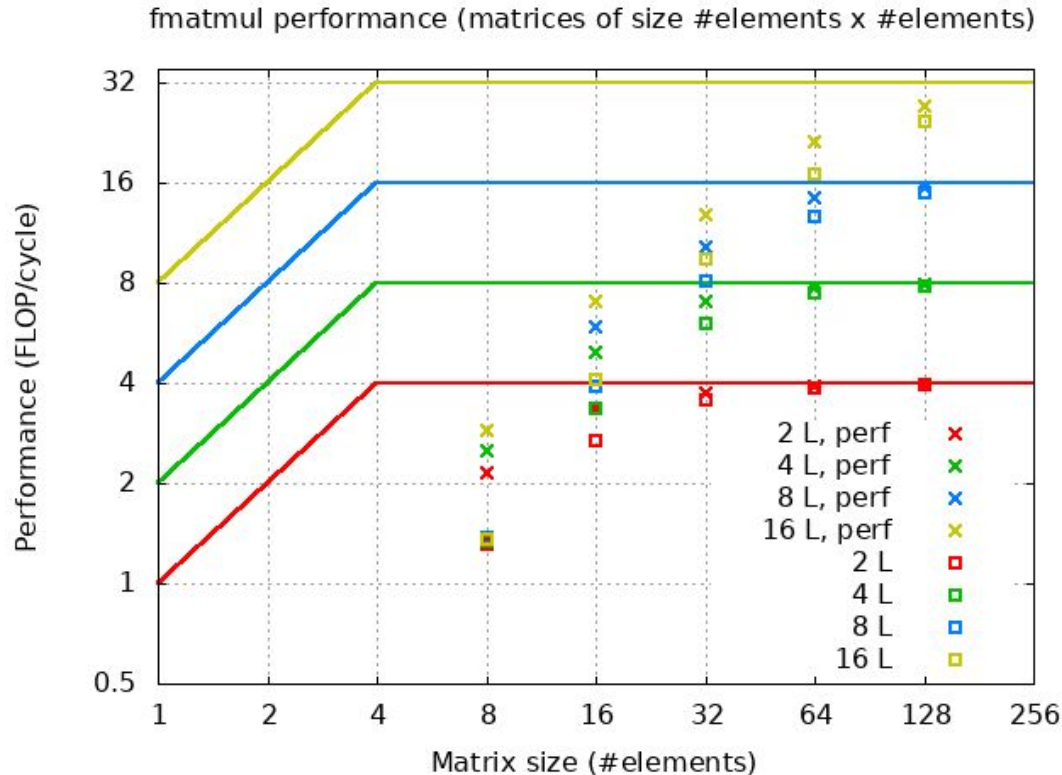
Ideal dispatcher

- Performance depends on:
 - CVA6
 - Ara
 - (Scalar memory accesses)
 - (Vector memory accesses)
- What does limit performance?
- Decouple the problem:
 - Make CVA6 an “ideal” dispatcher
- Now the performance depends only on Ara

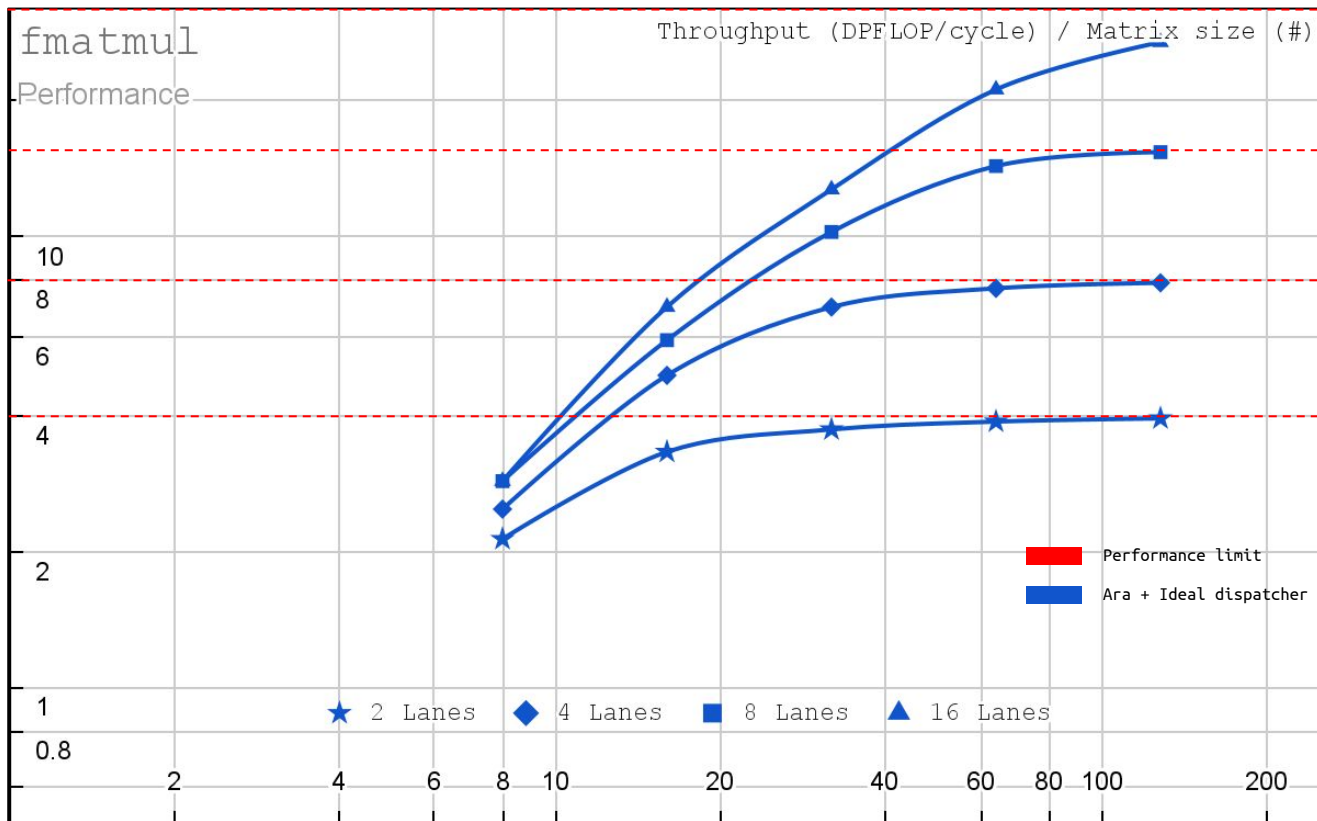
Ideal dispatcher



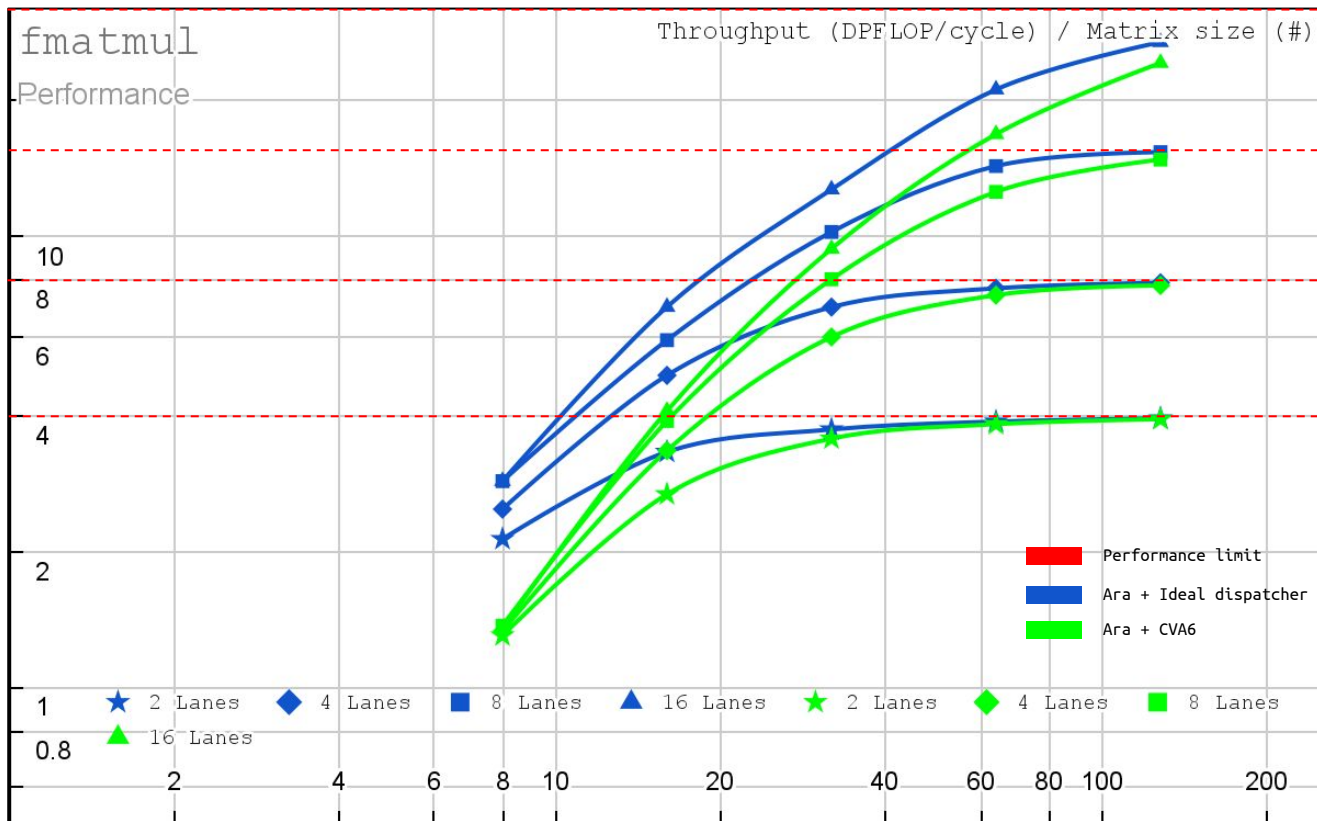
Ideal dispatcher - fmatmul



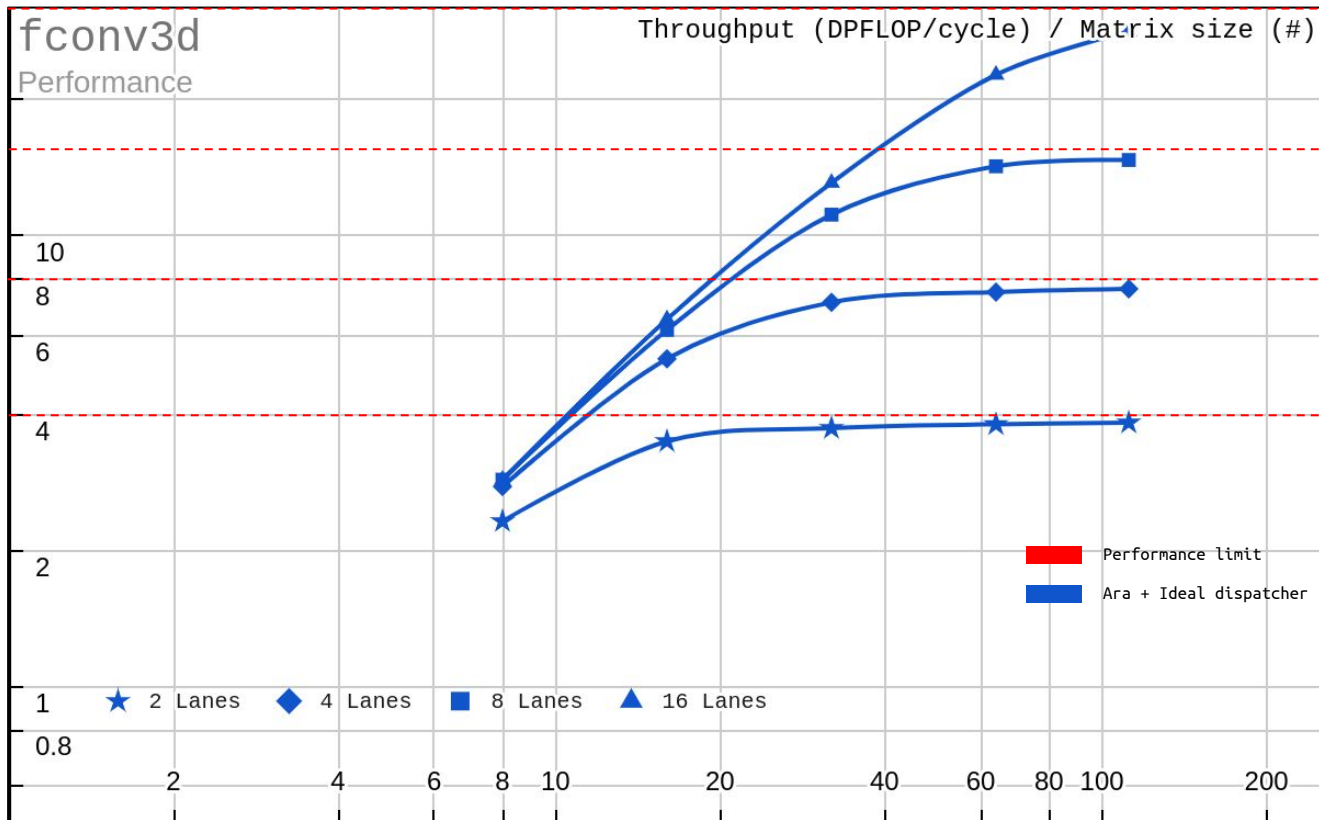
Ideal dispatcher - fmatmul



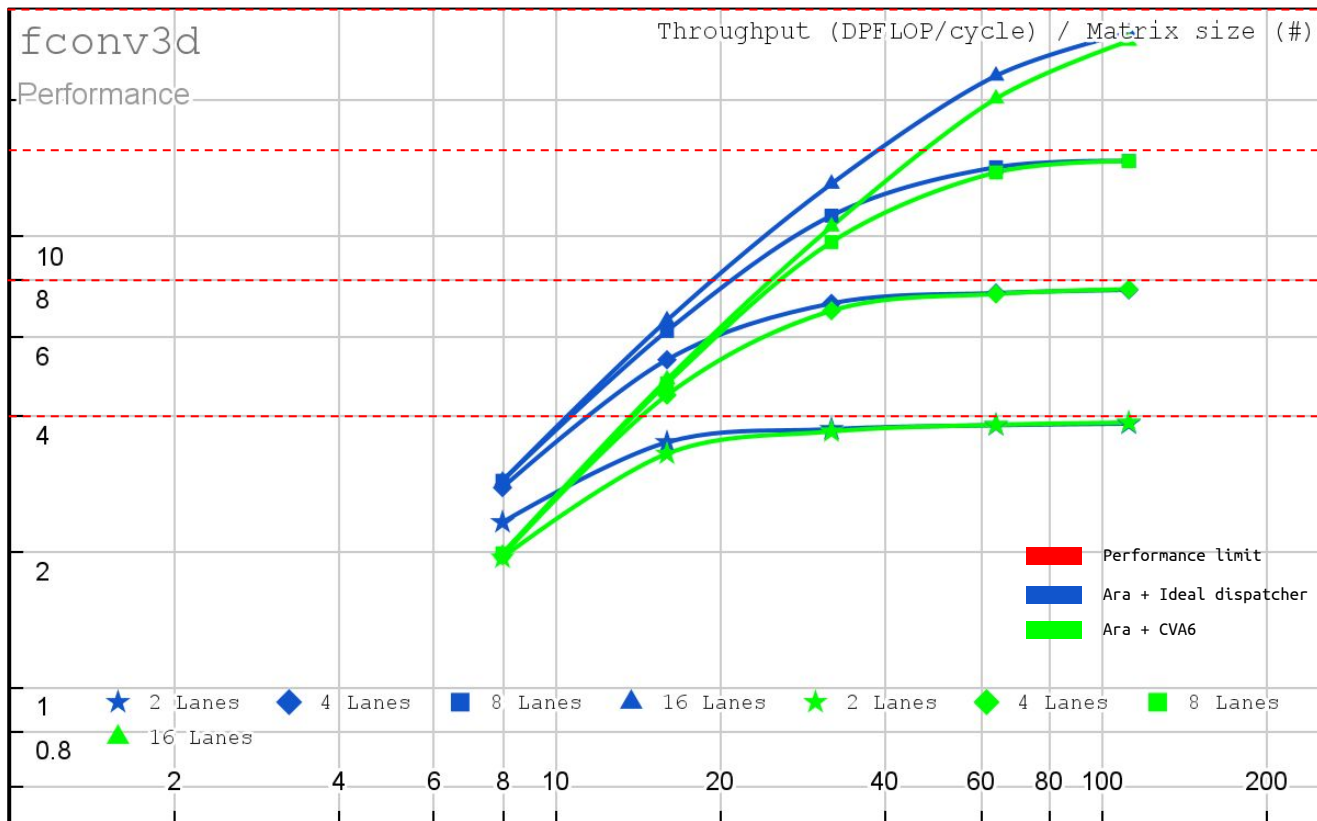
Ideal dispatcher - fmatmul



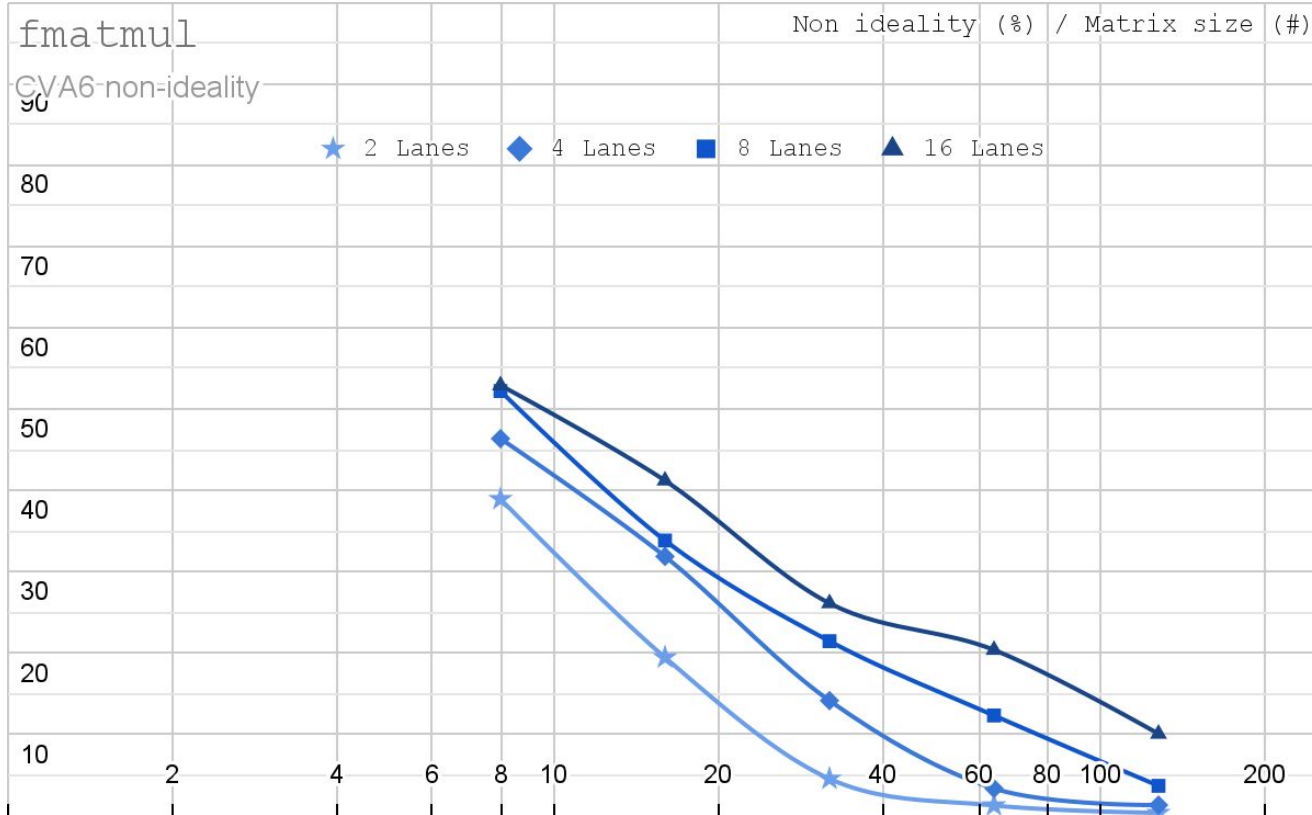
Ideal dispatcher - fconv3d



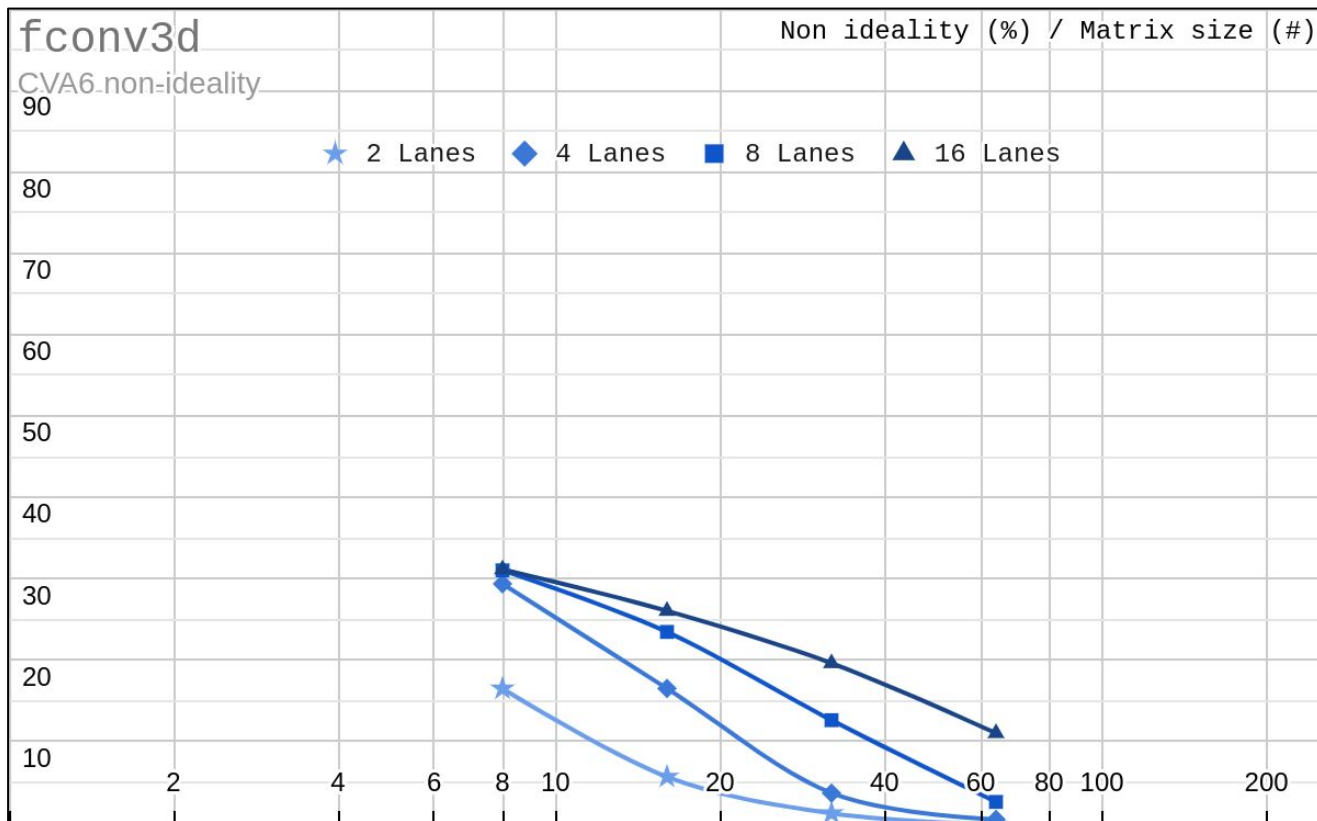
Ideal dispatcher - fconv3d



Ideal dispatcher - fmatmul



Ideal dispatcher - fconv3d



Bug fixes

- WIP - Sequencer:
 - Make it independent from ready signals
 - Use counters instead
 - Critical point for both frequency and IPC