Update on Ara

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Summary

- **T-Head**
  - First programs
- **New Backend trials**
  - Halve the caches
  - Power Breakdown
- **Ara projects**
  - Toward RVV 1.0

T-Head C906 Board

- Native toolchain does not compile Vector code

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- Vector code traps in illegal instruction!

T-Head C906 Board

The scalar code runs with no issues…

```
=============
=  FMATMUL  =
=============



----------------------------------------------------------------
Calculating a (4 x 4) x (4 x 4) matrix multiplication...
----------------------------------------------------------------

Initializing matrices...
Calculating fmatmul...
Illegal instruction
root@RVBoards:compiled_on_fenga9#
```

T-Head C906 Board

The vector code traps!

```
0000000000010e5c <fmatmul_vec_4x4_slice_init>:
   10e5c:   1141                    addi    sp,sp,-16
   10e5e:   e422                    sd  s0,8(sp)
   10e60:   0800                    addi    s0,sp,16
   10e62:   5e003057            vmv.v.i v0,0
   10e66:   5e003257            vmv.v.i v4,0
   10e6a:   5e003457            vmv.v.i v8,0
   10e6e:   5e003657            vmv.v.i v12,0
   10e72:   0001                    nop
   10e74:   6422                    ld  s0,8(sp)
   10e76:   0141                    addi    sp,sp,16
   10e78:   8082                    ret
```

```
=============
=  FMATMUL  =
=============


------------------------------------------------------------
Calculating a (4 x 4) x (4 x 4) matrix multiplication...
------------------------------------------------------------

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```
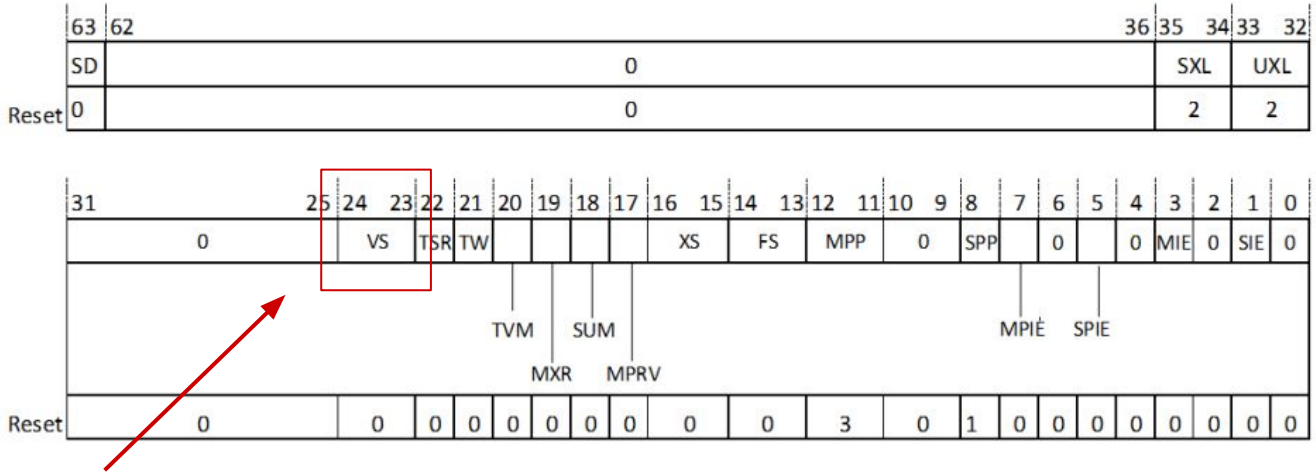

T-Head C906 Board

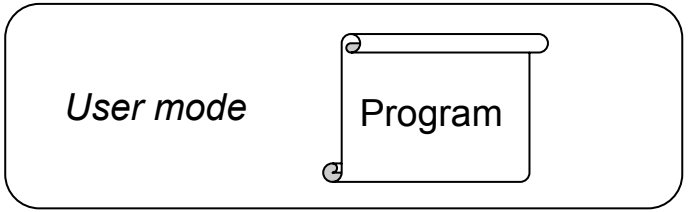
Should the vector engine be enabled through **MSTATUS CSR**?



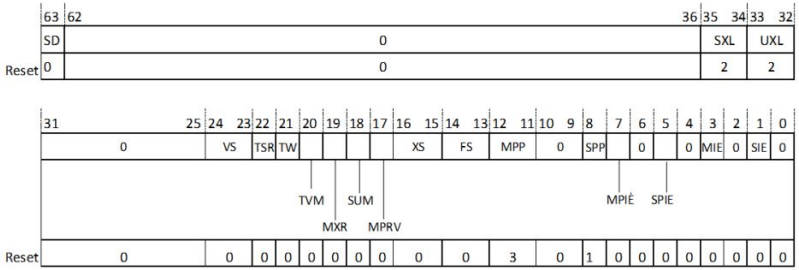
Non standard VS position!

picture 16.1: Machine mode processor status register (MSTATUS)

T-Head C906 Board



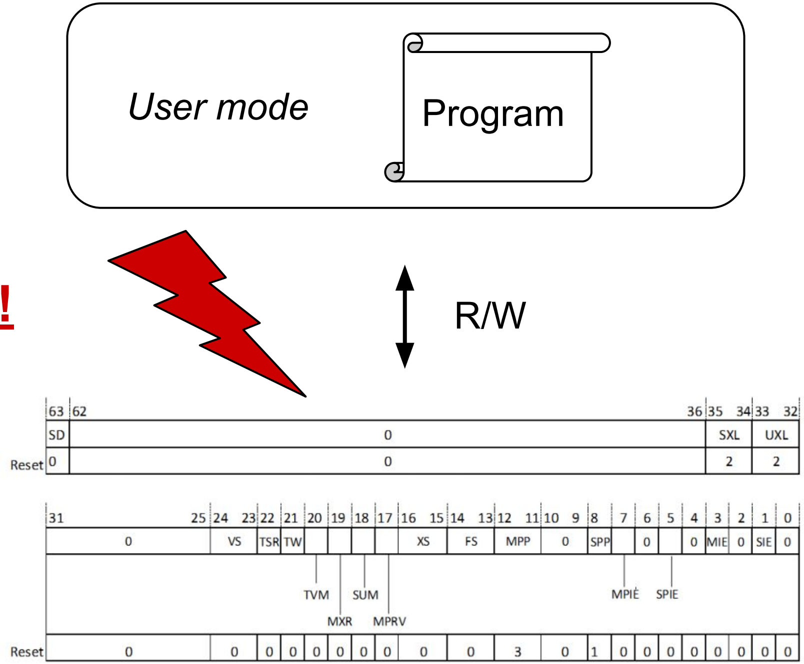
Try to enable the Vector extension…



MSTATUS (or SSTATUS)

T-Head C906 Board

EXCEPTION!



MSTATUS (or SSTATUS)

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➢ *Modify SSTATUS with a Kernel Module?*

T-Head NN Library

- T-Head NN optimized vector library for C906
- https://github.com/T-head-Semi/csi-nn2
- Try library functions on C906 and on Ara
- Some unsupported instructions, and RVV 0.7.1
- On C906 should run natively: baseline!

New Backend Trials

- L1 scalar caches are huge
- Not critical since computation is mostly on Ara
- Halve I$ and D$ line widths?
- `fmatmul` utilization within ±1%
- Smaller chip, lower power consumption, relaxed PnR timing?

Further

- Add power breakdown and more PnR data to paper
- Submit to ASAP conference
- Vectorize Embench
- Try NN lib on T-Head C906
- Yun testing