Update on Ara

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Summary

- **Research Paper**
  - DAC22
- **T-HEAD C906**
  - Exploration
- **Small Matrices problem**
  - Parametrize cache line width (CVA6)

Research Paper

- New Ara architecture and features
- RVV 0.5 to RVV 1.0 differences
- Impact on architecture with Lanes
  - Vector register file
  - Shuffle/deshuffle
  - Reshuffle
  - Mask unit
- Analyze small matrices performance

T-HEAD C906

✓ Initial exploration

✓ Environment setup and bug fixes

✓ Simulation of scalar code

✘ Simulation of V code -> V extension was not open-sourced

Small matrices (fmatmul)

- WIP: parametrize cache line width in CVA6
- Expected better performances due to fewer stalls