**TWG Meeting Record March 22 2021**

# 1. In Attendance

(see TWG meeting attendance file)

# 2. Voting Eligibility for March 22 2021 meeting (revised subsequent to the meeting)

- A member needs to attend 3 of 4 previous meetings to be eligible to vote. Note that the current meeting forms part of the “4 previous meetings” as stated in the bylaws. (This clarification was made after the TWG meeting)
- Because the December 2020 meeting was held close to Christmas, everyone will be counted as having attended the December meeting (this clarification made after the TWG meeting)
- So the voting eligibility for March, as revised after the TWG meeting, is determined by
    - Attending either or both the Jan/Feb meetings, as below, AND
    - Attending the March meeting

| **Members Voting-Eligible for March Meeting** | | **Feb 2021** | **Jan 2021** |
|---|---|---|---|
| | CMC | Y | |
| | Codeplay | Y | Y |
| | Embecosm | Y | Y |
| | EM Micro | Y | Y |
| | ETH Zurich | Y | |
| | Futurewei | Y | Y |
| | Imperas | Y | Y |
| | NXP | Y | Y |
| | Quicklogic | Y | Y |
| | SiLabs | Y | |
| | THALES | Y | Y |
| | | | |

## 3. TG reports highlighting changes to plan of record, critical issues on projects

| Group | Reporting | Link to report | Key Issues & Actions Noted |
|---|---|---|---|
| SW | Jeremy Bennet | SW TG March report | • IDE needs example projects<br>• Clang/LLVM work on assembler added from University of Tubigen<br>• Discussion raised: chairs in their capacity as chairs recommended to avoid endorsement of particular member products. |
| HW | Hugh Pollitt Smith | | • MCU - PR progress meeting to be held on **March 30**<br>• Intention to target combined PL/PA gate approval for next TWG meeting<br>• No new progress on Verilator project to report |
| Cores | Arjan Binks | | • A big pull request for E40S and E40X came at the end of last week. After Checkin was approved for the CQ, this was merged into OpenHW Github<br>• From now on, all PR are incremental into OpenHW Github.<br>• User manual links are available<br>• CV32E40P - RVVI/RVFI work is looking very promising - this will be the technology used working forward<br>• CVA6 - passed PL gate- meeting end of this week to define scope of DUT |
| Verif. | Steve Richmond | | • Improvements on Verification infrastructure<br>• Enhance ISA coverage model, benchmarking, Embench test bench to be used.<br>• RVVI/RVFI will help solve some of the issues encountered on CV32E40P<br>• Parallel core development with branching methodology<br>• CI flow went live this morning<br>• FORCE RISCV support for 32 bit is now merged into the OpenHW |

| | | | |
|---|---|---|---|
| | | | repo. |
| | | | |

## 4. Updated gate names

New gate names were presented.

PC = Project Concept (*formerly Preliminary Project Launch, PPL*)

↓

PL = Project Launch

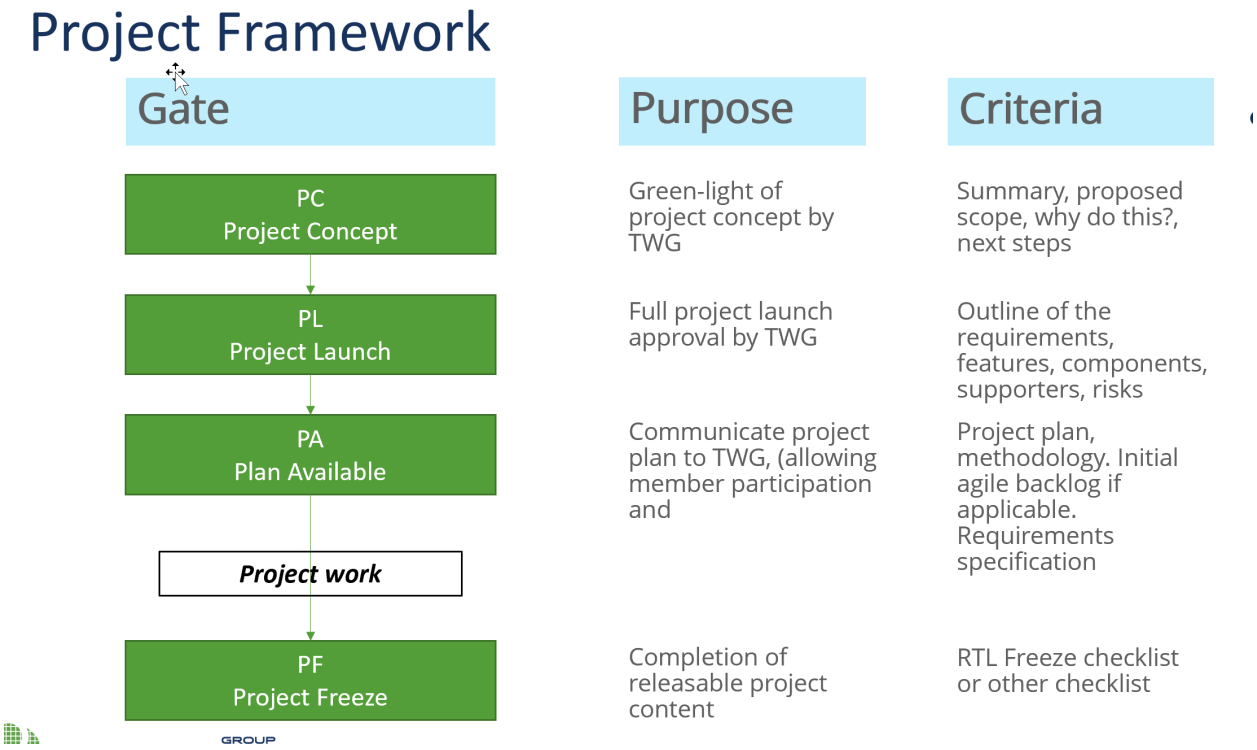
↓

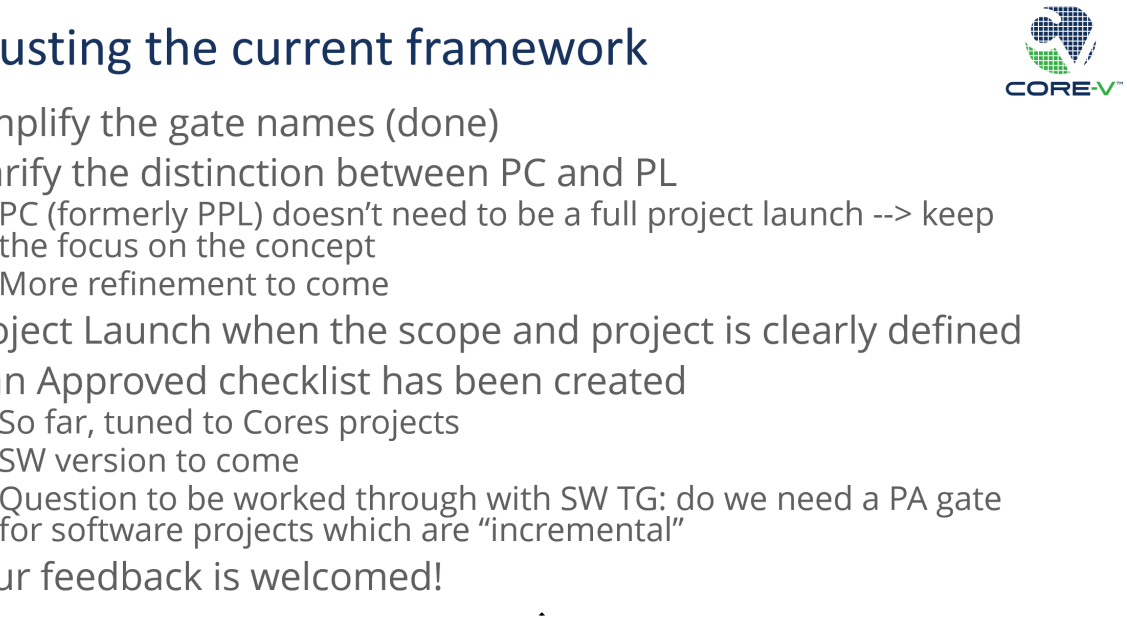
PA = Plan Approved (*formerly Project Plan Approved, PPA*)

↓

PF = Project Freeze (*formerly Project Completed, PC*)

Overall gate process was recapped (D Bees)






## 5. Plan Approved Gate Milestone for Cores Projects

The PA gate checklist, prepared for Cores projects, was presented. This was based mainly on the experiences of the CV32E40P project
Spreadsheet PA checklist

## 6. Plan Approved proposal CV32E40S and CV32E40X

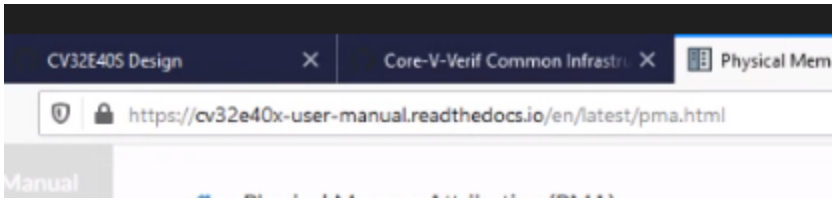
The PA gate approval request was presented by Arjan Bink for these two enhancements to the E40 family.

### Materials presented

E40S and E40P Plan Approval checklist. The PA checklist has been annotated with detailed material prepared by Arjan and the E40S and E40X teams.

E40S and E40P Project Plan document

Note that the Requirements Specification is available at the following Github location




**Member Vote on Approval of PA Gate**

| Member | Votes to Approve PA Gate for CV32E40S | Votes to Approve PA Gate for CV32E40X |
|---|---|---|
| **CMC** | Y | Y |
| **Codeplay** | Y | Y |
| **Embecosm** | Y | Y |
| **EM Micro** | Y | Y |
| **Futurewei** | Y | Y |
| **Imperas** | Y | Y |
| **NXP** | Y | Y |
| **Quicklogic** | Y | Y |
| **SiLabs** | Y | Y |
| **THALES** | Y | Y |

10 votes to approve PA Gate for CV32E40S project

0 abstain

0 against

10 votes to approve PA Gate for CV32E40X project

0 abstain

0 against

The Plan Approved Gates for both projects were overwhelmingly approved. Great job Arjan Binks and SiLabs team!