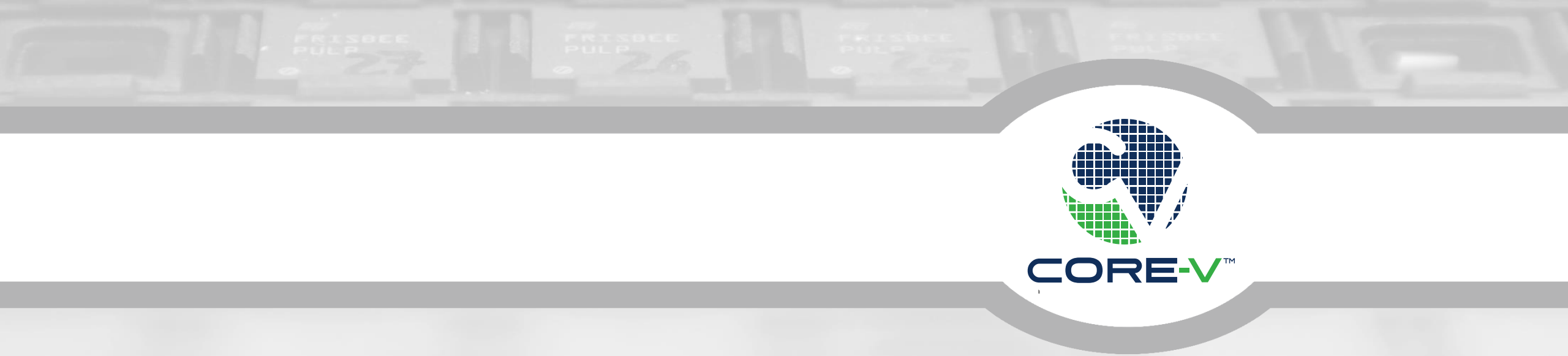


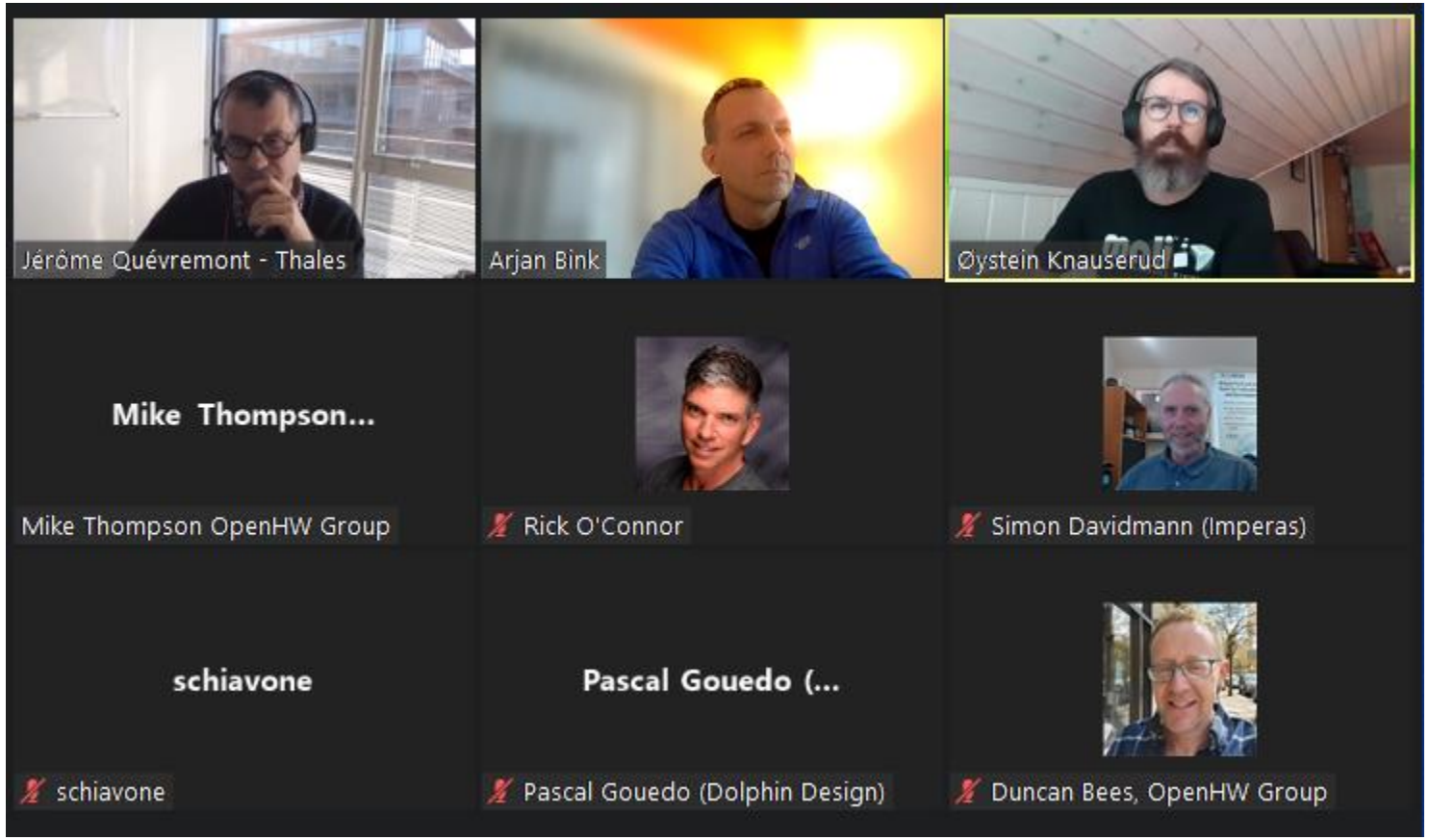
CORES TG – February 6 2023

Arjan Bink

Jérôme Quevremont

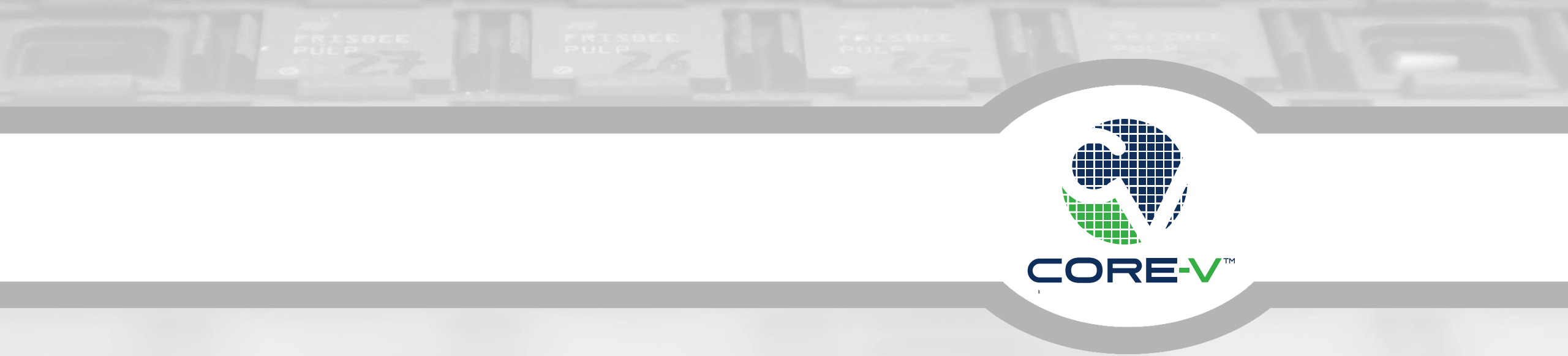
Davide Schiavone

Present


Jérôme Quévremont - Thales
Arjan Bink
Øystein Knauserud
Mike Thompson...
Mike Thompson OpenHW Group
Rick O'Connor
Simon Davidmann (Imperas)
schiavone
schiavone
Pascal Gouedo (...
Pascal Gouedo (Dolphin Design)
Duncan Bees, OpenHW Group

Agenda

- CV32E40X / CV32E40S status
- CVA6 status
- CV32E40Pv2 status
- Core overview



CV32E40X / CV32E40S status

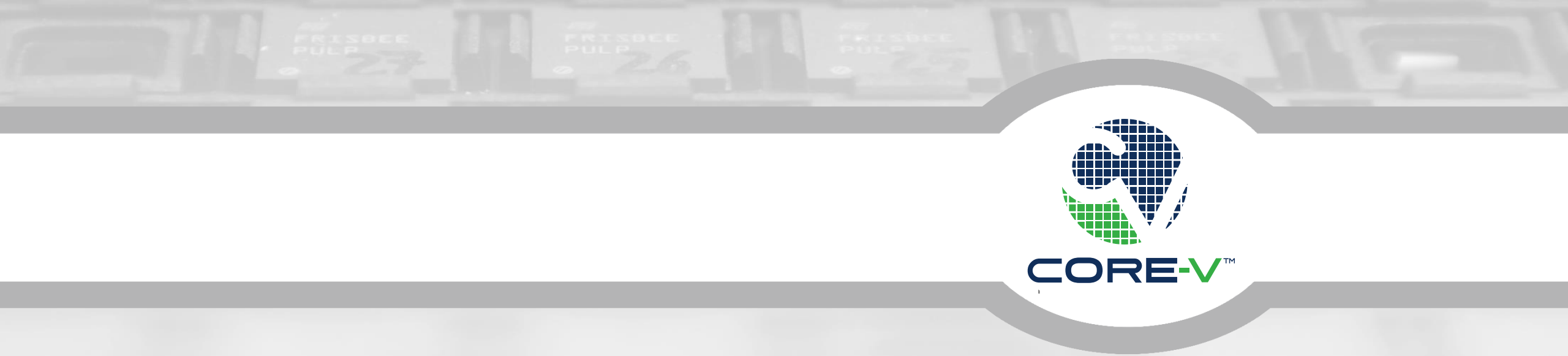
Øystein Knauserud

CV32E40X and CV32E40S

- Core debug updated to V1.0.0.
  - Including support for triggers 0x2, 0x5, 0x6 and 0xF
  - Configurable 0-4 triggers depending on parameter
  - Accesses to DM_REGION not blocked by PMA/PMP during debug
- Issue fixes (see next slide)
- RV32E support complete
- Updated to Zc V1.0.1
- Fence vs fence.i
- Yaml file for CSRs

Issues resolved

- CV32E40X
  - #751, #711
- CV32E40S
  - #397, #394, #391, #365, #363, #362, #361, #353, #343, #333
  - #369, #355, #350, #342, #334



CVA6 status

Jérôme Quévremont

Cores TG meeting, 2023-02-06

CVA6 highlights

- Core:
  - PRing FPGA resource optimizations
- SW:
  - Linux Yocto support released: https://github.com/thalesgroup/meta-openhw
- Verification kick-off meeting 24-26 January
  - OpenHW × TRISTAN project initiative
  - With Thales, OpenHW staff, Bosch, Mu Electronics, 10x Engineers, Synthara, Dolphin, Imperas, ETH Zürich, CSEM
- Version numbering:
  - Verification will be driver in several steps (1, 2, 3).
  - Current solution: number the core version: 0.1.0, 0.2.0, 0.3.0
  - But: CVA6 repo is at the 4.2.0 version (PULP legacy)
  - Should we instead number these steps starting as 4.3.0, … ?

Meetings in https://calendar.google.com/calendar/embed?src=meetings@openhwgroup.org

CV32E40Pv2 status

Pascal Gouédo

Yoann Pruvost

Xavier Aubert

Project

- Project
  - Design & Verification meeting
    - Wednesday 14:00 CET every 2 weeks(Ical)
  - Dedicated technical meetings when needed
  - Reporting to Cores TG
- Mattermost channels
  - TWG : Cores : CV32E4*P
  - TWG : Verification
- Resources
  - Pascal Gouédo
    - Specification, Design, Verification & Formal
  - Yoann Pruvost
    - Design, Verification & Formal
  - Xavier Aubert
    - Verification leader
  - Vaibhav Jain
    - Verification
- OpenHW staff
  - Mike Thompson
    - Verification support
  - Davide Schiavone
    - Architecture & Design support

Documentation

- User Manual
  - cv32e40p_v1.2.0
    - All Pulp instructions re-encoded in RISC-V custom extensions
    - Hardware Loops constraints clarification
  - cv32e40p_v1.2.1
    - Additional Hardware Loop constraints

Design

- RTL verified with Formal tool
  - Merged in cv32e40P repo and cv32e40p_v1.2.1 release created
  - Aligned with cv32e40p_v1.2.1 User Manual

Tools

- SW toolchain deliveries:
  - October 31th, 2022
    - Establish baseline RV32IMFCZicsr functionality and test
  - January 13th, 2023
    - Support of all march custom extensions
    - **Assembler** support of all but Hardware Loop PULP instructions

- Imperas Reference Model
  - v2 support expected beginning of February

Verification

- core-v-verif environment
  - COREV-DV supporting all PULP instructions
  - RVFI support pushed in core-v-verif repo
  - Updates for configurability (PULP, FPU, FPU instructions latency)
    - Implemented and tested
    - All PULP instructions tests can now be exercised
      - 15 are OK, 4 are failing

      ⇨ Created 4 GCC Toolchain issues
    - FPU test running fine with different latency configurations
  - Move to ImperasDV support started
- Verification test plans ready to be reviewed

Core overview

Core	TRL	Privilege	ISA	Debug	Interrupts	Bus	Gate count (min, typ, max)	CoreMark / MHz (min, typ, max)	Target date
CV32E20	5	M, U (v1.11)	RV32I, RV32E, C, M, Zicsr	0.13.2	CLINT	OBI	14K, 19K, -	-, 2,47, -	2023 Q1 (per August 2022)
CV32E40P	5	M (v1.11)	RV32I, C, F, M, Xpulp, Zicsr, Zfinx, Zifencei	0.13.2	CLINT	OBI	-, -, -	-, 2.91, -	2023 Q1 (per October 2022)
CV32E40S	5	M, U (v1.12)	RV32I, RV32E, C, M, Xsecure, Zba, Zbb, Zbc, Zbkc, Zbs, Zca, Zcb, Zcmp, Zcmt, Zicsr, Zifencei, Zkt, Zmmul	1.00	CLINT, CLIC	OBI	-, -, -	-, 2.91, 3.12	2023 Q2 (per December 2022)
CV32E40X	5	M (v1.12)	RV32I, RV32E, A, C, M, Xif, Zba, Zbb, Zbc, Zbkc, Zbs, Zca, Zcb, Zcmp, Zcmt, Zicntr, Zihpm, Zicsr, Zifencei, Zkt, Zmmul	1.00	CLINT, CLIC	OBI	-, -, -	-, 2.91, 3.12	2023 Q4 (per December 2022)
CV32E41P	3	M (v1.11)	RV32I, C, F, M, Zca, Zcb, Zcmb, Zcmp, Zcmt, Zfinx	0.13.2	CLINT	OBI	-, -, -	-, 2.91, -	Not in active development
CVA5	3	M, S, U	RV32I, A, M				-, -, -	-, -, -	Not applicable
CVA6	5	M, S, U (v1.10)		0.13.2	CLINT	AXI4	-, -, -	-, 2.93, -	Unknown

Thank you!