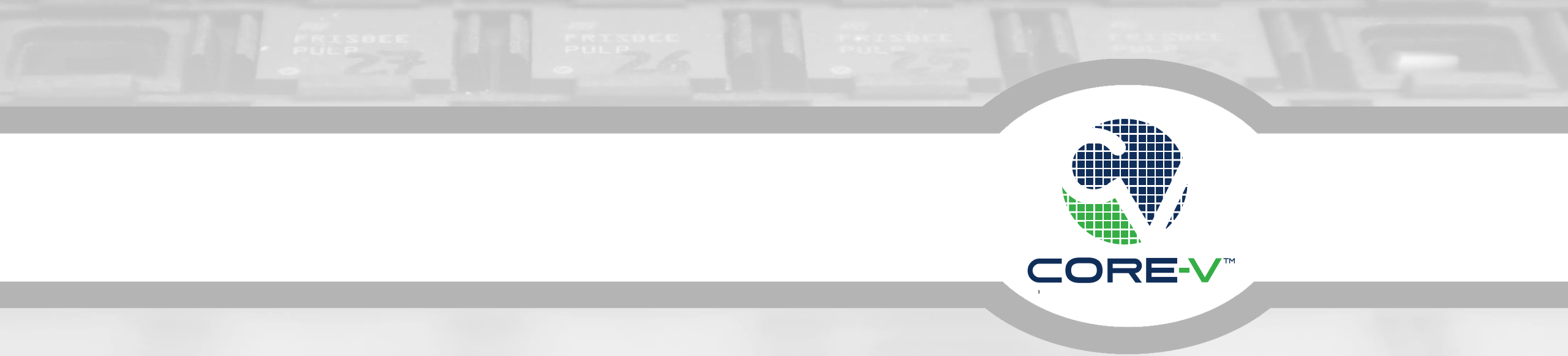


CORES TG – April 4 2022

Arjan Bink

Jérôme Quevremont

Davide Schiavone

Agenda

- CV32E40P (v2) status
- CV32E40X / CV32E40S status
- CV32E20 status
- CVA6 status
- Roadmap discussion

CV32E40Pv2 status

Pascal Gouédo

Yoann Pruvost

Project

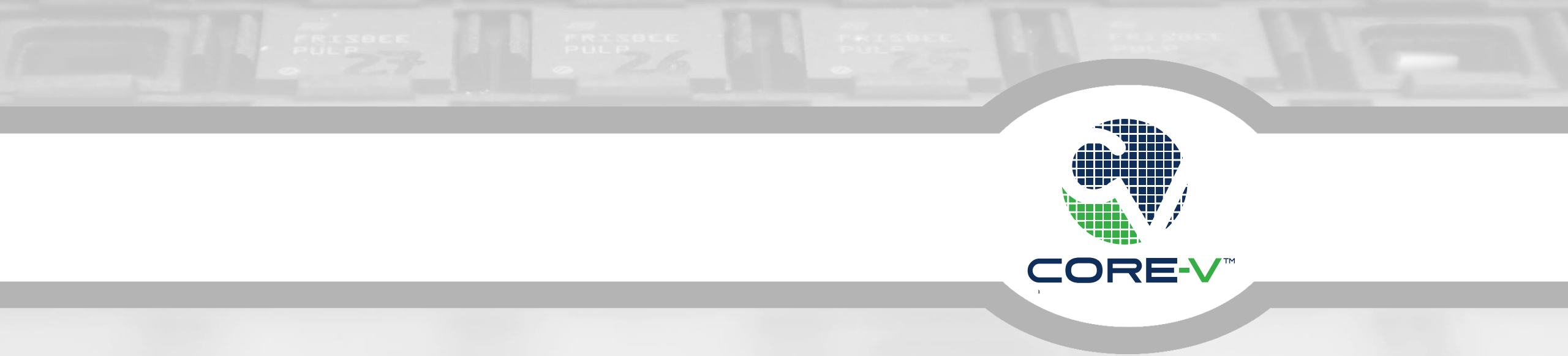
- Project
  - Verification & Design meeting
    - Wednesday 14:00 CEST every 2 weeks(Ical)
  - Dedicated technical meetings when needed
  - Reporting to Cores TG
  - Next: Make a mid-term schedule
- Mattermost channels
  - TWG : Cores : CV32E4*P
  - TWG : Verification
- Resources
  - Pascal Gouédo
    - Specification, Design, Verification
  - Yoann Pruvost
    - Design, Verification (core-v-verif & Formal)
  - 1 Sub-contractor
    - Formal Verification (with OneSpin support)
- OpenHW staff
  - Mike
    - Verification environment lead
    - Technical support
  - Davide
    - Architecture & Design technical support

Documentation

- Specification
  - PR #452: Re-encoding table submitted to review on February 24, 2022
    - Need PR update to remove X's in some instructions encoding (in the week)
  - instruction_set_extensions.rst update with re-encoding
    - nearly finished, PR expected this week
  - Next : Hardware loops
    - Add more details about constraints and behavior
    - Analyze all HWLoops issues (#266, #583, #584, #598, #618)
    - Specify behavior with respect to Interrupt and Debug

Design, Verification & Tools

- Design
  - on-going : update of Core Decoder with re-encoding
- Verification
  - E40P core-v-verif environment
    - Fatal error with Questasim when using Imperas ISS
      - Debug on-going on cv32e40p/dev branch of up-to-date Mike's fork
    - No pb with Cadence Xcelium
    - Cover group syntax error with Synopsys VCS
  - Executed some test on CV32E40X env to understand RVFI tracer
- SW toolchain
  - Embecosm business contract finalization nearly done



CV32E40X / CV32E40S status

Øystein Knauserud

CV32E40X

- User manual updates
  - Started using tags for versions and labels to generate changelogs
- RVFI updates
  - Handling of WFI/sleep and interrupts
- Simplified LSU sign extension
- Tracer with assembly annotation
- Started implementing CLIC core internal part

CV32E40S

- Weekly merges from CV32E40X
- User manual updates
  - Started using tags for versions and labels to generate changelogs
- Increased PMP to 64 regions
- Implemented PC and control flow hardening
- Implemented parity and checksum generation

CV32E20 Status

Lee Hoff, Joe Circello

OPENHW GROUP™
PROVEN PROCESSOR IP

CV32E20: Status

- Project Gates
  - PC gate passed on 6/2021
  - PL gate passed on 2/2022
  - PA TBD
    - Intended technical details are fairly well defined
    - Development of initial high-level development timeline
      - Need RTL design resource
- Project meetings
  - Every Tuesday 9:00 EDT (next on 2022-4-5)
- Mattermost channel -- TWG : Cores : CVE20
- Github repository github.com/openhwgroup/cve2

Status Continued

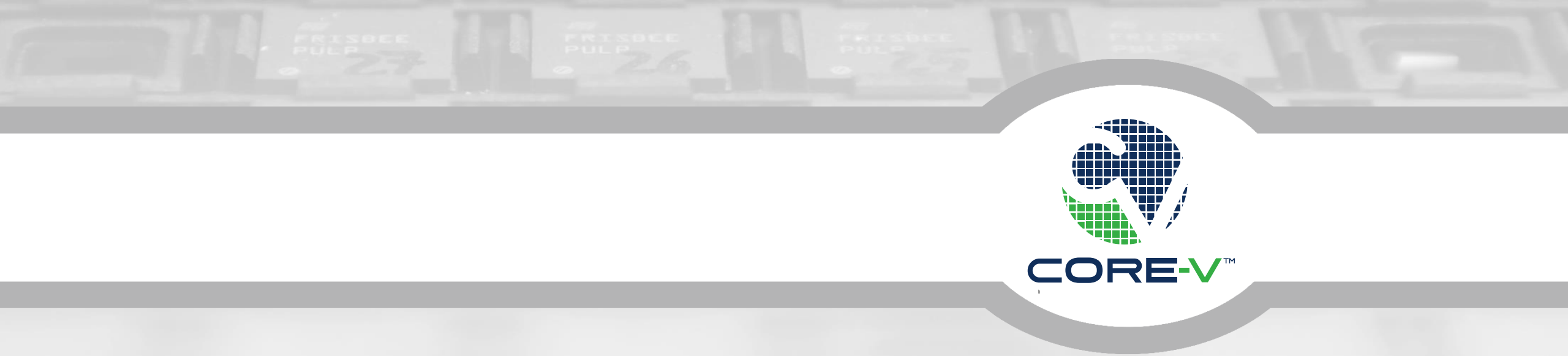
- Project Summary
  - Co-sponsored by NXP and Intrinsix
  - Ultra-low-end core based on Ibex
    - Use the IBEX core RTL design as the starting point
      - Intended as “minimum size” 32-bit RISC-V processor
      - Support for “micro” and “small” configurations
  - Optimized for minimum gate count and lowest power
  - Targeted at the low-end of RISC-V MCU roadmaps
    - Any “compute constrained socket”
    - Processor element in embedded SoC subsystems

https://github.com/lowRISC/ibex/blob/master/README.md

Config	"micro"	"small"
Features	RV32EC	RV32IMC, 3 cycle mult
Performance (CoreMark/MHz)	0.904	2.47
Area - Yosys (kGE)	17.44	26.06
Area - Commercial (estimated kGE)	~16	~24
Verification status	Red	Green

CV32E20: Current Activities

- Agreement on desired technical core details
- Two NXP resources identified and assigned
  - One specifically focused on E20 core verification
- Ongoing discussions with multiple stakeholders
  - OpenHW Verification (Mike Thompson)
  - Imperas (Larry Lapides, Kat Hsu)
  - Embecosm (Jeremy Bennett)
- Identified the Ibex RTL parameters to be supported vs. removed
- Working on Plan Approval document
- Work on core specifications has started



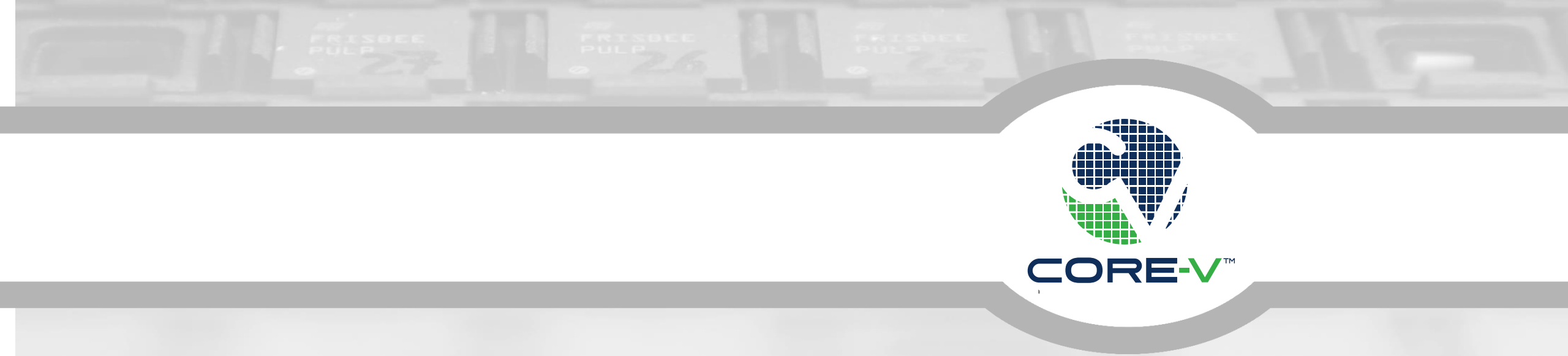
CVA6 status

Jérôme Quévremont

Cores TG meeting, 2022-04-04

CVA6 highlights

- Project
  - PA gate passed:
    - PA document with 2022 milestones (link)
    - Specification (temporary link before conversion to AsciiDoc)
  - Investigating GitHub Kanban boards to track project
  - Presentation at RISC-V Week (Paris, 3-5 May) and demo on OpenHW booth
- Core design:
  - Investigating solutions for configurable reset (sync/async, level)
    - Dropping the “no reset” FPGA style
  - Ongoing FPGA optimization: -28% LUT -30% FF as of today (front end optimization, L1 cache sizing, optional C extension)
  - Investigation CSR YAML description and use with JADE DA tool
  - Need to synchronize with CV-VEC team
- Verification:
  - Progress on CI environment: trigger Thales CI from OpenHW GitHub, add Linux boot on FPGA
  - CV-X-IF DVplan 1st version on GitHub; SiLabs review welcome
  - RV32F DIV & SQRT verification workplan identified (to be reused by CV32E40Pv2)



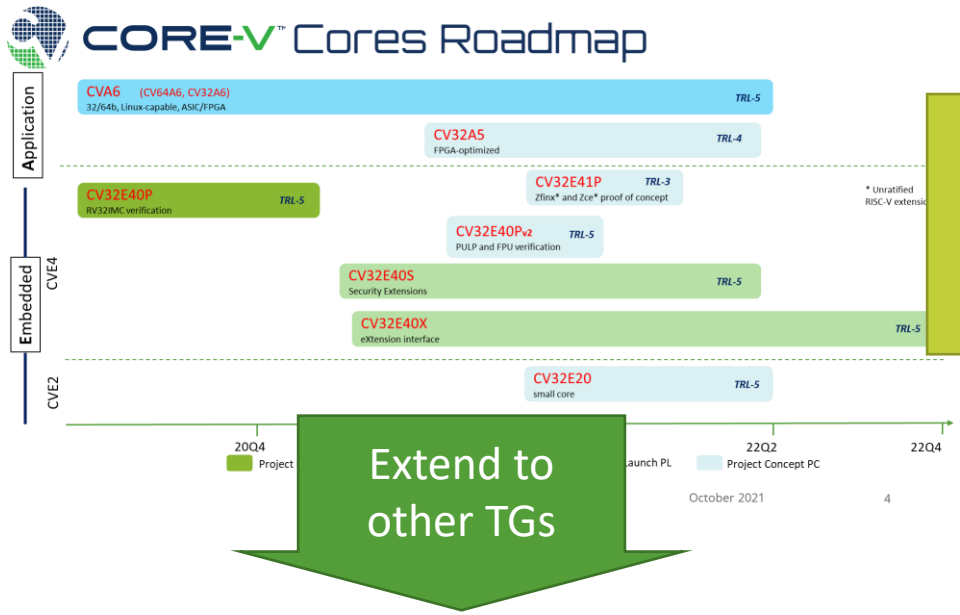
OpenHW Roadmapping

Jérôme Quévremont

Cores TG meeting, 2022-04-04

Presented in previous meeting

Roadmapping



Give directions beyond current projects

Extend to other TGs

- Verification TG
- SW TG
- HW TG
- Interconnect TG
- Functional Safety TG

Prepare and publish a consolidated OpenHW roadmap by mid 2022

- sets direction and plan of record
- common look and feel
- based on TG-level roadmap inputs and TWG member review

Next steps on OpenHW Roadmap

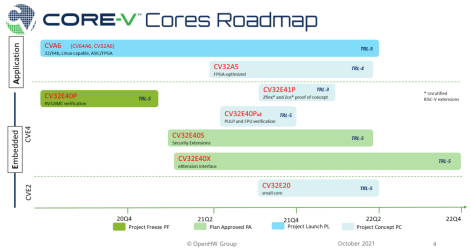
Presented in previous meeting
Beyond schedule ☹

- TWG TWG meeting to complete new project suggestions
- TGs prepare a timeline map of projects and deliverables by end of **March 2022**. Include
  - Confirmed and potential projects
  - Collaborations between members and with external groups
  - Target TRL…
- Consolidation of TG roadmaps (TG *chairs / TWG co-chairs / OpenHW staff)
- Presentation by TWG co-chairs to TWG for review and ratification (end of **June 2022**)

Feedback on this process welcome.

Suggested roadmap term 3 years (e/o 2024)

Roadmap items



- Updated CORE-V roadmap (dates…)
- CV-X-IF (spec, verification, supported cores, extension dev kit…)
- CV-VEC
- Concepts for future projects:
  - High performance core (OoO, dual issue…), need feedback from OpenHW Asia
  - TinyFPU for CV32E20
  - CHERI protection
- Off Cores TG (in OpenHW roadmap)
  - OpenHW specific SoC modules (debug, trace, interrupt ctrl)
  - IOMMU, IOPMP…
  - Multicore, need feedback from Jonathan
  - Multicore with safety features (bounded latency)
  - Chiplet
  - QEmu
- Not addressed: SW and HW TG

Discussed Feb. 18th with Duncan and Arjan
Waiting for common template

Thank you!