



CORES TG – February 7 2022

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Agenda

CORE-V

- CV32E40P (v2) status
- CV32E40X / CV32E40S status
- CVA6 status
- New project proposals / roadmapping







CV32E40Pv2 status

Pascal Gouédo



CV32E40Pv2: current activity



- Design
 - Started PULP re-encoding to evaluate complexity
- Verification
 - Imperas business contract finalized & PO signed
 - E40P core-v-verif test-bench
 - Evolution to either
 - a RVFI/RVVI (E40X like) test-bench or
 - an ImperasDV like test bench (RVVI API rather than RVVI SV interface)
 - ⇒ Actual tracer should be replaced by a native RVFI tracer. Workload evalution on-going.

- SW toolchain
 - Embecosm business contract finalization on-going







CV32E40X / CV32E40S status

Øystein Knauserud



CV32E40X



- Code cleanups / refactoring
- Removal of TODOs/FIXMEs
- User manual updates
 - Spec updates priv 20211105-signoff, debug 1.0.0, B 1.0.0-38g865e7a7and Zce 0.70.1
- PPA optimizations
- LSU prepared for XIF memory interface
- Introduced M_EXT parameter (Multiplier)
- Github issues



CV32E40S



- Weekly merges from CV32E40X
- Github issues
- Bugfixes
- User manual updates
- Dummy instruction insertion is complete
- PPA updates (mainly PMP for better timing)
- CSR shadow flops are now instantiated to avoid removal during synthesis.







CVA6 status

Jérôme Quévremont

Cores TG meeting, 2022-02-07



CVA6 highlights



- U. Minho likely to join OpenHW and contribute to CV64A6 with the H (hypervisor) extension
- Preparing PA gate for the Feb. 28th TWG meeting:
 - Polishing the specification (<u>link</u>)
 - Assembling 2022 work plan (milestones)
- Recent demos on CVA6:
 - FreeRTOS
 - UBoot + OpenSBI + Buildroot Linux + remote debug with Eclipse IDE
- On-going/upcoming work:
 - PPA optimization, CV-X-IF PoC, design updates, CSR YAML description
 - DV env. incremental setup, starting verification with RV32F DIV & SQRT (to be reused by CV32E40Pv2)
 - Yocto Linux





New project proposals / Roadmapping

Technical WG

2022-01-24 (excerpt from 2021-12-13)



Capturing strategic vision/roadmap for OpenHW



- Technical WG role:
 - Kick off and vote on new projects
 - Track TG progress
- Technical WG areas for improvement:
 - Members get to know each other (expertise, technical plans...) to foster collaborations
 - Steer OpenHW roadmap beyond current projects
- Actions taken
 - New members' introduction
 - Surveying members' suggestions for new projects → feed roadmap

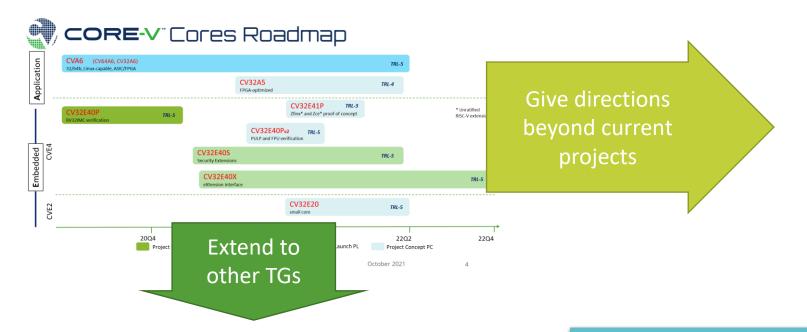
After 2 years, it is timely to refresh and publish the OpenHW technical roadmap





Roadmapping





- Verification TG
- SW TG
- HW TG
- Interconnect TG
- Functional Safety TG

Prepare and publish a consolidated OpenHW roadmap by mid 2022

- sets direction and plan of record
- common look and feel
- based on TG-level roadmap inputs and TWG member review



Next steps on OpenHW Roadmap

- Two TWG meeting to complete new project suggestions
- TGs prepare a timeline map of projects and deliverables by end of **March 2022**. Include
 - Confirmed and potential projects
 - Collaborations between members and with external groups
 - Target TRL...
- Consolidation of TG roadmaps (TG *chairs / TWG co-chairs / OpenHW staff)
- Presentation by TWG co-chairs to TWG for review and ratification (end of June 2022)



Feedback on this process welcome.

Suggested roadmap term 3 years (e/o 2024)



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Road ahead presentation



- Presented at December and January TWG meetings:
 - CHERI protection model
 - Tariq Kurd, Huawei
 - Tiny FPU & relationship to FPU/FPNEW
 - Joe Circello, NXP (+ETHZ)
 - Next steps on chiplets
 - Denis Dutoit, CEA
 - Suggested OpenHW roadmap/project for fault tolerant cores
 - Li Chen, U Sask
 - Out of order cores
 - Duncan on behalf of John Davis, BSC
 - Recap on Multicore interconnect
 - Jérôme Quévremont, Thales (next slides)
 - Qemu
 - Wei Wu, ISCAS
- Slides in https://github.com/openhwgroup/core-v-docs/tree/master/TWG/MeetingPresentations/RoadmapMeeting_211213

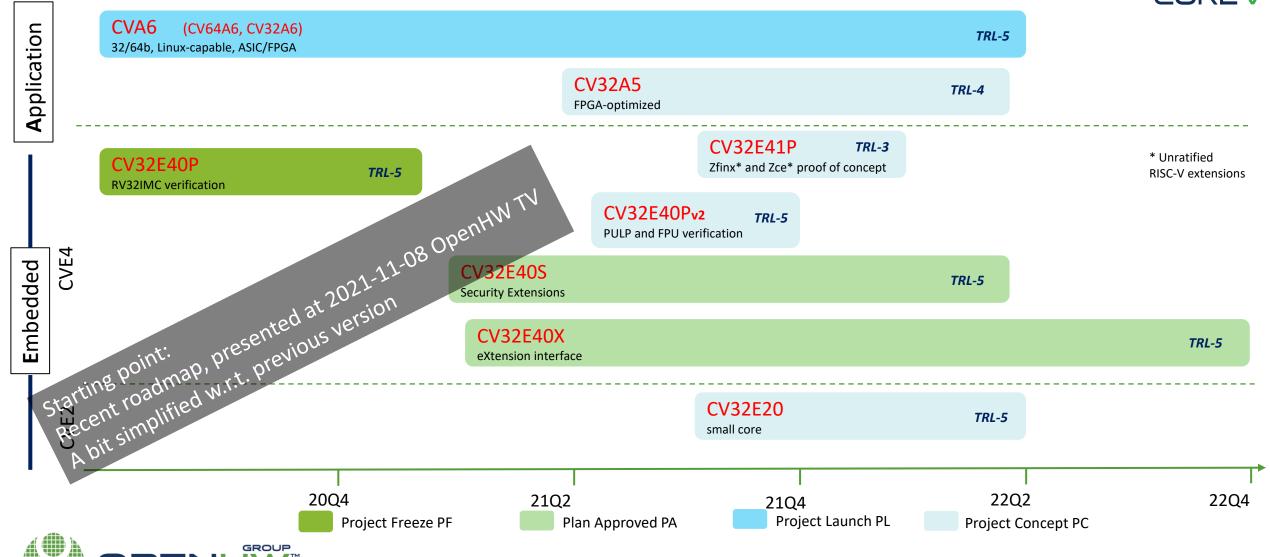




CORE-V[™] Cores Roadmap



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Thank you!

