CORE-V 180 MCU Proposal

Sorbonne Université/LIP6 & Global Foundries


Jean-Paul.Chaput@lip6.fr

April 24, 2023 @Internet

Overview

This project is jointly proposed by **Sorbonne Université** & **Global Foundries**.

- Design a CORE-V MCU on Global Foundries 180nm.
- Using the FOSS RTL-to-GDSII Coriolis toolchain.
- The GF 180nm process node is now NDA free.
- The final GDSII layout can be openly published.
- The whole building procedure can be published and reproduced by third parties.

Expected Outcomes

- A free RTL-to-GDSII toolchain, calibrated and proven for use with GF 180nm node.
- A CORE-V MCU chip usable for small applications.
- A CORE-V MCU design tutorial for academics and teaching, along with at least a basic test PCB board.
- A CORE-V 180 DevKit may also be developped either part of this project or as a follow up proposal.
- A free, CORE-V MCU readily customizable platform for all industrial partners.

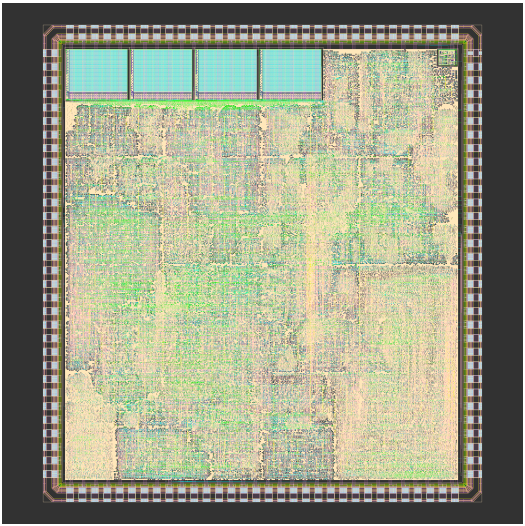
Contributions

- GF will support the GDSII physical design and supply the 180nm die.
- GF will define the MCU market requirements.
- SU/LIP6 will provides the RTL-to-GDSII toolchain, configure it, and build the design tutorial.
- In addition SU/LIP6 will provides simple analog blocs, like a PLL.
- Various Standard cells library, SRAM and I/O cells will be tested.
- A scaled down version of the CORE-V MCU will be used.

Tradeoffs

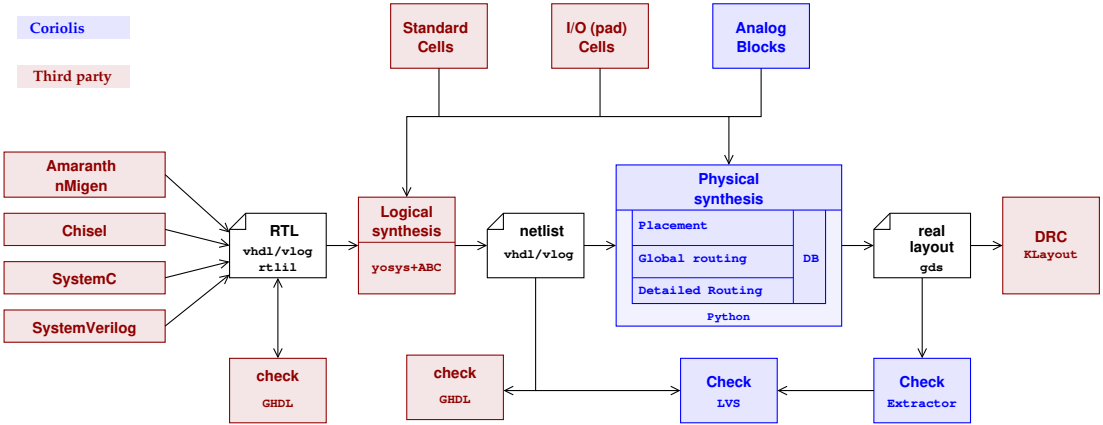
- The CORE-V MCU must be scaled down for two reasons:
  1. A 22nm design cannot fit into the envisionned 180nm area.
  2. The eFPGA will not be available.
- GF will define the alloted area for the design.
- Given the area, a scaled down version must be selected, in accordance to kind of application(s) it is choosen to run.

The SU/LIP6 Experience



- The LibreSOC chip.
- `https://libre-soc.org/`.
- TSMC 180nm.
- 1.3 Mt,
  standard cells: 500 Kt,
  SRAM: 800 Kt.
- 120K gates (SRAM excluded).
- 5.1 $\times$ 5.5 mm (28mm^2).

ASIC Design Flow



Standard Cells Libraries

- As an experiment, we will check three standard cells libraries:
  1. The GF library, supplied with the design kit.
  2. The portable cells, supplied by Chips4Makers (`https://chips4makers.io`).
  3. The SU/LIP6 portable cells (symbolic).
- And two SRAMs:
  1. The GF SRAM, supplied with the design kit.
  2. The portable SRAM supplied by Chips4Makers.
- The version to be send to the foundry will be choosen according to overall area and timing results.