CORES TG – November 7 2022

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Agenda

- CVA6 status
- CV32E40X / CV32E40S status
- Consistency of working with other TGs
- Agenda of December 15 Cores TG meeting
- Core overview

CVA6 status

Jérôme Quévremont

Cores TG meeting, 2022-11-07

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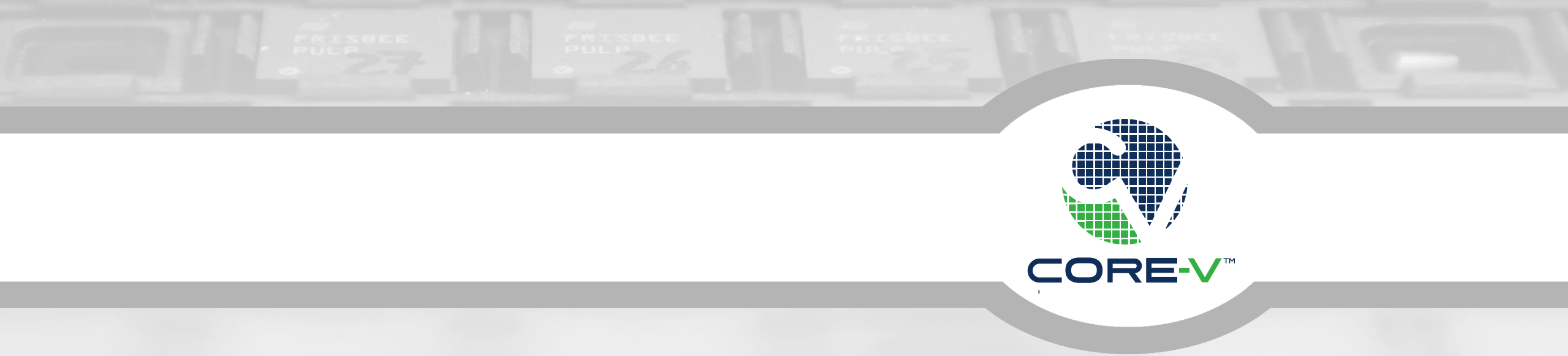
CVA6 highlights

- Project
  - Already 2 progress meetings using the GitHub-based Kanban board
  - Meeting every week at 2pm CET; last Fridays at 5pm CET / 8am PT
  - Nov. 17th: introduction to CVA6 and FPGA optimizations (Intel's Pathfinder context)
- Doc
  - JADE DA tool to produce CSR tables; connection with IP-XACT. One table for all configurations.
  - Very first template for user manual
- Core design:
  - Started PRing FPGA resource optimizations
  - Scratchpad: will be external to L1 caches (updated requirement spec accordingly).
  - Fixing RTL issues (most in CV-X-F)
  - Templating on hold. We first should try to get as far as possible with parameters.
- SW:
  - Yocto support functional in 32b & 64b; upcoming PRs
- Verification:
  - Refining verification planning
    - RV32IMAC with MMU and PMP (step 1: TRL4, step 2: TRL5)
    - Step 3: RV64IMACFD with MMU and PMP (step 3: TRL5)
  - CV-X-IF verification on going
  - VPTOOL being improved; first usable version targeted e/o 2022

Meetings in https://calendar.google.com/calendar/embed?src=meetings@openhwgroup.org

No CV__A6__ part numbers yet to avoid generating noise

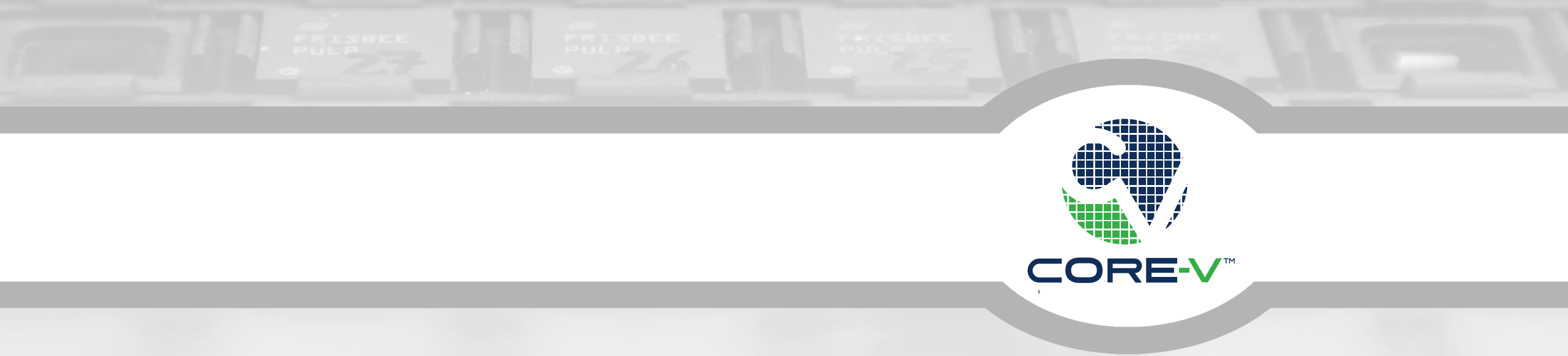


CV32E40X / CV32E40S status

Øystein Knauserud

CV32E40X and CV32E40S

- CLIC SHV
  - Handling of mret with mcause.minhv set
    - Causes lots of issues, mostly resolved but still needs work on RVFI
- RV32E
  - Near completion
- Issue fixing
  - Mostly CLIC and debug related
- Core debug v1.0.0 and trigger features
  - Should be complete before next Cores TG.



Consistency of working with other TGs

Simon Davidmann

Agenda of Dec 15 Cores TG meeting

December Cores TG meeting

OpenHW Face to Face Meeting			
Location:	San Jose, California (facility TBD)		
Date:	Dec 15, 2022		
Time Zone:	Pacific Standard Time		
Draft Agenda, subject to change			
Topic	Start	Duration, h:mm	Session Chair
Welcome/Agenda Review	8:45 AM	0:15	Rick O'Connor
TWG	9:00 AM	1:15	Jérôme Quévremont
Break	10:15 AM	0:20	
MWG	10:35 AM	0:30	Michelle Clancy
Report on EWG/AWG	11:05 AM	0:30	Duncan Bees
Cores TG	11:35 AM	1:00	Jérôme Quévremont
Lunch	12:35 PM	1:00	
Verification TG	1:35 PM	1:00	Simon Davidmann
SW TG	2:35 PM	1:00	Jeremy Bennett
Break	3:35 PM	0:20	
HW TG	3:55 PM	1:00	TBD
Annual General Meeting	4:55 PM	0:30	Rick O'Connor
End	5:25 PM		

- The Cores TG meeting in December will happen F2F at the end of the RISC-V Summit in San Jose on December 15th

Core overview

Core	TRL	Privilege	ISA	Debug	Interrupts	Bus	Gate count	CoreMark / MHz	Target date
CV32E20	5	M, U (v1.11)	RV32I, RV32E, C, M	0.13.2	Basic	OBI	14K, 19K, -	-, 2,47, -	2023 Q1 (per August 2022)
CV32E40P	5	M (v1.11)	RV32I, C, F, M, Xpulp	0.13.2	Basic	OBI	-, -, -	-, 2.91, -	2023 Q1 (per October 2022)
CV32E40S	5	M, U (v1.12)	RV32I, RV32E, C, M, Xsecure, Zba, Zbb, Zbc, Zbkc, Zbs, Zca, Zcb, Zcmp, Zcmt, Zicsr, Zifencei, Zkt, Zmmul	1.00	Basic, CLIC	OBI	-, -, -	-, 2.91, 3.12	2023 Q1 (per July 2022)
CV32E40X	5	M (v1.12)	RV32I, RV32E, A, C, M, Xif, Zba, Zbb, Zbc, Zbkc, Zbs, Zca, Zcb, Zcmp, Zcmt, Zicntr, Zihpm, Zicsr, Zifencei, Zkt, Zmmul	1.00	Basic, CLIC	OBI	-, -, -	-, 2.91, 3.12	2023 Q1 (per July 2022)
CV32E41P	3	M (v1.11)	RV32I, C, F, M, Zca, Zcb, Zcmb, Zcmp, Zcmt, Zfinx	0.13.2	Basic	OBI	-, -, -	-, 2.91, -	Not in active development
CVA5	3		RV32I, A, M				-, -, -	-, -, -	Not applicable
CVA6	5	M, S, U (v1.10)		0.13.2	Basic		-, -, -	-, 2.93, -	Unknown

Thank you!