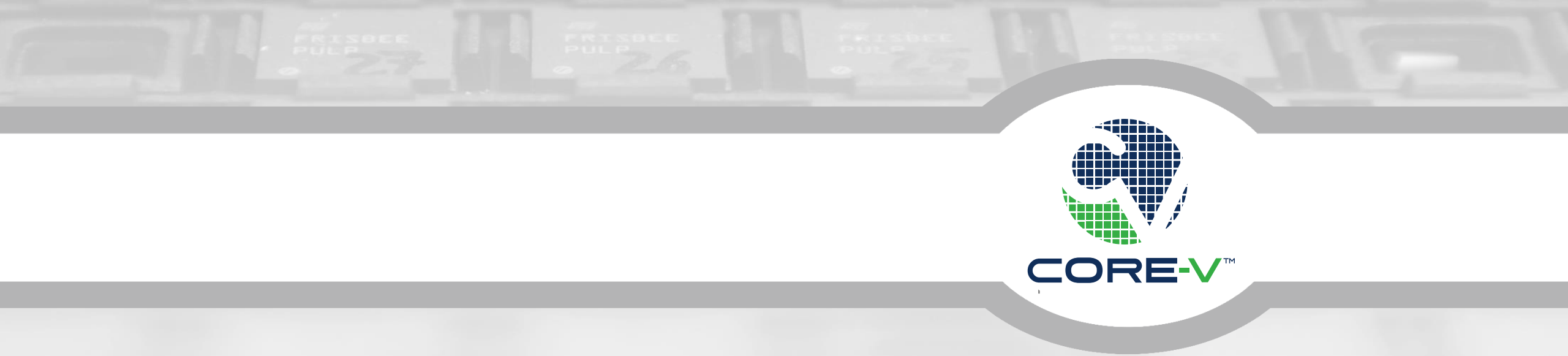

CORES TG – October 3 2022

Arjan Bink

Jérôme Quevremont

Davide Schiavone

Agenda

- CVA6 – Templating language
- CV32E40P status update
- CV32E40X / CV32E40S status update
- Core overview

CVA6 – Templating language

Yannick Casamatta

CV32E40Pv2 status

Pascal Gouédo

Yoann Pruvost

Xavier Aubert

Project

- Project
  - Design & Verification meeting
    - Wednesday 14:00 CEST every 2 weeks(Ical)
  - Dedicated technical meetings when needed
  - Reporting to Cores TG
  - Next: Make a mid-term schedule
- Mattermost channels
  - TWG : Cores : CV32E4*P
  - TWG : Verification
- Resources
  - Pascal Gouédo
    - Specification, Design, Verification
  - Yoann Pruvost
    - Design, Verification (core-v-verif & Formal)
  - Xavier Aubert
    - Verification leader
  - 1 Sub-contractor
    - Formal Verification (with OneSpin support)
- OpenHW staff
  - Mike
    - Verification technical support
  - Davide
    - Architecture & Design technical support

Documentation

- New re-encoding table (2022-09-26) added in PR #452

- User Manual
  - Updated local instruction_set_extensions.rst with last re-encoding table
    - Not pushed until documentation generation flow with versioning put in place

  - Next
    - Hardware loops re-encoding and new instructions definition
    - Understand/set up automatic rendered documents & versioning methodology

Design

- All RTL with re-encoded PULP instructions now available for internal Formal verification team (except Hardware loops)

- Added 2 new top-level parameters for FPU instructions latencies

- Next
  - Update Hardware Loops instructions encoding
  - Push internal work to cv32e40p repo

Verification

- E40P core-v-verif environment
  - Switched to RVFI support (based on E40X implementation)
    - First running version closer and closer to finalization (interrupts & debug fixing)
  - COREV-DV tests generator
    - PULP instructions creation on-going (75 %)
  - Next
    - PULP re-encoded instruction support (ISS option to enable XPULP v1 or v2)
    - Add some configurations files for different FPU instructions latencies

Formal Verification (1)

- Running on 6 configurations
  - IMC
  - + PULP
  - + PULP + F
  - + PULP + ZFINX
  - + PULP + CLUSTER
  - + PULP + CLUSTER + ZFINX
- Next
  - Add configurations with various FPU instructions latencies

Formal Verification (2)

- RV32IMC
  - 1 rule violation (scontext CSR)
- RV32F (all but DIV/SQRT results)
  - 16 rules violations
    - F instructions decoding
    - F instructions result impact on pipeline
    - FFLAGS not correctly set
    - Missing MSTATUS.FS and SD (when Zfinx = 0)
    - FMUL.S wrong result

Core Pb?

CV-FPU pb

- 12 issues created in CV43E40P repo
- 3 issues already reported during v1

- RV32X (PULP instructions)
  - All 320 instructions (but 6 hardware loops) are hold-bounded (10 cycles). Unbounded runs on-going (so far so good).

Tools

- SW toolchain
  - Toolchain development for re-encoded PULP instruction started on September 15th, 2022
  - Deliveries:
    - October 15th, 2022
      - Establish baseline RV32IMFCZcisr functionality, test and benchmarking environment
      - **Assembler** support of PULP instructions
        - Post-Incremented Load/Store
        - General ALU
        - 8- and 16-bit SIMD extensions

CV32E40X / CV32E40S status

Øystein Knauserud

CV32E40X

- Issue fixes
  - Mostly related to CLIC
- Added custom WFE instruction
  - Including changes to when the core retire WFI and WFE
  - WFE behaves like WFI but can in addition wake up to wfe_wu_i pin.
- User manual updates
  - Including updated versions of referenced specs
- Fixed performance issue in tracer

CV32E40S

- Weekly merges from CV32E40X
  - WFE, tracer performance and CLIC issues
- OBI integrity functionally complete
  - Parity checks for *_gnt_i and *_rvalid_i
  - Checksum comparisons for *_rchk_i
  - Some work left to make sure logic is not optimized away.
- Updated cpuctrl CSR
  - Integrity checks, PC hardening and data independent timing enabled out of reset.
- User manual updates
  - Including updated versions of referenced specs

Core overview

Core	TRL	Privilege	ISA	Debug	Interrupts	Bus	Gate count	CoreMark / MHz	Target date
CV32E20	5	M, U (v1.11)	RV32I, RV32E, C, M	0.13.2	Basic	OBI	14K, 19K, -	-, 2,47, -	2023 Q1 (per August 2022)
CV32E40P	5	M (v1.11)	RV32I, C, F, M, Xpulp	0.13.2	Basic	OBI	-, -, -	-, 2.91, -	2023 Q1 (per October 2022)
CV32E40S	5	M, U (v1.12)	RV32I, RV32E, C, M, Xsecure, Zba, Zbb, Zbc, Zbkc, Zbs, Zca, Zcb, Zcmp, Zcmt, Zicsr, Zifencei, Zkt, Zmmul	1.00	Basic, CLIC	OBI	-, -, -	-, 2.91, 3.12	2023 Q1 (per July 2022)
CV32E40X	5	M (v1.12)	RV32I, RV32E, A, C, M, Xif, Zba, Zbb, Zbc, Zbkc, Zbs, Zca, Zcb, Zcmp, Zcmt, Zicntr, Zihpm, Zicsr, Zifencei, Zkt, Zmmul	1.00	Basic, CLIC	OBI	-, -, -	-, 2.91, 3.12	2023 Q1 (per July 2022)
CV32E41P	3	M (v1.11)	RV32I, C, F, M, Zca, Zcb, Zcmb, Zcmp, Zcmt, Zfinx	0.13.2	Basic	OBI	-, -, -	-, 2.91, -	Not in active development
CVA5	3		RV32I, A, M				-, -, -	-, -, -	Not applicable
CVA6	5	M, S, U (v1.10)		0.13.2	Basic		-, -, -	-, -, -	Unknown

Thank you!