Mike Thompson <mike@openhwgroup.org>

Meeting Minutes: SiLabs Debug Verif #2

1 message

Mike Thompson <mike@openhwgroup.org> Wed, Apr 29, 2020 at 12:39 PM
To: Oivind Ekelund <oivind.Ekelund@silabs.com>, Wajid Minhass <wajid.minhass@silabs.com>, Sebastian Ahmed <sebastian.ahmed@silabs.com>, Steve Richmond <steve.richmond@silabs.com>, Davide Schiavone <davide@openhwgroup.org>, Paul Zavalney <Paul.Zavalney@silabs.com>
Cc: Jingliang Wang <jingliangwang@futurewei.com>, Rick O'Connor <rickoco@openhwgroup.org>, Jim Parisien <jim@openhwgroup.org>

Attendees:

OpenHW: Davide Schiavone,Mike Thompson
SiLabs: Oivind Ekelund, Wajid Minhass, Paul Zavalney, Sebastian Ahmed, Steve Richmon

Actions: Mike, Wajid, Paul.
Note: meeting minutes published on GitHub at core-v-docs/verif/MeetingMinutes.

Status of Actions from last meeting:

- Mike confirmed that riscv-dbg is being used by lowRISC Ibex.
- Davide reached out to Chips Alliance but has not received confirmation from them regarding their use/verification of riscv-dbg.
- Mike captured strategy for supporting both Core-level and Subsystem-level verification in a single UVM environment in the Verification Strategy. Arjan provided review comments.
- Wajid has not yet had a chance to start on the review of the core-level debug verification implementation at lowRISC Ibex.
- Davide and Paul completed an update of Debug and Trace features in the user_manual (see pr #287).
- Mike completed translation of user_manual into restructured text.
- Wajid has not yet had a chance to start on the cv32e40p debug Vplan.

New Leadership:

1. Mike will generate status for newly appointed VTG co-chairs Steve Richmond and Jingliang Wang.
2. Team agreed that our on-going debug-verification effort would proceed as usual since debug is a "low hanging fruit" that needs to be implemented/verified regardless of future direction from the VTG co-chairs and/or TWG.

Next Steps:

1. Team agreed to consolidate all debug verification into core-v-verif UVM environment.
   Action: **Mike** to retire the "dm", "scripts", "tb_MPU", tb_riscv" and "verilotor-model" testbenches in the core-v-verif repo.
2. Need to get started on the debug Vplan.
   Action: **Wajid** to provide an estimate of completion for the Vplan and review of the lowRISC Ibex implementation.

Other Business:

1. Team re-iterated that the current focus shall be on debug verification of the core, not subsystem. Subsystem considerations may be discussed at a future date.

2. SiLabs is interested in using the Pulp riscv-dbg IP as the DM for their cv32e40p based subsystem. No interest in a commercial DM at this time.
3. Paul has encountered issues using the PULP toolchain. Mike reported that this has been a long-standing open issue.
   Action: **Mike** to reach out to newly appointed SW TG co-chairs.
4. Team reviewed Paul's suggested additions to the Verification Strategy to support debug verif.
   Action: **Mike** and **Paul** to integrate into the core-v-verif verification strategy.
   Action: **Mike** to provide an explanation of how/why the toolchain, test program and testbench memory map need to be aligned.
5. Agree to hold weekly meetings in the same time-slot (Mike to book).

Cheers,
---mike