CV32E40X/CV32E40S project plan

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CV32E40X / CV32E40S project

- CV32E40X and CV32E40S are run as Agile projects following a scrum methodology involving only the active contributors
  - Daily scrum meetings
  - Sprint Review meetings
  - Sprint Planning meetings
  - Prioritized back log
- Do you want to become an active contributor?
  - Please contact arjan.bink@silabs.com for Design
  - Please contact steve.richmond@silabs.com for Verification
- Tasks involving alignment between multiple OpenHW contributors (e.g. contributors who are not involved on a day-to-day basis), as well as a subset of the larger tasks, are made visible via OpenHW github project boards
  - CV32E40X Design - https://github.com/openhwgroup/cv32e40x/projects/1
  - CV32E40S Design - https://github.com/openhwgroup/cv32e40s/projects/1
  - CV32E40X Testbench - https://github.com/openhwgroup/core-v-verif/projects/11
  - CV32E40S Testbench - https://github.com/openhwgroup/core-v-verif/projects/10
  - Core-V-Verif Common Infrastructure - https://github.com/openhwgroup/core-v-verif/projects/9

CV32E40X / CV32E40S high level phases (1/2)

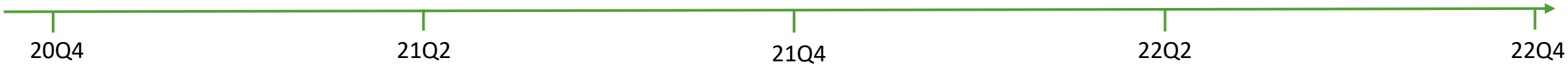
CV32E40X (p.1)
RV32IMCZicount_Zicsr_Zifencei, 4-stage, M-mode, CLINT, OBI, PMA, bus errors

CV32E40X (p.2)
+Zce
+[eXtension interface]

CV32E40X (p.3)
+[Atomics]
+[Bit manipulation]
+[Packed SIMD]

CV32E40S (p.1)
RV32IMC[Xsecure]Zicsr_Zifencei[_Zce], 4-stage, M/U-mode, CLINT, OBI, PMP, PMA, Security

CV32E40S (p.2)
+Zce



CV32E40X / CV32E40S high level phases (2/2)

- CV32E40X
  - Phase 1
    - RV32IMC – Optimized compared to CV32E40P
      - Smaller ALU/MUL
      - Reduced number of register file read/write ports
      - Smarter prefetch
    - Zicount – As on CV32E40P
    - Zicsr – As on CV32E40P
    - Zifencei – Extended with external interface
    - M-mode – As on CV32E40P
    - CLINT – Extended with NMI
    - OBI – Extended with ‘prot’, ‘err’, backward compatible
    - PMA – New feature
    - Bus errors – New feature
    - RVFI interface – New feature
  - Phase 2
    - Zce (Compressed ISA extension) - New feature
    - Extension (X) interface - New feature
  - Phase 3
    - Atomics (A) extension – New feature
    - Bit manipulation (B) extension – New feature
    - Packed SIMD (P) extension – New feature

- CV32E40S
  - Phase 1
    - RV32IMC - Optimized compared to CV32E40P
      - Smaller ALU/MUL
      - Reduced number of register file read/write ports
      - Smarter prefetch
    - Xsecure
      - Security alert outputs
      - Data independent timing
      - Dummy instruction insertion
      - Register file ECC
      - Hardened PC
      - Hardened CSRs
      - Control flow hardening
      - Functional unit and FSM hardening
      - Bus interface hardening
      - Reduction of profiling infrastructure
    - Zicsr - As on CV32E40P
    - Zifence - Extended with external interface
    - M/U-mode- User mode new compared to CV32E40P
    - CLINT – Extended with NMI
    - OBI – Extended with ‘prot’, ‘err’, ‘checksum’ backward compatible
    - PMA – New feature
    - PMP – New feature
    - Bus errors – New feature
    - RVFI interface – New feature
  - Phase 2
    - Zce (Compressed ISA extension) - New feature

Thank you!