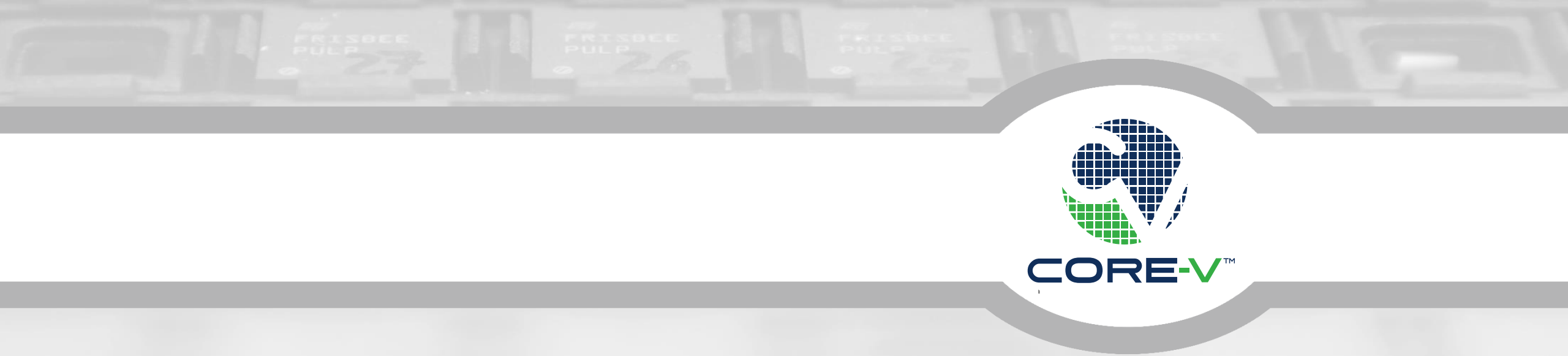


CORES TG – December 6 2021

Arjan Bink

Jérôme Quevremont

Davide Schiavone

Agenda

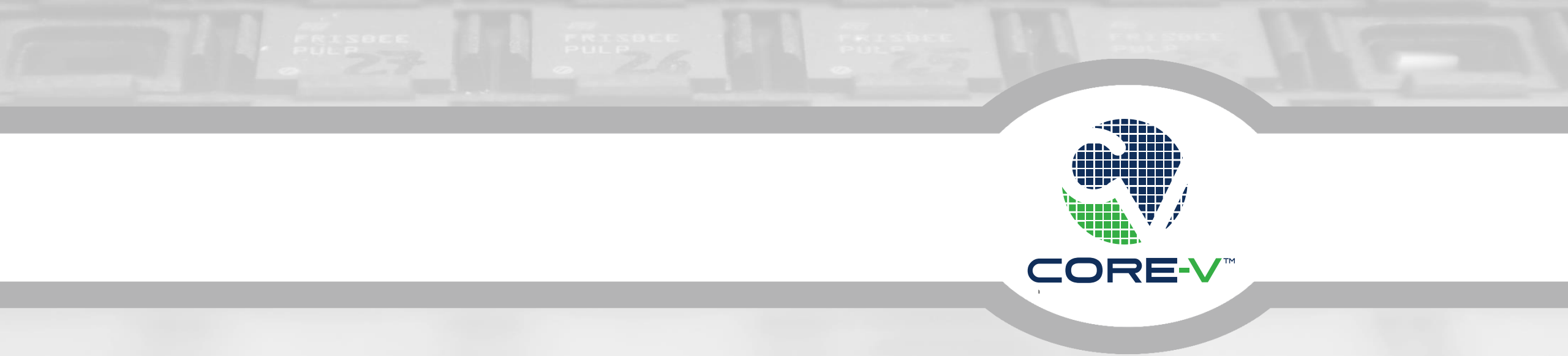
- CV32E40P (v2) status
- CV32E40X / CV32E40S status
- CV32E41P status
- CVA6 status
- Cores TG specific feedback from OpenHW members survey

CV32E40Pv2 status

Pascal Gouédo

CV32E40Pv2: current activity

- Gates
  - Project Launch presented on November 22nd 2021
- Plan
  - Working on activities scheduling to create a timeline with following resources
    - 1 architecture/design
    - 1 design/verification
    - 2 verification
    - 1 design
- Verification
  - Imperas business contract finalization
- SW toolchain
  - Business contract negotiation to re-initiate



CV32E40X / CV32E40S status

Øystein Knauserud

CV32E40X

- RVFI updates
  - nmip
  - Extended rvfi_trap
- User manual updates
- Github issues
  - #281, #315, #317, #280, #323, #332, #333, #300, #299, #275
- Bugfixes
- XIF commit/commit_kill implemented
- LSU write buffer implementation is complete
- Coremark with Zba/Zbb/Zbc/Zbs is now 3.12 Coremark/MHz

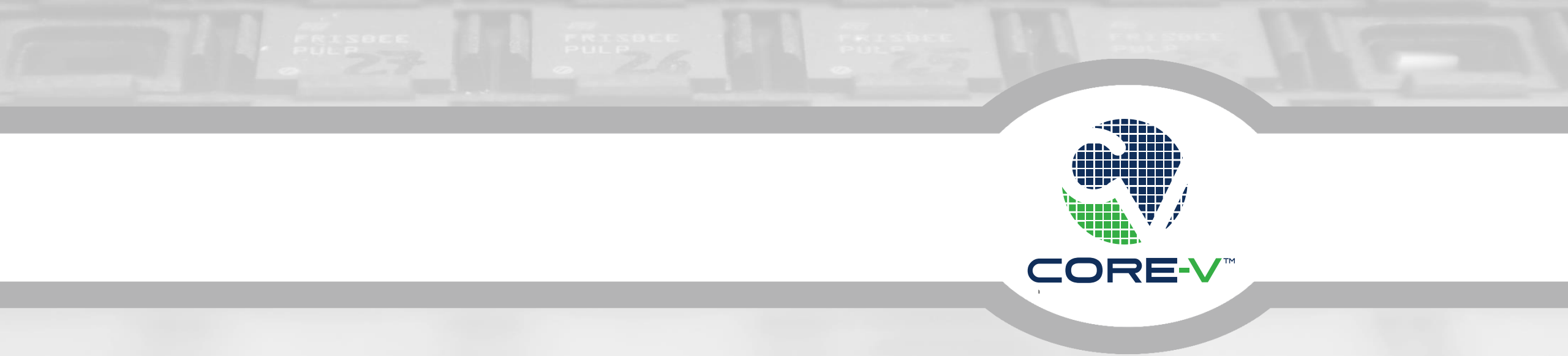
CV32E40S

- Weekly merges from CV32E40X
- Xsecure CSRs and LFSRs implemented
- Data independent timing almost complete
  - DIV and branches
- Dummy instruction insertion started

OneSpin status

- Way of working and progress still considered a bottleneck
  - Need insight in performed checks
  - Need setup for various CV32E40X configurations
  - Need setup for various CV32E40S configurations
  - Need (near daily) reports

- Rick O'Connor
  - "a limited number of OpenHW VTG members can be given access to the OneSpin formal tools within our OpenHW AWS VMs to help establish a 'core-v-formal' CI flow"
  - "Mike will coordinate with the VTG to assemble a small project team to get this up and running"



CV32E41P status

Tariq Kurd

CV32E41P: current activity

- Design
  - Zfinx implemented
  - Zce almost implemented
    - Instruction sequencer implemented
    - Table jump ongoing
    - Other instructions implemented
  - Decoder merged, no more 16->32-bit conversion
    - Zce has 16-bit instructions which don't have 32-bit equivalents
    - Register addresses decoded in IF stage
    - Other decode in ID stage
    - More IF stage predecode is possible if necessary
- Verification:
  - Using UVM testbench without OVPSim
    - It will take us longer to get the cost signed off to update it for Zce than it will take us to finish the project
    - Updated the tracer module to support 16-bit encodings, and will compare traces against Spike, which is useful as Spike needs verification too
  - Basic testing for most instructions done with directed tests
  - No random testing yet

CVA6 status

Jérôme Quévremont

CVA6: current activity

- Specification (link)
  - Quite stable, minor updates
  - OVPSim questionnaire reviewed
- CV-X-IF: PoC on-going
- Speed up CV32A6:
  - Kintex 7 FPGA: 66 → 99 MHz
  - FPGA assessment on-going to further improve PPA
  - Architectural analysis by ETH
- PR to create 4 reference configurations

- Verification:
  - CI environment in place
  - CV-X-IF DVPlan ongoing
  - CSR YAML description
    →Generate access tests
    →Generate documentation
  - Estimating total verification effort
- SW:
  - FreeRTOS: soon available
  - Linux: UBoot + OpenSBI integrated on CV32A6 and CV64A6
  - LLVM activity

CORE-V™

OPENHW™

OpenHW Group

2021 Member Survey - Summary

Duncan Bees duncan@openhwgroup.org

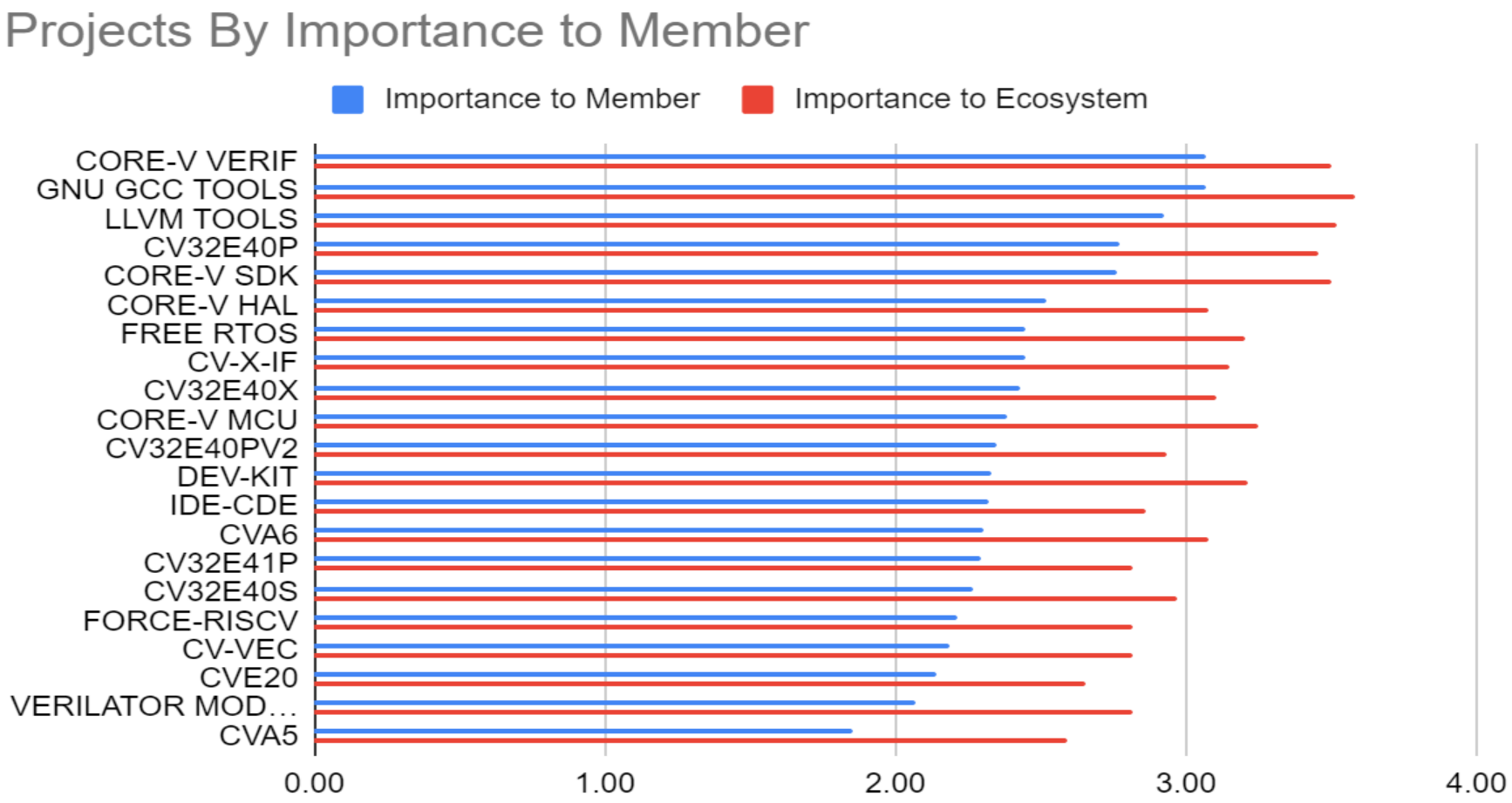
www.openhwgroup.org

GROUP OPENHW™ PROVEN PROCESSOR IP

Full survey

- Full survey can be found here
  - https://docs.google.com/presentation/d/1-wuIlsHbyjL6jjiNT1JiZ8IHvw0y3oF1/edit#slide=id.g104610f442e_0_329
- Here only presenting some slides related to Cores TG

B: Projects Ranked by Importance



SW
SW
SW
SW
SW

5/7 MOST IMPORTANT PROJECTS ARE SW!!

CV32E40P Comments

Project Comments - CV32E40P

- This is the first core to be produced, so is inherently important to OpenHW group. It is critically dependent on the CORE-V MCU project to allow it to be evaluated.
- Stupid name
- nothing to report at the moment
- Isnlt it reallly a 5-tage processor given conventional counting of piopeline stages?
- We are building a radiation tolerant version on it, very important to us.
- No extra comments.
- Havng studied it, there are numberous improvements which can be made (such as removing the PULP logic from the ALU with an ifdef or parameter, as currently it's always included)
- Have not been involved or taken a look at it
- OpenHW first delivered core!
- OneSpin was integral in the formal verification of the core

CV32E40PV2 Comments

Project Comments - CV32E40PV2

- The key factor here is the move to RISC-V compliant encodings for instruction extensions.
- No idea what this is
- nothing to report at the moment
- No extra comments.
- it's probably better to focus on standard extensions instead of XPULP
- Ditto
- PULP and the FPU bring performance to this "DSP" core.

CV32E40S Comments

Project Comments - CV32E40S

- I have marked this as less important, because it is a demonstrator of a specific core being derived using the generic CORE-V ecosystem.
- No idea what this is.. but security sounds important
- nothing to report at the moment
- This core is very useful to us in the future
- No extra comments.

CV32E40X Comments

CV32E40X

- The key feature of RISC-V is the ability to create new custom extensions, which CV-X-IF facilitates. This directly impacts Embecosm, since it will drive compiler work to support these extensions.
- I assume this is RI5CY with X interface.. going forward I have no idea why it makes sense to have a core that has NO x interface.. probably CV32E40PXS is what we want..
- nothing to report at the moment
- No extra comments.
- i think the extension should be part of other existing cores (CV32E40P v1 & v2)
- Ditto
- Interesting if we can use interoperable coprocessors between CV32E40X and CVA6.

CV32E41P Comments

CV32E41P

- This is more important to RISC-V International than OpenHW, since it will be the demonstrator of whether Zce actually yields the benefits suggested by the theoretical analysis (I am not convinced).
- No idea at all.. In theory P is PULP extensions. the 1 in the E41 should be an alternative version to E40..
- nothing to report at the moment
- No extra comments.
- not sure what is tge purpose of this core
- Ditto
- Important for OpenHW recognition as it loops back to a RISC-V draft extension.

CVA6 Comments

CVA6 Comment

- RISC-V has yet to establish a compelling offering in the 64-bit application class processor world. I think the importance is some way down the line, and CVA6 will be an element in the development of any market.
- nothing to report at the moment
- No extra comments.
- Ditto
- The sole OpenHW core that supports Linux.

CVA5 Comments

- FPGA cores have the potential to make custom extensions much more easily available. The real breakthrough will be if CVA5 can be combined with CV-X-IF.
- names get stupider by every entry... this should have been CVA32F50.. but since you like to argue that you have a naming standard and make a mess of it every single time.. be my guest :)
- using it in one of our research project
- No extra comments.
- Ditto
- CVA5 appears as a frontal competition to CV32A6 FPGA optimized version and generates risks of fragmentation, reducing synergies in the application-class cores.

CV32E20 Comments

CV32E20 Comment

- There is still a big demand for really small embedded cores.
- I am guessing this is Ibex?
- nothing to report at the moment
- No extra comments.
- Ditto
- Could be used by our company as a microsequencer. How to make it competitive vs. lowRISC offer?

CV-X-IF Specification Comments

CV-X-IF Specification Comment

- See comments on CV32E40X
- nothing to report at the moment
- No extra comments.
- The CV-X-IF is key to allow RISC-V processor feature diversification: standard or custom extensions. An OpenHW group action should be to have it adopted by CV-VEC project and possibly RISC-V International.

Thank you!