CORE-V™

OPENHW™

OpenHW Group

CORE-V: Open Source RISC-V Cores for High Volume Production

Duncan Bees duncan@openhwgroup.org

www.openhwgroup.org

Agenda

- Opening Remarks - Dr. Liang Peng, Futurewei
- Overview of OpenHW – Duncan Bees, OpenHW Staff
- OpenHW Cores roadmap - Davide Schiavone, OpenHW Staff
- OpenHW SW roadmap – Jeremy Bennett, SW TG Co-Chair
- OpenHW MCU and APU – Tim Saxe, HW TG Co-Chair
- OpenHW Verification – Mike Thompson, OpenHW Staff
- Open discussion

- OpenHW Group is a not-for-profit, global organization registered in Canada and driven by its members and individual contributors where HW and SW designers collaborate in the development of open-source cores, related IP, tools and SW such as the CORE-V Family of open-source RISC-V cores

  - International footprint with developers in North America, Europe and Asia
  - Providing an infrastructure for hosting high quality open-source HW developments in line with industry best practices
  - Strong support from industry, academia and individual contributors worldwide

Futurewei's Key Role in OpenHW

- Platinum Member of OpenHW Group
- Board Of Directors – Dr. Liang Peng
- Co-Chair of the Verification TG – Robert Chu
- Co-Chair of the Marketing WG – Danny Hua
- Contribution of FORCE-RISCV as open-source artefact

Thank you for Futurewei's involvement and support in OpenHW!

Industry Members
73+ Members & Partners

Academic Members
73+ Members & Partners

Partner Ecosystem

73+ Members & Partners

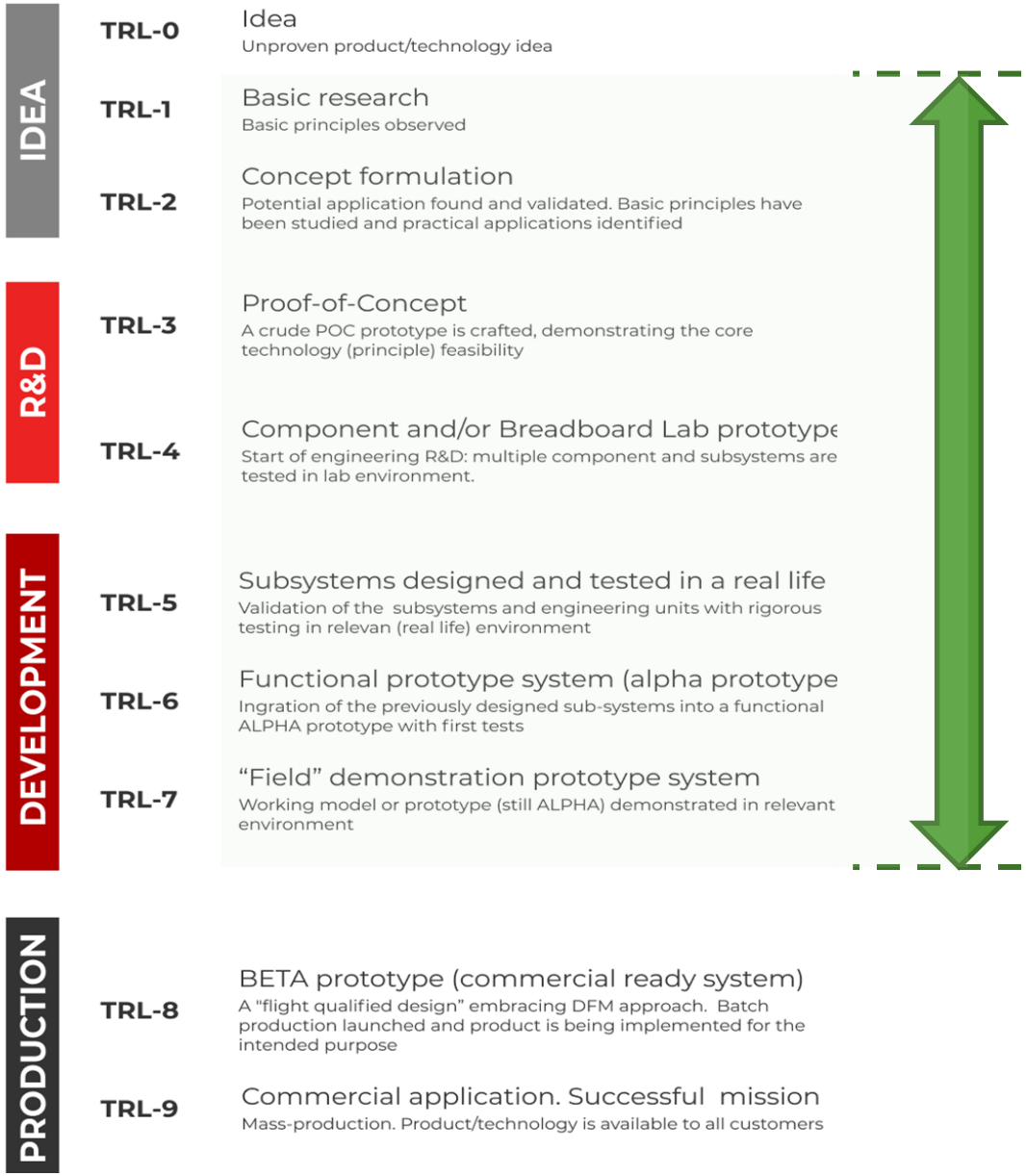
Accounting, Legal,

Ba

Open-Source Objectives

Open Source Objective	OpenHW Group
Community collaboration	•Silicon + Hardware + Software + University + EDA Tools •Product-ready baseline features
Enable flexibility and customization	•CORE-V building block approach •Companies differentiate at value-add
Innovation velocity	•Research results flow directly to front end •Collaborative project model •Infrastructure/governance
Industrial quality	•Open scrutiny of all contributions •Focus on Industrial quality verification
Enable freedom of action	•Open source licenses adapted to hardware •Freedom to innovate

TRL Scale



OpenHW Technology Outputs

OpenHW IP Adopters

TRL Map to OpenHW Activity

TRL	OpenHW Utilization
1-Basic Principles Observed	• **OpenHW research projects** may target TRL-1 as project output, e.g. to develop novel approaches to core or accelerator architecture
2-Concept Formulation	• Core IP or accelerator development projects to produce open source technology are typically initiated as TRL-2 concepts, identifying principles and applications of the IP • The **OpenHW Project Concept Gate** includes a TRL-2 description of the Core IP
3- Proof of Concept	• Core IP or accelerator development projects will pass through TRL-3 as **the (RTL) design completes**. Poof of concept is shown by core compilation and demonstration of basic operations (e.g. Linux booted, coremark results, hello-world)
4- Component Prototype	• Core IP or accelerator projects will pass through TRL-4 as they produce **preliminary PPA results** (via synthesis scripts for FPGA or ASIC) and/or **run preliminary application code**, such as an accelerator running machine learning code.
5- Subsystem Designed and Tested	• Core IP projects reach TRL-5 as they **complete full verification**. The OpenHW RTL Freeze checklist process verifies that the design is fully ready for industrial adoption.
6-Functional (Alpha) Prototype	• OpenHW **designed IP that is integrated into an MCU system** or other device reaches TRL-6 as prototype Silicon is fabricated and demonstrated
7-Field Demonstration Prototype	• **OpenHW development boards** incorporating a prototype Silicon system with OpenHW Software reach TRL-7 as they are demonstrated and deployed

Where can OpenHW Processors Play?

- Open source hardware IP:
  - Most important inroads already in the entry-level segment
  - Mid-range devices are now attracting interest and entries worldwide
  - High-end processor/accelerator segment making first steps

Vertical	Entry-level	Mid-range	High-end / AI
Automotive	Embedded controllers, ultra-low power	Real-time / safety-critical: Vision, motion control, engine management, safety, infotainment	ADAS/autonomous driving processors, sensor fusion
Industrial automation	Embedded controllers: ultra-low power, smart sensing	Embedded processors, sensor fusion; edge-cloud management	High-performance processors with AI acceleration, edge server processors
Communication	Baseband connectivity for wireless communication 5G/6G	Edge server processors, 5G/6G private networks, RF mgmt	5G/6G Base station front-end processors, V-RAN
Data infrastructure		Edge AI node processor	Processors for edge/fog servers; CPUs and accelerators (servers, HPC)
Other (Healthcare, CE, Defence, Aerospace…)	Embedded controllers in wearables and healthcare devices	Embedded processors	High-end Processors, AI

OpenHW opportunities

Slide credit: European Commission DG Connect

European Commission

Working Groups and Task Groups

- Technical Working Group
  - Cores Task Group
  - Verification Task Group
  - Hardware Task Group
  - Software Task Group
- Marketing Working Group
  - University Outreach Task Group
- OpenHW CEO + Staff
  - Facilitating/building project capacity
- OpenHW Board
  - Oversight of working group results

Project framework and decisions

Open-source development
Specification development
Driven by Engineering staff of member companies

Research proposal coordination/OpenHW Accelerate

Technical Working Group (TWG)

- Co-Chair: Jérôme Quévremont, Thales Research & Technology
- Drive the overall technical direction, development roadmap and project execution for all technology related activities within the OpenHW Group and oversee the Task Groups
  - TWG is essentially the OpenHW Group company's "R&D / Engineering Organization"
- OpenHW Group engineering release methodology is based on the Eclipse Development Process
  - All OpenHW Group Platinum / Gold / Silver members are also Solutions members of the Eclipse Foundation

Cores Task Group

- Chair: Arjan Bink, Silicon Laboratories
- Vice-Chair: Jérôme Quévremont, Thales Research & Technology
- Develop feature and functionality roadmap and the open-source IP for the cores within the OpenHW Group such as the CORE-V Family of open-source RISC-V processors.
- Initial contribution of open-source RISC-V cores from ETH Zurich PULP Platform and the OpenHW Group is the official committer for these repositories

Core	Bits/Stage	Description
CVE4 (RI5CY)	32bit / 4-stage	A family of 4-stage cores that implement, RV32IMFCXpulp, optional 32-bit FPU, instruction set extensions for DSP operations including HW loops, SIMD extensions, bit manipulation and post-increment instructions.
CVA6 (Ariane)	32 & 64bit / 6-stage	A family of 6-stage, single issue, in-order CPU cores implementing RV64GC extensions with three privilege levels M, S, U to fully support a Unix-like (Linux, BSD, etc.) operating system. The cores have configurable size, separate TLBs, a HW PTW and branch-prediction (branch target buffer, branch history table and a return address stack).

Verification Task Group

- Co-Chairs:
  - Robert Chu, Futurewei Technologies, Inc.
  - Steve Richmond, Silicon Laboratories

- Develop best in class verification test bench environments for the cores and IP blocks developed within the OpenHW Group.

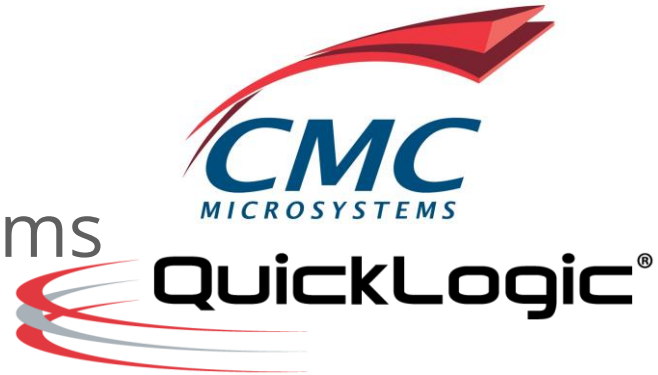
SW Task Group

- Chair: Jeremy Bennett, Embecosm
- Vice-Chair: Yunhai Shang, Alibaba T-Head

- Define, develop and support SW tool chain, operating system ports and firmware for the cores and IP developed within the OpenHW Group

- SW TG active projects include: GCC / LLVM, IDEs, FreeRTOS, HAL, CORE-V MCU SDK, etc.

HW Task Group



- Chair: Hugh Pollitt-Smith, CMC Microsystems
- Vice-Chair: Tim Saxe, QuickLogic
- Define, develop and support SoC and FPGA based evaluation / development platforms for the cores and IP developed within the OpenHW Group.

Marketing Working Group

- Co-Chairs:
  - Danny Hua, Futurewei Technologies, Inc.
  - Kevin Dobie, CMC
- Define and Implement strategies for the promotion and expansion of the OpenHW Group Ecosystem
- Manage
  - OpenHW TV
  - Events
  - PR

Regional Working Groups

- EWG (European Working Group)
- AWG (Asian Working Group)
- Purposes
  - Identify regional strategic/market requirements for OpenHW Cores and enabling technologies
  - Regional marketing initiatives to grow membership base
  - Project incubation
  - Identify and implement data sovereignty requirements appropriate to the region
  - Participate in regional cooperation projects

Asia Working Group

- OpenHW will initiate with regional members/expected members such as
  - Huawei
  - Alibaba
  - VeriSilicon
  - RIOSLab
  - VeriSilicon
  - ICT-CAS
  - CASPA
  - NEC
- Opportunities to deepen collaboration in the region
- Assistance of Danny Hua is invaluable

OpenHW Accelerate

- Multi Year research initiative totaling up to $22.5M USD of co-funded research
  - Up to $4.5M USD research funding per year
  - Funding available globally across Canadian and International Universities (75% Canadian / 25% International)
  - Available to Silver and above OpenHW Group member organizations
- OpenHW Accelerate managed within OpenHW Marketing Working Group
  - University Outreach Task Group Co-Chaired by Mitacs and CMC
  - Establishes project approval process
  - Peer Review Committee drawing on Academic and Industry subject matter experts for project approvals

Stage Gate Overview

Gate	Criteria
PC Project Concept	Concept formulation. Proposed scope. Why do this project?
PL Project Launch	Driving requirements, proposed features, work components, project supporters, high level schedule, project risks, license model
PA Plan Approved	Project plan checklist: project methodology, initial agile backlog, requirements specification (1st section of the user manual)
Project work	
PF Project Freeze	RTL Freeze checklist or other final checklist

Current Projects (post-PC, June 2021)

Responsible TG	Project	Status	Detail
Cores, Verification	CV32E40P	PF	4 stage, Embedded, 32b core
Cores, Verification	CV32E40S	PA	Security focused, 32b core
Cores, Verification	CV32E40X	PA	Extension interface, 32b core
Cores, Verification	CVA6	PL	6 stage, Application, 64/32b core
Verification	FORCE-RISCV	PL	Instruction Set Generator, 64/32b
SW	CORE-V IDE-CDT	PC	Eclipse Embedded IDE supporting CORE-V
SW	CORE-V GNU GCC Tools	PC	GNU GCC Tool chain supporting CORE-V
HW, Verification	CORE-V MCU	PL	FPGA and Prototype chip on GF22
SW	CORE-V LLVM Tools	PC	LLVM Tool chain supporting CORE-V
SW	FreeRTOS	PC	FreeRTOS supporting CORE-V
HW, SW	VERILATOR MODEL	PL	Verilator CORE-V model used for s/w dev
Cores, Verification	CV32E40Pv2	PC	Extension of CV32E40P with PULP instruction support
University Outreach, Cores	CV-VEC	PC	Vector Processor research device

Projects in Project Concept Evaluation

Responsible TG	Project	Status	Detail
Cores	CV-X-IF Extension Interface Specification	PC evaluation	Provides interface from RISC-V processor to external coprocessor executing offloaded instructions
Cores, Verification	CV32E41P	PC evaluation	Compressed Instruction – specification validation to TRL3
Cores, Verification	CV32E20	PC evaluation	Small and light microcontroller
Cores, Verification	CV32E40PV2	PC evaluation	PULP extension isupport for CV32E40P
SW	Hardware Abstraction Layer (HAL)	PC evaluation	S/W Abstraction layer for CORE-V devices

What's Next? Some Predictions…

1. OpenHW Group ecosystem continues to grow
   - Over 80 Members & Partners expected by end of 2021

2. New open-source RISC-V cores added to the CORE-V Family
   - CV32E4 and CV64A6 now – CV32E2, CV32A6, CV32E4 variants and more to come

3. On chip SoC interconnect (fabric & busses)

1. Heterogeneous clusters with accelerators and leveraging eFPGA

and

- OpenHW Group & CORE-V Family of open-source RISC-V cores for use in high-volume production SoCs
  - Visit www.openhwgroup.org for details
  - Learn more at OpenHW TV
- Follow us on Twitter @openhwgroup & LinkedIn OpenHW Group

Questions & Answers

1. From the OpenHW perspective, what do you see as the trend and interest in open hardware, given the recent news on Intel's potential acquisition of SiFive, Intel to make RISC-V chips?

   A: *These developments further the industry momentum behind RISC-V ISA and will lead to further interest in open-source implementations and toolchains.*

1. What's OpenHW's strategy to compete or maybe collaborate with commercial offerings of RISC-V chips from Intel or other commercial vendors? Would you envision a parallel between Linux versus Windows or Android versus iOS scenario in RISC-V?

   A: *OpenHW does not compete with these organizations (or any others). OpenHW is open to collaborate with any organization involved in RISC-V and/or open-source hardware/software development.*

1. What's OpenHW Group's strategy (organizational or project-wise) to ride the wave of broad adoption of RISC-V?

   A: *Our strategy as driven by the Board of Directors of the OpenHW Group, is to develop vendor neutral, open-source IP providing the adopters with true freedom of action to innovate as they see fit.*

1. What is the difference between RISC-V International and OpenHWGroup?

   A: *RISC-V International owns, develops and maintains the Instruction Set Architecture. The OpenHW Group is primarily focused on development of* ***implementations*** *of the ISA.*

1. What is the future direction for OpenHWGroup? What is the organization's vision you want to be?

   A: *CORE-V family, including enabling software, is our first area focus. We will move beyond to fabrics, accelerators and other IP that enables heterogeneous clusters*

Open Source Cross-Group Collaboration

***Case study*: Zce compressed instruction ISA**
Lead contributor for Zce ISA and E41P: Tariq Kurd, Huawei