OpenHW Group Project Execution Framework

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OpenHW Group: Open Source Objectives

Open Source Objective	OpenHW Group
Community collaboration	• Silicon + Hardware + Software + University + EDA Tools • Product-ready baseline features
Enable flexibility and customization	• CORE-V building block approach • Companies differentiate at value-add
Innovation velocity	• Research results flow directly to front end • Collaborative project model • Infrastructure/governance
Industrial quality	• Open scrutiny of all contributions • Focus on Industrial quality verification
Enable freedom of action	• Open source licenses adapted to hardware • Freedom to innovate

OpenHW Overview

- Technical Working Group
  - Cores Task Group
  - Verification Task Group
  - Hardware Task Group
  - Software Task Group
  - Interconnect Task Group
  - Safety and Security Task Group
- Marketing Working Group
- OpenHW CEO + Staff
  - Facilitating/building project capacity
- OpenHW Board
  - Oversight of working group results

Project framework and decisions

Open-source development
Specification development
Driven by Engineering staff of member companies

Industry Best Practices

- Project framework supporting planning, monitoring and community collaboration
- Agile/Hybrid Project organization models adapted to project needs
- Industry standard toolsets along with mindset: industrial quality
- Transparent, open-source contribution process
- Technology Readiness Level assessment of project outputs

Project Execution Framework: Goals

Overall

- Open, lightweight, and effective

Processor-IP + Enabling Ecosystem

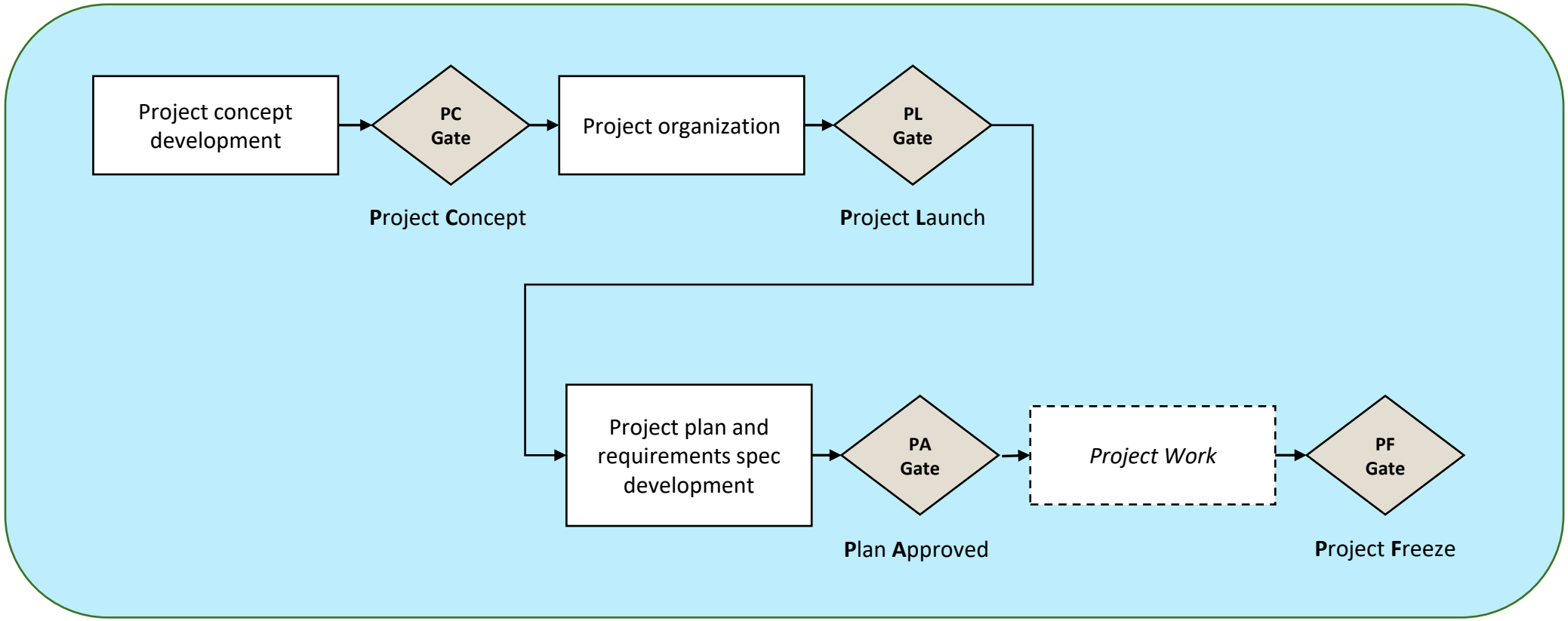
- Provide the checkpoints needed for processor design and verification
- Industry quality, fully verified IP as project deliverables
- Support multiple ecosystem outputs in one framework: RTL, software, hardware, FPGA, MCU, research

Collaborative Way of Working

- Bring project concepts forward at an early stage
- Project decisions in the hands of the members
- Keep the members informed of the full range and status of projects

Stage Gate Flow

- Gate reviews are held at monthly TWG meetings
- Project Team presents review materials
- Gate decisions by TWG majority vote



Gate Details

Gate	Criteria
PC Project Concept	Concept formulation. Proposed scope. Why do this project? Early view of PL details where available.
PL Project Launch	Driving requirements, proposed features, work components, project supporters, high level schedule, project risks, license model
PA Plan Approved	Project plan checklist: project methodology, initial agile backlog, requirements specification (1st section of the user manual)
Project work	
PF Project Freeze	RTL Freeze checklist or other final checklist

Cores Projects – Document Suite

1. Requirements (Feature) Specification
2. User Manual
    a. Chapter 1 = Requirements
3. Verification Architecture
4. Verification Plan(s)
5. Design Document(s) (optional for specific needs)

Plan Approved Checklist - extract

Item	Completion (Y/N/In progress/NA)	Comment
Project Concept Complete		
Project Launch Complete		
SW Target platform identified		
Cores Part Number identified		
Cores TRL Target identified		
Project release plan identified		
HL Project deliverables identified		
Feature list available		
Resource plan available		
Repo setup		
License.md file in place		
Project Manager identified		
Technical Project Leader per deliverable identified		
At least 1 project committer elected		
Work Breakdown Structure available		
Baseline schedule available		
Ongoing schedule tracking identified		e.g. Github project board
Regular project meeting setup		
Project Monthly report format agreed		
Risk Register available		
Set of Project Freeze/Release Checklists identified		

RTL Freeze Checklist - Example

- Design rules
- Coding rules
- Linting

- Verification planning
- Code coverage
- Functional coverage
- Regression suites
- Final report

- All IP reviews complete

master — core-v-docs / program / milestones / CV32E40P / **RTL_Freeze_v1.0.0** /

MikeOpenHWGroup Summary of issues found for cv32e40p_v1.0.0 (#332) ...

..	
Reports	Summary of issues found for cv32e40p_v1.0.0 (#332)
DesignChecklist.md	Added hash for frozen RTL
Design_openissues.md	update design open issues for RTL freeze
DocumentationChecklist.md	Added hash for frozen RTL
Documentation_openissues.md	Added hash for frozen RTL
FormalVerificationChecklist.md	checklist update
IPChecklist.md	SignOff IP Checklist
README.md	Match directory name to tag name (#288)
SimulationVerificati…hecklist.md	Update URL for final reports
Verification_openissu…	Fix formating

- OpenHW Checklists
  - Detailed sign-off metrics
  - Established Criteria
  - Actual signoff by a project committer
- When the set of Checklists is completed and reviewed
  - The project is “frozen”
  - A Github tag is created for the release
  - Eclipse Release process initiated

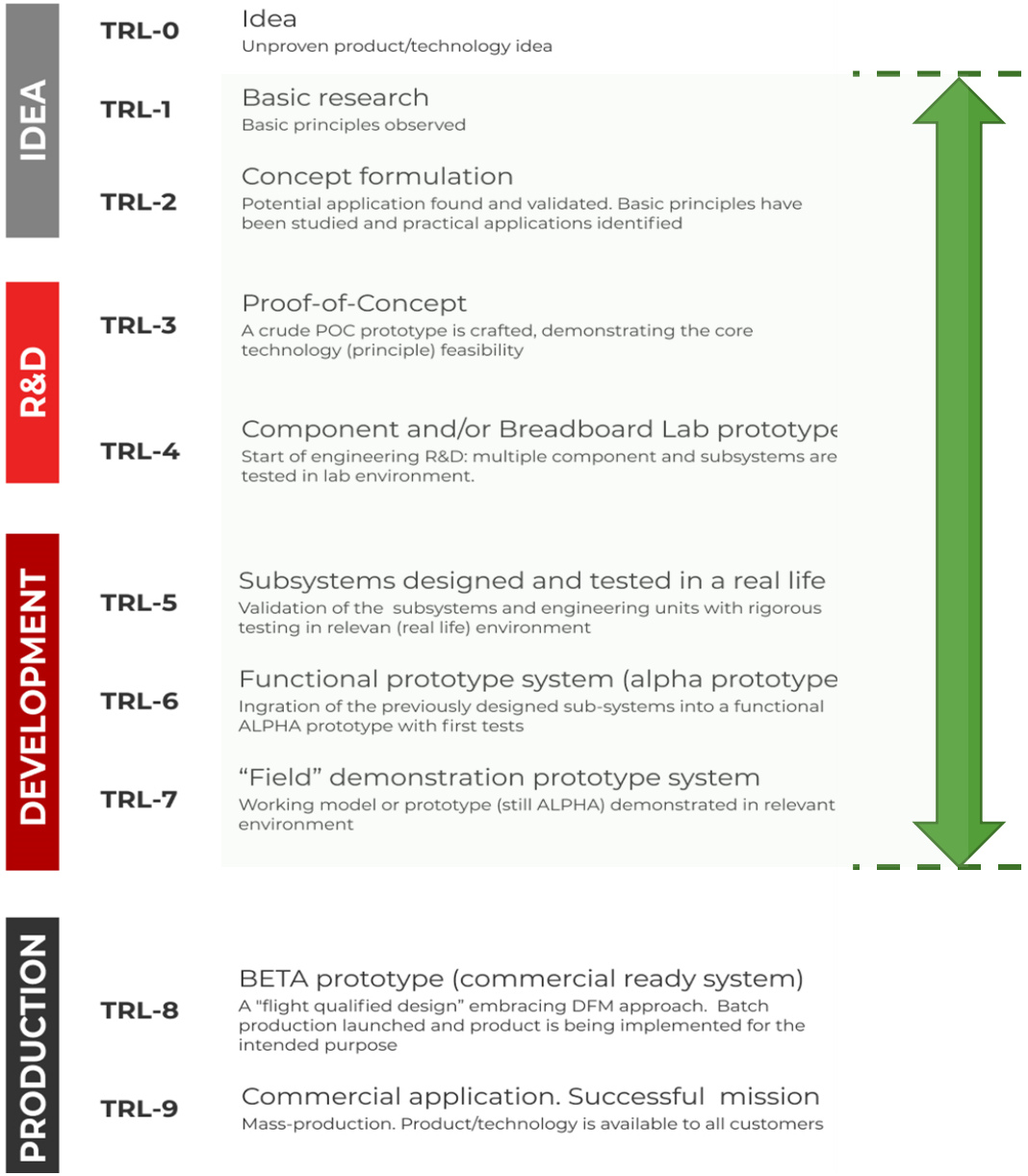
Project/Teams Organization

- Project organization
  - TG chairs play a significant role in project oversight
  - Technical Project Leader(s) drive project coordination
  - Regular project and TG meetings
  - Open messaging channels (Mattermost, email)
- Many projects use Github Project Boards
- Top level schedule view (Waterfall) to at least a coarse granularity often used to initially flesh out a project schedule and create the project board
- Coordination at TWG level
  - Cross-project coordination – for example simulator support for s/w development
  - Project gate reviews
  - Requirements specification review

Current Projects

https://github.com/openhwgroup/programs/tree/master/Project-Descriptions-and-Plans

TRL Scale



OpenHW Technology Outputs

OpenHW IP Adopters

TRL Levels as Utilized by OpenHW

TRL	OpenHW Utilization
1-Basic Principles Observed	• **OpenHW research projects** may target TRL-1 as project output, e.g. to develop novel approaches to core or accelerator architecture
2-Concept Formulation	• Core IP or accelerator development projects to produce open source technology are typically initiated as TRL-2 concepts, identifying principles and applications of the IP • The **OpenHW Project Concept Gate** includes a TRL-2 description of the Core IP
3- Proof of Concept	• Core IP or accelerator development projects will pass through TRL-3 as **the (RTL) design completes**. Poof of concept is shown by core compilation and demonstration of basic operations (e.g. Linux booted, coremark results, hello-world)
4- Component Prototype	• Core IP or accelerator projects will pass through TRL-4 as they produce **preliminary PPA results** (via synthesis scripts for FPGA or ASIC) and/or **run preliminary application code**, such as an accelerator running machine learning code.
5- Subsystem Designed and Tested	• Core IP projects reach TRL-5 as they **complete full verification**. The OpenHW RTL Freeze checklist process verifies that the design is fully ready for industrial adoption.
6-Functional (Alpha) Prototype	• OpenHW **designed IP that is integrated into an MCU system** or other device reaches TRL-6 as prototype Silicon is fabricated and demonstrated
7-Field Demonstration Prototype	• **OpenHW development boards** incorporating a prototype Silicon system with OpenHW Software reach TRL-7 as they are demonstrated and deployed

OpenHW and Eclipse Foundation

Processor-specific Ecosystem Requirements

OpenHW Project Framework

- Project Proposals and Selection
- Stage Gate Reviews
- Project Freeze Checklist
- Team Organization
- Continuous Integration
- Technology Readiness Level

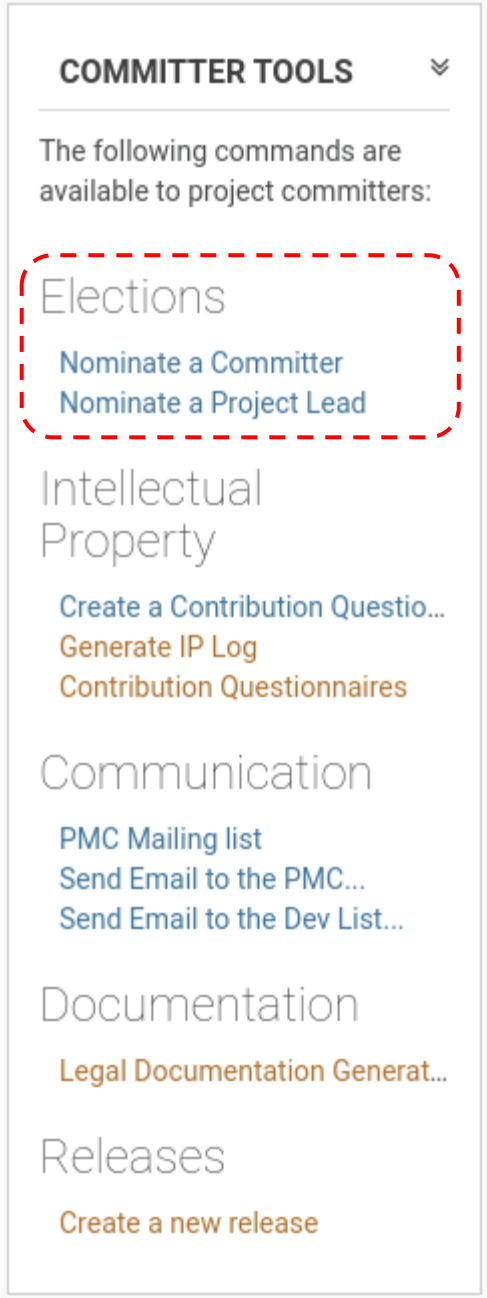
Open source foundation

Eclipse Development Process

- Contribution Process
- Intellectual Property Review
- Committer Responsibilities
- Committer Elections
- Release Management

Committers and Contributors

- "Committer meritocracy"
- Committers are project stewards and have write access
  - Committer duties
    - maintain vendor/employer neutrality
    - operate transparently
    - enforce IP policy
    - review pull requests
  - Merit shown through a pattern of contribution
  - New Committers elected by existing committers
- Any person who has signed the contribution agreement can make a pull request
- Both Committers and contributors need to sign appropriate contribution agreements



Licenses and IP Review

- Permissive project licenses
  - Solderpad 0.51/2.0
  - Apache 2.0
  - EPL 2.0
- Automated Git review of Pull Request
  - Ensure contribution agreements in place
- IP reviews on large contributions
- IP review on 3rd party content before it can be included in any release
  - Must be distributed under approved open source

Pulling it All Together

- OpenHW – CORE-V Ecosystem Development
  - Full range of ecosystem projects – hardware and software
  - Industrial project management methods
  - Stage Gates and Checklists
  - Industry standard verification tools
  - Agile teams
  - Comprehensive open source flow
  - Full transparency of all artifacts
  - Technology Readiness Level assessment to identify the target output
- Project dashboard at https://github.com/openhwgroup/programs/tree/master/dashboard