CORES TG – February 5 2024

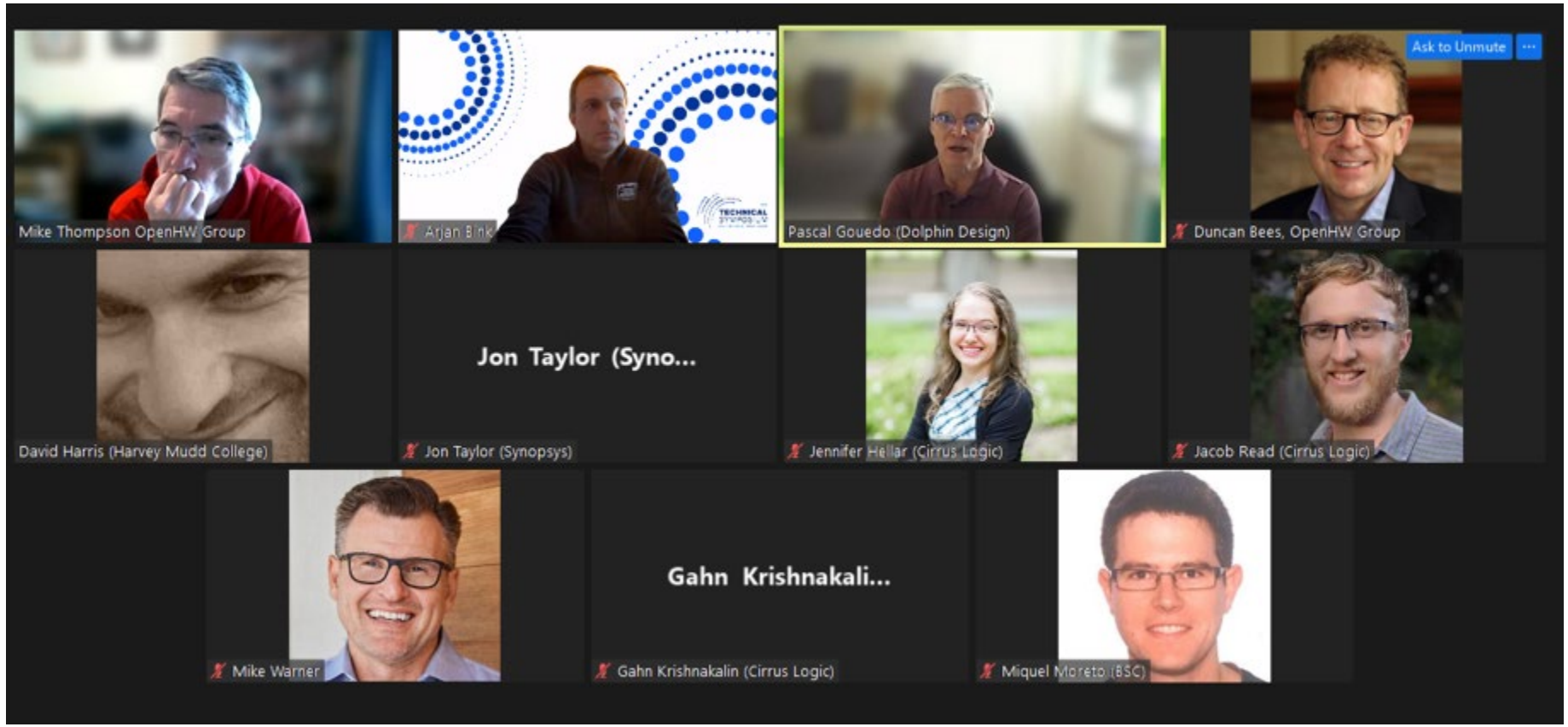
Arjan Bink

Jérôme Quevremont

Davide Schiavone

OPENHW GROUP™
PROVEN PROCESSOR IP

Attendance


Mike Thompson OpenHW Group
Arjan Bink
Pascal Gouedo (Dolphin Design)
Ask to Unmute
Duncan Bees, OpenHW Group
David Harris (Harvey Mudd College)
Jon Taylor (Syno...
Jon Taylor (Synopsys)
Jennifer Hellar (Cirrus Logic)
Jacob Read (Cirrus Logic)
Mike Warner
Gahn Krishnakali...
Gahn Krishnakalin (Cirrus Logic)
Miquel Moreto (BSC)

Agenda

- Cores plan of record – updated timeline plan (Duncan)
- CVA6 workshop (Mike Thompson)
- CV32E40Pv2 status (Pascal Gouedo)
- RTL freeze checklist (Pascal Gouedo)

Cores plan of record – updated timeline plan

Duncan Bees

CVA6 Workshop

Marseille, 16-18 January 2024

Some contributions to CVA6 are supported by the FRACTAL, TRISTAN and ISOLDE projects, which have received funding from the Chips Joint Undertaking (Chips JU), Austria, Belgium, Czechia, Finland, France, Germany, Italy, the Netherlands, Poland, Romania, Sweden, Switzerland, Spain and Turkey under grant agreements 877056, 101095947 and 101112274. The JU receives support from the European Union's Horizon Europe research and innovation program.

A joint open-source initiative

with members and staff

Task 2.4 (Application processor) partners

Some contributions to CVA6 are supported by the FRACTAL, TRISTAN and ISOLDE projects, which have received funding from the Chips Joint Undertaking (Chips JU), Austria, Belgium, Czechia, Finland, France, Germany, Italy, the Netherlands, Poland, Romania, Sweden, Switzerland, Spain and Turkey under grant agreements 877056, 101095947 and 101112274. The JU receives support from the European Union's Horizon Europe research and innovation program.

Participants

Goals

- Better know other CVA6 contributors
- Share knowledge, updates, upcoming features
- Identify possible cooperations, to mutualize efforts, especially on verification
- Identify solutions to manage more CVA6 configurations

CVA6 configurations

Upcoming verified configurations:

Part#		Led by	Domain
CV32A60AX	32-bit application core	10xEngineers	SoC design services, vision
CV32A60X	32-bit embedded core	Thales TSS	Security
CV32A65X	32-bit embedded core, dual issue	Thales TSS	Security
CV64A60AV	64-bit application core, interface to vector coprocessor	Axelera	AI acceleration
"Petit Robert"	32-bit real-time core, safety features	Bosch	Automotive
"Grand Robert"	64-bit application core, safety features	Bosch	Automotive

The teams will populate together the "High-level Features" list for their CVA6 configurations.

Highlights

- Focus on verification (DVplans, UVM agents, testbench, Spike…) and cooperations between configurations
- Need to customize the release process to accommodate several configurations
- Memory ECC considered in several configurations
- I+D scratchpad under way
- Dual-issue CVA6 under way: +40% CoreMark/MHz (expect +45%)
- Adoption of HPDCache considered
- LLVM in addition to GCC
- 10xEngineers: cloud-based RISC-V computing (incl. CVA6 on AWS F1)
- ETH research: Fast interrupts, virtualized interrupts, timing channel prevention, coherence&consistency

CVA6 project management needs an update

Latest TWG gate needs update

Divide and conquer to manage complexity

Optimize effort sharing

Keep a common RTL (with parameters)

Still be able to accept relevant evolutions (but be selective)

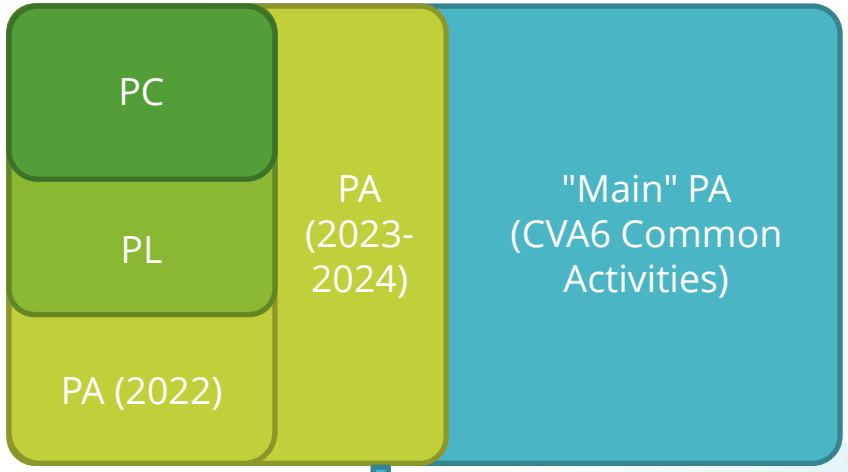
More configurations to verify

Document the family and the configurations

Varying verification goals: commercial grade, ISO 26262, Common Criteria…

Evolution of CVA6 project structure

past | upcoming



Sister projects: CVA6-H, HPDCache...

Arbitrary time scale

Spin off verification sub-projects

- PA CV32A60AX
- PA CV32A60X
- PA CV32A65X
- PA CV64A60AV
- "Petit Robert"
- "Grand Robert"
- Others...

CV32E40Pv2 status

Pascal Gouédo

Yoann Pruvost

Bee Nee Lim

OPENHW GROUP™
PROVEN PROCESSOR IP

Project

- Project
  - Design & Verification meeting
    - Wednesday 14:00 CET every 2 weeks(Ical)
  - Dedicated technical meetings when needed
  - Reporting to Cores TG

- Mattermost channels
  - TWG : Cores : CV32E4*P
  - TWG : Verification

- Resources
  - Pascal Gouédo
    - Specification, Design, Verification & Formal
  - Yoann Pruvost
    - Design, Verification & Formal
  - Bee Nee Lim
    - Verification leader
  - Xavier Aubert
    - Verification
  - Bao Shan Mak
    - Verification
  - ~~Vaibhav Jain~~
    - ~~Verification~~

- OpenHW staff
  - Mike Thompson
    - Verification support
  - Davide Schiavone
    - Architecture & Design support

User Manual

- Automatic dev to master merge broken for 2 months.
  Can’t make new release and User Manual.
- v1.5.x
  - Corrected MPEC/MEPC typo error in User Manual (PR #927)
  - Additional advice when setting up HWLoops. (PR #932)
  - Issue #937 (HW Loop Constraints question) corrections (PR #940)
  - User Manual html generation improvments (PR #942)
  - Added clipr/clipur note about rs2 (PR #944)

Design

- Lint script for Siemens tools pushed to CV32E40P git repo
- Starting to have implementation numbers to be added in User Manual

- No new RTL issue since November 8, 2023

- RTL/Imperas model mismatch on ebreak/debug request prioritization
  - RISC-V Debug v1.0.0-rc1 spec has backward compatibility with v0.13.2 on that point. Debug spec doesn't give any timing related priority.
  - Correction on CV32E40P to have same behavior among CORE-V cores?
    - ⇨ Will break Logic Equivalence Checking with respect to v1!

Verification : Non-regressions

- core-v-verif environment
  - Correcting RVFI tracer for instructions/events corner cases
  - Coverage files improvements
- Non-regression results
  - 4 non-regressions ran on 7 configurations
    - Total of 27 non-regressions
  - 17743 tests run
  - 0,5 % failing tests (94)
    - Mainly timeouts to fix
    - Some assembly compilation problems

Verification : Coverage analysis

- Simulation RTL Code Coverage analysis on PULP configuration
  - Statement: 96% Condition: 87%
  - Tests improvements (illegal instructions, corner cases,…)
- Combined Simulation and Formal Verification results
  - Successfully merged ucdb files from Simulation and Formal Verification
- Functional Coverage on PULP_FPU_0-cycle-latency
  - FPU: 91% HWLOOP: 85% Debug: 98% OBI: 59%
    Interrupts: 0% (v1 cov file relying on old isaCOV ⇨ conversion to RVVI COV IF)
- Waivers
  - v1 waivers analysis done
  - v2 waivers creation/refinement on-going

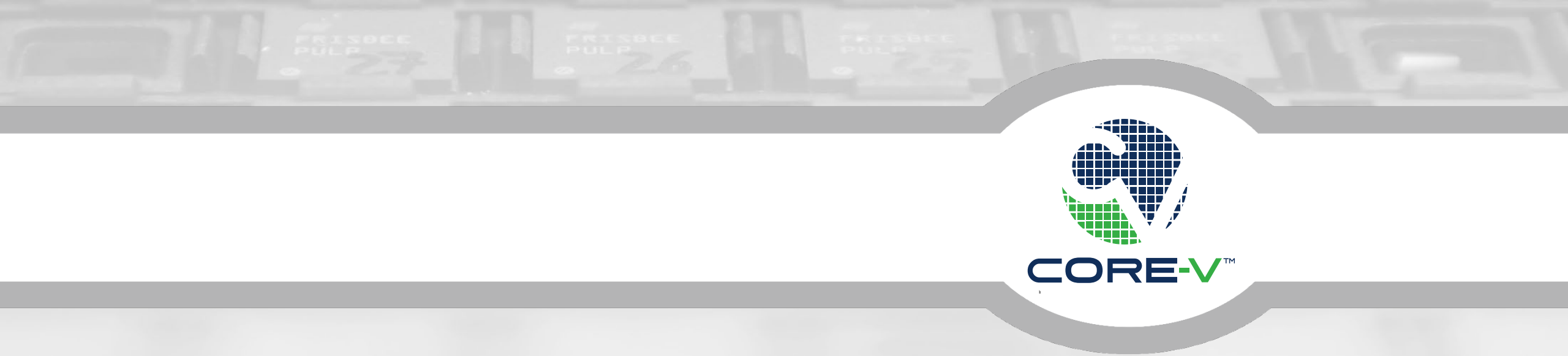
Tools

- SW toolchain deliveries:
  - Some releases since December 2023. Latest one is January 14, 2024.
  - Verilator model of X-Heep platform not working
  - X-Heep platform FPGA mapping for Nexys A7 up
    ⇨ gdb connexion working fine

- Imperas
  - 1 Reference Model release since December
    - Hwloop constraints checking partly implemented
  - 1 CV32E40Pv2 riscvISACOV coverage files release since December
    - Low level macro enables available but need refinement because of compilation failure
    - PULP finer grain macro enables to propose

TRL-5 RTL release

- Due to people resources number reduction on CV32E40Pv2, Project Freeze is now forecasted e/o Q1 2024.



RTL Freeze checklist

Pascal Gouédo

February 5, 2024

Possible improvements

- Some tabs could be enriched with additional information
  - RTL Design
  - Verification
  - Formal Verification
- Some tabs could be added concerning as different topics as
  - Physical Implementation
  - Software Toolchain
  - Tools list and Versions
  - Any additional ideas?

RTL Design

- For Coding rules, maybe add a line about which formatting tool as been used (verible…).
- For linting, maybe mention which tool has been used as a sign-off criteria.
- Mention which tool has been used for “Combinational loops”, “Multicycle path” and “No Latch” checks.

Verification

- Coverage
  - Only 100% Block/Statement and Condition metrics are mentioned to be achieved.
  - There are a lot of RTL cases which are only seen by Branch coverage but not Condition coverage resulting in coverage holes:
    - if (id_ready) begin
    - case values
    - signals used as case conditions
  - It is important to add 100% Branch coverage metric to cover those holes.

  - It is even mentioned that MC/DC (Modified Condition/Decision Coverage) required by Safety critical software could be used for hardware.

Formal Verification

- A category about assertions generator (if relevant) could be added.
- Generator
  - Tool name
  - Output format
  - Setup and scripts

Physical Implementation

- As this checklist is used to certify that concerned RTL is at TRL-5 level (Industrial grade ready for production), releasing this RTL without any physical implementation is somewhat … never seen in Industry world.
- During Core selection, PPA metrics are as important as TRL level.
- It also allows to highlight and develop any mandatory constraint/exception file to deliver together with the RTL to be able to physically implement it.
- Also allows to answer to RTL design rules questions like “Combinational loops”, “Multicycle path” and “No Latch”.

Software Toolchain

- If the toolchain is improved/changed/augmented with new instructions and is mandatory to use RTL targeted by this checklist, some information should be listed in a new specific tab:
  - Documentation
  - Where to find its source and pre-generated packages
  - How it has been verified?
  - …

Tools list and versions

- It is always interesting to have a list of all the tools (version and even OS) which have been used to achieve all the goals and to be able to reproduce all the metrics reported in the RTL Sign-Off checklist.
- It concerns as different areas as
  - EDA tools for verification, physical implementation…
  - Models of any kind
  - Software tool chain
  - Miscellaneous tools like python, verible…

Thank you!