CORES TG – May 6 2024

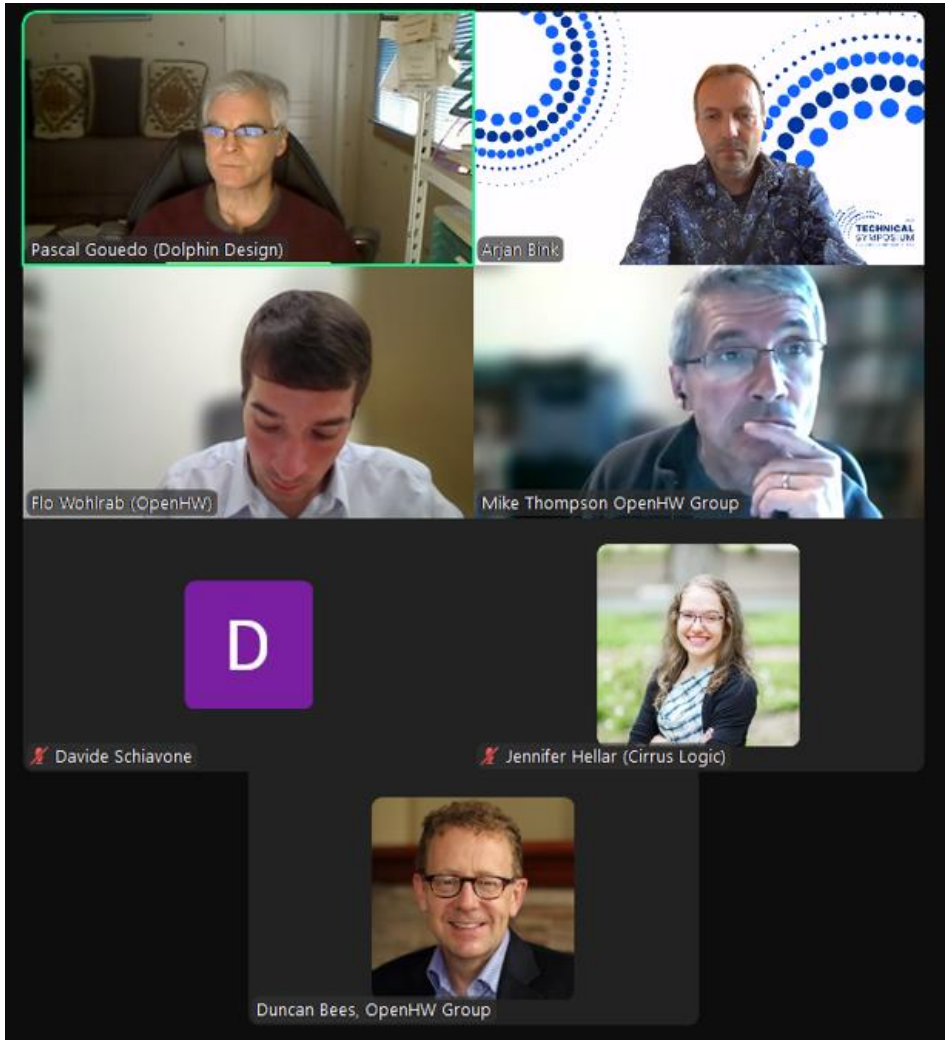
Arjan Bink

Jérôme Quevremont

Davide Schiavone

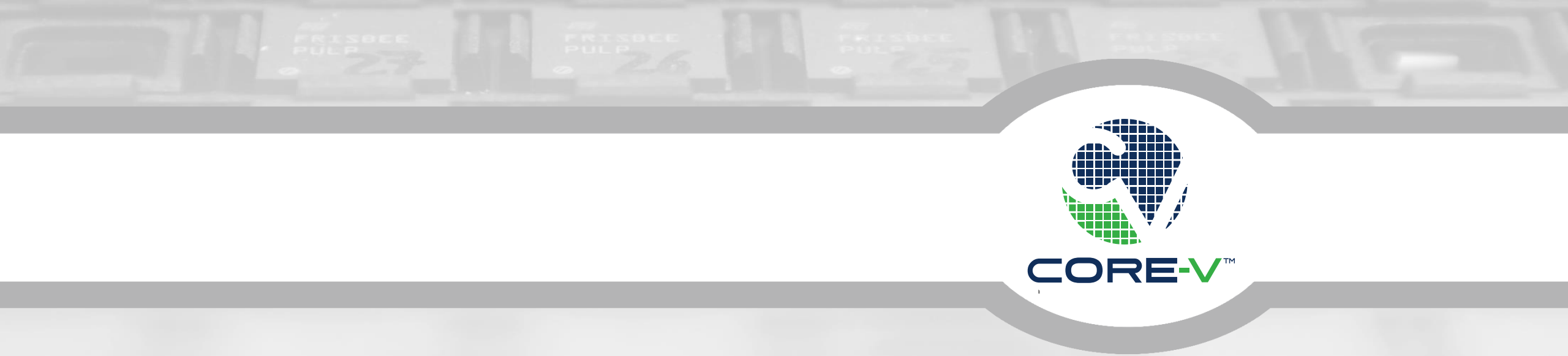
OPENHW GROUP™
PROVEN PROCESSOR IP

Attendance


Pascal Gouedo (Dolphin Design)
Arjan Bink
Flo Wohlrab (OpenHW)
Mike Thompson OpenHW Group
D
Davide Schiavone
Jennifer Hellar (Cirrus Logic)
Duncan Bees, OpenHW Group

Agenda

- CV32E40Pv2 status (Pascal Gouédo)
- CVE20 monthly report (Duncan Bees)



CV32E40Pv2 status

Pascal Gouédo

Yoann Pruvost

Bee Nee Lim

May 6, 2024

Project

- Project
  - Design & Verification meeting
    - Wednesday 14:00 CET every week (Ical)
  - Dedicated technical meetings when needed
  - Reporting to Cores TG

- Mattermost channels
  - TWG : Cores : CV32E4*P
  - TWG : Verification

- Resources
  - Pascal Gouédo
    - Specification, Design, Verification & Formal
  - Yoann Pruvost
    - Design, Verification & Formal
  - Bee Nee Lim
    - Verification leader
  - Xavier Aubert
    - Verification
  - Bao Shan Mak
    - Verification

- OpenHW staff
  - Mike Thompson
    - Verification support
  - Davide Schiavone
    - Architecture & Design support

User Manual

- **Automatic dev to master merge broken for 4 months**
  Release and User Manual created from dev branch
- v1.6.0
  - Corrected MPEC/MEPC typo error in User Manual (PR #927)
  - Additional advice when setting up HWLoops. (PR #932)
  - Issue #937 (HW Loop Constraints question) corrections (PR #940)
  - User Manual html generation improvments (PR #942)
  - Added clipr/clipur note about rs2 (PR #944/#956)
  - Additional details on HW Loop + FPGA synthesis with AMD® Vivado® and Intel® Quartus® (PR #956)
- v1.7.0
  - Better clipr/clipur description (PR #970)
- v1.7.1
  - Refined HW Loop instructions needing 32-bit alignment (PR #973)
  - Reworked v2.0.0 verification section (PR #976/#978)
- v1.8.0
  - Refined Imm6 description for some XPULP SIMD instructions (new illegal instruction exception cases) (PR #984)
- v1.8.1
  - Refined HW Loop CSRs save/restore section (PR #987)

Design

- **1 new RTL issue found since November 8, 2023 (Issue #975)**
  - Highlighted by a new test created for RTL Code Coverage holes

- v1.6.0
  - Some corrections for verilator (PR #952)
  - Updates for better RTL code coverage (PR #959/#960)
- v1.7.0
  - Restored v1 headers and updated copyrights and SHL (2.1) of all modified files (PR #964)
  - Improved FPU clock gating (PR #966)
  - Aligned clipr/clipur behavior to v1.7.0 User Manual (PR #971)
- v1.7.2
  - Bug issue #975 correction (PR #980)
- v1.8.0
  - PR #985
    Code cleanup for better RTL code coverage
    Added SIMD illegal instruction exception decoding on unused Imm6 bits for some SIMD instructions (User Manual v1.8.0)
    Code change to remove SiemensEDA Tessent fatal error

Verification : Non-regressions

- v1.8.1 RTL tag & v1.8.1 core-v-verif tag
- core-v-verif environment
  - RTL & Functional Coverage improvements & Waivers refinement
  - Correcting RVFI/RVVI for instructions/events corner cases
  - Aligned RVVI instructions log Tracer to old one and added new information (cancelled instructions)
- Non-regression results
  - Riscof Architecture tests passing on 4 PULP & PULP_FPU configurations
  - 4 non-regressions ran on 7 configurations
    - Total of 27 non-regressions
  - 32629 tests run, 28 failing tests (0,09 %)
    - 23 Debug corner case already known as tricky/impossible to align to RTL ⇨ To brainstorm again with Imperas
    - 2 Debug corner case reported as ISS mismatch while it shouldn't ⇨ Sent to Imperas
    - 1 auto-modifying test ⇨ Test to fix
    - 2 tests having stack overlap with virtual peripherals ⇨ Tests to fix

Verification : Coverage analysis

- Main work for last month is to cover remaining RTL Code Coverage & Functional Coverage holes
  - 1 hole shown a real RTL bug (Issue #975: Hardware Loop last instruction)
  - Tests improvements (illegal instructions, corner cases,...)

- Simulation RTL Code Coverage results
  - PULP configuration — Statement: 99.8% — Branch: 99.5% — Condition: 98.7%
  - PULP_FPU_0CYCLAT configuration — Statement: 99.9% — Branch: 99.5% — Condition: 97.5%

- Functional Coverage results
  - **Combined from 7 configurations** using PULP_FPU_0CYCLAT as master

    FPU: 100% — HWLOOP: 100% — Debug: 100%

    Interrupts: 100% — OBI: 100% — Assertions & Directive: 100%

    riscvISACOV: 94.9%
  - **Combined from 3 configurations** using PULP_ZFINX_0CYCLAT as master

    ZFINX: 99.9%

Verification : Remaining RTL coverage holes

- cv32e40p_controller: 12 causes resulting in 24 holes
  - 3 will be waived with a specific issue explaining why
  - 18 concern RTL lines specific to HW Loop with corner case conditions
    - After a lot of RTL and waveforms analysis, not sure that they are real conditions.
    - Impossible to formally prove it up to now.
  - 1 concerns AllFalse branch case of an If not having an else
    - Not sure it is a real case. Impossible to formally prove it up to now.
  - 2 concern specific Debug corner case conditions
    - Tricky to stimulate even in directed test
- cv32e40p_ex_stage: 5 holes
  - 4 proven using formal with new assertions
  - last one work-in-progress
- Shared analysis file for cv32e40p_controller
  - Help is welcome

Formal Verification

- On v1.8.0 RTL tag, Control and Datapath assertions checking runs launched on 3 configurations
  - PULP
  - PULP_FPU (0 cycle latency)
  - PULP_FPU_ZFINX_2CYCLAT (2 cycles latency)

- Successful unbounded check on PULP configuration (11 days)

- Control and Datapath checks running in parallel on PULP_FPU & PULP_FPU_ZFINX_2CYCLAT (still running after 18 days)

Tools

- SW toolchain
  - 2 releases since February 2024. Latest one is April 7, 2024.
  - Toolchain verification with X-Heep platform on Nexys A7 FPGA on-going

- Imperas Reference Model
  - 6 releases since February 2024. Latest one is May 1st, 2024.
    - Hwloop constraints checking finalized
    - 1 Debug corner case impossible to align on RTL
  - 4 riscvISACOV coverage files releases since February 2024.
    - CV32E40P coverage numbers (shown during Embedded World 24)

    Covergroups: 94.9% Covergroup Bins: 97.6%

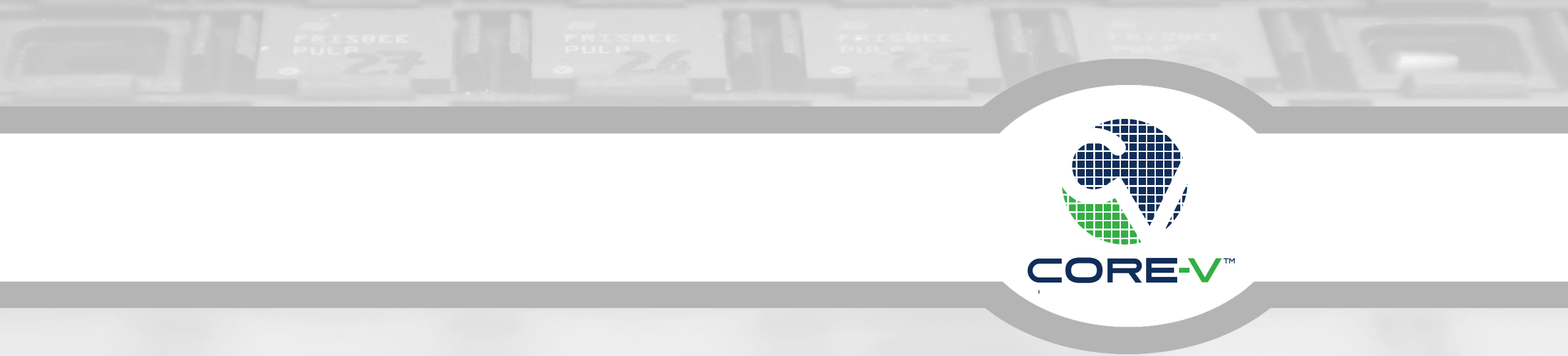
RTL Freeze preparation

- Started to fill RTL Freeze checklist

- But still a lot of issues/reports to create

TRL-5 RTL release

- Uncovered RTL Coverage holes are jeopardizing RTL Freeze. Trying to find either formal or other solution to prove they are either unreachable or can be safely waived.
  - That's why we need OpenHW Group community help to converge or decide.



CVE20 monthly report

Duncan Bees

May 6, 2024

Thank you!