CORES TG – November 8 2021

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PROVEN PROCESSOR IP

Agenda

- CV32E40Pv2 status
- CV32E40X / CV32E40S status
- CVA6 status
- RISC-V profiles

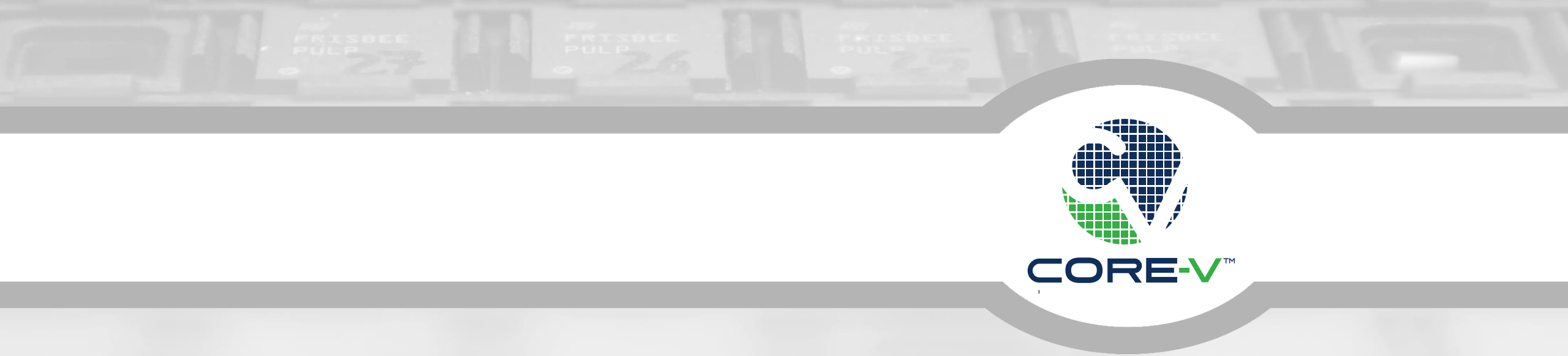
CV32E40Pv2 status

Pascal Gouédo

CV32E40Pv2

- Plan
  - All tasks list until TRL-5 (Specifications, Design, Verification, Implementation trials) created, quoted and reviewed with Davide, Mike and Duncan
  - Between 14 and 20 m.M (w/o risk factor) with 60-70 % on verification

- Resources and Schedule
  - Target is to start in January 2022 and to finish in June/September 2022



CV32E40X / CV32E40S status

Øystein Knauserud

CV32E40X

- NMI/LSU bus error support
  - DSCR.nmip
- Fence.i handshake
- Performance counter events implemented
- Timing optimization
  - minstret and related counters
  - IF stage/alignment buffer
- irq_ack_o and irq_id_o removed
- Write buffer implementation near complete
  - PMA update: Only data writes will be bufferable
- Updates for RISC-V Privileged spec v1.12 and RISC-V Debug v1.0.0
- Bugfixes and github issues

CV32E40X – core-v-xif

- Core-v-xif implementation started
  - Commit, issue and result
  - Timing constraints
- New contributor: Michael Platzer (Technische Universität Wien)
  - “Vicuna” Vector coprocessor (https://github.com/vproc/vicuna)

CV32E40S

- Weekly merges from E40X repository
- RVFI updates for user mode and PMP
- Register file ECC
- Alert outputs (major and minor)
- User mode controller integration
  - Privilege level and hazards
- Updates for RISC-V Privileged spec v1.12 and RISC-V Debug v1.0.0
- Bugfixes and github issues

OneSpin status

- CV32E40X has been reported to be passing OneSpin checks
- Way of working and progress still considered a bottleneck
  - Need insight in performed checks
  - Need setup for various CV32E40X configurations
  - Need setup for various CV32E40S configurations
  - Need (near daily) reports

CVA6 status

Jérôme Quévremont

CVA6: current activity

- Specification (link)
  - Google Docs → ReadTheDocs ongoing
  - OVPSim questionnaire reviewed
- CV-X-IF: taking part in specs with CV32E40X
- Design:
  - Complete CV32A6 available in https://github.com/openhwgroup/cva6
  - Speed up CV32A6:
    - Kintex 7 FPGA: 66 → 99 MHz
    - 3 modifications around MMU+PMP
  - Upcoming: more optimizations
  - Investigating divider speedup (nb of cycles divided by ~3)
- Verification:
  - Implemented CSR access tests based on YAML description
  - Opportunity to share fpnew verification with CV2E40Pv2
- SW:
  - FreeRTOS: progressing
  - Updated Linux 32b and 64b available in https://github.com/openhwgroup/cva6-sdk
  - LLVM activity

RISC-V Profiles

Jérôme Quévremont

CORE-V roadmap and profiles

- OpenHW TV episode broadcast on November 8th
  - https://newsroom.eclipse.org/news/announcements/register-openhw-tv-s2e08-core-v-cores-risc-v-profiles-november-8
- RISC-V references:
  - https://docs.google.com/spreadsheets/d/1A40dfm0nnn2-tgKIhdi3UYQ1GBr8iRiV2edFowvgp7E/edit#gid=951478947
  - https://docs.google.com/document/d/1iawUS0zi43bJnDdkr6Hf1pTSjABzFO1MrhQ94FluT9M/edit

Decoding profile names

RVA20[USM]64

RVM20M32

Contradictory information?

extension name - best guess	ratification package name	RVI20		RVA20 (64 only)				RVM20				RVA22 (64 only)				RVM22				RVA23				RVM23			
		m - mandatory, s - supported optional, u - unsupported optional, i - incompatible, x - not ratified at the date of the profile, n - not applicable																									
		RVI32 is only applicable to RVM and RVI profiles																									
				Mode				Mode				Mode				Mode				Mode				Mode			
			parameters	U	S	M	parameters	U	S	M	parameters	U	S	M	parameters	U	S	M	parameters	U	S	M	parameters	U	S	M	parameters
I	RVI32	m		m	m	m		m	m	m		m	m	m		m	m	m									
I	RVI64	m		m	m	m		m	m	m		m	m	m		m	m	m									
M	M	s		m	m	m		s	s	s		m	m	m		s	s	s									

➔ Take the next slide with a pinch of salt

Tentative RISC-V Profile Mapping

CORE-V	RISC-V Profile	Comment
CV64A6	RVA20[USM]64	At full configuration
CV32A6	RVM20[USM]32	At full configuration
CV32A5	RVM20[USM]32	At full configuration
CV32E40P CV32E40Pv2	RVM20M32	
CV32E40X	RVM20M32	
CV32E40S	RVM20[UM]32	
CV32E41P	RVM20M32	
CV32E20	RVM20M32	

Information provided as is without any warranty.

Thank you!