CORES TG – May 14 2020

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Introductions

- Arjan Bink (Chair)
- Jérôme Quevremont (Vice-chair)
- Davide Schiavone (Director of Engineering)
- Everybody on the call
  - Welcome!
  - Can you please introduce yourself?

Outline

- Scope / charter
- Cores
- Status of CV32E40P
- Call to action
- Next meetings

Scope / Charter

- Provide support to the OpenHW TWG*, specifically in aiding the definition of the cores IP roadmap and selection of donated core IP
- Obtain, develop, and, maintain selected donated and new Core IPs based on Roadmap
- Alignment and ratification of feature proposals and contributions from members and the open-source community
- Planning and coordination of development efforts, including assignment and tracking specific features, issues, and documentation tasks
- Open-source delivery of production quality IP core releases guaranteed to inter-operate with industry standard tools, flows, and interfaces including relevant documentation
- Generation and maintenance of OpenHW specific standard proposals
  - Contribution to the RISC-V foundation via relevant proposals (as required)

* Actual roadmap definition and donation acceptance is performed at TWG level using inputs from our Cores TG and the other TGs

Cores – Under design/verification* or under discussion

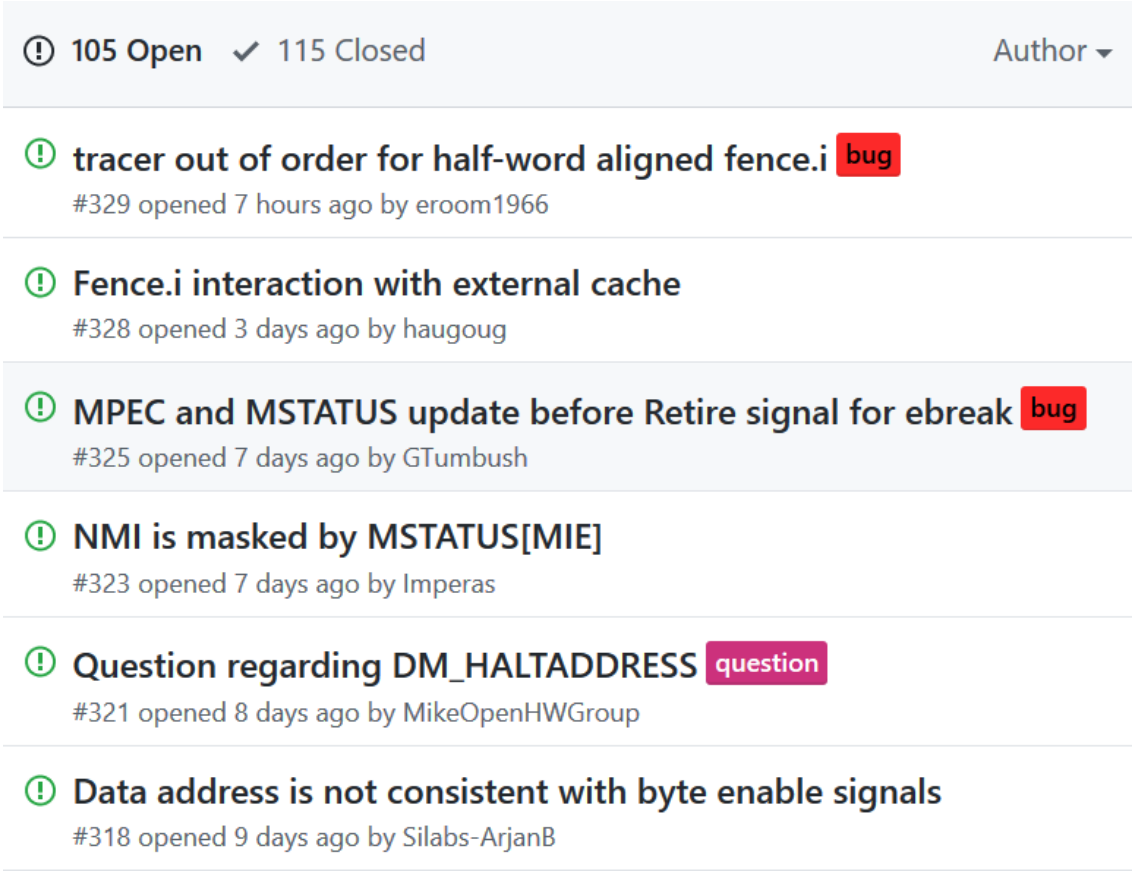
Core	Family	Key features	State	Comment
CV32E40P	CORE-V	RV32IM[F]CZfenceiZicsrXpulp[Xpulpzfinx] M-mode, OBI bus interfaces, CLINT, 4-stage pipeline	Feature set frozen Under design/verification	RI5CY
CV32E40	CORE-V	RV32IM[F]CBPZfenceiZicsr[Zfinx]Xpulp PMP, M/U-mode, OBI bus interfaces, CLIC, 4-stage pipeline	Feature set proposed Schedule after CV32E40P Optional Atomic extension?	
CV64A	CORE-V	RV64IMA[F,D]CZicsr M/S/U-mode, AXI bus interfaces, Caches, MMU, TLB, 6-stage pipeline	Ariane still maintained by ETH Zurich PULP team; when to move to OpenHW? B extension?	Ariane
CV32A	TBD	RV32IMA[F]CZicsr M/S/U-mode, AXI bus interfaces, Caches, MMU, TLB, 6-stage pipeline	Concept proposed by Thales Additional safety/security features? Hypervisor mode? CV32A optimized for FPGA? B extension?	32-bit Ariane

* Agreed earlier to limit initial design verification effort to one core (as initial infrastructure is under development)

Status of CV32E40P

- Design changes done
  - Interrupt architecture changed to Basic (a.k.a. CLINT)
  - Using the agreed parameter set
    - Hardware Loop parameterization
  - Bus interface improvements
  - Tracer for verification (Imperas)
- Design changes in progress
  - Debug trigger module
  - Convert performance counters
  - Sleep pin

- Drive to get issues closed



Call to action

- Asking for contributors to help fixing issues from https://github.com/openhwgroup/cv32e40p/issues
  - RTL fixes
  - Documentation
  - Questions
  - Future improvements (e.g. PMP, User mode)
- Asking for contributors to
  - Drive finalization of CV32E40 feature set discussion
  - Drive adoption of Ariane from ETH Zurich PULP team
  - Drive CV64A feature set discussion
  - Drive CV32A feature set discussion
- Asking for contributors to
  - Develop and maintain selected donated core IPs

Next meetings

- Preferences for frequency, date & time?
  - E.g. 16:00 CEST -> 7am in California, 10am in Ottawa, 10pm in China?
- Partner presentations (please ask us for a slot) ~15 minutes
  - Introduction of partner
  - How can you benefit from OpenHW?
    - Key interest?
  - How can you contribute to OpenHW?
    - On which Core can you commit resources (what are your plans)?
      - On Design?
      - On Verification?
      - On Software?
      - On Hardware?
- Open to suggestion for meeting topics