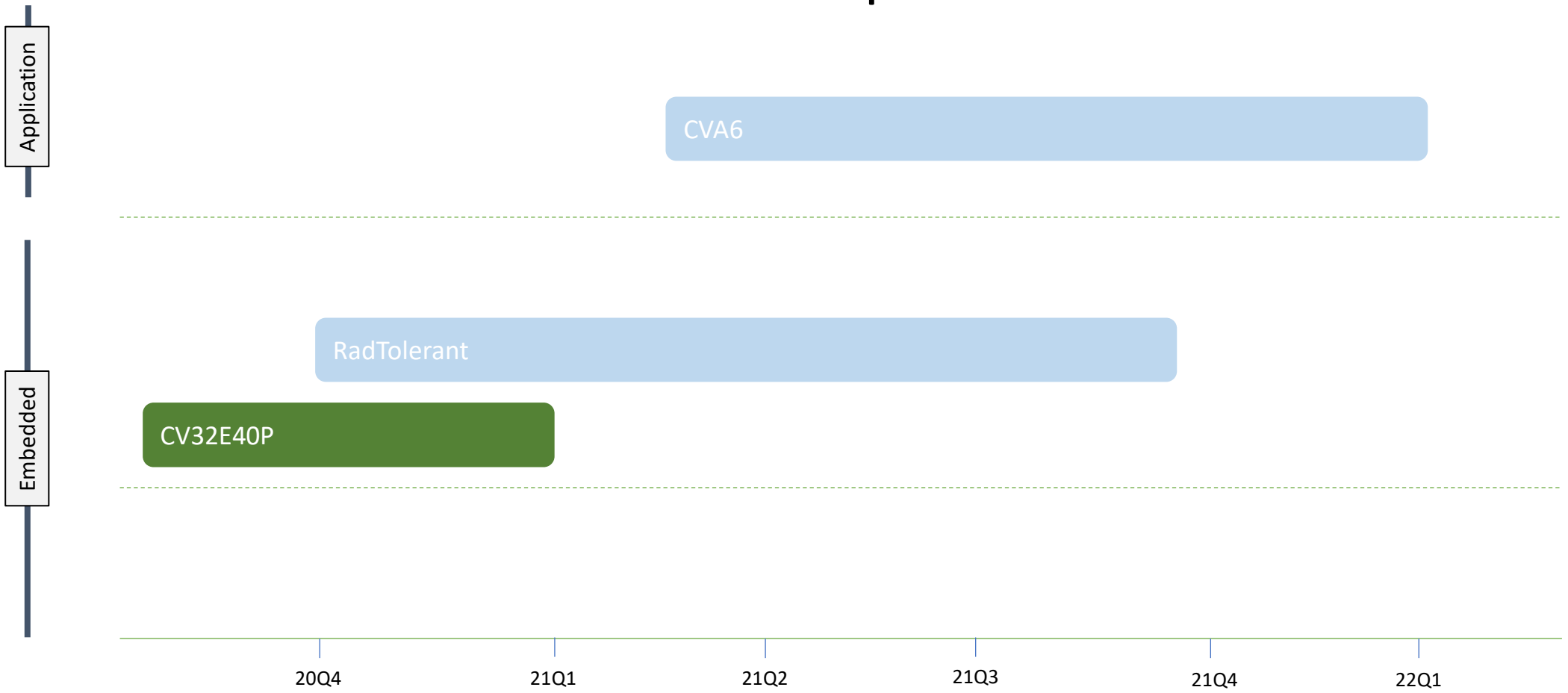
CORE-V-MCU Roadmap

CORE-V-MCU Family History

- The starting point is the Arnold design, one of the multiple open-source designs from the ETH Zurich PULP Platform

- The OpenHW HW Task Group has the mandate to define, develop and support SoC and FPGA based evaluation / development platforms for the cores and IP developed within the OpenHW Group
  - Chair: Hugh Pollitt-Smith, *CMC Microsystems*
  - Vice-chair: Tim Saxe, *QuickLogic Corporation*

CORE-V-MCU Roadmap

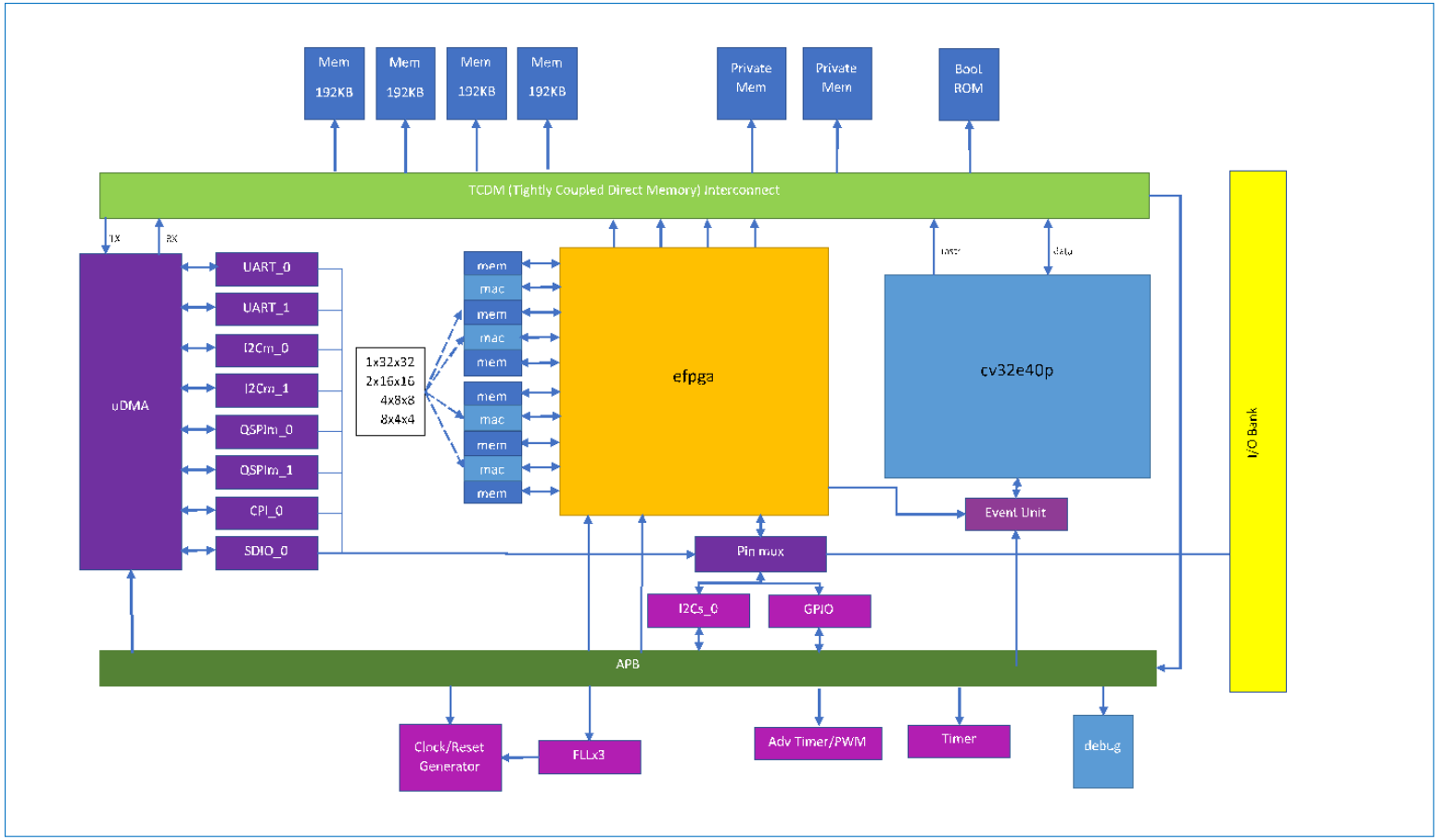


First CORE-V-MCU based on CV32E40P

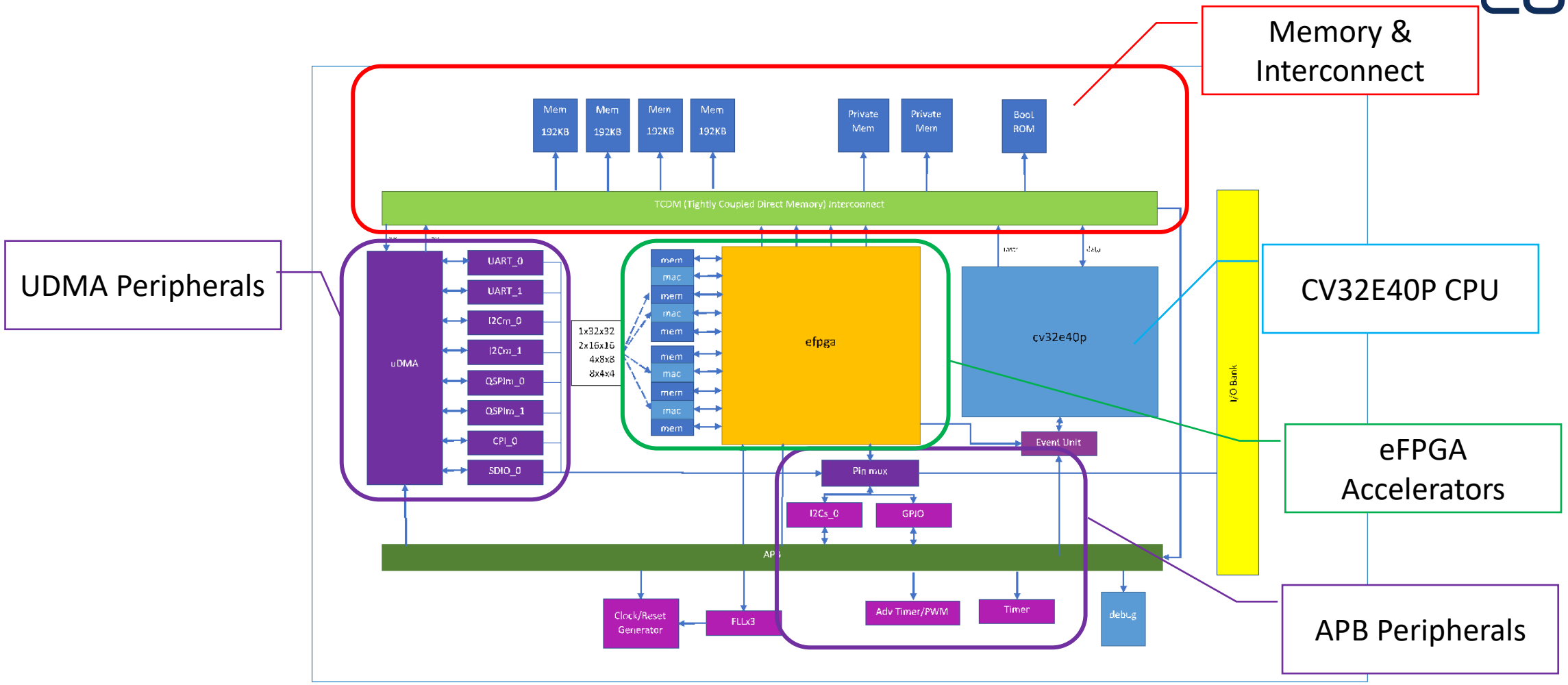
Core	Bits/Stages	Description
CV32E40P (RI5CY)	32bit / 4-stage	A family of 4-stage cores that implement, RV32IMFCXpulp, optional 32-bit FPU, instruction set extensions for DSP operations including HW loops, SIMD extensions, bit manipulation and post-increment instructions.
CVA6 (Ariane)	32 & 64bit / 6-stage	A family of 6-stage, single issue, in-order CPU cores implementing RV64GC extensions with three privilege levels M, S, U to fully support a Unix-like (Linux, BSD, etc.) operating system. The cores have configurable size, separate TLBs, a hardware PTW and branch-prediction (branch target buffer, branch history table and a return address stack).

- Basic elements:
  - CV32E40P – RISC-V Core
  - Interconnect & Memory
  - Peripherals
  - eFPGA based accelerators

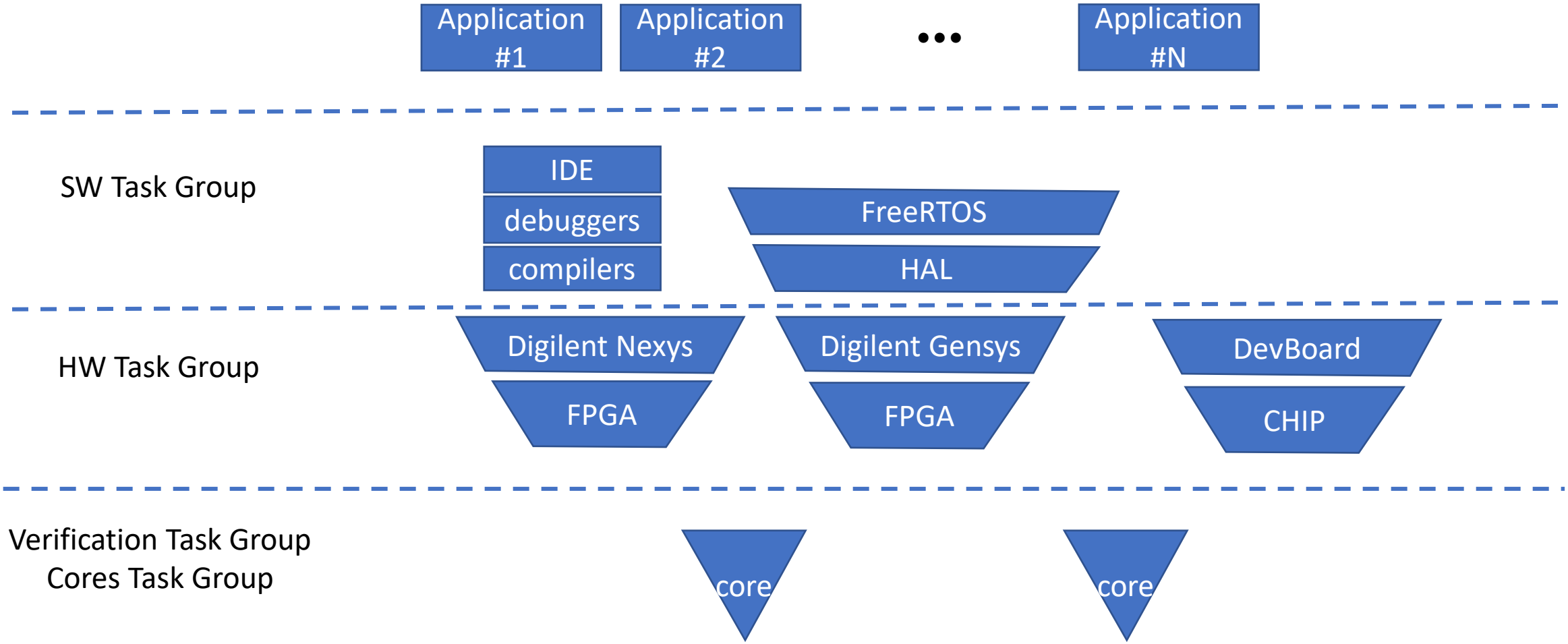
Block Diagram



Block Diagram



Outputs


Application #1
Application #2
...
Application #N
SW Task Group
IDE
debuggers
compilers
FreeRTOS
HAL
HW Task Group
Digilent Nexys
FPGA
Digilent Gensys
FPGA
DevBoard
CHIP
Verification Task Group
Cores Task Group
core
core

CORE-V-MCU Considerations

- OpenHW Cores and Verification Task Groups team up to deliver cores that are fully ready for industrial adoption
- CORE-V-MCU is intended to enable application developers to evaluate the performance of a core, not to be fully ready for industrial adoption
  - The major paths in CORE-V-MCU design will be tested with real-world applications running in FPGA emulations and in simulation
  - While the OpenHW Group cores are fully verified, the other open-source IP typically does not have a full test bench or verification suite and it is not the goal of this project to fill that gap

CORE-V-MCU Scalability

- The CORE-V-MCU is designed to be scalable:
  - Swapping between RI5CY and CV32 is parameterized, so it is anticipated that supporting other CV32 family members will be straightforward
  - Replacing the CV32 with the CVA6 core is under consideration
  - The FPGA build system is quite flexible making it easy to:
    - Support different FPGA boards
    - Support different FPGA pinouts
    - Support different memory sizes
    - Support different numbers of peripherals
    - Support emulation-based software regression tests