SFU RISC-V Processor Development and Formal Methods

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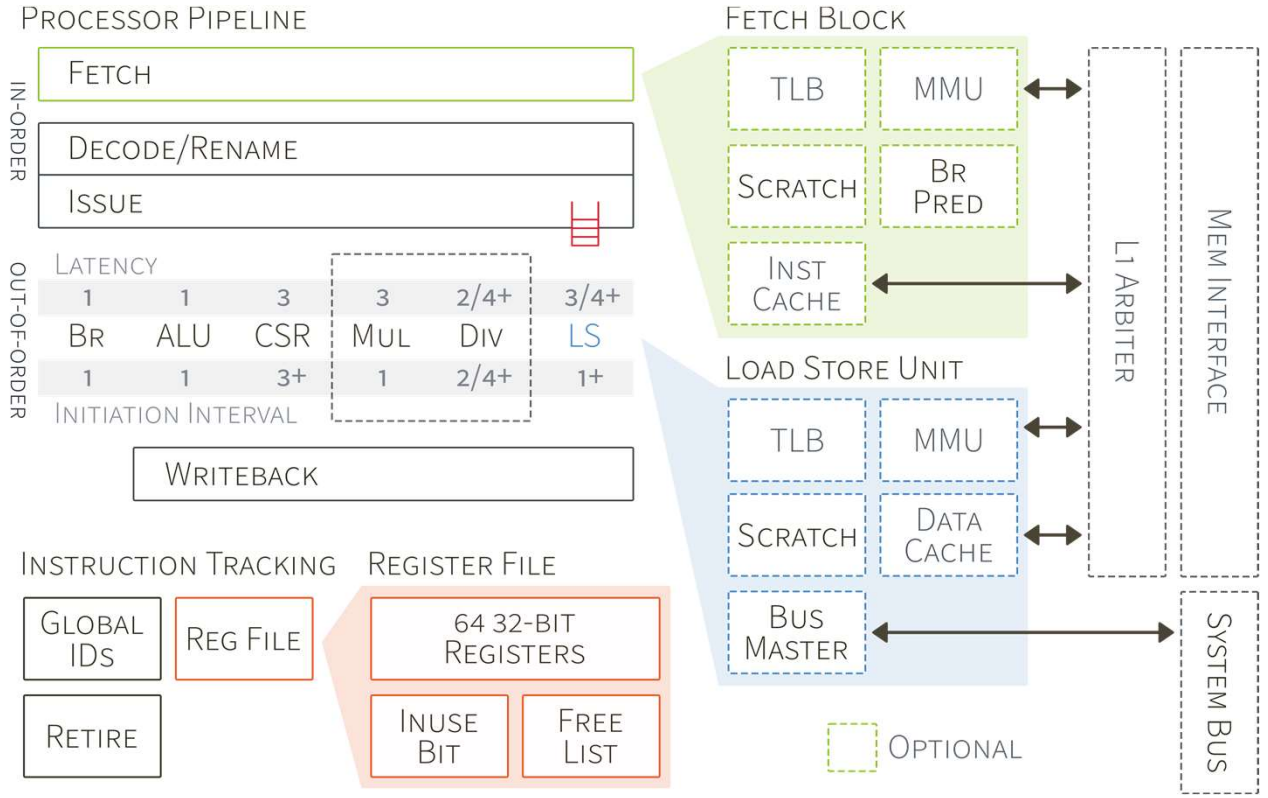
Taiga CPU: RV32IMA

gitlab.com/sfu-rcl/Taiga

- FPGA-Optimized
- Highly Configurable
- High Performance
  - Single-Issue
  - Out-Of-Order Execution
  - Parallel execution units
- 1st class Custom Instruction Support



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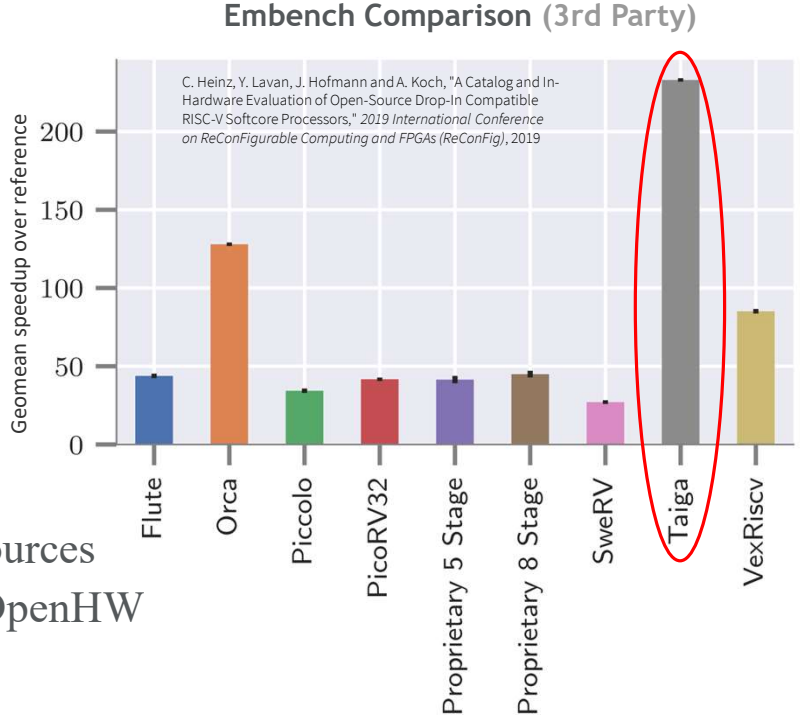
Taiga: Status and Future Work

- Passes RV32IM compliance tests
- Privileged ISA (1.11) testing underway
- Complete debug specification support and additional RISC-V extensions

- OpenHW Adoption of Taiga
  - ASIC-optimized cores often do not map well to FPGA resources
  - Provides a performance leading FPGA-optimized core to OpenHW (2.5x Fmax compared to CV32E40P on a Xilinx FPGA)
  - Expands OpenHW's competitiveness to FPGAs
  - Increases project exposure and potential for increased verification and collaboration



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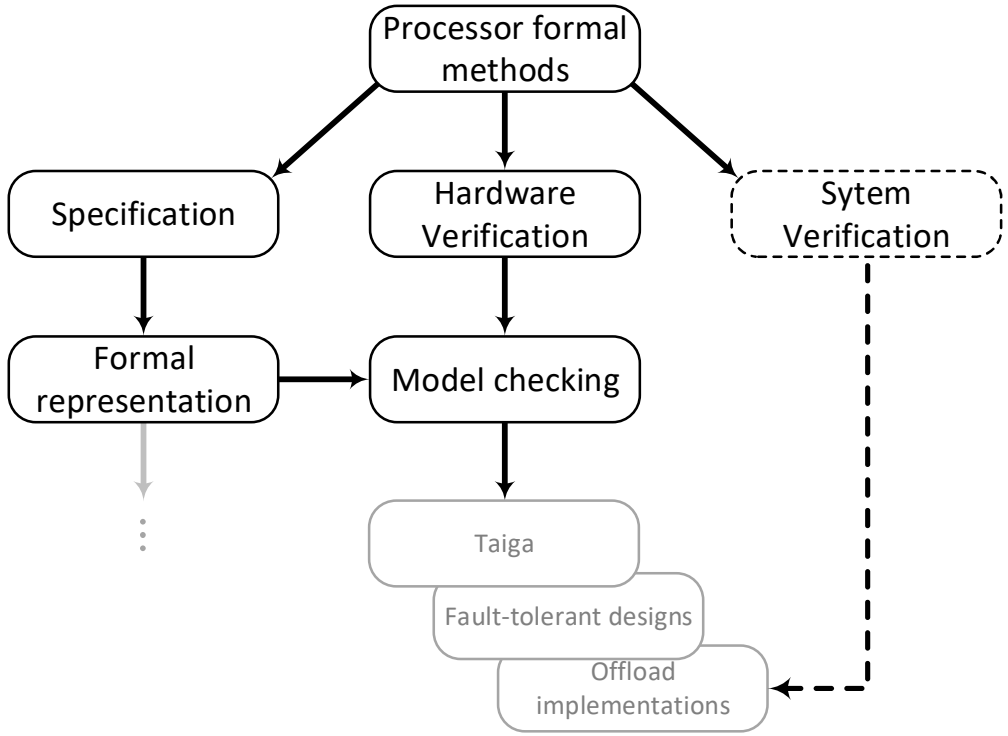
SFU Formal Methods Overview

- **Formal methods in processor system design**
- **Specification**
  - How to formally specify processor architecture
  - How to describe specific implementations
  - How to make ISA specifications widely useable
- **Hardware verification**
  - How to formally verify RTL implementations
- **System verification**
  - How to verify software-hardware systems
  - Allows us to consider and prove partition and boundaries



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SFU Formal: Status and future work

- RISC-V RV32/64I specification and representation completed
- Formal verification (model checking) of Taiga CPU ongoing
- Adding extensions, coverage generation, robustness, use-cases
  - Investigating language choices, and debug and RISC-V interrupt controller formalization

- Benefits to OpenHW and SFU RCL
  - Will accelerate improvements in quality of specification and formal representation
  - Supports a broad set of use cases with a common IR
  - Provides consistency across OpenHW use cases
  - Provides a wider set of targets implementations and feedback to prove the methodology
  - Provides leading edge formal techniques and expertise to OpenHW
  - Accelerates OpenHW developments

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