



40x/40s(/a6) – XIF and status

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Agenda

- Misc (minor items)
- XIF

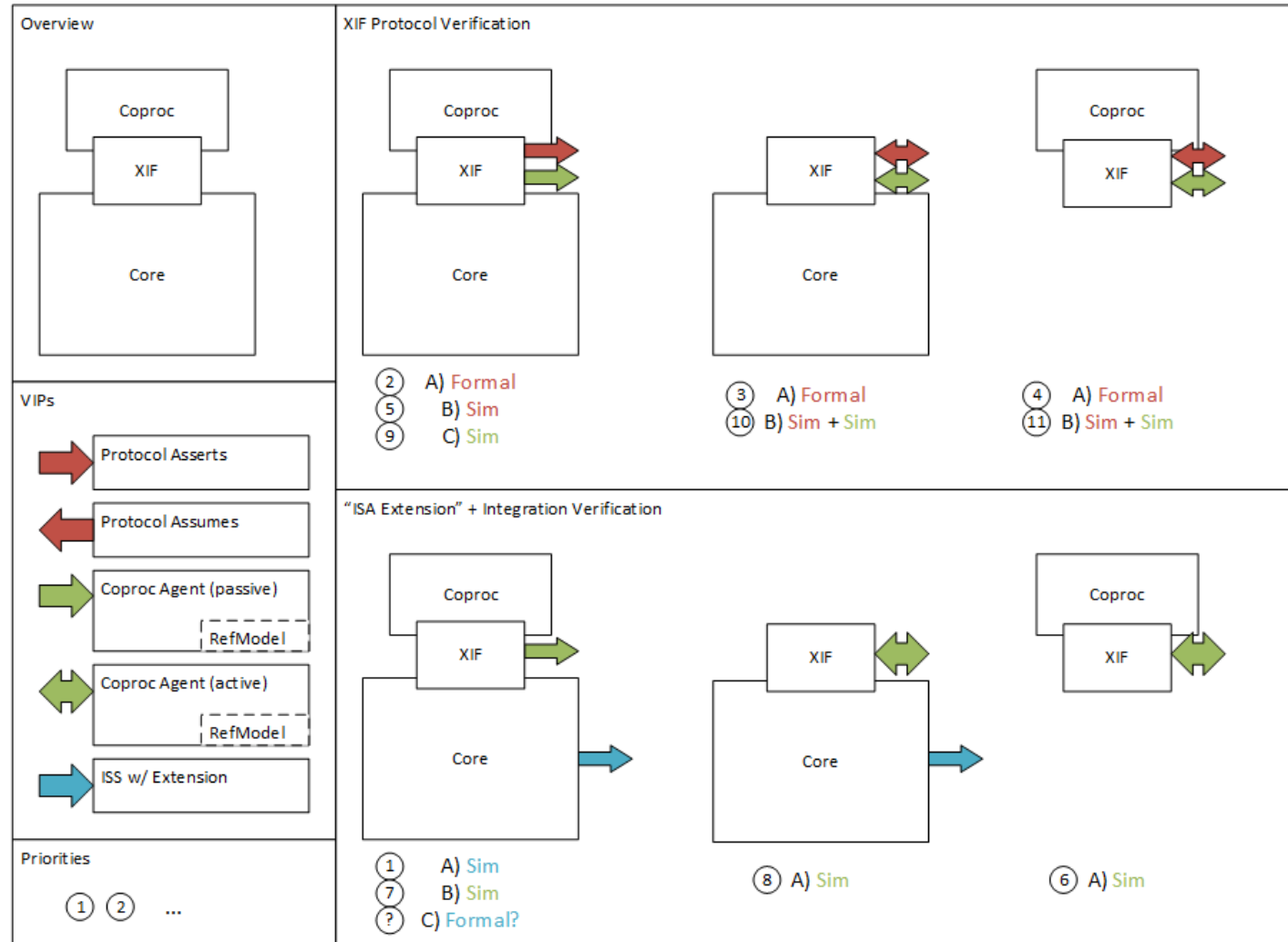
Misc (1/2)

- Idea: “core-v-rvfi”
 - 40x/40s made several amendments
 - “riscv_formal” isn’t responsive to updates
 - Rvfi amended spec is tied to 40x/40s spec
 - Resource allocation, push access, veto, ...

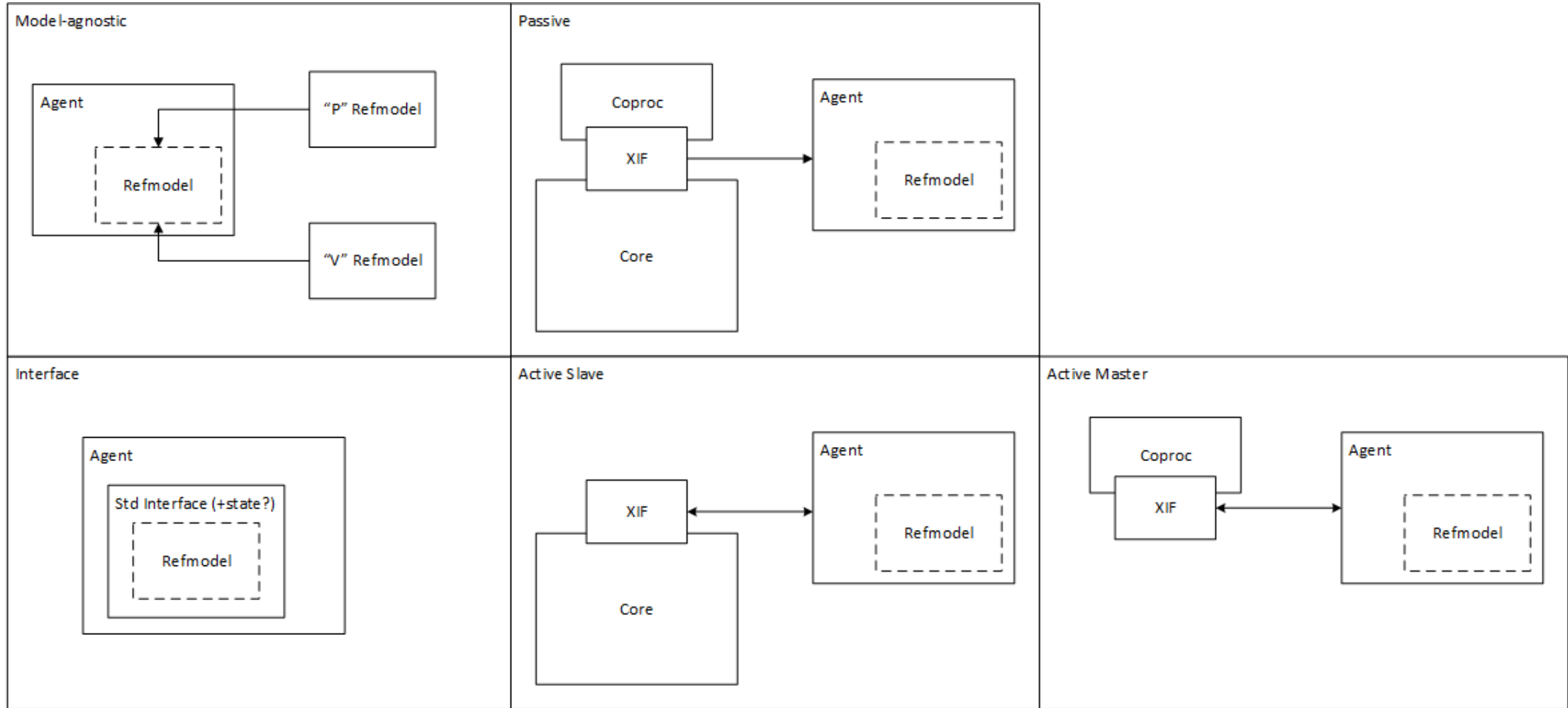
Misc (2/2)

- Idea: “core-v-rvfi”
 - 40x/40s made several amendments
 - “riscv_formal” isn’t responsive to updates
 - Rvfi amended spec is tied to 40x/40s spec
 - Resource allocation, push access, veto, ...
- Problem: vPlans not diffable?
 - Reviewing changes is hard
 - Working in parallel is hard
 - (Ref. XIF vPlans)

Plan & Priorities

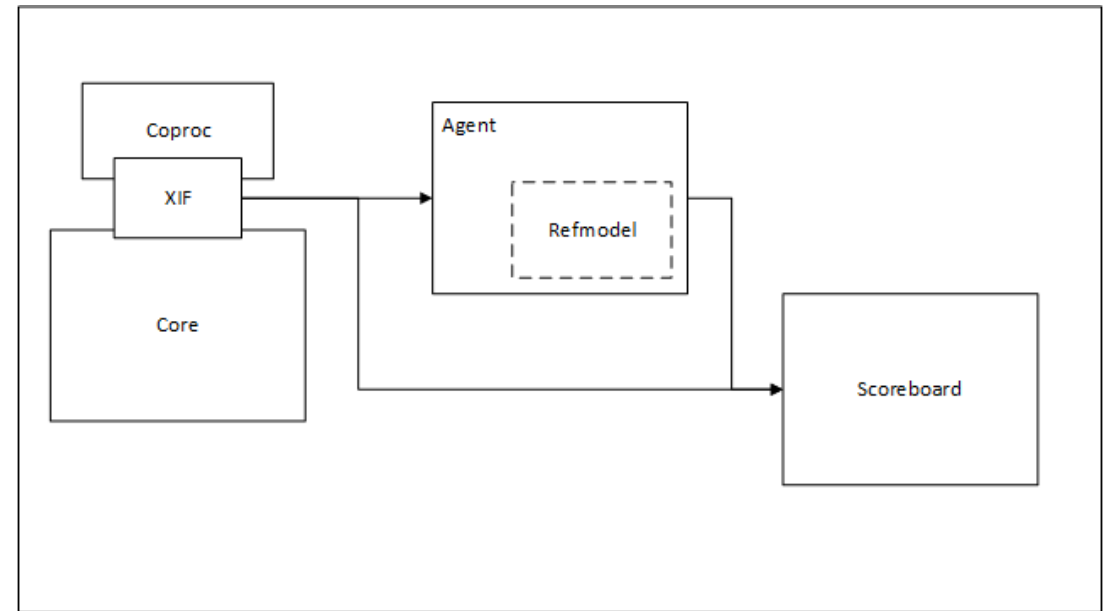


Agent + Refmodel (1/2)



Agent + Refmodel (2/2)

- Scoreboard
 - Passive agent
 - Compare RTL/Refmodel
 - XIF result object
 - Active agent
 - Use ISS scoreboard?



vPlan

- Nice vPlan!
 - Organized and clean
- Protocol vs Integration
 - Protocol
 - *“The instr and mode signals remain stable”*
 - Integration
 - *“rs signal correspond to rs1,rs2(rs3) value in CPU register file”*
 - Parameterizable?
 - *“mode take a value that the CPU supports [00, 01, 10, 11]”*
- Interfaces
 - Compressed + Memreq + Memres

Formal

- Protocol vs Integration
 - (As in vPlan)
- Assume-Assert

```
`define ... generate
  if (...) begin
    assume property(``prop``);
  end else begin
    assert property(``prop``);
  end
endgenerate
```

Delegate Responsibilities

- vPlans
 - Silabs: Compressed + Memreq + Memres
 - Silabs: Review rest of vplan
 - Thales: “Protocol vs Integration” separation/indicator?
- Assertions
 - Silabs: Compressed + Memreq + Memres
 - Thales: “Protocol vs Integration” split in >1 file?
 - Thales: Assume-Assert macro
- Agent
 - Model-agnostic?
 - Passive, Active (Master/Slave)?
- Refmodel
 - Hand-written? Imperas? Loan source code from Spike?
- Tests
 - Riscv-dv streams
 - Stand-alone tests?
- Infrastructure
 - Stand-alone tb?
 - ExternalRepos coprocessors?
 - External tests?

Other Discussions?

- ...

