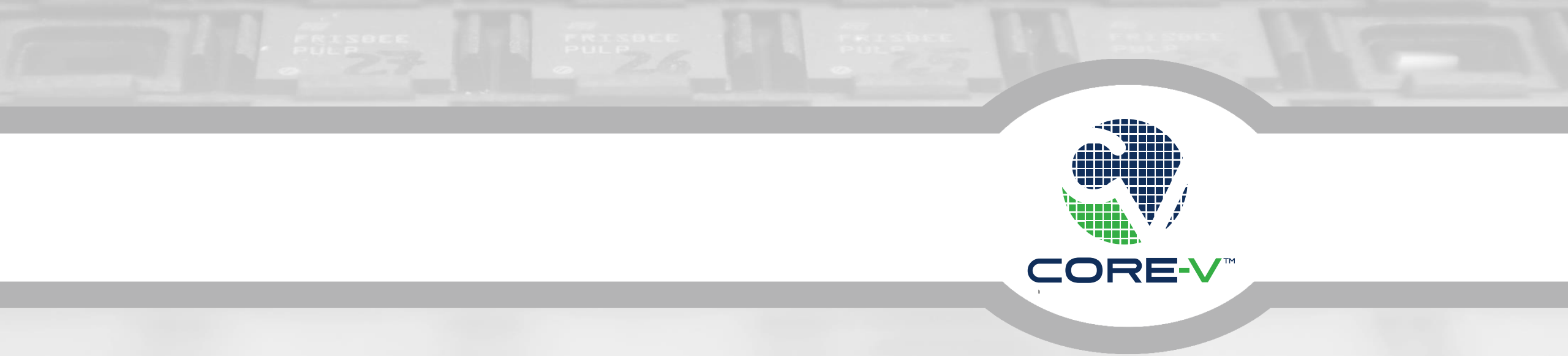


CORES TG – October 2 2023

Arjan Bink

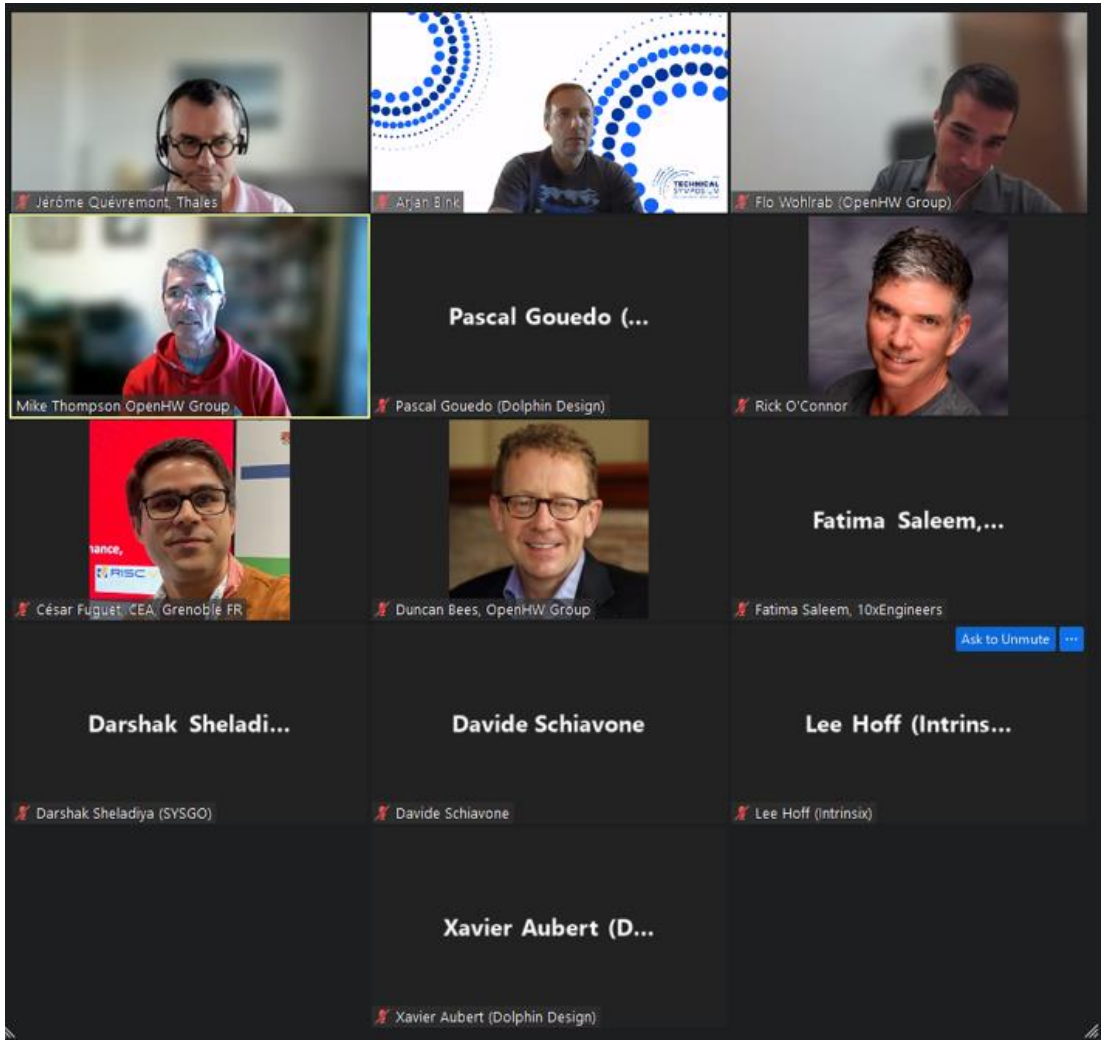
Jérôme Quevremont

Davide Schiavone

Agenda

- OpenHW process to sign-off for TRL-5
- CV32E40P v2 status
- CVA6 embedded configuration part number
- Core overview

Participants



CV32E40Pv2 status

Pascal Gouédo

Yoann Pruvost

Xavier Aubert

Project

- Project
  - Design & Verification meeting
    - Wednesday 14:00 CET every 2 weeks(Ical)
  - Dedicated technical meetings when needed
  - Reporting to Cores TG

- Mattermost channels
  - TWG : Cores : CV32E4*P
  - TWG : Verification

- Resources
  - Pascal Gouédo
    - Specification, Design, Verification & Formal
  - Yoann Pruvost
    - Design, Verification & Formal
  - Xavier Aubert
    - Verification leader
  - Vaibhav Jain
    - Verification
  - Bao Shan Mak
    - Verification

- OpenHW staff
  - Mike Thompson
    - Verification support
  - Davide Schiavone
    - Architecture & Design support

User Manual

- v1.4.1
  - Added some additional information on HW loop constraints
  - Verification section elaborated (a little bit)

Design

- All 18 bugs found by Formal Verification corrected and pushed to CV32E40P repo

- 5 new issues found by simulation
  #869 data forward violation, cv.bsetr followed by fp instructions
  #870 data forward violation, cv.insertr followed by fp instructions
  #876 data forward violation, cv.bclrr followed by fp instructions
  #877 data forward violation, cv.extractr / cv.extractur followed by fp instructions
  #880 when hwloop count programmed to 0, lpcount decrements at the end of loop to 0xFFFF_FFFF
  ⇨ Corrections to be pushed in coming days

Verification

- core-v-verif environment
  - Non-regression flow consolidation still needed to merge 20+ non-regressions on 9 configurations
- Architectural tests using RISCOF framework
  - riscv-arch-test from commit c21a2e8 (Aug 19 2020)
  - Integrated in core-v-verif (for cv32e40p only)

    Successfully generated RV32IMCF_Zicsr_Zifencei html reports with latest RTL

    236 Passed, 0 Failed
- Non-regression results
  - 3 non-regression ran on 7 configurations
    - Total of 20 non-regressions
  - 14253 tests run
  - 62 % passing tests (8816)

Tools

- SW toolchain deliveries:
  - 5 releases since April
  - Remaining
    - Automatic generation of HW loop instructions by GCC compiler

- Imperas
  - 6 Reference Model releases since April
  - 2 PULP riscvISACOV coverage files releases since April

TRL-5 RTL release

- Still expected to e/o Q4 2023

THALES

Building a future we can all trust

CVA6 embedded configuration part number

Embedded configuration

KICKOFF MEETING CV32A6 TRUST BUT VERIFY

New “embedded” CVA6 configuration for Thales needs

Scope:

- **Power:** 32bits, smaller I and D caches, no FPU, only Machine mode, no perf counters, exception gate count reduction, AXI simplification, (Dual issue?)
- **Security:** PMP (out of MMU), no debug mode, CVXIF
- **Performance:** (Data scratch pad?), bare metal, (ZBitmanip and Zicond extensions?)
- **Code size:** C, Zc extensions
- **Dual issue** to be decided.

New features are RTL options

Part number

Ongoing verification of CV32A60X

- With MMU and M/S/U privilege, Linux compatible
- X stands for CV-X-IF
- Part number already decided

Need a part number for the embedded configuration

Possible part numbers

Considered part #	Pros	Cons
CV32A60E		E/"Embedded" interferes with CVE2, CVE4
CV32A60B	B for baremetal implicitely assumes that there are also non-baremetal configurations	
CV32E60 CV32E60D (if dual issue is confirmed)	Clear it's not an application core	Unclear lineage with CVA6 family Interferences with CVE2, CVE4 families?
CV32Æ60 CV32Æ60D	Clearly shows the duality	Non-ASCII Key sequence (e.g. Alt+146)

Core overview

Core	TRL	Privilege	ISA	Debug	Interrupts	Bus	Gate count (min, typ, max)	CoreMark / MHz (min, typ, max)	Target date
CV32E20	5	M, U (v1.11)	RV32I, RV32E, C, M, Zicsr	0.13.2	CLINT	OBI	14K, 19K, -	-, 2,47, -	2024 Q1 (per October 2023)
CV32E40P	5	M (v1.11)	RV32I, C, F, M, Xpulp, Zicsr, Zfinx, Zifencei	0.13.2	CLINT	OBI	-, -, -	-, 2.91, -	2023 Q4 (per October 2023)
CV32E40S	5	M, U (v1.12)	RV32I, RV32E, C, M, Xsecure, Zba, Zbb, Zbc, Zbkc, Zbs, Zca, Zcb, Zcmp, Zcmt, Zicsr, Zifencei, Zkt, Zmmul	1.00	CLINT, CLIC	OBI	-, -, -	-, 2.91, 3.12	2023 Q4 (per August 2023)
CV32E40X	5	M (v1.12)	RV32I, RV32E, A, C, M, Xif, Zba, Zbb, Zbc, Zbkc, Zbs, Zca, Zcb, Zcmp, Zcmt, Zicntr, Zihpm, Zicsr, Zifencei, Zkt, Zmmul	1.00	CLINT, CLIC	OBI	-, -, -	-, 2.91, 3.12	2023 Q4 (per August 2023)
CV32E41P	3	M (v1.11)	RV32I, C, F, M, Zca, Zcb, Zcmb, Zcmp, Zcmt, Zfinx	0.13.2	CLINT	OBI	-, -, -	-, 2.91, -	Not in active development
CVA5	3	M, S, U	RV32I, A, M				-, -, -	-, -, -	Not applicable
CVA6	5	M, S, U (v1.10)		0.13.2	CLINT	AXI4	-, -, -	-, 2.93, -	2024 Q4 (CV32E6?X) 2024 Q4 (CV32A60X)

Thank you!