CORE-V™

OPENHW™

Technology Readiness Level (TRL)
Application in OpenHW Group

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GROUP OPENHW™ PROVEN PROCESSOR IP

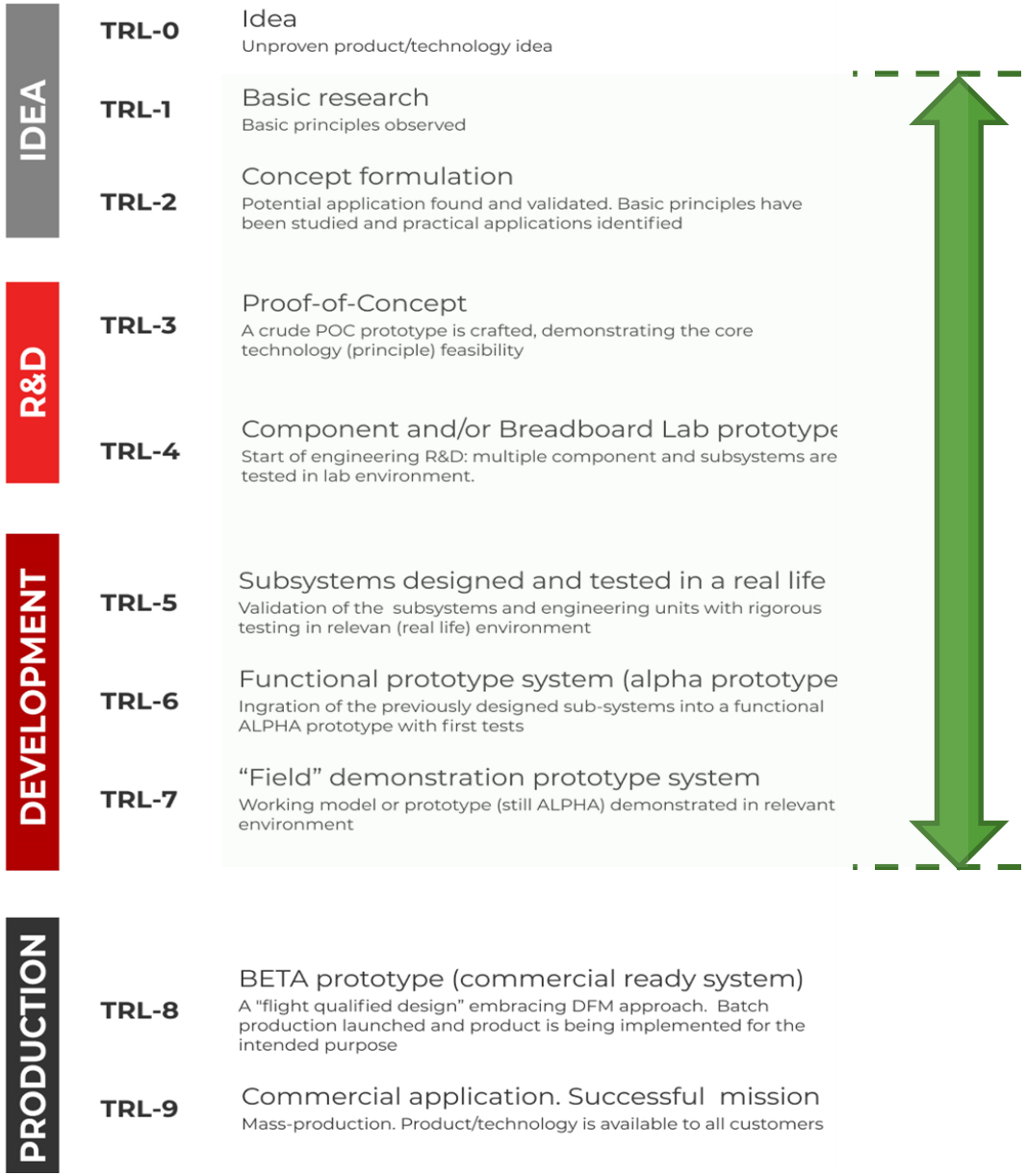
Technology Readiness Level

NASA:

"Technology Readiness Levels (TRL) are a type of measurement system used to assess the maturity level of a particular technology. Each technology project is evaluated against the parameters for each technology level and is then assigned a TRL rating based on the projects progress. There are nine technology readiness levels. TRL 1 is the lowest and TRL 9 is the highest."

https://www.nasa.gov/directorates/heo/scan/engineering/technology/technology_readiness_level

TRL Scale



OpenHW Technology Outputs

OpenHW IP Adopters

TRL Map to OpenHW Activity

TRL	OpenHW Utilization
1-Basic Principles Observed	•**OpenHW research projects** may target TRL-1 as project output, e.g. to develop novel approaches to core or accelerator architecture
2-Concept Formulation	•Core IP or accelerator development projects are typically initiated as TRL-2 concepts, identifying principles and applications of the IP •The **OpenHW Project Concept Gate** output includes a TRL-2 description of the Core IP
3- Proof of Concept	•Core IP or accelerator development projects will pass through TRL-3 **as the (RTL) design completes**. •Proof of concept is shown by core compilation and demonstration of basic operations (e.g. Linux booted, coremark results, hello-world)
4- Component Prototype	•Core IP or accelerator projects will pass through TRL-4 as they produce **preliminary PPA results** (via synthesis scripts for FPGA or ASIC) and/or **run preliminary application code**, such as an accelerator running machine learning code.
5- Subsystem Designed and Tested	•Core IP projects reach TRL-5 as they **complete full verification**. The OpenHW RTL Freeze checklist process verifies that the design is fully ready for industrial adoption.
6-Functional (Alpha) Prototype	•**OpenHW IP that is integrated into an MCU system** or other device reaches TRL-6 as prototype Silicon is **fabricated and demonstrated on a development board or other platform**.
7-Field Demonstration Prototype	•**OpenHW IP that is integrated into an MCU system** or other device reaches TRL-7 as prototype Silicon is fabricated, **deployed and demonstrated in the field**.

FAQ (1 of 3)

Why do we need TRLs?

We need TRLs to communicate on the maturity targets of our projects-in-progress (research, development, prototypes…) and the maturity achieved by completed projects. This provides developers and users of the IP a ready framework to understand the intent of projects.

Do TRLs duplicate project gates?

No, project gates determine the steps that a project progresses through from conception to completion. TRLs refer to the end-target of the project.

Why did we create a TRL map?

Standard TRL definitions may leave room for interpretation depending on the field (chemistry, electronics…). The OpenHW TRL map reduces ricks of ambiguities in the application of TRLs to our activity.

Do OpenHW TRL levels only refer to cores IP?

The current OpenHW maps focuses on CORE-V cores and other RTL IP. Conceptually, it can be applied for software projects and development boards.

FAQ (2 of 3)

How does OpenHW assess the TRL of a (sub)system formed of components at different levels?

This question arises, for example, when we take verified Core IP at TRL-5 and integrate it into MCU/System on Chip, and then further into development platforms. The Core IP may be integrated together with lower TRL components in order to achieve functional demonstrations of the Core IP.

As a result, the Core IP progresses to TRL-6 or 7 so long as the integration has enabled the required functional demonstration. That is,

- to reach TRL-6, the IP needs to be silicon-demonstrated;
- to reach TRL-7, the IP needs to be field-demonstrated.

We usually do not quantify the TRL of the actual SoC or field platform, except if those platforms themselves are technology blocks intended for volume use, such as to be used as components of a product.

To summarize, there is no fixed rule saying "TRL*n* subsystems shall include TRL*n+1* building blocks"

Example

- CV32E40P Core IP achieved TRL-5 after completion of verification and Project Freeze gate
- CV32E40P Core IP integrated in CORE-V MCU will achieve TRL-6 after demonstration in live Silicon and completion of CORE-V MCU Project Freeze gate
- CV32E40P Core IP integrated in CORE-V MCU and CORE-V Dev-Kit will achieve TRL-7 after demonstration of field operation and completion of CORE-V Dev-Kit Project Freeze gate

FAQ (3 of 3)

How should end users make use of OpenHW TRLs?

Note that there are no warranties associated with OpenHW TRL levels.

The OpenHW dashboard identifies the achieved TRL of completed projects and TRL targets of in-progress projects. Achieved TRLs are meant to convey the state of maturity of OpenHW IP. TRL Targets are not yet reached while the project is under development. TRL-5 IPs meet OpenHW's standards of industrial verification and can be considered for use in production ICs.

I have integrated OpenHW IP into my product or project. Should I inform OpenHW?

OpenHW is interested to know about your utilization of OpenHW IP and any feedback that you may have concerning the TRL levels. For example, we may be able promote the TRL levels of TRL-5 core IP based on your integration into prototypes. Please get in touch via info@openhwgroup.org.

What are the disclaimers?

TRL levels are not warranties. OpenHW makes open-source IPs available without warranties of any kind, as stated in the Apache and Solderpad licenses.