CORES TG – June 7 2021

Arjan Bink

Jérôme Quevremont

Davide Schiavone

OPENHW GROUP™
PROVEN PROCESSOR IP

Agenda

- CV32E40X status
- CVA6 status
- Zce (and maybe Zfinx) proof of concept
- University of Saskatchewan
  - Research Interests and Projects

CV32E40X status

Øystein Knauserud

CV32E40X p.1 (overlaps CV32E40S p.1)

- RVFI mostly completed, but not yet fully verified
- Started porting RVFI to new controller/pipeline
- Added fence.i flush_req/ack interface
- Added nmi_addr_i
- Added OBI memtype/prot outputs
- Structs for internal OBI control signals
- Lint cleaning
- ALU cleanup (separated ADD/SHIFT)
- User manual updates

CV32E40X p.1 (overlaps CV32E40S p.1)

- New controller being implemented
  - Exceptions, interrupts and special instructions handled in WB
  - Debug entry from WB in progress
  - Clarified pipeline valid/ready signalling
- CSR writes moved from EX to WB
- Updated default PMA attributes

CVA6 status

Jérôme Quévremont

CVA6

- Gates
  - PC (former PPL) passed
  - PL passed
  - PA (former PPA) to come: specification and detailed plan
- Next project meetings
  - Also spans on verification, SW topics…
  - June 11th: technical meeting
  - June 18th: progress meeting
  - June 25th: technical meeting
  - July 2nd and 9th: Resechuling needed (Jérôme unavailable)
  - https://calendar.google.com/calendar/u/0/embed?src=meetings@openhwgroup.org
- TWG : Cores : CVA6 Mattermost channel
  - Also spans on verification, SW topics…

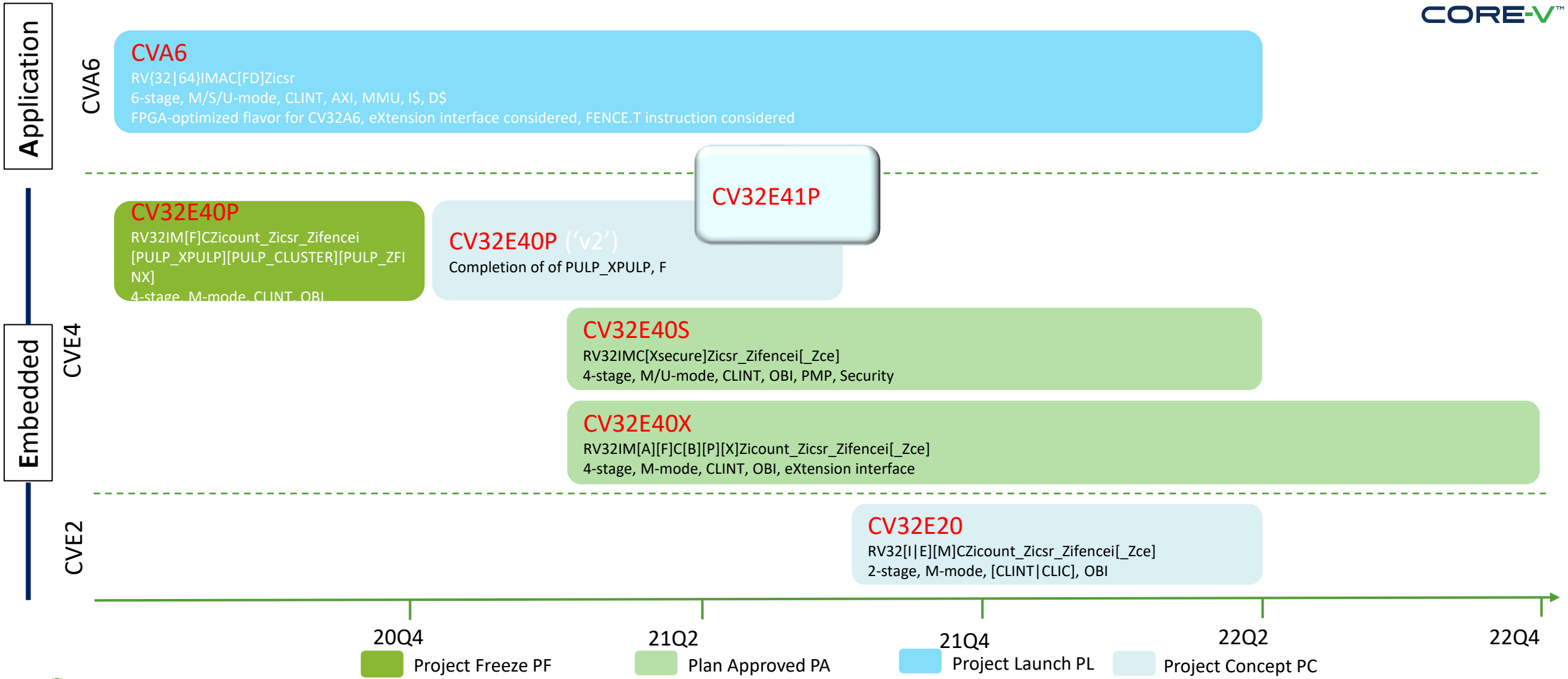
CVA6: current activity

- Specification on going
  - https://docs.google.com/document/d/11rsoO5WKraMCraSpnsVqmt4hJaCcDG0zq7LTWdXVkf0
  - Recent main events:
    - CVA6 shall be RISC-V compliant by implement all mandatory features (for its set of extensions)
    - CV32A6 will only support single-precision floating-point (RV32F)
      - CV64A6 will support double precision (RV32FD)
    - Adding a coprocessor interface and trying to align it with CV32E40X
  - The devil is in the details: need more time to complete CSR, perf counters, caches, coprocessor i/f…
    - Initial target planning
      - May 7th: complete draft (all sections contributed, not perfect)
      - May 28th: updated draft, ready for review
      - June 25th (latest): approved at CVA6 project meeting
      - June 28th: get TWG approval (part of PA gate)
- Verification: reorganizing repo to clearly delineate the core (=scope of the specification) and the APU (processor subsystem)
- SW: on-going FreeRTOS and 32b Linux ports
  - 32b Linux: flagged a few bugs (PR to come). Current status on Genesys 2: console displays log until the init processor.

Zce (and maybe Zfinx) proof of concept

Tariq Kurd

CORE-V RISC-V Cores Roadmap

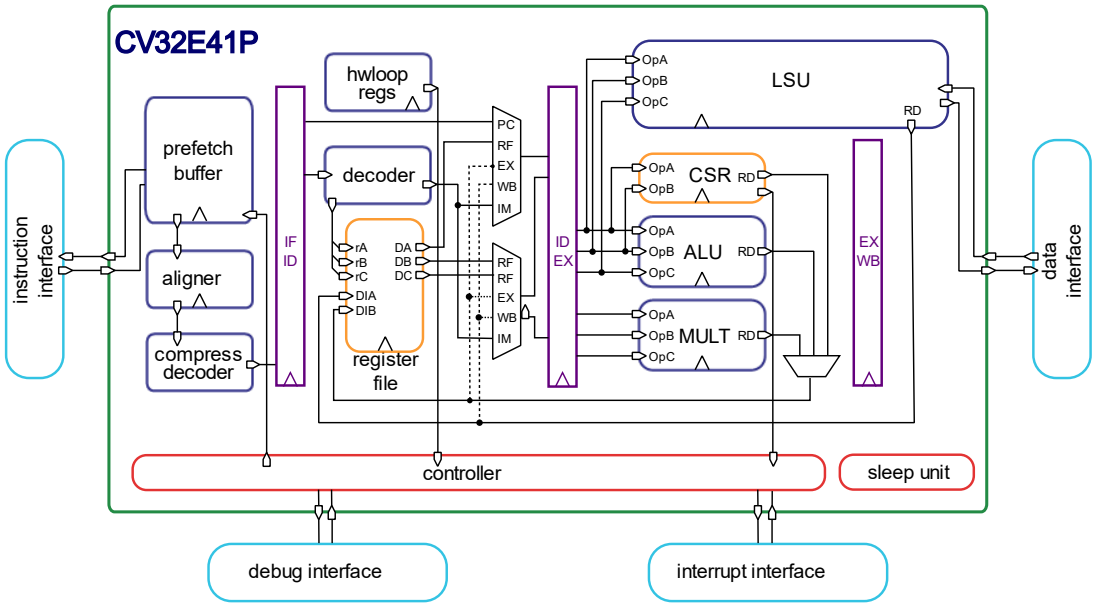


CV32E41P – TRL 3

- 4-stage, in-order, single-issue
- RV32IMCZicount_Zicsr_Zifencei **[_Zce][{F, _Zfinx}]**[PULP_XPULP][PULP_CLUSTER]
- M-mode, CLINT, OBI

- Starting from CV32E40P fork

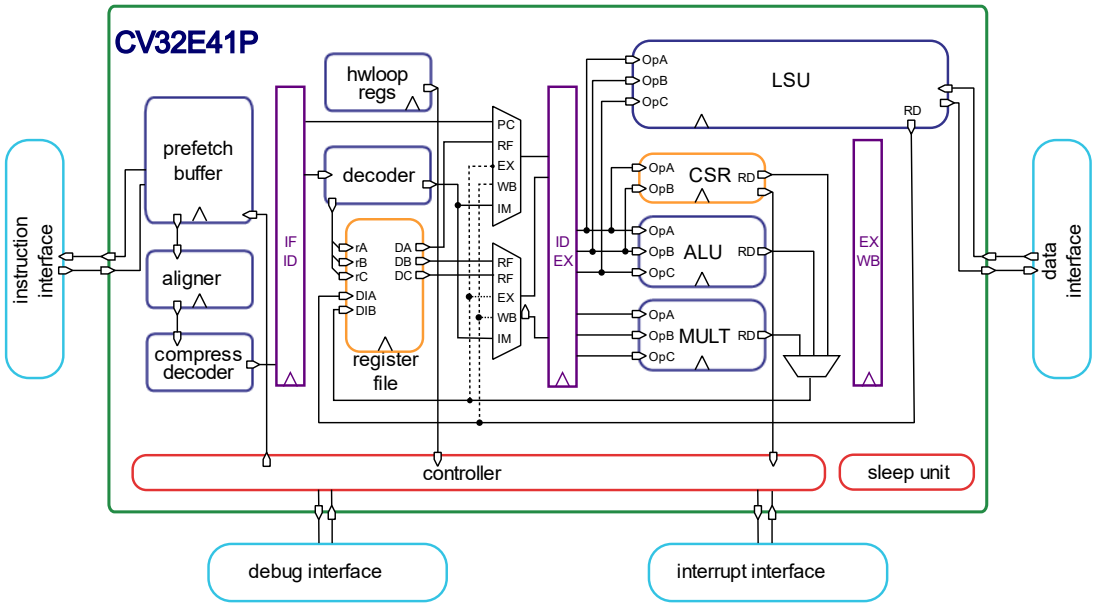
- Goals:
  - Proof of Concepts to demonstrate the PPA of Zce and Zfinx ISA extensions
    - Currently both 0.41v RISC-V draft spec
    - Zfinx: GCC, LVM, Spike, QEmu, OVPSim available
    - Zce: GCC, LVM, Spike, QEmu should be available by end of June ‘21



CV32E41P – TRL 3

- Verification strategy:
  - Designing and running Zfinx and Zce basic tests
    - Compliance
    - No ISS needed for Zce
    - OVPSim for Zfinx available
      - Check with Imperas if available for OpenHW Group to extend core-v-verif
    - Not aiming for 100% code coverage
      - No interrupts, no Debug, etc
      - Just proof of concept

- Deliverables:
  - A CORE-V CPU with Zce and Zfinx spec
  - After RISC-V spec ratified, aiming for TRL 5



University of Saskatchewan

Research Interests and Projects

Research Interests and Projects

Li Chen, Zonru Li
Department of Electrical and Computer Engineering
University of Saskatchewan
Saskatoon, SK, Canada

Expertise

Research expertise:

Radiation effects and mitigation techniques in digital and analog/mixed signal circuits

Technical Strength:

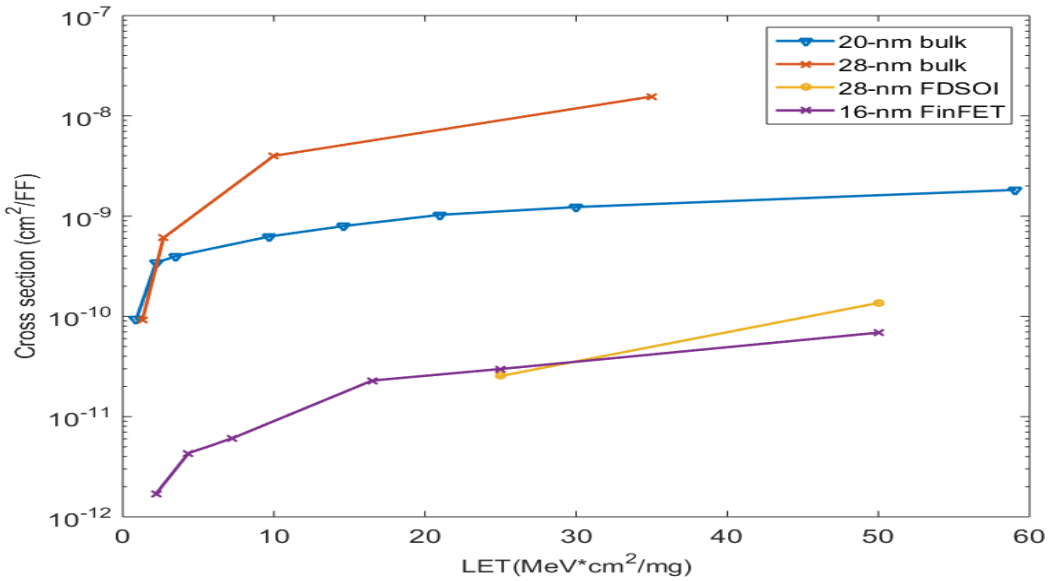
- ASIC design with advanced bulk and FDSOI technologies
- Digital circuits: FF, SRAM, microprocessor, clock tree, logic gates
- Analog circuits: VCO, PLL, bandgap circuit

Testing facilities

- Femto-second pulsed laser for SEE fault injection
- Co-60 source, Alpha source

SEE Laser Facility at University of Saskatchewan

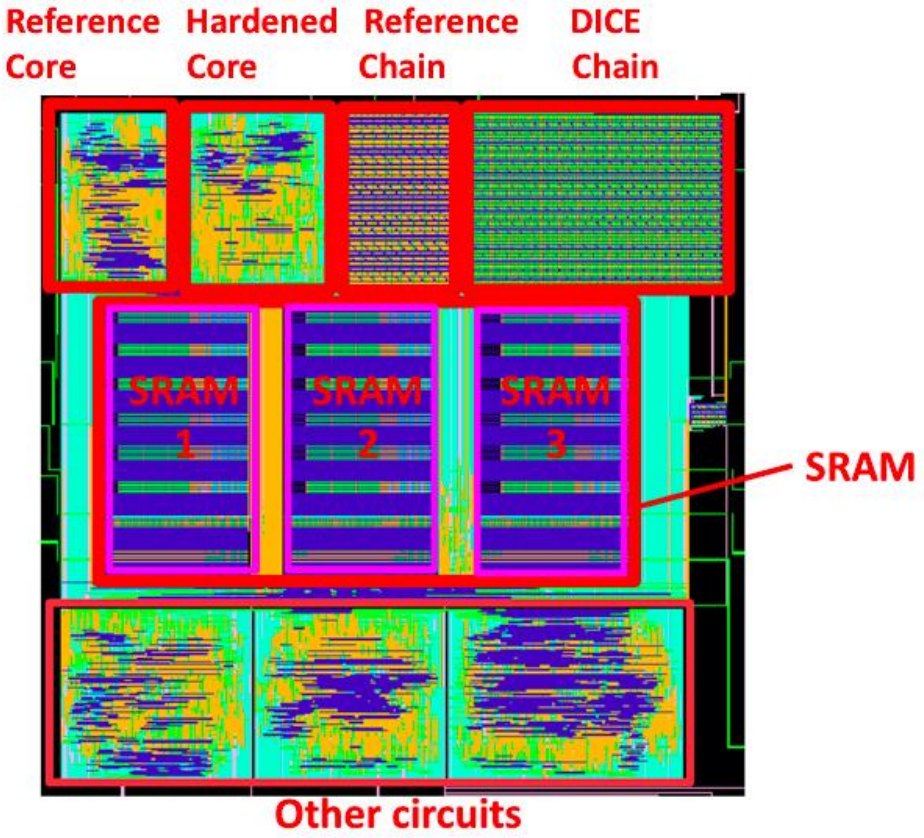
Radiation-Tolerant Flip-Flops with 22, 28, 65 nm Bulk and FDSOI

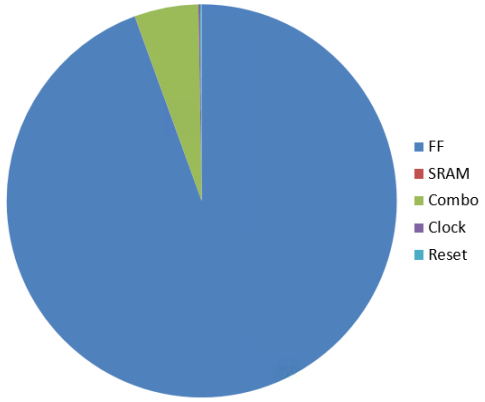


- Soft error rate in 28nm FDSOI is lower than that in 28nm bulk by 100x
- For high LET values, 28nm FDSOI is comparable to 16nm FinFET in terms of cross section

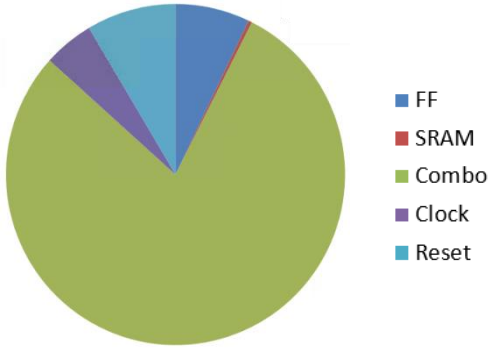
28nm FDSOI ARM Core Test Chip

5 ARM cores in one single die





Reference Core



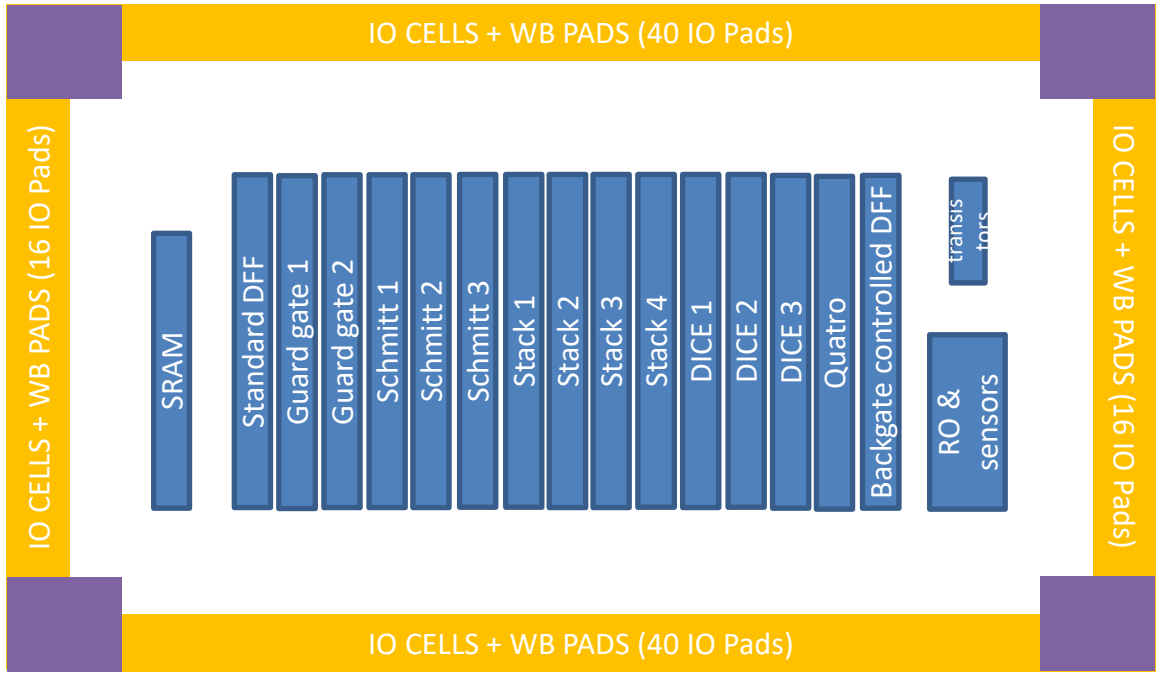
Hardened Core

Only protect the FFs and SRAM may not be sufficient for ARM processors

GF22nm FDSOI test chip

- **Study the single event and total dose effects in storage cells**

14 FF chains
256k RAM
RO/temperature sensors
Received the chips, ion testing within this year



RSIC-V project

- **Developing radiation tolerant RISC-V controller on 65nm and 22nm**
  - Based on the radiation-tolerant 65nm lib, and PLL
  - To be taped out end of 2021
  - Need support on the backend scripts

Thank you!