1. In Attendance

(see TWG meeting attendance file)

2. Voting Eligibility for March 22 2021 meeting (revised subsequent to the meeting)

- A member needs to attend 3 of 4 previous meetings to be eligible to vote. Note that the current meeting forms part of the "4 previous meetings" as stated in the bylaws. (This clarification was made after the TWG meeting)
- Because the December 2020 meeting was held close to Christmas, everyone will be counted as having attended the December meeting (this clarification made after the TWG meeting)
- So the voting eligibility for March, as revised after the TWG meeting, is determined by
 - o Attending either or both the Jan/Feb meetings, as below, AND
 - Attending the March meeting

Members Voting-Eligible for March Meeting		Feb 2021	Jan 2021
	CMC	Υ	
	Codeplay	Υ	Υ
	Embecosm	Υ	Υ
	EM Micro	Υ	Υ
	ETH Zurich	Υ	
	Futurewei	Υ	Υ
	Imperas	Υ	Υ
	NXP	Υ	Υ
	Quicklogic	Υ	Υ
	SiLabs	Υ	
	THALES	Υ	Υ

3. TG reports highlighting changes to plan of record, critical issues on projects

Group	Reporting	Link to report	Key Issues & Actions Noted
SW	Jeremy Bennet	SW TG March report	 IDE needs example projects Clang/LLVM work on assembler added from University of Tubigen Discussion raised: chairs in their capacity as chairs recommended to avoid endorsement of particular member products.
HW	Hugh Pollitt Smith		 MCU - PR progress meeting to be held on March 30 Intention to target combined PL/PA gate approval for next TWG meeting No new progress on Verilator project to report
Cores	Arjan Binks		 A big pull request for E40S and E40X came at the end of last week. After Checkin was approved for the CQ, this was merged into OpenHW Github From now on, all PR are incremental into OpenHW Github. User manual links are available CV32E40P - RVVI/RVFI work is looking very promising - this will be the technology used working forward CVA6 - passed PL gate- meeting end of this week to define scope of DUT
Verif.	Steve Richmond		 Improvements on Verification infrastructure Enhance ISA coverage model, benchmarking, Embench test bench to be used. RVVI/RVFI will help solve some of the issues encountered on CV32E40P Parallel core development with branching methodology CI flow went live this morning FORCE RISCV support for 32 bit is now merged into the OpenHW

	repo.

4. Updated gate names

New gate names were presented.

PC = Project Concept (formerly Preliminary Project Launch, PPL)

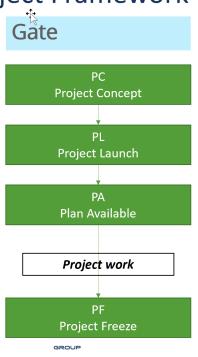
→
PL = Project Launch

PA = Plan Approved (formerly Project Plan Approved, PPA)

PF = Project Freeze (formerly Project Completed, PC)

Overall gate process was recapped (D Bees)

Project Framework



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Purpose

Green-light of project concept by TWG

Full project launch approval by TWG

Communicate project plan to TWG, (allowing member participation and

Completion of releasable project content

Criteria

Summary, proposed scope, why do this?, next steps

Outline of the requirements, features, components, supporters, risks

Project plan, methodology. Initial agile backlog if applicable. Requirements specification

RTL Freeze checklist or other checklist

Adjusting the current framework



- Simplify the gate names (done)
- Clarify the distinction between PC and PL
 - PC (formerly PPL) doesn't need to be a full project launch --> keep the focus on the concept
 - More refinement to come
- Project Launch when the scope and project is clearly defined
- Plan Approved checklist has been created
 - So far, tuned to Cores projects
 - SW version to come
 - Question to be worked through with SW TG: do we need a PA gate for software projects which are "incremental"
- Your feedback is welcomed!

5. Plan Approved Gate Milestone for Cores Projects

The PA gate checklist, prepared for Cores projects, was presented. This was based mainly on the experiences of the CV32E40P project

Spreadsheet PA checklist

6. Plan Approved proposal CV32E40S and CV32E40X

The PA gate approval request was presented by Arjan Bink for these two enhancements to the E40 family.

Materials presented

<u>E40S</u> and <u>E40P</u> Plan Approval checklist. The PA checklist has been annotated with detailed material prepared by Arjan and the E40S and E40X teams.

E40S and E40P Project Plan document

Note that the Requirements Specification is available at the following Github location



Member Vote on Approval of PA Gate

Member	Votes to Approve PA Gate for CV32E40S	Votes to Approve PA Gate for CV32E40X
СМС	Υ	Υ
Codeplay	Υ	Υ
Embecosm	Υ	Υ
EM Micro	Υ	Υ
Futurewei	Υ	Υ
Imperas	Υ	Υ
NXP	Υ	Υ
Quicklogic	Υ	Υ
SiLabs	Υ	Υ
THALES	Υ	Υ

10 votes to approve PA Gate for CV32E40S project

0 abstain

0 against

10 votes to approve PA Gate for CV32E40X project

0 abstain

0 against

The Plan Approved Gates for both projects were overwhelmingly approved. Great job Arjan Binks and SiLabs team!