SFU SOFT-PROCESSOR DEVELOPMENT

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Reconfigurable Computing Lab

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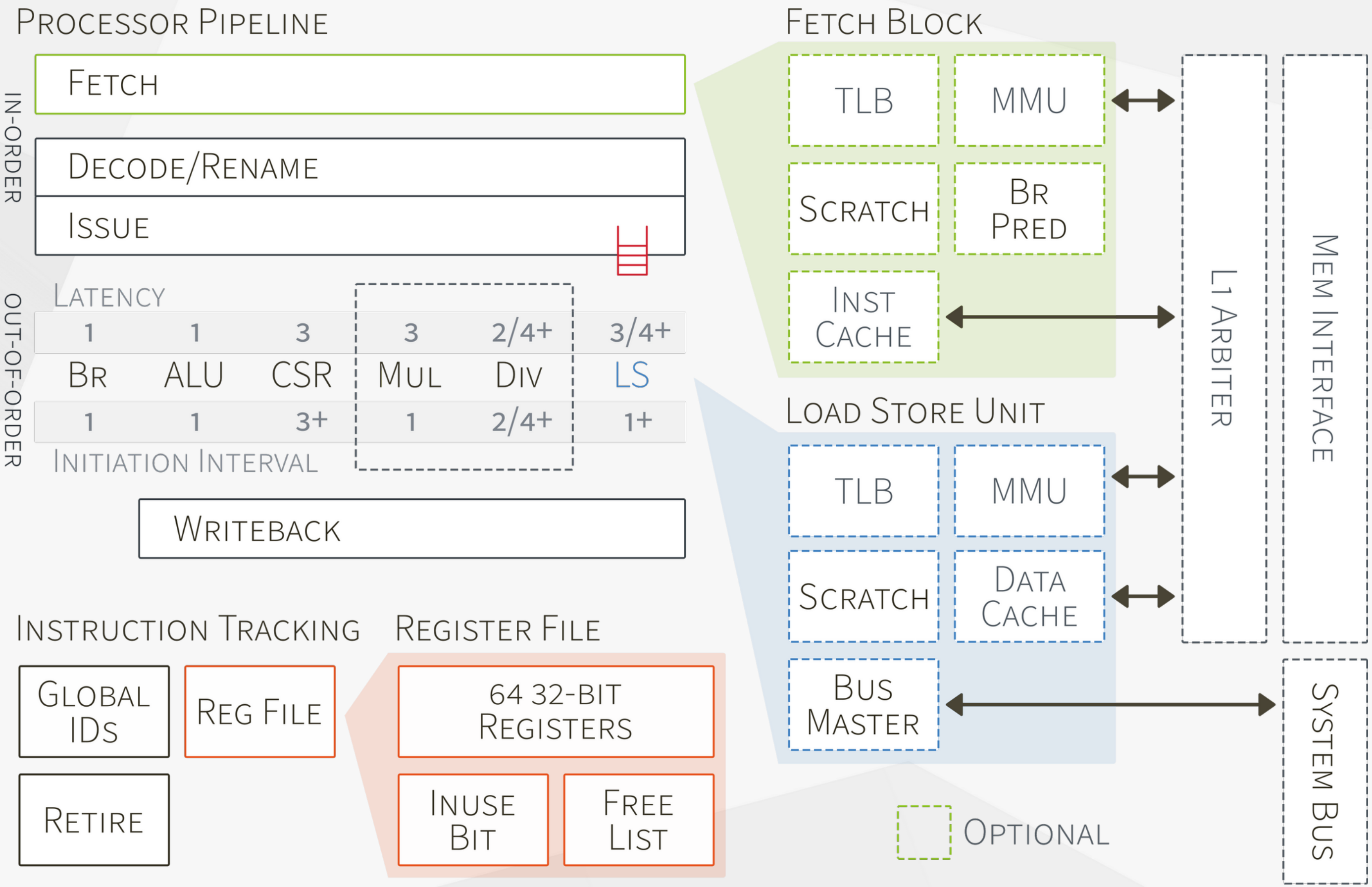
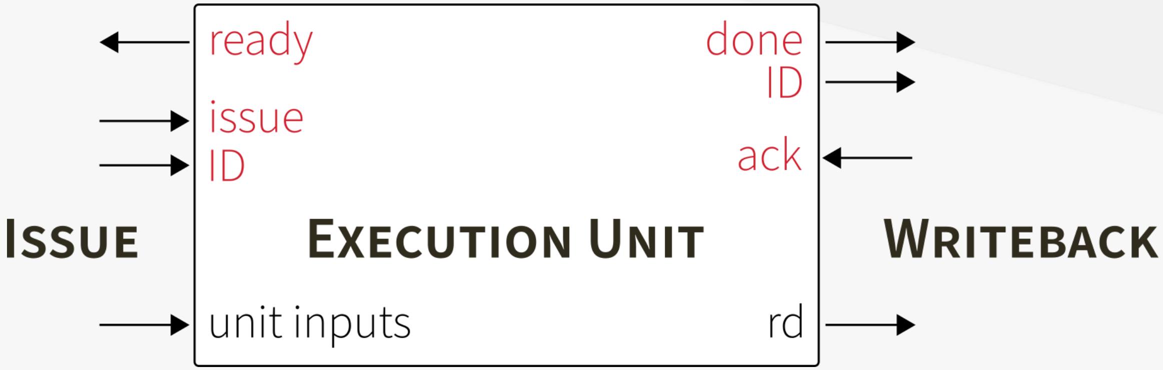
Taiga Overview RV32I[M][A]

- FPGA-Optimized
- Highly Configurable
- High Performance
  - Single-Issue
  - Parallel Execution Units
  - Variable Latency
- High Performance/LUT
- 1st Class Custom Instruction Support



Custom Instruction Support

- Fixed execution unit interface
- Variable-latency support
- Out-of-order execution support
  - inter and intra-unit
- Scalable to at least 8 custom execution units
- Taiga micro-architecture allows execution units to be fully utilized



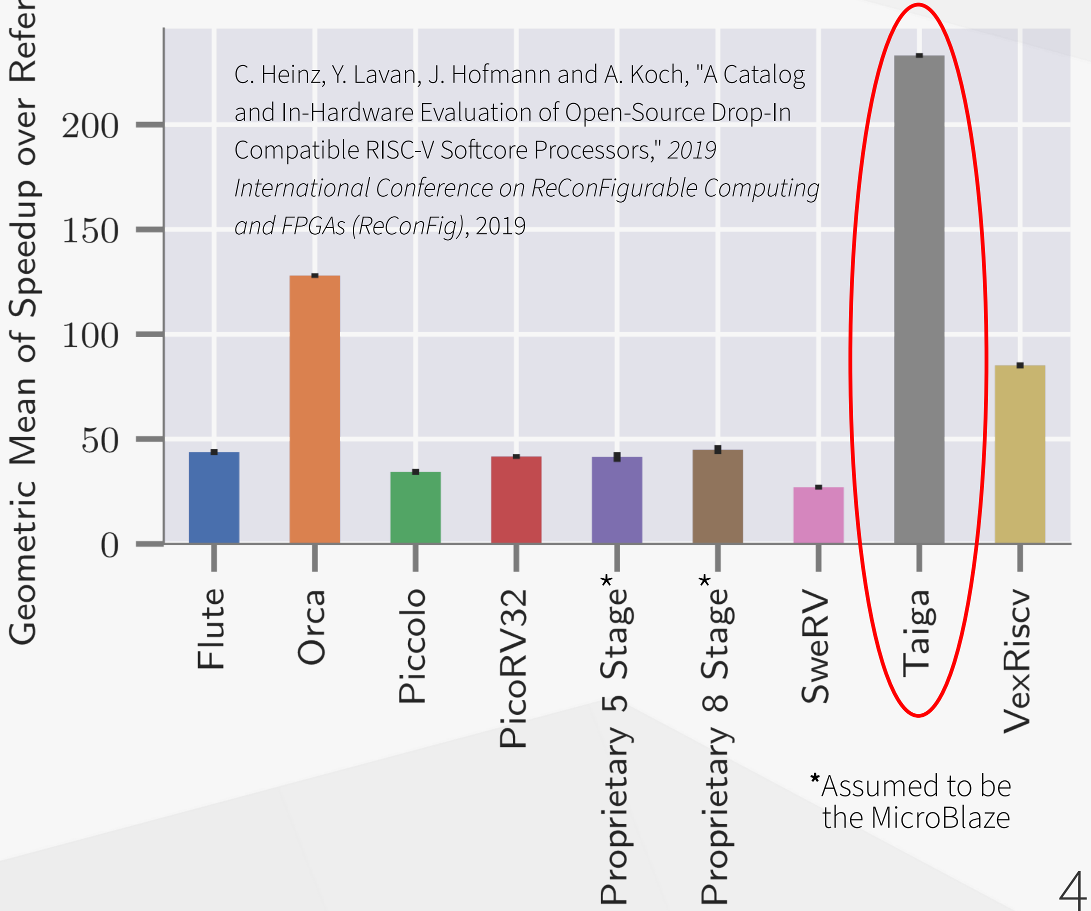
Performance

- Dhrystone: **1.63 DMIPS/MHz**
- Coremark: **2.66/MHz**
- Embench: **1.08 speed/MHz**
- Zedboard:

  1948 LUTs, 1129 FFs, 125 MHz

  2.5x Fmax of CV32E40P
- Highest performance of existing soft-processors

Embench Comparison (3rd Party)



C. Heinz, Y. Lavan, J. Hofmann and A. Koch, "A Catalog and In-Hardware Evaluation of Open-Source Drop-In Compatible RISC-V Softcore Processors," *2019 International Conference on ReConFigurable Computing and FPGAs (ReConFig)*, 2019

*Assumed to be the MicroBlaze

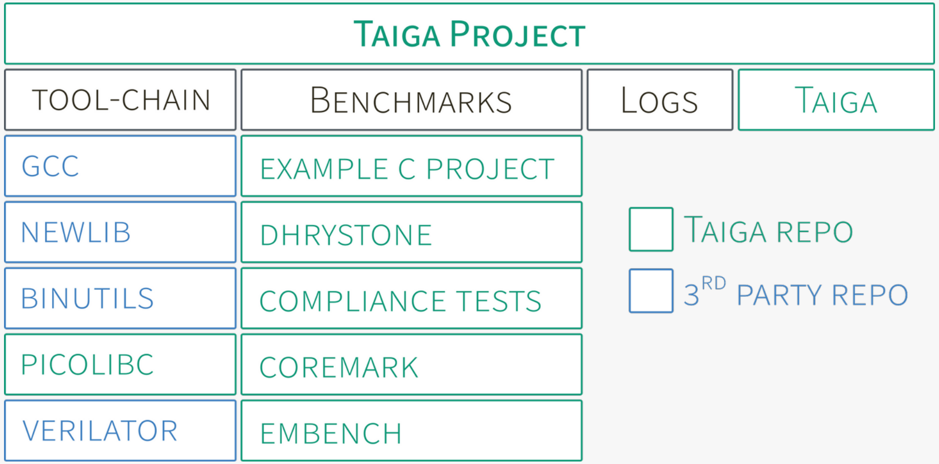
Current Status and Ongoing Work

Current Status

- Passes RV32IM compliance tests
- Makefile-based Verilator simulation
- Includes documentation and examples
- Platform support (picolibc) for Xilinx FPGAs

Ongoing Work

- Initial testing of privileged ISA (1.11)
- Optimization for Intel FPGAs
- FPU support



Taiga Project

Tool-chain	Benchmarks	Logs	Taiga
GCC	Example C Project		
Newlib	Dhrystone		
Binutils	Compliance Tests		
Picolibc	Coremark		
Verilator	Embench		

□ Taiga repo

□ 3rd party repo

Future Work And OpenHW Adoption

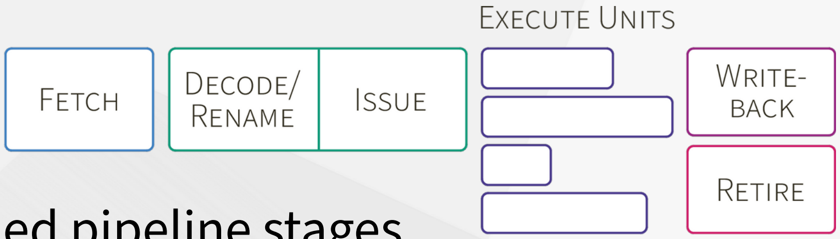
Future Work

- Complete debug integration (currently we have a working JTAG OpenOCD interface for Xilinx FPGAs)
- More detailed verification (including formal verification)
- Compressed and bit manipulation instruction support
- Multi-issue, improved branch prediction, speculative execution

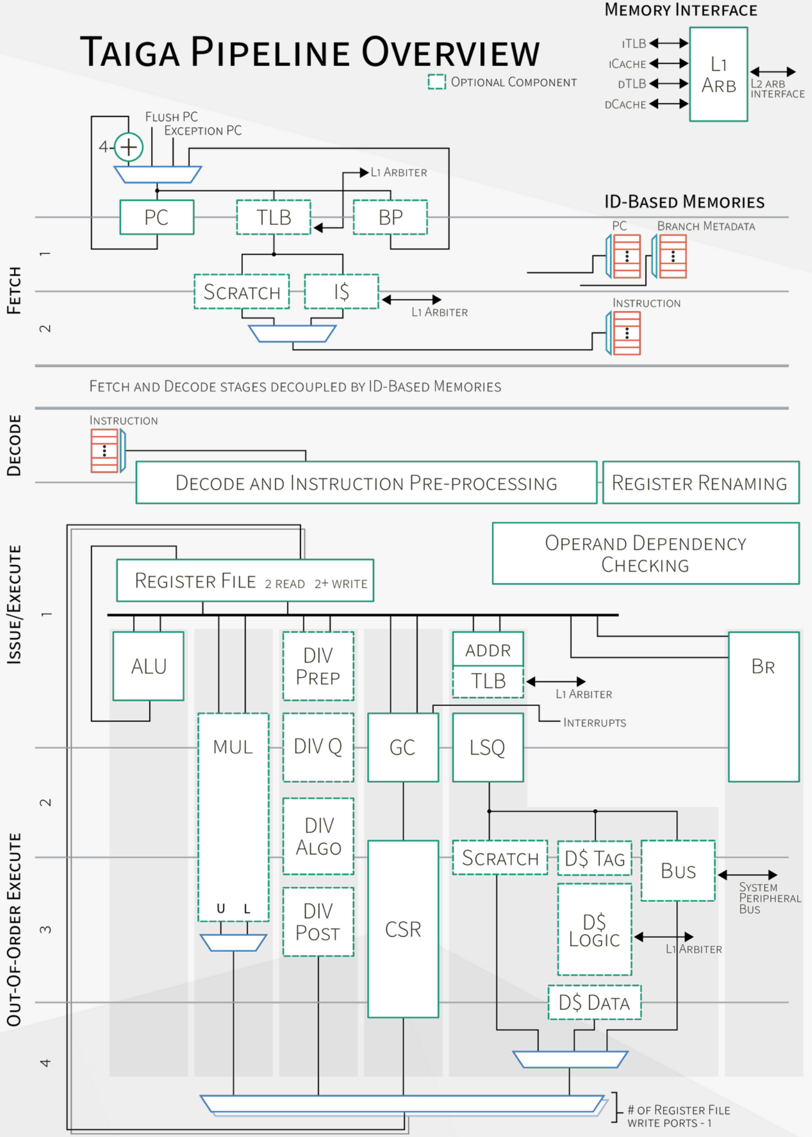
OpenHW Adoption

- Expands OpenHW's competitiveness to FPGAs
- Increased exposure and potential for increased verification and collaboration

Reference Slide



- Decoupled pipeline stages
  - 2-cycle fetch
- Fetch-to-Retire: Minimum 5-cycles (ALU)
  - Issue, Execute, and Writeback **stages can overlap**
- ID-based instruction tracking
- Register renaming
- Buffering between Fetch **and** Decode
- Support for multiple memory sources


Taiga Pipeline Overview

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