OpenHW Group

Proven Processor IP

CORE-V Verification Status Update

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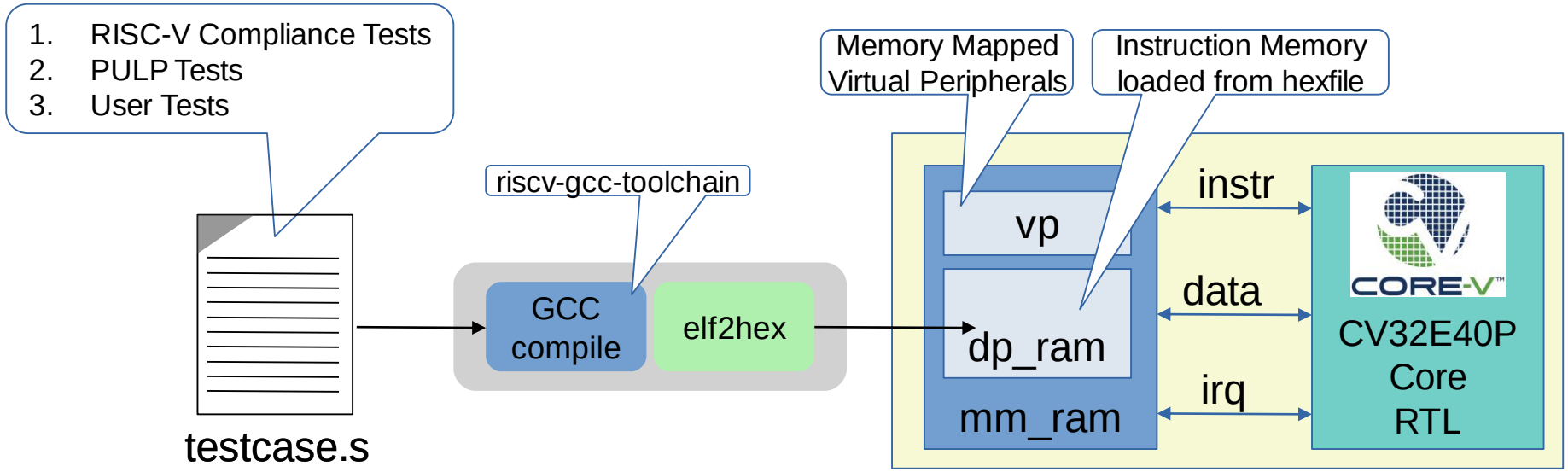
Objectives

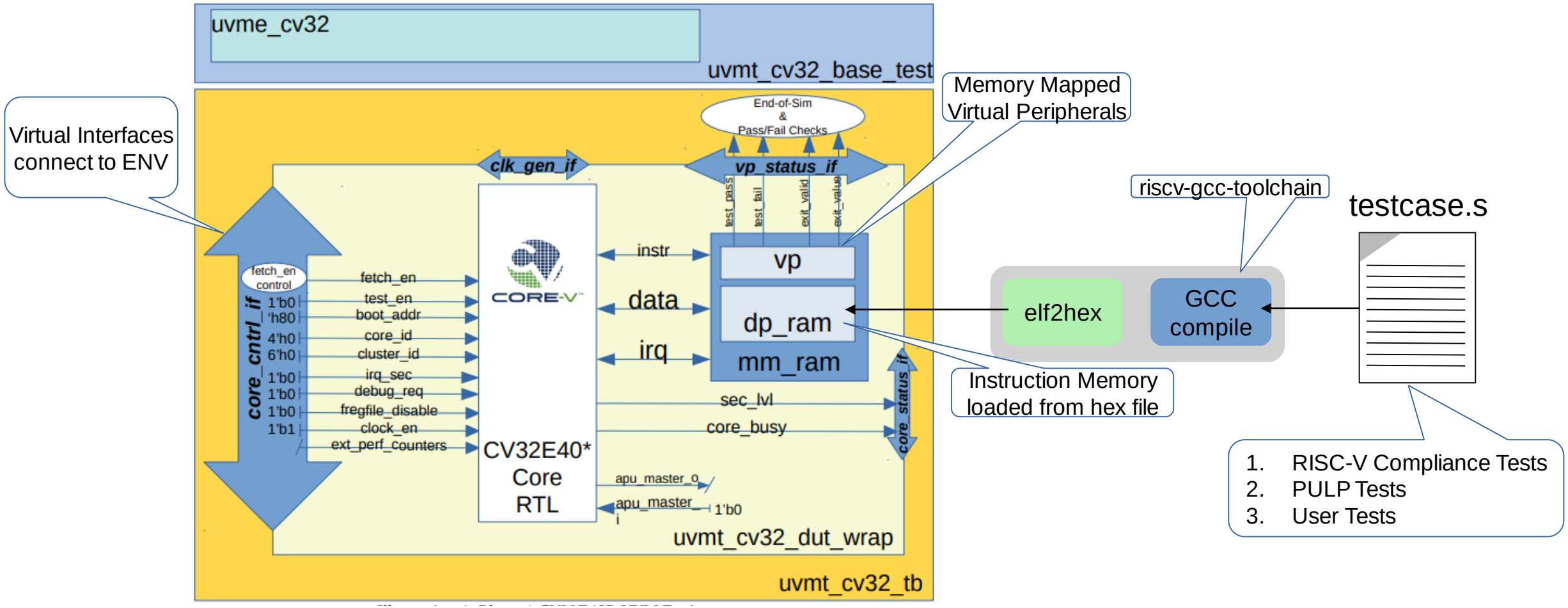
- Quick review and update of CORE-V verification (CV32E40P).
- Quick Status Update:
  - CV32E40P RTL has been moved from PULP to OpenHW
  - Vplans are (almost) as complete as they can be (waiting for User Manual)
  - “Core” testbench and UVM (uvmt-cv32) verification environment stable with DSIM
  - Workflow, including task management and continuous integration in place
- Understand Thales’s Contribution:
  - Detailed understanding who from Thales will be contributing to CV32E and CV64A verification:
    - Contribution level (days per week)
    - Skills
    - Specific tasks
- Is everyone on GitHub and MatterMost?

“CORE” Testbench

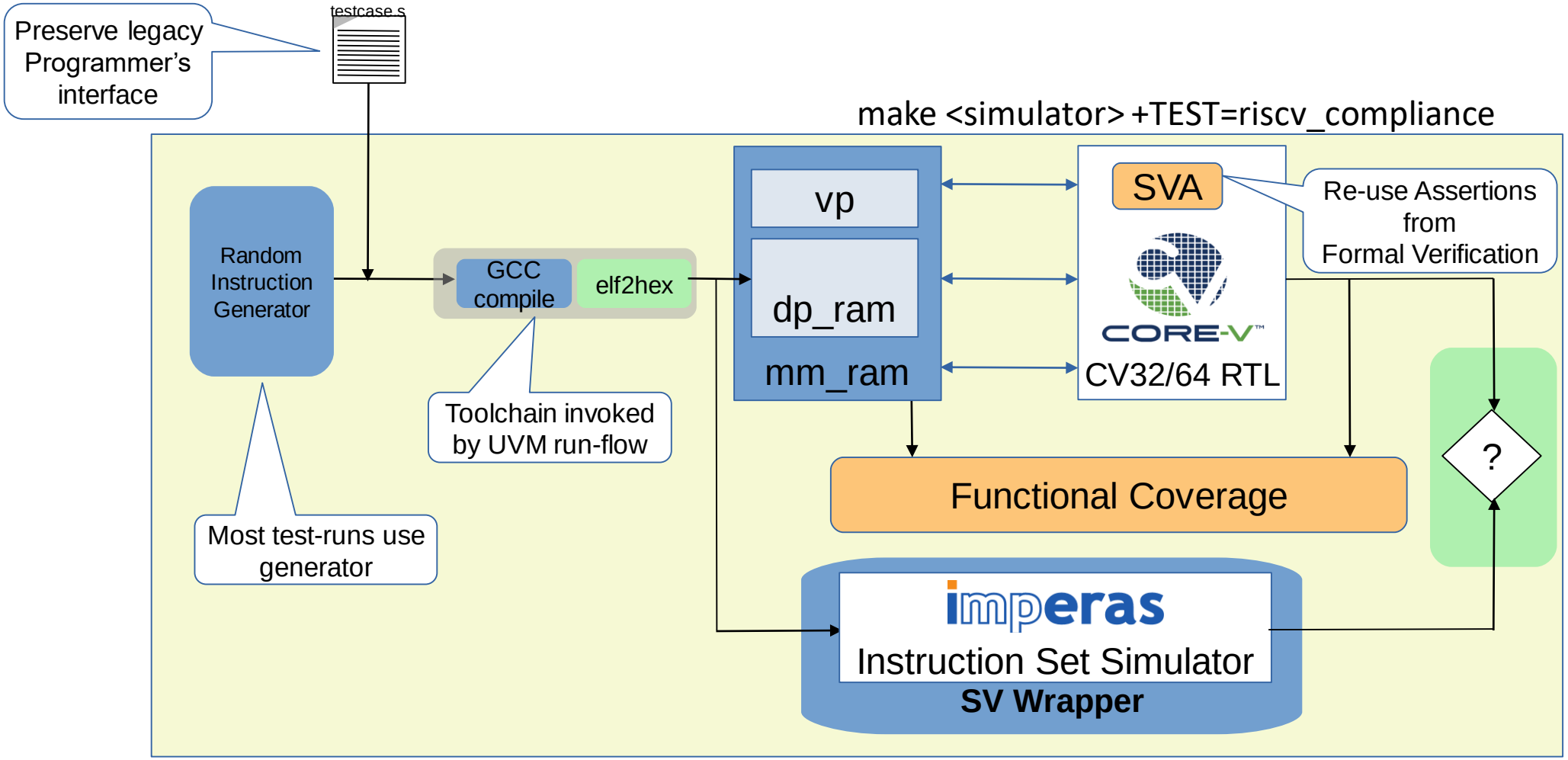


- At the request of several Member Companies, we will continue to maintain this Testbench:
  - Verilator will be supported on this Testbench.
  - OpenHW will not actively push on-going development of this Testbench other than to ensure it continues to function.

Phase 1 “UVMT_CV32” Verification Environment



Planned UVM Environment for CV32



Status of CORE and UVMT_CV32 as of 2020-03-06

- Both CORE testbench and Phase 1 UVMT_CV32:
  - Integrated with CV32E40P
  - Pervious work-around for issue #208 resolved
  - Properly clone RTL from source GitHub Repos and uses Designer Manifest.
  - Can run all inherited RISCY testcases (two known failures)

- Testplan review effort is blocked:
  - Architecture and Design team working to define CV32-specific specification.
  - No Designer time for reviews.

- Makefiles for both CORE and UVMT_CV32 continue to be an issue. Recommended solutions:
  - Enforce use of development branch (that is, all pull-requests to development, not master).
  - Move simulator-specific Make targets into separate files.

- Phase 2 development of UVM environment starting:
  - Integration of ISS
  - Early discussions regarding the Generator

Where Can Thales Help?

- Environment Stability
  - I need to ensure that the testbenches and verification environments are stable.
  - At this time Thales is the only Member Company using Questa, so your help is key.
- Near term activities:
  - Makefiles (hopefully we are almost there)
  - RISC-V Compliance Testing
    - The version of the Compliance tests we have is out-of-date.
    - We to audit each instruction and cross-reference to our testplans.
    - At least two tests are failing and nobody knows why. ☹
  - Pulp Compliance Testing:
    - State of these is not clearly understood.

Thank You!

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