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# Overview of the CVA6 open-source RISC-V application core

2022-11-17

OPENHW GROUP
PROVEN PROCESSOR IP

# Thales Overview

Over **81000** employees

**68** Countries Global presence

**1** bn € **Self-funded R&D***

* Does not include externally financed R&D

Sales in 2021 **16,2**bn €





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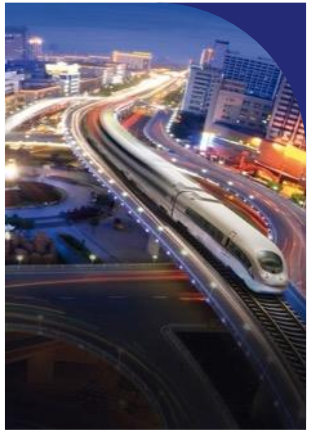
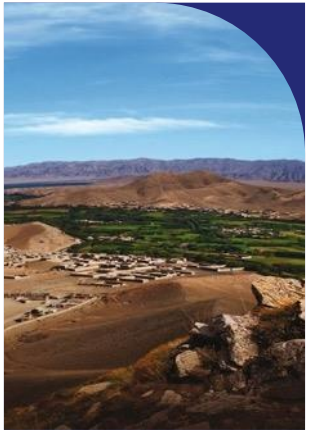
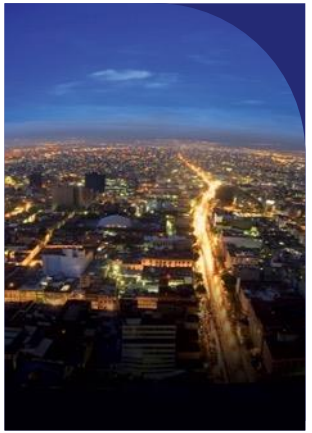
# Thales mission



**WHEREVER SAFETY AND SECURITY ARE CRITICAL, THALES DELIVERS.**
**TOGETHER, WE INNOVATE WITH OUR CUSTOMERS**
**TO BUILD SMARTER SOLUTIONS. EVERYWHERE.**

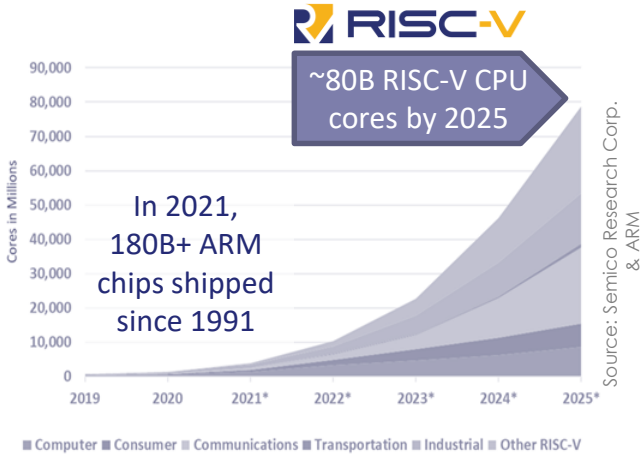
# What is RISC-V?

## Context

- ARM is the dominant player in the embedded processor market
- Licensing and royalty fees of proprietary ARM-based solutions

## Open HW: a credible FREE alternative for CPU cores

- RISC-V ISA initiative supported by a growing community
  - Membership more than doubled in 2021 to reach 2400 members
- Credible alternative to the ARM ecosystem
- Already many existing proprietary implementations
  - Andes Technology (V3/V5 cores), Google (Titan M2), GreenWaves (GAP8/9)
  - MIPS (eVocore), Intel (Nios-V), SiFive (E/S/U cores)
  - Gaisler (NOEL-V), Microchip (Mi-V), Nvidia (NV-RISCV)
  - And many more…
- And open-source RISC-V CPU designs
  - Western Digital (SweRV), Alibaba (XuanTie 910), ETHZ (PULPino)
  - OpenHW Group (e.g. CVAx), CHIPS Alliance, lowRISC (e.g. ibex, Rocket)
  - And many more…




**94 RISC-V chips (SoC, IP, FPGA) in 2021**

# Why Thales pays attention to RISC-V and open HW?

**Software**
*Large ecosystem compatible across implementations*

**Sovereignty**
*Possible commercial exploitation without export constraints*

**Performance**
*State-of-the-art processor*


**SWaP & customization**
*Exact fit between features and application needs*

**Security**
*A fully auditable processor*

**No vendor-locking**
*Business opportunities for support, customization…*

**Safety**
*No black-box*

# Our RISC-V communities


**RISC-V International** (“the Foundation”)

- Specifies the open **RISC-V instruction set**
  - ✓ Simple & modular
  - ✓ 32- or 64-bit
  - ✓ Custom extensions
  - ✓ Covers a wide range of needs, **from MCU to HPC**
- Currently specifying **upcoming optional extensions**
- Hosts several **special interest groups** (SIG)
- Does not deliver implementations


**OpenHW Group**

- **Not-for-profit corporation** steered by its members
- Goal: deliver **open-source IP for production SoCs**
  - ✓ RISC-V compatible cores
  - ✓ SoC IP blocks
  - ✓ Verification environment
  - ✓ Supporting SW and tools
- Permissive, open-source, export-friendly **license**

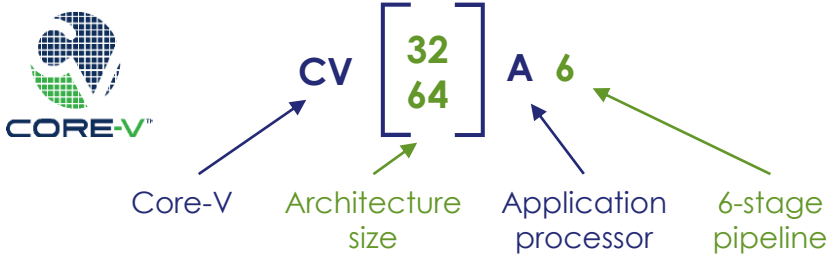
# CVA6 core

## Open-source RISC-V application core

- Supports rich OSes like Linux

## Common source code, two flavors:

- CV64A6
  - 64-bit
  - ARIANE donated by ETH Zürich to OpenHW
- CV32A6
  - 32-bit
  - Compact version designed by Thales





**An academic project turning into an industrial-grade CPU core**





Réf. : TRT-Fr/STI/LCHP/JQ,22/0018 – 2022-11-22
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# CVA6 architecture

- Fully compatible with the RISC-V open ISA
- 6-stage pipeline, single issue, branch prediction
- L1 data and instruction caches
- AXI4 interfaces
- M/S/U privileges
- Safe and secure features
- MMU and memory protection
- Ready for multi/many-core CPUs
  - e.g. open-source OpenPiton framework


A 6-stage application CPU

# Different cores, one solution

- 32/64 bit
- MMU / baremetal
- Floating-point: none, SP or DP
- Optional PMP (physical memory protection)
- Optional H (hypervisor) privilege mode
- Configurable L1 caches
  - Write-through/write-back
  - Size and number of ways
- Optional coprocessor interface (CV-X-IF)
- Design optimizations
  - ASIC/FPGA
  - Reset style (sync/async)

**Other options**

- C and A extensions
- Generic performance counters
- Bit extension on AXI (failure protection…)

**Configure CVA6 for your application and constraints, either on ASIC and FPGA**

**All configurations are RISC-V compatible and supported by GCC compiler**





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# An extendable core

## CV-X-IF interface to extend the CVA6 instruction set

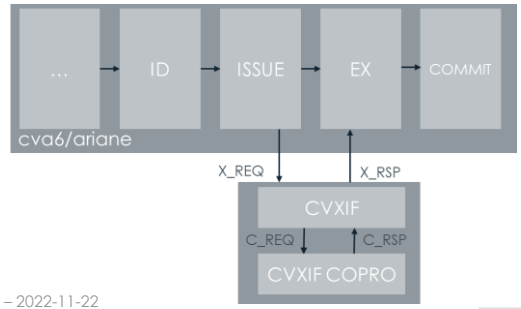
- Current or future RISC-V extensions (B, P…)
- Custom extensions (crypto, DSP, AI…)

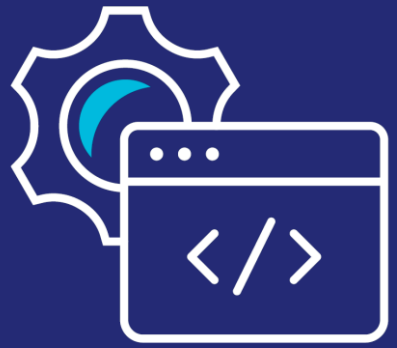
## CV-X-IF specified by OpenHW Group

- Open specification, can be used off OpenHW
- Reuse coprocessors between CORE-V cores (CVA6, CV32E40X, CVE2)

## Compiler support

- Seamless for RISC-V standard extensions (e.g. B)
- LLVM should ease the support of custom extensions
- Inline ASM possible for specific processing



**Speed up your application with a custom accelerator**

**Add extensions without fully re-validating the core**





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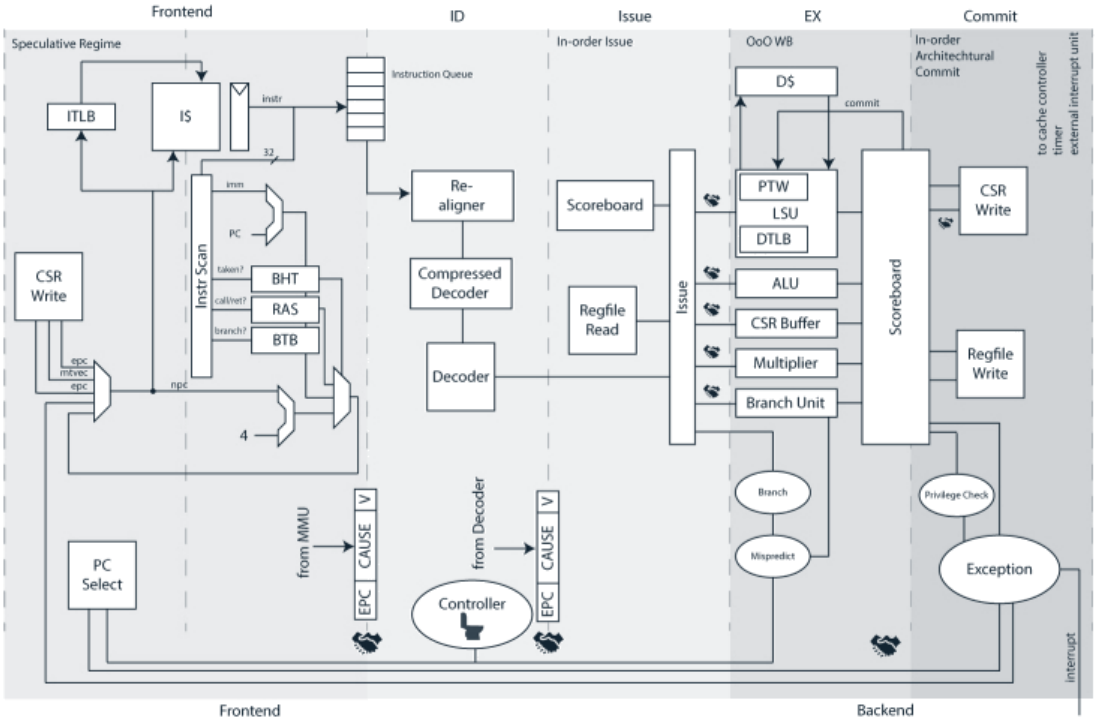
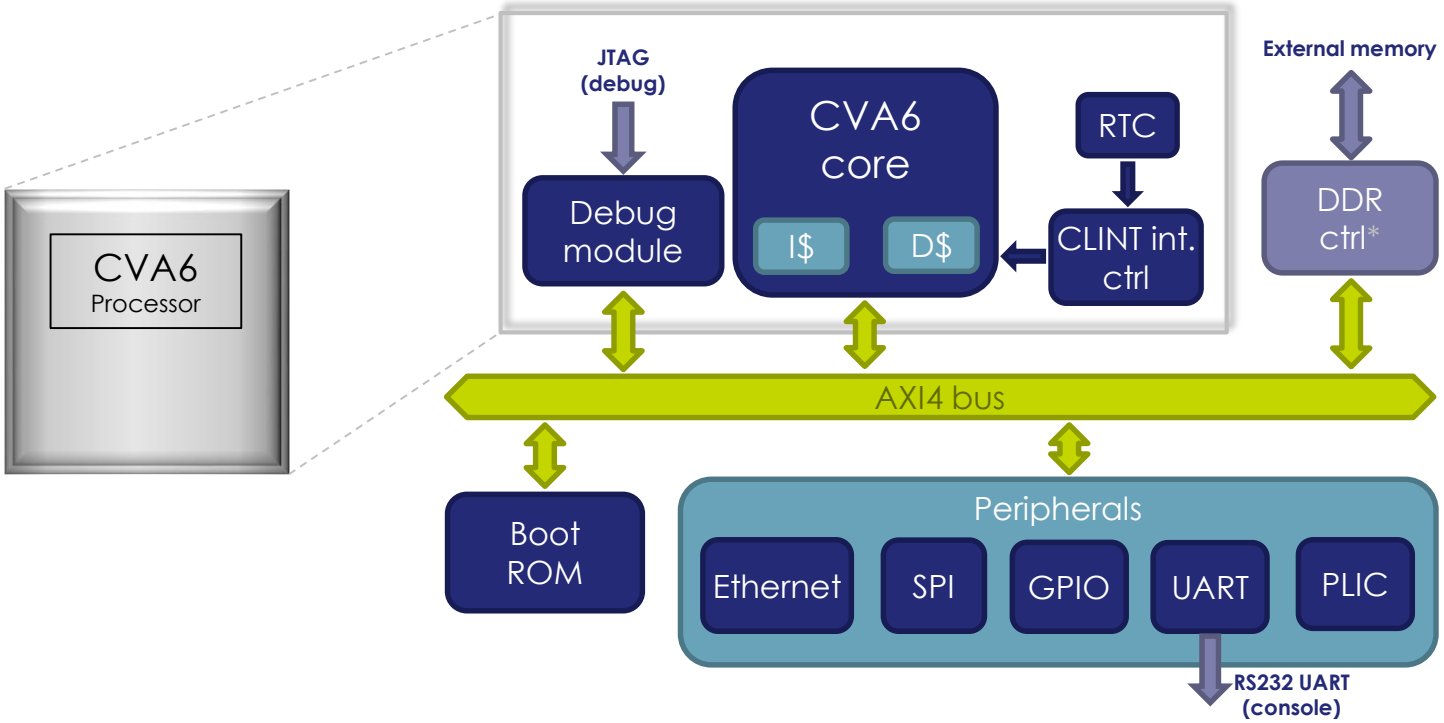
# CVA6 pipeline architecture & ISA




**CV32A6: RV32IMA[F][C]_Zicsr_Zifencei M/S/U [Sv32]**

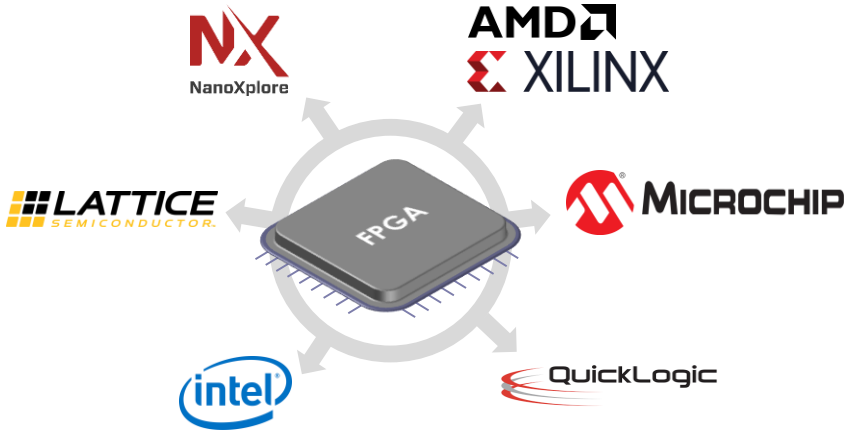
**CV64A6 - RV64IMA[F[D]][C]_Zicsr_Zifencei M/S/U[/H] [Sv39]**

# CPU sub-system



# Multi-sourcing

- For **ASIC targets** (32/64 bit)
- For **any FPGAs** (32 bit)




**Leverage your investment: reuse your HW/SW architectures throughout your product range (multi-sourcing: any ASIC and FPGA vendors)**

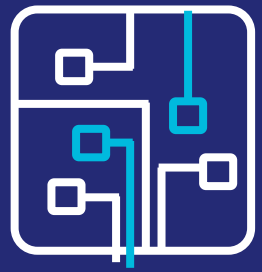
# HW implementations

| CV32A6 | FPGA | | | |
|---|---|---|---|---|
| Frequency | 189 MHz | | | |
| Performance | 2.8 CoreMark/MHz<br>530 CoreMark | | | |
| Resources | 8,108 LUT | 4,534 FF | 12 BRAM | 4 DSP |
| Technology | Zynq UltraScale+ -3 | | | |
| Configuration | RV32IMA, 8K D$ + 8K I$, noFPU, MMU | | | |

Upcoming commit of FPGA optimizations to OpenHW GitHub

| CV32A6 | ASIC |
|---|---|
| Frequency | 900 MHz |
| Performance | 2.93 CoreMark/MHz<br>2637 CoreMark |
| Resources | 80 kgates |
| Technology | 28 nm (worst case corner) |
| Configuration | RV32IMA, 8K I$ + no D$, noFPU, MMU |

Coremark conditions: gcc10.2.0, -O3 -funroll-all-loops -fno-tree-loop-distribute-patterns -DPREALLOCATE=1 -fvisibility=hidden -mcmodel=medany -lgcc -ffunction-sections -fdata-sections -Wl,-gc-sections -falign-jumps=4 -falign-functions=16



**Ongoing work.**

**More optimizations are coming!**





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# SW ecosystem

**Boot and FW**

- **U-Boot**
- **OpenSBI**

**OS support**

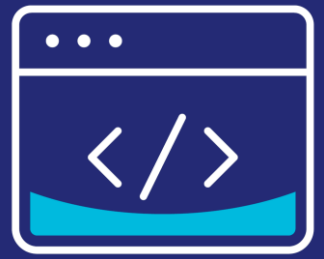
- **Linux:** 32 & 64 bit
- **Yocto** honister, Buildroot 2021.08
- **FreeRTOS:** 32 & 64 bit
- CVA6 compatible with many others

**Compiler**

- Standard **GCC** (11.2)
- Libraries: **glibc** (2.70) & others
- LLVM on the roadmap

**Debug**

- HW and baremetal: JTAG probe, OpenOCD, GDB
- Linux-based: GDB server, GDB/Eclipse IDE



**Full open-source software ecosystem**

**Protect your HW investments**

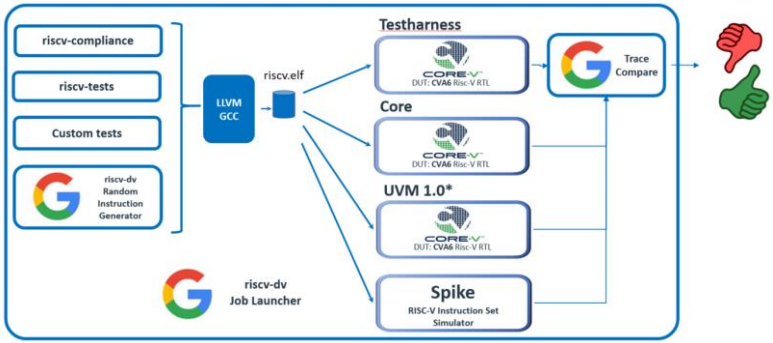
# CVA6 verification

## Continuous integration (CI)

## Leverages Google open-source components and OpenHW methodology

## Next steps:

- Complete UVM testbench
- New test sequences
- 100% functional coverage (UVM-based)



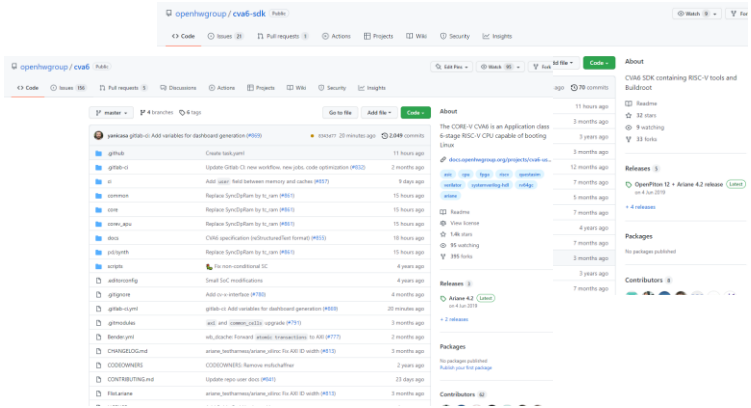

**Verification artifacts will be available as open-source.**

**Target is 100% verification coverage.**

# Open-source project

## Complete open-source package

- CVA6 core
- Verification: testbench, sequences, ISS…
- Linux, FreeRTOS support
- SolderPad HW license (no contamination)



https://github.com/openhwgroup/cva6
https://github.com/openhwgroup/cva6-sdk
https://github.com/openhwgroup/core-v-verif

**Evaluate CVA6 now for your next products generation**

**Open-source eases collaboration.**

# Open-source is suited for industrial use

## OpenHW governance

- Not-profit organization steered by its members
- Based on Eclipse Foundation's processes
- Target industrial-grade quality

## Participation is encouraged:

- Share IP development costs
- Influence technical content
- Get recognized as a contributor

## Apache / Solderpad permissive licences

- Freely use, modify, integrate in proprietary solutions
- No need to publish modifications, no viral effect

## Value generation

- Share cost instead of purchasing proprietary IIP
- Customize for own application
- Increase control on your solutions
- Easier white box certification

## Business models

- Commercial SW/HW/tooling add-ons
- Maintenance and support offers

## Reduced supplier / export risks

- Ability to fork; no end-of-life
- Significantly lower exposition to export control

# First industrial adoptions of the CVA6


Thales is developing a CVA6 secure processor
*(other applications under study)*

Other companies are considering CVA6:
- Edge computing
- Automotive domain
- Industry 4.0
- Space/aerospace

# Intel Pathfinder



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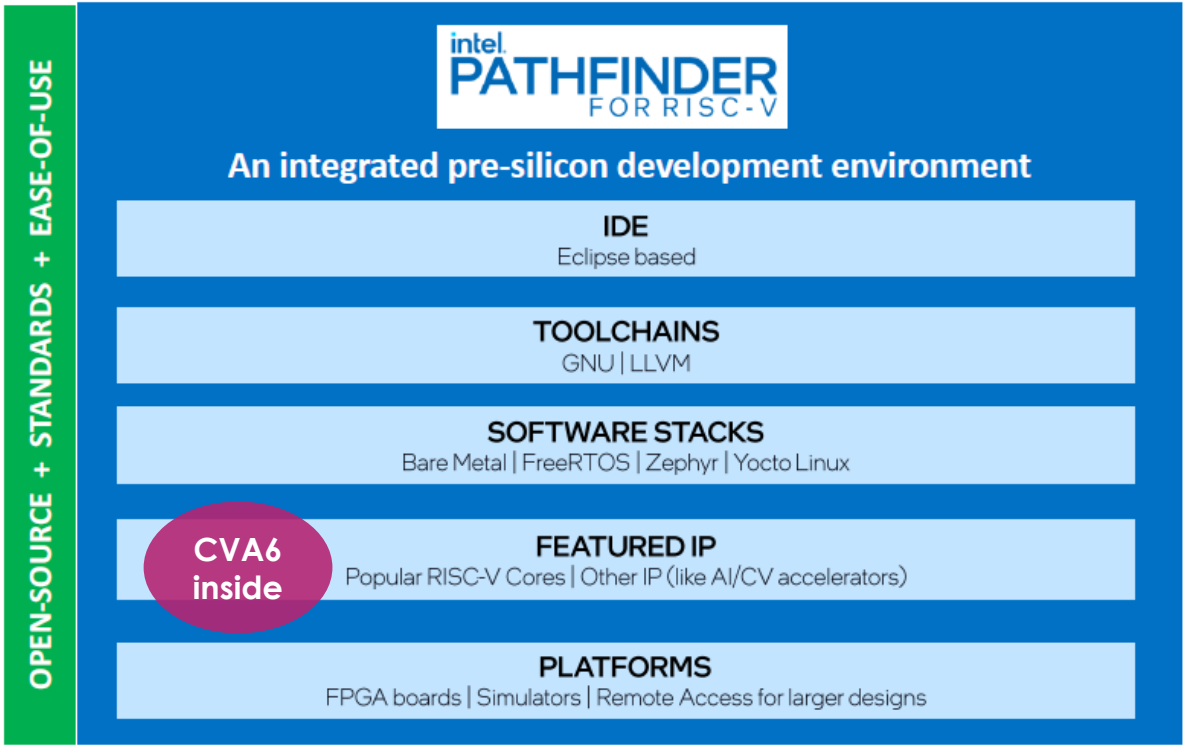
PROVEN PROCESSOR IP

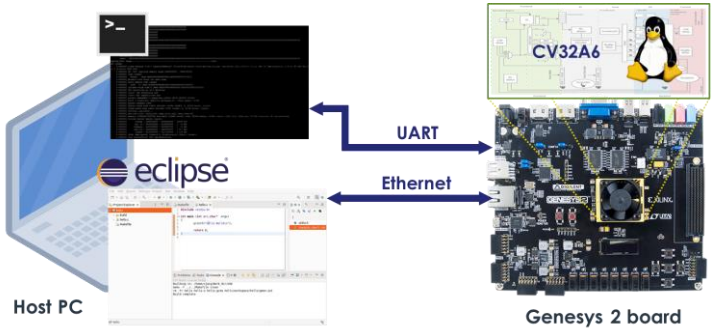
welcomes a new member to the fold



# Demonstrator

## Demonstrates the maturity of the CV32A6 soft-core processor

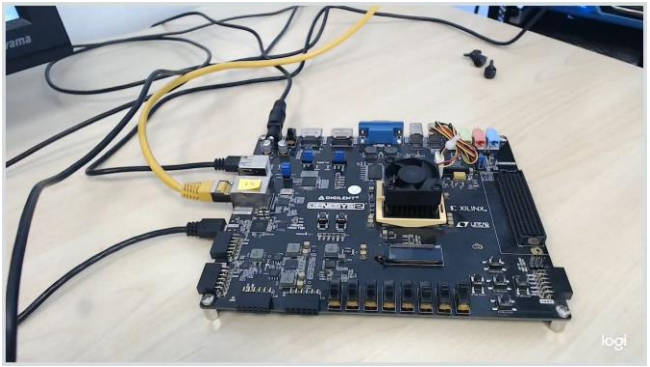
- Implementation on the Genesys 2 FPGA board
  - Kintex7 (XC7K325T-2FFG900C)
  - DDR3
  - Programmable over JTAG and Quad-SPI Flash
  - Ethernet Link with the host
- State-of-the-art boot flow
  - U-Boot
  - OpenSBI
  - Buildroot 2021.08
- Linux OS running



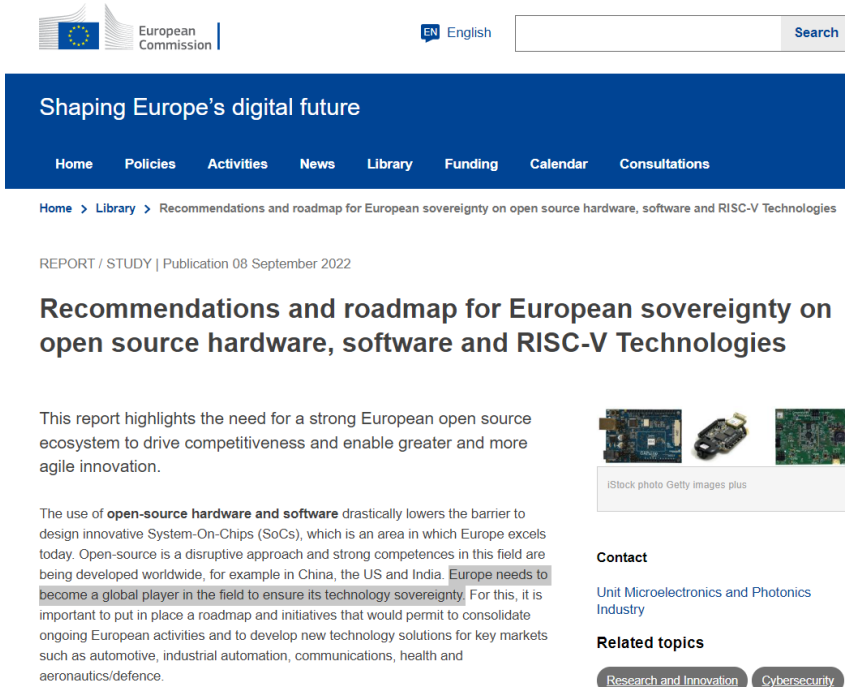

## Ready for SW development

- GNU/Linux standard developer tools
- Eclipse IDE debug environment

Also works on Microsemi Polarfire



# RISC-V and open-source HW European opportunities



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Shaping Europe's digital future

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Home > Library > Recommendations and roadmap for European sovereignty on open source hardware, software and RISC-V Technologies

REPORT / STUDY | Publication 08 September 2022

**Recommendations and roadmap for European sovereignty on open source hardware, software and RISC-V Technologies**

This report highlights the need for a strong European open source ecosystem to drive competitiveness and enable greater and more agile innovation.

The use of **open-source hardware and software** drastically lowers the barrier to design innovative System-On-Chips (SoCs), which is an area in which Europe excels today. Open-source is a disruptive approach and strong competences in this field are being developed worldwide, for example in China, the US and India. Europe needs to become a global player in the field to ensure its technology sovereignty. For this, it is important to put in place a roadmap and initiatives that would permit to consolidate ongoing European activities and to develop new technology solutions for key markets such as automotive, industrial automation, communications, health and aeronautics/defence.

iStock photo Getty images plus

**Contact**

Unit Microelectronics and Photonics Industry

**Related topics**

Research and Innovation Cybersecurity

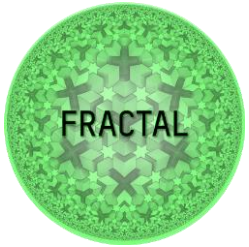
## Already two RISC-V KDT calls:

- HORIZON-KDT-JU-2021-1-IA "Development of open sources RISC-V building blocks"
- HORIZON-KDT-JU-2022-1-IA "Design of Customisable and Domain Specific Open-source RISC-V Processors"
- 40 M€ EU + 40 M€ national funding

## RISC-V adopted in several European projects:

- H2020 De-RISC
- ECSEL FRACTAL
- HE NeuroSoC
- EuroHPC eProcessor
- ESA…

# Acknowledgement




https://fractal-project.eu/

https://www.linkedin.com/company/fractal-european-research-project/

@project_fractal

Some Thales Research & Technology's CVA6 activities are supported by the FRACTAL project which has received funding from the ECSEL Joint Undertaking (JU) under grant agreement No 877056. The JU receives support from the European Union's Horizon 2020 research and innovation programme and Spain, Italy, Austria, Germany, Finland and Switzerland.

# Conclusion

## Join the development of an industrial-grade open-source processor

- Get European support
- Influence next developments for your future products

## Participate in the next open-source revolution

- The next “Linux” for hardware CPUs

## Use the CVA6 in your future products

- For ASIC and FPGAs
- With a strong open SW ecosystem

“Technology is best when it brings people together”
Matt Mullenweg

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# Thank you.

www.thalesgroup.com