HPDcache (CV L1-Dcache) Project

OpenHW Group - Interconnect Task Group - Monthly Status

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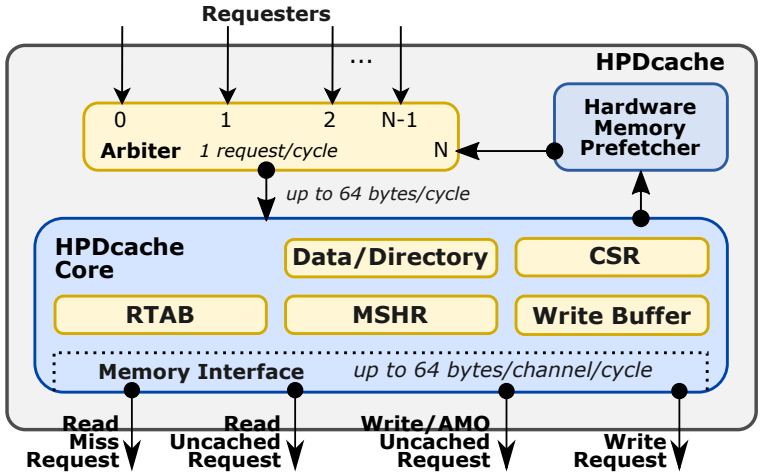
December 14, 2023

Outline

1. Overview
2. Performance
3. Gate Status and Schedule

Description

High-Performance, Out-of-Order, Level-1 Data Cache (HPDCache) compatible with RISC-V processor cores.

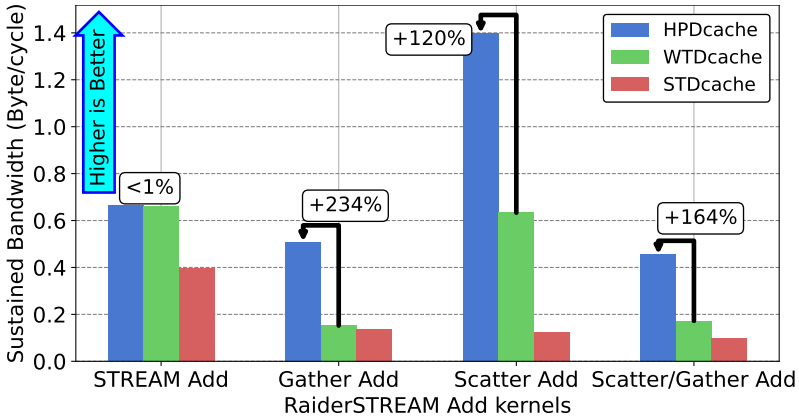


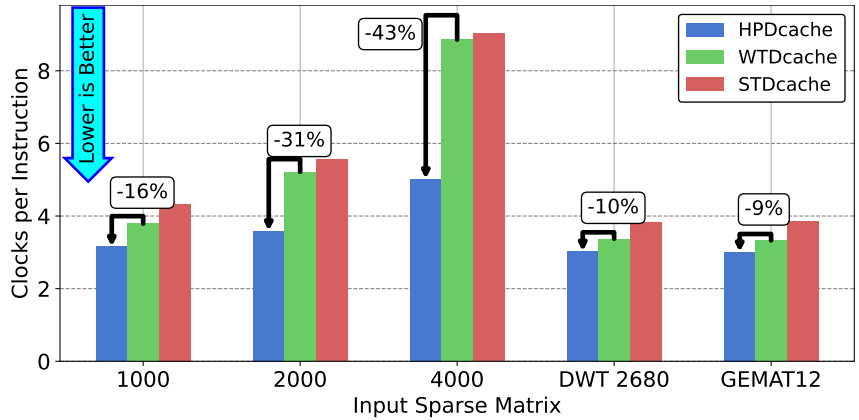
Highlights

- Successfully integrated with the CVA6 core.
- Support of multiple independent requesters, such as, CORE-V cores and tightly coupled accelerators.
- Allow high and flexible bandwidth between this cache and the requesters (up to 64 bytes/cycle).
- Supports a high (configurable) number of miss requests to the memory.
- Highly configurable (capacity, NoC interface width, dimensioning of internal buffers,...)

Performance

Throughput





Implementation[a]

CVA6-HPDcache/CVA6-WTDcache:

- **Area**: 5.92% larger (0.386mm^2 / 0.364mm^2)
- **Clock Frequency**: 2.06% faster (950MHz / 931MHz)

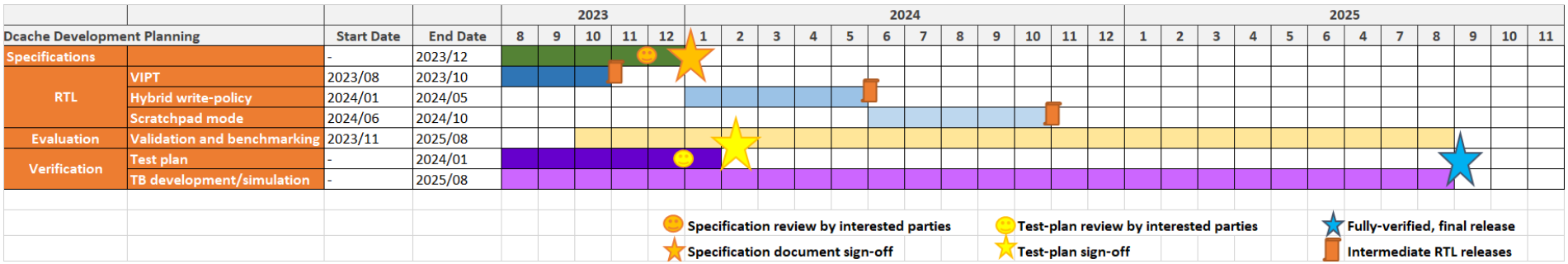
[a] GF22FDX Technology

Other related works

- Successfully integrated in the OpenPiton Cache-Coherent Multi-Core platform. Validated in platform with up to 16 CVA6+HPDCACHE cores.
- Barcelona Supercomputing Center (BSC) has successfully integrated the HPDcache with the recently open-source RISC-V core Sargantana.

Gate Status and Schedule

Current Gate: Project Concept → Project Launch → **Plan Approve**



Deliverables	Planned Date	Status
Specification/User Documentation	2023-12	Delayed (1 month)
Test-Plan	2024-01	Delayed (1 month)