CORE-V 180 MCU Update of October 23, 2023

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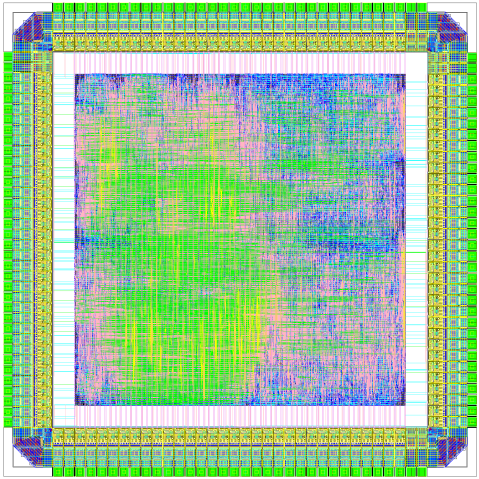
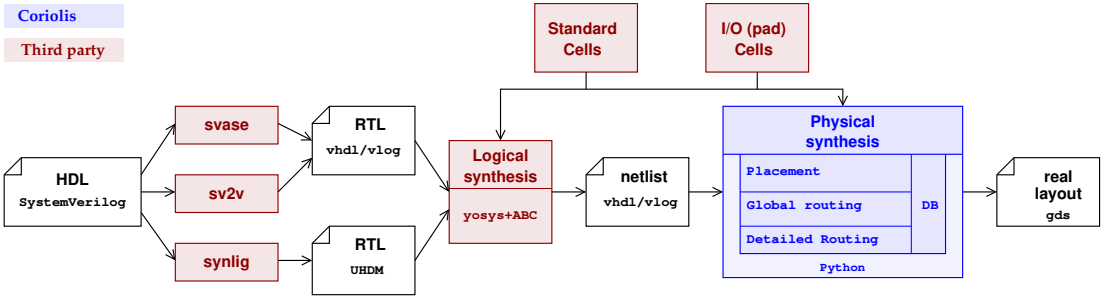
First Experiment



- The cv32e40p chip.
- Global Foundries 180nm.
- 50984 gates.
- 3.4 × 3.4 mm.
- `https://github.com/lip6/core-v-180-mcu.git`
  Can be reproduced with the `"cv34e40p layout (GDS)"` workflow (action).

Basic Design Flow



[SVase]	Not working
[sv2v]	Work on whole c32e40p
[synlig]	Work on sub-blocks of c32e40p

Design Kit Components

	Components		
Provider	Standard Cells	I/O lib	SRAM
[Chips4Makers] (c4m)	✓	–	–
[GF180MCU]	–	✓	–
LSxLib (symbolic)	–	–	–

Coriolis can use any combination of the above components.

First Findings

- The translation from SystemVerilog to Verilog :
  - The problem of the subset of translatable SystemVerilog construct for each tool.
  - Adapting the code so that it use the valid subset ?
  - Waiting for the tools to complete their features, maybe directly reaching to them ?

- Design size evaluation :
  - The c32e40p doesn't fit in a 3×3 mm area.
  - The standard cells are not optimized (yet), and their areas are around 50% too big.
  - So, in any case, we need to drastically reduce the number of peripherals

Questions & Next Steps

- The design flow, for now, is only a generative one. Checks must be performed, especially at the SystemVerilog to Verilog step.
- The set of peripherals needs to be redefined, it must be done in accordance with the kind of applications that is targeted.
- Support for GF 180 MCU standard cells in Coriolis, to get more accurate area estimations.

Références

- GF 180 MCU `https://github.com/google/gf180mcu-pdk.git`.
- Chips4Makers `https://chips4makers.io/`.
- SVase `https://github.com/pulp-platform/svase.git`.
- sv2v `https://github.com/zachjs/sv2v.git`.
- synlig `https://github.com/chipsalliance/synlig.git`.