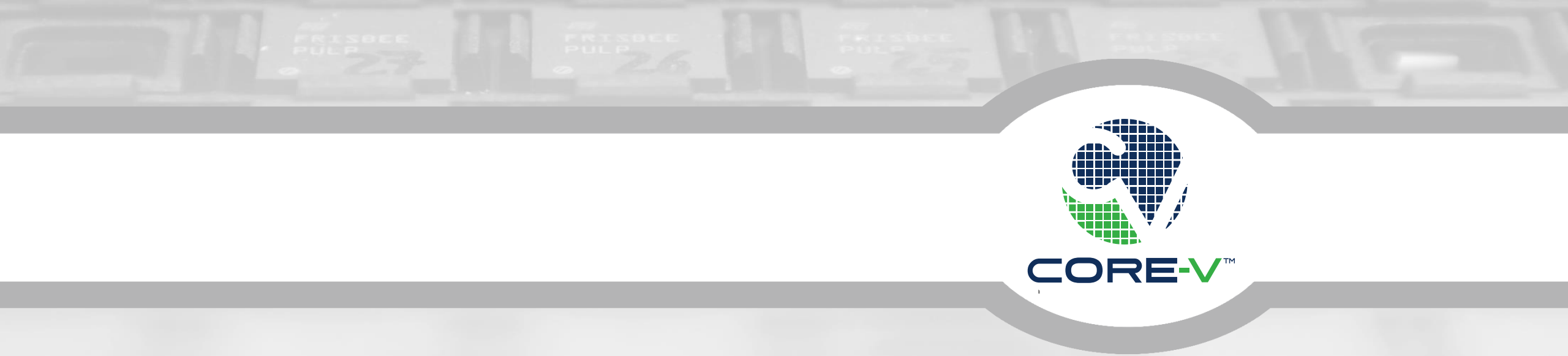


CORES TG – April 12 2021

Arjan Bink

Jérôme Quevremont

Davide Schiavone

Agenda

- CV32E40P updates
  - RVFI
  - LEC
  - X-interface ETH Thesis
- CV32E40X status
- CVA6 status
- Gates and TRLs

CV32E40P updates

Davide Schiavone

CV32E40P RVFI

- Behavioral model written as synthesizable RTL
  - NRET=2
    - Up 2 instructions retiring in the same cycle
  - 2 write ports per NRET
    - XPULP instructions (load post increment) can write 2 values to the RF

- Partially working on core-v-verif
  - Steve is testing it
  - Missing Imperas licence on CMC machines to continue working with that

- To be tested with debug
- Missing CSR interface

CV32E40P Cadence Conformal LEC script

- Developed first draft of script to check whether a revised RTL is LEC with the frozen RTL

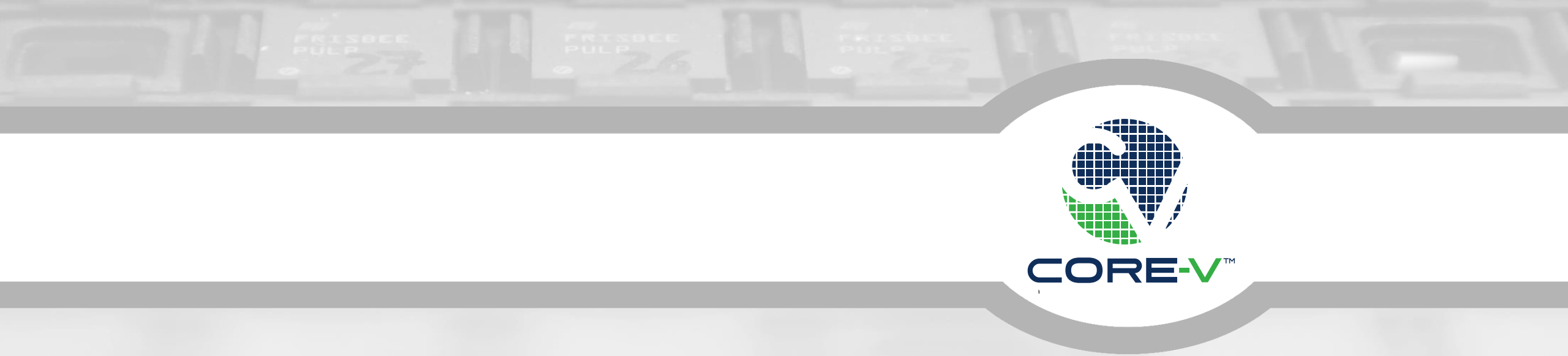
- PR #633 (https://github.com/openhwgroup/cv32e40p/pull/633)
  - **Need for expert people to revise it**

- Open Questions:
  - Do we allow new interfaces in the revised core?
    - e.g. X interface

CV32E40P X-Interface ETH Thesis

- ETH is implementing the first draft of the X-interface to CV32E40P to replace the APU interface
  - The APU interface hasn't been verified and it is used only for RV32F
  - The X-interface will replace the APU to offload RV32F instructions to a co-processor
  - When FPU parameter = 0, the core must be Logically Equivalent to the frozen version
- Scoreboard and pseudo dual-issue
  - The FPU pipeline independent from the core pipeline
  - The core can have *out-of-order* writes to the RF
  - *e.g. fdiv taking 3 cycles*

Cycle	IF Stage	ID Stage	EX Int Stage	EX FP Stage	WB
1	fdiv				
2	add	fdiv to X-interface			
3	sub	add		fdiv	
4	…	sub	add	fdiv	
5	…		sub	fdiv	add
6	…				**sub | fdiv**

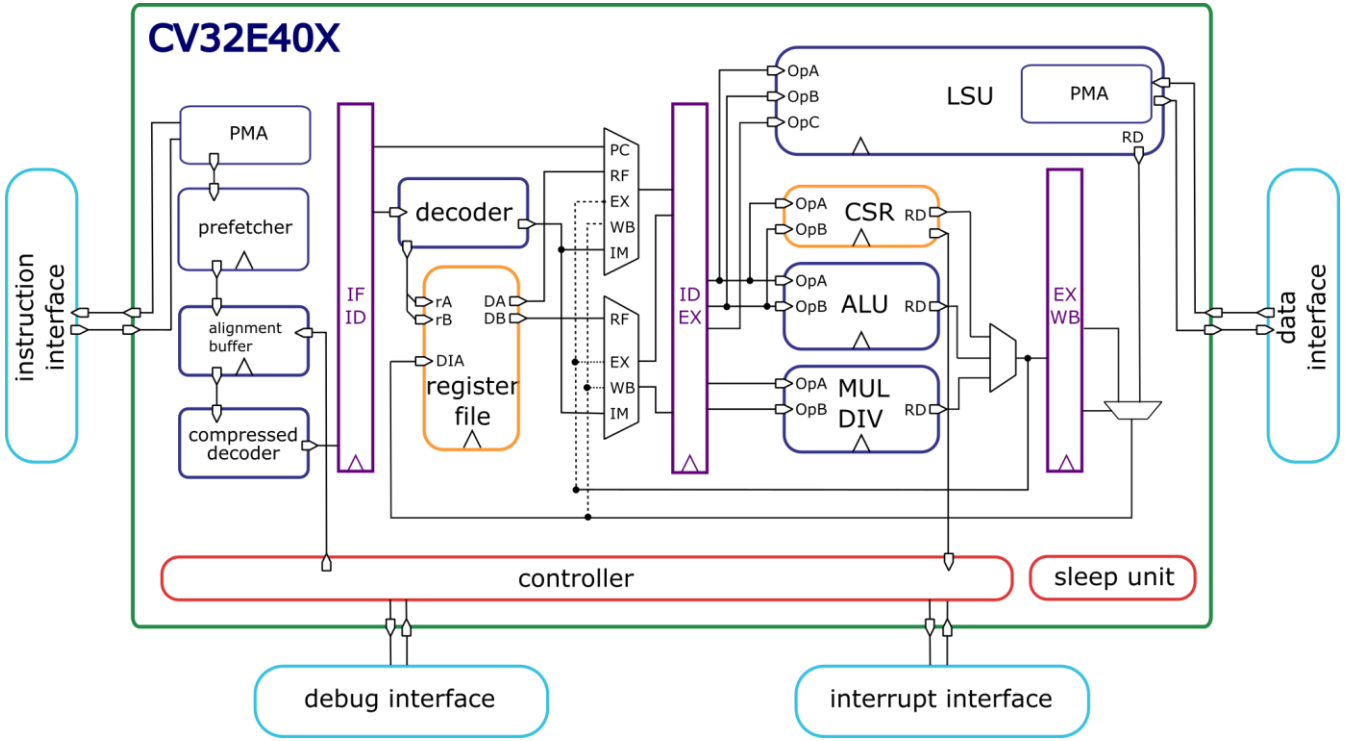


CV32E40X status

Øystein Knauserud

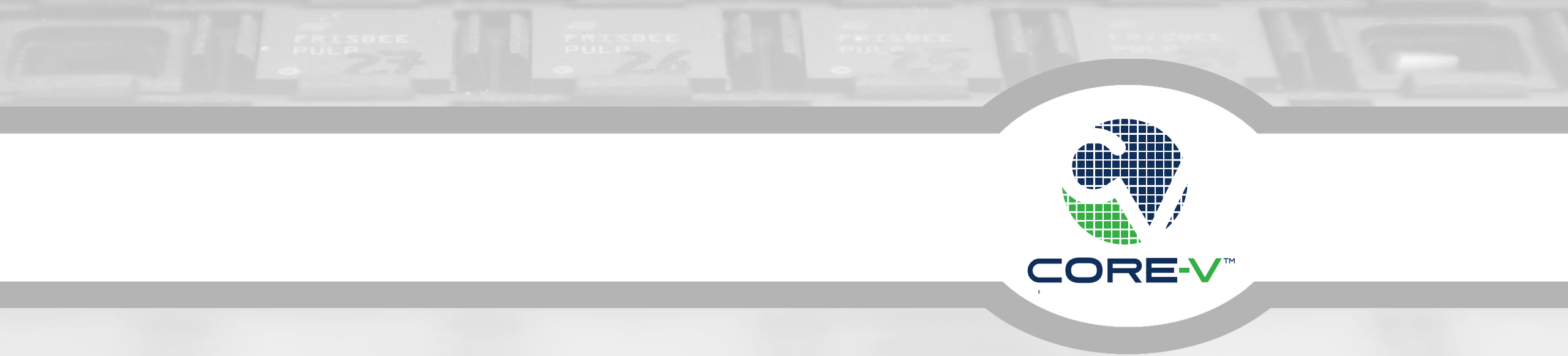
CV32E40X p.1

- Removed PULP, APU, FPU
- Optimized ALU/MUL
- Optimized instruction prefetching
- Parametrized RF number of R/W ports (current configuration is 2R+1W).
- Split decoder (I, M, C, etc.)
- Instruction side bus error and PMA
- Introduced structs for pipeline registers
- SystemVerilog interfaces internally for instructions and data
- Moved assertions out of RTL, binding assertions in wrapper



CV32E40X p.1

- Same (or better) cycle count as CV32E40P
- ~6% reduction in speculative instruction fetches (dependent on code executed)
- MULH* latency reduced from 5 to 4 cycles
- 13.4 % reduction in cell area as compared to same configuration CV32E40P with identical constraints



CVA6 status

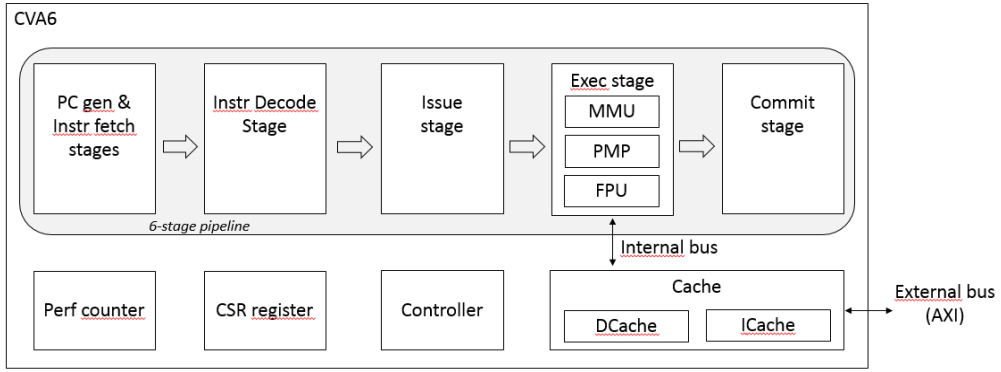
Jérôme Quévremont

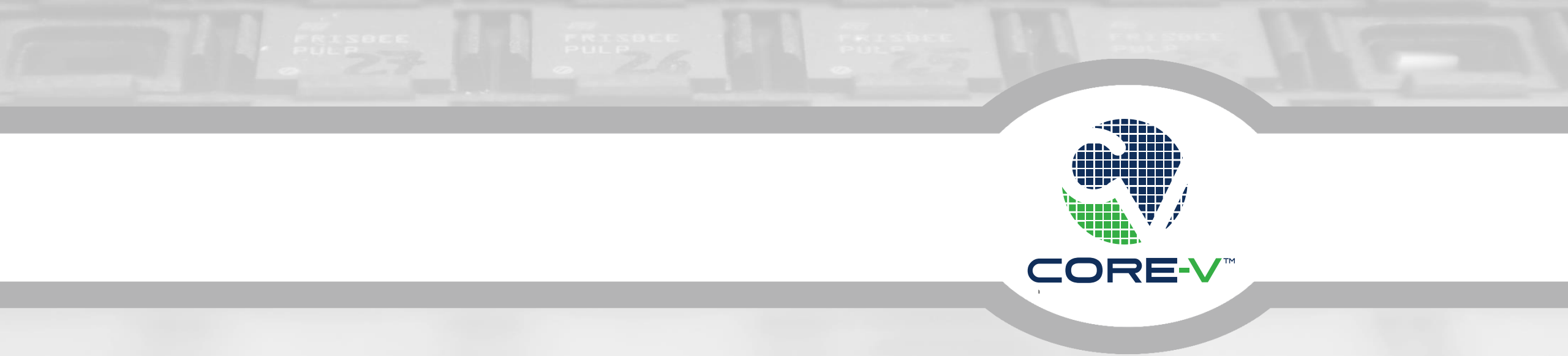
CVA6

- Gates
  - PC (former PPL) passed
  - PL passed
  - PA (former PPA) to come: specification and detailed plan
- Meetings
  - https://calendar.google.com/calendar/u/0/embed?src=meetings@openhwgroup.org
  - Progress meeting every second week:
    - April 9th
    - April 23rd…
  - “Save the date” technical meeting every other week:
    - April 16th: verification strategy
- TWG:Cores:CVA6 Mattermost channel
  - Not only “Cores”, Verification topics also addressed…

CVA6: current activity

- Defined the “scope of the IP”
  = verification target
  - Renamed (from DUT) as several testbenches might be needed
  - Important step to scope specification
- Specification on going
  - https://docs.google.com/document/d/11rsoO5WKraMCraSpnsVqmt4hJaCcDG0zq7LTWdXVkf0
  - Need to request editor privilege
  - Later converted to Ascii Doc
- RV32F support in CV32A6 progressing well
  - Analyzing the feasibility of RV32D support in CV32A6
- Ongoing: How to transition from existing DV environments to core-v-verif





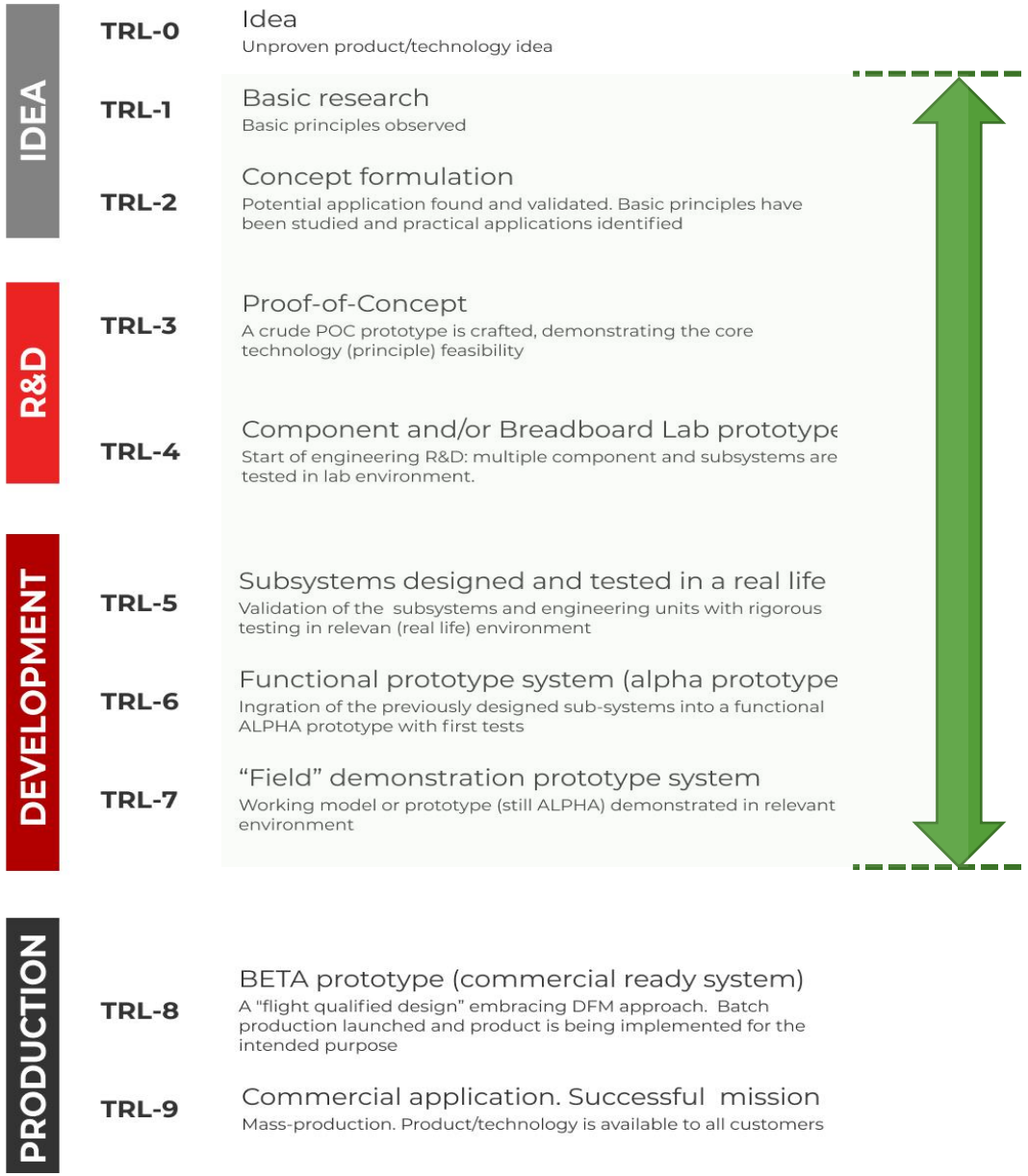
Gates and TRLs

As presented at OpenHW Day, April 1st

OpenHW Project Framework

Gate	Purpose	Criteria
PC Project Concept	Green-light of project concept by TWG	Proposed scope, initial view of the components and features, why do this project?
PL Project Launch	Full project launch approval by TWG	Outline of the requirements, features, components, project supporters, risks, high level schedule
PA Plan Approved	Communicate project plan to TWG, (allowing member participation and review	Project plan full checklist, project methodology. initial agile backlog, requirements specification
Project work		
PF Project Freeze	Completion of releasable project content	RTL Freeze checklist or other final checklist has been completed

TRL Scale



OpenHW Technology Outputs

OpenHW IP Adopters

TRL Levels as Utilized by OpenHW

TRL	OpenHW Utilization
1- Basic Principles Observed	• OpenHW research projects may target TRL-1 as project output, e.g. to develop novel approaches to core or accelerator architecture
2- Concept Formulation	• Core IP or accelerator development projects to produce open source technology are typically initiated as TRL-2 concepts, identifying principles and applications of the IP • The OpenHW Project Concept Gate output includes a TRL-2 description of the Core IP
3- Proof of Concept	• Core IP or accelerator development projects will pass through TRL-3 as the (RTL) design completes. Poof of concept is shown by core compilation and demonstration of basic operations (e.g. Linux booted, Coremark results, hello-world)
4- Component Prototype	• Core IP or accelerator projects will pass through TRL-4 as they produce preliminary PPA results (via synthesis scripts for FPGA or ASIC) and/or run preliminary application code, such as an accelerator running machine learning code.
5- Subsystem Designed and Tested	• Core IP projects reach TRL-5 as they complete full verification. The OpenHW RTL Freeze checklist process verifies that the design is fully ready for industrial adoption.
6- Functional (Alpha) Prototype	• OpenHW designed IP that is integrated into an MCU system or other device reaches TRL-6 as prototype Silicon is fabricated and demonstrated
7- Field Demonstration Prototype	• OpenHW development boards incorporating a prototype Silicon system with OpenHW Software reach TRL-7 as they are demonstrated and deployed