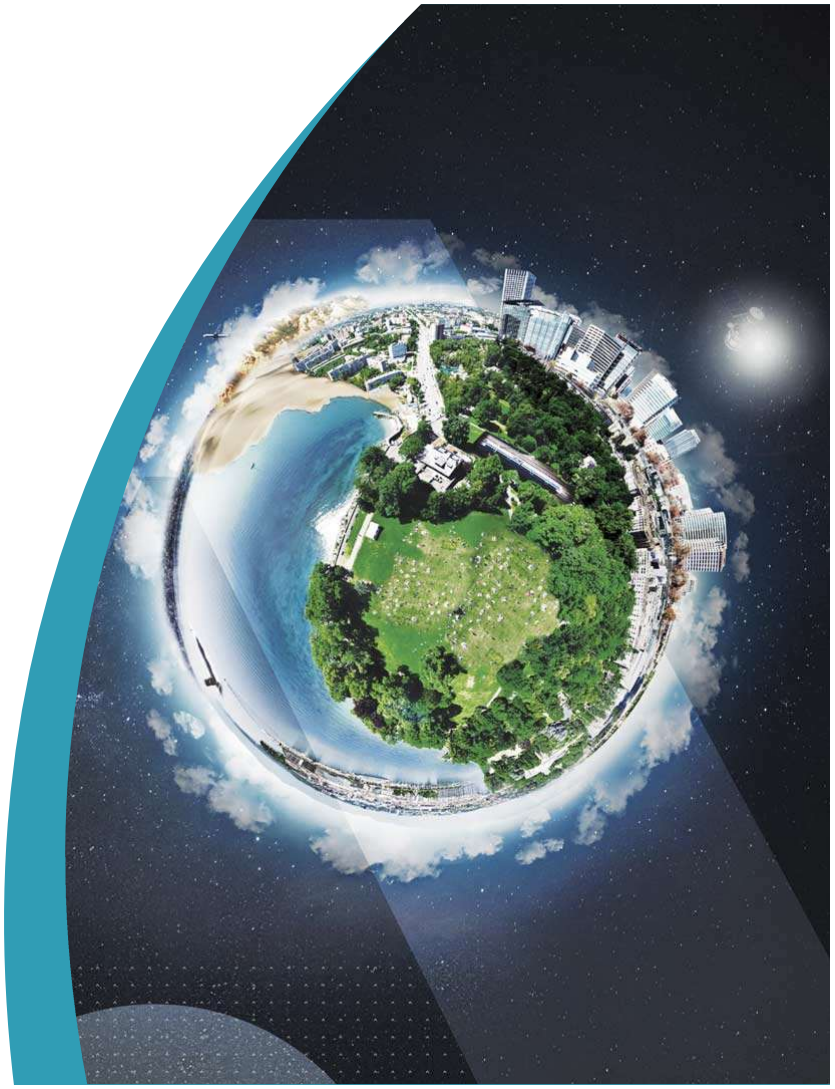
THALES

cva6_reorg branch:
cva6
core-v-verif
riscv-dv

2021-06-16



Commit summary

cva6 repository

- Support of rvfi
- Support of vcs
- Support of vsim
- FPGA build

core-v-verif repository

- Directories reorganization (similar to cve4)

Link between cva6 and core-v-verif modifications

riscv-dv repository

- Support of two DUT (veri-uvm: core, veri-testharness: corev_apu)

CI server

Configurations

- XLEN: 32-, 64-bit
- DUT: uvm, testharness
- Test suites: riscv-tests, riscv-compliance (as still more tests than riscv-arch-test)

Access to identified guests

- Next week

Pending points

PR pending on pulp-platform/riscv-dbg

- Needed for 32-bit verification
- https://github.com/pulp-platform/riscv-dbg/pull/83

Verilator multithreading

- 32-bit configuration not working with 4 threads

Execute test suites

- $ git clone git@github.com:ThalesGroup/core-v-verif.git -b pr/thales-cva6_reorg
- $ cd core-v-verif
- $ export RISCV=/path/to/gcc
- (optional if already installed) $ export VERILATOR_ROOT=/path/to/verilator-4.110
- (optional if already installed) $ export SPIKE_ROOT=/path/to/spike
- (only for tool installation) $ export NUM_JOBS=8 #(your mileage may vary)
- $ source cva6/regress/smoke-tests.sh
- $ source cva6/regress/dv-riscv-tests.sh