TWG Meeting Record Feb 22 2021

In Attendance

Attendee	Representing
Hugh Pollitt-Smith	CMC
Michael Wong	Codeplay
John Martin	EMC
Greg Tumbush	EMC
Jeremy Bennett	Embecosm
Florian Zaruba	ETH-Zurich
Robert Chu	Futurewei
Simon Davidmann	Imperas
Lee Moore	Imperas
Jerry Zhen	NXP
Tim Saze	Quicklogic
Arjan Bink	SiLabs
Steve Richmond	SiLabs
Oystein Knaserud	SiLabs
Oivind Ekelund	SiLabs
Halfdan Bechmann	SiLabs
Jerome Quevremont	Thales
Davide Schiavone	OpenHW
Mike Thompson	OpenHW
Rick O'Connor	OpenHW
Duncan Bees	OpenHW

Member Voting Eligibility for Feb 22 2021 meeting

General

- Meeting eligibility based on OpenHW byways. Members need a representative at 3 out of 4 previous TWG meetings as tracked in attendance record file in order to be eligible to vote

Special Arrangement for Feb 2021 TWG meeting

- **Special Note** Feb 2021 is the first meeting at which rollcall votes are held. At this meeting only, all companies attending the February meeting are given one-time voting eligibility. At subsequent meetings, the ¾ rule will apply.

Eligibility Calculation for Feb 2021 TWG Meeting (Not applied because of special arrangement noted above)

- What follows is the February meeting eligibility calculation. Although eligibility calculation is suspended for this particular meeting, it is calculated and shown below.
- Because the Dec 2020 meeting was held close to Christmas, absence will not count against eligibility, but attendance counts towards eligibility
- Eligibility is by 3 meetings out of the following 5:
    - Jan, Dec, Nov, Oct 26, Oct 5

Members Eligible for Feb Meeting	**TWG Voting Eligible Member for Feb meeting**	**Jan 2021**	**Dec 2020**	**Nov 2020**	**Oct 26 2020**	**Oct 5 2020**
	Codeplay	Y	Y	Y		
	Embecosm	Y	Y	Y	Y	Y
	EM Micro	Y		Y	Y	Y
	Futurewei	Y	Y	Y	Y	
	Imperas	Y	Y	Y	Y	Y
	NXP	Y	Y	Y	Y	Y
	Quicklogic	Y			Y	Y
	THALES	Y		Y	Y	
Members Ineligible for Feb Meeting						
	Axiomise			Y		
	UniBo				Y	Y
	CMC			Y		Y
	Datum			Y		

	ETH Zurich			Y		
	PolyTechnique MTL			Y		
	SiLabs				Y	Y
	Symbiotic					Y

TG reports highlighting changes to plan of record, critical issues on projects

- Cores – Arjan or Davide
  - CVA6 is ongoing

- HW – Hugh or Tim

https://github.com/openhwgroup/core-v-docs/blob/master/program/TG-reports-for-TWG/20210222-hw-tg.md

  - Core-V MCU
    - Detailed task breakdown is available
    - Formal project launch planned for next month
    - It was noted that the MCU specification needs a lot of work.

- SW – Jeremy or Junhai
  - Generally, projects are under-resourced
  - FreeRTOS lacks PM

- Verification – Steve or Robert

  - Restructuring of repo for cores in flight

PPL proposal for Verilator Modelling project

Hugh Pollitt-Smith presented in Alfredo's absence

- https://github.com/openhwgroup/core-v-docs/blob/master/program/verilator-modeling-ppl.md

Noted that the "who would make use of" section needs to be filled in

Member	**Intends to participate in Verlilator Modelling Project**	**Votes to Approve PPL Gate for Verilator Modelling Project**
CMC	No	Yes

Codeplay	No	Yes
Embecosm	Yes	Yes
EM Micro	No	Yes
ETH Z	No	Yes
Futurewei	No	Yes
Imperas	No	Abstain
NXP	No	Yes
Quicklogic	Yes	Yes
SiLabs	No	Yes
Thales	No	Yes
UniBo	No	Yes

11 votes to approve PPL for Verilator Modelling Project

1 abstain

None against

Motion carried, status is at PPL

Combined PPL/PL for both CV32E40S and CV32E40X

Presented by Arjan Bink

- https://github.com/openhwgroup/core-v-docs/blob/master/program/CV32E40S-PPL.md

CV32E40S
Highlights

- Agile approach - starting from stable base
- Will share backlog with active contributors
- Risks - several standards uncertainties
- S Higher priority than X - aimed in 2021

- https://github.com/openhwgroup/core-v-docs/blob/master/program/CV32E40X-PPL.md

CV32E40X
Highlights

- Substantial shared features with 40S
- One output is description of how to add new instruction

- Embecosm will be involved with tool chain component as this does imply tool chain requirements
- X interface: working with ETH Zurich and LowRisc team to get that defined
- Verification: same way of working with interface towards ISS more robust
- Should add Imperas as committed participants
- Current plan on X interface is to add ALU type instructions. These instructions will have access to the register flow. Also, enable FP extensions via the X interface. Stay in alignment with ETH Z
- Will attempt to lower the interrupt latency on long instructions
- The main goal is to add custom extensions without open sourcing them or invoking a long process.
- Simon: Zce spec is not likely to be ratified this year. Jeremy: divided into 2 phases, compressed push and pop and then table jump.

Member	**Intends to participate in CV32E40S**	**Votes to Approve PPL/PL Gates for CV32E40S**	**Intends to participate in CV32E40X**	**Votes to Approve PPL/PL Gates for CV32E40X**
CMC	No	Yes	No	Yes
Codeplay	No	Yes	No	Yes
Embecosm	No	Yes	Yes	Yes
EM Micro	Maybe	Yes	Maybe	Yes
ETH Z	No	Yes	Yes	Yes
Futurewei	Maybe	Yes	Maybe	Yes
Imperas	Yes	Yes	Yes	Yes
NXP	No	Yes	No	Yes
Quicklogic	No	Yes	No	Yes
SiLabs	Yes	Yes	Yes	Yes
Thales	No	Yes	No	Yes
UniBo	Maybe	Yes	Yes	Yes

12 votes to approve PL Gate for CV32E40S project

0 abstain

0 against

12 votes to approve PL Gate for CV32E40X project

0 abstain

0 against

Motions carried, status of CV32E40S and CV32E40X are both at PL