CV32E40P* Verification Schedule Proposal

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Purpose of this Presentation

- This presentation is intended to be a high-level overview of a Project Plan (schedule) to verify the CV32E40P*
  - The "*" is important – see next slide.

- Goals of the Project Plan:
  - "Industrial Grade" functional sign-off of the RTL.
  - Interim milestones to maintain focus.
  - RTL Freeze by 2020-09-25.
  - Maximum of 4 Full-Time-Equivalent engineers.

CV32E40P*

- The “Device Under Test” for this Project is the OpenHW CV32E40P CORE-V core.
  - Original proposed in CV32E40_Features_Parameters.pdf
  - RTL hosted in GitHub at https://github.com/openhwgroup/cv32e40p

- In order to achieve a high-confidence Project Plan, the verification of specific CV32E40P features are deferred:
  - Xpulp ISA
  - Floating point ← What are we doing with this?

- Preexisting RTL for these Features can remain in place:
  - It is probable that some level of verification of these Features will be covered by RTL Freeze.
  - Verification could continue after RTL Freeze to achieve a complete CV32E40P version of the core.

“Industrial Grade” Sign-off

- All “features to be verified” captured in detailed Verification Plan(s):
  - Capture of CV32E40P Vplans is ~60% complete
  - Requires reviews by both Design and Verification

- Features identified in the Verification Plans used to define Functional Coverage model:
  - Measurement of feature coverage is coded directly into verification environment
  - Regressions will automatically publish coverage results

- RTL Freeze is achieved when:
  - All Features of Vplan represented in functional coverage.
  - 100% Functional coverage.
  - 100% Code coverage (block, FSM, conditional).
  - No failing tests in regression.

Deviation from this will require waivers.

Milestones

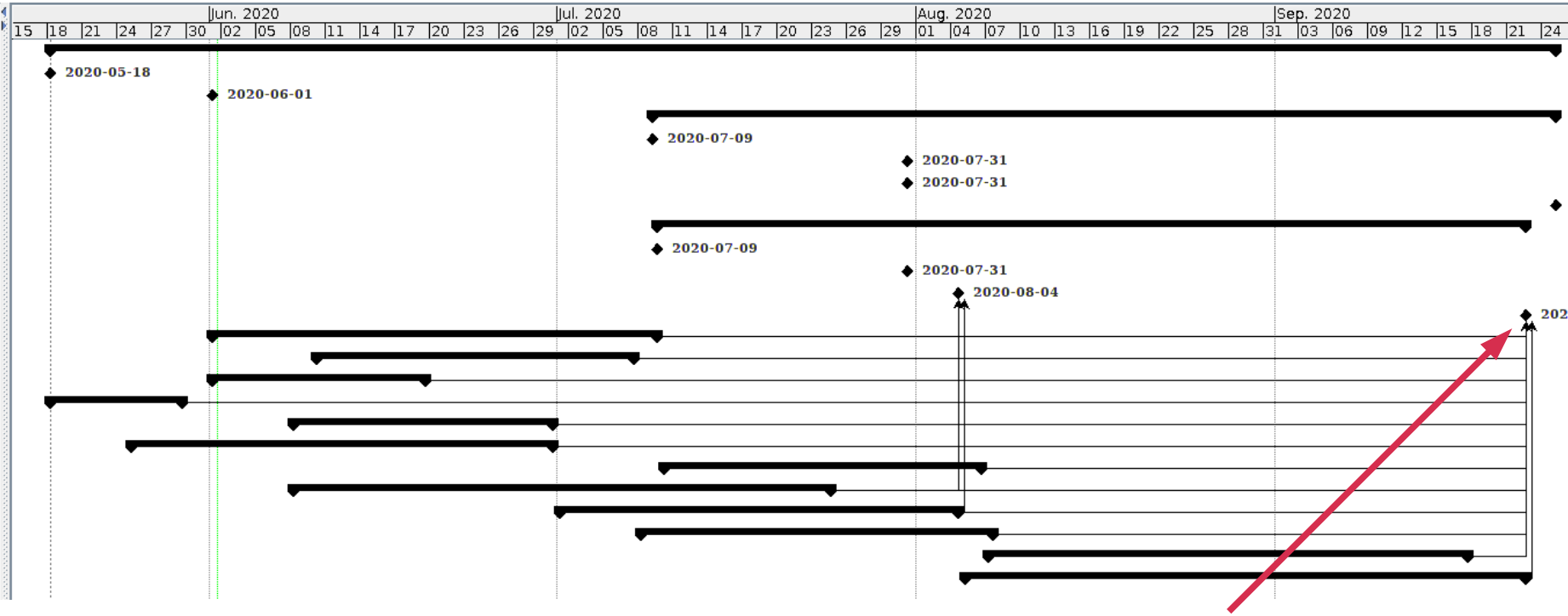
- Plan Execution Start:
  - Plan signed off and resourced.
  - Currently set to June 1!
- Documentation Complete:
  - Designer capture of user manual.
  - Verifier capture of Vplans.
  - Joint reviews.
- RTL Coding Complete:
  - Only fixes for functional bugs and synthesis issues after this point.
- RV32 ISA Compliance Verified:
  - Verification of all features except Exceptions, Debug.
- RTL Freeze:
  - Done is done.

Resourcing

- Project Plans assumes the following:
  - Davide Schiavone (OpenHW) and a support team can start doc'n work now.
  - Paul Zavalney (SiLabs) is *not* available for verification tasks in early June.
  - One FTE software engineer stating now for 3 weeks.
  - Sebastien Jacq (Thales TRT) available in June for Compliance work.
  - Jean Roch Coulon (Thales INVIA) available next week to help with Google ISG (~ 1wk).
  - Greg Tumbush and Wajid Minhass (SiLabs) participate at FTE level for entire project.
  - Mike Thompson (OpenHW) participates at FTE level in June and then again in August and September.
  - Two additional un-named FTE verifiers.

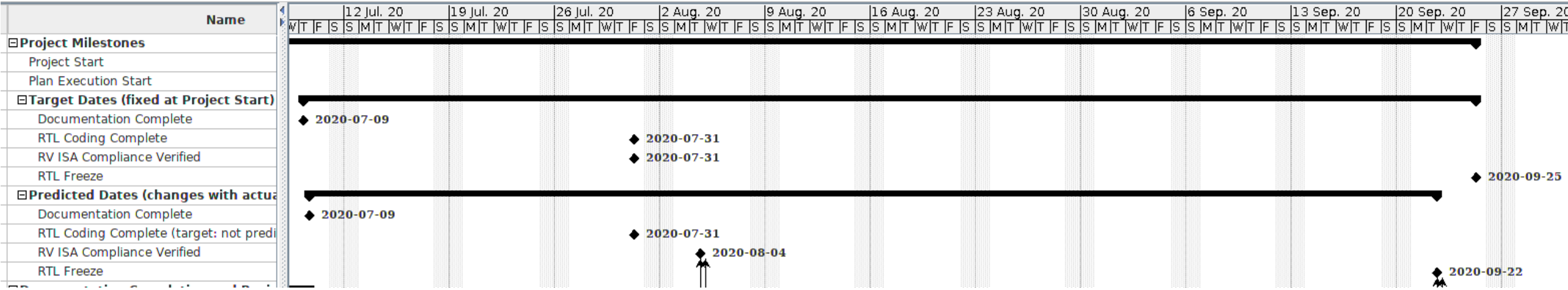
Gantt Chart View

		Name
1		⊟**Project Milestones**
2		Project Start
3		Plan Execution Start
4		⊟**Target Dates (fixed at Project Start)**
5		Documentation Complete
6		RTL Coding Complete
7		RV ISA Compliance Verified
8		RTL Freeze
9		⊟**Predicted Dates (changes with actual task durations)**
10		Documentation Complete
11		RTL Coding Complete (target: not predicted by this schedule)
12		RV ISA Compliance Verified
13		RTL Freeze
14		⊞**Documentation Completion and Review**
34		⊞**CV32E40P RTL + CV32 UVM Verification Environment Integrati**
41		⊞**Tool-chain and Programming Environment**
47		⊞**ISS Integration and Updates**
51		⊞**Random Instruction Generator (riscv-dv) Integration and Upd**
56		⊞**RISC-V ISA Compliance (Simulation)**
62		⊞**RVI Compliance**
67		⊞**Interrupt Verification**
74		⊞**Implement and execute access tests for all CSRs**
80		⊞**Exception Verification**
84		⊞**Debug Verification**
91		⊞**Coverage Signoff**



Predicted date for RTL Freeze is 2020-09-24

Milestones



Milestone	Target Date	Predicted Date
Execution Start	2020-06-01	TBD
Documentation Complete	2020-07-09	2020-07-09
RTL Coding Complete	2020-07-31	2020-07-31 (note: not predicted)
RV ISA Compliance	2020-07-31	2020-08-04
RTL Freeze	2020-09-25	2020-09-22

Risks

- Staffing is by far the #1 risk to the Project.

- Few of the tasks in the schedule have well thought out effort estimates.

- OVPsim Instruction Set Simulator:
  - Imperas support for RISC-V Compliance issues is expected to be very good.
  - Support for non-Compliance features (if any) is unknown:
    - OpenHW is not a paying customer.
  - On-the-fly “Step-and-Compare” of CSRs, GPRs and PC is cycle-timing sensitive.

- Google Random Instruction Set Generator:
  - No known RISC-V projects have attempted to use it to close coverage of full a full ISA implementation.

- DSIM code coverage feature is very new:
  - CV32E40P is a beta user.
  - Only block (line) coverage is currently available.

Thank You