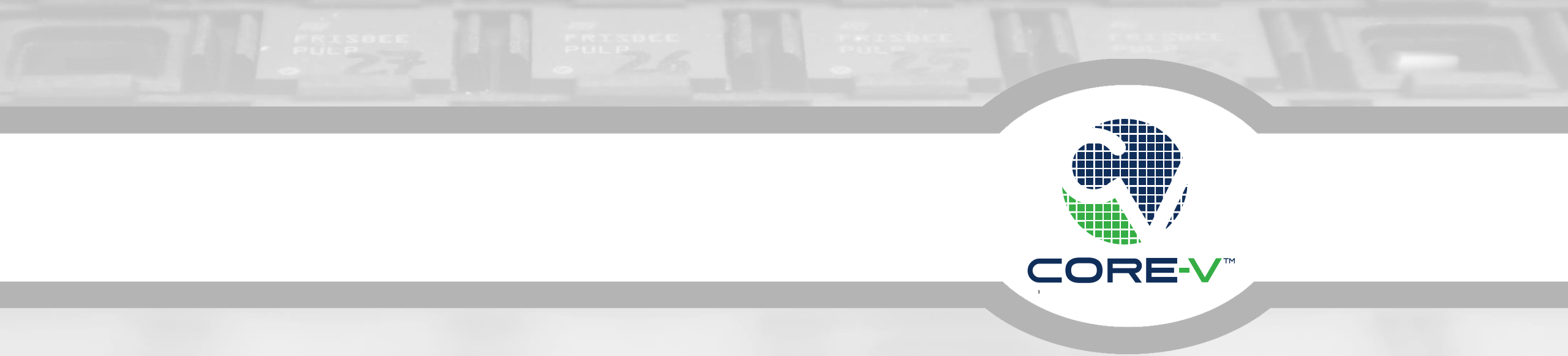


CORES TG – May 3 2021

Arjan Bink

Jérôme Quevremont

Davide Schiavone

Agenda

- CV32E40P status
- CV32E40X status
- CVA6 status
- CV32E20

CV32E40P status

Davide Schiavone

Updates on CV32E40P

- CV-X-IF RTL activities on RV32F ISA extensions
  - APU pins and logic removed and LEC script passing
  - Scoreboard and CV-X-IF implementation started

- Verible Formatter
  - Whitespaces, indentation, line breakers managed in accordance to a given a style allowing for nicer and consistent SystemVerilog style

original:

```
module m #(
  int  W,
  some_long_name T
);
  ...
endmodule
```

aligned:

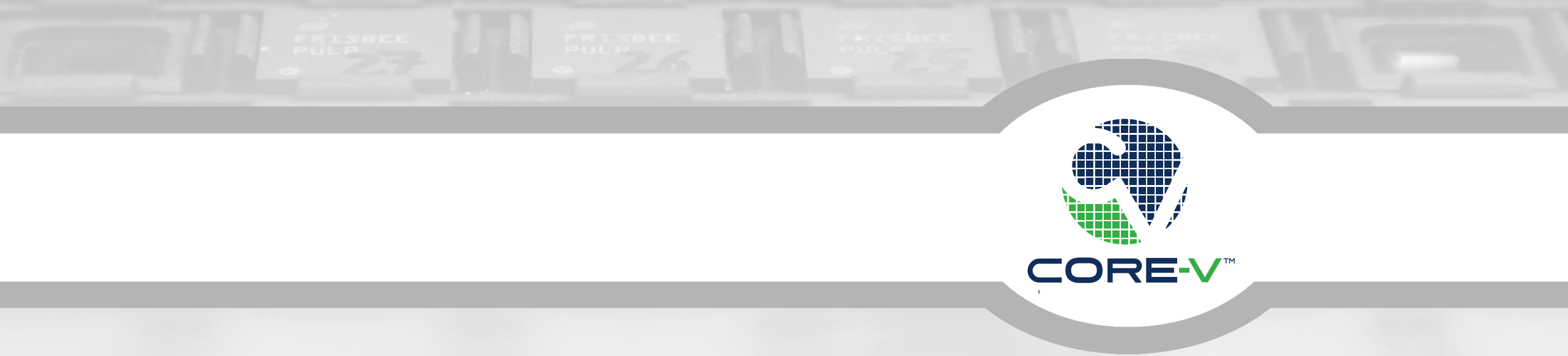
```
module m #(
  int            W,
  some_long_name T
);
  ...
endmodule
```

Miscellaneous Updates

- Joint paper OpenHW Group + lowRISC + ETH on the making
  - Comparing (PPA) the CV32E40P updates against Ibex on Embench and Coremark

- CV-X-IF mattermost channel activated
  - https://mattermost.openhwgroup.org/all-users/channels/twgcorescvxif
  - Imagination Technology (Trefor Southwell) as Project Manager
  - Now time to organize meetings and push the spec forwards

- ETH published a new low-area RISC-V FPU IP
  - A trade-off between performant FPU and SW emulation

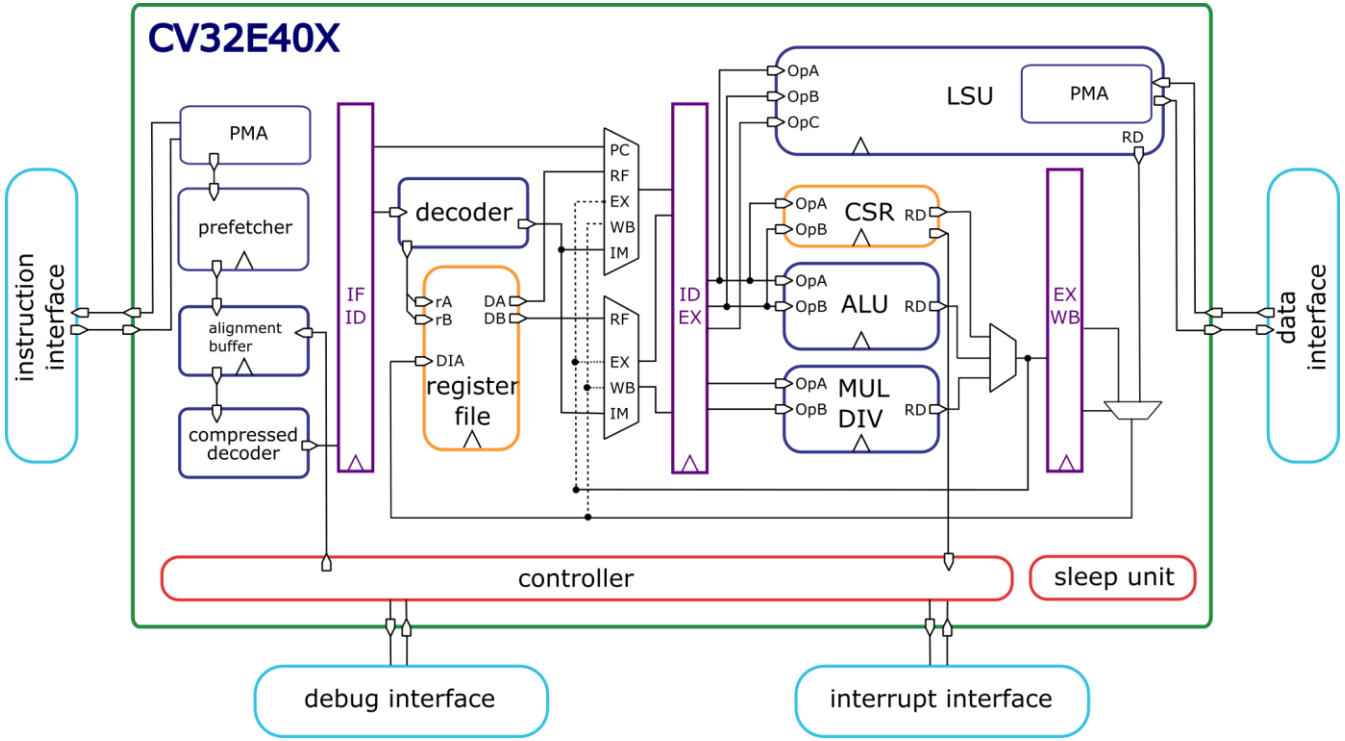


CV32E40X status

Øystein Knauserud

CV32E40X p.1 (overlaps CV32E40S p.1)

- Added PMA and bus error to LSU (excl. controller updates)
- Received *marchid* value
- RVFI addition well underway
- Moved controller, register file and interrupt controller out of ID stage and into top level
- Started implementation of WB centric controller
  - IRQs, exceptions, debug all handled in WB stage
  - Hello-world is passing with new controller
- User manual updates



CVA6 status

Jérôme Quévremont

CVA6

- Gates
  - PC (former PPL) passed
  - PL passed
  - PA (former PPA) to come: specification and detailed plan
- Next project meetings
  - Also spans on verification, SW topics…
  - May 7th: progress meeting
  - May 14th: cancelled (FR holiday)
  - May 25th: progress meeting (moved from May 21st)
  - May 28th: “save the date ” technical meeting
  - June 4th: progress meeting
  - https://calendar.google.com/calendar/u/0/embed?src=meetings@openhwgroup.org
- TWG : Cores : CVA6 Mattermost channel
  - Also spans on verification, SW topics…

CVA6: current activity

- Specification on going
  - https://docs.google.com/document/d/11rsoO5WKraMCraSpnsVqmt4hJaCcDG0zq7LTWdXVkf0
  - Target planning
    - May 7th: complete draft (all sections contributed, not perfect)
    - May 28th: updated draft, ready for review
    - June 25th (latest): approved at CVA6 project meeting
    - June 28th: get TWG approval (part of PA gate)
  - Major open topics: RV32D support (in CV32A6), coprocessor interface
- Verification: consensus on the DV environment breakdown ☺
  - Core testbench: self-checking tests
  - Core-v-verif UVM step and compare bench (includes core testbench)
  - APU (platform-level)
- SW: on-going FreeRTOS and 32b Linux ports
- Reorganizing CVA6 folder to clearly separate core and APU

CV32E20

Peter Militello of Intrinsix Corp, Joe Circello of NXP

Assessing Interest in CV32E2 Project

- NXP has taped out multiple designs using the ETH-Zurich PULPino ZeroRISCY core
- Intrinsix also currently uses 2-stage ZeroRISCY core originally developed as part of the PULP platform
- NXP and Intrinsix both have interest in a 2-stage RISC-V core with these features:
  - RV32IMC with RV32E option
  - Small gate count and low power
  - Debug port supporting ratified functionality
  - User mode (minimal implementation)
  - Qualified using industry-strength verification techniques
- Additional features would include:
  - OBI bus approach as per CV32E40{P}
  - AHB interface bridges
  - Vectored interrupts
  - Support for 2-pin CJTAG debug interface

INTRINSIX NXP

CV32E2 Initial Resourcing

- Use Ibex as starting point for CV32E20 project
- NXP contributes architectural resources
- Intrinsix contributes verification resources