Lab 1 Yuancheng Elijah Tan, Sadik Mohammad Farhan

Combinational logic:

myip module consists of a mealy machine with four different states:

1. Idle: Default state, waits for S_AXIS_TVALID == 1 to change to read input state
2. Read_Inputs : Reads S_AXIS_TDATA and writes it to A and B ram, changes to compute state when all data is received
3. Compute: Sets Start=1 to indicate to the multiply module to begin computing, changes to write outputs when the multiply module is done
4. Write_Outputs : Reads the multiplication result from RES ram and writes it to M_AXIS_TDATA, changes to idle once all data is written

Matrix_multiply module is moore machine with 5 different states

1. Idle: Waits for the start signal to change to read inputs state
2. Read_Inputs: Enables and sets the read address for A and B ram and changes to compute state
3. Compute: Takes the read out from A and B ram and computes the product of the data. If the end of the column is reached, state changes to write output, otherwise state changes to read inputs
4. Write_Outputs: Writes the accumulator to RES ram and resets it. State changes to done if it is at the last row, otherwise state changes to read input
5. DONE: Sets Done =1 to indicate to myip that the multiplication is complete, state changes to idle

Sequential: All counters and the accumulator are incremented only at the pos clock edge.

Resource Usage:

Report Cell Usage:

	Cell	Count
1	BUFG	1
2	CARRY8	8
3	LUT1	5
4	LUT2	40
5	LUT3	46
6	LUT4	32
7	LUT5	16
8	LUT6	43
9	RAM16X1S	24
10	FDRE	60
11	FDSE	1
12	IBUF	12
13	OBUF	35

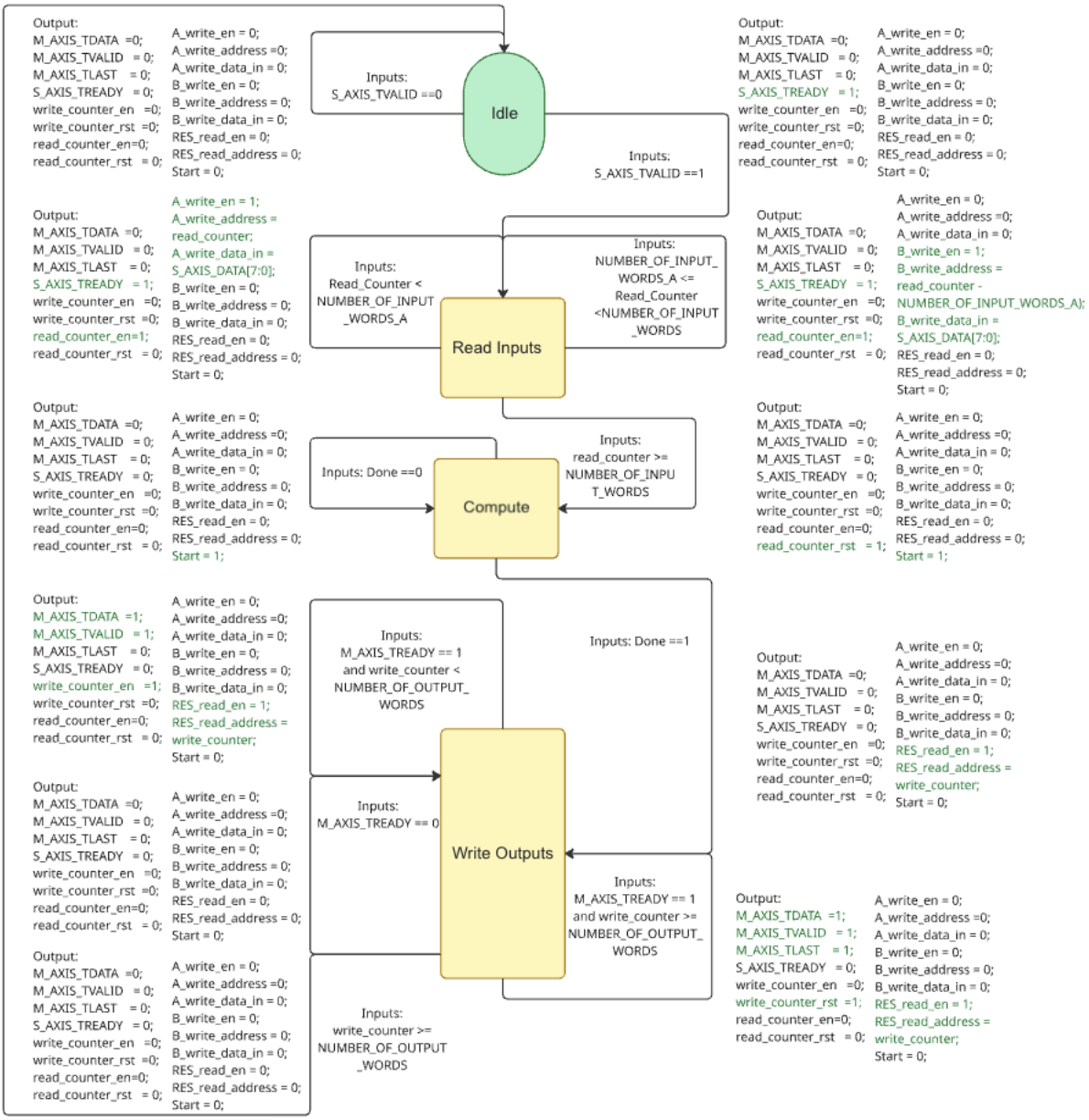
Report Instance Areas:

	Instance	Module	Cells
1	top		323
2	A_RAM	memory_RAM	51
3	B_RAM	memory_RAM__parameterized0	78
4	RES_RAM	memory_RAM__parameterized1	24
5	matrix_multiply_0	matrix_multiply	100

Expected Number of Cycles: 36 for A=2x4 matrix (1+12+2*10+1+2)

Read Inputs: 1+number of input words, Compute: 2*(elements in A +A_ROWS)+1, Write Outputs: Number of output words

myip State Diagram



Matrix Multiplier State Diagram