# UH2C/D Main Evaluation Board - 80 Ball BGA

| PAGE # | TITLE DESCRIPTION |
|---|---|
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| 2 | UH2C/D - MAIN |
| 3 | HDMI SECTION |
| 4 | MIPI SECTION |
| 5 | AUDIO I2S, IR |
| 6 | CONTROL<br>(I2C/ CLOCK/ RESET/ TEST ) |
| 7 | POWER SECTION |
| 8 | CHANGES/BLOCK DIAGRAM |

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|---|---|---|
| Title: UH2C - COVER PAGE | | |
| Size: B | Document Number: UH2C_80B_MAIN | Rev: J2.4 |
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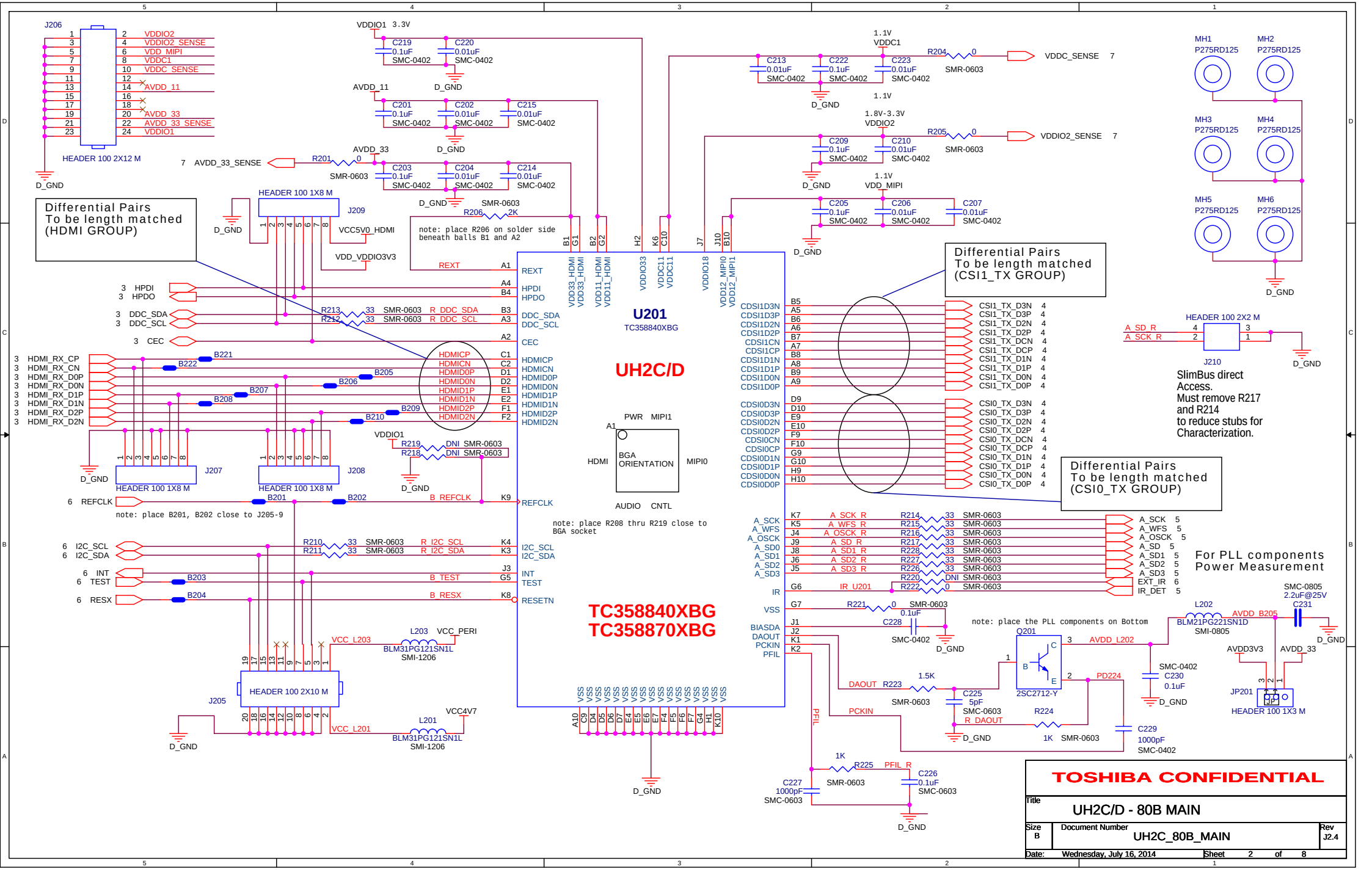
J206
HEADER 100 2X12 M
VDDIO2
VDDIO2_SENSE
VDD_MIPI
VDDC1
VDDC_SENSE
AVDD_11
AVDD_11_SENSE
AVDD_33
AVDD_33_SENSE
VDDIO1
D_GND
VDDIO1 3.3V
C219 0.1uF SMC-0402
C220 0.01uF SMC-0402
AVDD_11
C201 0.1uF SMC-0402
C202 0.01uF SMC-0402
C215 0.01uF SMC-0402
AVDD_33
R201 0 SMR-0603
C203 0.1uF SMC-0402
C204 0.01uF SMC-0402
C214 0.01uF SMC-0402
1.1V
VDDC1
C213 0.01uF SMC-0402
C222 0.1uF SMC-0402
C223 0.01uF SMC-0402
R204 0 SMR-0603
VDDC_SENSE 7
1.8V-3.3V
VDDIO2
C209 0.1uF SMC-0402
C210 0.01uF SMC-0402
R205 0 SMR-0603
VDDIO2_SENSE 7
1.1V
VDD_MIPI
C205 0.1uF SMC-0402
C206 0.01uF SMC-0402
C207 0.01uF SMC-0402
MH1 P275RD125
MH2 P275RD125
MH3 P275RD125
MH4 P275RD125
MH5 P275RD125
MH6 P275RD125
Differential Pairs
To be length matched
(HDMI GROUP)
HEADER 100 1X8 M
J209
VCC5V0_HDMI
VDD_VDDIO3V3
R206 2K SMR-0603
note: place R206 on solder side
beneath balls B1 and A2
REXT
HPDI
HPDO
DDC_SDA
DDC_SCL
CEC
R213 33 SMR-0603 R_DDC_SDA
R212 33 SMR-0603 R_DDC_SCL
U201
TC358840XBG
UH2C/D
HDMICP
HDMICN
HDMID0P
HDMID0N
HDMID1P
HDMID1N
HDMID2P
HDMID2N
PWR MIPI1
HDMI
BGA ORIENTATION
MIPI0
AUDIO CNTL
HDMI_RX_CP
HDMI_RX_CN
HDMI_RX_D0P
HDMI_RX_D0N
HDMI_RX_D1P
HDMI_RX_D1N
HDMI_RX_D2P
HDMI_RX_D2N
B221
B222
B205
B206
B207
B208
B209
B210
J207
J208
HEADER 100 1X8 M
R219 DNI SMR-0603
R218 DNI SMR-0603
REFCLK
B_REFCLK
B201
B202
note: place B201, B202 close to J205-9
I2C_SCL
I2C_SDA
R210 33 SMR-0603 R_I2C_SCL
R211 33 SMR-0603 R_I2C_SDA
INT
TEST
RESETN
B_TEST
B_RESX
B203
B204
note: place R208 thru R219 close to
BGA socket
TC358840XBG
TC358870XBG
L203 VCC_PERI
BLM31PG121SN1L
SMI-1206
VCC_L203
J205
HEADER 100 2X10 M
VCC4V7
L201
VCC_L201
Differential Pairs
To be length matched
(CSI1_TX GROUP)
CSI1_TX_D3N
CSI1_TX_D3P
CSI1_TX_D2N
CSI1_TX_D2P
CSI1_TX_DCN
CSI1_TX_DCP
CSI1_TX_D1N
CSI1_TX_D1P
CSI1_TX_D0N
CSI1_TX_D0P
Differential Pairs
To be length matched
(CSI0_TX GROUP)
CSI0_TX_D3N
CSI0_TX_D3P
CSI0_TX_D2N
CSI0_TX_D2P
CSI0_TX_DCN
CSI0_TX_DCP
CSI0_TX_D1N
CSI0_TX_D1P
CSI0_TX_D0N
CSI0_TX_D0P
HEADER 100 2X2 M
A_SD_R
A_SCK_R
J210
SlimBus direct
Access.
Must remove R217
and R214
to reduce stubs for
Characterization.
A_SCK
A_WFS
A_OSCK
A_SD
A_SD1
A_SD2
A_SD3
EXT_IR
IR_DET
R214 33 SMR-0603
R215 33 SMR-0603
R216 33 SMR-0603
R217 33 SMR-0603
R228 33 SMR-0603
R227 33 SMR-0603
R226 33 SMR-0603
R220 DNI SMR-0603
R222 0 SMR-0603
IR
IR_U201
VSS
BIASDA
DAOUT
PCKIN
PFIL
R221 0 SMR-0603
C228 0.1uF SMC-0402
For PLL components
Power Measurement
note: place the PLL components on Bottom
Q201
2SC2712-Y
DAOUT R223 1.5K SMR-0603
C225 5pF SMC-0603
R_DAOUT
R224 1K SMR-0603
PD224
AVDD_L202
C229 1000pF SMC-0402
C230 0.1uF SMC-0402
L202 BLM21PG221SN1D SMI-0805
AVDD_B205
C231 2.2uF@25V SMC-0805
AVDD3V3
AVDD_33
JP201
HEADER 100 1X3 M
R225 1K SMR-0603
PFIL_R
C227 1000pF SMC-0603
C226 0.1uF SMC-0603
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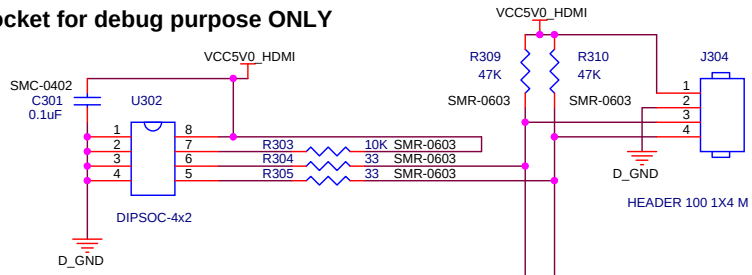
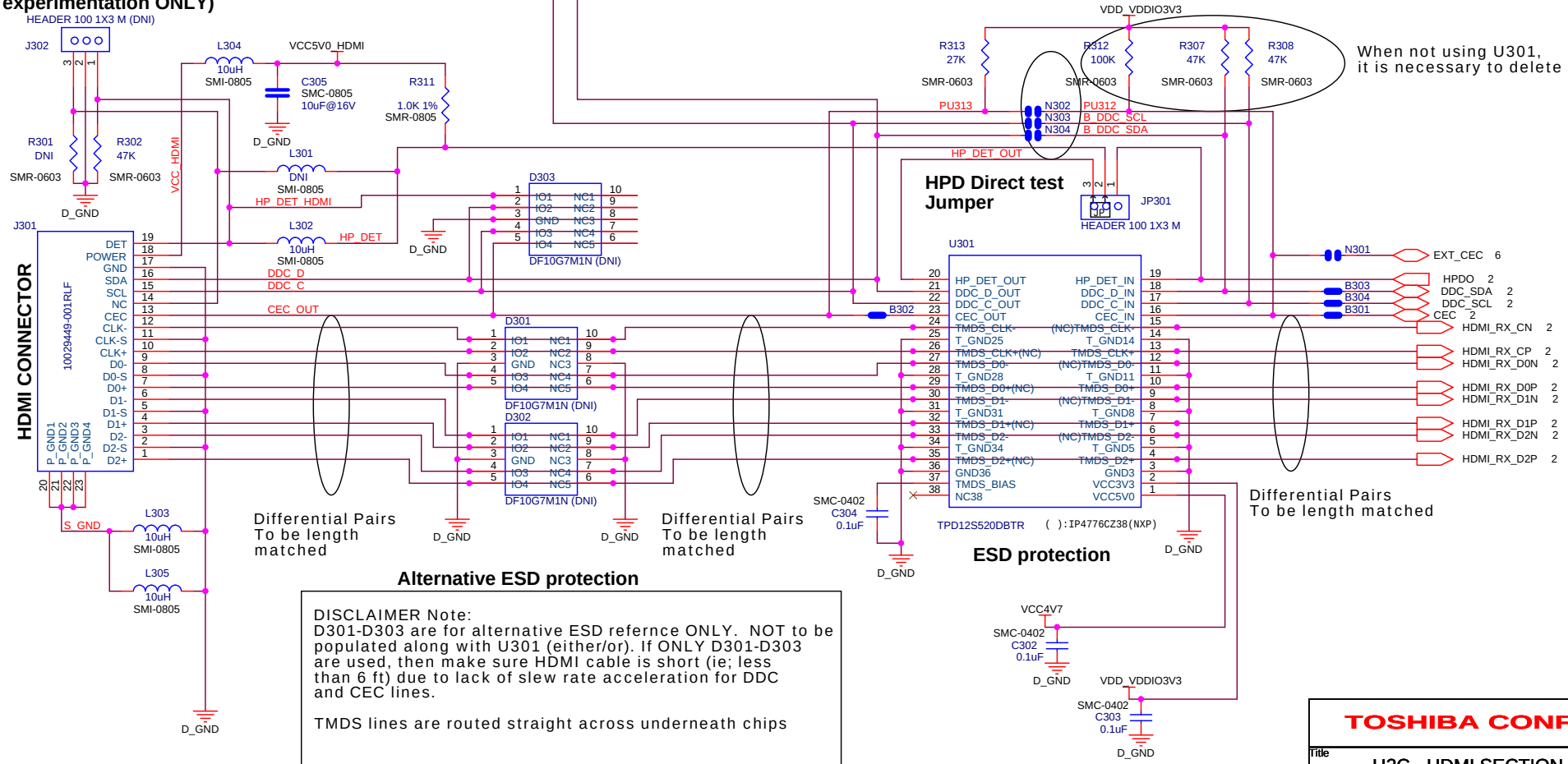
## EDID Socket for debug purpose ONLY



## eHDMI Tap (for experimentation ONLY)

these need to be BRIDGED if U301 is not populated

When not using U301, it is necessary to delete this resistance.




## Alternative ESD protection

DISCLAIMER Note:
D301-D303 are for alternative ESD refernce ONLY. NOT to be populated along with U301 (either/or). If ONLY D301-D303 are used, then make sure HDMI cable is short (ie; less than 6 ft) due to lack of slew rate acceleration for DDC and CEC lines.

TMDS lines are routed straight across underneath chips

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| | | |
|---|---|---|
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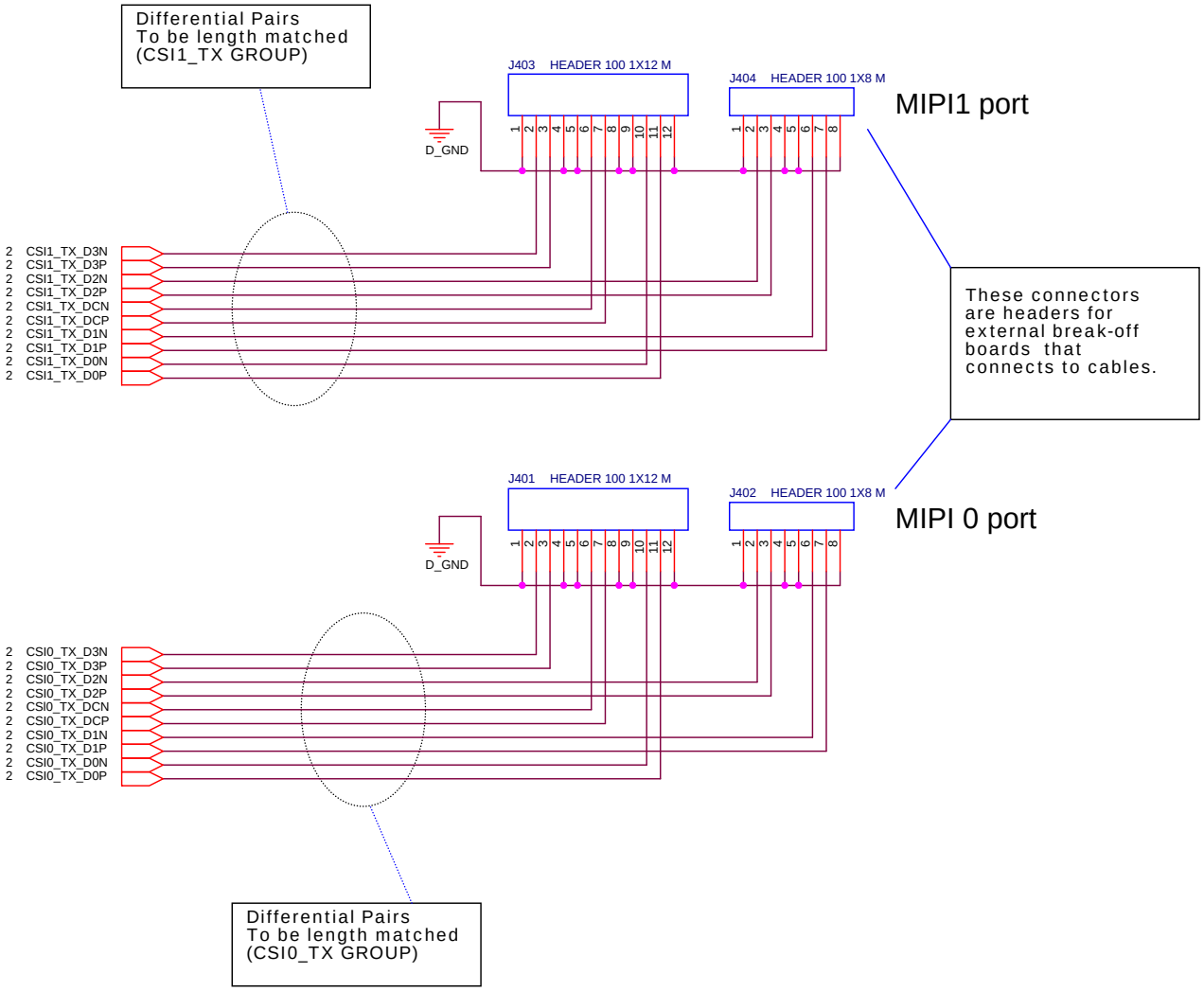
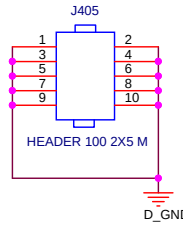
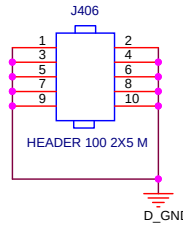
# MIPI Output Ports




## Grounding Headers




D_GND header




MIPI Ground header

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| | | |
|---|---|---|
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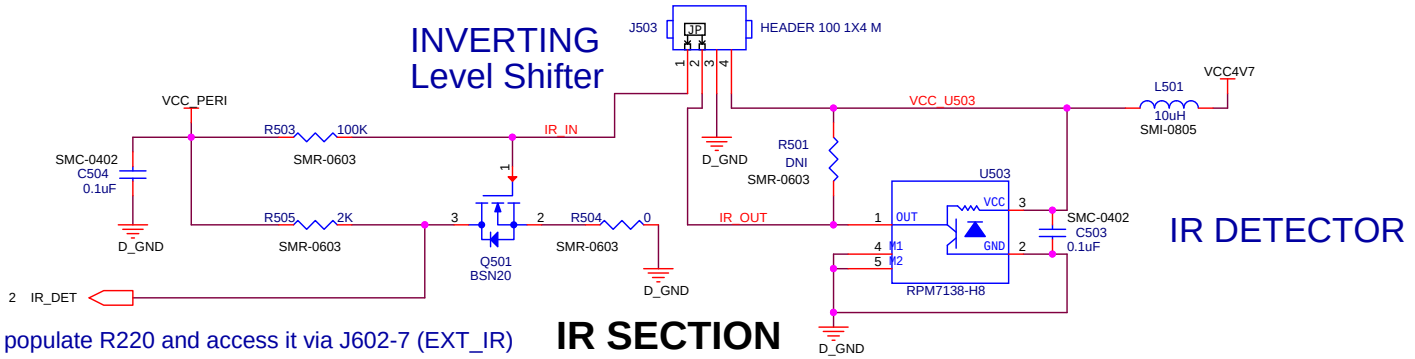
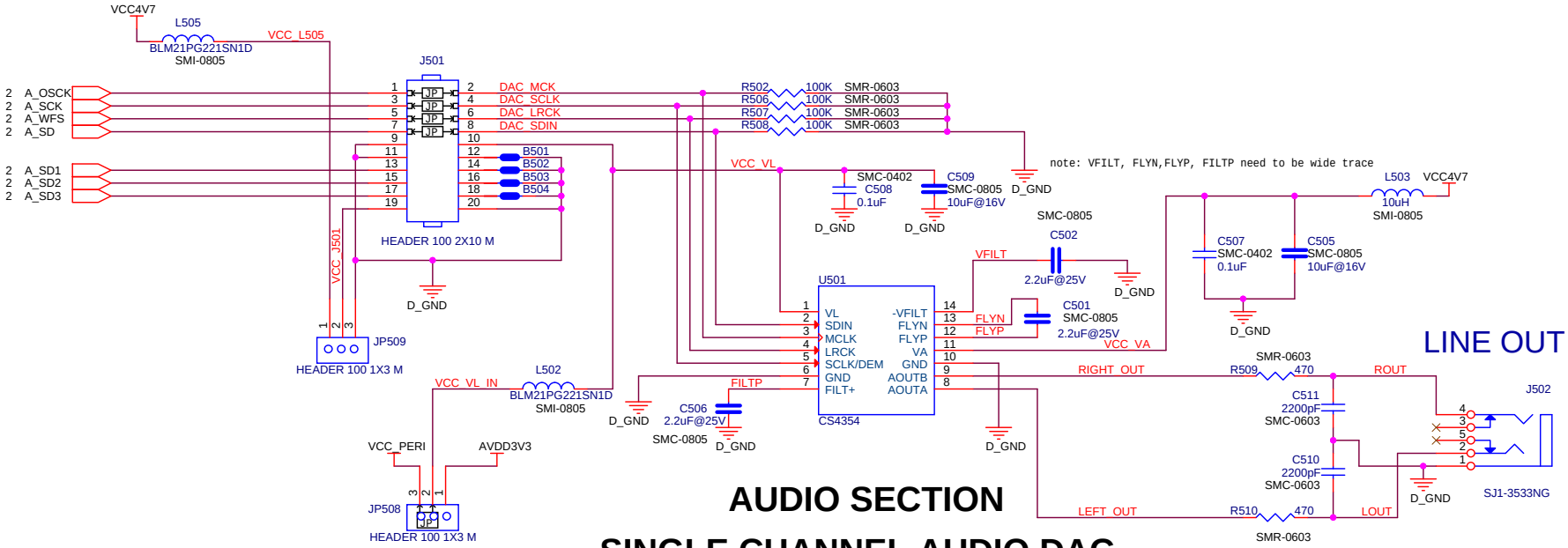
## IR Debug Header




To access IR ball (J6) directly, populate R220 and access it via J602-7 (EXT_IR)

**IR SECTION**

## PCM HEADER/JUMPER I2S




LINE OUT

# AUDIO SECTION

# SINGLE CHANNEL AUDIO DAC

(STEREO PCM ONLY)

Needs Gound necking near U501

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| | | |
|---|---|---|
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Note: New Reset device used, SOT23-5 Footprint, 1.4V threshold

## Power on Reset source

ON BOARD POR

U605 TPS3125G15DBVR (RSTn, GND2, RST, VDD, MR)

VCC_PERI, R623 SMR-0603 DNI, B619, C602 0.1uF SMC-0402, TP617 DNI, PTS635SL50 SW601, D_GND

RESX Status Indicator

2 RESX — R619 10K SMR-0603 — Q605 RN1110MFV (4.7K) — D605 APT2012CGCK GREEN — R642 470 SMR-0603 — VCC4V7, D_GND

ON_BRD_RESX — JP610 HEADER 100 1X3 M (RESX, EXT_RSTN)

Place Near Reset area

Extra Grounding Posts

TP607 5021, TP608 5021, TP609 5021, D_GND

## Clock Sources: Multiple Footprints

J601 5-1814832-1, R613 0 SMR-0603, R614 51 SMR-0603, MANUAL_CLK, SMA_REFCLK, D_GND

B601 — U601 OE, VCC, GND, OUT — 48 MHz (SMD) SG-210STF 48.0000MS3 — N601 — R609 33 SMR-0603 — R610 DNI SMR-0603 — C609 0.1uF SMC-0402, C608 0.01uF SMC-0402

B602 — U602 OE, VDD, GND, OUT — OSC-4PIN — N602 — R611 33 SMR-0603 — R612 DNI SMR-0603 — C611 0.1uF SMC-0402, C610 0.01uF SMC-0402

U601_CLK, U602_CLK → JP605 HEADER 100 2X5 M → REFCLK 2

EXT_CLK — N603 — CLK_EXT

Extra Grounding Posts

TP610 5021, TP611 5021, TP612 5021, D_GND

Note: New oscillator frequency from H2C and H2C+

## GPIO LED and Switches

Switch Enables JP614-JP619

SW602 EG1218 "1"/"0" — U607 MM74HC132MTC — SW603 EG1218 "1"/"0"

GPIOA — Debouce Circuit — GPIOB

TP613 DNI, TP614 DNI

JP614 HEADER 100 1X2 M, JP615 HEADER 100 1X2 M

R646 33K SMR-0603, R647 33K SMR-0603

U610 NC7SZ125M5X, U611 NC7SZ125M5X

TEST_GPIOA → TP601 DNI, TEST_GPIOB → TP602 DNI

R605 4.7M SMR-0603, R606 4.7M SMR-0603

Q601 EM6K6 (D1 G2 S2, S1 G1 D2)

GPIOA: D601 APT2012CGCK GREEN, R601 150 SMR-0603, VCC4V7

GPIOB: D602 APT2012CGCK GREEN, R602 150 SMR-0603, VCC4V7

SW604 EG1218 "1"/"0" — U608 MM74HC132MTC — SW605 EG1218 "1"/"0"

GPIOX — Debouce Circuit — GPIOY

TP615 DNI, TP616 DNI

JP616 HEADER 100 1X2 M, JP617 HEADER 100 1X2 M

R648 33K SMR-0603, R649 33K SMR-0603

U612 NC7SZ125M5X, U613 NC7SZ125M5X

TEST_GPIOX → TP603 DNI, TEST_GPIOY → TP604 DNI

R607 4.7M SMR-0603, R608 4.7M SMR-0603

Q602 EM6K6 (D1 G2 S2, S1 G1 D2)

GPIOX: D603 APT2012CGCK GREEN, R603 150 SMR-0603, VCC4V7

GPIOY: D604 APT2012CGCK GREEN, R604 150 SMR-0603, VCC4V7

Extra Test GPIOs

## External I2C , GPIO, INT Headers

### I2C User Header

VCC_EXT, J604 HEADER 100 1X4 M (TI_SCL, TI_SDA), D_GND

### GPIO Matrix

JP609 HEADER 100 2X5 M

TEST_GPIOA, TEST_GPIOB, TEST_GPIOY, TEST_GPIOX

PU644, MANUAL_CLK, INT_R, EXT_GPIOA, EXT_GPIOB

R644 470 SMR-0603, R643 10K SMR-0603, INT 2

## I2C Souce and Destination Jumper Matrix

JP613 HEADER 100 1X3 M, VCC4V7, VCC_EXT

C617 0.1uF SMC-0402, C616 0.01uF SMC-0402

JP606 HEADER 100 1X2 M, VCC_U603VL

U603 MAX3373EEKA (IOVCC2, GND, VL, IOVL2, IOVCC1, VCC, TRISTATEn, IOVL1)

TI_SDA, TI_SCL, VCC_U603, TRISTATE_U603, INT_SCL, B617

R628 2K SMR-0603, R630 DNI SMR-0603, R629 2K SMR-0603

C619 0.1uF SMC-0402, C618 0.01uF SMC-0402

PU628, PU629

JP607 HEADER 100 2X5 M (I2C_SDA, EXT_SDA, U604_SDA, PU635)

JP608 HEADER 100 2X5 M (I2C_SCL, EXT_SCL, U604_SCL, PU636)

R635 2K SMR-0603, R636 2K SMR-0603

## I2C memory TEST socket

JP604 HEADER 100 2X5 M — U604 DIPSOC-4x2 — VCC_PERI

U604_A0, U604_A1, U604_A2, U604_WP → U604_WP, U604_SCL, U604_SDA

C623 0.1uF SMC-0402

R652 33K, R653 33K, R654 33K, R655 33K SMR-0603

## EXTERNAL USER CONTROL HEADER

VCC_PERI, VCC_USER, VCC4V7

L602 BLM21PG221SN1D SMI-0805 — VCC_L602 — VCC_L601 — L601 BLM21PG221SN1D SMI-0805

JP601 HEADER 100 1X3 M

J602 HEADER 100 2X10 M

2 EXT_IR, 3 EXT_CEC

EXT_CLK, EXT_RSTN, EXT_GPIOA, EXT_GPIOB, EXT_SCL, EXT_SDA, INT

## TEST_GPIO jumpers for initial test mode strapping

JP603 HEADER 100 1X3 M — TEST_GPIOX — PD615 — R617 DNI SMR-0603 — R618 DNI SMR-0603

JP602 HEADER 100 1X3 M — TEST_GPIOY — PD617 — R615 470 SMR-0603 — R616 DNI SMR-0603 — 2 TEST

RESX

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| | | |
|---|---|---|
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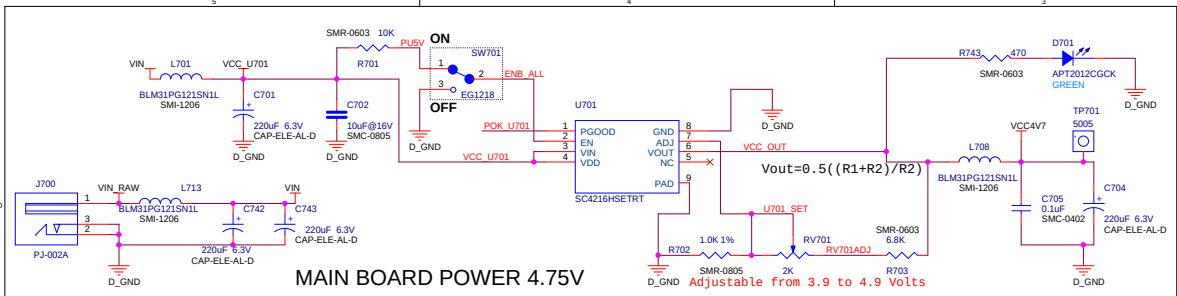
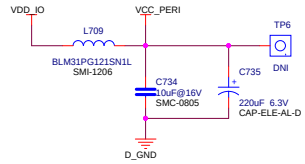
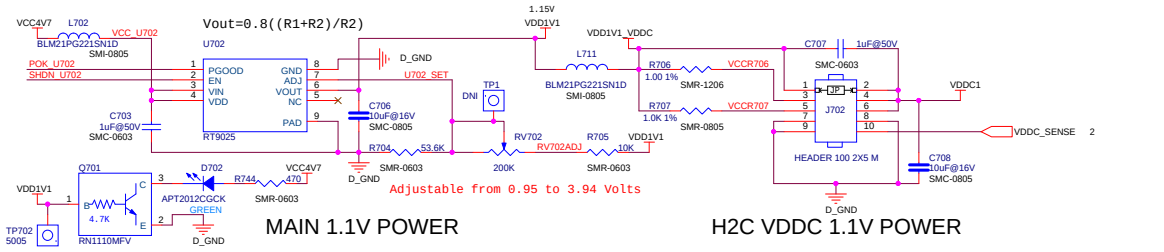
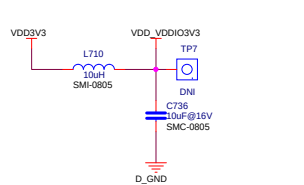


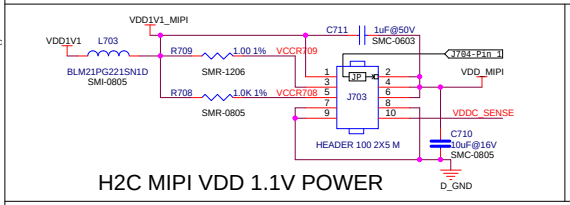




I/O Peripherial Power

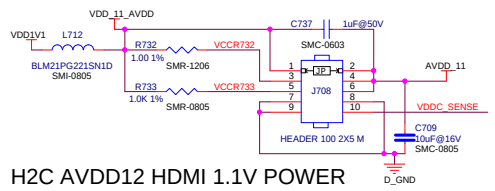


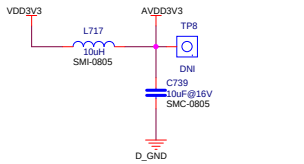

HDMI Peripherial Power




H2C MIPI VDD 1.1V POWER

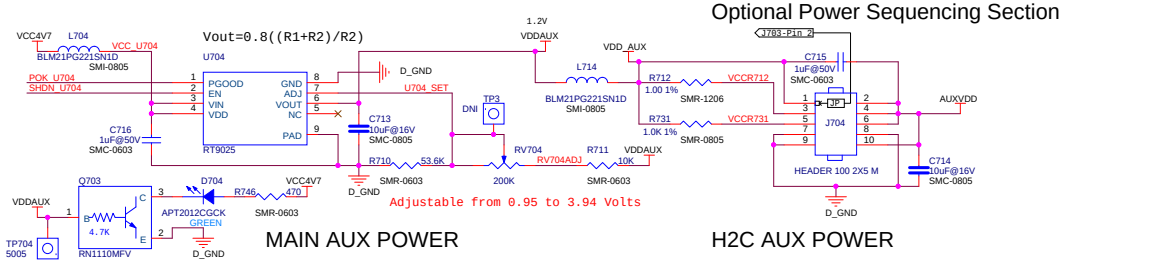


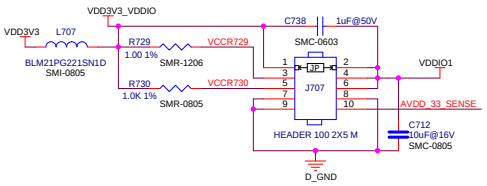

H2C AVDD12 HDMI 1.1V POWER



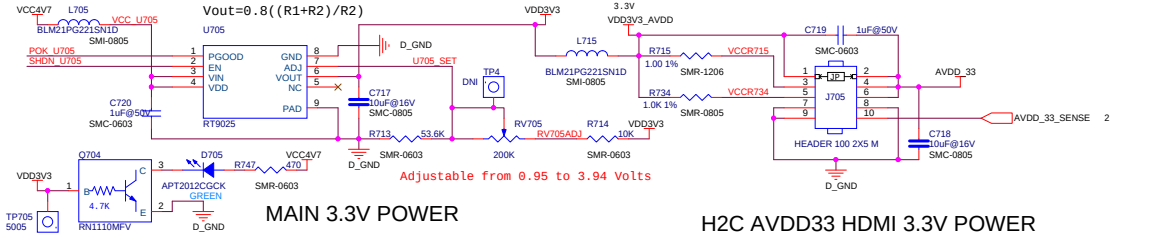

3.3V filtered source (for Audio PLL external components)

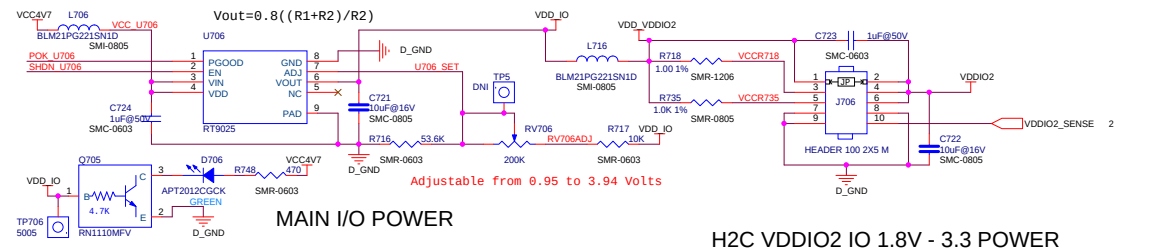
Optional Power Sequencing Section



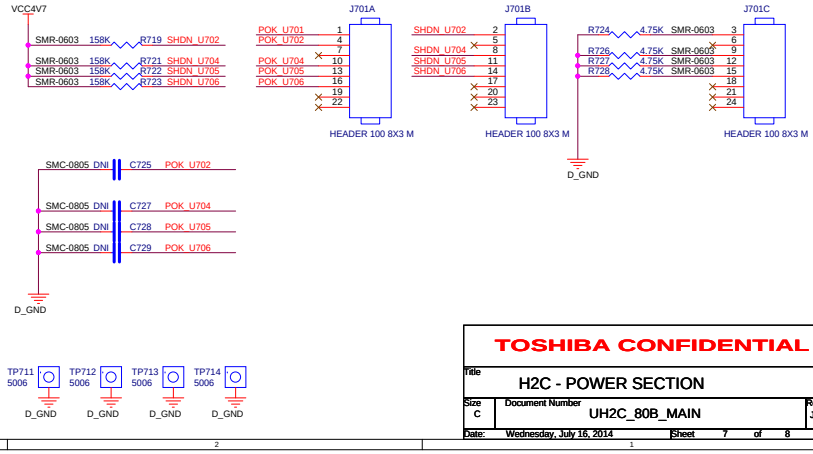




H2C VDDIO1 HDMI 3.3V POWER




Optional Power Sequencing Section

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| | | |
|---|---|---|
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| DATE | Rev# | |
|---|---|---|
| 12/06/13 | A1.0 | Schematics from H2C+ Rev C. |
| | | Changed BGA to new UH2C Ballout |
| | | Removed STBY path, AVDD_PLL, VDDC2, SPDIF |
| | | Replace Reset chip U605 with TPS3125G15DBVR, 1.4V threshold, SOT23-5 footprint |
| | | No more 2.5V, now 3.3. Added extra regulator for aux purpose |
| | | Added extra ferrite bead for HDMI shield |
| | | Added grounding headers for MIPI outputs |
| | | Changed ALL regulators to SOIC-8EDP FootPrint |
| | | Added page 8 for SCE break-out board. 5 New body parts |
| 1/17/14 | | REMOVED PAGE8, now on seperate schematics |
| 1/17/14 | | Modified J210 to 2x2 100 mil header |
| 1/19/14 | | Removed unconnected nets MMC*, N604 |
| | | Swapped A_SD_R and A_SCK_R on J210 |
| | | Changed UH2C to UH2C/D |
| | | Corrected VDD1V2 to VDD1V1 |
| 2/19/14 | A2.0 | Corrected BOM for build 2 assembly |
| 5/12/14 | J2.0 | Changed U301,R614 |
| 6/19/14 | J2.1 | Changed C226,C227,C229,R225 |
| 7/01/14 | J2.2 | Contact mark addition P2(R218),P6(R605,R607,R646,R647,R648,R649),P7(U701,TP701),Comment change P3 |
| 7/04/14 | J2.3 | Terminal name change of U201 (It is the same as the terminal name of technical data. ) |
| 7/16/14 | J2.4 | Changed R643, The initial setting addition of the short circuits-JP and SW. |
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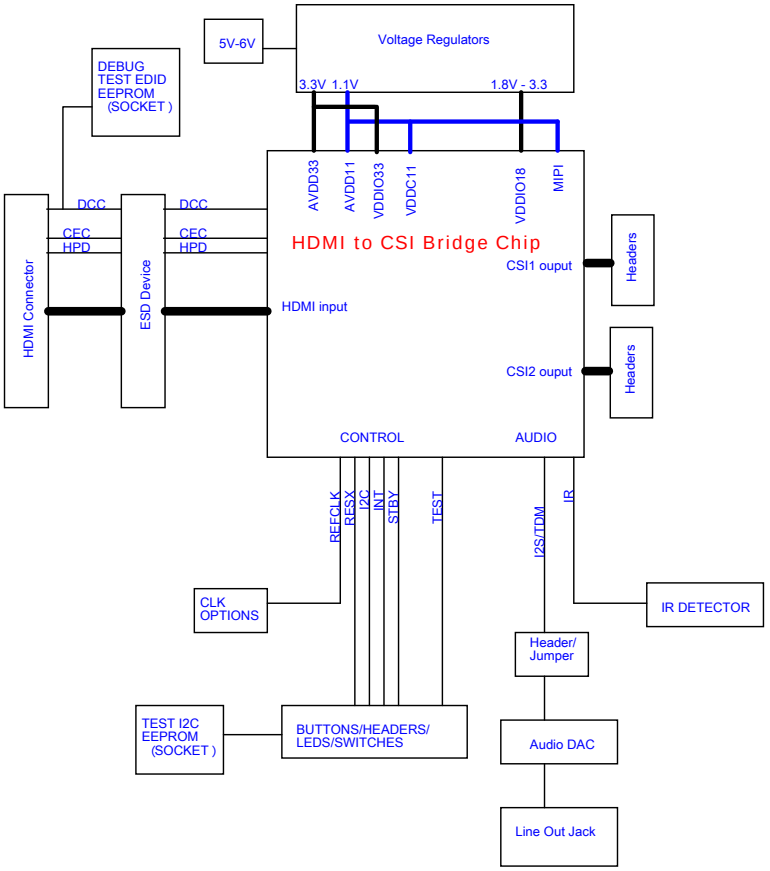


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