SYSC2310 Lab 4 Report

1.0 EXERCISE 1: DESIGN AN ARBITRARY FUNCTION

1.1 Description of Circuit's Operation

The circuit designed in Exercise 1 has four inputs and two outputs. The input is a 4-bit number. One of the outputs signals HIGH when the inputted number is prime and outputs LOW when it is not. The other output signals HIGH when the inputted number is divisible by 3 or 4 and signals LOW when the number meets neither of those conditions.

The circuit was designed using Logisim's Combinational Analysis function. The truth table for the circuit was inputted manually, the kmaps were generated, and the circuit diagram was produced by the program, shown in Figure 1.

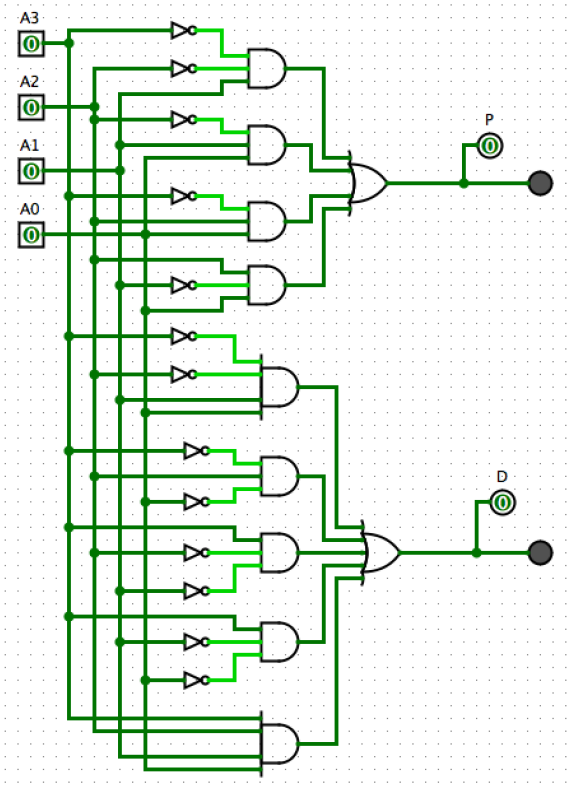
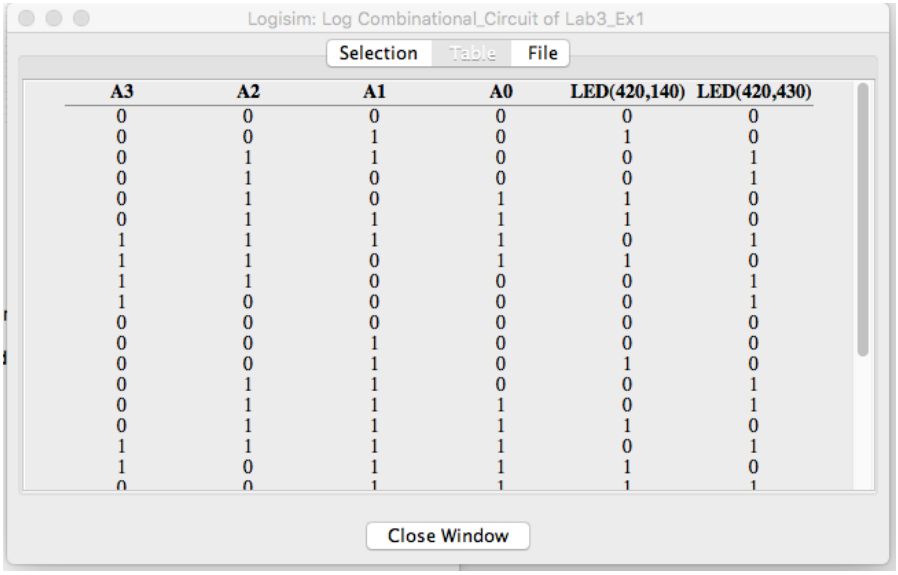


Figure 1. Diagram of Exercise 1 circuit

1.2 Verifying the Circuit's Operation

The circuit's operation was verified using Logisim's logging function, shown in Figure 2, by comparing actual outputs with their expected outputs.



A3	A2	A1	A0	LED(420,140)	LED(420,430)
0	0	0	0	0	0
0	0	1	0	1	0
0	1	1	0	0	1
0	1	0	0	0	1
0	1	0	1	1	0
0	1	1	1	1	0
1	1	1	1	0	1
1	1	0	1	1	0
1	1	0	0	0	1
1	0	0	0	0	1
0	0	0	0	0	0
0	0	1	0	0	0
0	0	1	0	1	0
0	1	1	0	0	1
0	1	1	1	0	1
0	1	1	1	1	0
1	1	1	1	0	1
1	0	1	1	1	0
0	0	1	1	1	1

Figure 2. Logging file used to verify circuit operation in Exercise 1

2.0 EXERCISE 2: BCD TO 7-SEGMENT DECODER

2.1 Description of Circuit's Operation

The circuit designed in Exercise 2 is a BCD to 7-segment decoder. As shown in Figure 3, the circuit takes in 4 inputs, representing a binary number and has 7 outputs which go to a 7-segment display, displaying the corresponding input between 0-9 on the 7-segment display. The circuit works in a desired manner only for inputs between 0-9. It has been observed that inputting any number between 10-15 will output either a 9, 5, mirrored 6, or 6, on the display, however the inputs are being falsely represented.

The circuit was designed using Logisim's Combinational Analysis function. The truth

table for the circuit was inputted manually, the K-maps were generated, and the circuit diagram was produced by the program.

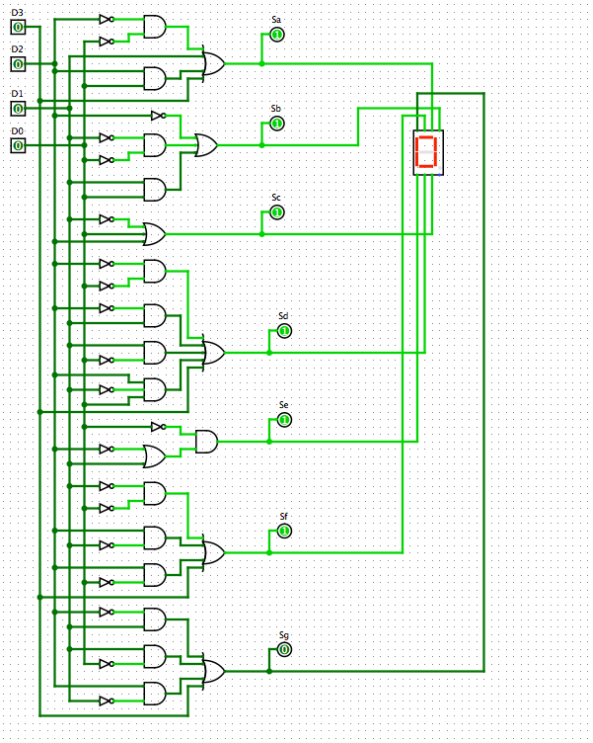
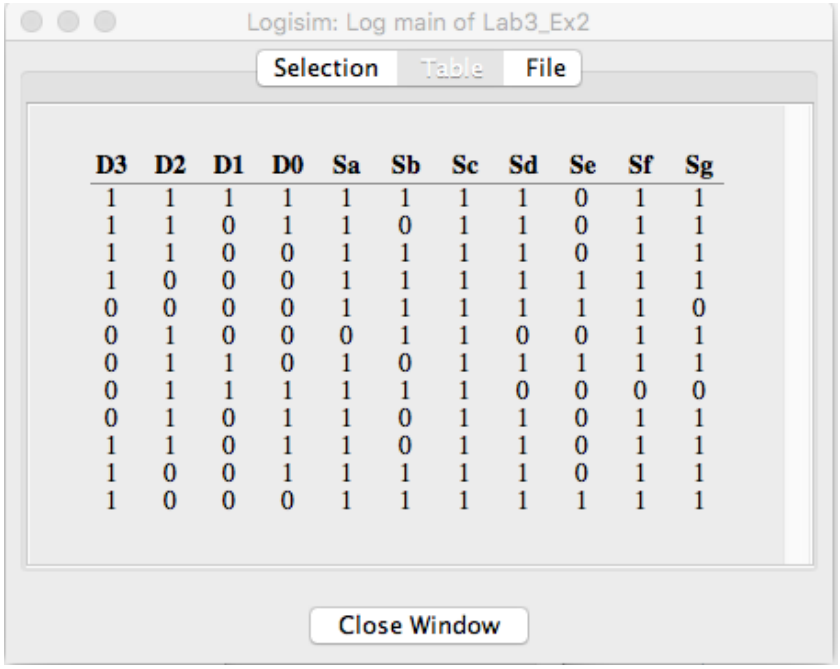


Figure 3. Diagram for the circuit in Exercise 2

2.2 Verifying the Circuit's Operation

The circuit's operation was verified using Logisim's logging function, shown in Figure 4, by comparing actual outputs with their expected outputs.



D3	D2	D1	D0	Sa	Sb	Sc	Sd	Se	Sf	Sg
1	1	1	1	1	1	1	1	0	1	1
1	1	0	1	1	0	1	1	0	1	1
1	1	0	0	1	1	1	1	0	1	1
1	0	0	0	1	1	1	1	1	1	1
0	0	0	0	1	1	1	1	1	1	0
0	1	0	0	0	1	1	0	0	1	1
0	1	1	0	1	0	1	1	1	1	1
0	1	1	1	1	1	1	0	0	0	0
0	1	0	1	1	0	1	1	0	1	1
1	1	0	1	1	0	1	1	0	1	1
1	0	0	1	1	1	1	1	0	1	1
1	0	0	0	1	1	1	1	1	1	1

Figure 4. Logging file used to verify circuit operation in Exercise 2