**SYSC2310 – LAB 2 REPORT**

1. EXERCISE 1: SIMPLIFY A BOOLEAN LOGIC FUNCTION

1.1 Description of Circuit’s Operation  
In Exercise 1, students were required to build a digital circuit representing the equation seen in Figure 1, labelled Function 1 (F1), and were then required to build an equivalent simplified circuit consisting of a max of 5 literals, shown in Figure 2, labelled Function 2 (F2).

Figure 1. Equation representing Function 1 in Exercise 1

Figure 2. Equation representing Function 2 in Exercise 1

Boolean logical equivalence rules were used to derive Function 2 from Function 1. The digital circuit diagrams for Function 1 and Function are shown in Figure 3 and in Figure 4, respectively.

Diagram, schematic

Description automatically generated

Figure 3. Screenshot of Function 1 circuit in Exercise 1

Diagram

Description automatically generatedFigure 4. Screenshot of Function 2 circuit in Exercise 1

1.2 Verifying the Circuit’s Operation  
To prove that Function 1 and Function 2 were equivalent, the outputs of the two functions were inputted into an XNOR gate, which produces a ‘1’ if the inputs are equal and a ‘0’ if the inputs are different, as seen in Figure 5.  
Diagram

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Figure 5. Screenshot of circuit comparing the equivalence of Function 1 and Function 2 in Exercise 1

1. EXERCISE 2: CONVERT A SET OF BOOLEAN FUNCTIONS TO A CIRCUIT

2.1 Description of Circuit’s Operation  
The circuit built in Exercise 2 performed 2-bit by 2-bit binary multiplication operation, shown in Figure 6. The circuit was designed using the functions shown in Figure 7 and were individually built as subcircuits and implemented together. The diagrams for and are found in Figures 8, 9, 10, and 11, respectively.

Diagram, schematic

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Figure 6. 2-bit by 2-bit binary multiplication circuit in Exercise 2

Figure 7. Functions implemented in 2-bit by 2-bit binary multiplication digital circuit in Exercise 2

Diagram

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Figure 8. Subcircuit diagram for in Exercise 2

Diagram, schematic

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Figure 9. Subcircuit diagram for in Exercise 2

Diagram, schematic

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Figure 10. Subcircuit diagram for in Exercise 2

Diagram

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Figure 11. Subcircuit diagram for in Exercise 2

2.2 Verification of Circuit’s Operation  
The circuit’s operation was verified though the use of log sheets, as shown in Figure 12. Since the circuit is a 2-bit by 2-bit multiplier, the range of the of inputs are from 0 to 3, and the range of the outputs are from 0 to 9.

Table

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Figure 12. Screenshot log sheet in Exercise 2

1. EXERCISE 3: DESIGN A 3-BIT BY 2-BIT BINARY MULTIPLIER

3.1 Description of Circuit’s Operation  
The circuit in Exercise 3 performs a 3-bit by 2-bit multiplication operation and the diagram is shown in Figure 13. The circuit utilizes the half-adder and full-adder from Lab 1. The equation was derived using the procedure for multiplying two binary numbers and combines inputs into the half- and full-adders and is found for this circuit in Figure 14. The 6 subcircuits in column use an AND gate on two inputs, seen in Figure 15. The half-adder and full-adder diagrams are shown in Figures 16 and 17, respectively.  
Diagram, schematic

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Figure 13. Screenshot of 3-bit by 2-bit multiplication circuit diagram in Exercise 3

Figure 14. Equations derived for the solution of a 3-bit by 2-bit binary multiplication operation

Diagram

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Figure 15. AND operation for two inputs in Exercise 3

Diagram

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Figure 16. Half-adder circuit from Lab 1, used in Exercise 3

Diagram

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Figure 17. Full-adder circuit from Lab 1, used in Exercise 3.  
3.2 Verification of Circuit’s Operation  
The circuit’s operation was verified using Logisim’s logging feature, seen in Figure 18. Since the circuit is a 3-bit by 2-bit multiplier, the range of the outputs is between 0 and 21.

Graphical user interface, application

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Figure 18. Screenshot of Logisim log