Abstract

This example program shows how to generate a stream of 32-bit data values, transmitted at a specific clock frequency, which are preceded by a synchronization pulse which is signaling the start of a new data frame to the receiver.

The SGPIO configuration is as follows:

SLICE B: serial clock output on SGPIO PIN 8 (1-bit mode)

SLICE I: synchronization pulse on SGPIO PIN 1 (1-bit mode)

SLICE A: 32-bit data stream on SGPIO PIN 0 (1-bit mode)

The clock and frame pulse are continuously running, and never stop.

The first LSB of the data is output in correspondence of the falling edge of the sync pulse, which is one serial clock wide. The data bits are transmitted on the rising edge of the clock, and the receiving side can sample the data on the falling edge of the clock.

The data is transmitted LSB first and the system is synchronous to the serial clock.

The frequency of the SGPIO block needs to be specified within the file sgpio.h by the following macro

```
/* assume running from PLL1 @ 204 MHz */
#define SGPIO_IP_CLOCK (204000000UL)
```

The desired data clock needs to be specified within the file SGPIO_makeFrame0Config.c by the following macro:

```
/* configure desired serial line frequency */
#define FRAME_CLOCK (51000000UL)
```