The PoC-Library Documentation

Release td

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Introduction

Part I

Introduction

This library is published and maintained by **Chair for VLSI Design, Diagnostics and Architecture** - Faculty of Computer Science, Technische Universität Dresden, Germany https://tu-dresden.de/ing/informatik/ti/vlsi

PoC - "Pile of Cores" provides implementations for often required hardware functions such as Arithmetic Units, Caches, Clock-Domain-Crossing Circuits, FIFOs, RAM wrappers, and I/O Controllers. The hardware modules are typically provided as VHDL or Verilog source code, so it can be easily re-used in a variety of hardware designs.

All hardware modules use a common set of VHDL packages to share new VHDL types, sub-programs and constants. Additionally, a set of simulation helper packages eases the writing of testbenches. Because PoC hosts a huge amount of IP cores, all cores are grouped into sub-namespaces to build a better hierachy.

Various simulation and synthesis tool chains are supported to interoperate with PoC. To generalize all supported free and commercial vendor tool chains, PoC is shipped with a Python based infrastructure to offer a command line based frontend.

News

See *Change Log* for latest updates.

Cite the PoC-Library

The PoC-Library hosted at GitHub.com. Please use the following biblatex entry to cite us:

```
# BibLaTex example entry
@online{poc,
  title={{PoC - Pile of Cores}},
  author={{Chair of VLSI Design, Diagnostics and Architecture}},
  organization={{Technische Universität Dresden}},
  year={2016},
  url={https://github.com/VLSI-EDA/PoC},
  urldate={2016-10-28},
}
```

CHAPTER 1

What is PoC?

PoC - “Pile of Cores” provides implementations for often required hardware functions such as Arithmetic Units, Caches, Clock-Domain-Crossing Circuits, FIFOs, RAM wrappers, and I/O Controllers. The hardware modules are typically provided as VHDL or Verilog source code, so it can be easily re-used in a variety of hardware designs.

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Various simulation and synthesis tool chains are supported to interoperate with PoC. To generalize all supported free and commercial vendor tool chains, PoC is shipped with a Python based Infrastruture to offer a command line based frontend.

The PoC-Library pursues the following five goals:

- independence in the platform, target, vendor and tool chain
- generic, efficient, resource sparing and fast implementations of IP cores
- optimized for several device architectures, if suitable
- supportive scripts to ease the IP core handling with all supported vendor tools on all listed operating systems
- ship all IP cores with testbenches for local and online verification

In detail the PoC-Library is:

- synthesizable for ASIC and FPGA devices, e.g. from Altera, Lattice, Xilinx, . . . ,
- supports a wide range of simulation and synthesis tool chains, and is
- executable on several host platforms: Darwin, Linux or Windows.

This is achieved by using generic HDL descriptions, which work with most synthesis and simulation tools mentioned above. If this is not the case, then PoC uses vendor or tool dependent work-arounds. These work-arounds can be different implementations switched by VHDL *generate* statements as well as different source files containing modified implementations.

One special feature of PoC is it, that the user has not to take care of such implementation switchings. PoC’s IP cores decide on their own what’s the *best* implementation for the chosen target platform. For this feature, PoC

implements a configuration package, which accepts a well-known development board name or a target device string. For example a FPGA device string is decoded into: vendor, device, generation, family, subtype, speed grade, pin count, etc. Out of these information, the PoC component can for example implement a vendor specific carry-chain description to speed up an algorithm or group computation units to effectively use 6-input LUTs.

1.1 What is the History of PoC?

In the past years, a lot of "IP cores" were developed at the chair of VLSI design[1] . This lose set of HDL designs was gathered in an old-fashioned CVS repository and grow over the years to a collection of basic HDL implementations like ALUs, FIFOs, UARTs or RAM controllers. For their final projects (bachelor, master, diploma thesis) students got access to PoC, so they could focus more on their main tasks than wasting time in developing and testing basic IP implementations from scratch. But the library was initially for internal and educational use only.

As a university chair for VLSI design, we have a wide range of different FPGA prototyping boards from various vendors and device families as well as generations. So most of the IP cores were developed for both major FPGA vendor platforms and their specific vendor tool chains. The main focus was to describe hardware in a more flexible and generic way, so that an IP core could be reused on multiple target platforms.

As the number of cores increased, the set of common functions and types increased too. In the end PoC is not only a collection of IP cores, its also shipped with a set of packages containing utility functions, new types and type conversions, which are used by most of the cores. This makes PoC a *library*, not only a *collection* of IPs.

As we started to search for ways to publish IP cores and maybe the whole PoC-Library, we found several platforms on the Internet, but none was very convincing. Some collective websites contained inactive projects, others were controlled by companies without the possibility to contribute and the majority was a long list of private projects with at most a handful of IP cores. Another disagreement were the used license types for these projects. We decided to use the Apache License, because it has no copyleft rule, a patent clause and allows commercial usage.

We transformed the old CVS repository into three Git repositories: An internal repository for the full set of IP cores (incl. classified code), a public one and a repository for examples, called PoC-Examples, both hosted on GitHub. PoC itself can be integrated into other HDL projects as a library directory or a Git submodule. The preferred usage is the submodule integration, which has the advantage of linked repository versions from hosting Git and the submodule Git. This is already exemplified by our PoC-Examples repository.

1.2 Which Tool Chains are supported?

The PoC-Library and its Python-based infrastructure currently supports the following free and commercial vendor tool chains:

- Synthesis Tool Chains:
  - **Altera Quartus** Tested with Quartus-II $\geq$ 13.0. Tested with Quartus Prime $\geq$ 15.1.
  - **Intel Quartus** Tested with Quartus Prime $\geq$ 16.1.
  - **Lattice Diamond** Tested with Diamond $\geq$ 3.6.
  - **Xilinx ISE** Only ISE 14.7 inclusive Core Generator 14.7 is supported.
  - **Xilinx PlanAhead** Only PlanAhead 14.7 is supported.
  - **Xilinx Vivado** Tested with Vivado $\geq$ 2015.4. Due to a limited VHDL language support compared to ISE 14.7, some PoC IP cores need special work arounds. See the synthesis documention section for Vivado for more details.
- Simulation Tool Chains:

[1] The PoC-Library is published and maintained by the **Chair for VLSI Design, Diagnostics and Architecture** - Faculty of Computer Science, Technische Universität Dresden, Germany http://tu-dresden.de/inf/vlsi-eda

- **Aldec Active-HDL** Tested with Active-HDL (or Student-Edition) $\geq$ 10.3 Tested with Active-HDL Lattice Edition $\geq$ 10.2
- **Cocotb with Mentor QuestaSim backend** Tested with Mentor QuestaSim 10.4d
- **Mentor Graphics ModelSim** Tested with ModelSim PE (or Student Edition) $\geq$ 10.5c Tested with ModelSim SE $\geq$ 10.5c Tested with ModelSim Altera Edition 10.3d (or Starter Edition)
- **Mentor Graphics QuestaSim/ModelSim** Tested with Mentor QuestaSim $\geq$ 10.4d
- **Xilinx ISE Simulator** Tested with ISE Simulator (iSim) 14.7. The Python infrastructure supports isim, but PoC's simulation helper packages and testbenches rely on VHDL-2008 features, which are not supported by isim.
- **Xilinx Vivado Simulator** Tested with Vivado Simulator (xsim) $\geq$ 2016.3. The Python infrastructure supports xsim, but PoC's simulation helper packages and testbenches rely on VHDL-2008 features, which are not fully supported by xsim, yet.
- **GHDL + GTKWave** Tested with GHDL $\geq$ 0.34dev and GTKWave $\geq$ 3.3.70 Due to ungoing development and bugfixes, we encourage to use the newest GHDL version.

1.3 Why should I use PoC?

Here is a brief list of advantages:

- We explicitly use the wording *PoC-Library* rather then *collection*, because PoC's packages and IP cores build an ecosystem. Complex IP cores are build on-top of basic IP cores - they are no lose set of cores. The cores offer a clean interface and can be configured by many generic parameters.
- PoC is target independent: It's possible to switch the target device or even the device vendor without switching the IP core.

Todo: Use a well tested set of packages to ease the use of VHDL

Use a well tested set of simulation helpers

Run testbenches in various simulators.

Run synthesis tests in varous synthesis tools.

Compare hardware usage for different target platfroms.

Supports simulation with vendor primitive libraries, ships with script to pre-compile vendor libraries.

Vendor tools have bugs, check you IP cores when a new tool release is available, before changing code base

---

1.4 Who uses PoC?

PoC has a related Git repository called PoC-Examples on GitHub. This repository hosts a list of example and reference implementations of the PoC-Library. Additional to reading an IP cores documention and viewing its characteristic stimulus waveform in a simulation, it can helper to investigate an IP core usage example from that repository.

- The Q27 Project 27-Queens Puzzle: Massively Parellel Enumeration and Solution Counting
- Reconfigurable Cloud Computing Framework (RC2F) An FPGA computing framework for virtualization and cloud integration.
- PicoBlaze-Library The PicoBlaze-Library offers several PicoBlaze devices and code routines to extend a common PicoBlaze environment to a little System on a Chip (SoC or SoFPGA).

- PicoBlaze-Examples A SoFPGA reference implementation, based on the PoC-Library and the PicoBlaze-Library.

CHAPTER 2

Quick Start Guide

This **Quick Start Guide** gives a fast and simple introduction into PoC. All topics can be found in the *Using PoC* section with much more details and examples.

Contents of this Page

2.1 Requirements and Dependencies

The PoC-Library comes with some scripts to ease most of the common tasks, like running testbenches or generating IP cores. PoC uses Python 3 as a platform independent scripting environment. All Python scripts are wrapped in Bash or PowerShell scripts, to hide some platform specifics of Darwin, Linux or Windows. See *Requirements* for further details.

PoC requires:

- A *supported synthesis tool chain*, if you want to synthezise IP cores.
- A *supported simulator too chain*, if you want to simulate IP cores.
- The **Python 3** programming language and runtime, if you want to use PoC's infrastructure.
- A shell to execute shell scripts:
  - **Bash** on Linux and OS X

  - **PowerShell** on Windows

PoC optionally requires:

- **Git** command line tools or
- **Git User Interface**, if you want to check out the latest 'master' or 'release' branch.

PoC depends on third part libraries:

- *Cocotb* A coroutine based cosimulation library for writing VHDL and Verilog testbenches in Python.
- *OSVVM* Open Source VHDL Verification Methodology.
- *UVVM* Universal VHDL Verification Methodology.
- *VUnit* An unit testing framework for VHDL.

All dependencies are available as GitHub repositories and are linked to PoC as Git submodules into the PoC-Root\lib directory. See *Third Party Libraries* for more details on these libraries.

2.2 Download

The PoC-Library can be downloaded as a zip-file (latest 'master' branch), cloned with `git clone` or embedded with `git submodule add` from GitHub. GitHub offers HTTPS and SSH as transfer protocols. See the *Download* page for further details. The installation directory is referred to as `PoCRoot`.

Protocol	Git Clone Command
HTTPS	`git clone --recursive https://github.com/VLSI-EDA/PoC.git PoC`
SSH	`git clone --recursive ssh://git@github.com:VLSI-EDA/PoC.git PoC`

2.3 Configuring PoC on a Local System

To explore PoC's full potential, it's required to configure some paths and synthesis or simulation tool chains. The following commands start a guided configuration process. Please follow the instructions on screen. It's possible to relaunch the process at any time, for example to register new tools or to update tool versions. See *Configuration* for more details. Run the following command line instructions to configure PoC on your local system:

```
cd PoCRoot
.\poc.ps1 configure
```

Use the keyboard buttons: to accept, to decline, to skip/pass a step and to accept a default value displayed in brackets.

2.4 Integration

The PoC-Library is meant to be integrated into other HDL projects. Therefore it's recommended to create a library folder and add the PoC-Library as a Git submodule. After the repository linking is done, some short configuration steps are required to setup paths, tool chains and the target platform. The following command line instructions show a short example on how to integrate PoC.

1. Adding the Library as a Git submodule

The following command line instructions will create the folder `lib\PoC\` and clone the PoC-Library as a Git submodule into that folder. `ProjectRoot` is the directory of the hosting Git. A detailed list of steps can be found at *Integration*.

```
cd ProjectRoot
mkdir lib | cd
git submodule add https://github.com:VLSI-EDA/PoC.git PoC
cd PoC
git remote rename origin github
cd ..\..
git add .gitmodules lib\PoC
git commit -m "Added new git submodule PoC in 'lib\PoC' (PoC-Library)."
```

2. Configuring PoC

The PoC-Library should be configured to explore its full potential. See *Configuration* for more details. The following command lines will start the configuration process:

```
cd ProjectRoot
.\lib\PoC\poc.ps1 configure
```

3. Creating PoC's `my_config.vhdl` and `my_project.vhdl` Files

The PoC-Library needs two VHDL files for its configuration. These files are used to determine the most suitable implementation depending on the provided target information. Copy the following two template files into your project's source folder. Rename these files to *.vhdl and configure the VHDL constants in the files:

```
cd ProjectRoot
cp lib\PoC\src\common\my_config.vhdl.template src\common\my_config.vhdl
cp lib\PoC\src\common\my_project.vhdl.template src\common\my_project.vhdl
```

my_config.vhdl defines two global constants, which need to be adjusted:

```
constant MY_BOARD            : string := "CHANGE THIS"; -- e.g. Custom, ML505,␣
↪KC705, Atlys
constant MY_DEVICE           : string := "CHANGE THIS"; -- e.g. None, XC5VLX50T-
↪1FF1136, EP2SGX90FF1508C3
```

my_project.vhdl also defines two global constants, which need to be adjusted:

```
constant MY_PROJECT_DIR      : string := "CHANGE THIS"; -- e.g. d:/vhdl/myproject/,
↪ /home/me/projects/myproject/"
constant MY_OPERATING_SYSTEM : string := "CHANGE THIS"; -- e.g. WINDOWS, LINUX
```

Further informations are provided at *Creating my_config/my_project.vhdl*.

4. Adding PoC's Common Packages to a Synthesis or Simulation Project

PoC is shipped with a set of common packages, which are used by most of its modules. These packages are stored in the `PoCRoot\src\common` directory. PoC also provides a VHDL context in `common.vhdl` , which can be used to reference all packages at once.

5. Adding PoC's Simulation Packages to a Simulation Project

Simulation projects additionally require PoC's simulation helper packages, which are located in the `PoCRoot\src\sim` directory. Because some VHDL version are incompatible among each other, PoC uses version suffixes like `*.v93.vhdl` or `*.v08.vhdl` in the file name to denote the supported VHDL version of a file.

6. Compiling Shipped IP Cores

Some IP Cores are shipped are pre-configured vendor IP Cores. If such IP cores shall be used in a HDL project, it's recommended to use PoC to create, compile and if needed patch these IP cores. See *Synthesis* for more details.

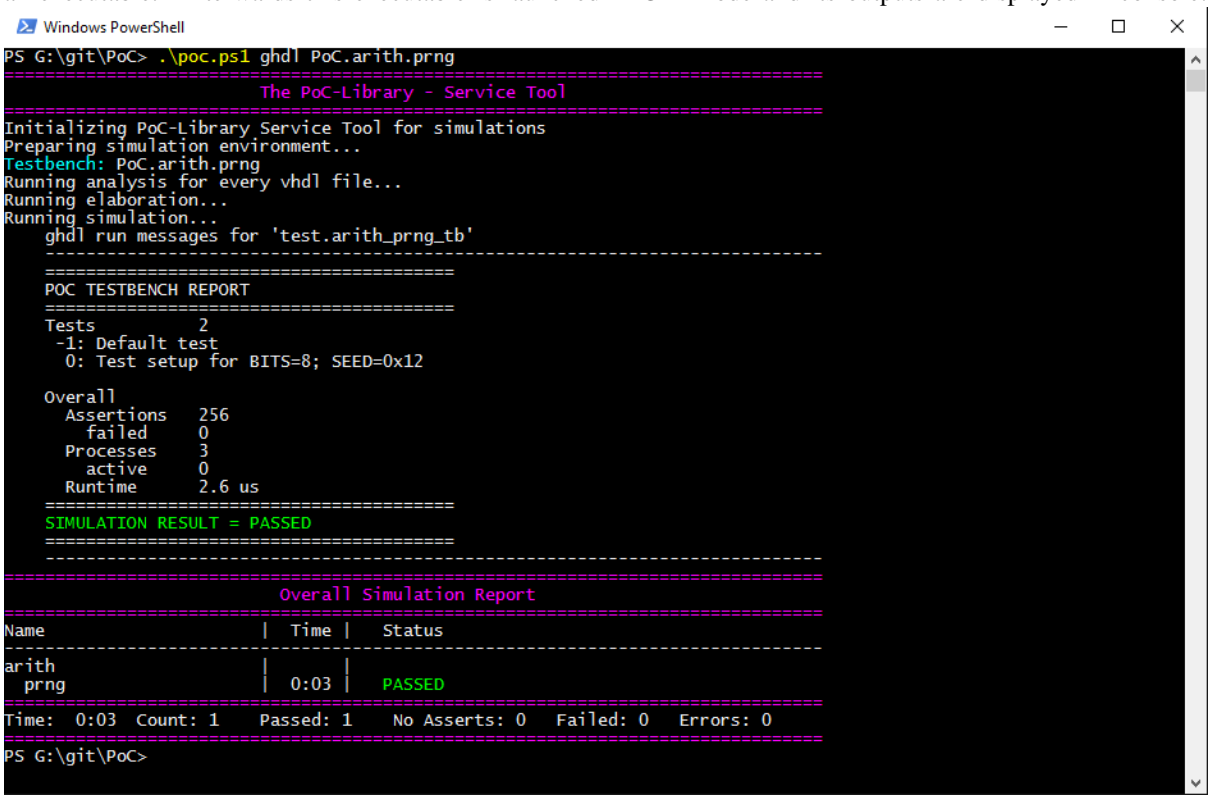
2.5 Run a Simulation

The following quick example uses the GHDL Simulator to analyze, elaborate and simulate a testbench for the module `arith_prng` (Pseudo Random Number Generator - PRNG). The VHDL file `arith_prng.vhdl` is located at `PoCRoot\src\arith` and virtually a member in the *PoC.arith* namespace. So the module can be identified by an unique name: `PoC.arith.prng`, which is passed to the frontend script.

Example:

```
cd PoCRoot
.\poc.ps1 ghdl PoC.arith.prng
```

The CLI command `ghdl` chooses *GHDL Simulator* as the simulator and passes the fully qualified PoC entity name `PoC.arith.prng` as a parameter to the tool. All required source file are gathered and compiled to an executable. Afterwards this executable is launched in CLI mode and its outputs are displayed in console:



Each testbench uses PoC's simulation helper packages to count asserts and to track active stimuli and checker processes. After a completed simulation run, an report is written to STDOUT or the simulator's console. Note the

line `SIMULATION RESULT = PASSED`. For each simulated PoC entity, a line in the overall report is created. It lists the runtime per testbench and the simulation status (`. . .` `ERROR`, `FAILED`, `NO ASSERTS` or `PASSED`). See *Simulation* for more details.

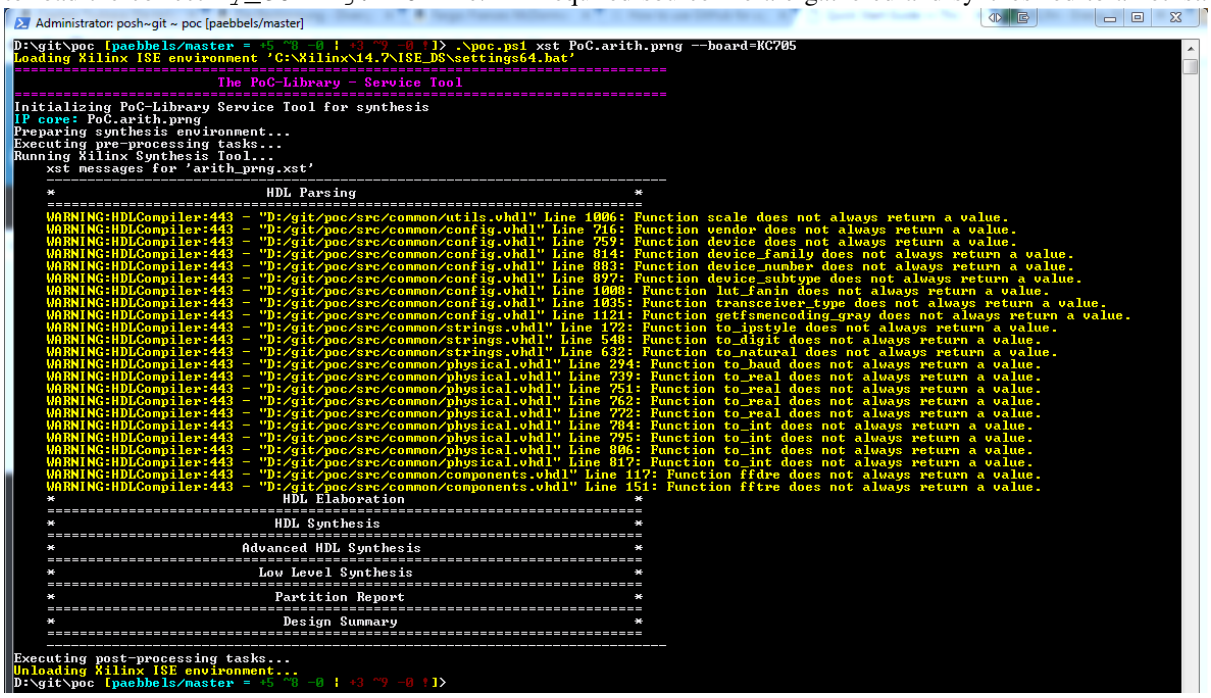
2.6 Run a Synthesis

The following quick example uses the Xilinx Systesis Tool (XST) to synthesize a netlist for IP core `arith_prng` (Pseudo Random Number Generator - PRNG). The VHDL file `arith_prng.vhdl` is located at `PoCRoot\src\arith` and virtually a member in the *PoC.arith* namespace. So the module can be identified by an unique name: `PoC.arith.prng`, which is passed to the frontend script.

Example:

```
cd PoCRoot
.\poc.ps1 xst PoC.arith.prng --board=KC705
```

The CLI command `xst` chooses *Xilinx Synthesis Tool* as the synthesizer and passes the fully qualified PoC entity name `PoC.arith.prng` as a parameter to the tool. Additionally, the development board name is required to load the correct `my_config.vhdl` file. All required source file are gathered and synthesized to a netlist.



2.7 Updating

The PoC-Library can be updated by using `git fetch` and `git merge`.

```
cd PoCRoot
# update the local repository
git fetch --prune
# review the commit tree and messages, using the 'treea' alias
git treea
# if all changes are OK, do a fast-forward merge
git merge
```

See also:

Running one or more testbenches The installation can be checked by running one or more of PoC's testbenches.

Running one or more netlist generation flows The installation can also be checked by running one or more of PoC's synthesis flows.

CHAPTER 3

Get Involved

A first step might be to use and explore PoC and it's infrastructure in an own project. Moreover, we encurage to read our online help which covers all aspects from quickstart example up to detailed IP core documentation. While using PoC, you might discover issues or missing feature. Please report them as *listed below*. If you have an interresting project, please send us feedback or get listed on our *Who uses PoC?* page.

If you are more familiar with PoC and it's components, you might start asking youself how components internally work. Please read our more advanced topics in the online help, read our inline source code comments or start a discussion on *Gitter* to ask us directly.

Now you should be very familiar with our work and you might be interessted in developing own components and contribute them to the main repository. See the *next section* for detailed instructions on the Git fork, commit, push and pull-request flow.

PoC ships some *third-party libraries*. If you are interessted in getting your library or components shipped as part of PoC or as a third-party components, please contact us.

3.1 Report a Bug

Please report issues of any kind in our Git provider's issue tracker. This allows us to categorize issues into groups and assign developers to them. You can track the issue's state and see how it's getting solved. All enhancements and feature requests are tracked on GitHub at GitHub Issues.

3.2 Feature Request

Please report missing features of any kind. We are allways looking forward to provide a full feature set. Please use our Git provider's issue tracker to report enhancements and feature requests, so you can track the request's status and implementation. All enhancements and feature requests are tracked on GitHub at GitHub Issues.

3.3 Talk to us on Gitter

You can chat with us on Gitter in our Giiter Room VLSI-EDA/PoC. You can use Gitter for free with your existing GitHub or Twitter account.

3.4 Contributers License Agreement

We require all contributers to sign a Contributor License Agreement (CLA). If you don't know whatfore a CLA is needed and how it prevents legal issues on both sides, read this short blog post. PoC uses the *Apache Contributor License Agreement* to match the *Apache License 2.0*.

So to get started, sign the Contributor License Agreement (CLA) at CLAHub.com. You can authenticate yourself with an existing GitHub account.

3.5 Contribute to PoC

Contibuting source code via Git is very easy. We don't provide direct write access to our repositories. Git offers the fork and pull-request philosophy, which means: You clone a repository, provide your changes in your own repository and notify us about outstanding changes via a pull-requests. We will then review your proposed changes and integrate them into our repository.

Steps 1 to 5 are done only once for setting up a forked repository.

3.5.1 1. Fork the PoC Repository

Git repositories can be cloned on a Git provider's server. This procedure is called *forking*. This allows Git providers to track the repository's network, check if repositories are related to each other and notify if pull-requests are available.

Fork our repository `VLSI-EDA/PoC` on GitHub into your or your's Git organisation's account. In the following the forked repository is referenced as `<username>/PoC`.

3.5.2 2. Clone the new Fork

Clone this new fork to your machine. See *Downloading via Git clone* for more details on how to clone PoC. If you have already cloned PoC, then you can setup the new fork as an additional *remote*. You should set `VLSI-EDA/PoC` as fetch target and the new fork `<username>/PoC` as push target.

Shell Commands for Cloning:

```
cd GitRoot
git clone --recursive "ssh://git@github.com:<username>/PoC.git" PoC
cd PoC
git remote rename origin github
git remote add upstream "ssh://git@github.com:VLSI-EDA/PoC.git"
git fetch --prune --tags
```

Shell Commands for Editing an existing Clone:

```
cd PoCRoot
git remote rename github upstream
git remote add github "ssh://git@github.com:<username>/PoC.git"
git fetch --prune --tags
```

These commands work for Git submodules too.

3.5.3 3. Checkout a Branch

Checkout the `master` or `release` branch and maybe stash outstanding changes.

```
cd PoCRoot
git checkout release
```

3.5.4 4. Setup PoC for Developers

Run PoC's *configuration routines* and setup the developer tools.

```
cd PoCRoot
.\PoC.ps1 configure git
```

3.5.5 5. Create your own `master` Branch

Each developer has his own `master` branch. So create one and check it out.

```
cd PoCRoot
git branch <username>/master
git checkout <username>/master
git push github <username>/master
```

If PoC's branches are moving forward, you can update your own master branch by merging changes into your branch.

3.5.6 6. Create your Feature Branch

Each new feature or bugfix is developed on a feature branch. Examples for branch names:

Branch name	Description
bugfix-utils	Fixes a bug in `utils.vhdl`.
docs-spelling	Fixes the documentation.
spi-controller	A new SPI controller implementation.

```
cd PoCRoot
git branch <username>/<feature>
git checkout <username>/<feature>
git push github <username>/<feature>
```

3.5.7 7. Commit and Push Changes

Commit your porposed changes onto your feature branch and push all changes to GitHub.

```
cd PoCRoot
# git add ....
git commit -m "Fixed a bug in function bounds() in utils.vhdl."
git push github <username>/<feature>
```

3.5.8 8. Create a Pull-Request

Go to your forked repository and klick on "Compare and Pull-Request" or go to our PoC repository and create a new pull request.

If this is your first Pull-Request, you need to sign our Contributers License Agreement (CLA).

3.5.9 9. Keep your `master` up-to-date

Todo: undocumented

3.6 Give us Feedback

Please send us feedback about the PoC documentation, our IP cores or your user story on how you use PoC.

3.7 List of Contributers

Contributor[1]	Contact E-Mail
Genßler, Paul	paul.genssler@tu-dresden.de
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Zabel, Martin[2]	martin.zabel@tu-dresden.de

Note: This is a local copy of the Apache License Version 2.0.

[1] In alphabetical order.
[2] Maintainer.

CHAPTER 4

Apache License 2.0

Version 2.0, January 2004

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4.1 1. Definitions.

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Appendix: How to apply the Apache License to your work

To apply the Apache License to your work, attach the following boilerplate notice, with the fields enclosed by brackets "[]" replaced with your own identifying information. (Don't include the brackets!) The text should be enclosed in the appropriate comment syntax for the file format. We also recommend that a file or class name and description of purpose be included on the same "printed page" as the copyright notice for easier identification within third-party archives.

Part II

Main Documentation

CHAPTER 5

Using PoC

PoC can be used in several ways, if all *Requirements* are fulfilled. Chose one of the following integration kinds:

- **Stand-Alone IP Core Library:** Download PoC as archive file (*.zip) from GitHub as latest branch copy or as tagged release file. IP cores can be copyed into one or more destination projects or the projects link to the selected IP core source files.

  Advantages:

  - Simple and fast setup, configuring PoC is optional.
  - Needs less disk space than a Git repository.
  - After a configuration, PoC's additional features: simulation, synthesis, etc. can be used.

  Disadvantages:

  - Manual updating via download and file overwrites.
  - Updated IP cores need to be copyed again into the destination project.
  - Using different PoC versions in different projects is not possible.
  - No possibility to contribute bugfixes and extensions via Git pull requests.

  Next steps: 1. See *Downloads* for how to download a stand-alone version (*.zip-file) of the PoC-Library. 2. See *Configuration* for how to configure PoC on a local system.

- **Stand-Alone IP Core Library cloned from Git:** Download PoC via `git clone` from GitHub as latest branch copy. IP cores can be copyed into one or more destination projects or the projects link to the selected IP core source files.

  Advantages:

  - Simple and fast setup, configuring PoC is optional.
  - Access to the newest commits on a branch: New IP cores, new features, bugfixes.
  - Fast and simple updates via `git pull`.
  - After a configuration, PoC's additional features: simulation, synthesis, etc. can be used.
  - Contribute bugfixes and extensions via Git pull requests.

  Disadvantages:

  - Updated IP cores need to be copyed again into the destination project.

  - Using different PoC versions in different projects is not possible

  Next steps: 1. See *Downloads* for how to clone a stand-alone version of the PoC-Library. 2. See *Configuration* for how to configure PoC on a local system.

- **Embedded IP Core Library as Git Submodule:** Integrate PoC as a Git submodule into the destination projects Git repository.

  Advantages:

  - Simple and fast setup, configuring PoC is optional, but recommended.
  - Access to the newest commits on a branch: New IP cores, new features, bugfixes.
  - Fast and simple updates via `git pull`.
  - After a configuration, PoC's additional features: simulation, synthesis, etc. can be used.
  - Moreover, some PoC infrastructure features can be used in the hosting repository and project as well.
  - Contribute bugfixes and extensions via Git pull requests.
  - Version linking between hosting Git and PoC.

  Next steps: 1. See *Integration* for how to integrate PoC as a Git submodule into an existing Git. 2. See *Configuration* for how to configure PoC on a local system.

5.1 Requirements

Contents of this Page

The PoC-Library comes with some scripts to ease most of the common tasks, like running testbenches or generating IP cores. We choose to use Python 3 as a platform independent scripting environment. All Python scripts are wrapped in Bash or PowerShell scripts, to hide some platform specifics of Darwin, Linux or Windows.

5.1.1 Common requirements:

Programming Languages and Runtime Environments:

- Python 3 ($\geq$ 3.5):
  - colorama
  - py-flags

  All Python requirements are listed in requirements.txt and can be installed via: `sudo python3.5 -m pip install -r requirements.txt`

Synthesis tool chains:

- Altera Quartus II $\geq$ 13.0 or

- Altera Quartus Prime $\geq$ 15.1 or
- Intel Quartus Prime $\geq$ 16.1 or
- Lattice Diamond $\geq$ 3.6 or
- Xilinx ISE 14.7[1] or
- Xilinx Vivado $\geq$ 2016.3[2]

Simulation tool chains

- Aldec Active-HDL (or Student Edition) or
- Aldec Active-HDL Lattice Edition or
- Mentor Graphics ModelSim PE (or Student Edition) or
- Mentor Graphics ModelSim SE or
- Mentor Graphics ModelSim Altera Edition or
- Mentor Graphics QuestaSim or
- Xilinx ISE Simulator 14.7 or
- Xilinx Vivado Simulator $\geq$ 2016.3[3] or
- GHDL $\geq$ 0.34dev and GTKWave $\geq$ 3.3.70

5.1.2 Linux specific requirements:

Debian and Ubuntu specific:

- `bash` is configured as `/bin/sh` (read more) `dpkg-reconfigure dash`

Optional Tools on Linux:

Git The command line tools to manage Git repositories. It's possible to extend the shell prompt with Git information.

SmartGit A Git client to handle complex Git flows in a GUI.

Generic Colouriser (grc) $\geq$ 1.9 Colorizes outputs of foreign scripts and programs. GRC is hosted on GitHub The latest *.deb installation packages can be downloaded here.

5.1.3 Mac OS specific requirements:

Bash $\geq$ 4.3 Mac OS is shipped with Bash 3.2. Use Homebrew to install an up-to-date Bash `brew install bash`

coreutils Mac OS' `readlink` program has a different behavior than the Linux version. The `coreutils` package installs a GNU readlink clone called `greadlink`. `brew install coreutils`

[1] Xilinx discontinued ISE since Oct. 2013. The last release was 14.7.

[2] Due to numerous bugs in the Xilinx Vivado Synthesis (incl. 2016.1), PoC can offer only a restricted Vivado support. See PoC's `Vivado` branch for a set of workarounds. The list of issues is documented on the *Known Issues* page.

[3] Due to numerous bugs in the Xilinx Simulator (incl. 2016.1), PoC can offer only a restricted Vivado support. The list of issues is documented on the *Known Issues* page.

Optional Tools on Mac OS:

Git The command line tools to manage Git repositories. It's possible to extend the shell prompt with Git information.

SmartGit or SourceTree A Git client to handle complex Git flows in a GUI.

Generic Colouriser (grc) $\geq$ 1.9 Colorizes outputs of foreign scripts and programs. GRC is hosted on GitHub `brew install Grc`

5.1.4 Windows specific requirements:

PowerShell

- **Allow local script execution** (read more) `PS> Set-ExecutionPolicy RemoteSigned`
- **PowerShell $\geq$ 5.0 (recommended)** PowerShell 5.0 is shipped since Windows 10. It is a part if the Windows Management Framework 5.0 (WMF). Windows 7 and 8/8.1 can be updated to WMF 5.0. The package does not include **PSReadLine**, which is included in the Windows 10 PowerShell environment. Install PSReadLine manually: `PS> Install-Module PSReadline`.
- **PowerShell 4.0** PowerShell is shipped with Windows since Vista. If the required version not already included in Windows, it can be downloaded from Microsoft.com: WMF 4.0

Optional Tools on Windows:

PowerShell $\geq$ 4.0

- **PSReadLine** replaces the command line editing experience in PowerShell for versions 3 and up.
- **PowerShell Community Extensions (PSCX) $\geq$ 3.2** The latest PSCX can be downloaded from PowerShellGallery `PS> Install-Module Pscx` Note: PSCX $\geq$ 3.2.1 is required for PowerShell $\geq$ 5.0.

Git (MSys-Git) The command line tools to manage Git repositories.

SmartGit or SourceTree A Git client to handle complex Git flows in a GUI.

posh-git PowerShell integration for Git `PS> Install-Module posh-git`

5.2 Downloading PoC

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5.2.1 Downloading from GitHub

The PoC-Library can be downloaded as a zip-file from GitHub. See the following table, to choose your desired git branch.

Branch	Download Link
master	zip-file
release	zip-file

5.2.2 Downloading via `git clone`

The PoC-Library can be downloaded (cloned) with `git clone` from GitHub. GitHub offers the transfer protocols HTTPS and SSH. You should use SSH if you have a GitHub account and have already uploaded an OpenSSH public key to GitHub, otherwise use HTTPS if you have no account or you want to use login credentials.

The created folder `<GitRoot>\PoC` is used as `<PoCRoot>` in later instructions or on other pages in this documentation.

Protocol	GitHub Repository URL
HTTPS	https://github.com/VLSI-EDA/PoC.git
SSH	ssh://git@github.com:VLSI-EDA/PoC.git

On Linux

Command line instructions to clone the PoC-Library onto a Linux machine with HTTPS protocol:

```
cd GitRoot
git clone --recursive "https://github.com/VLSI-EDA/PoC.git" PoC
cd PoC
git remote rename origin github
```

Command line instructions to clone the PoC-Library onto a Linux machine machine with SSH protocol:

```
cd GitRoot
git clone --recursive "ssh://git@github.com:VLSI-EDA/PoC.git" PoC
cd PoC
git remote rename origin github
```

On OS X

Please see the Linux instructions.

On Windows

Note: All Windows command line instructions are intended for **`Windows PowerShell`**, if not marked otherwise. So executing the following instructions in Windows Command Prompt (**`cmd.exe`**) won't function or result in errors! See the *Requirements section* on where to download or update PowerShell.

Command line instructions to clone the PoC-Library onto a Windows machine with HTTPS protocol:

```
cd GitRoot
git clone --recursive "https://github.com/VLSI-EDA/PoC.git" PoC
cd PoC
git remote rename origin github
```

Command line instructions to clone the PoC-Library onto a Windows machine with SSH protocol:

```
cd GitRoot
git clone --recursive "ssh://git@github.com:VLSI-EDA/PoC.git" PoC
cd PoC
git remote rename origin github
```

Note: The option `--recursive` performs a recursive clone operation for all linked git submodules. An additional `git submodule init` and `git submodule update` call is not needed anymore.

5.2.3 Downloading via `git submodule add`

The PoC-Library is meant to be integrated into other HDL projects (preferably Git versioned projects). Therefore it's recommended to create a library folder and add the PoC-Library as a git submodule.

The following command line instructions will create a library folder :file:'lib' and clone PoC as a git submodule into the subfolder :file:'<ProjectRoot>libPoC'.

On Linux

Command line instructions to clone the PoC-Library onto a Linux machine with HTTPS protocol:

```
cd ProjectRoot
mkdir lib
git submodule add "https://github.com/VLSI-EDA/PoC.git" lib/PoC
cd lib/PoC
git remote rename origin github
cd ../..
git add .gitmodules lib/PoC
git commit -m "Added new git submodule PoC in 'lib/PoC' (PoC-Library)."
```

Command line instructions to clone the PoC-Library onto a Linux machine machine with SSH protocol:

```
cd ProjectRoot
mkdir lib
git submodule add "ssh://git@github.com:VLSI-EDA/PoC.git" lib/PoC
cd lib/PoC
git remote rename origin github
cd ../..
git add .gitmodules lib/PoC
git commit -m "Added new git submodule PoC in 'lib/PoC' (PoC-Library)."
```

On OS X

Please see the Linux instructions.

On Windows

Note: All Windows command line instructions are intended for **`Windows PowerShell`**, if not marked otherwise. So executing the following instructions in Windows Command Prompt (**`cmd.exe`**) won't function or result in errors! See the *Requirements section* on where to download or update PowerShell.

Command line instructions to clone the PoC-Library onto a Windows machine with HTTPS protocol:

```
cd <ProjectRoot>
mkdir lib | cd
git submodule add "https://github.com/VLSI-EDA/PoC.git" PoC
cd PoC
git remote rename origin github
cd ..\..
git add .gitmodules lib\PoC
git commit -m "Added new git submodule PoC in 'lib\PoC' (PoC-Library)."
```

Command line instructions to clone the PoC-Library onto a Windows machine with SSH protocol:

```
cd <ProjectRoot>
mkdir lib | cd
git submodule add "ssh://git@github.com:VLSI-EDA/PoC.git" PoC
cd PoC
git remote rename origin github
cd ..\..
git add .gitmodules lib\PoC
git commit -m "Added new git submodule PoC in 'lib\PoC' (PoC-Library)."
```

5.3 Integrating PoC into Projects

Contents of this page

5.3.1 As a Git submodule

The following command line instructions will integrate PoC into a existing Git repository and register PoC as a Git submodule. Therefore a directory `lib\PoC\` is created and the PoC-Library is cloned as a Git submodule into that directory.

On Linux

```
cd ProjectRoot
mkdir lib
cd lib
git submodule add https://github.com/VLSI-EDA/PoC.git PoC
cd PoC
git remote rename origin github
cd ../..
git add .gitmodules lib\PoC
git commit -m "Added new git submodule PoC in 'lib/PoC' (PoC-Library)."
```

On OS X

Please see the Linux instructions.

On Windows

Note: All Windows command line instructions are intended for **`Windows PowerShell`**, if not marked otherwise. So executing the following instructions in Windows Command Prompt (**`cmd.exe`**) won't function or result in errors! See the *Requirements section* on where to download or update PowerShell.

```
cd ProjectRoot
mkdir lib | cd
git submodule add https://github.com/VLSI-EDA/PoC.git PoC
cd PoC
git remote rename origin github
cd ..\..
git add .gitmodules lib\PoC
git commit -m "Added new git submodule PoC in 'lib\PoC' (PoC-Library)."
```

See also:

Configuring PoC on a Local System

Create PoC's VHDL Configuration Files

5.4 Configuring PoC's Infrastructure

To explore PoC's full potential, it's required to configure some paths and synthesis or simulation tool chains. It's possible to relaunch the process at any time, for example to register new tools or to update tool versions.

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5.4.1 Overview

The setup process is started by invoking PoC's frontend script with the command `configure`. Please follow the instructions on screen. Use the keyboard buttons: to accept, to decline, to skip/pass a step and to accept a default value displayed in brackets.

Optionally, a vendor or tool chain name can be passed to the configuration process to launch only its configuration routines.

On Linux:

```
cd ProjectRoot
./lib/PoC/poc.sh configure
# with tool chain name
./lib/PoC/poc.sh configure Xilinx.Vivado
```

On OS X

Please see the Linux instructions.

On Windows

Note: All Windows command line instructions are intended for **`Windows PowerShell`**, if not marked otherwise. So executing the following instructions in Windows Command Prompt (**`cmd.exe`**) won't function or result in errors! See the *Requirements section* on where to download or update PowerShell.

```
cd ProjectRoot
.\lib\PoC\poc.ps1 configure
# with tool chain name
.\lib\PoC\poc.ps1 configure Xilinx.Vivado
```

Introduction screen:

```
PS D:\git\PoC> .\poc.ps1 configure
================================================================================
                        The PoC-Library - Service Tool
================================================================================
Explanation of abbreviations:
  Y - yes      P        - pass (jump to next question)
  N - no       Ctrl + C - abort (no changes are saved)
Upper case or value in '[...]' means default value
--------------------------------------------------------------------------------

Configuring PoC
  PoC version: v1.0.1 (found in git)
  Installation directory: D:\git\PoC (found in environment variable)
```

5.4.2 The PoC-Library

PoC itself has a fully automated configuration routine. It detects if PoC is under Git control. If so, it extracts the current version number from the latest Git tag. The installation directory is infered from `$PoCRootDirectory` setup by `PoC.ps1` or `poc.sh`.

```
Configuring PoC
  PoC version: v1.0.1 (found in git)
  Installation directory: D:\git\PoC (found in environment variable)
```

5.4.3 Git

Note: Setting up Git and Git developer settings, is an advanced feature recommended for all developers interrested in providing Git pull requests or patches.

```
Configuring Git
  Git installation directory [C:\Program Files\Git]:
  Install Git mechanisms for PoC developers? [y/N/p]: y
  Install Git filters? [Y/n/p]:
  Installing Git filters...
  Install Git hooks? [Y/n/p]:
  Installing Git hooks...
  Setting 'pre-commit' hook for PoC...
```

5.4.4 Aldec

Configure the installation directory for all Aldec tools.

```
Configuring Aldec
  Are Aldec products installed on your system? [Y/n/p]: Y
  Aldec installation directory [C:\Aldec]:
```

Active-HDL

```
Configuring Aldec Active-HDL
  Is Aldec Active-HDL installed on your system? [Y/n/p]: Y
  Aldec Active-HDL version [10.3]:
  Aldec Active-HDL installation directory [C:\Aldec\Active-HDL]: C:\Aldec\Active-
↪HDL-Student-Edition
```

5.4.5 Altera

Configure the installation directory for all Altera tools.

```
    Configuring Altera
Are Altera products installed on your system? [Y/n/p]: Y
Altera installation directory [C:\Altera]:
```

Quartus

```
Configuring Altera Quartus
  Is Altera Quartus-II or Quartus Prime installed on your system? [Y/n/p]: Y
  Altera Quartus version [15.1]: 16.0
  Altera Quartus installation directory [C:\Altera\16.0\quartus]:
```

ModelSim Altera Edition

```
Configuring ModelSim Altera Edition
  Is ModelSim Altera Edition installed on your system? [Y/n/p]: Y
  ModelSim Altera Edition installation directory [C:\Altera\15.0\modelsim_ae]:␣
↪C:\Altera\16.0\modelsim_ase
```

5.4.6 Lattice

Configure the installation directory for all Lattice Semiconductor tools.

```
Configuring Lattice
  Are Lattice products installed on your system? [Y/n/p]: Y
  Lattice installation directory [D:\Lattice]:
```

Diamond

```
Configuring Lattice Diamond
  Is Lattice Diamond installed on your system? [Y/n/p]: >
  Lattice Diamond version [3.7]:
  Lattice Diamond installation directory [D:\Lattice\Diamond\3.7_x64]:
```

Active-HDL Lattice Edition

```
Configuring Active-HDL Lattice Edition
  Is Aldec Active-HDL installed on your system? [Y/n/p]: Y
  Active-HDL Lattice Edition version [10.2]:
  Active-HDL Lattice Edition installation directory [D:\Lattice\Diamond\3.7_
↪x64\active-hdl]:
```

5.4.7 Mentor Graphics

Configure the installation directory for all mentor Graphics tools.

```
Configuring Mentor
  Are Mentor products installed on your system? [Y/n/p]: Y
  Mentor installation directory [C:\Mentor]:
```

QuestaSim

```
Configuring Mentor QuestaSim
  Is Mentor QuestaSim installed on your system? [Y/n/p]: Y
  Mentor QuestaSim version [10.4d]: 10.4c
  Mentor QuestaSim installation directory [C:\Mentor\QuestaSim\10.4c]:␣
↪C:\Mentor\QuestaSim64\10.4c
```

5.4.8 Xilinx

Configure the installation directory for all Xilinx tools.

```
Configuring Xilinx
  Are Xilinx products installed on your system? [Y/n/p]: Y
  Xilinx installation directory [C:\Xilinx]:
```

ISE

If an Xilinx ISE environment is available and shall be configured in PoC, then answer the following questions:

```
Configuring Xilinx ISE
  Is Xilinx ISE installed on your system? [Y/n/p]: Y
  Xilinx ISE installation directory [C:\Xilinx\14.7\ISE_DS]:
```

Vivado

If an Xilinx ISE environment is available and shall be configured in PoC, then answer the following questions:

```
Configuring Xilinx Vivado
  Is Xilinx Vivado installed on your system? [Y/n/p]: Y
  Xilinx Vivado version [2016.2]:
  Xilinx Vivado installation directory [C:\Xilinx\Vivado\2016.2]:
```

5.4.9 GHDL

```
Configuring GHDL
  Is GHDL installed on your system? [Y/n/p]: Y
  GHDL installation directory [C:\Tools\GHDL\0.34dev]:
```

5.4.10 GTKWave

```
Configuring GTKWave
  Is GTKWave installed on your system? [Y/n/p]: Y
  GTKWave installation directory [C:\Tools\GTKWave\3.3.71]:
```

5.4.11 Hook Files

PoC's wrapper scripts can be customized through pre- and post-hook file. See *Wrapper Script Hook Files* for more details.

5.5 Creating my_config/my_project.vhdl

The PoC-Library needs two VHDL files for its configuration. These files are used to determine the most suitable implementation depending on the provided platform information. These files are also used to select appropiate work arounds.

5.5.1 Create my_config.vhdl

The **my_config.vhdl** file can easily be created from the template file `my_config.vhdl.template` provided by PoC in `PoCRoot\src\common`. (View source on GitHub.) Copy this file into the project's source directory and rename it to `my_config.vhdl`.

This file should be included in version control systems and shared with other systems. `my_config.vhdl` defines three global constants, which need to be adjusted:

```
constant MY_BOARD   : string  := "CHANGE THIS"; -- e.g. Custom, ML505, KC705, Atlys
constant MY_DEVICE  : string  := "CHANGE THIS"; -- e.g. None, XC5VLX50T-1FF1136,␣
↪EP2SGX90FF1508C3
constant MY_VERBOSE : boolean := FALSE;         -- activate report statements in␣
↪VHDL subprograms
```

The easiest way is to define a board name and set `MY_DEVICE` to `None`. So the device name is infered from the board information stored in `PoCRoot\src\common\config.vhdl`. If the requested board is not known to PoC or it's custom made, then set `MY_BOARD` to `Custom` and `MY_DEVICE` to the full FPGA device string.

Example 1: A "Stratix II GX Audio Video Development Kit" board:

```
constant MY_BOARD  : string := "S2GXAV";  -- Stratix II GX Audio Video Development␣
↪Kit
constant MY_DEVICE : string := "None";    -- infer from MY_BOARD
```

Example 2: A custom made Spartan-6 LX45 board:

```
constant MY_BOARD  : string := "Custom";
constant MY_DEVICE : string := "XC6SLX45-3CSG324";
```

5.5.2 Create my_project.vhdl

The **my_project.vhdl** file can also be created from a template file `my_project.vhdl.template` provided by PoC in `PoCRoot\src\common`.

The file should to be copyed into a projects source directory and renamed into `my_project.vhdl`. This file **must not** be included into version control systems – it's private to a computer. `my_project.vhdl` defines two global constants, which need to be adjusted:

```
constant MY_PROJECT_DIR      : string := "CHANGE THIS"; -- e.g. "d:/vhdl/myproject/
↪", "/home/me/projects/myproject/"
constant MY_OPERATING_SYSTEM : string := "CHANGE THIS"; -- e.g. "WINDOWS", "LINUX"
```

Example 1: A Windows System:

```
constant MY_PROJECT_DIR      : string := "D:/git/GitHub/PoC/";
constant MY_OPERATING_SYSTEM : string := "WINDOWS";
```

Example 2: A Debian System:

```
constant MY_PROJECT_DIR      : string := "/home/paebbels/git/GitHub/PoC/";
constant MY_OPERATING_SYSTEM : string := "LINUX";
```

See also:

Running one or more testbenches The installation can be checked by running one or more of PoC's testbenches.

Running one or more netlist generation flows The installation can also be checked by running one or more of PoC's synthesis flows.

5.6 Adding IP Cores to a Project

5.6.1 Manually Addind IP Cores

Adding IP Cores to Altera Quartus

Todo: No documentation available.

Adding IP Cores to Lattice Diamond

Todo: No documentation available.

Adding IP Cores to Xilinx ISE

Todo: No documentation available.

Adding IP Cores to Xilinx Vivado

Todo: No documentation available.

5.7 Simulation

Contents of this Page

5.7.1 Overview

The Python Infrastructure shipped with the PoC-Library can launch manual, half-automated and fully automated testbenches. The testbench can be run in command line or GUI mode. If available, the used simulator is launched with pre-configured waveform files. This can be done by invoking one of PoC's frontend script:

- **poc.sh:** `poc.sh <common options> <simulator> <module> <simulator options>` Use this fronend script on Darwin, Linux and Unix platforms.

- **poc.ps1:** `poc.ps1 <common options> <simulator> <module> <simulator options>` Use this frontend script Windows platforms.

> **Attention:** All Windows command line instructions are intended for Windows PowerShell, if not marked otherwise. So executing the following instructions in Windows Command Prompt (`cmd.exe`) won't function or result in errors!

See also:

PoC Configuration See the Configuration page on how to configure PoC and your installed simulator tool chains. This is required to invoke the simulators.

Supported Simulators See the Intruction page for a list of supported simulators.

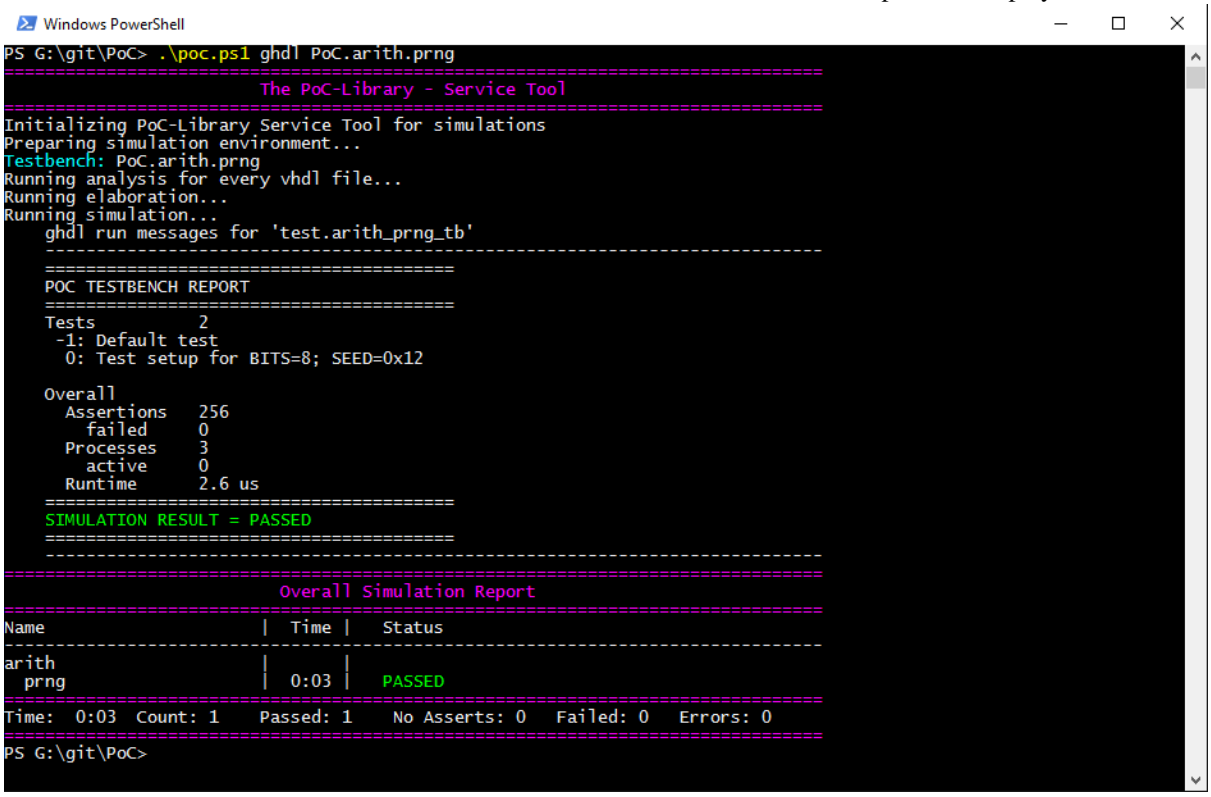
5.7.2 Quick Example

The following quick example uses the GHDL Simulator to analyze, elaborate and simulate a testbench for the module `arith_prng` (Pseudo Random Number Generator - PRNG). The VHDL file `arith_prng.vhdl` is located at `PoCRoot\src\arith` and virtually a member in the *PoC.arith* namespace. So the module can be identified by an unique name: `PoC.arith.prng`, which is passed to the frontend script.

Example 1:

```
cd PoCRoot
.\poc.ps1 ghdl PoC.arith.prng
```

The CLI command `ghdl` chooses *GHDL Simulator* as the simulator and passes the fully qualified PoC entity name `PoC.arith.prng` as a parameter to the tool. All required source file are gathered and compiled to an executable. Afterwards this executable is launched in CLI mode and it's outputs are displayed in console:



Each testbench uses PoC's simulation helper packages to count asserts and to track active stimuli and checker processes. After a completed simulation run, an report is written to STDOUT or the simulator's console. Note the

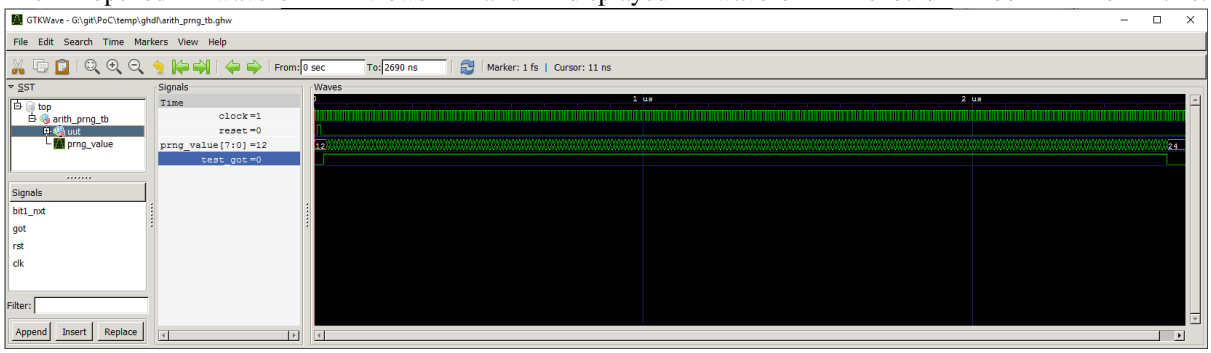
line `SIMULATION RESULT = PASSED`. For each simulated PoC entity, a line in the overall report is created. It lists the runtime per testbench and the simulation status (`... ERROR`, `FAILED`, `NO ASSERTS` or `PASSED`).

Example 2:

Passing an additional option `--gui` to the service tool, opens the testbench in GUI-mode. If a waveform configuration file is present (e.g. a `*.gtkw` file for GTKWave), then it is preloaded into the simulator's waveform viewer.

```
cd PoCRoot
.\poc.ps1 ghdl PoC.arith.prng --gui
```

The opened waveform viewer and displayed waveform should look like this:



5.7.3 Vendor Specific Testbenches

PoC is shipped with a set of well known FPGA development boards. This set is extended by a list of generic boards, named after each supported FPGA vendor. These generic boards can be used in simulations to select a representative FPGA of a supported device vendor. If no board or device name is passed to a testbench run, the `GENERIC` board is chosen.

Board Name	Target Board	Target Device
GENERIC	GENERIC	GENERIC
Altera	DE4	Stratix-IV 230
Lattice	ECP5Versa	ECP5-45UM
Xilinx	KC705	Kintex-7 325T

A vendor specific testbench can be launched by passing either `--board=xxx` or `--device=yyy` as an additional parameter to the PoC scripts.

```
# Example 1 - A Lattice board
.\poc.ps1 ghdl PoC.arith.prng --board=Lattice
# Example 2 - A Altera Stratix IV board
.\poc.ps1 ghdl PoC.arith.prng --board=DE4
# Example 3 - A Xilinx Kintex-7 325T device
.\poc.ps1 ghdl PoC.arith.prng --device=XC7K325T-2FFG900
```

Note: Running vendor specific testbenches may require pre-compiled vendor libraries. Some simulators are shipped with diverse pre-compiled libraries, others include scripts or user guides to pre-compile them on the target system.

PoC is shipped with a set of pre-compile scripts to offer a unified interface and common storage for all supported vendor's pre-compile procedures. See *Pre-Compiling Vendor Libraries*.

5.7.4 Running a Single Testbench

A testbench run is supervised by PoC's `PoCRoot\py\PoC.py` service tool, which offers a consistent interface to all simulators. Unfortunately, every platform has it's specialties, so a wrapper script is needed as abstraction from the host's operating system. Depending on the choosen tool chain, the wrapper script will source or invoke the vendor tool's environment scripts to pre-load the needed environment variables, paths or license file settings.

The order of options to the frontend script is as following: `<common options> <simulator> <module> <simulator options>`

The frontend offers several common options:

Common Option		Description
-q	–quiet	Quiet-mode (print nothing)
-v	–verbose	Print more messages
-d	–debug	Debug mode (print everything)
	–dryrun	Run in dry-run mode

One of the following supported simulators can be choosen, if installed and configured in PoC:

Simulator	Description
asim	Active-HDL Simulator
cocotb	Cocotb simulation using QuestaSim Simulator
ghdl	GHDL Simulator
isim	Xilinx ISE Simulator
vsim	QuestaSim Simulator or ModelSim
xsim	Xilinx Vivado Simulator

A testbench run can be interrupted by sending a keyboard interrupt to Python. On most operating systems this is done by pressing `Ctrl + C`. If PoC runs multiple testbenches at once, all finished testbenches are reported with there testbench result. The aborted testbench will be listed as errored.

Aldec Active-HDL

The command to invoke a simulation using Active-HDL is `asim` followed by a list of PoC entities. The following options are supported for Active-HDL:

Simulator Option		Description
	–board=<BOARD>	Specify a target board.
	–device=<DEVICE>	Specify a target device.
	–std=[87|93|02|08]	Select a VHDL standard. Default: 08

Note: GUI mode for Active-HDL is not yet supported.

Example:

```
cd PoCRoot
.\poc.ps1 asim PoC.arith.prng --std=93
```

Cocotb with QuestaSim backend

The command to invoke a Cocotb simulation using QuestaSim is `cocotb` followed by a list of PoC entities. The following options are supported for Cocotb:

Simulator Option		Description
	–board=<BOARD>	Specify a target board.
	–device=<DEVICE>	Specify a target device.
-g	–gui	Start the simulation in the QuestaSim GUI.

Note: Cocotb is currently only on Linux with QuestaSim supported. We are working to support the Windows platform and the GHDL backend.

Example:

```
cd PoCRoot
.\poc.ps1 cocotb PoC.cache.par
```

GHDL (plus GTKwave)

The command to invoke a simulation using GHDL is `ghdl` followed by a list of PoC entities. The following options are supported for GHDL:

Simulator Option		Description
	–board=<BOARD>	Specify a target board.
	–device=<DEVICE>	Specify a target device.
-g	–gui	Start GTKwave, if installed. Open *.gtkw, if available.
	–std=[87|93|02|08]	Select a VHDL standard. Default: 08

Example:

```
cd PoCRoot
.\poc.ps1 ghdl PoC.arith.prng --board=Atlys -g
```

Mentor Graphics QuestaSim

The command to invoke a simulation using QuestaSim or ModelSim is `vsim` followed by a list of PoC entities. The following options are supported for QuestaSim:

Simulator Option		Description
	–board=<BOARD>	Specify a target board.
	–device=<DEVICE>	Specify a target device.
-g	–gui	Start the simulation in the QuestaSim GUI.
	–std=[87|93|02|08]	Select a VHDL standard. Default: 08

Example:

```
cd PoCRoot
.\poc.ps1 vsim PoC.arith.prng --board=DE4 --gui
```

If QuestaSim is started in GUI mode (`--gui`), PoC will provide several Tcl files (`*.do`) in the simulator's working directory to recompile, restart or rerun the current simulation. The rerun command is based on the saved IP core's run script, which may default to `run -all`.

Tcl Script	Performed Tasks
`recompile.do`	recompile and restart
`relaunch.do`	recompile, restart and rerun
`saveWaveform.do`	save the current waveform viewer settings

Xilinx ISE Simulator

The command to invoke a simulation using ISE Simulator (isim) is `isim` followed by a list of PoC entities. The following options are supported for ISE Simulator:

Simulator Option		Description
	–board=<BOARD>	Specify a target board.
	–device=<DEVICE>	Specify a target device.
-g	–gui	Start the simulation in the ISE Simulator GUI (iSim).

Example:

```
cd PoCRoot
.\poc.ps1 isim PoC.arith.prng --board=Atlys -g
```

Xilinx Vivado Simulator

The command to invoke a simulation using Vivado Simulator (isim) is `xsim` followed by a list of PoC entities. The following options are supported for Vivado Simulator:

Simulator Option		Description
	–board=<BOARD>	Specify a target board.
	–device=<DEVICE>	Specify a target device.
-g	–gui	Start Vivado in simulation mode.
	–std=[93|08]	Select a VHDL standard. Default: 93

Example:

```
cd PoCRoot
.\poc.ps1 xsim PoC.arith.prng --board=Atlys -g
```

5.7.5 Running a Group of Testbenches

Each simulator can be invoked with a space seperated list of PoC entiries or a wildcard at the end of the fully qualified entity name.

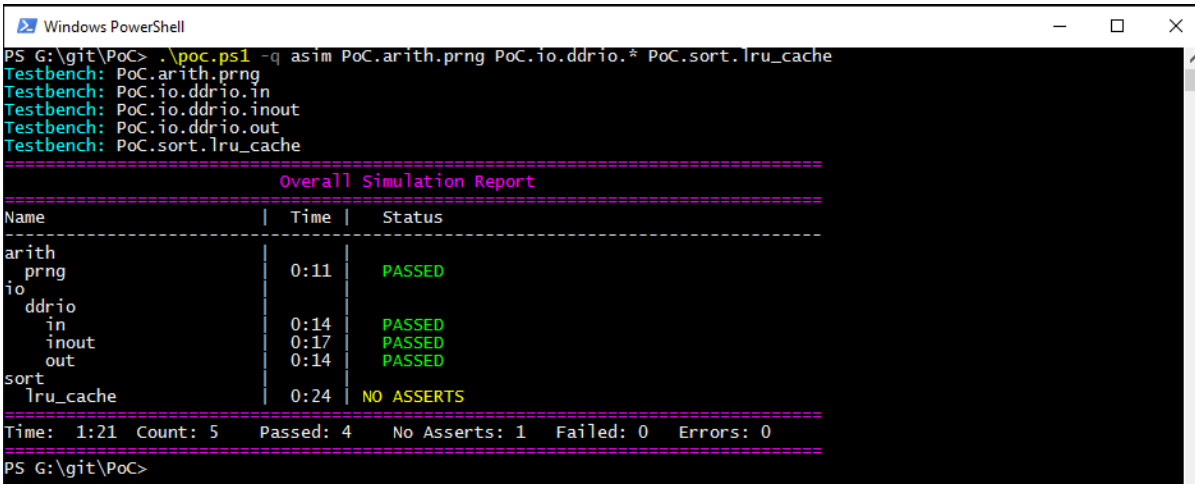
Supported wildcard patterns are `*` and `?`. Question mark refers to all entities in a PoC (sub-)namespace. Asterisk refers to all PoC entiries in the current namespace and all sub-namespaces.

Examples for testbenches groups:

PoC entity list	Description
PoC.arith.prng	A single PoC entity: `arith_prng`
PoC.*	All entities in the whole library
PoC.io.ddrio.?	All entities in `PoC.io.ddrio`: `ddrio_in`, `ddrio_inout`, `ddrio_out`
PoC.fifo.* PoC.cache.* PoC.dstruct.*	All FIFO, cache and data-structure testbenches.

```
cd PoCRoot
.\poc.ps1 -q asim PoC.arith.prng PoC.io.ddrio.* PoC.sort.lru_cache
```

Resulting output:

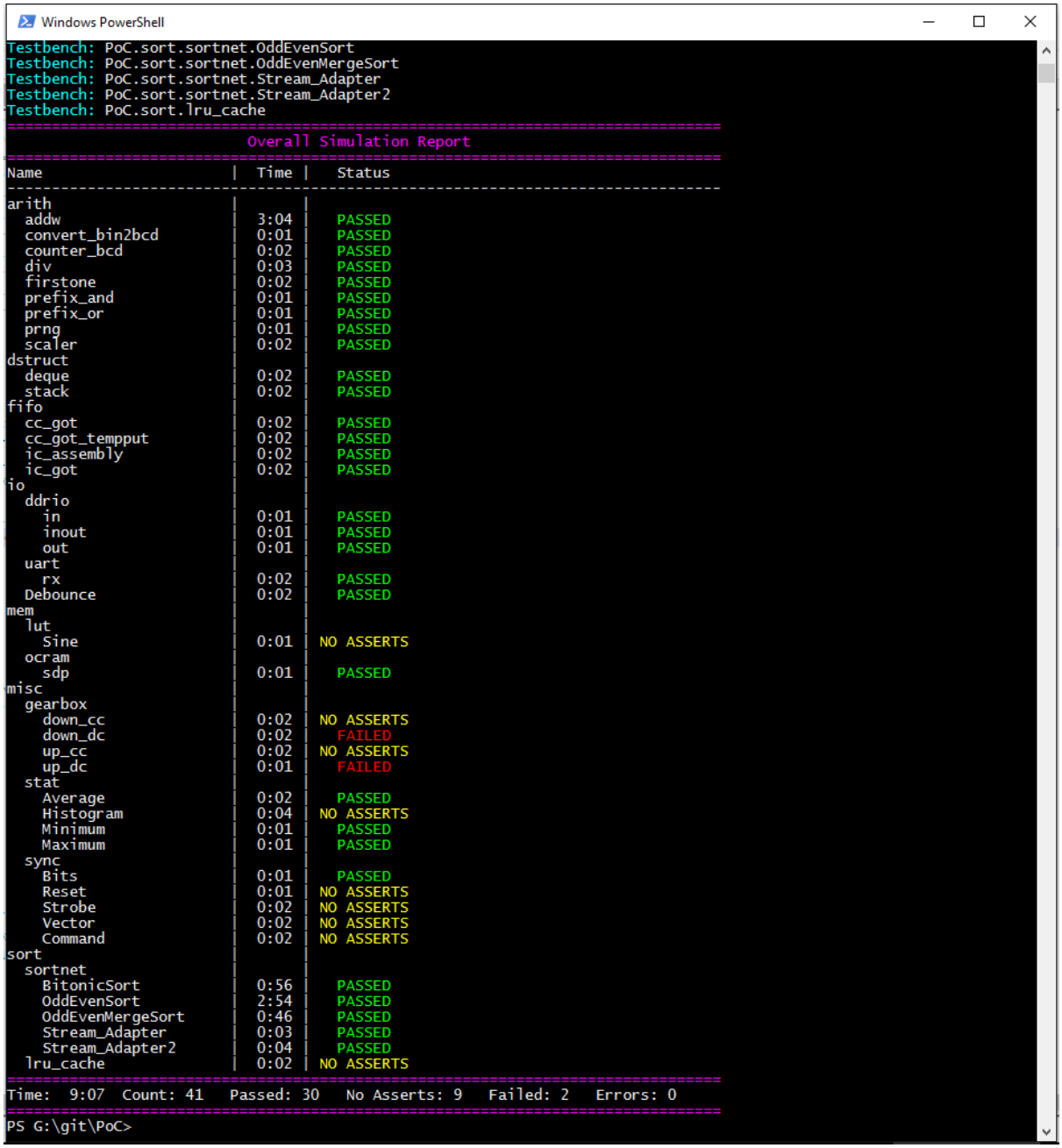


5.7.6 Continuous Integration (CI)

All PoC testbenches are executed on every GitHub upload (push) via Travis-CI. The testsuite runs all testbenches for the virtual board `GENERIC` with an FPGA device called `GENERIC`. We can't run vendor dependent testbenches, because we can't upload the vendor simulation libraries to Travis-CI.

To reproduce the Travis-CI results on a local machine, run the following command. The `-q` option, launches the frontend in quiet mode to reduce the command line messages:

```
cd PoCRoot
.\poc.ps1 -q ghdl PoC.*
```



If the vendor libraries are available and pre-compiled, then it's also possible to run a CI flow for a specific vendor. This is an Altera example for the Terrasic DE4 board:

```
cd PoCRoot
.\poc.ps1 -q vsim PoC.* --board=DE4
```

See also:

PoC Configuration See the Configuration page on how to configure PoC and your installed simulator tool chains. This is required to invoke the simulators.

Latest Travis-CI Report Browse the list of branches at Travis-CI.org.

5.8 Synthesis

Contents of this Page

5.8.1 Overview

The Python infrastructure shipped with the PoC-Library can launch manual, half-automated and fully automated synthesis runs. This can be done by invoking one of PoC's frontend script:

- **poc.sh:** `poc.sh <common options> <compiler> <module> <compiler options>` Use this fronend script on Darwin, Linux and Unix platforms.
- **poc.ps1:** `poc.ps1 <common options> <compiler> <module> <compiler options>` Use this frontend script Windows platforms.

> **Attention:** All Windows command line instructions are intended for Windows PowerShell, if not marked otherwise. So executing the following instructions in Windows Command Prompt (`cmd.exe`) won't function or result in errors!

See also:

PoC Configuration See the Configuration page on how to configure PoC and your installed synthesis tool chains. This is required to invoke the compilers.

Supported Compiler See the Intruction page for a list of supported compilers.

See also:

List of Supported FPGA Devices See this list to find a supported and well known target device.

List of Supported Development Boards See this list to find a supported and well known development board.

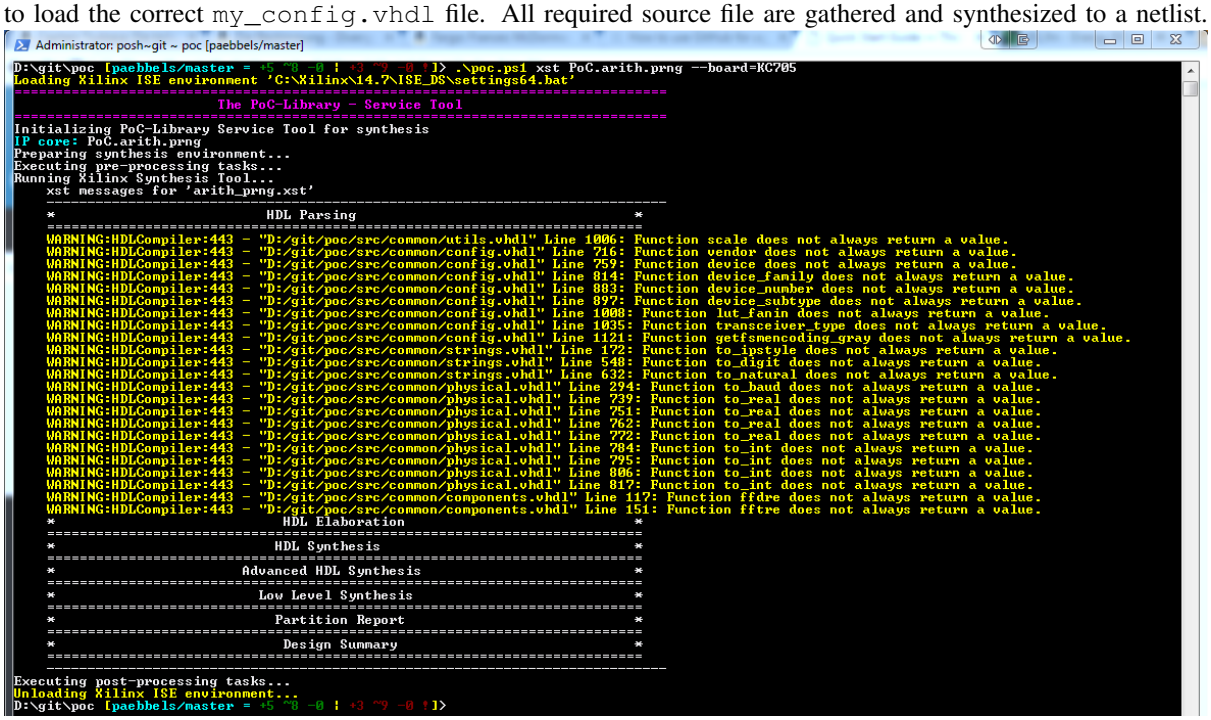
5.8.2 Quick Example

The following quick example uses the Xilinx Systesis Tool (XST) to synthesize a netlist for IP core `arith_prng` (Pseudo Random Number Generator - PRNG). The VHDL file `arith_prng.vhdl` is located at `PoCRoot\src\arith` and virtually a member in the *PoC.arith* namespace. So the module can be identified by an unique name: `PoC.arith.prng`, which is passed to the frontend script.

Example 1:

```
cd PoCRoot
.\poc.ps1 xst PoC.arith.prng --board=KC705
```

The CLI command `xst` chooses *Xilinx Synthesis Tool* as the synthesizer and passes the fully qualified PoC entity name `PoC.arith.prng` as a parameter to the tool. Additionally, the development board name is required to load the correct `my_config.vhdl` file. All required source file are gathered and synthesized to a netlist.



5.8.3 Running a single Synthesis

A synthesis run is supervised by PoC's *PoCRoot\py\PoC.py* service tool, which offers a consistent interface to all synthesizers. Unfortunately, every platform has it's specialties, so a wrapper script is needed as abstraction from the host's operating system. Depending on the choosen tool chain, the wrapper script will source or invoke the vendor tool's environment scripts to pre-load the needed environment variables, paths or license file settings.

The order of options to the frontend script is as following: `<common options> <synthesizer> <module> [<module>] <synthesizer options>`

The frontend offers several common options:

Common Option		Description
`-q`	`--quiet`	Quiet-mode (print nothing)
`-v`	`--verbose`	Print more messages
`-d`	`--debug`	Debug mode (print everything)
	`--dryrun`	Run in dry-run mode

One of the following supported synthesizers can be choosen, if installed and configured in PoC:

Synthesizer	Command Reference
Altera Quartus II or Intel Quartus Prime	PoC.py quartus
Lattice (Diamond) Synthesis Engine (LSE)	PoC.py lse
Xilinx ISE Systhesis Tool (XST)	PoC.py xst
Xilinx ISE Core Generator (CoreGen)	PoC.py coregen
Xilinx Vivado Synthesis	PoC.py vivado

Altera / Intel Quartus

The command to invoke a synthesis using Altera Quartus II or Intel Quartus Prime is quartus followed by a list of PoC entities. The following options are supported for Quartus:

Simulator Option		Description
	`--board=<Board>`	Specify a target board.
	`--device=<Device>`	Specify a target device.

Example:

```
cd PoCRoot
.\poc.ps1 quartus PoC.arith.prng --board=DE4
```

Lattice Diamond

The command to invoke a synthesis using Lattice Diamond is lse followed by a list of PoC entities. The following options are supported for the Lattice Synthesis Engine (LSE):

Simulator Option		Description
	`--board=<Board>`	Specify a target board.
	`--device=<Device>`	Specify a target device.

Example:

```
cd PoCRoot
.\poc.ps1 lse PoC.arith.prng --board=ECP5Versa
```

Xilinx ISE Synthesis Tool (XST)

The command to invoke a synthesis using Xilinx ISE Synthesis is xst followed by a list of PoC entities. The following options are supported for the Xilinx Synthesis Tool (XST):

Simulator Option		Description
	`--board=<Board>`	Specify a target board.
	`--device=<Device>`	Specify a target device.

Example:

```
cd PoCRoot
.\poc.ps1 xst PoC.arith.prng --board=KC705
```

Xilinx ISE Core Generator

The command to invoke an IP core generation using Xilinx Core Generator is coregen followed by a list of PoC entities. The following options are supported for Core Generator (CG):

Simulator Option		Description
	`--board=<Board>`	Specify a target board.
	`--device=<Device>`	Specify a target device.

Example:

```
cd PoCRoot
.\poc.ps1 coregen PoC.xil.mig.Atlys_1x128 --board=Atlys
```

Xilinx Vivado Synthesis

The command to invoke a synthesis using Xilinx Vivado Synthesis is vivado followed by a list of PoC entities. The following options are supported for Vivado Synthesis (Synth):

Simulator Option		Description
	`--board=<Board>`	Specify a target board.
	`--device=<Device>`	Specify a target device.

Example:

```
cd PoCRoot
.\poc.ps1 vivado PoC.arith.prng --board=KC705
```

5.9 Project Management

5.9.1 Overview

5.9.2 Solutions

5.9.3 Projects

5.10 Pre-Compiling Vendor Libraries

Contents of this Page

5.10.1 Overview

Running vendor specific testbenches may require pre-compiled vendor libraries. Some vendors ship their simulators with diverse pre-compiled libraries, but these don't include primitive libraries from hardware vendors. More over, many auxillary libraries are outdated. Hardware vendors ship their tool chains with pre-compile scripts or user guides to pre-compile the primitive libraries for a list of supported simulators on a target system.

PoC is shipped with a set of pre-compile scripts to offer a unified interface and common storage for all supported vendor's pre-compile procedures. The scripts are located in `\tools\precompile\` and the output is stored in `\temp\precompiled\<Simulator>\<Library>`.

5.10.2 Supported Simulators

The current set of pre-compile scripts support these simulators:

Vendor	Simulator and Edition	Altera	Lattice	Xilinx (ISE)	Xilinx (Vivado)
20. Gingold	GHDL with `--std=93c` GHDL with `--std=08`	yes yes	yes yes	yes yes	yes yes
Aldec	Active-HDL (or Stududent Ed.) Active-HDL Lattice Ed. Reviera-PRO	planned planned planned	planned shipped planned	planned planned planned	planned planned planned
Mentor	ModelSim PE (or Stududent Ed.) ModelSim SE ModelSim Altera Ed. QuestaSim	yes yes shipped yes	yes yes yes yes	yes yes yes yes	yes yes yes yes
Xilinx	ISE Simulator Vivado Simulator			shipped not supported	not supported shipped

5.10.3 FPGA Vendor's Primitive Libraries

Altera

Note: The Altera Quartus tool chain needs to be configured in PoC. See *Configuring PoC's Infrastruture* for further details.

On Linux

```
# Example 1 - Compile for all Simulators
./tools/precompile/compile-altera.sh --all
# Example 2 - Compile only for GHDL and VHDL-2008
./tools/precompile/compile-altera.sh --ghdl --vhdl2008
```

List of command line arguments:

Common Option		Parameter Description
`-h`	*`--help`*	Print embedded help page(s).
`-c`	*`--clean`*	Clean-up directories.
`-a`	*`--all`*	Compile for all simulators.
	`--ghdl`	Compile for GHDL.
	`--questa`	Compile for QuestaSim.
	`--vhdl93`	GHDL only: Compile only for VHDL-93.
	`--vhdl2008`	GHDL only: Compile only for VHDL-2008.

On Windows

```
# Example 1 - Compile for all Simulators
.\tools\precompile\compile-altera.ps1 -All
# Example 2 - Compile only for GHDL and VHDL-2008
.\tools\precompile\compile-altera.ps1 -GHDL -VHDL2008
```

List of command line arguments:

Common Option		Parameter Description
`-h`	*`-Help`*	Print embedded help page(s).
`-c`	*`-Clean`*	Clean-up directories.
`-a`	*`-All`*	Compile for all simulators.
	`-GHDL`	Compile for GHDL.
	`-Questa`	Compile for QuestaSim.
	`-VHDL93`	GHDL only: Compile only for VHDL-93.
	`-VHDL2008`	GHDL only: Compile only for VHDL-2008.

Lattice

Note: The Lattice Diamond tool chain needs to be configured in PoC. See *Configuring PoC's Infrastruture* for further details.

On Linux

```
# Example 1 - Compile for all Simulators
./tools/precompile/compile-lattice.sh --all
# Example 2 - Compile only for GHDL and VHDL-2008
./tools/precompile/compile-lattice.sh --ghdl --vhdl2008
```

List of command line arguments:

Common Option		Parameter Description
`-h`	*`--help`*	Print embedded help page(s).
`-c`	*`--clean`*	Clean-up directories.
`-a`	*`--all`*	Compile for all simulators.
	`--ghdl`	Compile for GHDL.
	`--questa`	Compile for QuestaSim.
	`--vhdl93`	GHDL only: Compile only for VHDL-93.
	`--vhdl2008`	GHDL only: Compile only for VHDL-2008.

On Windows

```
# Example 1 - Compile for all Simulators
.\tools\precompile\compile-lattice.ps1 -All
# Example 2 - Compile only for GHDL and VHDL-2008
.\tools\precompile\compile-lattice.ps1 -GHDL -VHDL2008
```

List of command line arguments:

Common Option		Parameter Description
`-h`	*`-Help`*	Print embedded help page(s).
`-c`	*`-Clean`*	Clean-up directories.
`-a`	*`-All`*	Compile for all simulators.
	`-GHDL`	Compile for GHDL.
	`-Questa`	Compile for QuestaSim.
	`-VHDL93`	GHDL only: Compile only for VHDL-93.
	`-VHDL2008`	GHDL only: Compile only for VHDL-2008.

Xilinx ISE

Note: The Xilinx ISE tool chain needs to be configured in PoC. See *Configuring PoC's Infrastruture* for further details.

On Linux

```
# Example 1 - Compile for all Simulators
./tools/precompile/compile-xilinx-ise.sh --all
# Example 2 - Compile only for GHDL and VHDL-2008
./tools/precompile/compile-xilinx-ise.sh --ghdl --vhdl2008
```

List of command line arguments:

Common Option		Parameter Description
`-h`	*`--help`*	Print embedded help page(s).
`-c`	*`--clean`*	Clean-up directories.
`-a`	*`--all`*	Compile for all simulators.
	`--ghdl`	Compile for GHDL.
	`--questa`	Compile for QuestaSim.
	`--vhdl93`	GHDL only: Compile only for VHDL-93.
	`--vhdl2008`	GHDL only: Compile only for VHDL-2008.

On Windows

```
# Example 1 - Compile for all Simulators
.\tools\precompile\compile-xilinx-ise.ps1 -All
# Example 2 - Compile only for GHDL and VHDL-2008
.\tools\precompile\compile-xilinx-ise.ps1 -GHDL -VHDL2008
```

List of command line arguments:

Common Option		Parameter Description
-h	*-Help*	Print embedded help page(s).
-c	*-Clean*	Clean-up directories.
-a	*-All*	Compile for all simulators.
	-GHDL	Compile for GHDL.
	-Questa	Compile for QuestaSim.
	-VHDL93	GHDL only: Compile only for VHDL-93.
	-VHDL2008	GHDL only: Compile only for VHDL-2008.

Xilinx Vivado

Note: The Xilinx Vivado tool chain needs to be configured in PoC. See *Configuring PoC's Infrastruture* for further details.

On Linux

```
# Example 1 - Compile for all Simulators
./tools/precompile/compile-xilinx-vivado.sh --all
# Example 2 - Compile only for GHDL and VHDL-2008
./tools/precompile/compile-xilinx-vivado.sh --ghdl --vhdl2008
```

List of command line arguments:

Common Option		Parameter Description
-h	*--help*	Print embedded help page(s).
-c	*--clean*	Clean-up directories.
-a	*--all*	Compile for all simulators.
	--ghdl	Compile for GHDL.
	--questa	Compile for QuestaSim.
	--vhdl93	GHDL only: Compile only for VHDL-93.
	--vhdl2008	GHDL only: Compile only for VHDL-2008.

On Windows

```
# Example 1 - Compile for all Simulators
.\tools\precompile\compile-xilinx-vivado.ps1 -All
# Example 2 - Compile only for GHDL and VHDL-2008
.\tools\precompile\compile-xilinx-vivado.ps1 -GHDL -VHDL2008
```

List of command line arguments:

Common Option		Parameter Description
-h	*-Help*	Print embedded help page(s).
-c	*-Clean*	Clean-up directories.
-a	*-All*	Compile for all simulators.
	-GHDL	Compile for GHDL.
	-Questa	Compile for QuestaSim.
	-VHDL93	GHDL only: Compile only for VHDL-93.
	-VHDL2008	GHDL only: Compile only for VHDL-2008.

5.10.4 Third-Party Libraries

OSVVM

On Linux

```
# Example 1 - Compile for all Simulators
./tools/precompile/compile-osvvm.sh --all
# Example 2 - Compile only for GHDL
./tools/precompile/compile-osvvm.sh --ghdl
```

List of command line arguments:

Common Option		Parameter Description
-h	*--help*	Print embedded help page(s).
-c	*--clean*	Clean-up directories.
-a	*--all*	Compile for all simulators.
	--ghdl	Compile for GHDL.
	--questa	Compile for QuestaSim.

On Windows

```
# Example 1 - Compile for all Simulators
.\tools\precompile\compile-osvvm.ps1 -All
# Example 2 - Compile only for GHDL
.\tools\precompile\compile-osvvm.ps1 -GHDL
```

List of command line arguments:

Common Option		Parameter Description
-h	*-Help*	Print embedded help page(s).
-c	*-Clean*	Clean-up directories.
-a	*-All*	Compile for all simulators.
	-GHDL	Compile for GHDL.
	-Questa	Compile for QuestaSim.

UVVM

On Linux

```
# Example 1 - Compile for all Simulators
./tools/precompile/compile-uvvm.sh --all
# Example 2 - Compile only for GHDL
./tools/precompile/compile-uvvm.sh --ghdl
```

List of command line arguments:

Common Option		Parameter Description
-h	*--help*	Print embedded help page(s).
-c	*--clean*	Clean-up directories.
-a	*--all*	Compile for all simulators.
	--ghdl	Compile for GHDL.
	--questa	Compile for QuestaSim.

On Windows

```
# Example 1 - Compile for all Simulators
.\tools\precompile\compile-uvvm.ps1 -All
# Example 2 - Compile only for GHDL
.\tools\precompile\compile-uvvm.ps1 -GHDL
```

List of command line arguments:

Common Option		Parameter Description
`-h`	*`-Help`*	Print embedded help page(s).
`-c`	*`-Clean`*	Clean-up directories.
`-a`	*`-All`*	Compile for all simulators.
	`-GHDL`	Compile for GHDL.
	`-Questa`	Compile for QuestaSim.

5.10.5 Simulator Adapters

Cocotb

On Linux

Attention: This is an experimental compile script.

```
# Example 1 - Compile for all Simulators
./tools/precompile/compile-cocotb.sh --all
# Example 2 - Compile only for GHDL
./tools/precompile/compile-cocotb.sh --ghdl
```

List of command line arguments:

Common Option		Parameter Description
`-h`	`--help`	Print embedded help page(s).
`-c`	`--clean`	Clean-up directories.
`-a`	`--all`	Compile for all simulators.
	`--ghdl`	Compile for GHDL.
	`--questa`	Compile for QuestaSim.

On Windows

Attention: This is an experimental compile script.

```
# Example 1 - Compile for all Simulators
.\tools\precompile\compile-cocotb.ps1 -All
# Example 2 - Compile only for GHDL
.\tools\precompile\compile-cocotb.ps1 -GHDL
```

List of command line arguments:

Common Option		Parameter Description
`-h`	`-Help`	Print embedded help page(s).
`-c`	`-Clean`	Clean-up directories.
`-a`	`-All`	Compile for all simulators.
	`-GHDL`	Compile for GHDL.
	`-Questa`	Compile for QuestaSim.

5.11 Miscellaneous

The directory `PoCRoot\tools\` contains several tools and addons to ease the work with the PoC-Library and VHDL.

5.11.1 GNU Emacs

Todo: No documentation available.

5.11.2 Git

- `git-alias.setup.ps1`/`git-alias.setup.sh` registers new global aliasses in Git
  - `git tree` - Prints the colored commit tree into the console
  - `git treea` - Prints the colored commit tree into the console

```
git config --global alias.tree 'log --decorate --pretty=oneline --abbrev-
↪commit --date-order --graph'
git config --global alias.tree 'log --decorate --pretty=oneline --abbrev-
↪commit --date-order --graph --all'
```

Browse the Git directory.

5.11.3 Notepad++

The PoC-Library is shipped with syntax highlighting rules for Notepad++. The following additional file types are supported:

- PoC Configuration Files (*.ini)
- PoC *.Files Files (*.files)
- PoC *.Rules Files (*.rules)
- Xilinx User Constraint Files (*.ucf): `Syntax Highlighting - Xilinx UCF`

Browse the Notepad++ directory.

CHAPTER 6

IP Core Interfaces

PoC defines a set of on-chip interfaces described in the next sections.

6.1 Command-Status-Error (PoC.CSE) Interface

Todo: Define the PoC.CSE (Command-Status-Error) interface used in ...

6.2 PoC.FIFO Interface

Todo: Define the PoC.FIFO interface (writer and reader) used in `PoC.fifo.*` ...

6.3 PoC.Mem Interface

PoC.Mem is a single-cycle, pipelined memory interface used by various memory controllers and related components like caches. Memory accesses are always word aligned, and during writes a mask defines which bytes are actually written to the memory (if supported by the memory controller).

6.3.1 Configuration

Each entity may have an individual configuration, especially if it has two PoC.Mem interfaces or if it adapts between PoC.Mem and another interface.

The typical configuration parameters are:

Parameter	Description
ADDR_BITS or A_BITS	Number of address bits. Each address identifies exactly one memory word.
DATA_BITS or D_BITS	Size of a memory word in bits. DATA_BITS must be divisible by 8.

A memory word consists of DATA_BITS/8 bytes.

Individual bytes are only addressed during writes by the write mask. The write mask has one mask-bit for each byte in a memory word.

For example, a 1 KiByte memory with a 32-bit datapath has the following configuration:

- 4 bytes per memory word,
- ADDR_BITS=8 because $\log_2(1\,\text{KiByte}/4\,\text{bytes}) = 8$, and
- DATA_BITS=32 which is the datapath size in bits.

6.3.2 Interface signals

The following signal names are typically prefixed in the port list of a concrete entity to separate the PoC.Mem interface from other interfaces of the entity. Moreover, clock and reset may be shared with other interfaces of the entity.

The PoC.Mem interface consists of the following signals:

Signal	Description
clk	The clock. All other signals are synchronous to the rising edge of this clock.
rst	High-active synchronous reset.
rdy	High-active ready for request.
req	High-active request.
write	'1' if write request, '0' if read request
addr	The (word) address.
wdata	The data to be written to the memory.
wmask (optional)	Write-mask, for each byte: '0' = write byte, '1' = mask byte from write. Signal/port is omitted if write mask is not supported.
rstb	High-active read-strobe.
rdata	The read-data returned from the memory.

The interface is actually splitted into two parts:

- the request part: signals `rdy`, `req`, `write`, `addr`, `wdata` and `wmask`, and
- the read-reply part: signals `rstb` and `rdata`.

6.3.3 Operation

The request and the read-reply part operate indepent of each other to support pipelined reading from memory. The pipeline depth is defined by the actual memory controller. If a user application does support only a specific number of outstanding reads, then the application must limit the number of issued reads on its own.

Requests

If `req` is low, then no request is issued to the memory in the current clock cycle. The state of the signals `write`, `addr`, `wdata` and `wmask` doesn't care.

If `req` is high, then a request is issued to the memory in the current clock cycle as given by `write`, `addr`, `wdata` and `wmask`. The request will be accepted by the memory, if `rdy` is high in the same clock cycle, otherwise the request will be ignored. `wdata` and `wmask` doesn't care if a read request is issued.

`rdy` does not depend on `req` in the current clock cycle. `rdy` may go low in the following clock cycle after a request has been issued or a synchronous reset has been applied.

Read Replies

If `rstb` is high in the current clock cycle, then `rdata` delivers the requested read data (read reply). Otherwise, if `rstb` is low, then `rdata` is unknown. The user application has to immediatly handle the incoming read data, because it cannot signal ready or acknowledge.

After issuing a read request, the memory responds with a read reply in the following clock cycle (i.e. synchronous read) or any later clock cycle depending on the pipeline depth. For each read request, a read reply is generated. Read requests are not reordered.

6.4 PoC.Stream Interface

Todo: Define the PoC.Stream interface used in PoC.net.* and `PoC.bus.stream.*` ...

CHAPTER 7

IP Core Documentations

Namespace for Packages:

7.1 Common Packages

These are common packages....

7.1.1 components

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7.1.2 context

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7.1.3 config

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7.1.4 fileio

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7.1.5 math

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7.1.6 strings

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7.1.7 utils

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7.1.8 vectors

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7.2 Simulation Packages

7.2.1 sim_types

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7.2.2 sim_global (VHDL-93)

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7.2.3 sim_global (VHDL-2008)

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7.2.4 sim_unprotected (VHDL-93)

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7.2.5 sim_protected (VHDL-2008)

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7.2.6 simulation (VHDL-93)

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7.2.7 simulation (VHDL-2008)

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7.2.8 sim_waveform

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Namespaces for Entities:

7.3 PoC.alt

Todo: This namespace is reserved for Altera specific entities.

7.4 PoC.arith

These are arithmetic entities. . . .

Package

PoC.arith Package

Entities

- *PoC.arith.addw*
- *PoC.arith.carrychain_inc*
- *PoC.arith.convert_bin2bcd*
- *PoC.arith.counter_bcd*
- *PoC.arith.counter_free*
- *PoC.arith.counter_gray*
- *PoC.arith.counter_ring*
- *PoC.arith.div*
- *PoC.arith.firstone*
- *PoC.arith.muls_wide*
- *PoC.arith.prefix_and*
- *PoC.arith.prefix_or*
- *PoC.arith.prng*
- *PoC.arith.same*
- *PoC.arith.scaler*
- *PoC.arith.shifter_barrel*
- *PoC.arith.sqrt*

7.4.1 PoC.arith Package

This package holds all component declarations for this namespace.

Exported Enumerations

- `tArch`
- `tBlocking`
- `tSkipping`

Exported Functions

- `arith_div_latency`

Exported Components

- *PoC.arith.addw*
- PoC.arith.carrychain_inc_xilinx
- *PoC.arith.counter_bcd*
- *PoC.arith.counter_gray*
- *PoC.arith.div*
- *PoC.arith.firstone*
- PoC.arith.inc_ovcy_xilinx
- *PoC.arith.muls_wide*
- PoC.arith.prefix_and_xilinx
- PoC.arith.prefix_or_xilinx
- *PoC.arith.prng*
- *PoC.arith.same*
- *PoC.arith.sqrt*

Source file: arith.pkg.vhdl

7.4.2 PoC.arith.addw

Implements wide addition providing several options all based on an adaptation of a carry-select approach.

References:

- Hong Diep Nguyen and Bogdan Pasca and Thomas B. Preusser: FPGA-Specific Arithmetic Optimizations of Short-Latency Adders, FPL 2011. -> ARCH: AAM, CAI, CCA -> SKIPPING: CCC
- Marcin Rogawski, Kris Gaj and Ekawat Homsirikamol: A Novel Modular Adder for One Thousand Bits and More Using Fast Carry Chains of Modern FPGAs, FPL 2014. -> ARCH: PAI -> SKIPPING: PPN_KS, PPN_BK

Entity Declaration:

```
entity arith_addw is
  generic (
    N : positive;                    -- Operand Width
    K : positive;                    -- Block Count

    ARCH        : tArch     := AAM;        -- Architecture
    BLOCKING    : tBlocking := DFLT;       -- Blocking Scheme
    SKIPPING    : tSkipping := CCC;        -- Carry Skip Scheme
    P_INCLUSIVE : boolean   := false       -- Use Inclusive Propagate, i.e. c^1
  );
  port (
    a, b : in std_logic_vector(N-1 downto 0);
    cin  : in std_logic;

    s    : out std_logic_vector(N-1 downto 0);
    cout : out std_logic
  );
end entity;
```

Source file: arith/arith_addw.vhdl

7.4.3 PoC.arith.carrychain_inc

This is a generic carry-chain abstraction for increment by one operations.

Y <= X + (0...0) & Cin

Entity Declaration:

```
entity arith_carrychain_inc is
  generic (
    BITS      : positive
  );
  port (
    X   : in  std_logic_vector(BITS - 1 downto 0);
    CIn : in  std_logic                           := '1';
    Y   : out std_logic_vector(BITS - 1 downto 0)
  );
end entity;
```

Source file: arith/arith_carrychain_inc.vhdl

7.4.4 PoC.arith.convert_bin2bcd

Todo: No documentation available.

Entity Declaration:

```
entity arith_convert_bin2bcd is
  generic (
    BITS          : positive    := 8;
```

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```
    DIGITS        : positive    := 3;
    RADIX         : positive    := 2
  );
  port (
    Clock         : in  std_logic;
    Reset         : in  std_logic;

    Start         : in  std_logic;
    Busy          : out std_logic;

    Binary        : in  std_logic_vector(BITS - 1 downto 0);
    IsSigned      : in  std_logic                           := '0';
    BCDDigits     : out T_BCD_VECTOR(DIGITS - 1 downto 0);
    Sign          : out std_logic
  );
end entity;
```

Source file: arith/arith_convert_bin2bcd.vhdl

7.4.5 PoC.arith.counter_bcd

Counter with output in binary coded decimal (BCD). The number of BCD digits is configurable by `DIGITS`.

All control signals (reset `rst`, increment `inc`) are high-active and synchronous to clock `clk`. The output `val` is the current counter state. Groups of 4 bit represent one BCD digit. The lowest significant digit is specified by `val(3 downto 0)`.

Todo:

- implement a `dec` input for decrementing
- implement a `load` input to load a value

Entity Declaration:

```
entity arith_counter_bcd is
  generic (
    DIGITS : positive                           -- Number of BCD digits
  );
  port (
    clk : in  std_logic;
    rst : in  std_logic;                        -- Reset to 0
    inc : in  std_logic;                        -- Increment
    val : out T_BCD_VECTOR(DIGITS-1 downto 0)   -- Value output
  );
end entity;
```

Source file: arith/arith_counter_bcd.vhdl

7.4.6 PoC.arith.counter_free

Implements a free-running counter that generates a strobe signal every DIVIDER-th cycle the increment input was asserted. There is deliberately no output or specification of the counter value so as to allow an implementation to optimize as much as possible.

The implementation guarantees a strobe output directly from a register. It is asserted exactly for one clock after DIVIDER cycles of an asserted increment input have been observed.

Entity Declaration:

```
entity arith_counter_free is
  generic (
    DIVIDER : positive
  );
  port (
    -- Global Control
    clk : in  std_logic;
    rst : in  std_logic;

    inc : in  std_logic;
    stb : out std_logic                  -- End-of-Period Strobe
  );
end entity arith_counter_free;
```

Source file: arith/arith_counter_free.vhdl

7.4.7 PoC.arith.counter_gray

Todo: No documentation available.

Entity Declaration:

```
entity arith_counter_gray is
  generic (
    BITS : positive;                                -- Bit width of the counter
    INIT : natural        := 0                      -- Initial/reset counter value
  );
  port (
    clk : in  std_logic;
    rst : in  std_logic;                            -- Reset to INIT value
    inc : in  std_logic;                            -- Increment
    dec : in  std_logic   := '0';                   -- Decrement
    val : out std_logic_vector(BITS-1 downto 0);    -- Value output
    cry : out std_logic                             -- Carry output
  );
end entity arith_counter_gray;
```

Source file: arith/arith_counter_gray.vhdl

7.4.8 PoC.arith.counter_ring

This module implements an up/down ring-counter with loadable initial value (`seed`) on reset. The counter can be configured to a Johnson counter by enabling `INVERT_FEEDBACK`. The number of counter bits is configurable with `BITS`.

Entity Declaration:

```
entity arith_counter_ring is
  generic (
    BITS            : positive;
    INVERT_FEEDBACK : boolean   := FALSE                                    -- FALSE
↪-> ring counter;   TRUE -> johnson counter
```

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```
  );
  port (
    Clock    : in  std_logic;                                                    -- Clock
    Reset    : in  std_logic;                                                    -- Reset
    seed     : in  std_logic_vector(BITS - 1 downto 0) := (others => '0'); --␣
↪initial counter vector / load value
    inc      : in  std_logic                           := '0';             --␣
↪increment counter
    dec      : in  std_logic                           := '0';             --␣
↪decrement counter
    value    : out std_logic_vector(BITS - 1 downto 0)                     --␣
↪counter value
  );
end entity;
```

Source file: arith/arith_counter_ring.vhdl

7.4.9 PoC.arith.div

Implementation of a Non-Performing restoring divider with a configurable radix. The multi-cycle division is controlled by 'start' / 'rdy'. A new division is started by asserting 'start'. The result Q = A/D is available when 'rdy' returns to '1'. A division by zero is identified by output Z. The Q and R outputs are undefined in this case.

Entity Declaration:

```
entity arith_div is
  generic (
    A_BITS              : positive;          -- Dividend Width
    D_BITS              : positive;          -- Divisor Width
    RAPOW               : positive := 1;     -- Power of Compute Radix (2**RAPOW)
    PIPELINED           : boolean  := false  -- Computation Pipeline
  );
  port (
    -- Global Reset/Clock
    clk : in std_logic;
    rst : in std_logic;

    -- Ready / Start
    start : in  std_logic;
    ready : out std_logic;

    -- Arguments / Result (2's complement)
    A : in  std_logic_vector(A_BITS-1 downto 0);  -- Dividend
    D : in  std_logic_vector(D_BITS-1 downto 0);  -- Divisor
    Q : out std_logic_vector(A_BITS-1 downto 0);  -- Quotient
    R : out std_logic_vector(D_BITS-1 downto 0);  -- Remainder
    Z : out std_logic  -- Division by Zero
  );
end entity arith_div;
```

Source file: arith/arith_div.vhdl

7.4.10 PoC.arith.firstone

Computes from an input word, a word of the same size that has, at most, one bit set. The output contains a set bit at the position of the rightmost set bit of the input if and only if such a set bit exists in the input.

A typical use case for this computation would be an arbitration over requests with a fixed and strictly ordered priority. The terminology of the interface assumes this use case and provides some useful extras:

- Set tin <= '0' (no input token) to disallow grants altogether.
- Read tout (unused token) to see whether or any grant was issued.
- Read bin to obtain the binary index of the rightmost detected one bit. The index starts at zero (0) in the rightmost bit position.

This implementation uses carry chains for wider implementations.

Entity Declaration:

```
entity arith_firstone is
  generic (
    N : positive                                  -- Length of Token Chain
  );
  port (
    tin  : in  std_logic := '1';                  -- Enable:   Fed Token
    rqst : in  std_logic_vector(N-1 downto 0);    -- Request:  Token Requests
    grnt : out std_logic_vector(N-1 downto 0);    -- Grant:    Token Output
    tout : out std_logic;                         -- Inactive: Unused Token
    bin  : out std_logic_vector(log2ceil(N)-1 downto 0)  -- Binary Grant Index
  );
end entity arith_firstone;
```

Source file: arith/arith_firstone.vhdl

7.4.11 PoC.arith.muls_wide

Signed wide multiplication spanning multiple DSP or MULT blocks. Small partial products are calculated through LUTs. For detailed documentation see below.

Entity Declaration:

Source file: arith/arith_muls_wide.vhdl

7.4.12 PoC.arith.prefix_and

Prefix AND computation: `y(i) <= '1' when x(i downto 0) = (i downto 0 => '1') else '0';` This implementation uses carry chains for wider implementations.

Entity Declaration:

```
entity arith_prefix_and is
  generic (
    N : positive
  );
  port (
    x : in  std_logic_vector(N-1 downto 0);
    y : out std_logic_vector(N-1 downto 0)
  );
end entity;
```

Source file: arith/arith_prefix_and.vhdl

7.4.13 PoC.arith.prefix_or

Prefix OR computation: `y(i) <= '0' when x(i downto 0) = (i downto 0 => '0') else '1';` This implementation uses carry chains for wider implementations.

Entity Declaration:

```
entity arith_prefix_or is
  generic (
    N : positive
  );
  port (
    x : in  std_logic_vector(N-1 downto 0);
    y : out std_logic_vector(N-1 downto 0)
  );
end entity;
```

Source file: arith/arith_prefix_or.vhdl

7.4.14 PoC.arith.prng

This module implementes a Pseudo-Random Number Generator (PRNG) with configurable bit count (`BITS`). This module uses an internal list of FPGA optimized polynomials from 3 to 168 bits. The polynomials have at most 5 tap positions, so that long shift registers can be inferred instead of single flip-flops.

The generated number sequence includes the value all-zeros, but not all-ones.

Entity Declaration:

```
entity arith_prng is
  generic (
    BITS : positive         := 32;
    SEED : std_logic_vector := "0"
  );
  port (
    clk  : in std_logic;
    rst  : in std_logic;                            -- reset value to initial seed
    got  : in std_logic;                            -- the current value has been got, and a new value should be calculated
    val  : out std_logic_vector(BITS - 1 downto 0)  -- the pseudo-random number
  );
end entity;
```

Source file: arith/arith_prng.vhdl

7.4.15 PoC.arith.same

This circuit may, for instance, be used to detect the first sign change and, thus, the range of a two's complement number.

These components may be chained by using the output of the predecessor as guard input. This chaining allows to have intermediate results available while still ensuring the use of a fast carry chain on supporting FPGA architectures. When chaining, make sure to overlap both vector slices by one bit position as to avoid an undetected sign change between the slices.

Entity Declaration:

```
entity arith_same is
  generic (
    N : positive                              -- Input width
  );
  port (
    g : in  std_logic := '1';                 -- Guard Input (!g => !y)
    x : in  std_logic_vector(N-1 downto 0); -- Input Vector
    y : out std_logic                         -- All-same Output
  );
end entity;
```

Source file: arith/arith_same.vhdl

7.4.16 PoC.arith.scaler

A flexible scaler for fixed-point values. The scaler is implemented for a set of multiplier and divider values. Each individual scaling operation can arbitrarily select one value from each these sets.

The computation calculates: `unsigned(arg) * MULS(msel) / DIVS(dsel)` rounded to the nearest (tie upwards) fixed-point result of the same precision as `arg`.

The computation is started by asserting `start` to high for one cycle. If a computation is running, it will be restarted. The completion of a calculation is signaled via `done`. `done` is high when no computation is in progress. The result of the last scaling operation is stable and can be read from `res`. The weight of the LSB of `res` is the same as the LSB of `arg`. Make sure to tap a sufficient number of result bits in accordance to the highest scaling ratio to be used in order to avoid a truncation overflow.

Entity Declaration:

```
entity arith_scaler is
  generic (
    MULS : T_POSVEC := (0 => 1);   -- The set of multipliers to choose from in␣
↪scaling operations.
    DIVS : T_POSVEC := (0 => 1)    -- The set of divisors to choose from in scaling␣
↪operations.
  );
  port (
    clk   : in std_logic;
    rst   : in std_logic;

    start : in  std_logic;           -- Start of Computation
    arg   : in std_logic_vector;     -- Fixed-point value to be scaled
    msel  : in  std_logic_vector(log2ceil(MULS'length)-1 downto 0) := (others => '0
↪');
    dsel  : in  std_logic_vector(log2ceil(DIVS'length)-1 downto 0) := (others => '0
↪');

    done  : out std_logic;           -- Completion
    res   : out std_logic_vector     -- Result
  );
end entity arith_scaler;
```

Source file: arith/arith_scaler.vhdl

7.4.17 PoC.arith.shifter_barrel

This Barrel-Shifter supports:

- shifting and rotating
- right and left operations
- arithmetic and logic mode (only valid for shift operations)

This is equivalent to the CPU instructions: SLL, SLA, SRL, SRA, RL, RR

Entity Declaration:

```
entity arith_shifter_barrel is
  generic (
    BITS         : positive    := 32
  );
  port (
    Input           : in  std_logic_vector(BITS - 1 downto 0);
    ShiftAmount     : in  std_logic_vector(log2ceilnz(BITS) - 1 downto 0);
    ShiftRotate     : in  std_logic;
    LeftRight       : in  std_logic;
    ArithmeticLogic : in  std_logic;
    Output          : out std_logic_vector(BITS - 1 downto 0)
  );
end entity;
```

Source file: arith/arith_shifter_barrel.vhdl

7.4.18 PoC.arith.sqrt

Iterative Square Root Extractor.

Its computation requires (N+1)/2 steps for an argument bit width of N.

Entity Declaration:

```
entity arith_sqrt is
  generic (
    N : positive -- := 8                    -- Bit Width of Argument
  );
  port (
    -- Global Control
    rst : in std_logic;                 -- Reset (synchronous)
    clk : in std_logic;                 -- Clock

    -- Inputs
    arg   : in std_logic_vector(N-1 downto 0); -- Radicand
    start : in std_logic;                       -- Start Strobe

    -- Outputs
    sqrt : out std_logic_vector((N-1)/2 downto 0);  -- Result
    rdy : out std_logic                             -- Ready / Done
  );
end entity arith_sqrt;
```

Source file: arith/arith_sqrt.vhdl

7.5 PoC.bus

These are bus entities. . . .

Sub-namespaces

- *PoC.bus.stream*
- *PoC.bus.wb*

Entities

- *PoC.bus.Arbiter*

7.5.1 PoC.bus.stream

PoC.Stream modules . . .

PoC.bus.stream Package

Source file: stream.pkg.vhdl

PoC.bus.stream.Buffer

This module implements a generic buffer (FIFO) for the *PoC.Stream* protocol. It is generic in `DATA_BITS` and in `META_BITS` as well as in FIFO depths for data and meta information.

Entity Declaration:

```
entity stream_Buffer is
  generic (
    FRAMES              : positive                                          :=␣
↪2;
    DATA_BITS           : positive                                          :=␣
↪8;
    DATA_FIFO_DEPTH     : positive                                          :=␣
↪8;
    META_BITS           : T_POSVEC                                          :=␣
↪(0 => 8);
    META_FIFO_DEPTH     : T_POSVEC                                          :=␣
↪(0 => 16)
  );
  port (
    Clock               : in  std_logic;
    Reset               : in  std_logic;
    -- IN Port
    In_Valid            : in  std_logic;
    In_Data             : in  std_logic_vector(DATA_BITS - 1 downto 0);
    In_SOF              : in  std_logic;
    In_EOF              : in  std_logic;
    In_Ack              : out std_logic;
    In_Meta_rst         : out std_logic;
    In_Meta_nxt         : out std_logic_vector(META_BITS'length - 1 downto 0);
    In_Meta_Data        : in  std_logic_vector(isum(META_BITS) - 1 downto 0);
    -- OUT Port
    Out_Valid           : out std_logic;
    Out_Data            : out std_logic_vector(DATA_BITS - 1 downto 0);
    Out_SOF             : out std_logic;
```

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```
    Out_EOF           : out std_logic;
    Out_Ack           : in  std_logic;
    Out_Meta_rst      : in  std_logic;
    Out_Meta_nxt      : in  std_logic_vector(META_BITS'length - 1 downto 0);
    Out_Meta_Data     : out std_logic_vector(isum(META_BITS) - 1 downto 0)
  );
end entity;
```

Source file: bus/stream/stream_Buffer.vhdl

PoC.bus.stream.DeMux

Todo: No documentation available.

Entity Declaration:

```
entity stream_DeMux is
  generic (
    PORTS             : positive                  := 2;
    DATA_BITS         : positive                  := 8;
    META_BITS         : natural                   := 8;
    META_REV_BITS     : natural                   := 2
  );
  port (
    Clock             : in  std_logic;
    Reset             : in  std_logic;
    -- Control interface
    DeMuxControl      : in  std_logic_vector(PORTS - 1 downto 0);
    -- IN Port
    In_Valid          : in  std_logic;
    In_Data           : in  std_logic_vector(DATA_BITS - 1 downto 0);
    In_Meta           : in  std_logic_vector(META_BITS - 1 downto 0);
    In_Meta_rev       : out std_logic_vector(META_REV_BITS - 1 downto 0);
    In_SOF            : in  std_logic;
    In_EOF            : in  std_logic;
    In_Ack            : out std_logic;
    -- OUT Ports
    Out_Valid         : out std_logic_vector(PORTS - 1 downto 0);
    Out_Data          : out T_SLM(PORTS - 1 downto 0, DATA_BITS - 1 downto 0);
    Out_Meta          : out T_SLM(PORTS - 1 downto 0, META_BITS - 1 downto 0);
    Out_Meta_rev      : in  T_SLM(PORTS - 1 downto 0, META_REV_BITS - 1 downto 0);
    Out_SOF           : out std_logic_vector(PORTS - 1 downto 0);
    Out_EOF           : out std_logic_vector(PORTS - 1 downto 0);
    Out_Ack           : in  std_logic_vector(PORTS - 1 downto 0)
  );
end entity;
```

Source file: bus/stream/stream_DeMux.vhdl

PoC.bus.stream.Mux

Todo: No documentation available.

Entity Declaration:

```
entity stream_Mux is
  generic (
    PORTS             : positive                    := 2;
    DATA_BITS         : positive                    := 8;
    META_BITS         : natural                     := 8;
    META_REV_BITS     : natural                     := 2--;
--    WEIGHTS           : T_INTVEC                    := (1, 1)
  );
  port (
    Clock             : in  std_logic;
    Reset             : in  std_logic;
    -- IN Ports
    In_Valid          : in  std_logic_vector(PORTS - 1 downto 0);
    In_Data           : in  T_SLM(PORTS - 1 downto 0, DATA_BITS - 1 downto 0);
    In_Meta           : in  T_SLM(PORTS - 1 downto 0, META_BITS - 1 downto 0);
    In_Meta_rev       : out T_SLM(PORTS - 1 downto 0, META_REV_BITS - 1 downto 0);
    In_SOF            : in  std_logic_vector(PORTS - 1 downto 0);
    In_EOF            : in  std_logic_vector(PORTS - 1 downto 0);
    In_Ack            : out std_logic_vector(PORTS - 1 downto 0);
    -- OUT Port
    Out_Valid         : out std_logic;
    Out_Data          : out std_logic_vector(DATA_BITS - 1 downto 0);
    Out_Meta          : out std_logic_vector(META_BITS - 1 downto 0);
    Out_Meta_rev      : in  std_logic_vector(META_REV_BITS - 1 downto 0);
    Out_SOF           : out std_logic;
    Out_EOF           : out std_logic;
    Out_Ack           : in  std_logic
  );
end entity;
```

Source file: bus/stream/stream_Mux.vhdl

PoC.bus.stream.Mirror

Todo: No documentation available.

Entity Declaration:

```
entity stream_Mirror is
  generic (
    PORTS             : positive                    := 2;
    DATA_BITS         : positive                    := 8;
    META_BITS         : T_POSVEC                    := (0 => 8);
    META_LENGTH       : T_POSVEC                    := (0 => 16)
  );
  port (
    Clock             : in  std_logic;
    Reset             : in  std_logic;
    -- IN Port
    In_Valid          : in  std_logic;
    In_Data           : in  std_logic_vector(DATA_BITS - 1 downto 0);
    In_SOF            : in  std_logic;
    In_EOF            : in  std_logic;
    In_Ack            : out std_logic;
    In_Meta_rst       : out std_logic;
```

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```
    In_Meta_nxt       : out std_logic_vector(META_BITS'length - 1 downto 0);
    In_Meta_Data      : in  std_logic_vector(isum(META_BITS) - 1 downto 0);
    -- OUT Port
    Out_Valid         : out std_logic_vector(PORTS - 1 downto 0);
    Out_Data          : out T_SLM(PORTS - 1 downto 0, DATA_BITS - 1 downto 0);
    Out_SOF           : out std_logic_vector(PORTS - 1 downto 0);
    Out_EOF           : out std_logic_vector(PORTS - 1 downto 0);
    Out_Ack           : in  std_logic_vector(PORTS - 1 downto 0);
    Out_Meta_rst      : in  std_logic_vector(PORTS - 1 downto 0);
    Out_Meta_nxt      : in  T_SLM(PORTS - 1 downto 0, META_BITS'length - 1 downto
↪0);
    Out_Meta_Data     : out T_SLM(PORTS - 1 downto 0, isum(META_BITS) - 1 downto 0)
  );
end entity;
```

Source file: bus/stream/stream_Mirror.vhdl

PoC.bus.stream.Sink

Todo: No documentation available.

Entity Declaration:

Source file: bus/stream/stream_Sink.vhdl

PoC.bus.stream.Source

Todo: No documentation available.

Entity Declaration:

```
entity stream_Source is
  generic (
    TESTCASES         : T_SIM_STREAM_FRAMEGROUP_VECTOR_8
  );
  port (
    Clock             : in  std_logic;
    Reset             : in  std_logic;
    -- Control interface
    Enable            : in  std_logic;
    -- OUT Port
    Out_Valid         : out std_logic;
    Out_Data          : out T_SLV_8;
    Out_SOF           : out std_logic;
    Out_EOF           : out std_logic;
    Out_Ack           : in  std_logic
  );
end entity;
```

Source file: bus/stream/stream_Source.vhdl

PoC.bus.stream.FrameGenerator

Todo: No documentation available.

Entity Declaration:

```
entity stream_FrameGenerator is
  generic (
    DATA_BITS          : positive                          := 8;
    WORD_BITS          : positive                          := 16;
    APPEND             : T_FRAMEGEN_APPEND                 := FRAMEGEN_APP_NONE;
    FRAMEGROUPS        : T_FRAMEGEN_FRAMEGROUP_VECTOR_8    := (0 => C_FRAMEGEN_
↪FRAMEGROUP_EMPTY)
  );
  port (
    Clock              : in  std_logic;
    Reset              : in  std_logic;
    -- CSE interface
    Command            : in  T_FRAMEGEN_COMMAND;
    Status             : out T_FRAMEGEN_STATUS;
    -- Control interface
    Pause              : in  T_SLV_16;
    FrameGroupIndex    : in  T_SLV_8;
    FrameIndex         : in  T_SLV_8;
    Sequences          : in  T_SLV_16;
    FrameLength        : in  T_SLV_16;
    -- OUT Port
    Out_Valid          : out std_logic;
    Out_Data           : out std_logic_vector(DATA_BITS - 1 downto 0);
    Out_SOF            : out std_logic;
    Out_EOF            : out std_logic;
    Out_Ack            : in  std_logic
  );
end entity;
```

Source file: bus/stream/stream_FrameGenerator.vhdl

7.5.2 PoC.bus.wb

WishBone modules ...

Entities:

PoC.bus.wb Package

Source file: wb.pkg.vhdl

PoC.bus.wb.ocram

This slave supports Wishbone Registered Feedback bus cycles (aka. burst transfers / advanced synchronous cycle termination). The mode "Incrementing burst cycle" (CTI = 010) with "Linear burst" (BTE = 00) is supported.

If your master does support Wishbone Classis bus cycles only, then connect wb_cti_i = "000" and wb_bte_i = "00".

Connect the ocram of your choice to the ram_* port signals. (Every RAM with single cyle read latency is supported.)

Configuration:

PIPE_STAGES = 1 The RAM output is directly connected to the bus. Thus, the read access latency (one cycle) is short. But, the RAM's read timing delay must be respected.

PIPE_STAGES = 2 The RAM output is registered again. Thus, the read access latency is two cycles.

Entity Declaration:

Source file: bus/wb/wb_ocram.vhdl

PoC.bus.wb.fifo_adapter

Small FIFOs are included in this module, if larger or asynchronous transmit / receive FIFOs are required, then they must be connected externally.

old comments: UART BAUD rate generator bclk_r = bit clock is rising bclk_x8_r = bit clock times 8 is rising

Entity Declaration:

Source file: bus/wb/wb_fifo_adapter.vhdl

PoC.bus.wb.uart_wrapper

Wrapper module for *PoC.io.uart.rx* and *PoC.io.uart.tx* to support the Wishbone interface. Synchronized reset is used.

Entity Declaration:

Source file: bus/wb/wb_uart_wrapper.vhdl

7.5.3 PoC.bus.Arbiter

This module implements a generic arbiter. It currently supports the following arbitration strategies:

- Round Robin (RR)

Entity Declaration:

```
entity bus_Arbiter is
  generic (
    STRATEGY                : string                        := "RR";       -- RR, LOT
    PORTS                   : positive                      := 1;
    WEIGHTS                 : T_INTVEC                      := (0 => 1);
    OUTPUT_REG              : boolean                       := TRUE
  );
  port (
    Clock                   : in  std_logic;
    Reset                   : in  std_logic;

    Arbitrate               : in  std_logic;
    Request_Vector          : in  std_logic_vector(PORTS - 1 downto 0);

```

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```
15      Arbitrated                : out std_logic;
16      Grant_Vector              : out std_logic_vector(PORTS - 1 downto 0);
17      Grant_Index               : out std_logic_vector(log2ceilnz(PORTS) - 1 downto␣
    ↪0)
18    );
19  end entity;
```

Source file: bus/bus_Arbiter.vhdl

7.6 PoC.cache

The namespace *PoC.cache* offers different cache implementations.

Entities

- *PoC.cache.cpu*: Cache with cache controller to be used within a CPU.
- *PoC.cache.mem*: Cache with *PoC.Mem Interface* interface on the "CPU" side.
- *PoC.cache.par*: Cache with parallel tag-unit and data memory (using infered memory).
- *PoC.cache.par2*: Cache with parallel tag-unit and data memory (using *PoC.mem.ocram.sp*).
- *PoC.cache.tagunit_par*: Tag-Unit with parallel tag comparison. Configurable as:
  - Full-associative cache,
  - Direct-mapped cache, or
  - Set-associative cache.
- *PoC.cache.tagunit_seq*: Tag-Unit with sequential tag comparison. Configurable as:
  - Full-associative cache,
  - Direct-mapped cache, or
  - Set-associative cache.

7.6.1 PoC.cache.cpu

This unit provides a cache (*PoC.cache.par2*) together with a cache controller which reads / writes cache lines from / to memory. The memory is accessed using a *PoC.Mem Interface* interfaces, the related ports and parameters are prefixed with `mem_`.

The CPU side (prefix `cpu_`) has a modified PoC.Mem interface, so that this unit can be easily integrated into processor pipelines. For example, let's have a pipeline where a load/store instruction is executed in 3 stages (after fetching, decoding, ...):

1. Execute (EX) for address calculation,
2. Load/Store 1 (LS1) for the cache access,
3. Load/Store 2 (LS2) where the cache returns the read data.

The read data is always returned one cycle after the cache access completes, so there is conceptually a pipeline register within this unit. The stage LS2 can be merged with a write-back stage if the clock period allows so.

The stage LS1 and thus EX and LS2 must stall, until the cache access is completed, i.e., the EX/LS1 pipeline register must hold the cache request until it is acknowledged by the cache. This is signaled by `cpu_got` as described in Section Operation below. The pipeline moves forward (is enabled) when:

```
pipeline_enable <= (not cpu_req) or cpu_got;
```

If the pipeline can stall due to other reasons, care must be taken to not unintentionally executing the cache access twice or missing the read data.

Of course, the EX/LS1 pipeline register can be omitted and the CPU side directly fed by the address caculator. But be aware of the high setup time of this unit and high propate time for `cpu_got`.

This unit supports only one outstanding CPU request. More outstanding requests are provided by *PoC.cache.mem*.

Configuration

Parameter	Description
REPLACEMENT_POLICY	Replacement policy of embedded cache. For supported values see PoC.cache_replacement_policy.
CACHE_LINES	Number of cache lines.
ASSOCIATIVITY	Associativity of embedded cache.
CPU_ADDR_BITS	Number of address bits on the CPU side. Each address identifies one memory word as seen from the CPU. Calculated from other parameters as described below.
CPU_DATA_BITS	Width of the data bus (in bits) on the CPU side. CPU_DATA_BITS must be divisible by 8.
MEM_ADDR_BITS	Number of address bits on the memory side. Each address identifies one word in the memory.
MEM_DATA_BITS	Width of a memory word and of a cache line in bits. MEM_DATA_BITS must be divisible by CPU_DATA_BITS.

If the CPU data-bus width is smaller than the memory data-bus width, then the CPU needs additional address bits to identify one CPU data word inside a memory word. Thus, the CPU address-bus width is calculated from:

```
CPU_ADDR_BITS=log2ceil(MEM_DATA_BITS/CPU_DATA_BITS)+MEM_ADDR_BITS
```

The write policy is: write-through, no-write-allocate.

Operation

Alignment of Cache / Memory Accesses

Memory accesses are always aligned to a word boundary. Each memory word (and each cache line) consists of MEM_DATA_BITS bits. For example if MEM_DATA_BITS=128:

- memory address 0 selects the bits 0..127 in memory,
- memory address 1 selects the bits 128..256 in memory, and so on.

Cache accesses are always aligned to a CPU word boundary. Each CPU word consists of CPU_DATA_BITS bits. For example if CPU_DATA_BITS=32:

- CPU address 0 selects the bits 0.. 31 in memory word 0,
- CPU address 1 selects the bits 32.. 63 in memory word 0,
- CPU address 2 selects the bits 64.. 95 in memory word 0,
- CPU address 3 selects the bits 96..127 in memory word 0,
- CPU address 4 selects the bits 0.. 31 in memory word 1,
- CPU address 5 selects the bits 32.. 63 in memory word 1, and so on.

Shared and Memory Side Interface

A synchronous reset must be applied even on a FPGA.

The memory side interface is documented in detail *here*.

CPU Side Interface

The CPU (pipeline stage LS1, see above) issues a request by setting `cpu_req`, `cpu_write`, `cpu_addr`, `cpu_wdata` and `cpu_wmask` as in the *PoC.Mem Interface* interface. The cache acknowledges the request by setting `cpu_got` to '1'. If the request is not acknowledged (`cpu_got = '0'`) in the current clock cycle, then the request must be repeated in the following clock cycle(s) until it is acknowledged, i.e., the pipeline must stall.

A cache access is completed when it is acknowledged. A new request can be issued in the following clock cycle.

Of course, `cpu_got` may be asserted in the same clock cycle where the request was issued if a read hit occurs. This allows a throughput of one (read) request per clock cycle, but the drawback is, that `cpu_got` has a high propagation delay. Thus, this output should only control a simple pipeline enable logic.

When `cpu_got` is asserted for a read access, then the read data will be available in the following clock cycle.

Due to the write-through policy, a write will always take several clock cycles and acknowledged when the data has been issued to the memory.

Warning: If the design is synthesized with Xilinx ISE / XST, then the synthesis option "Keep Hierarchy" must be set to SOFT or TRUE.

Entity Declaration:

```
entity cache_cpu is
  generic (
    REPLACEMENT_POLICY : string   := "LRU";
    CACHE_LINES        : positive;
    ASSOCIATIVITY      : positive;
    CPU_DATA_BITS      : positive;
    MEM_ADDR_BITS      : positive;
    MEM_DATA_BITS      : positive
  );
  port (
    clk : in std_logic; -- clock
    rst : in std_logic; -- reset

    -- "CPU" side
    cpu_req   : in  std_logic;
    cpu_write : in  std_logic;
    cpu_addr  : in  unsigned(log2ceil(MEM_DATA_BITS/CPU_DATA_BITS)+MEM_ADDR_BITS-1 downto 0);
    cpu_wdata : in  std_logic_vector(CPU_DATA_BITS-1 downto 0);
    cpu_wmask : in  std_logic_vector(CPU_DATA_BITS/8-1 downto 0);
    cpu_got   : out std_logic;
    cpu_rdata : out std_logic_vector(CPU_DATA_BITS-1 downto 0);

    -- Memory side
    mem_req   : out std_logic;
    mem_write : out std_logic;
    mem_addr  : out unsigned(MEM_ADDR_BITS-1 downto 0);
    mem_wdata : out std_logic_vector(MEM_DATA_BITS-1 downto 0);
```

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```
28      mem_wmask : out std_logic_vector(MEM_DATA_BITS/8-1 downto 0);
29      mem_rdy   : in  std_logic;
30      mem_rstb  : in  std_logic;
31      mem_rdata : in  std_logic_vector(MEM_DATA_BITS-1 downto 0)
32      );
33  end entity;
```

See also:

PoC.cache.mem

Source file: cache/cache_cpu.vhdl

7.6.2 PoC.cache.mem

This unit provides a cache (*PoC.cache.par2*) together with a cache controller which reads / writes cache lines from / to memory. It has two *PoC.Mem Interface* interfaces:

- one for the "CPU" side (ports with prefix `cpu_`), and
- one for the memory side (ports with prefix `mem_`).

Thus, this unit can be placed into an already available memory path between the CPU and the memory (controller). If you want to plugin a cache into a CPU pipeline, see *PoC.cache.cpu*.

Configuration

Parameter	Description
REPLACEMENT_POLICY	Replacement policy of embedded cache. For supported values see PoC.cache_replacement_policy.
CACHE_LINES	Number of cache lines.
ASSOCIATIVITY	Associativity of embedded cache.
CPU_ADDR_BITS	Number of address bits on the CPU side. Each address identifies one memory word as seen from the CPU. Calculated from other parameters as described below.
CPU_DATA_BITS	Width of the data bus (in bits) on the CPU side. CPU_DATA_BITS must be divisible by 8.
MEM_ADDR_BITS	Number of address bits on the memory side. Each address identifies one word in the memory.
MEM_DATA_BITS	Width of a memory word and of a cache line in bits. MEM_DATA_BITS must be divisible by CPU_DATA_BITS.
OUTSTANDING_REQ	Number of oustanding requests, see notes below.

If the CPU data-bus width is smaller than the memory data-bus width, then the CPU needs additional address bits to identify one CPU data word inside a memory word. Thus, the CPU address-bus width is calculated from:

```
CPU_ADDR_BITS=log2ceil(MEM_DATA_BITS/CPU_DATA_BITS)+MEM_ADDR_BITS
```

The write policy is: write-through, no-write-allocate.

The maximum throughput is one request per clock cycle, except for `OUSTANDING_REQ = 1`.

If `OUTSTANDING_REQ` is:

- 1: then 1 request is buffered by a single register. To give a short critical path (clock-to-output delay) for `cpu_rdy`, the throughput is degraded to one request per 2 clock cycles at maximum.
- 2: then 2 requests are buffered by *PoC.fifo.glue*. This setting has the lowest area requirements without degrading the performance.

- >2: then the requests are buffered by *PoC.fifo.cc_got*. The number of outstanding requests is rounded up to the next suitable value. This setting is useful in applications with out-of-order execution (of other operations). The CPU requests to the cache are always processed in-order.

Operation

Memory accesses are always aligned to a word boundary. Each memory word (and each cache line) consists of MEM_DATA_BITS bits. For example if MEM_DATA_BITS=128:

- memory address 0 selects the bits 0..127 in memory,
- memory address 1 selects the bits 128..256 in memory, and so on.

Cache accesses are always aligned to a CPU word boundary. Each CPU word consists of CPU_DATA_BITS bits. For example if CPU_DATA_BITS=32:

- CPU address 0 selects the bits 0.. 31 in memory word 0,
- CPU address 1 selects the bits 32.. 63 in memory word 0,
- CPU address 2 selects the bits 64.. 95 in memory word 0,
- CPU address 3 selects the bits 96..127 in memory word 0,
- CPU address 4 selects the bits 0.. 31 in memory word 1,
- CPU address 5 selects the bits 32.. 63 in memory word 1, and so on.

A synchronous reset must be applied even on a FPGA.

The interface is documented in detail *here*.

Warning: If the design is synthesized with Xilinx ISE / XST, then the synthesis option "Keep Hierarchy" must be set to SOFT or TRUE.

Entity Declaration:

```
entity cache_mem is
  generic (
    REPLACEMENT_POLICY : string   := "LRU";
    CACHE_LINES        : positive;
    ASSOCIATIVITY      : positive;
    CPU_DATA_BITS      : positive;
    MEM_ADDR_BITS      : positive;
    MEM_DATA_BITS      : positive;
    OUTSTANDING_REQ    : positive := 2
  );
  port (
    clk : in std_logic; -- clock
    rst : in std_logic; -- reset

    -- "CPU" side
    cpu_req   : in  std_logic;
    cpu_write : in  std_logic;
    cpu_addr  : in  unsigned(log2ceil(MEM_DATA_BITS/CPU_DATA_BITS)+MEM_ADDR_BITS-1 downto 0);
    cpu_wdata : in  std_logic_vector(CPU_DATA_BITS-1 downto 0);
    cpu_wmask : in  std_logic_vector(CPU_DATA_BITS/8-1 downto 0) := (others => '0');
    cpu_rdy   : out std_logic;
    cpu_rstb  : out std_logic;
    cpu_rdata : out std_logic_vector(CPU_DATA_BITS-1 downto 0);
```

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```
24
25      -- Memory side
26      mem_req   : out std_logic;
27      mem_write : out std_logic;
28      mem_addr  : out unsigned(MEM_ADDR_BITS-1 downto 0);
29      mem_wdata : out std_logic_vector(MEM_DATA_BITS-1 downto 0);
30      mem_wmask : out std_logic_vector(MEM_DATA_BITS/8-1 downto 0);
31      mem_rdy   : in  std_logic;
32      mem_rstb  : in  std_logic;
33      mem_rdata : in  std_logic_vector(MEM_DATA_BITS-1 downto 0)
34      );
35  end entity;
```

See also:

PoC.cache.cpu

Source file: cache/cache_mem.vhdl

7.6.3 PoC.cache.par

Implements a cache with parallel tag-unit and data memory.

Note: This component infers a single-port memory with read-first behavior, that is, upon writes the old-data is returned on the read output. Such memory (e.g. LUT-RAM) is not available on all devices. Thus, synthesis may infer a lot of flip-flops plus multiplexers instead, which is very inefficient. It is recommended to use *PoC.cache.par2* instead which has a slightly different interface.

All inputs are synchronous to the rising-edge of the clock *clock*.

Command truth table:

Request	ReadWrite	Invalidate	Replace	Command
0	0	0	0	None
1	0	0	0	Read cache line
1	1	0	0	Update cache line
1	0	1	0	Read cache line and discard it
1	1	1	0	Write cache line and discard it
0		0	1	Replace cache line.

All commands use `Address` to lookup (request) or replace a cache line. `Address` and `OldAddress` do not include the word/byte select part. Each command is completed within one clock cycle, but outputs are delayed as described below.

Upon requests, the outputs `CacheMiss` and `CacheHit` indicate (high-active) whether the `Address` is stored within the cache, or not. Both outputs have a latency of one clock cycle.

Upon writing a cache line, the new content is given by `CacheLineIn`. Upon reading a cache line, the current content is outputed on `CacheLineOut` with a latency of one clock cycle.

Upon replacing a cache line, the new content is given by `CacheLineIn`. The old content is outputed on `CacheLineOut` and the old tag on `OldAddress`, both with a latency of one clock cycle.

Warning: If the design is synthesized with Xilinx ISE / XST, then the synthesis option "Keep Hierarchy" must be set to SOFT or TRUE.

Entity Declaration:

```
entity cache_par is
  generic (
    REPLACEMENT_POLICY : string   := "LRU";
    CACHE_LINES        : positive := 32;--1024;
    ASSOCIATIVITY      : positive := 32;--4;
    ADDRESS_BITS       : positive := 8; --32-6;
    DATA_BITS          : positive := 8  --64*8
  );
  port (
    Clock : in std_logic;
    Reset : in std_logic;

    Request     : in std_logic;
    ReadWrite   : in std_logic;
    Invalidate  : in std_logic;
    Replace     : in std_logic;
    Address     : in std_logic_vector(ADDRESS_BITS - 1 downto 0);

    CacheLineIn  : in  std_logic_vector(DATA_BITS - 1 downto 0);
    CacheLineOut : out std_logic_vector(DATA_BITS - 1 downto 0);
    CacheHit     : out std_logic := '0';
    CacheMiss    : out std_logic := '0';
    OldAddress   : out std_logic_vector(ADDRESS_BITS - 1 downto 0)
  );
end entity;
```

Source file: cache/cache_par.vhdl

7.6.4 PoC.cache.par2

Cache with parallel tag-unit and data memory. For the data memory, *PoC.mem.ocram.sp* is used.

Configuration

Parameter	Description
REPLACE-MENT_POLICY	Replacement policy. For supported policies see PoC.cache_replacement_policy.
CACHE_LINES	Number of cache lines.
ASSOCIATIVITY	Associativity of the cache.
ADDR_BITS	Number of address bits. Each address identifies exactly one cache line in memory.
DATA_BITS	Size of a cache line in bits. DATA_BITS must be divisible by 8.

Command truth table

Request	ReadWrite	Invalidate	Replace	Command
0	0	0	0	None
1	0	0	0	Read cache line
1	1	0	0	Update cache line
1	0	1	0	Read cache line and discard it
1	1	1	0	Write cache line and discard it
0	0	0	1	Read cache line before replace.
0	1	0	1	Replace cache line.

Operation

All inputs are synchronous to the rising-edge of the clock *clock*.

All commands use `Address` to lookup (request) or replace a cache line. `Address` and `OldAddress` do not include the word/byte select part. Each command is completed within one clock cycle, but outputs are delayed as described below.

Upon requests, the outputs `CacheMiss` and `CacheHit` indicate (high-active) whether the `Address` is stored within the cache, or not. Both outputs have a latency of one clock cycle (pipelined) if `HIT_MISS_REG` is true, otherwise the result is outputted immediately (combinational).

Upon writing a cache line, the new content is given by `CacheLineIn`. Only the bytes which are not masked, i.e. the corresponding bit in WriteMask is '0', are actually written.

Upon reading a cache line, the current content is outputed on `CacheLineOut` with a latency of one clock cycle.

Replacing a cache line requires two steps, both with `Replace = '1'`:

1. Read old contents of cache line by setting `ReadWrite` to '0'. The old content is outputed on `CacheLineOut` and the old tag on `OldAddress`, both with a latency of one clock cycle.
2. Write new cache line by setting `ReadWrite` to '1'. The new content is given by `CacheLineIn`. All bytes shall be written, i.e. `WriteMask = 0`. The new cache line content will be outputed again on `CacheLineOut` in the next clock cycle (latency = 1).

Warning: If the design is synthesized with Xilinx ISE / XST, then the synthesis option "Keep Hierarchy" must be set to SOFT or TRUE.

Entity Declaration:

```
entity cache_par2 is
  generic (
    REPLACEMENT_POLICY : string   := "LRU";
    CACHE_LINES        : positive := 32;
    ASSOCIATIVITY      : positive := 32;
    ADDR_BITS          : positive := 8;
    DATA_BITS          : positive := 8;
    HIT_MISS_REG       : boolean  := true  -- must be true for Cocotb.
  );
  port (
    Clock : in std_logic;
    Reset : in std_logic;

    Request    : in std_logic;
    ReadWrite  : in std_logic;
    WriteMask  : in std_logic_vector(DATA_BITS/8 - 1 downto 0) := (others => '0');
    Invalidate : in std_logic;
    Replace    : in std_logic;
    Address    : in std_logic_vector(ADDR_BITS-1 downto 0);

    CacheLineIn  : in  std_logic_vector(DATA_BITS - 1 downto 0);
    CacheLineOut : out std_logic_vector(DATA_BITS - 1 downto 0);
    CacheHit     : out std_logic := '0';
    CacheMiss    : out std_logic := '0';
    OldAddress   : out std_logic_vector(ADDR_BITS-1 downto 0)
  );
end entity;
```

Source file: cache/cache_par2.vhdl

7.6.5 PoC.cache.replacement_policy

Supported policies:

Abbr.	Policies	supported
RR	round robin	not yet
RAND	random	not yet
CLOCK	clock algorithm	not yet
LRU	least recently used	YES
LFU	least frequently used	not yet

Command thruth table:

TagAccess	ReadWrite	Invalidate	Replace	Command
0			0	None
1	0	0	0	TagHit and reading a cache line
1	1	0	0	TagHit and writing a cache line
1	0	1	0	TagHit and invalidate a cache line (while reading)
1	1	1	0	TagHit and invalidate a cache line (while writing)
0		0	1	Replace cache line

In a set-associative cache, each cache-set has its own instance of this component.

The input `HitWay` specifies the accessed way in a fully-associative or set-associative cache.

The output `ReplaceWay` identifies the way which will be replaced as next by a replace command. In a set-associative cache, this is the way in a specific cache set (see above).

Entity Declaration:

```
entity cache_replacement_policy is
  generic (
    REPLACEMENT_POLICY : string   := "LRU";
    CACHE_WAYS         : positive := 32
  );
  port (
    Clock : in std_logic;
    Reset : in std_logic;

    -- replacement interface
    Replace    : in  std_logic;
    ReplaceWay : out std_logic_vector(log2ceilnz(CACHE_WAYS) - 1 downto 0);

    -- cacheline usage update interface
    TagAccess  : in std_logic;
    ReadWrite  : in std_logic;
    Invalidate : in std_logic;
    HitWay     : in std_logic_vector(log2ceilnz(CACHE_WAYS) - 1 downto 0)
  );
end entity;
```

Source file: cache/cache_replacement_policy.vhdl

7.6.6 PoC.cache.tagunit_par

Tag-unit with fully-parallel compare of tag.

Configuration

Parameter	Description
REPLACEMENT_POLICY	Replacement policy. For supported policies see PoC.cache_replacement_policy.
CACHE_LINES	Number of cache lines.
ASSOCIATIVITY	Associativity of the cache.
ADDRESS_BITS	Number of address bits. Each address identifies exactly one cache line in memory.

Command truth table

Request	ReadWrite	Invalidate	Replace	Command
0	0	0	0	None
1	0	0	0	Read cache line
1	1	0	0	Update cache line
1	0	1	0	Read cache line and discard it
1	1	1	0	Write cache line and discard it
0		0	1	Replace cache line.

Operation

All inputs are synchronous to the rising-edge of the clock *clock*.

All commands use `Address` to lookup (request) or replace a cache line. Each command is completed within one clock cycle.

Upon requests, the outputs `CacheMiss` and `CacheHit` indicate (high-active) immediately (combinational) whether the `Address` is stored within the cache, or not. But, the cache-line usage is updated at the rising-edge of the clock. If hit, `LineIndex` specifies the cache line where to find the content.

The output `ReplaceLineIndex` indicates which cache line will be replaced as next by a replace command. The output `OldAddress` specifies the old tag stored at this index. The replace command will store the `Address` and update the cache-line usage at the rising-edge of the clock.

For a direct-mapped cache, the number of `CACHE_LINES` must be a power of 2. For a set-associative cache, the expression `CACHE_LINES / ASSOCIATIVITY` must be a power of 2.

Note: The port `NewAddress` has been removed. Use `Address` instead as described above.

If `Address` is fed from a register and an Altera FPGA is used, then Quartus Map converts the tag memory from a memory with asynchronous read to a memory with synchronous read by adding a pass-through logic. Quartus Map reports warning 276020 which is intended.

Warning: If the design is synthesized with Xilinx ISE / XST, then the synthesis option "Keep Hierarchy" must be set to SOFT or TRUE.

Entity Declaration:

```
1 entity cache_tagunit_par is
2   generic (
3     REPLACEMENT_POLICY : string   := "LRU";
```

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```
    CACHE_LINES         : positive := 32;
    ASSOCIATIVITY       : positive := 32;
    ADDRESS_BITS        : positive := 8
  );
  port (
    Clock : in std_logic;
    Reset : in std_logic;

    Replace          : in  std_logic;
    ReplaceLineIndex : out std_logic_vector(log2ceilnz(CACHE_LINES) - 1 downto 0);
    OldAddress       : out std_logic_vector(ADDRESS_BITS - 1 downto 0);

    Request    : in  std_logic;
    ReadWrite  : in  std_logic;
    Invalidate : in  std_logic;
    Address    : in  std_logic_vector(ADDRESS_BITS - 1 downto 0);
    LineIndex  : out std_logic_vector(log2ceilnz(CACHE_LINES) - 1 downto 0);
    TagHit     : out std_logic;
    TagMiss    : out std_logic
  );
end entity;
```

Source file: cache/cache_tagunit_par.vhdl

7.6.7 PoC.cache.tagunit_seq

Todo: No documentation available.

Entity Declaration:

```
entity cache_tagunit_seq is
  generic (
    REPLACEMENT_POLICY : string       := "LRU";
    CACHE_LINES        : positive     := 32;
    ASSOCIATIVITY      : positive     := 32;
    TAG_BITS           : positive     := 128;
    CHUNK_BITS         : positive     := 8;
    TAG_BYTE_ORDER     : T_BYTE_ORDER := LITTLE_ENDIAN;
    USE_INITIAL_TAGS   : boolean      := false;
    INITIAL_TAGS       : T_SLM        := (0 downto 0 => (127 downto 0 => '0'))
  );
  port (
    Clock : in std_logic;
    Reset : in std_logic;

    Replace             : in  std_logic;
    Replaced            : out std_logic;
    Replace_NewTag_rst  : out std_logic;
    Replace_NewTag_rev  : out std_logic;
    Replace_NewTag_nxt  : out std_logic;
    Replace_NewTag_Data : in  std_logic_vector(CHUNK_BITS - 1 downto 0);
    Replace_NewIndex    : out std_logic_vector(log2ceilnz(CACHE_LINES) - 1 downto␣
↪0);

    Request            : in  std_logic;
    Request_ReadWrite  : in  std_logic;
```

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```
    Request_Invalidate : in  std_logic;
    Request_Tag_rst    : out std_logic;
    Request_Tag_rev    : out std_logic;
    Request_Tag_nxt    : out std_logic;
    Request_Tag_Data   : in  std_logic_vector(CHUNK_BITS - 1 downto 0);
    Request_Index      : out std_logic_vector(log2ceilnz(CACHE_LINES) - 1 downto
↪0);
    Request_TagHit     : out std_logic;
    Request_TagMiss    : out std_logic
  );
end entity;
```

Source file: cache/cache_tagunit_seq.vhdl

7.7 PoC.comm

These are communication entities. . . .

7.7.1 PoC.comm Package

Source file: comm.pkg.vhdl

7.7.2 PoC.comm.crc

Computes the Cyclic Redundancy Check (CRC) for a data packet as remainder of the polynomial division of the message by the given generator polynomial (GEN).

The computation is unrolled so as to process an arbitrary number of message bits per step. The generated CRC is independent from the chosen processing width.

Entity Declaration:

```
entity comm_crc is
  generic (
    GEN    : bit_vector;                                -- Generator Polynomial
    BITS   : positive;                                  -- Number of Bits to be
↪processed in parallel

    STARTUP_RMD : std_logic_vector  := "0";
    OUTPUT_REGS : boolean           := true
  );
  port (
    clk : in  std_logic;                                -- Clock

    set : in  std_logic;                                -- Parallel Preload of
↪Remainder
    init : in std_logic_vector(abs(mssb_idx(GEN)-GEN'right)-1 downto 0);  --
    step : in std_logic;                                -- Process Input Data (MSB
↪first)
    din : in  std_logic_vector(BITS-1 downto 0);        --

    rmd : out std_logic_vector(abs(mssb_idx(GEN)-GEN'right)-1 downto 0);  --
↪Remainder
    zero : out std_logic                                -- Remainder is Zero
```

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```
  );
end entity comm_crc;
```

Source file: comm/comm_crc.vhdl

7.7.3 PoC.comm.scramble

The LFSR computation is unrolled to generate an arbitrary number of mask bits in parallel. The mask are output in little endian. The generated bit sequence is independent from the chosen output width.

Entity Declaration:

```
entity comm_scramble is
  generic (
    GEN  : bit_vector;        -- Generator Polynomial (little endian)
    BITS : positive           -- Width of Mask Bits to be computed in parallel in␣
↪each step
  );
  port (
    clk  : in  std_logic;     -- Clock

    set  : in  std_logic;     -- Set LFSR to value provided on din
    din  : in  std_logic_vector(GEN'length-2 downto 0) := (others => '0');

    step : in  std_logic;     -- Compute a Mask Output
    mask : out std_logic_vector(BITS-1 downto 0)
  );
end entity comm_scramble;
```

Source file: comm/comm_scramble.vhdl

7.8 PoC.dstruct

The namespace *PoC.dstruct* offers different data structure implementations.

Package

The package *PoC.dstruct* holds all component declarations for this namespace.

Entities

- *PoC.dstruct.deque* implements a deque (two-sided FIFO).
- *PoC.dstruct.stack* implements a regular stack.

7.8.1 PoC.dstruct.deque

Implements a deque (double-ended queue). This data structure allows two acting entities to queue data elements for the consumption by the other while still being able to unqueue untaken ones in LIFO fashion.

Entity Declaration:

```
entity dstruct_deque is
  generic (
    D_BITS     : positive;                -- Data Width
    MIN_DEPTH : positive                  -- Minimum Deque Depth
  );
  port (
    -- Shared Ports
    clk, rst : in std_logic;

    -- Port A
    dinA   : in  std_logic_vector(D_BITS-1 downto 0);  -- DataA Input
    putA   : in  std_logic;
    gotA   : in  std_logic;
    doutA  : out std_logic_vector(D_BITS-1 downto 0);  -- DataA Output
    validA : out std_logic;
    fullA  : out std_logic;

    -- Port B
    dinB   : in  std_logic_vector(D_BITS-1 downto 0);  -- DataB Input
    putB   : in  std_logic;
    gotB   : in  std_logic;
    doutB  : out std_logic_vector(D_BITS-1 downto 0);
    validB : out std_logic;
    fullB  : out std_logic
  );
end entity dstruct_deque;
```

Source file: dstruct/dstruct_deque.vhdl

7.8.2 PoC.dstruct.stack

Implements a stack, a LIFO storage abstraction.

Entity Declaration:

```
entity dstruct_stack is
  generic (
    D_BITS     : positive;                -- Data Width
    MIN_DEPTH : positive                  -- Minimum Stack Depth
  );
  port (
    -- INPUTS
    clk, rst : in std_logic;

    -- Write Ports
    din  : in  std_logic_vector(D_BITS-1 downto 0);  -- Data Input
    put  : in  std_logic;  -- 0 -> pop, 1 -> push
    full : out std_logic;

    -- Read Ports
    got   : in  std_logic;
    dout  : out std_logic_vector(D_BITS-1 downto 0);
    valid : out std_logic
  );
end entity dstruct_stack;
```

Source file: dstruct/dstruct_stack.vhdl

7.9 PoC.fifo

The namespace *PoC.fifo* offers different FIFO (first-in, first-out) implementations.

Package

The package *PoC.fifo* holds all component declarations for this namespace.

Entities

PoC offers FIFOs with a *got*-interface. This means, the current read-pointer value is available on the output. Asserting the *got*-input, acknoledge the processing of the current output signals and moves the read-pointer to the next value, if available.

All FIFOs implement a bidirectional flow control (*put*/*full* and *valid*/*got*). Each FIFO also offers a EmptyState (write-side) and FullState (read-side) to indicate the current fill-state.

The prefixes *cc_* (common clock), *dc_* (dependent clock) and *ic_* (independent clock) refer to the write- and read-side clock relationship.

- *PoC.fifo.cc_got* implements a regular FIFO (one common clock, got-interface)
- *PoC.fifo.cc_got_tempgot* implements a regular FIFO (one common clock, got-interface), extended by a transactional *tempgot*-interface (read-side).
- *PoC.fifo.cc_got_tempput* implements a regular FIFO (one common clock, got-interface), extended by a transactional *tempput*-interface (write-side).
- IP:fifo_dc_got implements a cross-clock FIFO (two related clocks, got-interface)
- *PoC.fifo.ic_got* implements a cross-clock FIFO (two independent clocks, got-interface)
- *PoC.fifo.glue* implements a two-stage FIFO (one common clock, got-interface)
- *PoC.fifo.shift* implements a regular FIFO (one common clock, got-interface, optimized for FPGAs with shifter primitives)

7.9.1 PoC.fifo Package

This package holds all component declarations for this namespace.

Source file: fifo.pkg.vhdl

7.9.2 PoC.fifo.cc_got

This module implements a regular FIFO with common clock (cc), pipelined interface. Common clock means read and write port use the same clock. The FIFO size can be configured in word width (`D_BITS`) and minimum word count `MIN_DEPTH`. The specified depth is rounded up to the next suitable value.

`DATA_REG` (=true) is a hint, that distributed memory or registers should be used as data storage. The actual memory type depends on the device architecture. See implementation for details.

`*STATE_*_BITS` defines the granularity of the fill state indicator `*state_*`. If a fill state is not of interest, set `*STATE_*_BITS = 0`. `fstate_rd` is associated with the read clock domain and outputs the guaranteed number of words available in the FIFO. `estate_wr` is associated with the write clock domain and outputs the number of words that is guaranteed to be accepted by the FIFO without a capacity overflow. Note that both these indicators cannot replace the `full` or `valid` outputs as they may be implemented as giving pessimistic bounds that are minimally off the true fill state.

`fstate_rd` and `estate_wr` are combinatorial outputs and include an address comparator (subtractor) in their path.

Examples:

- FSTATE_RD_BITS = 1:

fstate_rd	filled (at least)
0	0/2 full
1	1/2 full (half full)

- FSTATE_RD_BITS = 2:

fstate_rd	filled (at least)
0	0/4 full
1	1/4 full
2	2/4 full (half full)
3	3/4 full

Entity Declaration:

```
entity fifo_cc_got is
  generic (
    D_BITS          : positive;           -- Data Width
    MIN_DEPTH       : positive;           -- Minimum FIFO Depth
    DATA_REG        : boolean := false;   -- Store Data Content in Registers
    STATE_REG       : boolean := false;   -- Registered Full/Empty Indicators
    OUTPUT_REG      : boolean := false;   -- Registered FIFO Output
    ESTATE_WR_BITS  : natural := 0;       -- Empty State Bits
    FSTATE_RD_BITS  : natural := 0        -- Full State Bits
  );
  port (
    -- Global Reset and Clock
    rst, clk : in  std_logic;

    -- Writing Interface
    put        : in  std_logic;                              -- Write Request
    din        : in  std_logic_vector(D_BITS-1 downto 0);    -- Input Data
    full       : out std_logic;
    estate_wr  : out std_logic_vector(imax(0, ESTATE_WR_BITS-1) downto 0);

    -- Reading Interface
    got        : in  std_logic;                              -- Read Completed
    dout       : out std_logic_vector(D_BITS-1 downto 0);    -- Output Data
    valid      : out std_logic;
    fstate_rd  : out std_logic_vector(imax(0, FSTATE_RD_BITS-1) downto 0)
  );
end entity fifo_cc_got;
```

See also:

IP:fifo_dc_got For a FIFO with dependent clocks.

PoC.fifo.ic_got For a FIFO with independent clocks (cross-clock FIFO).

PoC.fifo.glue For a minimal FIFO / pipeline decoupling.

Source file: fifo/fifo_cc_got.vhdl

7.9.3 PoC.fifo.cc_got_tempgot

The specified depth (`MIN_DEPTH`) is rounded up to the next suitable value.

As uncommitted reads occupy FIFO space that is not yet available for writing, an instance of this FIFO can, indeed, report `full` and `not vld` at the same time. While a `commit` would eventually make space available for writing (`not ful`), a `rollback` would re-iterate data for reading (`vld`).

`commit` and `rollback` are inclusive and apply to all reads (`got`) since the previous `commit` or `rollback` up to and including a potentially simultaneous read.

The FIFO state upon a simultaneous assertion of `commit` and `rollback` is *undefined*!

`*STATE_*_BITS` defines the granularity of the fill state indicator `*state_*`. `fstate_rd` is associated with the read clock domain and outputs the guaranteed number of words available in the FIFO. `estate_wr` is associated with the write clock domain and outputs the number of words that is guaranteed to be accepted by the FIFO without a capacity overflow. Note that both these indicators cannot replace the `full` or `valid` outputs as they may be implemented as giving pessimistic bounds that are minimally off the true fill state.

If a fill state is not of interest, set `*STATE_*_BITS = 0`.

`fstate_rd` and `estate_wr` are combinatorial outputs and include an address comparator (subtractor) in their path.

Examples:

- FSTATE_RD_BITS = 1:
  - fstate_rd == 0 => 0/2 full
  - fstate_rd == 1 => 1/2 full (half full)
- FSTATE_RD_BITS = 2:
  - fstate_rd == 0 => 0/4 full
  - fstate_rd == 1 => 1/4 full
  - fstate_rd == 2 => 2/4 full
  - fstate_rd == 3 => 3/4 full

Entity Declaration:

```
entity fifo_cc_got_tempgot is
  generic (
    D_BITS          : positive;           -- Data Width
    MIN_DEPTH       : positive;           -- Minimum FIFO Depth
    DATA_REG        : boolean := false;   -- Store Data Content in Registers
    STATE_REG       : boolean := false;   -- Registered Full/Empty Indicators
    OUTPUT_REG      : boolean := false;   -- Registered FIFO Output
    ESTATE_WR_BITS  : natural := 0;       -- Empty State Bits
    FSTATE_RD_BITS  : natural := 0        -- Full State Bits
  );
  port (
    -- Global Reset and Clock
    rst, clk : in  std_logic;

    -- Writing Interface
    put        : in  std_logic;                                 -- Write Request
    din        : in  std_logic_vector(D_BITS-1 downto 0);   -- Input Data
    full       : out std_logic;
    estate_wr  : out std_logic_vector(imax(0, ESTATE_WR_BITS-1) downto 0);

    -- Reading Interface
    got        : in  std_logic;                                 -- Read Completed
    dout       : out std_logic_vector(D_BITS-1 downto 0);   -- Output Data
    valid      : out std_logic;
    fstate_rd  : out std_logic_vector(imax(0, FSTATE_RD_BITS-1) downto 0);
```

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```
26
27      commit     : in  std_logic;
28      rollback   : in  std_logic
29    );
30  end entity fifo_cc_got_tempgot;
```

Source file: fifo/fifo_cc_got_tempgot.vhdl

7.9.4 PoC.fifo.cc_got_tempput

The specified depth (`MIN_DEPTH`) is rounded up to the next suitable value.

As uncommitted writes populate FIFO space that is not yet available for reading, an instance of this FIFO can, indeed, report `full` and `not vld` at the same time. While a `commit` would eventually make data available for reading (`vld`), a `rollback` would free the space for subsequent writing (`not ful`).

`commit` and `rollback` are inclusive and apply to all writes (`put`) since the previous 'commit' or 'rollback' up to and including a potentially simultaneous write.

The FIFO state upon a simultaneous assertion of `commit` and `rollback` is *undefined*.

`*STATE_*_BITS` defines the granularity of the fill state indicator `*state_*`. `fstate_rd` is associated with the read clock domain and outputs the guaranteed number of words available in the FIFO. `estate_wr` is associated with the write clock domain and outputs the number of words that is guaranteed to be accepted by the FIFO without a capacity overflow. Note that both these indicators cannot replace the `full` or `valid` outputs as they may be implemented as giving pessimistic bounds that are minimally off the true fill state.

If a fill state is not of interest, set `*STATE_*_BITS = 0`.

`fstate_rd` and `estate_wr` are combinatorial outputs and include an address comparator (subtractor) in their path.

Examples:

- FSTATE_RD_BITS = 1:
  - fstate_rd == 0 => 0/2 full
  - fstate_rd == 1 => 1/2 full (half full)
- FSTATE_RD_BITS = 2:
  - fstate_rd == 0 => 0/4 full
  - fstate_rd == 1 => 1/4 full
  - fstate_rd == 2 => 2/4 full
  - fstate_rd == 3 => 3/4 full

Entity Declaration:

```
1   entity fifo_cc_got_tempput is
2     generic (
3       D_BITS          : positive;          -- Data Width
4       MIN_DEPTH       : positive;          -- Minimum FIFO Depth
5       DATA_REG        : boolean := false;  -- Store Data Content in Registers
6       STATE_REG       : boolean := false;  -- Registered Full/Empty Indicators
7       OUTPUT_REG      : boolean := false;  -- Registered FIFO Output
8       ESTATE_WR_BITS  : natural := 0;      -- Empty State Bits
9       FSTATE_RD_BITS  : natural := 0       -- Full State Bits
10    );
11    port (
```

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```
    -- Global Reset and Clock
    rst, clk : in  std_logic;

    -- Writing Interface
    put       : in  std_logic;                              -- Write Request
    din       : in  std_logic_vector(D_BITS-1 downto 0);    -- Input Data
    full      : out std_logic;
    estate_wr : out std_logic_vector(imax(0, ESTATE_WR_BITS-1) downto 0);

    commit    : in  std_logic;
    rollback  : in  std_logic;

    -- Reading Interface
    got       : in  std_logic;                              -- Read Completed
    dout      : out std_logic_vector(D_BITS-1 downto 0);    -- Output Data
    valid     : out std_logic;
    fstate_rd : out std_logic_vector(imax(0, FSTATE_RD_BITS-1) downto 0)
  );
end entity fifo_cc_got_tempput;
```

Source file: fifo/fifo_cc_got_tempput.vhdl

7.9.5 PoC.fifo.glue

Its primary use is the decoupling of enable domains in a processing pipeline. Data storage is limited to two words only so as to allow both the `ful` and the `vld` indicators to be driven by registers.

Entity Declaration:

```
entity fifo_glue is
  generic (
    D_BITS : positive                                 -- Data Width
  );
  port (
    -- Control
    clk : in std_logic;                               -- Clock
    rst : in std_logic;                               -- Synchronous Reset

    -- Input
    put : in  std_logic;                              -- Put Value
    di  : in  std_logic_vector(D_BITS-1 downto 0);    -- Data Input
    ful : out std_logic;                              -- Full

    -- Output
    vld : out std_logic;                              -- Data Available
    do  : out std_logic_vector(D_BITS-1 downto 0);    -- Data Output
    got : in  std_logic                               -- Data Consumed
  );
end entity fifo_glue;
```

Source file: fifo/fifo_glue.vhdl

7.9.6 PoC.fifo.ic_assembly

This module assembles a FIFO stream from data blocks that may arrive slightly out of order. The arriving data is ordered according to their address. The streamed output starts with the data word written to address zero (0) and may proceed all the way to just before the first yet missing data. The association of data with addresses is used on

the input side for the sole purpose of reconstructing the correct order of the data. It is assumed to wrap so as to allow an infinite input sequence. Addresses are not actively exposed to the purely stream-based FIFO output.

The implemented functionality enables the reconstruction of streams that are tunnelled across address-based transports that are allowed to reorder the transmission of data blocks. This applies to many DMA implementations.

Entity Declaration:

```
entity fifo_ic_assembly is
  generic (
    D_BITS : positive;                  -- Data Width
    A_BITS : positive;                  -- Address Bits
    G_BITS : positive                   -- Generation Guard Bits
  );
  port (
    -- Write Interface
    clk_wr : in std_logic;
    rst_wr : in std_logic;

    -- Only write addresses in the range [base, base+2**(A_BITS-G_BITS)) are
    -- acceptable. This is equivalent to the test
    --   tmp(A_BITS-1 downto A_BITS-G_BITS) = 0 where tmp = addr - base.
    -- Writes performed outside the allowable range will assert the failure
    -- indicator, which will stick until the next reset.
    -- No write is to be performed before base turns zero (0) for the first
    -- time.
    base   : out std_logic_vector(A_BITS-1 downto 0);
    failed : out std_logic;

    addr : in  std_logic_vector(A_BITS-1 downto 0);
    din  : in  std_logic_vector(D_BITS-1 downto 0);
    put  : in  std_logic;

    -- Read Interface
    clk_rd : in std_logic;
    rst_rd : in std_logic;

    dout : out std_logic_vector(D_BITS-1 downto 0);
    vld  : out std_logic;
    got  : in  std_logic
  );
end entity fifo_ic_assembly;
```

Source file: fifo/fifo_ic_assembly.vhdl

7.9.7 PoC.fifo.ic_got

Independent clocks meens that read and write clock are unrelated.

This implementation uses dedicated block RAM for storing data.

First-word-fall-through (FWFT) mode is implemented, so data can be read out as soon as `valid` goes high. After the data has been captured, then the signal `got` must be asserted.

Synchronous reset is used. Both resets may overlap.

`DATA_REG` (=true) is a hint, that distributed memory or registers should be used as data storage. The actual memory type depends on the device architecture. See implementation for details.

`*STATE_*_BITS` defines the granularity of the fill state indicator `*state_*`. `fstate_rd` is associated with the read clock domain and outputs the guaranteed number of words available in the FIFO. `estate_wr` is associated with the write clock domain and outputs the number of words that is guaranteed to be accepted by the FIFO

without a capacity overflow. Note that both these indicators cannot replace the `full` or `valid` outputs as they may be implemented as giving pessimistic bounds that are minimally off the true fill state.

If a fill state is not of interest, set *STATE_*_BITS = 0.

`fstate_rd` and `estate_wr` are combinatorial outputs and include an address comparator (subtractor) in their path.

Examples: - FSTATE_RD_BITS = 1: fstate_rd == 0 => 0/2 full

fstate_rd == 1 => 1/2 full (half full)

- **FSTATE_RD_BITS = 2: fstate_rd == 0 => 0/4 full** fstate_rd == 1 => 1/4 full fstate_rd == 2 => 2/4 full fstate_rd == 3 => 3/4 full

Entity Declaration:

```
entity fifo_ic_got is
  generic (
    D_BITS          : positive;           -- Data Width
    MIN_DEPTH       : positive;           -- Minimum FIFO Depth
    DATA_REG        : boolean := false;   -- Store Data Content in Registers
    OUTPUT_REG      : boolean := false;   -- Registered FIFO Output
    ESTATE_WR_BITS : natural := 0;        -- Empty State Bits
    FSTATE_RD_BITS : natural := 0         -- Full State Bits
  );
  port (
    -- Write Interface
    clk_wr     : in  std_logic;
    rst_wr     : in  std_logic;
    put        : in  std_logic;
    din        : in  std_logic_vector(D_BITS-1 downto 0);
    full       : out std_logic;
    estate_wr : out std_logic_vector(imax(ESTATE_WR_BITS-1, 0) downto 0);

    -- Read Interface
    clk_rd     : in  std_logic;
    rst_rd     : in  std_logic;
    got        : in  std_logic;
    valid      : out std_logic;
    dout       : out std_logic_vector(D_BITS-1 downto 0);
    fstate_rd : out std_logic_vector(imax(FSTATE_RD_BITS-1, 0) downto 0)
  );
end entity fifo_ic_got;
```

Source file: fifo/fifo_ic_got.vhdl

7.9.8 PoC.fifo.shift

This FIFO implementation is based on an internal shift register. This is especially useful for smaller FIFO sizes, which can be implemented in LUT storage on some devices (e.g. Xilinx' SRLs). Only a single read pointer is maintained, which determines the number of valid entries within the underlying shift register.

The specified depth (`MIN_DEPTH`) is rounded up to the next suitable value.

Entity Declaration:

```
entity fifo_shift is
  generic (
```

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```
    D_BITS     : positive;                -- Data Width
    MIN_DEPTH  : positive                 -- Minimum FIFO Size in Words
  );
  port (
    -- Global Control
    clk : in std_logic;
    rst : in std_logic;

    -- Writing Interface
    put : in  std_logic;                                -- Write Request
    din : in  std_logic_vector(D_BITS-1 downto 0);      -- Input Data
    ful : out std_logic;                                -- Capacity Exhausted

    -- Reading Interface
    got  : in  std_logic;                               -- Read Done Strobe
    dout : out std_logic_vector(D_BITS-1 downto 0);     -- Output Data
    vld  : out std_logic                                -- Data Valid
  );
end entity fifo_shift;
```

Source file: fifo/fifo_shift.vhdl

7.10 PoC.io

The namespace `PoC.io` offers different general purpose I/O (GPIO) implementations, as well as low-speed bus protocol controllers.

Sub-namespaces

- *PoC.io.ddrio* - Double-Data-Rate (DDR) input/output abstraction layer.
- *PoC.io.iic* - I^{2}C bus controllers
- *PoC.io.jtag* - JTAG implementations
- *PoC.io.lcd* - LC-Display bus controllers
- *PoC.io.mdio* - Management Data I/O (MDIO) controllers for Ethernet PHYs
- *PoC.io.ow* - OneWire / iButton bus controllers
- *PoC.io.ps2* - Periphery bus of the Personal System/2 (PS/2)
- *PoC.io.uart* - Universal Asynchronous Receiver Transmitter (UART) controllers
- *PoC.io.vga* - VGA, DVI, HDMI controllers

Package

The package *PoC.io* holds all enum, function and component declarations for this namespace.

Entities

- *PoC.io.Debounce*
- *PoC.io.7SegmentMux_BCD*
- *PoC.io.7SegmentMux_HEX*
- *PoC.io.FanControl*
- *PoC.io.FrequencyCounter*
- *PoC.io.GlitchFilter*
- *PoC.io.PulseWidthModulation*

- *PoC.io.TimingCounter*

7.10.1 PoC.io.ddrio

These are DDR-I/O (Double Data Rate - Input/Output) entities. . . .

Entities

- *PoC.io.ddrio.in*
- *PoC.io.ddrio.inout*
- *PoC.io.ddrio.out*

PoC.io.ddrio Package

Source file: ddrio.pkg.vhdl

PoC.io.ddrio.in

Instantiates chip-specific DDR (Double Data Rate) input registers.

Both data `DataIn_high/low` are synchronously outputted to the on-chip logic with the rising edge of `Clock`. `DataIn_high` is the value at the `Pad` sampled with the same rising edge. `DataIn_low` is the value sampled with the falling edge directly before this rising edge. Thus sampling starts with the falling edge of the clock as depicted in the following waveform.

After power-up, the output ports `DataIn_high` and `DataIn_low` both equal INIT_VALUE.

`Pad` must be connected to a PAD because FPGAs only have these registers in IOBs.

Entity Declaration:

```
entity ddrio_in is
  generic (
    BITS          : positive;
    INIT_VALUE    : bit_vector  := x"FFFFFFFF"
  );
  port (
    Clock         : in    std_logic;
    ClockEnable   : in    std_logic;
    DataIn_high   : out   std_logic_vector(BITS - 1 downto 0);
    DataIn_low    : out   std_logic_vector(BITS - 1 downto 0);
    Pad           : in    std_logic_vector(BITS - 1 downto 0)
    );
end entity;
```

Source file: io/ddrio/ddrio_in.vhdl

PoC.io.ddrio.inout

Instantiates chip-specific DDR input and output registers.

Both data `DataOut_high/low` as well as `OutputEnable` are sampled with the `rising_edge(Clock)` from the on-chip logic. `DataOut_high` is brought out with this rising edge. `DataOut_low` is brought out with the falling edge.

`OutputEnable` (Tri-State) is high-active. It is automatically inverted if necessary. Output is disabled after power-up.

Both data `DataIn_high/low` are synchronously outputted to the on-chip logic with the rising edge of `Clock`. `DataIn_high` is the value at the `Pad` sampled with the same rising edge. `DataIn_low` is the value sampled with the falling edge directly before this rising edge. Thus sampling starts with the falling edge of the clock as depicted in the following waveform.

`Pad` must be connected to a PAD because FPGAs only have these registers in IOBs.

Entity Declaration:

```
entity ddrio_inout is
  generic (
    BITS          : positive
  );
  port (
    ClockOut        : in    std_logic;
    ClockOutEnable  : in    std_logic;
    OutputEnable    : in    std_logic;
    DataOut_high    : in    std_logic_vector(BITS - 1 downto 0);
    DataOut_low     : in    std_logic_vector(BITS - 1 downto 0);

    ClockIn         : in    std_logic;
    ClockInEnable   : in    std_logic;
    DataIn_high     : out   std_logic_vector(BITS - 1 downto 0);
    DataIn_low      : out   std_logic_vector(BITS - 1 downto 0);

    Pad             : inout std_logic_vector(BITS - 1 downto 0)
  );
end entity;
```

Source file: io/ddrio/ddrio_inout.vhdl

PoC.io.ddrio.out

Instantiates chip-specific DDR output registers.

Both data `DataOut_high/low` as well as `OutputEnable` are sampled with the `rising_edge(Clock)` from the on-chip logic. `DataOut_high` is brought out with this rising edge. `DataOut_low` is brought out with the falling edge.

`OutputEnable` (Tri-State) is high-active. It is automatically inverted if necessary. If an output enable is not required, you may save some logic by setting `NO_OUTPUT_ENABLE = true`.

If `NO_OUTPUT_ENABLE = false` then output is disabled after power-up. If `NO_OUTPUT_ENABLE = true` then output after power-up equals `INIT_VALUE`.

`Pad` must be connected to a PAD because FPGAs only have these registers in IOBs.

Entity Declaration:

```
entity ddrio_out is
  generic (
    NO_OUTPUT_ENABLE    : boolean     := false;
    BITS                : positive;
    INIT_VALUE          : bit_vector  := x"FFFFFFFF"
  );
  port (
    Clock         : in  std_logic;
    ClockEnable   : in  std_logic := '1';
    OutputEnable  : in  std_logic := '1';
```

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```
    DataOut_high  : in  std_logic_vector(BITS - 1 downto 0);
    DataOut_low   : in  std_logic_vector(BITS - 1 downto 0);
    Pad           : out std_logic_vector(BITS - 1 downto 0)
  );
end entity;
```

Source file: io/ddrio/ddrio_out.vhdl

7.10.2 PoC.io.iic

These are I2C entities. . . .

PoC.io.iic Package

Source file: iic.pkg.vhdl

PoC.io.iic.BusController

The I2C BusController transmitts bits over the I2C bus (SerialClock - SCL, SerialData - SDA) and also receives them. To send/receive words over the I2C bus, use the I2C Controller, which utilizes this controller. This controller is compatible to the System Management Bus (SMBus).

Entity Declaration:

Source file: io/iic/iic_BusController.vhdl

PoC.io.iic.Controller

The I2C Controller transmitts words over the I2C bus (SerialClock - SCL, SerialData - SDA) and also receives them. This controller utilizes the I2C BusController to send/receive bits over the I2C bus. This controller is compatible to the System Management Bus (SMBus).

Entity Declaration:

Source file: io/iic/iic_Controller.vhdl

PoC.io.iic.Switch_PCA9548A

Todo: No documentation available. TODO

Entity Declaration:

Source file: io/iic/iic_Switch_PCA9548A.vhdl

7.10.3 PoC.io.jtag

These are JTAG entities. . . .

7.10.4 PoC.io.lcd

These are LCD entities. . . .

PoC.io.lcd Package

Source file: lcd.pkg.vhdl

PoC.io.lcd.LCDBuffer

Todo: No documentation available.

Entity Declaration:

Source file: io/lcd/lcd_LCDBuffer.vhdl

PoC.io.lcd.LCDBusController

Todo: No documentation available.

Entity Declaration:

Source file: io/lcd/lcd_LCDBusController.vhdl

PoC.io.lcd.LCDController_KS0066U

Todo: No documentation available.

Entity Declaration:

Source file: io/lcd/lcd_LCDController_KS0066U.vhdl

PoC.io.lcd.LCDSynchronizer

Todo: No documentation available.

Entity Declaration:

Source file: io/lcd/lcd_LCDSynchronizer.vhdl

7.10.5 PoC.io.mdio

These are MDIO entities. . . .

mdio_BusController

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PoC.io.mdio.Controller

Todo: No documentation available.

Entity Declaration:

Source file: io/mdio/mdio_Controller.vhdl

PoC.io.mdio.IIC_Adapter

Todo: No documentation available.

Entity Declaration:

Source file: io/mdio/mdio_IIC_Adapter.vhdl

7.10.6 PoC.io.ow

These are OneWire entities. . . .

ow_BusController

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ow_Controller

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7.10.7 PoC.io.pio

These are Pmod entities. . . .

PoC.io.pio.in

Entity Declaration:

Source file: io/pio/pio_in.vhdl

PoC.io.pio.out

Entity Declaration:

Source file: io/pio/pio_out.vhdl

PoC.io.pio.fifo_in

Entity Declaration:

Source file: io/pio/pio_fifo_in.vhdl

PoC.io.pio.fifo_out

Entity Declaration:

Source file: io/pio/pio_fifo_out.vhdl

7.10.8 PoC.io.pmod

These are Pmod entities. . . .

Entities

- *PoC.io.pmod.KYPD*
- *PoC.io.pmod.SSD*
- *PoC.io.pmod.USBUART*

PoC.io.pmod Package

Source file: pmod.pkg.vhdl

PoC.io.pmod.KYPD

This module drives a 4-bit one-cold encoded column vector to read back a 4-bit rows vector. By scanning column-by-column it's possible to extract the current button state of the whole keypad. This wrapper converts the high-active signals from *PoC.io.KeypadScanner* to low-active signals for the pmod. An additional debounce circuit filters the button signals. The scan frequency and bounce time can be configured.

Entity Declaration:

```
entity pmod_KYPD is
  generic (
    CLOCK_FREQ     : FREQ         := 100 MHz;
    SCAN_FREQ      : FREQ         := 1 kHz;
    BOUNCE_TIME    : time         := 10 ms
  );
  port (
    Clock          : in  std_logic;
    Reset          : in  std_logic;
    -- Matrix interface
    Keys           : out T_PMOD_KYPD_KEYPAD;
    -- KeyPad interface
    Columns_n      : out std_logic_vector(3 downto 0);
    Rows_n         : in  std_logic_vector(3 downto 0)
  );
end entity;
```

Source file: io/pmod/pmod_KYPD.vhdl

PoC.io.pmod.SSD

This module drives a dual-digit 7-segment display (Pmod_SSD). The module expects two binary encoded 4-bit `Digit<i>` signals and drives a 2x6 bit Pmod connector (7 anode bits, 1 cathode bit).

```
Segment Pos./ Index
   AAA       |   000
  F   B      |  5   1
  F   B      |  5   1
   GGG       |   666
  E   C      |  4   2
  E   C      |  4   2
   DDD  DOT |   333  7
```

Entity Declaration:

```
entity pmod_SSD is
  generic (
    CLOCK_FREQ     : FREQ     := 100 MHz;
    REFRESH_RATE   : FREQ     := 1 kHz
  );
  port (
    Clock      : in  std_logic;

    Digit0     : in  std_logic_vector(3 downto 0);
    Digit1     : in  std_logic_vector(3 downto 0);

    SSD        : out T_PMOD_SSD_PINS
```

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```
  );
end entity;
```

Source file: io/pmod/pmod_SSD.vhdl

PoC.io.pmod.USBUART

This module abstracts a FTDI FT232R USB-UART bridge by instantiating a *PoC.io.uart.fifo*. The FT232R supports up to 3 MBaud. A synchronous FIFO interface with a 32 words buffer is provided. Hardware flow control (RTS_CTS) is enabled.

Entity Declaration:

```
entity pmod_USBUART is
  generic (
    CLOCK_FREQ     : FREQ     := 100 MHz;
    BAUDRATE       : BAUD     := 115200 Bd
  );
  port (
    Clock      : in  std_logic;
    Reset      : in  std_logic;

    TX_put     : in  std_logic;
    TX_Data    : in  std_logic_vector(7 downto 0);
    TX_Full    : out std_logic;

    RX_Valid   : out std_logic;
    RX_Data    : out std_logic_vector(7 downto 0);
    RX_got     : in  std_logic;

    UART_TX    : out std_logic;
    UART_RX    : in  std_logic;
    UART_RTS   : out std_logic;
    UART_CTS   : in  std_logic
  );
end entity;
```

Source file: io/pmod/pmod_USBUART.vhdl

7.10.9 PoC.io.ps2

These are PS/2 entities. . . .

7.10.10 PoC.io.uart

These are UART (Universal Asynchronous Receiver Transmitter) entities. . . .

Entities

- *PoC.io.uart.bclk*
- *PoC.io.uart.rx*
- *PoC.io.uart.tx*
- *PoC.io.uart.fifo*

PoC.io.uart Package

Source file: uart.pkg.vhdl

PoC.io.uart.bclk

Todo: No documentation available.

old comments: UART BAUD rate generator bclk_r = bit clock is rising bclk_x8_r = bit clock times 8 is rising

Entity Declaration:

```
entity uart_bclk is
  generic (
    CLOCK_FREQ     : FREQ       := 100 MHz;
    BAUDRATE       : BAUD       := 115200 Bd
  );
  port (
    clk        : in  std_logic;
    rst        : in  std_logic;
    bclk       : out std_logic;
    bclk_x8    : out std_logic
  );
end entity;
```

Source file: io/uart/uart_bclk.vhdl

PoC.io.uart.rx

UART Receiver: 1 Start + 8 Data + 1 Stop

Entity Declaration:

```
entity uart_rx is
  generic (
    SYNC_DEPTH : natural := 2  -- use zero for already clock-synchronous rx
  );
  port (
    -- Global Control
    clk : in std_logic;
    rst : in std_logic;

    -- Bit Clock and RX Line
    bclk_x8 : in std_logic;   -- bit clock, eight strobes per bit length
    rx      : in std_logic;

    -- Byte Stream Output
    do  : out std_logic_vector(7 downto 0);
    stb : out std_logic
  );
end entity;
```

Source file: io/uart/uart_rx.vhdl

PoC.io.uart.tx

UART Transmitter: 1 Start + 8 Data + 1 Stop

Entity Declaration:

```
entity uart_tx is
  port (
    -- Global Control
    clk : in std_logic;
    rst : in std_logic;

    -- Bit Clock and TX Line
    bclk : in  std_logic;  -- bit clock, one strobe each bit length
    tx   : out std_logic;

    -- Byte Stream Input
    di   : in  std_logic_vector(7 downto 0);
    put : in  std_logic;
    ful : out std_logic
  );
end entity;
```

Source file: io/uart/uart_tx.vhdl

PoC.io.uart.fifo

Small FIFO s are included in this module, if larger or asynchronous transmit / receive FIFOs are required, then they must be connected externally.

old comments: UART BAUD rate generator bclk = bit clock is rising bclk_x8 = bit clock times 8 is rising

Entity Declaration:

```
entity uart_fifo is
  generic (
    -- Communication Parameters
    CLOCK_FREQ               : FREQ;
    BAUDRATE                 : BAUD;
    ADD_INPUT_SYNCHRONIZERS  : boolean                        := TRUE;

    -- Buffer Dimensioning
    TX_MIN_DEPTH             : positive                       := 16;
    TX_ESTATE_BITS           : natural                        :=  0;
    RX_MIN_DEPTH             : positive                       := 16;
    RX_FSTATE_BITS           : natural                        :=  0;

    -- Flow Control
    FLOWCONTROL              : T_IO_UART_FLOWCONTROL_KIND     := UART_FLOWCONTROL_
↪NONE;
    SWFC_XON_CHAR            : std_logic_vector(7 downto 0)   := x"11"; -- ^Q
    SWFC_XON_TRIGGER         : real                           := 0.0625;
    SWFC_XOFF_CHAR           : std_logic_vector(7 downto 0)   := x"13"; -- ^S
    SWFC_XOFF_TRIGGER        : real                           := 0.75
  );
  port (
    Clock          : in  std_logic;
    Reset          : in  std_logic;
```

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```
24
25      -- FIFO interface
26      TX_put         : in  std_logic;
27      TX_Data        : in  std_logic_vector(7 downto 0);
28      TX_Full        : out std_logic;
29      TX_EmptyState  : out std_logic_vector(imax(0, TX_ESTATE_BITS-1) downto 0);
30
31      RX_Valid       : out std_logic;
32      RX_Data        : out std_logic_vector(7 downto 0);
33      RX_got         : in  std_logic;
34      RX_FullState   : out std_logic_vector(imax(0, RX_FSTATE_BITS-1) downto 0);
35      RX_Overflow    : out std_logic;
36
37      -- External pins
38      UART_TX        : out std_logic;
39      UART_RX        : in  std_logic;
40      UART_RTS       : out std_logic;
41      UART_CTS       : in  std_logic
42    );
43  end entity;
```

Source file: io/uart/uart_fifo.vhdl

7.10.11 PoC.io.vga

These are VGA entities. . . .

PoC.io.vga Package

Source file: vga.pkg.vhdl

PoC.io.vga.phy

Entity Declaration:

Source file: io/vga/vga_phy.vhdl

PoC.io.vga.phy_ch7301c

The clock frequency must be the same as used for the timing module, e.g., 25 MHZ for VGA 640x480. A phase-shifted clock must be provided: - clk0 : 0 degrees - clk90 : 90 degrees

pixel_data(23 downto 16) : red pixel_data(15 downto 8) : green pixel_data(7 downto 0) : blue

The `reset_b`-pin must be driven by other logic (such as the reset button).

The IIC_interface is not part of this modules, as an IIC-master controls several slaves. The following registers must be set, see tests/ml505/vga_test_ml505.vhdl for an example.

Register	Value	Description
0x49 PM	0xC0 0xD0	Enable DVI, RGB bypass off Enable DVI, RGB bypass on
0x33 TPCP	0x08 if clk_freq <= 65 MHz else 0x06	
0x34 TPD	0x16 if clk_freq <= 65 MHz else 0x26	
0x36 TPF	0x60 if clk_freq <= 65 MHz else 0xA0	
0x1F IDF	0x80 0x90	when using SMT (VS0, HS0) when using CVT (VS1, HS0)
0x21 DC	0x09	Enable DAC if RGB bypass is on

Entity Declaration:

Source file: io/vga/vga_phy_ch7301c.vhdl

PoC.io.vga.timing

Configuration:

MODE = 0: VGA mode with 640x480 pixels, 60 Hz, frequency(clk) ~ 25 MHz MODE = 1: HD 720p with 1280x720 pixels, 60 Hz, frequency(clk) = 74,5 MHz MODE = 2: HD 1080p with 1920x1080 pixels, 60 Hz, frequency(clk) = 138,5 MHz

MODE = 2 uses reduced blanking => only suitable for LCDs.

For MODE = 0, CVT can be configured: - CVT = false: Use Safe Mode Timing (SMT).

> The legacy fall-back mode supported by CRTs as well as LCDs. HSync: low-active. VSync: low-active. frequency(clk) = 25.175 MHz. (25 MHz works => 31 kHz / 59 Hz)

- **CVT = true: The "new" Coordinated Video Timing (since 2003).** The CVT supports some new features, such as reduced blanking (for LCDs) or aspect ratio encoding. See the web for more details. Standard CRT-based timing (CVT-GTF) has been implemented for best compatibility: HSync: low-active. VSync: high-active. frequency(clk) = 23.75 MHz. (25 MHz works => 31 kHz / 62 Hz)

Usage:

The frequency of `clk` must be equal to the pixel clock frequency of the selected video mode, see also above.

When using analog output, the VGA color signals must be blanked, during horizontal and vertical beam return. This could be achieved by combinatorial "anding" the color value with "beam_on" (part of "phy_ctrl") inside the PHY.

When using digital output (DVI), then "beam_on" is equal to "DE" (Data Enable) of the DVI transmitter.

xvalid and yvalid show if xpos respectivly ypos are in a valid range. beam_on is '1' iff both xvalid and yvalid = '1'.

xpos and ypos also show the pixel location during blanking. This might be useful in some applications. But be careful, that the ranges differ between SMT and CVT.

Entity Declaration:

Source file: io/vga/vga_timing.vhdl

7.10.12 PoC.io Package

This package holds all component declarations for this namespace.

Source file: io.pkg.vhdl

7.10.13 PoC.io.7SegmentMux_BCD

This module is a 7 segment display controller that uses time multiplexing to control a common anode for each digit in the display. The shown characters are BCD encoded. A dot per digit is optional. A minus sign for negative numbers is supported.

Entity Declaration:

```
entity io_7SegmentMux_BCD is
  generic (
    CLOCK_FREQ       : FREQ         := 100 MHz;
    REFRESH_RATE     : FREQ         := 1 kHz;
    DIGITS           : positive     := 4
  );
  port (
    Clock            : in  std_logic;

    BCDDigits        : in  T_BCD_VECTOR(DIGITS - 1 downto 0);
    BCDDots          : in  std_logic_vector(DIGITS - 1 downto 0);

    SegmentControl   : out std_logic_vector(7 downto 0);
    DigitControl     : out std_logic_vector(DIGITS - 1 downto 0)
  );
end entity;
```

Source file: io/io_7SegmentMux_BCD.vhdl

7.10.14 PoC.io.7SegmentMux_HEX

This module is a 7 segment display controller that uses time multiplexing to control a common anode for each digit in the display. The shown characters are HEX encoded. A dot per digit is optional.

Entity Declaration:

```
entity io_7SegmentMux_HEX is
  generic (
    CLOCK_FREQ       : FREQ         := 100 MHz;
    REFRESH_RATE     : FREQ         := 1 kHz;
    DIGITS           : positive     := 4
  );
  port (
    Clock            : in  std_logic;

    HexDigits        : in  T_SLVV_4(DIGITS - 1 downto 0);
    HexDots          : in  std_logic_vector(DIGITS - 1 downto 0);

    SegmentControl   : out std_logic_vector(7 downto 0);
    DigitControl     : out std_logic_vector(DIGITS - 1 downto 0)
  );
end entity;
```

Source file: io/io_7SegmentMux_HEX.vhdl

7.10.15 PoC.io.Debounce

This module debounces several input pins preventing input changes following a previous one within the configured BOUNCE_TIME to pass. Internally, the forwarded state is locked for, at least, this BOUNCE_TIME. As the backing timer is restarted on every input fluctuation, the next passing input update must have seen a stabilized input.

The parameter COMMON_LOCK uses a single internal timer for all processed inputs. Thus, all inputs must stabilize before any one may pass changed. This option is usually fully acceptable for user inputs such as push buttons.

The parameter ADD_INPUT_SYNCHRONIZERS triggers the optional instantiation of a two-FF input synchronizer on each input bit.

Entity Declaration:

```
entity io_Debounce is
  generic (
    CLOCK_FREQ               : FREQ;
    BOUNCE_TIME              : time;
    BITS                     : positive := 1;
    INIT                     : std_logic_vector    := x"00000000"; -- initial state␣
↪of Output
    ADD_INPUT_SYNCHRONIZERS : boolean  := true;
    COMMON_LOCK              : boolean  := false
  );
  port (
    Clock    : in  std_logic;
    Reset    : in  std_logic             := '0';
    Input    : in  std_logic_vector(BITS-1 downto 0);
    Output   : out std_logic_vector(BITS-1 downto 0) := resize(descend(INIT), BITS)
  );
end entity;
```

Source file: io/io_Debounce.vhdl

7.10.16 PoC.io.FanControl

```
This module generates a PWM signal for a 3-pin (transistor controlled) or
4-pin fan header. The FPGAs temperature is read from device specific system
monitors (normal, user temperature, over temperature).

For example the Xilinx System Monitors are configured as follows:

                                                                |
↪                                                                    /-----\
Temp_ov  on=80   |       -       -       -       -       -       -       /-------/ ␣
↪                                \
                                                                |
↪                                 /                             |                  ␣
↪             \
Temp_ov off=60   |       -       -       -       -       -       /       -       - ␣
↪     -       -       |       -       -       -       -       \----\
                                                                |
↪                      /                                        |                  ␣
↪                                           \
                                                                |
↪                     /                                                 |          ␣
↪                                          | \
```

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```
Temp_us  on=35  |       -        /---/                                                  | ␣
↪                                                      |      \
Temp_us off=30  |       -       /       -       -|-     -       -       -       -  ␣
↪      -       |       -       -       -       -       -       -       -|-  \------
↪\
                                                                 |  /              |␣
↪                                                  |                               ␣
↪                      |                                       \
----------------|--------|------------|--------------|----------|---------
pwm =                                                  |               min       |      ␣
↪medium          |               max                                  |       medium ␣
↪|       min
```

Entity Declaration:

```
entity io_FanControl is
  generic (
    CLOCK_FREQ               : FREQ;
    ADD_INPUT_SYNCHRONIZERS : boolean     := TRUE;
    ENABLE_TACHO             : boolean     := FALSE
  );
  port (
    -- Global Control
    Clock                    : in  std_logic;
    Reset                    : in  std_logic;

    -- Fan Control derived from internal System Health Monitor
    Fan_PWM                  : out std_logic;

    -- Decoding of Speed Sensor (Requires ENABLE_TACHO)
    Fan_Tacho       : in  std_logic := 'X';
    TachoFrequency : out std_logic_vector(15 downto 0)
  );
end entity;
```

Source file: io/io_FanControl.vhdl

7.10.17 PoC.io.FrequencyCounter

Todo: No documentation available.

Entity Declaration:

```
entity io_FrequencyCounter is
  generic (
    CLOCK_FREQ                : FREQ                    := 100 MHz;
    TIMEBASE                  : time                    := 1 sec;
    RESOLUTION                : positive                := 8
  );
  port (
    Clock        : in  std_logic;
    Reset        : in  std_logic;
    FreqIn       : in  std_logic;
    FreqOut      : out std_logic_vector(RESOLUTION - 1 downto 0)
```

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```
  );
end entity;
```

Source file: io/io_FrequencyCounter.vhdl

7.10.18 PoC.io.GlitchFilter

This module filters glitches on a wire. The high and low spike suppression cycle counts can be configured.

Entity Declaration:

```
entity io_GlitchFilter is
  generic (
    HIGH_SPIKE_SUPPRESSION_CYCLES     : natural       := 5;
    LOW_SPIKE_SUPPRESSION_CYCLES      : natural       := 5
  );
  port (
    Clock    : in  std_logic;
    Input    : in  std_logic;
    Output   : out std_logic
  );
end entity;
```

Source file: io/io_GlitchFilter.vhdl

7.10.19 PoC.io.KeyPadScanner

This module drives a one-hot encoded column vector to read back a rows vector. By scanning column-by-column it's possible to extract the current button state of the whole keypad. The scanner uses high-active logic. The keypad size and scan frequency can be configured. The outputed signal matrix is not debounced.

Entity Declaration:

```
entity io_KeyPadScanner is
  generic (
    CLOCK_FREQ               : FREQ        := 100 MHz;
    SCAN_FREQ                : FREQ        := 1 kHz;
    ROWS                     : positive    := 4;
    COLUMNS                  : positive    := 4;
    ADD_INPUT_SYNCHRONIZERS  : boolean     := TRUE
  );
  port (
    Clock         : in  std_logic;
    Reset         : in  std_logic;
    -- Matrix interface
    KeyPadMatrix  : out T_SLM(COLUMNS - 1 downto 0, ROWS - 1 downto 0);
    -- KeyPad interface
    ColumnVector  : out std_logic_vector(COLUMNS - 1 downto 0);
    RowVector     : in  std_logic_vector(ROWS - 1 downto 0)
  );
end entity;
```

Source file: io/io_KeyPadScanner.vhdl

7.10.20 PoC.io.PulseWidthModulation

This module generates a pulse width modulated signal, that can be configured in frequency (`PWM_FREQ`) and modulation granularity (`PWM_RESOLUTION`).

Entity Declaration:

```
entity io_PulseWidthModulation is
  generic (
    CLOCK_FREQ                : FREQ                    := 100 MHz;
    PWM_FREQ                  : FREQ                    := 1 kHz;
    PWM_RESOLUTION            : positive                := 8
  );
  port (
    Clock         : in  std_logic;
    Reset         : in  std_logic;
    PWMIn         : in  std_logic_vector(PWM_RESOLUTION - 1 downto 0);
    PWMOut        : out std_logic
  );
end entity;
```

Source file: io/io_PulseWidthModulation.vhdl

7.10.21 PoC.io.TimingCounter

This down-counter can be configured with a `TIMING_TABLE` (a ROM), from which the initial counter value is loaded. The table index can be selected by `Slot`. `Timeout` is a registered output. Up to 16 values fit into one ROM consisting of `log2ceilnz(imax(TIMING_TABLE)) + 1` 6-input LUTs.

Entity Declaration:

```
entity io_TimingCounter is
  generic (
    TIMING_TABLE  : T_NATVEC                                          -- timing␣
↪table
  );
  port (
    Clock         : in  std_logic;                                    -- clock
    Enable        : in  std_logic;                                    -- enable␣
↪counter
    Load          : in  std_logic;                                    -- load␣
↪Timing Value from TIMING_TABLE selected by slot
    Slot          : in  natural range 0 to (TIMING_TABLE'length - 1); --
    Timeout       : out std_logic                                     -- timing␣
↪reached
  );
end entity;
```

Source file: io/io_TimingCounter.vhdl

7.11 PoC.mem

The namespace `PoC.mem` offers different on-chip and off-chip memory and memory-controller implementations.

Sub-Namespaces

- *PoC.mem.ddr2* - DDR2 memory controllers
- *PoC.mem.ddr3* - DDR3 memory controllers
- *PoC.mem.lut* - Lookup-Table (LUT) implementations
- *PoC.mem.ocram* - On-Chip RAM abstraction layer
- *PoC.mem.ocrom* - On-Chip ROM abstraction layer
- *PoC.mem.sdram* - SDRAM controllers

Package

PoC.mem

7.11.1 PoC.mem Package

This package holds all component declarations, types and functions of the *PoC.mem* namespace.

It provides the following enumerations:

- `T_MEM_FILEFORMAT` specifies whether a file is in Intel Hex, Lattice Mem, or Xilinx Mem format.
- `T_MEM_CONTENT` specifies whether data in text file is in binary, decimal or hexadecimal format.

It provides the following functions:

- `mem_FileExtension` returns the file extension of a given filename.
- `mem_ReadMemoryFile` reads initial memory content from a given file.

Source file: mem.pkg.vhdl

7.11.2 PoC.mem.ddr2

The namespace `PoC.mem.ddr2` is designated for own implementations of DDR2 memory controllers as well as for adapters for vendor-specific implementations. At the top-level, all controllers and adapters provide the same simple memory interface to the user application.

Entities

- *PoC.mem.ddr2.mem2mig_adapter_Spartan6* - Adapter for the Xilinx MIG core for Spartan-6 FPGAs

PoC.mem.ddr2.mem2mig_adapter_Spartan6

Adapter between the *PoC.Mem* interface and the User Interface of the Xilinx MIG IP core for the Spartan-6 FPGA Memory Controller Block (MCB). The MCB can be configured to have multiple ports. One instance of this adapter is required for every port. The control signals for one port of the MIG IP core are prefixed by "cX_pY", meaning port Y on controller X.

Simplifies the User Interface ("user") of the Xilinx MIG IP core (UG388). The PoC.Mem interface provides single-cycle fully pipelined read/write access to the memory. All accesses are word-aligned. Always all bytes of a word are written to the memory. More details can be found *here*.

Generic parameters:

- D_BITS: Data bus width of the PoC.Mem and MIG / MCBinterface. Also size of one word in bits.
- MEM_A_BITS: Address bus width of the PoC.Mem interface.
- APP_A_BTIS: Address bus width of the MIG / MCB interface.

Containts only combinational logic.

Entity Declaration:

```
entity ddr2_mem2mig_adapter_Spartan6 is

  generic (
    D_BITS      : positive;
    MEM_A_BITS  : positive;
    APP_A_BITS  : positive
  );

  port (
    -- PoC.Mem interface
    mem_req    : in  std_logic;
    mem_write  : in  std_logic;
    mem_addr   : in  unsigned(MEM_A_BITS-1 downto 0);
    mem_wdata  : in  std_logic_vector(D_BITS-1 downto 0);
    mem_wmask  : in  std_logic_vector(D_BITS/8-1 downto 0) := (others => '0');
    mem_rdy    : out std_logic;
    mem_rstb   : out std_logic;
    mem_rdata  : out std_logic_vector(D_BITS-1 downto 0);

    -- Xilinx MIG IP Core interface
    mig_calib_done     : in  std_logic;
    mig_cmd_full       : in  std_logic;
    mig_wr_full        : in  std_logic;
    mig_rd_empty       : in  std_logic;
    mig_rd_data        : in  std_logic_vector((D_BITS)-1 downto 0);
    mig_cmd_instr      : out std_logic_vector(2 downto 0);
    mig_cmd_en         : out std_logic;
    mig_cmd_bl         : out std_logic_vector(5 downto 0);
    mig_cmd_byte_addr  : out std_logic_vector(APP_A_BITS-1 downto 0);
    mig_wr_data        : out std_logic_vector((D_BITS)-1 downto 0);
    mig_wr_mask        : out std_logic_vector((D_BITS)/8-1 downto 0);
    mig_wr_en          : out std_logic;
    mig_rd_en          : out std_logic
  );

end entity ddr2_mem2mig_adapter_Spartan6;
```

Source file: mem/ddr2/ddr2_mem2mig_adapter_Spartan6.vhdl

7.11.3 PoC.mem.ddr3

The namespace `PoC.mem.ddr3` is designated for own implementations of DDR3 memory controllers as well as for adapters for vendor-specific implementations. At the top-level, all controllers and adapters provide the same simple memory interface to the user application.

Entities

- *PoC.mem.ddr3.mem2mig_adapter_Series7* - Adapter for the Xilinx MIG core for 7-Series FPGAs

PoC.mem.ddr3.mem2mig_adapter_Series7

Adapter between the *PoC.Mem* interface and the application interface ("app") of the Xilinx MIG IP core for 7-Series FPGAs.

Simplifies the application interface ("app") of the Xilinx MIG IP core. The PoC.Mem interface provides single-cycle fully pipelined read/write access to the memory. All accesses are word-aligned. Always all bytes of a word are written to the memory. More details can be found *here*.

Generic parameters:

- D_BITS: Data bus width of the PoC.Mem and "app" interface. Also size of one word in bits.
- DQ_BITS: Size of data bus between memory controller and external memory (DIMM, SoDIMM).
- MEM_A_BITS: Address bus width of the PoC.Mem interface.
- APP_A_BTIS: Address bus width of the "app" interface.

Containts only combinational logic.

Entity Declaration:

```
entity ddr3_mem2mig_adapter_Series7 is

  generic (
    D_BITS      : positive;
    DQ_BITS     : positive;
    MEM_A_BITS  : positive;
    APP_A_BITS  : positive
  );

  port (
    -- PoC.Mem interface
    mem_req    : in  std_logic;
    mem_write  : in  std_logic;
    mem_addr   : in  unsigned(MEM_A_BITS-1 downto 0);
    mem_wdata  : in  std_logic_vector(D_BITS-1 downto 0);
    mem_wmask  : in  std_logic_vector(D_BITS/8-1 downto 0) := (others => '0');
    mem_rdy    : out std_logic;
    mem_rstb   : out std_logic;
    mem_rdata  : out std_logic_vector(D_BITS-1 downto 0);

    -- Xilinx MIG IP Core interface
    init_calib_complete : in  std_logic;
    app_rd_data         : in  std_logic_vector((D_BITS)-1 downto 0);
    app_rd_data_end     : in  std_logic;
    app_rd_data_valid   : in  std_logic;
    app_rdy             : in  std_logic;
    app_wdf_rdy         : in  std_logic;
    app_addr            : out std_logic_vector(APP_A_BITS-1 downto 0);
    app_cmd             : out std_logic_vector(2 downto 0);
    app_en              : out std_logic;
    app_wdf_data        : out std_logic_vector((D_BITS)-1 downto 0);
    app_wdf_end         : out std_logic;
    app_wdf_mask        : out std_logic_vector((D_BITS)/8-1 downto 0);
    app_wdf_wren        : out std_logic
  );

end entity ddr3_mem2mig_adapter_Series7;
```

Source file: mem/ddr3/ddr3_mem2mig_adapter_Series7.vhdl

7.11.4 PoC.mem.lut

The namespace `PoC.mem.lut` offers different lookup-tables (LUTs).

Entities

- *PoC.mem.lut.Sine* - a Sine implementation with 1,2 or 4 quadrants.

PoC.mem.lut.Sine

Todo: No documentation available.

Entity Declaration:

Source file: mem/lut/lut_Sine.vhdl

7.11.5 PoC.mem.ocram

The namespace `PoC.mem.ocram` offers different on-chip RAM abstractions.

Package

The package PoC.mem.ocram holds all component declarations for this namespace.

```
library PoC;
use     PoC.ocram.all;
```

Entities

- *PoC.mem.ocram.sp* - An on-chip RAM with a single port interface.
- *PoC.mem.ocram.sdp* - An on-chip RAM with a simple dual-port interface.
- *PoC.mem.ocram.sdp_wf* - An on-chip RAM with a simple dual-port interface and write-first behavior.
- *PoC.mem.ocram.tdp* - An on-chip RAM with a true dual-port interface.
- *PoC.mem.ocram.tdp_wf* - An on-chip RAM with a true dual-port interface and write-first behavior.

Simulation Helper

- *PoC.mem.ocram.tdp_sim* - Simulation model of on-chip RAM with a true dual port interface.

Deprecated Entities

- *PoC.mem.ocram.esdp* - An on-chip RAM with an extended simple dual port interface.

PoC.mem.ocram Package

Source file: ocram.pkg.vhdl

PoC.mem.ocram.sp

Inferring / instantiating single port memory, with:

- single clock, clock enable,
- 1 read/write port.

Command Truth Table:

ce	we	Command
0	X	No operation
1	0	Read from memory
1	1	Write to memory

Both reading and writing are synchronous to the rising-edge of the clock. Thus, when reading, the memory data will be outputted after the clock edge, i.e, in the following clock cycle.

When writing data, the read output will output the new data (in the following clock cycle) which is aka. "write-first behavior". This behavior also applies to Altera M20K memory blocks as described in the Altera: "Stratix 5 Device Handbook" (S5-5V1). The documentation in the Altera: "Embedded Memory User Guide" (UG-01068) is wrong.

Entity Declaration:

```
entity ocram_sp is
  generic (
    A_BITS     : positive;                                  -- number of address bits
    D_BITS     : positive;                                  -- number of data bits
    FILENAME   : string    := ""                            -- file-name for RAM␣
↪initialization
  );
  port (
    clk : in  std_logic;                                    -- clock
    ce  : in  std_logic;                                    -- clock enable
    we  : in  std_logic;                                    -- write enable
    a   : in unsigned(A_BITS-1 downto 0);                   -- address
    d   : in std_logic_vector(D_BITS-1 downto 0);           -- write data
    q   : out std_logic_vector(D_BITS-1 downto 0)           -- read output
  );
end entity;
```

Source file: mem/ocram/ocram_sp.vhdl

PoC.mem.ocram.sdp

Inferring / instantiating simple dual-port memory, with:

- dual clock, clock enable,
- 1 read port plus 1 write port.

Both reading and writing are synchronous to the rising-edge of the clock. Thus, when reading, the memory data will be outputted after the clock edge, i.e, in the following clock cycle.

The generalized behavior across Altera and Xilinx FPGAs since Stratix/Cyclone and Spartan-3/Virtex-5, respectively, is as follows:

Mixed-Port Read-During-Write When reading at the write address, the read value will be unknown which is aka. "don't care behavior". This applies to all reads (at the same address) which are issued during the write-cycle time, which starts at the rising-edge of the write clock and (in the worst case) extends until the next rising-edge of the write clock.

For simulation, always our dedicated simulation model *PoC.mem.ocram.tdp_sim* is used.

Entity Declaration:

```
entity ocram_sdp is
  generic (
    A_BITS     : positive;                                  -- number of address bits
    D_BITS     : positive;                                  -- number of data bits
    FILENAME   : string    := ""                            -- file-name for RAM␣
↪initialization
  );
  port (
    rclk  : in  std_logic;                                  -- read clock
    rce   : in  std_logic;                                  -- read clock-enable
```

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```
    wclk   : in  std_logic;                                -- write clock
    wce    : in  std_logic;                                -- write clock-enable
    we     : in  std_logic;                                -- write enable
    ra     : in  unsigned(A_BITS-1 downto 0);              -- read address
    wa     : in  unsigned(A_BITS-1 downto 0);              -- write address
    d      : in  std_logic_vector(D_BITS-1 downto 0);      -- data in
    q      : out std_logic_vector(D_BITS-1 downto 0)       -- data out
  );
end entity;
```

Source file: mem/ocram/ocram_sdp.vhdl

PoC.mem.ocram.sdp_wf

Inferring / instantiating simple dual-port memory, with:

- single clock, clock enable,
- 1 read port plus 1 write port.

Command truth table:

ce	we	Command
0	X	No operation
1	0	Read only from memory
1	1	Read from and Write to memory

Both reading and writing are synchronous to the rising-edge of the clock. Thus, when reading, the memory data will be outputted after the clock edge, i.e, in the following clock cycle.

Mixed-Port Read-During-Write When reading at the write address, the read value will be the new data, aka. "write-first behavior". Of course, the read is still synchronous, i.e, the latency is still one clock cyle.

Entity Declaration:

```
entity ocram_sdp_wf is
  generic (
    A_BITS    : positive;                                -- number of address bits
    D_BITS    : positive;                                -- number of data bits
    FILENAME  : string    := ""                          -- file-name for RAM␣
↪initialization
  );
  port (
    clk : in  std_logic;                                 -- clock
    ce  : in  std_logic;                                 -- clock-enable
    we  : in  std_logic;                                 -- write enable
    ra  : in  unsigned(A_BITS-1 downto 0);               -- read address
    wa  : in  unsigned(A_BITS-1 downto 0);               -- write address
    d   : in  std_logic_vector(D_BITS-1 downto 0);       -- data in
    q   : out std_logic_vector(D_BITS-1 downto 0)        -- data out
  );
end entity;
```

Source file: mem/ocram/ocram_sdp_wf.vhdl

PoC.mem.ocram.tdp

Inferring / instantiating true dual-port memory, with:

- dual clock, clock enable,
- 2 read/write ports.

Command truth table for port 1, same applies to port 2:

ce1	we1	Command
0	X	No operation
1	0	Read from memory
1	1	Write to memory

Both reading and writing are synchronous to the rising-edge of the clock. Thus, when reading, the memory data will be outputted after the clock edge, i.e, in the following clock cycle.

The generalized behavior across Altera and Xilinx FPGAs since Stratix/Cyclone and Spartan-3/Virtex-5, respectively, is as follows:

Same-Port Read-During-Write When writing data through port 1, the read output of the same port (`q1`) will output the new data (`d1`, in the following clock cycle) which is aka. "write-first behavior".

Same applies to port 2.

Mixed-Port Read-During-Write When reading at the write address, the read value will be unknown which is aka. "don't care behavior". This applies to all reads (at the same address) which are issued during the write-cycle time, which starts at the rising-edge of the write clock and (in the worst case) extends until the next rising-edge of that write clock.

For simulation, always our dedicated simulation model *PoC.mem.ocram.tdp_sim* is used.

Entity Declaration:

```
entity ocram_tdp is
  generic (
    A_BITS     : positive;                          -- number of address bits
    D_BITS     : positive;                          -- number of data bits
    FILENAME   : string    := ""                    -- file-name for RAM␣
↪initialization
  );
  port (
    clk1 : in std_logic;                            -- clock for 1st port
    clk2 : in std_logic;                            -- clock for 2nd port
    ce1 : in  std_logic;                            -- clock-enable for 1st port
    ce2 : in  std_logic;                            -- clock-enable for 2nd port
    we1 : in  std_logic;                            -- write-enable for 1st port
    we2 : in  std_logic;                            -- write-enable for 2nd port
    a1   : in unsigned(A_BITS-1 downto 0);          -- address for 1st port
    a2   : in unsigned(A_BITS-1 downto 0);          -- address for 2nd port
    d1   : in std_logic_vector(D_BITS-1 downto 0);  -- write-data for 1st port
    d2   : in std_logic_vector(D_BITS-1 downto 0);  -- write-data for 2nd port
    q1   : out std_logic_vector(D_BITS-1 downto 0); -- read-data from 1st port
    q2   : out std_logic_vector(D_BITS-1 downto 0)  -- read-data from 2nd port
  );
end entity;
```

Source file: mem/ocram/ocram_tdp.vhdl

PoC.mem.ocram.tdp_wf

Inferring / instantiating true dual-port memory, with:

- single clock, clock enable,

- 2 read/write ports.

Command truth table:

ce	we1	we2	Command
0	X	X	No operation
1	0	0	Read only from memory
1	0	1	Read from memory on port 1, write to memory on port 2
1	1	0	Write to memory on port 1, read from memory on port 2
1	1	1	Write to memory on both ports

Both reads and writes are synchronous to the clock.

The generalized behavior across Altera and Xilinx FPGAs since Stratix/Cyclone and Spartan-3/Virtex-5, respectively, is as follows:

Same-Port Read-During-Write When writing data through port 1, the read output of the same port (`q1`) will output the new data (`d1`, in the following clock cycle) which is aka. "write-first behavior".

Same applies to port 2.

Mixed-Port Read-During-Write When reading at the write address, the read value will be the new data, aka. "write-first behavior". Of course, the read is still synchronous, i.e, the latency is still one clock cyle.

If a write is issued on both ports to the same address, then the output of this unit and the content of the addressed memory cell are undefined.

For simulation, always our dedicated simulation model *PoC.mem.ocram.tdp_sim* is used.

Entity Declaration:

```
entity ocram_tdp_wf is
  generic (
    A_BITS    : positive;                          -- number of address bits
    D_BITS    : positive;                          -- number of data bits
    FILENAME  : string    := ""                    -- file-name for RAM␣
↪initialization
  );
  port (
    clk : in  std_logic;                           -- clock
    ce  : in  std_logic;                           -- clock-enable
    we1 : in  std_logic;                           -- write-enable for 1st port
    we2 : in  std_logic;                           -- write-enable for 2nd port
    a1   : in unsigned(A_BITS-1 downto 0);         -- address for 1st port
    a2   : in unsigned(A_BITS-1 downto 0);         -- address for 2nd port
    d1   : in std_logic_vector(D_BITS-1 downto 0); -- write-data for 1st port
    d2   : in std_logic_vector(D_BITS-1 downto 0); -- write-data for 2nd port
    q1   : out std_logic_vector(D_BITS-1 downto 0); -- read-data from 1st port
    q2   : out std_logic_vector(D_BITS-1 downto 0)  -- read-data from 2nd port
  );
end entity;
```

Source file: mem/ocram/ocram_tdp_wf.vhdl

PoC.mem.ocram.tdp_sim

Simulation model for true dual-port memory, with:

- dual clock, clock enable,
- 2 read/write ports.

The interface matches that of the IP core PoC.mem.ocram.tdp. But the implementation there is restricted to the description supported by various synthesis compilers. The implementation here also simulates the correct Mixed-Port Read-During-Write Behavior and handles X propagation.

Entity Declaration:

```
entity ocram_tdp_sim is
  generic (
    A_BITS    : positive;                                -- number of address bits
    D_BITS    : positive;                                -- number of data bits
    FILENAME  : string    := ""                          -- file-name for RAM␣
↪initialization
  );
  port (
    clk1 : in std_logic;                                 -- clock for 1st port
    clk2 : in std_logic;                                 -- clock for 2nd port
    ce1 : in  std_logic;                                 -- clock-enable for 1st port
    ce2 : in  std_logic;                                 -- clock-enable for 2nd port
    we1 : in  std_logic;                                 -- write-enable for 1st port
    we2 : in  std_logic;                                 -- write-enable for 2nd port
    a1   : in unsigned(A_BITS-1 downto 0);               -- address for 1st port
    a2   : in unsigned(A_BITS-1 downto 0);               -- address for 2nd port
    d1   : in std_logic_vector(D_BITS-1 downto 0);       -- write-data for 1st port
    d2   : in std_logic_vector(D_BITS-1 downto 0);       -- write-data for 2nd port
    q1   : out std_logic_vector(D_BITS-1 downto 0);      -- read-data from 1st port
    q2   : out std_logic_vector(D_BITS-1 downto 0)       -- read-data from 2nd port
  );
end entity;
```

Source file: mem/ocram/ocram_tdp_sim.vhdl

PoC.mem.ocram.esdp

Inferring / instantiating enhanced simple dual-port memory, with:

- dual clock, clock enable,
- 1 read/write port (1st port) plus 1 read port (2nd port).

Deprecated since version 1.1: **Please use** *PoC.mem.ocram.tdp* **for new designs. This component has been provided because older FPGA compilers where not able to infer true dual-port memory from an RTL description.**

Command truth table for port 1:

ce1	we1	Command
0	X	No operation
1	0	Read from memory
1	1	Write to memory

Command truth table for port 2:

ce2	Command
0	No operation
1	Read from memory

Both reading and writing are synchronous to the rising-edge of the clock. Thus, when reading, the memory data will be outputted after the clock edge, i.e, in the following clock cycle.

The generalized behavior across Altera and Xilinx FPGAs since Stratix/Cyclone and Spartan-3/Virtex-5, respectively, is as follows:

Same-Port Read-During-Write When writing data through port 1, the read output of the same port (`q1`) will output the new data (`d1`, in the following clock cycle) which is aka. "write-first behavior".

Mixed-Port Read-During-Write When reading at the write address, the read value will be unknown which is aka. "don't care behavior". This applies to all reads (at the same address) which are issued during the write-cycle time, which starts at the rising-edge of the write clock (`clk1`) and (in the worst case) extends until the next rising-edge of the write clock.

For simulation, always our dedicated simulation model *PoC.mem.ocram.tdp_sim* is used.

Entity Declaration:

```
entity ocram_esdp is
  generic (
    A_BITS     : positive;                                  -- number of address bits
    D_BITS     : positive;                                  -- number of data bits
    FILENAME   : string     := ""                           -- file-name for RAM␣
↪initialization
  );
  port (
    clk1 : in std_logic;                                    -- clock for 1st port
    clk2 : in std_logic;                                    -- clock for 2nd port
    ce1 : in  std_logic;                                    -- clock-enable for 1st port
    ce2 : in  std_logic;                                    -- clock-enable for 2nd port
    we1 : in  std_logic;                                    -- write-enable for 1st port
    a1   : in unsigned(A_BITS-1 downto 0);                  -- address for 1st port
    a2   : in unsigned(A_BITS-1 downto 0);                  -- address for 2nd port
    d1   : in std_logic_vector(D_BITS-1 downto 0);          -- write-data for 1st port
    q1   : out std_logic_vector(D_BITS-1 downto 0);         -- read-data from 1st port
    q2   : out std_logic_vector(D_BITS-1 downto 0)          -- read-data from 2nd port
  );
end entity;
```

Source file: mem/ocram/ocram_esdp.vhdl

7.11.6 PoC.mem.ocrom

The namespace `PoC.mem.ocrom` offers different on-chip ROM abstractions.

Package

The package PoC.mem.ocrom holds all component declarations for this namespace.

```
library PoC;
use     PoC.ocrom.all;
```

Entities

- *ocrom_sp* is a on-chip RAM with a single port interface.
- *ocrom_dp* is a on-chip RAM with a dual port interface.

PoC.mem.ocrom Package

Source file: ocrom.pkg.vhdl

PoC.mem.ocrom.sp

Inferring / instantiating single-port read-only memory

- single clock, clock enable
- 1 read port

Entity Declaration:

```
entity ocrom_sp is
  generic (
    A_BITS     : positive;
    D_BITS     : positive;
    FILENAME   : string    := ""
  );
  port (
    clk : in  std_logic;
    ce  : in  std_logic;
    a   : in  unsigned(A_BITS-1 downto 0);
    q   : out std_logic_vector(D_BITS-1 downto 0)
  );
end entity;
```

Source file: mem/ocrom/ocrom_sp.vhdl

PoC.mem.ocrom.dp

Inferring / instantiating dual-port read-only memory, with:

- dual clock, clock enable,
- 2 read ports.

The generalized behavior across Altera and Xilinx FPGAs since Stratix/Cyclone and Spartan-3/Virtex-5, respectively, is as follows:

WARNING: The simulated behavior on RT-level is not correct.

TODO: add timing diagram TODO: implement correct behavior for RT-level simulation

Entity Declaration:

```
entity ocrom_dp is
  generic (
    A_BITS     : positive;
    D_BITS     : positive;
    FILENAME   : string    := ""
  );
  port (
    clk1 : in std_logic;
    clk2 : in std_logic;
    ce1 : in  std_logic;
    ce2 : in  std_logic;
    a1   : in unsigned(A_BITS-1 downto 0);
    a2   : in unsigned(A_BITS-1 downto 0);
    q1   : out std_logic_vector(D_BITS-1 downto 0);
    q2   : out std_logic_vector(D_BITS-1 downto 0)
  );
end entity;
```

Source file: mem/ocrom/ocrom_dp.vhdl

7.11.7 PoC.mem.sdram

The namespace `PoC.mem.sdram` offers components for the access of external SDRAMs. A common finite state-machine is used to address the memory via banks, rows and columns. Different physical layers are provide for the single-data-rate (SDR) or double-data-rate (DDR, DDR2, ...) data bus. One has to instantiate the specific module required by the FPGA board.

SDRAM Controller for the Altera DE0 Board

The module *sdram_ctrl_de0* combines the finite state machine *sdram_ctrl_fsm* and the DE0 specific physical layer *sdram_ctrl_phy_de0*. It has been tested with the IS42S16400F SDR memory at a frequency of 133 MHz. A usage example is given in PoC-Examples.

SDRAM Controller for the Xilinx Spartan-3E Starter Kit (S3ESK)

The module *sdram_ctrl_s3esk* combines the finite state machine *sdram_ctrl_fsm* and the S3ESK specific physical layer *sdram_ctrl_phy_s3esk*. It has been tested with the MT46V32M16-6T DDR memory at a frequency of 100 MHz (DDR-200). A usage example is given in PoC-Examples.

Note: See also *PoC.xil.mig* for board specific memory controller implementations created by Xilinx's Memory Interface Generator (MIG).

PoC.mem.sdram.ctrl_fsm

This file contains the FSM as well as parts of the datapath. The board specific physical layer is defined in another file.

Configuration

SDRAM_TYPE activates some special cases:

- 0 for SDR-SDRAM
- 1 for DDR-SDRAM
- 2 for DDR2-SDRAM (no special support yet like ODT)

2**A_BITS specifies the number of memory cells in the SDRAM. This is the size of th memory in bits divided by the native data-path width of the SDRAM (also in bits).

D_BITS is the native data-path width of the SDRAM. The width might be doubled by the physical interface for DDR interfaces.

Furthermore, the memory array is divided into 2**R_BITS rows, 2**C_BITS columns and 2**B_BITS banks.

Note: For example, the MT46V32M16 has 512 Mbit = 8M x 4 banks x 16 bit = 32M cells x 16 bit, with 8K rows and 1K columns. Thus, the configuration is:

- A_BITS = $\log_2(32\,\mathrm{M}) = 25$
- D_BITS = 16
- data-path width of phy on user side: 32-bit because of DDR
- R_BITS = $\log_2(8\,\mathrm{K}) = 13$

- C_BITS = $\log_2(1\,\mathrm{K}) = 10$
- B_BITS = $\log_2(4) = 2$

Set CAS latency (CL, MR_CL) and burst length (BL, MR_BL) according to your needs.

If you have a DDR-SDRAM then set INIT_DLL = true, otherwise false.

The definition and values of generics T_* can be calculated from the datasheets of the specific SDRAM (e.g. MT46V). Just divide the minimum/maximum times by clock period. Auto refreshs are applied periodically, the datasheet either specifies the average refresh interval (T_REFI) or the total refresh cycle time (T_REF). In the latter case, divide the total time by the row count to get the average refresh interval. Substract about 50 clock cycles to account for pending read/writes.

INIT_WAIT specifies the time period to wait after the SDRAM is powered up. It is typically 100–200 us long, see datasheet. The waiting time is specified in number of average refresh periods (specified by T_REFI): INIT_WAIT = ceil(wait_time / clock_period / T_REFI) e.g. INIT_WAIT = ceil(200 us / 10 ns / 700) = 29

Operation

After user_cmd_valid is asserted high, the command (user_write) and address (user_addr) must be hold until user_got_cmd is asserted.

The FSM automatically waits for user_wdata_valid on writes. The data should be available soon. Otherwise the auto refresh might fail. The FSM only waits for the first word to write. All successive words of a burst must be valid in the following cycles. (A burst can't be stalled.) ATTENTION: During writes, user_cmd_got is asserted only if user_wdata_valid is set.

The write data must directly connected to the physical layer.

Entity Declaration:

```
entity sdram_ctrl_fsm is
  generic (
    SDRAM_TYPE : natural;                -- SDRAM type

    A_BITS       : positive;             -- log2ceil(memory cell count)
    D_BITS       : positive;             -- native data width
    R_BITS       : positive;             -- log2ceil(rows)
    C_BITS       : positive;             -- log2ceil(columns)
    B_BITS       : positive;             -- log2ceil(banks)

    CL : positive;  -- CAS Latency in clock cycles
    BL : positive;  -- Burst Length

    T_MRD      : integer;                -- in clock cycles
    T_RAS      : integer;                -- in clock cycles
    T_RCD      : integer;                -- in clock cycles
    T_RFC      : integer;                -- (or T_RC) in clock cycles
    T_RP       : integer;                -- in clock cycles
    T_WR       : integer;                -- in clock cycles
    T_WTR      : integer;                -- in clock cycles
    T_REFI     : integer;                -- in clock cycles
    INIT_WAIT : integer);                -- in T_REFI periods
  port (
    clk : in std_logic;
    rst : in std_logic;

    user_cmd_valid   : in  std_logic;
    user_wdata_valid : in  std_logic;
```

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```
    user_write       : in  std_logic;
    user_addr        : in  std_logic_vector(A_BITS-1 downto 0);
    user_got_cmd     : out std_logic;
    user_got_wdata   : out std_logic;

    sd_cke_nxt : out std_logic;
    sd_cs_nxt  : out std_logic;
    sd_ras_nxt : out std_logic;
    sd_cas_nxt : out std_logic;
    sd_we_nxt  : out std_logic;
    sd_a_nxt   : out std_logic_vector(imax(R_BITS,C_BITS+1)-1 downto 0);
    sd_ba_nxt  : out std_logic_vector(B_BITS-1 downto 0);
    rden_nxt   : out std_logic;
    wren_nxt   : out std_logic);


end sdram_ctrl_fsm;
```

Source file: mem/sdram/sdram_ctrl_fsm.vhdl

PoC.mem.sdram.ctrl_de0

Complete controller for ISSI SDR-SDRAM for Altera DE0 Board.

SDRAM Device: IS42S16400F

Configuration

Parameter	Description
CLK_PERIOD	Clock period in nano seconds. All SDRAM timings are calculated for the device stated above.
CL	CAS latency, choose according to clock frequency.
BL	Burst length. Choose BL=1 for single cycle memory transactions as required for the PoC.Mem interface.

Tested with: CLK_PERIOD = 7.5 (133 MHz), CL=2, BL=1.

Operation

Command, address and write data is sampled with `clk`. Read data is also aligned with `clk`.

For description on `clkout` see *sdram_ctrl_phy_de0*.

Synchronous resets are used.

Entity Declaration:

```
entity sdram_ctrl_de0 is

  generic (
    CLK_PERIOD   : real;
    CL           : positive;
    BL           : positive);

  port (
    clk         : in    std_logic;
```

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```
    clkout      : in    std_logic;
    rst         : in    std_logic;

    user_cmd_valid   : in  std_logic;
    user_wdata_valid : in  std_logic;
    user_write       : in  std_logic;
    user_addr        : in  std_logic_vector(21 downto 0);
    user_wdata       : in  std_logic_vector(15 downto 0);
    user_got_cmd     : out std_logic;
    user_got_wdata   : out std_logic;
    user_rdata       : out std_logic_vector(15 downto 0);
    user_rstb        : out std_logic;

    sd_ck       : out   std_logic;
    sd_cke      : out   std_logic;
    sd_cs       : out   std_logic;
    sd_ras      : out   std_logic;
    sd_cas      : out   std_logic;
    sd_we       : out   std_logic;
    sd_ba       : out   std_logic_vector(1 downto 0);
    sd_a        : out   std_logic_vector(11 downto 0);
    sd_dq       : inout std_logic_vector(15 downto 0));

end sdram_ctrl_de0;
```

Source file: mem/sdram/sdram_ctrl_de0.vhdl

PoC.mem.sdram.ctrl_phy_de0

Physical layer used by module *sdram_ctrl_de0*.

Instantiates input and output buffer components and adjusts the timing for the Altera DE0 board.

Clock and Reset Signals

Port	Description
clk	Base clock for command and write data path.
rst	Reset for `clk`.

Command signals and write data are sampled with `clk`. Read data is also aligned with `clk`.

Write and read enable (wren_nxt, rden_nxt) must be hold for:

- 1 clock cycle if BL = 1,
- 2 clock cycles if BL = 2, or
- 4 clock cycles if BL = 4, or
- 8 clock cycles if BL = 8.

They must be first asserted with the read and write command. Proper delay is included in this unit.

The first word to write must be asserted with the write command. Proper delay is included in this unit.

Synchronous resets are used. Reset must be hold for at least two cycles.

Entity Declaration:

```
entity sdram_ctrl_phy_de0 is
  generic (
    CL : positive);                     -- CAS latency
  port (
    clk      : in std_logic;
    clkout   : in std_logic;
    rst      : in std_logic;

    sd_cke_nxt : in std_logic;
    sd_cs_nxt  : in std_logic;
    sd_ras_nxt : in std_logic;
    sd_cas_nxt : in std_logic;
    sd_we_nxt  : in std_logic;
    sd_ba_nxt  : in std_logic_vector(1 downto 0);
    sd_a_nxt   : in std_logic_vector(11 downto 0);

    wren_nxt   : in std_logic;
    wdata_nxt  : in std_logic_vector(15 downto 0);

    rden_nxt : in  std_logic;
    rdata    : out std_logic_vector(15 downto 0);
    rstb     : out std_logic;

    sd_ck    : out   std_logic;
    sd_cke   : out   std_logic;
    sd_cs    : out   std_logic;
    sd_ras   : out   std_logic;
    sd_cas   : out   std_logic;
    sd_we    : out   std_logic;
    sd_ba    : out   std_logic_vector(1 downto 0);
    sd_a     : out   std_logic_vector(11 downto 0);
    sd_dq    : inout std_logic_vector(15 downto 0));

end sdram_ctrl_phy_de0;
```

Source file: mem/sdram/sdram_ctrl_phy_de0.vhdl

PoC.mem.sdram.ctrl_s3esk

Controller for Micron DDR-SDRAM on Spartan-3E Starter Kit Board.

SDRAM Device: MT46V32M16-6T

Configuration

Parameter	Description
CLK_PERIOD	Clock period in nano seconds. All SDRAM timings are calculated for the device stated above.
CL	CAS latency, choose according to clock frequency.
BL	Burst length. Choose BL=2 for single cycle memory transactions as required for the PoC.Mem interface.

Tested with: CLK_PERIOD = 10.0, CL=2, BL=2.

Operation

Command, address and write data are sampled with the rising edge of `clk`.

Read data is aligned with `clk_fb90_n`. Either process data in this clock domain, or connect a FIFO to transfer data into another clock domain of your choice. This FIFO should capable of storing at least one burst (size BL/2) + start of next burst (size 1).

Synchronous resets are used.

Entity Declaration:

```
entity sdram_ctrl_s3esk is

  generic (
    CLK_PERIOD : real;
    BL         : positive);

  port (
    clk         : in    std_logic;
    clk_n       : in    std_logic;
    clk90       : in    std_logic;
    clk90_n     : in    std_logic;
    rst         : in    std_logic;
    rst90       : in    std_logic;
    rst180      : in    std_logic;
    rst270      : in    std_logic;
    clk_fb90    : in    std_logic;
    clk_fb90_n  : in    std_logic;
    rst_fb90    : in    std_logic;
    rst_fb270   : in    std_logic;

    user_cmd_valid   : in  std_logic;
    user_wdata_valid : in  std_logic;
    user_write       : in  std_logic;
    user_addr        : in  std_logic_vector(24 downto 0);
    user_wdata       : in  std_logic_vector(31 downto 0);
    user_got_cmd     : out std_logic;
    user_got_wdata   : out std_logic;
    user_rdata       : out std_logic_vector(31 downto 0);
    user_rstb        : out std_logic;

    sd_ck_p     : out   std_logic;
    sd_ck_n     : out   std_logic;
    sd_cke      : out   std_logic;
    sd_cs       : out   std_logic;
    sd_ras      : out   std_logic;
    sd_cas      : out   std_logic;
    sd_we       : out   std_logic;
    sd_ba       : out   std_logic_vector(1 downto 0);
    sd_a        : out   std_logic_vector(12 downto 0);
    sd_ldqs     : out   std_logic;
    sd_udqs     : out   std_logic;
    sd_dq       : inout std_logic_vector(15 downto 0));

end sdram_ctrl_s3esk;
```

Source file: mem/sdram/sdram_ctrl_s3esk.vhdl

PoC.mem.sdram.ctrl_phy_s3esk

Physical layer used by module *sdram_ctrl_s3esk*.

Instantiates input and output buffer components and adjusts the timing for the Spartan-3E Starter Kit Board.

Clock and Reset Signals

Port	Description
clk	Base clock for command and write data path.
clk_n	`clk` phase shifted by 180 degrees.
clk90	`clk` phase shifted by 90 degrees.
clk90_n	`clk` phase shifted by 270 degrees.
clk_fb (on PCB)	Driven by external feedback (sd_ck_fb) of DDR-SDRAM clock (sd_ck_p). Actually unused, just referenced below.
clk_fb90	`clk_fb` phase shifted by 90 degrees.
clk_fb90_n	`clk_fb` phase shifted by 270 degrees.
rst	Reset for `clk`.
rst180	Reset for `clk_n`
rst90	Reset for `clk90`.
rst270	Reset for `clk270`.
rst_fb90	Reset for `clk_fb90`.
rst_fb90_n	Reset for `clk_fb90_n`.

Operation

Command signals and write data are sampled with the rising edge of `clk`.

Read data is aligned with `clk_fb90_n`. Either process data in this clock domain, or connect a FIFO to transfer data into another clock domain of your choice. This FIFO should capable of storing at least one burst (size BL/2) + start of next burst (size 1).

Write and read enable (`wren_nxt`, `rden_nxt`) must be hold for:

- 1 clock cycle if BL = 2,
- 2 clock cycles if BL = 4, or
- 4 clock cycles if BL = 8.

They must be first asserted with the read and write command. Proper delay is included in this unit.

The first word to write must be asserted with the write command. Proper delay is included in this unit.

The SDRAM clock is regenerated in this module. The following timing is chosen for minimum latency (should work up to 100 MHz):

- `rising_edge(clk90)` triggers `rising_edge(sd_ck_p)`,
- `rising_edge(clk90_n)` triggers `falling_edge(sd_ck_p)`.

XST options: Disable equivalent register removal.

Synchronous resets are used. Reset must be hold for at least two cycles.

Entity Declaration:

```
entity sdram_ctrl_phy_s3esk is
  port (
    clk      : in std_logic;
    clk_n    : in std_logic;
    clk90    : in std_logic;
    clk90_n  : in std_logic;
    rst      : in std_logic;
    rst90    : in std_logic;
    rst180   : in std_logic;
    rst270   : in std_logic;

    clk_fb90   : in std_logic;
    clk_fb90_n : in std_logic;
    rst_fb90   : in std_logic;
    rst_fb270  : in std_logic;

    sd_cke_nxt : in std_logic;
    sd_cs_nxt  : in std_logic;
    sd_ras_nxt : in std_logic;
    sd_cas_nxt : in std_logic;
    sd_we_nxt  : in std_logic;
    sd_ba_nxt  : in std_logic_vector(1 downto 0);
    sd_a_nxt   : in std_logic_vector(12 downto 0);

    wren_nxt  : in std_logic;
    wdata_nxt : in std_logic_vector(31 downto 0);

    rden_nxt : in  std_logic;
    rdata    : out std_logic_vector(31 downto 0);
    rstb     : out std_logic;

    sd_ck_p : out   std_logic;
    sd_ck_n : out   std_logic;
    sd_cke  : out   std_logic;
    sd_cs   : out   std_logic;
    sd_ras  : out   std_logic;
    sd_cas  : out   std_logic;
    sd_we   : out   std_logic;
    sd_ba   : out   std_logic_vector(1 downto 0);
    sd_a    : out   std_logic_vector(12 downto 0);
    sd_ldqs : out   std_logic;
    sd_udqs : out   std_logic;
    sd_dq   : inout std_logic_vector(15 downto 0));

end sdram_ctrl_phy_s3esk;
```

Source file: mem/sdram/sdram_ctrl_phy_s3esk.vhdl

7.12 PoC.misc

The namespace `PoC.misc` offers different yet uncathegorized entities.

Sub-Namespaces

- *PoC.misc.filter* contains 1-bit filter algorithms.
- *PoC.misc.stat* contains statistic modules.
- *PoC.misc.sync* offers clock-domain-crossing (CDC) modules.

Package

The package *PoC.misc* holds all component declarations for this namespace.

Entities

- *PoC.misc.Delay*
- *PoC.misc.FrequencyMeasurement*
- *PoC.misc.PulseTrain*
- *PoC.misc.Sequencer*
- *PoC.misc.StrobeGenerator*
- *PoC.misc.StrobeLimiter*
- IP:misc_WordAligner

7.12.1 PoC.misc.filter

These are filter entities. . . .

Entities

- *PoC.misc.filter.and*
- *PoC.misc.filter.mean*
- *PoC.misc.filter.or*

PoC.misc.filter.and

Todo: No documentation available.

Entity Declaration:

```
entity filter_and is
  generic (
    TAPS             : positive         := 4;        --
    INIT             : std_logic        := '0';      --
    ADD_OUTPUT_REG   : boolean          := FALSE     --
  );
  port (
    Clock            : in  std_logic;                -- clock
    DataIn           : in  std_logic;                -- data to filter
    DataOut          : out std_logic                 -- filtered signal
  );
end entity;
```

Source file: misc/filter/filter_and.vhdl

PoC.misc.filter.mean

Todo: No documentation available.

Entity Declaration:

```
entity filter_mean is
  generic (
    TAPS             : positive         := 4;        --
    INIT             : std_logic        := '1';      --
    ADD_OUTPUT_REG   : boolean          := FALSE     --
  );
  port (
    Clock            : in  std_logic;                -- clock
    DataIn           : in  std_logic;                -- data to filter
    DataOut          : out std_logic                 -- filtered signal
  );
end entity;
```

Source file: misc/filter/filter_mean.vhdl

PoC.misc.filter.or

Todo: No documentation available.

Entity Declaration:

```
entity filter_or is
  generic (
    TAPS             : positive         := 4;        --
    INIT             : std_logic        := '1';      --
    ADD_OUTPUT_REG   : boolean          := FALSE     --
  );
  port (
    Clock            : in  std_logic;                -- clock
    DataIn           : in  std_logic;                -- data to filter
    DataOut          : out std_logic                 -- filtered signal
  );
end entity;
```

Source file: misc/filter/filter_or.vhdl

7.12.2 PoC.misc.gearbox

These are gearbox entities. . . .

Entities

- *PoC.misc.gearbox.down_cc*
- *PoC.misc.gearbox.down_dc*
- *PoC.misc.gearbox.up_cc*
- *PoC.misc.gearbox.up_dc*

PoC.misc.gearbox.down_cc

This module provides a downscaling gearbox with a common clock (cc) interface. It perfoems a 'word' to 'byte' splitting. The default order is LITTLE_ENDIAN (starting at byte(0)). Input "In_Data" and output

"Out_Data" are of the same clock domain "Clock". Optional input and output registers can be added by enabling (ADD_***PUT_REGISTERS = TRUE).

Entity Declaration:

```
entity gearbox_down_cc is
  generic (
    INPUT_BITS             : positive  := 32;
    OUTPUT_BITS            : positive  := 24;
    META_BITS              : natural   := 0;
    ADD_INPUT_REGISTERS    : boolean   := FALSE;
    ADD_OUTPUT_REGISTERS   : boolean   := FALSE
  );
  port (
    Clock       : in  std_logic;

    In_Sync     : in  std_logic;
    In_Valid    : in  std_logic;
    In_Next     : out std_logic;
    In_Data     : in  std_logic_vector(INPUT_BITS - 1 downto 0);
    In_Meta     : in  std_logic_vector(META_BITS - 1 downto 0);

    Out_Sync    : out std_logic;
    Out_Valid   : out std_logic;
    Out_Data    : out std_logic_vector(OUTPUT_BITS - 1 downto 0);
    Out_Meta    : out std_logic_vector(META_BITS - 1 downto 0);
    Out_First   : out std_logic;
    Out_Last    : out std_logic
  );
end entity;
```

Source file: misc/gearbox/gearbox_down_cc.vhdl

PoC.misc.gearbox.down_dc

This module provides a downscaling gearbox with a dependent clock (dc) interface. It perfoems a 'word' to 'byte' splitting. The default order is LITTLE_ENDIAN (starting at byte(0)). Input "In_Data" is of clock domain "Clock1"; output "Out_Data" is of clock domain "Clock2". Optional input and output registers can be added by enabling (ADD_***PUT_REGISTERS = TRUE).

Assertions:

- Clock periods of Clock1 and Clock2 MUST be multiples of each other.
- Clock1 and Clock2 MUST be phase aligned (related) to each other.

Entity Declaration:

```
entity gearbox_down_dc is
  generic (
    INPUT_BITS             : positive        := 32;                    --␣
↪input bits ('words')
    OUTPUT_BITS            : positive        := 8;                     --␣
↪output bits ('byte')
    OUTPUT_ORDER           : T_BIT_ORDER     := LSB_FIRST;             -- LSB_
↪FIRST: start at byte(0), MSB_FIRST: start at byte(n-1)
```

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(continued from previous page)

```
    ADD_INPUT_REGISTERS    : boolean          := FALSE;                          -- add_
↪input register @Clock1
    ADD_OUTPUT_REGISTERS   : boolean          := FALSE                           -- add_
↪output register @Clock2
  );
  port (
    Clock1                 : in  std_logic;                                      --_
↪input clock domain
    Clock2                 : in  std_logic;                                      --_
↪output clock domain
    In_Data                : in  std_logic_vector(INPUT_BITS - 1 downto 0);      --_
↪input word
    Out_Data               : out std_logic_vector(OUTPUT_BITS - 1 downto 0)      --_
↪output word
  );
end entity;
```

Source file: misc/gearbox/gearbox_down_dc.vhdl

PoC.misc.gearbox.up_cc

This module provides a downscaling gearbox with a common clock (cc) interface. It perfoems a 'byte' to 'word' collection. The default order is LITTLE_ENDIAN (starting at byte(0)). Input "In_Data" and output "Out_Data" are of the same clock domain "Clock". Optional input and output registers can be added by enabling (ADD_***PUT_REGISTERS = TRUE).

Entity Declaration:

```
entity gearbox_up_cc is
  generic (
    INPUT_BITS             : positive  := 24;
    OUTPUT_BITS            : positive  := 32;
    META_BITS              : natural   := 0;
    ADD_INPUT_REGISTERS    : boolean   := FALSE;
    ADD_OUTPUT_REGISTERS   : boolean   := FALSE
  );
  port (
    Clock       : in  std_logic;

    In_Sync     : in  std_logic;
    In_Valid    : in  std_logic;
    In_Data     : in  std_logic_vector(INPUT_BITS - 1 downto 0);
    In_Meta     : in  std_logic_vector(META_BITS - 1 downto 0);

    Out_Sync    : out std_logic;
    Out_Valid   : out std_logic;
    Out_Data    : out std_logic_vector(OUTPUT_BITS - 1 downto 0);
    Out_Meta    : out std_logic_vector(META_BITS - 1 downto 0);
    Out_First   : out std_logic;
    Out_Last    : out std_logic
  );
end entity;
```

Source file: misc/gearbox/gearbox_up_cc.vhdl

PoC.misc.gearbox.up_dc

This module provides a upscaling gearbox with a dependent clock (dc) interface. It perfoems a 'byte' to 'word' collection. The default order is LITTLE_ENDIAN (starting at byte(0)). Input "In_Data" is of clock domain "Clock1"; output "Out_Data" is of clock domain "Clock2". The "In_Align" is required to mark the starting byte in the word. An optional input register can be added by enabling (ADD_INPUT_REGISTERS = TRUE).

Assertions:

- Clock periods of Clock1 and Clock2 MUST be multiples of each other.
- Clock1 and Clock2 MUST be phase aligned (related) to each other.

Entity Declaration:

```
entity gearbox_up_dc is
  generic (
    INPUT_BITS            : positive        := 8;                                 -- input bit width
    INPUT_ORDER           : T_BIT_ORDER     := LSB_FIRST;                         -- LSB_FIRST: start at byte(0), MSB_FIRST: start at byte(n-1)
    OUTPUT_BITS           : positive        := 32;                                -- output bit width
    ADD_INPUT_REGISTERS   : boolean         := FALSE                              -- add input register @Clock1
  );
  port (
    Clock1                : in  std_logic;                                        -- input clock domain
    Clock2                : in  std_logic;                                        -- output clock domain
    In_Align              : in  std_logic;                                        -- align word (one cycle high impulse)
    In_Data               : in  std_logic_vector(INPUT_BITS - 1 downto 0);        -- input word
    Out_Data              : out std_logic_vector(OUTPUT_BITS - 1 downto 0);       -- output word
    Out_Valid             : out std_logic                                         -- output is valid
  );
end entity;
```

Source file: misc/gearbox/gearbox_up_dc.vhdl

7.12.3 PoC.misc.stat

These are stat entities. . . .

Entities

- *PoC.misc.stat.Average*
- *PoC.misc.stat.Histogram*
- *PoC.misc.stat.Maximum*
- *PoC.misc.stat.Minimum*

PoC.misc.stat.Average

Todo: No documentation available.

Entity Declaration:

```
entity stat_Average is
  generic (
    DATA_BITS      : positive    := 8;
    COUNTER_BITS   : positive    := 16
  );
  port (
    Clock          : in  std_logic;
    Reset          : in  std_logic;

    Enable         : in  std_logic;
    DataIn         : in  std_logic_vector(DATA_BITS - 1 downto 0);

    Count          : out std_logic_vector(COUNTER_BITS - 1 downto 0);
    Sum            : out std_logic_vector(COUNTER_BITS - 1 downto 0);
    Average        : out std_logic_vector(COUNTER_BITS - 1 downto 0);
    Valid          : out std_logic
  );
end entity;
```

Source file: misc/stat/stat_Average.vhdl

PoC.misc.stat.Histogram

Todo: No documentation available.

Entity Declaration:

```
entity stat_Histogram is
  generic (
    DATA_BITS      : positive    := 16;
    COUNTER_BITS   : positive    := 16
  );
  port (
    Clock          : in  std_logic;
    Reset          : in  std_logic;

    Enable         : in  std_logic;
    DataIn         : in  std_logic_vector(DATA_BITS - 1 downto 0);

    Histogram      : out T_SLM(2**DATA_BITS - 1 downto 0, COUNTER_BITS - 1 downto 0)
  );
end entity;
```

Source file: misc/stat/stat_Histogram.vhdl

PoC.misc.stat.Maximum

Todo: No documentation available.

Entity Declaration:

```
entity stat_Maximum is
  generic (
    DEPTH          : positive    := 8;
    DATA_BITS      : positive    := 16;
    COUNTER_BITS   : positive    := 16
  );
  port (
    Clock          : in  std_logic;
    Reset          : in  std_logic;

    Enable         : in  std_logic;
    DataIn         : in  std_logic_vector(DATA_BITS - 1 downto 0);

    Valids         : out std_logic_vector(DEPTH - 1 downto 0);
    Maximums       : out T_SLM(DEPTH - 1 downto 0, DATA_BITS - 1 downto 0);
    Counts         : out T_SLM(DEPTH - 1 downto 0, COUNTER_BITS - 1 downto 0)
  );
end entity;
```

Source file: misc/stat/stat_Maximum.vhdl

PoC.misc.stat.Minimum

Todo: No documentation available.

Entity Declaration:

```
entity stat_Minimum is
  generic (
    DEPTH          : positive    := 8;
    DATA_BITS      : positive    := 16;
    COUNTER_BITS   : positive    := 16
  );
  port (
    Clock          : in  std_logic;
    Reset          : in  std_logic;

    Enable         : in  std_logic;
    DataIn         : in  std_logic_vector(DATA_BITS - 1 downto 0);

    Valids         : out std_logic_vector(DEPTH - 1 downto 0);
    Minimums       : out T_SLM(DEPTH - 1 downto 0, DATA_BITS - 1 downto 0);
    Counts         : out T_SLM(DEPTH - 1 downto 0, COUNTER_BITS - 1 downto 0)
  );
end entity;
```

Source file: misc/stat/stat_Minimum.vhdl

7.12.4 PoC.misc.sync

The namespace `PoC.misc.sync` offers different clock-domain-crossing (CDC) synchronizer circuits. All synchronizers are based on the basic 2 flip-flop synchonizer called *sync_Bits*. PoC has two platform specific implementations for Altera and Xilinx, which are choosen, if the appropriate `MY_DEVICE` constant is configured in `my_config.vhdl`.

Decision Table:

Behavior	Flag[1]	Strobe[2]	Continuous Data	Reset[4]	Pulse[3]
1 Bit	*sync_Bits*	*sync_Strobe*	fifo_ic_got[5]	*sync_Reset*	*sync_Pulse*
n Bit	*sync_Vector*	*sync_Command*	fifo_ic_got[5]		

Basic 2 Flip-Flop Synchronizer

The basic 2 flip-flop synchronizer is called *sync_Bits*. It's possible to configure the bit count of indivital bits. If a vector shall be synchronized, use one of the special synchronizers like *sync_Vector*. The vendor specific implementations are named `sync_Bits_Altera` and `sync_Bits_Xilinx` respectivily.

A second variant of the 2-FF synchronizer is called *sync_Reset*. It's for `Reset`-signals, implementing asynchronous assertion and synchronous deassertion. The vendor specific implementations are named `sync_Reset_Altera` and `sync_Reset_Xilinx` respectivily.

A third variant of a 2-FF synchronizer is called *sync_Pulse*. It's for very short `Pulsed`-signals. It uses an addition asynchronous capture FF to latch the very short pulse. The vendor specific implementations are named `sync_Pulse_Altera` and `sync_Pulse_Xilinx` respectivily.

Special Synchronizers

Based on the 2-FF synchronizer, several "high-level" synchronizers are build.

- *sync_Strobe* synchronizer `strobe`-signals across clock-domain-boundaries. A busy signal indicates the synchronization status and can be used as a internal gate-signal to disallow new incoming strobes. A `strobe`-signal is only for one clock period active.
- *sync_Command* like `sync_Strobe`, it synchronizes a one clock period active signal across the clock-domain-boundary, but the input has multiple bits. After the multi bit strobe (Command) was transfered, the output goes to its idle value.
- *sync_Vector* synchronizes a complete vector across the clock-domain-boundary. A changed detection on the input vector causes a register to latch the current state. The changed event is transfered to the new clock-domain and triggers a register to store the latched content, but in the new clock domain.

See also:

PoC.fifo.ic_got For a cross-clock capable FIFO.

PoC.misc.sync Package

Source file: sync.pkg.vhdl

[1] A *flag* or *status* signal is a continuous, long time stable signal.
[2] A *strobe* signal is active for only one cycle.
[4] To be refumented
[3] A *pulse* signal is a very short event.
[5] See the `PoC.fifo` namespace for cross-clock capable FIFOs.

PoC.misc.sync.Bits

This module synchronizes multiple flag bits into clock-domain `Clock`. The clock-domain boundary crossing is done by two synchronizer D-FFs. All bits are independent from each other. If a known vendor like Altera or Xilinx are recognized, a vendor specific implementation is chosen.

> **Attention:** Use this synchronizer only for long time stable signals (flags).

Constraints:

General: Please add constraints for meta stability to all '_meta' signals and timing ignore constraints to all '_async' signals.

Xilinx: In case of a Xilinx device, this module will instantiate the optimized module PoC.xil.sync.Bits. Please attend to the notes of sync_Bits.vhdl.

Altera sdc file: TODO

Entity Declaration:

```
entity sync_Bits is
  generic (
    BITS          : positive            := 1;                         -- number of␣
↪bit to be synchronized
    INIT          : std_logic_vector    := x"00000000";               --␣
↪initialization bits
    SYNC_DEPTH    : T_MISC_SYNC_DEPTH   := T_MISC_SYNC_DEPTH'low      -- generate␣
↪SYNC_DEPTH many stages, at least 2
  );
  port (
    Clock         : in  std_logic;                                    -- <Clock> ␣
↪output clock domain
    Input         : in  std_logic_vector(BITS - 1 downto 0);          -- @async: ␣
↪input bits
    Output        : out std_logic_vector(BITS - 1 downto 0)           -- @Clock: ␣
↪output bits
  );
end entity;
```

See also:

PoC.misc.sync.Reset For a special 2 D-FF synchronizer for *reset*-signals.

PoC.misc.sync.Pulse For a special 1+2 D-FF synchronizer for *pulse*-signals.

PoC.misc.sync.Strobe For a synchronizer for *strobe*-signals.

PoC.misc.sync.Vector For a multiple bits capable synchronizer.

Source file: misc/sync/sync_Bits.vhdl

PoC.misc.sync.Command

This module synchronizes a vector of bits from clock-domain `Clock1` to clock-domain `Clock2`. The clock-domain boundary crossing is done by a change comparator, a T-FF, two synchronizer D-FFs and a reconstructive XOR indicating a value change on the input. This changed signal is used to capture the input for the new output. A busy flag is additionally calculated for the input clock-domain. The output has strobe character and is reset to it's `INIT` value after one clock cycle.

Constraints: This module uses sub modules which need to be constrained. Please attend to the notes of the instantiated sub modules.

Entity Declaration:

```
entity sync_Command is
  generic (
    BITS          : positive            := 8;                       -- number of␣
↪bit to be synchronized
    INIT          : std_logic_vector    := x"00000000";             --
    SYNC_DEPTH    : T_MISC_SYNC_DEPTH   := T_MISC_SYNC_DEPTH'low    -- generate␣
↪SYNC_DEPTH many stages, at least 2
  );
  port (
    Clock1        : in  std_logic;                                  -- <Clock> ␣
↪input clock
    Clock2        : in  std_logic;                                  -- <Clock> ␣
↪output clock
    Input         : in  std_logic_vector(BITS - 1 downto 0);        -- @Clock1:␣
↪input vector
    Output        : out std_logic_vector(BITS - 1 downto 0);        -- @Clock2:␣
↪output vector
    Busy          : out std_logic;                                  -- @Clock1:␣
↪busy bit
    Changed       : out std_logic                                   -- @Clock2:␣
↪changed bit
  );
end entity;
```

Source file: misc/sync/sync_Command.vhdl

PoC.misc.sync.Pulse

This module synchronizes multiple pulsed bits into the clock-domain `Clock`. The clock-domain boundary crossing is done by two synchronizer D-FFs. All bits are independent from each other. If a known vendor like Altera or Xilinx are recognized, a vendor specific implementation is chosen.

Attention: Use this synchronizer for very short signals (pulse).

Constraints:

General: Please add constraints for meta stability to all '_meta' signals and timing ignore constraints to all '_async' signals.

Xilinx: In case of a Xilinx device, this module will instantiate the optimized module PoC.xil.sync.Pulse. Please attend to the notes of sync_Bits.vhdl.

Altera sdc file: TODO

Entity Declaration:

```
entity sync_Pulse is
  generic (
    BITS          : positive            := 1;                       -- number of␣
↪bit to be synchronized
    SYNC_DEPTH    : T_MISC_SYNC_DEPTH   := T_MISC_SYNC_DEPTH'low    -- generate␣
↪SYNC_DEPTH many stages, at least 2
  );
  port (
    Clock         : in  std_logic;                                  -- <Clock> ␣
↪output clock domain
```

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```
    Input          : in  std_logic_vector(BITS - 1 downto 0);         -- @async: input bits
    Output         : out std_logic_vector(BITS - 1 downto 0)          -- @Clock: output bits
  );
end entity;
```

See also:

PoC.misc.sync.Bits For a common 2 D-FF synchronizer for *flag*-signals.

PoC.misc.sync.Reset For a special 2 D-FF synchronizer for *reset*-signals.

PoC.misc.sync.Strobe For a synchronizer for *strobe*-signals.

PoC.misc.sync.Vector For a multiple bits capable synchronizer.

Source file: misc/sync/sync_Pulse.vhdl

PoC.misc.sync.Reset

This module synchronizes an asynchronous reset signal to the clock `Clock`. The `Input` can be asserted and de-asserted at any time. The `Output` is asserted asynchronously and de-asserted synchronously to the clock.

Attention: Use this synchronizer only to asynchronously reset your design. The 'Output' should be feed by global buffer to the destination FFs, so that, it reaches their reset inputs within one clock cycle.

Constraints:

General: Please add constraints for meta stability to all '_meta' signals and timing ignore constraints to all '_async' signals.

Xilinx: In case of a Xilinx device, this module will instantiate the optimized module xil_SyncReset. Please attend to the notes of xil_SyncReset.

Altera sdc file: TODO

Entity Declaration:

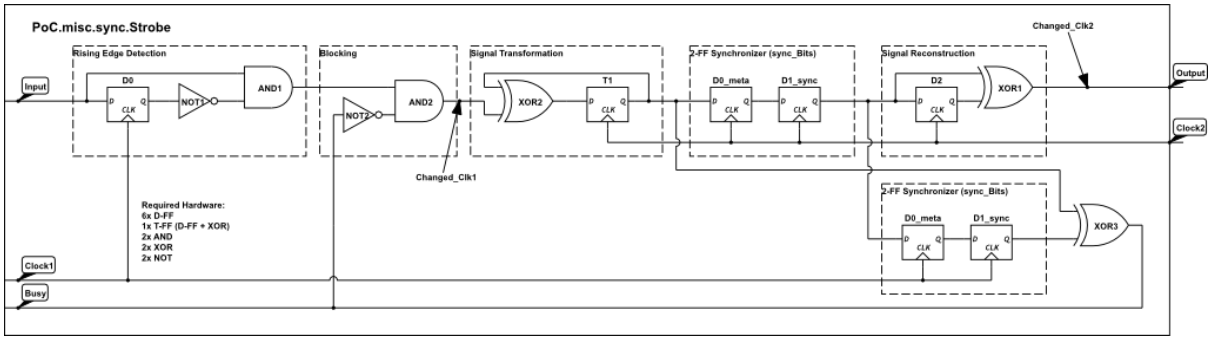
```
entity sync_Reset is
  generic (
    SYNC_DEPTH     : T_MISC_SYNC_DEPTH    := T_MISC_SYNC_DEPTH'low     -- generate SYNC_DEPTH many stages, at least 2
  );
  port (
    Clock          : in  std_logic;                                    -- <Clock> output clock domain
    Input          : in  std_logic;                                    -- @async: reset input
    Output         : out std_logic                                     -- @Clock: reset output
  );
end entity;
```

Source file: misc/sync/sync_Reset.vhdl

PoC.misc.sync.Strobe

This module synchronizes multiple high-active bits from clock-domain `Clock1` to clock-domain `Clock2`. The clock-domain boundary crossing is done by a T-FF, two synchronizer D-FFs and a reconstructive XOR. A busy flag is additionally calculated and can be used to block new inputs. All bits are independent from each other. Multiple consecutive strobes are suppressed by a rising edge detection.

Attention: Use this synchronizer only for one-cycle high-active signals (strobes).



Constraints: This module uses sub modules which need to be constrained. Please attend to the notes of the instantiated sub modules.

Entity Declaration:

```
entity sync_Strobe is
  generic (
    BITS                : positive            := 1;                       -- number of bit to be synchronized
    GATED_INPUT_BY_BUSY : boolean             := TRUE;                    -- use gated input (by busy signal)
    SYNC_DEPTH          : T_MISC_SYNC_DEPTH   := T_MISC_SYNC_DEPTH'low    -- generate SYNC_DEPTH many stages, at least 2
  );
  port (
    Clock1              : in  std_logic;                                  -- <Clock> input clock domain
    Clock2              : in  std_logic;                                  -- <Clock> output clock domain
    Input               : in  std_logic_vector(BITS - 1 downto 0);        -- @Clock1: input bits
    Output              : out std_logic_vector(BITS - 1 downto 0);        -- @Clock2: output bits
    Busy                : out  std_logic_vector(BITS - 1 downto 0)        -- @Clock1: busy bits
  );
end entity;
```

Source file: misc/sync/sync_Strobe.vhdl

PoC.misc.sync.Vector

This module synchronizes a vector of bits from clock-domain `Clock1` to clock-domain `Clock2`. The clock-domain boundary crossing is done by a change comparator, a T-FF, two synchronizer D-FFs and a reconstructive XOR indicating a value change on the input. This changed signal is used to capture the input for the new output. A busy flag is additionally calculated for the input clock domain.

Constraints: This module uses sub modules which need to be constrained. Please attend to the notes of the instantiated sub modules.

Entity Declaration:

```
entity sync_Vector is
  generic (
    MASTER_BITS    : positive            := 8;                          -- number of bit to be synchronized
    SLAVE_BITS     : natural             := 0;
    INIT           : std_logic_vector    := x"00000000";                --
    SYNC_DEPTH     : T_MISC_SYNC_DEPTH   := T_MISC_SYNC_DEPTH'low       -- generate SYNC_DEPTH many stages, at least 2
  );
  port (
    Clock1         : in  std_logic;                                      -- <Clock>  input clock
    Clock2         : in  std_logic;                                      -- <Clock>  output clock
    Input          : in  std_logic_vector((MASTER_BITS + SLAVE_BITS) - 1 downto 0); -- @Clock1:  input vector
    Output         : out std_logic_vector((MASTER_BITS + SLAVE_BITS) - 1 downto 0); -- @Clock2:  output vector
    Busy           : out  std_logic;                                     -- @Clock1:  busy bit
    Changed        : out  std_logic                                      -- @Clock2:  changed bit
  );
end entity;
```

Source file: misc/sync/sync_Vector.vhdl

7.12.5 PoC.misc Package

This package holds all component declarations for this namespace.

Source file: misc.pkg.vhdl

7.12.6 PoC.misc.Delay

Todo: No documentation available.

Entity Declaration:

```
entity misc_Delay is
  generic (
    BITS           : positive;
    TAPS           : T_NATVEC          -- select one or multiple delay tap points
  );
  port (
    Clock          : in  std_logic;                                      --clock
    Reset          : in  std_logic   := '0';                             --reset; avoid reset to enable SRL16/SRL32 usage
```

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```
    Enable        : in  std_logic   := '1';                                    --␣
↪enable
    DataIn        : in  std_logic_vector(BITS - 1 downto 0);                   --␣
↪data to delay
    DataOut       : out T_SLM(TAPS'length - 1 downto 0, BITS - 1 downto 0)   --␣
↪delayed ouputs, tapped at TAPS(i)
  );
end entity;
```

Source file: misc/misc_Delay.vhdl

7.12.7 PoC.misc.FrequencyMeasurement

This module counts 1 second in a reference timer at reference clock. This reference time is used to start and stop a timer at input clock. The counter value is the measured frequency in Hz.

Entity Declaration:

```
entity misc_FrequencyMeasurement is
  generic (
    REFERENCE_CLOCK_FREQ  : FREQ      := 100 MHz
  );
  port (
    Reference_Clock   : in  std_logic;
    Input_Clock       : in  std_logic;

    Start             : in  std_logic;
    Done              : out std_logic;
    Result            : out T_SLV_32
  );
end entity;
```

Source file: misc/misc_FrequencyMeasurement.vhdl

7.12.8 PoC.misc.PulseTrain

This module generates pulse trains. This module was written as a answer for a StackOverflow question: http://stackoverflow.com/questions/25783320

Entity Declaration:

Source file: misc/misc_PulseTrain.vhdl

7.12.9 PoC.misc.Sequencer

Todo: No documentation available.

Entity Declaration:

Source file: misc/misc_Sequencer.vhdl

7.12.10 PoC.misc.StrobeGenerator

Todo: No documentation available.

Entity Declaration:

Source file: misc/misc_StrobeGenerator.vhdl

7.12.11 PoC.misc.StrobeLimiter

Todo: No documentation available.

Entity Declaration:

Source file: misc/misc_StrobeLimiter.vhdl

7.12.12 WordAligner

Todo: No documentation available.

Entity Declaration:

Source file: misc/misc_WordAligner.vhdl

7.13 PoC.net

These are bus entities. . . .

Sub-Namespaces

- *PoC.net.arp*
- *PoC.net.eth*
- *PoC.net.icmpv4*
- *PoC.net.icmpv6*
- *PoC.net.ipv4*
- *PoC.net.ipv6*
- *PoC.net.mac*
- *PoC.net.ndp*
- *PoC.net.stack*
- *PoC.net.udp*

Entities

- *PoC.net.FrameChecksum*
- IP:net_FrameLoopback

7.13.1 PoC.net.arp

These are ARP entities. . . .

PoC.net.arp.BroadCast_Receiver

Todo: No documentation available.

Entity Declaration:

```
entity arp_BroadCast_Receiver is
  generic (
    ALLOWED_PROTOCOL_IPV4       : boolean                       := TRUE;
    ALLOWED_PROTOCOL_IPV6       : boolean                       := FALSE
  );
  port (
    Clock                       : in  std_logic;                                -
↪-
    Reset                       : in  std_logic;                                -
↪-

    RX_Valid                    : in  std_logic;
    RX_Data                     : in  T_SLV_8;
    RX_SOF                      : in  std_logic;
    RX_EOF                      : in  std_logic;
    RX_Ack                      : out std_logic;
    RX_Meta_rst                 : out std_logic;
    RX_Meta_SrcMACAddress_nxt   : out std_logic;
    RX_Meta_SrcMACAddress_Data  : in  T_SLV_8;
    RX_Meta_DestMACAddress_nxt  : out std_logic;
    RX_Meta_DestMACAddress_Data : in  T_SLV_8;

    Clear                       : in  std_logic;
    Error                       : out std_logic;

    RequestReceived             : out std_logic;
    Address_rst                 : in  std_logic;
    SenderMACAddress_nxt        : in  std_logic;
    SenderMACAddress_Data       : out T_SLV_8;
    SenderIPAddress_nxt         : in  std_logic;
    SenderIPAddress_Data        : out T_SLV_8;
    TargetIPAddress_nxt         : in  std_logic;
    TargetIPAddress_Data        : out T_SLV_8
  );
end entity;
```

Source file: net/arp/arp_BroadCast_Receiver.vhdl

PoC.net.arp.BroadCast_Requester

Todo: No documentation available.

Entity Declaration:

```
entity arp_BroadCast_Requester is
  generic (
    ALLOWED_PROTOCOL_IPV4         : boolean                       := TRUE;
    ALLOWED_PROTOCOL_IPV6         : boolean                       := FALSE
  );
  port (
    Clock                         : in  std_logic;
    Reset                         : in  std_logic;

    SendRequest                   : in  std_logic;
    Complete                      : out std_logic;

    Address_rst                   : out std_logic;
    SenderMACAddress_nxt          : out std_logic;
    SenderMACAddress_Data         : in  T_SLV_8;
    SenderIPv4Address_nxt         : out std_logic;
    SenderIPv4Address_Data        : in  T_SLV_8;
    TargetMACAddress_nxt          : out std_logic;
    TargetMACAddress_Data         : in  T_SLV_8;
    TargetIPv4Address_nxt         : out std_logic;
    TargetIPv4Address_Data        : in  T_SLV_8;

    TX_Valid                      : out std_logic;
    TX_Data                       : out T_SLV_8;
    TX_SOF                        : out std_logic;
    TX_EOF                        : out std_logic;
    TX_Ack                        : in  std_logic;
    TX_Meta_DestMACAddress_rst    : in  std_logic;
    TX_Meta_DestMACAddress_nxt    : in  std_logic;
    TX_Meta_DestMACAddress_Data   : out T_SLV_8
  );
end entity;
```

Source file: net/arp/arp_BroadCast_Requester.vhdl

PoC.net.arp.Cache

Todo: No documentation available.

Entity Declaration:

```
entity arp_Cache is
  generic (
    CLOCK_FREQ                : FREQ                                := 125 MHz;
    REPLACEMENT_POLICY        : string                              := "LRU";
    TAG_BYTE_ORDER            : T_BYTE_ORDER                        := BIG_
↪ENDIAN;
    DATA_BYTE_ORDER           : T_BYTE_ORDER                        := BIG_
↪ENDIAN;
```

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```
    INITIAL_CACHE_CONTENT     : T_NET_ARP_ARPCACHE_VECTOR
  );
  port (
    Clock                     : in  std_logic;                                    --
    Reset                     : in  std_logic;                                    --

    Command                   : in  T_NET_ARP_ARPCACHE_COMMAND;
    Status                    : out T_NET_ARP_ARPCACHE_STATUS;
    NewIPv4Address_rst        : out std_logic;
    NewIPv4Address_nxt        : out std_logic;
    NewIPv4Address_Data       : in  T_SLV_8;
    NewMACAddress_rst         : out std_logic;
    NewMACAddress_nxt         : out std_logic;
    NewMACAddress_Data        : in  T_SLV_8;

    Lookup                    : in  std_logic;
    IPv4Address_rst           : out std_logic;
    IPv4Address_nxt           : out std_logic;
    IPv4Address_Data          : in  T_SLV_8;

    CacheResult               : out T_CACHE_RESULT;
    MACAddress_rst            : in  std_logic;
    MACAddress_nxt            : in  std_logic;
    MACAddress_Data           : out T_SLV_8
  );
end entity;
```

Source file: net/arp/arp_Cache.vhdl

PoC.net.arp.IPPool

Todo: No documentation available.

Entity Declaration:

```
entity arp_IPPool is
  generic (
    IPPOOL_SIZE                 : positive;
    INITIAL_IPV4ADDRESSES       : T_NET_IPV4_ADDRESS_VECTOR     := (0 to 7 => C_
↪NET_IPV4_ADDRESS_EMPTY)
  );
  port (
    Clock                       : in  std_logic;                                  
↪ --
    Reset                       : in  std_logic;                                  
↪ --

--    Command                     : in  T_ETHERNET_ARP_IPPOOL_COMMAND;
--    IPv4Address                 : in  T_NET_IPV4_ADDRESS;
--    MACAddress                  : in  T_ETHERNET_MAC_ADDRESS;

    Lookup                      : in  std_logic;
    IPv4Address_rst             : out std_logic;
    IPv4Address_nxt             : out std_logic;
    IPv4Address_Data            : in  T_SLV_8;

```

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```
    PoolResult                    : out T_CACHE_RESULT
  );
end entity;
```

Source file: net/arp/arp_IPPool.vhdl

PoC.net.arp.Tester

Todo: No documentation available.

Entity Declaration:

Source file: net/arp/arp_Tester.vhdl

PoC.net.arp.UniCast_Receiver

Todo: No documentation available.

Entity Declaration:

```
entity arp_UniCast_Receiver is
  generic (
    ALLOWED_PROTOCOL_IPV4       : boolean                       := TRUE;
    ALLOWED_PROTOCOL_IPV6       : boolean                       := FALSE
  );
  port (
    Clock                       : in  std_logic;                                -
↪-
    Reset                       : in  std_logic;                                -
↪-

    RX_Valid                    : in  std_logic;
    RX_Data                     : in  T_SLV_8;
    RX_SOF                      : in  std_logic;
    RX_EOF                      : in  std_logic;
    RX_Ack                      : out std_logic;
    RX_Meta_rst                 : out std_logic;
    RX_Meta_SrcMACAddress_nxt   : out std_logic;
    RX_Meta_SrcMACAddress_Data  : in  T_SLV_8;
    RX_Meta_DestMACAddress_nxt  : out std_logic;
    RX_Meta_DestMACAddress_Data : in  T_SLV_8;

    Clear                       : in  std_logic;
    Error                       : out std_logic;

    ResponseReceived            : out std_logic;
    Address_rst                 : in  std_logic;
    SenderMACAddress_nxt        : in  std_logic;
    SenderMACAddress_Data       : out T_SLV_8;
    SenderIPAddress_nxt         : in  std_logic;
    SenderIPAddress_Data        : out T_SLV_8;
```

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```
    TargetIPAddress_nxt          : in  std_logic;
    TargetIPAddress_Data         : out T_SLV_8;
    TargetMACAddress_nxt         : in  std_logic;
    TargetMACAddress_Data        : out T_SLV_8
  );
end entity;
```

Source file: net/arp/arp_UniCast_Receiver.vhdl

PoC.net.arp.UniCast_Responder

Todo: No documentation available.

Entity Declaration:

```
entity arp_UniCast_Responder is
  generic (
    ALLOWED_PROTOCOL_IPV4          : boolean                       := TRUE;
    ALLOWED_PROTOCOL_IPV6          : boolean                       := FALSE
  );
  port (
    Clock                          : in  std_logic;
    --
    Reset                          : in  std_logic;
    --

    SendResponse                   : in  std_logic;
    Complete                       : out std_logic;

    Address_rst                    : out std_logic;
    SenderMACAddress_nxt           : out std_logic;
    SenderMACAddress_Data          : in  T_SLV_8;
    SenderIPv4Address_nxt          : out std_logic;
    SenderIPv4Address_Data         : in  T_SLV_8;
    TargetMACAddress_nxt           : out std_logic;
    TargetMACAddress_Data          : in  T_SLV_8;
    TargetIPv4Address_nxt          : out std_logic;
    TargetIPv4Address_Data         : in  T_SLV_8;

    TX_Valid                       : out std_logic;
    TX_Data                        : out T_SLV_8;
    TX_SOF                         : out std_logic;
    TX_EOF                         : out std_logic;
    TX_Ack                         : in  std_logic;
    TX_Meta_DestMACAddress_rst     : in  std_logic;
    TX_Meta_DestMACAddress_nxt     : in  std_logic;
    TX_Meta_DestMACAddress_Data    : out T_SLV_8
  );
end entity;
```

Source file: net/arp/arp_UniCast_Responder.vhdl

PoC.net.arp.Wrapper

Todo: No documentation available.

Entity Declaration:

```
entity arp_Wrapper is
  generic (
    CLOCK_FREQ                          : FREQ                                  := 125 MHz;
    INTERFACE_MACADDRESS                : T_NET_MAC_ADDRESS                     := C_NET_MAC_ADDRESS_EMPTY;
    INITIAL_IPV4ADDRESSES               : T_NET_IPV4_ADDRESS_VECTOR             := (0 => C_NET_IPV4_ADDRESS_EMPTY);
    INITIAL_ARPCACHE_CONTENT            : T_NET_ARP_ARPCACHE_VECTOR             := (0 => (Tag => C_NET_IPV4_ADDRESS_EMPTY, MAC => C_NET_MAC_ADDRESS_EMPTY));
    APR_REQUEST_TIMEOUT                 : time                                  := 100 ms
  );
  port (
    Clock                               : in  std_logic;
    Reset                               : in  std_logic;

    IPPool_Announce                     : in  std_logic;
    IPPool_Announced                    : out std_logic;

    IPCache_Lookup                      : in  std_logic;
    IPCache_IPv4Address_rst             : out std_logic;
    IPCache_IPv4Address_nxt             : out std_logic;
    IPCache_IPv4Address_Data            : in  T_SLV_8;

    IPCache_Valid                       : out std_logic;
    IPCache_MACAddress_rst              : in  std_logic;
    IPCache_MACAddress_nxt              : in  std_logic;
    IPCache_MACAddress_Data             : out T_SLV_8;

    Eth_UC_TX_Valid                     : out std_logic;
    Eth_UC_TX_Data                      : out T_SLV_8;
    Eth_UC_TX_SOF                       : out std_logic;
    Eth_UC_TX_EOF                       : out std_logic;
    Eth_UC_TX_Ack                       : in  std_logic;
    Eth_UC_TX_Meta_rst                  : in  std_logic;
    Eth_UC_TX_Meta_DestMACAddress_nxt   : in  std_logic;
    Eth_UC_TX_Meta_DestMACAddress_Data  : out T_SLV_8;

    Eth_UC_RX_Valid                     : in  std_logic;
    Eth_UC_RX_Data                      : in  T_SLV_8;
    Eth_UC_RX_SOF                       : in  std_logic;
    Eth_UC_RX_EOF                       : in  std_logic;
    Eth_UC_RX_Ack                       : out std_logic;
    Eth_UC_RX_Meta_rst                  : out std_logic;
    Eth_UC_RX_Meta_SrcMACAddress_nxt    : out std_logic;
    Eth_UC_RX_Meta_SrcMACAddress_Data   : in  T_SLV_8;
    Eth_UC_RX_Meta_DestMACAddress_nxt   : out std_logic;
    Eth_UC_RX_Meta_DestMACAddress_Data  : in  T_SLV_8;

    Eth_BC_RX_Valid                     : in  std_logic;
    Eth_BC_RX_Data                      : in  T_SLV_8;
    Eth_BC_RX_SOF                       : in  std_logic;
    Eth_BC_RX_EOF                       : in  std_logic;
    Eth_BC_RX_Ack                       : out std_logic;
```

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```
51      Eth_BC_RX_Meta_rst                    : out std_logic;
52      Eth_BC_RX_Meta_SrcMACAddress_nxt      : out std_logic;
53      Eth_BC_RX_Meta_SrcMACAddress_Data     : in  T_SLV_8;
54      Eth_BC_RX_Meta_DestMACAddress_nxt     : out std_logic;
55      Eth_BC_RX_Meta_DestMACAddress_Data    : in  T_SLV_8
56    );
57  end entity;
```

Source file: net/arp/arp_Wrapper.vhdl

7.13.2 PoC.net.eth

These are eth entities. . . .

PoC.net.eth.GEMAC_GMII

Todo: No documentation available.

Entity Declaration:

Source file: net/eth/eth_GEMAC_GMII.vhdl

PoC.net.eth.GEMAC_RX

Todo: No documentation available.

Entity Declaration:

Source file: net/eth/eth_GEMAC_RX.vhdl

PoC.net.eth.GEMAC_TX

Todo: No documentation available.

Entity Declaration:

Source file: net/eth/eth_GEMAC_TX.vhdl

PoC.net.eth.PHYController

Todo: No documentation available.

Entity Declaration:

Source file: net/eth/eth_PHYController.vhdl

PoC.net.eth.PHYController_Marvell_88E1111

Todo: No documentation available.

Entity Declaration:

Source file: net/eth/eth_PHYController_Marvell_88E1111.vhdl

PoC.net.eth.Wrapper

Todo: No documentation available.

Entity Declaration:

Source file: net/eth/eth_Wrapper.vhdl

7.13.3 PoC.net.icmpv4

These are icmpv4 entities. . . .

PoC.net.icmpv4.RX

Todo: No documentation available.

Entity Declaration:

```
1  entity icmpv4_RX is
2    generic (
3      DEBUG                         : boolean                       := FALSE
4    );
5    port (
6      Clock                         : in  std_logic;                          ↵
   ↪ --
7      Reset                         : in  std_logic;                          ↵
   ↪ --
8      -- CSE interface
9      Command                       : in  T_NET_ICMPV4_RX_COMMAND;
10     Status                        : out T_NET_ICMPV4_RX_STATUS;
11     Error                         : out T_NET_ICMPV4_RX_ERROR;
12     -- IN port
13     In_Valid                      : in  std_logic;
14     In_Data                       : in  T_SLV_8;
```

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```
    In_SOF                          : in  std_logic;
    In_EOF                          : in  std_logic;
    In_Ack                          : out std_logic;
    In_Meta_rst                     : out std_logic;
    In_Meta_SrcMACAddress_nxt       : out std_logic;
    In_Meta_SrcMACAddress_Data      : in  T_SLV_8;
    In_Meta_DestMACAddress_nxt      : out std_logic;
    In_Meta_DestMACAddress_Data     : in  T_SLV_8;
    In_Meta_SrcIPv4Address_nxt      : out std_logic;
    In_Meta_SrcIPv4Address_Data     : in  T_SLV_8;
    In_Meta_DestIPv4Address_nxt     : out std_logic;
    In_Meta_DestIPv4Address_Data    : in  T_SLV_8;
    In_Meta_Length                  : in  T_SLV_16;
    -- OUT Port
    Out_Meta_rst                    : in  std_logic;
    Out_Meta_SrcMACAddress_nxt      : in  std_logic;
    Out_Meta_SrcMACAddress_Data     : out T_SLV_8;
    Out_Meta_DestMACAddress_nxt     : in  std_logic;
    Out_Meta_DestMACAddress_Data    : out T_SLV_8;
    Out_Meta_SrcIPv4Address_nxt     : in  std_logic;
    Out_Meta_SrcIPv4Address_Data    : out T_SLV_8;
    Out_Meta_DestIPv4Address_nxt    : in  std_logic;
    Out_Meta_DestIPv4Address_Data   : out T_SLV_8;
    Out_Meta_Length                 : out T_SLV_16;
    Out_Meta_Type                   : out T_SLV_8;
    Out_Meta_Code                   : out T_SLV_8;
    Out_Meta_Identification         : out T_SLV_16;
    Out_Meta_SequenceNumber         : out T_SLV_16;
    Out_Meta_Payload_nxt            : in  std_logic;
    Out_Meta_Payload_last           : out std_logic;
    Out_Meta_Payload_Data           : out T_SLV_8
  );
end entity;
```

Source file: net/icmpv4/icmpv4_RX.vhdl

PoC.net.icmpv4.TX

Todo: No documentation available.

Entity Declaration:

```
entity icmpv4_TX is
  generic (
    DEBUG                           : boolean                       := FALSE;
    SOURCE_IPV4ADDRESS              : T_NET_IPV4_ADDRESS            := C_NET_IPV4_
↪ADDRESS_EMPTY
  );
  port (
    Clock                           : in  std_logic;
↪ --
    Reset                           : in  std_logic;
↪ --
    -- CSE interface
    Command                         : in  T_NET_ICMPV4_TX_COMMAND;
    Status                          : out T_NET_ICMPV4_TX_STATUS;
```

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```
    Error                          : out T_NET_ICMPV4_TX_ERROR;
    -- OUT port
    Out_Valid                      : out std_logic;
    Out_Data                       : out T_SLV_8;
    Out_SOF                        : out std_logic;
    Out_EOF                        : out std_logic;
    Out_Ack                        : in  std_logic;
    Out_Meta_rst                   : in  std_logic;
    Out_Meta_SrcIPv4Address_nxt    : in  std_logic;
    Out_Meta_SrcIPv4Address_Data   : out T_SLV_8;
    Out_Meta_DestIPv4Address_nxt   : in  std_logic;
    Out_Meta_DestIPv4Address_Data  : out T_SLV_8;
    Out_Meta_Length                : out T_SLV_16;
    -- IN port
    In_Meta_rst                    : out std_logic;
    In_Meta_IPv4Address_nxt        : out std_logic;
    In_Meta_IPv4Address_Data       : in  T_SLV_8;
    In_Meta_Type                   : in  T_SLV_8;
    In_Meta_Code                   : in  T_SLV_8;
    In_Meta_Identification         : in  T_SLV_16;
    In_Meta_SequenceNumber         : in  T_SLV_16;
    In_Meta_Payload_nxt            : out std_logic;
    In_Meta_Payload_last           : in  std_logic;
    In_Meta_Payload_Data           : in  T_SLV_8
  );
end entity;
```

Source file: net/icmpv4/icmpv4_TX.vhdl

PoC.net.icmpv4.Wrapper

Todo: No documentation available.

Entity Declaration:

```
entity icmpv4_Wrapper is
  generic (
    DEBUG                          : boolean              := FALSE;
    SOURCE_IPV4ADDRESS             : T_NET_IPV4_ADDRESS   := C_NET_IPV4_
↪ADDRESS_EMPTY
  );
  port (
    Clock                          : in  std_logic;
    Reset                          : in  std_logic;
    -- CSE interface
    Command                        : in  T_NET_ICMPV4_COMMAND;
    Status                         : out T_NET_ICMPV4_STATUS;
    Error                          : out T_NET_ICMPV4_ERROR;
    -- Echo-Request destination address
    IPv4Address_rst                : out std_logic;
    IPv4Address_nxt                : out std_logic;
    IPv4Address_Data               : in  T_SLV_8;
    -- to IPv4 layer
    IP_TX_Valid                    : out std_logic;
    IP_TX_Data                     : out T_SLV_8;
    IP_TX_SOF                      : out std_logic;
```

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```
    IP_TX_EOF                           : out std_logic;
    IP_TX_Ack                           : in  std_logic;
    IP_TX_Meta_rst                      : in  std_logic;
    IP_TX_Meta_SrcIPv4Address_nxt       : in  std_logic;
    IP_TX_Meta_SrcIPv4Address_Data      : out T_SLV_8;
    IP_TX_Meta_DestIPv4Address_nxt      : in  std_logic;
    IP_TX_Meta_DestIPv4Address_Data     : out T_SLV_8;
    IP_TX_Meta_Length                   : out T_SLV_16;
    -- from IPv4 layer
    IP_RX_Valid                         : in  std_logic;
    IP_RX_Data                          : in  T_SLV_8;
    IP_RX_SOF                           : in  std_logic;
    IP_RX_EOF                           : in  std_logic;
    IP_RX_Ack                           : out std_logic;
    IP_RX_Meta_rst                      : out std_logic;
    IP_RX_Meta_SrcMACAddress_nxt        : out std_logic;
    IP_RX_Meta_SrcMACAddress_Data       : in  T_SLV_8;
    IP_RX_Meta_DestMACAddress_nxt       : out std_logic;
    IP_RX_Meta_DestMACAddress_Data      : in  T_SLV_8;
--    IP_RX_Meta_EthType                  : in  T_SLV_16;
    IP_RX_Meta_SrcIPv4Address_nxt       : out std_logic;
    IP_RX_Meta_SrcIPv4Address_Data      : in  T_SLV_8;
    IP_RX_Meta_DestIPv4Address_nxt      : out std_logic;
    IP_RX_Meta_DestIPv4Address_Data     : in  T_SLV_8;
--    IP_RX_Meta_TrafficClass             : in  T_SLV_8;
--    IP_RX_Meta_FlowLabel                : in  T_SLV_24;
    IP_RX_Meta_Length                   : in  T_SLV_16
--    IP_RX_Meta_Protocol                 : in  T_SLV_8
  );
end entity;
```

Source file: net/icmpv4/icmpv4_Wrapper.vhdl

7.13.4 PoC.net.icmpv6

These are icmpv6 entities. . . .

PoC.net.icmpv6.RX

Todo: No documentation available.

Entity Declaration:

Source file: net/icmpv6/icmpv6_RX.vhdl

PoC.net.icmpv6.TX

Todo: No documentation available.

Entity Declaration:

Source file: net/icmpv6/icmpv6_TX.vhdl

PoC.net.icmpv6.Wrapper

Todo: No documentation available.

Entity Declaration:

Source file: net/icmpv6/icmpv6_Wrapper.vhdl

7.13.5 PoC.net.ipv4

These are ipv4 entities. . . .

PoC.net.ipv4.RX

Todo: No documentation available.

Entity Declaration:

```
entity ipv4_RX is
  generic (
    DEBUG                           : boolean             := FALSE
  );
  port (
    Clock                           : in  std_logic;                    --
    Reset                           : in  std_logic;                    --
    -- STATUS port
    Error                           : out std_logic;
    -- IN port
    In_Valid                        : in  std_logic;
    In_Data                         : in  T_SLV_8;
    In_SOF                          : in  std_logic;
    In_EOF                          : in  std_logic;
    In_Ack                          : out std_logic;
    In_Meta_rst                     : out std_logic;
    In_Meta_SrcMACAddress_nxt       : out std_logic;
    In_Meta_SrcMACAddress_Data      : in  T_SLV_8;
    In_Meta_DestMACAddress_nxt      : out std_logic;
    In_Meta_DestMACAddress_Data     : in  T_SLV_8;
    In_Meta_EthType                 : in  T_SLV_16;
    -- OUT port
    Out_Valid                       : out std_logic;
    Out_Data                        : out T_SLV_8;
    Out_SOF                         : out std_logic;
    Out_EOF                         : out std_logic;
    Out_Ack                         : in  std_logic;
    Out_Meta_rst                    : in  std_logic;
    Out_Meta_SrcMACAddress_nxt      : in  std_logic;
```

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```
    Out_Meta_SrcMACAddress_Data      : out T_SLV_8;
    Out_Meta_DestMACAddress_nxt      : in  std_logic;
    Out_Meta_DestMACAddress_Data     : out T_SLV_8;
    Out_Meta_EthType                 : out T_SLV_16;
    Out_Meta_SrcIPv4Address_nxt      : in  std_logic;
    Out_Meta_SrcIPv4Address_Data     : out T_SLV_8;
    Out_Meta_DestIPv4Address_nxt     : in  std_logic;
    Out_Meta_DestIPv4Address_Data    : out T_SLV_8;
    Out_Meta_Length                  : out T_SLV_16;
    Out_Meta_Protocol                : out T_SLV_8
  );
end entity;
```

Source file: net/ipv4/ipv4_RX.vhdl

PoC.net.ipv4.TX

Todo: No documentation available.

Entity Declaration:

```
entity ipv4_TX is
  generic (
    DEBUG                          : boolean             := FALSE
  );
  port (
    Clock                          : in  std_logic;                    --
    Reset                          : in  std_logic;                    --
    -- IN port
    In_Valid                       : in  std_logic;
    In_Data                        : in  T_SLV_8;
    In_SOF                         : in  std_logic;
    In_EOF                         : in  std_logic;
    In_Ack                         : out std_logic;
    In_Meta_rst                    : out std_logic;
    In_Meta_SrcIPv4Address_nxt     : out std_logic;
    In_Meta_SrcIPv4Address_Data    : in  T_SLV_8;
    In_Meta_DestIPv4Address_nxt    : out std_logic;
    In_Meta_DestIPv4Address_Data   : in  T_SLV_8;
    In_Meta_Length                 : in  T_SLV_16;
    In_Meta_Protocol               : in  T_SLV_8;
    -- ARP port
    ARP_IPCache_Query              : out std_logic;
    ARP_IPCache_IPv4Address_rst    : in  std_logic;
    ARP_IPCache_IPv4Address_nxt    : in  std_logic;
    ARP_IPCache_IPv4Address_Data   : out T_SLV_8;
    ARP_IPCache_Valid              : in  std_logic;
    ARP_IPCache_MACAddress_rst     : out std_logic;
    ARP_IPCache_MACAddress_nxt     : out std_logic;
    ARP_IPCache_MACAddress_Data    : in  T_SLV_8;
    -- OUT port
    Out_Valid                      : out std_logic;
    Out_Data                       : out T_SLV_8;
    Out_SOF                        : out std_logic;
    Out_EOF                        : out std_logic;
    Out_Ack                        : in  std_logic;
```

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```
    Out_Meta_rst                    : in  std_logic;
    Out_Meta_DestMACAddress_nxt     : in  std_logic;
    Out_Meta_DestMACAddress_Data    : out T_SLV_8
  );
end entity;
```

Source file: net/ipv4/ipv4_TX.vhdl

PoC.net.ipv4.FrameLoopback

Todo: No documentation available.

Entity Declaration:

```
entity ipv4_FrameLoopback is
  generic (
    MAX_FRAMES                  : positive          := 4
  );
  port (
    Clock                       : in  std_logic;
    Reset                       : in  std_logic;
    -- IN port
    In_Valid                    : in  std_logic;
    In_Data                     : in  T_SLV_8;
    In_SOF                      : in  std_logic;
    In_EOF                      : in  std_logic;
    In_Ack                      : out std_logic;
    In_Meta_rst                 : out std_logic;
    In_Meta_SrcIPv4Address_nxt  : out std_logic;
    In_Meta_SrcIPv4Address_Data : in  T_SLV_8;
    In_Meta_DestIPv4Address_nxt : out std_logic;
    In_Meta_DestIPv4Address_Data: in  T_SLV_8;
    In_Meta_Length              : in  T_SLV_16;
    -- OUT port
    Out_Valid                   : out std_logic;
    Out_Data                    : out T_SLV_8;
    Out_SOF                     : out std_logic;
    Out_EOF                     : out std_logic;
    Out_Ack                     : in  std_logic;
    Out_Meta_rst                : in  std_logic;
    Out_Meta_SrcIPv4Address_nxt : in  std_logic;
    Out_Meta_SrcIPv4Address_Data: out T_SLV_8;
    Out_Meta_DestIPv4Address_nxt: in  std_logic;
    Out_Meta_DestIPv4Address_Data: out T_SLV_8;
    Out_Meta_Length             : out T_SLV_16
  );
end entity;
```

Source file: net/ipv4/ipv4_FrameLoopback.vhdl

PoC.net.ipv4.Wrapper

Todo: No documentation available.

Entity Declaration:

```
entity ipv4_Wrapper is
  generic (
    DEBUG                           : boolean                       := FALSE;
    PACKET_TYPES                    : T_NET_IPV4_PROTOCOL_VECTOR    := (0 => x"00")
  );
  port (
    Clock                           : in  std_logic;
    Reset                           : in  std_logic;
    -- to MAC layer
    MAC_TX_Valid                    : out std_logic;
    MAC_TX_Data                     : out T_SLV_8;
    MAC_TX_SOF                      : out std_logic;
    MAC_TX_EOF                      : out std_logic;
    MAC_TX_Ack                      : in  std_logic;
    MAC_TX_Meta_rst                 : in  std_logic;
    MAC_TX_Meta_DestMACAddress_nxt  : in  std_logic;
    MAC_TX_Meta_DestMACAddress_Data : out T_SLV_8;
    -- from MAC layer
    MAC_RX_Valid                    : in  std_logic;
    MAC_RX_Data                     : in  T_SLV_8;
    MAC_RX_SOF                      : in  std_logic;
    MAC_RX_EOF                      : in  std_logic;
    MAC_RX_Ack                      : out std_logic;
    MAC_RX_Meta_rst                 : out std_logic;
    MAC_RX_Meta_SrcMACAddress_nxt   : out std_logic;
    MAC_RX_Meta_SrcMACAddress_Data  : in  T_SLV_8;
    MAC_RX_Meta_DestMACAddress_nxt  : out std_logic;
    MAC_RX_Meta_DestMACAddress_Data : in  T_SLV_8;
    MAC_RX_Meta_EthType             : in  T_SLV_16;
    -- to ARP
    ARP_IPCache_Query               : out std_logic;
    ARP_IPCache_IPv4Address_rst     : in  std_logic;
    ARP_IPCache_IPv4Address_nxt     : in  std_logic;
    ARP_IPCache_IPv4Address_Data    : out T_SLV_8;
    -- from ARP
    ARP_IPCache_Valid               : in  std_logic;
    ARP_IPCache_MACAddress_rst      : out std_logic;
    ARP_IPCache_MACAddress_nxt      : out std_logic;
    ARP_IPCache_MACAddress_Data     : in  T_SLV_8;
    -- from upper layer
    TX_Valid                        : in  std_logic_vector(PACKET_TYPES'length - 1
↪downto 0);
    TX_Data                         : in  T_SLVV_8(PACKET_TYPES'length - 1 downto
↪0);
    TX_SOF                          : in  std_logic_vector(PACKET_TYPES'length - 1
↪downto 0);
    TX_EOF                          : in  std_logic_vector(PACKET_TYPES'length - 1
↪downto 0);
    TX_Ack                          : out std_logic_vector(PACKET_TYPES'length - 1
↪downto 0);
    TX_Meta_rst                     : out std_logic_vector(PACKET_TYPES'length - 1
↪downto 0);
    TX_Meta_SrcIPv4Address_nxt      : out std_logic_vector(PACKET_TYPES'length - 1
↪downto 0);
    TX_Meta_SrcIPv4Address_Data     : in  T_SLVV_8(PACKET_TYPES'length - 1 downto
↪0);
    TX_Meta_DestIPv4Address_nxt     : out std_logic_vector(PACKET_TYPES'length - 1
↪downto 0);
    TX_Meta_DestIPv4Address_Data    : in  T_SLVV_8(PACKET_TYPES'length - 1 downto
↪0);
```

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```
    TX_Meta_Length                  : in  T_SLVV_16(PACKET_TYPES'length - 1 downto 0);
    -- to upper layer
    RX_Valid                        : out std_logic_vector(PACKET_TYPES'length - 1 downto 0);
    RX_Data                         : out T_SLVV_8(PACKET_TYPES'length - 1 downto 0);
    RX_SOF                          : out std_logic_vector(PACKET_TYPES'length - 1 downto 0);
    RX_EOF                          : out std_logic_vector(PACKET_TYPES'length - 1 downto 0);
    RX_Ack                          : in  std_logic_vector(PACKET_TYPES'length - 1 downto 0);
    RX_Meta_rst                     : in  std_logic_vector(PACKET_TYPES'length - 1 downto 0);
    RX_Meta_SrcMACAddress_nxt       : in  std_logic_vector(PACKET_TYPES'length - 1 downto 0);
    RX_Meta_SrcMACAddress_Data      : out T_SLVV_8(PACKET_TYPES'length - 1 downto 0);
    RX_Meta_DestMACAddress_nxt      : in  std_logic_vector(PACKET_TYPES'length - 1 downto 0);
    RX_Meta_DestMACAddress_Data     : out T_SLVV_8(PACKET_TYPES'length - 1 downto 0);
    RX_Meta_EthType                 : out T_SLVV_16(PACKET_TYPES'length - 1 downto 0);
    RX_Meta_SrcIPv4Address_nxt      : in  std_logic_vector(PACKET_TYPES'length - 1 downto 0);
    RX_Meta_SrcIPv4Address_Data     : out T_SLVV_8(PACKET_TYPES'length - 1 downto 0);
    RX_Meta_DestIPv4Address_nxt     : in  std_logic_vector(PACKET_TYPES'length - 1 downto 0);
    RX_Meta_DestIPv4Address_Data    : out T_SLVV_8(PACKET_TYPES'length - 1 downto 0);
    RX_Meta_Length                  : out T_SLVV_16(PACKET_TYPES'length - 1 downto 0);
    RX_Meta_Protocol                : out T_SLVV_8(PACKET_TYPES'length - 1 downto 0)
  );
end entity;
```

Source file: net/ipv4/ipv4_Wrapper.vhdl

7.13.6 PoC.net.ipv6

These are ipv6 entities. . . .

PoC.net.ipv6.RX

Todo: No documentation available.

Entity Declaration:

```
entity ipv6_RX is
  generic (
    DEBUG                           : boolean             := FALSE
```

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```
  );
  port (
    Clock                           : in  std_logic;                    --
    Reset                           : in  std_logic;                    --
    -- STATUS port
    Error                           : out std_logic;
    -- IN port
    In_Valid                        : in  std_logic;
    In_Data                         : in  T_SLV_8;
    In_SOF                          : in  std_logic;
    In_EOF                          : in  std_logic;
    In_Ack                          : out std_logic;
    In_Meta_rst                     : out std_logic;
    In_Meta_SrcMACAddress_nxt       : out std_logic;
    In_Meta_SrcMACAddress_Data      : in  T_SLV_8;
    In_Meta_DestMACAddress_nxt      : out std_logic;
    In_Meta_DestMACAddress_Data     : in  T_SLV_8;
    In_Meta_EthType                 : in  T_SLV_16;
    -- OUT port
    Out_Valid                       : out std_logic;
    Out_Data                        : out T_SLV_8;
    Out_SOF                         : out std_logic;
    Out_EOF                         : out std_logic;
    Out_Ack                         : in  std_logic;
    Out_Meta_rst                    : in  std_logic;
    Out_Meta_SrcMACAddress_nxt      : in  std_logic;
    Out_Meta_SrcMACAddress_Data     : out T_SLV_8;
    Out_Meta_DestMACAddress_nxt     : in  std_logic;
    Out_Meta_DestMACAddress_Data    : out T_SLV_8;
    Out_Meta_EthType                : out T_SLV_16;
    Out_Meta_SrcIPv6Address_nxt     : in  std_logic;
    Out_Meta_SrcIPv6Address_Data    : out T_SLV_8;
    Out_Meta_DestIPv6Address_nxt    : in  std_logic;
    Out_Meta_DestIPv6Address_Data   : out T_SLV_8;
    Out_Meta_TrafficClass           : out T_SLV_8;
    Out_Meta_FlowLabel              : out T_SLV_24; --STD_LOGIC_VECTOR(19 downto␣
↪0);
    Out_Meta_Length                 : out T_SLV_16;
    Out_Meta_NextHeader             : out T_SLV_8
  );
end entity;
```

Source file: net/ipv6/ipv6_RX.vhdl

PoC.net.ipv6.TX

Todo: No documentation available.

Entity Declaration:

```
entity ipv6_TX is
  generic (
    DEBUG                           : boolean             := FALSE
  );
  port (
    Clock                           : in  std_logic;                    --
```

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```
    Reset                           : in  std_logic;                  --
    -- IN port
    In_Valid                        : in  std_logic;
    In_Data                         : in  T_SLV_8;
    In_SOF                          : in  std_logic;
    In_EOF                          : in  std_logic;
    In_Ack                          : out std_logic;
    In_Meta_rst                     : out std_logic;
    In_Meta_SrcIPv6Address_nxt      : out std_logic;
    In_Meta_SrcIPv6Address_Data     : in  T_SLV_8;
    In_Meta_DestIPv6Address_nxt     : out std_logic;
    In_Meta_DestIPv6Address_Data    : in  T_SLV_8;
    In_Meta_TrafficClass            : in  T_SLV_8;
    In_Meta_FlowLabel               : in  T_SLV_24; --STD_LOGIC_VECTOR(19 downto␣
↪0);
    In_Meta_Length                  : in  T_SLV_16;
    In_Meta_NextHeader              : in  T_SLV_8;
    -- to NDP layer
    NDP_NextHop_Query               : out std_logic;
    NDP_NextHop_IPv6Address_rst     : in  std_logic;
    NDP_NextHop_IPv6Address_nxt     : in  std_logic;
    NDP_NextHop_IPv6Address_Data    : out T_SLV_8;
    -- from NDP layer
    NDP_NextHop_Valid               : in  std_logic;
    NDP_NextHop_MACAddress_rst      : out std_logic;
    NDP_NextHop_MACAddress_nxt      : out std_logic;
    NDP_NextHop_MACAddress_Data     : in  T_SLV_8;
    -- OUT port
    Out_Valid                       : out std_logic;
    Out_Data                        : out T_SLV_8;
    Out_SOF                         : out std_logic;
    Out_EOF                         : out std_logic;
    Out_Ack                         : in  std_logic;
    Out_Meta_rst                    : in  std_logic;
    Out_Meta_DestMACAddress_nxt     : in  std_logic;
    Out_Meta_DestMACAddress_Data    : out T_SLV_8
  );
end entity;
```

Source file: net/ipv6/ipv6_TX.vhdl

PoC.net.ipv6.FrameLoopback

Todo: No documentation available.

Entity Declaration:

```
entity ipv6_FrameLoopback is
  generic (
    MAX_FRAMES                  : positive          := 4
  );
  port (
    Clock                       : in  std_logic;
    Reset                       : in  std_logic;
    -- IN port
    In_Valid                    : in  std_logic;
```

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```
    In_Data                         : in  T_SLV_8;
    In_SOF                          : in  std_logic;
    In_EOF                          : in  std_logic;
    In_Ack                          : out std_logic;
    In_Meta_rst                     : out std_logic;
    In_Meta_SrcIPv6Address_nxt      : out std_logic;
    In_Meta_SrcIPv6Address_Data     : in  T_SLV_8;
    In_Meta_DestIPv6Address_nxt     : out std_logic;
    In_Meta_DestIPv6Address_Data    : in  T_SLV_8;
    In_Meta_Length                  : in  T_SLV_16;
    -- OUT port
    Out_Valid                       : out std_logic;
    Out_Data                        : out T_SLV_8;
    Out_SOF                         : out std_logic;
    Out_EOF                         : out std_logic;
    Out_Ack                         : in  std_logic;
    Out_Meta_rst                    : in  std_logic;
    Out_Meta_SrcIPv6Address_nxt     : in  std_logic;
    Out_Meta_SrcIPv6Address_Data    : out T_SLV_8;
    Out_Meta_DestIPv6Address_nxt    : in  std_logic;
    Out_Meta_DestIPv6Address_Data   : out T_SLV_8;
    Out_Meta_Length                 : out T_SLV_16
  );
end entity;
```

Source file: net/ipv6/ipv6_FrameLoopback.vhdl

PoC.net.ipv6.Wrapper

Todo: No documentation available.

Entity Declaration:

```
entity ipv6_Wrapper is
  generic (
    DEBUG                           : boolean                           := FALSE;
    PACKET_TYPES                    : T_NET_IPV6_NEXT_HEADER_VECTOR     := (0 => x"00
↪")
  );
  port (
    Clock                           : in  std_logic;
    Reset                           : in  std_logic;
    -- to MAC layer
    MAC_TX_Valid                    : out std_logic;
    MAC_TX_Data                     : out T_SLV_8;
    MAC_TX_SOF                      : out std_logic;
    MAC_TX_EOF                      : out std_logic;
    MAC_TX_Ack                      : in  std_logic;
    MAC_TX_Meta_rst                 : in  std_logic;
    MAC_TX_Meta_DestMACAddress_nxt  : in  std_logic;
    MAC_TX_Meta_DestMACAddress_Data : out T_SLV_8;
    -- from MAC layer
    MAC_RX_Valid                    : in  std_logic;
    MAC_RX_Data                     : in  T_SLV_8;
    MAC_RX_SOF                      : in  std_logic;
    MAC_RX_EOF                      : in  std_logic;
```

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```
    MAC_RX_Ack                      : out std_logic;
    MAC_RX_Meta_rst                 : out std_logic;
    MAC_RX_Meta_SrcMACAddress_nxt   : out std_logic;
    MAC_RX_Meta_SrcMACAddress_Data  : in  T_SLV_8;
    MAC_RX_Meta_DestMACAddress_nxt  : out std_logic;
    MAC_RX_Meta_DestMACAddress_Data : in  T_SLV_8;
    MAC_RX_Meta_EthType             : in  T_SLV_16;
    -- to NDP layer
    NDP_NextHop_Query               : out std_logic;
    NDP_NextHop_IPv6Address_rst     : in  std_logic;
    NDP_NextHop_IPv6Address_nxt     : in  std_logic;
    NDP_NextHop_IPv6Address_Data    : out T_SLV_8;
    -- from NDP layer
    NDP_NextHop_Valid               : in  std_logic;
    NDP_NextHop_MACAddress_rst      : out std_logic;
    NDP_NextHop_MACAddress_nxt      : out std_logic;
    NDP_NextHop_MACAddress_Data     : in  T_SLV_8;
    -- from upper layer
    TX_Valid                        : in  std_logic_vector(PACKET_TYPES'length - 1
↪downto 0);
    TX_Data                         : in  T_SLVV_8(PACKET_TYPES'length - 1 downto
↪0);
    TX_SOF                          : in  std_logic_vector(PACKET_TYPES'length - 1
↪downto 0);
    TX_EOF                          : in  std_logic_vector(PACKET_TYPES'length - 1
↪downto 0);
    TX_Ack                          : out std_logic_vector(PACKET_TYPES'length - 1
↪downto 0);
    TX_Meta_rst                     : out std_logic_vector(PACKET_TYPES'length - 1
↪downto 0);
    TX_Meta_SrcIPv6Address_nxt      : out std_logic_vector(PACKET_TYPES'length - 1
↪downto 0);
    TX_Meta_SrcIPv6Address_Data     : in  T_SLVV_8(PACKET_TYPES'length - 1 downto
↪0);
    TX_Meta_DestIPv6Address_nxt     : out std_logic_vector(PACKET_TYPES'length - 1
↪downto 0);
    TX_Meta_DestIPv6Address_Data    : in  T_SLVV_8(PACKET_TYPES'length - 1 downto
↪0);
    TX_Meta_TrafficClass            : in  T_SLVV_8(PACKET_TYPES'length - 1 downto
↪0);
    TX_Meta_FlowLabel               : in  T_SLVV_24(PACKET_TYPES'length - 1 downto
↪0);
    TX_Meta_Length                  : in  T_SLVV_16(PACKET_TYPES'length - 1 downto
↪0);
    -- to upper layer
    RX_Valid                        : out std_logic_vector(PACKET_TYPES'length - 1
↪downto 0);
    RX_Data                         : out T_SLVV_8(PACKET_TYPES'length - 1 downto
↪0);
    RX_SOF                          : out std_logic_vector(PACKET_TYPES'length - 1
↪downto 0);
    RX_EOF                          : out std_logic_vector(PACKET_TYPES'length - 1
↪downto 0);
    RX_Ack                          : in  std_logic_vector(PACKET_TYPES'length - 1
↪downto 0);
    RX_Meta_rst                     : in  std_logic_vector(PACKET_TYPES'length - 1
↪downto 0);
    RX_Meta_SrcMACAddress_nxt       : in  std_logic_vector(PACKET_TYPES'length - 1
↪downto 0);
    RX_Meta_SrcMACAddress_Data      : out T_SLVV_8(PACKET_TYPES'length - 1 downto
↪0);
```

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```
    RX_Meta_DestMACAddress_nxt      : in  std_logic_vector(PACKET_TYPES'length - 1 downto 0);
    RX_Meta_DestMACAddress_Data     : out T_SLVV_8(PACKET_TYPES'length - 1 downto 0);
    RX_Meta_EthType                 : out T_SLVV_16(PACKET_TYPES'length - 1 downto 0);
    RX_Meta_SrcIPv6Address_nxt      : in  std_logic_vector(PACKET_TYPES'length - 1 downto 0);
    RX_Meta_SrcIPv6Address_Data     : out T_SLVV_8(PACKET_TYPES'length - 1 downto 0);
    RX_Meta_DestIPv6Address_nxt     : in  std_logic_vector(PACKET_TYPES'length - 1 downto 0);
    RX_Meta_DestIPv6Address_Data    : out T_SLVV_8(PACKET_TYPES'length - 1 downto 0);
    RX_Meta_TrafficClass            : out T_SLVV_8(PACKET_TYPES'length - 1 downto 0);
    RX_Meta_FlowLabel               : out T_SLVV_24(PACKET_TYPES'length - 1 downto 0);
    RX_Meta_Length                  : out T_SLVV_16(PACKET_TYPES'length - 1 downto 0);
    RX_Meta_NextHeader              : out T_SLVV_8(PACKET_TYPES'length - 1 downto 0)
  );
end entity;
```

Source file: net/ipv6/ipv6_Wrapper.vhdl

7.13.7 PoC.net.mac

These are mac entities. . . .

PoC.net.mac.RX_DestMAC_Switch

Todo: No documentation available.

Entity Declaration:

```
entity mac_RX_DestMAC_Switch is
  generic (
    DEBUG                       : boolean                       := FALSE;
    MAC_ADDRESSES               : T_NET_MAC_ADDRESS_VECTOR    := (0 => C_NET_MAC_ADDRESS_EMPTY);
    MAC_ADDRESSE_MASKS          : T_NET_MAC_ADDRESS_VECTOR    := (0 => C_NET_MAC_MASK_DEFAULT)
  );
  port (
    Clock                       : in  std_logic;
    Reset                       : in  std_logic;

    In_Valid                    : in  std_logic;
    In_Data                     : in  T_SLV_8;
    In_SOF                      : in  std_logic;
    In_EOF                      : in  std_logic;
    In_Ack                      : out std_logic;

```

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```
    Out_Valid                     : out std_logic_vector(MAC_ADDRESSES'length - 1 downto 0);
    Out_Data                      : out T_SLVV_8(MAC_ADDRESSES'length - 1 downto 0);
    Out_SOF                       : out std_logic_vector(MAC_ADDRESSES'length - 1 downto 0);
    Out_EOF                       : out std_logic_vector(MAC_ADDRESSES'length - 1 downto 0);
    Out_Ack                       : in  std_logic_vector(MAC_ADDRESSES'length - 1 downto 0);
    Out_Meta_DestMACAddress_rst   : in  std_logic_vector(MAC_ADDRESSES'length - 1 downto 0);
    Out_Meta_DestMACAddress_nxt   : in  std_logic_vector(MAC_ADDRESSES'length - 1 downto 0);
    Out_Meta_DestMACAddress_Data  : out T_SLVV_8(MAC_ADDRESSES'length - 1 downto 0)
  );
end entity;
```

Source file: net/mac/mac_RX_DestMAC_Switch.vhdl

PoC.net.mac.RX_SrcMAC_Filter

Todo: No documentation available.

Entity Declaration:

```
entity mac_RX_SrcMAC_Filter is
  generic (
    DEBUG                         : boolean                         := FALSE;
    MAC_ADDRESSES                 : T_NET_MAC_ADDRESS_VECTOR        := (0 => C_NET_MAC_ADDRESS_EMPTY);
    MAC_ADDRESSE_MASKS            : T_NET_MAC_ADDRESS_VECTOR        := (0 => C_NET_MAC_MASK_DEFAULT)
  );
  port (
    Clock                         : in  std_logic;
    Reset                         : in  std_logic;

    In_Valid                      : in  std_logic;
    In_Data                       : in  T_SLV_8;
    In_SOF                        : in  std_logic;
    In_EOF                        : in  std_logic;
    In_Ack                        : out std_logic;
    In_Meta_rst                   : out std_logic;
    In_Meta_DestMACAddress_nxt    : out std_logic;
    In_Meta_DestMACAddress_Data   : in  T_SLV_8;

    Out_Valid                     : out std_logic;
    Out_Data                      : out T_SLV_8;
    Out_SOF                       : out std_logic;
    Out_EOF                       : out std_logic;
    Out_Ack                       : in  std_logic;
    Out_Meta_rst                  : in  std_logic;
    Out_Meta_DestMACAddress_nxt   : in  std_logic;
    Out_Meta_DestMACAddress_Data  : out T_SLV_8;
    Out_Meta_SrcMACAddress_nxt    : in  std_logic;
```

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```
    Out_Meta_SrcMACAddress_Data    : out T_SLV_8
  );
end entity;
```

Source file: net/mac/mac_RX_SrcMAC_Filter.vhdl

PoC.net.mac.RX_Type_Switch

Todo: No documentation available.

Entity Declaration:

```
entity mac_RX_Type_Switch is
  generic (
    DEBUG                          : boolean                          := FALSE;
    ETHERNET_TYPES                 : T_NET_MAC_ETHERNETTYPE_VECTOR    := (0 => C_NET_
↪MAC_ETHERNETTYPE_EMPTY)
  );
  port (
    Clock                          : in  std_logic;
    Reset                          : in  std_logic;

    In_Valid                       : in  std_logic;
    In_Data                        : in  T_SLV_8;
    In_SOF                         : in  std_logic;
    In_EOF                         : in  std_logic;
    In_Ack                         : out std_logic;
    In_Meta_rst                    : out std_logic;
    In_Meta_SrcMACAddress_nxt      : out std_logic;
    In_Meta_SrcMACAddress_Data     : in  T_SLV_8;
    In_Meta_DestMACAddress_nxt     : out std_logic;
    In_Meta_DestMACAddress_Data    : in  T_SLV_8;

    Out_Valid                      : out std_logic_vector(ETHERNET_TYPES'length - 1␣
↪downto 0);
    Out_Data                       : out T_SLVV_8(ETHERNET_TYPES'length - 1 downto␣
↪0);
    Out_SOF                        : out std_logic_vector(ETHERNET_TYPES'length - 1␣
↪downto 0);
    Out_EOF                        : out std_logic_vector(ETHERNET_TYPES'length - 1␣
↪downto 0);
    Out_Ack                        : in  std_logic_vector(ETHERNET_TYPES'length - 1␣
↪downto 0);
    Out_Meta_rst                   : in  std_logic_vector(ETHERNET_TYPES'length - 1␣
↪downto 0);
    Out_Meta_SrcMACAddress_nxt     : in  std_logic_vector(ETHERNET_TYPES'length - 1␣
↪downto 0);
    Out_Meta_SrcMACAddress_Data    : out T_SLVV_8(ETHERNET_TYPES'length - 1 downto␣
↪0);
    Out_Meta_DestMACAddress_nxt    : in  std_logic_vector(ETHERNET_TYPES'length - 1␣
↪downto 0);
    Out_Meta_DestMACAddress_Data   : out T_SLVV_8(ETHERNET_TYPES'length - 1 downto␣
↪0);
    Out_Meta_EthType               : out T_NET_MAC_ETHERNETTYPE_VECTOR(ETHERNET_
↪TYPES'length - 1 downto 0)
  );
```

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```
33 end entity;
```

Source file: net/mac/mac_RX_Type_Switch.vhdl

PoC.net.mac.TX_SrcMAC_Prepender

Todo: No documentation available.

Entity Declaration:

```
1  entity mac_TX_SrcMAC_Prepender is
2    generic (
3      DEBUG                         : boolean                         := FALSE;
4      MAC_ADDRESSES                 : T_NET_MAC_ADDRESS_VECTOR        := (0 => C_NET_
   ↪MAC_ADDRESS_EMPTY)
5    );
6    port (
7      Clock                         : in  std_logic;
8      Reset                         : in  std_logic;
9      -- IN Port
10     In_Valid                      : in  std_logic_vector(MAC_ADDRESSES'length - 1␣
   ↪downto 0);
11     In_Data                       : in  T_SLVV_8(MAC_ADDRESSES'length - 1 downto␣
   ↪0);
12     In_SOF                        : in  std_logic_vector(MAC_ADDRESSES'length - 1␣
   ↪downto 0);
13     In_EOF                        : in  std_logic_vector(MAC_ADDRESSES'length - 1␣
   ↪downto 0);
14     In_Ack                        : out std_logic_vector(MAC_ADDRESSES'length - 1␣
   ↪downto 0);
15     In_Meta_rst                   : out std_logic_vector(MAC_ADDRESSES'length - 1␣
   ↪downto 0);
16     In_Meta_DestMACAddress_nxt    : out std_logic_vector(MAC_ADDRESSES'length - 1␣
   ↪downto 0);
17     In_Meta_DestMACAddress_Data   : in  T_SLVV_8(MAC_ADDRESSES'length - 1 downto␣
   ↪0);
18     -- OUT Port
19     Out_Valid                     : out std_logic;
20     Out_Data                      : out T_SLV_8;
21     Out_SOF                       : out std_logic;
22     Out_EOF                       : out std_logic;
23     Out_Ack                       : in  std_logic;
24     Out_Meta_rst                  : in  std_logic;
25     Out_Meta_DestMACAddress_nxt   : in  std_logic;
26     Out_Meta_DestMACAddress_Data  : out T_SLV_8
27   );
28 end entity;
```

Source file: net/mac/mac_TX_SrcMAC_Prepender.vhdl

PoC.net.mac.TX_DestMAC_Prepender

Todo: No documentation available.

Entity Declaration:

```
entity mac_TX_DestMAC_Prepender is
  generic (
    DEBUG                           : boolean                       := FALSE
  );
  port (
    Clock                           : in  std_logic;
    Reset                           : in  std_logic;

    In_Valid                        : in  std_logic;
    In_Data                         : in  T_SLV_8;
    In_SOF                          : in  std_logic;
    In_EOF                          : in  std_logic;
    In_Ack                          : out std_logic;
    In_Meta_rst                     : out std_logic;
    In_Meta_DestMACAddress_nxt      : out std_logic;
    In_Meta_DestMACAddress_Data     : in  T_SLV_8;

    Out_Valid                       : out std_logic;
    Out_Data                        : out T_SLV_8;
    Out_SOF                         : out std_logic;
    Out_EOF                         : out std_logic;
    Out_Ack                         : in  std_logic
  );
end entity;
```

Source file: net/mac/mac_TX_DestMAC_Prepender.vhdl

PoC.net.mac.TX_Type_Prepender

Todo: No documentation available.

Entity Declaration:

Source file: net/mac/mac_TX_Type_Prepender.vhdl

PoC.net.mac.FrameLoopback

Todo: No documentation available.

Entity Declaration:

```
entity mac_FrameLoopback is
  generic (
    MAX_FRAMES                      : positive              := 4
  );
  port (
    Clock                           : in  std_logic;
    Reset                           : in  std_logic;
    -- IN Port
    In_Valid                        : in  std_logic;
```

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```
    In_Data                         : in  T_SLV_8;
    In_SOF                          : in  std_logic;
    In_EOF                          : in  std_logic;
    In_Ack                          : out std_logic;
    In_Meta_rst                     : out std_logic;
    In_Meta_SrcMACAddress_nxt       : out std_logic;
    In_Meta_SrcMACAddress_Data      : in  T_SLV_8;
    In_Meta_DestMACAddress_nxt      : out std_logic;
    In_Meta_DestMACAddress_Data     : in  T_SLV_8;
    -- OUT Port
    Out_Valid                       : out std_logic;
    Out_Data                        : out T_SLV_8;
    Out_SOF                         : out std_logic;
    Out_EOF                         : out std_logic;
    Out_Ack                         : in  std_logic;
    Out_Meta_rst                    : in  std_logic;
    Out_Meta_SrcMACAddress_nxt      : in  std_logic;
    Out_Meta_SrcMACAddress_Data     : out T_SLV_8;
    Out_Meta_DestMACAddress_nxt     : in  std_logic;
    Out_Meta_DestMACAddress_Data    : out T_SLV_8
  );
end entity;
```

Source file: net/mac/mac_FrameLoopback.vhdl

PoC.net.mac.Wrapper

Todo: No documentation available.

Entity Declaration:

```
entity mac_Wrapper is
  generic (
    DEBUG                           : boolean                                 := FALSE;
    MAC_CONFIG                      : T_NET_MAC_CONFIGURATION_VECTOR
  );
  port (
    Clock                           : in  std_logic;
    Reset                           : in  std_logic;

    Eth_TX_Valid                    : out std_logic;
    Eth_TX_Data                     : out T_SLV_8;
    Eth_TX_SOF                      : out std_logic;
    Eth_TX_EOF                      : out std_logic;
    Eth_TX_Ack                      : in  std_logic;

    Eth_RX_Valid                    : in  std_logic;
    Eth_RX_Data                     : in  T_SLV_8;
    Eth_RX_SOF                      : in  std_logic;
    Eth_RX_EOF                      : in  std_logic;
    Eth_RX_Ack                      : out std_logic;

    TX_Valid                        : in  std_logic_vector(getPortCount(MAC_CONFIG) -␣
↪1 downto 0);
    TX_Data                         : in  T_SLVV_8(getPortCount(MAC_CONFIG) - 1 downto␣
↪0);
```

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```
    TX_SOF                        : in  std_logic_vector(getPortCount(MAC_CONFIG) - 1 downto 0);
    TX_EOF                        : in  std_logic_vector(getPortCount(MAC_CONFIG) - 1 downto 0);
    TX_Ack                        : out std_logic_vector(getPortCount(MAC_CONFIG) - 1 downto 0);
    TX_Meta_rst                   : out std_logic_vector(getPortCount(MAC_CONFIG) - 1 downto 0);
    TX_Meta_DestMACAddress_nxt    : out std_logic_vector(getPortCount(MAC_CONFIG) - 1 downto 0);
    TX_Meta_DestMACAddress_Data   : in  T_SLVV_8(getPortCount(MAC_CONFIG) - 1 downto 0);

    RX_Valid                      : out std_logic_vector(getPortCount(MAC_CONFIG) - 1 downto 0);
    RX_Data                       : out T_SLVV_8(getPortCount(MAC_CONFIG) - 1 downto 0);
    RX_SOF                        : out std_logic_vector(getPortCount(MAC_CONFIG) - 1 downto 0);
    RX_EOF                        : out std_logic_vector(getPortCount(MAC_CONFIG) - 1 downto 0);
    RX_Ack                        : in  std_logic_vector(getPortCount(MAC_CONFIG) - 1 downto 0);
    RX_Meta_rst                   : in  std_logic_vector(getPortCount(MAC_CONFIG) - 1 downto 0);
    RX_Meta_SrcMACAddress_nxt     : in  std_logic_vector(getPortCount(MAC_CONFIG) - 1 downto 0);
    RX_Meta_SrcMACAddress_Data    : out T_SLVV_8(getPortCount(MAC_CONFIG) - 1 downto 0);
    RX_Meta_DestMACAddress_nxt    : in  std_logic_vector(getPortCount(MAC_CONFIG) - 1 downto 0);
    RX_Meta_DestMACAddress_Data   : out T_SLVV_8(getPortCount(MAC_CONFIG) - 1 downto 0);
    RX_Meta_EthType               : out T_NET_MAC_ETHERNETTYPE_VECTOR(getPortCount(MAC_CONFIG) - 1 downto 0)
  );
end entity;
```

Source file: net/mac/mac_Wrapper.vhdl

7.13.8 PoC.net.ndp

These are ndp entities. . . .

PoC.net.ndp.DestinationCache

Todo: No documentation available.

Entity Declaration:

Source file: net/ndp/ndp_DestinationCache.vhdl

PoC.net.ndp.FSMQuery

Todo: No documentation available.

Entity Declaration:

Source file: net/ndp/ndp_FSMQuery.vhdl

PoC.net.ndp.NeighborCache

Todo: No documentation available.

Entity Declaration:

Source file: net/ndp/ndp_NeighborCache.vhdl

PoC.net.ndp.Wrapper

Todo: No documentation available.

Entity Declaration:

Source file: net/ndp/ndp_Wrapper.vhdl

7.13.9 PoC.net.stack

These are udp entities. . . .

stack_IPv4

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stack_IPv6

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PoC.net.stack.UDPv4

Todo: No documentation available.

Entity Declaration:

Source file: net/stack/stack_UDPv4.vhdl

stack_UDPv6

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stack_MAC

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7.13.10 PoC.net.udp

These are udp entities. . . .

PoC.net.udp.RX

Todo: No documentation available.

Entity Declaration:

```
entity udp_RX is
  generic (
    DEBUG                          : boolean           := FALSE;
    IP_VERSION                     : positive          := 6
  );
  port (
    Clock                          : in  std_logic;                --
    Reset                          : in  std_logic;                --
    -- STATUS port
    Error                          : out std_logic;
    -- IN port
    In_Valid                       : in  std_logic;
    In_Data                        : in  T_SLV_8;
```

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```
    In_SOF                          : in  std_logic;
    In_EOF                          : in  std_logic;
    In_Ack                          : out std_logic;
    In_Meta_rst                     : out std_logic;
    In_Meta_SrcMACAddress_nxt       : out std_logic;
    In_Meta_SrcMACAddress_Data      : in  T_SLV_8;
    In_Meta_DestMACAddress_nxt      : out std_logic;
    In_Meta_DestMACAddress_Data     : in  T_SLV_8;
    In_Meta_EthType                 : in  T_SLV_16;
    In_Meta_SrcIPAddress_nxt        : out std_logic;
    In_Meta_SrcIPAddress_Data       : in  T_SLV_8;
    In_Meta_DestIPAddress_nxt       : out std_logic;
    In_Meta_DestIPAddress_Data      : in  T_SLV_8;
--    In_Meta_TrafficClass            : in  T_SLV_8;
--    In_Meta_FlowLabel               : in  T_SLV_24;
    In_Meta_Length                  : in  T_SLV_16;
    In_Meta_Protocol                : in  T_SLV_8;
    -- OUT port
    Out_Valid                       : out std_logic;
    Out_Data                        : out T_SLV_8;
    Out_SOF                         : out std_logic;
    Out_EOF                         : out std_logic;
    Out_Ack                         : in  std_logic;
    Out_Meta_rst                    : in  std_logic;
    Out_Meta_SrcMACAddress_nxt      : in  std_logic;
    Out_Meta_SrcMACAddress_Data     : out T_SLV_8;
    Out_Meta_DestMACAddress_nxt     : in  std_logic;
    Out_Meta_DestMACAddress_Data    : out T_SLV_8;
    Out_Meta_EthType                : out T_SLV_16;
    Out_Meta_SrcIPAddress_nxt       : in  std_logic;
    Out_Meta_SrcIPAddress_Data      : out T_SLV_8;
    Out_Meta_DestIPAddress_nxt      : in  std_logic;
    Out_Meta_DestIPAddress_Data     : out T_SLV_8;
--    Out_Meta_TrafficClass           : out T_SLV_8;
--    Out_Meta_FlowLabel              : out T_SLV_24;
    Out_Meta_Length                 : out T_SLV_16;
    Out_Meta_Protocol               : out T_SLV_8;
    Out_Meta_SrcPort                : out T_SLV_16;
    Out_Meta_DestPort               : out T_SLV_16
  );
end entity;
```

Source file: net/udp/udp_RX.vhdl

PoC.net.udp.TX

Todo: No documentation available.

Entity Declaration:

```
entity udp_TX is
  generic (
    DEBUG                       : boolean           := FALSE;
    IP_VERSION                  : positive          := 6
  );
  port (
```

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```
    Clock                         : in  std_logic;                    --
    Reset                         : in  std_logic;                    --
    -- IN port
    In_Valid                      : in  std_logic;
    In_Data                       : in  T_SLV_8;
    In_SOF                        : in  std_logic;
    In_EOF                        : in  std_logic;
    In_Ack                        : out std_logic;
    In_Meta_rst                   : out std_logic;
    In_Meta_SrcIPAddress_nxt      : out std_logic;
    In_Meta_SrcIPAddress_Data     : in  T_SLV_8;
    In_Meta_DestIPAddress_nxt     : out std_logic;
    In_Meta_DestIPAddress_Data    : in  T_SLV_8;
    In_Meta_SrcPort               : in  T_SLV_16;
    In_Meta_DestPort              : in  T_SLV_16;
    In_Meta_Length                : in  T_SLV_16;
    In_Meta_Checksum              : in  T_SLV_16;
    -- OUT port
    Out_Valid                     : out std_logic;
    Out_Data                      : out T_SLV_8;
    Out_SOF                       : out std_logic;
    Out_EOF                       : out std_logic;
    Out_Ack                       : in  std_logic;
    Out_Meta_rst                  : in  std_logic;
    Out_Meta_SrcIPAddress_nxt     : in  std_logic;
    Out_Meta_SrcIPAddress_Data    : out T_SLV_8;
    Out_Meta_DestIPAddress_nxt    : in  std_logic;
    Out_Meta_DestIPAddress_Data   : out T_SLV_8;
    Out_Meta_Length               : out T_SLV_16
  );
end entity;
```

Source file: net/udp/udp_TX.vhdl

PoC.net.udp.FrameLoopback

Todo: No documentation available.

Entity Declaration:

```
entity udp_FrameLoopback is
  generic (
    IP_VERSION                    : positive            := 6;
    MAX_FRAMES                    : positive            := 4
  );
  port (
    Clock                         : in  std_logic;
    Reset                         : in  std_logic;
    -- IN port
    In_Valid                      : in  std_logic;
    In_Data                       : in  T_SLV_8;
    In_SOF                        : in  std_logic;
    In_EOF                        : in  std_logic;
    In_Ack                        : out std_logic;
    In_Meta_rst                   : out std_logic;
    In_Meta_DestIPAddress_nxt     : out std_logic;
```

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```
    In_Meta_DestIPAddress_Data     : in  T_SLV_8;
    In_Meta_SrcIPAddress_nxt       : out std_logic;
    In_Meta_SrcIPAddress_Data      : in  T_SLV_8;
    In_Meta_DestPort               : in  T_NET_UDP_PORT;
    In_Meta_SrcPort                : in  T_NET_UDP_PORT;
    -- OUT port
    Out_Valid                      : out std_logic;
    Out_Data                       : out T_SLV_8;
    Out_SOF                        : out std_logic;
    Out_EOF                        : out std_logic;
    Out_Ack                        : in  std_logic;
    Out_Meta_rst                   : in  std_logic;
    Out_Meta_DestIPAddress_nxt     : in  std_logic;
    Out_Meta_DestIPAddress_Data    : out T_SLV_8;
    Out_Meta_SrcIPAddress_nxt      : in  std_logic;
    Out_Meta_SrcIPAddress_Data     : out T_SLV_8;
    Out_Meta_DestPort              : out T_NET_UDP_PORT;
    Out_Meta_SrcPort               : out T_NET_UDP_PORT
  );
end entity;
```

Source file: net/udp/udp_FrameLoopback.vhdl

PoC.net.udp.Wrapper

Todo: No documentation available.

Entity Declaration:

```
entity udp_Wrapper is
  generic (
    DEBUG                           : boolean                     := FALSE;
    IP_VERSION                      : positive                    := 6;
    PORTPAIRS                       : T_NET_UDP_PORTPAIR_VECTOR   := (0 => (x
↪"0000", x"0000"))
  );
  port (
    Clock                           : in  std_logic;
    Reset                           : in  std_logic;
    -- from IP layer
    IP_TX_Valid                     : out std_logic;
    IP_TX_Data                      : out T_SLV_8;
    IP_TX_SOF                       : out std_logic;
    IP_TX_EOF                       : out std_logic;
    IP_TX_Ack                       : in  std_logic;
    IP_TX_Meta_rst                  : in  std_logic;
    IP_TX_Meta_SrcIPAddress_nxt     : in  std_logic;
    IP_TX_Meta_SrcIPAddress_Data    : out T_SLV_8;
    IP_TX_Meta_DestIPAddress_nxt    : in  std_logic;
    IP_TX_Meta_DestIPAddress_Data   : out T_SLV_8;
    IP_TX_Meta_Length               : out T_SLV_16;
    -- to IP layer
    IP_RX_Valid                     : in  std_logic;
    IP_RX_Data                      : in  T_SLV_8;
    IP_RX_SOF                       : in  std_logic;
    IP_RX_EOF                       : in  std_logic;
```

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```
    IP_RX_Ack                       : out std_logic;
    IP_RX_Meta_rst                  : out std_logic;
    IP_RX_Meta_SrcMACAddress_nxt    : out std_logic;
    IP_RX_Meta_SrcMACAddress_Data   : in  T_SLV_8;
    IP_RX_Meta_DestMACAddress_nxt   : out std_logic;
    IP_RX_Meta_DestMACAddress_Data  : in  T_SLV_8;
    IP_RX_Meta_EthType              : in  T_SLV_16;
    IP_RX_Meta_SrcIPAddress_nxt     : out std_logic;
    IP_RX_Meta_SrcIPAddress_Data    : in  T_SLV_8;
    IP_RX_Meta_DestIPAddress_nxt    : out std_logic;
    IP_RX_Meta_DestIPAddress_Data   : in  T_SLV_8;
--    IP_RX_Meta_TrafficClass         : in  T_SLV_8;
--    IP_RX_Meta_FlowLabel            : in  T_SLV_24;
    IP_RX_Meta_Length               : in  T_SLV_16;
    IP_RX_Meta_Protocol             : in  T_SLV_8;
    -- from upper layer
    TX_Valid                        : in  std_logic_vector(PORTPAIRS'length - 1
↪downto 0);
    TX_Data                         : in  T_SLVV_8(PORTPAIRS'length - 1 downto
↪0);
    TX_SOF                          : in  std_logic_vector(PORTPAIRS'length - 1
↪downto 0);
    TX_EOF                          : in  std_logic_vector(PORTPAIRS'length - 1
↪downto 0);
    TX_Ack                          : out std_logic_vector(PORTPAIRS'length - 1
↪downto 0);
    TX_Meta_rst                     : out std_logic_vector(PORTPAIRS'length - 1
↪downto 0);
    TX_Meta_SrcIPAddress_nxt        : out std_logic_vector(PORTPAIRS'length - 1
↪downto 0);
    TX_Meta_SrcIPAddress_Data       : in  T_SLVV_8(PORTPAIRS'length - 1 downto
↪0);
    TX_Meta_DestIPAddress_nxt       : out std_logic_vector(PORTPAIRS'length - 1
↪downto 0);
    TX_Meta_DestIPAddress_Data      : in  T_SLVV_8(PORTPAIRS'length - 1 downto
↪0);
    TX_Meta_SrcPort                 : in  T_SLVV_16(PORTPAIRS'length - 1 downto
↪0);
    TX_Meta_DestPort                : in  T_SLVV_16(PORTPAIRS'length - 1 downto
↪0);
    TX_Meta_Length                  : in  T_SLVV_16(PORTPAIRS'length - 1 downto
↪0);
    -- to upper layer
    RX_Valid                        : out std_logic_vector(PORTPAIRS'length - 1
↪downto 0);
    RX_Data                         : out T_SLVV_8(PORTPAIRS'length - 1 downto
↪0);
    RX_SOF                          : out std_logic_vector(PORTPAIRS'length - 1
↪downto 0);
    RX_EOF                          : out std_logic_vector(PORTPAIRS'length - 1
↪downto 0);
    RX_Ack                          : in  std_logic_vector(PORTPAIRS'length - 1
↪downto 0);
    RX_Meta_rst                     : in  std_logic_vector(PORTPAIRS'length - 1
↪downto 0);
    RX_Meta_SrcMACAddress_nxt       : in  std_logic_vector(PORTPAIRS'length - 1
↪downto 0);
    RX_Meta_SrcMACAddress_Data      : out T_SLVV_8(PORTPAIRS'length - 1 downto
↪0);
    RX_Meta_DestMACAddress_nxt      : in  std_logic_vector(PORTPAIRS'length - 1
↪downto 0);
```

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```
    RX_Meta_DestMACAddress_Data       : out T_SLVV_8(PORTPAIRS'length - 1 downto 0);
    RX_Meta_EthType                   : out T_SLVV_16(PORTPAIRS'length - 1 downto 0);
    RX_Meta_SrcIPAddress_nxt          : in  std_logic_vector(PORTPAIRS'length - 1 downto 0);
    RX_Meta_SrcIPAddress_Data         : out T_SLVV_8(PORTPAIRS'length - 1 downto 0);
    RX_Meta_DestIPAddress_nxt         : in  std_logic_vector(PORTPAIRS'length - 1 downto 0);
    RX_Meta_DestIPAddress_Data        : out T_SLVV_8(PORTPAIRS'length - 1 downto 0);
--    RX_Meta_TrafficClass              : out T_SLVV_8(PORTPAIRS'length - 1 downto 0);
--    RX_Meta_FlowLabel                 : out T_SLVV_24(PORTPAIRS'length - 1 downto 0);
    RX_Meta_Length                    : out T_SLVV_16(PORTPAIRS'length - 1 downto 0);
    RX_Meta_Protocol                  : out T_SLVV_8(PORTPAIRS'length - 1 downto 0);
    RX_Meta_SrcPort                   : out T_SLVV_16(PORTPAIRS'length - 1 downto 0);
    RX_Meta_DestPort                  : out T_SLVV_16(PORTPAIRS'length - 1 downto 0)
  );
end entity;
```

Source file: net/udp/udp_Wrapper.vhdl

7.13.11 PoC.net Package

Source file: net.pkg.vhdl

7.13.12 PoC.net.FrameChecksum

Todo: No documentation available.

Entity Declaration:

```
entity net_FrameChecksum is
  generic (
    MAX_FRAMES                    : positive        := 8;
    MAX_FRAME_LENGTH              : positive        := 2048;
    META_BITS                     : T_POSVEC        := (0 => 8);
    META_FIFO_DEPTH               : T_POSVEC        := (0 => 16)
  );
  port (
    Clock                         : in  std_logic;
    Reset                         : in  std_logic;
    -- IN port
    In_Valid                      : in  std_logic;
    In_Data                       : in  T_SLV_8;
    In_SOF                        : in  std_logic;
    In_EOF                        : in  std_logic;
    In_Ack                        : out std_logic;
```

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```
    In_Meta_rst                     : out std_logic;
    In_Meta_nxt                     : out std_logic_vector(META_BITS'length - 1
↪downto 0);
    In_Meta_Data                    : in  std_logic_vector(isum(META_BITS) - 1
↪downto 0);
    -- OUT port
    Out_Valid                       : out std_logic;
    Out_Data                        : out T_SLV_8;
    Out_SOF                         : out std_logic;
    Out_EOF                         : out std_logic;
    Out_Ack                         : in  std_logic;
    Out_Meta_rst                    : in  std_logic;
    Out_Meta_nxt                    : in  std_logic_vector(META_BITS'length - 1
↪downto 0);
    Out_Meta_Data                   : out std_logic_vector(isum(META_BITS) - 1
↪downto 0);
    Out_Meta_Length                 : out T_SLV_16;
    Out_Meta_Checksum               : out T_SLV_16
  );
end entity;
```

Source file: net/net_FrameChecksum.vhdl

7.13.13 PoC.net.FrameLoopback

Todo: No documentation available.

Entity Declaration:

```
entity FrameLoopback is
  generic (
    DATA_BW                     : positive        := 8;
    META_BW                     : natural         := 0
  );
  port (
    Clock                       : in  std_logic;
    Reset                       : in  std_logic;

    In_Valid                    : in  std_logic;
    In_Data                     : in  std_logic_vector(DATA_BW - 1 downto 0);
    In_Meta                     : in  std_logic_vector(META_BW - 1 downto 0);
    In_SOF                      : in  std_logic;
    In_EOF                      : in  std_logic;
    In_Ack                      : out std_logic;


    Out_Valid                   : out std_logic;
    Out_Data                    : out std_logic_vector(DATA_BW - 1 downto 0);
    Out_Meta                    : out std_logic_vector(META_BW - 1 downto 0);
    Out_SOF                     : out std_logic;
    Out_EOF                     : out std_logic;
    Out_Ack                     : in  std_logic
  );
end entity;
```

Source file: net/net_FrameLoopback.vhdl

7.14 PoC.sort

These are sorting entities. . . .

Sub-Namespaces

- *PoC.sort.sortnet*

Entities

- IP:sort_ExpireList
- IP:sort_InsertSort
- *PoC.sort.LeastFrequentlyUsed*
- *PoC.sort.lru_cache*
- *PoC.sort.lru_list*

7.14.1 PoC.sort.sortnet

This sub-namespace contains sorting network implementations.

Entities

- *PoC.sort.sortnet.BitonicSort*
- *PoC.sort.sortnet.MergeSort_Streamed*
- *PoC.sort.sortnet.OddEvenMergeSort*
- *PoC.sort.sortnet.OddEvenSort*
- *PoC.sort.sortnet.Stream_Adapter*
- *PoC.sort.sortnet.Stream_Adapter2*
- *PoC.sort.sortnet.Transform*

PoC.sort.sortnet Package

```
type T_SORTNET_IMPL is (
  SORT_SORTNET_IMPL_ODDEVEN_SORT,
  SORT_SORTNET_IMPL_ODDEVEN_MERGESORT,
  SORT_SORTNET_IMPL_BITONIC_SORT
);
```

T_SORTNET_IMPL

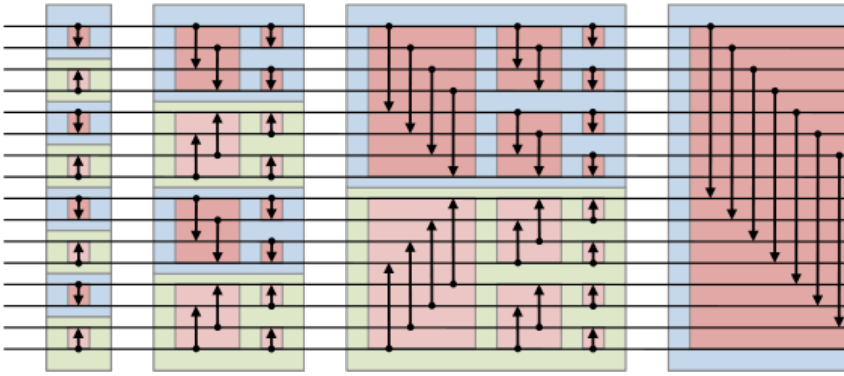
SORT_SORTNET_IMPL_ODDEVEN_SORT Instantiate a *PoC.sort.sortnet.OddEvenSort* sorting network.

SORT_SORTNET_IMPL_ODDEVEN_MERGESORT Instantiate a *PoC.sort.sortnet.OddEvenMergeSort* sorting network.

SORT_SORTNET_IMPL_BITONIC_SORT Instantiate a *PoC.sort.sortnet.BitonicSort* sorting network.

Source file: sortnet.pkg.vhdl

PoC.sort.sortnet.BitonicSort



This sorting network uses the *bitonic sort* algorithm.

Entity Declaration:

```
entity sortnet_BitonicSort is
  generic (
    INPUTS                : positive  := 32;       -- input count
    KEY_BITS              : positive  := 32;       -- the first KEY_BITS of In_Data
↪are used as a sorting critera (key)
    DATA_BITS             : positive  := 64;       -- inclusive KEY_BITS
    META_BITS             : natural   := 2;        -- additional bits, not sorted
↪but delayed as long as In_Data
    PIPELINE_STAGE_AFTER  : natural   := 2;        -- add a pipline stage after n
↪sorting stages
    ADD_INPUT_REGISTERS   : boolean   := FALSE;    --
    ADD_OUTPUT_REGISTERS  : boolean   := TRUE      --
  );
  port (
    Clock       : in  std_logic;
    Reset       : in  std_logic;

    Inverse     : in  std_logic   := '0';

    In_Valid    : in  std_logic;
    In_IsKey    : in  std_logic;
    In_Data     : in  T_SLM(INPUTS - 1 downto 0, DATA_BITS - 1 downto 0);
    In_Meta     : in  std_logic_vector(META_BITS - 1 downto 0);

    Out_Valid   : out std_logic;
    Out_IsKey   : out std_logic;
    Out_Data    : out T_SLM(INPUTS - 1 downto 0, DATA_BITS - 1 downto 0);
    Out_Meta    : out std_logic_vector(META_BITS - 1 downto 0)
  );
end entity;
```

Source file: sort/sortnet/sortnet_BitonicSort.vhdl

PoC.sort.sortnet.MergeSort_Streamed

Todo: No documentation available.

Entity Declaration:

```
entity sortnet_MergeSort_Streamed is
  generic (
    FIFO_DEPTH   : positive    := 32;
    KEY_BITS     : positive    := 32;
    DATA_BITS    : positive    := 32
  );
  port (
    Clock      : in  std_logic;
    Reset      : in  std_logic;

    Inverse    : in  std_logic     := '0';

    In_Valid   : in  std_logic;
    In_Data    : in  std_logic_vector(DATA_BITS - 1 downto 0);
    In_SOF     : in  std_logic;
    In_IsKey   : in  std_logic;
    In_EOF     : in  std_logic;
    In_Ack     : out std_logic;

    Out_Sync   : out std_logic;
    Out_Valid  : out std_logic;
    Out_Data   : out std_logic_vector(DATA_BITS - 1 downto 0);
    Out_SOF    : out std_logic;
    Out_IsKey  : out std_logic;
    Out_EOF    : out std_logic;
    Out_Ack    : in  std_logic
  );
end entity;
```

Source file: sort/sortnet/sortnet_MergeSort_Streamed.vhdl

PoC.sort.sortnet.OddEvenMergeSort

Todo: No documentation available.

Entity Declaration:

```
entity sortnet_OddEvenMergeSort is
  generic (
    INPUTS                : positive  := 128;    -- input count
    KEY_BITS              : positive  := 32;     -- the first KEY_BITS of In_Data
↪are used as a sorting critera (key)
    DATA_BITS             : positive  := 32;     -- inclusive KEY_BITS
    META_BITS             : natural   := 2;      -- additional bits, not sorted but
↪delayed as long as In_Data
    PIPELINE_STAGE_AFTER  : natural   := 2;      -- add a pipline stage after n
↪sorting stages
    ADD_INPUT_REGISTERS   : boolean   := FALSE; --
    ADD_OUTPUT_REGISTERS  : boolean   := TRUE   --
  );
  port (
    Clock       : in  std_logic;
    Reset       : in  std_logic;

    Inverse     : in  std_logic   := '0';
```

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```
16
17      In_Valid     : in  std_logic;
18      In_IsKey     : in  std_logic;
19      In_Data      : in  T_SLM(INPUTS - 1 downto 0, DATA_BITS - 1 downto 0);
20      In_Meta      : in  std_logic_vector(META_BITS - 1 downto 0);
21
22      Out_Valid    : out std_logic;
23      Out_IsKey    : out std_logic;
24      Out_Data     : out T_SLM(INPUTS - 1 downto 0, DATA_BITS - 1 downto 0);
25      Out_Meta     : out std_logic_vector(META_BITS - 1 downto 0)
26    );
27  end entity;
```

Source file: sort/sortnet/sortnet_OddEvenMergeSort.vhdl

PoC.sort.sortnet.OddEvenSort

Todo: No documentation available.

Entity Declaration:

```
1   entity sortnet_OddEvenSort is
2     generic (
3       INPUTS                : positive  := 8;      -- input count
4       KEY_BITS              : positive  := 32;     -- the first KEY_BITS of In_Data␣
    ↪are used as a sorting critera (key)
5       DATA_BITS             : positive  := 32;     -- inclusive KEY_BITS
6       META_BITS             : natural   := 2;      -- additional bits, not sorted but␣
    ↪delayed as long as In_Data
7       PIPELINE_STAGE_AFTER  : natural   := 2;      -- add a pipline stage after n␣
    ↪sorting stages
8       ADD_INPUT_REGISTERS   : boolean   := FALSE; --
9       ADD_OUTPUT_REGISTERS  : boolean   := TRUE   --
10    );
11    port (
12      Clock        : in  std_logic;
13      Reset        : in  std_logic;
14
15      Inverse      : in  std_logic   := '0';
16
17      In_Valid     : in  std_logic;
18      In_IsKey     : in  std_logic;
19      In_Data      : in  T_SLM(INPUTS - 1 downto 0, DATA_BITS - 1 downto 0);
20      In_Meta      : in  std_logic_vector(META_BITS - 1 downto 0);
21
22      Out_Valid    : out std_logic;
23      Out_IsKey    : out std_logic;
24      Out_Data     : out T_SLM(INPUTS - 1 downto 0, DATA_BITS - 1 downto 0);
25      Out_Meta     : out std_logic_vector(META_BITS - 1 downto 0)
26    );
27  end entity;
```

Source file: sort/sortnet/sortnet_OddEvenSort.vhdl

PoC.sort.sortnet.Stream_Adapter

Todo: No documentation available.

Entity Declaration:

```
entity sortnet_Stream_Adapter is
  generic (
    STREAM_DATA_BITS      : positive        := 32;
    STREAM_META_BITS      : positive        := 2;
    SORTNET_IMPL          : T_SORTNET_IMPL  := SORT_SORTNET_IMPL_ODDEVEN_MERGESORT;
    SORTNET_SIZE          : positive        := 32;
    SORTNET_KEY_BITS      : positive        := 32;
    SORTNET_DATA_BITS     : natural         := 32;
    INVERSE               : boolean         := FALSE
  );
  port (
    Clock       : in  std_logic;
    Reset       : in  std_logic;

    In_Valid    : in  std_logic;
    In_IsKey    : in  std_logic;
    In_Data     : in  std_logic_vector(STREAM_DATA_BITS - 1 downto 0);
    In_Meta     : in  std_logic_vector(STREAM_META_BITS - 1 downto 0);
    In_Ack      : out std_logic;

    Out_Valid   : out std_logic;
    Out_IsKey   : out std_logic;
    Out_Data    : out std_logic_vector(STREAM_DATA_BITS - 1 downto 0);
    Out_Meta    : out std_logic_vector(STREAM_META_BITS - 1 downto 0);
    Out_Ack     : in  std_logic
  );
end entity;
```

Source file: sort/sortnet/sortnet_Stream_Adapter.vhdl

PoC.sort.sortnet.Stream_Adapter2

Todo: No documentation available.

Entity Declaration:

```
entity sortnet_Stream_Adapter2 is
  generic (
    STREAM_DATA_BITS      : positive        := 32;
    STREAM_META_BITS      : positive        := 2;
    DATA_COLUMNS          : positive        := 2;
    SORTNET_IMPL          : T_SORTNET_IMPL  := SORT_SORTNET_IMPL_ODDEVEN_MERGESORT;
    SORTNET_SIZE          : positive        := 32;
    SORTNET_KEY_BITS      : positive        := 32;
    SORTNET_DATA_BITS     : natural         := 32;
    SORTNET_REG_AFTER     : natural         := 2;
    MERGENET_STAGES       : positive        := 2
  );
  port (
```

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```
    Clock       : in  std_logic;
    Reset       : in  std_logic;

    Inverse     : in  std_logic       := '0';

    In_Valid    : in  std_logic;
    In_Data     : in  std_logic_vector(STREAM_DATA_BITS - 1 downto 0);
    In_Meta     : in  std_logic_vector(STREAM_META_BITS - 1 downto 0);
    In_SOF      : in  std_logic;
    In_IsKey    : in  std_logic;
    In_EOF      : in  std_logic;
    In_Ack      : out std_logic;

    Out_Valid   : out std_logic;
    Out_Data    : out std_logic_vector(STREAM_DATA_BITS - 1 downto 0);
    Out_Meta    : out std_logic_vector(STREAM_META_BITS - 1 downto 0);
    Out_SOF     : out std_logic;
    Out_IsKey   : out std_logic;
    Out_EOF     : out std_logic;
    Out_Ack     : in  std_logic
  );
end entity;
```

Source file: sort/sortnet/sortnet_Stream_Adapter2.vhdl

PoC.sort.sortnet.Transform

Todo: No documentation available.

Entity Declaration:

```
entity sortnet_Transform is
  generic (
    ROWS        : positive    := 16;
    COLUMNS     : positive    := 4;
    DATA_BITS   : positive    := 8
  );
  port (
    Clock     : in  std_logic;
    Reset     : in  std_logic;

    In_Valid  : in  std_logic;
    In_Data   : in  T_SLM(ROWS - 1 downto 0, DATA_BITS - 1 downto 0);
    In_SOF    : in  std_logic;
    In_EOF    : in  std_logic;

    Out_Valid : out std_logic;
    Out_Data  : out T_SLM(COLUMNS - 1 downto 0, DATA_BITS - 1 downto 0);
    Out_SOF   : out std_logic;
    Out_EOF   : out std_logic
  );
end entity;
```

Source file: sort/sortnet/sortnet_Transform.vhdl

7.14.2 PoC.sort.ExpireList

Todo: No documentation available.

Entity Declaration:

Source file: sort/sort_ExpireList.vhdl

7.14.3 PoC.sort.InsertSort

Todo: No documentation available.

Entity Declaration:

Source file: sort/sort_InsertSort.vhdl

7.14.4 PoC.sort.LeastFrequentlyUsed

Todo: No documentation available.

Entity Declaration:

Source file: sort/sort_LeastFrequentlyUsed.vhdl

7.14.5 PoC.sort.lru_cache

This is an optimized implementation of `sort_lru_list` to be used for caches. Only keys are stored within this list, and these keys are the index of the cache lines. The list initially contains all indizes from 0 to ELEMENTS-1. The least-recently used index `KeyOut` is always valid.

The first outputed least-recently used index will be ELEMENTS-1.

The inputs `Insert`, `Free`, `KeyIn`, and `Reset` are synchronous to the rising-edge of the clock `clock`. All control signals are high-active.

Supported operations:

- **Insert:** Mark index `KeyIn` as recently used, e.g., when a cache-line was accessed.
- **Free:** Mark index `KeyIn` as least-recently used. Apply this operation, when a cache-line gets invalidated.

Entity Declaration:

```
entity sort_lru_cache is
  generic (
    ELEMENTS        : positive          := 32
  );
  port (
    Clock    : in std_logic;
    Reset    : in std_logic;

    Insert   : in  std_logic;
    Free     : in  std_logic;
    KeyIn    : in  std_logic_vector(log2ceilnz(ELEMENTS) - 1 downto 0);

    KeyOut   : out std_logic_vector(log2ceilnz(ELEMENTS) - 1 downto 0)
  );
end entity;
```

Source file: sort/sort_lru_cache.vhdl

7.14.6 PoC.sort.lru_list

List storing `(key, value)` pairs. The least-recently inserted pair is outputed on `DataOut` if `Valid = '1'`. If `Valid = '0'`, then the list empty.

The inputs `Insert`, `Remove`, `DataIn`, and `Reset` are synchronous to the rising-edge of the clock `clock`. All control signals are high-active.

Supported operations:

- **Insert:** Insert `DataIn` as recently used `(key, value)` pair. If key is already within the list, then the corresponding value is updated and the pair is moved to the recently used position.
- **Remove:** Remove `(key, value)` pair with the given key. The list is not modified if key is not within the list.

Entity Declaration:

```
entity sort_lru_list is
  generic (
    ELEMENTS                : positive                      := 16;
    KEY_BITS                : positive                      := 4;
    DATA_BITS               : positive                      := 8;
    INITIAL_ELEMENTS        : T_SLM                         := (0 to 15 => (0␣
↪to 7 => '0'));
    INITIAL_VALIDS          : std_logic_vector              := (0 to 15 => '0')
  );
  port (
    Clock                   : in  std_logic;
    Reset                   : in  std_logic;

    Insert                  : in  std_logic;
    Remove                  : in  std_logic;
    DataIn                  : in  std_logic_vector(DATA_BITS - 1 downto 0);

    Valid                   : out std_logic;
    DataOut                 : out std_logic_vector(DATA_BITS - 1 downto 0)
  );
end entity;
```

Source file: sort/sort_lru_list.vhdl

7.15 PoC.xil

This namespace is for Xilinx specific modules.

Sub-Namespaces

- *PoC.xil.mig*
- *PoC.xil.reconfig*

Entities

- *PoC.xil.BSCAN*
- *PoC.xil.ChipScopeICON*
- *PoC.xil.DRP_BusMux*
- *PoC.xil.DRP_BusSync*
- *PoC.xil.ICAP*
- *PoC.xil.Reconfigurator*
- *PoC.xil.SystemMonitor*
- IP:xil_SystemMonitor_Virtex6
- IP:xil_SystemMonitor_Series7

7.15.1 PoC.xil.mig

The namespace `PoC.xil.mig` offers pre-configured memory controllers generated with Xilinx's Memory Interface Generator (MIG).

- **for Spartan-6 boards:**
  - *mig_Atlys_1x128* - A DDR2 memory controller for the Digilent Atlys board.
- **for Kintex-7 boards:**
  - *mig_KC705_MT8JTF12864HZ_1G6* - A DDR3 memory controller for the Xilinx KC705 board.
- **for Virtex-7 boards:**

mig_Atlys_1x128

This DDR2 memory controller is pre-configured for the Digilent Atlys development board. The board is equipped with a single 1 GiBit DDR2 memory chip (128 MiByte) from MIRA (MIRA P3R1GE3EGF G8E DDR2).

Run the following two steps to create the IP core:

1. Generate the source files from the IP core using Xilinx MIG and afterwards patch them `PS> .\poc.ps1 coregen PoC.xil.mig.Atlys_1x128 --board=Atlys`
2. Compile the patched sources into a ready to use netlist (*.ngc) and constraint file (*.ucf) `PS> .\poc.ps1 xst PoC.xil.mig.Atlys_1x128 --board=Atlys`

See also:

Using PoC -> Synthesis For how to run Core Generator and XST from PoC.

mig_KC705_MT8JTF12864HZ_1G6

This DDR2 memory controller is pre-configured for the Xilinx KC705 development board. The board is equipped with a single 1 GiBit DDR3 memory chip (128 MiByte) from Micron Technology (MT8JTF12864HZ-1G6G1).

Run the following two steps to create the IP core:

1. Generate the source files from the IP core using Xilinx MIG and afterwards patch them `PS> .\poc.ps1 coregen PoC.xil.mig.KC705_MT8JTF12864HZ_1G6 --board=KC705`
2. Compile the patched sources into a ready to use netlist (*.ngc) and constraint file (*.ucf) `PS> .\poc.ps1 xst PoC.xil.mig.KC705_MT8JTF12864HZ_1G6 --board=KC705`

See also:

Using PoC -> Synthesis For how to run Core Generator and XST from PoC.

7.15.2 PoC.xil.reconfig

These are reconfig entities. . . .

Entities

- *PoC.xil.reconfig.icap_fsm*
- *PoC.xil.reconfig.icap_wrapper*

PoC.xil.reconfig.icap_fsm

This module parses the data stream to the Xilinx "Internal Configuration Access Port" (ICAP) primitives to generate control signals. Tested on:

- Virtex-6
- Virtex-7

Entity Declaration:

```
entity reconfig_icap_fsm is
  port  (
    clk       : in  std_logic;
    reset     : in  std_logic;            -- high-active reset
    -- interface to connect to the icap
    icap_in     : out std_logic_vector(31 downto 0);  -- data that will go into␣
↪the icap
    icap_out    : in  std_logic_vector(31 downto 0);  -- data from the icap
    icap_csb    : out std_logic;
    icap_rw     : out std_logic;

    -- data interface, no internal fifos
    in_data     : in  std_logic_vector(31 downto 0);  -- new configuration data
    in_data_valid : in  std_logic;            -- input data is valid
    in_data_rden  : out std_logic;            -- possible to send data
    out_data    : out std_logic_vector(31 downto 0);  -- data read from the fifo
    out_data_valid  : out std_logic;            -- data from icap is valid
    out_data_full : in  std_logic;            -- receiving buffer is full, halt␣
↪icap

    -- control structures
    status      : out std_logic_vector(31 downto 0) -- status vector
  );
end reconfig_icap_fsm;
```

Source file: xil/reconfig/reconfig_icap_fsm.vhdl

PoC.xil.reconfig.icap_wrapper

This module was designed to connect the Xilinx "Internal Configuration Access Port" (ICAP) to a PCIe endpoint on a Dini board. Tested on:

tbd

Entity Declaration:

```
entity reconfig_icap_wrapper is
  generic (
    MIN_DEPTH_OUT     : positive := 256;
    MIN_DEPTH_IN      : positive := 256
  );
  port (
    clk       : in  std_logic;
    reset     : in  std_logic;
    clk_icap    : in  std_logic;    -- clock signal for ICAP, max 100 MHz (double␣
↪check with manual)

    icap_busy   : out std_logic;    -- the ICAP is processing the data
    icap_readback : out std_logic;    -- high during a readback
    icap_partial_res: out std_logic;    -- high during reconfiguration

    -- data in
    write_put   : in  std_logic;
    write_full    : out std_logic;
    write_data    : in  std_logic_vector(31 downto 0);
    write_done    : in  std_logic;    -- high pulse/edge after all data was written

    -- data out
    read_got    : in  std_logic;
    read_valid    : out std_logic;
    read_data     : out std_logic_vector(31 downto 0)
  );
end reconfig_icap_wrapper;
```

Source file: xil/reconfig/reconfig_icap_wrapper.vhdl

7.15.3 PoC.xil Package

This package holds all component declarations for this namespace.

Source file: xil.pkg.vhdl

7.15.4 PoC.xil.BSCAN

This module wraps Xilinx "Boundary Scan" (JTAG) primitives in a generic module. Supported devices are:

- Spartan-3, Spartan-6
- Virtex-5, Virtex-6
- Series-7 (Artix-7, Kintex-7, Virtex-7, Zynq-7000)

Entity Declaration:

```
entity xil_BSCAN is
  generic (
    JTAG_CHAIN          : natural;
    DISABLE_JTAG        : boolean     := FALSE
  );
  port (
    Reset               : out std_logic;
    RunTest             : out std_logic;
    Sel                 : out std_logic;
    Capture             : out std_logic;
    drck                : out std_logic;
    Shift               : out std_logic;
    Test_Clock          : out std_logic;
    Test_DataIn         : out std_logic;
    Test_DataOut        : in  std_logic;
    Test_ModeSelect     : out std_logic;
    Update              : out std_logic
  );
end entity;
```

Source file: xil/xil_BSCAN.vhdl

7.15.5 PoC.xil.ChipScopeICON

This module wraps 15 ChipScope ICON IP core netlists generated from ChipScope ICON xco files. The generic parameter `PORTS` selects the apropriate ICON instance with 1 to 15 ICON `ControlBus` ports. Each `ControlBus` port is of type `T_XIL_CHIPSCOPE_CONTROL` and of mode `inout`.

Compile required CoreGenerator IP Cores to Netlists with PoC

Please use the provided Xilinx ISE compile command `ise` in PoC to recreate the needed source and netlist files on your local machine.

```
cd PoCRoot
.\poc.ps1 ise PoC.xil.ChipScopeICON --board=KC705
```

Entity Declaration:

```
entity xil_ChipScopeICON is
  generic (
    PORTS       : positive
  );
  port (
    ControlBus  : inout T_XIL_CHIPSCOPE_CONTROL_VECTOR(PORTS - 1 downto 0)
  );
end entity;
```

See also:

Using PoC -> Synthesis For how to run synthesis with PoC and CoreGenerator.

Source file: xil/xil_ChipScopeICON.vhdl

7.15.6 PoC.xil.DRP_BusMux

Todo: No documentation available.

Entity Declaration:

Source file: xil/xil_DRP_BusMux.vhdl

7.15.7 PoC.xil.DRP_BusSync

Todo: No documentation available.

Entity Declaration:

Source file: xil/xil_DRP_BusSync.vhdl

7.15.8 PoC.xil.ICAP

This module wraps Xilinx "Internal Configuration Access Port" (ICAP) primitives in a generic module. Supported devices are:

- Spartan-6
- Virtex-4, Virtex-5, Virtex-6
- Series-7 (Artix-7, Kintex-7, Virtex-7, Zynq-7000)

Entity Declaration:

```
entity xil_ICAP is
  generic (
    ICAP_WIDTH  : string := "X32";          -- Specifies the input and output data width to be used
                                -- Spartan 6: fixed to 16 bit
                                -- Virtex 4:  X8 or X32
                                -- Rest: X8, X16, X32
    DEVICE_ID : bit_vector := X"1234567";       -- pre-programmed Device ID value for simulation
                                -- supported by Spartan 6, Virtex 6 and above
    SIM_CFG_FILE_NAME : string  := "NONE"     -- Raw Bitstream (RBT) file to be parsed by the simulation model
                                -- supported by Spartan 6, Virtex 6 and above
  );
  port (
    clk     : in std_logic;           -- up to 100 MHz (Virtex-6 and above, Virtex-5??)
    disable   : in std_logic;           -- low active enable -> high active disable
    rd_wr   : in std_logic;           -- 0 - write, 1 - read
    busy    : out std_logic;            -- on Series-7 devices always '0'
    data_in   : in std_logic_vector(31 downto 0); -- on Spartan-6 only 15 downto 0
    data_out  : out std_logic_vector(31 downto 0) -- on Spartan-6 only 15 downto 0
```

(continues on next page)

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```
  );
end entity;
```

Source file: xil/xil_ICAP.vhdl

7.15.9 PoC.xil.Reconfigurator

Many complex primitives in a Xilinx device offer a Dynamic Reconfiguration Port (DRP) to reconfigure a primitive at runtime without reconfiguring the whole FPGA.

This module is a DRP master that can be pre-configured at compile time with different configuration sets. The configuration sets are mapped into a ROM. The user can select a stored configuration with `ConfigSelect`. Sending a strobe to `Reconfig` will start the reconfiguration process. The operation completes with another strobe on `ReconfigDone`.

Entity Declaration:

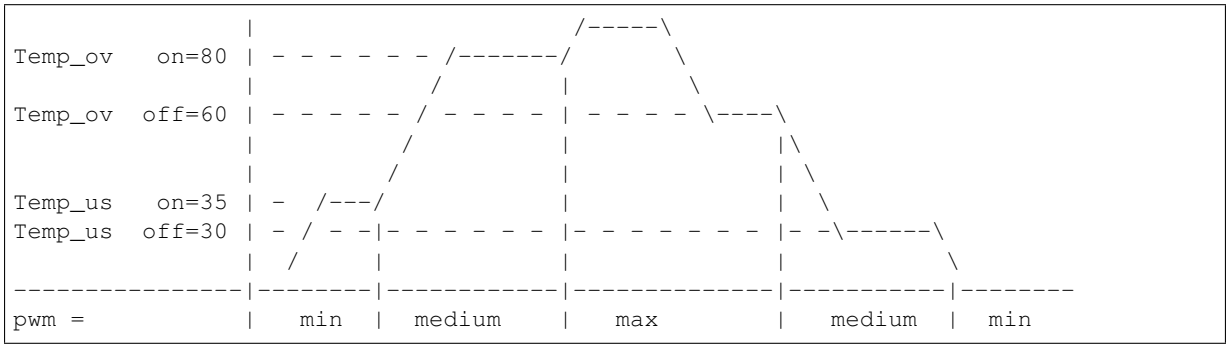
```
entity xil_Reconfigurator is
  generic (
    DEBUG            : boolean                    := FALSE;                  --
    CLOCK_FREQ       : FREQ                       := 100 MHz;                --
    CONFIG_ROM       : in  T_XIL_DRP_CONFIG_ROM   := (0 downto 0 => C_XIL_DRP_CONFIG_SET_EMPTY)   --
  );
  port (
    Clock            : in  std_logic;
    Reset            : in  std_logic;

    Reconfig         : in  std_logic;                                        --
    ReconfigDone     : out std_logic;                                        --
    ConfigSelect     : in  std_logic_vector(log2ceilnz(CONFIG_ROM'length) - 1 downto 0);          --

    DRP_en           : out std_logic;                                        --
    DRP_Address      : out T_XIL_DRP_ADDRESS;                                --
    DRP_we           : out std_logic;                                        --
    DRP_DataIn       : in  T_XIL_DRP_DATA;                                   --
    DRP_DataOut      : out T_XIL_DRP_DATA;                                   --
    DRP_Ack          : in  std_logic                                         --
  );
end entity;
```

Source file: xil/xil_Reconfigurator.vhdl

7.15.10 PoC.xil.SystemMonitor

This module wraps a SYSMON or XADC to report if preconfigured temperature values are overrun. The XADC was formerly known as “System Monitor”.

Temperature Curve



Entity Declaration:

```
entity xil_SystemMonitor is
  port (
    Reset               : in  std_logic;        -- Reset signal for the System Monitor control logic

    Alarm_UserTemp      : out std_logic;        -- Temperature-sensor alarm output
    Alarm_OverTemp      : out std_logic;        -- Over-Temperature alarm output
    Alarm               : out std_logic;        -- OR'ed output of all the Alarms
    VP                  : in  std_logic;        -- Dedicated Analog Input Pair
    VN                  : in  std_logic
  );
end entity;
```

Source file: xil/xil_SystemMonitor.vhdl

CHAPTER 8

Third Party Libraries

The PoC-Library is shiped with different third party libraries, which are located in the `<PoCRoot>/lib/` folder. This document lists all these libraries, their websites and licenses.

8.1 Cocotb

Cocotb is a coroutine based cosimulation library for writing VHDL and Verilog testbenches in Python.

Folder:	`<PoCRoot>\lib\cocotb\`
Copyright:	Copyright © 2013, Potential Ventures Ltd., SolarFlare Communications Inc.
License:	*Revised BSD License (local copy)*
Documentation:	http://cocotb.readthedocs.org/
Source:	https://github.com/potentialventures/cocotb

8.2 OSVVM

Open Source VHDL Verification Methodology (OS-VVM) is an intelligent testbench methodology that allows mixing of "Intelligent Coverage" (coverage driven randomization) with directed, algorithmic, file based, and constrained random test approaches. The methodology can be adopted in part or in whole as needed. With OSVVM you can add advanced verification methodologies to your current testbench without having to learn a new language or throw out your existing testbench or testbench models.

Folder:	`<PoCRoot>\lib\osvvm\`
Copyright:	Copyright © 2012-2016 by SynthWorks Design Inc.
License:	*Artistic License 2.0 (local copy)*
Website:	http://osvvm.org/
Source:	https://github.com/JimLewis/OSVVM

8.3 UVVM

The Open Source **UVVM (Universal VHDL Verification Methodology) - VVC (VHDL Verification Component) Framework** for making structured VHDL testbenches for verification of FPGA. UVVM consists currently of: Utility Library, VVC Framework and Verification IPs (VIP) for various protocols.

For what do I need this VVC Framework? The VVC Framework is a VHDL Verification Component system that allows multiple interfaces on a DUT to be stimulated/handled simultaneously in a very structured manner, and controlled by a very simple to understand software like a test sequencer. VVC Framework is unique as an open source VHDL approach to building a structured testbench architecture using Verification components and a simple protocol to access these. As an example a simple command like `uart_expect(UART_VVCT, my_data)`, or `axilite_write(AXILITE_VVCT, my_addr, my_data, my_message)` will automatically tell the respective VVC (for UART or AXI-Lite) to execute the `uart_receive()` or `axilite_write()` BFM respectively.

Folder:	`<PoCRoot>\lib\uvvm\`
Copyright:	Copyright © 2016 by Bitvis AS
License:	*The MIT License (local copy)*
Website:	http://bitvis.no/
Source:	https://github.com/UVVM/UVVM_All

8.4 VUnit

VUnit is an open source unit testing framework for VHDL released under the terms of *Mozilla Public License, v. 2.0*. It features the functionality needed to realize continuous and automated testing of your VHDL code. VUnit doesn't replace but rather complements traditional testing methodologies by supporting a "test early and often" approach through automation.

Folder:	`<PoCRoot>\lib\vunit\`
Copyright:	Copyright © 2014-2016, Lars Asplund lars.anders.asplund@gmail.com
License:	*Mozilla Public License, Version 2.0 (local copy)*
Website:	https://vunit.github.io/
Source:	https://github.com/VUnit/vunit

8.5 Updating Linked Git Submodules

The third party libraries are embedded as Git submodules. So if the PoC-Library was not cloned with option `--recursive` it's required to run the sub-module initialization manually:

8.5.1 On Linux

```
cd PoCRoot
git submodule init
git submodule update
```

We recommend to rename the default remote repository name from 'origin' to 'github'.

```
cd PoCRoot\lib\
```

Todo: write Bash code for Linux

8.5.2 On OS X

Please see the Linux instructions.

8.5.3 On Windows

```
cd PoCRoot
git submodule init
git submodule update
```

We recommend to rename the default remote repository name from ‘origin’ to ‘github’.

```
cd PoCRoot\lib\
foreach($dir in (dir -Directory)) {
  cd $dir
  git remote rename origin github
  cd ..
}
```

CHAPTER 9

Constraint Files

9.1 IP Core Constraint Files

- fifo
- misc
  - sync
- net
  - eth

9.1.1 fifo

- fifo_ic_got

fifo_ic_got

9.1.2 misc

- sync

sync

- sync_Bits
- sync_Reset
- sync_Vector
- sync_Command

fifo_ic_got

fifo_ic_got

fifo_ic_got

fifo_ic_got

9.1.3 net

- eth

eth

- eth_RSLayer_GMII_GMII_KC705
- eth_RSLayer_GMII_GMII_ML505
- eth_RSLayer_GMII_GMII_ML605

eth_RSLayer_GMII_GMII_KC705

eth_RSLayer_GMII_GMII_ML505

eth_RSLayer_GMII_GMII_ML605

9.2 Board Constraint Files

- Altera Boards
  - Cyclone III
  - Stratix IV
  - Stratix V
- Lattice Boards
- Xilinx Boards
  - Artix-7
  - Kintex-7
  - Spartan-3 Boards
  - Spartan-6 Boards
  - Virtex-5
  - Virtex-6
  - Virtex-7
  - Zynq-7000

9.2.1 Altera

- Cyclone III * DE0 * DE0 nano
- Stratix IV * DE4
- Stratix V * DE5

Cyclone III

- DE0
- DE0 nano

ECP5 Versa

ECP5 Versa

Stratix IV

- DE4

DE4

Stratix V

- DE5

DE5

9.2.2 Lattice

- ECP5 * ECP5 Versa

ECP5

- ECP5 Versa

ECP5 Versa

9.2.3 Xilinx

- **Spartan-3 Boards**
  - Spartan-3 Starter Kit (S3SK)
  - Spartan-3E Starter Kit (S3ESK)
- **Spartan-6 Boards**
  - Atlys
- **Artix-7**
  - AC701
- **Kintex-7**

    - KC705
- **Virtex-5**
    - ML505
    - ML506
    - XUPV5
- **Virtex-6**
    - ML605
- **Virtex-7**
    - VC707
- **Zynq-7000**
    - ZC706
    - ZedBoard

Spartan-3

- Spartan-3 Starter Kit (S3SK)
- Spartan-3E Starter Kit (S3ESK)

S3SK

S3ESK

Spartan-6

- Atlys

Atlys

Artix-7

- AC701

AC701

Kintex-7

- KC705

KC705

Virtex-5

- ML505
- ML506
- XUPV5

ML505

ML506

XUPV5

Virtex-6

- ML605

ML605

Virtex-7

- VC707

VC707

Zynq-7000

- ZC706
- ZedBoard

ZC706

ZedBoard

CHAPTER 10

Tool Chain Specifics

Attention: This page is under construction.

10.1 Aldec Active-HDL

Todo:

- No GUI mode supported
- VHDL-2008 parser bug in Active-HDL 10.3

10.2 Mentor QuestaSim

Special feature: embedded poc prodecures to recompile relaunch, rerun and save waveforms...

10.3 Xilinx ISE

- Describe the `use_new_parser yes` option

10.4 Xilinx Vivado

- Describe the `vivado` branch (Git).

CHAPTER 11

Examples

Note: Under construction.

PoC-Exmaples repository on GitHub.

Part III

References

CHAPTER 12

Command Reference

This is the command line option reference for all provided scripts (Bash, PowerShell, Perl) and programs (Python) shipped with PoC.

12.1 PoC Wrapper Scripts

The PoC main program **PoC.py** requires a prepared environment, which needs to be setup by platform specific wrapper scripts written as shell scripts language (PowerShell/Bash). Moreover, the main program requires a supported Python version, so the wrapper script will search the best matching language environment.

The wrapper script offers the ability to hook in user-defined scripts to prepared (before) and clean up the environment (after) a PoC execution. E.g. it's possible to load the environment variable `LM_LICENSE_FILE` for the FlexLM license manager.

Created Environment Variables

PoCRootDirectory
: The path to PoC's root directory.

12.1.1 poc.ps1

`PoC.ps1` is the wrapper for the Windows platform using a PowerShell script. It can be debugged by adding the command line switch *-D*. All parameters are passed to `PoC.py`.

-D
: Enabled debug mode in the wrapper script.

Other arguments
: All remaining arguments are passed to `PoC.py`.

12.1.2 poc.sh

`PoC.sh` is the wrapper for Linux and Unix platforms using a Bash script. It can be debugged by adding the command line switch `-D`. All parameters are passed to `PoC.py`.

`-D`
: Enabled debug mode in the wrapper script.

`Other arguments`
: All remaining arguments are passed to `PoC.py`.

12.2 Main Program (`PoC.py`)

The main program `PoC.py` expects the environment variable *`PoCRootDirectory`* to be set.

12.3 Pre-compile Scripts

The following scripts can be used to pre-compile vendor's primitives or third party libraries. Pre-compile vendor primitives are required for vendor specific simulations or if no generic IP core implementation is available. Third party libraries are usually used as simulation helpers and thus needed by many testbenches.

The pre-compiled packages and libraries are stored in the directory `/temp/precompiled/`. Per simulator, one `<simulator>/` sub-directory is created. Each simulator directory in turn contains library directories, which may be grouped by the library vendor's name: `[<vendor>/]<library>/`.

So for example: *OSVVM* pre-compiled with GHDL is stored in `/temp/precompiled/ghdl/osvvm/`. Note OSVVM is a single library and thus no vendor directory is used to group the generated files. GHDL will also create VHDL language revision sub-directories like `v93/` or `v08/`.

Currently the provided scripts support 2 simulator targets and one combined target:

Target	Description
All	pre-compile for all simulators
GHDL	pre-compile for the GHDL simulator
Questa	pre-compile for Metor Graphics QuestaSim

The GHDL simulator distinguishes various VHDL language revisions and thus can pre-compile the source for these language revisions into separate output directories. The command line switch `-All`/`--all` will build the libraries for all major VHDL revisions (93, 2008).

Pre-compile Altera Libraries

12.3.1 compile-altera.sh

This script pre-compiles the Altera primitives. This script will generate all outputs into a `altera` directory.

Supported Simulators

Target	Description
All	pre-compile for all simulators
GHDL	pre-compile for the GHDL simulator
Questa	pre-compile for Metor Graphics QuestaSim

Command Line Options

--help
Show the embedded help page(s).

--clean
Clean up directory before analyzing.

--all
Pre-compile all libraries and packages for all simulators.

--ghdl
Pre-compile the Altera Quartus libraries for GHDL.

--questa
Pre-compile the Altera Quartus libraries for QuestaSim.

Additional Options for GHDL

--vhdl93
For GHDL only: Set VHDL Standard to '93.

--vhdl2008
For GHDL only: Set VHDL Standard to '08.

GHDL Notes

Not all primitives and macros are available as plain VHDL source code. Encrypted primitives and netlists cannot be pre-compiled by GHDL.

QuestaSim Notes

The pre-compilation for QuestaSim uses a build in program from Altera.

12.3.2 compile-altera.ps1

This script pre-compiles the Altera primitives. This script will generate all outputs into a `altera` directory.

Supported Simulators

Target	Description
All	pre-compile for all simulators
GHDL	pre-compile for the GHDL simulator
Questa	pre-compile for Metor Graphics QuestaSim

Command Line Options

-Help
Show the embedded help page(s).

-Clean
Clean up directory before analyzing.

-All
Pre-compile all libraries and packages for all simulators.

-GHDL
Pre-compile the Altera Quartus libraries for GHDL.

-Questa
Pre-compile the Altera Quartus libraries for QuestaSim.

Additional Options for GHDL

-VHDL93
For GHDL only: Set VHDL Standard to '93.

-VHDL2008
For GHDL only: Set VHDL Standard to '08.

GHDL Notes

Not all primitives and macros are available as plain VHDL source code. Encrypted primitives and netlists cannot be pre-compiled by GHDL.

QuestaSim Notes

The pre-compilation for QuestaSim uses a build in program from Altera.

Pre-compile Lattice Libraries

12.3.3 compile-lattice.sh

This script pre-compiles the Lattice primitives. This script will generate all outputs into a `lattice` directory.

Supported Simulators

Target	Description
All	pre-compile for all simulators
GHDL	pre-compile for the GHDL simulator
Questa	pre-compile for Metor Graphics QuestaSim

Command Line Options

--help
Show the embedded help page(s).

--clean
Clean up directory before analyzing.

--all
Pre-compile all libraries and packages for all simulators.

--ghdl
Pre-compile the Altera Quartus libraries for GHDL.

--questa
Pre-compile the Altera Quartus libraries for QuestaSim.

Additional Options for GHDL

--vhdl93
For GHDL only: Set VHDL Standard to '93.

--vhdl2008
For GHDL only: Set VHDL Standard to '08.

GHDL Notes

Not all primitives and macros are available as plain VHDL source code. Encrypted primitives and netlists cannot be pre-compiled by GHDL.

QuestaSim Notes

The pre-compilation for QuestaSim uses a build in program from Lattice.

12.3.4 compile-lattice.ps1

This script pre-compiles the Lattice primitives. This script will generate all outputs into a `lattice` directory.

Supported Simulators

Target	Description
All	pre-compile for all simulators
GHDL	pre-compile for the GHDL simulator
Questa	pre-compile for Metor Graphics QuestaSim

Command Line Options

-Help
Show the embedded help page(s).

-Clean
Clean up directory before analyzing.

-All
Pre-compile all libraries and packages for all simulators.

-GHDL
Pre-compile the Altera Quartus libraries for GHDL.

-Questa
Pre-compile the Altera Quartus libraries for QuestaSim.

Additional Options for GHDL

-VHDL93
For GHDL only: Set VHDL Standard to '93.

-VHDL2008
For GHDL only: Set VHDL Standard to '08.

GHDL Notes

Not all primitives and macros are available as plain VHDL source code. Encrypted primitives and netlists cannot be pre-compiled by GHDL.

QuestaSim Notes

The pre-compilation for QuestaSim uses a build in program from Lattice.

Pre-compile OSVVM Libraries

12.3.5 compile-osvvm.sh

This script pre-compiles the OSVVM packages. This script will generate all outputs into a `osvvm` directory.

Supported Simulators

Target	Description
All	pre-compile for all simulators
GHDL	pre-compile for the GHDL simulator
Questa	pre-compile for Metor Graphics QuestaSim

Command Line Options

--help
Show the embedded help page(s).

--clean
Clean up directory before analyzing.

--all
Pre-compile all libraries and packages for all simulators.

--ghdl
Pre-compile the Altera Quartus libraries for GHDL.

--questa
Pre-compile the Altera Quartus libraries for QuestaSim.

Additional Options for GHDL

--vhdl93
For GHDL only: Set VHDL Standard to '93.

--vhdl2008
For GHDL only: Set VHDL Standard to '08.

12.3.6 compile-osvvm.ps1

This script pre-compiles the OSVVM packages. This script will generate all outputs into a `osvvm` directory.

Supported Simulators

Target	Description
All	pre-compile for all simulators
GHDL	pre-compile for the GHDL simulator
Questa	pre-compile for Metor Graphics QuestaSim

Command Line Options

-Help
Show the embedded help page(s).

-Clean
Clean up directory before analyzing.

-All
Pre-compile all libraries and packages for all simulators.

-GHDL
Pre-compile the Altera Quartus libraries for GHDL.

-Questa
Pre-compile the Altera Quartus libraries for QuestaSim.

Additional Options for GHDL

-VHDL93
For GHDL only: Set VHDL Standard to '93.

-VHDL2008
For GHDL only: Set VHDL Standard to '08.

Pre-compile UVVM Libraries

12.3.7 compile-uvvm.sh

This script pre-compiles the UVVM framework. This script will generate all outputs into a `uvvm` directory.

Supported Simulators

Target	Description
All	pre-compile for all simulators
GHDL	pre-compile for the GHDL simulator
Questa	pre-compile for Metor Graphics QuestaSim

Command Line Options

--help
Show the embedded help page(s).

--clean
Clean up directory before analyzing.

--all
Pre-compile all libraries and packages for all simulators.

--ghdl
Pre-compile the Altera Quartus libraries for GHDL.

--questa
Pre-compile the Altera Quartus libraries for QuestaSim.

Additional Options for GHDL

--vhdl93
For GHDL only: Set VHDL Standard to '93.

--vhdl2008
For GHDL only: Set VHDL Standard to '08.

12.3.8 compile-uvvm.ps1

This script pre-compiles the UVVM framework. This script will generate all outputs into a `uvvm` directory.

Supported Simulators

Target	Description
All	pre-compile for all simulators
GHDL	pre-compile for the GHDL simulator
Questa	pre-compile for Metor Graphics QuestaSim

Command Line Options

-Help
Show the embedded help page(s).

-Clean
Clean up directory before analyzing.

-All
Pre-compile all libraries and packages for all simulators.

-GHDL
Pre-compile the Altera Quartus libraries for GHDL.

-Questa
Pre-compile the Altera Quartus libraries for QuestaSim.

Additional Options for GHDL

-VHDL93
For GHDL only: Set VHDL Standard to '93.

-VHDL2008
For GHDL only: Set VHDL Standard to '08.

Pre-compile Xilinx ISE Libraries

12.3.9 compile-xilinx-ise.sh

This script pre-compiles the Xilinx primitives. Because Xilinx offers two tool chains (ISE, Vivado), this script will generate all outputs into a `xilinx-ise` directory and a symlink to `xilinx` will be created. This eases the coexistence of pre-compiled primitives from ISE and Vivado.

Supported Simulators

Target	Description
All	pre-compile for all simulators
GHDL	pre-compile for the GHDL simulator
Questa	pre-compile for Metor Graphics QuestaSim

Command Line Options

`--help`
Show the embedded help page(s).

`--clean`
Clean up directory before analyzing.

`--all`
Pre-compile all libraries and packages for all simulators.

`--ghdl`
Pre-compile the Altera Quartus libraries for GHDL.

`--questa`
Pre-compile the Altera Quartus libraries for QuestaSim.

Additional Options for GHDL

`--vhdl93`
For GHDL only: Set VHDL Standard to '93.

`--vhdl2008`
For GHDL only: Set VHDL Standard to '08.

GHDL Notes

Not all primitives and macros are available as plain VHDL source code. Encrypted SecureIP primitives and netlists cannot be pre-compiled by GHDL.

QuestaSim Notes

The pre-compilation for QuestaSim uses a build in program from Xilinx.

12.3.10 compile-xilinx-ise.ps1

This script pre-compiles the Xilinx primitives. Because Xilinx offers two tool chains (ISE, Vivado), this script will generate all outputs into a `xilinx-ise` directory and a symlink to `xilinx` will be created. This eases the coexistence of pre-compiled primitives from ISE and Vivado. The symlink can be changed by the user or via *-ReLink*.

Supported Simulators

Target	Description
All	pre-compile for all simulators
GHDL	pre-compile for the GHDL simulator
Questa	pre-compile for Metor Graphics QuestaSim

Command Line Options

-Help
: Show the embedded help page(s).

-Clean
: Clean up directory before analyzing.

-All
: Pre-compile all libraries and packages for all simulators.

-GHDL
: Pre-compile the Altera Quartus libraries for GHDL.

-Questa
: Pre-compile the Altera Quartus libraries for QuestaSim.

-ReLink
: Change the 'xilinx' symlink to 'xilinx-ise'.

Additional Options for GHDL

-VHDL93
: For GHDL only: Set VHDL Standard to '93.

-VHDL2008
: For GHDL only: Set VHDL Standard to '08.

GHDL Notes

Not all primitives and macros are available as plain VHDL source code. Encrypted SecureIP primitives and netlists cannot be pre-compiled by GHDL.

QuestaSim Notes

The pre-compilation for QuestaSim uses a build in program from Xilinx.

Pre-compile Xilinx Vivado Libraries

12.3.11 compile-xilinx-vivado.sh

This script pre-compiles the Xilinx primitives. Because Xilinx offers two tool chains (ISE, Vivado), this script will generate all outputs into a `xilinx-vivado` directory and a symlink to `xilinx` will be created. This eases the coexistence of pre-compiled primitives from ISE and Vivado.

Supported Simulators

Target	Description
All	pre-compile for all simulators
GHDL	pre-compile for the GHDL simulator
Questa	pre-compile for Metor Graphics QuestaSim

Command Line Options

`--help`
Show the embedded help page(s).

`--clean`
Clean up directory before analyzing.

`--all`
Pre-compile all libraries and packages for all simulators.

`--ghdl`
Pre-compile the Altera Quartus libraries for GHDL.

`--questa`
Pre-compile the Altera Quartus libraries for QuestaSim.

Additional Options for GHDL

`--vhdl93`
For GHDL only: Set VHDL Standard to '93.

`--vhdl2008`
For GHDL only: Set VHDL Standard to '08.

GHDL Notes

Not all primitives and macros are available as plain VHDL source code. Encrypted SecureIP primitives and netlists cannot be pre-compiled by GHDL.

QuestaSim Notes

The pre-compilation for QuestaSim uses a build in program from Xilinx.

12.3.12 compile-xilinx-vivado.ps1

This script pre-compiles the Xilinx primitives. Because Xilinx offers two tool chains (ISE, Vivado), this script will generate all outputs into a `xilinx-vivado` directory and a symlink to `xilinx` will be created. This eases the coexistence of pre-compiled primitives from ISE and Vivado. The symlink can be changed by the user or via *-ReLink*.

Supported Simulators

Target	Description
All	pre-compile for all simulators
GHDL	pre-compile for the GHDL simulator
Questa	pre-compile for Metor Graphics QuestaSim

Command Line Options

-Help
: Show the embedded help page(s).

-Clean
: Clean up directory before analyzing.

-All
: Pre-compile all libraries and packages for all simulators.

-GHDL
: Pre-compile the Altera Quartus libraries for GHDL.

-Questa
: Pre-compile the Altera Quartus libraries for QuestaSim.

-ReLink
: Change the 'xilinx' symlink to 'xilinx-vivado'.

Additional Options for GHDL

-VHDL93
: For GHDL only: Set VHDL Standard to '93.

-VHDL2008
: For GHDL only: Set VHDL Standard to '08.

GHDL Notes

Not all primitives and macros are available as plain VHDL source code. Encrypted SecureIP primitives and netlists cannot be pre-compiled by GHDL.

QuestaSim Notes

The pre-compilation for QuestaSim uses a build in program from Xilinx.

CHAPTER 13

IP Core Database

Contents of this Page

13.1 Overview

PoC internal IP core database uses INI files and advanced interpolation rules provided by ExtendedConfigParser. The database consists of 5 *.ini files:

- **`pyconfig.boards.ini`** This files contains all known *FPGA boards* and *FPGA devices*.

- **pyconfig.defaults.ini** This files contains all default options and values for all supported node types.
- **pyconfig.entity.ini** This file contains all IP cores (entities) and theirs corresponding testbench or netlist settings.
- **pyconfig.private.ini** This files is created by `.\poc.ps1 configure` and contains settings for the local PoC installation. This files must not be shared with other PoC instances. See *Configuring PoC's Infrastructure* on how to configure PoC on a local system.
- **pyconfig.structure.ini** Nodes in this file describe PoC's namespace tree and which IP cores are assigned to which namespace.

Additionally, the database refers to **.files* and **.rules* files. The first file type describes, in an imperative language, which files are needed to compile a simulation or to run a synthesis. The latter file type contains patch instructions per IP core. See *Files Formats* for more details.

13.2 Database Structure

The database is stored in multiple *INI files*, which are merged in memory to a single configuration database. Each INI file defines an associative array of *sections* and option lines. The content itself is an associative array of *options* and values. Section names are inclosed in square brackets `[...]` and allow simple case-sensitive strings as names. A section name is followed by its section content, which consists of option lines.

One option is stored per option line and consists of an option name and a value separated by an equal sign =. The option name is also a case-sensitive simple string. The value is string, starts after the first non-whitespace character and end before the newline character at the end of the line. The content can be of any string, except for the newline characters. Support for escape sequences depends on the option usage.

Values containing `${...}` and `%{...}` are raw values, which need to be interpolated by the ExtendedConfigParser. See *Value Interpolation* and *Node Interpolation* for more details.

Sections can have a default section called `DEFAULT`. Options not found in a normal section are looked up in the default section. If found, the value of the matching option name is the lookup result.

Example

```
[section1]
option1 = value1
opt2 =    val ue $2

[section2]
option1 = ${section1:option1}
opt2 =    ${option1}
```

Option lines can be of three kinds: An option, a reference, or a user defined variable. While the syntax is always the same, the meaning is infered from the context.

Option Line Kind	Distinguishing Characteristic
Reference	The option name is called a (node) reference, if the valueof an option is a predefined keyword for the current nodeclass. Because the option's value is a keyword, it can notbe an interpolated value.
Option	The option uses a defined option name valid for the currentnode class. The value can be a fixed or interpolated string.
User Defined Variable	Otherwise an option line is a user defined variable. It canhave fixed or interpolated string values.

```
[PoC]
Name =
Prefix =
arith =          Namespace
bus =            Namespace

[PoC.arith]
addw =           Entity
prng =           Entity

[PoC.bus]
stream =         Namespace
wb =             Namespace
Arbiter =        Entity

[PoC.bus.stream]
Buffer =         Entity
DeMux =          Entity
Mirror =         Entity
Mux =            Entity

[PoC.bus.wb]
fifo_adapter =   Entity
ocram_adapter =  Entity
uart_wrapper =   Entity
```

13.2.1 Nodes

The database is build of nested associative arrays and generated in-memory from 5 *.ini files. This implies that all section names are required to be unique. (Section merging is not allowed.) A fully qualified section name has a prefix and a section name delimited by a dot character. The section name itself can consist of parts also delimited by dot characters. All nodes with the same prefix shape a node class.

The following table lists all used prefixes:

Prefix	Description
INSTALL	A installed tool (chain) or program.
SOLUTION	Registered external solutions / projects.
CONFIG	Configurable PoC settings.
BOARD	A node to describe a known board.
CONST	A node to describe constraint file set for a known board.
PoC	Nodes to describe PoC's namespace structure.
IP	A node describing an IP core.
TB	A node describing testbenches.
COCOTB	A node describing Cocotb testbenches.
CG	A node storing Core Generator settings.
LSE	A node storing settings for LSE based netlist generation.
QMAP	A node storing settings for Quartus based netlist generation.
XST	A node storing settings for XST based netlist generation.
VIVADO	A node storing settings for Vivado based netlist generation.
XCI	A node storing settings for IP Catalog based netlist generation.

The database has 3 special sections without prefixes:

Section Name	Description
PoC	Root node for PoC's namespace hierarchy.
BOARDS	Lists all known boards.
SPECIAL	Section with dummy values. This is needed by synthesis and overwritten at runtime.

Example section names

```
[PoC]
[PoC.arith]
[PoC.bus]
[PoC.bus.stream]
[PoC.bus.wb]
```

The fully qualified section name `PoC.bus.stream` has the prefix `PoC` and the section name `bus.stream`. The section name has two parts: `bus` and `stream`. The dot delimited section name can be considered a path in a hierarchical database. The parent node is `PoC.bus` and its grandparent is `PoC`. (Note this is a special section. See the special sections table from above.)

13.2.2 References

Whatever this is handy to create new field

13.2.3 Options

13.2.4 Values

13.2.5 Value Interpolation

13.2.6 Node Interpolation

13.2.7 Root Nodes

13.3 Supported Options

Note: See `py\config.defaults.ini` for predefined default values (options) and predefined variables, which can be used as a shortcut.

13.4 Files in detail

13.4.1 config.structure.ini

13.4.2 config.entity.ini

13.4.3 config.boards.ini

13.4.4 config.private.ini

13.5 User Defined Variables

CHAPTER 14

Python Infrastructure

14.1 PoC.py

Classes

- `PoCEntityAttribute`: Undocumented.
- `BoardDeviceAttributeGroup`: Undocumented.
- `VHDLVersionAttribute`: Undocumented.
- `SimulationStepsAttributeGroup`: Undocumented.
- `CompileStepsAttributeGroup`: Undocumented.
- `PileOfCores`: A mixin class to provide local logging methods.

Functions

- `main()`: This is the entry point for PoC.py written as a function.

class PoC.**PoCEntityAttribute**

Inheritance

Members

classmethod GetAttributes(*method*)

classmethod GetMethods(*cl*)

static _AppendAttribute(*attribute*)

_debug = False

class PoC.**BoardDeviceAttributeGroup**

Inheritance

Members

classmethod GetAttributes(*method*)

classmethod GetMethods(*cl*)

static _AppendAttribute(*attribute*)

_debug = False

class PoC.**VHDLVersionAttribute**

Inheritance

Members

classmethod GetAttributes(*method*)

classmethod GetMethods(*cl*)

static _AppendAttribute(*attribute*)

_debug = False

class PoC.**SimulationStepsAttributeGroup**

Inheritance

Members

classmethod GetAttributes(*method*)

classmethod GetMethods(*cl*)

static _AppendAttribute(*attribute*)

_debug = False

class PoC.**CompileStepsAttributeGroup**

Inheritance

Members

classmethod GetAttributes(*method*)

classmethod GetMethods(*cl*)

static _AppendAttribute(*attribute*)

_debug = False

class PoC.**PileOfCores**(*debug*, *verbose*, *quiet*, *dryRun*, *sphinx=False*)

Inheritance

Members

HeadLine = 'The PoC-Library - Service Tool'

Platform

DryRun

Directories

ConfigFiles

PoCConfig

Root

Repository

SaveAndReloadPoCConfiguration()

Run()

PrintHeadline()

HandleDefault(*_*)

HandleHelp(*args*)

HandleInfo(*args*)

HandleConfiguration(*args*)
Handle 'configure' command.

HandleSelection(*args*)
Handle 'select' command.

HandleAddSolution(*_*)

HandleListSolution(*_*)

HandleRemoveSolution(*args*)

HandleListProject(*args*)

HandleQueryConfiguration(*args*)

_ExtractBoard(*BoardName*, *DeviceName*, *force=False*)

_ExtractFQNs(*fqns*, *defaultLibrary='PoC'*, *defaultType=<EntityTypes.Testbench: 2>*)

_ExtractVHDLVersion(*vhdlVersion*, *defaultVersion=None*)

_CheckActiveHDL()

_CheckRivieraPRO()

_CheckQuartus()

_CheckDiamond()

_CheckModelSim()

_CheckISE()

_CheckVivado()

_CheckGHDL()

static _ExtractSimulationSteps(*analyze*, *elaborate*, *optimize*, *recompile*, *simulate*, *showWaveform*, *showCoverage*, *resimulate*, *showReport*, *cleanUp*)

static _ExtractCompileSteps(*synthesize*, *showReport*, *cleanUp*)

HandleListTestbenches(*args*)

HandleActiveHDLSimulation(*args*)

HandleGHDLSimulation(*args*)

HandleISESimulation(*args*)

HandleModelSimSimulation(*args*)

HandleAnyMentorSimulation(*args*)

HandleRivieraPROSimulation(*args*)

HandleQuestaSimSimulation(*args*)

HandleVivadoSimulation(*args*)

HandleCocotbSimulation(*args*)

HandleListNetlist(*args*)

HandleISECompilation(*args*)

HandleCoreGeneratorCompilation(*args*)

HandleXstCompilation(*args*)

HandleIpCatalogCompilation(*args*)

HandleVivadoCompilation(*args*)

HandleQuartusCompilation(*args*)

HandleLSECompilation(*args*)

static GetAttributes()

GetMethods()

static HasAttribute()

Log(*entry*, *condition=True*)
Write an entry to the local logger.

LogDebug(**args*, *condition=True*, ***kwargs*)

LogDryRun(**args*, *condition=True*, ***kwargs*)

LogError(**args*, *condition=True*, ***kwargs*)

LogFatal(**args*, *condition=True*, ***kwargs*)

LogInfo(**args*, *condition=True*, ***kwargs*)

LogNormal(**args*, *condition=True*, ***kwargs*)

LogQuiet(**args*, *condition=True*, ***kwargs*)

LogVerbose(**args*, *condition=True*, ***kwargs*)

LogWarning(**args*, *condition=True*, ***kwargs*)

Logger
Return the local logger instance.

MainParser

SubParsers

_ArgParseMixin__mainParser = None

_ArgParseMixin__subParser = None

_ArgParseMixin__subParsers = {}

_PileOfCores__BackupPoCConfiguration()

_PileOfCores__CONFIGFILE_BOARDS = 'config.boards.ini'

_PileOfCores__CONFIGFILE_DEFAULTS = 'config.defaults.ini'

_PileOfCores__CONFIGFILE_DIRECTORY = 'py'

_PileOfCores__CONFIGFILE_IPCORES = 'config.entity.ini'

_PileOfCores__CONFIGFILE_PRIVATE = 'config.private.ini'

_PileOfCores__CONFIGFILE_STRUCTURE = 'config.structure.ini'

_PileOfCores__CheckEnvironment()

_PileOfCores__CheckSection(*sectionName*, *toolName*)

_PileOfCores__PLATFORM = 'Linux'

_PileOfCores__PrepareForConfiguration()

_PileOfCores__PrepareForSimulation()

_PileOfCores__PrepareForSynthesis()

_PileOfCores__ReadPoCConfiguration()

_PileOfCores__WritePoCConfiguration()

_TryLog(**args*, *condition=True*, ***kwargs*)

Functions

PoC.**main**()
This is the entry point for PoC.py written as a function.

1. It extracts common flags from the script's arguments list, before `ArgumentParser` is fully loaded.
2. It initializes colorama for colored outputs
3. It creates an instance of PoC and hands over to class based execution. All is wrapped in a big `try..except` block to catch every unhandled exception.
4. Shutdown the script and return its exit code.

14.2 Base

Submodules

14.2.1 Base.Exceptions

Exceptions

- *ExceptionBase*: Base exception derived from `Exception` for all
- *EnvironmentException*: `EnvironmentException` is raised when an expected environment variable is
- *PlatformNotSupportedException*: `PlatformNotSupportedException` is raise if the platform is not supported
- *NotConfiguredException*: `NotConfiguredException` is raise if PoC or the requested tool chain
- *SkipableException*: Base class for all skipable exceptions.
- *CommonException*: Base exception derived from `Exception` for all
- *SkipableCommonException*: `SkipableCommonException` is a *CommonException*, which can be

exception Base.Exceptions.**ExceptionBase**(*message=''*)
Base exception derived from `Exception` for all custom exceptions in PoC.

Inheritance

Members

__init__(*message=''*)
Exception initializer

Parameters **message** (*str*) – The exception message.

__str__()
Returns the exception's message text.

args

exception Base.Exceptions.**EnvironmentException**(*message=''*)
EnvironmentException is raised when an expected environment variable is missing for PoC.

Inheritance

Members

__init__(*message=''*)
Exception initializer

Parameters **message** (*str*) – The exception message.

__str__()
Returns the exception's message text.

args

exception Base.Exceptions.**PlatformNotSupportedException**(*message=''*)
PlatformNotSupportedException is raise if the platform is not supported by PoC, or the selected tool flow is not supported on the host system by PoC.

Inheritance

Members

__init__(*message=''*)
Exception initializer

Parameters **message** (*str*) – The exception message.

__str__()
Returns the exception's message text.

args

exception Base.Exceptions.**NotConfiguredException**(*message=''*)
NotConfiguredException is raise if PoC or the requested tool chain setting is not configured in PoC.

Inheritance

Members

__init__(*message=''*)
Exception initializer

Parameters **message** (*str*) – The exception message.

__str__()
Returns the exception's message text.

args

exception Base.Exceptions.**SkipableException**(*message=''*)
Base class for all skipable exceptions.

Inheritance

Members

__init__(*message=''*)
Exception initializer

Parameters **message** (*str*) – The exception message.

__str__()
Returns the exception's message text.

args

exception Base.Exceptions.**CommonException**(*message=''*)

Inheritance

Members

__init__(*message=''*)
Exception initializer

Parameters **message** (*str*) – The exception message.

__str__()
Returns the exception's message text.

args

exception Base.Exceptions.**SkipableCommonException**(*message=''*)
`SkipableCommonException` is a *CommonException*, which can be skipped.

Inheritance

Members

__init__(*message=''*)
Exception initializer

Parameters **message** (*str*) – The exception message.

__str__()
Returns the exception's message text.

args

14.2.2 Base.Executable

Exceptions

- *ExecutableException*: This exception is raised by all executable abstraction classes.

Classes

- *CommandLineArgument*: Base class (and meta class) for all Arguments classes.
- *ExecutableArgument*: Represents the executable.
- *NamedCommandLineArgument*: Base class for all command line arguments with a name.
- *CommandArgument*: Represents a command name.
- *ShortCommandArgument*: Represents a command name with a single dash.
- *LongCommandArgument*: Represents a command name with a double dash.
- *WindowsCommandArgument*: Represents a command name with a single slash.
- *StringArgument*: Represents a simple string argument.
- *StringListArgument*: Represents a list of string arguments.
- *PathArgument*: Represents a path argument.
- *FlagArgument*: Base class for all FlagArgument classes, which represents a simple flag argument.
- *ShortFlagArgument*: Represents a flag argument with a single dash.
- *LongFlagArgument*: Represents a flag argument with a double dash.
- *WindowsFlagArgument*: Represents a flag argument with a single slash.
- *ValuedFlagArgument*: Class and base class for all ValuedFlagArgument classes, which represents a flag argument with data.
- *ShortValuedFlagArgument*: Represents a *ValuedFlagArgument* with a single dash.
- *LongValuedFlagArgument*: Represents a *ValuedFlagArgument* with a double dash.
- *WindowsValuedFlagArgument*: Represents a *ValuedFlagArgument* with a single slash.
- *ValuedFlagListArgument*: Class and base class for all ValuedFlagListArgument classes, which represents a list of *ValuedFlagArgument* instances.
- *ShortValuedFlagListArgument*: Represents a *ValuedFlagListArgument* with a single dash.
- *LongValuedFlagListArgument*: Represents a *ValuedFlagListArgument* with a double dash.
- *WindowsValuedFlagListArgument*: Represents a *ValuedFlagListArgument* with a single slash.
- *TupleArgument*: Class and base class for all TupleArgument classes, which represents a switch with separate data.
- *ShortTupleArgument*: Represents a *TupleArgument* with a single dash in front of the switch name.
- *LongTupleArgument*: Represents a *TupleArgument* with a double dash in front of the switch name.
- *WindowsTupleArgument*: Represents a *TupleArgument* with a single slash in front of the switch name.
- *CommandLineArgumentList*: Represent a list of all available commands, flags and switch of an executable.
- *Environment*: Undocumented.
- *Executable*: Represent an executable.

exception Base.Executable.**ExecutableException**(*message=''*)
This exception is raised by all executable abstraction classes.

Inheritance

Members

__str__()
Returns the exception's message text.

args

class Base.Executable.**CommandLineArgument**
Base class (and meta class) for all Arguments classes.

Inheritance

Members

_value = None

mro() → list
return a type's method resolution order

class Base.Executable.**ExecutableArgument**
Represents the executable.

Inheritance

Members

Value

AsArgument()

_value = None

mro() → list
return a type's method resolution order

class Base.Executable.**NamedCommandLineArgument**
Base class for all command line arguments with a name.

Inheritance

Members

_name = None

Name

_value = None

mro() → list
return a type's method resolution order

class Base.Executable.**CommandArgument**
Represents a command name.

It is usually used to select a sub parser in a CLI argument parser or to hand over all following parameters to a separate tool. An example for a command is 'checkout' in `git.exe checkout`, which calls `git-checkout.exe`.

Inheritance

Members

_pattern = '{0}'

Value

AsArgument()

Name

_name = None

_value = None

mro() → list
return a type's method resolution order

class Base.Executable.**ShortCommandArgument**
Represents a command name with a single dash.

Inheritance

Members

_pattern = '-{0}'

AsArgument()

Name

Value

_name = None

_value = None

mro() → list
return a type's method resolution order

class Base.Executable.**LongCommandArgument**
Represents a command name with a double dash.

Inheritance

Members

_pattern = '--{0}'

AsArgument()

Name

Value

_name = None

_value = None

mro() → list
return a type's method resolution order

class Base.Executable.**WindowsCommandArgument**
Represents a command name with a single slash.

Inheritance

Members

_pattern = '/{0}'

AsArgument()

Name

Value

_name = None

_value = None

mro() → list
return a type's method resolution order

class Base.Executable.**StringArgument**
Represents a simple string argument.

Inheritance

Members

_pattern = '{0}'

Value

AsArgument()

_value = None

mro() → list
return a type's method resolution order

class Base.Executable.**StringListArgument**
Represents a list of string arguments.

Inheritance

Members

_pattern = '{0}'

Value

AsArgument()

_value = None

mro() → list
return a type's method resolution order

class Base.Executable.**PathArgument**
Represents a path argument.

The output format can be forced to the POSIX format with *_PosixFormat*.

Inheritance

Members

_PosixFormat = False

Value

AsArgument()

_value = None

mro() → list
return a type's method resolution order

class Base.Executable.**FlagArgument**
Base class for all FlagArgument classes, which represents a simple flag argument.

A simple flag is a single boolean value (absent/present or off/on) with no data.

Inheritance

Members

_pattern = '{0}'

Value

AsArgument()

Name

_name = None

_value = None

mro() → list
return a type's method resolution order

class Base.Executable.**ShortFlagArgument**
Represents a flag argument with a single dash.

Example: `-optimize`

Inheritance

Members

_pattern = '-{0}'

AsArgument()

Name

Value

_name = None

_value = None

mro() → list
return a type's method resolution order

class Base.Executable.**LongFlagArgument**
Represents a flag argument with a double dash.

Example: `--optimize`

Inheritance

Members

_pattern = '--{0}'

AsArgument()

Name

Value

_name = None

_value = None

mro() → list
return a type's method resolution order

class Base.Executable.**WindowsFlagArgument**
Represents a flag argument with a single slash.

Example: `/optimize`

Inheritance

Members

_pattern = '/{0}'

AsArgument()

Name

Value

_name = None

_value = None

mro() → list
return a type's method resolution order

class Base.Executable.**ValuedFlagArgument**
Class and base class for all ValuedFlagArgument classes, which represents a flag argument with data.

A valued flag is a flag name followed by a value. The default delimiter sign is equal (=). Name and value are passed as one arguments to the executable even if the delimiter sign is a whitespace character.

Example: `width=100`

Inheritance

Members

_pattern = '{0}={1}'

Value

AsArgument()

Name

_name = None

_value = None

mro() → list
return a type's method resolution order

class Base.Executable.**ShortValuedFlagArgument**
Represents a *ValuedFlagArgument* with a single dash.

Example: `-optimizer=on`

Inheritance

Members

_pattern = '-{0}={1}'

AsArgument()

Name

Value

_name = None

_value = None

mro() → list
return a type's method resolution order

class Base.Executable.**LongValuedFlagArgument**
Represents a *ValuedFlagArgument* with a double dash.

Example: `--optimizer=on`

Inheritance

Members

_pattern = '--{0}={1}'

AsArgument()

Name

Value

_name = None

_value = None

mro() → list
return a type's method resolution order

class Base.Executable.**WindowsValuedFlagArgument**
Represents a *ValuedFlagArgument* with a single slash.

Example: `/optimizer:on`

Inheritance

Members

_pattern = '/{0}:{1}'

AsArgument()

Name

Value

_name = None

_value = None

mro() → list
return a type's method resolution order

class Base.Executable.**ValuedFlagListArgument**
Class and base class for all ValuedFlagListArgument classes, which represents a list of *ValuedFlagArgument* instances.

Each list item gets translated into a *ValuedFlagArgument*, with the same flag name, but differing values. Each *ValuedFlagArgument* is passed as a single argument to the executable, even if the delimiter sign is a whitespace character.

Example: `file=file1.txt file=file2.txt`

Inheritance

Members

_pattern = '{0}={1}'

Value

AsArgument()

Name

_name = None

_value = None

mro() → list
return a type's method resolution order

class Base.Executable.**ShortValuedFlagListArgument**
Represents a *ValuedFlagListArgument* with a single dash.

Example: `-file=file1.txt -file=file2.txt`

Inheritance

Members

_pattern = '-{0}={1}'

AsArgument()

Name

Value

_name = None

_value = None

mro() → list
return a type's method resolution order

class Base.Executable.**LongValuedFlagListArgument**
Represents a *ValuedFlagListArgument* with a double dash.

Example: `--file=file1.txt --file=file2.txt`

Inheritance

Members

_pattern = '--{0}={1}'

AsArgument()

Name

Value

_name = None

_value = None

mro() → list
return a type's method resolution order

class Base.Executable.**WindowsValuedFlagListArgument**
Represents a *ValuedFlagListArgument* with a single slash.

Example: `/file:file1.txt /file:file2.txt`

Inheritance

Members

_pattern = '/{0}:{1}'

AsArgument()

Name

Value

_name = None

_value = None

mro() → list
return a type's method resolution order

class Base.Executable.**TupleArgument**
Class and base class for all TupleArgument classes, which represents a switch with separate data.

A tuple switch is a command line argument followed by a separate value. Name and value are passed as two arguments to the executable.

Example: `width 100`

Inheritance

Members

_switchPattern = '{0}'

_valuePattern = '{0}'

Value

AsArgument()

Name

_name = None

_value = None

mro() → list
return a type's method resolution order

class Base.Executable.**ShortTupleArgument**
Represents a *TupleArgument* with a single dash in front of the switch name.

Example: `-file file1.txt`

Inheritance

Members

_switchPattern = '-{0}'

AsArgument()

Name

Value

_name = None

_value = None

_valuePattern = '{0}'

mro() → list
return a type's method resolution order

class Base.Executable.**LongTupleArgument**
Represents a *TupleArgument* with a double dash in front of the switch name.

Example: `--file file1.txt`

Inheritance

Members

_switchPattern = '--{0}'

AsArgument()

Name

Value

_name = None

_value = None

_valuePattern = '{0}'

mro() → list
return a type's method resolution order

class Base.Executable.**WindowsTupleArgument**
Represents a *TupleArgument* with a single slash in front of the switch name.

Example: `/file file1.txt`

Inheritance

Members

_switchPattern = '/{0}'

AsArgument()

Name

Value

_name = None

_value = None

_valuePattern = '{0}'

mro() → list
return a type's method resolution order

class Base.Executable.**CommandLineArgumentList**(**args*)
Represent a list of all available commands, flags and switch of an executable.

Inheritance

Members

ToArgumentList()

append(*object*) → None – append object to end

clear() → None – remove all items from L

copy() → list – a shallow copy of L

count(*value*) → integer – return number of occurrences of value

extend(*iterable*) → None – extend list by appending elements from the iterable

index(*value*[, *start*[, *stop*]]) → integer – return first index of value.
Raises ValueError if the value is not present.

insert()
L.insert(index, object) – insert object before index

pop([*index*]) → item – remove and return item at index (default last).
Raises IndexError if list is empty or index is out of range.

remove(*value*) → None – remove first occurrence of value.
Raises ValueError if the value is not present.

reverse()
L.reverse() – reverse *IN PLACE*

sort(*key=None*, *reverse=False*) → None – stable sort *IN PLACE*

class Base.Executable.**Environment**

Inheritance

Members

class Base.Executable.**Executable**(*platform: str*, *dryrun: bool*, *executablePath: pathlib.Path*, *environment: Base.Executable.Environment = None*, *logger: Base.Logging.Logger = None*)

Represent an executable.

Inheritance

Members

_POC_BOUNDARY = '====== POC BOUNDARY ======'

Log(*entry*, *condition=True*)

Write an entry to the local logger.

LogDebug(**args*, *condition=True*, ***kwargs*)

LogDryRun(**args*, *condition=True*, ***kwargs*)

LogError(**args*, *condition=True*, ***kwargs*)

LogFatal(**args*, *condition=True*, ***kwargs*)

LogInfo(**args*, *condition=True*, ***kwargs*)

LogNormal(**args*, *condition=True*, ***kwargs*)

LogQuiet(**args*, *condition=True*, ***kwargs*)

LogVerbose(**args*, *condition=True*, ***kwargs*)

LogWarning(**args*, *condition=True*, ***kwargs*)

Logger

Return the local logger instance.

_TryLog(**args*, *condition=True*, ***kwargs*)

Path

StartProcess(*parameterList*)

Send(*line*, *end='\n'*)

SendBoundary()

Terminate()

GetReader()

ReadUntilBoundary(*indent=0*)

14.2.3 Base.Logging

Classes

- *Severity*: Logging message severity levels.
- *LogEntry*: Represents a single line log message with a severity and indentation level.

- *Logger*: Undocumented.
- *ILogable*: A mixin class to provide local logging methods.

class Base.Logging.**Severity**(*_)
Logging message severity levels.

Inheritance

Members

Fatal = 30

Error = 25

Quiet = 20

Warning = 15

Info = 10

DryRun = 5

Normal = 4

Verbose = 2

Debug = 1

All = 0

class Base.Logging.**LogEntry**(*message*, *severity=<Severity.Normal: 4>*, *indent=0*, *appendLinebreak=True*)
Represents a single line log message with a severity and indentation level.

Inheritance

Members

_Log_MESSAGE_FORMAT__ = {<Severity.Debug: 1>: 'DEBUG: {message}', <Severity.Verbos

Severity
Return the log message's severity level.

Indent
Return the log message's indentation level.

Message
Return the indented log message.

IndentBy(*indent*)
Increase a log message's indentation level.

class Base.Logging.**Logger**(*logLevel*, *printToStdOut=True*)

Inheritance

Members

LogLevel
Return the currently logged minimal severity level.

BaseIndent

_Log_MESSAGE_FORMAT__ = {<Severity.Debug: 1>: '{DARK_GRAY}{message}{NOCOLOR}', <Se

Write(*entry*)

TryWrite(*entry*)

WriteFatal(*message*, *indent=0*, *appendLinebreak=True*)

WriteError(*message*, *indent=0*, *appendLinebreak=True*)

WriteWarning(*message*, *indent=0*, *appendLinebreak=True*)

WriteInfo(*message*, *indent=0*, *appendLinebreak=True*)

WriteQuiet(*message*, *indent=0*, *appendLinebreak=True*)

WriteNormal(*message*, *indent=0*, *appendLinebreak=True*)

WriteVerbose(*message*, *indent=1*, *appendLinebreak=True*)

WriteDebug(*message*, *indent=2*, *appendLinebreak=True*)

WriteDryRun(*message*, *indent=2*, *appendLinebreak=True*)

class Base.Logging.**ILogable**(*logger=None*)

A mixin class to provide local logging methods.

Inheritance

Members

Logger

Return the local logger instance.

Log(*entry*, *condition=True*)

Write an entry to the local logger.

_TryLog(**args*, *condition=True*, ***kwargs*)

LogFatal(**args*, *condition=True*, ***kwargs*)

LogError(**args*, *condition=True*, ***kwargs*)

LogWarning(**args*, *condition=True*, ***kwargs*)

LogInfo(**args*, *condition=True*, ***kwargs*)

LogQuiet(**args*, *condition=True*, ***kwargs*)

LogNormal(**args*, *condition=True*, ***kwargs*)

LogVerbose(**args*, *condition=True*, ***kwargs*)

LogDebug(**args*, *condition=True*, ***kwargs*)

LogDryRun(**args*, *condition=True*, ***kwargs*)

14.2.4 Base.Project

Classes

- *FileTypes*: Undocumented.
- *Environment*: An enumeration.
- *ToolChain*: An enumeration.
- *Tool*: An enumeration.
- *VHDLVersion*: An enumeration.

- *Project*: Undocumented.
- *FileSet*: Undocumented.
- *VHDLLibrary*: Undocumented.
- *File*: Undocumented.
- *ProjectFile*: Undocumented.
- *ConstraintFile*: Undocumented.
- *SettingsFile*: Undocumented.
- *SourceFile*: Undocumented.
- *VHDLSourceFile*: Undocumented.
- *VerilogSourceFile*: Undocumented.
- *PythonSourceFile*: Undocumented.
- *CocotbSourceFile*: Undocumented.

class Base.Project.**FileTypes**

Inheritance

Members

Extension()

_FlagsArithmeticMixin__bits

_FlagsArithmeticMixin__create_flags_instance(*bits*)

_Flags__internal_str()

classmethod bits_from_simple_str(*s*)

classmethod bits_from_str(*s*)
Converts the output of __str__ into an integer.

data

classmethod from_simple_str(*s*)
Accepts only the output of to_simple_str(). The output of __str__() is invalid as input.

classmethod from_str(*s*)
Accepts both the output of to_simple_str() and __str__().

is_disjoint(**flags_instances*)

is_member
flags.is_member is a shorthand for *flags.properties is not None*. If this property is False then this Flags instance has either zero bits or holds a combination of flag member bits. If this property is True then the bits of this Flags instance match exactly the bits associated with one of the members. This however doesn't necessarily mean that this flag instance isn't a combination of several flags because the bits of a member can be the subset of another member. For example if member0_bits=0x1 and member1_bits=0x3 then the bits of member0 are a subset of the bits of member1. If a flag instance holds the bits of member1 then Flags.is_member returns True and Flags.properties returns the properties of member1 but __len__() returns 2 and __iter__() yields both member0 and member1.

name

properties

Returns Returns None if this flag isn't an exact member of a flags class but a combination of flags,

returns an object holding the properties (e.g.: name, data, index, ...) of the flag otherwise. We don't store flag properties directly in Flags instances because this way Flags instances that are the (temporary) result of flags arithmetic don't have to maintain these fields and it also has some benefits regarding memory usage.

to_simple_str()

class Base.Project.**Environment**
An enumeration.

Inheritance

Members

Any = 0

Simulation = 1

Synthesis = 2

class Base.Project.**ToolChain**
An enumeration.

Inheritance

Members

Any = 0

Aldec_ActiveHDL = 10

Aldec_RivieraPRO = 15

Altera_Quartus = 20

Altera_ModelSim = 21

Cocotb = 30

GHDL_GTKWave = 40

Intel_Quartus = 50

Intel_ModelSim = 51

Lattice_Diamond = 60

Lattice_Synplify = 65

Mentor_ModelSim = 70

Mentor_QuestaSim = 75

Xilinx_ISE = 80

Xilinx_PlanAhead = 81

Xilinx_Vivado = 82

class Base.Project.**Tool**(*_)
An enumeration.

Inheritance

Members

Any = 0

Aldec_aSim = ('ASIM', 'Aldec Active-HDL', 'Aldec Active-HDL')

Aldec_rPro = ('RPRO', 'Aldec Riviera-PRO', 'Aldec Riviera-PRO')

Altera_Quartus_Map = ('QMAP', 'Quartus Map', 'Altera Quartus Map (quartus_map)')

Cocotb_QuestaSim = ('COCO', 'Cocotb', 'Coroutine Cosimulation Testbench (Cocotb)')

GHDL = ('GHDL', 'GHDL', 'GHDL')

GTKwave = ('GTKW', 'GTKWave', 'GTKWave')

Lattice_LSE = ('LSE', 'Lattice LSE', 'Lattice Synthesis Engine (LSE)')

Mentor_vSim = ('VSIM', 'Mentor ModelSim', 'Mentor Graphics ModelSim (vSim)')

Xilinx_iSim = ('XSIM', 'Xilinx iSim', 'Xilinx ISE Simulator (iSim)')

Xilinx_XST = ('XST', 'Xilinx XST', 'Xilinx Synthesis Tool (XST)')

Xilinx_CoreGen = ('CG', 'Xilinx CoreGen', 'Xilinx Core Generator Tool (CoreGen)')

Xilinx_xSim = ('XSIM', 'Xilinx xSim', 'Xilinx Vivado Simulator (xSim)')

Xilinx_Synth = ('VIVADO', 'Xilinx Vivado Synthesis', 'Xilinx Vivado Synthesis (synth

Xilinx_IPCatalog = ('XCI', 'Xilinx Vivado IP Catalog', 'Xilinx Vivado IP Catalog')

class Base.Project.**VHDLVersion**(*_)

An enumeration.

Inheritance

Members

Any = 0

VHDL87 = 87

VHDL93 = 93

VHDL2002 = 2002

VHDL2008 = 2008

class Base.Project.**Project**(*name*)

Inheritance

Members

Name

RootDirectory

Board

Device

Environment

ToolChain

Tool

VHDLVersion

CreateFileSet (*name*, *setDefault=True*)

AddFileSet (*fileSet*)

FileSets

DefaultFileSet

AddFile (*file*, *fileSet=None*)

AddSourceFile (*file*, *fileSet=None*)

Files (*fileType=<FileTypes(Text|ProjectFile|FileListFile|RulesFile|SourceFile|VHDLSourceFile|VerilogSourceFile|Python*
bits=0xFFFF>, *fileSet=None*)

ExtractVHDLLibrariesFromVHDLSourceFiles ()

VHDLLibraries

ExternalVHDLLibraries

AddExternalVHDLLibraries (*library*)

GetVariables ()

pprint (*indent=0*)

class Base.Project.**FileSet** (*name*, *project=None*)

Inheritance

Members

Name

Project

Files

AddFile (*file*)

AddSourceFile (*file*)

class Base.Project.**VHDLLibrary** (*name*, *project=None*)

Inheritance

Members

Name

Project

Files

AddFile (*file*)

class Base.Project.**File** (*file*, *project=None*, *fileSet=None*)

Inheritance

Members

_FileType = <FileTypes() bits=0x0000>

Project

FileSet

FileType

FileName

Path

Open()

ReadFile()

_ReadContent()

class Base.Project.**ProjectFile**(*file*, *project=None*, *fileSet=None*)

Inheritance

Members

_FileType = <FileTypes.ProjectFile bits=0x0002 data=UNDEFINED>

FileName

FileSet

FileType

Open()

Path

Project

ReadFile()

_ReadContent()

class Base.Project.**ConstraintFile**(*file*, *project=None*, *fileSet=None*)

Inheritance

Members

_FileType = <FileTypes.ConstraintFile bits=0x0200 data=UNDEFINED>

FileName

FileSet

FileType

Open()

Path

Project

ReadFile()

_ReadContent()

class Base.Project.**SettingsFile**(*file*, *project=None*, *fileSet=None*)

Inheritance

Members

_FileType = <FileTypes.SettingsFile bits=0x4000 data=UNDEFINED>

FileName

FileSet

FileType

Open()

Path

Project

ReadFile()

_ReadContent()

class Base.Project.**SourceFile**(*file*, *project=None*, *fileSet=None*)

Inheritance

Members

_FileType = <FileTypes.SourceFile bits=0x0010 data=UNDEFINED>

FileName

FileSet

FileType

Open()

Path

Project

ReadFile()

_ReadContent()

class Base.Project.**VHDLSourceFile**(*file*, *vhdlLibraryName*, *project=None*, *fileSet=None*)

Inheritance

Members

_FileType = <FileTypes.VHDLSourceFile bits=0x0020 data=UNDEFINED>

Parse()

File

FileName

FileSet

FileType

LibraryName

Open()

Path

Project

ReadFile()

_ReadContent()

class Base.Project.**VerilogSourceFile**(*file*, *project=None*, *fileSet=None*)

Inheritance

Members

File

FileName

FileSet

FileType

Open()

Path

Project

ReadFile()

_ReadContent()

_FileType = <FileTypes.VerilogSourceFile bits=0x0040 data=UNDEFINED>

class Base.Project.**PythonSourceFile**(*file*, *project=None*, *fileSet=None*)

Inheritance

Members

FileName

FileSet

FileType

Open()

Path

Project

ReadFile()

_ReadContent()

_FileType = <FileTypes.PythonSourceFile bits=0x0080 data=UNDEFINED>

class Base.Project.**CocotbSourceFile**(*file*, *project=None*, *fileSet=None*)

Inheritance

Members

File

FileName

FileSet

FileType

Open()

Path

Project

ReadFile()

_ReadContent()

_FileType = <FileTypes.CocotbSourceFile bits=0x0100 data=UNDEFINED>

14.2.5 Base.Shared

Classes

- *Shared*: Base class for Simulator and Compiler.

Functions

- *to_time()*: Convert *n* seconds to a `str` with this pattern: "{min}:{sec:02}".

class Base.Shared.**Shared**(*host: Base.IHost*, *dryRun*)
Base class for Simulator and Compiler.

Parameters

- **host** (*object*) – The hosting instance for this instance.
- **dryRun** (*bool*) – Enable dry-run mode
- **noCleanUp** (*bool*) – Don't clean up after a run.

Inheritance

Members

ENVIRONMENT = 0

TOOL_CHAIN = 0

TOOL = 0

VHDL_VERSION = 2008

Host

DryRun

VHDLVersion

PoCProject

Directories

_GetTimeDeltaSinceLastEvent()

_PrepareEnvironment()

_PrepareEnvironment_PurgeDirectory()

_PrepareEnvironment_CreatingDirectory()

_PrepareEnvironment_ChangeDirectory()
Change working directory to temporary path 'temp/<tool>'.

_Prepare()

_CreatePoCProject(*projectName*, *board*)

_AddFileListFile(*fileListFilePath*)

_GetHDLParameters(*configSectionName*)
Parse option 'HDLParameters' for Verilog Parameters / VHDL Generics.

Log(*entry*, *condition=True*)
Write an entry to the local logger.

LogDebug(**args*, *condition=True*, ***kwargs*)

LogDryRun(**args*, *condition=True*, ***kwargs*)

LogError(**args*, *condition=True*, ***kwargs*)

LogFatal(**args*, *condition=True*, ***kwargs*)

LogInfo(**args*, *condition=True*, ***kwargs*)

LogNormal(**args*, *condition=True*, ***kwargs*)

LogQuiet(**args*, *condition=True*, ***kwargs*)

LogVerbose(**args*, *condition=True*, ***kwargs*)

LogWarning(**args*, *condition=True*, ***kwargs*)

Logger
Return the local logger instance.

_TryLog(**args*, *condition=True*, ***kwargs*)

Functions

Base.Shared.**to_time**(*seconds*)
Convert *n* seconds to a str with this pattern: "{min}:{sec:02}".

Parameters **seconds** (*int*) – Number of seconds to be converted.

Return type str

Returns Returns a string formatted as #:##. E.g. "1:05"

Classes

- *IHost*: This is a type hint class (interface description) for a host instance.

class Base.**IHost**(*logger=None*)
This is a type hint class (interface description) for a host instance.

It's needed until PoC requires Python 3.6.

Inheritance

Members

Platform = 'string'

PoCConfig = <lib.ExtendedConfigParser.ExtendedConfigParser object>

SaveAndReloadPoCConfiguration()

Log(*entry*, *condition=True*)
Write an entry to the local logger.

LogDebug(**args*, *condition=True*, ***kwargs*)

LogDryRun(**args*, *condition=True*, ***kwargs*)

LogError(**args*, *condition=True*, ***kwargs*)

LogFatal(**args*, *condition=True*, ***kwargs*)

LogInfo(**args*, *condition=True*, ***kwargs*)

LogNormal(**args*, *condition=True*, ***kwargs*)

LogQuiet(**args*, *condition=True*, ***kwargs*)

LogVerbose(**args*, *condition=True*, ***kwargs*)

LogWarning(**args*, *condition=True*, ***kwargs*)

Logger
Return the local logger instance.

_TryLog(**args*, *condition=True*, ***kwargs*)

14.3 Compiler

Submodules

14.3.1 Compiler.ISECompiler

Classes

- *Compiler*: Base class for all Compiler classes.

class Compiler.ISECompiler.**Compiler**(*host*, *dryRun*, *noCleanUp*)

Inheritance

Members

TOOL_CHAIN = 80

TOOL = 0

_PrepareCompiler()
Prepare for compilation. This method forwards to `Base.Compiler.Compiler._Prepare()`, which is inherited from *Base.Shared.Shared*.

RunAll(*fqnList*, **args*, ***kwargs*)

Run(*entity*, *args*, *kwargs*)
Run a testbench.

Directories

DryRun

ENVIRONMENT = 2

Host

Log(*entry*, *condition=True*)
Write an entry to the local logger.

LogDebug(**args*, *condition=True*, ***kwargs*)

LogDryRun(**args*, *condition=True*, ***kwargs*)

LogError(**args*, *condition=True*, ***kwargs*)

LogFatal(**args*, *condition=True*, ***kwargs*)

LogInfo(**args*, *condition=True*, ***kwargs*)

LogNormal(**args*, *condition=True*, ***kwargs*)

LogQuiet(**args*, *condition=True*, ***kwargs*)

LogVerbose(**args*, *condition=True*, ***kwargs*)

LogWarning(**args*, *condition=True*, ***kwargs*)

Logger
Return the local logger instance.

NoCleanUp

PoCProject

PrintCompileReportLine(*testObject*, *indent*, *nameColumnWidth*)

PrintOverallCompileReport()

TryRun(*netlist*, **args*, ***kwargs*)
Try to run a testbench. Skip skipable exceptions by printing the error and its cause.

VHDLVersion

VHDL_VERSION = 93

_AddFileListFile(*fileListFilePath*)

_AddRulesFiles(*rulesFilePath*)

_CreatePoCProject(*projectName*, *board*)

_ExecuteCopyTasks(*tasks*, *text*)

_ExecuteDeleteTasks(*tasks*, *text*)

_ExecuteReplaceTasks(*tasks*, *text*)

_GetHDLParameters(*configSectionName*)
Parse option 'HDLParameters' for Verilog Parameters / VHDL Generics.

_GetTimeDeltaSinceLastEvent()

_ParseCopyRules(*rawList*, *copyTasks*, *text*)

_ParseDeleteRules(*rawList*, *deleteTasks*, *text*)

_ParseReplaceRules(*rawList*, *replaceTasks*, *text*)

_Prepare()

_PrepareCompilerEnvironment(*device*)

_PrepareEnvironment()

_PrepareEnvironment_ChangeDirectory()
Change working directory to temporary path 'temp/<tool>'.

_PrepareEnvironment_CreatingDirectory()

_PrepareEnvironment_PurgeDirectory()

_RunPostCopy(*netlist*)

_RunPostDelete(*netlist*)

_RunPostReplace(*netlist*)

_RunPreCopy(*netlist*)

_RunPreReplace(*netlist*)

_TryLog(**args*, *condition=True*, ***kwargs*)

_WriteSpecialSectionIntoConfig(*device*)

14.3.2 Compiler.LSECompiler

Classes

- *Compiler*: Base class for all Compiler classes.

class Compiler.LSECompiler.**Compiler**(*host*, *dryRun*, *noCleanUp*)

Inheritance

Members

TOOL_CHAIN = 60

TOOL = ('LSE', 'Lattice LSE', 'Lattice Synthesis Engine (LSE)')

_PrepareCompiler()
Prepare for compilation. This method forwards to Base.Compiler.Compiler._Prepare(), which is inherited from *Base.Shared.Shared*.

RunAll(*fqnList*, **args*, ***kwargs*)
Run a list of netlist compilations. Expand wildcards to all selected netlists.

Run(*netlist*, *board*)
Run a testbench.

_WriteLSEProjectFile(*netlist*, *board*)

_RunCompile(*netlist*, *lseArgumentFile*)

Directories

DryRun

ENVIRONMENT = 2

Host

Log(*entry*, *condition=True*)
Write an entry to the local logger.

LogDebug(**args*, *condition=True*, ***kwargs*)

LogDryRun(**args*, *condition=True*, ***kwargs*)

LogError(**args*, *condition=True*, ***kwargs*)

LogFatal(**args*, *condition=True*, ***kwargs*)

LogInfo(**args*, *condition=True*, ***kwargs*)

LogNormal(**args*, *condition=True*, ***kwargs*)

LogQuiet(**args*, *condition=True*, ***kwargs*)

LogVerbose(**args*, *condition=True*, ***kwargs*)

LogWarning(**args*, *condition=True*, ***kwargs*)

Logger
Return the local logger instance.

NoCleanUp

PoCProject

PrintCompileReportLine(*testObject*, *indent*, *nameColumnWidth*)

PrintOverallCompileReport()

TryRun(*netlist*, **args*, ***kwargs*)
Try to run a testbench. Skip skipable exceptions by printing the error and its cause.

VHDLVersion

VHDL_VERSION = 93

_AddFileListFile(*fileListFilePath*)

_AddRulesFiles(*rulesFilePath*)

_CreatePoCProject(*projectName*, *board*)

_ExecuteCopyTasks(*tasks*, *text*)

_ExecuteDeleteTasks(*tasks*, *text*)

_ExecuteReplaceTasks(*tasks*, *text*)

_GetHDLParameters(*configSectionName*)
Parse option 'HDLParameters' for Verilog Parameters / VHDL Generics.

_GetTimeDeltaSinceLastEvent()

_ParseCopyRules(*rawList*, *copyTasks*, *text*)

_ParseDeleteRules(*rawList*, *deleteTasks*, *text*)

_ParseReplaceRules(*rawList*, *replaceTasks*, *text*)

_Prepare()

_PrepareCompilerEnvironment(*device*)

_PrepareEnvironment()

_PrepareEnvironment_ChangeDirectory()
Change working directory to temporary path 'temp/<tool>'.

_PrepareEnvironment_CreatingDirectory()

_PrepareEnvironment_PurgeDirectory()

_RunPostCopy(*netlist*)

_RunPostDelete(*netlist*)

_RunPostReplace(*netlist*)

_RunPreCopy(*netlist*)

_RunPreReplace(*netlist*)

_TryLog(**args*, *condition=True*, ***kwargs*)

_WriteSpecialSectionIntoConfig(*device*)

14.3.3 Compiler.QuartusCompiler

Classes

- *Compiler*: Base class for all Compiler classes.

class Compiler.QuartusCompiler.**Compiler**(*host*, *dryRun*, *noCleanUp*)

Inheritance

Members

TOOL_CHAIN = 20

TOOL = ('QMAP', 'Quartus Map', 'Altera Quartus Map (quartus_map)')

_PrepareCompiler()
Prepare for compilation. This method forwards to Base.Compiler.Compiler._Prepare(), which is inherited from *Base.Shared.Shared*.

RunAll(*fqnList*, **args*, ***kwargs*)
Run a list of netlist compilations. Expand wildcards to all selected netlists.

Run(*netlist*, *board*)
Run a testbench.

_WriteSpecialSectionIntoConfig(*device*)

_WriteQuartusProjectFile(*netlist*, *device*)

_RunCompile(*netlist*)

Directories

DryRun

ENVIRONMENT = 2

Host

Log(*entry*, *condition=True*)
Write an entry to the local logger.

LogDebug(**args*, *condition=True*, ***kwargs*)

LogDryRun(**args*, *condition=True*, ***kwargs*)

LogError(**args*, *condition=True*, ***kwargs*)

LogFatal(**args*, *condition=True*, ***kwargs*)

LogInfo(**args*, *condition=True*, ***kwargs*)

LogNormal(**args*, *condition=True*, ***kwargs*)

LogQuiet(**args*, *condition=True*, ***kwargs*)

LogVerbose(**args*, *condition=True*, ***kwargs*)

LogWarning(**args*, *condition=True*, ***kwargs*)

Logger
Return the local logger instance.

NoCleanUp

PoCProject

PrintCompileReportLine(*testObject*, *indent*, *nameColumnWidth*)

PrintOverallCompileReport()

TryRun(*netlist*, **args*, ***kwargs*)
Try to run a testbench. Skip skipable exceptions by printing the error and its cause.

VHDLVersion

VHDL_VERSION = 93

_AddFileListFile(*fileListFilePath*)

_AddRulesFiles(*rulesFilePath*)

_CreatePoCProject(*projectName*, *board*)

_ExecuteCopyTasks(*tasks*, *text*)

_ExecuteDeleteTasks(*tasks*, *text*)

_ExecuteReplaceTasks(*tasks*, *text*)

_GetHDLParameters(*configSectionName*)
Parse option 'HDLParameters' for Verilog Parameters / VHDL Generics.

_GetTimeDeltaSinceLastEvent()

_ParseCopyRules(*rawList*, *copyTasks*, *text*)

_ParseDeleteRules(*rawList*, *deleteTasks*, *text*)

_ParseReplaceRules(*rawList*, *replaceTasks*, *text*)

_Prepare()

_PrepareCompilerEnvironment(*device*)

_PrepareEnvironment()

_PrepareEnvironment_ChangeDirectory()
Change working directory to temporary path 'temp/<tool>'.

_PrepareEnvironment_CreatingDirectory()

_PrepareEnvironment_PurgeDirectory()

_RunPostCopy(*netlist*)

_RunPostDelete(*netlist*)

_RunPostReplace(*netlist*)

_RunPreCopy(*netlist*)

_RunPreReplace(*netlist*)

_TryLog(**args*, *condition=True*, ***kwargs*)

14.3.4 Compiler.VivadoCompiler

Classes

- *Compiler*: Base class for all Compiler classes.

class Compiler.VivadoCompiler.**Compiler**(*host*, *dryRun*, *noCleanUp*)

Inheritance

Members

TOOL_CHAIN = 82

TOOL = ('VIVADO', 'Xilinx Vivado Synthesis', 'Xilinx Vivado Synthesis (synth)')

_PrepareCompiler()
Prepare for compilation. This method forwards to `Base.Compiler.Compiler._Prepare()`, which is inherited from *Base.Shared.Shared*.

RunAll(*fqnList*, **args*, ***kwargs*)
Run a list of netlist compilations. Expand wildcards to all selected netlists.

Run(*netlist*, *board*)
Run a testbench.

_WriteSpecialSectionIntoConfig(*device*)

_RunCompile(*netlist*)

_WriteTclFile(*netlist*, *device*)

Directories

DryRun

ENVIRONMENT = 2

Host

Log(*entry*, *condition=True*)
Write an entry to the local logger.

LogDebug(**args*, *condition=True*, ***kwargs*)

LogDryRun(**args*, *condition=True*, ***kwargs*)

LogError(**args*, *condition=True*, ***kwargs*)

LogFatal(**args*, *condition=True*, ***kwargs*)

LogInfo(**args*, *condition=True*, ***kwargs*)

LogNormal(**args*, *condition=True*, ***kwargs*)

LogQuiet(**args*, *condition=True*, ***kwargs*)

LogVerbose(**args*, *condition=True*, ***kwargs*)

LogWarning(**args*, *condition=True*, ***kwargs*)

Logger
Return the local logger instance.

NoCleanUp

PoCProject

PrintCompileReportLine(*testObject*, *indent*, *nameColumnWidth*)

PrintOverallCompileReport()

TryRun(*netlist*, **args*, ***kwargs*)
Try to run a testbench. Skip skipable exceptions by printing the error and its cause.

VHDLVersion

VHDL_VERSION = 93

_AddFileListFile(*fileListFilePath*)

_AddRulesFiles(*rulesFilePath*)

_CreatePoCProject(*projectName*, *board*)

_ExecuteCopyTasks(*tasks*, *text*)

_ExecuteDeleteTasks(*tasks*, *text*)

_ExecuteReplaceTasks(*tasks*, *text*)

_GetHDLParameters(*configSectionName*)
Parse option 'HDLParameters' for Verilog Parameters / VHDL Generics.

_GetTimeDeltaSinceLastEvent()

_ParseCopyRules(*rawList*, *copyTasks*, *text*)

_ParseDeleteRules(*rawList*, *deleteTasks*, *text*)

_ParseReplaceRules(*rawList*, *replaceTasks*, *text*)

_Prepare()

_PrepareCompilerEnvironment(*device*)

_PrepareEnvironment()

_PrepareEnvironment_ChangeDirectory()
Change working directory to temporary path 'temp/<tool>'.

_PrepareEnvironment_CreatingDirectory()

_PrepareEnvironment_PurgeDirectory()

_RunPostCopy(*netlist*)

_RunPostDelete(*netlist*)

_RunPostReplace(*netlist*)

_RunPreCopy(*netlist*)

_RunPreReplace(*netlist*)

_TryLog(**args*, *condition=True*, ***kwargs*)

14.3.5 Compiler.XCICompiler

Classes

- *Compiler*: Base class for all Compiler classes.

class Compiler.XCICompiler.**Compiler**(*host*, *dryRun*, *noCleanUp*)

Inheritance

Members

TOOL_CHAIN = 82

TOOL = ('XCI', 'Xilinx Vivado IP Catalog', 'Xilinx Vivado IP Catalog')

_PrepareCompiler()
Prepare for compilation. This method forwards to Base.Compiler.Compiler._Prepare(), which is inherited from *Base.Shared.Shared*.

RunAll(*fqnList*, **args*, ***kwargs*)
Run a list of netlist compilations. Expand wildcards to all selected netlists.

Run(*netlist*, *board*)
Run a testbench.

_WriteSpecialSectionIntoConfig(*device*)

_RunCompile(*netlist*, *device*)

_WriteTclFile(*netlist*, *device*)

Directories

DryRun

ENVIRONMENT = 2

Host

Log(*entry*, *condition=True*)
Write an entry to the local logger.

LogDebug(**args*, *condition=True*, ***kwargs*)

LogDryRun(**args*, *condition=True*, ***kwargs*)

LogError(**args*, *condition=True*, ***kwargs*)

LogFatal(**args*, *condition=True*, ***kwargs*)

LogInfo(**args*, *condition=True*, ***kwargs*)

LogNormal(**args*, *condition=True*, ***kwargs*)

LogQuiet(**args*, *condition=True*, ***kwargs*)

LogVerbose(**args*, *condition=True*, ***kwargs*)

LogWarning(**args*, *condition=True*, ***kwargs*)

Logger
Return the local logger instance.

NoCleanUp

PoCProject

PrintCompileReportLine(*testObject*, *indent*, *nameColumnWidth*)

PrintOverallCompileReport()

TryRun(*netlist*, **args*, ***kwargs*)
Try to run a testbench. Skip skipable exceptions by printing the error and its cause.

VHDLVersion

VHDL_VERSION = 93

_AddFileListFile(*fileListFilePath*)

_AddRulesFiles(*rulesFilePath*)

_CreatePoCProject(*projectName*, *board*)

_ExecuteCopyTasks(*tasks*, *text*)

_ExecuteDeleteTasks(*tasks*, *text*)

_ExecuteReplaceTasks(*tasks*, *text*)

_GetHDLParameters(*configSectionName*)
Parse option 'HDLParameters' for Verilog Parameters / VHDL Generics.

_GetTimeDeltaSinceLastEvent()

_ParseCopyRules(*rawList*, *copyTasks*, *text*)

_ParseDeleteRules(*rawList*, *deleteTasks*, *text*)

_ParseReplaceRules(*rawList*, *replaceTasks*, *text*)

_Prepare()

_PrepareCompilerEnvironment(*device*)

_PrepareEnvironment()

_PrepareEnvironment_ChangeDirectory()
Change working directory to temporary path 'temp/<tool>'.

_PrepareEnvironment_CreatingDirectory()

_PrepareEnvironment_PurgeDirectory()

_RunPostCopy(*netlist*)

_RunPostDelete(*netlist*)

_RunPostReplace(*netlist*)

_RunPreCopy(*netlist*)

_RunPreReplace(*netlist*)

_TryLog(**args*, *condition=True*, ***kwargs*)

14.3.6 Compiler.XCOCompiler

Classes

- *Compiler*: Base class for all Compiler classes.

class Compiler.XCOCompiler.**Compiler**(*host*, *dryRun*, *noCleanUp*)

Inheritance

Members

TOOL_CHAIN = 80

TOOL = ('CG', 'Xilinx CoreGen', 'Xilinx Core Generator Tool (CoreGen)')

_PrepareCompiler()
Prepare for compilation. This method forwards to Base.Compiler.Compiler._Prepare(), which is inherited from *Base.Shared.Shared*.

RunAll(*fqnList*, **args*, ***kwargs*)
Run a list of netlist compilations. Expand wildcards to all selected netlists.

Run(*netlist*, *board*)
Run a testbench.

_WriteSpecialSectionIntoConfig(*device*)

_RunCompile(*netlist*, *device*)

Directories

DryRun

ENVIRONMENT = 2

Host

Log(*entry*, *condition=True*)
Write an entry to the local logger.

LogDebug(**args*, *condition=True*, ***kwargs*)

LogDryRun(**args*, *condition=True*, ***kwargs*)

LogError(**args*, *condition=True*, ***kwargs*)

LogFatal(**args*, *condition=True*, ***kwargs*)

LogInfo(**args*, *condition=True*, ***kwargs*)

LogNormal(**args*, *condition=True*, ***kwargs*)

LogQuiet(**args*, *condition=True*, ***kwargs*)

LogVerbose(**args*, *condition=True*, ***kwargs*)

LogWarning(**args*, *condition=True*, ***kwargs*)

Logger
Return the local logger instance.

NoCleanUp

PoCProject

PrintCompileReportLine(*testObject*, *indent*, *nameColumnWidth*)

PrintOverallCompileReport()

TryRun(*netlist*, **args*, ***kwargs*)
Try to run a testbench. Skip skipable exceptions by printing the error and its cause.

VHDLVersion

VHDL_VERSION = 93

_AddFileListFile(*fileListFilePath*)

_AddRulesFiles(*rulesFilePath*)

_CreatePoCProject(*projectName*, *board*)

_ExecuteCopyTasks(*tasks*, *text*)

_ExecuteDeleteTasks(*tasks*, *text*)

_ExecuteReplaceTasks(*tasks*, *text*)

_GetHDLParameters(*configSectionName*)
Parse option 'HDLParameters' for Verilog Parameters / VHDL Generics.

_GetTimeDeltaSinceLastEvent()

_ParseCopyRules(*rawList*, *copyTasks*, *text*)

_ParseDeleteRules(*rawList*, *deleteTasks*, *text*)

_ParseReplaceRules(*rawList*, *replaceTasks*, *text*)

_Prepare()

_PrepareCompilerEnvironment(*device*)

_PrepareEnvironment()

_PrepareEnvironment_ChangeDirectory()
Change working directory to temporary path 'temp/<tool>'.

_PrepareEnvironment_CreatingDirectory()

_PrepareEnvironment_PurgeDirectory()

_RunPostCopy(*netlist*)

_RunPostDelete(*netlist*)

_RunPostReplace(*netlist*)

_RunPreCopy(*netlist*)

_RunPreReplace(*netlist*)

_TryLog(**args*, *condition=True*, ***kwargs*)

14.3.7 Compiler.XSTCompiler

Classes

- *Compiler*: Base class for all Compiler classes.

class Compiler.XSTCompiler.**Compiler**(*host*, *dryRun*, *noCleanUp*)

Inheritance

Members

TOOL_CHAIN = 80

TOOL = ('XST', 'Xilinx XST', 'Xilinx Synthesis Tool (XST)')

_PrepareCompiler()
Prepare for compilation. This method forwards to Base.Compiler.Compiler._Prepare(), which is inherited from *Base.Shared.Shared*.

RunAll(*fqnList*, **args*, ***kwargs*)
Run a list of netlist compilations. Expand wildcards to all selected netlists.

Run(*netlist*, *board*)
Run a testbench.

_WriteSpecialSectionIntoConfig(*device*)

_RunCompile(*netlist*)

_WriteXstOptionsFile(*netlist*, *device*)

Directories

DryRun

ENVIRONMENT = 2

Host

Log(*entry*, *condition=True*)
Write an entry to the local logger.

LogDebug(**args*, *condition=True*, ***kwargs*)

LogDryRun(**args*, *condition=True*, ***kwargs*)

LogError(**args*, *condition=True*, ***kwargs*)

LogFatal(**args*, *condition=True*, ***kwargs*)

LogInfo(**args*, *condition=True*, ***kwargs*)

LogNormal(**args*, *condition=True*, ***kwargs*)

LogQuiet(**args*, *condition=True*, ***kwargs*)

LogVerbose(**args*, *condition=True*, ***kwargs*)

LogWarning(**args*, *condition=True*, ***kwargs*)

Logger
Return the local logger instance.

NoCleanUp

PoCProject

PrintCompileReportLine(*testObject*, *indent*, *nameColumnWidth*)

PrintOverallCompileReport()

TryRun(*netlist*, **args*, ***kwargs*)
Try to run a testbench. Skip skipable exceptions by printing the error and its cause.

VHDLVersion

VHDL_VERSION = 93

_AddFileListFile(*fileListFilePath*)

_AddRulesFiles(*rulesFilePath*)

_CreatePoCProject(*projectName*, *board*)

_ExecuteCopyTasks(*tasks*, *text*)

_ExecuteDeleteTasks(*tasks*, *text*)

_ExecuteReplaceTasks(*tasks*, *text*)

_GenerateXilinxProjectFileContent(*tool*, *vhdlVersion=93*)

_GetHDLParameters(*configSectionName*)
Parse option 'HDLParameters' for Verilog Parameters / VHDL Generics.

_GetTimeDeltaSinceLastEvent()

_ParseCopyRules(*rawList*, *copyTasks*, *text*)

_ParseDeleteRules(*rawList*, *deleteTasks*, *text*)

_ParseReplaceRules(*rawList*, *replaceTasks*, *text*)

_Prepare()

_PrepareCompilerEnvironment(*device*)

_PrepareEnvironment()

_PrepareEnvironment_ChangeDirectory()
Change working directory to temporary path 'temp/<tool>'.

_PrepareEnvironment_CreatingDirectory()

_PrepareEnvironment_PurgeDirectory()

_RunPostCopy(*netlist*)

_RunPostDelete(*netlist*)

_RunPostReplace(*netlist*)

_RunPreCopy(*netlist*)

_RunPreReplace(*netlist*)

_TryLog(**args*, *condition=True*, ***kwargs*)

_WriteXilinxProjectFile(*projectFilePath*, *tool*, *vhdlVersion=93*)

Exceptions

- *CompilerException*: Base class for all CompilerException classes. It is raised while running
- *SkipableCompilerException*: SkipableCompilerException is a *CompilerException*, which

Classes

- *CopyTask*: This class represents a 'copy task' and inherits the partial class
- *DeleteTask*: This class represents a 'delete task' and inherits the partial class
- *ReplaceTask*: This class represents a 'replace task' and inherits the partial class
- *AppendLineTask*: This class represents a 'append line task' and inherits the partial class

- *CompileState*: Compile state enumeration.
- *CompileResult*: Compilation result enumeration.
- *Compiler*: Base class for all Compiler classes.

exception Compiler.**CompilerException**(*message=''*)
Base class for all CompilerException classes. It is raised while running compiler (synthesis) tasks in PoC.

Inheritance

Members

__init__(*message=''*)
Exception initializer

Parameters **message** (*str*) – The exception message.

__str__()
Returns the exception's message text.

args

exception Compiler.**SkipableCompilerException**(*message=''*)
SkipableCompilerException is a *CompilerException*, which can be skipped.

Inheritance

Members

__init__(*message=''*)
Exception initializer

Parameters **message** (*str*) – The exception message.

__str__()
Returns the exception's message text.

args

class Compiler.**CopyTask**(*sourcePath*, *destinationPath*)
This class represents a 'copy task' and inherits the partial class *CopyRuleMixIn*.

Inheritance

Members

DestinationPath

SourcePath

class Compiler.**DeleteTask**(*filePath*)
This class represents a 'delete task' and inherits the partial class *DeleteRuleMixIn*.

Inheritance

Members

FilePath

class Compiler.**ReplaceTask**(*filePath*, *searchPattern*, *replacePattern*, *multiLine*, *dotAll*, *caseInSensitive*)

This class represents a 'replace task' and inherits the partial class *ReplaceRuleMixIn*.

Inheritance

Members

FilePath

RegExpOption_CaseInsensitive

RegExpOption_DotAll

RegExpOption_MultiLine

ReplacePattern

SearchPattern

class Compiler.**AppendLineTask**(*filePath*, *appendPattern*)

This class represents a 'append line task' and inherits the partial class *AppendLineRuleMixIn*.

Inheritance

Members

AppendPattern

FilePath

class Compiler.**CompileState**

Compile state enumeration.

Inheritance

Members

Prepare = 0

PreCopy = 10

PrePatch = 11

Compile = 50

PostCopy = 90

PostPatch = 91

PostDelete = 92

CleanUp = 99

class Compiler.**CompileResult**

Compilation result enumeration.

Inheritance

Members

NotRun = 0

Error = 1

Failed = 2

Success = 3

class Compiler.**Compiler**(*host: Base.IHost*, *dryRun*, *noCleanUp*)
Base class for all Compiler classes.

Inheritance

Members

ENVIRONMENT = 2

VHDL_VERSION = 93

__init__(*host: Base.IHost*, *dryRun*, *noCleanUp*)
Class initializer

Parameters

- **host** (*object*) – The hosting instance for this instance.
- **dryRun** (*bool*) – Enable dry-run mode
- **noCleanUp** (*bool*) – Don't clean up after a run.

NoCleanUp

_PrepareCompiler()
Prepare for compilation. This method forwards to Base.Compiler.Compiler._Prepare(), which is inherited from *Base.Shared.Shared*.

TryRun(*netlist*, **args*, ***kwargs*)
Try to run a testbench. Skip skipable exceptions by printing the error and its cause.

Run(*netlist*, *board*)
Run a testbench.

_PrepareCompilerEnvironment(*device*)

_WriteSpecialSectionIntoConfig(*device*)

_AddRulesFiles(*rulesFilePath*)

_RunPreCopy(*netlist*)

_RunPostCopy(*netlist*)

_ParseCopyRules(*rawList*, *copyTasks*, *text*)

_ExecuteCopyTasks(*tasks*, *text*)

_RunPostDelete(*netlist*)

_ParseDeleteRules(*rawList*, *deleteTasks*, *text*)

_ExecuteDeleteTasks(*tasks*, *text*)

_RunPreReplace(*netlist*)

_RunPostReplace(*netlist*)

_ParseReplaceRules(*rawList*, *replaceTasks*, *text*)

_ExecuteReplaceTasks(*tasks*, *text*)

PrintOverallCompileReport()

PrintCompileReportLine(*testObject*, *indent*, *nameColumnWidth*)

Directories

DryRun

Host

Log(*entry*, *condition=True*)
Write an entry to the local logger.

LogDebug(**args*, *condition=True*, ***kwargs*)

LogDryRun(**args*, *condition=True*, ***kwargs*)

LogError(**args*, *condition=True*, ***kwargs*)

LogFatal(**args*, *condition=True*, ***kwargs*)

LogInfo(**args*, *condition=True*, ***kwargs*)

LogNormal(**args*, *condition=True*, ***kwargs*)

LogQuiet(**args*, *condition=True*, ***kwargs*)

LogVerbose(**args*, *condition=True*, ***kwargs*)

LogWarning(**args*, *condition=True*, ***kwargs*)

Logger
Return the local logger instance.

PoCProject

TOOL = 0

TOOL_CHAIN = 0

VHDLVersion

_AddFileListFile(*fileListFilePath*)

_CreatePoCProject(*projectName*, *board*)

_GetHDLParameters(*configSectionName*)
Parse option 'HDLParameters' for Verilog Parameters / VHDL Generics.

_GetTimeDeltaSinceLastEvent()

_Prepare()

_PrepareEnvironment()

_PrepareEnvironment_ChangeDirectory()
Change working directory to temporary path 'temp/<tool>'.

_PrepareEnvironment_CreatingDirectory()

_PrepareEnvironment_PurgeDirectory()

_TryLog(**args*, *condition=True*, ***kwargs*)

14.4 DataBase

Submodules

14.4.1 DataBase.Config

Classes

- *BaseEnum*: An enumeration.
- *Vendors*: An enumeration.
- *Families*: Base enum for all Family enums.
- *GenericFamilies*: Enumeration of all generic families.
- *AlteraFamilies*: Enumeration of all Altera families.
- *LatticeFamilies*: Enumeration of all Lattice families.
- *XilinxFamilies*: Enumeration of all Xilinx families.
- *Devices*: Base enum for all Device enums.
- *GenericDevices*: Enumeration of all generic devices.
- *AlteraDevices*: Enumeration of all Altera devices.
- *LatticeDevices*: Enumeration of all Lattice devices.
- *XilinxDevices*: Enumeration of all Xilinx devices.
- *SubTypes*: Base enum for all SubType enums.
- *GenericSubTypes*: Enumeration of all generic device subtype.
- *AlteraSubTypes*: Enumeration of all Altera device subtype.
- *LatticeSubTypes*: Enumeration of all Lattice device subtype.
- *XilinxSubTypes*: Enumeration of all Xilinx device subtype.
- *Packages*: An enumeration.
- *Device*: Undocumented.
- *Board*: Undocumented.

class DataBase.Config.**BaseEnum**
An enumeration.

Inheritance

Members

class DataBase.Config.**Vendors**
An enumeration.

Inheritance

Members

Unknown = 0

Generic = 1

Altera = 2

Lattice = 3

MicroSemi = 4

Xilinx = 5

class DataBase.Config.**Families**
Base enum for all Family enums.

Inheritance

Members

class DataBase.Config.**GenericFamilies**
Enumeration of all generic families.

Inheritance

Members

Unknown = None

Generic = 'g'

class DataBase.Config.**AlteraFamilies**
Enumeration of all Altera families.

Inheritance

Members

Max = 'm'

Cyclone = 'c'

Arria = 'a'

Stratix = 's'

class DataBase.Config.**LatticeFamilies**
Enumeration of all Lattice families.

Inheritance

Members

ECP = 'lfe'

class DataBase.Config.**XilinxFamilies**
Enumeration of all Xilinx families.

Inheritance

Members

Spartan = 's'

Artix = 'a'

Kintex = 'k'

Virtex = 'v'

Zynq = 'z'

class DataBase.Config.**Devices**
Base enum for all Device enums.

Inheritance

Members

class DataBase.Config.**GenericDevices**
Enumeration of all generic devices.

Inheritance

Members

Unknown = 0

Generic = 1

class DataBase.Config.**AlteraDevices**
Enumeration of all Altera devices.

Inheritance

Members

Max2 = 100

Max4 = 101

Max5 = 102

Max10 = 103

Cyclone3 = 110

Cyclone4 = 111

Cyclone5 = 112

Arria2 = 120

Arria5 = 121

Stratix2 = 130

Stratix4 = 131

Stratix5 = 132

Stratix10 = 133

class DataBase.Config.**LatticeDevices**
Enumeration of all Lattice devices.

Inheritance

Members

iCE40 = 200

MachXO = 210

MachXO2 = 211

MachXO3 = 212

ECP2 = 220

ECP3 = 221

ECP5 = 222

class DataBase.Config.**XilinxDevices**
Enumeration of all Xilinx devices.

Inheritance

Members

Spartan3 = 310

Spartan6 = 311

Artix7 = 320

Kintex7 = 330

KintexUltraScale = 331

KintexUltraScalePlus = 332

Virtex2 = 340

Virtex4 = 341

Virtex5 = 342

Virtex6 = 343

Virtex7 = 344

VirtexUltraScale = 345

VirtexUltraScalePlus = 346

Zynq7000 = 350

class DataBase.Config.**SubTypes**
Base enum for all SubType enums.

Inheritance

Members

class DataBase.Config.**GenericSubTypes**
Enumeration of all generic device subtype.

Inheritance

Members

Unknown = None

Generic = 1

NoSubType = ('', '')

class DataBase.Config.**AlteraSubTypes**
Enumeration of all Altera device subtype.

Inheritance

Members

NoSubType = ('', '')

LS = ('ls', '')

E = ('e', '')

GS = ('gs', '')

GX = ('gx', '')

GT = ('gt', '')

GZ = ('gz', '')

SX = ('sx', '')

ST = ('st', '')

class DataBase.Config.**LatticeSubTypes**
Enumeration of all Lattice device subtype.

Inheritance

Members

NoSubType = ('', '')

U = ('u', '')

UM = ('um', '')

class DataBase.Config.**XilinxSubTypes**
Enumeration of all Xilinx device subtype.

Inheritance

Members

NoSubType = ('', '')

DA = ('d', 'a')

E = ('', 'e')

AN = ('', 'an')

```
X = ('x', '')
T = ('', 't')
XT = ('x', 't')
HT = ('h', 't')
LX = ('lx', '')
SXT = ('sx', 't')
LXT = ('lx', 't')
TXT = ('tx', 't')
FXT = ('fx', 't')
CXT = ('cx', 't')
HXT = ('hx', 't')
```

class DataBase.Config.**Packages**
An enumeration.

Inheritance

Members

```
Unknown = 0
Generic = 1
TQG = 10
CLG = 20
CPG = 21
CSG = 22
CABGA = 25
FBG = 30
FF = 31
FFG = 32
FG = 33
FGG = 34
FLG = 35
FT = 36
FTG = 37
RB = 40
RBG = 41
RF = 42
RS = 43
E = 50
Q = 51
F = 52
```

U = 53

M = 54

class DataBase.Config.**Device**(*deviceString*)

Inheritance

Members

_DecodeGeneric()

_DecodeAltera(*deviceString*)

_DecodeLatticeICE(*deviceString*)

_DecodeLatticeLCM(*deviceString*)

_DecodeLatticeLFE(*deviceString*)

_DecodeLatticeECP3(*deviceString*)

_DecodeLatticeECP5(*deviceString*)

_DecodeXilinx(*deviceString*)

Vendor

Family

Device

Generation

Number

SpeedGrade

PinCount

Package

Name

ShortName

FullName

FullName2

FamilyName

Series

GetVariables()

class DataBase.Config.**Board**(*host*, *boardName=None*, *device=None*)

Inheritance

Members

Name

Device

GetVariables()

14.4.2 DataBase.Entity

Classes

- *EntityTypes*: An enumeration.
- *BaseFlags*: Undocumented.
- *TestbenchKind*: Undocumented.
- *NetlistKind*: Undocumented.
- *NamespaceRoot*: Undocumented.
- *Visibility*: An enumeration.
- *PathElement*: Undocumented.
- *Namespace*: Undocumented.
- *Library*: Undocumented.
- *WildCard*: Undocumented.
- *StarWildCard*: Undocumented.
- *AskWildCard*: Undocumented.
- *IPCore*: Undocumented.
- *LazyPathElement*: Undocumented.
- *Testbench*: Undocumented.
- *VHDLTestbench*: Undocumented.
- *CocoTestbench*: Undocumented.
- *Netlist*: Undocumented.
- *XstNetlist*: Undocumented.
- *QuartusNetlist*: Undocumented.
- *LatticeNetlist*: Undocumented.
- *CoreGeneratorNetlist*: Undocumented.
- *VivadoNetlist*: Undocumented.
- *FQN*: Undocumented.

Functions

- *_PoCEntityTypes_parser()*: Undocumented.

class DataBase.Entity.**EntityTypes**
An enumeration.

Inheritance

Members

Unknown = 0

Source = 1

Testbench = 2

NetList = 3

class DataBase.Entity.**BaseFlags**

Inheritance

Members

_FlagsArithmeticMixin__bits

_FlagsArithmeticMixin__create_flags_instance(*bits*)

_Flags__internal_str()

classmethod bits_from_simple_str(*s*)

classmethod bits_from_str(*s*)
Converts the output of __str__ into an integer.

data

classmethod from_simple_str(*s*)
Accepts only the output of to_simple_str(). The output of __str__() is invalid as input.

classmethod from_str(*s*)
Accepts both the output of to_simple_str() and __str__().

is_disjoint(**flags_instances*)

is_member
flags.is_member is a shorthand for *flags.properties is not None*. If this property is False then this Flags instance has either zero bits or holds a combination of flag member bits. If this property is True then the bits of this Flags instance match exactly the bits associated with one of the members. This however doesn't necessarily mean that this flag instance isn't a combination of several flags because the bits of a member can be the subset of another member. For example if member0_bits=0x1 and member1_bits=0x3 then the bits of member0 are a subset of the bits of member1. If a flag instance holds the bits of member1 then Flags.is_member returns True and Flags.properties returns the properties of member1 but __len__() returns 2 and __iter__() yields both member0 and member1.

name

properties

> **Returns** Returns None if this flag isn't an exact member of a flags class but a combination of flags,

returns an object holding the properties (e.g.: name, data, index, ...) of the flag otherwise. We don't store flag properties directly in Flags instances because this way Flags instances that are the (temporary) result of flags arithmetic don't have to maintain these fields and it also has some benefits regarding memory usage.

to_simple_str()

class DataBase.Entity.**TestbenchKind**

Inheritance

Members

_FlagsArithmeticMixin__bits

_FlagsArithmeticMixin__create_flags_instance(*bits*)

_Flags__internal_str()

classmethod bits_from_simple_str(*s*)

classmethod bits_from_str(*s*)
Converts the output of __str__ into an integer.

data

classmethod from_simple_str(*s*)
Accepts only the output of to_simple_str(). The output of __str__() is invalid as input.

classmethod from_str(*s*)
Accepts both the output of to_simple_str() and __str__().

is_disjoint(**flags_instances*)

is_member
flags.is_member is a shorthand for *flags.properties is not None*. If this property is False then this Flags instance has either zero bits or holds a combination of flag member bits. If this property is True then the bits of this Flags instance match exactly the bits associated with one of the members. This however doesn't necessarily mean that this flag instance isn't a combination of several flags because the bits of a member can be the subset of another member. For example if member0_bits=0x1 and member1_bits=0x3 then the bits of member0 are a subset of the bits of member1. If a flag instance holds the bits of member1 then Flags.is_member returns True and Flags.properties returns the properties of member1 but __len__() returns 2 and __iter__() yields both member0 and member1.

name

properties

Returns Returns None if this flag isn't an exact member of a flags class but a combination of flags,

returns an object holding the properties (e.g.: name, data, index, ...) of the flag otherwise. We don't store flag properties directly in Flags instances because this way Flags instances that are the (temporary) result of flags arithmetic don't have to maintain these fields and it also has some benefits regarding memory usage.

to_simple_str()

class DataBase.Entity.**NetlistKind**

Inheritance

Members

_FlagsArithmeticMixin__bits

_FlagsArithmeticMixin__create_flags_instance(*bits*)

_Flags__internal_str()

classmethod bits_from_simple_str(*s*)

classmethod bits_from_str(*s*)
Converts the output of __str__ into an integer.

data

classmethod from_simple_str(*s*)
Accepts only the output of to_simple_str(). The output of __str__() is invalid as input.

classmethod from_str(*s*)
Accepts both the output of to_simple_str() and __str__().

is_disjoint(**flags_instances*)

is_member
flags.is_member is a shorthand for *flags.properties is not None*. If this property is False then this Flags instance has either zero bits or holds a combination of flag member bits. If this property is True then the bits of this Flags instance match exactly the bits associated with one of the members. This however doesn't necessarily mean that this flag instance isn't a combination of several flags because the

bits of a member can be the subset of another member. For example if member0_bits=0x1 and member1_bits=0x3 then the bits of member0 are a subset of the bits of member1. If a flag instance holds the bits of member1 then Flags.is_member returns True and Flags.properties returns the properties of member1 but __len__() returns 2 and __iter__() yields both member0 and member1.

name

properties

Returns Returns None if this flag isn't an exact member of a flags class but a combination of flags,

returns an object holding the properties (e.g.: name, data, index, ...) of the flag otherwise. We don't store flag properties directly in Flags instances because this way Flags instances that are the (temporary) result of flags arithmetic don't have to maintain these fields and it also has some benefits regarding memory usage.

to_simple_str()

class DataBase.Entity.**NamespaceRoot**(*host*)

Inheritance

Members

Libraries

LibraryNames

GetLibraries()

GetLibraryNames()

AddLibrary(*libraryName*, *libraryPrefix*)

_NamespaceRoot__POCRoot_Name = 'PoC'

_NamespaceRoot__POCRoot_SectionName = 'PoC'

class DataBase.Entity.**Visibility**

An enumeration.

Inheritance

Members

Unknown = 0

Private = 1

Public = 2

class DataBase.Entity.**PathElement**(*host*, *name*, *configSectionName*, *parent*)

Inheritance

Members

Name

Parent

ConfigSectionName

ConfigSection

Level

Visibility

IsVisible

Path

_Load()

class DataBase.Entity.**Namespace**(*host*, *name*, *configSectionName*, *parent*)

Inheritance

Members

_Load()

Namespaces

NamespaceNames

Entities

EntityNames

GetNamespaces()

GetNamespaceNames()

GetEntities()

GetEntityNames()

GetAllEntities()

pprint(*indent=0*)

ConfigSection

ConfigSectionName

IsVisible

Level

Name

Parent

Path

Visibility

class DataBase.Entity.**Library**(*host*, *name*, *configSectionName*, *parent*)

Inheritance

Members

Level

ConfigSection

ConfigSectionName

Entities

EntityNames

GetAllEntities()

GetEntities()

GetEntityNames()

GetNamespaceNames()

GetNamespaces()

IsVisible

Name

NamespaceNames

Namespaces

Parent

Path

Visibility

_Load()

pprint(*indent=0*)

class DataBase.Entity.**WildCard**(*host*, *name*, *configSectionName*, *parent*)

Inheritance

Members

GetEntities()

GetTestbenches(*kind=<TestbenchKind(VHDLTestbench|CocoTestbench) bits=0x0003>*)

GetVHDLTestbenches()

GetCocoTestbenches()

GetNetlists(*kind=<NetlistKind(LatticeNetlist|QuartusNetlist|XstNetlist|CoreGeneratorNetlist|VivadoNetlist) bits=0x001F>*)

GetLatticeNetlists()

GetQuartusNetlists()

GetXSTNetlists()

GetCoreGenNetlists()

GetVivadoNetlists()

Testbenches

VHDLTestbenches

CocoTestbenches

Netlists

LatticeNetlists

QuartusNetlists

XSTNetlists

CoreGenNetlists

VivadoNetlists

ConfigSection

ConfigSectionName

IsVisible

Level

Name

Parent

Path

Visibility

_Load()

class DataBase.Entity.**StarWildCard**(*host*, *name*, *configSectionName*, *parent*)

Inheritance

Members

_Load()

GetEntities()

CocoTestbenches

ConfigSection

ConfigSectionName

CoreGenNetlists

GetCocoTestbenches()

GetCoreGenNetlists()

GetLatticeNetlists()

GetNetlists(*kind=<NetlistKind(LatticeNetlist|QuartusNetlist|XstNetlist|CoreGeneratorNetlist|VivadoNetlist) bits=0x001F>*)

GetQuartusNetlists()

GetTestbenches(*kind=<TestbenchKind(VHDLTestbench|CocoTestbench) bits=0x0003>*)

GetVHDLTestbenches()

GetVivadoNetlists()

GetXSTNetlists()

IsVisible

LatticeNetlists

Level

Name

Netlists

Parent

Path

QuartusNetlists

Testbenches

VHDLTestbenches

Visibility

VivadoNetlists

XSTNetlists

class DataBase.Entity.**AskWildCard**(*host*, *name*, *configSectionName*, *parent*)

Inheritance

Members

_Load()

GetEntities()

CocoTestbenches

ConfigSection

ConfigSectionName

CoreGenNetlists

GetCocoTestbenches()

GetCoreGenNetlists()

GetLatticeNetlists()

GetNetlists(*kind=<NetlistKind(LatticeNetlist|QuartusNetlist|XstNetlist|CoreGeneratorNetlist|VivadoNetlist) bits=0x001F>*)

GetQuartusNetlists()

GetTestbenches(*kind=<TestbenchKind(VHDLTestbench|CocoTestbench) bits=0x0003>*)

GetVHDLTestbenches()

GetVivadoNetlists()

GetXSTNetlists()

IsVisible

LatticeNetlists

Level

Name

Netlists

Parent

Path

QuartusNetlists

Testbenches

VHDLTestbenches

Visibility

VivadoNetlists

XSTNetlists

class DataBase.Entity.**IPCore**(*host*, *name*, *configSectionName*, *parent*)

Inheritance

Members

Dependencies

VHDLTestbench

CocoTestbench

GetTestbenches(*kind=<TestbenchKind(VHDLTestbench|CocoTestbench) bits=0x0003>*)

LatticeNetlist

QuartusNetlist

XSTNetlist

CGNetlist

VivadoNetlist

GetNetlists(*kind=<NetlistKind(LatticeNetlist|QuartusNetlist|XstNetlist|CoreGeneratorNetlist|VivadoNetlist) bits=0x001F>*)

_Load()

pprint(*indent=0*)

ConfigSection

ConfigSectionName

IsVisible

Level

Name

Parent

Path

Visibility

class DataBase.Entity.**LazyPathElement**(*host*, *name*, *configSectionName*, *parent*)

Inheritance

Members

Kind

ConfigSection

ConfigSectionName

IsVisible

LazyLoadable_IsLoaded

Level

Name

Parent

Path

Visibility

_LazyLoadable_Load()

_Load()

class DataBase.Entity.**Testbench**(*host*, *name*, *configSectionName*, *parent*)

Inheritance

Members

ModuleName

FilesFile

Result

_LazyLoadable_Load()

pprint(*indent*)

ConfigSection

ConfigSectionName

IsVisible

Kind

LazyLoadable_IsLoaded

Level

Name

Parent

Path

Visibility

_Load()

class DataBase.Entity.**VHDLTestbench**(*host*, *name*, *configSectionName*, *parent*)

Inheritance

Members

_LazyLoadable_Load()

pprint(*indent*)

ConfigSection

ConfigSectionName

FilesFile

IsVisible

Kind

LazyLoadable_IsLoaded

Level

ModuleName

Name

Parent

Path

Result

Visibility

_Load()

class DataBase.Entity.**CocoTestbench**(*host*, *name*, *configSectionName*, *parent*)

Inheritance

Members

TopLevel

_LazyLoadable_Load()

pprint(*indent*)

ConfigSection

ConfigSectionName

FilesFile

IsVisible

Kind

LazyLoadable_IsLoaded

Level

ModuleName

Name

Parent

Path

Result

Visibility

_Load()

class DataBase.Entity.**Netlist**(*host*, *name*, *configSectionName*, *parent*)

Inheritance

Members

ModuleName

RulesFile

_LazyLoadable_Load()

ConfigSection

ConfigSectionName

IsVisible

Kind

LazyLoadable_IsLoaded

Level

Name

Parent

Path

Visibility

_Load()

class DataBase.Entity.**XstNetlist**(*host*, *name*, *configSectionName*, *parent*)

Inheritance

Members

FilesFile

XcfFile

FilterFile

XstTemplateFile

PrjFile

XstFile

_LazyLoadable_Load()

pprint(*indent*)

ConfigSection

ConfigSectionName

IsVisible

Kind

LazyLoadable_IsLoaded

Level

ModuleName

Name

Parent

Path

RulesFile

Visibility

_Load()

class DataBase.Entity.**QuartusNetlist**(*host*, *name*, *configSectionName*, *parent*)

Inheritance

Members

FilesFile

QsfFile

_LazyLoadable_Load()

pprint(*indent*)

ConfigSection

ConfigSectionName

IsVisible

Kind

LazyLoadable_IsLoaded

Level

ModuleName

Name

Parent

Path

RulesFile

Visibility

_Load()

class DataBase.Entity.**LatticeNetlist**(*host*, *name*, *configSectionName*, *parent*)

Inheritance

Members

FilesFile

PrjFile

_LazyLoadable_Load()

pprint(*indent*)

ConfigSection

ConfigSectionName

IsVisible

Kind

LazyLoadable_IsLoaded

Level

ModuleName

Name

Parent

Path

RulesFile

Visibility

_Load()

class DataBase.Entity.**CoreGeneratorNetlist**(*host*, *name*, *configSectionName*, *parent*)

Inheritance

Members

FilesFile

XcoFile

_LazyLoadable_Load()

pprint(*indent*)

ConfigSection

ConfigSectionName

IsVisible

Kind

LazyLoadable_IsLoaded

Level

ModuleName

Name

Parent

Path

RulesFile

Visibility

_Load()

class DataBase.Entity.**VivadoNetlist**(*host*, *name*, *configSectionName*, *parent*)

Inheritance

Members

FilesFile

TclFile

_LazyLoadable_Load()

pprint(*indent*)

ConfigSection

ConfigSectionName

IsVisible

Kind

LazyLoadable_IsLoaded

Level

ModuleName

Name

Parent

Path

RulesFile

Visibility

_Load()

class DataBase.Entity.**FQN**(*host*, *fqn*, *defaultLibrary='PoC'*, *defaultType=<EntityTypes.Source: 1>*)

Inheritance

Members

Root()

Entity

Functions

DataBase.Entity.**_PoCEntityTypes_parser**(*cls*, *value*)

14.4.3 DataBase.Solution

Classes

- *Base*: Base class for Repository, Solution and Project.
- *Repository*: Base class for Repository, Solution and Project.
- *Solution*: Base class for Repository, Solution and Project.
- *Project*: Base class for Repository, Solution and Project.
- *ISEProject*: Base class for Repository, Solution and Project.
- *VivadoProject*: Base class for Repository, Solution and Project.
- *QuartusProject*: Base class for Repository, Solution and Project.
- *LatticeProject*: Base class for Repository, Solution and Project.
- *VirtualProject*: Undocumented.
- *FileListFile*: Undocumented.
- *RulesFile*: Undocumented.

class DataBase.Solution.**Base**(*host*, *sectionPrefix*, *sectionID*, *parent*)

Base class for Repository, Solution and Project. It implements ILazyLoadable.

Inheritance

Members

ID

Parent

ConfigSectionName

_Load()

Implement this method for early loading.

LazyLoadable_IsLoaded

_LazyLoadable_Load()

class DataBase.Solution.**Repository**(*host*)

Inheritance

Members

Kind

_Load()
Implement this method for early loading.

_LazyLoadable_Load()

AddSolution(*solutionID*, *solutionName*, *solutionRootPath*)

RemoveSolution(*solution*)

Solutions

SolutionNames

ConfigSectionName

ID

LazyLoadable_IsLoaded

Parent

class DataBase.Solution.**Solution**(*host*, *slnID*, *parent*)

Inheritance

Members

Register()

Unregister()

CreateFiles()

_LazyLoadable_Load()

Name

Path

Projects

ProjectNames

ConfigSectionName

ID

LazyLoadable_IsLoaded

Parent

_Load()
Implement this method for early loading.

class DataBase.Solution.**Project**(*host*, *prjID*, *parent*)

Inheritance

Members

Name

ConfigSectionName

ID

LazyLoadable_IsLoaded

Parent

_LazyLoadable_Load()

_Load()
Implement this method for early loading.

class DataBase.Solution.**ISEProject**(*host*, *prjID*, *parent*)

Inheritance

Members

ConfigSectionName

ID

LazyLoadable_IsLoaded

Name

Parent

_LazyLoadable_Load()

_Load()
Implement this method for early loading.

class DataBase.Solution.**VivadoProject**(*host*, *prjID*, *parent*)

Inheritance

Members

ConfigSectionName

ID

LazyLoadable_IsLoaded

Name

Parent

_LazyLoadable_Load()

_Load()
Implement this method for early loading.

class DataBase.Solution.**QuartusProject**(*host*, *prjID*, *parent*)

Inheritance

Members

ConfigSectionName

ID

LazyLoadable_IsLoaded

Name

Parent

_LazyLoadable_Load()

_Load()
Implement this method for early loading.

class DataBase.Solution.**LatticeProject**(*host*, *prjID*, *parent*)

Inheritance

Members

ConfigSectionName

ID

LazyLoadable_IsLoaded

Name

Parent

_LazyLoadable_Load()

_Load()
Implement this method for early loading.

class DataBase.Solution.**VirtualProject**(*name*)

Inheritance

Members

AddExternalVHDLLibraries(*library*)

AddFile(*file*, *fileSet=None*)

AddFileSet(*fileSet*)

AddSourceFile(*file*, *fileSet=None*)

Board

CreateFileSet(*name*, *setDefault=True*)

DefaultFileSet

Device

Environment

ExternalVHDLLibraries

ExtractVHDLLibrariesFromVHDLSourceFiles()

FileSets

Files (*fileType=<FileTypes(Text|ProjectFile|FileListFile|RulesFile|SourceFile|VHDLSourceFile|VerilogSourceFile|Python*
bits=0xFFFF>, *fileSet=None*)

GetVariables()

Name

RootDirectory

Tool

ToolChain

VHDLLibraries

VHDLVersion

pprint (*indent=0*)

class DataBase.Solution.**FileListFile** (*file*, *project=None*, *fileSet=None*)

Inheritance

Members

_FileType = <FileTypes.FileListFile bits=0x0004 data=UNDEFINED>

_classVHDLSourceFile
alias of *Parser.FilesParser.VHDLSourceFileMixIn*

_classVerilogSourceFile
alias of *Parser.FilesParser.VerilogSourceFileMixIn*

_classCocotbSourceFile
alias of *Parser.FilesParser.CocotbSourceFileMixIn*

Parse (*host*)

CopyFilesToFileSet()

CopyExternalLibraries()

FileName

FileSet

FileType

Files

Includes

Libraries

Open()

Path

Project

ReadFile()

Warnings

_Evaluate (*host*, *expr*)

_EvaluatePath (*host*, *expr*)

_Parse()

_ReadContent()

_Resolve(*host*, *statements=None*)

_classIncludeFile
alias of *Parser.FilesParser.IncludeFileMixIn*

_classLDCSourceFile
alias of *Parser.FilesParser.LDCSourceFileMixIn*

_classSDCSourceFile
alias of *Parser.FilesParser.SDCSourceFileMixIn*

_classUCFSourceFile
alias of *Parser.FilesParser.UCFSourceFileMixIn*

_classXDCSourceFile
alias of *Parser.FilesParser.XDCSourceFileMixIn*

class DataBase.Solution.**RulesFile**(*file*, *project=None*, *fileSet=None*)

Inheritance

Members

_FileType = <FileTypes.RulesFile bits=0x0008 data=UNDEFINED>

FileName

FileSet

FileType

Open()

Path

PostProcessRules

PreProcessRules

Project

ReadFile()

_Parse()

_ReadContent()

_Resolve()

_ResolveRule(*ruleStatement*, *lst*)

_classAppendLineRule
alias of *Parser.RulesParser.AppendLineRuleMixIn*

_classCopyRule
alias of *Parser.RulesParser.CopyRuleMixIn*

_classDeleteRule
alias of *Parser.RulesParser.DeleteRuleMixIn*

_classReplaceRule
alias of *Parser.RulesParser.ReplaceRuleMixIn*

Parse()

14.4.4 DataBase.TestCase

Classes

- *SimulationStatus*: An enumeration.
- *CompileStatus*: An enumeration.
- *ElementBase*: Undocumented.
- *GroupBase*: Undocumented.
- *TestGroup*: Undocumented.
- *SynthesisGroup*: Undocumented.
- *SuiteMixIn*: Undocumented.
- *TestSuite*: Undocumented.
- *SynthesisSuite*: Undocumented.
- *TestBase*: Undocumented.
- *TestCase*: Undocumented.
- *Synthesis*: Undocumented.

class DataBase.TestCase.**SimulationStatus**
An enumeration.

Inheritance

Members

Unknown = 0

DryRun = 1

SystemError = 5

InternalError = 6

AnalyzeError = 7

ElaborationError = 8

SimulationError = 9

SimulationFailed = 10

SimulationNoAsserts = 15

SimulationSuccess = 20

SimulationGUIRun = 30

class DataBase.TestCase.**CompileStatus**
An enumeration.

Inheritance

Members

Unknown = 0

DryRun = 1

SystemError = 5

InternalError = 6

CompileError = 7

CompileFailed = 10

CompileSuccess = 20

class DataBase.TestCase.**ElementBase**(*name*, *parent*)

Inheritance

Members

Name

Parent

class DataBase.TestCase.**GroupBase**(*name*, *parent*)

Inheritance

Members

Groups

Count

Name

Parent

class DataBase.TestCase.**TestGroup**(*name*, *parent*)

Inheritance

Members

TestCases

PassedCount

NoAssertsCount

DryRunCount

FailedCount

ErrorCount

Count

Groups

Name

Parent

class DataBase.TestCase.**SynthesisGroup**(*name*, *parent*)

Inheritance

Members

Synthesises

SuccessCount

DryRunCount

FailedCount

ErrorCount

Count

Groups

Name

Parent

class DataBase.TestCase.**SuiteMixIn**

Inheritance

Members

StartTimer()

StopTimer()

StartTime

EndTime

InitializationTime

OverallRunTime

class DataBase.TestCase.**TestSuite**

Inheritance

Members

IsAllPassed

AddTestCase(*testCase*)

Count

DryRunCount

EndTime

ErrorCount

FailedCount

Groups

InitializationTime

Name

NoAssertsCount

OverallRunTime

Parent

PassedCount

StartTime

StartTimer()

StopTimer()

TestCases

class DataBase.TestCase.**SynthesisSuite**

Inheritance

Members

IsAllSuccess

AddSynthesis(*synthesis*)

Count

DryRunCount

EndTime

ErrorCount

FailedCount

Groups

InitializationTime

Name

OverallRunTime

Parent

StartTime

StartTimer()

StopTimer()

SuccessCount

Synthesises

class DataBase.TestCase.**TestBase**(*test*)

Inheritance

Members

Parent

TestGroup

Status

StartTimer()

StopTimer()

OverallRunTime

Name

class DataBase.TestCase.**TestCase**(*testbench*)

Inheritance

Members

Testbench

UpdateStatus(*testResult*)

Name

OverallRunTime

Parent

StartTimer()

Status

StopTimer()

TestGroup

class DataBase.TestCase.**Synthesis**(*synthesis*)

Inheritance

Members

Name

OverallRunTime

Parent

StartTimer()

Status

StopTimer()

TestGroup

Netlist

UpdateStatus(*synthResult*)

Variables

- *__POC_SOLUTION_KEYWORD__*
- *__POC_PROJECT_KEYWORD__*

Classes

- *Query*: Undocumented.

DataBase.**__POC_SOLUTION_KEYWORD__**

str(object='') -> str str(bytes_or_buffer[, encoding[, errors]]) -> str

Create a new string object from the given object. If encoding or errors is specified, then the object must expose a data buffer that will be decoded using the given encoding and error handler. Otherwise, returns the

result of object.__str__() (if defined) or repr(object). encoding defaults to sys.getdefaultencoding(). errors defaults to 'strict'.

```
'Solution'
```

DataBase.**__POC_PROJECT_KEYWORD__**
str(object='') -> str str(bytes_or_buffer[, encoding[, errors]]) -> str

Create a new string object from the given object. If encoding or errors is specified, then the object must expose a data buffer that will be decoded using the given encoding and error handler. Otherwise, returns the result of object.__str__() (if defined) or repr(object). encoding defaults to sys.getdefaultencoding(). errors defaults to 'strict'.

```
'Project'
```

class DataBase.**Query**(*host*)

Inheritance

Members

Host

Platform

PoCConfig

QueryConfiguration(*query*)

_GetModelSimInstallationDirectory()

_GetModelSimBinaryDirectory()

_GetXilinxISESettingsFile()

_GetXilinxVivadoSettingsFile()

14.5 Parser

Submodules

14.5.1 Parser.FilesCodeDOM

Classes

- *BlockedStatement*: Undocumented.
- *IfThenElseExpressions*: Undocumented.
- *ListElementExpressions*: Undocumented.
- *PathExpressions*: Undocumented.
- *ListConstructorExpression*: Undocumented.
- *SubDirectoryExpression*: Undocumented.
- *ConcatenateExpression*: Undocumented.
- *ExistsFunction*: Undocumented.
- *VHDLStatement*: Undocumented.
- *VerilogStatement*: Undocumented.

- *CocotbStatement*: Undocumented.
- *ConstraintStatement*: Undocumented.
- *LDCStatement*: Undocumented.
- *SDCStatement*: Undocumented.
- *UCFStatement*: Undocumented.
- *XDCStatement*: Undocumented.
- *InterpolateLiteral*: Undocumented.
- *PathStatement*: Undocumented.
- *ReportStatement*: Undocumented.
- *LibraryStatement*: Undocumented.
- *IncludeStatement*: Undocumented.
- *IfStatement*: Undocumented.
- *ElseIfStatement*: Undocumented.
- *ElseStatement*: Undocumented.
- *IfElseIfElseStatement*: Undocumented.
- *Document*: Undocumented.

class Parser.FilesCodeDOM.**BlockedStatement**

Inheritance

Members

_allowedStatements = [<class 'Parser.FilesCodeDOM.IncludeStatement'>, <class 'Parser

classmethod AddChoice(*value*)

classmethod GetParser()

classmethod Parse(*string*, *printChar*)

class Parser.FilesCodeDOM.**IfThenElseExpressions**

Inheritance

Members

_allowedExpressions = [<class 'lib.CodeDOM.Identifier'>, <class 'lib.CodeDOM.StringL

classmethod AddChoice(*value*)

classmethod GetParser()

classmethod Parse(*string*, *printChar*)

class Parser.FilesCodeDOM.**ListElementExpressions**

Inheritance

Members

_allowedExpressions = [<class 'lib.CodeDOM.Identifier'>, <class 'lib.CodeDOM.StringL

classmethod AddChoice(*value*)

classmethod GetParser()

classmethod Parse(*string*, *printChar*)

class Parser.FilesCodeDOM.**PathExpressions**

Inheritance

Members

_allowedExpressions = [<class 'lib.CodeDOM.Identifier'>, <class 'lib.CodeDOM.StringL

classmethod AddChoice(*value*)

classmethod GetParser()

classmethod Parse(*string*, *printChar*)

class Parser.FilesCodeDOM.**ListConstructorExpression**

Inheritance

Members

List

AddElement(*element*)

classmethod GetParser()

classmethod Parse(*string*, *printChar*)

class Parser.FilesCodeDOM.**SubDirectoryExpression**(*leftChild*, *rightChild*)

Inheritance

Members

classmethod GetParser()

LeftChild

classmethod Parse(*string*, *printChar*)

RightChild

class Parser.FilesCodeDOM.**ConcatenateExpression**(*leftChild*, *rightChild*)

Inheritance

Members

classmethod GetParser()

LeftChild

classmethod Parse(*string*, *printChar*)

RightChild

class Parser.FilesCodeDOM.**ExistsFunction**(*expression*)

Inheritance

Members

Expression

classmethod GetParser()

classmethod Parse(*string*, *printChar*)

class Parser.FilesCodeDOM.**VHDLStatement**(*libraryName*, *pathExpression*, *commentText*)

Inheritance

Members

LibraryName

PathExpression

classmethod GetParser()

CommentText

classmethod Parse(*string*, *printChar*)

class Parser.FilesCodeDOM.**VerilogStatement**(*pathExpression*, *commentText*)

Inheritance

Members

PathExpression

classmethod GetParser()

CommentText

classmethod Parse(*string*, *printChar*)

class Parser.FilesCodeDOM.**CocotbStatement**(*pathExpression*, *commentText*)

Inheritance

Members

PathExpression

classmethod GetParser()

CommentText

classmethod Parse(*string*, *printChar*)

class Parser.FilesCodeDOM.**ConstraintStatement**(*pathExpression*, *commentText*)

Inheritance

Members

PathExpression

classmethod GetParser()

CommentText

classmethod Parse(*string*, *printChar*)

class Parser.FilesCodeDOM.**LDCStatement**(*pathExpression*, *commentText*)

Inheritance

Members

CommentText

classmethod GetParser()

classmethod Parse(*string*, *printChar*)

PathExpression

class Parser.FilesCodeDOM.**SDCStatement**(*pathExpression*, *commentText*)

Inheritance

Members

CommentText

classmethod GetParser()

classmethod Parse(*string*, *printChar*)

PathExpression

class Parser.FilesCodeDOM.**UCFStatement**(*pathExpression*, *commentText*)

Inheritance

Members

CommentText

classmethod GetParser()

classmethod Parse(*string*, *printChar*)

PathExpression

class Parser.FilesCodeDOM.**XDCStatement**(*pathExpression*, *commentText*)

Inheritance

Members

CommentText

classmethod GetParser()

classmethod Parse(*string*, *printChar*)

PathExpression

class Parser.FilesCodeDOM.**InterpolateLiteral**(*sectionName*, *optionName*)

Inheritance

Members

SectionName

OptionName

classmethod GetParser()

classmethod Parse(*string*, *printChar*)

class Parser.FilesCodeDOM.**PathStatement**(*variable*, *pathExpression*, *commentText*)

Inheritance

Members

Variable

PathExpression

classmethod GetParser()

CommentText

classmethod Parse(*string*, *printChar*)

class Parser.FilesCodeDOM.**ReportStatement**(*message*, *commentText*)

Inheritance

Members

Message

classmethod GetParser()

CommentText

classmethod Parse(*string*, *printChar*)

class Parser.FilesCodeDOM.**LibraryStatement**(*library*, *pathExpression*, *commentText*)

Inheritance

Members

Library

PathExpression

classmethod GetParser()

CommentText

classmethod Parse(*string*, *printChar*)

class Parser.FilesCodeDOM.**IncludeStatement**(*pathExpression*, *commentText*)

Inheritance

Members

PathExpression

classmethod GetParser()

CommentText

classmethod Parse(*string*, *printChar*)

class Parser.FilesCodeDOM.**IfStatement**(*expression*, *commentText*)

Inheritance

Members

classmethod GetParser()

AddStatement(*stmt*)

CommentText

Expression

classmethod Parse(*string*, *printChar*)

Statements

class Parser.FilesCodeDOM.**ElseIfStatement**(*expression*, *commentText*)

Inheritance

Members

classmethod GetParser()

AddStatement(*stmt*)

CommentText

Expression

classmethod Parse(*string*, *printChar*)

Statements

class Parser.FilesCodeDOM.**ElseStatement**(*commentText*)

Inheritance

Members

classmethod GetParser()

AddStatement(*stmt*)

CommentText

classmethod Parse(*string*, *printChar*)

Statements

class Parser.FilesCodeDOM.**IfElseIfElseStatement**

Inheritance

Members

IfClause

ElseIfClauses

ElseClause

classmethod GetParser()

CommentText

classmethod Parse(*string*, *printChar*)

class Parser.FilesCodeDOM.**Document**(*commentText=''*)

Inheritance

Members

AddStatement(*stmt*)

CommentText

classmethod Parse(*string*, *printChar*)

Statements

classmethod GetParser()

14.5.2 Parser.FilesParser

Classes

- *FileReference*: Undocumented.
- *IncludeFileMixIn*: Undocumented.
- *VHDLSourceFileMixIn*: Undocumented.
- *VerilogSourceFileMixIn*: Undocumented.
- *CocotbSourceFileMixIn*: Undocumented.
- *LDCSourceFileMixIn*: Undocumented.
- *SDCSourceFileMixIn*: Undocumented.
- *UCFSourceFileMixIn*: Undocumented.
- *XDCSourceFileMixIn*: Undocumented.
- *VHDLLibraryReference*: Undocumented.
- *FilesParserMixIn*: Undocumented.

class Parser.FilesParser.**FileReference**(*file*)

Inheritance

Members

File

class Parser.FilesParser.**IncludeFileMixIn**(*file*)

Inheritance

Members

File

class Parser.FilesParser.**VHDLSourceFileMixIn**(*file*, *library*)

Inheritance

Members

LibraryName

File

class Parser.FilesParser.**VerilogSourceFileMixIn**(*file*)

Inheritance

Members

File

class Parser.FilesParser.**CocotbSourceFileMixIn**(*file*)

Inheritance

Members

File

class Parser.FilesParser.**LDCSourceFileMixIn**(*file*)

Inheritance

Members

File

class Parser.FilesParser.**SDCSourceFileMixIn**(*file*)

Inheritance

Members

File

class Parser.FilesParser.**UCFSourceFileMixIn**(*file*)

Inheritance

Members

File

class Parser.FilesParser.**XDCSourceFileMixIn**(*file*)

Inheritance

Members

File

class Parser.FilesParser.**VHDLLibraryReference**(*name*, *path*)

Inheritance

Members

Name

Path

class Parser.FilesParser.**FilesParserMixIn**

Inheritance

Members

_classIncludeFile
alias of *IncludeFileMixIn*

_classVHDLSourceFile
alias of *VHDLSourceFileMixIn*

_classVerilogSourceFile
alias of *VerilogSourceFileMixIn*

_classCocotbSourceFile
alias of *CocotbSourceFileMixIn*

_classLDCSourceFile
alias of *LDCSourceFileMixIn*

_classSDCSourceFile
alias of *SDCSourceFileMixIn*

_classUCFSourceFile
alias of *UCFSourceFileMixIn*

_classXDCSourceFile
alias of *XDCSourceFileMixIn*

_Parse()

_Resolve(*host*, *statements=None*)

_Evaluate(*host*, *expr*)

_EvaluatePath(*host*, *expr*)

Files

Includes

Libraries

Warnings

14.5.3 Parser.RulesCodeDOM

Classes

- *InFileStatements*: Undocumented.
- *PreProcessStatements*: Undocumented.
- *PostProcessStatements*: Undocumented.
- *DocumentStatements*: Undocumented.

- *CopyStatement*: Undocumented.
- *DeleteStatement*: Undocumented.
- *ReplaceStatement*: Undocumented.
- *AppendLineStatement*: Undocumented.
- *FileStatement*: Undocumented.
- *ProcessRulesBlockStatement*: Undocumented.
- *PreProcessRulesStatement*: Undocumented.
- *PostProcessRulesStatement*: Undocumented.
- *Document*: Undocumented.

class Parser.RulesCodeDOM.**InFileStatements**

Inheritance

Members

_allowedStatements = [<class 'Parser.RulesCodeDOM.ReplaceStatement'>, <class 'Parser

classmethod AddChoice(*value*)

classmethod GetParser()

classmethod Parse(*string*, *printChar*)

class Parser.RulesCodeDOM.**PreProcessStatements**

Inheritance

Members

_allowedStatements = [<class 'Parser.RulesCodeDOM.CopyStatement'>, <class 'Parser.Ru

classmethod AddChoice(*value*)

classmethod GetParser()

classmethod Parse(*string*, *printChar*)

class Parser.RulesCodeDOM.**PostProcessStatements**

Inheritance

Members

_allowedStatements = [<class 'Parser.RulesCodeDOM.CopyStatement'>, <class 'Parser.Ru

classmethod AddChoice(*value*)

classmethod GetParser()

classmethod Parse(*string*, *printChar*)

class Parser.RulesCodeDOM.**DocumentStatements**

Inheritance

Members

_allowedStatements = [<class 'Parser.RulesCodeDOM.PreProcessRulesStatement'>, <class

classmethod AddChoice(*value*)

classmethod GetParser()

classmethod Parse(*string*, *printChar*)

class Parser.RulesCodeDOM.**CopyStatement**(*source*, *destination*, *commentText*)

Inheritance

Members

SourcePath

DestinationPath

classmethod GetParser()

CommentText

classmethod Parse(*string*, *printChar*)

class Parser.RulesCodeDOM.**DeleteStatement**(*file*, *commentText*)

Inheritance

Members

FilePath

classmethod GetParser()

CommentText

classmethod Parse(*string*, *printChar*)

class Parser.RulesCodeDOM.**ReplaceStatement**(*searchPattern*, *replacePattern*, *caseInsensitive*, *multiLine*, *dotAll*, *commentText*)

Inheritance

Members

SearchPattern

ReplacePattern

CaseInsensitive

MultiLine

DotAll

classmethod GetParser()

CommentText

classmethod Parse(*string*, *printChar*)

class Parser.RulesCodeDOM.**AppendLineStatement**(*appendPattern*, *commentText*)

Inheritance

Members

AppendPattern

classmethod GetParser()

CommentText

classmethod Parse(*string*, *printChar*)

class Parser.RulesCodeDOM.**FileStatement**(*file*, *commentText*)

Inheritance

Members

FilePath

classmethod GetParser()

AddStatement(*stmt*)

CommentText

classmethod Parse(*string*, *printChar*)

Statements

class Parser.RulesCodeDOM.**ProcessRulesBlockStatement**(*commentText*)

Inheritance

Members

classmethod GetParser()

AddStatement(*stmt*)

CommentText

classmethod Parse(*string*, *printChar*)

Statements

class Parser.RulesCodeDOM.**PreProcessRulesStatement**(*commentText*)

Inheritance

Members

AddStatement(*stmt*)

CommentText

classmethod GetParser()

classmethod Parse(*string*, *printChar*)

Statements

class Parser.RulesCodeDOM.**PostProcessRulesStatement**(*commentText*)

Inheritance

Members

AddStatement(*stmt*)

CommentText

classmethod GetParser()

classmethod Parse(*string*, *printChar*)

Statements

class Parser.RulesCodeDOM.**Document**(*commentText=''*)

Inheritance

Members

classmethod GetParser()

AddStatement(*stmt*)

CommentText

classmethod Parse(*string*, *printChar*)

Statements

14.5.4 Parser.RulesParser

Classes

- *Rule*: Base class for all Rule and RuleMixIn classes.
- *CopyRuleMixIn*: A partial class (MixIn) to represent a 'copy rule'.
- *DeleteRuleMixIn*: A partial class (MixIn) to represent a 'delete rule'.
- *ReplaceRuleMixIn*: A partial class (MixIn) to represent a 'replace rule'.
- *AppendLineRuleMixIn*: A partial class (MixIn) to represent a 'append line rule'.
- *RulesParserMixIn*: Undocumented.

class Parser.RulesParser.**Rule**
Base class for all Rule and RuleMixIn classes.

Inheritance

Members

class Parser.RulesParser.**CopyRuleMixIn**(*sourcePath*, *destinationPath*)
A partial class (MixIn) to represent a 'copy rule'.

Inheritance

Members

SourcePath

DestinationPath

class Parser.RulesParser.**DeleteRuleMixIn** (*filePath*)
A partial class (MixIn) to represent a 'delete rule'.

Inheritance

Members

FilePath

class Parser.RulesParser.**ReplaceRuleMixIn** (*filePath*, *searchPattern*, *replacePattern*, *multiLine*, *dotAll*, *caseInSensitive*)
A partial class (MixIn) to represent a 'replace rule'.

Inheritance

Members

FilePath

SearchPattern

ReplacePattern

RegExpOption_MultiLine

RegExpOption_DotAll

RegExpOption_CaseInsensitive

class Parser.RulesParser.**AppendLineRuleMixIn** (*filePath*, *appendPattern*)
A partial class (MixIn) to represent a 'append line rule'.

Inheritance

Members

FilePath

AppendPattern

class Parser.RulesParser.**RulesParserMixIn**

Inheritance

Members

_classCopyRule
alias of *CopyRuleMixIn*

_classDeleteRule
alias of *DeleteRuleMixIn*

_classReplaceRule
alias of *ReplaceRuleMixIn*

_classAppendLineRule
alias of *AppendLineRuleMixIn*

_Parse()

_Resolve()

_ResolveRule(*ruleStatement*, *lst*)

PreProcessRules

PostProcessRules

14.6 Simulator

Submodules

14.6.1 Simulator.ActiveHDLSimulator

Classes

- *Simulator*: Base class for all Simulator classes.

class Simulator.ActiveHDLSimulator.**Simulator**(*host*, *dryRun*, *simulationSteps*)

Inheritance

Members

TOOL_CHAIN = 10

TOOL = ('ASIM', 'Aldec Active-HDL', 'Aldec Active-HDL')

_PrepareSimulator()
Create the Active-HDL executable factory.

_RunAnalysis(*_*)

_RunSimulation(*testbench*)

_RunSimulationWithGUI(*testbench*)

Directories

DryRun

ENVIRONMENT = 1

Host

Log(*entry*, *condition=True*)
Write an entry to the local logger.

LogDebug(**args*, *condition=True*, ***kwargs*)

LogDryRun(**args*, *condition=True*, ***kwargs*)

LogError(**args*, *condition=True*, ***kwargs*)

LogFatal(**args*, *condition=True*, ***kwargs*)

LogInfo(**args*, *condition=True*, ***kwargs*)

LogNormal(**args*, *condition=True*, ***kwargs*)

LogQuiet(**args*, *condition=True*, ***kwargs*)

LogVerbose(**args*, *condition=True*, ***kwargs*)

LogWarning(**args*, *condition=True*, ***kwargs*)

Logger
Return the local logger instance.

PoCProject

PrintOverallSimulationReport()

PrintSimulationReportLine(*testObject*, *indent*, *nameColumnWidth*)

Run(*testbench*, *board*, *vhdlVersion*, *vhdlGenerics=None*)
Write the Testbench message line, create a PoCProject and add the first *.files file to it.

RunAll(*fqnList*, **args*, ***kwargs*)
Run a list of testbenches. Expand wildcards to all selected testbenches.

TestSuite

TryRun(*testbench*, **args*, ***kwargs*)
Try to run a testbench. Skip skipable exceptions by printing the error and its cause.

VHDLVersion

VHDL_VERSION = 2008

_AddFileListFile(*fileListFilePath*)

_CreatePoCProject(*projectName*, *board*)

_GetHDLParameters(*configSectionName*)
Parse option 'HDLParameters' for Verilog Parameters / VHDL Generics.

_GetTimeDeltaSinceLastEvent()

_Prepare()

_PrepareEnvironment()

_PrepareEnvironment_ChangeDirectory()
Change working directory to temporary path 'temp/<tool>'.

_PrepareEnvironment_CreatingDirectory()

_PrepareEnvironment_PurgeDirectory()

_PrepareSimulationEnvironment()

_RunCoverage(*testbench*)

_RunElaboration(*testbench*)

_RunView(*testbench*)

_TryLog(**args*, *condition=True*, ***kwargs*)

14.6.2 Simulator.CocotbSimulator

Classes

- *Simulator*: Base class for all Simulator classes.

class Simulator.CocotbSimulator.**Simulator**(*host*, *dryRun*, *simulationSteps*)

Inheritance

Members

TOOL_CHAIN = 30

TOOL = ('COCO', 'Cocotb', 'Coroutine Cosimulation Testbench (Cocotb)')

COCOTB_SIMBUILD_DIRECTORY = 'sim_build'

_PrepareSimulator()

RunAll(*fqnList*, **args*, ***kwargs*)
Run a list of testbenches. Expand wildcards to all selected testbenches.

_RunSimulation(*testbench*)

Directories

DryRun

ENVIRONMENT = 1

Host

Log(*entry*, *condition=True*)
Write an entry to the local logger.

LogDebug(**args*, *condition=True*, ***kwargs*)

LogDryRun(**args*, *condition=True*, ***kwargs*)

LogError(**args*, *condition=True*, ***kwargs*)

LogFatal(**args*, *condition=True*, ***kwargs*)

LogInfo(**args*, *condition=True*, ***kwargs*)

LogNormal(**args*, *condition=True*, ***kwargs*)

LogQuiet(**args*, *condition=True*, ***kwargs*)

LogVerbose(**args*, *condition=True*, ***kwargs*)

LogWarning(**args*, *condition=True*, ***kwargs*)

Logger
Return the local logger instance.

PoCProject

PrintOverallSimulationReport()

PrintSimulationReportLine(*testObject*, *indent*, *nameColumnWidth*)

Run(*testbench*, *board*, *vhdlVersion*, *vhdlGenerics=None*)
Write the Testbench message line, create a PoCProject and add the first *.files file to it.

TestSuite

TryRun(*testbench*, **args*, ***kwargs*)
Try to run a testbench. Skip skipable exceptions by printing the error and its cause.

VHDLVersion

VHDL_VERSION = 2008

_AddFileListFile(*fileListFilePath*)

_CreatePoCProject(*projectName*, *board*)

_GetHDLParameters(*configSectionName*)
Parse option 'HDLParameters' for Verilog Parameters / VHDL Generics.

_GetTimeDeltaSinceLastEvent()

_Prepare()

_PrepareEnvironment()

_PrepareEnvironment_ChangeDirectory()
Change working directory to temporary path 'temp/<tool>'.

_PrepareEnvironment_CreatingDirectory()

_PrepareEnvironment_PurgeDirectory()

_PrepareSimulationEnvironment()

_RunAnalysis(*testbench*)

_RunCoverage(*testbench*)

_RunElaboration(*testbench*)

_RunView(*testbench*)

_TryLog(**args*, *condition=True*, ***kwargs*)

14.6.3 Simulator.GHDLSimulator

Classes

- *Simulator*: This class encapsulates the GHDL simulator.

class Simulator.GHDLSimulator.**Simulator**(*host*, *dryRun*, *simulationSteps*)
This class encapsulates the GHDL simulator.

Inheritance

Members

TOOL_CHAIN = 40

TOOL = ('GHDL', 'GHDL', 'GHDL')

_PrepareSimulator()
Create the GHDL executable factory instance.

Run(*testbench*, *board*, *vhdlVersion*, *vhdlGenerics=None*, *withCoverage=False*)
Write the Testbench message line, create a PoCProject and add the first *.files file to it.

_RunAnalysis(*testbench*)

_SetVHDLVersionAndIEEEFlavor(*ghdl*)

_SetExternalLibraryReferences(*ghdl*)

_RunElaboration(*testbench*)

_RunSimulation(*testbench*)

_RunView(*testbench*)
foo

_RunCoverage(*testbench*)

Directories

DryRun

ENVIRONMENT = 1

Host

Log(*entry*, *condition=True*)
Write an entry to the local logger.

LogDebug(**args*, *condition=True*, ***kwargs*)

LogDryRun(**args*, *condition=True*, ***kwargs*)

LogError(**args*, *condition=True*, ***kwargs*)

LogFatal(**args*, *condition=True*, ***kwargs*)

LogInfo(**args*, *condition=True*, ***kwargs*)

LogNormal(**args*, *condition=True*, ***kwargs*)

LogQuiet(**args*, *condition=True*, ***kwargs*)

LogVerbose(**args*, *condition=True*, ***kwargs*)

LogWarning(**args*, *condition=True*, ***kwargs*)

Logger
Return the local logger instance.

PoCProject

PrintOverallSimulationReport()

PrintSimulationReportLine(*testObject*, *indent*, *nameColumnWidth*)

RunAll(*fqnList*, **args*, ***kwargs*)
Run a list of testbenches. Expand wildcards to all selected testbenches.

TestSuite

TryRun(*testbench*, **args*, ***kwargs*)
Try to run a testbench. Skip skipable exceptions by printing the error and its cause.

VHDLVersion

VHDL_VERSION = 2008

_AddFileListFile(*fileListFilePath*)

_CreatePoCProject(*projectName*, *board*)

_GetHDLParameters(*configSectionName*)
Parse option 'HDLParameters' for Verilog Parameters / VHDL Generics.

_GetTimeDeltaSinceLastEvent()

_Prepare()

_PrepareEnvironment()

_PrepareEnvironment_ChangeDirectory()
Change working directory to temporary path 'temp/<tool>'.

_PrepareEnvironment_CreatingDirectory()

_PrepareEnvironment_PurgeDirectory()

_PrepareSimulationEnvironment()

_TryLog(**args*, *condition=True*, ***kwargs*)

14.6.4 Simulator.ISESimulator

Classes

- *Simulator*: Base class for all Simulator classes.

class Simulator.ISESimulator.**Simulator**(*host*, *dryRun*, *simulationSteps*)

Inheritance

Members

TOOL_CHAIN = 80

TOOL = ('XSIM', 'Xilinx iSim', 'Xilinx ISE Simulator (iSim)')

_PrepareSimulator()

_RunElaboration(*testbench*)

_RunSimulation(*testbench*)

Directories

DryRun

ENVIRONMENT = 1

Host

Log(*entry*, *condition=True*)
Write an entry to the local logger.

LogDebug(**args*, *condition=True*, ***kwargs*)

LogDryRun(**args*, *condition=True*, ***kwargs*)

LogError(**args*, *condition=True*, ***kwargs*)

LogFatal(**args*, *condition=True*, ***kwargs*)

LogInfo(**args*, *condition=True*, ***kwargs*)

LogNormal(**args*, *condition=True*, ***kwargs*)

LogQuiet(**args*, *condition=True*, ***kwargs*)

LogVerbose(**args*, *condition=True*, ***kwargs*)

LogWarning(**args*, *condition=True*, ***kwargs*)

Logger
Return the local logger instance.

PoCProject

PrintOverallSimulationReport()

PrintSimulationReportLine(*testObject*, *indent*, *nameColumnWidth*)

Run(*testbench*, *board*, *vhdlVersion*, *vhdlGenerics=None*)
Write the Testbench message line, create a PoCProject and add the first *.files file to it.

RunAll(*fqnList*, **args*, ***kwargs*)
Run a list of testbenches. Expand wildcards to all selected testbenches.

TestSuite

TryRun(*testbench*, **args*, ***kwargs*)
Try to run a testbench. Skip skipable exceptions by printing the error and its cause.

VHDLVersion

VHDL_VERSION = 2008

_AddFileListFile(*fileListFilePath*)

_CreatePoCProject(*projectName*, *board*)

_GenerateXilinxProjectFileContent(*tool*, *vhdlVersion=93*)

_GetHDLParameters(*configSectionName*)
Parse option 'HDLParameters' for Verilog Parameters / VHDL Generics.

_GetTimeDeltaSinceLastEvent()

_Prepare()

_PrepareEnvironment()

_PrepareEnvironment_ChangeDirectory()
Change working directory to temporary path 'temp/<tool>'.

_PrepareEnvironment_CreatingDirectory()

_PrepareEnvironment_PurgeDirectory()

_PrepareSimulationEnvironment()

_RunAnalysis(*testbench*)

_RunCoverage(*testbench*)

_RunView(*testbench*)

_TryLog(**args*, *condition=True*, ***kwargs*)

_WriteXilinxProjectFile(*projectFilePath*, *tool*, *vhdlVersion=93*)

14.6.5 Simulator.ModelSimSimulator

Classes

- *Simulator*: Base class for all Simulator classes.

class Simulator.ModelSimSimulator.**Simulator**(*host*, *dryRun*, *simulationSteps*)

Inheritance

Members

TOOL_CHAIN = 70

TOOL = ('VSIM', 'Mentor ModelSim', 'Mentor Graphics ModelSim (vSim)')

_PrepareSimulator()

Run(*testbench*, *board*, *vhdlVersion*, *vhdlGenerics=None*, *withCoverage=False*)
Write the Testbench message line, create a PoCProject and add the first *.files file to it.

_RunAnalysis(*_*)

_RunSimulation(*testbench*)

_RunSimulationWithGUI(*testbench*)

Directories

DryRun

ENVIRONMENT = 1

Host

Log (*entry*, *condition=True*)
Write an entry to the local logger.

LogDebug (**args*, *condition=True*, ***kwargs*)

LogDryRun (**args*, *condition=True*, ***kwargs*)

LogError (**args*, *condition=True*, ***kwargs*)

LogFatal (**args*, *condition=True*, ***kwargs*)

LogInfo (**args*, *condition=True*, ***kwargs*)

LogNormal (**args*, *condition=True*, ***kwargs*)

LogQuiet (**args*, *condition=True*, ***kwargs*)

LogVerbose (**args*, *condition=True*, ***kwargs*)

LogWarning (**args*, *condition=True*, ***kwargs*)

Logger
Return the local logger instance.

PoCProject

PrintOverallSimulationReport ()

PrintSimulationReportLine (*testObject*, *indent*, *nameColumnWidth*)

RunAll (*fqnList*, **args*, ***kwargs*)
Run a list of testbenches. Expand wildcards to all selected testbenches.

TestSuite

TryRun (*testbench*, **args*, ***kwargs*)
Try to run a testbench. Skip skipable exceptions by printing the error and its cause.

VHDLVersion

VHDL_VERSION = 2008

_AddFileListFile (*fileListFilePath*)

_CreatePoCProject (*projectName*, *board*)

_GetHDLParameters (*configSectionName*)
Parse option 'HDLParameters' for Verilog Parameters / VHDL Generics.

_GetTimeDeltaSinceLastEvent ()

_Prepare ()

_PrepareEnvironment ()

_PrepareEnvironment_ChangeDirectory ()
Change working directory to temporary path 'temp/<tool>'.

_PrepareEnvironment_CreatingDirectory ()

_PrepareEnvironment_PurgeDirectory ()

_PrepareSimulationEnvironment ()

_RunCoverage (*testbench*)

_RunElaboration (*testbench*)

_RunView (*testbench*)

_TryLog (**args*, *condition=True*, ***kwargs*)

14.6.6 Simulator.QuestaSimulator

Classes

- *Simulator*: Base class for all Simulator classes.

class Simulator.QuestaSimulator.**Simulator**(*host*, *dryRun*, *simulationSteps*)

Inheritance

Members

TOOL_CHAIN = 75

TOOL = ('VSIM', 'Mentor ModelSim', 'Mentor Graphics ModelSim (vSim)')

_PrepareSimulator()

Run(*testbench*, *board*, *vhdlVersion*, *vhdlGenerics=None*)
Write the Testbench message line, create a PoCProject and add the first *.files file to it.

_RunAnalysis(*_*)

_RunSimulation(*testbench*)

_RunSimulationWithGUI(*testbench*)

Directories

DryRun

ENVIRONMENT = 1

Host

Log(*entry*, *condition=True*)
Write an entry to the local logger.

LogDebug(**args*, *condition=True*, ***kwargs*)

LogDryRun(**args*, *condition=True*, ***kwargs*)

LogError(**args*, *condition=True*, ***kwargs*)

LogFatal(**args*, *condition=True*, ***kwargs*)

LogInfo(**args*, *condition=True*, ***kwargs*)

LogNormal(**args*, *condition=True*, ***kwargs*)

LogQuiet(**args*, *condition=True*, ***kwargs*)

LogVerbose(**args*, *condition=True*, ***kwargs*)

LogWarning(**args*, *condition=True*, ***kwargs*)

Logger
Return the local logger instance.

PoCProject

PrintOverallSimulationReport()

PrintSimulationReportLine(*testObject*, *indent*, *nameColumnWidth*)

RunAll(*fqnList*, **args*, ***kwargs*)
Run a list of testbenches. Expand wildcards to all selected testbenches.

TestSuite

TryRun (*testbench*, **args*, ***kwargs*)
Try to run a testbench. Skip skipable exceptions by printing the error and its cause.

VHDLVersion

VHDL_VERSION = 2008

_AddFileListFile (*fileListFilePath*)

_CreatePoCProject (*projectName*, *board*)

_GetHDLParameters (*configSectionName*)
Parse option 'HDLParameters' for Verilog Parameters / VHDL Generics.

_GetTimeDeltaSinceLastEvent ()

_Prepare ()

_PrepareEnvironment ()

_PrepareEnvironment_ChangeDirectory ()
Change working directory to temporary path 'temp/<tool>'.

_PrepareEnvironment_CreatingDirectory ()

_PrepareEnvironment_PurgeDirectory ()

_PrepareSimulationEnvironment ()

_RunCoverage (*testbench*)

_RunElaboration (*testbench*)

_RunView (*testbench*)

_TryLog (**args*, *condition=True*, ***kwargs*)

14.6.7 Simulator.RivieraPROSimulator

14.6.8 Simulator.VivadoSimulator

Classes

- *Simulator*: Base class for all Simulator classes.

class Simulator.VivadoSimulator.**Simulator** (*host*, *dryRun*, *simulationSteps*)

Inheritance

Members

TOOL_CHAIN = 82

TOOL = ('XSIM', 'Xilinx xSim', 'Xilinx Vivado Simulator (xSim)')

_PrepareSimulator ()

_RunElaboration (*testbench*)

_RunSimulation (*testbench*)

Directories

DryRun

ENVIRONMENT = 1

Host

Log (*entry*, *condition=True*)
Write an entry to the local logger.

LogDebug (**args*, *condition=True*, ***kwargs*)

LogDryRun (**args*, *condition=True*, ***kwargs*)

LogError (**args*, *condition=True*, ***kwargs*)

LogFatal (**args*, *condition=True*, ***kwargs*)

LogInfo (**args*, *condition=True*, ***kwargs*)

LogNormal (**args*, *condition=True*, ***kwargs*)

LogQuiet (**args*, *condition=True*, ***kwargs*)

LogVerbose (**args*, *condition=True*, ***kwargs*)

LogWarning (**args*, *condition=True*, ***kwargs*)

Logger
Return the local logger instance.

PoCProject

PrintOverallSimulationReport ()

PrintSimulationReportLine (*testObject*, *indent*, *nameColumnWidth*)

Run (*testbench*, *board*, *vhdlVersion*, *vhdlGenerics=None*)
Write the Testbench message line, create a PoCProject and add the first *.files file to it.

RunAll (*fqnList*, **args*, ***kwargs*)
Run a list of testbenches. Expand wildcards to all selected testbenches.

TestSuite

TryRun (*testbench*, **args*, ***kwargs*)
Try to run a testbench. Skip skipable exceptions by printing the error and its cause.

VHDLVersion

VHDL_VERSION = 2008

_AddFileListFile (*fileListFilePath*)

_CreatePoCProject (*projectName*, *board*)

_GenerateXilinxProjectFileContent (*tool*, *vhdlVersion=93*)

_GetHDLParameters (*configSectionName*)
Parse option 'HDLParameters' for Verilog Parameters / VHDL Generics.

_GetTimeDeltaSinceLastEvent ()

_Prepare ()

_PrepareEnvironment ()

_PrepareEnvironment_ChangeDirectory ()
Change working directory to temporary path 'temp/<tool>'.

_PrepareEnvironment_CreatingDirectory ()

_PrepareEnvironment_PurgeDirectory ()

_PrepareSimulationEnvironment ()

_RunAnalysis (*testbench*)

_RunCoverage (*testbench*)

_RunView (*testbench*)

_TryLog(**args*, *condition=True*, ***kwargs*)

_WriteXilinxProjectFile(*projectFilePath*, *tool*, *vhdlVersion=93*)

Exceptions

- *SimulatorException*: Base class for all SimulatorException classes. It is raised while running
- *SkipableSimulatorException*: SkipableSimulatorException is a *SimulatorException*, which
- *PoCSimulationResultNotFoundException*: This exception is raised if the expected PoC simulation result string was

Classes

- *SimulationSteps*: Simulation step enumeration.
- *SimulationState*: Simulation state enumeration.
- *SimulationResult*: Simulation result enumeration.
- *Simulator*: Base class for all Simulator classes.

Functions

- *PoCSimulationResultFilter()*: Undocumented.

exception Simulator.**SimulatorException**(*message=''*)
Base class for all SimulatorException classes. It is raised while running simulation tasks in PoC.

Inheritance

Members

__init__(*message=''*)
Exception initializer

Parameters **message** (*str*) – The exception message.

__str__()
Returns the exception's message text.

args

exception Simulator.**SkipableSimulatorException**(*message=''*)
SkipableSimulatorException is a *SimulatorException*, which can be skipped.

Inheritance

Members

__init__(*message=''*)
Exception initializer

Parameters **message** (*str*) – The exception message.

__str__()
Returns the exception's message text.

args

exception Simulator.**PoCSimulationResultNotFoundException**(*message=''*)
This exception is raised if the expected PoC simulation result string was not found in the simulator's output.

Inheritance

Members

__init__(*message=''*)
Exception initializer

Parameters **message** (*str*) – The exception message.

__str__()
Returns the exception's message text.

args

class Simulator.**SimulationSteps**
Simulation step enumeration.

Inheritance

Members

_FlagsArithmeticMixin__bits

_FlagsArithmeticMixin__create_flags_instance(*bits*)

_Flags__internal_str()

classmethod bits_from_simple_str(*s*)

classmethod bits_from_str(*s*)
Converts the output of __str__ into an integer.

data

classmethod from_simple_str(*s*)
Accepts only the output of to_simple_str(). The output of __str__() is invalid as input.

classmethod from_str(*s*)
Accepts both the output of to_simple_str() and __str__().

is_disjoint(**flags_instances*)

is_member
flags.is_member is a shorthand for *flags.properties is not None*. If this property is False then this Flags instance has either zero bits or holds a combination of flag member bits. If this property is True then the bits of this Flags instance match exactly the bits associated with one of the members. This however doesn't necessarily mean that this flag instance isn't a combination of several flags because the bits of a member can be the subset of another member. For example if member0_bits=0x1 and member1_bits=0x3 then the bits of member0 are a subset of the bits of member1. If a flag instance holds the bits of member1 then Flags.is_member returns True and Flags.properties returns the properties of member1 but __len__() returns 2 and __iter__() yields both member0 and member1.

name

properties

Returns Returns None if this flag isn't an exact member of a flags class but a combination of flags,

returns an object holding the properties (e.g.: name, data, index, ...) of the flag otherwise. We don't store flag properties directly in Flags instances because this way Flags instances that are the (temporary) result of flags arithmetic don't have to maintain these fields and it also has some benefits regarding memory usage.

to_simple_str()

class Simulator.**SimulationState**
Simulation state enumeration.

Inheritance

Members

Prepare = 0

Analyze = 1

Elaborate = 2

Optimize = 3

Simulate = 4

View = 5

Coverage = 6

class Simulator.**SimulationResult**
Simulation result enumeration.

Inheritance

Members

NotRun = 0

DryRun = 1

Error = 2

Failed = 3

NoAsserts = 4

Passed = 5

GUIRun = 6

class Simulator.**Simulator**(*host: Base.IHost*, *dryRun*, *simulationSteps: Simulator.SimulationSteps*)
Base class for all Simulator classes.

Inheritance

Members

ENVIRONMENT = 1

VHDL_VERSION = 2008

__init__(*host: Base.IHost*, *dryRun*, *simulationSteps: Simulator.SimulationSteps*)
Class initializer

Parameters

- **host** (*object*) – The hosting instance for this instance.
- **dryRun** (*bool*) – Enable dry-run mode
- **simulationSteps** (SimulationSteps) – A set of simulation step to precess.

TestSuite

_PrepareSimulationEnvironment()

_PrepareEnvironment_PurgeDirectory()

_PrepareSimulator()

RunAll(*fqnList*, **args*, ***kwargs*)
Run a list of testbenches. Expand wildcards to all selected testbenches.

TryRun(*testbench*, **args*, ***kwargs*)
Try to run a testbench. Skip skipable exceptions by printing the error and its cause.

Run(*testbench*, *board*, *vhdlVersion*, *vhdlGenerics=None*)
Write the Testbench message line, create a PoCProject and add the first *.files file to it.

_RunAnalysis(*testbench*)

_RunElaboration(*testbench*)

_RunSimulation(*testbench*)

_RunView(*testbench*)

_RunCoverage(*testbench*)

PrintOverallSimulationReport()

PrintSimulationReportLine(*testObject*, *indent*, *nameColumnWidth*)

Directories

DryRun

Host

Log(*entry*, *condition=True*)
Write an entry to the local logger.

LogDebug(**args*, *condition=True*, ***kwargs*)

LogDryRun(**args*, *condition=True*, ***kwargs*)

LogError(**args*, *condition=True*, ***kwargs*)

LogFatal(**args*, *condition=True*, ***kwargs*)

LogInfo(**args*, *condition=True*, ***kwargs*)

LogNormal(**args*, *condition=True*, ***kwargs*)

LogQuiet(**args*, *condition=True*, ***kwargs*)

LogVerbose(**args*, *condition=True*, ***kwargs*)

LogWarning(**args*, *condition=True*, ***kwargs*)

Logger
Return the local logger instance.

PoCProject

TOOL = 0

TOOL_CHAIN = 0

VHDLVersion

_AddFileListFile(*fileListFilePath*)

_CreatePoCProject(*projectName*, *board*)

_GetHDLParameters(*configSectionName*)
Parse option 'HDLParameters' for Verilog Parameters / VHDL Generics.

_GetTimeDeltaSinceLastEvent()

_Prepare()

_PrepareEnvironment()

_PrepareEnvironment_ChangeDirectory()
Change working directory to temporary path 'temp/<tool>'.

_PrepareEnvironment_CreatingDirectory()

_TryLog(**args*, *condition=True*, ***kwargs*)

Functions

Simulator.**PoCSimulationResultFilter**(*gen*, *simulationResult*)

14.7 ToolChain

Submodules

14.7.1 ToolChain.Aldec

Submodules

ToolChain.Aldec.ActiveHDL

Exceptions

- *ActiveHDLException*: An ActiveHDLException is raised if Active-HDL catches a system exception.

Classes

- *AldecActiveHDLEditions*: Enumeration of all Active-HDL editions provided by Aldec itself.
- *ActiveHDLEditions*: Enumeration of all Active-HDL editions provided by Aldec inclusive editions
- *Configuration*: Base class for all tool Configuration classes.
- *ActiveHDL*: Factory for executable abstractions in Active-HDL.
- *VHDLLibraryTool*: Abstraction layer of Active-HDL's VHDL library management tool 'vlib'.
- *VHDLCompiler*: Abstraction layer of Active-HDL's VHDL compiler 'vcom'.
- *VHDLStandaloneSimulator*: Abstraction layer of Active-HDL's VHDL standalone simulator 'vsimsa'.

Functions

- *VLibFilter()*: A line based output stream filter for Active-HDL's VHDL library management
- *VComFilter()*: A line based output stream filter for Active-HDL's VHDL compiler.
- *VSimFilter()*: A line based output stream filter for Active-HDL's VHDL simulator.

exception ToolChain.Aldec.ActiveHDL.**ActiveHDLException**(*message=''*)
An ActiveHDLException is raised if Active-HDL catches a system exception.

Inheritance

Members

__init__(*message=''*)
Exception initializer

Parameters **message** (*str*) – The exception message.

__str__()
Returns the exception's message text.

args

class ToolChain.Aldec.ActiveHDL.**AldecActiveHDLEditions**(*name*, *section*)
Enumeration of all Active-HDL editions provided by Aldec itself.

Inheritance

Members

StandardEdition = 1

StudentEdition = 2

class ToolChain.Aldec.ActiveHDL.**ActiveHDLEditions**(*name*, *section*)
Enumeration of all Active-HDL editions provided by Aldec inclusive editions shipped by other vendors.

Inheritance

Members

StandardEdition = 1

LatticeEdition = 2

class ToolChain.Aldec.ActiveHDL.**Configuration**(*host: Base.IHost*)

Inheritance

Members

_vendor = 'Aldec'
The name of the tools vendor.

_toolName = 'Aldec Active-HDL'
The name of the tool.

_section = 'INSTALL.Aldec.ActiveHDL'
The name of the configuration section. Pattern: INSTALL.Vendor.ToolName.

_multiVersionSupport = True
Aldec Active-HDL supports multiple versions installed on the same system.

_template = {'Windows': {'INSTALL.Aldec.ActiveHDL': {'Version': '10.3', 'SectionNa
The template for the configuration sections represented as nested dictionaries.

CheckDependency()
Check if general Aldec support is configured in PoC.

ConfigureForAll()
Configuration routine for Aldec Active-HDL on all supported platforms.

1. Ask if Active-HDL is installed.

- Pass → skip this configuration. Don't change existing settings.
- Yes → collect installation information for Active-HDL.
- No → clear the Active-HDL configuration section.

1. Ask for Active-HDL's version.
2. Ask for Active-HDL's edition (normal, student).
3. Ask for Active-HDL's installation directory.

_ConfigureEdition()
Configure Active-HDL for Aldec.

ClearSection(*writeWarnings=False*)
Clear the configuration section associated to this Configuration class.

ConfigureForDarwin()
Start the configuration procedure for Darwin.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Darwin specific configuration routine.

ConfigureForLinux()
Start the configuration procedure for Linux.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Linux specific configuration routine.

ConfigureForWindows()
Start the configuration procedure for Windows.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Windows specific configuration routine.

classmethod GetSections(*platform*)
Return all section names for this configuration.

Host
Return the hosting object.

IsConfigured()
Return true if the configurations section is configured

IsSupportedPlatform()
Return true if the given platform is supported by this configuration routine.

Log(*entry*, *condition=True*)
Write an entry to the local logger.

LogDebug(**args*, *condition=True*, ***kwargs*)

LogDryRun(**args*, *condition=True*, ***kwargs*)

LogError(**args*, *condition=True*, ***kwargs*)

LogFatal(**args*, *condition=True*, ***kwargs*)

LogInfo(**args*, *condition=True*, ***kwargs*)

LogNormal(**args*, *condition=True*, ***kwargs*)

LogQuiet(**args*, *condition=True*, ***kwargs*)

LogVerbose(**args*, *condition=True*, ***kwargs*)

LogWarning(**args*, *condition=True*, ***kwargs*)

Logger
Return the local logger instance.

PrepareOptions(*writeWarnings=True*)

PrepareSections(*warningWasWritten*, *writeWarnings=True*)

PrepareVersionedSections(*writeWarnings=False*)

RunPostConfigurationTasks()
Virtual method. Overwrite to execute post-configuration tasks.

SectionName
Return the configuration's section name.

State
Return the configuration state.

_Ask(*question*, *default*, *beforeDefault=''*, *afterDefault=''*, *indent=1*)

_AskInstalled(*question*)
Ask a Yes/No/Pass question.

_AskYes_NoPass(*question*, *indent=1*)
Ask a yes/NO/pass question.

_Ask_YesNoPass(*question*, *indent=1*)
Ask a YES/no/pass question.

_Configuration__CheckActiveHDLVersion(*binPath*, *version*)
Compare the given Active-HDL version with the tool's version string.

_ConfigureBinaryDirectory()
Updates section with value from `_template` and returns directory as `Path` object.

_ConfigureInstallationDirectory()
Asks for installation directory and updates section. Checks if entered directory exists and returns Path object. If no installation directory was configured before, then _GetDefaultInstallationDir is called.

_ConfigureVersion()
If no version was configured before, then _GetDefaultVersion is called. Asks for version and updates section. Returns version as string.

_GetDefaultEdition()
Returns unresolved default edition (str) from template.

Overwrite this method in a sub-class for automatic search of editions.

_GetDefaultInstallationDirectory()
Return unresolved default installation directory (str) from template.

Overwrite function in sub-class for automatic search of installation directory.

_GetDefaultOptionValue(*optionName*)

_GetDefaultVersion()
Returns unresolved default version (str) from template.

Overwrite this method in a sub-class for automatic search of version.

_PrintAvailableEditions(*editions*, *selectedEdition*)
Print all available editions and return the selected index.

_TestDefaultInstallPath(*defaults*)
Helper function for automatic search of installation directory.

_TryLog(**args*, *condition=True*, ***kwargs*)

class ToolChain.Aldec.ActiveHDL.**ActiveHDL**(*platform*, *dryrun*, *binaryDirectoryPath*, *version*, *logger=None*)

Factory for executable abstractions in Active-HDL.

Inheritance

Members

GetVHDLLibraryTool()
Return an instance of Active-HDL's VHDL library management tool 'vlib'.

GetVHDLCompiler()
Return an instance of Active-HDL's VHDL compiler 'vcom'.

GetSimulator()
Return an instance of Active-HDL's VHDL simulator 'vsim'.

class ToolChain.Aldec.ActiveHDL.**VHDLLibraryTool**(*toolchain: ToolChain.ToolMixIn*)

Abstraction layer of Active-HDL's VHDL library management tool 'vlib'.

Inheritance

Members

class Executable

_value = None

class SwitchLibraryName

_value = None

Parameters = [<class 'ToolChain.Aldec.ActiveHDL.VHDLLibraryTool.Executable'>, <class

CreateLibrary()

GetReader()

HasErrors
True if errors or fatals errors were found while processing the output stream.

HasWarnings
True if errors or fatals errors were found while processing the output stream.

Log(*entry*, *condition=True*)
Write an entry to the local logger.

LogDebug(**args*, *condition=True*, ***kwargs*)

LogDryRun(**args*, *condition=True*, ***kwargs*)

LogError(**args*, *condition=True*, ***kwargs*)

LogFatal(**args*, *condition=True*, ***kwargs*)

LogInfo(**args*, *condition=True*, ***kwargs*)

LogNormal(**args*, *condition=True*, ***kwargs*)

LogQuiet(**args*, *condition=True*, ***kwargs*)

LogVerbose(**args*, *condition=True*, ***kwargs*)

LogWarning(**args*, *condition=True*, ***kwargs*)

Logger
Return the local logger instance.

Path

ReadUntilBoundary(*indent=0*)

Send(*line*, *end='\n'*)

SendBoundary()

StartProcess(*parameterList*)

Terminate()

_POC_BOUNDARY = '====== POC BOUNDARY ======'

_TryLog(**args*, *condition=True*, ***kwargs*)

class ToolChain.Aldec.ActiveHDL.**VHDLCompiler**(*toolchain: ToolChain.ToolMixIn*)
Abstraction layer of Active-HDL's VHDL compiler 'vcom'.

Inheritance

Members

class Executable

_value = None

class FlagNoRangeCheck

_name = 'norangecheck'

_value = None

class SwitchVHDLVersion

_pattern = '-{1}'

_name = ''

_value = None

class SwitchVHDLLibrary

_name = 'work'

_value = None

class ArgSourceFile

_value = None

Parameters = [<class 'ToolChain.Aldec.ActiveHDL.VHDLCompiler.Executable'>, <class '

Compile()

GetReader()

HasErrors
True if errors or fatals errors were found while processing the output stream.

HasWarnings
True if errors or fatals errors were found while processing the output stream.

Log(*entry*, *condition=True*)
Write an entry to the local logger.

LogDebug(**args*, *condition=True*, ***kwargs*)

LogDryRun(**args*, *condition=True*, ***kwargs*)

LogError(**args*, *condition=True*, ***kwargs*)

LogFatal(**args*, *condition=True*, ***kwargs*)

LogInfo(**args*, *condition=True*, ***kwargs*)

LogNormal(**args*, *condition=True*, ***kwargs*)

LogQuiet(**args*, *condition=True*, ***kwargs*)

LogVerbose(**args*, *condition=True*, ***kwargs*)

LogWarning(**args*, *condition=True*, ***kwargs*)

Logger
Return the local logger instance.

Path

ReadUntilBoundary(*indent=0*)

Send(*line*, *end='\n'*)

SendBoundary()

StartProcess(*parameterList*)

Terminate()

_POC_BOUNDARY = '====== POC BOUNDARY ======'

_TryLog(**args*, *condition=True*, ***kwargs*)

class ToolChain.Aldec.ActiveHDL.**VHDLStandaloneSimulator**(*toolchain: ToolChain.ToolMixIn*)
Abstraction layer of Active-HDL's VHDL standalone simulator 'vsimsa'.

Inheritance

Members

class Executable

_value = None

class SwitchBatchCommand

_name = 'do'

_value = None

Parameters = [<class 'ToolChain.Aldec.ActiveHDL.VHDLStandaloneSimulator.Executable'>

Simulate()

GetReader()

HasErrors
True if errors or fatals errors were found while processing the output stream.

HasWarnings
True if errors or fatals errors were found while processing the output stream.

Log(*entry*, *condition=True*)
Write an entry to the local logger.

LogDebug(**args*, *condition=True*, ***kwargs*)

LogDryRun(**args*, *condition=True*, ***kwargs*)

LogError(**args*, *condition=True*, ***kwargs*)

LogFatal(**args*, *condition=True*, ***kwargs*)

LogInfo(**args*, *condition=True*, ***kwargs*)

LogNormal(**args*, *condition=True*, ***kwargs*)

LogQuiet(**args*, *condition=True*, ***kwargs*)

LogVerbose(**args*, *condition=True*, ***kwargs*)

LogWarning(**args*, *condition=True*, ***kwargs*)

Logger
Return the local logger instance.

Path

ReadUntilBoundary(*indent=0*)

Send(*line*, *end='\n'*)

SendBoundary()

StartProcess(*parameterList*)

Terminate()

_POC_BOUNDARY = '====== POC BOUNDARY ======'

_TryLog(**args*, *condition=True*, ***kwargs*)

Functions

ToolChain.Aldec.ActiveHDL.**VLibFilter**(*gen*)
A line based output stream filter for Active-HDL's VHDL library management tool.

ToolChain.Aldec.ActiveHDL.**VComFilter**(*gen*)
A line based output stream filter for Active-HDL's VHDL compiler.

ToolChain.Aldec.ActiveHDL.**VSimFilter**(*gen*)
A line based output stream filter for Active-HDL's VHDL simulator.

ToolChain.Aldec.RivieraPRO

Exceptions

- *RivieraPROException*: An RivieraPROException is raised if Riviera-PRO catches a system exception.

Classes

- *Configuration*: Base class for all tool Configuration classes.
- *RivieraPRO*: Factory for executable abstractions in Riviera-PRO.
- *VHDLLibraryTool*: Abstraction layer of Riviera-PRO's VHDL library management tool 'vlib'.
- *VHDLCompiler*: Abstraction layer of Riviera-PRO's VHDL compiler 'vcom'.
- *VHDLSimulator*: Represent an executable.

Functions

- *VLibFilter()*: A line based output stream filter for Riviera-PRO's VHDL library management tool.

- *VComFilter()*: A line based output stream filter for Riviera-PRO's VHDL compiler.
- *VSimFilter()*: A line based output stream filter for Riviera-PRO's VHDL simulator.

exception ToolChain.Aldec.RivieraPRO.**RivieraPROException**(*message=''*)
An RivieraPROException is raised if Riviera-PRO catches a system exception.

Inheritance

Members

__init__(*message=''*)
Exception initializer

Parameters **message** (*str*) – The exception message.

__str__()
Returns the exception's message text.

args

class ToolChain.Aldec.RivieraPRO.**Configuration**(*host: Base.IHost*)

Inheritance

Members

_vendor = 'Aldec'
The name of the tools vendor.

_toolName = 'Aldec Riviera-PRO'
The name of the tool.

_section = 'INSTALL.Aldec.RivieraPRO'
The name of the configuration section. Pattern: INSTALL.Vendor.ToolName.

_multiVersionSupport = True
Aldec Riviera-PRO supports multiple versions installed on the same system.

_template = {'Linux': {'INSTALL.Aldec.RivieraPRO': {'Version': '2017.02', 'Sectio
The template for the configuration sections represented as nested dictionaries.

CheckDependency()
Check if general Aldec support is configured in PoC.

ConfigureForAll()
Configuration routine for Aldec Riviera-PRO on all supported platforms.

1. Ask if Riviera-PRO is installed.
   - Pass → skip this configuration. Don't change existing settings.
   - Yes → collect installation information for Riviera-PRO.
   - No → clear the Riviera-PRO configuration section.
1. Ask for Riviera-PRO's version.
2. Ask for Riviera-PRO's edition (normal, student).
3. Ask for Riviera-PRO's installation directory.

ClearSection(*writeWarnings=False*)
Clear the configuration section associated to this Configuration class.

ConfigureForDarwin()
Start the configuration procedure for Darwin.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Darwin specific configuration routine.

ConfigureForLinux()
Start the configuration procedure for Linux.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Linux specific configuration routine.

ConfigureForWindows()
Start the configuration procedure for Windows.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Windows specific configuration routine.

classmethod GetSections(*platform*)
Return all section names for this configuration.

Host
Return the hosting object.

IsConfigured()
Return true if the configurations section is configured

IsSupportedPlatform()
Return true if the given platform is supported by this configuration routine.

Log(*entry*, *condition=True*)
Write an entry to the local logger.

LogDebug(**args*, *condition=True*, ***kwargs*)

LogDryRun(**args*, *condition=True*, ***kwargs*)

LogError(**args*, *condition=True*, ***kwargs*)

LogFatal(**args*, *condition=True*, ***kwargs*)

LogInfo(**args*, *condition=True*, ***kwargs*)

LogNormal(**args*, *condition=True*, ***kwargs*)

LogQuiet(**args*, *condition=True*, ***kwargs*)

LogVerbose(**args*, *condition=True*, ***kwargs*)

LogWarning(**args*, *condition=True*, ***kwargs*)

Logger
Return the local logger instance.

PrepareOptions(*writeWarnings=True*)

PrepareSections(*warningWasWritten*, *writeWarnings=True*)

PrepareVersionedSections(*writeWarnings=False*)

RunPostConfigurationTasks()
Virtual method. Overwrite to execute post-configuration tasks.

SectionName
Return the configuration's section name.

State
Return the configuration state.

_Ask(*question*, *default*, *beforeDefault=''*, *afterDefault=''*, *indent=1*)

_AskInstalled(*question*)
Ask a Yes/No/Pass question.

_AskYes_NoPass(*question*, *indent=1*)
Ask a yes/NO/pass question.

_Ask_YesNoPass(*question*, *indent=1*)
Ask a YES/no/pass question.

_Configuration__CheckRivieraPROVersion(*binPath*, *version*)
Compare the given Riviera-PRO version with the tool's version string.

_ConfigureBinaryDirectory()
Updates section with value from `_template` and returns directory as `Path` object.

_ConfigureEdition(*editions*, *defaultEdition*)

_ConfigureInstallationDirectory()
Asks for installation directory and updates section. Checks if entered directory exists and returns Path object. If no installation directory was configured before, then _GetDefaultInstallationDir is called.

_ConfigureVersion()
If no version was configured before, then _GetDefaultVersion is called. Asks for version and updates section. Returns version as string.

_GetDefaultEdition()
Returns unresolved default edition (str) from template.

Overwrite this method in a sub-class for automatic search of editions.

_GetDefaultInstallationDirectory()
Return unresolved default installation directory (str) from template.

Overwrite function in sub-class for automatic search of installation directory.

_GetDefaultOptionValue(*optionName*)

_GetDefaultVersion()
Returns unresolved default version (str) from template.

Overwrite this method in a sub-class for automatic search of version.

_PrintAvailableEditions(*editions*, *selectedEdition*)
Print all available editions and return the selected index.

_TestDefaultInstallPath(*defaults*)
Helper function for automatic search of installation directory.

_TryLog(**args*, *condition=True*, ***kwargs*)

class ToolChain.Aldec.RivieraPRO.**RivieraPRO**(*platform*, *dryrun*, *binaryDirectoryPath*, *version*, *logger=None*)
Factory for executable abstractions in Riviera-PRO.

Inheritance

Members

GetVHDLLibraryTool()
Return an instance of Riviera-PRO's VHDL library management tool 'vlib'.

GetVHDLCompiler()
Return an instance of Riviera-PRO's VHDL compiler 'vcom'.

GetSimulator()
Return an instance of Riviera-PRO's VHDL simulator 'vsim'.

class ToolChain.Aldec.RivieraPRO.**VHDLLibraryTool**(*toolchain: ToolChain.ToolMixIn*)

Abstraction layer of Riviera-PRO's VHDL library management tool 'vlib'.

Inheritance

Members

class Executable

_value = None

class SwitchLibraryName

_value = None

Parameters = [<class 'ToolChain.Aldec.RivieraPRO.VHDLLibraryTool.Executable'>, <clas

CreateLibrary()

GetReader()

HasErrors
True if errors or fatals errors were found while processing the output stream.

HasWarnings
True if errors or fatals errors were found while processing the output stream.

Log(*entry*, *condition=True*)
Write an entry to the local logger.

LogDebug(**args*, *condition=True*, ***kwargs*)

LogDryRun(**args*, *condition=True*, ***kwargs*)

LogError(**args*, *condition=True*, ***kwargs*)

LogFatal(**args*, *condition=True*, ***kwargs*)

LogInfo(**args*, *condition=True*, ***kwargs*)

LogNormal(**args*, *condition=True*, ***kwargs*)

LogQuiet(**args*, *condition=True*, ***kwargs*)

LogVerbose(**args*, *condition=True*, ***kwargs*)

LogWarning(**args*, *condition=True*, ***kwargs*)

Logger
Return the local logger instance.

Path

ReadUntilBoundary(*indent=0*)

Send(*line*, *end='\n'*)

SendBoundary()

StartProcess(*parameterList*)

Terminate()

_POC_BOUNDARY = '====== POC BOUNDARY ======'

_TryLog(**args*, *condition=True*, ***kwargs*)

class ToolChain.Aldec.RivieraPRO.**VHDLCompiler**(*toolchain: ToolChain.ToolMixIn*)
Abstraction layer of Riviera-PRO's VHDL compiler 'vcom'.

Inheritance

Members

class Executable

_value = None

class SwitchVHDLVersion

_pattern = '-{1}'

_name = ''

_value = None

class SwitchVHDLLibrary

_name = 'work'

_value = None

class ArgSourceFile

_value = None

Parameters = [<class 'ToolChain.Aldec.RivieraPRO.VHDLCompiler.Executable'>, <class

Compile()

GetReader()

HasErrors
True if errors or fatals errors were found while processing the output stream.

HasWarnings
True if errors or fatals errors were found while processing the output stream.

Log(*entry*, *condition=True*)
Write an entry to the local logger.

LogDebug(**args*, *condition=True*, ***kwargs*)

LogDryRun(**args*, *condition=True*, ***kwargs*)

LogError(**args*, *condition=True*, ***kwargs*)

LogFatal(**args*, *condition=True*, ***kwargs*)

LogInfo(**args*, *condition=True*, ***kwargs*)

LogNormal(**args*, *condition=True*, ***kwargs*)

LogQuiet(**args*, *condition=True*, ***kwargs*)

LogVerbose(**args*, *condition=True*, ***kwargs*)

LogWarning(**args*, *condition=True*, ***kwargs*)

Logger
Return the local logger instance.

Path

ReadUntilBoundary(*indent=0*)

Send(*line*, *end='\n'*)

SendBoundary()

StartProcess(*parameterList*)

Terminate()

_POC_BOUNDARY = '====== POC BOUNDARY ======'

_TryLog(**args*, *condition=True*, ***kwargs*)

class ToolChain.Aldec.RivieraPRO.**VHDLSimulator**(*toolchain: ToolChain.ToolMixIn*)

Inheritance

Members

class Executable
The executable to launch.

_value = None

class SwitchBatchCommand
Specify a Tcl batch script for the batch mode.

_name = 'do'

_value = None

class FlagCommandLineMode
Run simulation in command line mode.

_name = 'c'

_value = None

class SwitchTimeResolution
Set simulation time resolution.

_name = 't'

_value = None

class SwitchTopLevel
The top-level for simulation.

_value = None

Parameters = [<class 'ToolChain.Aldec.RivieraPRO.VHDLSimulator.Executable'>, <class
Specify all accepted command line arguments

Simulate()
Start a simulation.

GetReader()

HasErrors
True if errors or fatals errors were found while processing the output stream.

HasWarnings
True if errors or fatals errors were found while processing the output stream.

Log(*entry*, *condition=True*)
Write an entry to the local logger.

LogDebug(**args*, *condition=True*, ***kwargs*)

LogDryRun(**args*, *condition=True*, ***kwargs*)

LogError(**args*, *condition=True*, ***kwargs*)

LogFatal(**args*, *condition=True*, ***kwargs*)

LogInfo(**args*, *condition=True*, ***kwargs*)

LogNormal(**args*, *condition=True*, ***kwargs*)

LogQuiet(**args*, *condition=True*, ***kwargs*)

LogVerbose(**args*, *condition=True*, ***kwargs*)

LogWarning(**args*, *condition=True*, ***kwargs*)

Logger
Return the local logger instance.

Path

ReadUntilBoundary(*indent=0*)

Send(*line*, *end='\n'*)

SendBoundary()

StartProcess(*parameterList*)

Terminate()

_POC_BOUNDARY = '====== POC BOUNDARY ======'

_TryLog(**args*, *condition=True*, ***kwargs*)

Functions

ToolChain.Aldec.RivieraPRO.**VLibFilter**(*gen*)
A line based output stream filter for Riviera-PRO's VHDL library management tool.

ToolChain.Aldec.RivieraPRO.**VComFilter**(*gen*)
A line based output stream filter for Riviera-PRO's VHDL compiler.

ToolChain.Aldec.RivieraPRO.**VSimFilter**(*gen*)
A line based output stream filter for Riviera-PRO's VHDL simulator.

Exceptions

- *AldecException*: Base class for all Aldec tool's exceptions.

Classes

- *Configuration*: Configuration routines for Aldec as a vendor.

exception ToolChain.Aldec.**AldecException**(*message=''*)
Base class for all Aldec tool's exceptions.

Inheritance

Members

__init__(*message=''*)
Exception initializer

Parameters **message** (*str*) – The exception message.

__str__()
Returns the exception's message text.

args

class ToolChain.Aldec.**Configuration**(*host: Base.IHost*)
Configuration routines for Aldec as a vendor.

This configuration provides a common installation directory setup for all Aldec tools installed on a system.

Inheritance

Members

_vendor = 'Aldec'
The name of the tools vendor.

_section = 'INSTALL.Aldec'
The name of the configuration section. Pattern: INSTALL.Vendor.ToolName.

_template = {'ALL': {'INSTALL.ActiveHDL': {'SectionName': '', 'Version': '${${Se
The template for the configuration sections represented as nested dictionaries.

ConfigureForAll()
Start a generic (platform independent) vendor configuration procedure.

This method configures a vendor path. Overwrite this method to implement a vendor specific configuration routine for a vendor Configuration class.

_GetDefaultInstallationDirectory()
Return unresolved default installation directory (str) from template.

Overwrite function in sub-class for automatic search of installation directory.

CheckDependency()
Check if all vendor or tool dependencies are fulfilled to configure this tool.

ClearSection(*writeWarnings=False*)
Clear the configuration section associated to this Configuration class.

ConfigureForDarwin()
Start the configuration procedure for Darwin.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Darwin specific configuration routine.

ConfigureForLinux()
Start the configuration procedure for Linux.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Linux specific configuration routine.

ConfigureForWindows()
Start the configuration procedure for Windows.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Windows specific configuration routine.

classmethod GetSections(*platform*)
Return all section names for this configuration.

Host
Return the hosting object.

IsConfigured()
Return true if the configurations section is configured

IsSupportedPlatform()
Return true if the given platform is supported by this configuration routine.

Log(*entry*, *condition=True*)
Write an entry to the local logger.

LogDebug(**args*, *condition=True*, ***kwargs*)

LogDryRun(**args*, *condition=True*, ***kwargs*)

LogError(**args*, *condition=True*, ***kwargs*)

LogFatal(**args*, *condition=True*, ***kwargs*)

LogInfo(**args*, *condition=True*, ***kwargs*)

LogNormal(**args*, *condition=True*, ***kwargs*)

LogQuiet(**args*, *condition=True*, ***kwargs*)

LogVerbose(**args*, *condition=True*, ***kwargs*)

LogWarning(**args*, *condition=True*, ***kwargs*)

Logger
Return the local logger instance.

PrepareOptions(*writeWarnings=True*)

PrepareSections(*warningWasWritten*, *writeWarnings=True*)

RunPostConfigurationTasks()
Virtual method. Overwrite to execute post-configuration tasks.

SectionName
Return the configuration's section name.

State
Return the configuration state.

_Ask(*question*, *default*, *beforeDefault=''*, *afterDefault=''*, *indent=1*)

_AskInstalled(*question*)
Ask a Yes/No/Pass question.

_AskYes_NoPass(*question*, *indent=1*)
Ask a yes/NO/pass question.

_Ask_YesNoPass(*question*, *indent=1*)
Ask a YES/no/pass question.

_ConfigureInstallationDirectory()
Asks for installation directory and updates section. Checks if entered directory exists and returns Path object. If no installation directory was configured before, then _GetDefaultInstallationDir is called.

_GetDefaultOptionValue(*optionName*)

_PrintAvailableEditions(*editions*, *selectedEdition*)
Print all available editions and return the selected index.

_TestDefaultInstallPath(*defaults*)
Helper function for automatic search of installation directory.

_TryLog(**args*, *condition=True*, ***kwargs*)

_multiVersionSupport = False

14.7.2 ToolChain.Altera

Submodules

ToolChain.Altera.ModelSim

Exceptions

- *ModelSimException*: Base class for all tool specific exceptions

Classes

- *AlteraModelSimEditions*: Enumeration of all ModelSim editions provided by Altera.
- *Configuration*: Base class for all tool Configuration classes.
- *AlteraEditionConfiguration*: Base class for all tool Configuration classes.
- *AlteraStarterEditionConfiguration*: Base class for all tool Configuration classes.

exception ToolChain.Altera.ModelSim.**ModelSimException**(*message=''*)

Inheritance

Members

__init__(*message=''*)
Exception initializer

Parameters **message** (*str*) – The exception message.

__str__()
Returns the exception's message text.

args

class ToolChain.Altera.ModelSim.**AlteraModelSimEditions**(*name*, *section*)
Enumeration of all ModelSim editions provided by Altera.

Inheritance

Members

ModelSimAlteraEdition = 1

ModelSimAlteraStarterEdition = 2

class ToolChain.Altera.ModelSim.**Configuration**(*host: Base.IHost*)

Inheritance

Members

_vendor = 'Altera'
The name of the tools vendor.

_multiVersionSupport = False
ModelSim Altera (Starter) Edition doesn't support multiple versions.

CheckDependency()
Check if general Altera support is configured in PoC.

ConfigureForAll()
Configuration routine for Mentor Graphics ModelSim on all supported platforms.

1. Ask if ModelSim is installed.

- Pass → skip this configuration. Don't change existing settings.
- Yes → collect installation information for ModelSim.
- No → clear the ModelSim configuration section.

1. Ask for ModelSim's version.
2. Ask for ModelSim's edition (PE, PE student, SE 32-bit, SE 64-bit).
3. Ask for ModelSim's installation directory.

_ConfigureEdition()
Configure ModelSim for Altera.

ClearSection(*writeWarnings=False*)
Clear the configuration section associated to this Configuration class.

ConfigureForDarwin()
Start the configuration procedure for Darwin.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Darwin specific configuration routine.

ConfigureForLinux()
Start the configuration procedure for Linux.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Linux specific configuration routine.

ConfigureForWindows()
Start the configuration procedure for Windows.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Windows specific configuration routine.

classmethod GetSections(*platform*)
Return all section names for this configuration.

Host
Return the hosting object.

IsConfigured()
Return true if the configurations section is configured

IsSupportedPlatform()
Return true if the given platform is supported by this configuration routine.

Log(*entry*, *condition=True*)
Write an entry to the local logger.

LogDebug(**args*, *condition=True*, ***kwargs*)

LogDryRun(**args*, *condition=True*, ***kwargs*)

LogError(**args*, *condition=True*, ***kwargs*)

LogFatal(**args*, *condition=True*, ***kwargs*)

LogInfo(**args*, *condition=True*, ***kwargs*)

LogNormal(**args*, *condition=True*, ***kwargs*)

LogQuiet(**args*, *condition=True*, ***kwargs*)

LogVerbose(**args*, *condition=True*, ***kwargs*)

LogWarning(**args*, *condition=True*, ***kwargs*)

Logger
Return the local logger instance.

PrepareOptions(*writeWarnings=True*)

PrepareSections(*warningWasWritten*, *writeWarnings=True*)

PrepareVersionedSections(*writeWarnings=False*)

RunPostConfigurationTasks()
Virtual method. Overwrite to execute post-configuration tasks.

SectionName
Return the configuration's section name.

State
Return the configuration state.

_Ask(*question*, *default*, *beforeDefault=''*, *afterDefault=''*, *indent=1*)

_AskInstalled(*question*)
Ask a Yes/No/Pass question.

_AskYes_NoPass(*question*, *indent=1*)
Ask a yes/NO/pass question.

_Ask_YesNoPass(*question*, *indent=1*)
Ask a YES/no/pass question.

_CheckModelSimVersion(*binPath*, *version*)

_Configuration__GetModelSimVersion(*binPath*)

_ConfigureBinaryDirectory()
Updates section with value from `_template` and returns directory as `Path` object.

_ConfigureInstallationDirectory()
Asks for installation directory and updates section. Checks if entered directory exists and returns Path object. If no installation directory was configured before, then _GetDefaultInstallationDir is called.

_ConfigureVersion()
If no version was configured before, then _GetDefaultVersion is called. Asks for version and updates section. Returns version as string.

_GetDefaultEdition()
Returns unresolved default edition (str) from template.

Overwrite this method in a sub-class for automatic search of editions.

_GetDefaultInstallationDirectory()
Return unresolved default installation directory (str) from template.

Overwrite function in sub-class for automatic search of installation directory.

_GetDefaultOptionValue(*optionName*)

_GetDefaultVersion()
Returns unresolved default version (str) from template.

Overwrite this method in a sub-class for automatic search of version.

_GetModelSimVersion(*binPath*)

_PrintAvailableEditions(*editions*, *selectedEdition*)
Print all available editions and return the selected index.

_TestDefaultInstallPath(*defaults*)
Helper function for automatic search of installation directory.

_TryLog(**args*, *condition=True*, ***kwargs*)

_section = 'INSTALL.Vendor.Tool'

_template = {'ALL': {'INSTALL.Vendor.Tool': {'Version': '1.0'}}, 'Darwin': {'INST

_toolName = 'Mentor ModelSim'

class ToolChain.Altera.ModelSim.**AlteraEditionConfiguration**(*host: Base.IHost*)

Inheritance

Members

_toolName = 'Altera ModelSim'
The name of the tool.

__editionName = None
The name of the tool.

_section = 'INSTALL.Altera.ModelSimAE'
The name of the configuration section. Pattern: INSTALL.Vendor.ToolName.

_template = {'Linux': {'INSTALL.Altera.ModelSimAE': {'Version': '10.5b', 'Edition

CheckDependency()
Check if general Altera support is configured in PoC.

ClearSection(*writeWarnings=False*)
Clear the configuration section associated to this Configuration class.

ConfigureForAll()
Configuration routine for Mentor Graphics ModelSim on all supported platforms.

1. Ask if ModelSim is installed.

- Pass → skip this configuration. Don't change existing settings.
- Yes → collect installation information for ModelSim.
- No → clear the ModelSim configuration section.

1. Ask for ModelSim's version.
2. Ask for ModelSim's edition (PE, PE student, SE 32-bit, SE 64-bit).
3. Ask for ModelSim's installation directory.

ConfigureForDarwin()
Start the configuration procedure for Darwin.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Darwin specific configuration routine.

ConfigureForLinux()
Start the configuration procedure for Linux.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Linux specific configuration routine.

ConfigureForWindows()
Start the configuration procedure for Windows.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Windows specific configuration routine.

classmethod GetSections(*platform*)
Return all section names for this configuration.

Host
Return the hosting object.

IsConfigured()
Return true if the configurations section is configured

IsSupportedPlatform()
Return true if the given platform is supported by this configuration routine.

Log(*entry*, *condition=True*)
Write an entry to the local logger.

LogDebug(**args*, *condition=True*, ***kwargs*)

LogDryRun(**args*, *condition=True*, ***kwargs*)

LogError(**args*, *condition=True*, ***kwargs*)

LogFatal(**args*, *condition=True*, ***kwargs*)

LogInfo(**args*, *condition=True*, ***kwargs*)

LogNormal(**args*, *condition=True*, ***kwargs*)

LogQuiet(**args*, *condition=True*, ***kwargs*)

LogVerbose(**args*, *condition=True*, ***kwargs*)

LogWarning(**args*, *condition=True*, ***kwargs*)

Logger
Return the local logger instance.

PrepareOptions(*writeWarnings=True*)

PrepareSections(*warningWasWritten*, *writeWarnings=True*)

PrepareVersionedSections(*writeWarnings=False*)

RunPostConfigurationTasks()
Virtual method. Overwrite to execute post-configuration tasks.

SectionName
Return the configuration's section name.

State
Return the configuration state.

_AlteraEditionConfiguration__editionName = 'ModelSim Altera Edition'

_Ask(*question*, *default*, *beforeDefault=''*, *afterDefault=''*, *indent=1*)

_AskInstalled(*question*)
Ask a Yes/No/Pass question.

_AskYes_NoPass(*question*, *indent=1*)
Ask a yes/NO/pass question.

_Ask_YesNoPass(*question*, *indent=1*)
Ask a YES/no/pass question.

_CheckModelSimVersion(*binPath*, *version*)

_Configuration__GetModelSimVersion(*binPath*)

_ConfigureBinaryDirectory()
Updates section with value from `_template` and returns directory as `Path` object.

_ConfigureEdition()
Configure ModelSim for Altera.

_ConfigureInstallationDirectory()
Asks for installation directory and updates section. Checks if entered directory exists and returns Path object. If no installation directory was configured before, then _GetDefaultInstallationDir is called.

_ConfigureVersion()
If no version was configured before, then _GetDefaultVersion is called. Asks for version and updates section. Returns version as string.

_GetDefaultEdition()
Returns unresolved default edition (str) from template.

Overwrite this method in a sub-class for automatic search of editions.

_GetDefaultInstallationDirectory()
Return unresolved default installation directory (str) from template.

Overwrite function in sub-class for automatic search of installation directory.

_GetDefaultOptionValue(*optionName*)

_GetDefaultVersion()
Returns unresolved default version (str) from template.

Overwrite this method in a sub-class for automatic search of version.

_GetModelSimVersion(*binPath*)

_PrintAvailableEditions(*editions*, *selectedEdition*)
Print all available editions and return the selected index.

_TestDefaultInstallPath(*defaults*)
Helper function for automatic search of installation directory.

_TryLog(**args*, *condition=True*, ***kwargs*)

_multiVersionSupport = False

_vendor = 'Altera'

class ToolChain.Altera.ModelSim.**AlteraStarterEditionConfiguration**(*host: Base.IHost*)

Inheritance

Members

_toolName = 'Altera ModelSim (Starter Edition)'
The name of the tool.

__editionName = None
The name of the tool.

_section = 'INSTALL.Altera.ModelSimASE'
The name of the configuration section. Pattern: `INSTALL.Vendor.ToolName`.

_template = {'Linux': {'INSTALL.Altera.ModelSimASE': {'Version': '10.5b', 'Editio

CheckDependency()
Check if general Altera support is configured in PoC.

ClearSection(*writeWarnings=False*)
Clear the configuration section associated to this Configuration class.

ConfigureForAll()
Configuration routine for Mentor Graphics ModelSim on all supported platforms.

1. Ask if ModelSim is installed.

- Pass → skip this configuration. Don't change existing settings.
- Yes → collect installation information for ModelSim.

- No → clear the ModelSim configuration section.

1. Ask for ModelSim's version.
2. Ask for ModelSim's edition (PE, PE student, SE 32-bit, SE 64-bit).
3. Ask for ModelSim's installation directory.

ConfigureForDarwin()
Start the configuration procedure for Darwin.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Darwin specific configuration routine.

ConfigureForLinux()
Start the configuration procedure for Linux.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Linux specific configuration routine.

ConfigureForWindows()
Start the configuration procedure for Windows.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Windows specific configuration routine.

classmethod GetSections(*platform*)
Return all section names for this configuration.

Host
Return the hosting object.

IsConfigured()
Return true if the configurations section is configured

IsSupportedPlatform()
Return true if the given platform is supported by this configuration routine.

Log(*entry*, *condition=True*)
Write an entry to the local logger.

LogDebug(**args*, *condition=True*, ***kwargs*)

LogDryRun(**args*, *condition=True*, ***kwargs*)

LogError(**args*, *condition=True*, ***kwargs*)

LogFatal(**args*, *condition=True*, ***kwargs*)

LogInfo(**args*, *condition=True*, ***kwargs*)

LogNormal(**args*, *condition=True*, ***kwargs*)

LogQuiet(**args*, *condition=True*, ***kwargs*)

LogVerbose(**args*, *condition=True*, ***kwargs*)

LogWarning(**args*, *condition=True*, ***kwargs*)

Logger
Return the local logger instance.

PrepareOptions(*writeWarnings=True*)

PrepareSections(*warningWasWritten*, *writeWarnings=True*)

PrepareVersionedSections(*writeWarnings=False*)

RunPostConfigurationTasks()
Virtual method. Overwrite to execute post-configuration tasks.

SectionName
Return the configuration's section name.

State
Return the configuration state.

_AlteraStarterEditionConfiguration__editionName = 'ModelSim Altera Starter Edition'

_Ask(*question*, *default*, *beforeDefault=''*, *afterDefault=''*, *indent=1*)

_AskInstalled(*question*)
Ask a Yes/No/Pass question.

_AskYes_NoPass(*question*, *indent=1*)
Ask a yes/NO/pass question.

_Ask_YesNoPass(*question*, *indent=1*)
Ask a YES/no/pass question.

_CheckModelSimVersion(*binPath*, *version*)

_Configuration__GetModelSimVersion(*binPath*)

_ConfigureBinaryDirectory()
Updates section with value from *_template* and returns directory as Path object.

_ConfigureEdition()
Configure ModelSim for Altera.

_ConfigureInstallationDirectory()
Asks for installation directory and updates section. Checks if entered directory exists and returns Path object. If no installation directory was configured before, then _GetDefaultInstallationDir is called.

_ConfigureVersion()
If no version was configured before, then _GetDefaultVersion is called. Asks for version and updates section. Returns version as string.

_GetDefaultEdition()
Returns unresolved default edition (str) from template.

Overwrite this method in a sub-class for automatic search of editions.

_GetDefaultInstallationDirectory()
Return unresolved default installation directory (str) from template.

Overwrite function in sub-class for automatic search of installation directory.

_GetDefaultOptionValue(*optionName*)

_GetDefaultVersion()
Returns unresolved default version (str) from template.

Overwrite this method in a sub-class for automatic search of version.

_GetModelSimVersion(*binPath*)

_PrintAvailableEditions(*editions*, *selectedEdition*)
Print all available editions and return the selected index.

_TestDefaultInstallPath(*defaults*)
Helper function for automatic search of installation directory.

_TryLog(**args*, *condition=True*, ***kwargs*)

_multiVersionSupport = False

_vendor = 'Altera'

ToolChain.Altera.Quartus

Exceptions

- *QuartusException*: Base class for all tool specific exceptions

Classes

- *QuartusEditions*: Enumeration of all Quartus editions provided by Altera itself.
- *Configuration*: Base class for all tool Configuration classes.
- *Quartus*: Undocumented.
- *Map*: Represent an executable.
- *TclShell*: Represent an executable.
- *QuartusSession*: Undocumented.
- *QuartusProject*: Undocumented.
- *QuartusSettings*: Undocumented.
- *QuartusProjectFile*: Undocumented.

Functions

- *MapFilter()*: Undocumented.

exception ToolChain.Altera.Quartus.**QuartusException**(*message=''*)

Inheritance

Members

__init__(*message=''*)
Exception initializer

Parameters **message** (*str*) – The exception message.

__str__()
Returns the exception's message text.

args

class ToolChain.Altera.Quartus.**QuartusEditions**(*name*, *section*)
Enumeration of all Quartus editions provided by Altera itself.

Inheritance

Members

AlteraQuartus = 1

IntelQuartus = 2

class ToolChain.Altera.Quartus.**Configuration**(*host: Base.IHost*)

Inheritance

Members

_vendor = 'Altera'
The name of the tools vendor.

_toolName = 'Altera Quartus'
The name of the tool.

_section = 'INSTALL.Altera.Quartus'
The name of the configuration section. Pattern: `INSTALL.Vendor.ToolName`.

_multiVersionSupport = True
Altera Quartus supports multiple versions installed on the same system.

_template = {'Linux': {'INSTALL.Altera.Quartus': {'Version': '16.0', 'SectionName
The template for the configuration sections represented as nested dictionaries.

CheckDependency()
Check if general Altera support is configured in PoC.

ConfigureForAll()
Start a generic (platform independent) configuration procedure.

Overwrite this method to implement a generic configuration routine for a (tool) Configuration class.

ClearSection(*writeWarnings=False*)
Clear the configuration section associated to this Configuration class.

ConfigureForDarwin()
Start the configuration procedure for Darwin.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Darwin specific configuration routine.

ConfigureForLinux()
Start the configuration procedure for Linux.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Linux specific configuration routine.

ConfigureForWindows()
Start the configuration procedure for Windows.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Windows specific configuration routine.

classmethod GetSections(*platform*)
Return all section names for this configuration.

Host
Return the hosting object.

IsConfigured()
Return true if the configurations section is configured

IsSupportedPlatform()
Return true if the given platform is supported by this configuration routine.

Log(*entry*, *condition=True*)
Write an entry to the local logger.

LogDebug(**args*, *condition=True*, ***kwargs*)

LogDryRun(**args*, *condition=True*, ***kwargs*)

LogError(**args*, *condition=True*, ***kwargs*)

LogFatal(**args*, *condition=True*, ***kwargs*)

LogInfo(**args*, *condition=True*, ***kwargs*)

LogNormal(**args*, *condition=True*, ***kwargs*)

LogQuiet(**args*, *condition=True*, ***kwargs*)

LogVerbose(**args*, *condition=True*, ***kwargs*)

LogWarning(**args*, *condition=True*, ***kwargs*)

Logger
Return the local logger instance.

PrepareOptions(*writeWarnings=True*)

PrepareSections(*warningWasWritten*, *writeWarnings=True*)

PrepareVersionedSections(*writeWarnings=False*)

RunPostConfigurationTasks()
Virtual method. Overwrite to execute post-configuration tasks.

SectionName
Return the configuration's section name.

State
Return the configuration state.

_Ask(*question*, *default*, *beforeDefault=''*, *afterDefault=''*, *indent=1*)

_AskInstalled(*question*)
Ask a Yes/No/Pass question.

_AskYes_NoPass(*question*, *indent=1*)
Ask a yes/NO/pass question.

_Ask_YesNoPass(*question*, *indent=1*)
Ask a YES/no/pass question.

_Configuration__CheckQuartusVersion(*binPath*, *version*)

_ConfigureBinaryDirectory()
Updates section with value from `_template` and returns directory as `Path` object.

_ConfigureEdition(*editions*, *defaultEdition*)

_ConfigureInstallationDirectory()
Asks for installation directory and updates section. Checks if entered directory exists and returns Path object. If no installation directory was configured before, then _GetDefaultInstallationDir is called.

_ConfigureVersion()
If no version was configured before, then _GetDefaultVersion is called. Asks for version and updates section. Returns version as string.

_GetDefaultEdition()
Returns unresolved default edition (str) from template.

Overwrite this method in a sub-class for automatic search of editions.

_GetDefaultInstallationDirectory()
Return unresolved default installation directory (str) from template.

Overwrite function in sub-class for automatic search of installation directory.

_GetDefaultOptionValue(*optionName*)

_GetDefaultVersion()
Returns unresolved default version (str) from template.

Overwrite this method in a sub-class for automatic search of version.

_PrintAvailableEditions(*editions*, *selectedEdition*)
Print all available editions and return the selected index.

_TestDefaultInstallPath(*defaults*)
Helper function for automatic search of installation directory.

_TryLog(**args*, *condition=True*, ***kwargs*)

class ToolChain.Altera.Quartus.**Quartus**(*platform*, *dryrun*, *binaryDirectoryPath*, *version*, *logger=None*)

Inheritance

Members

GetMap()

GetTclShell()

class ToolChain.Altera.Quartus.**Map**(*toolchain: ToolChain.ToolMixIn*)

Inheritance

Members

class Executable

class ArgProjectName

class SwitchArgumentFile

```
    _name = 'f'
```

class SwitchDeviceFamily

```
    _name = 'family'
```

class SwitchDevicePart

```
    _name = 'part'
```

```
Parameters = [<class 'ToolChain.Altera.Quartus.Map.Executable'>, <class 'ToolChain.A
```

Compile()

GetReader()

HasErrors
True if errors or fatals errors were found while processing the output stream.

HasWarnings
True if errors or fatals errors were found while processing the output stream.

Log(*entry*, *condition=True*)
Write an entry to the local logger.

LogDebug(**args*, *condition=True*, ***kwargs*)

LogDryRun(**args*, *condition=True*, ***kwargs*)

LogError(**args*, *condition=True*, ***kwargs*)

LogFatal(**args*, *condition=True*, ***kwargs*)

LogInfo(**args*, *condition=True*, ***kwargs*)

LogNormal(**args*, *condition=True*, ***kwargs*)

LogQuiet(**args*, *condition=True*, ***kwargs*)

LogVerbose(**args*, *condition=True*, ***kwargs*)

LogWarning(**args*, *condition=True*, ***kwargs*)

Logger
Return the local logger instance.

Path

ReadUntilBoundary(*indent=0*)

Send(*line*, *end='\n'*)

SendBoundary()

StartProcess(*parameterList*)

Terminate()

_POC_BOUNDARY = '====== POC BOUNDARY ======'

_TryLog(**args*, *condition=True*, ***kwargs*)

class ToolChain.Altera.Quartus.**TclShell**(*toolchain: ToolChain.ToolMixIn*)

Inheritance

Members

class Executable

class SwitchShell

_name = 's'

Parameters = [<class 'ToolChain.Altera.Quartus.TclShell.Executable'>, <class 'ToolCh

GetReader()

Log(*entry*, *condition=True*)
Write an entry to the local logger.

LogDebug(**args*, *condition=True*, ***kwargs*)

LogDryRun(**args*, *condition=True*, ***kwargs*)

LogError(**args*, *condition=True*, ***kwargs*)

LogFatal(**args*, *condition=True*, ***kwargs*)

LogInfo(**args*, *condition=True*, ***kwargs*)

LogNormal(**args*, *condition=True*, ***kwargs*)

LogQuiet(**args*, *condition=True*, ***kwargs*)

LogVerbose(**args*, *condition=True*, ***kwargs*)

LogWarning(**args*, *condition=True*, ***kwargs*)

Logger
Return the local logger instance.

Path

ReadUntilBoundary(*indent=0*)

Send(*line*, *end='\n'*)

SendBoundary()

StartProcess(*parameterList*)

Terminate()

_POC_BOUNDARY = '====== POC BOUNDARY ======'

_TryLog(**args*, *condition=True*, ***kwargs*)

class ToolChain.Altera.Quartus.**QuartusSession**(*host*)

Inheritance

Members

exit()

class ToolChain.Altera.Quartus.**QuartusProject**(*host*, *name*, *projectFile=None*)

Inheritance

Members

Create(*session=None*)

Save(*session*)

Read()

Open(*session*)

Close(*session*)

AddExternalVHDLLibraries(*library*)

AddFile(*file*, *fileSet=None*)

AddFileSet(*fileSet*)

AddSourceFile(*file*, *fileSet=None*)

Board

CreateFileSet(*name*, *setDefault=True*)

DefaultFileSet

Device

Environment

ExternalVHDLLibraries

ExtractVHDLLibrariesFromVHDLSourceFiles()

FileSets

Files(*fileType=<FileTypes(Text|ProjectFile|FileListFile|RulesFile|SourceFile|VHDLSourceFile|VerilogSourceFile|Python*
bits=0xFFFF>, *fileSet=None*)

GetVariables()

Name

RootDirectory

Tool

ToolChain

VHDLLibraries

VHDLVersion

pprint(*indent=0*)

class ToolChain.Altera.Quartus.**QuartusSettings**(*name*, *settingsFile=None*)

Inheritance

Members

File

GlobalAssignments

Parameters

CopySourceFilesFromProject(*project*)

Write()

FileName

FileSet

FileType

Open()

Path

Project

ReadFile()

_FileType = <FileTypes.SettingsFile bits=0x4000 data=UNDEFINED>

_ReadContent()

class ToolChain.Altera.Quartus.**QuartusProjectFile**(*file*)

Inheritance

Members

FileName

FileSet

FileType

Open()

Path

Project

ReadFile()

_FileType = <FileTypes.ProjectFile bits=0x0002 data=UNDEFINED>

_ReadContent()

Functions

ToolChain.Altera.Quartus.**MapFilter**(*gen*)

Exceptions

- *AlteraException*: Base class for all tool specific exceptions

Classes

- *Configuration*: Configuration routines for Altera as a vendor.

exception ToolChain.Altera.**AlteraException**(*message=''*)

Inheritance

Members

__init__(*message=''*)
Exception initializer

Parameters **message** (*str*) – The exception message.

__str__()
Returns the exception's message text.

args

class ToolChain.Altera.**Configuration**(*host: Base.IHost*)
Configuration routines for Altera as a vendor.

This configuration provides a common installation directory setup for all Altera tools installed on a system.

Inheritance

Members

_vendor = 'Altera'
The name of the tools vendor.

_section = 'INSTALL.Altera'
The name of the configuration section. Pattern: INSTALL.Vendor.ToolName.

_template = {'ALL': {'INSTALL.Quartus': {'SectionName': '', 'Version': '${${Sect
The template for the configuration sections represented as nested dictionaries.

_GetDefaultInstallationDirectory()
Return default installation directory (str).

CheckDependency()
Check if all vendor or tool dependencies are fulfilled to configure this tool.

ClearSection(*writeWarnings=False*)
Clear the configuration section associated to this Configuration class.

ConfigureForAll()
Start a generic (platform independent) vendor configuration procedure.

This method configures a vendor path. Overwrite this method to implement a vendor specific configuration routine for a vendor Configuration class.

ConfigureForDarwin()
Start the configuration procedure for Darwin.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Darwin specific configuration routine.

ConfigureForLinux()
Start the configuration procedure for Linux.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Linux specific configuration routine.

ConfigureForWindows()
Start the configuration procedure for Windows.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Windows specific configuration routine.

classmethod GetSections(*platform*)
Return all section names for this configuration.

Host
Return the hosting object.

IsConfigured()
Return true if the configurations section is configured

IsSupportedPlatform()
Return true if the given platform is supported by this configuration routine.

Log(*entry*, *condition=True*)
Write an entry to the local logger.

LogDebug(**args*, *condition=True*, ***kwargs*)

LogDryRun(**args*, *condition=True*, ***kwargs*)

LogError(**args*, *condition=True*, ***kwargs*)

LogFatal(**args*, *condition=True*, ***kwargs*)

LogInfo(**args*, *condition=True*, ***kwargs*)

LogNormal(**args*, *condition=True*, ***kwargs*)

LogQuiet(**args*, *condition=True*, ***kwargs*)

LogVerbose(**args*, *condition=True*, ***kwargs*)

LogWarning(**args*, *condition=True*, ***kwargs*)

Logger
Return the local logger instance.

PrepareOptions(*writeWarnings=True*)

PrepareSections(*warningWasWritten*, *writeWarnings=True*)

RunPostConfigurationTasks()
Virtual method. Overwrite to execute post-configuration tasks.

SectionName
Return the configuration's section name.

State
Return the configuration state.

_Ask(*question*, *default*, *beforeDefault=''*, *afterDefault=''*, *indent=1*)

_AskInstalled(*question*)
Ask a Yes/No/Pass question.

_AskYes_NoPass(*question*, *indent=1*)
Ask a yes/NO/pass question.

_Ask_YesNoPass(*question*, *indent=1*)
Ask a YES/no/pass question.

_ConfigureInstallationDirectory()
Asks for installation directory and updates section. Checks if entered directory exists and returns Path object. If no installation directory was configured before, then _GetDefaultInstallationDir is called.

_GetDefaultOptionValue(*optionName*)

_PrintAvailableEditions(*editions*, *selectedEdition*)
Print all available editions and return the selected index.

_TestDefaultInstallPath(*defaults*)
Helper function for automatic search of installation directory.

_TryLog(**args*, *condition=True*, ***kwargs*)

_multiVersionSupport = False

14.7.3 ToolChain.GHDL

Exceptions

- *GHDLException*: Base class for all tool specific exceptions
- *GHDLReanalyzeException*: Base class for all tool specific exceptions

Classes

- *Configuration*: Base class for all tool Configuration classes.
- *GHDL*: Represent an executable.
- *GHDLAnalyze*: Represent an executable.
- *GHDLElaborate*: Represent an executable.
- *GHDLRun*: Represent an executable.

Functions

- *GHDLAnalyzeFilter()*: Undocumented.
- *GHDLElaborateFilter()*: Undocumented.
- *GHDLRunFilter()*: Undocumented.

exception ToolChain.GHDL.**GHDLException**(*message=''*)

Inheritance

Members

__init__(*message=''*)
Exception initializer

Parameters **message** (*str*) – The exception message.

__str__()
Returns the exception's message text.

args

exception ToolChain.GHDL.**GHDLReanalyzeException**(*message=''*)

Inheritance

Members

__init__(*message=''*)
Exception initializer

Parameters **message** (*str*) – The exception message.

__str__()
Returns the exception's message text.

args

class ToolChain.GHDL.**Configuration**(*host: Base.IHost*)

Inheritance

Members

_vendor = 'tgingold'
The name of the tools vendor.

_toolName = 'GHDL'
The name of the tool.

_section = 'INSTALL.GHDL'
The name of the configuration section. Pattern: INSTALL.Vendor.ToolName.

_multiVersionSupport = True
Git supports multiple versions installed on the same system.

_template = {'Darwin': {'INSTALL.GHDL': {'Version': '0.34-dev', 'Backend': 'llvm
The template for the configuration sections represented as nested dictionaries.

ConfigureForAll()
Start a generic (platform independent) configuration procedure.

Overwrite this method to implement a generic configuration routine for a (tool) Configuration class.

_GetDefaultInstallationDirectory()
Return unresolved default installation directory (str) from template.

Overwrite function in sub-class for automatic search of installation directory.

_ConfigureBinaryDirectory()
Updates section with value from _template and returns directory as Path object.

_ConfigureScriptDirectory()
Updates section with value from _template and returns directory as Path object.

CheckDependency()
Check if all vendor or tool dependencies are fulfilled to configure this tool.

ClearSection(*writeWarnings=False*)
Clear the configuration section associated to this Configuration class.

ConfigureForDarwin()
Start the configuration procedure for Darwin.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Darwin specific configuration routine.

ConfigureForLinux()
Start the configuration procedure for Linux.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Linux specific configuration routine.

ConfigureForWindows()
Start the configuration procedure for Windows.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Windows specific configuration routine.

classmethod GetSections(*platform*)
Return all section names for this configuration.

Host
Return the hosting object.

IsConfigured()
Return true if the configurations section is configured

IsSupportedPlatform()
Return true if the given platform is supported by this configuration routine.

Log(*entry*, *condition=True*)
Write an entry to the local logger.

LogDebug(**args*, *condition=True*, ***kwargs*)

LogDryRun(**args*, *condition=True*, ***kwargs*)

LogError(**args*, *condition=True*, ***kwargs*)

LogFatal(**args*, *condition=True*, ***kwargs*)

LogInfo(**args*, *condition=True*, ***kwargs*)

LogNormal(**args*, *condition=True*, ***kwargs*)

LogQuiet(**args*, *condition=True*, ***kwargs*)

LogVerbose(**args*, *condition=True*, ***kwargs*)

LogWarning(**args*, *condition=True*, ***kwargs*)

Logger
Return the local logger instance.

PrepareOptions(*writeWarnings=True*)

PrepareSections(*warningWasWritten*, *writeWarnings=True*)

PrepareVersionedSections(*writeWarnings=False*)

RunPostConfigurationTasks()
Virtual method. Overwrite to execute post-configuration tasks.

SectionName
Return the configuration's section name.

State
Return the configuration state.

_Ask(*question*, *default*, *beforeDefault=''*, *afterDefault=''*, *indent=1*)

_AskInstalled(*question*)
Ask a Yes/No/Pass question.

_AskYes_NoPass(*question*, *indent=1*)
Ask a yes/NO/pass question.

_Ask_YesNoPass(*question*, *indent=1*)
Ask a YES/no/pass question.

_Configuration__WriteGHDLSection(*binPath*)

_ConfigureEdition(*editions*, *defaultEdition*)

_ConfigureInstallationDirectory()
Asks for installation directory and updates section. Checks if entered directory exists and returns Path object. If no installation directory was configured before, then _GetDefaultInstallationDir is called.

_ConfigureVersion()
If no version was configured before, then _GetDefaultVersion is called. Asks for version and updates section. Returns version as string.

_GetDefaultEdition()
Returns unresolved default edition (str) from template.

Overwrite this method in a sub-class for automatic search of editions.

_GetDefaultOptionValue(*optionName*)

_GetDefaultVersion()
Returns unresolved default version (str) from template.

Overwrite this method in a sub-class for automatic search of version.

_PrintAvailableEditions(*editions*, *selectedEdition*)
Print all available editions and return the selected index.

_TestDefaultInstallPath(*defaults*)
Helper function for automatic search of installation directory.

_TryLog(**args*, *condition=True*, ***kwargs*)

class ToolChain.GHDL.**GHDL**(*platform*, *dryrun*, *binaryDirectoryPath*, *version*, *backend*, *logger=None*)

Inheritance

Members

BinaryDirectoryPath

Backend

Version

deco()

Executable

class CmdAnalyze

```
    _name = 'a'
```

class CmdElaborate

```
    _name = 'e'
```

class CmdRun

```
    _name = 'r'
```

class FlagVerbose

```
    _name = 'v'
class FlagDebug

    _name = 'g'
class FlagExplicit

    _name = 'fexplicit'
class FlagRelaxedRules

    _name = 'frelaxed-rules'
class FlagWarnBinding

    _name = 'warn-binding'
class FlagNoVitalChecks

    _name = 'no-vital-checks'
class FlagMultiByteComments

    _name = 'mb-comments'
class FlagSynBinding

    _name = 'syn-binding'
class FlagPSL

    _name = 'fpsl'
class FlagProfileArcs

    _name = 'fprofile-arcs'
class FlagTestCoverage

    _name = 'ftest-coverage'
class SwitchCompilerOption

    _pattern = '-{0},{1}'
    _name = 'Wc'
class SwitchAssemblerOption

    _pattern = '-{0},{1}'
    _name = 'Wa'
class SwitchLinkerOption

    _pattern = '-{0},{1}'
    _name = 'Wl'
```

```
class SwitchIEEEFlavor

    _name = 'ieee'
class SwitchVHDLVersion

    _name = 'std'
class SwitchVHDLLibrary

    _name = 'work'
class ArgListLibraryReferences

    _pattern = '-{0}{1}'
    _name = 'P'
class ArgSourceFile
class ArgTopLevel
Parameters = [<class 'ToolChain.GHDL.GHDL.CmdAnalyze'>, <class 'ToolChain.GHDL.GHDL
class SwitchIEEEAsserts

    _name = 'ieee-asserts'
class SwitchStopDelta

    _name = 'stop-delta'
class SwitchVCDWaveform

    _name = 'vcd'
class SwitchVCDGZWaveform

    _name = 'vcdgz'
class SwitchFastWaveform

    _name = 'fst'
class SwitchGHDLWaveform

    _name = 'wave'
class SwitchWaveformOptionFile

    _name = 'read-wave-opt'
RunOptions = [<class 'ToolChain.GHDL.GHDL.SwitchIEEEAsserts'>, <class 'ToolChain.GHD
GetGHDLAnalyze()
GetGHDLElaborate()
GetGHDLRun()
GetReader()
```

HasErrors
: True if errors or fatals errors were found while processing the output stream.

HasWarnings
: True if errors or fatals errors were found while processing the output stream.

Log(*entry*, *condition=True*)
: Write an entry to the local logger.

LogDebug(**args*, *condition=True*, ***kwargs*)

LogDryRun(**args*, *condition=True*, ***kwargs*)

LogError(**args*, *condition=True*, ***kwargs*)

LogFatal(**args*, *condition=True*, ***kwargs*)

LogInfo(**args*, *condition=True*, ***kwargs*)

LogNormal(**args*, *condition=True*, ***kwargs*)

LogQuiet(**args*, *condition=True*, ***kwargs*)

LogVerbose(**args*, *condition=True*, ***kwargs*)

LogWarning(**args*, *condition=True*, ***kwargs*)

Logger
: Return the local logger instance.

Path

ReadUntilBoundary(*indent=0*)

Send(*line*, *end='\n'*)

SendBoundary()

StartProcess(*parameterList*)

Terminate()

_POC_BOUNDARY = '====== POC BOUNDARY ======'

_TryLog(**args*, *condition=True*, ***kwargs*)

class ToolChain.GHDL.**GHDLAnalyze**(*platform*, *dryrun*, *binaryDirectoryPath*, *version*, *backend*, *logger=None*)

Inheritance

Members

Analyze()

class ArgListLibraryReferences

```
    _name = 'P'
    _pattern = '-{0}{1}'
```

class ArgSourceFile

class ArgTopLevel

Backend

BinaryDirectoryPath

```
class CmdAnalyze

    _name = 'a'
class CmdElaborate

    _name = 'e'
class CmdRun

    _name = 'r'
Executable
class FlagDebug

    _name = 'g'
class FlagExplicit

    _name = 'fexplicit'
class FlagMultiByteComments

    _name = 'mb-comments'
class FlagNoVitalChecks

    _name = 'no-vital-checks'
class FlagPSL

    _name = 'fpsl'
class FlagProfileArcs

    _name = 'fprofile-arcs'
class FlagRelaxedRules

    _name = 'frelaxed-rules'
class FlagSynBinding

    _name = 'syn-binding'
class FlagTestCoverage

    _name = 'ftest-coverage'
class FlagVerbose

    _name = 'v'
class FlagWarnBinding

    _name = 'warn-binding'
GetGHDLAnalyze()
```

GetGHDLElaborate()

GetGHDLRun()

GetReader()

HasErrors
True if errors or fatals errors were found while processing the output stream.

HasWarnings
True if errors or fatals errors were found while processing the output stream.

Log(*entry*, *condition=True*)
Write an entry to the local logger.

LogDebug(**args*, *condition=True*, ***kwargs*)

LogDryRun(**args*, *condition=True*, ***kwargs*)

LogError(**args*, *condition=True*, ***kwargs*)

LogFatal(**args*, *condition=True*, ***kwargs*)

LogInfo(**args*, *condition=True*, ***kwargs*)

LogNormal(**args*, *condition=True*, ***kwargs*)

LogQuiet(**args*, *condition=True*, ***kwargs*)

LogVerbose(**args*, *condition=True*, ***kwargs*)

LogWarning(**args*, *condition=True*, ***kwargs*)

Logger
Return the local logger instance.

Parameters = [<class 'ToolChain.GHDL.GHDL.CmdAnalyze'>, <class 'ToolChain.GHDL.GHDL

Path

ReadUntilBoundary(*indent=0*)

RunOptions = [<class 'ToolChain.GHDL.GHDL.SwitchIEEEAsserts'>, <class 'ToolChain.GHD

Send(*line*, *end='\n'*)

SendBoundary()

StartProcess(*parameterList*)

class SwitchAssemblerOption

```
    _name = 'Wa'
    _pattern = '-{0},{1}'
```

class SwitchCompilerOption

```
    _name = 'Wc'
    _pattern = '-{0},{1}'
```

class SwitchFastWaveform

```
    _name = 'fst'
```

class SwitchGHDLWaveform

```
    _name = 'wave'
```

class SwitchIEEEAsserts

_name = 'ieee-asserts'

class SwitchIEEEFlavor

_name = 'ieee'

class SwitchLinkerOption

_name = 'Wl'

_pattern = '-{0},{1}'

class SwitchStopDelta

_name = 'stop-delta'

class SwitchVCDGZWaveform

_name = 'vcdgz'

class SwitchVCDWaveform

_name = 'vcd'

class SwitchVHDLLibrary

_name = 'work'

class SwitchVHDLVersion

_name = 'std'

class SwitchWaveformOptionFile

_name = 'read-wave-opt'

Terminate()

Version

_POC_BOUNDARY = '====== POC BOUNDARY ======'

_TryLog(**args*, *condition=True*, ***kwargs*)

deco()

class ToolChain.GHDL.**GHDLElaborate**(*platform*, *dryrun*, *binaryDirectoryPath*, *version*, *backend*, *logger=None*)

Inheritance

Members

Elaborate()

class ArgListLibraryReferences

_name = 'P'

```
    _pattern = '-{0}{1}'
class ArgSourceFile
class ArgTopLevel
Backend
BinaryDirectoryPath
class CmdAnalyze

    _name = 'a'
class CmdElaborate

    _name = 'e'
class CmdRun

    _name = 'r'
Executable
class FlagDebug

    _name = 'g'
class FlagExplicit

    _name = 'fexplicit'
class FlagMultiByteComments

    _name = 'mb-comments'
class FlagNoVitalChecks

    _name = 'no-vital-checks'
class FlagPSL

    _name = 'fpsl'
class FlagProfileArcs

    _name = 'fprofile-arcs'
class FlagRelaxedRules

    _name = 'frelaxed-rules'
class FlagSynBinding

    _name = 'syn-binding'
class FlagTestCoverage

    _name = 'ftest-coverage'
```

class FlagVerbose

_name = 'v'

class FlagWarnBinding

_name = 'warn-binding'

GetGHDLAnalyze()

GetGHDLElaborate()

GetGHDLRun()

GetReader()

HasErrors
True if errors or fatals errors were found while processing the output stream.

HasWarnings
True if errors or fatals errors were found while processing the output stream.

Log(*entry*, *condition=True*)
Write an entry to the local logger.

LogDebug(**args*, *condition=True*, ***kwargs*)

LogDryRun(**args*, *condition=True*, ***kwargs*)

LogError(**args*, *condition=True*, ***kwargs*)

LogFatal(**args*, *condition=True*, ***kwargs*)

LogInfo(**args*, *condition=True*, ***kwargs*)

LogNormal(**args*, *condition=True*, ***kwargs*)

LogQuiet(**args*, *condition=True*, ***kwargs*)

LogVerbose(**args*, *condition=True*, ***kwargs*)

LogWarning(**args*, *condition=True*, ***kwargs*)

Logger
Return the local logger instance.

Parameters = [<class 'ToolChain.GHDL.GHDL.CmdAnalyze'>, <class 'ToolChain.GHDL.GHDL

Path

ReadUntilBoundary(*indent=0*)

RunOptions = [<class 'ToolChain.GHDL.GHDL.SwitchIEEEAsserts'>, <class 'ToolChain.GHD

Send(*line*, *end='\n'*)

SendBoundary()

StartProcess(*parameterList*)

class SwitchAssemblerOption

_name = 'Wa'

_pattern = '-{0},{1}'

class SwitchCompilerOption

_name = 'Wc'

_pattern = '-{0},{1}'

class SwitchFastWaveform

_name = 'fst'

class SwitchGHDLWaveform

_name = 'wave'

class SwitchIEEEAsserts

_name = 'ieee-asserts'

class SwitchIEEEFlavor

_name = 'ieee'

class SwitchLinkerOption

_name = 'Wl'

_pattern = '-{0},{1}'

class SwitchStopDelta

_name = 'stop-delta'

class SwitchVCDGZWaveform

_name = 'vcdgz'

class SwitchVCDWaveform

_name = 'vcd'

class SwitchVHDLLibrary

_name = 'work'

class SwitchVHDLVersion

_name = 'std'

class SwitchWaveformOptionFile

_name = 'read-wave-opt'

Terminate()

Version

_POC_BOUNDARY = '====== POC BOUNDARY ======'

_TryLog(**args*, *condition=True*, ***kwargs*)

deco()

class ToolChain.GHDL.**GHDLRun**(*platform*, *dryrun*, *binaryDirectoryPath*, *version*, *backend*, *logger=None*)

Inheritance

Members

```
Run()
class ArgListLibraryReferences

    _name = 'P'
    _pattern = '-{0}{1}'
class ArgSourceFile
class ArgTopLevel
Backend
BinaryDirectoryPath
class CmdAnalyze

    _name = 'a'
class CmdElaborate

    _name = 'e'
class CmdRun

    _name = 'r'
Executable
class FlagDebug

    _name = 'g'
class FlagExplicit

    _name = 'fexplicit'
class FlagMultiByteComments

    _name = 'mb-comments'
class FlagNoVitalChecks

    _name = 'no-vital-checks'
class FlagPSL

    _name = 'fpsl'
class FlagProfileArcs

    _name = 'fprofile-arcs'
class FlagRelaxedRules
```

```
    _name = 'frelaxed-rules'
class FlagSynBinding

    _name = 'syn-binding'
class FlagTestCoverage

    _name = 'ftest-coverage'
class FlagVerbose

    _name = 'v'
class FlagWarnBinding

    _name = 'warn-binding'
```

GetGHDLAnalyze()

GetGHDLElaborate()

GetGHDLRun()

GetReader()

HasErrors
True if errors or fatals errors were found while processing the output stream.

HasWarnings
True if errors or fatals errors were found while processing the output stream.

Log(*entry*, *condition=True*)
Write an entry to the local logger.

LogDebug(**args*, *condition=True*, ***kwargs*)

LogDryRun(**args*, *condition=True*, ***kwargs*)

LogError(**args*, *condition=True*, ***kwargs*)

LogFatal(**args*, *condition=True*, ***kwargs*)

LogInfo(**args*, *condition=True*, ***kwargs*)

LogNormal(**args*, *condition=True*, ***kwargs*)

LogQuiet(**args*, *condition=True*, ***kwargs*)

LogVerbose(**args*, *condition=True*, ***kwargs*)

LogWarning(**args*, *condition=True*, ***kwargs*)

Logger
Return the local logger instance.

```
Parameters = [<class 'ToolChain.GHDL.GHDL.CmdAnalyze'>, <class 'ToolChain.GHDL.GHDL
```

Path

ReadUntilBoundary(*indent=0*)

```
RunOptions = [<class 'ToolChain.GHDL.GHDL.SwitchIEEEAsserts'>, <class 'ToolChain.GHD
```

Send(*line*, *end='\n'*)

SendBoundary()

StartProcess(*parameterList*)

```
    class SwitchAssemblerOption

        _name = 'Wa'
        _pattern = '-{0},{1}'
    class SwitchCompilerOption

        _name = 'Wc'
        _pattern = '-{0},{1}'
    class SwitchFastWaveform

        _name = 'fst'
    class SwitchGHDLWaveform

        _name = 'wave'
    class SwitchIEEEAsserts

        _name = 'ieee-asserts'
    class SwitchIEEEFlavor

        _name = 'ieee'
    class SwitchLinkerOption

        _name = 'Wl'
        _pattern = '-{0},{1}'
    class SwitchStopDelta

        _name = 'stop-delta'
    class SwitchVCDGZWaveform

        _name = 'vcdgz'
    class SwitchVCDWaveform

        _name = 'vcd'
    class SwitchVHDLLibrary

        _name = 'work'
    class SwitchVHDLVersion

        _name = 'std'
    class SwitchWaveformOptionFile

        _name = 'read-wave-opt'
    Terminate()
```

Version

_POC_BOUNDARY = '====== POC BOUNDARY ======'

_TryLog(**args*, *condition=True*, ***kwargs*)

deco()

Functions

ToolChain.GHDL.**GHDLAnalyzeFilter**(*gen*)

ToolChain.GHDL.**GHDLElaborateFilter**(*gen*)

ToolChain.GHDL.**GHDLRunFilter**(*gen*)

14.7.4 ToolChain.GNU

Exceptions

- *GNUException*: Base class for all tool specific exceptions

Classes

- *Make*: Represent an executable.

Functions

- *GNUMakeQuestaSimFilter()*: Undocumented.
- *CocotbSimulationResultFilter()*: Undocumented.

exception ToolChain.GNU.**GNUException**(*message=''*)

Inheritance

Members

__init__(*message=''*)
Exception initializer

Parameters **message** (*str*) – The exception message.

__str__()
Returns the exception's message text.

args

class ToolChain.GNU.**Make**(*platform*, *dryrun*, *logger=None*)

Inheritance

Members

class Executable

class SwitchGui

_name = 'GUI'

Parameters = [<class 'ToolChain.GNU.Make.Executable'>, <class 'ToolChain.GNU.Make.Sw

RunCocotb()

GetReader()

HasErrors
: True if errors or fatals errors were found while processing the output stream.

HasWarnings
: True if errors or fatals errors were found while processing the output stream.

Log(*entry*, *condition=True*)
: Write an entry to the local logger.

LogDebug(**args*, *condition=True*, ***kwargs*)

LogDryRun(**args*, *condition=True*, ***kwargs*)

LogError(**args*, *condition=True*, ***kwargs*)

LogFatal(**args*, *condition=True*, ***kwargs*)

LogInfo(**args*, *condition=True*, ***kwargs*)

LogNormal(**args*, *condition=True*, ***kwargs*)

LogQuiet(**args*, *condition=True*, ***kwargs*)

LogVerbose(**args*, *condition=True*, ***kwargs*)

LogWarning(**args*, *condition=True*, ***kwargs*)

Logger
: Return the local logger instance.

Path

ReadUntilBoundary(*indent=0*)

Send(*line*, *end='\n'*)

SendBoundary()

StartProcess(*parameterList*)

Terminate()

_POC_BOUNDARY = '====== POC BOUNDARY ======'

_TryLog(**args*, *condition=True*, ***kwargs*)

Functions

ToolChain.GNU.**GNUMakeQuestaSimFilter**(*gen*)

ToolChain.GNU.**CocotbSimulationResultFilter**(*gen*, *simulationResult*)

14.7.5 ToolChain.GTKWave

Exceptions

- *GTKWaveException*: Base class for all tool specific exceptions

Classes

- *Configuration*: Base class for all tool Configuration classes.
- *GTKWave*: Represent an executable.

Functions

- *GTKWaveFilter()*: Undocumented.

exception ToolChain.GTKWave.**GTKWaveException**(*message=''*)

Inheritance

Members

__init__(*message=''*)
Exception initializer

Parameters **message** (*str*) – The exception message.

__str__()
Returns the exception's message text.

args

class ToolChain.GTKWave.**Configuration**(*host: Base.IHost*)

Inheritance

Members

_vendor = 'TonyBybell'
The name of the tools vendor.

_toolName = 'GTKWave'
The name of the tool.

_section = 'INSTALL.GTKWave'
The name of the configuration section. Pattern: INSTALL.Vendor.ToolName.

_multiVersionSupport = True
GTKWave supports multiple versions installed on the same system.

_template = {'Darwin': {'INSTALL.GTKWave': {'Version': '3.3.80', 'SectionName':
The template for the configuration sections represented as nested dictionaries.

CheckDependency()
Check if all vendor or tool dependencies are fulfilled to configure this tool.

ConfigureForAll()
Start a generic (platform independent) configuration procedure.

Overwrite this method to implement a generic configuration routine for a (tool) Configuration class.

_GetDefaultInstallationDirectory()
Return unresolved default installation directory (str) from template.

Overwrite function in sub-class for automatic search of installation directory.

ClearSection(*writeWarnings=False*)
Clear the configuration section associated to this Configuration class.

ConfigureForDarwin()
Start the configuration procedure for Darwin.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Darwin specific configuration routine.

ConfigureForLinux()
Start the configuration procedure for Linux.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Linux specific configuration routine.

ConfigureForWindows()
Start the configuration procedure for Windows.

This method is a wrapper for `ConfigureForAll()`. Overwrite this method to implement a Windows specific configuration routine.

classmethod GetSections(*platform*)
Return all section names for this configuration.

Host
Return the hosting object.

IsConfigured()
Return true if the configurations section is configured

IsSupportedPlatform()
Return true if the given platform is supported by this configuration routine.

Log(*entry*, *condition=True*)
Write an entry to the local logger.

LogDebug(**args*, *condition=True*, ***kwargs*)

LogDryRun(**args*, *condition=True*, ***kwargs*)

LogError(**args*, *condition=True*, ***kwargs*)

LogFatal(**args*, *condition=True*, ***kwargs*)

LogInfo(**args*, *condition=True*, ***kwargs*)

LogNormal(**args*, *condition=True*, ***kwargs*)

LogQuiet(**args*, *condition=True*, ***kwargs*)

LogVerbose(**args*, *condition=True*, ***kwargs*)

LogWarning(**args*, *condition=True*, ***kwargs*)

Logger
Return the local logger instance.

PrepareOptions(*writeWarnings=True*)

PrepareSections(*warningWasWritten*, *writeWarnings=True*)

PrepareVersionedSections(*writeWarnings=False*)

RunPostConfigurationTasks()
Virtual method. Overwrite to execute post-configuration tasks.

SectionName
Return the configuration's section name.

State
Return the configuration state.

_Ask(*question*, *default*, *beforeDefault=''*, *afterDefault=''*, *indent=1*)

_AskInstalled(*question*)
Ask a Yes/No/Pass question.

_AskYes_NoPass(*question*, *indent=1*)
Ask a yes/NO/pass question.

_Ask_YesNoPass(*question*, *indent=1*)
Ask a YES/no/pass question.

_Configuration__WriteGtkWaveSection(*binPath*)

_ConfigureBinaryDirectory()
Updates section with value from `_template` and returns directory as `Path` object.

_ConfigureEdition(*editions*, *defaultEdition*)

_ConfigureInstallationDirectory()
Asks for installation directory and updates section. Checks if entered directory exists and returns Path object. If no installation directory was configured before, then _GetDefaultInstallationDir is called.

_ConfigureVersion()
If no version was configured before, then _GetDefaultVersion is called. Asks for version and updates section. Returns version as string.

_GetDefaultEdition()
Returns unresolved default edition (str) from template.

Overwrite this method in a sub-class for automatic search of editions.

_GetDefaultOptionValue(*optionName*)

_GetDefaultVersion()
Returns unresolved default version (str) from template.

Overwrite this method in a sub-class for automatic search of version.

_PrintAvailableEditions(*editions*, *selectedEdition*)
Print all available editions and return the selected index.

_TestDefaultInstallPath(*defaults*)
Helper function for automatic search of installation directory.

_TryLog(**args*, *condition=True*, ***kwargs*)

class ToolChain.GTKWave.**GTKWave**(*platform*, *dryrun*, *binaryDirectoryPath*, *version*, *logger=None*)

Inheritance

Members

BinaryDirectoryPath

Version

class Executable

class SwitchDumpFile

```
    _name = 'dump'
```

class SwitchSaveFile

```
    _name = 'save'
```

```
Parameters = [<class 'ToolChain.GTKWave.GTKWave.Executable'>, <class 'ToolChain.GTKW
```

View()

GetReader()

HasErrors
True if errors or fatals errors were found while processing the output stream.

HasWarnings
True if errors or fatals errors were found while processing the output stream.

Log(*entry*, *condition=True*)
Write an entry to the local logger.

LogDebug(**args*, *condition=True*, ***kwargs*)

LogDryRun(**args*, *condition=True*, ***kwargs*)

LogError(**args*, *condition=True*, ***kwargs*)

LogFatal(**args*, *condition=True*, ***kwargs*)

LogInfo(**args*, *condition=True*, ***kwargs*)

LogNormal(**args*, *condition=True*, ***kwargs*)

LogQuiet(**args*, *condition=True*, ***kwargs*)

LogVerbose(**args*, *condition=True*, ***kwargs*)

LogWarning(**args*, *condition=True*, ***kwargs*)

Logger
Return the local logger instance.

Path

ReadUntilBoundary(*indent=0*)

Send(*line*, *end='\n'*)

SendBoundary()

StartProcess(*parameterList*)

Terminate()

_POC_BOUNDARY = '====== POC BOUNDARY ======'

_TryLog(**args*, *condition=True*, ***kwargs*)

Functions

ToolChain.GTKWave.**GTKWaveFilter**(*gen*)

14.7.6 ToolChain.Git

Exceptions

- *GitException*: Base class for all tool specific exceptions

Classes

- *Configuration*: Base class for all tool Configuration classes.
- *Git*: Undocumented.
- *GitSCM*: Represent an executable.
- *GitRevParse*: Represent an executable.
- *GitRevList*: Represent an executable.
- *GitDescribe*: Represent an executable.
- *GitConfig*: Represent an executable.

exception ToolChain.Git.**GitException**(*message=''*)

Inheritance

Members

__init__(*message=''*)
Exception initializer

Parameters **message** (*str*) – The exception message.

__str__()
Returns the exception's message text.

args

class ToolChain.Git.**Configuration**(*host*)

Inheritance

Members

_vendor = 'Git SCM'
The name of the tools vendor.

_toolName = 'Git'
The name of the tool.

_section = 'INSTALL.Git'
The name of the configuration section. Pattern: INSTALL.Vendor.ToolName.

_template = {'Linux': {'INSTALL.Git': {'Version': '2.8.1', 'InstallationDirectory
The template for the configuration sections represented as nested dictionaries.

ConfigureForAll()
Start a generic (platform independent) configuration procedure.

Overwrite this method to implement a generic configuration routine for a (tool) Configuration class.

_GetDefaultInstallationDirectory()
Return unresolved default installation directory (str) from template.

Overwrite function in sub-class for automatic search of installation directory.

RunPostConfigurationTasks()
Virtual method. Overwrite to execute post-configuration tasks.

CheckDependency()
Check if all vendor or tool dependencies are fulfilled to configure this tool.

ClearSection(*writeWarnings=False*)
Clear the configuration section associated to this Configuration class.

ConfigureForDarwin()
Start the configuration procedure for Darwin.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Darwin specific configuration routine.

ConfigureForLinux()
Start the configuration procedure for Linux.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Linux specific configuration routine.

ConfigureForWindows()
Start the configuration procedure for Windows.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Windows specific configuration routine.

classmethod GetSections(*platform*)
Return all section names for this configuration.

Host
Return the hosting object.

IsConfigured()
Return true if the configurations section is configured

IsSupportedPlatform()
Return true if the given platform is supported by this configuration routine.

Log(*entry*, *condition=True*)
Write an entry to the local logger.

LogDebug(**args*, *condition=True*, ***kwargs*)

LogDryRun(**args*, *condition=True*, ***kwargs*)

LogError(**args*, *condition=True*, ***kwargs*)

LogFatal(**args*, *condition=True*, ***kwargs*)

LogInfo(**args*, *condition=True*, ***kwargs*)

LogNormal(**args*, *condition=True*, ***kwargs*)

LogQuiet(**args*, *condition=True*, ***kwargs*)

LogVerbose(**args*, *condition=True*, ***kwargs*)

LogWarning(**args*, *condition=True*, ***kwargs*)

Logger
Return the local logger instance.

PrepareOptions(*writeWarnings=True*)

PrepareSections(*warningWasWritten*, *writeWarnings=True*)

PrepareVersionedSections(*writeWarnings=False*)

SectionName
Return the configuration's section name.

State
Return the configuration state.

_Ask(*question*, *default*, *beforeDefault=''*, *afterDefault=''*, *indent=1*)

_AskInstalled(*question*)
Ask a Yes/No/Pass question.

_AskYes_NoPass(*question*, *indent=1*)
Ask a yes/NO/pass question.

_Ask_YesNoPass(*question*, *indent=1*)
Ask a YES/no/pass question.

_Configuration__GetGitDirectory()

_Configuration__InstallGitFilters()

_Configuration__InstallGitHooks()

_Configuration__IsUnderGitControl()

_Configuration__UninstallGitFilters()

_Configuration__UninstallGitHooks()

_Configuration__WriteGitSection(*binPath*)

_ConfigureBinaryDirectory()
Updates section with value from `_template` and returns directory as `Path` object.

_ConfigureEdition(*editions*, *defaultEdition*)

_ConfigureInstallationDirectory()
Asks for installation directory and updates section. Checks if entered directory exists and returns Path object. If no installation directory was configured before, then _GetDefaultInstallationDir is called.

_ConfigureVersion()
If no version was configured before, then _GetDefaultVersion is called. Asks for version and updates section. Returns version as string.

_GetDefaultEdition()
Returns unresolved default edition (str) from template.

Overwrite this method in a sub-class for automatic search of editions.

_GetDefaultOptionValue(*optionName*)

_GetDefaultVersion()
Returns unresolved default version (str) from template.

Overwrite this method in a sub-class for automatic search of version.

_PrintAvailableEditions(*editions*, *selectedEdition*)
Print all available editions and return the selected index.

_TestDefaultInstallPath(*defaults*)
Helper function for automatic search of installation directory.

_TryLog(**args*, *condition=True*, ***kwargs*)

_multiVersionSupport = False

class ToolChain.Git.**Git**(*platform*, *dryrun*, *binaryDirectoryPath*, *version*, *logger=None*)

Inheritance

Members

GetGitRevParse()

GetGitRevList()

GetGitDescribe()

GetGitConfig()

class ToolChain.Git.**GitSCM**(*toolchain: ToolChain.ToolMixIn*)

Inheritance

Members

Clear()

class Executable

class Switch_Version

_name = 'version'

Parameters = [<class 'ToolChain.Git.GitSCM.Executable'>, <class 'ToolChain.Git.GitSC

GetReader()

Log(*entry*, *condition=True*)
Write an entry to the local logger.

LogDebug(**args*, *condition=True*, ***kwargs*)

LogDryRun(**args*, *condition=True*, ***kwargs*)

LogError(**args*, *condition=True*, ***kwargs*)

LogFatal(**args*, *condition=True*, ***kwargs*)

LogInfo(**args*, *condition=True*, ***kwargs*)

LogNormal(**args*, *condition=True*, ***kwargs*)

LogQuiet(**args*, *condition=True*, ***kwargs*)

LogVerbose(**args*, *condition=True*, ***kwargs*)

LogWarning(**args*, *condition=True*, ***kwargs*)

Logger
Return the local logger instance.

Path

ReadUntilBoundary(*indent=0*)

Send(*line*, *end='\n'*)

SendBoundary()

StartProcess(*parameterList*)

Terminate()

_POC_BOUNDARY = '====== POC BOUNDARY ======'

_TryLog(**args*, *condition=True*, ***kwargs*)

class ToolChain.Git.**GitRevParse**(*toolchain: ToolChain.ToolMixIn*)

Inheritance

Members

Clear()

class Command

_name = 'rev-parse'

class SwitchInsideWorkingTree

_name = 'is-inside-work-tree'

class SwitchShowTopLevel

_name = 'show-toplevel'

class SwitchGitDir

_name = 'git-dir'

RevParseParameters = [<class 'ToolChain.Git.GitRevParse.Command'>, <class 'ToolChain

Execute()

class Executable

GetReader()

Log(*entry*, *condition=True*)
Write an entry to the local logger.

LogDebug(**args*, *condition=True*, ***kwargs*)

LogDryRun(**args*, *condition=True*, ***kwargs*)

LogError(**args*, *condition=True*, ***kwargs*)

LogFatal(**args*, *condition=True*, ***kwargs*)

LogInfo(**args*, *condition=True*, ***kwargs*)

LogNormal(**args*, *condition=True*, ***kwargs*)

LogQuiet(**args*, *condition=True*, ***kwargs*)

LogVerbose(**args*, *condition=True*, ***kwargs*)

LogWarning(**args*, *condition=True*, ***kwargs*)

Logger
Return the local logger instance.

Parameters = [<class 'ToolChain.Git.GitSCM.Executable'>, <class 'ToolChain.Git.GitSC

Path

ReadUntilBoundary(*indent=0*)

Send(*line*, *end='\n'*)

SendBoundary()

StartProcess(*parameterList*)

class Switch_Version

_name = 'version'

Terminate()

_POC_BOUNDARY = '====== POC BOUNDARY ======'

_TryLog(**args*, *condition=True*, ***kwargs*)

class ToolChain.Git.**GitRevList**(*toolchain: ToolChain.ToolMixIn*)

Inheritance

Members

Clear()

class Command

_name = 'rev-list'

class SwitchTags

_name = 'tags'

class SwitchMaxCount

_name = 'max-count'

RevListParameters = [<class 'ToolChain.Git.GitRevList.Command'>, <class 'ToolChain.G

Execute()

class Executable

GetReader()

Log(*entry*, *condition=True*)
Write an entry to the local logger.

LogDebug(**args*, *condition=True*, ***kwargs*)

LogDryRun(**args*, *condition=True*, ***kwargs*)

LogError(**args*, *condition=True*, ***kwargs*)

LogFatal(**args*, *condition=True*, ***kwargs*)

LogInfo(**args*, *condition=True*, ***kwargs*)

LogNormal(**args*, *condition=True*, ***kwargs*)

LogQuiet(**args*, *condition=True*, ***kwargs*)

LogVerbose(**args*, *condition=True*, ***kwargs*)

LogWarning(**args*, *condition=True*, ***kwargs*)

Logger
Return the local logger instance.

Parameters = [<class 'ToolChain.Git.GitSCM.Executable'>, <class 'ToolChain.Git.GitSC

Path

ReadUntilBoundary(*indent=0*)

Send(*line*, *end='\n'*)

SendBoundary()

StartProcess(*parameterList*)

class Switch_Version

```
    _name = 'version'
```

Terminate()

_POC_BOUNDARY = '====== POC BOUNDARY ======'

_TryLog(**args*, *condition=True*, ***kwargs*)

class ToolChain.Git.**GitDescribe**(*toolchain: ToolChain.ToolMixIn*)

Inheritance

Members

Clear()

class Command

```
    _name = 'describe'
```

class SwitchAbbrev

```
    _name = 'abbrev'
```

class SwitchTags

_name = 'tags'

DescribeParameters = [<class 'ToolChain.Git.GitDescribe.Command'>, <class 'ToolChain

Execute()

class Executable

GetReader()

Log(*entry*, *condition=True*)
Write an entry to the local logger.

LogDebug(**args*, *condition=True*, ***kwargs*)

LogDryRun(**args*, *condition=True*, ***kwargs*)

LogError(**args*, *condition=True*, ***kwargs*)

LogFatal(**args*, *condition=True*, ***kwargs*)

LogInfo(**args*, *condition=True*, ***kwargs*)

LogNormal(**args*, *condition=True*, ***kwargs*)

LogQuiet(**args*, *condition=True*, ***kwargs*)

LogVerbose(**args*, *condition=True*, ***kwargs*)

LogWarning(**args*, *condition=True*, ***kwargs*)

Logger
Return the local logger instance.

Parameters = [<class 'ToolChain.Git.GitSCM.Executable'>, <class 'ToolChain.Git.GitSC

Path

ReadUntilBoundary(*indent=0*)

Send(*line*, *end='\n'*)

SendBoundary()

StartProcess(*parameterList*)

class Switch_Version

_name = 'version'

Terminate()

_POC_BOUNDARY = '====== POC BOUNDARY ======'

_TryLog(**args*, *condition=True*, ***kwargs*)

class ToolChain.Git.**GitConfig**(*toolchain: ToolChain.ToolMixIn*)

Inheritance

Members

Clear()

class Command

_name = 'config'

class SwitchUnset

    _name = 'unset'

class SwitchRemoveSection

    _name = 'remove-section'

class ValueFilterClean

    _name = 'clean'

    _pattern = 'filter.{1}.{0}'

class ValueFilterSmudge

    _name = 'smudge'

    _pattern = 'filter.{1}.{0}'

class ValueFilterParameters

ConfigParameters = [<class 'ToolChain.Git.GitConfig.Command'>, <class 'ToolChain.Git

Execute()

class Executable

GetReader()

Log(*entry*, *condition=True*)
    Write an entry to the local logger.

LogDebug(**args*, *condition=True*, ***kwargs*)

LogDryRun(**args*, *condition=True*, ***kwargs*)

LogError(**args*, *condition=True*, ***kwargs*)

LogFatal(**args*, *condition=True*, ***kwargs*)

LogInfo(**args*, *condition=True*, ***kwargs*)

LogNormal(**args*, *condition=True*, ***kwargs*)

LogQuiet(**args*, *condition=True*, ***kwargs*)

LogVerbose(**args*, *condition=True*, ***kwargs*)

LogWarning(**args*, *condition=True*, ***kwargs*)

Logger
    Return the local logger instance.

Parameters = [<class 'ToolChain.Git.GitSCM.Executable'>, <class 'ToolChain.Git.GitSC

Path

ReadUntilBoundary(*indent=0*)

Send(*line*, *end='\n'*)

SendBoundary()

StartProcess(*parameterList*)

class Switch_Version

    _name = 'version'

Terminate()

_POC_BOUNDARY = '====== POC BOUNDARY ======'

_TryLog(**args*, *condition=True*, ***kwargs*)

14.7.7 ToolChain.Intel

Submodules

ToolChain.Intel.ModelSim

Exceptions

- *ModelSimException*: Base class for all tool specific exceptions

Classes

- *IntelModelSimEditions*: An enumeration.
- *Configuration*: Base class for all tool Configuration classes.
- *IntelEditionConfiguration*: Base class for all tool Configuration classes.
- *IntelStarterEditionConfiguration*: Base class for all tool Configuration classes.

exception ToolChain.Intel.ModelSim.**ModelSimException**(*message=''*)

Inheritance

Members

__init__(*message=''*)
Exception initializer

Parameters **message** (*str*) – The exception message.

__str__()
Returns the exception's message text.

args

class ToolChain.Intel.ModelSim.**IntelModelSimEditions**(*name*, *section*)
An enumeration.

Inheritance

Members

ModelSimIntelEdition = 1

ModelSimIntelStarterEdition = 2

class ToolChain.Intel.ModelSim.**Configuration**(*host: Base.IHost*)

Inheritance

Members

_vendor = 'Intel'
The name of the tools vendor.

_multiVersionSupport = False
Intel ModelSim Edition doesn't support multiple versions.

CheckDependency()
Check if general Intel support is configured in PoC.

ConfigureForAll()
Configuration routine for Mentor Graphics ModelSim on all supported platforms.

1. Ask if ModelSim is installed.

- Pass → skip this configuration. Don't change existing settings.
- Yes → collect installation information for ModelSim.
- No → clear the ModelSim configuration section.

1. Ask for ModelSim's version.
2. Ask for ModelSim's edition (PE, PE student, SE 32-bit, SE 64-bit).
3. Ask for ModelSim's installation directory.

_ConfigureEdition()
Configure ModelSim for Intel.

ClearSection(*writeWarnings=False*)
Clear the configuration section associated to this Configuration class.

ConfigureForDarwin()
Start the configuration procedure for Darwin.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Darwin specific configuration routine.

ConfigureForLinux()
Start the configuration procedure for Linux.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Linux specific configuration routine.

ConfigureForWindows()
Start the configuration procedure for Windows.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Windows specific configuration routine.

classmethod GetSections(*platform*)
Return all section names for this configuration.

Host
Return the hosting object.

IsConfigured()
Return true if the configurations section is configured

IsSupportedPlatform()
Return true if the given platform is supported by this configuration routine.

Log(*entry*, *condition=True*)
Write an entry to the local logger.

LogDebug(**args*, *condition=True*, ***kwargs*)

LogDryRun(**args*, *condition=True*, ***kwargs*)

LogError(**args*, *condition=True*, ***kwargs*)

LogFatal(**args*, *condition=True*, ***kwargs*)

LogInfo(**args*, *condition=True*, ***kwargs*)

LogNormal(**args*, *condition=True*, ***kwargs*)

LogQuiet(**args*, *condition=True*, ***kwargs*)

LogVerbose(**args*, *condition=True*, ***kwargs*)

LogWarning(**args*, *condition=True*, ***kwargs*)

Logger
Return the local logger instance.

PrepareOptions(*writeWarnings=True*)

PrepareSections(*warningWasWritten*, *writeWarnings=True*)

PrepareVersionedSections(*writeWarnings=False*)

RunPostConfigurationTasks()
Virtual method. Overwrite to execute post-configuration tasks.

SectionName
Return the configuration's section name.

State
Return the configuration state.

_Ask(*question*, *default*, *beforeDefault=''*, *afterDefault=''*, *indent=1*)

_AskInstalled(*question*)
Ask a Yes/No/Pass question.

_AskYes_NoPass(*question*, *indent=1*)
Ask a yes/NO/pass question.

_Ask_YesNoPass(*question*, *indent=1*)
Ask a YES/no/pass question.

_CheckModelSimVersion(*binPath*, *version*)

_Configuration__GetModelSimVersion(*binPath*)

_ConfigureBinaryDirectory()
Updates section with value from `_template` and returns directory as `Path` object.

_ConfigureInstallationDirectory()
Asks for installation directory and updates section. Checks if entered directory exists and returns Path object. If no installation directory was configured before, then _GetDefaultInstallationDir is called.

_ConfigureVersion()
If no version was configured before, then _GetDefaultVersion is called. Asks for version and updates section. Returns version as string.

_GetDefaultEdition()
Returns unresolved default edition (str) from template.

Overwrite this method in a sub-class for automatic search of editions.

_GetDefaultInstallationDirectory()
Return unresolved default installation directory (str) from template.

Overwrite function in sub-class for automatic search of installation directory.

_GetDefaultOptionValue(*optionName*)

_GetDefaultVersion()
Returns unresolved default version (str) from template.

Overwrite this method in a sub-class for automatic search of version.

_GetModelSimVersion(*binPath*)

_PrintAvailableEditions(*editions*, *selectedEdition*)
Print all available editions and return the selected index.

_TestDefaultInstallPath(*defaults*)
Helper function for automatic search of installation directory.

_TryLog(**args*, *condition=True*, ***kwargs*)

_section = 'INSTALL.Vendor.Tool'

_template = {'ALL': {'INSTALL.Vendor.Tool': {'Version': '1.0'}}, 'Darwin': {'INST

_toolName = 'Mentor ModelSim'

class ToolChain.Intel.ModelSim.**IntelEditionConfiguration**(*host: Base.IHost*)

Inheritance

Members

_toolName = 'Intel ModelSim'
The name of the tool.

__editionName = None
The name of the tool.

_section = 'INSTALL.Intel.ModelSimAE'
The name of the configuration section. Pattern: INSTALL.Vendor.ToolName.

_template = {'Linux': {'INSTALL.Intel.ModelSimAE': {'Version': '10.5b', 'Edition'

CheckDependency()
Check if general Intel support is configured in PoC.

ClearSection(*writeWarnings=False*)
Clear the configuration section associated to this Configuration class.

ConfigureForAll()
Configuration routine for Mentor Graphics ModelSim on all supported platforms.

1. Ask if ModelSim is installed.

- Pass → skip this configuration. Don't change existing settings.
- Yes → collect installation information for ModelSim.
- No → clear the ModelSim configuration section.

1. Ask for ModelSim's version.
2. Ask for ModelSim's edition (PE, PE student, SE 32-bit, SE 64-bit).
3. Ask for ModelSim's installation directory.

ConfigureForDarwin()
Start the configuration procedure for Darwin.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Darwin specific configuration routine.

ConfigureForLinux()
Start the configuration procedure for Linux.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Linux specific configuration routine.

ConfigureForWindows()
Start the configuration procedure for Windows.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Windows specific configuration routine.

classmethod GetSections(*platform*)
Return all section names for this configuration.

Host
Return the hosting object.

IsConfigured()
Return true if the configurations section is configured

IsSupportedPlatform()
Return true if the given platform is supported by this configuration routine.

Log(*entry*, *condition=True*)
Write an entry to the local logger.

LogDebug(**args*, *condition=True*, ***kwargs*)

LogDryRun(**args*, *condition=True*, ***kwargs*)

LogError(**args*, *condition=True*, ***kwargs*)

LogFatal(**args*, *condition=True*, ***kwargs*)

LogInfo(**args*, *condition=True*, ***kwargs*)

LogNormal(**args*, *condition=True*, ***kwargs*)

LogQuiet(**args*, *condition=True*, ***kwargs*)

LogVerbose(**args*, *condition=True*, ***kwargs*)

LogWarning(**args*, *condition=True*, ***kwargs*)

Logger
Return the local logger instance.

PrepareOptions(*writeWarnings=True*)

PrepareSections(*warningWasWritten*, *writeWarnings=True*)

PrepareVersionedSections(*writeWarnings=False*)

RunPostConfigurationTasks()
Virtual method. Overwrite to execute post-configuration tasks.

SectionName
Return the configuration's section name.

State
Return the configuration state.

_Ask(*question*, *default*, *beforeDefault=''*, *afterDefault=''*, *indent=1*)

_AskInstalled(*question*)
Ask a Yes/No/Pass question.

_AskYes_NoPass(*question*, *indent=1*)
Ask a yes/NO/pass question.

_Ask_YesNoPass(*question*, *indent=1*)
Ask a YES/no/pass question.

_CheckModelSimVersion(*binPath*, *version*)

_Configuration__GetModelSimVersion(*binPath*)

_ConfigureBinaryDirectory()
Updates section with value from `_template` and returns directory as `Path` object.

_ConfigureEdition()
Configure ModelSim for Intel.

_ConfigureInstallationDirectory()
Asks for installation directory and updates section. Checks if entered directory exists and returns Path object. If no installation directory was configured before, then _GetDefaultInstallationDir is called.

_ConfigureVersion()
If no version was configured before, then _GetDefaultVersion is called. Asks for version and updates section. Returns version as string.

_GetDefaultEdition()
Returns unresolved default edition (str) from template.

Overwrite this method in a sub-class for automatic search of editions.

_GetDefaultInstallationDirectory()
Return unresolved default installation directory (str) from template.

Overwrite function in sub-class for automatic search of installation directory.

_GetDefaultOptionValue(*optionName*)

_GetDefaultVersion()
Returns unresolved default version (str) from template.

Overwrite this method in a sub-class for automatic search of version.

_GetModelSimVersion(*binPath*)

_IntelEditionConfiguration__editionName = 'ModelSim Intel Edition'

_PrintAvailableEditions(*editions*, *selectedEdition*)
Print all available editions and return the selected index.

_TestDefaultInstallPath(*defaults*)
Helper function for automatic search of installation directory.

_TryLog(**args*, *condition=True*, ***kwargs*)

_multiVersionSupport = False

_vendor = 'Intel'

class ToolChain.Intel.ModelSim.**IntelStarterEditionConfiguration**(*host: Base.IHost*)

Inheritance

Members

_toolName = 'Intel ModelSim (Starter Edition)'
The name of the tool.

__editionName = None

_section = 'INSTALL.Intel.ModelSimASE'
The name of the configuration section. Pattern: `INSTALL.Vendor.ToolName`.

_template = {'Linux': {'INSTALL.Intel.ModelSimASE': {'Version': '10.5b', 'Edition

CheckDependency()
Check if general Intel support is configured in PoC.

ClearSection(*writeWarnings=False*)
Clear the configuration section associated to this Configuration class.

ConfigureForAll()
Configuration routine for Mentor Graphics ModelSim on all supported platforms.

1. Ask if ModelSim is installed.

   - Pass → skip this configuration. Don't change existing settings.
   - Yes → collect installation information for ModelSim.
   - No → clear the ModelSim configuration section.

1. Ask for ModelSim's version.
2. Ask for ModelSim's edition (PE, PE student, SE 32-bit, SE 64-bit).
3. Ask for ModelSim's installation directory.

ConfigureForDarwin()
Start the configuration procedure for Darwin.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Darwin specific configuration routine.

ConfigureForLinux()
Start the configuration procedure for Linux.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Linux specific configuration routine.

ConfigureForWindows()
Start the configuration procedure for Windows.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Windows specific configuration routine.

classmethod GetSections(*platform*)
Return all section names for this configuration.

Host
Return the hosting object.

IsConfigured()
Return true if the configurations section is configured

IsSupportedPlatform()
Return true if the given platform is supported by this configuration routine.

Log(*entry*, *condition=True*)
Write an entry to the local logger.

LogDebug(**args*, *condition=True*, ***kwargs*)

LogDryRun(**args*, *condition=True*, ***kwargs*)

LogError(**args*, *condition=True*, ***kwargs*)

LogFatal(**args*, *condition=True*, ***kwargs*)

LogInfo(**args*, *condition=True*, ***kwargs*)

LogNormal(**args*, *condition=True*, ***kwargs*)

LogQuiet(**args*, *condition=True*, ***kwargs*)

LogVerbose(**args*, *condition=True*, ***kwargs*)

LogWarning(**args*, *condition=True*, ***kwargs*)

Logger
Return the local logger instance.

PrepareOptions(*writeWarnings=True*)

PrepareSections(*warningWasWritten*, *writeWarnings=True*)

PrepareVersionedSections(*writeWarnings=False*)

RunPostConfigurationTasks()
Virtual method. Overwrite to execute post-configuration tasks.

SectionName
Return the configuration's section name.

State
Return the configuration state.

_Ask(*question*, *default*, *beforeDefault=''*, *afterDefault=''*, *indent=1*)

_AskInstalled(*question*)
Ask a Yes/No/Pass question.

_AskYes_NoPass(*question*, *indent=1*)
Ask a yes/NO/pass question.

_Ask_YesNoPass(*question*, *indent=1*)
Ask a YES/no/pass question.

_CheckModelSimVersion(*binPath*, *version*)

_Configuration__GetModelSimVersion(*binPath*)

_ConfigureBinaryDirectory()
Updates section with value from `_template` and returns directory as `Path` object.

_ConfigureEdition()
Configure ModelSim for Intel.

_ConfigureInstallationDirectory()
Asks for installation directory and updates section. Checks if entered directory exists and returns Path object. If no installation directory was configured before, then _GetDefaultInstallationDir is called.

_ConfigureVersion()
If no version was configured before, then _GetDefaultVersion is called. Asks for version and updates section. Returns version as string.

_GetDefaultEdition()
Returns unresolved default edition (str) from template.

Overwrite this method in a sub-class for automatic search of editions.

_GetDefaultInstallationDirectory()
Return unresolved default installation directory (str) from template.

Overwrite function in sub-class for automatic search of installation directory.

_GetDefaultOptionValue(*optionName*)

_GetDefaultVersion()
Returns unresolved default version (str) from template.

Overwrite this method in a sub-class for automatic search of version.

_GetModelSimVersion(*binPath*)

_IntelStarterEditionConfiguration__editionName = 'ModelSim Intel Starter Edition'

_PrintAvailableEditions(*editions*, *selectedEdition*)
Print all available editions and return the selected index.

_TestDefaultInstallPath(*defaults*)
Helper function for automatic search of installation directory.

_TryLog(**args*, *condition=True*, ***kwargs*)

_multiVersionSupport = False

_vendor = 'Intel'

ToolChain.Intel.Quartus

Exceptions

- *QuartusException*: Base class for all tool specific exceptions

Classes

- *Configuration*: Base class for all tool Configuration classes.
- *Quartus*: Undocumented.
- *Map*: Represent an executable.

exception ToolChain.Intel.Quartus.**QuartusException**(*message=''*)

Inheritance

Members

__init__(*message=''*)
Exception initializer

Parameters **message** (*str*) – The exception message.

__str__()
Returns the exception's message text.

args

class ToolChain.Intel.Quartus.**Configuration**(*host: Base.IHost*)

Inheritance

Members

_vendor = 'Intel'
The name of the tools vendor.

_toolName = 'Intel Quartus Prime'
The name of the tool.

_section = 'INSTALL.Intel.Quartus'
The name of the configuration section. Pattern: `INSTALL.Vendor.ToolName`.

_multiVersionSupport = True
Intel Quartus supports multiple versions installed on the same system.

CheckDependency()
Check if general Intel support is configured in PoC.

ConfigureForAll()
Start a generic (platform independent) configuration procedure.

Overwrite this method to implement a generic configuration routine for a (tool) Configuration class.

ClearSection(*writeWarnings=False*)
Clear the configuration section associated to this Configuration class.

ConfigureForDarwin()
Start the configuration procedure for Darwin.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Darwin specific configuration routine.

ConfigureForLinux()
Start the configuration procedure for Linux.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Linux specific configuration routine.

ConfigureForWindows()
Start the configuration procedure for Windows.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Windows specific configuration routine.

classmethod GetSections(*platform*)
Return all section names for this configuration.

Host
Return the hosting object.

IsConfigured()
Return true if the configurations section is configured

IsSupportedPlatform()
Return true if the given platform is supported by this configuration routine.

Log(*entry*, *condition=True*)
Write an entry to the local logger.

LogDebug(**args*, *condition=True*, ***kwargs*)

LogDryRun(**args*, *condition=True*, ***kwargs*)

LogError(**args*, *condition=True*, ***kwargs*)

LogFatal(**args*, *condition=True*, ***kwargs*)

LogInfo(**args*, *condition=True*, ***kwargs*)

LogNormal(**args*, *condition=True*, ***kwargs*)

LogQuiet(**args*, *condition=True*, ***kwargs*)

LogVerbose(**args*, *condition=True*, ***kwargs*)

LogWarning(**args*, *condition=True*, ***kwargs*)

Logger
Return the local logger instance.

PrepareOptions(*writeWarnings=True*)

PrepareSections(*warningWasWritten*, *writeWarnings=True*)

PrepareVersionedSections(*writeWarnings=False*)

RunPostConfigurationTasks()
Virtual method. Overwrite to execute post-configuration tasks.

SectionName
Return the configuration's section name.

State
Return the configuration state.

_Ask(*question*, *default*, *beforeDefault=''*, *afterDefault=''*, *indent=1*)

_AskInstalled(*question*)
Ask a Yes/No/Pass question.

_AskYes_NoPass(*question*, *indent=1*)
Ask a yes/NO/pass question.

_Ask_YesNoPass(*question*, *indent=1*)
Ask a YES/no/pass question.

_Configuration__CheckQuartusVersion(*binPath*, *version*)

_ConfigureBinaryDirectory()
Updates section with value from `_template` and returns directory as `Path` object.

_ConfigureEdition(*editions*, *defaultEdition*)

_ConfigureInstallationDirectory()
Asks for installation directory and updates section. Checks if entered directory exists and returns Path object. If no installation directory was configured before, then _GetDefaultInstallationDir is called.

_ConfigureVersion()
If no version was configured before, then _GetDefaultVersion is called. Asks for version and updates section. Returns version as string.

_GetDefaultEdition()
Returns unresolved default edition (str) from template.

Overwrite this method in a sub-class for automatic search of editions.

_GetDefaultInstallationDirectory()
Return unresolved default installation directory (str) from template.

Overwrite function in sub-class for automatic search of installation directory.

_GetDefaultOptionValue(*optionName*)

_GetDefaultVersion()
Returns unresolved default version (str) from template.

Overwrite this method in a sub-class for automatic search of version.

_PrintAvailableEditions(*editions*, *selectedEdition*)
Print all available editions and return the selected index.

_TestDefaultInstallPath(*defaults*)
Helper function for automatic search of installation directory.

_TryLog(**args*, *condition=True*, ***kwargs*)

_template = {'Linux': {'INSTALL.Altera.Quartus': {'Version': '16.0', 'SectionName

class ToolChain.Intel.Quartus.**Quartus**(*platform*, *dryrun*, *binaryDirectoryPath*, *version*, *logger=None*)

Inheritance

Members

GetMap()

GetTclShell()

class ToolChain.Intel.Quartus.**Map**(*toolchain: ToolChain.ToolMixIn*)

Inheritance

Members

class ArgProjectName

Compile()

class Executable

GetReader()

HasErrors
True if errors or fatals errors were found while processing the output stream.

HasWarnings
True if errors or fatals errors were found while processing the output stream.

Log(*entry*, *condition=True*)
Write an entry to the local logger.

LogDebug(**args*, *condition=True*, ***kwargs*)

LogDryRun(**args*, *condition=True*, ***kwargs*)

LogError(**args*, *condition=True*, ***kwargs*)

LogFatal(**args*, *condition=True*, ***kwargs*)

LogInfo(**args*, *condition=True*, ***kwargs*)

LogNormal(**args*, *condition=True*, ***kwargs*)

LogQuiet(**args*, *condition=True*, ***kwargs*)

LogVerbose(**args*, *condition=True*, ***kwargs*)

LogWarning(**args*, *condition=True*, ***kwargs*)

Logger
Return the local logger instance.

Parameters = [<class 'ToolChain.Altera.Quartus.Map.Executable'>, <class 'ToolChain.A

Path

ReadUntilBoundary(*indent=0*)

Send(*line*, *end='\n'*)

SendBoundary()

StartProcess(*parameterList*)

class SwitchArgumentFile

_name = 'f'

class SwitchDeviceFamily

_name = 'family'

class SwitchDevicePart

_name = 'part'

Terminate()

_POC_BOUNDARY = '====== POC BOUNDARY ======'

_TryLog(**args*, *condition=True*, ***kwargs*)

Exceptions

- *IntelException*: Base class for all tool specific exceptions

Classes

- *Configuration*: Configuration routines for Intel as a vendor.

exception ToolChain.Intel.**IntelException**(*message=''*)

Inheritance

Members

__init__(*message=''*)
Exception initializer

Parameters **message** (*str*) – The exception message.

__str__()
Returns the exception's message text.

args

class ToolChain.Intel.**Configuration**(*host: Base.IHost*)
Configuration routines for Intel as a vendor.

This configuration provides a common installation directory setup for all Intel tools installed on a system.

Inheritance

Members

_vendor = 'Intel'
The name of the tools vendor.

_section = 'INSTALL.Intel'
The name of the configuration section. Pattern: INSTALL.Vendor.ToolName.

_template = {'Linux': {'INSTALL.Intel': {'InstallationDirectory': '/opt/IntelFPGA
The template for the configuration sections represented as nested dictionaries.

_GetDefaultInstallationDirectory()
Return unresolved default installation directory (str) from template.

Overwrite function in sub-class for automatic search of installation directory.

CheckDependency()
Check if all vendor or tool dependencies are fulfilled to configure this tool.

ClearSection(*writeWarnings=False*)
Clear the configuration section associated to this Configuration class.

ConfigureForAll()
Start a generic (platform independent) vendor configuration procedure.

This method configures a vendor path. Overwrite this method to implement a vendor specific configuration routine for a vendor Configuration class.

ConfigureForDarwin()
Start the configuration procedure for Darwin.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Darwin specific configuration routine.

ConfigureForLinux()
Start the configuration procedure for Linux.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Linux specific configuration routine.

ConfigureForWindows()
Start the configuration procedure for Windows.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Windows specific configuration routine.

classmethod GetSections(*platform*)
Return all section names for this configuration.

Host
Return the hosting object.

IsConfigured()
Return true if the configurations section is configured

IsSupportedPlatform()
Return true if the given platform is supported by this configuration routine.

Log(*entry*, *condition=True*)
Write an entry to the local logger.

LogDebug(**args*, *condition=True*, ***kwargs*)

LogDryRun(**args*, *condition=True*, ***kwargs*)

LogError(**args*, *condition=True*, ***kwargs*)

LogFatal(**args*, *condition=True*, ***kwargs*)

LogInfo(**args*, *condition=True*, ***kwargs*)

LogNormal(**args*, *condition=True*, ***kwargs*)

LogQuiet(**args*, *condition=True*, ***kwargs*)

LogVerbose(**args*, *condition=True*, ***kwargs*)

LogWarning(**args*, *condition=True*, ***kwargs*)

Logger
Return the local logger instance.

PrepareOptions(*writeWarnings=True*)

PrepareSections(*warningWasWritten*, *writeWarnings=True*)

RunPostConfigurationTasks()
Virtual method. Overwrite to execute post-configuration tasks.

SectionName
Return the configuration's section name.

State
Return the configuration state.

_Ask(*question*, *default*, *beforeDefault=”*, *afterDefault=”*, *indent=1*)

_AskInstalled(*question*)
Ask a Yes/No/Pass question.

_AskYes_NoPass(*question*, *indent=1*)
Ask a yes/NO/pass question.

_Ask_YesNoPass(*question*, *indent=1*)
Ask a YES/no/pass question.

_ConfigureInstallationDirectory()
Asks for installation directory and updates section. Checks if entered directory exists and returns Path object. If no installation directory was configured before, then _GetDefaultInstallationDir is called.

_GetDefaultOptionValue(*optionName*)

_PrintAvailableEditions(*editions*, *selectedEdition*)
Print all available editions and return the selected index.

_TestDefaultInstallPath(*defaults*)
Helper function for automatic search of installation directory.

_TryLog(**args*, *condition=True*, ***kwargs*)

_multiVersionSupport = False

14.7.8 ToolChain.Lattice

Submodules

ToolChain.Lattice.ActiveHDL

ToolChain.Lattice.Diamond

Exceptions

- *DiamondException*: Base class for all tool specific exceptions

Classes

- *Configuration*: Base class for all tool Configuration classes.
- *Diamond*: Undocumented.
- *Synth*: Represent an executable.
- *SynthesisArgumentFile*: Undocumented.

Functions

- *MapFilter()*: Undocumented.
- *CompilerFilter()*: Undocumented.

exception ToolChain.Lattice.Diamond.**DiamondException**(*message=”*)

Inheritance

Members

__init__(*message=''*)
Exception initializer

Parameters **message** (*str*) – The exception message.

__str__()
Returns the exception's message text.

args

class ToolChain.Lattice.Diamond.**Configuration**(*host: Base.IHost*)

Inheritance

Members

_vendor = 'Lattice'
The name of the tools vendor.

_toolName = 'Lattice Diamond'
The name of the tool.

_section = 'INSTALL.Lattice.Diamond'
The name of the configuration section. Pattern: INSTALL.Vendor.ToolName.

_multiVersionSupport = True
Lattice Diamond supports multiple versions installed on the same system.

_template = {'Linux': {'INSTALL.Lattice.Diamond': {'Version': '3.8', 'SectionName
The template for the configuration sections represented as nested dictionaries.

CheckDependency()
Check if general Lattice support is configured in PoC.

ConfigureForAll()
Start a generic (platform independent) configuration procedure.

Overwrite this method to implement a generic configuration routine for a (tool) Configuration class.

_ConfigureBinaryDirectory()
Updates section with value from _template and returns directory as Path object.

ClearSection(*writeWarnings=False*)
Clear the configuration section associated to this Configuration class.

ConfigureForDarwin()
Start the configuration procedure for Darwin.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Darwin specific configuration routine.

ConfigureForLinux()
Start the configuration procedure for Linux.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Linux specific configuration routine.

ConfigureForWindows()
Start the configuration procedure for Windows.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Windows specific configuration routine.

classmethod GetSections(*platform*)
Return all section names for this configuration.

Host
Return the hosting object.

IsConfigured()
Return true if the configurations section is configured

IsSupportedPlatform()
Return true if the given platform is supported by this configuration routine.

Log(*entry*, *condition=True*)
Write an entry to the local logger.

LogDebug(**args*, *condition=True*, ***kwargs*)

LogDryRun(**args*, *condition=True*, ***kwargs*)

LogError(**args*, *condition=True*, ***kwargs*)

LogFatal(**args*, *condition=True*, ***kwargs*)

LogInfo(**args*, *condition=True*, ***kwargs*)

LogNormal(**args*, *condition=True*, ***kwargs*)

LogQuiet(**args*, *condition=True*, ***kwargs*)

LogVerbose(**args*, *condition=True*, ***kwargs*)

LogWarning(**args*, *condition=True*, ***kwargs*)

Logger
Return the local logger instance.

PrepareOptions(*writeWarnings=True*)

PrepareSections(*warningWasWritten*, *writeWarnings=True*)

PrepareVersionedSections(*writeWarnings=False*)

RunPostConfigurationTasks()
Virtual method. Overwrite to execute post-configuration tasks.

SectionName
Return the configuration's section name.

State
Return the configuration state.

_Ask(*question*, *default*, *beforeDefault=''*, *afterDefault=''*, *indent=1*)

_AskInstalled(*question*)
Ask a Yes/No/Pass question.

_AskYes_NoPass(*question*, *indent=1*)
Ask a yes/NO/pass question.

_Ask_YesNoPass(*question*, *indent=1*)
Ask a YES/no/pass question.

_Configuration__CheckDiamondVersion(*binPath*, *version*)

_ConfigureEdition(*editions*, *defaultEdition*)

_ConfigureInstallationDirectory()
Asks for installation directory and updates section. Checks if entered directory exists and returns Path object. If no installation directory was configured before, then _GetDefaultInstallationDir is called.

_ConfigureVersion()
If no version was configured before, then _GetDefaultVersion is called. Asks for version and updates section. Returns version as string.

_GetDefaultEdition()
Returns unresolved default edition (str) from template.

Overwrite this method in a sub-class for automatic search of editions.

_GetDefaultInstallationDirectory()
Return unresolved default installation directory (str) from template.

Overwrite function in sub-class for automatic search of installation directory.

_GetDefaultOptionValue(*optionName*)

_GetDefaultVersion()
Returns unresolved default version (str) from template.

Overwrite this method in a sub-class for automatic search of version.

_PrintAvailableEditions(*editions*, *selectedEdition*)
Print all available editions and return the selected index.

_TestDefaultInstallPath(*defaults*)
Helper function for automatic search of installation directory.

_TryLog(**args*, *condition=True*, ***kwargs*)

class ToolChain.Lattice.Diamond.**Diamond**(*platform*, *dryrun*, *binaryDirectoryPath*, *version*, *logger=None*)

Inheritance

Members

PreparseEnvironment(*installationDirectory*)

GetSynthesizer()

class ToolChain.Lattice.Diamond.**Synth**(*toolchain: ToolChain.ToolMixIn*)

Inheritance

Members

class Executable

class SwitchProjectFile

```
    _name = 'f'
    _value = None
```

Parameters = [<class 'ToolChain.Lattice.Diamond.Synth.Executable'>, <class 'ToolChai

static GetLogFileReader()

Compile(*logFile*)

GetReader()

HasErrors
True if errors or fatals errors were found while processing the output stream.

HasWarnings
: True if errors or fatals errors were found while processing the output stream.

Log(*entry*, *condition=True*)
: Write an entry to the local logger.

LogDebug(**args*, *condition=True*, ***kwargs*)

LogDryRun(**args*, *condition=True*, ***kwargs*)

LogError(**args*, *condition=True*, ***kwargs*)

LogFatal(**args*, *condition=True*, ***kwargs*)

LogInfo(**args*, *condition=True*, ***kwargs*)

LogNormal(**args*, *condition=True*, ***kwargs*)

LogQuiet(**args*, *condition=True*, ***kwargs*)

LogVerbose(**args*, *condition=True*, ***kwargs*)

LogWarning(**args*, *condition=True*, ***kwargs*)

Logger
: Return the local logger instance.

Path

ReadUntilBoundary(*indent=0*)

Send(*line*, *end='\n'*)

SendBoundary()

StartProcess(*parameterList*)

Terminate()

_POC_BOUNDARY = '====== POC BOUNDARY ======'

_TryLog(**args*, *condition=True*, ***kwargs*)

class ToolChain.Lattice.Diamond.**SynthesisArgumentFile**(*file*)

Inheritance

Members

Architecture

Device

SpeedGrade

Package

TopLevel

FileName

FileSet

FileType

LogFile

Open()

Path

Project

ReadFile()

_FileType = <FileTypes() bits=0x0000>

_ReadContent()

VHDLVersion

HDLParams

Write(*project*)

Functions

ToolChain.Lattice.Diamond.**MapFilter**(*gen*)

ToolChain.Lattice.Diamond.**CompilerFilter**(*gen*)

ToolChain.Lattice.Synplify

Exceptions

- *SynplifyException*: Base class for all tool specific exceptions

Classes

- *Configuration*: Base class for all tool Configuration classes.

exception ToolChain.Lattice.Synplify.**SynplifyException**(*message=''*)

Inheritance

Members

__init__(*message=''*)
Exception initializer

Parameters **message** (*str*) – The exception message.

__str__()
Returns the exception's message text.

args

class ToolChain.Lattice.Synplify.**Configuration**(*host*)

Inheritance

Members

CheckDependency()
Check if all vendor or tool dependencies are fulfilled to configure this tool.

ClearSection(*writeWarnings=False*)
Clear the configuration section associated to this Configuration class.

ConfigureForAll()
Start a generic (platform independent) configuration procedure.

Overwrite this method to implement a generic configuration routine for a (tool) Configuration class.

ConfigureForDarwin()
Start the configuration procedure for Darwin.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Darwin specific configuration routine.

ConfigureForLinux()
Start the configuration procedure for Linux.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Linux specific configuration routine.

ConfigureForWindows()
Start the configuration procedure for Windows.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Windows specific configuration routine.

classmethod GetSections(*platform*)
Return all section names for this configuration.

Host
Return the hosting object.

IsConfigured()
Return true if the configurations section is configured

IsSupportedPlatform()
Return true if the given platform is supported by this configuration routine.

Log(*entry*, *condition=True*)
Write an entry to the local logger.

LogDebug(**args*, *condition=True*, ***kwargs*)

LogDryRun(**args*, *condition=True*, ***kwargs*)

LogError(**args*, *condition=True*, ***kwargs*)

LogFatal(**args*, *condition=True*, ***kwargs*)

LogInfo(**args*, *condition=True*, ***kwargs*)

LogNormal(**args*, *condition=True*, ***kwargs*)

LogQuiet(**args*, *condition=True*, ***kwargs*)

LogVerbose(**args*, *condition=True*, ***kwargs*)

LogWarning(**args*, *condition=True*, ***kwargs*)

Logger
Return the local logger instance.

PrepareOptions(*writeWarnings=True*)

PrepareSections(*warningWasWritten*, *writeWarnings=True*)

PrepareVersionedSections(*writeWarnings=False*)

RunPostConfigurationTasks()
Virtual method. Overwrite to execute post-configuration tasks.

SectionName
Return the configuration's section name.

State
Return the configuration state.

_Ask(*question*, *default*, *beforeDefault=''*, *afterDefault=''*, *indent=1*)

_AskInstalled(*question*)
Ask a Yes/No/Pass question.

_AskYes_NoPass(*question*, *indent=1*)
Ask a yes/NO/pass question.

_Ask_YesNoPass(*question*, *indent=1*)
Ask a YES/no/pass question.

_ConfigureBinaryDirectory()
Updates section with value from *_template* and returns directory as Path object.

_ConfigureEdition(*editions*, *defaultEdition*)

_ConfigureInstallationDirectory()
Asks for installation directory and updates section. Checks if entered directory exists and returns Path object. If no installation directory was configured before, then _GetDefaultInstallationDir is called.

_ConfigureVersion()
If no version was configured before, then _GetDefaultVersion is called. Asks for version and updates section. Returns version as string.

_GetDefaultEdition()
Returns unresolved default edition (str) from template.

Overwrite this method in a sub-class for automatic search of editions.

_GetDefaultInstallationDirectory()
Return unresolved default installation directory (str) from template.

Overwrite function in sub-class for automatic search of installation directory.

_GetDefaultOptionValue(*optionName*)

_GetDefaultVersion()
Returns unresolved default version (str) from template.

Overwrite this method in a sub-class for automatic search of version.

_PrintAvailableEditions(*editions*, *selectedEdition*)
Print all available editions and return the selected index.

_TestDefaultInstallPath(*defaults*)
Helper function for automatic search of installation directory.

_TryLog(**args*, *condition=True*, ***kwargs*)

_multiVersionSupport = False

_section = 'INSTALL.Vendor.Tool'

_template = {'ALL': {'INSTALL.Vendor.Tool': {'Version': '1.0'}}, 'Darwin': {'INST

_toolName = 'Tool'

_vendor = 'Unknown'

Exceptions

- *LatticeException*: Base class for all tool specific exceptions

Classes

- *Configuration*: Configuration routines for Lattice as a vendor.
- *LatticeDesignConstraintFile*: Undocumented.

exception ToolChain.Lattice.**LatticeException**(*message=''*)

Inheritance

Members

__init__(*message=''*)
Exception initializer

Parameters **message** (*str*) – The exception message.

__str__()
Returns the exception's message text.

args

class ToolChain.Lattice.**Configuration**(*host: Base.IHost*)
Configuration routines for Lattice as a vendor.

This configuration provides a common installation directory setup for all Lattice tools installed on a system.

Inheritance

Members

_vendor = 'Lattice'
The name of the tools vendor.

_section = 'INSTALL.Lattice'
The name of the configuration section. Pattern: INSTALL.Vendor.ToolName.

_template = {'Linux': {'INSTALL.Lattice': {'InstallationDirectory': '/usr/local'
The template for the configuration sections represented as nested dictionaries.

_GetDefaultInstallationDirectory()
Return unresolved default installation directory (str) from template.

Overwrite function in sub-class for automatic search of installation directory.

CheckDependency()
Check if all vendor or tool dependencies are fulfilled to configure this tool.

ClearSection(*writeWarnings=False*)
Clear the configuration section associated to this Configuration class.

ConfigureForAll()
Start a generic (platform independent) vendor configuration procedure.

This method configures a vendor path. Overwrite this method to implement a vendor specific configuration routine for a vendor Configuration class.

ConfigureForDarwin()
Start the configuration procedure for Darwin.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Darwin specific configuration routine.

ConfigureForLinux()
Start the configuration procedure for Linux.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Linux specific configuration routine.

ConfigureForWindows()
Start the configuration procedure for Windows.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Windows specific configuration routine.

classmethod GetSections(*platform*)
Return all section names for this configuration.

Host
Return the hosting object.

IsConfigured()
Return true if the configurations section is configured

IsSupportedPlatform()
Return true if the given platform is supported by this configuration routine.

Log(*entry*, *condition=True*)
Write an entry to the local logger.

LogDebug(**args*, *condition=True*, ***kwargs*)

LogDryRun(**args*, *condition=True*, ***kwargs*)

LogError(**args*, *condition=True*, ***kwargs*)

LogFatal(**args*, *condition=True*, ***kwargs*)

LogInfo(**args*, *condition=True*, ***kwargs*)

LogNormal(**args*, *condition=True*, ***kwargs*)

LogQuiet(**args*, *condition=True*, ***kwargs*)

LogVerbose(**args*, *condition=True*, ***kwargs*)

LogWarning(**args*, *condition=True*, ***kwargs*)

Logger
Return the local logger instance.

PrepareOptions(*writeWarnings=True*)

PrepareSections(*warningWasWritten*, *writeWarnings=True*)

RunPostConfigurationTasks()
Virtual method. Overwrite to execute post-configuration tasks.

SectionName
Return the configuration's section name.

State
Return the configuration state.

_Ask(*question*, *default*, *beforeDefault=”*, *afterDefault=”*, *indent=1*)

_AskInstalled(*question*)
Ask a Yes/No/Pass question.

_AskYes_NoPass(*question*, *indent=1*)
Ask a yes/NO/pass question.

_Ask_YesNoPass(*question*, *indent=1*)
Ask a YES/no/pass question.

_ConfigureInstallationDirectory()
Asks for installation directory and updates section. Checks if entered directory exists and returns Path object. If no installation directory was configured before, then _GetDefaultInstallationDir is called.

_GetDefaultOptionValue(*optionName*)

_PrintAvailableEditions(*editions*, *selectedEdition*)
Print all available editions and return the selected index.

_TestDefaultInstallPath(*defaults*)
Helper function for automatic search of installation directory.

_TryLog(**args*, *condition=True*, ***kwargs*)

_multiVersionSupport = False

class ToolChain.Lattice.**LatticeDesignConstraintFile**(*file*, *project=None*, *fileSet=None*)

Inheritance

Members

_FileType = <FileTypes.LdcConstraintFile bits=0x2000 data=UNDEFINED>

FileName

FileSet

FileType

Open()

Path

Project

ReadFile()

_ReadContent()

14.7.9 ToolChain.Mentor

Submodules

ToolChain.Mentor.ModelSim

Exceptions

- *ModelSimException*: Base class for all tool specific exceptions

Classes

- *MentorModelSimPEEditions*: Enumeration of all ModelSim editions provided by Mentor Graphics itself.
- *ModelSimEditions*: Enumeration of all ModelSim editions provided by Mentor Graphics inclusive
- *Configuration*: Base class for all tool Configuration classes.
- *ModelSimPEConfiguration*: Base class for all tool Configuration classes.
- *ModelSimSE32Configuration*: Base class for all tool Configuration classes.
- *ModelSimSE64Configuration*: Base class for all tool Configuration classes.
- *Selector*: Base class for all Selector classes.
- *ModelSim*: Undocumented.
- *VHDLLibraryTool*: Represent an executable.
- *VHDLCompiler*: Represent an executable.
- *VHDLSimulator*: Represent an executable.

Functions

- *VLibFilter()*: Undocumented.

- *VComFilter()*: Undocumented.
- *VSimFilter()*: Undocumented.

exception ToolChain.Mentor.ModelSim.**ModelSimException**(*message=''*)

Inheritance

Members

__init__(*message=''*)
Exception initializer

Parameters **message** (*str*) – The exception message.

__str__()
Returns the exception's message text.

args

class ToolChain.Mentor.ModelSim.**MentorModelSimPEEditions**(*name*, *section*)
Enumeration of all ModelSim editions provided by Mentor Graphics itself.

Inheritance

Members

ModelSimPE = 1

ModelSimPEEducation = 2

class ToolChain.Mentor.ModelSim.**ModelSimEditions**(*name*, *section*)
Enumeration of all ModelSim editions provided by Mentor Graphics inclusive editions shipped by other vendors.

Inheritance

Members

ModelSimPE = 1

ModelSimDE = 2

ModelSimSE32 = 3

ModelSimSE64 = 4

ModelSimAlteraEdition = 5

ModelSimAlteraStarterEdition = 6

ModelSimIntelEdition = 7

ModelSimIntelStarterEdition = 8

QuestaSim = 9

class ToolChain.Mentor.ModelSim.**Configuration**(*host: Base.IHost*)

Inheritance

Members

_vendor = 'Mentor'
The name of the tools vendor.

_toolName = 'Mentor ModelSim'
The name of the tool.

_multiVersionSupport = True
Mentor ModelSim supports multiple versions installed on the same system.

CheckDependency()
Check if general Mentor Graphics support is configured in PoC.

ConfigureForAll()
Configuration routine for Mentor Graphics ModelSim on all supported platforms.

1. Ask if ModelSim is installed.

- Pass → skip this configuration. Don't change existing settings.
- Yes → collect installation information for ModelSim.
- No → clear the ModelSim configuration section.

1. Ask for ModelSim's version.
2. Ask for ModelSim's edition (PE, PE student, SE 32-bit, SE 64-bit).
3. Ask for ModelSim's installation directory.

_GetModelSimVersion(*binPath*)

_CheckModelSimVersion(*binPath*, *version*)

RunPostConfigurationTasks()
Virtual method. Overwrite to execute post-configuration tasks.

ClearSection(*writeWarnings=False*)
Clear the configuration section associated to this Configuration class.

ConfigureForDarwin()
Start the configuration procedure for Darwin.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Darwin specific configuration routine.

ConfigureForLinux()
Start the configuration procedure for Linux.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Linux specific configuration routine.

ConfigureForWindows()
Start the configuration procedure for Windows.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Windows specific configuration routine.

classmethod GetSections(*platform*)
Return all section names for this configuration.

Host
Return the hosting object.

IsConfigured()
Return true if the configurations section is configured

IsSupportedPlatform()
Return true if the given platform is supported by this configuration routine.

Log(*entry*, *condition=True*)
Write an entry to the local logger.

LogDebug(**args*, *condition=True*, ***kwargs*)

LogDryRun(**args*, *condition=True*, ***kwargs*)

LogError(**args*, *condition=True*, ***kwargs*)

LogFatal(**args*, *condition=True*, ***kwargs*)

LogInfo(**args*, *condition=True*, ***kwargs*)

LogNormal(**args*, *condition=True*, ***kwargs*)

LogQuiet(**args*, *condition=True*, ***kwargs*)

LogVerbose(**args*, *condition=True*, ***kwargs*)

LogWarning(**args*, *condition=True*, ***kwargs*)

Logger
Return the local logger instance.

PrepareOptions(*writeWarnings=True*)

PrepareSections(*warningWasWritten*, *writeWarnings=True*)

PrepareVersionedSections(*writeWarnings=False*)

SectionName
Return the configuration's section name.

State
Return the configuration state.

_Ask(*question*, *default*, *beforeDefault=''*, *afterDefault=''*, *indent=1*)

_AskInstalled(*question*)
Ask a Yes/No/Pass question.

_AskYes_NoPass(*question*, *indent=1*)
Ask a yes/NO/pass question.

_Ask_YesNoPass(*question*, *indent=1*)
Ask a YES/no/pass question.

_ConfigureBinaryDirectory()
Updates section with value from `_template` and returns directory as `Path` object.

_ConfigureEdition(*editions*, *defaultEdition*)

_ConfigureInstallationDirectory()
Asks for installation directory and updates section. Checks if entered directory exists and returns Path object. If no installation directory was configured before, then _GetDefaultInstallationDir is called.

_ConfigureVersion()
If no version was configured before, then _GetDefaultVersion is called. Asks for version and updates section. Returns version as string.

_GetDefaultEdition()
Returns unresolved default edition (str) from template.

Overwrite this method in a sub-class for automatic search of editions.

_GetDefaultInstallationDirectory()
Return unresolved default installation directory (str) from template.

Overwrite function in sub-class for automatic search of installation directory.

_GetDefaultOptionValue(*optionName*)

_GetDefaultVersion()
Returns unresolved default version (str) from template.

Overwrite this method in a sub-class for automatic search of version.

_PrintAvailableEditions(*editions*, *selectedEdition*)
Print all available editions and return the selected index.

_TestDefaultInstallPath(*defaults*)
Helper function for automatic search of installation directory.

_TryLog(**args*, *condition=True*, ***kwargs*)

_section = 'INSTALL.Vendor.Tool'

_template = {'ALL': {'INSTALL.Vendor.Tool': {'Version': '1.0'}}, 'Darwin': {'INST

class ToolChain.Mentor.ModelSim.**ModelSimPEConfiguration**(*host: Base.IHost*)

Inheritance

Members

_toolName = 'Mentor ModelSim PE'
The name of the tool.

_section = 'INSTALL.Mentor.ModelSimPE'
The name of the configuration section. Pattern: `INSTALL.Vendor.ToolName`.

_template = {'Windows': {'INSTALL.Mentor.ModelSimPE': {'Version': '10.5c', 'Sectio
The template for the configuration sections represented as nested dictionaries.

_ConfigureEdition()
Configure ModelSim PE for Mentor Graphics.

CheckDependency()
Check if general Mentor Graphics support is configured in PoC.

ClearSection(*writeWarnings=False*)
Clear the configuration section associated to this Configuration class.

ConfigureForAll()
Configuration routine for Mentor Graphics ModelSim on all supported platforms.

1. Ask if ModelSim is installed.

- Pass → skip this configuration. Don't change existing settings.
- Yes → collect installation information for ModelSim.
- No → clear the ModelSim configuration section.

1. Ask for ModelSim's version.
2. Ask for ModelSim's edition (PE, PE student, SE 32-bit, SE 64-bit).
3. Ask for ModelSim's installation directory.

ConfigureForDarwin()
Start the configuration procedure for Darwin.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Darwin specific configuration routine.

ConfigureForLinux()
Start the configuration procedure for Linux.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Linux specific configuration routine.

ConfigureForWindows()
Start the configuration procedure for Windows.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Windows specific configuration routine.

classmethod GetSections(*platform*)
Return all section names for this configuration.

Host
Return the hosting object.

IsConfigured()
Return true if the configurations section is configured

IsSupportedPlatform()
Return true if the given platform is supported by this configuration routine.

Log(*entry*, *condition=True*)
Write an entry to the local logger.

LogDebug(**args*, *condition=True*, ***kwargs*)

LogDryRun(**args*, *condition=True*, ***kwargs*)

LogError(**args*, *condition=True*, ***kwargs*)

LogFatal(**args*, *condition=True*, ***kwargs*)

LogInfo(**args*, *condition=True*, ***kwargs*)

LogNormal(**args*, *condition=True*, ***kwargs*)

LogQuiet(**args*, *condition=True*, ***kwargs*)

LogVerbose(**args*, *condition=True*, ***kwargs*)

LogWarning(**args*, *condition=True*, ***kwargs*)

Logger
Return the local logger instance.

PrepareOptions(*writeWarnings=True*)

PrepareSections(*warningWasWritten*, *writeWarnings=True*)

PrepareVersionedSections(*writeWarnings=False*)

RunPostConfigurationTasks()
Virtual method. Overwrite to execute post-configuration tasks.

SectionName
Return the configuration's section name.

State
Return the configuration state.

_Ask(*question*, *default*, *beforeDefault=''*, *afterDefault=''*, *indent=1*)

_AskInstalled(*question*)
Ask a Yes/No/Pass question.

_AskYes_NoPass(*question*, *indent=1*)
Ask a yes/NO/pass question.

_Ask_YesNoPass(*question*, *indent=1*)
Ask a YES/no/pass question.

_CheckModelSimVersion(*binPath*, *version*)

_ConfigureBinaryDirectory()
Updates section with value from *_template* and returns directory as Path object.

_ConfigureInstallationDirectory()
Asks for installation directory and updates section. Checks if entered directory exists and returns Path object. If no installation directory was configured before, then _GetDefaultInstallationDir is called.

_ConfigureVersion()
If no version was configured before, then _GetDefaultVersion is called. Asks for version and updates section. Returns version as string.

_GetDefaultEdition()
Returns unresolved default edition (str) from template.

Overwrite this method in a sub-class for automatic search of editions.

_GetDefaultInstallationDirectory()
Return unresolved default installation directory (str) from template.

Overwrite function in sub-class for automatic search of installation directory.

_GetDefaultOptionValue(*optionName*)

_GetDefaultVersion()
Returns unresolved default version (str) from template.

Overwrite this method in a sub-class for automatic search of version.

_GetModelSimVersion(*binPath*)

_PrintAvailableEditions(*editions*, *selectedEdition*)
Print all available editions and return the selected index.

_TestDefaultInstallPath(*defaults*)
Helper function for automatic search of installation directory.

_TryLog(**args*, *condition=True*, ***kwargs*)

_multiVersionSupport = True

_vendor = 'Mentor'

class ToolChain.Mentor.ModelSim.**ModelSimSE32Configuration**(*host: Base.IHost*)

Inheritance

Members

_toolName = 'Mentor ModelSim SE 32-bit'
The name of the tool.

_section = 'INSTALL.Mentor.ModelSimSE32'
The name of the configuration section. Pattern: INSTALL.Vendor.ToolName.

_template = {'Windows': {'INSTALL.Mentor.ModelSimSE32': {'Version': '10.5c', 'Se
The template for the configuration sections represented as nested dictionaries.

_ConfigureEdition()

CheckDependency()
Check if general Mentor Graphics support is configured in PoC.

ClearSection(*writeWarnings=False*)
Clear the configuration section associated to this Configuration class.

ConfigureForAll()
Configuration routine for Mentor Graphics ModelSim on all supported platforms.

1. Ask if ModelSim is installed.

   - Pass → skip this configuration. Don't change existing settings.
   - Yes → collect installation information for ModelSim.
   - No → clear the ModelSim configuration section.

1. Ask for ModelSim's version.
2. Ask for ModelSim's edition (PE, PE student, SE 32-bit, SE 64-bit).
3. Ask for ModelSim's installation directory.

ConfigureForDarwin()
Start the configuration procedure for Darwin.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Darwin specific configuration routine.

ConfigureForLinux()
Start the configuration procedure for Linux.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Linux specific configuration routine.

ConfigureForWindows()
Start the configuration procedure for Windows.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Windows specific configuration routine.

classmethod GetSections(*platform*)
Return all section names for this configuration.

Host
Return the hosting object.

IsConfigured()
Return true if the configurations section is configured

IsSupportedPlatform()
Return true if the given platform is supported by this configuration routine.

Log(*entry*, *condition=True*)
Write an entry to the local logger.

LogDebug(**args*, *condition=True*, ***kwargs*)

LogDryRun(**args*, *condition=True*, ***kwargs*)

LogError(**args*, *condition=True*, ***kwargs*)

LogFatal(**args*, *condition=True*, ***kwargs*)

LogInfo(**args*, *condition=True*, ***kwargs*)

LogNormal(**args*, *condition=True*, ***kwargs*)

LogQuiet(**args*, *condition=True*, ***kwargs*)

LogVerbose(**args*, *condition=True*, ***kwargs*)

LogWarning(**args*, *condition=True*, ***kwargs*)

Logger
Return the local logger instance.

PrepareOptions(*writeWarnings=True*)

PrepareSections(*warningWasWritten*, *writeWarnings=True*)

PrepareVersionedSections(*writeWarnings=False*)

RunPostConfigurationTasks()
Virtual method. Overwrite to execute post-configuration tasks.

SectionName
Return the configuration's section name.

State
Return the configuration state.

_Ask(*question*, *default*, *beforeDefault=''*, *afterDefault=''*, *indent=1*)

_AskInstalled(*question*)
Ask a Yes/No/Pass question.

_AskYes_NoPass(*question*, *indent=1*)
Ask a yes/NO/pass question.

_Ask_YesNoPass(*question*, *indent=1*)
Ask a YES/no/pass question.

_CheckModelSimVersion(*binPath*, *version*)

_ConfigureBinaryDirectory()
Updates section with value from `_template` and returns directory as `Path` object.

_ConfigureInstallationDirectory()
Asks for installation directory and updates section. Checks if entered directory exists and returns Path object. If no installation directory was configured before, then _GetDefaultInstallationDir is called.

_ConfigureVersion()
If no version was configured before, then _GetDefaultVersion is called. Asks for version and updates section. Returns version as string.

_GetDefaultEdition()
Returns unresolved default edition (str) from template.

Overwrite this method in a sub-class for automatic search of editions.

_GetDefaultInstallationDirectory()
Return unresolved default installation directory (str) from template.

Overwrite function in sub-class for automatic search of installation directory.

_GetDefaultOptionValue(*optionName*)

_GetDefaultVersion()
Returns unresolved default version (str) from template.

Overwrite this method in a sub-class for automatic search of version.

_GetModelSimVersion(*binPath*)

_PrintAvailableEditions(*editions*, *selectedEdition*)
Print all available editions and return the selected index.

_TestDefaultInstallPath(*defaults*)
Helper function for automatic search of installation directory.

_TryLog(**args*, *condition=True*, ***kwargs*)

_multiVersionSupport = True

_vendor = 'Mentor'

class ToolChain.Mentor.ModelSim.**ModelSimSE64Configuration**(*host: Base.IHost*)

Inheritance

Members

_toolName = 'Mentor ModelSim SE 64-bit'
The name of the tool.

_section = 'INSTALL.Mentor.ModelSimSE64'
The name of the configuration section. Pattern: INSTALL.Vendor.ToolName.

_template = {'Linux': {'INSTALL.Mentor.ModelSimSE64': {'Version': '10.5c', 'Secti
The template for the configuration sections represented as nested dictionaries.

_ConfigureEdition()

CheckDependency()
Check if general Mentor Graphics support is configured in PoC.

ClearSection(*writeWarnings=False*)
Clear the configuration section associated to this Configuration class.

ConfigureForAll()
Configuration routine for Mentor Graphics ModelSim on all supported platforms.

1. Ask if ModelSim is installed.

- Pass → skip this configuration. Don't change existing settings.
- Yes → collect installation information for ModelSim.
- No → clear the ModelSim configuration section.

1. Ask for ModelSim's version.
2. Ask for ModelSim's edition (PE, PE student, SE 32-bit, SE 64-bit).
3. Ask for ModelSim's installation directory.

ConfigureForDarwin()
Start the configuration procedure for Darwin.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Darwin specific configuration routine.

ConfigureForLinux()
Start the configuration procedure for Linux.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Linux specific configuration routine.

ConfigureForWindows()
Start the configuration procedure for Windows.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Windows specific configuration routine.

classmethod GetSections(*platform*)
Return all section names for this configuration.

Host
Return the hosting object.

IsConfigured()
Return true if the configurations section is configured

IsSupportedPlatform()
Return true if the given platform is supported by this configuration routine.

Log(*entry*, *condition=True*)
Write an entry to the local logger.

LogDebug(**args*, *condition=True*, ***kwargs*)

LogDryRun(**args*, *condition=True*, ***kwargs*)

LogError(**args*, *condition=True*, ***kwargs*)

LogFatal(**args*, *condition=True*, ***kwargs*)

LogInfo(**args*, *condition=True*, ***kwargs*)

LogNormal(**args*, *condition=True*, ***kwargs*)

LogQuiet(**args*, *condition=True*, ***kwargs*)

LogVerbose(**args*, *condition=True*, ***kwargs*)

LogWarning(**args*, *condition=True*, ***kwargs*)

Logger
Return the local logger instance.

PrepareOptions(*writeWarnings=True*)

PrepareSections(*warningWasWritten*, *writeWarnings=True*)

PrepareVersionedSections(*writeWarnings=False*)

RunPostConfigurationTasks()
Virtual method. Overwrite to execute post-configuration tasks.

SectionName
Return the configuration's section name.

State
Return the configuration state.

_Ask(*question*, *default*, *beforeDefault=''*, *afterDefault=''*, *indent=1*)

_AskInstalled(*question*)
Ask a Yes/No/Pass question.

_AskYes_NoPass(*question*, *indent=1*)
Ask a yes/NO/pass question.

_Ask_YesNoPass(*question*, *indent=1*)
Ask a YES/no/pass question.

_CheckModelSimVersion(*binPath*, *version*)

_ConfigureBinaryDirectory()
Updates section with value from `_template` and returns directory as `Path` object.

_ConfigureInstallationDirectory()
Asks for installation directory and updates section. Checks if entered directory exists and returns Path object. If no installation directory was configured before, then _GetDefaultInstallationDir is called.

_ConfigureVersion()
If no version was configured before, then _GetDefaultVersion is called. Asks for version and updates section. Returns version as string.

_GetDefaultEdition()
Returns unresolved default edition (str) from template.

Overwrite this method in a sub-class for automatic search of editions.

_GetDefaultInstallationDirectory()
Return unresolved default installation directory (str) from template.

Overwrite function in sub-class for automatic search of installation directory.

_GetDefaultOptionValue(*optionName*)

_GetDefaultVersion()
Returns unresolved default version (str) from template.

Overwrite this method in a sub-class for automatic search of version.

_GetModelSimVersion(*binPath*)

_PrintAvailableEditions(*editions*, *selectedEdition*)
Print all available editions and return the selected index.

_TestDefaultInstallPath(*defaults*)
Helper function for automatic search of installation directory.

_TryLog(**args*, *condition=True*, ***kwargs*)

_multiVersionSupport = True

_vendor = 'Mentor'

class ToolChain.Mentor.ModelSim.**Selector**(*host: Base.IHost*)

Inheritance

Members

_toolName = 'ModelSim'

Select()

Log(*entry*, *condition=True*)
Write an entry to the local logger.

LogDebug(**args*, *condition=True*, ***kwargs*)

LogDryRun(**args*, *condition=True*, ***kwargs*)

LogError(**args*, *condition=True*, ***kwargs*)

LogFatal(**args*, *condition=True*, ***kwargs*)

LogInfo(**args*, *condition=True*, ***kwargs*)

LogNormal(**args*, *condition=True*, ***kwargs*)

LogQuiet(**args*, *condition=True*, ***kwargs*)

LogVerbose(**args*, *condition=True*, ***kwargs*)

LogWarning(**args*, *condition=True*, ***kwargs*)

Logger
Return the local logger instance.

ToolName

_Ask(*question*, *default*, *beforeDefault=”*, *afterDefault=”*, *indent=1*)

_AskSelection(*editions*, *defaultEdition*)

_AskYes_NoPass(*question*, *indent=1*)
Ask a yes/NO/pass question.

_Ask_YesNoPass(*question*, *indent=1*)
Ask a YES/no/pass question.

_GetConfiguredEditions(*editions*)
Return all configured editions.

_PrintAvailableEditions(*editions*, *selectedEdition*)
Print all available editions and return the selected index.

_TryLog(**args*, *condition=True*, ***kwargs*)

class ToolChain.Mentor.ModelSim.**ModelSim**(*platform*, *dryrun*, *binaryDirectoryPath*, *version*, *logger=None*)

Inheritance

Members

GetVHDLLibraryTool()

GetVHDLCompiler()

GetSimulator()

class ToolChain.Mentor.ModelSim.**VHDLLibraryTool**(*toolchain: ToolChain.ToolMixIn*)

Inheritance

Members

class Executable

class SwitchLibraryName

Parameters = [<class 'ToolChain.Mentor.ModelSim.VHDLLibraryTool.Executable'>, <class

CreateLibrary()

GetReader()

HasErrors
True if errors or fatals errors were found while processing the output stream.

HasWarnings
True if errors or fatals errors were found while processing the output stream.

Log(*entry*, *condition=True*)
Write an entry to the local logger.

LogDebug(**args*, *condition=True*, ***kwargs*)

LogDryRun(**args*, *condition=True*, ***kwargs*)

LogError(**args*, *condition=True*, ***kwargs*)

LogFatal(**args*, *condition=True*, ***kwargs*)

LogInfo(**args*, *condition=True*, ***kwargs*)

LogNormal(**args*, *condition=True*, ***kwargs*)

LogQuiet(**args*, *condition=True*, ***kwargs*)

LogVerbose(**args*, *condition=True*, ***kwargs*)

LogWarning(**args*, *condition=True*, ***kwargs*)

Logger
Return the local logger instance.

Path

ReadUntilBoundary(*indent=0*)

Send(*line*, *end='\n'*)

SendBoundary()

StartProcess(*parameterList*)

Terminate()

_POC_BOUNDARY = '====== POC BOUNDARY ======'

_TryLog(**args*, *condition=True*, ***kwargs*)

class ToolChain.Mentor.ModelSim.**VHDLCompiler**(*toolchain: ToolChain.ToolMixIn*)

Inheritance

Members

class Executable

_value = None

class FlagTime

_name = 'time'

_value = None

class FlagExplicit

_name = 'explicit'

_value = None

class FlagQuietMode

_name = 'quiet'

_value = None

class SwitchModelSimIniFile

_name = 'modelsimini'

_value = None

class FlagRangeCheck

_name = 'rangecheck'

_value = None

class SwitchCoverage

_name = 'cover'

```
class FlagEnableFocusedExpressionCoverage

    _name = 'coverfec'
class FlagDisableFocusedExpressionCoverage

    _name = 'nocoverfec'
class FlagEnableRapidExpressionCoverage

    _name = 'coverrec'
class FlagDisableRapidExpressionCoverage

    _name = 'nocoverrec'
class FlagEnableRecognitionOfImplicitFSMResetTransitions

    _name = 'fsmresettrans'
class FlagDisableRecognitionOfImplicitFSMResetTransitions

    _name = 'nofsmresettrans'
class FlagEnableRecognitionOfSingleBitFSMState

    _name = 'fsmsingle'
class FlagDisableRecognitionOfSingleBitFSMState

    _name = 'nofsmsingle'
class FlagEnableRecognitionOfImplicitFSMTransitions

    _name = 'fsmimplicittrans'
class FlagDisableRecognitionOfImplicitFSMTransitions

    _name = 'nofsmimplicittrans'
class SwitchFSMVerbosityLevel

    _name = 'fsmverbose'
class FlagReportAsNote

    _name = 'note'
    _value = None
class FlagReportAsError

    _name = 'error'
    _value = None
class FlagReportAsWarning

    _name = 'warning'
```

```
    _value = None
class FlagReportAsFatal

    _name = 'fatal'
    _value = None
class FlagRelaxLanguageChecks

    _name = 'permissive'
class FlagForceLanguageChecks

    _name = 'pedanticerrors'
class SwitchVHDLVersion

    _pattern = '-{0}'
    _value = None
class ArgLogFile

    _name = 'l'
    _value = None
class SwitchVHDLLibrary

    _name = 'work'
    _value = None
class ArgSourceFile

    _value = None
Parameters = [<class 'ToolChain.Mentor.ModelSim.VHDLCompiler.Executable'>, <class '
```

Compile()

GetTclCommand()

GetReader()

HasErrors
: True if errors or fatals errors were found while processing the output stream.

HasWarnings
: True if errors or fatals errors were found while processing the output stream.

Log(*entry*, *condition=True*)
: Write an entry to the local logger.

LogDebug(**args*, *condition=True*, ***kwargs*)

LogDryRun(**args*, *condition=True*, ***kwargs*)

LogError(**args*, *condition=True*, ***kwargs*)

LogFatal(**args*, *condition=True*, ***kwargs*)

LogInfo(**args*, *condition=True*, ***kwargs*)

LogNormal(**args*, *condition=True*, ***kwargs*)

LogQuiet(**args*, *condition=True*, ***kwargs*)

LogVerbose(**args*, *condition=True*, ***kwargs*)

LogWarning(**args*, *condition=True*, ***kwargs*)

Logger
Return the local logger instance.

Path

ReadUntilBoundary(*indent=0*)

Send(*line*, *end='\n'*)

SendBoundary()

StartProcess(*parameterList*)

Terminate()

_POC_BOUNDARY = '====== POC BOUNDARY ======'

_TryLog(**args*, *condition=True*, ***kwargs*)

class ToolChain.Mentor.ModelSim.**VHDLSimulator**(*toolchain: ToolChain.ToolMixIn*)

Inheritance

Members

class Executable
The executable to launch.

_value = None

class FlagQuietMode
Run simulation in quiet mode. (Don't show 'Loading...' messages.

_name = 'quiet'

_value = None

class FlagBatchMode
Run simulation in batch mode.

_name = 'batch'

_value = None

class FlagGuiMode
Run simulation in GUI mode.

_name = 'gui'

_value = None

class SwitchBatchCommand
Specify a Tcl batch script for the batch mode.

_name = 'do'

_value = None

class FlagCommandLineMode
Run simulation in command line mode.

_name = 'c'

_value = None

class SwitchModelSimIniFile
Specify the used 'modelsim.ini' file.

```
_name = 'modelsimini'
_value = None
```

class FlagEnableOptimization
Enabled optimization while elaborating the design.

```
_name = 'vopt'
```

class FlagDisableOptimization
Disabled optimization while elaborating the design.

```
_name = 'novopt'
```

class FlagEnableOptimizationVerbosity
Enabled optimization while elaborating the design.

```
_name = 'vopt_verbose'
```

class FlagEnableKeepAssertionCountsForCoverage

```
_name = 'assertcover'
```

class FlagDisableKeepAssertionCountsForCoverage

```
_name = 'noassertcover'
```

class FlagEnableCoverage

```
_name = 'coverage'
```

class FlagDisableCoverage

```
_name = 'nocoverage'
```

class FlagEnablePSL

```
_name = 'psl'
```

class FlagDisablePSL

```
_name = 'nopsl'
```

class FlagEnableFSMDebugging

```
_name = 'fsmdebug'
```

class FlagReportAsNote

```
_name = 'note'
_value = None
```

class FlagReportAsError

```
_name = 'error'
_value = None
```

class FlagReportAsWarning

```
    _name = 'warning'
    _value = None
class FlagReportAsFatal

    _name = 'fatal'
    _value = None
class FlagRelaxLanguageChecks

    _name = 'permissive'
class FlagForceLanguageChecks

    _name = 'pedanticerrors'
class SwitchTimeResolution
```
Set simulation time resolution.

```
    _name = 't'
    _value = None
class ArgLogFile

    _name = 'l'
    _value = None
class ArgKeepStdOut

    _name = 'keepstdout'
class ArgVHDLLibraryName

    _name = 'lib'
    _value = None
class ArgOnFinishMode

    _name = 'onfinish'
    _value = None
class SwitchTopLevel
```
The top-level for simulation.

```
    _value = None
Parameters = [<class 'ToolChain.Mentor.ModelSim.VHDLSimulator.Executable'>, <class
```
Specify all accepted command line arguments

Simulate()
Start a simulation.

GetReader()

HasErrors
True if errors or fatals errors were found while processing the output stream.

HasWarnings
True if errors or fatals errors were found while processing the output stream.

Log(*entry*, *condition=True*)
Write an entry to the local logger.

LogDebug(**args*, *condition=True*, ***kwargs*)

LogDryRun(**args*, *condition=True*, ***kwargs*)

LogError(**args*, *condition=True*, ***kwargs*)

LogFatal(**args*, *condition=True*, ***kwargs*)

LogInfo(**args*, *condition=True*, ***kwargs*)

LogNormal(**args*, *condition=True*, ***kwargs*)

LogQuiet(**args*, *condition=True*, ***kwargs*)

LogVerbose(**args*, *condition=True*, ***kwargs*)

LogWarning(**args*, *condition=True*, ***kwargs*)

Logger
Return the local logger instance.

Path

ReadUntilBoundary(*indent=0*)

Send(*line*, *end='\n'*)

SendBoundary()

StartProcess(*parameterList*)

Terminate()

_POC_BOUNDARY = '====== POC BOUNDARY ======'

_TryLog(**args*, *condition=True*, ***kwargs*)

Functions

ToolChain.Mentor.ModelSim.**VLibFilter**(*gen*)

ToolChain.Mentor.ModelSim.**VComFilter**(*gen*)

ToolChain.Mentor.ModelSim.**VSimFilter**(*gen*)

ToolChain.Mentor.QuestaSim

Exceptions

- *QuestaSimException*: Base class for all tool specific exceptions

Classes

- *Configuration*: Base class for all tool Configuration classes.

exception ToolChain.Mentor.QuestaSim.**QuestaSimException**(*message=''*)

Inheritance

Members

__init__(*message=''*)
Exception initializer

Parameters **message** (*str*) – The exception message.

__str__()
Returns the exception's message text.

args

class ToolChain.Mentor.QuestaSim.**Configuration**(*host: Base.IHost*)

Inheritance

Members

_vendor = 'Mentor'
The name of the tools vendor.

_toolName = 'Mentor QuestaSim'
The name of the tool.

_section = 'INSTALL.Mentor.QuestaSim'
The name of the configuration section. Pattern: INSTALL.Vendor.ToolName.

_multiVersionSupport = True
Mentor QuestaSim supports multiple versions installed on the same system.

_template = {'Linux': {'INSTALL.Mentor.QuestaSim': {'Version': '10.5c', 'SectionN
The template for the configuration sections represented as nested dictionaries.

ConfigureForAll()
Configuration routine for Mentor Graphics ModelSim on all supported platforms.

1. Ask if ModelSim is installed.

   - Pass → skip this configuration. Don't change existing settings.
   - Yes → collect installation information for ModelSim.
   - No → clear the ModelSim configuration section.

1. Ask for ModelSim's version.
2. Ask for ModelSim's edition (PE, PE student, SE 32-bit, SE 64-bit).
3. Ask for ModelSim's installation directory.

_CheckQuestaSimVersion(*binPath*, *version*)

CheckDependency()
Check if general Mentor Graphics support is configured in PoC.

ClearSection(*writeWarnings=False*)
Clear the configuration section associated to this Configuration class.

ConfigureForDarwin()
Start the configuration procedure for Darwin.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Darwin specific configuration routine.

ConfigureForLinux()
Start the configuration procedure for Linux.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Linux specific configuration routine.

ConfigureForWindows()
Start the configuration procedure for Windows.

This method is a wrapper for `ConfigureForAll()`. Overwrite this method to implement a Windows specific configuration routine.

classmethod GetSections(*platform*)
Return all section names for this configuration.

Host
Return the hosting object.

IsConfigured()
Return true if the configurations section is configured

IsSupportedPlatform()
Return true if the given platform is supported by this configuration routine.

Log(*entry*, *condition=True*)
Write an entry to the local logger.

LogDebug(**args*, *condition=True*, ***kwargs*)

LogDryRun(**args*, *condition=True*, ***kwargs*)

LogError(**args*, *condition=True*, ***kwargs*)

LogFatal(**args*, *condition=True*, ***kwargs*)

LogInfo(**args*, *condition=True*, ***kwargs*)

LogNormal(**args*, *condition=True*, ***kwargs*)

LogQuiet(**args*, *condition=True*, ***kwargs*)

LogVerbose(**args*, *condition=True*, ***kwargs*)

LogWarning(**args*, *condition=True*, ***kwargs*)

Logger
Return the local logger instance.

PrepareOptions(*writeWarnings=True*)

PrepareSections(*warningWasWritten*, *writeWarnings=True*)

PrepareVersionedSections(*writeWarnings=False*)

RunPostConfigurationTasks()
Virtual method. Overwrite to execute post-configuration tasks.

SectionName
Return the configuration's section name.

State
Return the configuration state.

_Ask(*question*, *default*, *beforeDefault=''*, *afterDefault=''*, *indent=1*)

_AskInstalled(*question*)
Ask a Yes/No/Pass question.

_AskYes_NoPass(*question*, *indent=1*)
Ask a yes/NO/pass question.

_Ask_YesNoPass(*question*, *indent=1*)
Ask a YES/no/pass question.

_CheckModelSimVersion(*binPath*, *version*)

_ConfigureBinaryDirectory()
Updates section with value from `_template` and returns directory as `Path` object.

_ConfigureEdition(*editions*, *defaultEdition*)

_ConfigureInstallationDirectory()
Asks for installation directory and updates section. Checks if entered directory exists and returns Path object. If no installation directory was configured before, then _GetDefaultInstallationDir is called.

_ConfigureVersion()
If no version was configured before, then _GetDefaultVersion is called. Asks for version and updates section. Returns version as string.

_GetDefaultEdition()
Returns unresolved default edition (str) from template.

Overwrite this method in a sub-class for automatic search of editions.

_GetDefaultInstallationDirectory()
Return unresolved default installation directory (str) from template.

Overwrite function in sub-class for automatic search of installation directory.

_GetDefaultOptionValue(*optionName*)

_GetDefaultVersion()
Returns unresolved default version (str) from template.

Overwrite this method in a sub-class for automatic search of version.

_GetModelSimVersion(*binPath*)

_PrintAvailableEditions(*editions*, *selectedEdition*)
Print all available editions and return the selected index.

_TestDefaultInstallPath(*defaults*)
Helper function for automatic search of installation directory.

_TryLog(**args*, *condition=True*, ***kwargs*)

Exceptions

- *MentorException*: Base class for all tool specific exceptions

Classes

- *Configuration*: Configuration routines for Mentor Graphics as a vendor.

exception ToolChain.Mentor.**MentorException**(*message=''*)

Inheritance

Members

__init__(*message=''*)
Exception initializer

Parameters **message** (*str*) – The exception message.

__str__()
Returns the exception's message text.

args

class ToolChain.Mentor.**Configuration**(*host: Base.IHost*)
Configuration routines for Mentor Graphics as a vendor.

This configuration provides a common installation directory setup for all Mentor Graphics tools installed on a system.

Inheritance

Members

_vendor = 'Mentor'
The name of the tools vendor.

_section = 'INSTALL.Mentor'
The name of the configuration section. Pattern: `INSTALL.Vendor.ToolName`.

_template = {'ALL': {'INSTALL.ModelSim': {'SectionName': '', 'Version': '${${Sec
The template for the configuration sections represented as nested dictionaries.

_GetDefaultInstallationDirectory()
Return unresolved default installation directory (str) from template.

Overwrite function in sub-class for automatic search of installation directory.

CheckDependency()
Check if all vendor or tool dependencies are fulfilled to configure this tool.

ClearSection(*writeWarnings=False*)
Clear the configuration section associated to this Configuration class.

ConfigureForAll()
Start a generic (platform independent) vendor configuration procedure.

This method configures a vendor path. Overwrite this method to implement a vendor specific configuration routine for a vendor Configuration class.

ConfigureForDarwin()
Start the configuration procedure for Darwin.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Darwin specific configuration routine.

ConfigureForLinux()
Start the configuration procedure for Linux.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Linux specific configuration routine.

ConfigureForWindows()
Start the configuration procedure for Windows.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Windows specific configuration routine.

classmethod GetSections(*platform*)
Return all section names for this configuration.

Host
Return the hosting object.

IsConfigured()
Return true if the configurations section is configured

IsSupportedPlatform()
Return true if the given platform is supported by this configuration routine.

Log(*entry*, *condition=True*)
Write an entry to the local logger.

LogDebug(**args*, *condition=True*, ***kwargs*)

LogDryRun(**args*, *condition=True*, ***kwargs*)

LogError(**args*, *condition=True*, ***kwargs*)

LogFatal(**args*, *condition=True*, ***kwargs*)

LogInfo(**args*, *condition=True*, ***kwargs*)

LogNormal(**args*, *condition=True*, ***kwargs*)

LogQuiet(**args*, *condition=True*, ***kwargs*)

LogVerbose(**args*, *condition=True*, ***kwargs*)

LogWarning(**args*, *condition=True*, ***kwargs*)

Logger
Return the local logger instance.

PrepareOptions(*writeWarnings=True*)

PrepareSections(*warningWasWritten*, *writeWarnings=True*)

RunPostConfigurationTasks()
Virtual method. Overwrite to execute post-configuration tasks.

SectionName
Return the configuration's section name.

State
Return the configuration state.

_Ask(*question*, *default*, *beforeDefault=''*, *afterDefault=''*, *indent=1*)

_AskInstalled(*question*)
Ask a Yes/No/Pass question.

_AskYes_NoPass(*question*, *indent=1*)
Ask a yes/NO/pass question.

_Ask_YesNoPass(*question*, *indent=1*)
Ask a YES/no/pass question.

_ConfigureInstallationDirectory()
Asks for installation directory and updates section. Checks if entered directory exists and returns Path object. If no installation directory was configured before, then _GetDefaultInstallationDir is called.

_GetDefaultOptionValue(*optionName*)

_PrintAvailableEditions(*editions*, *selectedEdition*)
Print all available editions and return the selected index.

_TestDefaultInstallPath(*defaults*)
Helper function for automatic search of installation directory.

_TryLog(**args*, *condition=True*, ***kwargs*)

_multiVersionSupport = False

14.7.10 ToolChain.PoC

Classes

- *Configuration*: Base class for all tool Configuration classes.

class ToolChain.PoC.**Configuration**(*host: Base.IHost*)

Inheritance

Members

_vendor = 'VLSI-EDA'
The name of the tools vendor.

_toolName = 'PoC'
The name of the tool.

_section = 'INSTALL.PoC'
The name of the configuration section. Pattern: `INSTALL.Vendor.ToolName`.

_template = {'ALL': {'INSTALL.PoC': {'Version': '1.1.1', 'InstallationDirectory':
The template for the configuration sections represented as nested dictionaries.

ConfigureForAll()
Start a generic (platform independent) configuration procedure.

Overwrite this method to implement a generic configuration routine for a (tool) Configuration class.

RunPostConfigurationTasks()
Virtual method. Overwrite to execute post-configuration tasks.

CheckDependency()
Check if all vendor or tool dependencies are fulfilled to configure this tool.

ClearSection(*writeWarnings=False*)
Clear the configuration section associated to this Configuration class.

ConfigureForDarwin()
Start the configuration procedure for Darwin.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Darwin specific configuration routine.

ConfigureForLinux()
Start the configuration procedure for Linux.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Linux specific configuration routine.

ConfigureForWindows()
Start the configuration procedure for Windows.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Windows specific configuration routine.

classmethod GetSections(*platform*)
Return all section names for this configuration.

Host
Return the hosting object.

IsConfigured()
Return true if the configurations section is configured

IsSupportedPlatform()
Return true if the given platform is supported by this configuration routine.

Log(*entry*, *condition=True*)
Write an entry to the local logger.

LogDebug(**args*, *condition=True*, ***kwargs*)

LogDryRun(**args*, *condition=True*, ***kwargs*)

LogError(**args*, *condition=True*, ***kwargs*)

LogFatal(**args*, *condition=True*, ***kwargs*)

LogInfo(**args*, *condition=True*, ***kwargs*)

LogNormal(**args*, *condition=True*, ***kwargs*)

LogQuiet(**args*, *condition=True*, ***kwargs*)

LogVerbose(**args*, *condition=True*, ***kwargs*)

LogWarning(**args*, *condition=True*, ***kwargs*)

Logger
Return the local logger instance.

PrepareOptions(*writeWarnings=True*)

PrepareSections(*warningWasWritten*, *writeWarnings=True*)

PrepareVersionedSections(*writeWarnings=False*)

SectionName
Return the configuration's section name.

State
Return the configuration state.

_Ask(*question*, *default*, *beforeDefault=''*, *afterDefault=''*, *indent=1*)

_AskInstalled(*question*)
Ask a Yes/No/Pass question.

_AskYes_NoPass(*question*, *indent=1*)
Ask a yes/NO/pass question.

_Ask_YesNoPass(*question*, *indent=1*)
Ask a YES/no/pass question.

_ConfigureBinaryDirectory()
Updates section with value from `_template` and returns directory as `Path` object.

_ConfigureEdition(*editions*, *defaultEdition*)

_ConfigureInstallationDirectory()
Asks for installation directory and updates section. Checks if entered directory exists and returns Path object. If no installation directory was configured before, then _GetDefaultInstallationDir is called.

_ConfigureVersion()
If no version was configured before, then _GetDefaultVersion is called. Asks for version and updates section. Returns version as string.

_GetDefaultEdition()
Returns unresolved default edition (str) from template.

Overwrite this method in a sub-class for automatic search of editions.

_GetDefaultInstallationDirectory()
Return unresolved default installation directory (str) from template.

Overwrite function in sub-class for automatic search of installation directory.

_GetDefaultOptionValue(*optionName*)

_GetDefaultVersion()
Returns unresolved default version (str) from template.

Overwrite this method in a sub-class for automatic search of version.

_PrintAvailableEditions(*editions*, *selectedEdition*)
Print all available editions and return the selected index.

_TestDefaultInstallPath(*defaults*)
Helper function for automatic search of installation directory.

_TryLog(**args*, *condition=True*, ***kwargs*)

_multiVersionSupport = False

14.7.11 ToolChain.Synopsys

Exceptions

- *SynopsysException*: Base class for all tool specific exceptions

Classes

- *Configuration*: Configuration routines for Synopsys as a vendor.
- *SynopsysDesignConstraintFile*: Undocumented.

exception ToolChain.Synopsys.**SynopsysException**(*message=''*)

Inheritance

Members

__init__(*message=''*)
Exception initializer

Parameters **message** (*str*) – The exception message.

__str__()
Returns the exception's message text.

args

class ToolChain.Synopsys.**Configuration**(*host: Base.IHost*)
Configuration routines for Synopsys as a vendor.

This configuration provides a common installation directory setup for all Synopsys tools installed on a system.

Inheritance

Members

_vendor = 'Synopsys'
The name of the tools vendor.

_section = 'INSTALL.Synopsys'
The name of the configuration section. Pattern: INSTALL.Vendor.ToolName.

_template = {'Linux': {'INSTALL.Synopsys': {'InstallationDirectory': '/opt/Synops
The template for the configuration sections represented as nested dictionaries.

_GetDefaultInstallationDirectory()
Return unresolved default installation directory (str) from template.

Overwrite function in sub-class for automatic search of installation directory.

CheckDependency()
Check if all vendor or tool dependencies are fulfilled to configure this tool.

ClearSection(*writeWarnings=False*)
Clear the configuration section associated to this Configuration class.

ConfigureForAll()
Start a generic (platform independent) vendor configuration procedure.

This method configures a vendor path. Overwrite this method to implement a vendor specific configuration routine for a vendor Configuration class.

ConfigureForDarwin()
Start the configuration procedure for Darwin.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Darwin specific configuration routine.

ConfigureForLinux()
Start the configuration procedure for Linux.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Linux specific configuration routine.

ConfigureForWindows()
Start the configuration procedure for Windows.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Windows specific configuration routine.

classmethod GetSections(*platform*)
Return all section names for this configuration.

Host
Return the hosting object.

IsConfigured()
Return true if the configurations section is configured

IsSupportedPlatform()
Return true if the given platform is supported by this configuration routine.

Log(*entry*, *condition=True*)
Write an entry to the local logger.

LogDebug(**args*, *condition=True*, ***kwargs*)

LogDryRun(**args*, *condition=True*, ***kwargs*)

LogError(**args*, *condition=True*, ***kwargs*)

LogFatal(**args*, *condition=True*, ***kwargs*)

LogInfo(**args*, *condition=True*, ***kwargs*)

LogNormal(**args*, *condition=True*, ***kwargs*)

LogQuiet(**args*, *condition=True*, ***kwargs*)

LogVerbose(**args*, *condition=True*, ***kwargs*)

LogWarning(**args*, *condition=True*, ***kwargs*)

Logger
Return the local logger instance.

PrepareOptions(*writeWarnings=True*)

PrepareSections(*warningWasWritten*, *writeWarnings=True*)

RunPostConfigurationTasks()
Virtual method. Overwrite to execute post-configuration tasks.

SectionName
Return the configuration's section name.

State
Return the configuration state.

_Ask(*question*, *default*, *beforeDefault=”*, *afterDefault=”*, *indent=1*)

_AskInstalled(*question*)
Ask a Yes/No/Pass question.

_AskYes_NoPass(*question*, *indent=1*)
Ask a yes/NO/pass question.

_Ask_YesNoPass(*question*, *indent=1*)
Ask a YES/no/pass question.

_ConfigureInstallationDirectory()
Asks for installation directory and updates section. Checks if entered directory exists and returns Path object. If no installation directory was configured before, then _GetDefaultInstallationDir is called.

_GetDefaultOptionValue(*optionName*)

_PrintAvailableEditions(*editions*, *selectedEdition*)
Print all available editions and return the selected index.

_TestDefaultInstallPath(*defaults*)
Helper function for automatic search of installation directory.

_TryLog(**args*, *condition=True*, ***kwargs*)

_multiVersionSupport = False

class ToolChain.Synopsys.**SynopsysDesignConstraintFile**(*file*, *project=None*, *fileSet=None*)

Inheritance

Members

_FileType = <FileTypes.SdcConstraintFile bits=0x1000 data=UNDEFINED>

FileName

FileSet

FileType

Open()

Path

Project

ReadFile()

_ReadContent()

14.7.12 ToolChain.Windows

Exceptions

- *WindowsException*: Base class for all tool specific exceptions

Classes

- *Cmd*: Represent an executable.

exception ToolChain.Windows.**WindowsException**(*message=”*)

Inheritance

Members

__init__(*message=''*)
Exception initializer

Parameters **message** (*str*) – The exception message.

__str__()
Returns the exception's message text.

args

class ToolChain.Windows.**Cmd**(*platform*, *dryrun*, *logger=None*)

Inheritance

Members

class Executable

class SwitchCommand

_name = 'C'

Parameters = [<class 'ToolChain.Windows.Cmd.Executable'>, <class 'ToolChain.Windows

GetEnvironment(*settingsFile=None*)

GetReader()

Log(*entry*, *condition=True*)
Write an entry to the local logger.

LogDebug(**args*, *condition=True*, ***kwargs*)

LogDryRun(**args*, *condition=True*, ***kwargs*)

LogError(**args*, *condition=True*, ***kwargs*)

LogFatal(**args*, *condition=True*, ***kwargs*)

LogInfo(**args*, *condition=True*, ***kwargs*)

LogNormal(**args*, *condition=True*, ***kwargs*)

LogQuiet(**args*, *condition=True*, ***kwargs*)

LogVerbose(**args*, *condition=True*, ***kwargs*)

LogWarning(**args*, *condition=True*, ***kwargs*)

Logger
Return the local logger instance.

Path

ReadUntilBoundary(*indent=0*)

Send(*line*, *end='\n'*)

SendBoundary()

StartProcess(*parameterList*)

Terminate()

_POC_BOUNDARY = '====== POC BOUNDARY ======'

_TryLog(**args*, *condition=True*, ***kwargs*)

14.7.13 ToolChain.Xilinx

Submodules

ToolChain.Xilinx.ISE

Exceptions

- *ISEException*: Base class for all tool specific exceptions

Classes

- *Configuration*: Base class for all tool Configuration classes.
- *ISE*: Undocumented.
- *Fuse*: Represent an executable.
- *ISESimulator*: Represent an executable.
- *Xst*: Represent an executable.
- *CoreGenerator*: Represent an executable.
- *ISEProject*: Undocumented.
- *ISEProjectFile*: Undocumented.
- *UserConstraintFile*: Undocumented.

Functions

- *VhCompFilter()*: Undocumented.
- *FuseFilter()*: Undocumented.
- *SimulatorFilter()*: Undocumented.
- *XstFilter()*: Undocumented.
- *CoreGeneratorFilter()*: Undocumented.

exception ToolChain.Xilinx.ISE.**ISEException**(*message=''*)

Inheritance

Members

__init__(*message=''*)
Exception initializer

Parameters **message** (*str*) – The exception message.

__str__()
Returns the exception's message text.

args

class ToolChain.Xilinx.ISE.**Configuration**(*host: Base.IHost*)

Inheritance

Members

_vendor = 'Xilinx'
The name of the tools vendor.

_toolName = 'Xilinx ISE'
The name of the tool.

_section = 'INSTALL.Xilinx.ISE'
The name of the configuration section. Pattern: `INSTALL.Vendor.ToolName`.

_multiVersionSupport = True
Xilinx ISE supports multiple versions installed on the same system.

_template = {'Linux': {'INSTALL.Xilinx.ISE': {'Version': '14.7', 'SectionName':
The template for the configuration sections represented as nested dictionaries.

CheckDependency()
Check if general Xilinx support is configured in PoC.

ConfigureForAll()
Start a generic (platform independent) configuration procedure.

Overwrite this method to implement a generic configuration routine for a (tool) Configuration class.

ClearSection(*writeWarnings=False*)
Clear the configuration section associated to this Configuration class.

ConfigureForDarwin()
Start the configuration procedure for Darwin.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Darwin specific configuration routine.

ConfigureForLinux()
Start the configuration procedure for Linux.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Linux specific configuration routine.

ConfigureForWindows()
Start the configuration procedure for Windows.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Windows specific configuration routine.

classmethod GetSections(*platform*)
Return all section names for this configuration.

Host
Return the hosting object.

IsConfigured()
Return true if the configurations section is configured

IsSupportedPlatform()
Return true if the given platform is supported by this configuration routine.

Log(*entry*, *condition=True*)
Write an entry to the local logger.

LogDebug(**args*, *condition=True*, ***kwargs*)

LogDryRun(**args*, *condition=True*, ***kwargs*)

LogError(**args*, *condition=True*, ***kwargs*)

LogFatal(**args*, *condition=True*, ***kwargs*)

LogInfo(**args*, *condition=True*, ***kwargs*)

LogNormal(**args*, *condition=True*, ***kwargs*)

LogQuiet(**args*, *condition=True*, ***kwargs*)

LogVerbose(**args*, *condition=True*, ***kwargs*)

LogWarning(**args*, *condition=True*, ***kwargs*)

Logger
Return the local logger instance.

PrepareOptions(*writeWarnings=True*)

PrepareSections(*warningWasWritten*, *writeWarnings=True*)

PrepareVersionedSections(*writeWarnings=False*)

RunPostConfigurationTasks()
Virtual method. Overwrite to execute post-configuration tasks.

SectionName
Return the configuration's section name.

State
Return the configuration state.

_Ask(*question*, *default*, *beforeDefault=''*, *afterDefault=''*, *indent=1*)

_AskInstalled(*question*)
Ask a Yes/No/Pass question.

_AskYes_NoPass(*question*, *indent=1*)
Ask a yes/NO/pass question.

_Ask_YesNoPass(*question*, *indent=1*)
Ask a YES/no/pass question.

_Configuration__CheckISEVersion(*binPath*)

_ConfigureBinaryDirectory()
Updates section with value from `_template` and returns directory as `Path` object.

_ConfigureEdition(*editions*, *defaultEdition*)

_ConfigureInstallationDirectory()
Asks for installation directory and updates section. Checks if entered directory exists and returns Path object. If no installation directory was configured before, then _GetDefaultInstallationDir is called.

_ConfigureVersion()
If no version was configured before, then _GetDefaultVersion is called. Asks for version and updates section. Returns version as string.

_GetDefaultEdition()
Returns unresolved default edition (str) from template.

Overwrite this method in a sub-class for automatic search of editions.

_GetDefaultInstallationDirectory()
Return unresolved default installation directory (str) from template.

Overwrite function in sub-class for automatic search of installation directory.

_GetDefaultOptionValue(*optionName*)

_GetDefaultVersion()
Returns unresolved default version (str) from template.

Overwrite this method in a sub-class for automatic search of version.

_PrintAvailableEditions(*editions*, *selectedEdition*)
Print all available editions and return the selected index.

_TestDefaultInstallPath(*defaults*)
Helper function for automatic search of installation directory.

_TryLog(**args*, *condition=True*, ***kwargs*)

class ToolChain.Xilinx.ISE.**ISE**(*platform*, *dryrun*, *binaryDirectoryPath*, *version*, *logger=None*)

Inheritance

Members

PreparseEnvironment(*installationDirectory*)

GetVHDLCompiler()

GetFuse()

GetXst()

GetCoreGenerator()

class ToolChain.Xilinx.ISE.**Fuse**(*toolchain: ToolChain.ToolMixIn*)

Inheritance

Members

class Executable

class FlagIncremental

```
    _name = 'incremental'
```

class FlagRangeCheck

```
    _name = 'rangecheck'
```

class SwitchMultiThreading

```
    _name = 'mt'
```

class SwitchTimeResolution

```
    _name = 'timeprecision_vhdl'
```

class SwitchProjectFile

```
    _name = 'prj'
```

class SwitchOutputFile

```
    _name = 'o'
```

class ArgTopLevel

```
Parameters = [<class 'ToolChain.Xilinx.ISE.Fuse.Executable'>, <class 'ToolChain.Xili
```

Link()

GetReader()

HasErrors
True if errors or fatals errors were found while processing the output stream.

HasWarnings
True if errors or fatals errors were found while processing the output stream.

Log(*entry*, *condition=True*)
Write an entry to the local logger.

LogDebug(**args*, *condition=True*, ***kwargs*)

LogDryRun(**args*, *condition=True*, ***kwargs*)

LogError(**args*, *condition=True*, ***kwargs*)

LogFatal(**args*, *condition=True*, ***kwargs*)

LogInfo(**args*, *condition=True*, ***kwargs*)

LogNormal(**args*, *condition=True*, ***kwargs*)

LogQuiet(**args*, *condition=True*, ***kwargs*)

LogVerbose(**args*, *condition=True*, ***kwargs*)

LogWarning(**args*, *condition=True*, ***kwargs*)

Logger
Return the local logger instance.

Path

ReadUntilBoundary(*indent=0*)

Send(*line*, *end='\n'*)

SendBoundary()

StartProcess(*parameterList*)

Terminate()

_POC_BOUNDARY = '====== POC BOUNDARY ======'

_TryLog(**args*, *condition=True*, ***kwargs*)

class ToolChain.Xilinx.ISE.**ISESimulator**(*platform*, *dryrun*, *executablePath*, *environment*, *logger=None*)

Inheritance

Members

class Executable

class SwitchLogFile

_name = 'log'

class FlagGuiMode

_name = 'gui'

class SwitchTclBatchFile

```
        _name = 'tclbatch'
```

class SwitchWaveformFile

```
        _name = 'view'
```

Parameters = [<class 'ToolChain.Xilinx.ISE.ISESimulator.Executable'>, <class 'ToolCh

Simulate()

GetReader()

HasErrors
: True if errors or fatals errors were found while processing the output stream.

HasWarnings
: True if errors or fatals errors were found while processing the output stream.

Log(*entry*, *condition=True*)
: Write an entry to the local logger.

LogDebug(**args*, *condition=True*, ***kwargs*)

LogDryRun(**args*, *condition=True*, ***kwargs*)

LogError(**args*, *condition=True*, ***kwargs*)

LogFatal(**args*, *condition=True*, ***kwargs*)

LogInfo(**args*, *condition=True*, ***kwargs*)

LogNormal(**args*, *condition=True*, ***kwargs*)

LogQuiet(**args*, *condition=True*, ***kwargs*)

LogVerbose(**args*, *condition=True*, ***kwargs*)

LogWarning(**args*, *condition=True*, ***kwargs*)

Logger
: Return the local logger instance.

Path

ReadUntilBoundary(*indent=0*)

Send(*line*, *end='\n'*)

SendBoundary()

StartProcess(*parameterList*)

Terminate()

_POC_BOUNDARY = '====== POC BOUNDARY ======'

_TryLog(**args*, *condition=True*, ***kwargs*)

class ToolChain.Xilinx.ISE.**Xst**(*toolchain: ToolChain.ToolMixIn*)

Inheritance

Members

class Executable

class SwitchIntStyle

```
        _name = 'intstyle'
```

class SwitchXstFile

_name = 'ifn'

class SwitchReportFile

_name = 'ofn'

Parameters = [<class 'ToolChain.Xilinx.ISE.Xst.Executable'>, <class 'ToolChain.Xilin

Compile()

GetReader()

HasErrors
True if errors or fatals errors were found while processing the output stream.

HasWarnings
True if errors or fatals errors were found while processing the output stream.

Log(*entry*, *condition=True*)
Write an entry to the local logger.

LogDebug(**args*, *condition=True*, ***kwargs*)

LogDryRun(**args*, *condition=True*, ***kwargs*)

LogError(**args*, *condition=True*, ***kwargs*)

LogFatal(**args*, *condition=True*, ***kwargs*)

LogInfo(**args*, *condition=True*, ***kwargs*)

LogNormal(**args*, *condition=True*, ***kwargs*)

LogQuiet(**args*, *condition=True*, ***kwargs*)

LogVerbose(**args*, *condition=True*, ***kwargs*)

LogWarning(**args*, *condition=True*, ***kwargs*)

Logger
Return the local logger instance.

Path

ReadUntilBoundary(*indent=0*)

Send(*line*, *end='\n'*)

SendBoundary()

StartProcess(*parameterList*)

Terminate()

_POC_BOUNDARY = '====== POC BOUNDARY ======'

_TryLog(**args*, *condition=True*, ***kwargs*)

class ToolChain.Xilinx.ISE.**CoreGenerator**(*toolchain: ToolChain.ToolMixIn*)

Inheritance

Members

class Executable

class FlagRegenerate

_name = 'r'

class SwitchProjectFile

_name = 'p'

class SwitchBatchFile

_name = 'b'

Parameters = [<class 'ToolChain.Xilinx.ISE.CoreGenerator.Executable'>, <class 'ToolC

Generate()

GetReader()

HasErrors
True if errors or fatals errors were found while processing the output stream.

HasWarnings
True if errors or fatals errors were found while processing the output stream.

Log(*entry*, *condition=True*)
Write an entry to the local logger.

LogDebug(**args*, *condition=True*, ***kwargs*)

LogDryRun(**args*, *condition=True*, ***kwargs*)

LogError(**args*, *condition=True*, ***kwargs*)

LogFatal(**args*, *condition=True*, ***kwargs*)

LogInfo(**args*, *condition=True*, ***kwargs*)

LogNormal(**args*, *condition=True*, ***kwargs*)

LogQuiet(**args*, *condition=True*, ***kwargs*)

LogVerbose(**args*, *condition=True*, ***kwargs*)

LogWarning(**args*, *condition=True*, ***kwargs*)

Logger
Return the local logger instance.

Path

ReadUntilBoundary(*indent=0*)

Send(*line*, *end='\n'*)

SendBoundary()

StartProcess(*parameterList*)

Terminate()

_POC_BOUNDARY = '====== POC BOUNDARY ======'

_TryLog(**args*, *condition=True*, ***kwargs*)

class ToolChain.Xilinx.ISE.**ISEProject**(*name*)

Inheritance

Members

AddExternalVHDLLibraries(*library*)

AddFile(*file*, *fileSet=None*)

AddFileSet(*fileSet*)

AddSourceFile(*file*, *fileSet=None*)

Board

CreateFileSet(*name*, *setDefault=True*)

DefaultFileSet

Device

Environment

ExternalVHDLLibraries

ExtractVHDLLibrariesFromVHDLSourceFiles()

FileSets

Files(*fileType=<FileTypes(Text|ProjectFile|FileListFile|RulesFile|SourceFile|VHDLSourceFile|VerilogSourceFile|Python*
bits=0xFFFF>, *fileSet=None*)

GetVariables()

Name

RootDirectory

Tool

ToolChain

VHDLLibraries

VHDLVersion

pprint(*indent=0*)

class ToolChain.Xilinx.ISE.**ISEProjectFile**(*file*)

Inheritance

Members

FileName

FileSet

FileType

Open()

Path

Project

ReadFile()

_FileType = <FileTypes.ProjectFile bits=0x0002 data=UNDEFINED>

_ReadContent()

class ToolChain.Xilinx.ISE.**UserConstraintFile**(*file*, *project=None*, *fileSet=None*)

Inheritance

Members

_FileType = <FileTypes.UcfConstraintFile bits=0x0400 data=UNDEFINED>

FileName

FileSet

FileType

Open()

Path

Project

ReadFile()

_ReadContent()

Functions

ToolChain.Xilinx.ISE.**VhCompFilter**(*gen*)

ToolChain.Xilinx.ISE.**FuseFilter**(*gen*)

ToolChain.Xilinx.ISE.**SimulatorFilter**(*gen*)

ToolChain.Xilinx.ISE.**XstFilter**(*gen*)

ToolChain.Xilinx.ISE.**CoreGeneratorFilter**(*gen*)

ToolChain.Xilinx.Vivado

Exceptions

- *VivadoException*: Base class for all tool specific exceptions

Classes

- *Configuration*: Base class for all tool Configuration classes.
- *ToolMixIn*: Undocumented.
- *Vivado*: Undocumented.
- *XElab*: Represent an executable.
- *XSim*: Represent an executable.
- *Synth*: Represent an executable.
- *VivadoProject*: Undocumented.
- *VivadoProjectFile*: Undocumented.
- *XilinxDesignConstraintFile*: Undocumented.

Functions

- *ElaborationFilter()*: Undocumented.
- *SimulatorFilter()*: Undocumented.
- *CompilerFilter()*: Undocumented.

exception ToolChain.Xilinx.Vivado.**VivadoException**(*message=''*)

Inheritance

Members

__init__(*message=''*)
Exception initializer

Parameters **message** (*str*) – The exception message.

__str__()
Returns the exception's message text.

args

class ToolChain.Xilinx.Vivado.**Configuration**(*host: Base.IHost*)

Inheritance

Members

_vendor = 'Xilinx'
The name of the tools vendor.

_toolName = 'Xilinx Vivado'
The name of the tool.

_section = 'INSTALL.Xilinx.Vivado'
The name of the configuration section. Pattern: INSTALL.Vendor.ToolName.

_multiVersionSupport = True
Xilinx Vivado supports multiple versions installed on the same system.

_template = {'Linux': {'INSTALL.Xilinx.Vivado': {'Version': '2016.3', 'SectionNa
The template for the configuration sections represented as nested dictionaries.

CheckDependency()
Check if general Xilinx support is configured in PoC.

ConfigureForAll()
Start a generic (platform independent) configuration procedure.

Overwrite this method to implement a generic configuration routine for a (tool) Configuration class.

ClearSection(*writeWarnings=False*)
Clear the configuration section associated to this Configuration class.

ConfigureForDarwin()
Start the configuration procedure for Darwin.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Darwin specific configuration routine.

ConfigureForLinux()
Start the configuration procedure for Linux.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Linux specific configuration routine.

ConfigureForWindows()
Start the configuration procedure for Windows.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Windows specific configuration routine.

classmethod GetSections(*platform*)
Return all section names for this configuration.

Host
Return the hosting object.

IsConfigured()
Return true if the configurations section is configured

IsSupportedPlatform()
Return true if the given platform is supported by this configuration routine.

Log(*entry*, *condition=True*)
Write an entry to the local logger.

LogDebug(**args*, *condition=True*, ***kwargs*)

LogDryRun(**args*, *condition=True*, ***kwargs*)

LogError(**args*, *condition=True*, ***kwargs*)

LogFatal(**args*, *condition=True*, ***kwargs*)

LogInfo(**args*, *condition=True*, ***kwargs*)

LogNormal(**args*, *condition=True*, ***kwargs*)

LogQuiet(**args*, *condition=True*, ***kwargs*)

LogVerbose(**args*, *condition=True*, ***kwargs*)

LogWarning(**args*, *condition=True*, ***kwargs*)

Logger
Return the local logger instance.

PrepareOptions(*writeWarnings=True*)

PrepareSections(*warningWasWritten*, *writeWarnings=True*)

PrepareVersionedSections(*writeWarnings=False*)

RunPostConfigurationTasks()
Virtual method. Overwrite to execute post-configuration tasks.

SectionName
Return the configuration's section name.

State
Return the configuration state.

_Ask(*question*, *default*, *beforeDefault=''*, *afterDefault=''*, *indent=1*)

_AskInstalled(*question*)
Ask a Yes/No/Pass question.

_AskYes_NoPass(*question*, *indent=1*)
Ask a yes/NO/pass question.

_Ask_YesNoPass(*question*, *indent=1*)
Ask a YES/no/pass question.

_Configuration__CheckVivadoVersion(*binPath*, *version*)

_ConfigureBinaryDirectory()
Updates section with value from `_template` and returns directory as `Path` object.

_ConfigureEdition(*editions*, *defaultEdition*)

_ConfigureInstallationDirectory()
Asks for installation directory and updates section. Checks if entered directory exists and returns Path object. If no installation directory was configured before, then _GetDefaultInstallationDir is called.

_ConfigureVersion()
If no version was configured before, then _GetDefaultVersion is called. Asks for version and updates section. Returns version as string.

_GetDefaultEdition()
Returns unresolved default edition (str) from template.

Overwrite this method in a sub-class for automatic search of editions.

_GetDefaultInstallationDirectory()
Return unresolved default installation directory (str) from template.

Overwrite function in sub-class for automatic search of installation directory.

_GetDefaultOptionValue(*optionName*)

_GetDefaultVersion()
Returns unresolved default version (str) from template.

Overwrite this method in a sub-class for automatic search of version.

_PrintAvailableEditions(*editions*, *selectedEdition*)
Print all available editions and return the selected index.

_TestDefaultInstallPath(*defaults*)
Helper function for automatic search of installation directory.

_TryLog(**args*, *condition=True*, ***kwargs*)

class ToolChain.Xilinx.Vivado.**ToolMixIn**(*platform*, *dryrun*, *binaryDirectoryPath*, *version*, *logger=None*)

Inheritance

Members

class ToolChain.Xilinx.Vivado.**Vivado**(*platform*, *dryrun*, *binaryDirectoryPath*, *version*, *logger=None*)

Inheritance

Members

PreparseEnvironment(*installationDirectory*)

GetElaborator()

GetSimulator()

GetSynthesizer()

class ToolChain.Xilinx.Vivado.**XElab**(*toolchain: ToolChain.ToolMixIn*)

Inheritance

Members

class Executable

_value = None

```
class FlagRangeCheck

    _name = 'rangecheck'
    _value = None
class SwitchMultiThreading

    _name = 'mt'
    _value = None
class SwitchVerbose

    _name = 'verbose'
    _value = None
class SwitchDebug

    _name = 'debug'
    _value = None
class SwitchOptimization

    _pattern = '--{0}{1}'
    _name = 'O'
    _value = None
class SwitchTimeResolution

    _name = 'timeprecision_vhdl'
    _value = None
class SwitchProjectFile

    _name = 'prj'
    _value = None
class SwitchLogFile

    _name = 'log'
    _value = None
class SwitchSnapshot

    _name = 's'
    _value = None
class ArgTopLevel

    _value = None
Parameters = [<class 'ToolChain.Xilinx.Vivado.XElab.Executable'>, <class 'ToolChain
Link()
```

GetReader()

HasErrors
True if errors or fatals errors were found while processing the output stream.

HasWarnings
True if errors or fatals errors were found while processing the output stream.

Log(*entry*, *condition=True*)
Write an entry to the local logger.

LogDebug(**args*, *condition=True*, ***kwargs*)

LogDryRun(**args*, *condition=True*, ***kwargs*)

LogError(**args*, *condition=True*, ***kwargs*)

LogFatal(**args*, *condition=True*, ***kwargs*)

LogInfo(**args*, *condition=True*, ***kwargs*)

LogNormal(**args*, *condition=True*, ***kwargs*)

LogQuiet(**args*, *condition=True*, ***kwargs*)

LogVerbose(**args*, *condition=True*, ***kwargs*)

LogWarning(**args*, *condition=True*, ***kwargs*)

Logger
Return the local logger instance.

Path

ReadUntilBoundary(*indent=0*)

Send(*line*, *end='\n'*)

SendBoundary()

StartProcess(*parameterList*)

Terminate()

_POC_BOUNDARY = '====== POC BOUNDARY ======'

_TryLog(**args*, *condition=True*, ***kwargs*)

class ToolChain.Xilinx.Vivado.**XSim**(*toolchain: ToolChain.ToolMixIn*)

Inheritance

Members

class Executable

_value = None

class SwitchLogFile

_name = '-log'

_value = None

class FlagGuiMode

_name = '-gui'

```
        _value = None
    class SwitchTclBatchFile

        _name = '-tclbatch'
        _value = None
    class SwitchWaveformFile

        _name = '-view'
        _value = None
    class SwitchSnapshot

        _value = None
    Parameters = [<class 'ToolChain.Xilinx.Vivado.XSim.Executable'>, <class 'ToolChain.X
```

Simulate()

GetReader()

HasErrors
: True if errors or fatals errors were found while processing the output stream.

HasWarnings
: True if errors or fatals errors were found while processing the output stream.

Log(*entry*, *condition=True*)
: Write an entry to the local logger.

LogDebug(**args*, *condition=True*, ***kwargs*)

LogDryRun(**args*, *condition=True*, ***kwargs*)

LogError(**args*, *condition=True*, ***kwargs*)

LogFatal(**args*, *condition=True*, ***kwargs*)

LogInfo(**args*, *condition=True*, ***kwargs*)

LogNormal(**args*, *condition=True*, ***kwargs*)

LogQuiet(**args*, *condition=True*, ***kwargs*)

LogVerbose(**args*, *condition=True*, ***kwargs*)

LogWarning(**args*, *condition=True*, ***kwargs*)

Logger
: Return the local logger instance.

Path

ReadUntilBoundary(*indent=0*)

Send(*line*, *end='\n'*)

SendBoundary()

StartProcess(*parameterList*)

Terminate()

_POC_BOUNDARY = '====== POC BOUNDARY ======'

_TryLog(**args*, *condition=True*, ***kwargs*)

class ToolChain.Xilinx.Vivado.**Synth**(*toolchain: ToolChain.ToolMixIn*)

Inheritance

Members

class Executable

    _value = None

class SwitchLogFile

    _name = 'log'

    _value = None

class SwitchSourceFile

    _name = 'source'

    _value = None

class SwitchMode

    _name = 'mode'

    _value = 'batch'

Parameters = [<class 'ToolChain.Xilinx.Vivado.Synth.Executable'>, <class 'ToolChain

Compile()

GetReader()

HasErrors
    True if errors or fatals errors were found while processing the output stream.

HasWarnings
    True if errors or fatals errors were found while processing the output stream.

Log(*entry*, *condition=True*)
    Write an entry to the local logger.

LogDebug(**args*, *condition=True*, ***kwargs*)

LogDryRun(**args*, *condition=True*, ***kwargs*)

LogError(**args*, *condition=True*, ***kwargs*)

LogFatal(**args*, *condition=True*, ***kwargs*)

LogInfo(**args*, *condition=True*, ***kwargs*)

LogNormal(**args*, *condition=True*, ***kwargs*)

LogQuiet(**args*, *condition=True*, ***kwargs*)

LogVerbose(**args*, *condition=True*, ***kwargs*)

LogWarning(**args*, *condition=True*, ***kwargs*)

Logger
    Return the local logger instance.

Path

ReadUntilBoundary(*indent=0*)

Send(*line*, *end='\n'*)

SendBoundary()

StartProcess(*parameterList*)

Terminate()

_POC_BOUNDARY = '====== POC BOUNDARY ======'

_TryLog(**args*, *condition=True*, ***kwargs*)

class ToolChain.Xilinx.Vivado.**VivadoProject**(*name*)

Inheritance

Members

AddExternalVHDLLibraries(*library*)

AddFile(*file*, *fileSet=None*)

AddFileSet(*fileSet*)

AddSourceFile(*file*, *fileSet=None*)

Board

CreateFileSet(*name*, *setDefault=True*)

DefaultFileSet

Device

Environment

ExternalVHDLLibraries

ExtractVHDLLibrariesFromVHDLSourceFiles()

FileSets

Files(*fileType=<FileTypes(Text|ProjectFile|FileListFile|RulesFile|SourceFile|VHDLSourceFile|VerilogSourceFile|Python*
bits=0xFFFF>, *fileSet=None*)

GetVariables()

Name

RootDirectory

Tool

ToolChain

VHDLLibraries

VHDLVersion

pprint(*indent=0*)

class ToolChain.Xilinx.Vivado.**VivadoProjectFile**(*file*)

Inheritance

Members

FileName

FileSet

FileType

Open()

Path

Project

ReadFile()

_FileType = <FileTypes.ProjectFile bits=0x0002 data=UNDEFINED>

_ReadContent()

class ToolChain.Xilinx.Vivado.**XilinxDesignConstraintFile**(*file*, *project=None*, *fileSet=None*)

Inheritance

Members

_FileType = <FileTypes.XdcConstraintFile bits=0x0800 data=UNDEFINED>

FileName

FileSet

FileType

Open()

Path

Project

ReadFile()

_ReadContent()

Functions

ToolChain.Xilinx.Vivado.**ElaborationFilter**(*gen*)

ToolChain.Xilinx.Vivado.**SimulatorFilter**(*gen*)

ToolChain.Xilinx.Vivado.**CompilerFilter**(*gen*)

Exceptions

- *XilinxException*: Base class for all tool specific exceptions

Classes

- *Configuration*: Configuration routines for Xilinx as a vendor.
- *XilinxProjectExportMixIn*: Undocumented.

exception ToolChain.Xilinx.**XilinxException**(*message=''*)

Inheritance

Members

__init__(*message=''*)
Exception initializer

Parameters **message** (*str*) – The exception message.

__str__()
Returns the exception's message text.

args

class ToolChain.Xilinx.**Configuration**(*host: Base.IHost*)
Configuration routines for Xilinx as a vendor.

This configuration provides a common installation directory setup for all Xilinx tools installed on a system.

Inheritance

Members

_vendor = 'Xilinx'
The name of the tools vendor.

_section = 'INSTALL.Xilinx'
The name of the configuration section. Pattern: INSTALL.Vendor.ToolName.

_template = {'Linux': {'INSTALL.Xilinx': {'InstallationDirectory': '/opt/Xilinx'
The template for the configuration sections represented as nested dictionaries.

_GetDefaultInstallationDirectory()
Return unresolved default installation directory (str) from template.

Overwrite function in sub-class for automatic search of installation directory.

CheckDependency()
Check if all vendor or tool dependencies are fulfilled to configure this tool.

ClearSection(*writeWarnings=False*)
Clear the configuration section associated to this Configuration class.

ConfigureForAll()
Start a generic (platform independent) vendor configuration procedure.

This method configures a vendor path. Overwrite this method to implement a vendor specific configuration routine for a vendor Configuration class.

ConfigureForDarwin()
Start the configuration procedure for Darwin.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Darwin specific configuration routine.

ConfigureForLinux()
Start the configuration procedure for Linux.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Linux specific configuration routine.

ConfigureForWindows()
Start the configuration procedure for Windows.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Windows specific configuration routine.

classmethod GetSections(*platform*)
Return all section names for this configuration.

Host
Return the hosting object.

IsConfigured()
Return true if the configurations section is configured

IsSupportedPlatform()
Return true if the given platform is supported by this configuration routine.

Log(*entry*, *condition=True*)
Write an entry to the local logger.

LogDebug(**args*, *condition=True*, ***kwargs*)

LogDryRun(**args*, *condition=True*, ***kwargs*)

LogError(**args*, *condition=True*, ***kwargs*)

LogFatal(**args*, *condition=True*, ***kwargs*)

LogInfo(**args*, *condition=True*, ***kwargs*)

LogNormal(**args*, *condition=True*, ***kwargs*)

LogQuiet(**args*, *condition=True*, ***kwargs*)

LogVerbose(**args*, *condition=True*, ***kwargs*)

LogWarning(**args*, *condition=True*, ***kwargs*)

Logger
Return the local logger instance.

PrepareOptions(*writeWarnings=True*)

PrepareSections(*warningWasWritten*, *writeWarnings=True*)

RunPostConfigurationTasks()
Virtual method. Overwrite to execute post-configuration tasks.

SectionName
Return the configuration's section name.

State
Return the configuration state.

_Ask(*question*, *default*, *beforeDefault=''*, *afterDefault=''*, *indent=1*)

_AskInstalled(*question*)
Ask a Yes/No/Pass question.

_AskYes_NoPass(*question*, *indent=1*)
Ask a yes/NO/pass question.

_Ask_YesNoPass(*question*, *indent=1*)
Ask a YES/no/pass question.

_ConfigureInstallationDirectory()
Asks for installation directory and updates section. Checks if entered directory exists and returns Path object. If no installation directory was configured before, then _GetDefaultInstallationDir is called.

_GetDefaultOptionValue(*optionName*)

_PrintAvailableEditions(*editions*, *selectedEdition*)
Print all available editions and return the selected index.

_TestDefaultInstallPath(*defaults*)
Helper function for automatic search of installation directory.

_TryLog(**args*, *condition=True*, ***kwargs*)

_multiVersionSupport = False

class ToolChain.Xilinx.**XilinxProjectExportMixIn**

Inheritance

Members

_GenerateXilinxProjectFileContent(*tool*, *vhdlVersion=93*)

_WriteXilinxProjectFile(*projectFilePath*, *tool*, *vhdlVersion=93*)

Exceptions

- *ToolChainException*: Base class for all tool specific exceptions
- *ConfigurationException*: `ConfigurationException` is raise while running configuration or database
- *SkipConfigurationException*: `SkipConfigurationException` is a *ConfigurationException*,

Classes

- *ConfigurationState*: Describes the configuration state of a tool or vendor.
- *ChangeState*: Describes if a configuration was changed.
- *ToolMixIn*: Undocumented.
- *AskMixIn*: Undocumented.
- *Configuration*: Base class for all Configuration classes.
- *VendorConfiguration*: Base class for all vendor Configuration classes.
- *ToolConfiguration*: Base class for all tool Configuration classes.
- *EditionDescription*: EditionDescription(Name, Section)
- *Edition*: An enumeration.
- *ToolSelector*: Base class for all Selector classes.
- *Configurator*: A instance of this class controls the interactive configuration process.

exception ToolChain.**ToolChainException**(*message=''*)
Base class for all tool specific exceptions

Inheritance

Members

__init__(*message=''*)
Exception initializer

Parameters **message** (*str*) – The exception message.

__str__()
Returns the exception's message text.

args

exception ToolChain.**ConfigurationException**(*message=''*)
`ConfigurationException` is raise while running configuration or database tasks in PoC

Inheritance

Members

__init__(*message=''*)
Exception initializer

Parameters **message** (*str*) – The exception message.

__str__()
Returns the exception's message text.

args

exception ToolChain.**SkipConfigurationException**(*message=''*)
SkipConfigurationException is a *ConfigurationException*, which can be skipped.

Inheritance

Members

__init__(*message=''*)
Exception initializer

Parameters **message** (*str*) – The exception message.

__str__()
Returns the exception's message text.

args

class ToolChain.**ConfigurationState**
Describes the configuration state of a tool or vendor.

Inheritance

Members

Unconfigured = 0

Configured = 1

class ToolChain.**ChangeState**
Describes if a configuration was changed.

Inheritance

Members

Unchanged = 0

Changed = 1

class ToolChain.**ToolMixIn**(*platform*, *dryrun*, *binaryDirectoryPath*, *version*, *logger=None*)

Inheritance

Members

class ToolChain.**AskMixIn**

Inheritance

Members

_Ask(*question*, *default*, *beforeDefault=”*, *afterDefault=”*, *indent=1*)

_Ask_YesNoPass(*question*, *indent=1*)
Ask a YES/no/pass question.

_AskYes_NoPass(*question*, *indent=1*)
Ask a yes/NO/pass question.

_PrintAvailableEditions(*editions*, *selectedEdition*)
Print all available editions and return the selected index.

class ToolChain.**Configuration**(*host: Base.IHost*)
Base class for all Configuration classes.

Inheritance

Members

_vendor = 'Unknown'
The name of the tools vendor.

_section = 'INSTALL.Name'
The name of the configuration section. Pattern: `INSTALL.Tool`.

_multiVersionSupport = False
True if a tool supports multiple versions installed on the same system.

_template = {'ALL': {'INSTALL.Name': {}}, 'Darwin': {'INSTALL.Name': {}}, 'Linux
The template for the configuration sections represented as nested dictionaries.

Host
Return the hosting object.

State
Return the configuration state.

SectionName
Return the configuration’s section name.

IsSupportedPlatform()
Return true if the given platform is supported by this configuration routine.

IsConfigured()
Return true if the configurations section is configured

CheckDependency()
Check if all vendor or tool dependencies are fulfilled to configure this tool.

classmethod GetSections(*platform*)
Return all section names for this configuration.

PrepareSections(*warningWasWritten*, *writeWarnings=True*)

ClearSection(*writeWarnings=False*)
Clear the configuration section associated to this Configuration class.

PrepareOptions(*writeWarnings=True*)

ConfigureForDarwin()
Start the configuration procedure for Darwin.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Darwin specific configuration routine.

ConfigureForLinux()
Start the configuration procedure for Linux.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Linux specific configuration routine.

ConfigureForWindows()
Start the configuration procedure for Windows.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Windows specific configuration routine.

ConfigureForAll()
Start a generic (platform independent) configuration procedure.

Overwrite this method to implement a generic configuration routine for a (tool) Configuration class.

_AskInstalled(*question*)
Ask a Yes/No/Pass question.

_ConfigureInstallationDirectory()
Asks for installation directory and updates section. Checks if entered directory exists and returns Path object. If no installation directory was configured before, then _GetDefaultInstallationDir is called.

_GetDefaultInstallationDirectory()
Return unresolved default installation directory (str) from template.

Overwrite function in sub-class for automatic search of installation directory.

_GetDefaultOptionValue(*optionName*)

_TestDefaultInstallPath(*defaults*)
Helper function for automatic search of installation directory.

RunPostConfigurationTasks()
Virtual method. Overwrite to execute post-configuration tasks.

Log(*entry*, *condition=True*)
Write an entry to the local logger.

LogDebug(**args*, *condition=True*, ***kwargs*)

LogDryRun(**args*, *condition=True*, ***kwargs*)

LogError(**args*, *condition=True*, ***kwargs*)

LogFatal(**args*, *condition=True*, ***kwargs*)

LogInfo(**args*, *condition=True*, ***kwargs*)

LogNormal(**args*, *condition=True*, ***kwargs*)

LogQuiet(**args*, *condition=True*, ***kwargs*)

LogVerbose(**args*, *condition=True*, ***kwargs*)

LogWarning(**args*, *condition=True*, ***kwargs*)

Logger
Return the local logger instance.

_Ask(*question*, *default*, *beforeDefault=''*, *afterDefault=''*, *indent=1*)

_AskYes_NoPass(*question*, *indent=1*)
Ask a yes/NO/pass question.

_Ask_YesNoPass(*question*, *indent=1*)
Ask a YES/no/pass question.

_PrintAvailableEditions(*editions*, *selectedEdition*)
Print all available editions and return the selected index.

_TryLog(**args*, *condition=True*, ***kwargs*)

class ToolChain.**VendorConfiguration**(*host: Base.IHost*)
Base class for all vendor Configuration classes.

Inheritance

Members

_section = 'INSTALL.Vendor.Tool'
The name of the configuration section. Pattern: INSTALL.Vendor.

_template = {'Darwin': {'INSTALL.Vendor.Tool': {'InstallationDirectory': '/opt/Ve
The template for the configuration section represented as nested dictionaries.

IsConfigured()
Return true if the vendor represented by this Configuration class is configured in PoC.

Inherited method *IsConfigured()* from class *Configuration*.

ConfigureForAll()
Start a generic (platform independent) vendor configuration procedure.

This method configures a vendor path. Overwrite this method to implement a vendor specific configuration routine for a vendor Configuration class.

CheckDependency()
Check if all vendor or tool dependencies are fulfilled to configure this tool.

ClearSection(*writeWarnings=False*)
Clear the configuration section associated to this Configuration class.

ConfigureForDarwin()
Start the configuration procedure for Darwin.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Darwin specific configuration routine.

ConfigureForLinux()
Start the configuration procedure for Linux.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Linux specific configuration routine.

ConfigureForWindows()
Start the configuration procedure for Windows.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Windows specific configuration routine.

classmethod GetSections(*platform*)
Return all section names for this configuration.

Host
Return the hosting object.

IsSupportedPlatform()
Return true if the given platform is supported by this configuration routine.

Log(*entry*, *condition=True*)
Write an entry to the local logger.

LogDebug(**args*, *condition=True*, ***kwargs*)

LogDryRun(**args*, *condition=True*, ***kwargs*)

LogError(**args*, *condition=True*, ***kwargs*)

LogFatal(**args*, *condition=True*, ***kwargs*)

LogInfo(**args*, *condition=True*, ***kwargs*)

LogNormal(**args*, *condition=True*, ***kwargs*)

LogQuiet(**args*, *condition=True*, ***kwargs*)

LogVerbose(**args*, *condition=True*, ***kwargs*)

LogWarning(**args*, *condition=True*, ***kwargs*)

Logger
Return the local logger instance.

PrepareOptions(*writeWarnings=True*)

PrepareSections(*warningWasWritten*, *writeWarnings=True*)

RunPostConfigurationTasks()
Virtual method. Overwrite to execute post-configuration tasks.

SectionName
Return the configuration's section name.

State
Return the configuration state.

_Ask(*question*, *default*, *beforeDefault=''*, *afterDefault=''*, *indent=1*)

_AskInstalled(*question*)
Ask a Yes/No/Pass question.

_AskYes_NoPass(*question*, *indent=1*)
Ask a yes/NO/pass question.

_Ask_YesNoPass(*question*, *indent=1*)
Ask a YES/no/pass question.

_ConfigureInstallationDirectory()
Asks for installation directory and updates section. Checks if entered directory exists and returns Path object. If no installation directory was configured before, then _GetDefaultInstallationDir is called.

_GetDefaultInstallationDirectory()
Return unresolved default installation directory (str) from template.

Overwrite function in sub-class for automatic search of installation directory.

_GetDefaultOptionValue(*optionName*)

_PrintAvailableEditions(*editions*, *selectedEdition*)
Print all available editions and return the selected index.

_TestDefaultInstallPath(*defaults*)
Helper function for automatic search of installation directory.

_TryLog(**args*, *condition=True*, ***kwargs*)

_multiVersionSupport = False

_vendor = 'Unknown'

class ToolChain.**ToolConfiguration**(*host: Base.IHost*)
Base class for all tool Configuration classes.

Inheritance

Members

_section = 'INSTALL.Vendor.Tool'
The name of the configuration section. Pattern: `INSTALL.Vendor.ToolName`.

_toolName = 'Tool'
The name of the tool.

_template = {'ALL': {'INSTALL.Vendor.Tool': {'Version': '1.0'}}, 'Darwin': {'INST
The template for the configuration section represented as nested dictionaries.

IsConfigured()
Return true if the tool represented by this Configuration class is configured in PoC.

Inherited method *IsConfigured()* from class *Configuration*.

_ConfigureVersion()
If no version was configured before, then _GetDefaultVersion is called. Asks for version and updates section. Returns version as string.

_GetDefaultVersion()
Returns unresolved default version (str) from template.

Overwrite this method in a sub-class for automatic search of version.

_ConfigureEdition(*editions*, *defaultEdition*)

_GetDefaultEdition()
Returns unresolved default edition (str) from template.

Overwrite this method in a sub-class for automatic search of editions.

_ConfigureBinaryDirectory()
Updates section with value from *_template* and returns directory as `Path` object.

PrepareVersionedSections(*writeWarnings=False*)

CheckDependency()
Check if all vendor or tool dependencies are fulfilled to configure this tool.

ClearSection(*writeWarnings=False*)
Clear the configuration section associated to this Configuration class.

ConfigureForAll()
Start a generic (platform independent) configuration procedure.

Overwrite this method to implement a generic configuration routine for a (tool) Configuration class.

ConfigureForDarwin()
Start the configuration procedure for Darwin.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Darwin specific configuration routine.

ConfigureForLinux()
Start the configuration procedure for Linux.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Linux specific configuration routine.

ConfigureForWindows()
Start the configuration procedure for Windows.

This method is a wrapper for *ConfigureForAll()*. Overwrite this method to implement a Windows specific configuration routine.

classmethod GetSections(*platform*)
Return all section names for this configuration.

Host
Return the hosting object.

IsSupportedPlatform()
Return true if the given platform is supported by this configuration routine.

Log(*entry*, *condition=True*)
Write an entry to the local logger.

LogDebug(**args*, *condition=True*, ***kwargs*)

LogDryRun(**args*, *condition=True*, ***kwargs*)

LogError(**args*, *condition=True*, ***kwargs*)

LogFatal(**args*, *condition=True*, ***kwargs*)

LogInfo(**args*, *condition=True*, ***kwargs*)

LogNormal(**args*, *condition=True*, ***kwargs*)

LogQuiet(**args*, *condition=True*, ***kwargs*)

LogVerbose(**args*, *condition=True*, ***kwargs*)

LogWarning(**args*, *condition=True*, ***kwargs*)

Logger
Return the local logger instance.

PrepareOptions(*writeWarnings=True*)

PrepareSections(*warningWasWritten*, *writeWarnings=True*)

RunPostConfigurationTasks()
Virtual method. Overwrite to execute post-configuration tasks.

SectionName
Return the configuration's section name.

State
Return the configuration state.

_Ask(*question*, *default*, *beforeDefault=''*, *afterDefault=''*, *indent=1*)

_AskInstalled(*question*)
Ask a Yes/No/Pass question.

_AskYes_NoPass(*question*, *indent=1*)
Ask a yes/NO/pass question.

_Ask_YesNoPass(*question*, *indent=1*)
Ask a YES/no/pass question.

_ConfigureInstallationDirectory()
Asks for installation directory and updates section. Checks if entered directory exists and returns Path object. If no installation directory was configured before, then _GetDefaultInstallationDir is called.

_GetDefaultInstallationDirectory()
Return unresolved default installation directory (str) from template.

Overwrite function in sub-class for automatic search of installation directory.

_GetDefaultOptionValue(*optionName*)

_PrintAvailableEditions(*editions*, *selectedEdition*)
Print all available editions and return the selected index.

_TestDefaultInstallPath(*defaults*)
Helper function for automatic search of installation directory.

_TryLog(**args*, *condition=True*, ***kwargs*)

_multiVersionSupport = False

_vendor = 'Unknown'

class ToolChain.**EditionDescription**(*Name*, *Section*)

Inheritance

Members

Name
Alias for field number 0

Section
Alias for field number 1

_asdict()
Return a new OrderedDict which maps field names to their values.

_fields = ('Name', 'Section')

classmethod _make(*iterable*, *new=<built-in method __new__ of type object>*, *len=<built-in function len>*)
Make a new EditionDescription object from a sequence or iterable

_replace(***kwds*)
Return a new EditionDescription object replacing specified fields with new values

_source = "from builtins import property as _property, tuple as _tuple\nfrom operato

count(*value*) → integer – return number of occurrences of value

index(*value*[, *start*[, *stop*]]) → integer – return first index of value.
Raises ValueError if the value is not present.

class ToolChain.**Edition**(*name*, *section*)
An enumeration.

Inheritance

Members

class ToolChain.**ToolSelector**(*host: Base.IHost*)
Base class for all Selector classes.

Inheritance

Members

_toolName = ''

ToolName

_GetConfiguredEditions(*editions*)
Return all configured editions.

_AskSelection(*editions*, *defaultEdition*)

Log (*entry*, *condition=True*)
Write an entry to the local logger.

LogDebug (**args*, *condition=True*, ***kwargs*)

LogDryRun (**args*, *condition=True*, ***kwargs*)

LogError (**args*, *condition=True*, ***kwargs*)

LogFatal (**args*, *condition=True*, ***kwargs*)

LogInfo (**args*, *condition=True*, ***kwargs*)

LogNormal (**args*, *condition=True*, ***kwargs*)

LogQuiet (**args*, *condition=True*, ***kwargs*)

LogVerbose (**args*, *condition=True*, ***kwargs*)

LogWarning (**args*, *condition=True*, ***kwargs*)

Logger
Return the local logger instance.

_Ask (*question*, *default*, *beforeDefault=''*, *afterDefault=''*, *indent=1*)

_AskYes_NoPass (*question*, *indent=1*)
Ask a yes/NO/pass question.

_Ask_YesNoPass (*question*, *indent=1*)
Ask a YES/no/pass question.

_PrintAvailableEditions (*editions*, *selectedEdition*)
Print all available editions and return the selected index.

_TryLog (**args*, *condition=True*, ***kwargs*)

class ToolChain.**Configurator** (*host: Base.IHost*)
A instance of this class controls the interactive configuration process.

Inheritance

Members

ConfigureAll ()
Select all tool chains for configuration

ConfigureTool (*toolChain*)
Select tool chains for configuration.

InitializeConfiguration ()
Initialize PoC's configuration with empty sections.

The list of sections is gathered from all enabled configurators' `_template` fields.

UpdateConfiguration ()
Update an existing configuration e.g. after a PoC update.

_ConfigureTools (*configurators*)
Run the configuration routines for a list of configurators

_ConfigurationLoop (*configurator*)
Retry to configure a vendor or tool until it succeeds or the user presses `P` to pass a configuration step.

A **:py:exec:'KeyboardInterrupt'** should be handled in a calling method.

ConfigureDefaultTools ()

_ConfigureDefaultTools ()

_WriteConfigurationHeader()
Write a header containing general information about the configuration and list allowed input values for yes/no/pass questions.

_AskConfigureDefaultTools()
Ask if default tools should be configured now.

Relocated()

Log(*entry*, *condition=True*)
Write an entry to the local logger.

LogDebug(**args*, *condition=True*, ***kwargs*)

LogDryRun(**args*, *condition=True*, ***kwargs*)

LogError(**args*, *condition=True*, ***kwargs*)

LogFatal(**args*, *condition=True*, ***kwargs*)

LogInfo(**args*, *condition=True*, ***kwargs*)

LogNormal(**args*, *condition=True*, ***kwargs*)

LogQuiet(**args*, *condition=True*, ***kwargs*)

LogVerbose(**args*, *condition=True*, ***kwargs*)

LogWarning(**args*, *condition=True*, ***kwargs*)

Logger
Return the local logger instance.

_Ask(*question*, *default*, *beforeDefault=''*, *afterDefault=''*, *indent=1*)

_AskYes_NoPass(*question*, *indent=1*)
Ask a yes/NO/pass question.

_Ask_YesNoPass(*question*, *indent=1*)
Ask a YES/no/pass question.

_PrintAvailableEditions(*editions*, *selectedEdition*)
Print all available editions and return the selected index.

_TryLog(**args*, *condition=True*, ***kwargs*)

14.8 lib

Submodules

14.8.1 lib.CodeDOM

Classes

- *CodeDOMMeta*: type(object_or_name, bases, dict)
- *CodeDOMObject*: Undocumented.
- *Expression*: Undocumented.
- *UnaryExpression*: Undocumented.
- *NotExpression*: Undocumented.
- *BinaryExpression*: Undocumented.
- *LogicalExpression*: Undocumented.
- *CompareExpression*: Undocumented.

- *EqualExpression*: Undocumented.
- *UnequalExpression*: Undocumented.
- *LessThanExpression*: Undocumented.
- *LessThanEqualExpression*: Undocumented.
- *GreaterThanExpression*: Undocumented.
- *GreaterThanEqualExpression*: Undocumented.
- *AndExpression*: Undocumented.
- *OrExpression*: Undocumented.
- *XorExpression*: Undocumented.
- *InExpression*: Undocumented.
- *NotInExpression*: Undocumented.
- *Function*: Undocumented.
- *ListElement*: Undocumented.
- *Literal*: Undocumented.
- *StringLiteral*: Undocumented.
- *IntegerLiteral*: Undocumented.
- *Identifier*: Undocumented.
- *Statement*: Undocumented.
- *BlockStatement*: Undocumented.
- *ConditionalBlockStatement*: Undocumented.
- *EmptyLine*: Undocumented.
- *CommentLine*: Undocumented.
- *BlockedStatement*: Undocumented.
- *ExpressionChoice*: Undocumented.

class lib.CodeDOM.**CodeDOMMeta**

Inheritance

Members

parse()

static GetChoiceParser()

static GetRepeatParser(*generator*)

mro() → list
return a type's method resolution order

class lib.CodeDOM.**CodeDOMObject**

Inheritance

Members

classmethod Parse(*string*, *printChar*)

class lib.CodeDOM.**Expression**

Inheritance

Members

classmethod Parse(*string*, *printChar*)

class lib.CodeDOM.**UnaryExpression**(*child*)

Inheritance

Members

Child

classmethod Parse(*string*, *printChar*)

class lib.CodeDOM.**NotExpression**(*child*)

Inheritance

Members

classmethod GetParser()

Child

classmethod Parse(*string*, *printChar*)

class lib.CodeDOM.**BinaryExpression**(*leftChild*, *rightChild*)

Inheritance

Members

LeftChild

RightChild

classmethod GetParser()

classmethod Parse(*string*, *printChar*)

class lib.CodeDOM.**LogicalExpression**(*leftChild*, *rightChild*)

Inheritance

Members

classmethod GetParser()

LeftChild

classmethod Parse(*string*, *printChar*)

RightChild

class lib.CodeDOM.**CompareExpression**(*leftChild*, *rightChild*)

Inheritance

Members

classmethod GetParser()

LeftChild

classmethod Parse(*string*, *printChar*)

RightChild

class lib.CodeDOM.**EqualExpression**(*leftChild*, *rightChild*)

Inheritance

Members

classmethod GetParser()

LeftChild

classmethod Parse(*string*, *printChar*)

RightChild

class lib.CodeDOM.**UnequalExpression**(*leftChild*, *rightChild*)

Inheritance

Members

classmethod GetParser()

LeftChild

classmethod Parse(*string*, *printChar*)

RightChild

class lib.CodeDOM.**LessThanExpression**(*leftChild*, *rightChild*)

Inheritance

Members

classmethod GetParser()

LeftChild

classmethod Parse(*string*, *printChar*)

RightChild

class lib.CodeDOM.**LessThanEqualExpression**(*leftChild*, *rightChild*)

Inheritance

Members

classmethod GetParser()

LeftChild

classmethod Parse(*string*, *printChar*)

RightChild

class lib.CodeDOM.**GreaterThanExpression**(*leftChild*, *rightChild*)

Inheritance

Members

classmethod GetParser()

LeftChild

classmethod Parse(*string*, *printChar*)

RightChild

class lib.CodeDOM.**GreaterThanEqualExpression**(*leftChild*, *rightChild*)

Inheritance

Members

classmethod GetParser()

LeftChild

classmethod Parse(*string*, *printChar*)

RightChild

class lib.CodeDOM.**AndExpression**(*leftChild*, *rightChild*)

Inheritance

Members

classmethod GetParser()

LeftChild

classmethod Parse(*string*, *printChar*)

RightChild

class lib.CodeDOM.**OrExpression**(*leftChild*, *rightChild*)

Inheritance

Members

classmethod GetParser()

LeftChild

classmethod Parse(*string*, *printChar*)

RightChild

class lib.CodeDOM.**XorExpression**(*leftChild*, *rightChild*)

Inheritance

Members

classmethod GetParser()

LeftChild

classmethod Parse(*string*, *printChar*)

RightChild

class lib.CodeDOM.**InExpression**(*leftChild*, *rightChild*)

Inheritance

Members

classmethod GetParser()

LeftChild

classmethod Parse(*string*, *printChar*)

RightChild

class lib.CodeDOM.**NotInExpression**(*leftChild*, *rightChild*)

Inheritance

Members

classmethod GetParser()

LeftChild

classmethod Parse(*string*, *printChar*)

RightChild

class lib.CodeDOM.**Function**

Inheritance

Members

classmethod Parse(*string*, *printChar*)

class lib.CodeDOM.**ListElement**

Inheritance

Members

classmethod GetParser()

classmethod Parse(*string*, *printChar*)

class lib.CodeDOM.**Literal**

Inheritance

Members

classmethod Parse(*string*, *printChar*)

class lib.CodeDOM.**StringLiteral**(*value*)

Inheritance

Members

Value

classmethod GetParser()

classmethod Parse(*string*, *printChar*)

class lib.CodeDOM.**IntegerLiteral**(*value*)

Inheritance

Members

Value

classmethod GetParser()

classmethod Parse(*string*, *printChar*)

class lib.CodeDOM.**Identifier**(*name*)

Inheritance

Members

Name

classmethod GetParser()

classmethod Parse(*string*, *printChar*)

class lib.CodeDOM.**Statement**(*commentText=”*)

Inheritance

Members

CommentText

classmethod Parse(*string*, *printChar*)

class lib.CodeDOM.**BlockStatement**(*commentText=”*)

Inheritance

Members

AddStatement(*stmt*)

Statements

CommentText

classmethod Parse(*string*, *printChar*)

class lib.CodeDOM.**ConditionalBlockStatement**(*expression*, *commentText=”*)

Inheritance

Members

Expression

AddStatement(*stmt*)

CommentText

classmethod Parse(*string*, *printChar*)

Statements

class lib.CodeDOM.**EmptyLine**

Inheritance

Members

classmethod GetParser()

classmethod Parse(*string*, *printChar*)

class lib.CodeDOM.**CommentLine**(*commentText*)

Inheritance

Members

Text

classmethod GetParser()

classmethod Parse(*string*, *printChar*)

class lib.CodeDOM.**BlockedStatement**

Inheritance

Members

_allowedStatements = []

classmethod AddChoice(*value*)

classmethod GetParser()

classmethod Parse(*string*, *printChar*)

class lib.CodeDOM.**ExpressionChoice**

Inheritance

Members

_allowedExpressions = []

classmethod AddChoice(*value*)

classmethod GetParser()

classmethod Parse(*string*, *printChar*)

14.8.2 lib.Decorators

Classes

- *MethodAlias*: MethodAlias creates a local method, which is an alias to another method
- *ILazyLoadable*: Undocumented.

- *LazyLoadTrigger*: Undocumented.
- *CachedReadOnlyProperty*: Undocumented.

class lib.Decorators.**MethodAlias**(*method*)
MethodAlias creates a local method, which is an alias to another method local or inherited method.

Inheritance

Members

__init__(*method*)
Initialize self. See help(type(self)) for accurate signature.

__call__(*func*)
Call self as a function.

class lib.Decorators.**ILazyLoadable**

Inheritance

Members

_LazyLoadable_Load()

LazyLoadable_IsLoaded

class lib.Decorators.**LazyLoadTrigger**(*func*)

Inheritance

Members

class lib.Decorators.**CachedReadOnlyProperty**(*func*)

Inheritance

Members

14.8.3 lib.ExtendedConfigParser

Classes

- *ExtendedSectionProxy*: A proxy for a single section from a parser.
- *ExtendedInterpolation*: Dummy interpolation that passes the value through with no changes.
- *ExtendedConfigParser*: ConfigParser implementing interpolation.

class lib.ExtendedConfigParser.**ExtendedSectionProxy**(*parser*, *name*)

Inheritance

Members

_MutableMapping__marker = <object object>

_abc_cache = <_weakrefset.WeakSet object>

_abc_negative_cache = <_weakrefset.WeakSet object>

_abc_negative_cache_version = 42

_abc_registry = <_weakrefset.WeakSet object>

_options()

clear() → None. Remove all items from D.

get(*option*, *fallback=None*, *, *raw=False*, *vars=None*, *_impl=None*, ***kwargs*)
Get an option value.

Unless *fallback* is provided, *None* will be returned if the option is not found.

items() → a set-like object providing a view on D's items

keys() → a set-like object providing a view on D's keys

name

parser

pop(*k*[, *d*]) → v, remove specified key and return the corresponding value.
If key is not found, d is returned if given, otherwise KeyError is raised.

popitem() → (k, v), remove and return some (key, value) pair
as a 2-tuple; but raise KeyError if D is empty.

setdefault(*k*[, *d*]) → D.get(k,d), also set D[k]=d if k not in D

update([*E*], ***F*) → None. Update D from mapping/iterable E and F.
If E present and has a .keys() method, does: for k in E: D[k] = E[k] If E present and lacks .keys() method, does: for (k, v) in E: D[k] = v In either case, this is followed by: for k, v in F.items(): D[k] = v

values() → an object providing a view on D's values

class lib.ExtendedConfigParser.**ExtendedInterpolation**

Inheritance

Members

_KEYCRE = re.compile('\\$\\{(?P<ref>[^}]+)\\}')

_KEYCRE2 = re.compile('\\$\\[(?P<ref>[^\\]]+)\\}')

clear_cache()

before_get(*parser*, *section*, *option*, *value*, *defaults*)

before_set(*parser*, *section*, *option*, *value*)

interpolate(*parser*, *section*, *option*, *value*, *_*, *depth=0*)

static GetSpecial(*option*, *path*)

GetValue(*parser*, *section*, *option*, *path*)

GetCached(*section*, *option*)

UpdateCache(*section*, *option*, *value*)

before_read(*parser*, *section*, *option*, *value*)

before_write(*parser*, *section*, *option*, *value*)

class lib.ExtendedConfigParser.**ExtendedConfigParser**(*defaults=None*, *dict_type=<class 'collections.OrderedDict'>*, *allow_no_value=False*, ***, *delimiters=('=', ':')*, *comment_prefixes=('#', ';')*, *inline_comment_prefixes=None*, *strict=True*, *empty_lines_in_values=True*, *default_section='DEFAULT'*, *interpolation=<object object>*, *converters=<object object>*)

Inheritance

Members

_DEFAULT_INTERPOLATION = <lib.ExtendedConfigParser.ExtendedInterpolation object>

BOOLEAN_STATES = {'0': False, '1': True, 'false': False, 'no': False, 'off': Fa

NONSPACECRE = re.compile('\\S')

OPTCRE = re.compile('\n (?P<option>.*?) # very permissive!\n \\s*(?P<vi>=|:)\\s* # a

OPTCRE_NV = re.compile('\n (?P<option>.*?) # very permissive!\n \\s*(?: # any numbe

SECTCRE = re.compile('\n \\[# [\n (?P<header>[^]]+) # very permissive!\n \\] #]\n

_MutableMapping__marker = <object object>

_OPT_NV_TMPL = '\n (?P<option>.*?) # very permissive!\n \\s*(?: # any number of spa

_OPT_TMPL = '\n (?P<option>.*?) # very permissive!\n \\s*(?P<vi>{delim})\\s* # any r

_SECT_TMPL = '\n \\[# [\n (?P<header>[^]]+) # very permissive!\n \\] #]\n '

_abc_cache = <_weakrefset.WeakSet object>

_abc_negative_cache = <_weakrefset.WeakSet object>

_abc_negative_cache_version = 42

_abc_registry = <_weakrefset.WeakSet object>

_convert_to_boolean(*value*)
Return a boolean value translating from other types if necessary.

_get(*section*, *conv*, *option*, ***kwargs*)

_get_conv(*section*, *option*, *conv*, ***, *raw=False*, *vars=None*, *fallback=<object object>*, ***kwargs*)

_handle_error(*exc*, *fpname*, *lineno*, *line*)

_join_multiline_values()

_read(*fp*, *fpname*)
Parse a sectioned configuration file.

Each section in a configuration file contains a header, indicated by a name in square brackets (‘[]’), plus key/value options, indicated by ‘name’ and ‘value’ delimited with a specific substring (‘=’ or ‘:’ by default).

Values can span multiple lines, as long as they are indented deeper than the first line of the value. Depending on the parser’s mode, blank lines may be treated as parts of multiline values or ignored.

Configuration files may include comments, prefixed by specific characters (‘#’ and ‘;’ by default). Comments may appear on their own in an otherwise empty line or may be entered in lines holding values or section names.

_validate_value_types (*, *section=''*, *option=''*, *value=''*)
Raises a TypeError for non-string values.

The only legal non-string value if we allow valueless options is None, so we need to check if the value is a string if: - we do not allow valueless options, or - we allow valueless options but the value is not None

For compatibility reasons this method is not used in classic set() for RawConfigParsers. It is invoked in every case for mapping protocol access and in ConfigParser.set().

_write_section (*fp*, *section_name*, *section_items*, *delimiter*)
Write a single section to the specified ‘fp’.

add_section (*section*)
Create a new section in the configuration. Extends RawConfigParser.add_section by validating if the section name is a string.

clear () → None. Remove all items from D.

converters

defaults ()

get (*section*, *option*, *, *raw=False*, *vars=None*, *fallback=<object object>*)
Get an option value for a given section.

If ‘vars’ is provided, it must be a dictionary. The option is looked up in ‘vars’ (if provided), ‘section’, and in ‘DEFAULTSECT’ in that order. If the key is not found and ‘fallback’ is provided, it is used as a fallback value. ‘None’ can be provided as a ‘fallback’ value.

If interpolation is enabled and the optional argument ‘raw’ is False, all interpolations are expanded in the return values.

Arguments ‘raw’, ‘vars’, and ‘fallback’ are keyword only.

The section DEFAULT is special.

getboolean (*section*, *option*, *, *raw=False*, *vars=None*, *fallback=<object object>*, ***kwargs*)

getfloat (*section*, *option*, *, *raw=False*, *vars=None*, *fallback=<object object>*, ***kwargs*)

getint (*section*, *option*, *, *raw=False*, *vars=None*, *fallback=<object object>*, ***kwargs*)

has_section (*section*)
Indicate whether the named section is present in the configuration.

The DEFAULT section is not acknowledged.

items (*section=<object object>*, *raw=False*, *vars=None*)
Return a list of (name, value) tuples for each option in a section.

All % interpolations are expanded in the return values, based on the defaults passed into the constructor, unless the optional argument ‘raw’ is true. Additional substitutions may be provided using the ‘vars’ argument, which must be a dictionary whose contents overrides any pre-existing defaults.

The section DEFAULT is special.

keys () → a set-like object providing a view on D’s keys

options (*section*)
Return a list of option names for the given section name.

optionxform (*optionstr*)

pop (*k*[, *d*]) → v, remove specified key and return the corresponding value.
If key is not found, d is returned if given, otherwise KeyError is raised.

popitem()
Remove a section from the parser and return it as a (section_name, section_proxy) tuple. If no section is present, raise KeyError.

The section DEFAULT is never returned because it cannot be removed.

read(*filenames*, *encoding=None*)
Read and parse a filename or a list of filenames.

Files that cannot be opened are silently ignored; this is designed so that you can specify a list of potential configuration file locations (e.g. current directory, user's home directory, systemwide directory), and all existing configuration files in the list will be read. A single filename may also be given.

Return list of successfully read files.

read_dict(*dictionary*, *source='<dict>'*)
Read configuration from a dictionary.

Keys are section names, values are dictionaries with keys and values that should be present in the section. If the used dictionary type preserves order, sections and their keys will be added in order.

All types held in the dictionary are converted to strings during reading, including section names, option names and keys.

Optional second argument is the 'source' specifying the name of the dictionary being read.

read_file(*f*, *source=None*)
Like read() but the argument must be a file-like object.

The 'f' argument must be iterable, returning one line at a time. Optional second argument is the 'source' specifying the name of the file being read. If not given, it is taken from f.name. If 'f' has no 'name' attribute, '<???>' is used.

read_string(*string*, *source='<string>'*)
Read configuration from a given string.

readfp(*fp*, *filename=None*)
Deprecated, use read_file instead.

remove_option(*section*, *option*)
Remove an option.

remove_section(*section*)
Remove a file section.

sections()
Return a list of section names, excluding [DEFAULT]

set(*section*, *option*, *value=None*)
Set an option. Extends RawConfigParser.set by validating type and interpolation syntax on the value.

setdefault(*k*[, *d*]) → D.get(k,d), also set D[k]=d if k not in D

update([*E*], ***F*) → None. Update D from mapping/iterable E and F.
If E present and has a .keys() method, does: for k in E: D[k] = E[k] If E present and lacks .keys() method, does: for (k, v) in E: D[k] = v In either case, this is followed by: for k, v in F.items(): D[k] = v

values() → an object providing a view on D's values

write(*fp*, *space_around_delimiters=True*)
Write an .ini-format representation of the configuration state.

If 'space_around_delimiters' is True (the default), delimiters between keys and values are surrounded by spaces.

Interpolation

_unify_values(*section*, *variables*)
Create a sequence of lookups with 'variables' taking priority over the 'section' which takes priority over the DEFAULTSECT.

has_option(*section*, *option*)
Check for the existence of a given option in a given section. If the specified *section* is None or an empty string, DEFAULT is assumed. If the specified *section* does not exist, returns False.

14.8.4 lib.Functions

Classes

- *CallByRefParam*: Implements a "call by reference" parameter.
- *Init*: Undocumented.
- *Exit*: Undocumented.

Functions

- *merge()*: Merge 2 or more dictionaries.
- *merge_with()*: Merge 2 or more dictionaries. Apply function f to each element during merge.

class lib.Functions.**CallByRefParam**(*value=None*)
Implements a "call by reference" parameter.

See also:

CallByRefBoolParam A special "call by reference" implementation for boolean reference types.

CallByRefIntParam A special "call by reference" implementation for integer reference types.

Inheritance

Members

class lib.Functions.**Init**

Inheritance

Members

classmethod init()

Foreground = {'BLUE': '\x1b[94m', 'CYAN': '\x1b[96m', 'DARK_CYAN': '\x1b[36m', 'DARK

class lib.Functions.**Exit**

Inheritance

Members

classmethod exit(*returnCode=0*)

classmethod versionCheck(*version*)

classmethod printException(*ex*)

classmethod printNotImplementedError(*ex*)

classmethod printExceptionBase(*ex*)

classmethod printPlatformNotSupportedException(*ex*)

classmethod printEnvironmentException(*ex*)

classmethod printNotConfiguredException(*ex*)

Functions

lib.Functions.**merge**(**dicts*)
Merge 2 or more dictionaries.

lib.Functions.**merge_with**(*f*, **dicts*)
Merge 2 or more dictionaries. Apply function f to each element during merge.

14.8.5 lib.Parser

Exceptions

- *ParserException*: Common base class for all non-exit exceptions.
- *MismatchingParserResult*: Signal the end from iterator.__next__().
- *EmptyChoiseParserResult*: Signal the end from iterator.__next__().
- *MatchingParserResult*: Signal the end from iterator.__next__().
- *GreedyMatchingParserResult*: Signal the end from iterator.__next__().

Classes

- *SourceCodePosition*: Undocumented.
- *Token*: Undocumented.
- *SuperToken*: Undocumented.
- *ValuedToken*: Undocumented.
- *StartOfDocumentToken*: Undocumented.
- *CharacterToken*: Undocumented.
- *SpaceToken*: Undocumented.
- *DelimiterToken*: Undocumented.
- *NumberToken*: Undocumented.
- *StringToken*: Undocumented.
- *Tokenizer*: Undocumented.

exception lib.Parser.**ParserException**

Inheritance

Members

args

with_traceback()
Exception.with_traceback(tb) – set self.__traceback__ to tb and return self.

exception lib.Parser.**MismatchingParserResult**

Inheritance

Members

args

value
generator return value

with_traceback()
Exception.with_traceback(tb) – set self.__traceback__ to tb and return self.

exception lib.Parser.**EmptyChoiseParserResult**

Inheritance

Members

args

value
generator return value

with_traceback()
Exception.with_traceback(tb) – set self.__traceback__ to tb and return self.

exception lib.Parser.**MatchingParserResult**

Inheritance

Members

args

value
generator return value

with_traceback()
Exception.with_traceback(tb) – set self.__traceback__ to tb and return self.

exception lib.Parser.**GreedyMatchingParserResult**

Inheritance

Members

args

value
generator return value

with_traceback()
Exception.with_traceback(tb) – set self.__traceback__ to tb and return self.

class lib.Parser.**SourceCodePosition**(*row*, *column*, *absolute*)

Inheritance

Members

class lib.Parser.**Token**(*previousToken*, *start*, *end=None*)

Inheritance

Members

PreviousToken

Length

class lib.Parser.**SuperToken**(*startToken*, *endToken=None*)

Inheritance

Members

Length

PreviousToken

class lib.Parser.**ValuedToken**(*previousToken*, *value*, *start*, *end=None*)

Inheritance

Members

Length

PreviousToken

class lib.Parser.**StartOfDocumentToken**

Inheritance

Members

Length

PreviousToken

class lib.Parser.**CharacterToken**(*previousToken*, *value*, *start*)

Inheritance

Members

Length

PreviousToken

class lib.Parser.**SpaceToken**(*previousToken*, *value*, *start*, *end=None*)

Inheritance

Members

Length

PreviousToken

class lib.Parser.**DelimiterToken**(*previousToken*, *value*, *start*, *end=None*)

Inheritance

Members

Length

PreviousToken

class lib.Parser.**NumberToken**(*previousToken*, *value*, *start*, *end=None*)

Inheritance

Members

Length

PreviousToken

class lib.Parser.**StringToken**(*previousToken*, *value*, *start*, *end=None*)

Inheritance

Members

Length

PreviousToken

class lib.Parser.**Tokenizer**

Inheritance

Members

class TokenKind

An enumeration.

SpaceChars = 0

AlphaChars = 1

NumberChars = 2

DelimiterChars = 3

OtherChars = 4

static GetCharacterTokenizer()

classmethod GetWordTokenizer(*iterable*, *alphaCharacters='abcdefghijklmnopqrstuvwxyzABCDEFGHIJKLMNO*
numberCharacters='0123456789', *whiteSpaceCharac-*
ters='\t')

14.8.6 lib.SphinxExtensions

Classes

- *DocumentMemberAttribute*: Undocumented.

class lib.SphinxExtensions.**DocumentMemberAttribute**(*value=True*)

Inheritance

Members

classmethod GetAttributes(*method*)

classmethod GetMethods(*cl*)

static _AppendAttribute(*attribute*)

_debug = False

14.8.7 lib.pyAttribute

Submodules

lib.pyAttribute.ArgParseAttributes

Classes

- *CommandGroupAttribute*: Undocumented.
- *DefaultAttribute*: Undocumented.
- *CommandAttribute*: Undocumented.
- *ArgumentAttribute*: Undocumented.
- *SwitchArgumentAttribute*: Undocumented.
- *CommonArgumentAttribute*: Undocumented.
- *CommonSwitchArgumentAttribute*: Undocumented.
- *ArgParseMixin*: Undocumented.

class lib.pyAttribute.ArgParseAttributes.**CommandGroupAttribute**(*groupName*)

Inheritance

Members

GroupName

classmethod GetAttributes(*method*)

classmethod GetMethods(*cl*)

static _AppendAttribute(*attribute*)

_CommandGroupAttribute__groupName = ''

_debug = False

class lib.pyAttribute.ArgParseAttributes.**DefaultAttribute**

Inheritance

Members

Handler

classmethod GetAttributes(*method*)

classmethod GetMethods(*cl*)

static _AppendAttribute(*attribute*)

_DefaultAttribute__handler = None

_debug = False

class lib.pyAttribute.ArgParseAttributes.**CommandAttribute**(*command*, ***kwargs*)

Inheritance

Members

Command

Handler

KWArgs

classmethod GetAttributes(*method*)

classmethod GetMethods(*cl*)

static _AppendAttribute(*attribute*)

_CommandAttribute__command = ''

_CommandAttribute__handler = None

_CommandAttribute__kwargs = None

_debug = False

class lib.pyAttribute.ArgParseAttributes.**ArgumentAttribute**(**args*, ***kwargs*)

Inheritance

Members

Args

KWArgs

classmethod GetAttributes(*method*)

classmethod GetMethods(*cl*)

static _AppendAttribute(*attribute*)

_ArgumentAttribute__args = None

_ArgumentAttribute__kwargs = None

_debug = False

class lib.pyAttribute.ArgParseAttributes.**SwitchArgumentAttribute**(**args*, ***kwargs*)

Inheritance

Members

Args

classmethod GetAttributes(*method*)

classmethod GetMethods(*cl*)

KWArgs

static _AppendAttribute(*attribute*)

_ArgumentAttribute__args = None

_ArgumentAttribute__kwargs = None

_debug = False

class lib.pyAttribute.ArgParseAttributes.**CommonArgumentAttribute**(**args*, ***kwargs*)

Inheritance

Members

Args

classmethod GetAttributes(*method*)

classmethod GetMethods(*cl*)

KWArgs

static _AppendAttribute(*attribute*)

_ArgumentAttribute__args = None

_ArgumentAttribute__kwargs = None

_debug = False

class lib.pyAttribute.ArgParseAttributes.**CommonSwitchArgumentAttribute**(**args*, ***kwargs*)

Inheritance

Members

Args

classmethod GetAttributes(*method*)

classmethod GetMethods(*cl*)

KWArgs

static _AppendAttribute(*attribute*)

_ArgumentAttribute__args = None

_ArgumentAttribute__kwargs = None

_debug = False

class lib.pyAttribute.ArgParseAttributes.**ArgParseMixin**(***kwargs*)

Inheritance

Members

static GetAttributes()

GetMethods()

static HasAttribute()

_ArgParseMixin__mainParser = None

_ArgParseMixin__subParser = None

_ArgParseMixin__subParsers = {}

Run()

MainParser

SubParsers

Classes

- *Attribute*: Undocumented.
- *AttributeHelperMixin*: Undocumented.

class lib.pyAttribute.**Attribute**

Inheritance

Members

_debug = False

static _AppendAttribute(*attribute*)

classmethod GetMethods(*cl*)

classmethod GetAttributes(*method*)

class lib.pyAttribute.**AttributeHelperMixin**

Inheritance

Members

GetMethods()

static HasAttribute()

static GetAttributes()

CHAPTER 15

More References

15.1 List of Supported FPGA Devices

Vendor	Family	Device Name
Altera	Max	Max-II, Max 10
	Cyclone	Cyclone III, Cyclone V
	Stratix	Stratix II, Stratix IV, Stratix V, Stratix 10
	Arria	Arria II, Arria V
Lattice	Mach	MachXO
	ECP	ECP3, ECP5
Xilinx	Coolrunner	Coolrunner-II
	Spartan	Spartan-3, Spartan-6
	Artix	Artix-7
	Kintex	Kintex-7, Kintex UltraScale, Kintex UltraScale+
	Virtex	Virtex-II, Virtex-4, Virtex-5, Virtex-7, Virtex UltraScale, Virtex UltraScale+
	Zynq	Zynq-7000

15.2 List of Supported Boards

Board Name	Device String	Device Name
GENERIC	GENERIC	Generic board and device
Altera	⇒ **DE4**	
DE0	EP3C16F484	Altera Cyclone III
S2GXAV	EP2SGX90FF1508C3	Altera Stratix II
DE4	EP4SGX230KF40C2	Altera Stratix IV
DE5	EP5SGXEA7N2F45C2	Altera Stratix V
Lattice	⇒ **ECP5Versa**	
ECP5Versa	LFE5UM-45F-6BG381C	Lattice ECP5
Xilinx	⇒ **KC705**	
S3SK200	XC3S200FT256	Xilinx Spartan-3
S3ESK500	XC3S500EFT256	Xilinx Spartan-3
S3SK1000	XC3S1000FT256	Xilinx Spartan-3
S3ESK1600	XC3S1600EFT256	Xilinx Spartan-3
ATLYS	XC6SLX45-3CSG324	Xilinx Spartan-6
ZC706	XC7Z045-2FFG900	Xilinx Zynq-7000
ZedBoard	XC7Z020-1CLG484	Xilinx Zynq-7000
AC701	XC7A200T-2FBG676C	Xilinx Artix-7
KC705	XC7K325T-2FFG900C	Xilinx Kintex-7
ML505	XC5VLX50T-1FF1136	Xilinx Virtex-5
ML506	XC5VSX50T-1FFG1136	Xilinx Virtex-5
ML507	XC5VFX70T-1FFG1136	Xilinx Virtex-5
XUPV5	XC5VLX110T-1FF1136	Xilinx Virtex-5
ML605	XC6VLX240T-1FF1156	Xilinx Virtex-6
VC707	XC7VX485T-2FFG1761C	Xilinx Virtex-7
VC709	XC7VX690T-2FFG1761C	Xilinx Virtex-7
Custom	**<any device>**	

15.3 Wrapper Script Hook Files

The shell scripts `poc.ps1` and `poc.sh` can be customized though hook files, which are executed before and after a PoC command is executed. The wrapper scripts support 4 kinds of hook files:

- VendorPreHookFile
- ToolPreHookFile
- VendorPostHookFile
- ToolPostHookFile

The wrapper scans the arguments given to the front-end script and searches for known commands. If one is found, the hook files are scheduled before and after the execution of the wrapped executable. The hook files are sourced into the current execution and need to be located in the `./py/Wrapper/Hooks` directory.

A common use case is the preparation of special vendor or tool chain environments. For example many EDA tools are using FlexLM as a license manager, which needs the environments variable `LM_LICENSE_FILE` to be set. A `PreHookFile` can be used to load/export such an environment variable.

15.3.1 Examples

Mentor QuestaSim on Linux:

The PoC infrastructure is called with this command line:

```
./poc.sh -v vsim PoC.arith.prng
```

The `vsim` command is recognized and the following events are scheduled:

1. `source ./py/Wrapper/Hooks/Mentor.pre.sh`
2. `source ./py/Wrapper/Hooks/Mentor.QuestaSim.pre.sh`
3. Execute `./py/PoC.py -v vsim PoC.arith.prng`
4. `source ./py/Wrapper/Hooks/Mentor.QuestaSim.post.sh`
5. `source ./py/Wrapper/Hooks/Mentor.post.sh`

If a hook files doesn't exist, it's skipped.

Mentor QuestaSim on Windows:

The PoC infrastructure is called with this command line:

```
.\poc.ps1 -v vsim PoC.arith.prng
```

The `vsim` command is recognized and the following events are scheduled:

1. `. .\py\Wrapper\Hooks\Mentor.pre.ps1`
2. `. .\py\Wrapper\Hooks\Mentor.QuestaSim.pre.ps1`
3. Execute `.\py\PoC.py -v vsim PoC.arith.prng`
4. `. .\py\Wrapper\Hooks\Mentor.QuestaSim.post.ps1`
5. `. .\py\Wrapper\Hooks\Mentor.post.ps1`

If a hook files doesn't exist, it's skipped.

15.3.2 FlexLM

Many EDA tools require an environment variable called `LM_LICENSE_FILE`. If no other tool settings are required, a common `FlexLM.sh` can be generated. This file is used as a symlink target for each tool specific hook file.

Content of the 'FlexLM.sh' script:

```
export LM_LICENSE_FILE=1234@flexlm.company.com
```

Create symlinks:

```
ln -s FlexLM.sh Altera.Quartus.pre.sh
ln -s FlexLM.sh Mentor.QuestaSim.pre.sh
```

15.4 File Formats

15.4.1 *.ini Format

Document rule:

DocumentLine rule:

Section rule:

OptionLine rule:

FQSectionName rule:

15.4.2 *.files Format

Contents of this Page

Files files are used to ...

Line comments start with `#`.

Document

Source File Statements

Bla `VHDLStatement` blub

- `vhdl Library "<VHDLFile>"` This statement references a VHDL source file.
- `verilog "<VerilogFile>"` This statement references a Verilog source file.
- `cocotb "<PythonFile>"` This statement references a Cocotb testbench file (Python file).
- `ucf "<UCFFile>"` This statement references a Xilinx User Constraint File (UCF).
- `sdc "<SDCFile>"` This statement references a Synopsys Design Constraint file (SDC).
- `xdc "<XDCFile>"` This statement references a Xilinx Design Constraint file (XDC).
- `ldc "<LDCFile>"` This statement references a Lattice Design Constraint file (LDC).

Conditional Statements

- `If (<Expression>) Then ... [ElseIf (<Expression>) Then ...][Else ...] End IF` This allows the user to define conditions, when to load a source file into the file list. The `ElseIF` and `Else` clause of an `If` statement are optional.

Boolean Expressions

Unary operators

- `!` - not
- `[...]` - list construction
- `?` - file exists

Binary operators

- `and` - and
- `or` - or
- `xor` - exclusive or
- `in` - in list
- `=` - equal
- `!=` - unequal
- `<` - less than
- `<=` - less than or equal
- `>` - greater than
- `>=` - greater than or equal

Literals

- `<constant>` - a pre-defined constant
- `"<String>"` - Strings are enclosed in quote signs
- `<Integer>` - Integers as decimal values

Pre-defined constants

- Environment Variables:
  - **`Environment`** Values:
    - `"Simulation"`
    - `"Synthesis"`
  - `ToolChain` - The used tool chain. E.g. `"Xilinx_ISE"`
  - `Tool` - The used tool. E.g. `"Mentor_QuestaSim"` or `"Xilinx_XST"`
  - `VHDL` - The used VHDL version. `1987`, `1993`, `2002`, `2008`
- Board Variables:
  - `BoardName` - A string. E.g. `"KC705"`
- Device Variables:
  - `DeviceVendor` - The vendor of the device. E.g. `"Altera"`
  - `DeviceDevice` -
  - `DeviceFamily` -
  - `DeviceGeneration` -
  - `DeviceSeries` -

Path Expressions

- `/` - sub-directory
- `&` - string concat

Other Statements

- `include "<FilesFile>"` Include another *.files file.
- `library <VHDLLibrary> "<LibraryPath>"` Reference an existing (pre-compiled) VHDL library, which is passed to the simulator, if external libraries are supported.
- `report "<Message>"` Print a critical warning in the log window. This critical warning is treated as an error.

15.4.3 *.rules Format

Contents of this Page

Headline 1

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15.5 Naming Conventions

Todo: Write an intruduction paragraph for this page.

15.5.1 Root Directory Overview (PoCRoot)

The PoC-Library is structured into several sub-directories, naming the purpose of the directory like `src` for sources files or `tb` for testbench files. The structure within these directories is most likely the same and based on PoC's *sub-namespace tree*. PoC's installation directory is also referred to as `PoCRoot`.

- **`lib`** Third party libraries like Coctb, OSVVM or VUnit are shipped in this folder. The external library is stored in a sub directory named like the library. If a library is available as a Git submodule, then it is linked as a submodule for better version tracking.
- **`netlist`** This is the output directory for pre-configured netlists, synthesized by PoC. Netlists and related constaint files are the result of IP core synthesis flows, either from PoC's source files or from vendor specific IP core files like *.xco files from Xilinx Core Generator. Generated IP cores are stored in device sub-directories, because most netlists formats are device specific. For example the IP core `PoC.arith.prng` created from source file `src\arith\arith_prng.vhdl` generated for a Kintex-7 325T mounted on a KC705 board will be copied to `netlist\XC7K325T-2FFG900\arith\arith_prng.ngc` if Xilinx ISE XST is used for synthesis.
- **`py`** The supporting Python infrastructure, the configuration files and the IP core 'database' is stored in this directory.
- **`sim`** Some of PoC's testbenches are shipped with pre-configured waveform views/ waveform configuration files for selected simulators or waveform viewers. If a testbench is launched in GUI mode (`--gui`) and a waveform view for the choosen simulator is found, it's loaded as the default view.
- **`src`** The source files of PoC's IP cores are stored in this directory. The IP cores are grouped by their sub-namespace into sub-directories according to the *sub-namespace tree*. See the paragraph below, for how IP cores are named and how PoC core names map to the sub-namespace hierachy and the resulting sub-namespace directory structure.
- **`tb`** PoC is shipped with testbenches. All testbenches are categorized and stored in sub-directories like the IP core, which is tested.
- **`tcl`** Supporting Tcl files.
- **`temp`** A pre-created temporary directors for various tool's intermediate outputs. In case of errors in a used vendor tool or in PoC's infrastructure, this directory contains intermediate files, log files and report files, which can be used to analyze the error.
- **`tools`** This directory contains miscelaneous files or scripts for external tools like emacs, git or text editor syntax highlighting files.
- **`ucf`** Pre-configured constraint files (*.ucf, *.xdc, *.sdc) for many FPGA boards, containing physical (pin, placement) and timing constraints.
- **`xst`** Configuration files to synthesize PoC modules with Xilinx XST into a netlist.

15.5.2 Namespaces and Modules

Namespaces

PoC uses namespaces and sub-namespaces to categorize all VHDL and Verilog modules. Despite VHDL doesn't support sub-namespaces yet, PoC already uses sub-namespaces enforced by a strict naming schema.

Rules: 1. Namespace names are lower-case, underscore free, valid VHDL identifiers. 2. A namespace name is unique, but can be part of a entity name.

Module Names

Module names are prefixed with its parents namespace name. A module name can contain underscores to denote implementation variants of a module.

Rules: 3. Modul names are valid VHDL identifiers prefixed with its parent namespace's name. 4. The first part of module name must not contain the parents namespace name.

Example 1 - `PoC.fifo.cc_got`

For example a FIFO module with a common clock interface and a *got* semantic is named `PoC.fifo.cc_got` (fully qualified name). This name can be split at every dot and underscore sign, resulting in the following table of name parts:

PoC	fifo	cc	got
Root Namespace	Sub-Namespace	Common Clock Interface	Got Semantic

Because `PoC.fifo.cc_got` refers to an IP core, the source file is located in the `<PoCRoot>\src` directory. The (sub-)namespace of the PoC entity is `fifo`, so it's stored in the sub-directory `fifo`. The file name `cc_got` FIFO is prefixed with the last sub-namespace: In this case `fifo_`. This is summarized in the following table:

Property	Value
Fully Qualified Name	PoC.fifo.cc_got
VHDL entity name	fifo_cc_got
File name	fifo_cc_got.vhdl
IP Core Description File	\src\fifo\fifo_cc_got.files
Source File Location	\src\fifo\fifo_cc_got.vhdl
Testbench Location	\tb\fifo\fifo_cc_got_tb.vhdl
Testbench Description File	\tb\fifo\fifo_cc_got_tb.files
Waveform Description Files	\sim\fifo\fifo_cc_got_tb.*

Other implementation variants are:

- `_dc` – dependent clock / related clock
- `_ic` – independent clock / cross clock
- `_got_tempgot` – got interface extended by a temporary got interface
- `_got_tempput` – got interface extended by a temporary put interface

Example 2 - `PoC.mem.ocram.tdp`

PoC	mem	ocram	tdp
Root Namespace	Sub-Namespace	Sub-Namespace	True-Dual-Port

Property	Value
Fully Qualified Name	PoC.mem.ocram.tdp
VHDL entity name	ocram_tdp
File name	ocram_tdp.vhdl
IP Core Description File	\src\mem\ocram\ocram_tdp.files
Source File Location	\src\mem\ocram\ocram_tdp.vhdl
Testbench Location	\tb\mem\ocram\ocram_tdp_tb.vhdl
Testbench Description File	\tb\mem\ocram\ocram_tdp_tb.files
Waveform Description Files	\sim\mem\ocram\ocram_tdp_tb.*

Note: Not all sub-namespace parts are include as a prefix in the name, only the last one.

15.5.3 Signal Names

Todo: No documentation available.

15.6 Known Issues

15.6.1 General

Synthesis of tri-state signals

Tri-state signals should be only used when they are connected (through the hierarchy) to top-level bidirectional or output pins.

Descriptions which infer a tri-state driver like:

```
pin <= data when tri = '0' else 'Z';
```

should not be included in any IP core description because these hinder or even inhibit block-based design flows. If a netlist is generated from such an IP core, the netlist may contain only a simple internal (on-chip) tri-state buffer instead of the correct tri-state I/O block primitive because I/O buffers are not automatically added for netlist generation. If the netlist is then used in another design, the mapper, e.g. Xilinx ISE Map, may fail to merge the internal tri-state buffer of the IP core netlist with the I/O buffer automatically created for the top-level netlist. This failing behavior is not considered as a tool bug.

Thus, if tri-state drivers should be included in an IP core, then the IP core description must instantiate the appropriate I/O block primitive of the target architecture like it is done by the Xilinx MIG.

Synthesis of bidirectional records

Records are useful to group several signals of an IP core interface. But the corresponding port of this record type should not be of mode `inout` to pass data in both direction. This restriction holds even if a record member will be driven only by one source in the real hardware and even if all the drivers (one for each record member) are visible to the current synthesis run. The following observations have been made:

- An IP core (entity or procedure) must drive all record members with value 'Z' which are only used as an input in the IP core. If this is missed, then the respective record member will be driven by 'U' and the effective value after resolution will be 'U' as well, see IEEE Std. 1076-2008 para. 12.6.1. Thus simulation will fail.

  But these 'Z' drivers will flood the RTL / Netlist view of Altera Quartus-II, Intel Quartus Prime and Lattice Diamond with always tri-stated drivers and make this view unusable.

Note: Simulation with ModelSim shows correct output even when the 'Z' driver is missing, but a warning is reported that the behavior is not VHDL Standard compliant.

- Altera Quartus-II and Intel Quartus Prime report warnings about this meaningless 'Z' drivers. Synthesis result is as expected if each record member is only driven by one source in real hardware.
- The synthesis result of the Lattice Synthesis Engine (3.7.0 / 3.8.0) is not optimal. It seems that the synthesizer tries to implement the internal (on-chip) tristate bus using AND-OR logic but failed to optimize it away because there was only one real source. Test case was a simple SRAM controller which used the record type `T_IO_TRISTATE` to bring-out the data-bus so that the tri-state driver could be instantiated on the top-level.

Use separate records for the input and output data flow instead.

15.6.2 Aldec Active-HDL

- Aliases to functions and protected type methods

15.6.3 Altera Quartus-II / Intel Quartus Prime

- Generic types of type strings filled with NUL

15.6.4 GHDL

- Aliases to protected type methods

15.6.5 Xilinx ISE

- Shared Variables in Simulation (VHDL-93)

15.6.6 Xilinx Vivado

- Physical types in synthesis
- VHDL-2008 mode in simulation
- Shared variables in simulation (VHDL-93 and VHDL-2008))

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[1] Formatted means, that reStructured Test (reST) markup is used to highlight headlines, to display lists as unordered or ordered lists and to emphasis special wording in bold. There is no change in words, spelling or paragraph numbering. The formatting is needed to allow a proper rendering with Sphinx and to create a correct toctree (Table of Content Tree).

15.7.1 Apache License 2.0

Version 2.0, January 2004

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Part IV

Appendix

CHAPTER 16

Change Log

CHAPTER 17

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