fft_wrapper Project Status (11/14/2014 - 03:03:05)			
Project File:	final_deadline3.xise	**Parser Errors:**	No Errors
Module Name:	fft_wrapper	**Implementation State:**	Synthesized
Target Device:	xc7z020-1clg484	• **Errors:**	No Errors
Product Version:	ISE 14.4	• **Warnings:**	39 Warnings (39 new)
Design Goal:	Balanced	• **Routing Results:**	
Design Strategy:	Xilinx Default (unlocked)	• **Timing Constraints:**	
Environment:	System Settings	• **Final Timing Score:**	

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	1477	106400	1%
Number of Slice LUTs	1388	53200	2%
Number of fully used LUT-FF pairs	1085	1780	60%
Number of bonded IOBs	83	200	41%
Number of BUFG/BUFGCTRLs	2	32	6%
Number of DSP48E1s	3	220	1%

Detailed Reports					[-]
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	Fri 14. Nov 03:03:03 2014	0	39 Warnings (39 new)	7 Infos (7 new)
Translation Report					
Map Report					
Place and Route Report					
Power Report					
Post-PAR Static Timing Report					
Bitgen Report					

Secondary Reports			[-]
Report Name	**Status**	**Generated**	

Date Generated: 11/14/2014 - 03:07:31