fft_wrapper Project Status (11/14/2014 - 14:38:29)			
Project File:	final_deadline3.xise	**Parser Errors:**	No Errors
Module Name:	fft_wrapper	**Implementation State:**	Placed and Routed
Target Device:	xc7z020-1clg484	• **Errors:**	No Errors
Product Version:	ISE 14.4	• **Warnings:**	140 Warnings (140 new)
Design Goal:	Balanced	• **Routing Results:**	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	• **Timing Constraints:**	All Constraints Met
Environment:	System Settings	• **Final Timing Score:**	0 (Timing Report)

Device Utilization Summary				[-]
Slice Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Registers	1,457	106,400	1%	
Number used as Flip Flops	1,457			
Number used as Latches	0			
Number used as Latch-thrus	0			
Number used as AND/OR logics	0			
Number of Slice LUTs	1,292	53,200	2%	
Number used as logic	981	53,200	1%	
Number using O6 output only	487			
Number using O5 output only	24			
Number using O5 and O6	470			
Number used as ROM	0			
Number used as Memory	241	17,400	1%	
Number used as Dual Port RAM	128			
Number using O6 output only	128			
Number using O5 output only	0			
Number using O5 and O6	0			
Number used as Single Port RAM	0			
Number used as Shift Register	113			
Number using O6 output only	62			
Number using O5 output only	0			
Number using O5 and O6	51			

Number used exclusively as route-thrus	70			
Number with same-slice register load	68			
Number with same-slice carry load	2			
Number with other load	0			
Number of occupied Slices	483	13,300	3%	
Number of LUT Flip Flop pairs used	1,477			
Number with an unused Flip Flop	224	1,477	15%	
Number with an unused LUT	185	1,477	12%	
Number of fully used LUT-FF pairs	1,068	1,477	72%	
Number of unique control sets	18			
Number of slice register sites lost to control set restrictions	59	106,400	1%	
Number of bonded IOBs	83	200	41%	
IOB Latches	32			
Number of RAMB36E1/FIFO36E1s	0	140	0%	
Number of RAMB18E1/FIFO18E1s	0	280	0%	
Number of BUFG/BUFGCTRLs	1	32	3%	
Number used as BUFGs	1			
Number used as BUFGCTRLs	0			
Number of IDELAYE2/IDELAYE2_FINEDELAYs	0	200	0%	
Number of ILOGICE2/ILOGICE3/ISERDESE2s	0	200	0%	
Number of ODELAYE2/ODELAYE2_FINEDELAYs	0			
Number of OLOGICE2/OLOGICE3/OSERDESE2s	32	200	16%	
Number used as OLOGICE2s	32			
Number used as OLOGICE3s	0			
Number used as OSERDESE2s	0			
Number of PHASER_IN/PHASER_IN_PHYs	0	16	0%	
Number of PHASER_OUT/PHASER_OUT_PHYs	0	16	0%	
Number of BSCANs	0	4	0%	
Number of BUFHCEs	0	72	0%	
Number of BUFRs	0	16	0%	
Number of CAPTUREs	0	1	0%	
Number of DNA_PORTs	0	1	0%	
Number of DSP48E1s	3	220	1%	
Number of EFUSE_USRs	0	1	0%	

Number of FRAME_ECCs	0	1	0%	
Number of ICAPs	0	2	0%	
Number of IDELAYCTRLs	0	4	0%	
Number of IN_FIFOs	0	16	0%	
Number of MMCME2_ADVs	0	4	0%	
Number of OUT_FIFOs	0	16	0%	
Number of PHASER_REFs	0	4	0%	
Number of PHY_CONTROLs	0	4	0%	
Number of PLLE2_ADVs	0	4	0%	
Number of PS7s	0	1	0%	
Number of STARTUPs	0	1	0%	
Number of XADCs	0	1	0%	
Average Fanout of Non-Clock Nets	2.73			

Performance Summary			[-]
Final Timing Score:	0 (Setup: 0, Hold: 0)	**Pinout Data:**	Pinout Report
Routing Results:	All Signals Completely Routed	**Clock Data:**	Clock Report
Timing Constraints:	All Constraints Met		

Detailed Reports					[-]
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	Fri 14. Nov 03:03:03 2014	0	39 Warnings (39 new)	7 Infos (7 new)
Translation Report	Current	Fri 14. Nov 14:31:44 2014	0	16 Warnings (16 new)	0
Map Report	Current	Fri 14. Nov 14:35:51 2014	0	85 Warnings (85 new)	7 Infos (7 new)
Place and Route Report	Current	Fri 14. Nov 14:37:29 2014	0	0	2 Infos (2 new)
Power Report					
Post-PAR Static Timing Report	Current	Fri 14. Nov 14:38:27 2014	0	0	4 Infos (4 new)
Bitgen Report					

Secondary Reports		[-]
Report Name	**Status**	**Generated**
ISIM Simulator Log	Current	Fri 14. Nov 03:22:57 2014

Date Generated: 11/14/2014 - 14:38:29