# KEYPAD SCANNER

**Aditya Sundararajan, Sagar Bhanushali, Dishant Gala, Rahul Ghuge**

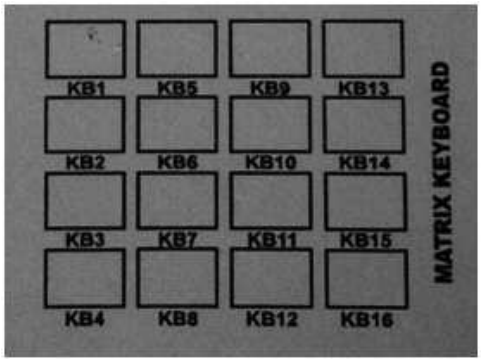
October 22, 2009

## 1 Abstract

A 4x4 matrix keypad is often used others in mobile phone and building entry control.This project objective is to design an interface for such a keypad that could be used for example in building entry control system. The task is to detect whenever a key is pressed on the keypad, and display its output on 7-Segment Display.

## 2 Introduction

The keyboard consists of 16 keys being named KB1 to KB16. It consists of hexadecimal numerals for 0 to F. The keys have been organized as four rows of four keys each in a sense, matrix of four rows and four columns. The processor scans the rows and monitors the columns for a logic change. When a change occurs, it indicates that one of the buttons in that column was pressed. By knowing which row was being scanned, and which column changed state, the processor can deduce which specific button was pushed.




KEY DETAILS

| KEY | CODE |
|---|---|
| KB1 | 0 |
| KB2 | 1 |
| KB3 | 2 |
| KB4 | 3 |
| KB5 | 4 |
| KB6 | 5 |
| KB7 | 6 |
| KB8 | 7 |
| KB9 | 8 |
| KB10 | 9 |
| KB11 | A |
| KB12 | B |
| KB13 | C |
| KB14 | D |
| KB15 | E |
| KB16 | F |

## 3 Analysis

**Keypad:**

The basic features of the interface are explained with the help of the enclosed program.

The enclosed program illustrates how the keyboard is scanned, detects a key closure, debounces it, decodes it, and displays the corresponding hex code in the display. The program will scan the keyboard row by row and checks whether any key is closed.

If it finds a key closure, it will find the code of the closed key and displays its Program uses two-key lockouts. If two keys are pressed simultaneously, key code corresponding to the key released last will be displayed.

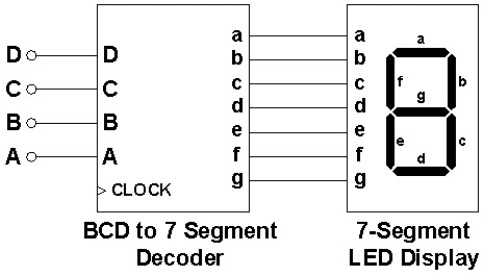
The user can press any other keys and corresponding key code to the closed key will be displayed on the seven-segment display provided on the baseboard of the CPLD/ FPGA trainer. The corresponding key code to each key is given in the following table.

A KEY is sensed using a keyboard routine. In this routine, the rows are continuously scanned at fixed intervals (once in one milliseconds).

The RESET (TS1) key present on the Baseboard has to be made '0' to display the numerals on the seven-segment display. If it is made '1', it will only display 'F' irrespective of the key pressed.

**Seven - Segment Display:**

Seven-segment display is the most popular display device used in digital systems. For displaying data using this device, the data have to be in the 7-segment code format. The program converts four binary inputs to seven-segment format. The binary input is given through 4 switches. In a seven-segment display there are 8 segments including the DOT.




These eight outputs from the FPGA are connected to cathodes of the Seven-segment display. Anodes are common. It has a SEL (select) switches with enable ENA1 or ENA2 depending on the status. The figure below shows the block diagram of the design.

| INPUTS | | | | h | g | f | e | d | c | b | a |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 |

# 4 Applications

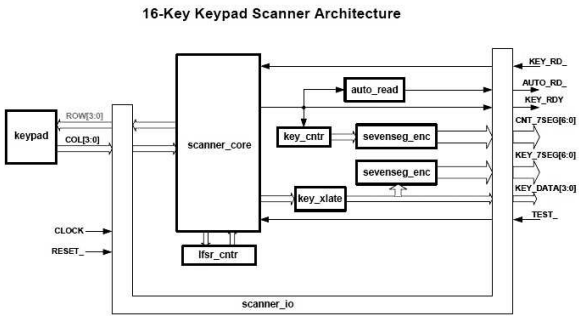
1. This project can be used to interface the keypad with LCD.

2. The interfaced keypad can be used for access control.

3. The interfaced keypad can be used for calculators.

# 5 Logic used in VHDL program

The CPLD scans the rows and monitors the columns for a change in state. When a key is pressed, the CPLD stops scanning and immediately sends an encoded word out to the processor indicating the key pressed.




To scan the keypad rows, a barrel shift register is initialized with all ones except for one bit preset to a zero. Each bit of the shift register drives a CPLD output pin that is connected to a row of the keypad.

As the shift register is clocked the zero shifts through the barrel shifter and scans the rows by driving them low one at a time.

The columns are inputs to the CPLD. Each input is pulled up with an internal pull up resistor. When no keys are pushed, all column inputs to the CPLD are passively pulled up to a logic high state. All column inputs are ANDed together. A logic one at the output of the AND gate indicates no keys are pressed. The output of the AND is used as an enable to the shift register.

When a key is pressed, a connection between a row and column is made. The column with the key being pressed will be driven low by the row associated with that key. The output of the AND will go low and disable the shift register for how ever long the key is pressed.

At this point the shift register is driving the row of the key being pressed to a low, and the column of that key is also at a low. Two encoders are used, one for the row bits (outputs of the shift register), and another for the column inputs. The outputs of the two encoders are grouped together to form the resulting encoded word that is presented to the processor.

# 6 Working

The synthesis (hardware implementation) of the project was done on CPLD using Xilinx IC XC9572/XC95180 Module. The CPLD provides very high clock frequencies (100KHz-5MHz) for high speed applications which can be reduced using clock reduction code to suit the circuit requirements. The inputs and enable pins are assigned switches through which they can be toggled. All the four 7-segment displays are common anode(thus has active low inputs)and the outputs are multiplexed(all four displays show same output). Each display has an active low enable input. Particular segments can be hindered by using the appropriate switches provided alongside the SSD's.

# 7 About Xilinx

Xilinx designs, develops and markets programmable logic products including integrated circuits (ICs), software design tools, predefined system functions delivered as intellectual property (IP) cores, design services, customer training, field engineering and technical support. Xilinx sells both FPGAs and CPLDs programmable logic devices for electronic equipment manufacturers in end markets such as communications, industrial, consumer, automotive and data processing. Xilinx FPGAs can run a regular embedded OS (such as Linux or vxWorks) and can implement processor peripherals in programmable logic. Xilinx delivers programmable platforms to help design engineers make their vision a reality. Xilinx programmable chips are the innovation platform of choice for today's leading companies for the design of tens of thousands of products that improve the quality of our everyday lives. Xilinx designs, develops and markets programmable logic products including integrated circuits (ICs), software design tools, predefined system functions delivered as intellectual property (IP) cores, design services, customer training, field engineering and technical support. Xilinx sells both FPGAs and CPLDs programmable logic devices for electronic equipment manufacturers in end markets such as communications, industrial, consumer, automotive and data processing. Xilinx's FPGAs have been used for the ALICE (A Large Ion Collider Experiment) at the CERN European laboratory on the French-Swiss border to map and disentangle the trajectories of thousands of subatomic particles. Xilinx has also engaged in a partnership with the United States Air Force Research Laboratories Space Vehicles Directorate to develop FPGAs to withstand the damaging effects of radiation in space for deployment in new satellites, which are 1,000 times less sensitive to space radiation than the commercial equivalent. The Virtex-II Pro, Virtex-4, Virtex-5, and Virtex-6 FPGA families are focused on system-on-chip (SoC) designers because they include up to two embedded IBM PowerPC cores. There are no PowerPC blocks in any Xilinx devices other than Virtex-II Pro. Xilinx FPGAs can run a regular embedded OS (such

as Linux or vxWorks) and can implement processor peripherals in programmable logic. Xilinx's IP cores include IP for simple functions (BCD encoders, counters, etc.), for domain specific cores (digital signal processing, FFT and FIR cores) to complex systems (multi-gigabit networking cores, MicroBlaze soft microprocessor, and the compact Picoblaze microcontroller). Xilinx also creates custom cores for a fee. The ISE Design Suite is the central electronic design automation (EDA) product family sold by Xilinx. The ISE Design Suite features include design entry and synthesis supporting Verilog or VHDL, place-and-route (PAR), completed verification and debug using ChipScope Pro tools, and creation of the bit files that are used to configure the chip. Xilinx's Embedded Developer's Kit (EDK) supports the embedded PowerPC 405 and 440 cores (in Virtex-II Pro and some Virtex-4 and -5 chips) and the Microblaze core. Xilinx's System Generator for DSP implements DSP designs on Xilinx FPGAs. A freeware version of its EDA software called ISE WebPACK is used with some of its non-high-performance chips. Xilinx is the only (as of 2007) FPGA vendor to distribute a native Linux freeware synthesis tool chain. Xilinx announced the architecture for an Extensible Processing Platform, which licenses the ARM Cortex-A9 MPCore processor for embedded systems designers familiar with the ARM platform. The Extensible Processing Platform architecture abstracts much of the hardware burden away from the embedded software developers' point of view, giving them an unprecedented level of control in the development process. With this platform, software developers can leverage their existing system code based on ARM technology and utilize vast off-the-shelf open-source and commercially available software component libraries. Because the system boots an OS at reset, software development can get under way quickly within familiar development and debug environments using tools such as ARMs RealView development suite and related third-party tools, Eclipse-based IDEs, GNU, the Xilinx Software Development Kit and others. The platform targets embedded designers working on market applications that require multifunctionality and real-time responsiveness, such as automotive driver assistance, intelligent video surveillance, industrial automation, aerospace and defense, and next-generation wireless.Xilinx announced, in early 2011, a new Zynq product family specifically based on its extensible processing platform.

# 8 Features of CPLD

1. High performance -5 ns pin to pin logic delay - Counter frequency 125 MHz

2. Large density range -36-288 macrocells with upto 6000 usable gates.

3. Enhanced pin locking architecture.

4. Programmable power reduction mode in each macrocell.

5. Slew rate control.

6. High drive 24 mA output.

7. Advanced CMOS 5v fast Flash technology.

8. Flexible 36V 18 function block-90 product terms drive any or all of 18 macro cells within function block-global and product term clocks, output enables, set and reset signals.

9. Extensive IEEE std 1149.1 boundary scan(JTAG) support.

10. Programmable power reduction mode in each macrocell.

11. Skew rate controlled on individual outputs.

12. User programmable ground pin capability.

# 9 CPLD Kit

The design of a digital system using PLD often requires the connection of several devices to produce the complete specification. For these type of applications, Complex Programmable Logic Devices(CPLD) are more suitable. A CPLD is a collection of individual PLDs on a single integrated circuit. A programmable interconnection structure allows the PLDs to be connected to each other in the same way that can be done with the individual PLDs.

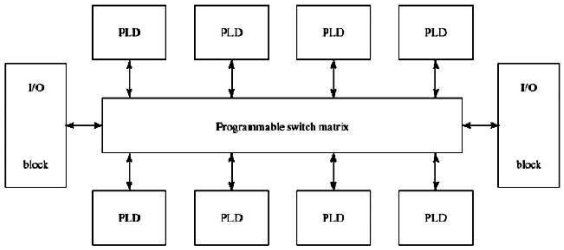
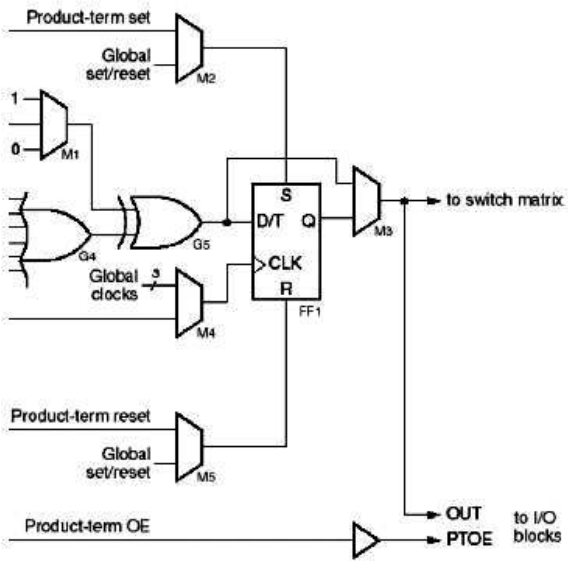



Fig. 7-20 General CPLD Configuration

Now, the switch matrix receives inputs from the I/O block and directs it to the individual macrocells. Similarly, selected outputs from macrocells are sent to the outputs as needed. Each PLD typically contains from 8 to 16 macrocells. The macrocells within each PLD are usually fully connected. If a macrocell has unused product terms they can be used by other nearby macrocells. Different manufacturers use different approaches to make individual PLDs, the type of macrocells, I/O blocks and the programmable interconnection structure. The basic component used in PLD is the gate array. A gate array consists of pattern of gates fabricated in an area of silicon that is repeated thousands of times until the entire chip is covered with the gates.




**CPLD FAMILIES**

The basic construction of a CPLD remains a constant. The differentiator in various CPLD families is the different number of PLD blocks and the different number of I/O pins. Many CPLDs have fewer I/O pins than macrocells. The IC package size dictates the number of I/O pins but not the total number of macrocells. Typical CPLD families have devices with differing resources in the same IC package. The various families are described below:

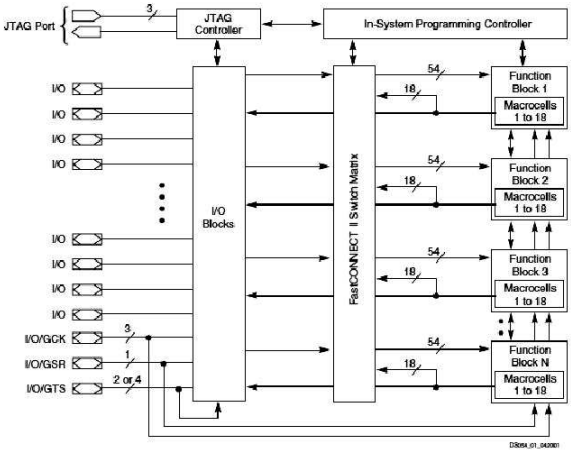
**CoolRunner-II 1.8 Volt CPLD:**
Low power
Up to 512 macrocells
Up to 4 I/O banks
Advanced security features
XC9500XV 2.5 Volt CPLD
Up to 4 I/O banks
2.5V, 3.3V I/O tolerance
Up to 288 macrocells
More product terms per macrocell

**XC9500XL 3.3 Volt CPLD**
5V tolerance
Up to 288 macrocells
More product terms per macrocell
Industry's highest I/O per package

**CoolRunner XPLA3 3.3 Volt CPLD**
Low power
5V tolerance
Up to 512 macrocells

**XC9500 5 Volt CPLD**
5V I/O tolerance
Up to 288 macrocells
24mA I/O drive

Now in the XC9500 family, various CPLDs can be distinguished as follows:




The above figure is a block diagram of the internal architecture of a typical XC9500 family CPLD. Each internal I/O pin can be used as a input, an output or a bidirectional pin according to the devices programming. The pins at the bottom of the figure can also be used for special purposes. Any of the three pins can be used as "Global Clocks" (GCK). One pin can be used as a "Global Set/Reset"(GSR) . Finally two or four pins can be used as "Global Three State Controls"(GTS). Only four FBs are shown in the figure, but the XC9500 architecture scales to accommodate 16 FBs in the XC95288. Regardless of the specific family member, each FB programmably receives 36 signals from the switch matrix. The inputs to the switch matrix are the 18 macrocell outputs from each of the FBs and the external inputs from the I/O pins. Each FB also has 18 outputs that run under the switch matrix.

**Xilinx XC9500 Product Family**

| | 9536 | 9572 | 95108 | 95144 | 95216 | 95288 |
|---|---|---|---|---|---|---|
| Macrocells | 36 | 72 | 108 | 144 | 216 | 288 |
| Usable Gates | 800 | 1600 | 2400 | 3200 | 4800 | 6400 |
| $t_{PD}$ (ns) | 5 | 7.5 | 7.5 | 7.5 | 10 | 10 |
| Registers | 36 | 72 | 108 | 144 | 216 | 288 |
| Max I/O | 34 | 72 | 108 | 133 | 166 | 192 |
| Packages | VQ44<br>PC44 | PC44<br>PC84<br>TQ100<br>PQ100 | PC84<br>TQ100<br>PQ100<br>PQ160 | PQ100<br>PQ160 | PQ160<br>HQ208<br>BG352 | HQ208<br>BG352 |

We have used the XC9572-15pc84 CPLD to implement our program. Since it belongs to the XC9500, the many features of the family are elaborated.

The architechture of the CPLD is as follows:

# 10 Conclusion

This project dealt with the design of a keypad encoding circuit. The keypad matrix was interfaced with the Seven-Segment Display. Moreover, the logic and code used for this project can be used for calculators, access control, etc.

# 11 References


1. **Bookname:** Circuit Design with VHDL
   **Author:** Volnei A. Pedroni
   **Publication:** The MIT Press

2. **Bookname:** Modern Digital Design.
   **Author:** R.P. Jain.
   **Publication:** Tata McGraw Hill.