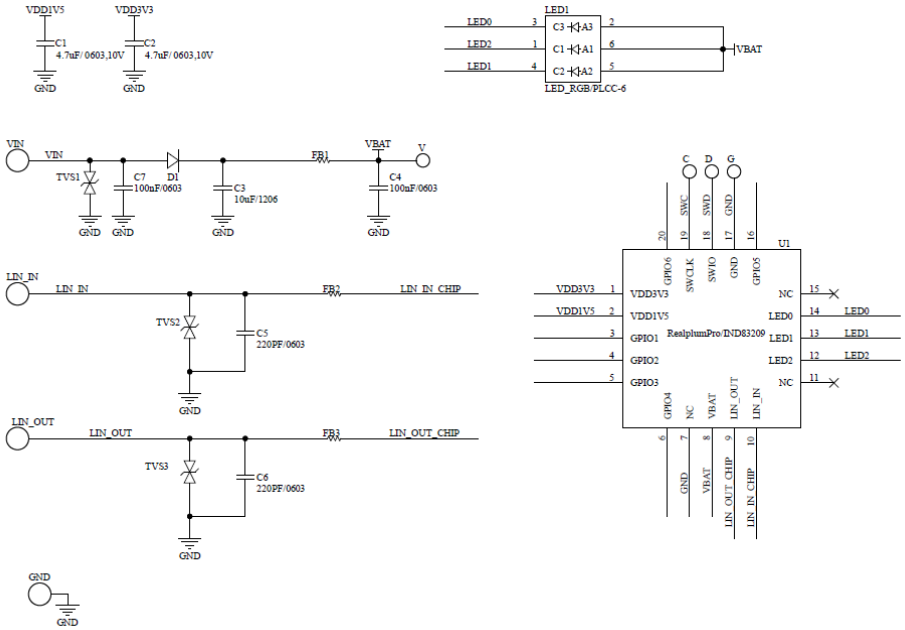
iND83209
iND83211
Hardware User Guide

OVERVIEW

1.Introduction of iND83209（realplumPro） circuit schematic
   a. design details
   b. the selection of components
2. The requirements of layout for iND83209
3. Introduction of iND83211(rugbyPro) circuit schematic
   a. design details
   b. the selection of components
4. The requirements of layout for iND83211
   a. buck circuit design

CIRCUIT SCHEMATIC (iND83209)

- Design details



This diagram shows the typical circuit schematic for iND83209.

Do not reduce the recommended components.

Component Selection

- 1.TVS(TVS1,TVS2,TVS3)

The TVS is used for ESD protection. It should be bidirectional (negative voltage). The ability of protection should be stronger than ESD test.

Also, the clamping voltage should be less than 45V.

e.g. ESD Test level: +/-8kV contact discharge +/-15kV air discharge

Maximum Ratings

Rating	Symbol	Value	Unit
Peak pulse power (tp=10/1000μs waveform)	P_{PP}	200	W
Peak pulse power (tp=8/20μs waveform)	P_{PP}	1000	W
ESD voltage (Contact discharge)	V_{ESD}	±30	kV
ESD voltage (Air discharge)		±30	
Storage & operating temperature range	T_{STG} ,T_J	-55~+150	℃

2. Diode(D1)

In EMC test, the test pulse has negative peak voltage. So, The maximum negative voltage of diode should higher than the testing standard.

Another parameter should be noticed is forward current. It should be larger than the total current in circuit.

e.g. testing standard: negative peak voltage is 450V.

PARAMETER	SYMBOL	GS1000FL-AU	GS1001FL-AU	GS1002FL-AU	GS1004FL-AU	GS1006FL-AU	GS1008FL-AU	GS1010FL-AU	UNITS
Marking Code		1A	1B	1D	1G	1J	1K	1M	
Maximum Recurrent Peak Reverse Voltage	V_{RRM}	50	100	200	400	600	800	1000	V
Maximum RMS Voltage	V_{RMS}	35	70	140	280	420	640	700	V
Maximum DC Blocking Voltage	V_{DC}	50	100	200	400	600	800	1000	V

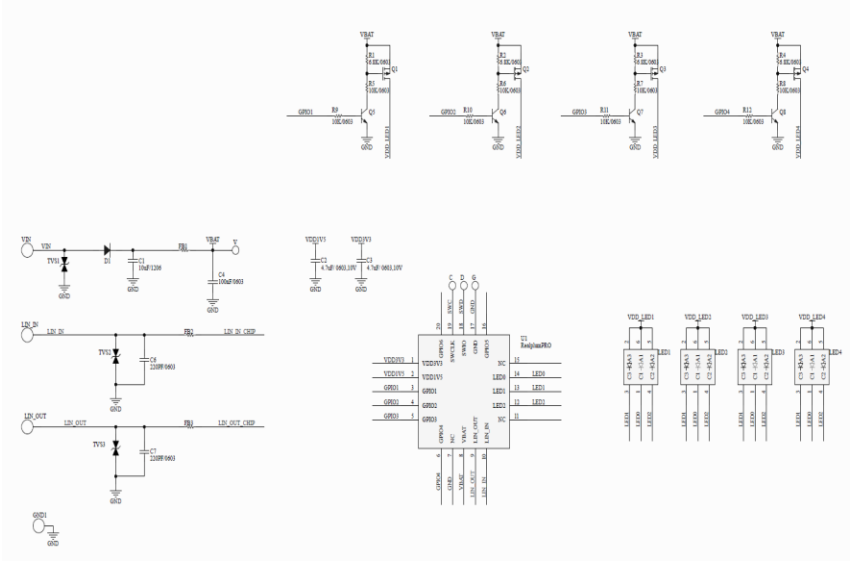
Component Selection

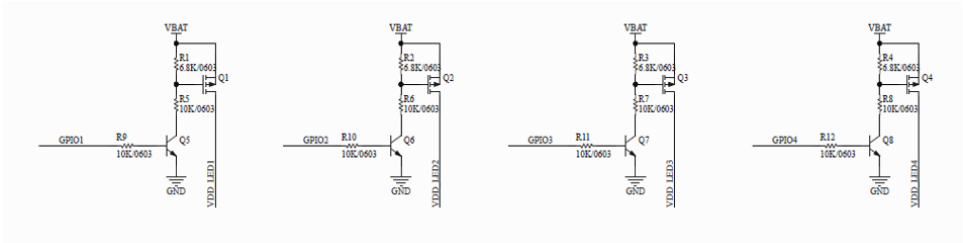
3 Ceramic Capacitor(C1, C2, C3, C4, C5, C6, C7) and ferrite bead(FB1,FB2,FB3)

All these components are used to improve EMC performance. (in layout)

It should be mentioned that the rated current of magnetic bead is larger than the total current in circuit.

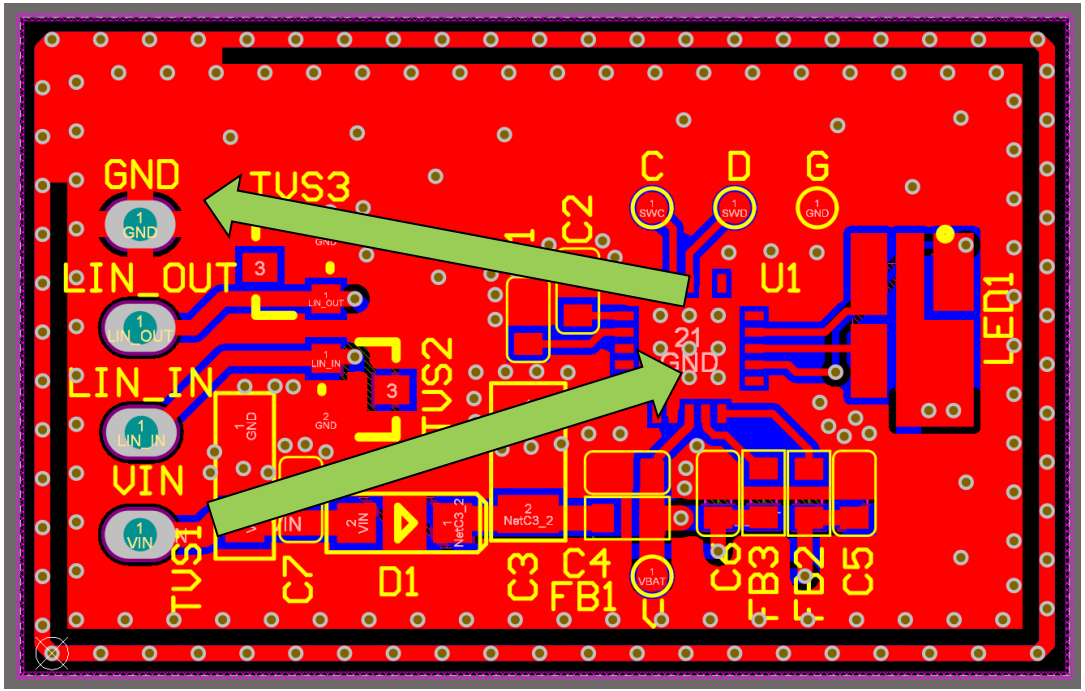
time multiplexing application





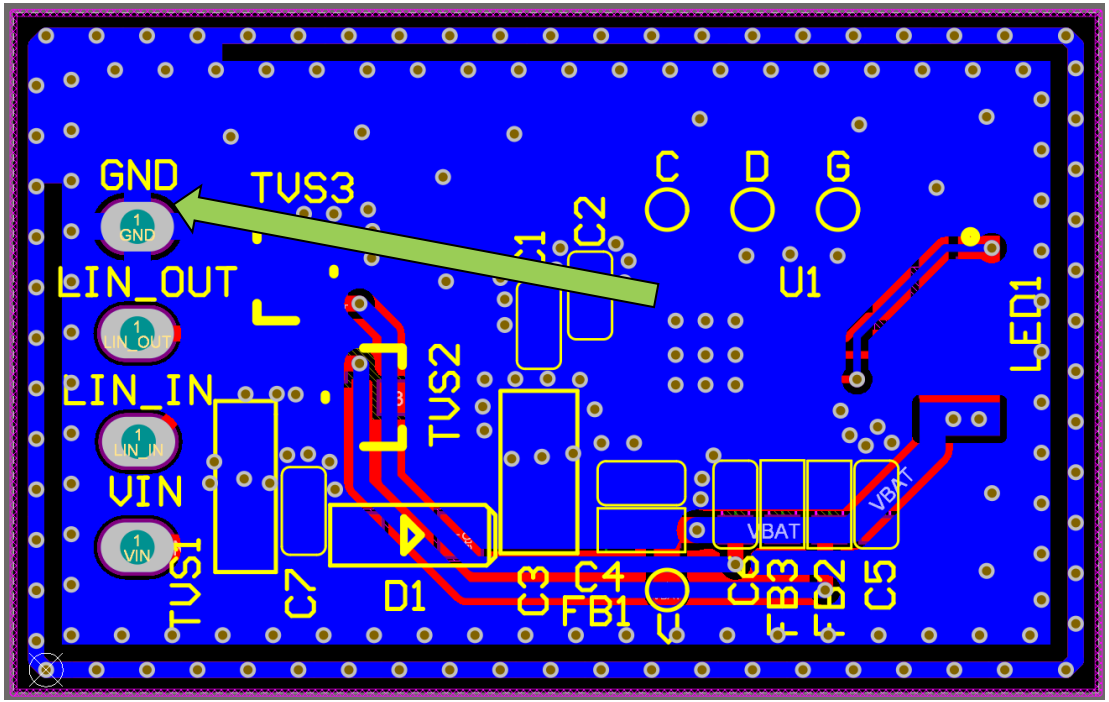
The number of LED should meet the customer’s requirement.

Layout(iND83209)



The major circuit loop area (green arrow) should be as small as possible.

Layout(iND83209)



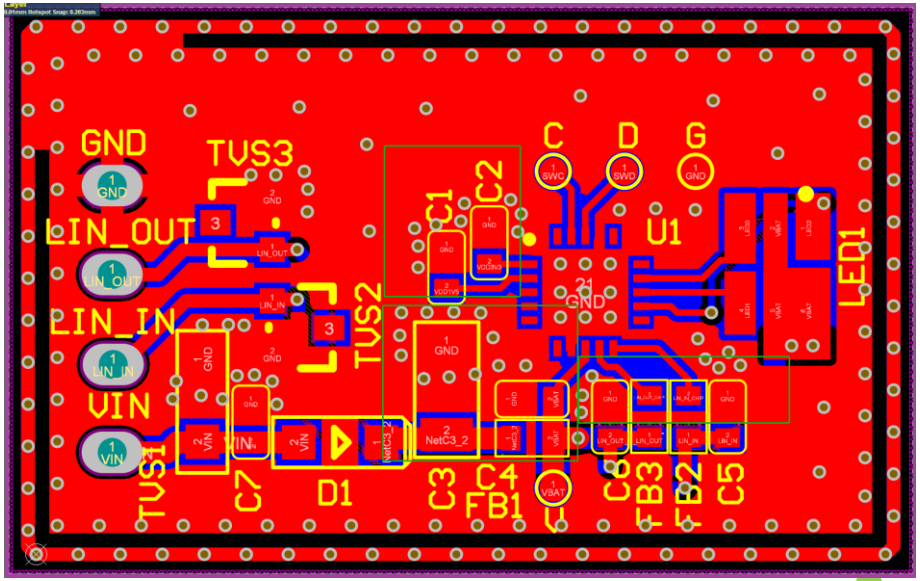
The GND loop from chip GND to connector GND should be short and clear.

Layout(iND83209)

1. All the decoupling capacitor should be set close to the chip. The GND of capacitor directly goes back to chip GND. So, it can filter noise from the chip. Such as C1,C2,C3,C4,C5,C6.

C7 is used to pass BCI test.

2. All the TVS should be put near the connector.

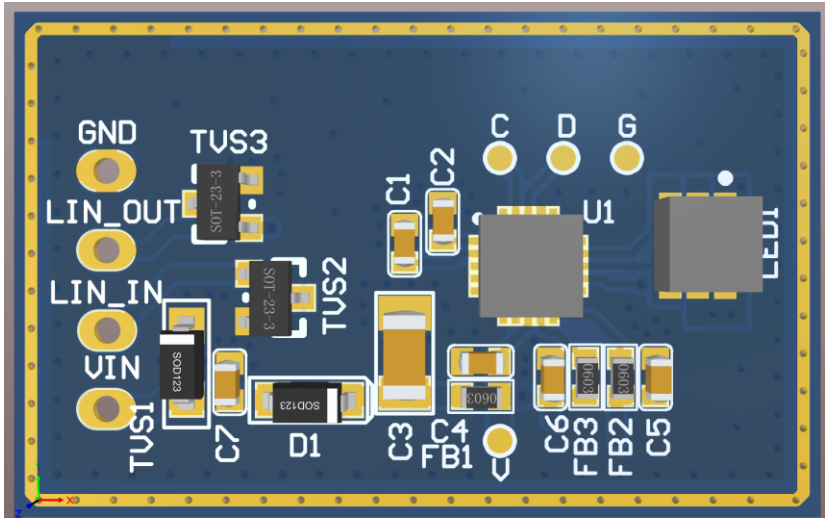


Layout(iND83209)

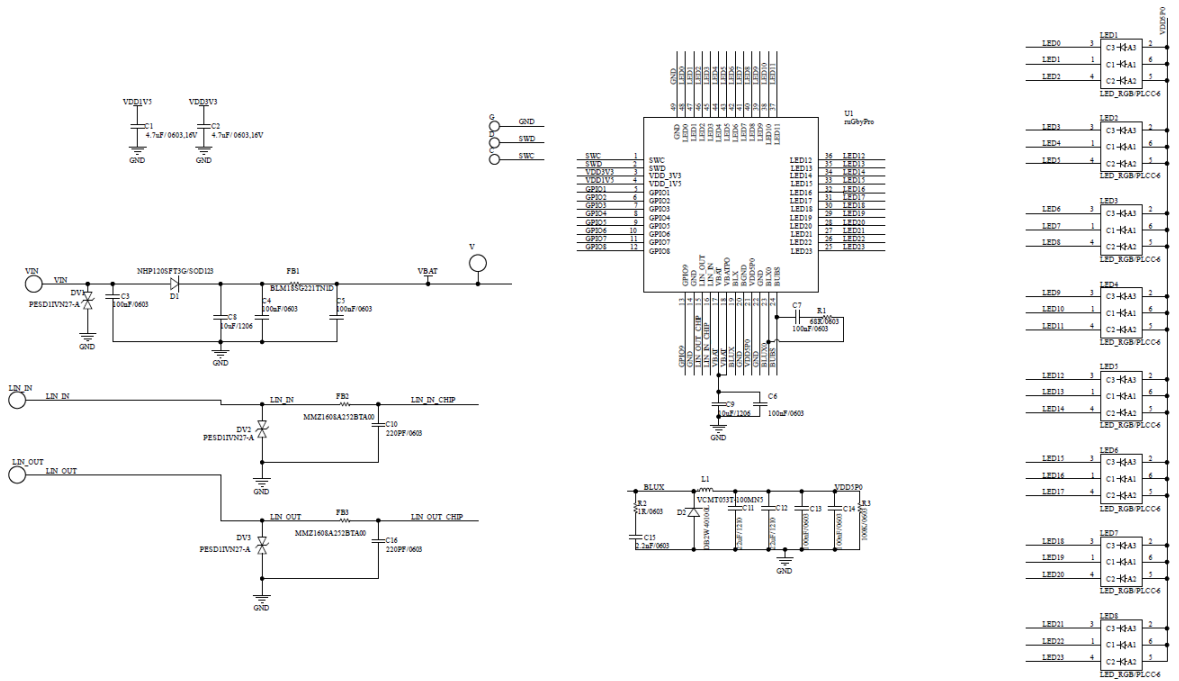
The yellow ring is used to protect chip from electrostatic damage.

It uses independent GND(differ from chip GND).

Only connect with connector GND.



CIRCUIT SCHEMATIC (iND83211)



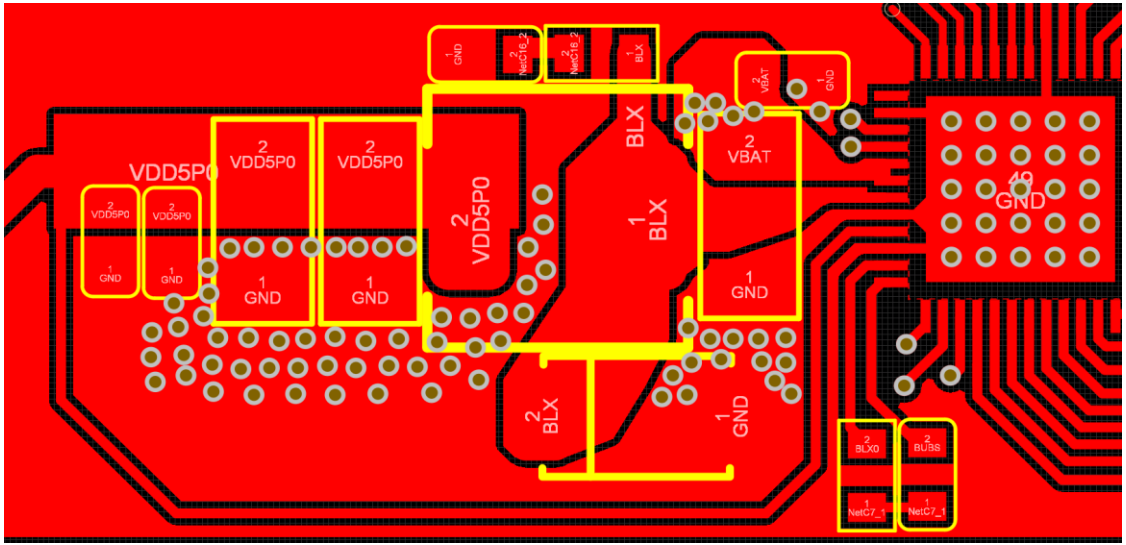
This diagram shows the typical circuit schematic for iND83211.

Do not reduce the recommended components.

Component Selection

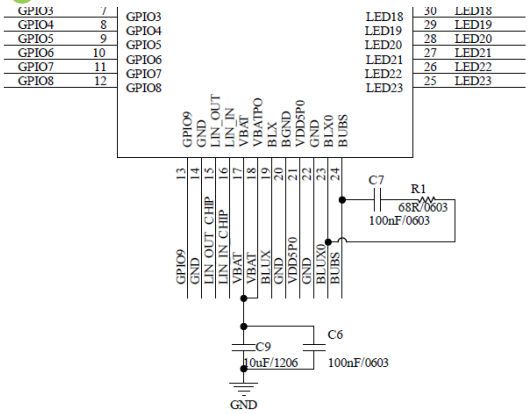
- The requirement of component selection is the same as the one of iND83209.

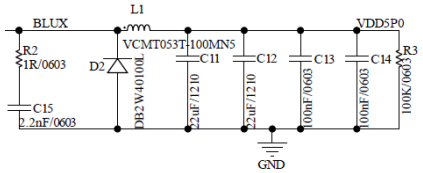
BUCK CIRCUIT LAYOUT

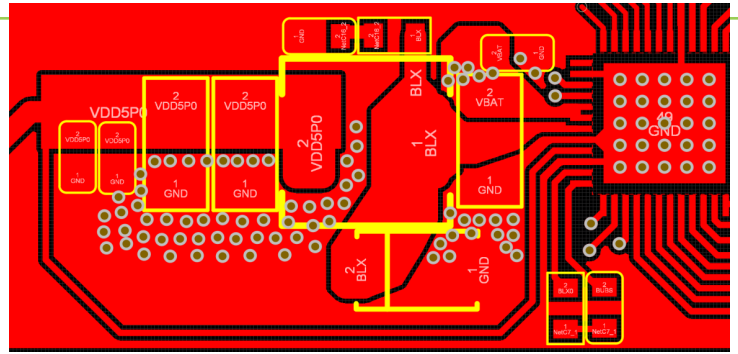


This picture shows the requirements of buck circuit layout.

BUCK CIRCUIT LAYOUT







1.The buck circuit GND should be complete and clear.

2. C9(10uF 1206) should be set near the vbat PIN, the GND of this capacitor is in the buck circuit GND.

3.The GND of Schottky diode(D2) is as close as possible to BGND.

4.The feedback signal line(VDD5P0) should be from the output voltage to the PIN 21.

5.The RC circuit(C7 R1) also need to be separated by GND.

6.Any requirement is intended to improve EMC performance.

Thanks