ICS HW 2

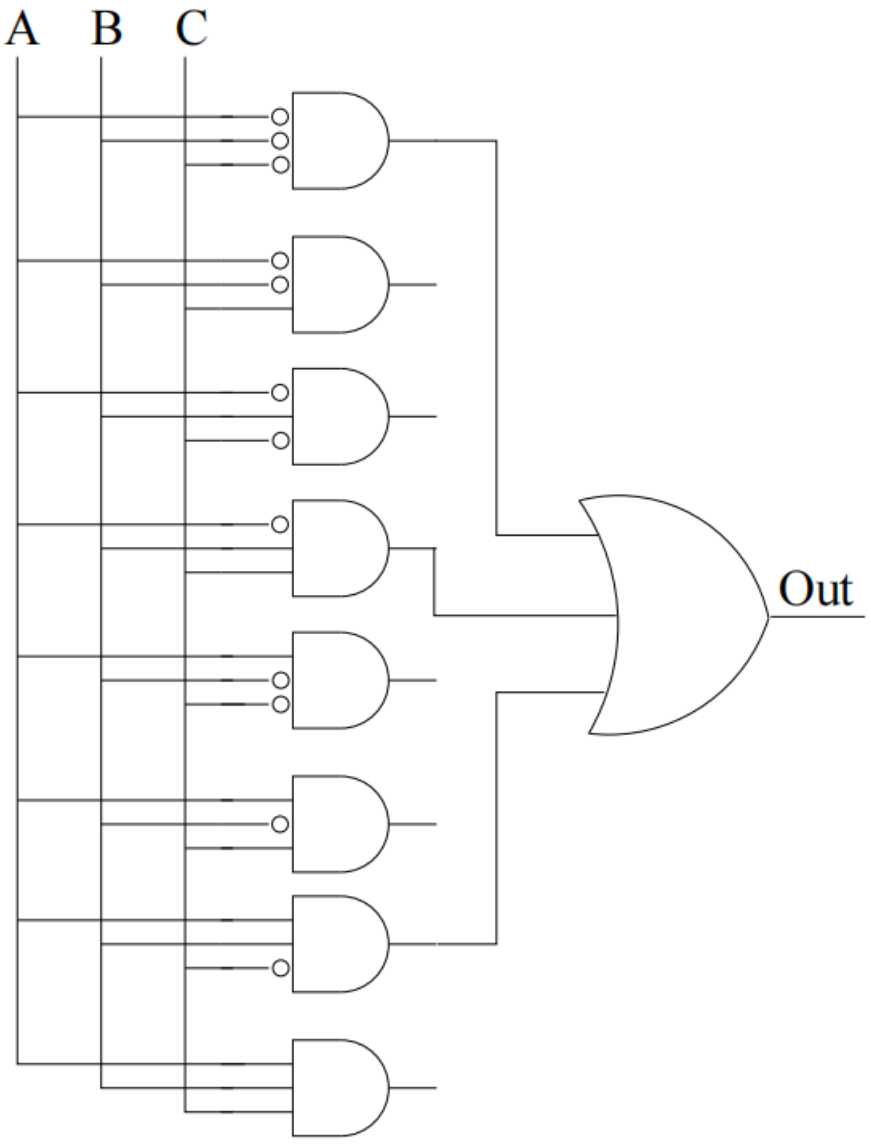
T1

Shown below are several logical identities with one item missing in each. X represents the case where it can be replaced by either a 0 or a 1 and the identity will still hold. Your job: Fill in the blanks with either a 0, 1, or X. For example, in the first place, the missing item is X. That is 0 OR 0 = 0 and 0 OR 1 = 1.

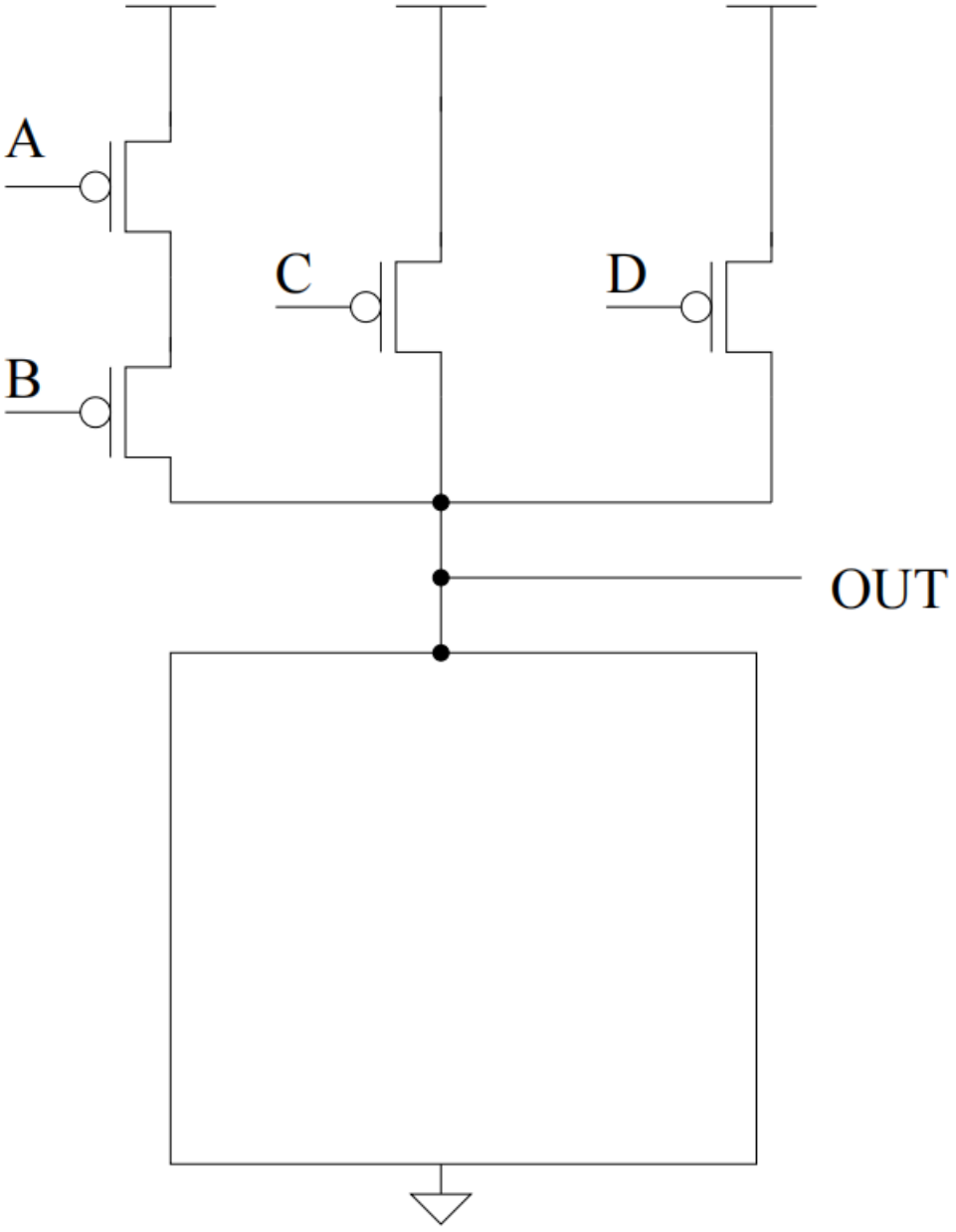
- 0 OR X = __
- 1 OR X = __
- 0 AND X = __
- 1 AND X = __
- __ XOR X = X

T2

1. Construct the output of the truth table for the PLA shown.



2. In the transistor circuit below, all transistors in the path to the power supply are shown. None of the transistors in the path to ground are shown.Please draw the missing transistor circuit in the box.



T3

1. Prove that the NOR gate, by itself, is logically complete (see Section 3.3.5).
2. Please explain why the XOR gate is not logically complete. (Hint: A logically complete set should be able to represent any logical gate. You can prove it by contradiction.)

T4

1. What is the **smallest** positive **normalized** number that can be represented using the IEEE 32-bit Floating Point standard?
2. What is the range of positive **subnormal** number that can be represented using the IEEE 32-bit Floating Point standard?
3. Why does the IEEE 32-bit floating-point standard need subnormal numbers?

4. If both normalized and subnormal numbers are regarded as valid data ranges, is the distribution of the data uniform? If not, what are its distribution characteristics?

T5

Design a **XOR** gate with NAND gates.

a	b	a XOR b
0	0	0
0	1	1
1	0	1
1	1	0

T6

For the memory shown in Figure 3.45:

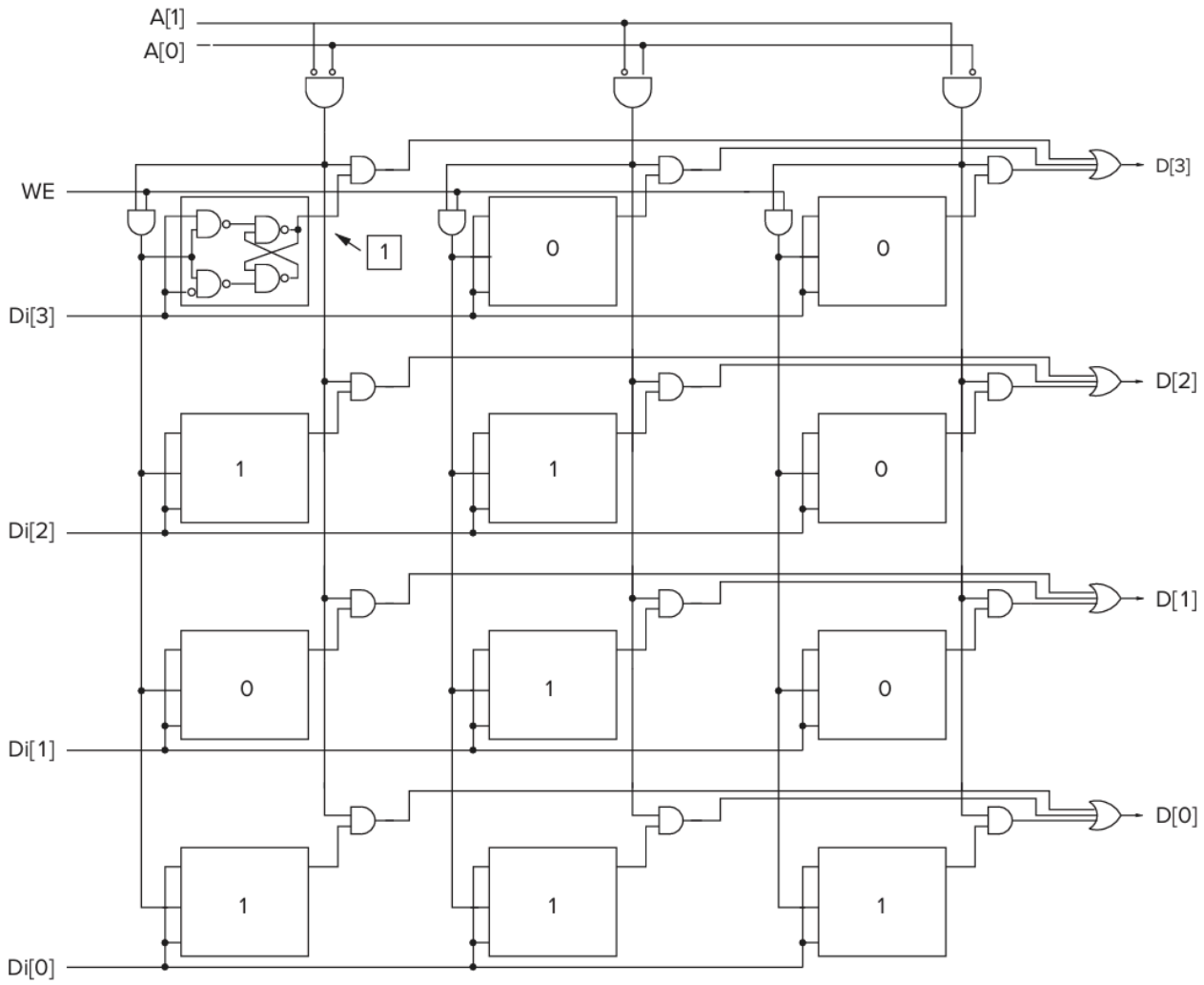


Figure 3.45 Diagram for Exercise 3.40.

1. To write data into the first memory location, what must the values of A[1:0] and WE be?

2. What is the address space? What is the addressability? What are these values respectively in the figure?
3. To increase the addressability of the memory to k(k>4),please describe in text what you should change.

T7

Suppose a 32-bit instruction takes the following format:

If there are 48 opcodes and 28 registers, what is the range of values that can be represented by the immediate (IMM)? Assume IMM is a 2's complement value.

T8

1. Briefly describe the main components of the von Neumann model.
2. Describe the core idea of the von Neumann model and conduct a simple investigation to explain why quantum computers cannot directly apply the von Neumann model.

T9

A logic circuit consisting of 6 gated D latches and 1 inverter is shown below:

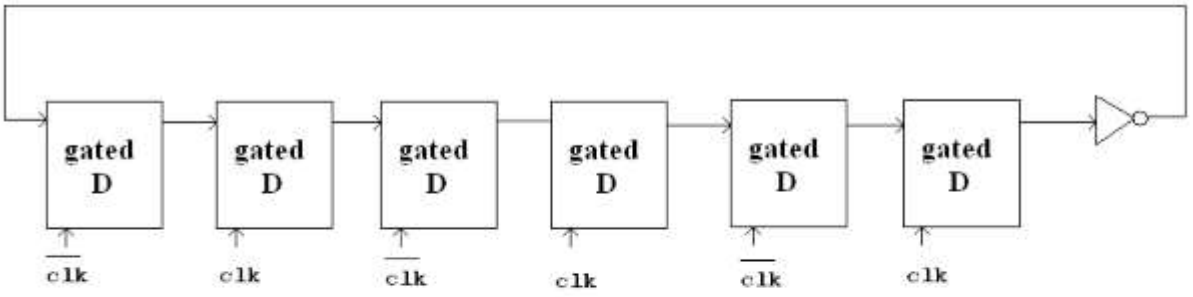
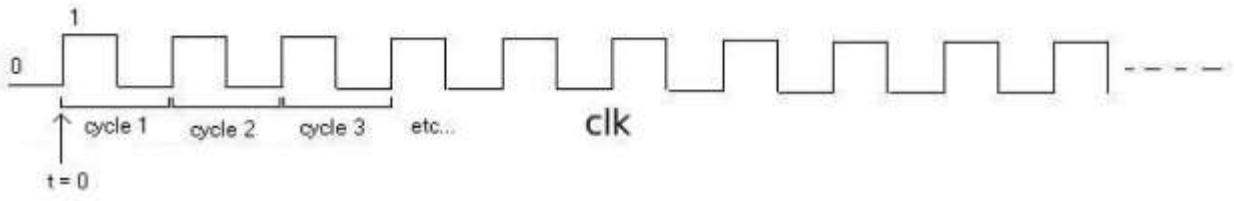


Figure 5



Let the state of the circuit be defined by the state of the 6 D latches. Assume initially the state is 000000 and clk starts at the point labeled t0.

1. What is the state after 77 cycles ?
2. How many different states can occur in total?
3. If records are made after each cycle ends, how many different states are there?
4. How many cycles does it take for a specific state to show up again?

T10

A certain vending machine only sells one type of beverage, priced at 8 yuan.

The machine only accepts two types of coins: 1 yuan, 5 yuan.

When the total amount of coins inserted reaches or exceeds 8 yuan, the goods will be automatically dispatched.

Please design a finite state Machine (FSM) to describe the state transition process of the remaining amount in this vending machine.

T11

There are eight bottles of wine on the table, and one of them has been poisoned. There are now four mice available for poison testing. The poison takes effect very quickly - as long as it is drunk, the mouse will die that very night.

1. Please design a strategy to determine which bottle of wine is poisonous based on the death situation of the mice.
2. In your strategy, the maximum number of bottles of wine that four mice can detect is that one is poisonous.
3. How many mice do you expect to die in your strategy? Could you modify the strategy to reduce the expected number of dead mice even more?