OS Lab7 Caching

1. Basic requirements (60)

   In this Lab, you are required to write a direct mapped cache simulator. The constraints are as follows:

   a) The cacheable memory size is 256Mbytes (address size in main memory)
   b) The cache size is 1k bytes (total cache size)
   c) Each cache line can store 16 bytes (the size of each cache line)
   d) Initially, all cache lines are invalid

   The system input will be up to 100 lines. Each line is either an address in Hexadecimal form or a word "END" (without quotes). You are required to print Miss or Hit after each address input. And when you get the input "END", print the total hit ratio.

   Output format:

   If the result is miss, print "Miss" (without quotes), otherwise, print "Hit" (without quotes)

   When you need to print hit ratio, print it as "Hit ratio = xx.xx%" (without quotes). Please remember, your result should be rounded up to 2 the decimal places.

   Reminder: Do not print any characters the output format does not mention.

   Example Input:

   ```
   BCDE000
   00010B2
   00010BA
   END
   ```

   Output:

   ```
   Miss
   Miss
   Hit
   Hit ratio = 33.33%
   ```

   If you failed on even one of the system tests, you will only get 30 points at most! (Base on your code quality)

2. Lab report(40)

   a) Write the report carefully and concretely. (20)
   b) We will not give you any test case except the example. You are required to construct at least two test cases (Each test case should contain at least two hits and two misses), you should take screenshot of your result and show why your program works (or not). (20) [If you failed on system test, this two test cases will still give you points when they are right.]