library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--use IEEE.NUMERIC\_STD.ALL;

-- Uncomment the following library declaration if instantiating

-- any Xilinx primitives in this code.

--library UNISIM;

--use UNISIM.VComponents.all;

entity serial is

port(

serialdata: in std\_logic;

clk: in std\_logic;

csn,wrn,rdn: in std\_logic;

addr: in std\_logic\_vector(1 downto 0);

data: inout std\_logic\_vector(7 downto 0);

intn: out std\_logic;

perr,oerr,buff:inout std\_logic);

end serial;

architecture Behavioral of serial is

component ctrl is

port(

d9,d11:in std\_logic;

sq0,sq1: in std\_logic;

rq:in std\_logic\_vector(7 downto 0);

clrn:inout std\_logic;

start:out std\_logic;

serial,clk:in std\_logic;

csn,wrn,rdn:in std\_logic;

addr:in std\_logic\_vector(1 downto 0);

data: inout std\_logic\_vector(7 downto 0);

intn: out std\_logic;

perr,oerr,buff:inout std\_logic);

end component;

component decode4 is --元件声明

port(

d:in std\_logic\_vector(3 downto 0);

enable:in std\_logic;

q8,q9,q11:out std\_logic);

end component;

component reg8 is

port(

clrn,clk:in std\_logic;

d:in std\_logic\_vector(7 downto 0);

q:out std\_logic\_vector(7 downto 0));

end component;

component sreg is

port(

clk,clrn,serial:in std\_logic;

q:out std\_logic\_vector(7 downto 0));

end component;

component count4 is

port(

clk:in std\_logic;

clrn: in std\_logic;

q:out std\_logic\_vector(3 downto 0));

end component;

signal c:std\_logic\_vector(3 downto 0);

signal start,t8,t9,t11,clrn:std\_logic;

signal tdata,treg:std\_logic\_vector(7 downto 0);

begin

my\_count4:count4 port map(clk,start,c); --元件例化

my\_decode4:decode4 port map(c,start,t8,t9,t11);

my\_sreg:sreg port map(clk,start,serialdata,tdata);

my\_reg8:reg8 port map(clrn,t8,tdata,treg);

my\_ctrl:ctrl port map(t9,t11,tdata(0),tdata(1),treg,clrn,start,serialdata,clk,csn,wrn,rdn,addr,data,intn,perr,oerr,buff);

end Behavioral;

#PACE: Start of Constraints generated by PACE

#PACE: Start of PACE I/O Pin Assignments

NET "K40" LOC = "P41" ;

NET "K41" LOC = "P40" ;

NET "K42" LOC = "P39" ;

NET "K43" LOC = "P38" ;

NET "K44" LOC = "P36" ;

NET "K47" LOC = "P33" ;

NET "ADDRin(15)" LOC = "P56" ;

NET "ADDRin(14)" LOC = "P55" ;

NET "ADDRin(13)" LOC = "P54" ;

NET "ADDRin(12)" LOC = "P53" ;

NET "ADDRin(11)" LOC = "P50" ;

NET "ADDRin(10)" LOC = "P49" ;

NET "ADDRin(9)" LOC = "P48" ;

NET "ADDRin(8)" LOC = "P47" ;

NET "ADDRin(7)" LOC = "P63" ;

NET "ADDRin(6)" LOC = "P64" ;

NET "ADDRin(5)" LOC = "P65" ;

NET "ADDRin(4)" LOC = "P66" ;

NET "ADDRin(3)" LOC = "P70" ;

NET "ADDRin(2)" LOC = "P71" ;

NET "ADDRin(1)" LOC = "P72" ;

NET "ADDRin(0)" LOC = "P73" ;

NET "DATAin(15)" LOC = "P79" ;

NET "DATAin(14)" LOC = "P80" ;

NET "DATAin(13)" LOC = "P81" ;

NET "DATAin(12)" LOC = "P82" ;

NET "DATAin(11)" LOC = "P84" ;

NET "DATAin(10)" LOC = "P85" ;

NET "DATAin(9)" LOC = "P86" ;

NET "DATAin(8)" LOC = "P87" ;

NET "DATAin(7)" LOC = "P94" ;

NET "DATAin(6)" LOC = "P95" ;

NET "DATAin(5)" LOC = "P96" ;

NET "DATAin(4)" LOC = "P97" ;

NET "DATAin(3)" LOC = "P100" ;

NET "DATAin(2)" LOC = "P101" ;

NET "DATAin(1)" LOC = "P102" ;

NET "DATAin(0)" LOC = "P103" ;

NET "ADDRout(15)" LOC = "P187" ;

NET "ADDRout(14)" LOC = "P205" ;

NET "ADDRout(13)" LOC = "P206" ;

NET "ADDRout(12)" LOC = "P207" ;

NET "ADDRout(11)" LOC = "P208" ;

NET "ADDRout(10)" LOC = "P185" ;

NET "ADDRout(9)" LOC = "P186" ;

NET "ADDRout(8)" LOC = "P176" ;

NET "ADDRout(7)" LOC = "P175" ;

NET "ADDRout(6)" LOC = "P174" ;

NET "ADDRout(5)" LOC = "P173" ;

NET "ADDRout(4)" LOC = "P157" ;

NET "ADDRout(3)" LOC = "P156" ;

NET "ADDRout(2)" LOC = "P155" ;

NET "ADDRout(1)" LOC = "P154" ;

NET "ADDRout(0)" LOC = "P153" ;

NET "MEMdata(15)" LOC = "P192" ;

NET "MEMdata(14)" LOC = "P193" ;

NET "MEMdata(13)" LOC = "P194" ;

NET "MEMdata(12)" LOC = "P195" ;

NET "MEMdata(11)" LOC = "P199" ;

NET "MEMdata(10)" LOC = "P200" ;

NET "MEMdata(9)" LOC = "P201" ;

NET "MEMdata(8)" LOC = "P202" ;

NET "MEMdata(7)" LOC = "P170" ;

NET "MEMdata(6)" LOC = "P169" ;

NET "MEMdata(5)" LOC = "P168" ;

NET "MEMdata(4)" LOC = "P167" ;

NET "MEMdata(3)" LOC = "P163" ;

NET "MEMdata(2)" LOC = "P162" ;

NET "MEMdata(1)" LOC = "P161" ;

NET "MEMdata(0)" LOC = "P160" ;

NET "CSout" LOC = "P159" ;

NET "WRout" LOC = "P171" ;

NET "RDout" LOC = "P188" ;

NET "BHout" LOC = "P189" ;

NET "BLout" LOC = "P191" ;

NET "HDATAout(7)" LOC = "P224" ;

NET "HDATAout(6)" LOC = "P228" ;

NET "HDATAout(5)" LOC = "P229" ;

NET "HDATAout(4)" LOC = "P230" ;

NET "HDATAout(3)" LOC = "P231" ;

NET "HDATAout(2)" LOC = "P232" ;

NET "HDATAout(1)" LOC = "P234" ;

NET "HDATAout(0)" LOC = "P235" ;

NET "LDATAout(7)" LOC = "P215" ;

NET "LDATAout(6)" LOC = "P216" ;

NET "LDATAout(5)" LOC = "P217" ;

NET "LDATAout(4)" LOC = "P218" ;

NET "LDATAout(3)" LOC = "P220" ;

NET "LDATAout(2)" LOC = "P221" ;

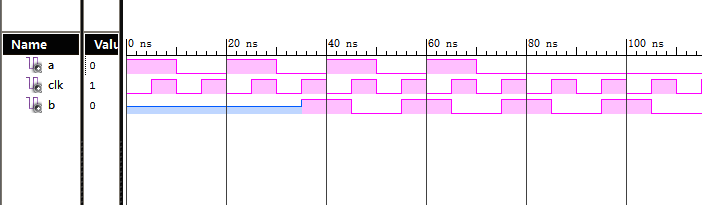
NET "LDATAout(1)" LOC = "P222" ;

NET "LDATAout(0)" LOC = "P223" ;

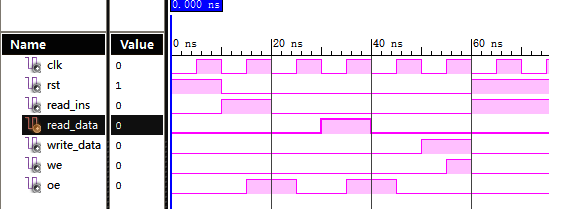
#PACE: Start of PACE Area Constraints

#PACE: Start of PACE Prohibit Constraints

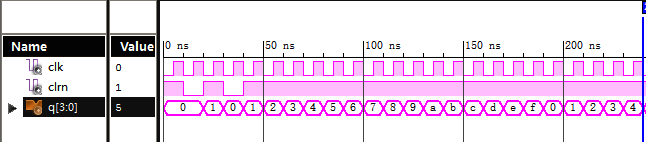
shift4



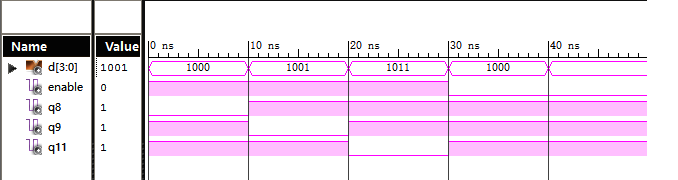
state



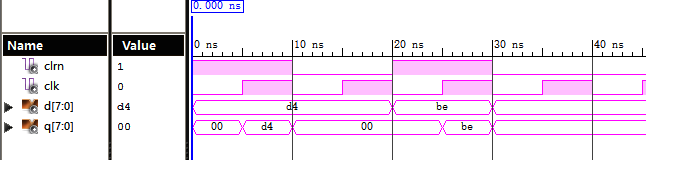
3count4



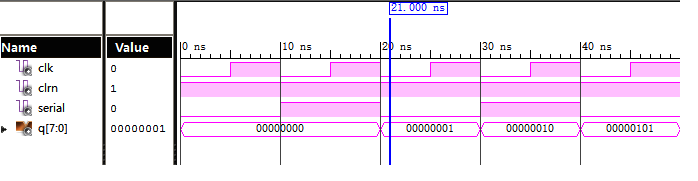
3decode



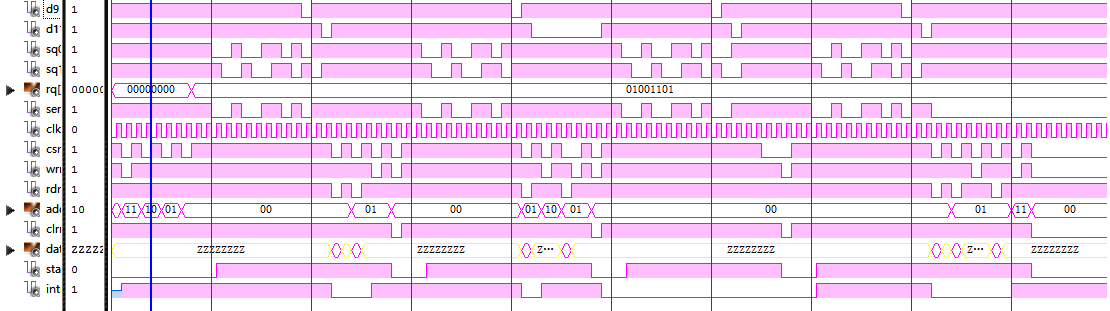
3reg8



3sreg



3ctrl



all

