Inter-Chip Supplement to the USB Revision 3.0 Specification

Revision 1.01

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Revision History

Revision	Issue Date	Comment
1.0	05/03/2012	Version 1.0 release of the supplement.
1.01	02/11/2013	• Clarification in Section 2.5.2 about contiguous nature of RRAP and Response Packet behavior. • Update in Table 2-5 for optional disabling of LUP/LDN and a change in the MPHY.TEST register address space. • Update in Table 3-2 for value of PM_ENTRY_TIMER and a new entry for tPortConfiguration. • Clarification in the implementation note of Section 3.2 regarding TX_ProtDORDY behavior. • Clarification in Section 3.8.2.6 for requirements to exit to the MPHY.TEST state. • Clarifications in Section 5.1.2 for the operational model of a DSP disconnect. • Updates in Section 6 for scope for multi-lane support, addition of Analog Loopback and Tx Compliance modes, clarification of requirements for Receive Burst Testing and a change in the MPHY.TEST register address space. • Update to Section 7.3 for a missing label in the figure.

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1 Introduction

USB is the ubiquitous peripheral-interconnect of choice for a large number of computing and consumer applications. Many systems provide a comprehensive set of software drivers to support commonly available USB peripherals. In addition there is an existing USB ecosystem that includes USB silicon suppliers, design IP houses and verification and testing vendors that lowers the cost for product manufacturers of USB hosts and peripherals.

These advantages have made USB attractive as a chip-to-chip interconnect within a product (without use of cables or connectors). This usage has been validated by the adoption of the High Speed Inter-Chip Supplement [HSIC] in mobile platforms. HSIC leveraged the benefits of High Speed USB while optimizing the link for power, cost and complexity. However the 480 Mbps bandwidth limitation of HSIC poses a limitation for the next generation of applications that require higher bandwidth.

The USB 3.0 specification adds support for transfer speeds of 5 Gbps to address the need for higher bandwidth. However the USB3.0 specification as-is does not meet the requirements of embedded inter-chip interfaces with respect to power and EMI robustness. To address this need, this supplement describes Super Speed Inter-Chip (SSIC) as an optimized inter-chip version of USB3.0.

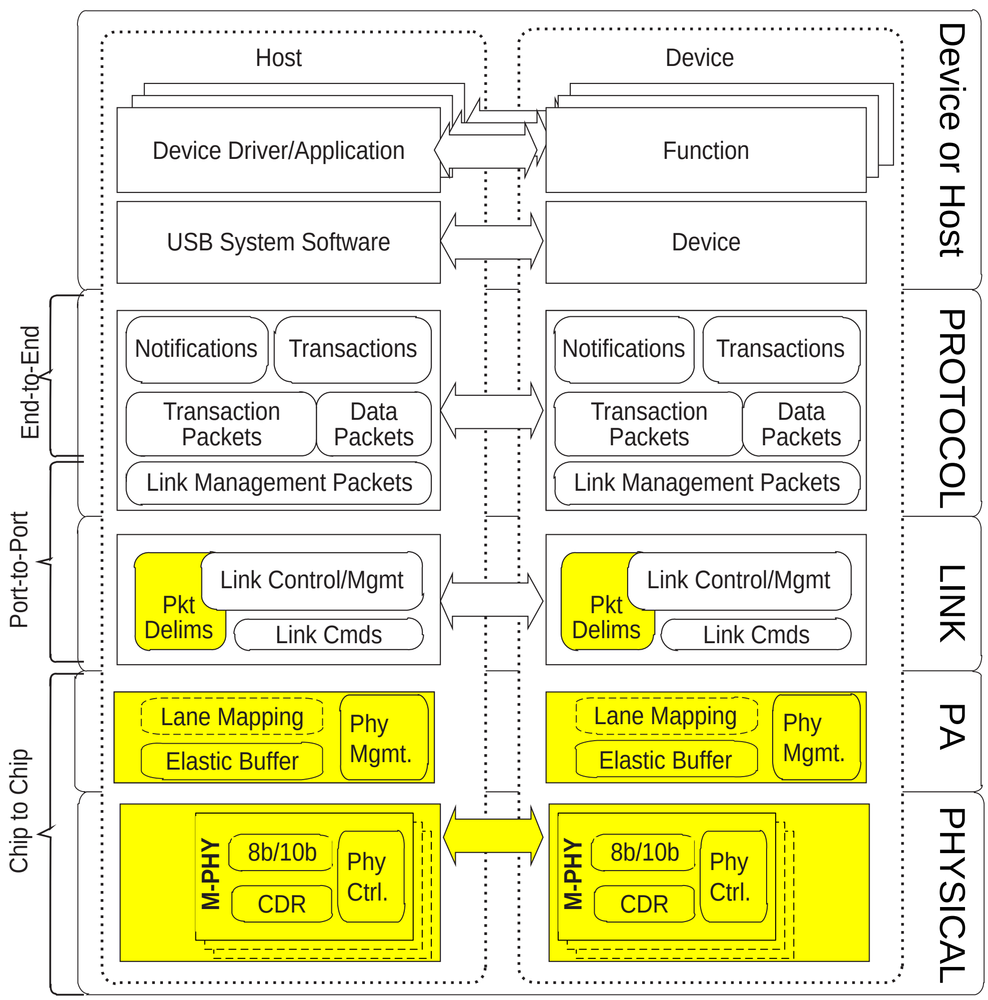


Figure 1-1 SSIC Layers with modifications from [USB3.0] highlighted

As shown in Figure 1-1, SSIC uses the MIPI M-PHY specification as the physical layer of the interconnect to meet the requirements of embedded inter-chip interfaces. The MIPI M-PHY [M-PHY] specification describes a serial physical layer technology with high bandwidth capabilities, which is specifically developed for mobile applications to obtain low pin count combined with very good power efficiency.

1.1 SSIC Significant Features

The following summarizes the key features of SSIC:

- Support for the SuperSpeed protocol only as defined in [USB 3.0]
- Optimized for power, area, cost and EMI robustness for embedded inter-chip interfaces
- Compliant with the Type-I M-PORTs from the MIPI M-PHY specification [M-PHY]
- Support for x1, x2 and x4 LANE configurations.

This supplement only focuses on peripherals that are directly attached to hosts. Support for hubs is not defined and may be achieved in an implementation-specific manner.

1.2 SSIC and Standard SuperSpeed Comparison

SSIC has been designed to replace a standard SuperSpeed Controller and PHY with an implementation that maps the SuperSpeed controller on the MIPI M-PHY. ***This supplement does not specify details of any particular implementation*** and it is intended that SSIC be implementable in multiple ways, depending on what is appropriate for a particular product.

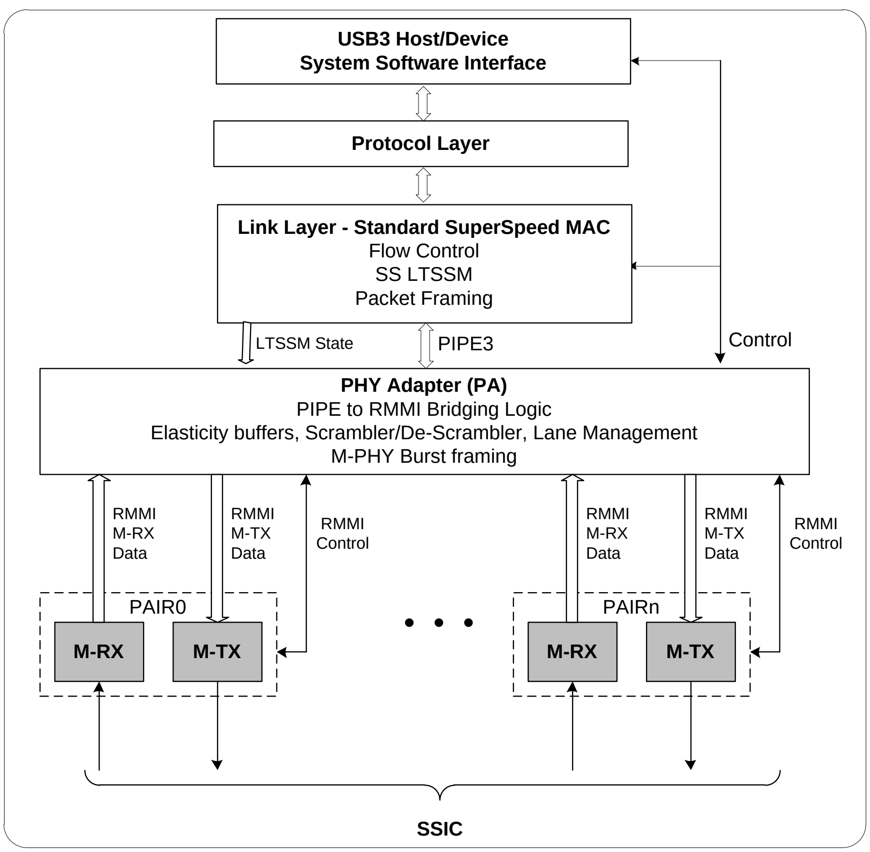


Figure 1-2 Example of an implementation with a PHY Adapter Layer to a Standard SS MAC

Figure 1-2 shows an example of an SSIC implementation that leverages a standard SuperSpeed controller with minimal modifications in the link layer and above. All specifics related to SSIC including bridging logic between the PIPE3 interface of the controller and the Reference M-PHY MODULE

Interface (RMMI) of the M-PHY are contained in the PHY Adapter (PA). In such an implementation, it is necessary for the PHY Adapter to implement whatever mechanisms are needed to allow the controller to operate as if it were connected to a SuperSpeed link, for example by tracking the Link Training Status State Machine (LTSSM) and providing the expected responses on the link. Other alternatives to this example may also be designed that are compliant to this supplement.

1.3 Related Documents

This is not a stand-alone document. It is a supplement to [USB 3.0]. Any aspects of USB which are not specifically changed by this supplement are governed by [USB 3.0].

The following referenced documents can be found on the USB-IF website www.usb.org:

[USB 3.0]	*Universal Serial Bus Revision 3.0 Specification including ECNs*
[HSIC]	*High Speed Inter-Chip USB Electrical Specification including ECNs*

The following referenced documents are published by the MIPI Alliance:

[M-PHY]	*MIPI® Alliance Specification for M-PHY℠ Version 2.0*
[CTS]	*MIPI M-PHY Conformance Test Suite*

1.4 Terminology

“Shall” is normative and used to indicate mandatory requirements which are to be followed strictly in order to conform to this standard.

“Should” is normative and used to indicate a recommended option or possibility.

“May” is normative and used to indicate permitted behavior.

“Can” is informative and used to indicate behavior which is possible or may be seen

The use of “must” and “will” is deprecated for requirements and shall only be used for statements of fact.

1.5 Acronyms and Terms

This section lists and defines terms and abbreviations used throughout this specification.

Acronyms and Terms defined in [USB 3.0] and [M-PHY] are not reproduced here. Except where explicitly noted, when there is a terminology conflict between the [USB 3.0] and [M-PHY] specifications, the [USB 3.0] definition is used in this document.

Acronym/Term	Description
DSP	DownStream Port (DSP) refers to the port of a host to which a peripheral is connected.

Link	Refers to the Link Layer as defined in [USB 3.0]. To be distinguished from "M-PHY LINK".
M-PHY LINK	Refers to LINK as defined in [M-PHY] .
PA	PHY Adapter (PA). Term that refers to logic that interfaces the link layer with the M-PHY.
PAIR	A PAIR consists of a LANE in the downstream SUB-LINK and a counterpart LANE in the upstream SUB-LINK.
RRAP	Remote Register Access Protocol (RRAP) is used while in the PWM-BURST LS-MODE of operation.
SSIC	SuperSpeed Inter-Chip.
USP	UpStream Port (USP) refers to the port that a peripheral uses to connect to a host.

2 Adaptation of M-PHY for the Physical Layer

This document references the MIPI M-PHY [M-PHY] specification for the definition of the physical layer. This section includes an overview of the relevant M-PHY features, defines required M-PHY capabilities and describes functionality while in the [M-PHY] LS-MODE of operation.

2.1 M-PHY for SSIC Overview

The following summarizes relevant M-PHY features:

- Requirement to implement Type-I M-PHY
- Support for PWM-G1 and HS-G1/G2/G3 BURST mode operation
- SSIC profile definitions to aid in inter-operability of M-PHYs in SSIC implementations
- M-PHY SAVE states mapped appropriately to SuperSpeed link states
- Compliant to M-PHY Symbol coding (8b10b) engine for spectral conditioning and clock recovery
- Ability to operate with shared and non-shared reference clocks.

2.1.1 M-PHY Architecture and the Definition of PAIRs

The architecture of the M-PHY is defined in terms of LANEs, SUB-LINKs and LINKs. The M-PHY LINK shall comply with the following:

- The two SUB-LINKs of an SSIC implementation shall support the same number of LANEs.
- All LANEs in the M-PHY LINK shall enter and exit HIBERN8 simultaneously.

In addition this supplement defines the concept of a PAIR.

A LANE in the downstream SUB-LINK and a counterpart LANE in the upstream SUB-LINK are together referred to as a PAIR. A multi-LANE implementation consists of multiple PAIRs and shall have a specific PAIR be statically pre-determined as PAIR0. A single-LANE implementation shall consist of only one PAIR which shall be PAIR0.

2.2 M-PHY MODULE Capabilities

The M-PHY specification defines capability, configuration and status attributes for an M-TX and for an M-RX MODULE. Capability attributes describe the capability of M-PHY MODULEs and may vary depending on the implementation.

To aid in the inter-operability of devices, this document defines profiles within which specific M-PHY Capabilities are mandated.

2.2.1 Profile Definitions

Profiles are indicated by jointly specifying the speed, the multi-LANE capabilities and the rate series such as:

SSIC-G*gr*-L*l* where

- *g* = 1, 2 or 3 and indicates the specific HS-GEAR that the M-PHY LINK operates in
- *r* = A or B and indicates the Rate Series that the M-PHY LINK operates in
- *l* = 1, 2 or 4 and indicates the number of LANEs active in each SUB-LINK (See Section 2.2.2)

All lanes in an implementation shall only operate at the HS-GEAR that corresponds to the profile that is supported. An implementation is permitted to support one or more profiles, however the combination of different profiles supported by a specific implementation are out of scope of this specification. For example: an SSIC-G2A-L1 may or may not choose to support SSIC-G1B-L1.

An implementation of a profile shall support the corresponding speed, multi-LANE and mandated capabilities of the M-TX and M-RX MODULEs as specified in Section 2.2.3.

Certain M-PHY MODULE configurations attributes are chosen not based on the choice of profile or the mandate of this document but instead are based on implementation-specific constraints. A complete list of such parameters is specified in Section 2.3.

2.2.2 Multi-LANE Capabilities

An implementation may choose to feature one (x1), two (x2) or four (x4) LANEs in each SUB-LINK.

The HS-TX LANE-to-LANE skew shall be established by the receipt of a MK0 symbol at the start of a HS-Burst. Receivers shall accept LANE-to-LANE skew up to the allowed limit.

For multi-LANE M-PHY LINKs, Table 2-1 specifies the required timing parameters.

Table 2-1 Multi-LANE Parameters

Symbol	Parameter	Value	Comments
$T_{L2L\_SKEW\_HS\_TX}$	Permitted skew between any two LANEs measured at the M-TX's pins	1300ps	To be measured by the receipt of MK0 at the start of a HS-BURST and as defined in Section 5.1.2.4 of [M-PHY]
$T_{L2L\_SKEW\_HS\_RX}$	Permitted skew between any two LANEs measured at the receiver's pins	4000ps	

2.2.3 M-TX and M-RX Capabilities

An implementation shall ensure that the local and remote M-PORTs are configured to the selected profile. M-PORTs are required to support the M-TX and M-RX capabilities required in this section.

Table 2-2 and Table 2-3 define the set of capabilities that are mandated for M-TX and M-RX MODULEs respectively. The tables list attributes for which this supplement imposes specific requirements. Attributes defined by [M-PHY] which are not specified by this supplement may be set to implementation-specific values.

Table 2-2 M-TX Capability Attributes

Attribute	AttrID	Description	M-PHY range	Required Value
TX_HSMODE_Capability	0x01	Specifies support for HS-MODE.	0=no 1=yes	1
TX_HSGEAR_Capability	0x02	Specifies supported HS-GEARs.	1=HS-G1 2=HS-G1/G2 3=HS-G1/G2/G3	≥1 for SSIC-G1 ≥2 for SSIC-G2 =3 for SSIC-G3
TX_PWMGEAR_Capability	0x04	Specifies support for PWM-GEARs other than PWM-G0.	PWM_G1_ONLY = 1, PWM_G1_TO_G2 = 2, PWM_G1_TO_G3 = 3, PWM_G1_TO_G4 = 4, PWM_G1_TO_G5 = 5, PWM_G1_TO_G6 = 6, PWM_G1_TO_G7 = 7	≥ 1
TX_Amplitude_Capability	0x05	Specifies supported signal amplitude levels.	1=SA 2=LA 3=SA and LA	3 = SA and LA. Both options supported.
TX_ExternalSYNC_Capability	0x06	Specifies support for external SYNC pattern.	0=no 1=yes	≥ 0
TX_HS_Unterminated_LINE_Drive_Capability	0x07	Specifies whether or not M-TX supports driving an unterminated LINE in HS-MODE.	0=no 1=yes	≥ 0
TX_LS_Terminated_LINE_Drive_Capability	0x08	Specifies whether or not M-TX supports driving a terminated LINE in LS-MODE.	0=no 1=yes	≥ 0
TX_Min_SLEEP_NoConfig_Time_Capability	0x09	Specifies minimum time (in SI) in SLEEP state needed when inline configuration was not performed.	1 to 15	≤ 15
TX_Min_STALL_NoConfig_Time_Capability	0x0A	Specifies minimum time (in SI) in STALL state needed when inline configuration was not performed.	1 to 255	≤ 8

Attribute	AttrID	Description	M-PHY range	Required Value
TX_Min_SAVE_Config_Time_Capability	0x0B	Specifies minimum reconfiguration time (in 40 ns steps). This applies only to SLEEP and STALL states.	1 to 250 (10000 ns)	≤ 125 (5000 ns)
TX_REF_CLOCK_SHARED_Capability	0x0C	Specifies support for a shared reference Clock.	0 = no 1 = yes	≥ 0
TX_PHY_MajorMinor_Release_Capability	0x0D	Specifies the major and minor numbers of the M-PHY version supported by the M-TX.	Major version 0 to 9 Minor version 0 to 9	Based on M-PHY Spec Rev in Section 1.3
TX_PHY_Editorial_Release_Capability	0x0E	Specifies the sequence number of the M-PHY version supported by the M-TX.	1 to 99	Based on M-PHY Spec Rev in Section 1.3
TX_Hibern8Time_Capability	0x0F	Specifies minimum time (in 100 µs steps) in HIBERN8 state.	1 to 128 (100 µs to 12.8 ms)	1 (100 µs)

Table 2-3 M-RX Capability Attributes

Attribute	AttrID	Description	M-PHY Range	Required Value
RX_HSMODE_Capability	0x81	Specifies support for HS-MODE.	0=no 1=yes	1=yes
RX_HSGEAR_Capability	0x82	Specifies supported HS-GEARs.	1=HS-G1 2=HS-G1/G2 3=HS-G1/G2/G3	≥1 for SSIC-G1 ≥2 for SSIC-G2 =3 for SSIC-G3
RX_PWMGEAR_Capability	0x84	Specifies support for PWM-GEARs other than PWM-G0.	PWM_G1_ONLY = 1, PWM_G1_TO_G2 = 2, PWM_G1_TO_G3 = 3, PWM_G1_TO_G4 = 4, PWM_G1_TO_G5 = 5, PWM_G1_TO_G6 = 6, PWM_G1_TO_G7 = 7	≥ 1
RX_HS_Unterminated_Capability	0x85	Specifies support for disconnection of resistive termination in HS-MODE.	0=no 1=yes	0 = no for all profiles
RX_LS_Terminated_LINE_Drive_Capability	0x86	Specifies support for enabling resistive termination in LS-MODE.	0=no 1=yes	≥ 0

Attribute	AttrID	Description	M-PHY Range	Required Value
RX_Min_SLEEP_NoConfig_Time_Capability	0x87	Specifies minimum time (in SI) in SLEEP state needed when inline configuration was not performed.	1 to 15	≤ 15
RX_Min_STALL_NoConfig_Time_Capability	0x88	Specifies minimum time (in SI) in STALL state needed when inline configuration was not performed.	1 to 255	≤ 8 *Please see **Note 1.***
RX_Min_SAVE_Config_Time_Capability	0x89	Specifies minimum reconfiguration time (in 40 ns steps). This applies only to SLEEP and STALL states.	1 to 250 (10000 ns)	≤ 125 (5000 ns)
RX_REF_CLOCK_SHARED_Capability	0x8A	Specifies support for a shared reference Clock.	0=no 1=yes	≥ 0
RX_HS_G1_SYNC_LENGTH_Capability	0x8B	HS-G1 Synchronization pattern length in SI.	{Sync range, Sync Length}	≤ {1,4}
RX_HS_G1_PREPARE_LENGTH_Capability	0x8C	HS-G1 prepare length multiplier for M-RX	0 to 15	≤ 4
RX_LS_PREPARE_LENGTH_Capability	0x8D	PWM-BURST or SYS-BURST PREPARE length multiplier for M-RX.	0 to 15	≤ 8
RX_PWM_Burst_Closure_Length_Capability	0x8E	Specifies minimum burst closure time (in SI) necessary to guarantee complete data processing inside M-RX.	0 to 31	≤ 7
RX_Min_ActivateTime_Capability	0x8F	Specifies minimum activate time needed in 100us steps	1 to 9	1
RX_PHY_MajorMinor_Release_Capability	0x90	Specifies the major and minor numbers of the M-PHY version supported by the M-RX.	Major version 0 to 9 Minor version 0 to 9	Based on M-PHY Spec Rev in Section 1.3
RX_PHY_Editorial_Release_Capability	0x91	Specifies the sequence number of the M-PHY version supported by the M-RX.	1 to 99	Based on M-PHY Spec Rev in Section 1.3
RX_Hibern8Time_Capability	0x92	Specifies minimum time (in 100 μs steps) in HIBERN8 state.	1 to 128 (100 μs to 12.8 ms)	1 (100 μs)

Attribute	AttrID	Description	M-PHY Range	Required Value
RX_HS_G2_SYNC_LENGTH_Capability	0x94	HS-G2 Synchronization pattern length in SI.	{Sync range, Sync Length}	≤ {1,5}
RX_HS_G3_SYNC_LENGTH_Capability	0x95	HS-G3 Synchronization pattern length in SI.	{Sync range, Sync Length}	≤ {1,6}
RX_HS_G2_PREPARE_LENGTH_Capability	0x96	HS-G2 prepare length multiplier for M-RX	0 to 15	≤ 4
RX_HS_G3_PREPARE_LENGTH_Capability	0x97	HS-G3 prepare length multiplier for M-RX	0 to 15	≤ 4

Note 1*: [M-PHY] requires an RMMI based M-RX to output at least two cycles of RX_SymbolClk after the end of a HS-BURST. An M-RX cannot exit STALL to start a new HS-BURST until after it has output two cycles of RX_SymbolClk from the previous HS-BURST. Depending on the width of RX_Symbol (ie 10/20/40 bits), two cycles of RX_SymbolClk may be either 2, 4 or 8 SIs. For an RX_Symbol width of 40 bits, the M-RX needs to remain in stall for at least 8 SIs before the start of the next burst.*

2.3 M-PHY Configuration Attributes

As noted in Annex D.2 in [M-PHY] , M-TX Configuration attributes shall be set appropriately to match the corresponding M-RX capability attribute values.   Depending on the profile supported by the implementation, default values for the configuration attributes for the M-TX and M-RX MODULE shall be suitably chosen and configured by implementations. Optimizations to the default values for the configuration attributes may be applied in an implementation-specific manner. For more details on the configuration attributes please refer to [M-PHY]

However there are some M-PHY configuration attributes listed in Table 2-4 that are not based on the profile but are instead configured depending on implementation considerations. This section makes note of these implementation-specific configuration parameters. This supplement does not specify recommended values for these parameters and does not mandate a mechanism for configuring and coordinating the values of these parameters across the M-PHY LINK.

Table 2-4 TX Configuration Attributes

Attribute	AttrID	Description	M-PHY range	Required Value
TX_HS_SlewRate	0x26	Slew Rate control of M-TX output driver.	0 to 255	Depending on implementation.
TX_DRIVER_POLARITY	0x2F	M-TX output driver polarity.	NORMAL = 0, INVERTED = 1	Depending on implementation.

2.4 M-PHY State Machine

This supplement is in compliance with the State Machine for Type-I MODULEs as described in Figure 7 for M-TX and Figure 8 for M-RX in [M-PHY] .

However the following is to be noted:

- The LINE-CFG states are not required for SSIC implementations.
- Optical Media Converters are not supported.

Details regarding the mapping of the SSIC Link Training and Status State Machine (LTSSM) on the M-PHY Type-I state machines are provided in Section 3.8.

2.5 LS-MODE Support

The M-TX and M-RX MODULEs enter the LS-MODE of operation following events such as a power-on-reset, a warm reset, a USP disconnect or a DSP disconnect. Section 3.8 includes further details on the link layer conditions for entering LS-MODE.

The only PWM-GEAR that is used in a PWM-BURST is PWM-G1. The Remote Register Access Protocol (RRAP) defined in Section 2.5.2 shall be implemented for data transmission in this mode.

Data transmission in a PWM-BURST shall take place in one of the following scenarios:

- In the Rx.Detect LTSSM state between a USP and a DSP or
- in the MPHY.TEST LTSSM state when the USP or DSP operates as a DUT under the control of external Test Equipment.

The following section details the entry conditions for PWM-BURST in the Rx.Detect state. For details on the entry requirements in the MPHY.TEST state please refer to Section 6.2.

2.5.1 PWM-BURST Entry in Rx.Detect

Upon entering the Rx.Detect LTSSM state and the LS-MODE sub-state as described in Section 3.8.2, a DSP and an USP shall:

- Disable Support for LCCs in the M-TX for all PAIRs.
- Initiate a PWM-BURST as defined in this section.

> ***Implementation Note:***
>
> *As per [M-PHY] disabling support for LCC requires configuring a value of “NO = 0” to the LCC_ENABLE Configuration Attribute in the Effective Bank and subsequently asserting the TX_CfgUpdt signal of the M-TX for all PAIRs.*

The DSP shall initiate a PWM-BURST as per [M-PHY] on the M-TX MODULE of PAIR0. The DSP shall then monitor the M-RX of PAIR0 for the USP to initiate a PWM-BURST.

The USP shall initiate a PWM-BURST as per [M-PHY] on the M-TX MODULE of PAIR0 after it detects a PWM-BURST on the M-RX of PAIR0.

In a multi-LANE M-PHY LINK the remaining M-TX MODULEs shall remain in the SLEEP state.

2.5.2 Remote Register Access Protocol (RRAP)

While in the PWM-BURST mode, communication is achieved using the RRAP which consists of the following packet types:

- Write Command
- Write Response
- Read Command
- Read Response

An RRAP Master shall be capable of issuing Command packets while a RRAP Target shall issue response packets.

Write Command

	P	Rsvd							Data								LowerAddr								UpperAddr				Rsvd		0	0
Bit	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Byte	3								2								1								0							

Write Response

	P	Rsvd																													0	1
Bit	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Byte	3								2								1								0							

Read Command

	P	Rsvd															LowerAddr								UpperAddr				Rsvd		1	0
Bit	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Byte	3								2 1								1								0							

Read Response

	P	Rsvd							Data								Rsvd														1	1
Bit	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Byte	3								2								1								0							

Figure 2-1 RRAP Packet Types

The RRAP packets are described in Figure 2-1 along with the following additional requirements:

- "LowerAddr" and "UpperAddr" values are set based on the address map defined in Table 2-5.
- The "Rsvd" fields shall not be used and shall be set to 0.
- The "P" field functions as an odd-parity bit for the entire packet.
- The entire packet is transmitted continuously without intervening symbols.

The following requirements apply to the RRAP:

- When in PWM-BURST mode and not transmitting a RRAP packet, the M-TX MODULEs in SUB-LINKs shall transmit the FLR symbol as per [M-PHY] .
- The RRAP follows the bit and byte ordering rules defined in Section 3.1.
- A DSP shall support RRAP Master functionality. A DSP that supports the optional MPHY.TEST state shall support RRAP Target functionality.

- When in PWM-BURST, a DSP that supports the optional MPHY.TEST state shall always support the receipt of a Write Command to enable a transition to that state.
- A USP shall only support RRAP Target functionality.
- Test Equipment shall function as a RRAP Master with either the DSP or the USP as the Device Under Test (DUT).
- A DSP serving as a RRAP Master shall only send commands and receive responses on PAIR0.
- A DSP or an USP serving as a RRAP Target shall support receiving commands over any PAIRx and shall return a response on the same PAIRx.
- Test Equipment serving as a RRAP Master may send commands and receive responses on any PAIR.
- Upon receiving a Write Command packet, a Target shall transmit the corresponding response packet within tRRAPTargetResponse. This requirement shall apply for any Write Command received including Writes to Reserved Registers and Registers that are identified in Table 2-5 as having no effect.
- Upon receiving a Read Command packet, a Target shall transmit the corresponding response packet within tRRAPTargetResponse.
- If a Master has issued a Command, then the Master shall not retry the Command or issue another Command until either the Target has provided a Response, or after tRRAPInitiatorResponse has elapsed.
- A Target shall map the attributes of all implemented PAIRs to RRAP addresses as defined in Table 2-5.
- A Target shall not send a response until the RRAP Command is fully received with a valid parity.

Implementation Note:

Additional steps to improve the reliability offered by a single parity bit may be taken at the RRAP level using implementation specific means such as redundant write commands or performing reads after writes to ensure the correctness of operations.

Table 2-5 RRAP Address Map

UpperAddr	LowerAddr	Register Name	Description
0x0	0x00-0xFF	As defined in [M-PHY]	Capability, configuration and status attributes for PAIR0. Writes to these registers shall only affect the shadow bank until an RCT is executed. The Target shall provide a Write Response only after the Write Command is completed.
0x1	0x00-0xFF	As defined in [M-PHY]	Capability, configuration and status attributes for PAIR1. Writes to these registers shall only affect the shadow bank until an RCT is executed. The Target shall provide a Write Response only after the Write Command is completed.
0x2	0x00-0xFF	As defined in [M-PHY]	Capability, configuration and status attributes for PAIR2. Writes to these registers shall only affect the shadow bank until an RCT is executed. The Target shall provide a Write Response only after the Write Command is completed.

UpperAddr	LowerAddr	Register Name	Description
0x3	0x00-0xFF	As defined in [M-PHY]	Capability, configuration and status attributes for PAIR3. Writes to these registers shall only affect the shadow bank until an RCT is executed. The Target shall provide a Write Response only after the Write Command is completed.
0x4	0x00	DSP_DISCONNECT	This Register is used by a DSP following a LINE-RESET to signal a DSP Disconnect. This bit is required only for an USP only. A DSP or a USP in the MPHY.TEST state shall ignore writes to this register. Read/Write Attributes: • R/W Reset Default: • Value on the assertion of M-PHY local RESET: 0x00 Bit [0]: • Writing 1’b1 signals a DSP disconnect as detailed in Section 5.1.2. • Writing 1’b0 shall have no effect. Bit [7:1] Reserved. • Writes shall be ignored and Reads shall return zero values.
0x4	0x01	CONFIGURE_FOR_HS	This Register is used to direct the Target to update its shadow bank for HS-BURST with the settings that correspond to the SSIC profile supported. As noted in Section 2.2.1 this profile is statically determined and this supplement provides no means for selecting between different profiles if so supported. The Target shall provide a Write Response to this Command only after the shadow bank registers are updated. Read/Write Attributes: • R/W Reset Default: • Value on the assertion of M-PHY local RESET: 0x00 Bit [0]: • Writing 1’b1 directs the Target to update its shadow bank with the settings that correspond to its SSIC profile. • Writing 1’b0 shall have no effect.

UpperAddr	LowerAddr	Register Name	Description
			Once the bit is set the action cannot be undone and can only be reset via a LINE-RESET. Bit[7:1] Reserved. • Writes shall be ignored and Reads shall return zero values.
0x4	0x02	BURST_CLOSURE	This Register is used to direct the Target to terminate the PWM-BURST. Read/Write Attributes: • R/W Reset Default: • Value on the assertion of M-PHY local RESET: 0x00 Bit [0]: • Writing 1’b1 terminates the PWM-BURST and initiates an RCT to exit LS-MODE as defined in Section 2.5.3. • Writing 1’b0 shall have no effect. Once the bit is set the action cannot be undone and can only be reset via a LINE-RESET. Bit[7:1] Reserved. • Writes shall be ignored and Reads shall return zero values.
0x4	0x03	DISABLE_SCRAMBLING	This Register is used by a DSP to indicate to an USP that data transmission in HS-MODE shall have scrambling disabled. A DSP or a USP in the MPHY.TEST state shall ignore writes to this register. Read/Write Attributes: • R/W Reset Default: • Value on the assertion of M-PHY local RESET: 0x00 Bit [0]: • Writing 1’b1 configures the USP to disable HS-MODE scrambling. • Writing 1’b0 shall have no effect. Once the bit is set the action cannot be undone and can only be reset via a LINE-RESET.

UpperAddr	LowerAddr	Register Name	Description
			Bit [7:1] Reserved. • Writes shall be ignored and Reads shall return zero values.
0x4	0x04	DISABLE_STALL_IN_U0	This Register is used by a DSP to disable STALL entry in U0 in an USP. A DSP or a USP in the MPHY.TEST state shall ignore writes to this register. Read/Write Attributes: • R/W Reset Default: • Value on the assertion of M-PHY local RESET: 0x00 Bit [0]: • Writing 1’b1 configures the USP to disable STALL entry while in U0. • Writing 1’b0 shall have no effect. Once the bit is set the action cannot be undone and can only be reset via a LINE-RESET. Bit [7:1] Reserved. • Writes shall be ignored and Reads shall return zero values.
0x4	0x05	DISABLE_LUP_LDN	This optional Register is used by a DSP to disable the use of the LDN and LUP Link Commands defined in [USB 3.0] to allow additional power optimizations in the M-TX. Read/Write Attributes: • R/W Reset Default: • Value on the assertion of M-PHY local RESET: 0x00 Bit [0]: • Writing 1’b1 configures the USP to disable LUP/LDN commands. In addition, the USP shall not flag a tU0LTimeout Error or transition to Recovery upon detecting a missing LUP or LDN. • A DSP that generates a RRAP command to set this bit shall not transmit any LUP and LDN link commands. In addition, the DSP shall not flag a tU0LTimeout Error or transition to Recovery upon detecting a missing LUP or LDN.

UpperAddr	LowerAddr	Register Name	Description
			• Writing 1’b0 shall have no effect. Once the bit is set the action cannot be undone and can only be reset via a LINE-RESET. Bit [7:1] Reserved. • Writes shall be ignored and Reads shall return zero values.
0x4	0x06-0xFE	RESERVED	Reserved. Writes shall be ignored and Reads shall return zero values.
0x4	0xFF	TEST_MODE	This Register is used by Test Equipment to configure a Target in the MPHY.TEST state. The Target shall complete its configuration to the MPHY.TEST state prior to issuing a Write Response to the command. Read/Write Attributes: • R/W Reset Default: • Value on the assertion of M-PHY local RESET: 0x00 Bit [0]: • Writing 1’b1 configures the RRAP Target in the MPHY.TEST state. • Writing 1’b0 shall have no effect. Once the bit is set the action cannot be undone and can only be reset via a LINE-RESET. Bit [7:1] Reserved. • Writes shall be ignored and Reads shall return zero values.

<table>
<tr><th>UpperAddr</th><th>LowerAddr</th><th>Register Name</th><th>Description</th></tr>
<tr><td>0x5</td><td>0x00</td><td>PAIR_CAPABILITY</td><td>This Register is used by a Master to determine the number PAIRs supported by a Target.
Read/Write Attributes:
• RO
• Writes to this register shall be ignored.
Reset Default:
• Implementation-specific.
Bit [0]:
• A read of this field shall always return a value of 1’b1
Bit [1]:
• A read of this field shall return a value of 1’b1 if PAIR0 and PAIR1 are supported.
Bit [2]:
• A read of this field shall return a value of 1’b1 if PAIR0, PAIR1, PAIR2 and PAIR3 are supported.
Bit [7:3] Reserved.
• Reads shall return zero values.</td></tr>
<tr><td>0x5</td><td>0x01- 0xFF</td><td>RESERVED</td><td>Reserved. Writes shall be ignored and Reads shall return zero values.</td></tr>
<tr><td>0x6-0xD</td><td>0x00-0xFF</td><td>RESERVED</td><td>Reserved. Writes shall be ignored and Reads shall return zero values.</td></tr>
<tr><td>0xE</td><td>0x00-0xFF</td><td>MPHY.TEST Registers</td><td>Refer to Section 6.</td></tr>
<tr><td>0xF</td><td>0x00-0xFF</td><td>VENDOR-SPECIFIC REGISTERS</td><td>Registers in this address space are not defined in this specification and are reserved to implement vendor-specific functionality.</td></tr>
</table>

2.5.3 PWM-BURST Closure

PWM-BURST closure shall be implemented in the following manner:

- The Master shall set BURST_CLOSURE[0] register in the Target.
- Upon the receipt of a Write Response with a valid parity from the Target, the Master shall end the PWM-BURST on its M-TX.
- On detecting the closure of the PWM-BURST on its M-RX, the RRAP Target shall end the PWM-BURST on its M-TX.

After the closure of the PWM-BURST, the conditions for a Re-Configuration Trigger (RCT) as defined in [M-PHY] shall be met upon which the Effective bank of the Configuration Attributes are updated.

2.5.4 RRAP Timing Parameters

This section defines the timing parameters relevant to the RRAP.

Table 2-6 RRAP Timing Parameters

Name	Description	Min	Max	Units
tRRAPTargetResponse	Time between the receipt of a RRAP command and the transmission of the response by a Target		50	ms
tRRAPInitiatorResponse	Time between the transmission of a RRAP command and the reception of the response by an Initiator		60	ms

3 Link Layer

This chapter specifies the Link layer including:

- Reset signaling
- Bit and byte ordering
- Packet framing
- Logical idle
- SSIC LTSSM and operations
- Scrambling
- Clock Compensation

3.1 Bit and Byte Ordering

Bit ordering shall be big-endian as defined by [M-PHY] and as shown in Figure 3-1.

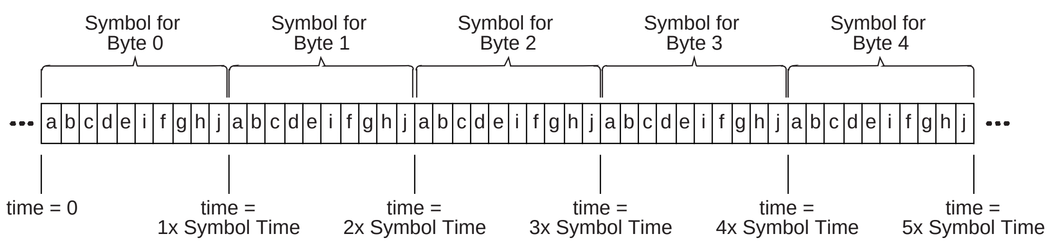


Figure 3-1 Bit Ordering

In a Single-LANE (x1) implementations, all bytes are transmitted in-order as shown in Figure 3-2.

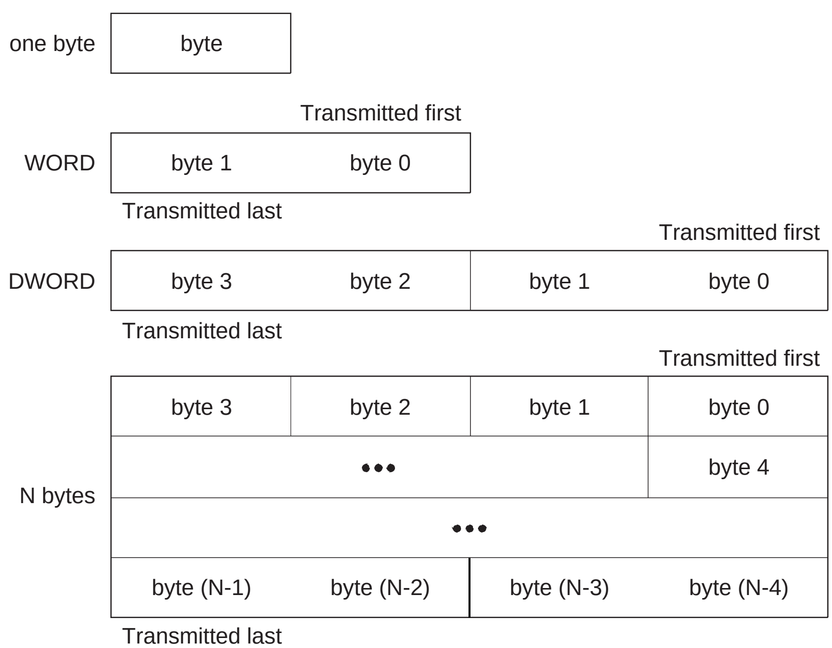


Figure 3-2 Byte Ordering

In multi-LANE implementations, all bytes are transmitted by mapping them to the multiple lanes as shown in Figure 3-3 and Figure 3-4. These rules apply for all packets (including Link Commands, TPs and DPs) as well as special symbols such as Training Sets.

Lane 1	Lane 0
byte 1	byte 0
byte 3	byte 2
...	...

Figure 3-3 Byte Ordering in a 2 LANE Configuration

Lane 3	Lane 2	Lane 1	Lane 0
byte 3	byte 2	byte 1	byte 0
byte 7	byte 6	byte 5	byte 4
...	...	...	...

Figure 3-4 Byte Ordering in a 4 LANE Configuration

3.2 Logical Idle and FLR non-insertion

The Logical Idle Symbol D0.0 - scrambled as defined in Section 3.5 – shall be transmitted when the M-TX is in the HS-BURST state and no SS packets (Link Commands, TPs or DPs) are being transferred on the link. Once started, the transmission of a SS packet shall continue without the insertion of any logical idle symbols as per [USB 3.0].

In a multi-LANE implementation, the first byte of a SS packet may be placed on any LANE. When ending an HS-BURST, if the packet transmission finishes misaligned, logical idle symbols shall be transmitted on all remaining LANEs. Figure 3-5 presents two examples of D0.0 logical idle transmission between packets.

Lane 3	Lane 2	Lane 1	Lane 0
...	...	...	...
END	END	END	Dx
SHP	SHP	D0.0	EPF
...	...	...	...

Lane 3	Lane 2	Lane 1	Lane 0
MK0	MK0	MK0	MK0
SHP	D0.0	D0.0	D0.0
Dx	EPF	SHP	SHP
...	...	...	...

Figure 3-5 Two examples of Logical Idle insertion in a 4x LANE configuration

The M-TX shall not insert any FLRs in the transmit stream.

> ***Implementation Note:*** *To prevent the M-TX from inserting FLR symbols in the transmit stream, the PA layer needs to always provide symbols for transmission (by always asserting TX_ProtDORDY during a HS-BURST) and also ensure the M-TX never throttles transmission by deasserting TX_PhyDIRDY on the M-PHY RMMI. This may place specific requirements on the clocking implementation of the M-TX such as ensuring that the TX_BitClk and TX_SymbolClk are derived from the same reference.*

3.3 Line Coding

All information communicated in the PWM-BURST and HS-BURST states shall be 8b10b encoded as per the data and control symbols assignments prescribed in [M-PHY] and the symbol mapping assignment described in this section.

Data symbols shall be directly mapped as per the assignment described in [M-PHY] .

Table 3-1 Mapping of SS Control Symbols

Control Symbols	SS Encoding	SSIC Encoding	M-PHY Usage	Notes
COM	K28.5	K28.5	MARKER0	MK0 sent at start of HS-BURST. Also re-used for COM.
EDB	K28.3	K28.3	MARKER1	MK1 used only for EDB.
SDP	K28.2	K28.6	MARKER2	MK2 used only for SDP - encoding differs from [USB3.0]
EPF	K23.7	K23.7	MARKER3	MARKER3 used only for EPF
SHP	K27.7	K27.7	MARKER4	MARKER4 used for SHP
END	K29.7	K29.7	MARKER5	MARKER5 used for END

SLC	K30.7	K30.7	MARKER6	MARKER6 used for SLC
SKP	K28.1	K28.1	FILLER	FLR used only for SKP.
SUB	K28.4	n/a	n/a	SUB not used in SSIC

Table 3-1 describes the mapping of the SS control symbols. As noted most of the the SuperSpeed control symbols (COM, EPF, SHP, END, SLC, SKP, EDB) are K-encoded as defined in [USB 3.0] with the one exception (SDP) that has a different K-encoding.

The FLR symbol is only used to indicate a SuperSpeed SKP Symbol and implementations shall ensure that an M-TX shall not independently insert FLRs as noted in Section 3.2.

8b/10b decode errors are handled as specified in [M-PHY] and the SUB symbol which is defined in [USB 3.0] for when a decode error is detected does not require a M-PHY mapping.

3.4 Clock Compensation

The following rules replace those defined in Section 6.4.3. of [USB 3.0]:

- A SKP Ordered Set shall consist of two SKP symbols transmitted one after the other on a single LANE
- For x2 and x4 M-PHY LINKs, when transmitted, SKP Ordered Sets shall be transmitted on all LANEs such that the same number of SKP Ordered Sets are transmitted on all LANEs, however the SKP Ordered Set transmission is permitted to start on any LANE
- SKP Ordered Sets shall not be transmitted within any packet or Ordered Set
- For a x1 M-PHY LINK, while in HS.BURST mode, transmitting TS1 Ordered Set, TS2 Ordered Set, LMP, TP, DP, or Logical Idle, transmitters shall transmit SKP Ordered Sets such that at least 4 SKP Ordered Sets are transmitted within a sliding window of 1416 non-SKP symbols transmitted
- For a x2 M-PHY LINK, while in HS.BURST mode, transmitting TS1 Ordered Set, TS2 Ordered Set, LMP, TP, DP, or Logical Idle, transmitters shall transmit SKP Ordered Sets such that at least 2 SKP Ordered Sets are transmitted per LANE within a sliding window of 708 non-SKP symbols transmitted per LANE (which results in a total of 4 SKP Ordered Sets being transmitted per 1416 non-SKP symbols transmitted over the full M-PHY LINK)
- For a x4 M-PHY LINK, while in HS.BURST mode, transmitting TS1 Ordered Set, TS2 Ordered Set, LMP, TP, DP, or Logical Idle, transmitters shall transmit SKP Ordered Sets such that at least 1 SKP Ordered Sets is transmitted per LANE within a sliding window of 354 non-SKP symbols transmitted per LANE (which results in a total of 4 SKP Ordered Sets being transmitted per 1416 non-SKP symbols transmitted over the full M-PHY LINK)
- It is permitted for a transmitter to transmit SKP Ordered Sets more frequently than this minimum requirement.
- For x1 M-PHY LINKs, receivers shall be tolerant to receive between 0 and 1416 non-SKP symbols between received SKP receptions, and as few as 4 SKP Ordered Sets received within a sliding window of 1416 non-SKP symbols
- For x2 M-PHY LINKs, receivers shall be tolerant to receive between 0 and 708 non-SKP symbols per LANE between received SKP receptions, and as few as 2 SKP Ordered Sets received within a sliding window of 708 non-SKP symbols per LANE (which results in a total of 4 SKP Ordered Sets being received per 1416 non-SKP symbols received over the full M-PHY LINK)
- For x4 M-PHY LINKs, receivers shall be tolerant to receive between 0 and 354 non-SKP symbols per LANE between received SKP receptions, and as few as 1 SKP Ordered Sets received within a sliding window of 354 non-SKP symbols per LANE (which results in a total of 4 SKP Ordered Sets being received per 1416 non-SKP symbols received over the full M-PHY LINK)

Figure 3-6 shows an example of SKPs between two packet transmissions on a x4 M-PHY LINK.

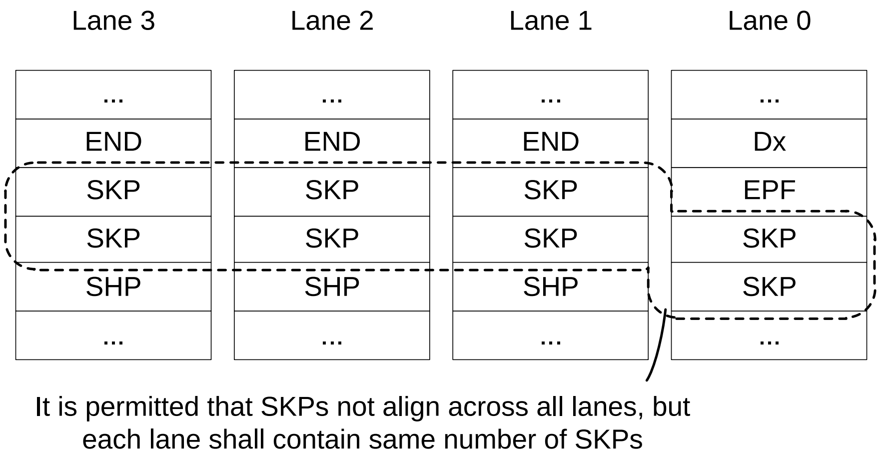


Figure 3-6 Example of SKP Insertion in a 4x LANE Configuration

Implementation Note:

When reusing existing SuperSpeed controllers with x2 or x4 M-PHY LINKs, it may be desirable to avoid increasing the number of SKPs transmitted for a given amount of data transferred. However, the requirement that SKP transmissions include the same number of SKPs on all LANEs means that, if, when the controller indicates a SKP transmission, that the transmission is simply replicated across all LANEs, the average number of SKPs transmitted would be increased relative to the amount of data transferred. It is possible to satisfy the above rules and at the same time avoid needlessly increasing the relative number of SKPs transmitted by implementing an algorithm that accumulates SKPs for transmission, such that, for example, on a x2 M-PHY LINK, the transmitter would transmit two SKPs on each LANE, but only at alternate intervals. If the transmit controller already buffered up multiple SKPs, then it is not necessary to implement interval skipping, as this has in effect already been done by the controller.

The recommended algorithm is the following:

- *A transmitter should keep a running count of the number of transmitted symbols across all LANEs since the last SKP symbol transmission, referred to as Z.*
- *Z should be reset to 0 whenever the transmitter enters HS.Burst*
- *The non-integer remainder of the following Z calculations should not be discarded and shall be used in the calculation to schedule the next SKP symbols*
- *While transmitting TS1 Ordered Set, TS2 Ordered Set, LMP, TP, DP, or Logical Idle, when the integer result of*

  $$\frac{Z}{354 * NumberOfLanes}$$

  reaches one, the transmitter should buffer one (additional) SKP Ordered Set to be transmitted on each LANE at the end of the current packet or Ordered Set transmission

3.5 Data Scrambling

Data shall be scrambled according to the following rules on a per-LANE basis:

- Scrambling shall be done using an LFSR applied
- The LFSR implements the polynomial: G(X)=X16+X5+X4+X3+1
- The LFSR value shall be advanced eight serial shifts for each Data Symbol and K Code **except** for SKP.
- All 8b/10b D-codes, *including* those within the Training Sequence Ordered Sets shall be scrambled.
- K codes shall not be scrambled.
- During a HS-BURST the LFSR on the transmit side shall be initialized to FFFFh after the transmission of any MK0 symbol.
- During a HS-BURST the LFSR on the receive side shall be initialized to FFFFh after the receipt of any MK0 symbol.
- Scrambling shall only be applied while in HS-BURST and shall not be used in PWM-BURST.
- Scrambling can be optionally disabled via the DISABLE_SCRAMBLING RRAP command as described in Section 2.5.2.

Implementation Note:

In the implementation example described in Figure 1-2, this implies that the standard SuperSpeed scrambler is disabled and a scrambler compliant with this section is implemented in the PHY Adapter layer on a per-LANE basis.

3.6 PowerOn Reset and Inband Reset

3.6.1 PowerOn Reset

PowerOn Reset refers to a condition that shall be defined as the power supply of the port achieving a steady state, the details of which are implementation specific and not defined by this document.

When an implementation is powered and the PowerOn Reset is asserted the SSIC LTSSM shall enter the SS.Disabled state. On the deassertion of PowerOn Reset, the SSIC LTSSM shall enter the RX.Detect state.

Upon assertion and de-assertion of PowerOn Reset, M-PHY MODULEs shall enter and exit the DISABLED state as defined in Section 4.7.1.4 of [M-PHY] .

3.6.2 Inband Reset (Hot Reset and Warm Reset)

Both mechanisms of Inband reset defined in [USB 3.0] are supported: Hot Reset and Warm Reset. However the reset signaling mechanisms are modified to be implemented on top of the M-PHY as defined in this section.

3.6.2.1 Hot Reset

Hot Reset is signaled by a DSP by sending TS2 ordered sets with the Reset bit asserted. A Hot Reset shall cause the SSIC LTSSM to transition to the Hot Reset state as described in 3.8.9. Upon completion of Hot Reset, the following shall occur:

- A DSP shall reset its Link Error Count.
- The port configuration information of a USP shall remain unchanged.
- The M-PHY configuration settings shall remain unchanged.
- The LTSSM of a port shall transition to U0.

If a Hot Reset fails, the DSP shall signal a Warm Reset as per [USB 3.0].

3.6.2.2 Warm Reset

Warm Reset is signaled by a DSP using the LINE-RESET mechanism defined in [M-PHY] .

The operational model of a Warm Reset is as follows:

- The DSP shall drive DIF-N on the M-TX of PAIR0 for a period of tResetDIFN.
- The DSP shall issue a LINE-RESET on the M-TX of PAIR0.
- When a LINE-RESET is signaled, the LTSSM shall transition to the Rx.Detect.Reset state.

Signaling a LINE-RESET on any M-TX other than that of PAIR0 has undefined results. Only a DSP shall issue Warm Reset via the LINE-RESET mechanism. A USP shall use the LINE-RESET mechanism to signal a USP disconnect as defined in Section 5.

3.7 Link Layer Timing Requirements

Link layer timing requirements shall remain the same as specified in [USB 3.0] except for the parameters defined below.

Table 3-2 Link Layer Timing Parameter

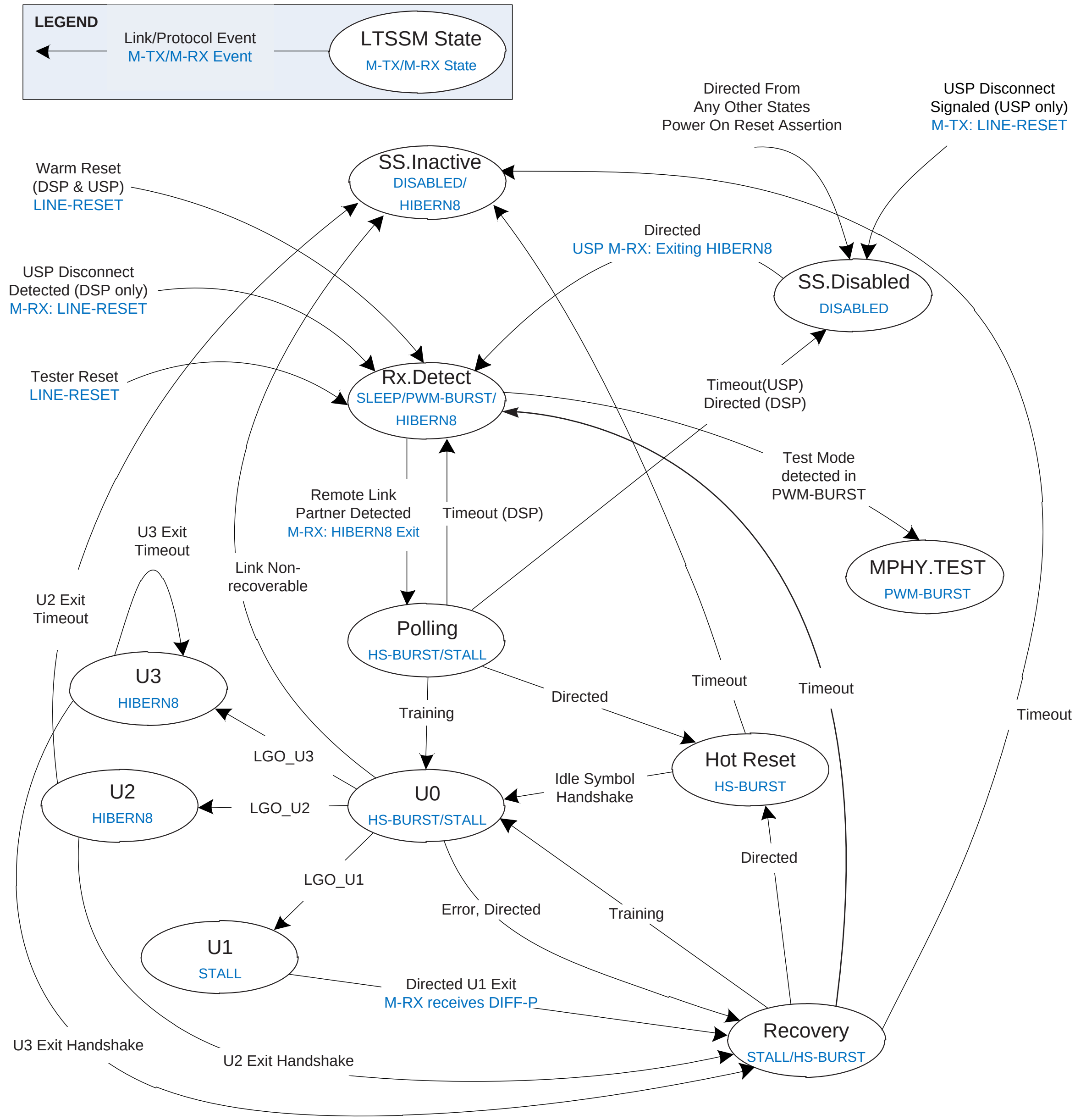
Name	Description	Min	Max	Units
PENDING_HP_TIMER	As described in [USB 3.0]		100	µs
PM_LC_TIMER	As described in [USB 3.0]		100	µs
PM_ENTRY_TIMER	As described in [USB 3.0]		120	µs
tRetrain	Timer to detect improper training of the local and remote M-RX as part of HS-BURST entry. Timer is implemented in the Polling and Recovery LTSSM states as described in Section 3.8.3 and Section 3.8.8.	40	50	µs
tResetDIFN	Period of time a DSP is required to drive a DIF-N prior to a LINE-RESET. Defined to ensure USP is ready to receive the LINE-RESET and to not break Warm Reset timing as defined in [USB 3.0].	60	80	ms
tPollingSTALLResidency	Period of time spent in the Polling.STALL sub-state. Timing values are specified to allow for designs using an existing [USB 3.0] LTSSM as shown in Figure 1 2. Such implementations may require up to two legacy Receiver detection cycles to be performed in this sub-state that may take up to 12 ms each along with some operating margin.		40	ms
tPollingActiveTimeout	As described in [USB 3.0]. Increased from the 12ms value prescribed in [USB 3.0] to account for maximum of 40ms in the Polling.STALL state along with some operating margin.		58	ms
tPortConfiguration	As described in [USB 3.0]. Increased from the 20µs value prescribed in [USB 3.0] to be in sync with the increase to the PENDING_HP_TIMER		110	µs

3.8 SSIC Link Training and Status State Machine (LTSSM)

The SSIC Link Training and Status State Machine (LTSSM) of the link layer is shown in Figure 3-7. The figure and following section documents relevant state details, associated transitions and details of the mapping of the LTSSM state to the M-PHY state machines.

Unless otherwise noted, requirements for LTSSM states and sub-states defined in [USB 3.0] also apply to this supplement and are not reproduced here. However [USB 3.0] LTSSM requirements corresponding to the physical layer do not apply and instead M-PHY M-TX and M-RX requirements detailed in this section shall be followed. Specifically Low Frequency Periodic Signaling (LFPS) and Receiver Termination Detection and the various signaling mechanisms thereof do not apply to this supplement.

> ***Implementation Note:*** *This section has been specified to allow compliant implementations to be designed using an existing [USB 3.0] compliant LTSSM and a suitable PA layer as shown in Figure 1-2. This does not imply preference for any particular style of implementation, and other implementations are supported, provided they comply to the requirements of this section.*



Note: Figure is illustrative only. Not all of the transition conditions are listed. Refer to text for details.

Figure 3-7 SSIC LTSSM state diagram

3.8.1 SS.Disabled

SS.Disabled is a logical power-off state when a port is unpowered or when the SSIC port's functionality is disabled.

A DSP when directed to do so shall signal a DSP disconnect and transition to this state.

3.8.1.1 SS.Disabled Requirements

The SS.Disabled state does not contain any sub-states as shown in Figure 3-8:

- The M-PHY local RESET to the M-RX and M-TX of all PAIRs shall be asserted which maintains the modules in the DISABLED state

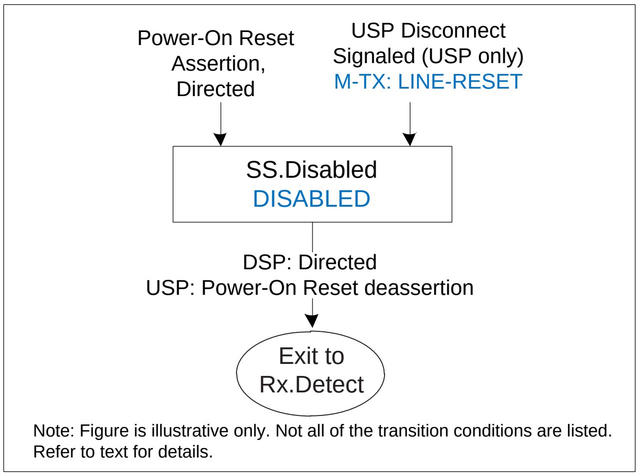


Figure 3-8 SS.Disabled state

3.8.1.2 Exit from SS.Disabled

- Exit shall take place for a USP via the deassertion of Power-On Reset and for a DSP when directed to exit:
    - The M-PHY local RESET to the M-RX and M-TX of all PAIRs shall be de-asserted which transitions the modules from the DISABLED to the HIBERN8 state.
    - the LTSSM shall transition to Rx.Detect.Active LTSSM state.

3.8.2 RX.Detect

The Rx.Detect state of the LTSSM is entered in the following scenarios:

- Signaling of a Warm Reset by a DSP
- Detection of a Warm Reset by a USP
- Detection of a USP disconnect by a DSP
- Completion of Power on Reset by both a DSP and USP
- When Polling or Recovery is unsuccessful for a DSP as defined in [USB 3.0]
- Signaling of a LINE-RESET by Test Equipment

The concept of far-end terminations as defined in [USB 3.0] does not apply to this supplement and instead M-PHY based mechanisms shall be used to detect the presence of a link partner and to synchronize operation as defined in this section.

Rx.Detect contains a sub-state machine as shown in Figure 3-9 with the following sub-states:

- Rx.Detect.Reset
- Rx.Detect.Active
- Rx.Detect.LS-MODE

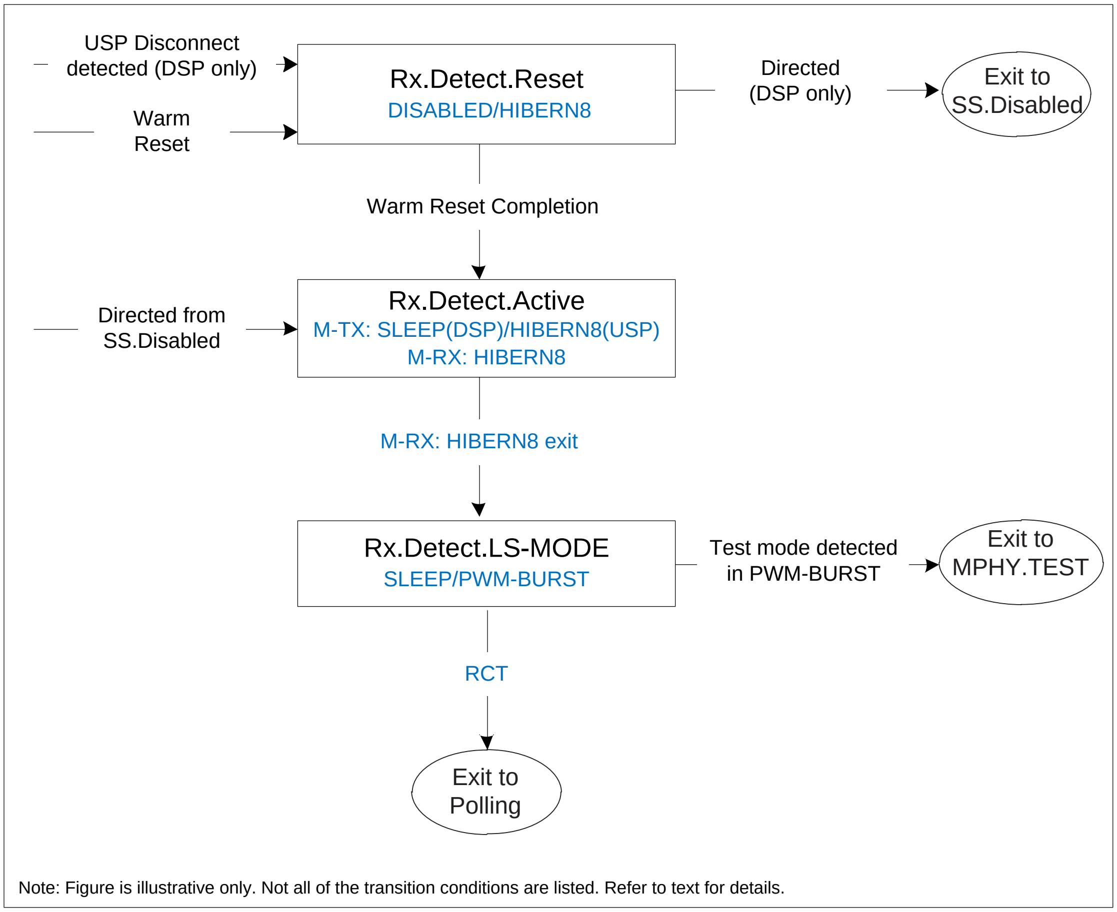


Figure 3-9 Rx.Detect Sub-state Machine

3.8.2.1 RX.Detect.Reset Requirements

This sub-state is entered in following scenarios:

- LINE-RESET signaled by a DSP as part of Warm Reset as defined in 3.6.2.2 (both USP and DSP enter) or
- LINE-RESET is signaled during a USP disconnect as defined in Section 5.1.1(DSP only enters)
- LINE-RESET is signaled by Test Equipment

In this sub-state the USP and DSP shall complete the following steps in the following order:

- Wait for the completion of LINE-RESET signaling.
- Assert the local M-PHY Reset bringing the M-TX and M-RX to the DISABLED state on all PAIRs.
- De-assert the local M-PHY Reset bringing the M-TX and M-RX to the HIBERN8 state on all PAIRs.

The time taken to complete the steps is not mandated by this supplement. In the case of a warm reset, a DSP may handle any delays in completion of the above steps by an USP in an implementation-specific manner. In the case of a USP disconnect, the DSP may remain in the DISABLED state for longer periods for power saving reasons before finally completing the steps to enable a USP to subsequently re-connect.

3.8.2.2 Exit from RX.Detect.Reset

- A port shall transition to Rx.Detect.Active after completing the required steps as defined in Section 3.8.2.1.
- A DSP shall transition to SS.Disabled when directed.

3.8.2.3 RX.Detect.Active Requirements

Rx.Detect.Active is a sub-state to detect the presence of a link partner.

- For a DSP:
  - The M-TX shall be configured to exit HIBERN8 into the SLEEP state which results in a DIF-N value being driven on all PAIRs.
  - The M-RX shall remain in HIBERN8 on all PAIRs until the link partner initiates a HIBERN8 exit
- For a USP:
  - The M-TX and M-RX shall remain in HIBERN8 until the link partner initiates a HIBERN8 exit

3.8.2.4 Exit from RX.Detect.Active

- Upon detection of a HIBERN8 exit on its M-RX on all PAIRs the USP shall initiate an exit from HIBERN8 on its M-TX of all PAIRs and shall transition to Rx.Detect.LS-MODE.
- Upon detection of a HIBERN8 exit on its M-RX on all PAIRs the DSP shall wait a minimum Tactivate time before transitioning to Rx.Detect.LS-MODE.
- A DSP shall transition to SS.Disabled when directed.

3.8.2.5 RX.Detect.LS-MODE Requirements

Rx.Detect.LS-MODE is a sub-state in which communication takes place in the LS-MODE using the RRAP.

The requirements for this sub-state for a USP, DSP are defined in Section 2.5.

3.8.2.6 Exit from RX.Detect.LS-MODE

- A DSP shall transition to SS.Disabled when directed.
- An USP and a DSP shall exit to the MPHY.TEST state when an RRAP write command to the TEST_MODE register is received as defined in Table 2-5.
- An USP and a DSP shall execute a RCT to exit this sub-state and enter Polling when configured to do so using the RRAP as defined in Section 2.5.3.
- After executing an RCT, the M-TX shall wait for a period equal to the RX_Min_ActivateTime_Capability defined in Section 2.2.3 prior to exiting this sub-state into the Polling state.
- Note: A delay equivalent to the RX_Min_ActivateTime_Capability timing parameter is prescribed in this sub-state to allow flexibility for implementations to prepare for STALL and HS-BURST.

3.8.3 Polling

In the Polling state the M-PHY is configured prior to entering HS-BURST. While in HS-BURST, the training ordered sets of TS1, and TS2 as defined in [USB 3.0] are transmitted.

Polling contains a sub-state machine shown in Figure 3-10 with the following sub-states:

- Polling.STALL
- Polling.Active

- Polling.Configuration
- Polling.Idle

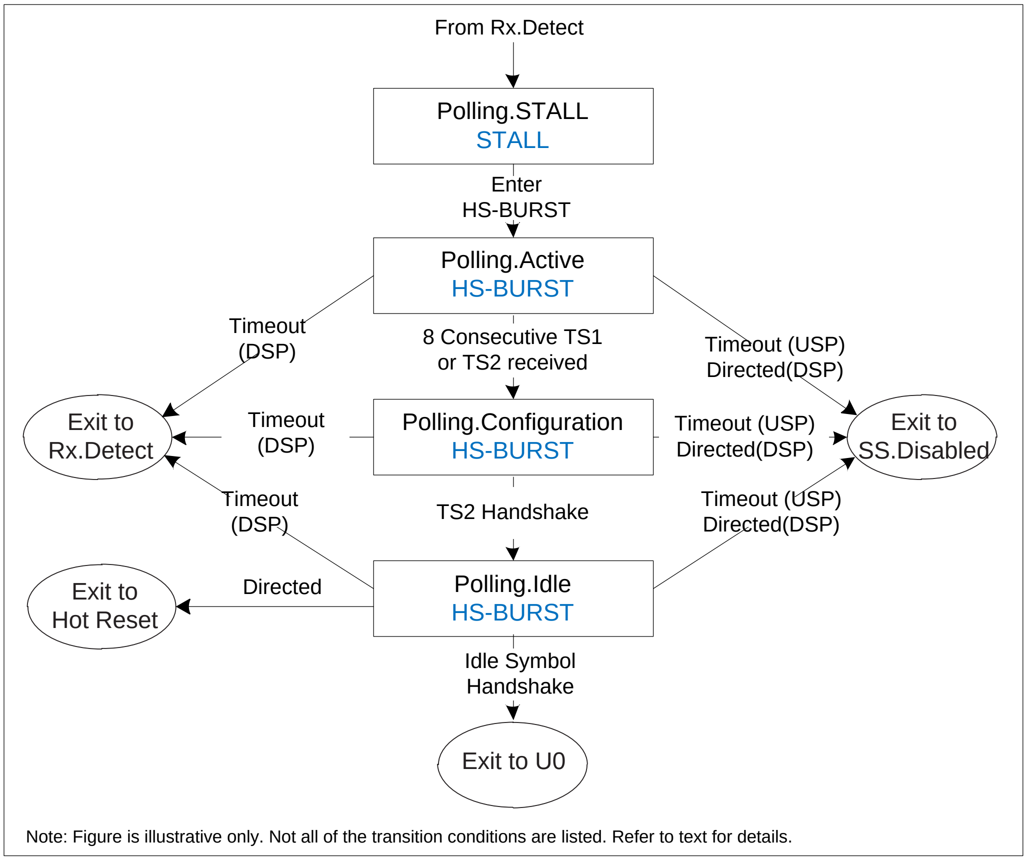


Figure 3-10 Polling Sub-state Machine

3.8.3.1.1 Polling.STALL Requirements

- The Polling.STALL sub-state is a transitory sub-state which is used to prepare the M-TX to enter the HS-BURST mode.
- The M-TX and M-RX are in the STALL state.
- An exit from this sub-state should be completed within tPollingSTALLResidency.

3.8.3.2 Exit from Polling.STALL

The following requirements shall be met in the following order when exiting from this sub-state:

- The M-TX shall be configured to enter HS-BURST as per [M-PHY] .
- A timer shall be started and set to expire after tRetrain.
- The LTSSM shall transition to Polling.Active.

3.8.3.3 Polling.Active/Configuration/Idle Requirements

- If the tRetrain timer expires, M-TX shall be cycled from HS-BURST to STALL and then back to HS-BURST, and the tRetrain timer shall then be restarted.
- The M-TX and M-RX shall remain in the HS-BURST state for the remaining Polling sub-states except as required based on tRetrain timer expiration.
- An equivalent of Polling.RxEQ as defined in [USB 3.0] for receiver equalizer training is not required and shall be bypassed.

- The Disabling Scrambling bit and the Loopback bit in the link configuration field of the TS2 Ordered Set shall be ignored.
- Upon successful completion of the Polling sub-states the LTSSM shall transition to U0.
- The requirements in these sub-states including the handshake sequences and transitions due to the expiry of relevant timers are as defined in [USB 3.0], without regard to transitions through STALL due to tRetrain timer expiration.
- Note: M-RX receiver bit synchronization and training is completed using mechanisms specified in [M-PHY] . The supplement defines the tRetrain timer as a contingency to enable [M-PHY] specific training mechanism to be re-performed. As a result, none of the Polling.Active/Configuration/Idle Timeouts defined in [USB 3.0] are expected to expire in SSIC implementations with correctly operating M-TX and M-RX modules.

3.8.4 U0

U0 is the normal operational state in which the M-TX and M-RX are in the HS-Burst state and are actively transmitting and receiving traffic. U0 contains no sub-states.

While in U0 the M-TX and the M-RX of a PORT may independently transition between the HS-BURST and STALL states as shown in Figure 3-11.

The M-TX may optionally transition to the STALL state instead of transmitting logical idle symbols. The conditions under which this transition is made such as number of logical idle symbols that are transmitted prior to entering the STALL state are not specified in this supplement. For example, implementations may choose to transition to STALL immediately without transmitting any logical idle symbols or may continue to transmit logical idle symbols without entering the STALL state.

Independently the M-RX shall transition to the STALL state when the link partner’s M-TX implementation chooses to enter the STALL state.

> ***Implementation Note:***
>
> *In the implementation example described in Figure 1-2, when the PA detects a STALL entry on its M-RX while in U0, the PA may have to manufacture logical idle symbols to be sent to the link layer to maintain the U0 state in the legacy LTSSM.*

3.8.4.1 Exit from U0

- A successful LGO_U1 entry sequence shall transition the link state to U1 and the M-TX/M-RX to STALL as follows:
    - The DSP shall initiate LGO_U1 and shall disable STALL entry on all PAIRs until a LXU is received (indicating abort of U1 entry) or it successfully enters U1.
    - The USP, upon receipt of the LGO_U1 and if accepting U1 entry, shall in the following order:
        - disable STALL entry on all PAIRs until it successfully enters U1
        - respond with a LAU
    - After sending an LPMA, the DSP shall transition to U1 and transition its M-TX to the STALL state on all PAIRs.
    - After receiving an LPMA, the USP shall transition to U1 and transition its M-TX to the STALL state on all PAIRs.
    - U1 can also be initiated by a USP in which case the above sequence takes place with the roles of DSP and USP reversed.
- A successful LGO_U2/LGO_U3 entry sequence shall transition the link state to U2/U3 and the M-TX/M-RX to HIBERN8 as follows:
    - The DSP shall in the following order:

    - disable STALL entry on all PAIRs and then
    - initiate U2/U3 entry via transmission of LGO_U2/LGO_U3
  - The DSP shall re-enable STALL entry only if either LXU is received (indicating abort of U2 entry) or U2/U3 entry is successful
  - The USP, upon receipt of the LGO_U2/LGO_U3 and if accepting U2/U3 entry, shall in the following order:
    - disable STALL entry on all PAIRs until it successfully enters U2/U3
    - configure M-TX and M-RX modules on all PAIRs for HIBERN8 entry
    - respond with a LAU
  - The DSP, upon receipt of the LAU shall in the following order:
    - configure M-TX and M-RX modules on all PAIRs for HIBERN8 entry
    - respond with a LPMA
  - After sending an LPMA, the DSP shall transition to U2/U3 and shall terminate the HS-BURST on the M-TX of all PAIRs.
  - After receiving an LPMA, the USP shall transition to U2/U3 and shall terminate the HS-BURST on the M-TX of all PAIRs.

Implementation Note:

As per [M-PHY] configuring M-TX and M-RX modules for HIBERN8 entry requires an INLINE-CR registry change and the assertion of the RX_CfgUpdt/TX_CfgUpdt signal of the M-RX/M-TX for all PAIRs. As a result of this configuration change, the termination of HS-BURST results in a RCT and causes local M-TX and remote M-RX to enter HIBERN8.

  - As per [M-PHY] , the following is guaranteed on HIBERN8 entry:
    - the remote M-RX enters HIBERN8 and shall hold the line in DIF-Z before the local M-TX enters HIBERN8
    - During HIBERN8 entry the M-RX ignores any transitions on the line until it drives and senses a DIF-Z on the line.
  - U2 can also be initiated by a USP in which case the above sequence takes place with the roles of DSP and USP reversed.
- The remaining exit conditions and timeouts for U0 listed in [USB 3.0] also apply.

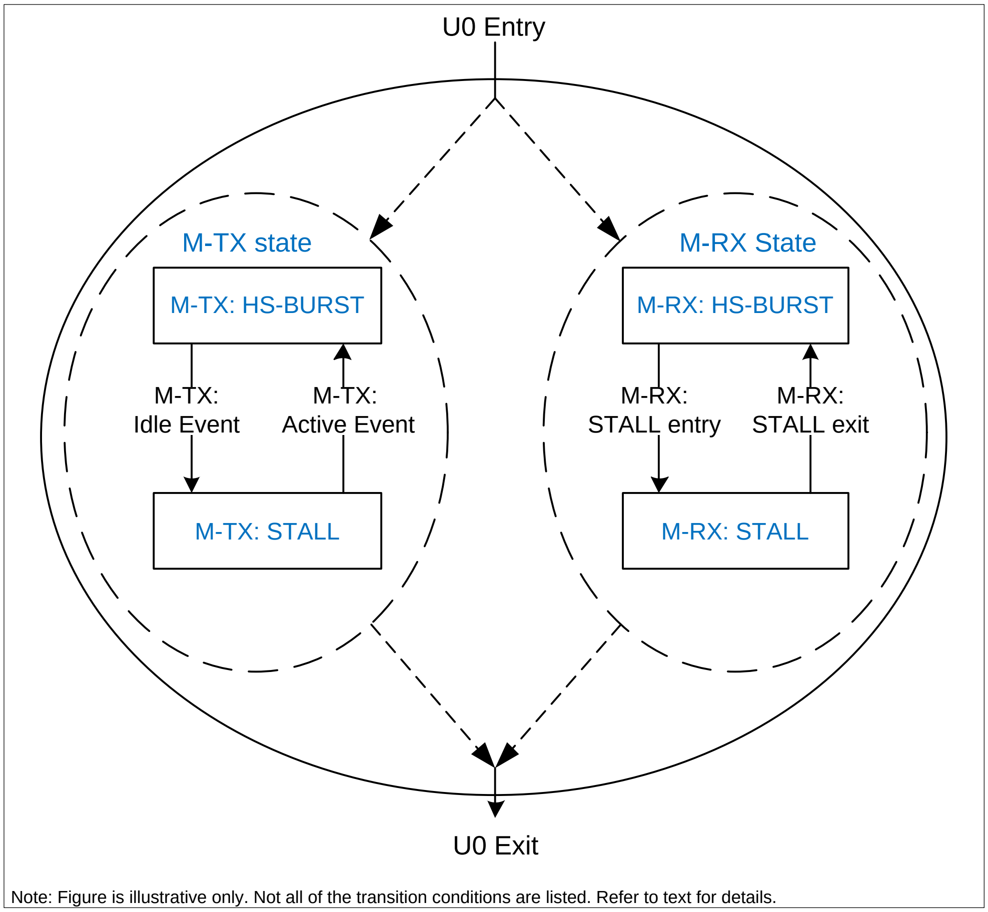


Figure 3-11 U0 Sub-state Machine

3.8.5 U1

U1 is a low-power state with minimum exit latency. Either a DSP or a USP may initiate entry to this state.

- In this state the M-TX and M-RX state machines shall transition to and stay in the STALL state.

This LTSSM state is distinguished from transitions to the STALL state in U0 by the fact that U1 is entered under direction from the link layer as defined in [USB 3.0].

3.8.5.1 U1 Requirements

- SSIC ***shall not*** support a direct transition from U1 to U2.
- Upon timeout of the U2 inactivity timer a transition to U0 shall be made prior to initiating an entry to U2.

3.8.5.2 Exit from U1

- The port shall ensure that both M-RX and M-TX are in the STALL state prior to initiating a U1 exit.
- The port shall exit to Recovery by initiating an HS-BURST on its M-TX or when an HS-BURST is detected by its M-RX.
- The U1 to SS.Inactive transition due to an unsuccessful U1 exit as defined in [USB 3.0] does not apply to this supplement. When initiated the exit from U1 to Recovery shall be unconditionally completed.

3.8.6 U2

U2 is a link state where more power saving opportunities are allowed compared to U1, but with an increased exit latency. U2 does not contain any sub-states. Either a DSP or a USP may initiate entry to this state.

3.8.6.1 U2 Requirements

- The M-TX and the M-RX state machines shall stay in the HIBERN8 state for all PAIRs.
- The concept of far end receiver termination detection as defined in [USB 3.0] does not apply and does not have to be completed while in this state.

3.8.6.2 Exit from U2

- The port shall transition to Recovery when a successful U2 exit handshake completes in the following manner:
  - The M-RX receives an HIBERN8 exit indication on all PAIRs or M-TX initiates a HIBERN8 exit on all PAIRs when port is directed to exit U2 by the link layer and
  - Both M-TX and M-RX successfully exit HIBERN8 on all PAIRs and transition to STALL.
- The port shall transition to SS.Inactive if the tNoLFPSResponseTimeout timer (as defined in [USB 3.0]) expires and if a successful U2 exit handshake as described above is not achieved.

The following [M-PHY] capability attributes described in Section 2.2.3 imply a minimum residency of 200us in U2:

- Rx/Tx_Hibern8Time_Capability = 100us: Minimum residency time in HIBERN8 state
- RX_Min_ActivateTime_Capability = 100us: Minimum time to exit HIBERN8

The SSIC LTSSM shall ensure that these residency requirements in [M-PHY] are met prior to initiating a U2 exit.

3.8.7 U3

U3 is a link state where a device is put into a suspend state. Though both U2 and U3 map to HIBERN8, U3 may provide additional power savings opportunities at a system level due to the requirement to complete a handshake upon an exit. Details of such system-level power savings opportunities and the means for enabling them are out of scope of this supplement.

U3 does not contain any sub-states.

3.8.7.1 U3 Requirements

- In this state the M-TX and M-RX state machines are in the HIBERN8 State for all PAIRs.
- A port not able to respond to U3 exit handshake within tNoLFPSResponseTimeout (as defined in [USB 3.0]) may respond when it is ready.
- The concept of far end receiver termination detection as defined in [USB 3.0] does not apply and does not have to be completed while in this state.

3.8.7.2 Exit from U3

- The port shall transition to Recovery when a successful U3 exit handshake completes in the following manner:
  - One of the following initial conditions is true:

        - The M-TX drives a HIBERN8 exit on all PAIRs when the port is directed to exit U3 by the link layer or
        - the M-RX receives a HIBERN8 exit indication on all PAIRs
    - and the M-TX successfully exit HIBERN8 on all PAIRs and transitions to STALL
    - and a minimum Tactivate time has elapsed after M-RX receives a HIBERN8 exit on all PAIRs.
- The port shall remain in U3 when a successful U3 exit handshake as described above is not achieved.
    - In this case the M-TX which initiated the HIBERN8 exit shall continue to drive DIF-N until the U3 exit handshake successfully completes.

3.8.8 Recovery

Recovery is a LTSSM state that is entered to retrain the M-PORT. During this state TS1, and TS2 training ordered sets are transmitted as defined in [USB 3.0] to synchronize the link and to exchange the link configuration information.

Recovery contains the following sub-states:

- Recovery.Active
- Recovery.Configuration
- Recovery.Idle

3.8.8.1 Recovery.Active Requirements

- A timer set to expire after tRecoveryActiveTimeout (as defined in [USB 3.0]) shall be started upon entry to this sub-state.
- Initial conditions for this sub-state are dependent on the entry condition:
    - When entered from U0, the M-TX shall be brought to a STALL state in order to re-train the M-TX for a new HS-BURST. The M-RX state is dependent on the link partner M-TX.
    - When entered from U1, the M-RX or M-TX shall initially be in the STALL state as per U1 requirements defined in 3.8.5.2.
    - When entered from U2 or U3, the M-RX and M-TX are initially in the STALL state.
- The M-TX is then brought to the HS-BURST state and the port shall transmit the TS1 ordered sets upon entry to this sub-state.
- Upon M-TX entry into HS-BURST, the LTSSM shall start a tRetrain timer.

3.8.8.2 Recovery.Active/Configuration/Idle Requirements

- If the tRetrain timer expires, M-TX shall be cycled from HS-BURST to STALL and then back to HS-BURST, and the tRetrain timer shall then be restarted.
- The M-TX and M-RX shall remain in the HS-BURST state for the remaining Recovery sub-states, except as required based on tRetrain timer expiration.
- The requirements for the traffic, handshake sequences and exit conditions for these sub-states are as defined in [USB 3.0], without regard to transitions through STALL due to tRetrain timer expiration.
- The Disabling Scrambling bit and the Loopback bit in the link configuration field of the TS2 Ordered Set shall be ignored.
- Upon successful completion of the Recovery sub-states the LTSSM shall transition to U0.

3.8.9 Hot Reset

The Hot Reset state shall be implemented as specified in [USB 3.0].

3.8.9.1 Hot Reset Requirements

- In this state the M-TX and M-RX are in the HS-BURST state.
- The port shall implement the Hot Reset sub-states, associated timers and exit conditions as defined in [USB 3.0].

3.8.10 SS.Inactive

SS.Inactive is an error state where the link becomes non-operational.

A DSP in this state, shall transition its M-TX and M-RX to the DISABLED state. In this state, the DSP is not able to receive any communication from the USP. A DSP shall only exit from this state when directed to issue a Warm Reset. In order to signal a warm reset, the DSP shall transition out of the DISABLED state and drive a LINE-RESET as defined in [M-PHY] on PAIR0.

An USP in this state, shall assert and then de-assert the local M-PHY Reset for all LANEs bringing the M-TX and M-RX to the HIBERN8 state on all PAIRs. A USP shall only exit upon the receipt of a Warm Reset. While in SS.Inactive an USP shall ignore any data received on the M-RX until a LINE-RESET is received.

The concept of far end receiver termination detection as defined in [USB 3.0] does not apply and does not have to be completed while in this state.

3.8.11 MPHY.TEST

MPHY.TEST is an LTSSM state used for testing the M-PHY Physical layer.

The initial state of the M-TX and M-RX state machines in this state is PWM-BURST.

For details of the operational behavior in this state please refer to Section 6.

4 Protocol Layer

Implementations incorporate the protocol layer defined in [USB 3.0] except as defined in this section.

4.1 Port Capability Link Management Packet (LMP)

The Port Capability LMP describes each port's link capabilities and is sent by both link partners after the successful completion of training and link initialization.

Implementations shall ignore the Link Speed field of the Port capability LMP. The operational speed of the link shall be defined by the profile as defined in Section 2.2.1.

Implementations shall ignore the USB 3.0 OTG Capable (OTG) field of the Port Capability LMP. The Direction (D) field shall be used to identify the DSP and the USP as defined in [USB 3.0].

4.2 Timing Parameters

The protocol-layer timing parameters described in Section 8.13 of [USB 3.0] also apply to this supplement.

However certain timing parameters are modified as shown in Table 4-1 to account for a slower bit-rate (for HS-G1/G2) and latencies introduced due to STALL entry and exit while in U0.

Table 4-1 Protocol Timing Parameters

Name	Description	Min	Max	Units
tPingResponse	Time between device reception of the last framing symbol of a ping and the first framing symbol of the ping_response		5000	ns
tNRDYorSTALLResponse	Time between device reception of the last framing symbol for an ACK TP or a DPP or a STATUS TP and the first framing symbol of an NRDY or STALL response		5000	ns
tDPResponse	Time between device reception of the last framing symbol for an ACK TP and the first framing symbol of a DP response		5000	ns
tACKResponse	Time between device reception of the last framing symbol for a DPP or a STATUS TP and the first framing symbol of an ACK response		5000	ns
tMaxBurstInterval	Time between DPs when the device or host is bursting. If the device cannot meet this maximum time, then it shall set the EOB flag in the last DP it sends.		1000	ns
tHostACKResponse	Time between host reception of the last framing symbol for a DPP and the first framing symbol of an ACK response		5000	ns

5 Device Framework

Implementations incorporate the device framework defined in [USB 3.0] except as defined in this section.

5.1 Dynamic Attachment and Removal

Though this interconnect is intended for embedded inter-chip links, there is a usage requirement to support dynamic removal and subsequent attachment to support power management goals or to present an alternative device configuration. This supplement supports mechanisms to have either the USP or the DSP initiate a disconnect as described in the following sections.

5.1.1 USP Disconnect

The use case for signaling an USP Disconnect is to enable a peripheral to re-enumerate with a different device configuration. A USP achieves this by indicating a disconnect and a subsequent re-connect as defined in this section.

The operational model for a USP to signal a Disconnect is as follows:

- The USP shall signal a Disconnect by signaling a LINE-RESET on its M-TX on PAIR0.
- The USP shall maintain a DIF-N prior to driving a DIF-P on its M-TX as per the LINE-RESET timing specified in [M-PHY] .
- Signaling a LINE-RESET on any M-TX other than that of PAIR0 has undefined results.
- Upon completion of the LINE-RESET, the USP shall assert local M-PHY Reset for all LANEs.
- The USP M-TX and M-RX of all the LANES shall subsequently transition to the DISABLED state
- The USP LTSSM shall transition to the SS.Disabled state.
- The Peripheral Upstream Device port shall transition to USDPORT.Powered-Off (as defined in Fig 10-25 of [USB 3.0]).
- If a USP is in U3, a U3 exit handshake shall be completed prior to signaling a disconnect. Signaling of a USP disconnect while in U3 is not supported and has undefined results.

The operational model for a DSP upon detecting a USP Disconnect is as follows:

- The DSP shall toggle local M-PHY Reset for all LANEs.
- The DSP shall then transition to Rx.Detect.Active as described in Section 3.8.2 in order to detect a subsequent re-connect from the USP.

The operational model for a USP to signal a subsequent re-connect is as follows:

- When ready to re-connect, the USP shall de-assert local M-PHY Reset on all LANEs.
- The USP M-TX and M-RX shall transition to the HIBERN8 state for all LANEs.
- The USP LTSSM shall transition to the Rx.Detect.Active state.
- The Peripheral Upstream Device port shall transition to USDPORT.Powered On (as defined in Fig 10-25 of [USB 3.0]).

5.1.2 DSP Disconnect

The DSP disconnect is a host-initiated mechanism to enable a peripheral to re-enumerate with a different device configuration.

An additional use case for signaling a DSP disconnect is to disable the associated port. In this case, a USP can re-connect only after the DSP is subsequently re-enabled. A mechanism for the USP to request DSP to be re-enabled is out of scope of this supplement.

The operational model for a DSP to signal a Disconnect is as follows:

- The DSP shall signal a Warm Reset on the M-TX of PAIR0 as defined in Section 3.6.2.2.
- Upon completion of the Warm Reset, the LTSSM shall transition to Rx.Detect.Active and then to Rx.Detect.LS-MODE
- In the Rx.Detect.LS-MODE sub-state, while in PWM-BURST mode, the DSP shall signal a disconnect by signaling a RRAP write command and shall ensure a valid RRAP write response is received as defined in Section 2.5.2 before terminating the PWM-BURST by transitioning the M-TX to SLEEP.
- A BURST_CLOSURE RRAP command shall not be transmitted by the DSP prior to terminating the PWM-BURST.
- A DSP shall then assert the local M-PHY reset for all LANES:
    - The DSP M-TX and M-RX of all the LANES are in the DISABLED state
    - The DSP LTSSM is in the SS.Disabled state.

The operational model for a USP upon detecting a DSP Disconnect is as follows:

- The USP shall wait for the PWM-BURST to be terminated on its M-RX and then terminate the PWM-BURST on its M-TX.
- The USP shall assert and then de-assert the local M-PHY Reset for all LANEs bringing the M-TX and M-RX to the HIBERN8 state on all PAIRs
- The USP LTSSM shall transition to the RxDetect.Active state.
- The Peripheral Upstream Device port shall transition to USDPORT.Powered-On (as defined in Fig 10-25 of [USB 3.0]).
- This behavior enables a USP to detect a re-connect when the DSP is subsequently re-enabled.
- The USP may optionally be powered down, the Peripheral Upstream Device port transitioned to the USDPORT.Powered-Off state and the M-PHY transitioned to the SS.Disabled state. In this case the USP will not be able to detect a re-connect from the DSP. In such a scenario, a mechanism for powering up the USP to detect a subsequent re-connect is out of scope of this supplement.

6 MPHY.TEST

This section is ***optional normative*** and defines the behavior of a USP or a DSP in the optional MPHY.TEST state. If the MPHY.TEST state is supported, the following requirements defined in this section shall apply.

6.1 Overview

The purpose of the MPHY.TEST state is to allow standardized electrical testing of SSIC M-PHYs. For example, [CTS] defines a set of M-PHY electrical tests which are independent of the protocol layer. The M-PHY based protocols that use these tests are listed in Appendix D of [CTS].

Figure 6-1 shows an SSIC Device Under Test attached to Test Equipment and illustrates the various components involved in the support of the MPHY.TEST state. In the figure below, “n” indicates the number of supported PAIRs.

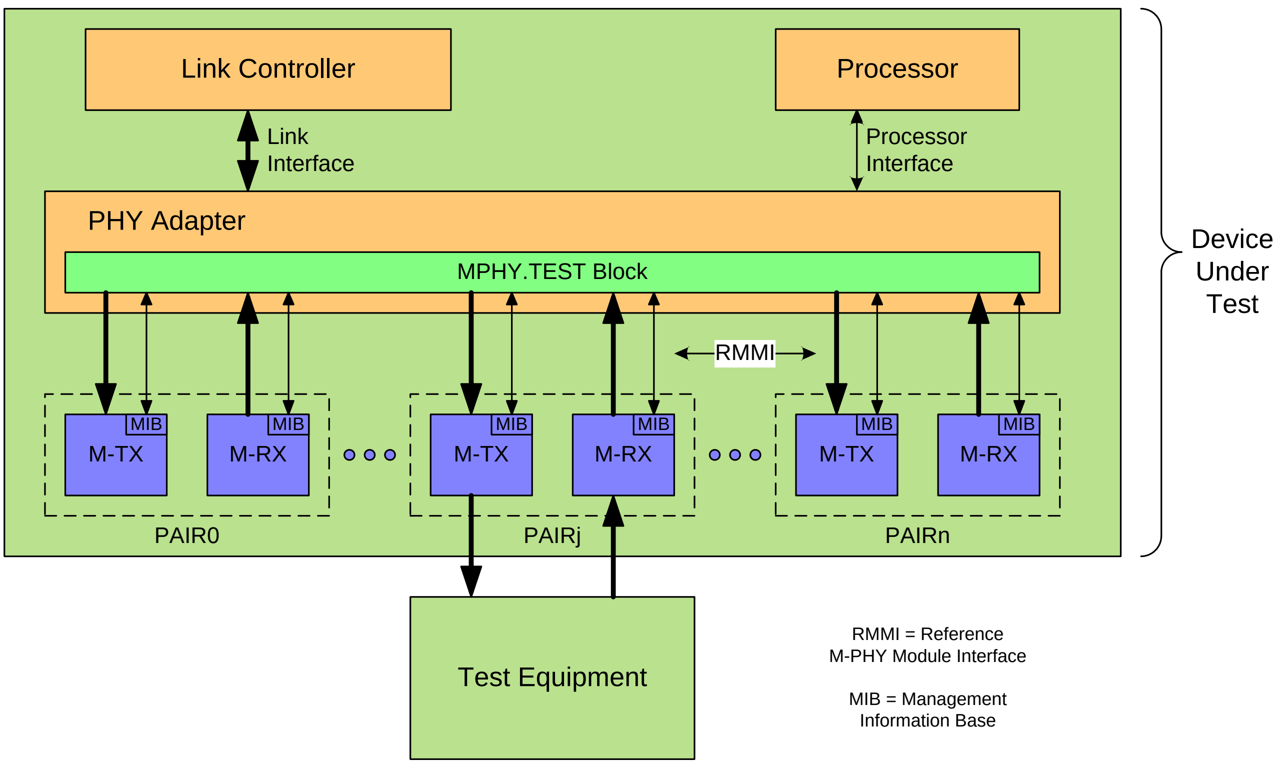


Figure 6-1 MPHY.TEST Overview

This section currently defines support for x1 LANE implementations of SSIC and the PAIR that the Test Equipment is attached to is referred to in this section as the PAIR Under Test. After issuing a LINE-RESET to the DUT, the Test Equipment transitions the DUT into the MPHY.TEST state using RRAP commands. In the MPHY.TEST state, the Test Equipment configures the M-PHY's electrical parameters and the the MPHY.TEST Block for either loopback or receive BURST testing.

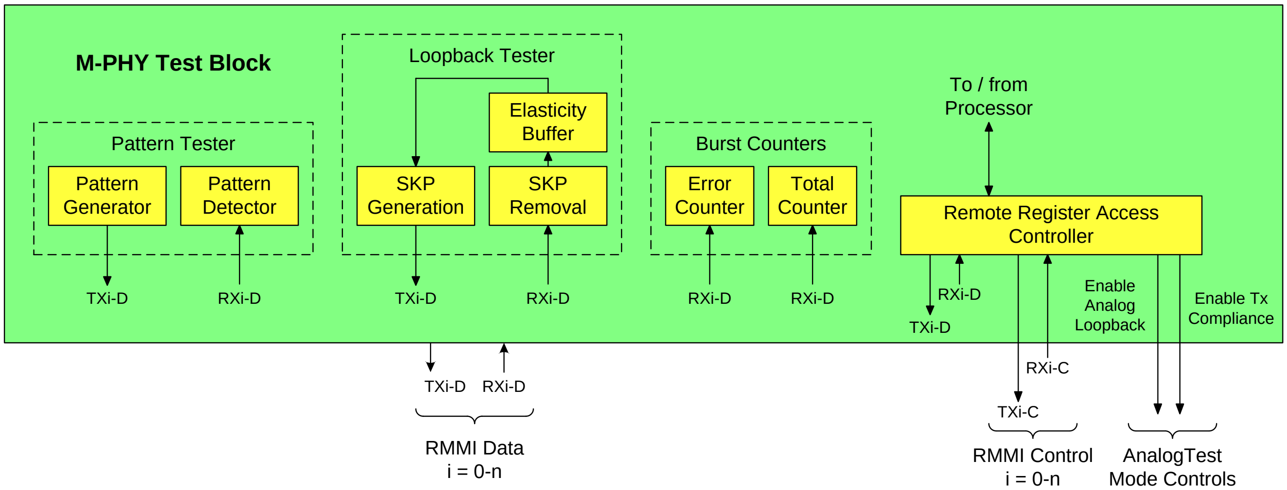


Figure 6-2 Example of an MPHY.TEST Block

Figure 6-2 provides an example of an implementation of various functional blocks in the MPHY.TEST Block.

The functional blocks shown in the Loopback Tester box, enable sensitivity and transmit signal integrity tests by receiving HS-BURSTs from the Test Equipment and looping them back. (Note: Loopback Testing and Analog Loopback are two distinct and separate modes as described in Sections 6.3 and 6.6)

The functional blocks shown in the Receive Counters block enable testing of HS-BURST entry and exit parameters such as PREPARE time, SYNC length, Tail-Of-Burst length and STALL time.

The Remote Register Access controller enables functionality related to the RRAP for the MPHY.TEST registers including the control of test modes in the M-PHY such as the Analog loopback and Tx Compliance modes.

Figure 6-3 illustrates an example of a receive BURST testing sequence including an initial PWM-BURST for DUT configuration, a series of appropriate HS-BURSTs for the actual receive BURST testing, a LINE-RESET and a final PWM-BURST that is used by the Test Equipment to read the results in the Receive Counters in the DUT.

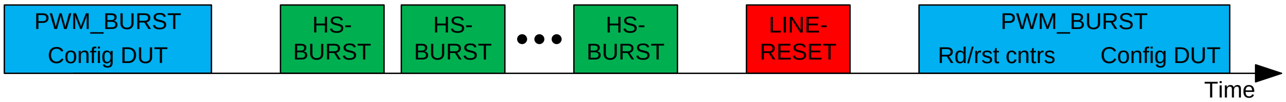


Figure 6-3 Receive BURST Test Sequence

The following sections detail the following various DUT requirements for:

- entering the MPHY.TEST state
- Loopback testing
- Receive Burst testing
- MPHY.TEST registers

6.2 Entering MPHY.TEST

The operational model for entering the MPHY.TEST state and the associated DUT requirements are described below:

- Test Equipment transitions the DUT through the Rx.Detect.Reset, Rx.Detect.Active and the Rx.Detect.LS-MODE states as described in Section 3.8.2 on the PAIR under Test.
- In the Rx.Detect.LS-MODE state, the DUT shall support the receipt of a PWM-BURST from the Test Equipment on any of the supported PAIRs.
- In the PWM-BURST mode, the DUT shall support the receipt of a RRAP Write Command to enable the transition to the MPHY.TEST state and shall issue a valid Write Response as defined in Table 2-5.

6.3 Loopback Testing

The operational model for enabling Loopback Testing and the associated DUT requirements are described below:

- Test Equipment issues a RRAP Write Command to set the LOOPBACK_EN[0] register bit as defined in Table 6-1.
- Upon receipt of the Write command, the DUT shall enable Loopback Testing for the PAIR under Test and shall issue a valid Write Response.
- Test Equipment appropriately configures the PAIR under Test for HS-MODE.
- Test Equipment closes the PWM-BURST and ensures conditions are met for a RCT to transition the DUT to the HS-MODE.
- Upon detecting the start of HS-BURST on M-RX, the DUT stall initiate a HS-BURST on the M-TX
- Upon detecting the end of HS-BURST on M-RX, the DUT shall terminate the HS-BURST on the M-TX.
- Upon initiating a HS-BURST on the M-TX of the PAIR under Test, the DUT shall loop back received HS-BURST payloads until a LINE-RESET is received.
- Upon initiating a HS-BURST on the M-TX of the PAIR under Test, the DUT may insert one or more MK0 or FLR symbols until the loop back begins.
- Both M-RX and M-TX shall use the Configuration Attribute values as programmed using RRAP.
- Data Scrambling shall be enabled by default in this mode unless specifically disabled using the corresponding RRAP command by the Tester Equipment.

The following additional requirements for the PAIR under Test shall apply during Loopback Testing:

- The M-TX shall maintain running disparity of transmitted symbols.
- The PAIR is allowed to discard received SKP ordered sets in order to avoid receiver overflow
- The PAIR is allowed to inject SKP ordered sets in the transmitted data to avoid transmit underflow
- The M-TX shall close the HS-BURST when a HS-BURST closure is detected on the M-RX.

Upon detecting the start of an HS-BURST at the M-RX, the M-TX shall start output a HS-BURST. If the PREPARE and SYNC period received on the M-RX is longer than the corresponding values in the M-TX, the M-TX may inject SKP ordered sets after the initial MK0 of the transmit payload. If the PREPARE and SYNC period received on the M-RX is shorter than the corresponding values in the M-TX, the M-TX may drop symbols after the initial MK0 of the received payload. Test Equipment can ensure that the PREPARE and SYNC period received on the M-RX is equal or greater than the corresponding values in the M-TX, to prevent the dropping of symbols by the PAIR under Test.

The size of the Elasticity Buffer shown in Figure 6-2 shall be sufficient to handle the maximum clock skew allowed by [M-PHY] between two M-PORTs, given that the Test Equipment is required to inject at least one SKP every 354 symbols.

6.4 Receive Burst Testing

The following requirements shall apply during Receive Burst Testing:

- The DUT shall implement the RX_BURST_COUNT, RX_ERR_COUNT and the RX_COUNT_RESET registers as defined in Table 6-1.
- The RX_BURST_COUNT registers shall increment each time the M-RX of the PAIR under Test transitions from HS-BURST to STALL.
- The four RX_BURST_COUNT registers implement a 4 Byte counter for the PAIR under Test with RX_BURST_COUNT_0 indicating the LSB and RX_BURST_COUNT_3 the MSB of the count.
- The RX_ERR_COUNT registers shall increment each time the M-RX of the PAIR under Test transitions from HS-BURST to STALL without detecting an MK0 during the burst.
- The four RX_ERR_COUNT registers implement a 4 Byte counter for the PAIR under Test with RX_ERR_COUNT_0 indicating the LSB and RX_ERR_COUNT_3 the MSB of the count.
- The RX_BURST_COUNT and RX_ERR_COUNT registers shall be reset when the DUT receives a RRAP Write Command that sets the RX_COUNT_RESET[0] register. These registers shall not be reset upon the receipt of a LINE-RESET.
- The RX_BURST_COUNT and RX_ERR_COUNT registers shall remain unchanged and not rollover when they have reached their maximum values.
- The RX_BURST_COUNT and RX_ERR_COUNT registers shall always be updated as described above when in the MPHY.TEST state.

6.5 Tx Compliance Mode

The operational model for enabling Tx Compliance mode and the associated DUT requirements are described below:

- Test equipment transitions the DUT to the MPHY.TEST mode prior to configuring it in Tx Compliance Mode.
- Test Equipment issues a RRAP Write Command to set the TX_COMP_MODE_EN[0] register bit as defined in Table 6-1.
- Upon receipt of the Write command, the DUT shall enable Tx Compliance mode for the PAIR under Test and shall issue a valid Write Response.
- Test Equipment closes the PWM-BURST on the M-RX of the PAIR under Test.
- Upon detecting the end of PWM-BURST on its M-RX, the DUT shall terminate the PWM-BURST on the M-TX.
- The M-TX of the PAIR under Test shall then continuously transmit the CRPAT compliance pattern as defined in [M-PHY] Annex B.1.2.
- The DUT shall remain in the Tx Compliance Mode until a LINE-RESET is received from the Test Equipment.

6.6 Analog Loopback Mode

The operational model for enabling Analog Loopback mode and the associated DUT requirements are described below:

- Test equipment transitions the DUT to the MPHY.TEST mode prior to configuring it in Analog Loopback Mode.
- Test Equipment issues a RRAP Write Command to set the ANALOG_LOOPBACK _EN[0] register bit as defined in Table 6-1.
- Upon receipt of the Write command, the DUT shall enable Analog Loopback mode for the PAIR under Test and shall issue a valid Write Response.
- Test Equipment closes the PWM-BURST on the M-RX of the PAIR under Test.

- Upon detecting the end of PWM-BURST on its M-RX, the DUT shall terminate the PWM-BURST on the M-TX.
- Subsequently all the data received on the M-RX of the Pair under Test shall be transmitted back on the M-TX of the PAIR under Test.
- This functionality is analogous to the mode defined in [M-PHY] Annex B.2.2 as “Analog Loopback” mode. Specifically a “Synchronous Loopback” mechanism is employed as described in Annex B.2.2.1 in which the recovered clock from M-RX is used to retransmit the data on the M-TX.
- The DUT shall remain in Analog Loopback Mode until a LINE-RESET is received from the Test Equipment.

6.7 MPHY.TEST Block Registers

Table 6-1 MPHY.TEST Block Registers

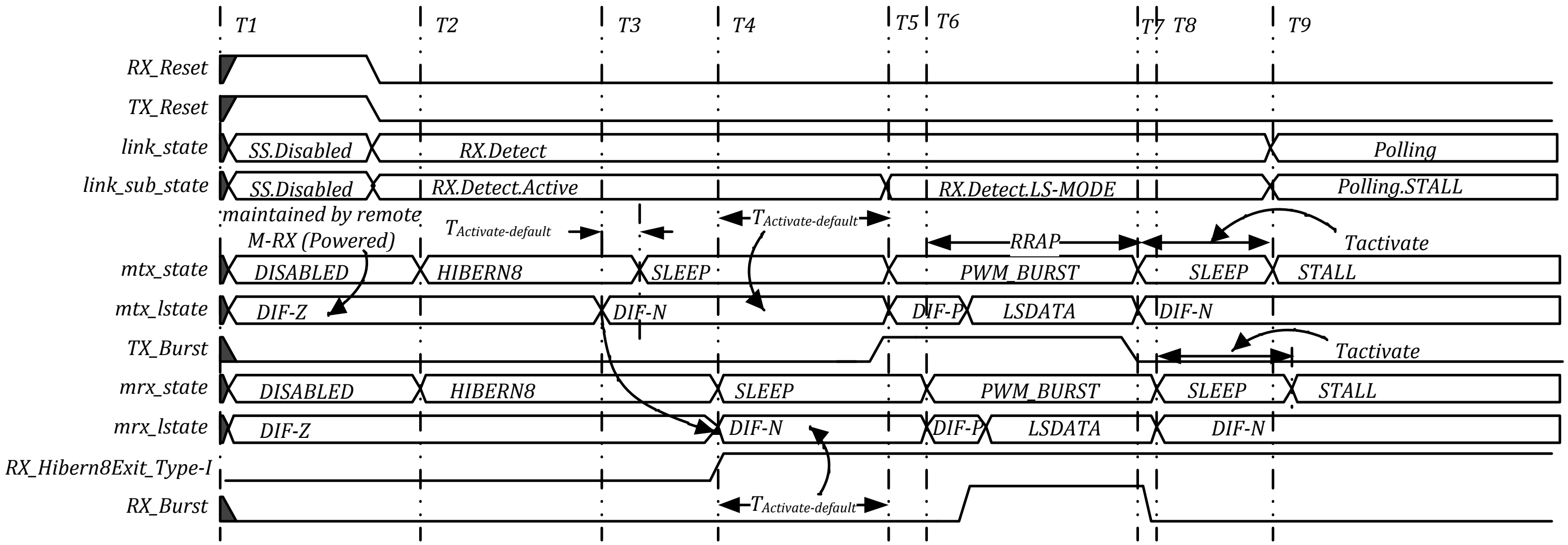
UpperAddr	LowerAddr	Register Name	Description
0xE	0x00	LOOPBACK_EN	This Register is used to enable Loopback Testing for the PAIR under Test. Read/Write Attributes: • R/W Reset Default: • Value after LINE-RESET: 0x00 Bit [0]: • Writing 1’b1 enables the loopback mode for the PAIR under Test. • Writing 1’b0 shall have no effect. Bit[7:1] Reserved. • Writes shall be ignored and Reads shall return zero values.
0xE	0x01-0x04	RX_BURST_COUNT_0 RX_BURST_COUNT_1 RX_BURST_COUNT_2 RX_BURST_COUNT_3	These Registers count the number of bursts by incrementing on each HS-BURST to STALL transition. RX_BURST_COUNT_0 is the LSB. R/W attributes: • Read Only Reset Default: • Value after LINE-RESET: Unchanged • Cleared when RX_COUNT_RESET[0] is set.

UpperAddr	LowerAddr	Register Name	Description
0xE	0x05-0x08	RX_ERR_COUNT_0 RX_ERR_COUNT_1 RX_ERR_COUNT_2 RX_ERR_COUNT_3	These Registers count the number of errors by incrementing on each HS-BURST to STALL transition for which an MK0 was not detected. RX_ERR_COUNT_0 is the LSB. R/W attributes: • Read Only Reset Default: • Value after LINE-RESET: Unchanged • Cleared when RX_COUNT_RESET[0] is set.
0xE	0x09	RX_COUNT_RESET	This register is used to reset the RX_BURST_COUNT and the RX_ERR_COUNT registers R/W attributes: • Write Only, Self Clearing Reset Default: • Value after LINE-RESET: 0x00 Bit [0]: • Writing 1’b1 resets the RX_BURST_COUNT and the RX_ERR_COUNT registers Bits [7:1]: Reserved.
0xE	0x0A	TX_COMP_MODE_EN	This register is used to enable M-TX of the PAIR under Test in TX Compliance mode. Writes to this register are undefined unless the DUT is in the MPHY.TEST state. R/W Attributes: • Write Only Reset Default: • Value after LINE-RESET: 0x00 Bit [0]: • Writing 1’b1 enables Tx Compliance Mode for the PAIR under Test • Writing 1’b0 shall be ignored and Reads shall return zero values. Bits[7:1] Reserved: • Writes shall be ignored and Reads shall return zero values.

UpperAddr	LowerAddr	Register Name	Description
0xE	0x0B	ANALOG_LOOPBACK_EN	This register is used to place the M-RX of the PAIR under Test in Analog Loopback mode. Writes to this register are undefined unless the DUT is in the MPHY.TEST state. R/W Attributes: • Write Only Reset Default: • Value after LINE-RESET: 0x00 Bit [0]: • Writing 1’b1 enables Analog Loopback Mode for the PAIR under Test • Writing 1’b0 shall be ignored and Reads shall return zero values. Bits[7:1] Reserved: • Writes shall be ignored and Reads shall return zero values.
0xE	0x0C- 0xFF	RESERVED	Reserved. Writes shall be ignored and Reads shall return zero values.

7 Timing Diagrams Appendix (Informative)

7.1 SS.DISABLED TO RX.DETECT



SS.Disabled to Rx.Detect

T1: Power On Reset, TX_Reset and RX_Reset asserted

T2: After finishing Power On Reset, DSP enters into HIBERN8

T3: DSP starts HIBERN8 exit on it's M-TX

T4: After receiving HIBERN8 exit on M-RX, USP starts HIBERN8 exit on it's M-TX

T5: After receiving HIBERN8 exit on M-RX, DSP enters into PWRM_BURST and starts issuing RRAP commands

T6: M-Rx enters PWM-BURST. During PWM-BURST the RRAP Commands and Responses are sent

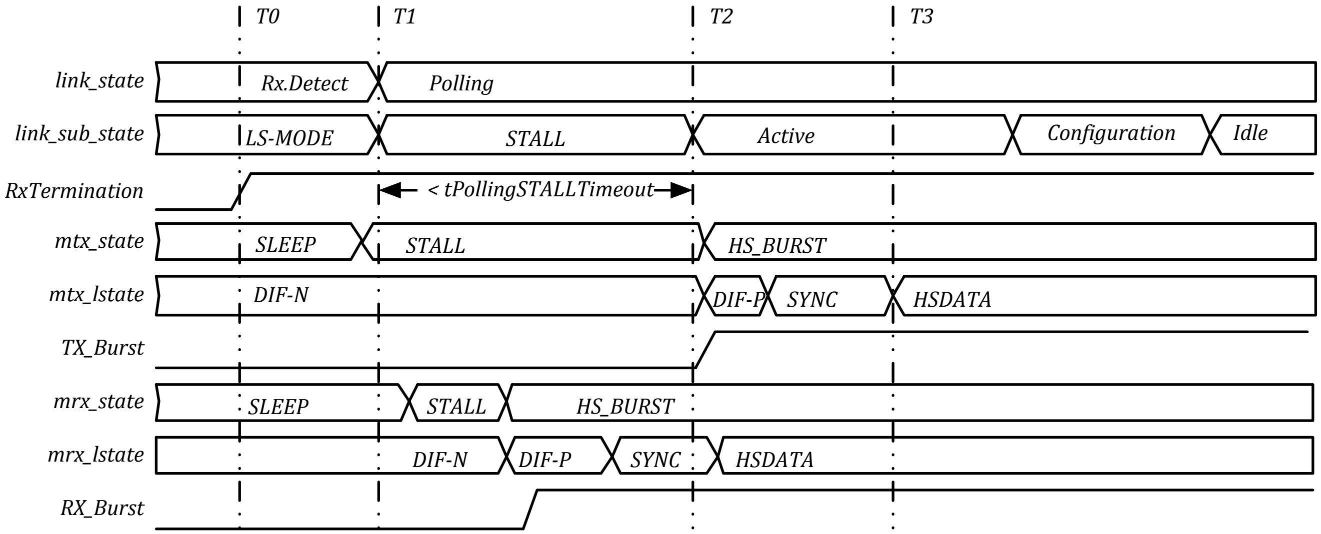
T7: DSP and USP finished all RRAP commands. DSP initiates exit from PWM_BURST and enters into SLEEP

T8: Upon receiving PWM_BURST exit on M-RX, USP intiates PWM_BURST exit on it's M-TX and enters into SLEEP
T9: After entering SLEEP, both DSP and USP executes RCT and moves to STALL

Note:

- *Time between T3 and T4 shown in figure is illustrative only. Spec does not define this time interval*
- *Tactivate-default is the reset value of TX_Min_ActivateTime = 1.5ms as per MPHY spec*
- *Tactivate is 100us as per SSIC profile definition*
- *This diagram is for DSP only.*

7.2 RX.DETECT TO POLLING



Rx.Detect to Polling

T0: RRAP has completed successfully and PA is ready for connect, Indicates termination present to link layer.

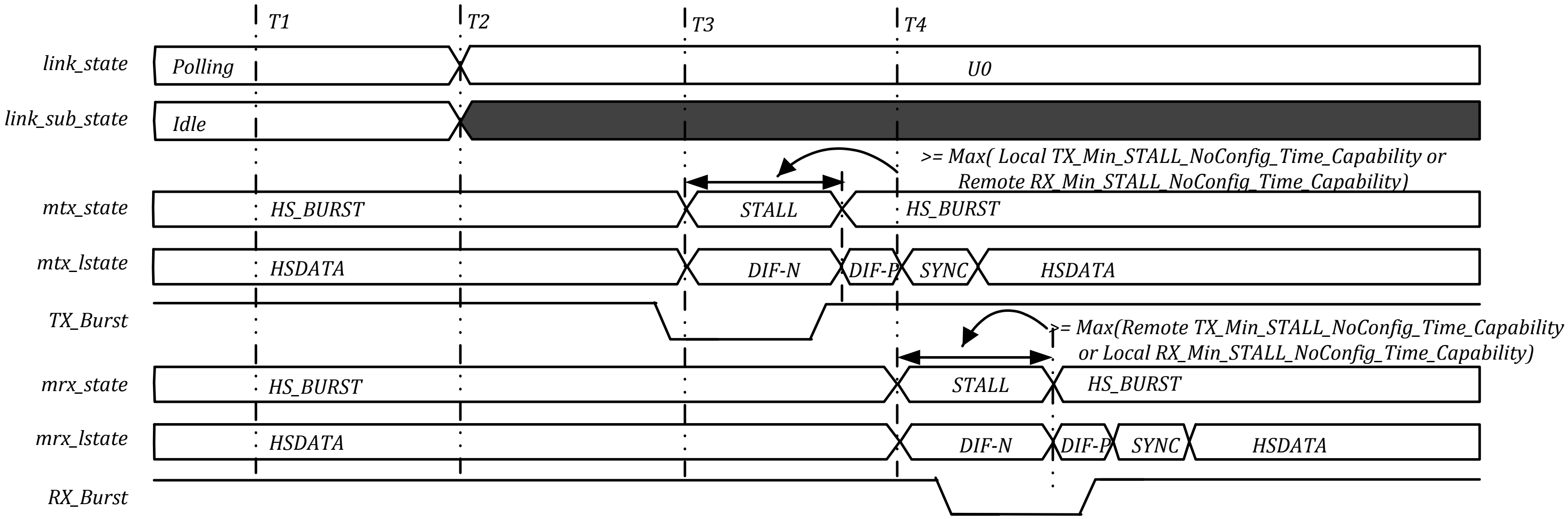
T1: Link detects termination and moves to Polling state

T2: Link enters into Polling.Active state and starts sending TS1 sets, PA puts M-TX into HS_BURST state

T3: Both link partners are in Polling with it's M-TX and M-RX in HS_BURST and exchanging Training sets

Note: RxTermination is conceptual signal indicating remote receiver is present

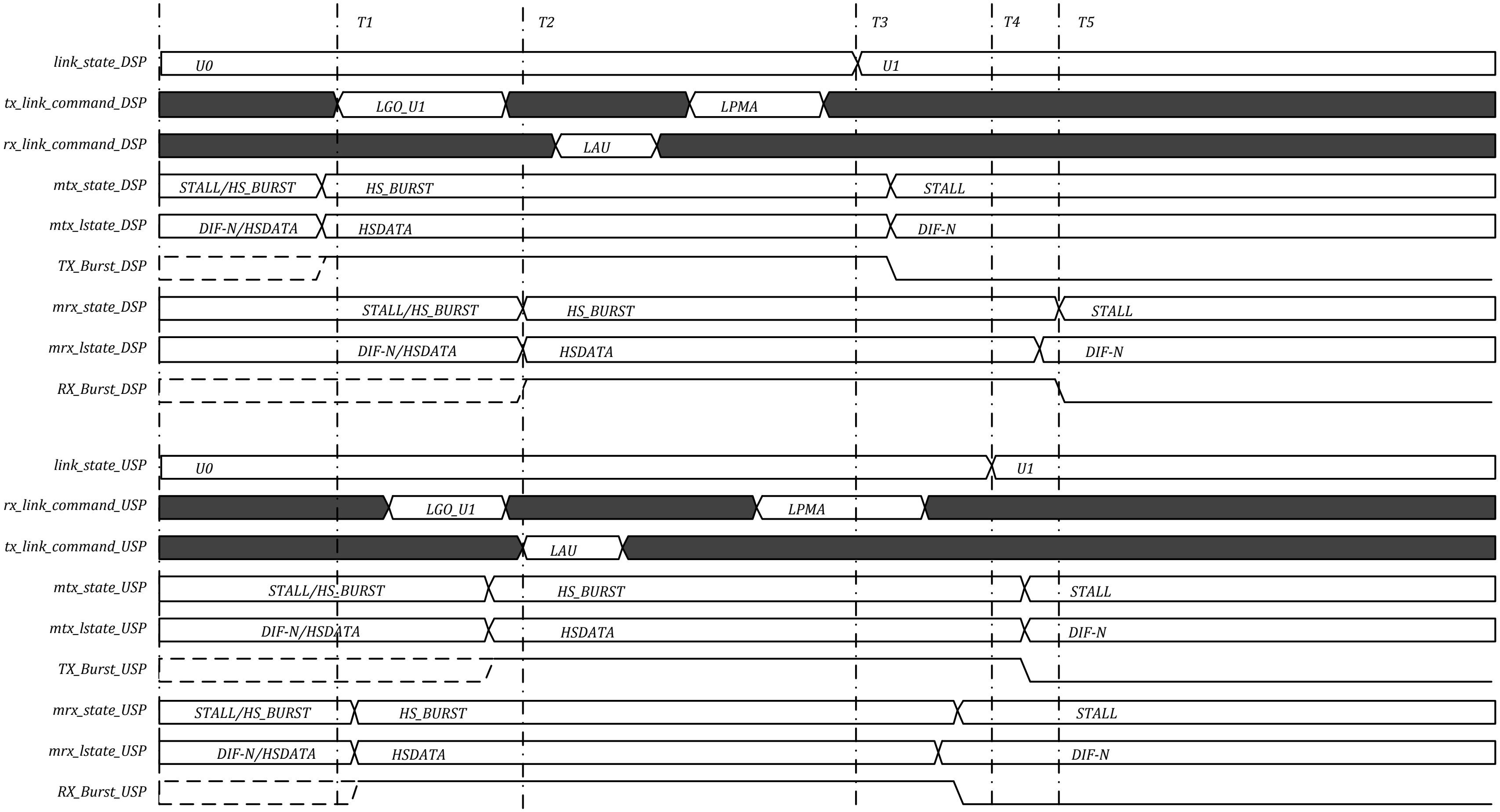
7.3 POLLING TO U0



Polling to U0

T1: Both Link partner are in Polling state. Both M-TX and M-RX in HS_BURST state.
T2: After successful handshake of TS1/TS2/Logical IDLE, Both link partner enters into U0 state.
T3: M-TX transitions to the STALL state when link is not sending any packets other than logical IDLE symbol
T4: Independently the M-RX transitions to the STALL state when the link partner's M-TX enter the STALL state

7.4 U0 TO U1

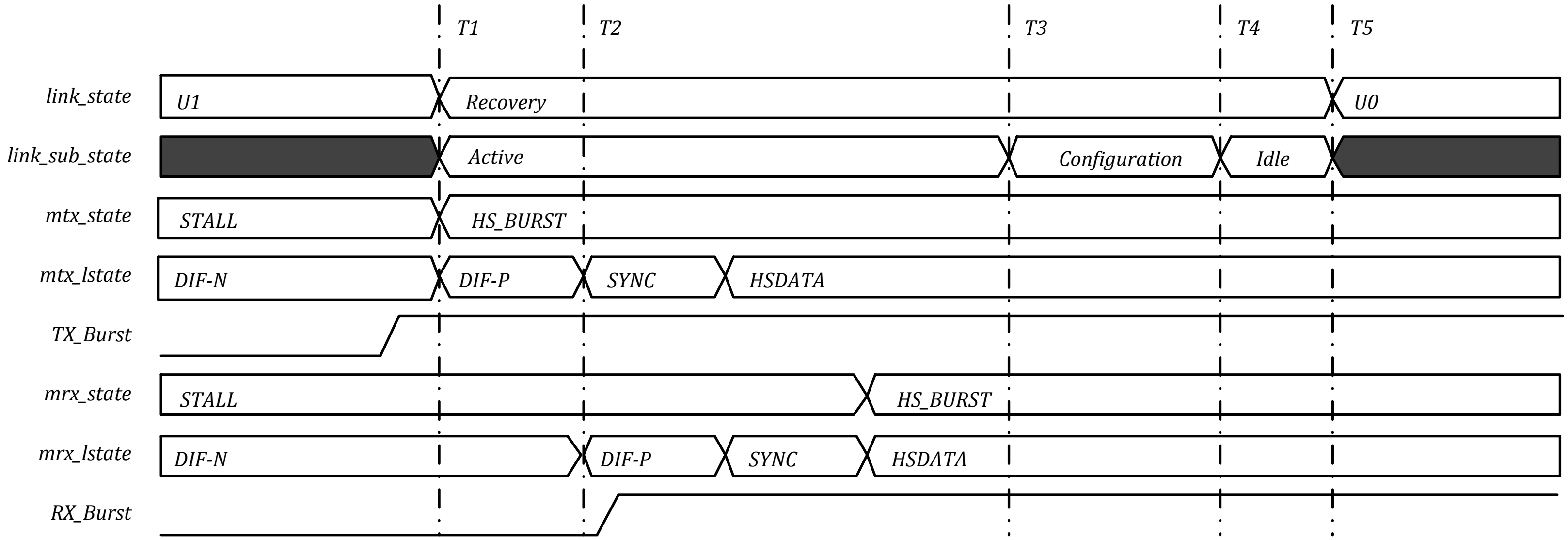


U0 to U1

T1: DSP link sends initiates U1 entry by sending LGO_U1 and disables its M-TX entering in to STALL
T2: USP link accepts U1 entry by sending LAU and disables its M-TX entering in to STALL
T3: After receiving LAU, DSP sends LPMA, enters in U1and puts its M-TX in to STALL
T4: After receiving LPMA USP enters in U1 and puts its M-TX in to STALL
T5: U1 entry completed. Both DSP and USP has its M-TX/M-RX in STALL

Note: link shall not initiates U1 exit until both M-TX (local) and M-RX (local) is in STALL. This is to ensure that both link partner are in U1.
Note: In this diagram, U1 entry is initiated by DSP but USP can also initiate U1 entry in a same way.

7.5 U1 TO U0



U1 to U0

T1: Link partner 1 intiates U1 exit by making sure that it's M-RX and M-TX is in STALL

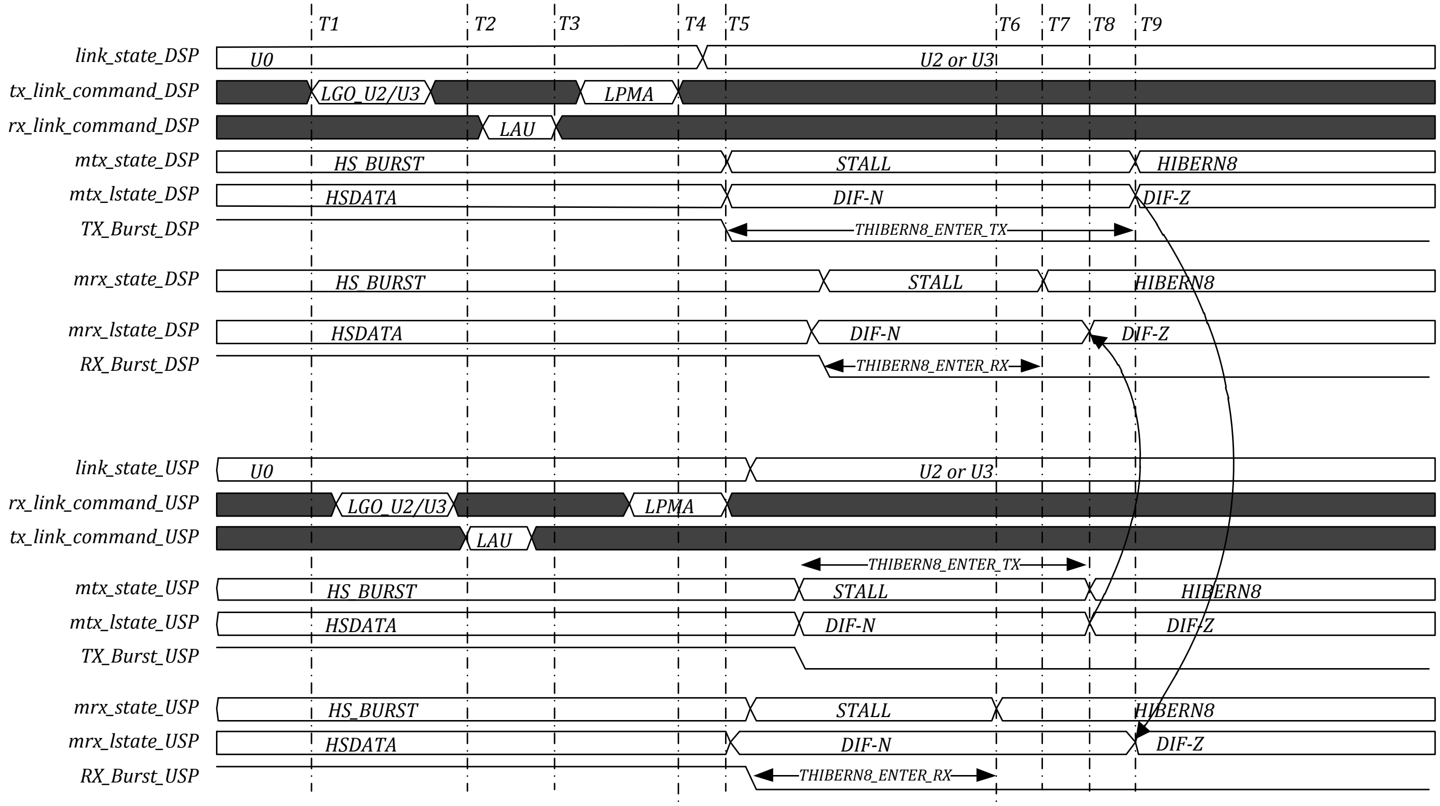
T2: Link partner 2 detects U1 exit on it's M-RX and starts HS_BURST on it's M-TX.

T3: Both Link partners are in HS_BURST. Link enters Recovery.Configuration after successful TS1 handshake.

T4: Link enters Recovery.Idle after successful TS2 handshake.

T5 Link enters U0 after successful LIDLE handshake.

7.6 U0 TO U2/U3



U0 to U2/U3

T1: DSP send LGO_U2 or LGO_U3 and disables STALL entry until it receives LXU or enters into U2/U3 state
T2: USP accepts low power entry as per section 3.8.4.1 "Exit from U0"
T3: The DSP, upon receipt of the LAU, configures M-TX and M-RX for HIBERN8 entry and responds with LPMA as per 3.8.4.1 "Exit from U0"
T4: After sending LPMA, DSP enters into U2/U3 and put it's M-TX into STALL
T5: After receiving LPMA, USP enters into U2/U3 and put it's M-TX into STALL
T6: USP M-RX enters into HIBERN8 within THIBERN8_ENTER_RX time
T7: DSP M-RX into HIBERN8 within THIBERN8_ENTER_RX time
T8: USP M-TX enters into HIBERN8 within THIBERN8_ENTER_TX time
T9: DSP M-TX enters into HIBERN8 within THIBERN8_ENTER_TX time

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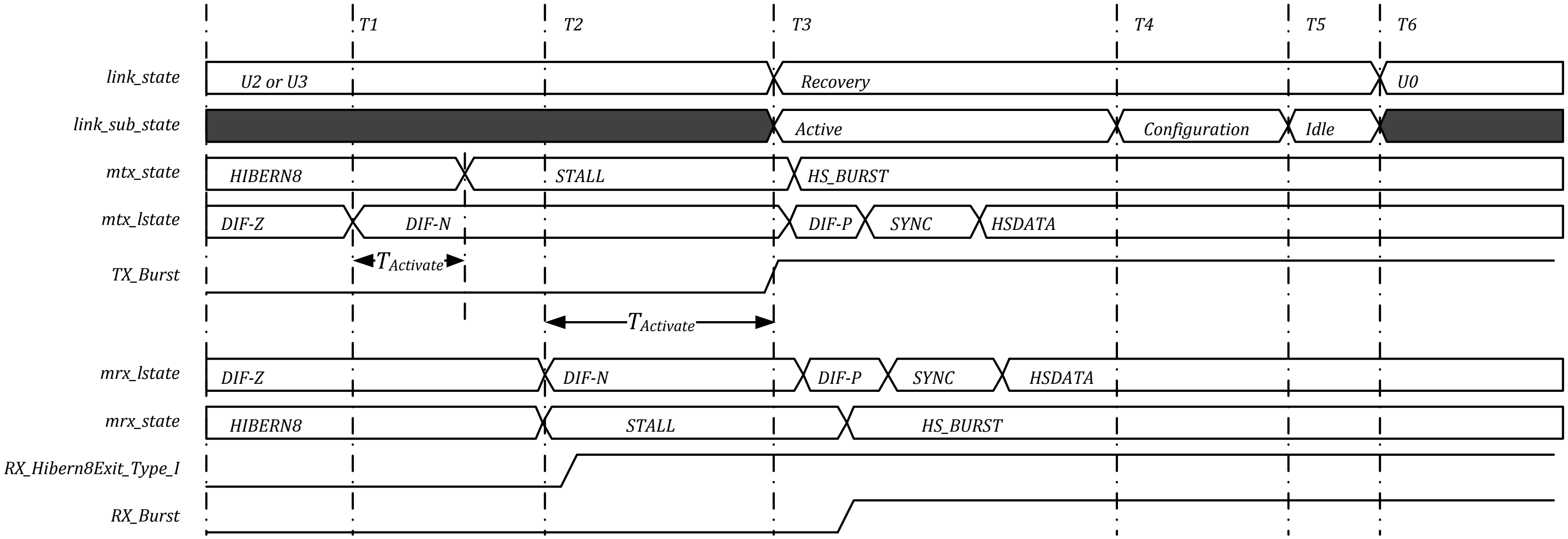
Note: In this diagram, U2 entry is initiated by DSP but USP can also initiate U2 entry. However U3 entry can be initiated by DSP only

7.7 U2/U3 TO U0



U2/U3 to U0

T1: Link partner 1 intiates U2/U3 exit by making sure that it's M-RX and M-TX is in HIBERN8 for atleast Thibern8 time

T2: Link partner 2 detects HIBERN8 exit on it's M-RX and starts HIBERN8 exit on it's M-TX.

T3: Link partner 2 detects STALL exit on it's M-RX and starts STALL exit on it's M-TX.

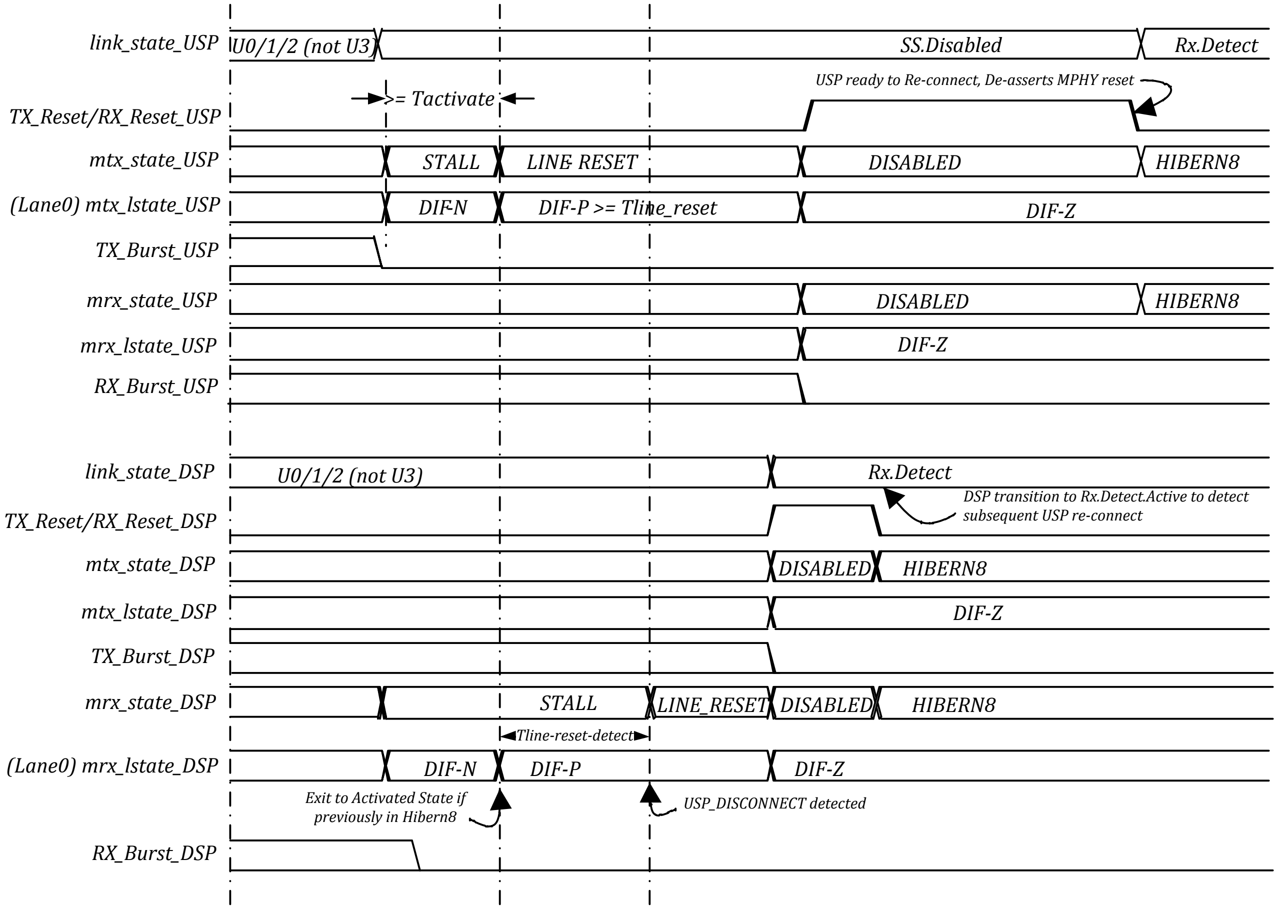
T4: Both Link partners are in HS_BURST. Link enters Recovery.Configuration after successful TS1 handshake.

T5: Link enters Recovery.Idle after successful TS2 handshake.

T6 Link enters U0 after successful LIDLE handshake.

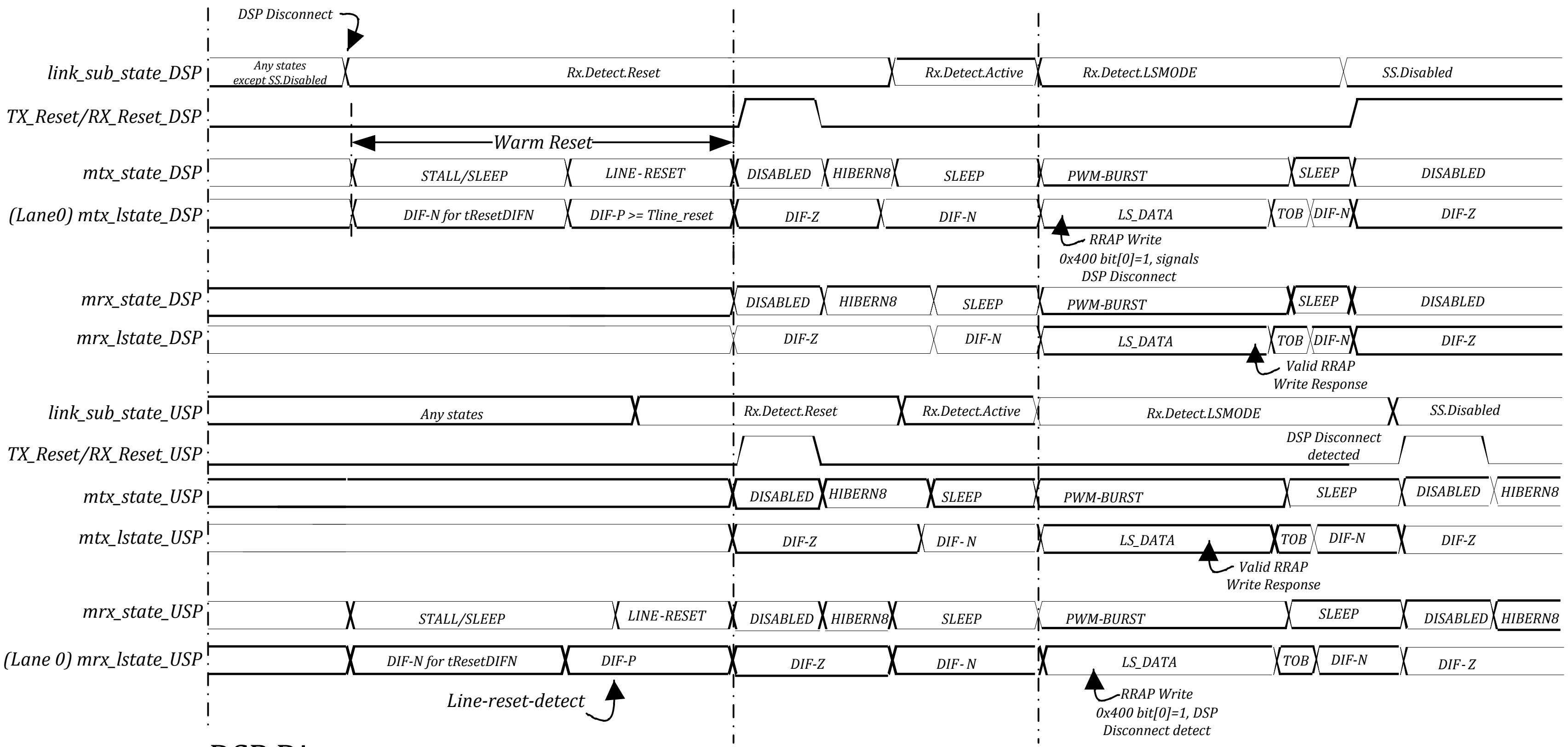
Note: TActivate is 100us as per SSIC profile definition

7.8 USP Disconnect



USP Disconnect

7.9 DSP Disconnect



DSP Disconnect

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