Ujjawal

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Education

B. Tech, Electronics and Instrumentation
VIT University, Vellore (Class of 2015) 78%
AISSCE (CBSE)
Delhi Public School, Patna (Class of 2010) 83.6%
AISSE (CBSE)
Delhi Public School, Patna (Class of 2008) 87.6%

Technical Skill Set

Programming Languages: C/C++, Python
Internet Technologies: HTML5, CSS3
Designing Tools: Adobe Photoshop

Experience

South Bihar Power Distribution Corporation
Intern – (June 2013)
The interns were required to study and analyze the energy meters. The construction, working, installation, testing and extracting data from them.

International Society of Automation (ISA-VIT)
Core Member (March 2012 to April 2013)
The job included technical and management work of the society including Website and Poster designing and organizing workshops.

Projects

Personal Branding Page
July 2014
- Used Flexible Box Model Layout
- Responsive Page and Cross Browser Support

Technologies Used – HTML5, CSS3
URL: www.ujjawal.in

Design of Low-Power Wide-Range Delay Locked Loop in CMOS
July 2013 to November 2013
This project consist of designing a Delay Locked Loop (DLL) suitable for low power and low-voltage operations. Generation and distribution of clock signals inside the VLSI system is the most important problem in the design of VLSI systems.
Software Used: Cadence

Areas of Interest

Web Intelligence and Big Data, Computer Networks, Website Development

Achievements

- **Chitra Visharad Pratham Khand**, Pracheen Kala Kendra, Chandigarh
- **Design Member** of **'graVITas'** the Annual Tech Fest of VIT University, 2012
- **Scholar's Memento Award** for outstanding academic performance for three consecutive years
- **State Topper,** English in IAIS 2009 conducted by the University of New South Wales
- Third Prize, Inter-School **Debate Competition** organized by RBI Patna, 2009