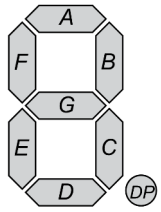
CSARCH1

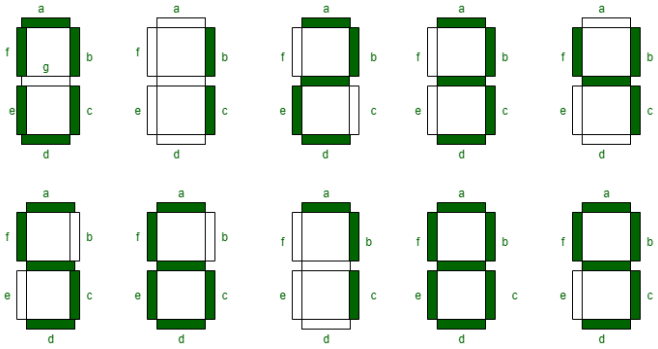
Design Exercise 1: (2,1,2,6) to 7-segment converter

Design exercise 1:



Given an input encoded in (2,1,2,6) code with variables W,X,Y,Z. design a circuit that outputs the number in a 7-segment display. The 7-segment display has seven light-emitting segments (A, B, C, D, E, F, G). Each segment will light up when the value is 1. It should output nothing if the code is invalid (i.e. for code 1111) and output the corresponding number when it is valid (i.e. B and C should light up when the code is 0100). Note that you can have multiple codes with the same output. Submit a report regarding your design process. **You can only use logic gates for now.**

The numbers are shown as follows for your reference



INSTRUCTIONS

Design a digital circuit and implement in circuitverse. You will need to demonstrate your circuit is running in CircuitVerse with your instructor. Afterwards, export your circuit to verilog, and run the Verilog file in iverilog. You can find a tutorial of iverilog here and here.

Documentation Deadline: February 7 (7pm). You should have demonstrated the Circuit Verse file to your instructor before that.

Make sure you sign up on a Design Exercise #1 group in Canvas. Maximum of 3 students.

Checking:

1. Present your Circuit Verse Design to your instructor.

Submission:

2. Verilog File (.v)
3. Verilog Testbench (_tb.v)
4. Circuit Verse File (.cv)
5. PDF of your documentation of the design process. This should include everything necessary during your design process (i.e. truth table, equations, logic circuit, waveforms, etc.)

Grading System:

- CircuitVerse Demo [30%] – output to be determined by your instructor
- Running Verilog Design [30%] – all possibilities outputs
- Documentation [40%]
- Bonus [5%] to the group with the least number of gates in each section. If there's a tie, the bonus is divided with the number of groups.