Discovery Series #05: Software architecture_memory

Started: Sep 26 at 5:02pm

Quiz Instructions

Reminding you of the academic honor pledge that you signed.

*****Strongly recommend that your SASM is working before you proceed with the discovery series*****

This discovery series is all about how x86-64 views memory.

Please note the following instructions:

1.) Choose the best answer if the question is multiple choice.

2.) For fill in the blank:

(a) DO NOT include radix prefix (i.e., 0x12CA is incorrect) or radix suffix (i.e. 12CAh is incorrect).

(b) NO space between digits (i.e., 1101 0100 is incorrect).

(c) Hex digit in CAPITAL letter (i.e., 12ca is incorrect).

Question 1 1 pts

1007	7F
1006	12
1005	78
1004	67
1003	34
1002	EF
1001	CD
1000	AB

If an Intel x86-64 architecture based processor fetches a word data at address 1002, what is that data?

34EF

Question 2 1 pts

1010	FF
100F	F5
100E	D4
100D	C3
100C	E2
100B	D1
100A	BA
1009	FE
1008	CA
1007	7F
1006	12
1005	78
1004	67
1003	34
1002	EF
1001	CD
1000	AB

If big-endian ordering is used and a processor fetches a 16-bit data at address 1004, what is that data?

6778

Question 3 1 pts

label	address	byte data in hex
	1007	09
	1006	00
	1005	09
	1004	00
	1003	09
	1002	00
	1001	09
var1	1000	00

The above memory is based on the declaration below:

section .data

var1 times 4 dw 9

○ True

◉ False

Question 4 1 pts

1007	7F
1006	12
1005	78
1004	67
1003	34
1002	EF
1001	CD
1000	AB

If an Intel x86-64 architecture based processor fetches a double-word data at address 1004, what is that data?

7F127867

Question 5 1 pts

label	address	byte data in hex
	1007	00
	1006	08
	1005	00
	1004	08
	1003	00
	1002	08
	1001	00
var1	1000	08

The above memory is based on the declaration below:

section .data

var1 times 4 dw 8

◉ True

○ False

Question 6 1 pts

1010	FF
100F	F5
100E	D4
100D	C3
100C	E2
100B	D1
100A	BA
1009	FE
1008	CA
1007	7F
1006	12
1005	78
1004	67
1003	34
1002	EF
1001	CD
1000	AB

If an Intel x86-64 architecture based processor fetches a quad-word data at address 1000, what is that data?

7F12786734EFCDAB

Question 7 1 pts

This pseudo-instruction is use to allocate and initialize a 16-bit data in the memory.

○
DB

○
none of the choices

○
DQ

○
DD

◉
DW

Question 8 1 pts

Intel x86-64 architecture uses what type of multi-byte ordering?

○
Big endian

◉
Little endian

○
Hybrid endian

○
none of the choices

Question 9 1 pts

Given the data declaration below:

```
section .text
var1 db 0x12, 0x34, 0x56, 0x78
var2 dw 0x1234, 0x5678, 0x9ABC, 0xDEF0
var3 dd 0x12345678, 0x9ABCDEF0
var4 dq 0x123456789ABCDEF0, 0x8877665544332211
```

What *gdb* command is used to display the 1st element of *var4*?

note: *variable_name+1* means the address of the *variable_name*+1

○
x/1xw var4

○
x/1xb var4

○
none of the choices

◉
x/1xg var4

Question 10 1 pts

This pseudo-instruction is use to allocate and initialize a 32-bit data in the memory

○
none of the choices

○
DW

○
DB

○
DQ

◉
DD

Quiz saved at 5:22pm Submit Quiz