Submitted in partial fulfillment of the course requirements

For CSARCH1

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Chapter 1: The Project and Its Background

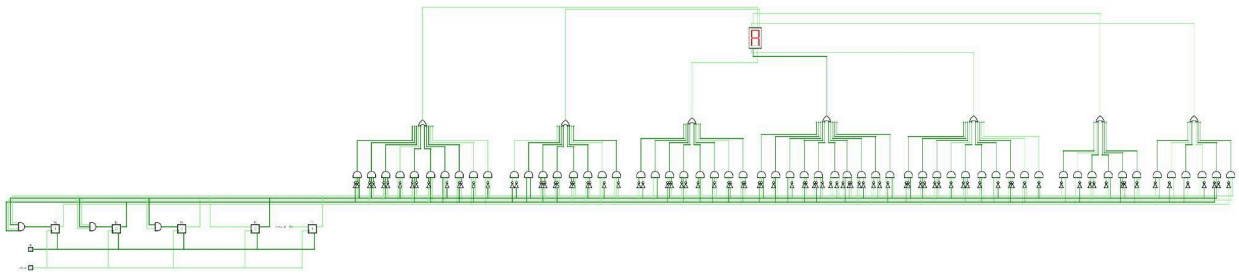
Introduction

The Euler's totient function, also known as the phi (φ) function, is a number theoretic function that has a deep relationship with prime numbers and the order of integers. It is defined as the number of positive integers less than a given integer n that are coprime to n. For example, the totient of 10 is four because four positive integers are less than 10 (1, 3, 7, and 9) that are co-prime to 10 (*Euler's Totient Function and Euler's Theorem*, n.d.).

The project uses Euler's Totient Function to create a counter showing the Totient numbers from 1 to 16. It will be tested against a test bench to determine whether the project waveform matches the waveform of the test bench.

Chapter 2: Circuit Design

Logic Circuit



The circuit diagram above shows how Euler's Totient Function counter uses logic gates consisting of AND gates, OR gates, NOT gates, and T Flip-Flops with a clock and a reset input.

Chapter 3: Verilog Observations

Verilog Code

```
module TestBench();

 reg R, clk_0;



 Main DUT0(clk_0, R);

 always begin
  #10
  clk_0 = 0;
  #10
  clk_0 = 1;
 end

 initial begin
  R = 0;

  #15

  #10
```

```
    $finish;

  end
endmodule

*/

module EulerTotient(R, clk_0, A, B, C, D, E, F, G);
  input R, clk_0;
  output A, B, C, D, E, F, G;
  wire T4_Q, and_58_out, T5_Q, not_88_out, and_54_out, or_6_out, and_57_out, not_82_out,
and_52_out, not_78_out, and_49_out, or_5_out, not_76_out, and_48_out, and_47_out,
not_74_out, and_46_out, and_45_out, or_4_out, and_44_out, and_43_out, not_68_out,
and_41_out, not_66_out, and_40_out, not_61_out, and_37_out, and_35_out, or_3_out,
and_34_out, and_33_out, not_51_out, and_32_out, not_49_out, and_31_out, not_46_out,
and_30_out, and_29_out, not_42_out, and_27_out, and_23_out, or_2_out, and_22_out,
not_34_out, and_20_out, not_32_out, and_19_out, and_17_out, or_1_out, and_16_out,
and_15_out, not_21_out, and_14_out, not_19_out, and_13_out, not_16_out, and_12_out,
and_9_out, or_0_out, and_8_out, and_7_out, not_8_out, and_5_out, not_6_out, and_4_out,
not_2_out, and_1_out, not_86_out, and_53_out, and_56_out, not_83_out, and_55_out,
and_51_out, and_50_out, not_75_out, not_72_out, not_70_out, and_42_out, not_59_out,
and_36_out, not_58_out, not_47_out, not_44_out, and_28_out, not_40_out, and_26_out,
```

```
not_38_out, not_36_out, and_21_out, not_29_out, and_18_out, not_20_out, not_17_out,
and_11_out, not_14_out, and_10_out, not_12_out, not_10_out, and_6_out, not_0_out,
and_0_out, T1_Q, T2_Q, and_60_out, T3_Q, and_59_out, not_84_out, not_81_out,
not_79_out, not_71_out, and_39_out, not_63_out, and_38_out, not_60_out, not_56_out,
not_54_out, not_45_out, not_41_out, not_35_out, not_33_out, and_25_out, not_27_out,
and_24_out, not_22_out, not_18_out, not_11_out, and_3_out, not_3_out, and_2_out,
not_1_out, not_85_out, not_80_out, not_73_out, not_69_out, not_65_out, not_55_out,
not_52_out, not_50_out, not_43_out, not_37_out, not_30_out, not_28_out, not_25_out,
not_23_out, not_15_out, not_13_out, not_9_out, not_5_out, not_89_out, not_87_out,
not_77_out, not_67_out, not_64_out, not_62_out, not_57_out, not_53_out, not_48_out,
not_39_out, not_31_out, not_26_out, not_24_out, not_7_out, not_4_out, const_0;
  TflipFlop T4(T4_Q, , clk_0, and_59_out, R, , );
  assign and_58_out = T2_Q & T1_Q & T3_Q & T4_Q;
  TflipFlop T5(T5_Q, , clk_0, and_58_out, R, , );
  assign not_88_out = ~T5_Q;
  assign and_54_out = not_88_out & T3_Q & T1_Q;
  assign or_6_out = and_52_out | and_55_out | and_56_out | and_57_out | and_53_out |
and_54_out;


     always @ (*)
       $display("SevenSegDisplay:SevenSegDisplay_0.abcdefg. = %b%b%b%b%b%b%b%b}",
              or_0_out, or_1_out, or_2_out, or_3_out, or_4_out, or_5_out, or_6_out, );
  assign and_57_out = T5_Q & not_85_out;
```

```
  assign not_82_out = ~T5_Q;
  assign and_52_out = not_82_out & T2_Q;
  assign not_78_out = ~T5_Q;
  assign and_49_out = not_78_out & T3_Q & T2_Q;
  assign or_5_out = and_46_out | and_47_out | and_48_out | and_49_out | and_50_out |
and_51_out;
  assign not_76_out = ~T5_Q;
  assign and_48_out = not_76_out & T3_Q & not_77_out;
  assign and_47_out = T5_Q & not_75_out;
  assign not_74_out = ~T5_Q;
  assign and_46_out = not_74_out & T4_Q;
  assign and_45_out = T5_Q & not_73_out & T1_Q;
  assign or_4_out = and_36_out | and_37_out | and_38_out | and_39_out | and_40_out |
and_41_out | and_42_out | and_43_out | and_44_out | and_45_out;
  assign and_44_out = T5_Q & not_72_out & T1_Q;
  assign and_43_out = T5_Q & not_70_out & not_71_out;
  assign not_68_out = ~T5_Q;
  assign and_41_out = not_68_out & T4_Q & T3_Q;
  assign not_66_out = ~T5_Q;
  assign and_40_out = not_66_out & T4_Q & not_67_out;
  assign not_61_out = ~T5_Q;
  assign and_37_out = not_61_out & T2_Q & not_62_out;
  assign and_35_out = not_58_out & T5_Q & T2_Q & T1_Q;
```

```
  assign or_3_out = and_26_out | and_27_out | and_28_out | and_29_out | and_30_out |
and_31_out | and_32_out | and_33_out | and_34_out | and_35_out;
  assign and_34_out = not_56_out & T5_Q & T2_Q & not_57_out;
  assign and_33_out = not_54_out & T5_Q & not_55_out & T1_Q;
  assign not_51_out = ~T5_Q;
  assign and_32_out = T4_Q & not_51_out & not_52_out & not_53_out;
  assign not_49_out = ~T5_Q;
  assign and_31_out = T3_Q & not_49_out & not_50_out & T1_Q;
  assign not_46_out = ~T5_Q;
  assign and_30_out = not_47_out & not_46_out & T2_Q & not_48_out;
  assign and_29_out = T5_Q & not_44_out & not_45_out;
  assign not_42_out = ~T5_Q;
  assign and_27_out = not_42_out & T4_Q & T3_Q;
  assign and_23_out = T5_Q & not_38_out & not_39_out;
  assign or_2_out = and_24_out | and_25_out | and_18_out | and_19_out | and_20_out |
and_21_out | and_22_out | and_23_out;
  assign and_22_out = T5_Q & not_36_out & not_37_out;
  assign not_34_out = ~T5_Q;
  assign and_20_out = not_34_out & T4_Q & T1_Q;
  assign not_32_out = ~T5_Q;
  assign and_19_out = not_32_out & T4_Q & not_33_out;
  assign and_17_out = T5_Q & T3_Q & not_26_out;
  assign or_1_out = and_10_out | and_11_out | and_12_out | and_13_out | and_14_out |
```

```
and_15_out | and_16_out | and_17_out;

  assign and_16_out = T5_Q & T3_Q & not_25_out;

  assign and_15_out = T5_Q & not_23_out & not_24_out;

  assign not_21_out = ~T5_Q;

  assign and_14_out = not_21_out & not_22_out & T1_Q;

  assign not_19_out = ~T5_Q;

  assign and_13_out = not_19_out & not_20_out & T1_Q;

  assign not_16_out = ~T5_Q;

  assign and_12_out = not_16_out & not_17_out & not_18_out;

  assign and_9_out = T5_Q & not_13_out & T1_Q;

  assign or_0_out = and_0_out | and_1_out | and_2_out | and_3_out | and_4_out | and_5_out |
and_6_out | and_7_out | and_8_out | and_9_out;

  assign and_8_out = T5_Q & not_12_out & T1_Q;

  assign and_7_out = T5_Q & not_10_out & not_11_out;

  assign not_8_out = ~T5_Q;

  assign and_5_out = not_8_out & T4_Q & T3_Q;

  assign not_6_out = ~T5_Q;

  assign and_4_out = not_6_out & T4_Q & not_7_out;

  assign not_2_out = ~T5_Q;

  assign and_1_out = not_2_out & T2_Q & not_89_out;

  assign not_86_out = ~T4_Q;

  assign and_53_out = not_86_out & T2_Q & not_87_out;

  assign and_56_out = T4_Q & not_84_out;
```

```
assign not_83_out = ~T4_Q;

assign and_55_out = not_83_out & T3_Q;

assign and_51_out = T4_Q & not_81_out & T1_Q;

assign and_50_out = T4_Q & not_79_out & not_80_out;

assign not_75_out = ~T4_Q;

assign not_72_out = ~T4_Q;

assign not_70_out = ~T4_Q;

assign and_42_out = T4_Q & T3_Q & not_69_out;

assign not_59_out = ~T4_Q;

assign and_36_out = not_59_out & not_60_out & T2_Q;

assign not_58_out = ~T4_Q;

assign not_47_out = ~T4_Q;

assign not_44_out = ~T4_Q;

assign and_28_out = T4_Q & T3_Q & not_43_out;

assign not_40_out = ~T4_Q;

assign and_26_out = not_40_out & not_41_out & T2_Q;

assign not_38_out = ~T4_Q;

assign not_36_out = ~T4_Q;

assign and_21_out = T4_Q & not_35_out & T1_Q;

assign not_29_out = ~T4_Q;

assign and_18_out = not_29_out & not_30_out & not_31_out;

assign not_20_out = ~T4_Q;

assign not_17_out = ~T4_Q;
```

```
assign and_11_out = T4_Q & T2_Q;

assign not_14_out = ~T4_Q;

assign and_10_out = not_14_out & not_15_out;

assign not_12_out = ~T4_Q;

assign not_10_out = ~T4_Q;

assign and_6_out = T4_Q & T3_Q & not_9_out;

assign not_0_out = ~T4_Q;

assign and_0_out = not_0_out & not_1_out & T2_Q;

TflipFlop T1(T1_Q, , clk_0, const_0, R, , );

TflipFlop T2(T2_Q, , clk_0, T1_Q, R, , );

assign and_60_out = T2_Q & T1_Q;

TflipFlop T3(T3_Q, , clk_0, and_60_out, R, , );

assign and_59_out = T3_Q & T2_Q & T1_Q;

assign not_84_out = ~T3_Q;

assign not_81_out = ~T3_Q;

assign not_79_out = ~T3_Q;

assign not_71_out = ~T3_Q;

assign and_39_out = T3_Q & not_65_out & T1_Q;

assign not_63_out = ~T3_Q;

assign and_38_out = not_63_out & T2_Q & not_64_out;

assign not_60_out = ~T3_Q;

assign not_56_out = ~T3_Q;

assign not_54_out = ~T3_Q;
```

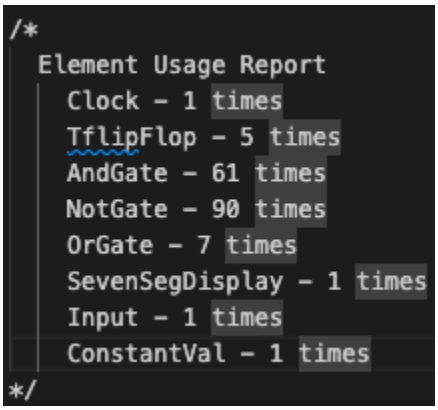
```
assign not_45_out = ~T3_Q;

assign not_41_out = ~T3_Q;

assign not_35_out = ~T3_Q;

assign not_33_out = ~T3_Q;

assign and_25_out = T3_Q & T2_Q;

assign not_27_out = ~T3_Q;

assign and_24_out = not_27_out & not_28_out;

assign not_22_out = ~T3_Q;

assign not_18_out = ~T3_Q;

assign not_11_out = ~T3_Q;

assign and_3_out = T3_Q & not_5_out & T1_Q;

assign not_3_out = ~T3_Q;

assign and_2_out = not_3_out & T2_Q & not_4_out;

assign not_1_out = ~T3_Q;

assign not_85_out = ~T2_Q;

assign not_80_out = ~T2_Q;

assign not_73_out = ~T2_Q;

assign not_69_out = ~T2_Q;

assign not_65_out = ~T2_Q;

assign not_55_out = ~T2_Q;

assign not_52_out = ~T2_Q;

assign not_50_out = ~T2_Q;

assign not_43_out = ~T2_Q;
```

```
assign not_37_out = ~T2_Q;

assign not_30_out = ~T2_Q;

assign not_28_out = ~T2_Q;

assign not_25_out = ~T2_Q;

assign not_23_out = ~T2_Q;

assign not_15_out = ~T2_Q;

assign not_13_out = ~T2_Q;

assign not_9_out = ~T2_Q;

assign not_5_out = ~T2_Q;

assign not_89_out = ~T1_Q;

assign not_87_out = ~T1_Q;

assign not_77_out = ~T1_Q;

assign not_67_out = ~T1_Q;

assign not_64_out = ~T1_Q;

assign not_62_out = ~T1_Q;

assign not_57_out = ~T1_Q;

assign not_53_out = ~T1_Q;

assign not_48_out = ~T1_Q;

assign not_39_out = ~T1_Q;

assign not_31_out = ~T1_Q;

assign not_26_out = ~T1_Q;

assign not_24_out = ~T1_Q;

assign not_7_out = ~T1_Q;
```

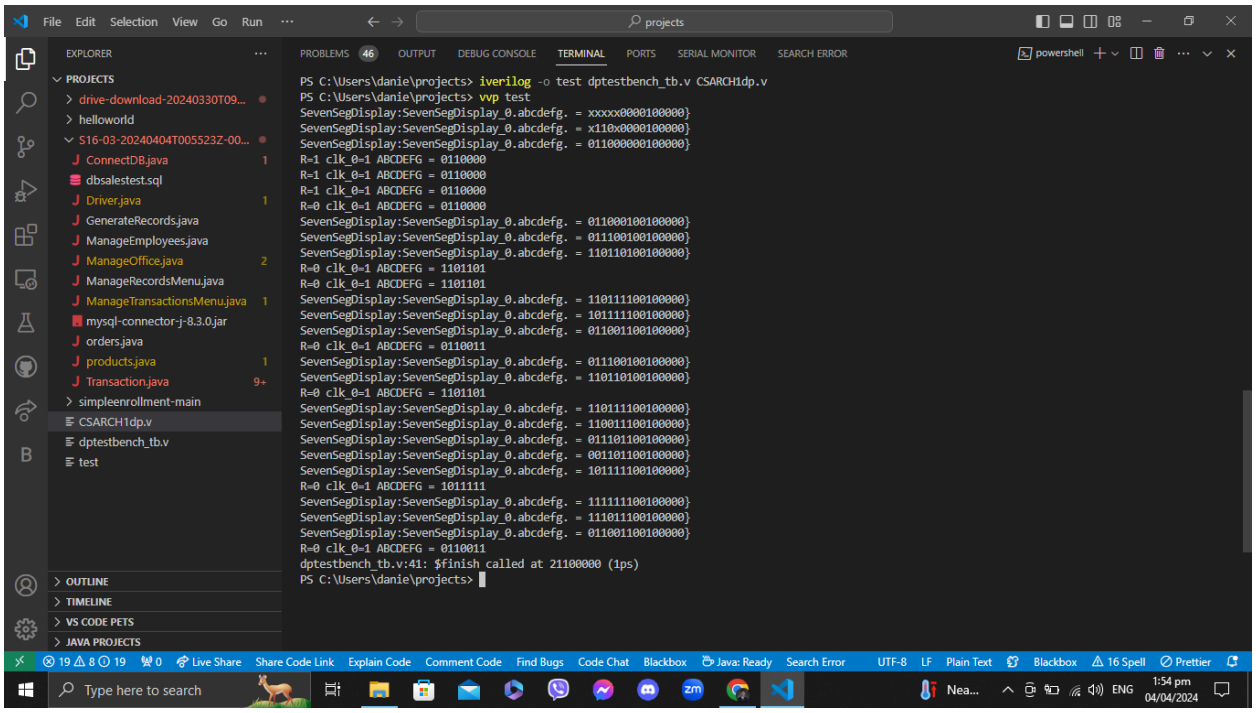
```
  assign not_4_out = ~T1_Q;
  assign const_0 = 1'b1;
  assign A = or_0_out;
  assign B = or_1_out;
  assign C = or_2_out;
  assign D = or_3_out;
  assign E = or_4_out;
  assign F = or_5_out;
  assign G = or_6_out;
endmodule


       module TflipFlop(q, q_inv, clk, t, a_rst, pre, en);
         parameter WIDTH = 1;
         output reg [WIDTH-1:0] q, q_inv;
         input clk, a_rst, pre, en;
         input [WIDTH-1:0] t;


         always @ (posedge clk or posedge a_rst)
           if (a_rst) begin
             q <= 'b0;
             q_inv <= 'b1;
           end else if (en == 0) ;
           else if (t) begin
```

```
        q <= q ^ t;
        q_inv <= ~q ^ t;
    end
endmodule
```

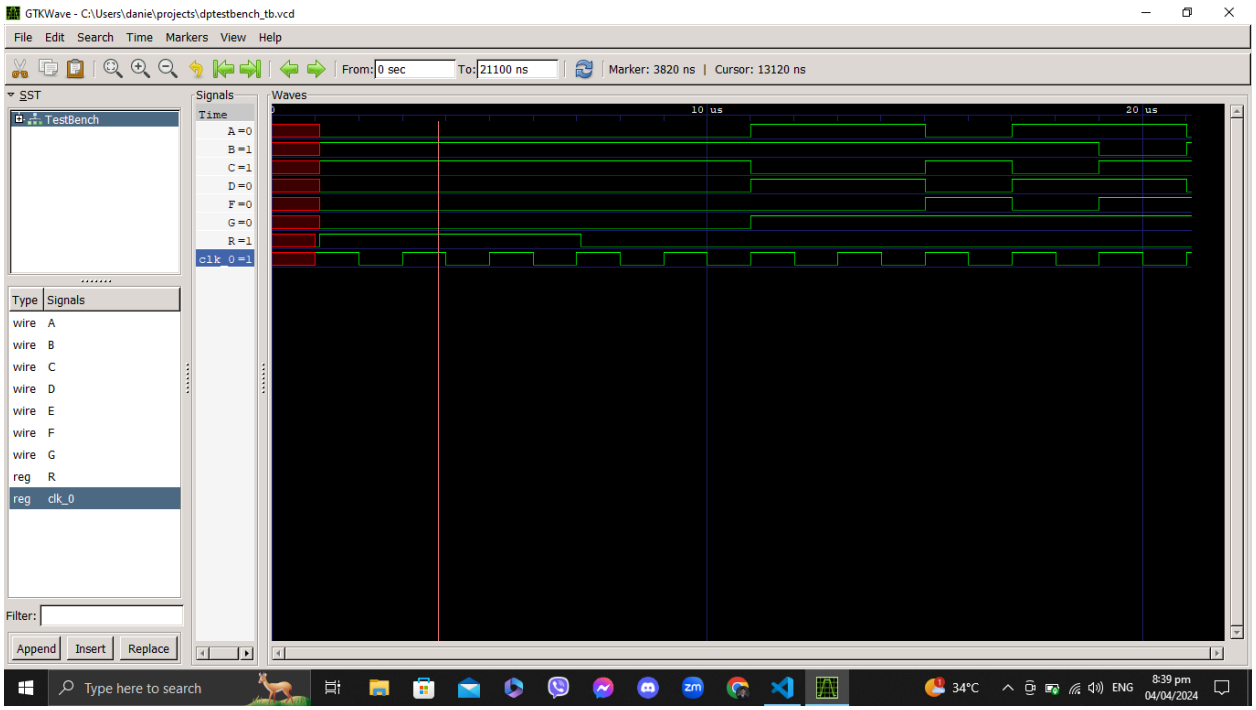
Above are the modules of the exported Verilog file from CircuitVerse. The generated Verilog file also provides the number of gates used in the logic circuit. As seen below, there are 158 logic gates, one clock, 5 T Flip-flops, and one 7-segment display.



Output


File Edit Selection View Go Run
projects
EXPLORER
PROJECTS
drive-download-20240330T09...
helloworld
S16-03-20240404T005523Z-00...
ConnectDB.java
dbsalestest.sql
Driver.java
GenerateRecords.java
ManageEmployees.java
ManageOffice.java
ManageRecordsMenu.java
ManageTransactionsMenu.java
mysql-connector-j-8.3.0.jar
orders.java
products.java
Transaction.java
simpleenrollment-main
CSARCH1dp.v
dptestbench_tb.v
test
OUTLINE
TIMELINE
VS CODE PETS
JAVA PROJECTS
PROBLEMS 46
OUTPUT
DEBUG CONSOLE
TERMINAL
PORTS
SERIAL MONITOR
SEARCH ERROR
powershell
PS C:\Users\danie\projects> iverilog -o test dptestbench_tb.v CSARCH1dp.v
PS C:\Users\danie\projects> vvp test
SevenSegDisplay:SevenSegDisplay_0.abcdefg. = xxxxx0000100000}
SevenSegDisplay:SevenSegDisplay_0.abcdefg. = x110x0000100000}
SevenSegDisplay:SevenSegDisplay_0.abcdefg. = 01100000100000}
R=1 clk_0=1 ABCDEFG = 0110000
R=1 clk_0=1 ABCDEFG = 0110000
R=1 clk_0=1 ABCDEFG = 0110000
R=0 clk_0=1 ABCDEFG = 0110000
SevenSegDisplay:SevenSegDisplay_0.abcdefg. = 011000100100000}
SevenSegDisplay:SevenSegDisplay_0.abcdefg. = 011100100100000}
SevenSegDisplay:SevenSegDisplay_0.abcdefg. = 110110100100000}
R=0 clk_0=1 ABCDEFG = 1101101
R=0 clk_0=1 ABCDEFG = 1101101
SevenSegDisplay:SevenSegDisplay_0.abcdefg. = 110111100100000}
SevenSegDisplay:SevenSegDisplay_0.abcdefg. = 101111100100000}
SevenSegDisplay:SevenSegDisplay_0.abcdefg. = 011001100100000}
R=0 clk_0=1 ABCDEFG = 0110011
SevenSegDisplay:SevenSegDisplay_0.abcdefg. = 011100100100000}
SevenSegDisplay:SevenSegDisplay_0.abcdefg. = 110110100100000}
R=0 clk_0=1 ABCDEFG = 1101101
SevenSegDisplay:SevenSegDisplay_0.abcdefg. = 110111100100000}
SevenSegDisplay:SevenSegDisplay_0.abcdefg. = 110011100100000}
SevenSegDisplay:SevenSegDisplay_0.abcdefg. = 011101100100000}
SevenSegDisplay:SevenSegDisplay_0.abcdefg. = 001101100100000}
SevenSegDisplay:SevenSegDisplay_0.abcdefg. = 101111100100000}
R=0 clk_0=1 ABCDEFG = 1011111
SevenSegDisplay:SevenSegDisplay_0.abcdefg. = 111111100100000}
SevenSegDisplay:SevenSegDisplay_0.abcdefg. = 111011100100000}
SevenSegDisplay:SevenSegDisplay_0.abcdefg. = 011001100100000}
R=0 clk_0=1 ABCDEFG = 0110011
dptestbench_tb.v:41: $finish called at 21100000 (1ps)
PS C:\Users\danie\projects>
Live Share
Share Code Link
Explain Code
Comment Code
Find Bugs
Code Chat
Blackbox
Java: Ready
Search Error
UTF-8
LF
Plain Text
Blackbox
16 Spell
Prettier
Type here to search
ENG
1:54 pm
04/04/2024

WaveForm


GTKWave - C:\Users\danie\projects\dptestbench_tb.vcd
File Edit Search Time Markers View Help
From: 0 sec
To: 21100 ns
Marker: 3820 ns | Cursor: 13120 ns
SST
TestBench
Type Signals
wire A
wire B
wire C
wire D
wire E
wire F
wire G
reg R
reg clk_0
Filter:
Append Insert Replace
Signals
Time
A =0
B =1
C =1
D =0
F =0
G =0
R =1
clk_0 =1
Waves
10 us
20 us
Type here to search
34°C
ENG
8:39 pm
04/04/2024

Reference List

Euler's totient Function and Euler's Theorem. (n.d.).

https://www.doc.ic.ac.uk/~mrh/330tutor/ch05s02.html