CSARCH2	8-Nov-2024
Exam #2	R. Pascual, M. Peradilla, R.L. Uy

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General instructions:

1. Read ALL instructions carefully and thoroughly before proceeding to answer this exam.
2. Write, in ballpen ink, the final answers in the space provided. Answers not written in ink, and multiple answers will not be considered.
3. Write legibly. No credit will be given for messy and/or ambiguous answers.
4. Cheating of any form during the exam is considered a major offense and will warrant a final grade of 0.0 in the course.

I. Understanding IEEE-754 Decimal Floating Point Representation – Write "N/A" in every field if not possible. Place a space after every half the length (i.e., Coefficient continuation is xxxxx xxxxx; Combi is xx xxx)

1.) Express $9758{,}123_{10} \times 10^{22}$ using IEEE 754 Single Precision decimal (Decimal-32) format [8pts]

Sign Bit	Combination bits	Exponent continuation bits
0	11 101	111 011

Coefficient continuation bits	
1111 0 11000	00101 00011

(8)

2.) Express $-5812457346991898_{10} \times 10^{-201}$ using IEEE 754 Double Precision decimal (Decimal-64) format [8pts]

Sign Bit	Combination bits	Exponent continuation bits
1	11 101	000 101

Coefficient continuation bits				
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(0) +1

3.) What is the normalized decimal equivalent of IEEE 754 decimal-32 representation 0xB734D3CF? [4pts]	N/A (0)

II. Understanding Unicode Representation #1: Convert the given Unicode code point to its equivalent UTF representation. The final answer should be in <u>hexadecimal</u>. "N/A" if not possible [10pts]

Given: U+2BFF5	UTF Representation
UTF-8 (answer format: xx xx xx xx)	N/A
UTF-16 (answer format: xxxx xxxx)	D86F DFF5
UTF-32 (answer format: xxxx xxxx)	0002 BFF5

(6) +1

III. Understanding Unicode Representation #2: Determine the Unicode code point equivalent of the given UTF representation. No need to write "U+". "N/A" if not possible [10pts]

UTF Representation	Unicode Code Point
(UTF-8) DF BC	N/A
(UTF-16) D86A DEDE	2EADE
(UTF-32) 0010 AB45	10AB45

(2) +1

IV. Understanding BCD representation. Write "N/A" if not possible [10pts]

10-bit representation	2's complement integer (Decimal)	Unsigned integer (Decimal)	Densely packed BCD
1110101001	N/A	N/A	729
111 001 111	-1846	----------	991

(2)

V. Understanding memory representation: Determine the equivalent fixed-point decimal number or special case. If there is no equivalent, write "N/A." Special cases {-/+ Infinity \| sNaN \| qNaN \| Denormalized} [10pts]

Memory Data	Representation	Fixed-point Decimal equivalent /Special case
0x003B0000	IEEE 754 Binary32 floating-point	+ infinity
0xEE03173D	IEEE 754 Decimal32 floating-point	sNAN

(0) +2

VI. Understanding Cache memory #1 [20pts]

*A full associative cache memory has 8 blocks; block size is 8 words; cache access time is 1ns; memory access time is 10 ns; non-load thru read policy; Least recently used (LRU) replacement algorithm. Note: associativity should occupy the first available block as discussed in the class.

* Given the main memory BLOCK sequence (in decimal): 41, 47, 45, 60, 59, 58, 41, 62, 50, 53

* Show the final content of the cache memory after fetching all the sequences. Use the table below; write the letter E to denote empty).

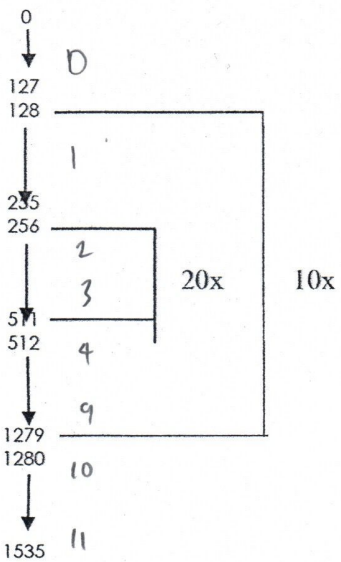
Cache block	MM block mapped here
0	41
1	53
2	45
3	60
4	59
5	58
6	62
7	50

(16)

- What is the miss penalty of the cache (in ns)? (9)
- What is the average access time of the MM block sequences (in ns)? (1)

VII. Understanding Cache Memory #2: [20pts]

A program consisting of two nested loops (see figure) is to be run on a computer that has a cache with the following parameters: MM memory size: 65536-word; cache size = 1024-word; block size = 128 words; set size = 4 blocks; memory access time is 10ns and the cache access time is 1ns. Non load-thru read policy. Full associative mapping using LRU replacement algorithm. Note: address in decimal.



1.) How many bits are needed for the main memory address bus?	16
2.) How many cache blocks?	3
3.) How many bits are allocated as "TAG" in main memory address?	8
4.) How many unique MM blocks will be mapped to a particular cache block?	512
5.) How long will the CPU fetch those memory locations, assuming NO cache memory (in ns)?	605 440
6.) What is the cache miss penalty (in ns)?	10
7.) During the initial and the 1st pass, how many MM blocks are cache miss?	38
8.) During the 2nd pass, how many MM blocks are cache miss?	45
9.) During the initial and the 1st pass, how long will take to fetch those blocks (in ns)?	4340
10.) During the 2nd pass, how long will take to fetch those blocks (in ns)?	4370

(6) +2

---------- **Do not write below this line** ----------

I	/20	III -	/ 10	V -	/10	VII - /20	
II	/10	IV -	/ 10	VI -	/ 20		Total -