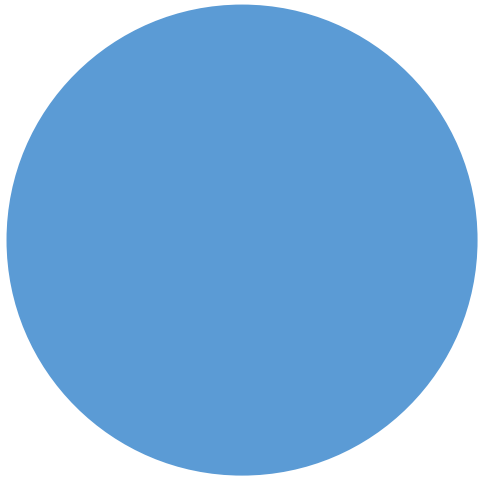
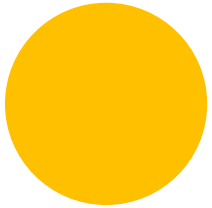


CSARCH Lecture Series: Von Neumann Architecture

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Overview

Reflect on the following question:

Given the following code, which part is the data and which part is the program and where data and program stored in the computer?

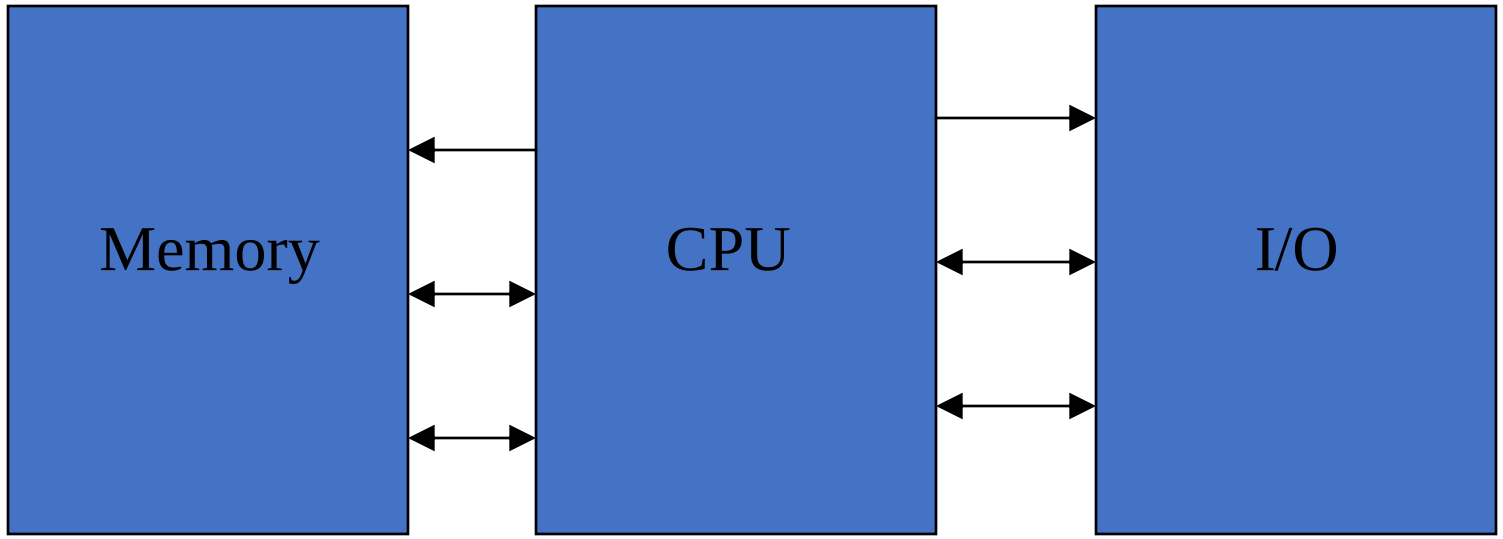
```
int main()
{int i;
i = 0;
for (int c=10; c=0; c--)
        i=i+c;
}
```

Overview

- This sub-module discusses the Von Neumann Architecture
- The objective is as follows:
  - ✓Describe the concept of Von Neumann Architecture

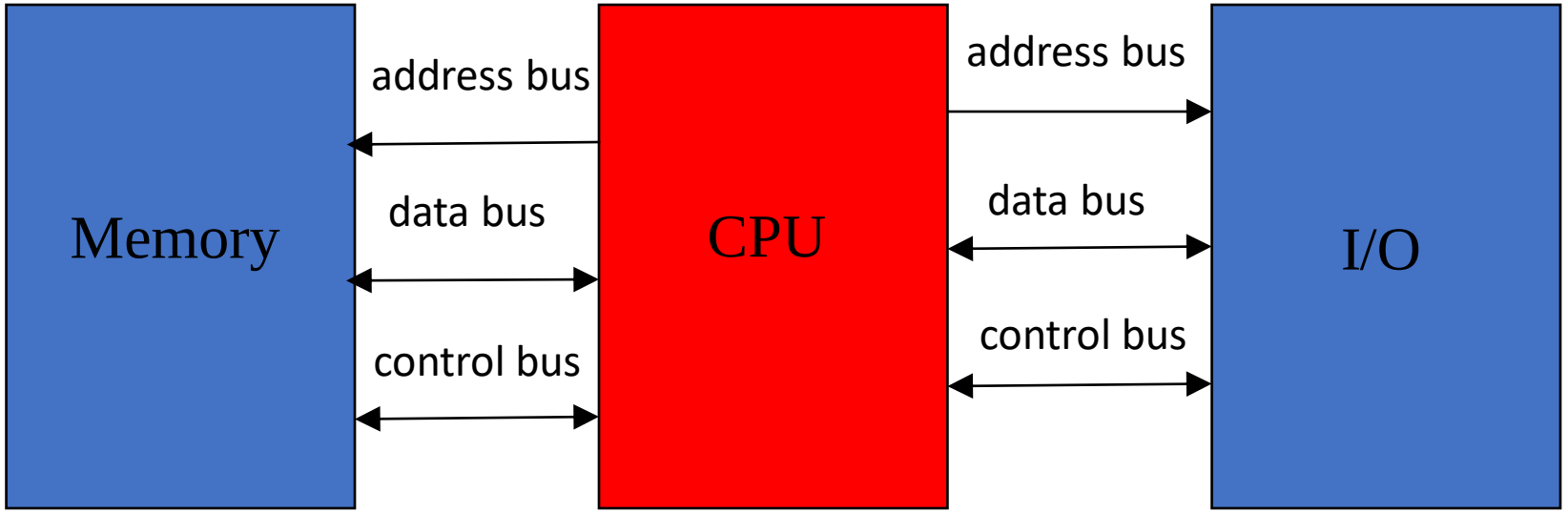
Von Neumann Architecture

- Store Program Architecture – program & data are stored in the main memory and **not** in the CPU
- Instructions in the main memory are **Fetched, Decoded** and **Executed** sequentially (or at least it appears to be)



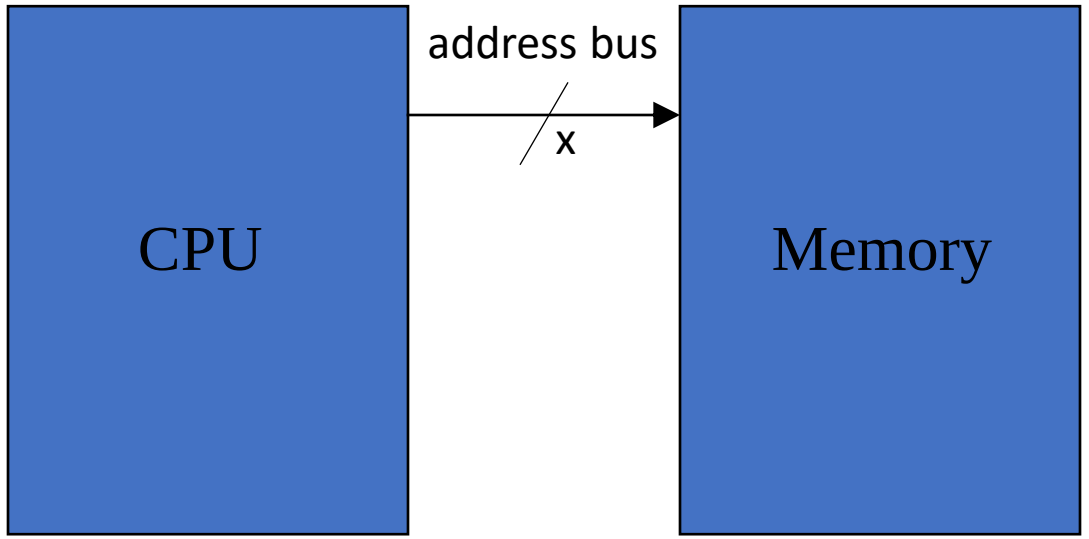
Address/Data/Control Bus

- CPU communicates externally via a **bus**
- Bus – set of parallel wires or lines
- Three types of bus
  - Address
  - Data
  - Control



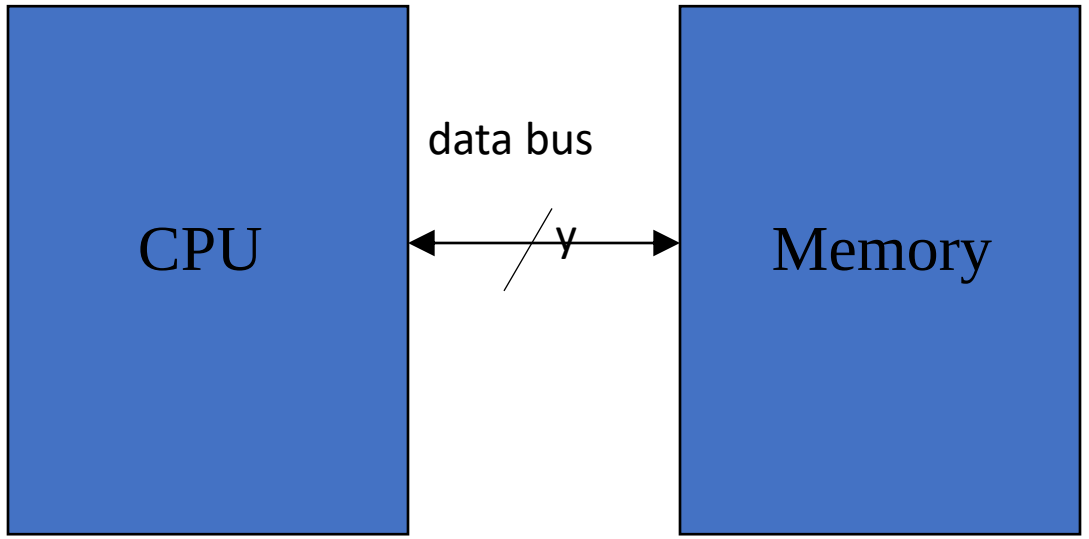
Address Bus

- Address Bus – used to select the desired memory or I/O devices by providing a unique address that corresponds to one of the memory or I/O devices
- It is uni-directional (from CPU to external)
- If a CPU has *x* address bus, it means that it could access up to 2^x possible address locations



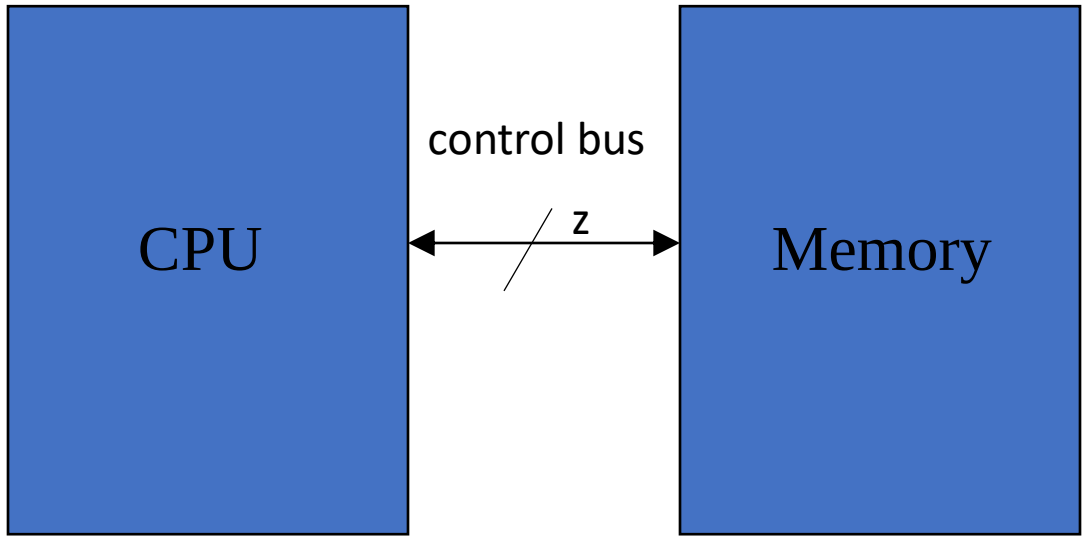
Data Bus

- Data Bus – used to transfer data to and from the memory or I/O devices
- It is bi-directional
- If a CPU has *y* data bus, it means that it could transfer data *y* bit at a time



Control Bus

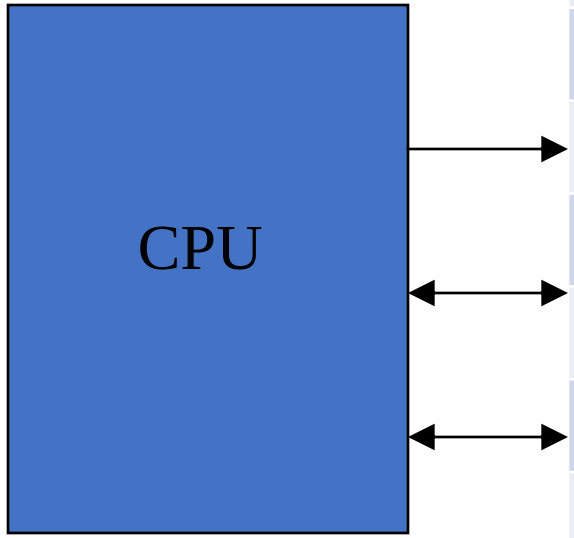
- Control Bus – used to carry control signals to the memory or I/O devices
- If a CPU has *z* control bus, it means that it has 2^z possible control signals



- Example: read signal, write signal

Try

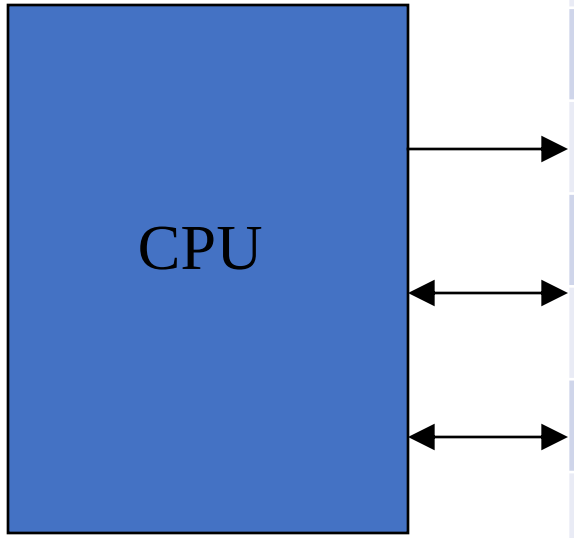
- Given the following bus specifications:
  - address bus: 3-bits
  - data bus: 8-bits
  - control bus: 4-bits
- What is the range of address that the CPU can access?
- How bits of data are transferred at one time?
- How many possible control signals can CPU have?



Address (in hex)	Memory data (in hex)
C	FF
B	FE
A	CA
9	AD
8	0B
7	F0
6	DE
5	BC
4	9A
3	78
2	56
1	34
0	12

Try

- Given the following bus specifications:
  - address bus: 3-bits
  - data bus: 8-bits
  - control bus: 4-bits
- What is the range of address that the CPU can access? 0-7
- How bits of data are transferred at one time? 8
- How many possible control signals can CPU have? 16



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1	34
0	12

Bus Clock

- Common **bus clock** is used to coordinate activities in a system bus.
- The time interval from one clock pulse to the next is called a **bus cycle**.
- **Bus cycle time** is the inverse of the bus clock rate.

Bus Clock

- Example: if the bus clock rate is 400MHz, the bus cycle time is therefore:

Bus cycle time = $\frac{1}{bus\ clock\ rate}$

Bus cycle time = $\frac{1}{400{,}000{,}000Hz}$

Bus cycle time = 2.5×10^{-9} seconds

= 2.5 nanoseconds

Bus capacity or Data Transfer Rate

- Bus capacity is also known as data transfer rate
- Bus capacity = data transfer unit * clock rate
- For **example**, what is the bus capacity of a parallel bus with 64-bit data lines and a 400MHz clock rate

Bus capacity = data transfer unit * clock rate

= 64 bits * 400,000,000hz

= 8 bytes*400,000,000hz

= 3,200,000,000 bytes per second or 3.2Gbytes/sec

To recall…

- What we have learned:
  - ✓Describe the concept of Von Neumann Architecture