Assembly Language Lecture Series: X86-64 Floating-Point Register

Sensei RL Uy, College of Computer Studies, De La Salle University, Manila, Philippines

Copyright Notice

This lecture contains copyrighted materials and is use solely for instructional purposes only, and not for redistribution.

Do not edit, alter, transform, republish or distribute the contents without obtaining express written permission from the author.

SIMD Register

- SIMD registers can be used in scalar or packed format. Can store either integer or floating-point data type
 - Sixteen (16) 128-bit XMM registers (XMM0-XMM15)

SIMD Packed Register

Single-Precision FP	Single-Precision FP	Single-Precision FP	Single-Precision FP
127-96	95-64	63-32	bits 31-0

Each XMM register can support up to 4 packed single-precision floating-point

Double-Precision FP	Double-Precision FP	
127-64	Bits 63-0	

Each XMM register can support up to 2 packed double-precision floating-point

SIMD Scalar Register

	Single-Precision FP
	bits 31-0

XMM register can also be used as **scalar single-precision register**. Only the **least significant 32-bit** is used.

Double-Precision FP	
Bits 63-0	

XMM register can also be used as **scalar double-precision register**. Only the **least significant 64-bit** is used.

x86-64 Instructions: MOVSS

MOVSS (Move scalar single-precision)

Syntax: MOVSS dst, src

dst ← src MOVSS xmmR, m32 MOVSS xmmR/m32,xmmR

Flags Affected:

*all status flags no change: if count is 0

x86-64 Instructions: MOVSS

MOVSS (Move scalar single-precision)

Syntax: MOVSS dst, src

dst ← src MOVSS xmmR, m32 MOVSS xmmR/m32,xmmR

Example:

```
section .data
var1 dd 2.5
section .text
MOVSS XMM1, [var1]
```

x86-64 Instructions: MOVSS

MOVSS (Move scalar single-precision)

Syntax: MOVSS dst, src

dst ← src MOVSS xmmR, m32 MOVSS xmmR/m32,xmmR

Example:

```
section .data
var1 dd 2.5
section .text
MOVSS XMM1, [var1]
```

```
XMM1 = 40200000
or
XMM1 = 2.5
```

x86-64 Instructions: MOVSD

MOVSD (Move scalar double-precision)

Syntax: MOVSD dst, src

dst ← src MOVSD xmmR, m64 MOVSD xmmR/m64, xmmR

x86-64 Instructions: MOVSD

MOVSD (Move scalar double-precision)

Syntax: MOVSD dst, src

dst ← src MOVSD xmmR, m64 MOVSD xmmR/m64, xmmR

Example:

```
section .data
var1 dq 2.5
section .text
MOVSD XMM1, [var1]
```

x86-64 Instructions: MOVSD

MOVSD (Move scalar double-precision)

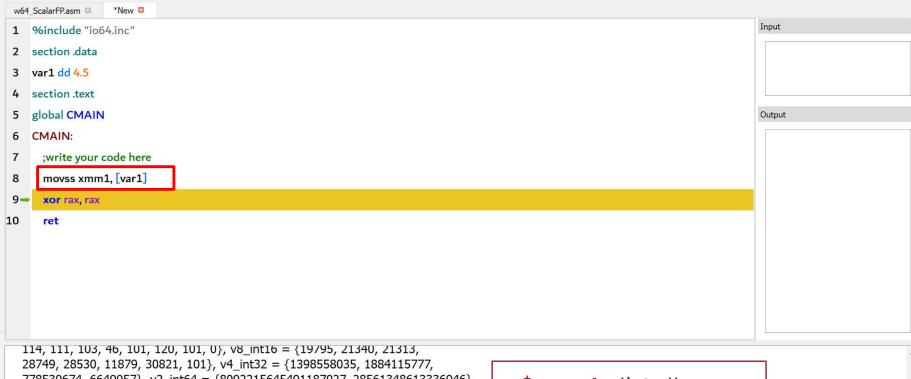
Syntax: MOVSD dst, src

dst ← src MOVSD xmmR, m64 MOVSD xmmR/m64, xmmR

Example:

```
section .data
var1 dq 2.5
section .text
MOVSD XMM1, [var1]
```

```
XMM1=4004_0000_0000_0000
or
XMM1=2.5
```



778530674, 6649957}, $v2 int64 = \{8092215645491187027, 28561348613336946\}$, uint128 = 0x006578652e676f72704d5341535c4d53

> p \$xmm1

 $$3 = \{v4_float = \{4.5, 0, 0, 0\}, v2_double = \{5.3516153614920076e-315, 0\},$ v16 int8 = $\{0, 0, -112, 64, 0 < \text{repeats } 12 \text{ times} > \}$, v8 int16 = $\{0, 16528, 0, 16528, 0, 16528,$ 0}, uint128 = 1083179008}

p \$xmm1 - list all packed combinations of an XMM register

