

Akshat Baranwal

[✉ abaranw2@asu.edu](mailto:abaranw2@asu.edu) | [+1-6028049027](tel:+1-6028049027) | linkedin.com/in/akshatbaranwal21/

Relevant Engineering Projects

- **ASIC Design for accelerating GCNs (Spring 2025):**

Designed and implemented a low-power artificial intelligence GCN accelerator using a **7nm PDK** process. Performed synthesis using Synopsys Design Compiler and automated place-and-route (**APR**) using customized TCL scripts on Cadence Innovus, achieving **66.55 ns** latency at 15.03 MHz, **4.81 mW** total power, and **2.0980 cm²** area. Executed the complete **RTL-to-GDSII** flow. Verified design correctness through post-layout simulation, DRC, and LVS clean reports, and achieved 51.7% placement density with 29,978 gates and 10,076 standard cells. Passed DRC and cleared placement-routing violation in Innovus as well as exported design to Virtuoso and cleared **DRC/LVS** using calibre tools.

- **Hardware Verification Project: Data Aligner Module (Fall 2025):**

Setup a **UVM** verification environment for a high speed Aligner module, ensuring seamless data transformation. Implemented custom MD protocol agents and an **APB** interface to validate error handling, resulting in zero bugs in post-verification regressions. Automated sticky interrupt monitoring and backpressure testing, guaranteeing protection against critical FIFO overflows.

- **MIPS SoC Design & Implementation Project (Fall 2025):**

Architected and developed a functional 32-bit, single-cycle **MIPS CPU** from the ground up using SystemVerilog. Designed and implemented all core hardware modules, including the **ALU, Control Unit, Register File, Memory, and Program Counter**. Implemented the decoding and datapath logic for over **30 MIPS instructions**, covering arithmetic, memory access, logical, and control flow operations. Verified processor functionality by writing custom **assembly programs**, simulating with Synopsys Verdi, and analyzing results using verdi waveform.

- **Neural Network Hardware Implementation on FPGA (Fall 2024):**

Designed and implemented a **feed forward neural network** in Verilog, complete with training and gradient computation **modules synthesized on FPGA**. Built memory initialization (.mif) files and FSM-based control logic for loading datasets and updating weights. Verified functional correctness through ModelSim simulations and deployed a fully synthesizable training architecture using Quartus Prime.

Education

Arizona State University, Tempe M.S. in Computer Engineering (Electrical Engineering) VLSI Design, Machine Learning & FPGA deployment, Digital Design for SoCs, Digital Verification & Testing	08/24 to 05/26 CGPA: 3.4
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RGPV University B.Tech. in Electrical Engineering Relevant Coursework: Microprocessor and Digital Electronics, Analog Electronics, Power Electronics, Control Systems.	08/19 to 06/23 GPA: 7.8/10 First Division With Distinction
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Work Experience

Larsen & Toubro Infotech, India	01/24 to 08/24
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Data Engineer

- Engineered an automated **data pipeline using Python scripting** to parse, shred, and load massive, semi-structured XML files (200,000+ records) into structured Snowflake tables.
- Optimized data ingestion and decreased processing time by 90%, enabling faster data availability for analysis.
- Developed and deployed internal **data visualization** dashboards to monitor pipeline health, track data quality metrics, and provide stakeholders with real-time process insights.

Energy Institute, Bangalore, India	01/23 to 05/23
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Research Intern

- Tested and validated power electronics converters for electric vehicle (EV) applications using a **Hardware-in-the-Loop**.
- Performed hands-on experiments in the lab, utilizing **oscilloscopes and power analyzers** to measure hardware performance and system efficiency.
- Configured and executed test procedures to analyze the behavior of power circuits under various load conditions.
- Analyzed hardware test data to verify and refine EV powertrain simulations, improving their real-world accuracy.

Certificates

- Cadence "Design for Test Fundamentals":** [\[Link\]](#)
- Cadence "RTL to GDSII Flow":** [\[Link\]](#)