Akshat Baranwal

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Education

Arizona State University 08/24 – 05/26
M.S. in Computer Engineering (Electrical Engineering) ***CGPA: 3.4***

Madhav Institute of Technology & Science-RGPV University 08/19 – 06/23
B.Tech. in Electrical Engineering ***GPA: 7.8/10 First Division With Distinction***

Relevant Coursework

- Digital Verification & Testing
- VLSI Design Semiconductor Heterogeneous Integration
- Real-Time Embedded Systems
- Digital Design for SOCs
- Machine Learning with Deployment to FPGAs
- Digital Electronics and Microprocessor

Relevant Engineering Projects

ASIC Design: GCN Hardware Accelerator *Spring 2025*

- **Full RTL-to-GDSII Flow:** Designed and implemented a low power Graph Convolutional Network (GCNs) accelerator using a **7nm PDK** process, executing the complete physical design pipeline.
- **Synthesis & PnR:** Performed logic synthesis via Synopsys Design Compiler and automated **APR** using customized TCL scripts in Cadence Innovus.
- **Performance Metrics:** Achieved **66.55 ns** latency, **4.81 mW** total power, and **20980.037 um^2** area.
- **Physical Verification:** Cleared **DRC,LVS** using Calibre tools and performed post layout simulations to ensure timing and functional correctness.

Hardware Verification: Data Aligner Module *Fall 2025*

- **UVM:** Architected a **UVM** based verification environment for a high speed Aligner module to ensure seamless data transformation.
- **Protocol Validation:** Implemented custom MD protocol agents and an **APB** interface to validate error handling & control transactions.
- **Register Testing:** Automated sticky interrupt monitoring and backpressure testing, eliminating critical FIFO overflow.
- **Regression Testing:** Achieved zero bugs in post-verification regressions through comprehensive **functional coverage**.

MIPS SoC Design & Implementation *Fall 2025*

- **CPU Architecture:** Developed a 32-bit single-cycle **MIPS CPU** from scratch using **SystemVerilog**.
- **RTL Development:** Designed the **ALU, Control Unit, Register File, and Memory** modules with optimized datapath logic for 30+ instructions.
- **Instruction Support:** Implemented decoding logic for arithmetic, memory access, logical, and control flow operations.
- **Functional Verification:** Validated the processor by writing custom **assembly programs** and debugging via waveforms.

Work Experience

Larsen & Toubro Infotech *01/24 – 08/24*
Data Engineer *Pune, India*

- **Data Pipeline Engineering:** Engineered an automated **ETL pipeline** using Python to parse and load semi-structured XML datasets (200,000+ records) into **Snowflake** tables.
- **Performance Optimization:** Optimized data ingestion workflows, decreasing processing time by **90%** and significantly accelerating data availability for downstream analytics.
- **Data Visualization & Monitoring:** Developed internal dashboards to monitor pipeline health and track **data quality metrics**, providing stakeholders with real-time process insights.

Energy Institute *01/23 to 05/23*
Research Intern *Bangalore, India*

- **Data Acquisition & HIL:** Engineered automated data collection workflows using **Hardware-in-the-Loop (HIL)** systems to capture **high frequency telemetry** from EV power converters.
- **Signal Processing:** Processed raw sensor data from **oscilloscopes and power analyzers**, implementing **noise filtering and feature extraction** to analyze system efficiency.
- **Data Validation:** Developed test procedures to validate experimental data against **EV powertrain simulations**, utilizing **statistical analysis** to identify and resolve discrepancies.
- **Pipeline Optimization:** Refined data driven simulation parameters by correlating hardware test results with digital models, improving powertrain predictive accuracy.

Technical Skills

Design & Verification: SystemVerilog, Verilog, UVM, SVA, Functional Coverage, Constrained-Random Verification, APB Protocol, FSM Design, MIPS Assembly, Synopsys VCS, Verdi
EDA Tools & Silicon Flow: Synopsys Design Compiler, Cadence Innovus, Virtuoso, Mentor Graphics Calibre (DRC/LVS), HSPICE, RTL-to-GDSII Flow, Static Timing Analysis (STA), Clock Tree Synthesis (CTS), Parasitic Extraction, PPA Analysis, 7nm PDK
FPGA, Embedded & Automation: Xilinx Spartan-7 FPGA, Vivado IP Catalog, Block RAM (BRAM), Logic Analyzer, TCL Scripting, Python, Embedded C, MATLAB, I2C, SPI, UART, Hardware-in-the-Loop (HIL)

Certificates

Cadence RTL to GDSII Flow [Link]

Cadence Basic Static Timing Analysis (STA) [Link]