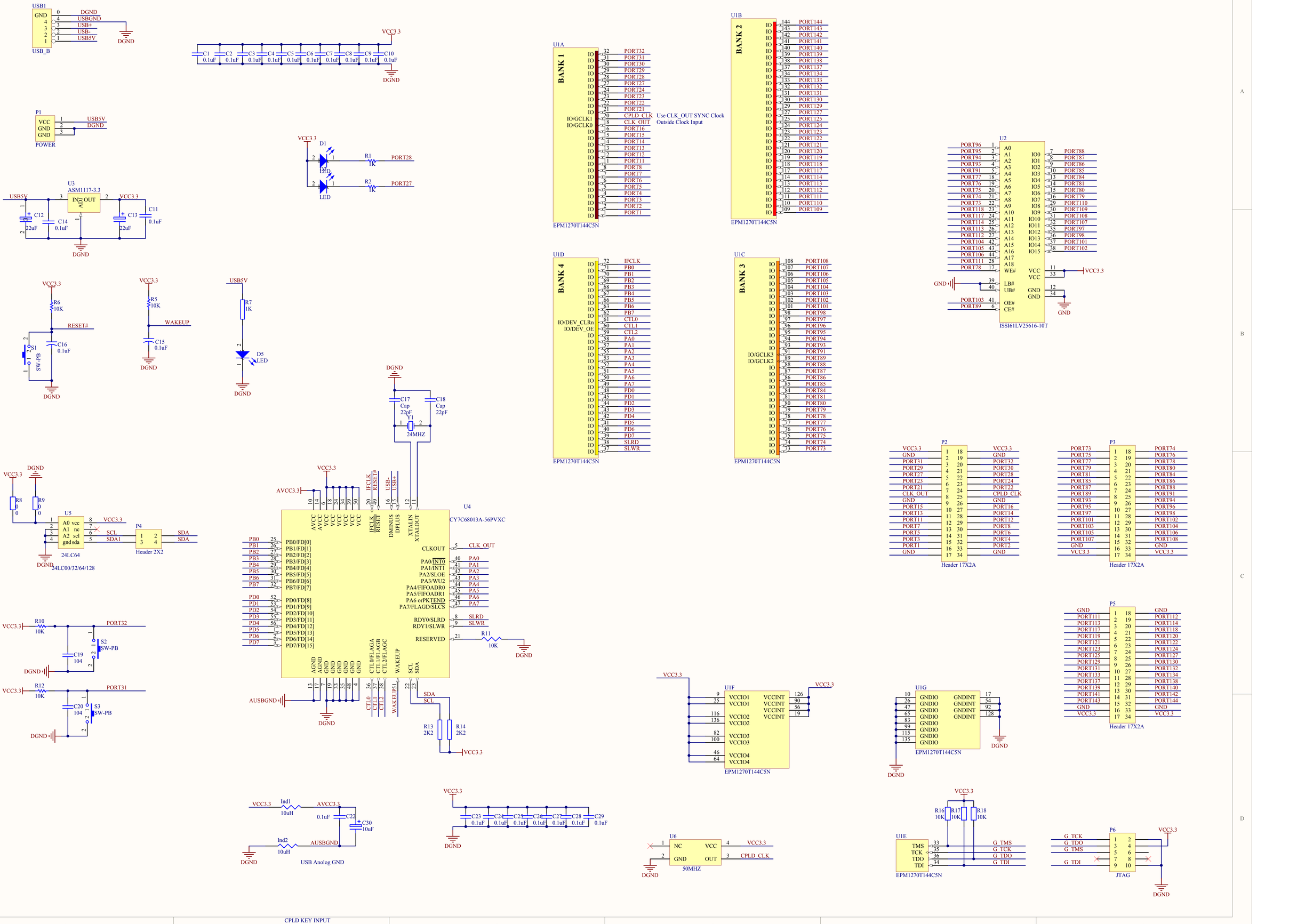
USB1
USB_B
DGND
USBGND
USB+
USB-
USB5V
VCC3.3
C1 0.1uF
C2 0.1uF
C3 0.1uF
C4 0.1uF
C5 0.1uF
C6 0.1uF
C7 0.1uF
C8 0.1uF
C9 0.1uF
C10 0.1uF
P1
POWER
VCC
GND
U3
ASM1117-3.3
IN
OUT
ADJ
C12 22uF
C14 0.1uF
C13 22uF
C11 0.1uF
D1
LED
R1 1K
R2 1K
PORT28
PORT27
U1A
BANK 1
EPM1270T144C5N
IO/GCLK1
IO/GCLK0
CPLD_CLK
CLK_OUT
Use CLK_OUT SYNC Clock Outside Clock Input
U1B
BANK 2
U1C
BANK 3
U1D
BANK 4
IO/DEV_CLRn
IO/DEV_OE
IO/GCLK3
IO/GCLK2
U2
ISSI61LV25616-10T
WE#
LB#
UB#
OE#
CE#
R6 10K
R5 10K
R7 1K
RESET#
WAKEUP
S1
SW-PB
C16 0.1uF
C15 0.1uF
D5
LED
C17 Cap 22pF
C18 Cap 22pF
Y1
24MHZ
P2
P3
R8 0
R9 0
U5
24LC64
24LC00/32/64/128
P4
Header 2X2
U4
CY7C68013A-56PVXC
AVCC3.3
AUSBGND
IFCLK
RESET#
USB-
USB+
CLKOUT
RDY0/SLRD
RDY1/SLWR
RESERVED
R11 10K
R13 2K2
R14 2K2
SDA
SCL
R10 10K
R12 10K
S2
S3
C19 104
C20 104
U1F
U1G
Header 17X2A
P5
R16 10K
R17 10K
R18 10K
U1E
TMS
TCK
TDO
TDI
G_TMS
G_TCK
G_TDO
G_TDI
U6
50MHZ
CPLD_CLK
P6
JTAG
Ind1 10uH
Ind2 10uH
C22 0.1uF
C30 10uF
USB Anolog GND
C23 0.1uF
C24 0.1uF
C25 0.1uF
C26 0.1uF
C27 0.1uF
C28 0.1uF
C29 0.1uF
CPLD KEY INPUT