Development of the device parametric conversion digital signal's capacity

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I. Introduction

The paper studies some existing and describes the new algorithms of fixed-point numbers rounding for FPGA. Our goal is to implement 3 types of rounding algorithms: truncation, rounding to the nearest integer and rounding to the nearest even. But existing algorithms has been designed for float-point binary numbersso these algorithms are unsuitable for this goal. Also module must have certain ports for binary code, dot's position, type of algorithm, clock rate signal and size of binary code.

Algorithm for FPGA must have two realisation: Verilog/VHDL realisation and C-realization. Methods of translating code from Matlab to Verilog/C were considered, but this Matlab's tool has short coming. This tool allow create port for 32- or 64-bit binary words. Thus new algorithms for rounding were designed and were realised on Verilog and C. At the end of developing comparison of two realisations was made. Parameters of comparison are maximum clock rate and numbers of used registers.

In this work existing algorithms of rounding binary numbers were considered and new algorithms were developed. At the end two realization of this algorithms (C- and Verilog-realization) were made.