A company of SIM Tech

SIMCOM WCDMA Wireless Module

SIM5xxx SPI Application Note

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Version history

Date	Version	Description of change	Author
2010-03-26	1.01	Origin	libing
2011-08-16	1.02	Add SIM5320 description.	Libing

1 Introduction

1.1 Overview

SIMcom modules provide a SPI interface that supports a duplex, synchronous, serial communication link. It is 1.8V operation. Clock rates up to 26 MHz. SPI must be configured as the master.. This document describes SPI interface application of SIMcom modules that is used to design for POS, handset, include the dual-mode mobile phone, PDA, and the others.

SIM5xxx SPI Features

- Master support only.
- Serial clock with programmable polarity and phase
- Programmed Clock rates, up to 26 MHz
- One chip-select
- 1.8 V operation
- Operates in three modes: Run mode, Wait mode and stop mode.

1.2 Scope of the document

This document is intended for the following versions of the SIMCom modules

- SIM5320A
- SIM5320E
- SIM5320J

1.3 References

The present document is based on the following documents:

[1] SIMCOM_SIM53xx_ATC_EN.pdf

[2] SIMCOM_SIM53xx_HD_EN.pdf

1.4 Terms and Abbreviations

For the purposes of the present document, the following abbreviations apply:

- AT ATtention; the two-character abbreviation is used to start a command line to be sent from TE/DTE to TA/DCE
- TA Terminal Adaptor; e.g. a data card (equal to DCE)
- TE Terminal Equipment; e.g. a computer (equal to DTE)
- UMTS Universal Mobile Telecommunications System
- URC Unsolicited Result Code
- USIM Universal Subscriber Identity Module

- WCDMA Wideband Code Division Multiple Access

2 Recommended application circuit

2.1 SPI interface circuit

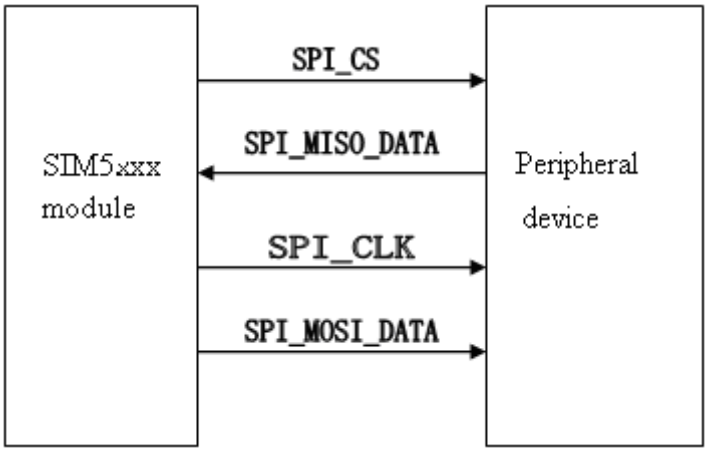

Figure 1: SPI interface circuit

The SIM5XXX module SPI must be configured as the master.Only a master SPI module can initiate transmissions. A transmission begins by writing to the master SPI data register. The data begins shifting out on the SDO/MOSI pin under the control of the serial clock.

The SPI operates in three modes:

- Run mode – the basic mode of operation.
- Wait mode – SPI operation in wait mode is a configurable low-power mode that is enabled by AT+CSPISETCLK . During wait mode, the SPI goes into a power-conservative state with the SPI clock generation turned off.
- Stop mode – The SPI is inactive in stop mode by AT+CSPISETCS for reduced power consumption. If the SPI is configured as a master, any transmission in progress stops, but resumes after the controller returns to run mode.

Note: SPI is 1.8V operation.

The SPI should include ESD protection. Although some ESD components have been added in our model, to improve ESD, one should put some ESD components on customer host board. The ESD components should be placed beside the connectors which the human body might touch. We recommend using an Electro-Static discharge device DF2S6.8S.

2.2 Electrical Specifications

SIM5XXX SPI Digital I/O specifications are presented in Table 1.

Table 1: Pin Description

Pins	PCM functionality	I/O Dir	DC CHARACTERISTICS
SPI_CLK	SPI clock	O	SPI interface is 1.8V standard. VILmin=0V VILmax=0.3*1.8V VIHmin=0.7*1.8V VIHmax=(1.8+0.3)V VOLmin=GND VOLmax=0.2V VOHmin=1.8 -0.2V VOHmax=1.8V
SPI_CS_N	SPI chip-select	O	
SPI_MOSI_DATA	SPI (master only) master out/slave in data	O	
SPI_MISO_DATA	SPI (master only) master in/slave out data	I	

SIM5XXX SPI timing requirements are illustrated in Figure 2 and listed in Table 2.

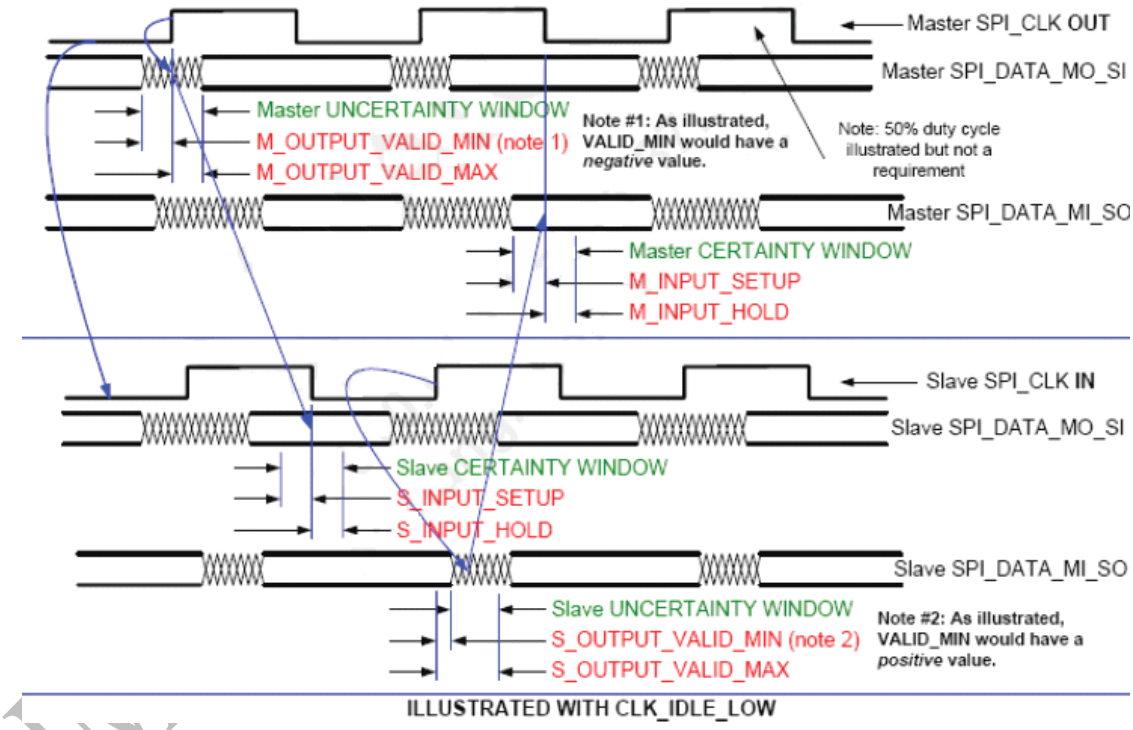

Figure 2: SPI timing diagram

Table 2: SPI timing characteristics

Parameter	Comments	Min	Typical	Max	Unit
M_SPI_CLK(frequency)		0	–	26	MHz

M_SPI_CLK(period)		38	–	–	ns
M_SPI_CLK_HIGH	P= period	17	0.45xP	–	ns
M_SPI_CLK_LOW	P= period	17	0.45xP	–	ns
M_OUTPUT_VALID2		-5	–	+5	ns
M_INPUT_SETUP		0	–	3	ns
M_INPUT_HOLD		0	–	3	ns
M_TRI_STATE_EN		-5	–	+5	ns
M_TRI_STATE_DIS		-5	–	+5	ns

3 AT command about SPI

3.1 AT+CSPISETCLK SPI clock rate setting

Description

You can use this command to set SPI clock configuration and trigger mode.

SIM PIN	References
NO	Vendor

Syntax

Test Command	Responses
AT+CSPISETCLK=?	+ CSPISETCLK: (0-1), (0-1),(0-1) OK
Read Command	Responses
AT+CSPISETCLK?	+ CSPISETCLK: <polarity>,<mode>,<trigger mode> OK
Write Command	Responses
AT+CSPISETCLK =<polarity>,<mode>,<trigger mode>	OK
	ERROR

Defined values

<polarity>
0 : the SPI clock signal is low when the clock is idle
1 : the SPI clock signal is high when the clock is idle
<mode>
0 : the SPI clock runs only during a transfer unit

1 : the SPI clock runs continuously from the start of the transfer
<trigger mode>
0 : the SPI data input signal is sampled on the leading clock edge
1 : the SPI data input signal is sampled on the trailing clock edge

Examples

AT+ CSPISETCLK =1,0,1
OK
AT+ CSPISETCLK?
+ CSPISETCLK: 1,0,1
OK
AT+ CSPISETCLK =?
+ CSPISETCLK: (0-1),(0-1),(0-1)
OK

3.2 AT+CSPISETCS SPI chip select setting

Description

You can use this command to set SPI chip select polarity and mode.

SIM PIN	References
NO	Vendor

Syntax

Test Command	Responses
AT+CSPISETCS=?	+ CSPISETCS: (0-1), (0-1) OK
Read Command	Responses
AT+CSPISETCS?	+ CSPISETCS: <mode>,<polarity> OK
Write Command	Responses
AT+CSPISETCS =<mode>,<polarity>	OK ERROR

Defined values

<mode>
0 : the SPI chip select is de-asserted between transfer units
1 : the SPI chip select is kept asserted between transfer units
<polarity>

0 : the SPI chip select is active low

1 : the SPI chip select is active high

Examples

```
AT+ CSPISETCS =1,0
OK
AT+ CSPISETCS?
+ CSPISETCS: 1,0
OK
AT+ CSPISETCS =?
+ CSPISETCS: (0-1),(0-1)
OK
```

3.3 AT+CSPISETF SPI clock frequency setting

Description

You can use this command to set SPI clock frequency

SIM PIN	References
NO	Vendor

Syntax

Test Command	Responses
AT+CSPISETF=?	+ CSPISETF: (0-26000000), (0-26000000),(0-64) OK
Read Command	Responses
AT+CSPISETF?	+ CSPISETF: <min>,<max>,<de-assertion time> OK
Write Command	Responses
AT+CSPISETF =<min>,<max>,<de-assertion time>	OK ERROR

Defined values

<min>
0-26000000 : in master mode, set the minimum SPI clock frequency by the slave device
<max>
0-26000000 : in master mode, set the maximum SPI clock frequency by the slave device
<de-assertion time>

0-64 : in master mode, set the minimum time to wait between transfer units in nanoseconds

Examples

```
AT+ CSPISETF =960000,10000000,0
OK
AT+ CSPISETF?
+ CSPISETF: 960000,10000000,0
OK
AT+ CSPISETF =?
+ CSPISETF: (0-26000000), (0-26000000),(0-64)
OK
```

3.4 AT+CSPISETPARA SPI transfer parameters setting

Description

You can use this command to set SPI transfer parameters

SIM PIN	References
NO	Vendor

Syntax

Test Command	Responses
AT+CSPISETPARA=?	+ CSPISETPARA: (0-32), (0-1),(0-1) OK
Read Command	Responses
AT+CSPISETPARA?	+ CSPISETPARA: <bit>,<input packed>,<output unpacked> OK
Write Command	Responses
AT+CSPISETPARA =<bit>,<input packed>, <output unpacked>	OK ERROR

Defined values

<bit>

0-32 : set the number of bits to use per transfer unit, only support 8,16,32 bits

<input packed>

0 : data should be not packed into the user input buffer

1 : data should be packed into the user input buffer

<output unpacked>

0 : data should be not packed from the user output buffer

1 : data should be packed from the user output buffer

Examples

```
AT+ CSPISETPARA =16,0,1
OK
AT+ CSPISETPARA?
+ CSPISETPARA:16,0,1
OK
AT+ CSPISETPARA=?
+ CSPISETPARA : (0-32), (0-1),(0-1)
OK
```

3.5 AT+CSPIW write data

Description

You can use this command to write data

SIM PIN	References
NO	Vendor

Syntax

Test Command	Responses
AT+CSPIW=?	OK
Write Command	Responses
AT+CSPIW =<reg>,<data> ,<len>	OK
	ERROR

Defined values

<reg>

Register address. Input format must be hex, such as 0xFF.

<data>

Data written. Input format must be hex, such as 0xFF – 0xFFFFFFFF.

<len>

Read length. Range: 1-4; unit: byte.

Examples

```
AT+ CSPIW =0x0F, 0x1234, 2
OK
```

Note: If you want to write data only when you use SPI to connect to some special slave device, you can set <reg> to 0xFFFF.

3.6 AT+CSPIR read data

Description

You can use this command to read data

SIM PIN	References
NO	Vendor

Syntax

Test Command	Responses
AT+CSPIR=?	OK
Write Command	Responses
AT+CSPIR =<reg>,<len>	+ CSPIR: <data> OK
	ERROR

Defined values

<reg>
Register address. Input format must be hex, such as 0xFF.
<data>
Data read. Input format must be hex, such as 0xFF – 0xFFFFFFFF.
<len>
Read length. Range: 1-4; unit: byte.

Examples

AT+ CSPIR =0x0F, 2

+ CSPIR : 0x1234

OK

Note: If you want to read data only when you use SPI to connect to some special slave device, you can set <reg> to 0xFFFF.

4 SPI operating guide

SIM5XXX modules can support many kinds of device with SPI interface, such as: LCD module, AD/DA device, EEPROM , and so on. Our module SPI must be configured as the master.
The following steps give an example of using SPI function. In this example, the external slave device can be operated by AT commands.

- Step1: SPI clock rate setting. If your want to set clock is high when the clock is idle, clock runs only during a transfer start, and data input signal is sampled on the leading clock edge, you can set SIM5XXX by underside AT:

  AT+ CSPISETCLK =1,0,1

  OK

- Step2: SPI clock frequency setting. If slave device's clock is 13MHZ,AT+CSPISETF can be executed as follows. The last parameter is used to set the minimum time to wait between transfer units in nanoseconds。

  AT+ CSPISETF =1000000, 15000000 0,0

  OK

- Step3: SPI chip select setting. You want that slave is enabled all the time between transfer units and chip select is active low, AT+CSPISETCS is availability.

  AT+ CSPISETCS =1,0

  OK

- Step4: SPI transfer parameters setting. AT+ CSPISETPARA can set the number of bits to use per transfer unit and whether data is packed on data input or data ouput.Underside AT command can set 16 bits per transfer unit, input packed and output unpacked.

  AT+ CSPISETPARA =16,0,1

  OK

- Step5:Read data from slave device or write data to slave device.

  Read two byte data from valid address(such as 0x99) in slave device:

  AT+ CSPIR =0x99, 2

  + CSPIR : 0x1234

  OK

  Write two byte data(0x1234) to valid address(such as 0xff) in slave device:

  AT+ CSPIW =0xFF, 0x1234, 2

  OK

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