Digital Camera Register Reference

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1 Introduction

The Point Grey Digital Camera Register Reference is a source of general information pertaining to all PGR IEEE-1394 Imaging Products and select Stereo Vision Products.

This manual attempts to provide the user with a detailed specification of the various features, formats, modes, frame rates, and control parameters implemented by each PGR IEEE-1394 camera. It should be used in conjunction with the camera-specific *Technical Reference Manual* or *Getting Started Manual* to determine the full functionality offered by an individual camera system.

The reader should be aware that PGR camera systems are complex and dynamic – if any errors or omissions are found during experimentation, please contact us using our support web form at http://www.ptgrey.com/support/contact.

1.1. Scope and Applicable Cameras

The *Point Grey Digital Camera Register Reference* lists all of the registers that are used by the following PGR IEEE-1394 cameras:

- Bumblebee®2 (listed as BB2 in *Feature Availability* tables)
- Bumblebee XB3 (listed as BBX3 in *Feature Availability* tables)
- Chameleon™ (listed as CMLN in *Feature Availability* tables)
- Dragonfly®
- Dragonfly Express™ (listed as DX in *Feature Availability* tables)
- Dragonfly®2 (listed as DR2 in *Feature Availability* tables)
- Flea®
- Flea®2
- Firefly® MV (listed as FFMV in *Feature Availability* tables)
- Grasshopper (listed as GRAS in *Feature Availability* tables)
- Scorpion™

For a list of implemented registers for the Firefly and Firefly2, consult the TI chipset datasheet found at http://www.ptgrey.com/support/kb/details.asp?id=34.

Registers that implement a "Presence_Inq" bit will not have a "Feature Availability" table, since availability of the feature is indicated by a value of 1 for Presence_Inq. Not all registers are implemented by all cameras (see the section *Using this Manual*). For model-specific information, such as supported format and frame rates and detailed technical information, consult the *Technical Reference Manual* specifically for your camera.

1.2. IIDC DCAM Compliance

Most registers are implemented according to the *IIDC 1394-based Digital Camera (DCAM) Specification Version 1.30*. Other registers are implemented according to Version 1.31 of the DCAM specification; these registers are noted with a **(v1.31)** beside the register name. Most registers detailed in *Advanced Registers* are outside of the DCAM specification; those that are not are explicitly noted.

1.3. Using this Manual

1.3.1. Register Hex Values

Register offsets and values are generally referred to in their hexadecimal forms, represented by either a '0x' before the number or 'h' after the number, e.g. the decimal number 255 can be represented as 0xFF or FFh.

1.3.2. Format

The *Format* table describes the purpose of each bit in the 32-bit register. Bit 0 is always the most significant bit of the register value. Some bits have an associated field name listed in the *Field* column of the *Format* table. Field names are always *italicized* when referred to outside of the *Format* table.

1.3.3. Feature Availability

The *Feature Availability* table describes whether some or all of the functionality defined by that register is implemented or used by the specified camera (indicated by a '✓'). Registers that implement a *Presence_Inq* bit, or where a separate feature inquiry (e.g. BRIGHTNESS_INQ) register is present, will not have this table.

Some registers have multiple functions associated with them e.g. ONE_SHOT / MULTI_SHOT register 0x61C, or IMAGE_DATA_FORMAT register 0x1048. A '✓' is not meant to indicate that the specified camera implements all of these functions. To determine the specific functions that are implemented, use the appropriate Feature Inquiry Registers or refer to the camera's *Technical Reference* manual.

If a camera family (e.g. Dragonfly2) or specific model of camera (e.g. DR2-HICOL) does not implement any of the functionality defined by a register, it will not be listed in the *Feature Availability* table. In some cases, it may be listed but with a minus (**-**) sign shown together with the comment, "Not implemented".

> *In cases where only a single camera is listed in the* Feature Availability *table, this register is used only by the specified camera and no other cameras.*

1.3.4. Other Resources

The *Other Resources* table points users to other sources of information pertinent to the register being described. These sources can include other reference manuals or documents, software programs or example code, or on-line knowledge base articles.

> *The* Glossary *section near the end of this manual is a useful reference for many of the words used throughout.*

2 Camera Control Command Registers

This section details all of the registers implemented by PGR IEEE-1394 cameras. As a general rule, PGR IEEE-1394 cameras conform to the *IIDC 1394-based Digital Camera Specification v1.30* (DCAM specification). Many PGR cameras also conform to the later 1.31 version of the specification; check your camera's *Technical Reference* or *Getting Started Manual* for specific DCAM compliance. The DCAM specification can be purchased from the 1394 Trade Association (http://www.1394ta.org/).

2.1. Register Memory Map

The IEEE-1394 specification uses a 64-bit fixed addressing model. The upper 10 bits show the Bus ID, and the next six bits show the Node ID. The next 20 bits must be 1 (FFFF Fh).

Address	Register Name	Description	Section
FFFF F000 0000h	1394 base address		
FFFF F000 0400h	Config ROM		
FFFF F0F0 0000h	Base address for all camera control command registers		
The following register addresses are offset from the base address, FFFF F0F0 0000h.			
000h	INITIALIZE	Camera initialize register	*2.4*
100h 180h	V_FORMAT_INQ V_MODE_INQ_X	Inquiry register for video format Inquiry register for video mode	*2.5.1* *2.5.2*
200h	V_RATE_INQ_y_X	Inquiry register for video frame rate	*2.5.3*
300h	Reserved		
400h	BASIC_FUNC_INQ FEATURE_HI_INQ FEATURE_LO_INQ	Inquiry register for feature presence	*2.6* *2.7*
500h	*Feature_Name*_INQ	Inquiry register for feature elements	*2.8*
600h 640h	CAM_STA_CTRL	Status and control register for camera Feature control error status register	*2.9*
700h	ABS_CSR_HI_INQ_x	Inquiry register for Absolute value CSR offset address	*2.12.1*
800h	*Feature_Name*	Status and control register for feature	*2.10*

The *PGR FlyCapture* API library has function calls to get and set camera register values. These function calls automatically take into account the base address. For example, to get the 32-bit value of the SHUTTER register at 0xFFFF F0F0 081C:

```
flycaptureGetCameraRegister( context, 0x81C, &ulValue );
```

2.2. Config ROM

2.2.1. Root Directory

	Offset	Bit	Description
Bus Info Block	400h	[0-7]	04h
		[8-15]	crc_length
		[16-31]	rom_crc_value
	404h	[0-7]	31h
		[8-15]	33h
		[16-23]	39h
		[24-31]	34h
	408h	[0-3]	0010 (binary)
		[4-7]	Reserved
		[8-15]	FFh
		[16-19]	max_rec
		[20]	Reserved
		[21-23]	mxrom
		[24-31]	chip_id_hi
	40Ch	[0-23]	node_vendor_id
		[24-31]	chip_id_hi
	410h	[0-31]	chip_id_lo
Root Directory	414h	[0-15]	0004h
		[16-31]	CRC
	418h	[0-7]	03h
		[8-31]	module_vendor_id
	41Ch	[0-7]	0Ch
		[8-15]	Reserved
		[16-31]	1000001111000000 (binary)
	420h	[0-7]	8Dh
		[8-31]	indirect_offset
	424h	[0-7]	D1h
		[8-31]	unit_directory_offset

2.2.2. Unit Directory

	Offset	Bit	Description
Unit Directory	0000h	[0-15]	0003h
		[16-31]	CRC
	0004h	[0-7]	12h
		[8-31]	unit_spec_ID (=0x00A02D)
	0008h	[0-7]	13h
		[8-31]	unit_sw_version (=0x000102)
	000Ch	[0-7]	D4h
		[8-31]	unit dependent directory offset

2.2.3. Unit Dependent Info

	Offset	Bit	Description
Unit Dependent Info	0000h	[0-15]	unit_dep_info_length
		[16-31]	CRC
	0004h	[0-7]	40h
		[8-31]	command_regs_base
	0008h	[0-7]	81h
		[8-31]	vendor_name_leaf
	000Ch	[0-7]	82h
		[8-31]	model_name_leaf
	0010h	[0-7]	38h
		[8-31]	unit_sub_sw_version
	0014h	[0-7]	39h
		[8-31]	Reserved
	0018h	[0-7]	3Ah
		[8-31]	Reserved
	001Ch	[0-7]	3Bh
		[8-31]	Reserved
	0020h	[0-7]	3Ch
		[8-31]	vendor_unique_info_0
	0024h	[0-7]	3Dh
		[8-31]	vendor_unique_info_1
	0028h	[0-7]	3Eh
		[8-31]	vendor_unique_info_2
	002Ch	[0-7]	3Fh
		[8-31]	vendor_unique_info_3

- *command_regs_base* is the quadlet offset from the base address of initial register space of the base address of the command registers.
- *vendor_name_leaf* specifies the number of quadlets from the address of the vendor_name_leaf entry to the address of the vendor_name leaf containing an ASCII representation of the vendor name of this node.
- *model_name_leaf* specifies the number of quadlets from the address of the model_name_leaf entry to the address of the model_name leaf containing an ASCII representation of the model name of this node.
- *unit_sub_sw_version* specifies the sub version information of this unit:
  - unit_sub_sw_version = 0x000000h or unspecified for IIDC v1.30
  - unit_sub_sw_version = 0x000010h for IIDC v1.31
  - unit_sub_sw_version = 0x000090h for IIDC v1.39

2.3. Calculating Register Addresses using Quadlet Offsets

The addresses for many DCAM control and status registers (CSR's), such as those that provide control over absolute values, Format_7 video modes, PIO, SIO and strobe output, vary between camera manufacturers. In order to provide a common mechanism across camera models for determining the location of these CSR's relative to the 1394 base address, the DCAM specification provides fixed locations for inquiry registers that contain quadlet offsets, or pointers, to the actual offsets.

For example, the Absolute Value CSR's provide minimum, maximum and current real-world values for camera properties such as gain, shutter, etc., as described in the *Absolute Value Register Format* section. To determine the location of the shutter absolute value registers (code snippets use function calls included in the PGR FlyCapture SDK):

1. Read the ABS_CSR_HI_INQ_7 register 71Ch to obtain the quadlet offset for the absolute value CSR for shutter:

   ```
   flycaptureGetCameraRegister( context, 0x71C, &ulValue );
   ```

2. The 32-bit ulValue is a quadlet offset, so multiply by 4 to get the actual offset:

   ```
   ulValue = ulValue * 4; // ulValue == 0x3C0244, actual offset == 0xF00910
   ```

3. The actual offset 0xF00910 represents the offset from the 1394 base address 0xFFFF Fxxx xxxx. Since the *PGR FlyCapture API* automatically takes into account the 1394 base offset 0xFFFF F0F0 0000, the actual offset in this example would be 0x910.

   ```
   ulValue = ulValue << 12; // Bit shift left 12 bits == 0x910
   ```

2.4. Camera Initialize Register

Format:

Offset	Name	Field	Bit	Description
000h	INITIALIZE	Initialize	[0]	If this bit is set to 1, the camera will reset to its initial state and default settings. This bit is self-cleared.
		-	[1-31]	Reserved

Feature Availability:

Camera	Model/Sensor	Firmware	Avail.	Notes
ALL	ALL	ALL	✓	This register is supported on all PGR IEEE-1394 DCAM cameras

2.5. Inquiry Registers for Video Format / Mode / Frame Rate

The following registers may be used to determine the video formats, modes and frame rates that are available with the camera.

(Bit values = 0: Not Available, 1: Available)

2.5.1. Video Format Inquiry Registers

Format:

Offset	Name	Field	Bit	Description

100h	V_FORMAT_INQ	Format_0	[0]	VGA non-compressed format (160x120 through 640x480)
		Format_1	[1]	Super VGA non-compressed format (1) (800x600 through 1024x768)
		Format_2	[2]	Super VGA non-compressed format (2) (1280x960 through 1600x1200)
		Format_x	[3-5]	Reserved for other formats
		Format_6	[6]	Still Image Format
		Format_7	[7]	Partial Image Size Format
			[8-31]	Reserved

2.5.2. Video Mode Inquiry Registers

Format:

Offset	Name	Field	Bit	Description
180h	V_MODE_INQ_O (Format 0)	Mode_0	[0]	160x120 YUV(4:4:4) Mode (24bit/pixel)
		Mode_1	[1]	320x240 YUV(4:2:2) Mode (16bit/pixel)
		Mode_2	[2]	640x480 YUV(4:1:1) Mode (12bit/pixel)
		Mode_3	[3]	640x480 YUV(4:2:2) Mode (16bit/pixel)
		Mode_4	[4]	640x480 RGB Mode (24bit/pixel)
		Mode_5	[5]	640x480 Y8 (Mono) Mode (8bit/pixel)
		Mode_6	[6]	640x480 Y16 (Mono16) Mode (16bit/pixel)
			[7-31]	Reserved
184h	V_MODE_INQ_1 (Format 1)	Mode_0	[0]	800x600 YUV(4:2:2) Mode (16bit/pixel)
		Mode_1	[1]	800x600 RGB Mode (24bit/pixel)
		Mode_2	[2]	800x600 Y (Mono) Mode (8bit/pixel)
		Mode_3	[3]	1024x768 YUV(4:2:2) Mode (16bit/pixel)
		Mode_4	[4]	1024x768 RGB Mode (24bit/pixel)
		Mode_5	[5]	1024X768 Y (MONO) MODE (8BIT/PIXEL)
		Mode_6	[6]	800x600 Y (Mono16) Mode (16bit/pixel)
		Mode_7	[7]	1024x768 Y (Mono16) Mode (16bit/pixel)
			[8-31]	Reserved
188h	V_MODE_INQ_2 (Format 2)	Mode_0	[0]	1280x960 YUV(4:2:2) Mode (16bit/pixel)
		Mode_1	[1]	1280x960 RGB Mode (24bit/pixel)
		Mode_2	[2]	1280x960 Y (Mono) Mode (8bit/pixel)
		Mode_3	[3]	1600x1200 YUV(4:2:2) Mode (16bit/pixel)
		Mode_4	[4]	1600X1200 RGB MODE (24BIT/PIXEL)
		Mode_5	[5]	1600x1200 Y (Mono) Mode (8bit/pixel)
		Mode_6	[6]	1280x960 Y (Mono16) Mode (16bit/pixel)
		Mode_7	[7]	1600X 1200 Y (Mono16) Mode (16bit/pixel)
			[8-31]	Reserved
18Ch : 197h	Reserved			
19Ch	V_MODE_INQ_7 (Format 7)	Mode_0	[0]	Format_7 Mode_0
		Mode_1	[1]	Format_7 Mode_1
		Mode_2	[2]	Format_7 Mode_2

		Mode_3	[3]	Format_7 Mode_3
		Mode_4	[4]	Format_7 Mode_4
		Mode_5	[5]	Format_7 Mode_5
		Mode_6	[6]	Format_7 Mode_6
		Mode_7	[7]	Format_7 Mode_7
			[8-31]	Reserved

2.5.3. Video Frame Rate Inquiry Registers

This set of registers allows the user to query the available frame rates for all Formats and Modes.

Format:

Offset	Name	Field	Bit	Description
200h	V_RATE_INQ_0_0 (Format 0, Mode 0)	FrameRate_0	[0]	Reserved
		FrameRate_1	[1]	Reserved
		FrameRate_2	[2]	7.5fps
		FrameRate_3	[3]	15fps
		FrameRate_4	[4]	30fps
		FrameRate_5	[5]	60fps
		FrameRate_6	[6]	120fps
		FrameRate_7	[7]	240fps
			[8-31]	Reserved
204h	V_RATE_INQ_0_1 (Format 0, Mode 1)	FrameRate_0	[0]	1.875fps
		FrameRate_1	[1]	3.75fps
		FrameRate_2	[2]	7.5fps
		FrameRate_3	[3]	15fps
		FrameRate_4	[4]	30fps
		FrameRate_5	[5]	60fps
		FrameRate_6	[6]	120fps
		FrameRate_7	[7]	240fps
			[8-31]	Reserved
208h	V_RATE_INQ_0_2 (Format 0, Mode 2)	FrameRate_0	[0]	1.875fps
		FrameRate_1	[1]	3.75fps
		FrameRate_2	[2]	7.5fps
		FrameRate_3	[3]	15fps
		FrameRate_4	[4]	30fps
		FrameRate_5	[5]	60fps
		FrameRate_6	[6]	120fps
		FrameRate_7	[7]	240fps
			[8-31]	Reserved
20Ch	V_RATE_INQ_0_3 (Format 0, Mode 3)	FrameRate_0	[0]	1.875fps
		FrameRate_1	[1]	3.75fps
		FrameRate_2	[2]	7.5fps
		FrameRate_3	[3]	15fps
		FrameRate_4	[4]	30fps
		FrameRate_5	[5]	60fps
		FrameRate_6	[6]	120fps

		FrameRate_7	[7]	240fps
			[8-31]	Reserved
210h	V_RATE_INQ_0_4 (Format 0, Mode 4)	FrameRate_0	[0]	1.875fps
		FrameRate_1	[1]	3.75fps
		FrameRate_2	[2]	7.5fps
		FrameRate_3	[3]	15fps
		FrameRate_4	[4]	30fps
		FrameRate_5	[5]	60fps
		FrameRate_6	[6]	120fps
		FrameRate_7	[7]	240fps
			[8-31]	Reserved
214h	V_RATE_INQ_0_5 (Format 0, Mode 5)	FrameRate_0	[0]	1.875fps
		FrameRate_1	[1]	3.75fps
		FrameRate_2	[2]	7.5fps
		FrameRate_3	[3]	15fps
		FrameRate_4	[4]	30fps
		FrameRate_5	[5]	60fps
		FrameRate_6	[6]	120fps
		FrameRate_7	[7]	240fps
			[8-31]	Reserved
218h	V_RATE_INQ_0_6 (Format 0, Mode 6)	FrameRate_0	[0]	1.875fps
		FrameRate_1	[1]	3.75fps
		FrameRate_2	[2]	7.5fps
		FrameRate_3	[3]	15fps
		FrameRate_4	[4]	30fps
		FrameRate_5	[5]	60fps
		FrameRate_6	[6]	120fps
		FrameRate_7	[7]	240fps
			[8-31]	Reserved
21Ch : 21Fh	Reserved			
220h	V_RATE_INQ_1_0 (Format 1, Mode 0)	FrameRate_0	[0]	Reserved
		FrameRate_1	[1]	3.75fps
		FrameRate_2	[2]	7.5fps
		FrameRate_3	[3]	15fps
		FrameRate_4	[4]	30fps
		FrameRate_5	[5]	60fps
		FrameRate_6	[6]	120fps
		FrameRate_7	[7]	240fps
			[8-31]	Reserved
224h	V_RATE_INQ_1_1 (Format 1, Mode 1)	FrameRate_0	[0]	Reserved
		FrameRate_1	[1]	Reserved
		FrameRate_2	[2]	7.5fps
		FrameRate_3	[3]	15fps
		FrameRate_4	[4]	30fps

		FrameRate_5	[5]	60fps
		FrameRate_6	[6]	120fps
		FrameRate_7	[7]	Reserved
			[8-31]	Reserved
228h	V_RATE_INQ_1_2 (Format 1, Mode 2)	FrameRate_0	[0]	Reserved
		FrameRate_1	[1]	Reserved
		FrameRate_2	[2]	7.5fps
		FrameRate_3	[3]	15fps
		FrameRate_4	[4]	30fps
		FrameRate_5	[5]	60fps
		FrameRate_6	[6]	120fps
		FrameRate_7	[7]	240fps
			[8-31]	Reserved
22Ch	V_RATE_INQ_1_3 (Format 1, Mode 3)	FrameRate_0	[0]	1.875fps
		FrameRate_1	[1]	3.75fps
		FrameRate_2	[2]	7.5fps
		FrameRate_3	[3]	15fps
		FrameRate_4	[4]	30fps
		FrameRate_5	[5]	60fps
		FrameRate_6	[6]	120fps
		FrameRate_7	[7]	Reserved
			[8-31]	Reserved
230h	V_RATE_INQ_1_4 (Format 1, Mode 4)	FrameRate_0	[0]	1.875fps
		FrameRate_1	[1]	3.75fps
		FrameRate_2	[2]	7.5fps
		FrameRate_3	[3]	15fps
		FrameRate_4	[4]	30fps
		FrameRate_5	[5]	60fps
		FrameRate_6	[6]	Reserved
		FrameRate_7	[7]	Reserved
			[8-31]	Reserved
234h	V_RATE_INQ_1_5 (Format 1, Mode 5)	FrameRate_1	[1]	3.75fps
		FrameRate_2	[2]	7.5fps
		FrameRate_3	[3]	15fps
		FrameRate_4	[4]	30fps
		FrameRate_5	[5]	60fps
		FrameRate_6	[6]	120fps
		FrameRate_7	[7]	240fps
			[8-31]	Reserved
238h	V_RATE_INQ_1_6 (Format 1, Mode 6)	FrameRate_0	[0]	Reserved
		FrameRate_1	[1]	3.75fps
		FrameRate_2	[2]	7.5fps
		FrameRate_3	[3]	15fps
		FrameRate_4	[4]	30fps
		FrameRate_5	[5]	60fps
		FrameRate_6	[6]	120fps

		FrameRate_7	[7]	240fps
			[8-31]	Reserved
23Ch	V_RATE_INQ_1_7 (Format 1, Mode 7)	FrameRate_0	[0]	1.875fps
		FrameRate_1	[1]	3.75fps
		FrameRate_2	[2]	7.5fps
		FrameRate_3	[3]	15fps
		FrameRate_4	[4]	30fps
		FrameRate_5	[5]	60fps
		FrameRate_6	[6]	120fps
		FrameRate_7	[7]	Reserved
			[8-31]	Reserved
240h	V_RATE_INQ_2_0 (Format 2, Mode 0)	FrameRate_0	[0]	1.875fps
		FrameRate_1	[1]	3.75fps
		FrameRate_2	[2]	7.5fps
		FrameRate_3	[3]	15fps
		FrameRate_4	[4]	30fps
		FrameRate_5	[5]	60fps
		FrameRate_6	[6]	Reserved
		FrameRate_7	[7]	Reserved
			[8-31]	Reserved
244h	V_RATE_INQ_2_1 (Format 2, Mode 1)	FrameRate_0	[0]	1.875fps
		FrameRate_1	[1]	3.75fps
		FrameRate_2	[2]	7.5fps
		FrameRate_3	[3]	15fps
		FrameRate_4	[4]	30fps
		FrameRate_5	[5]	60fps
		FrameRate_6	[6]	Reserved
		FrameRate_7	[7]	Reserved
			[8-31]	Reserved
248h	V_RATE_INQ_2_2 (Format 2, Mode 2)	FrameRate_0	[0]	1.875fps
		FrameRate_1	[1]	3.75fps
		FrameRate_2	[2]	7.5fps
		FrameRate_3	[3]	15fps
		FrameRate_4	[4]	30fps
		FrameRate_5	[5]	60fps
		FrameRate_6	[6]	120fps
		FrameRate_7	[7]	Reserved
			[8-31]	Reserved
24Ch	V_RATE_INQ_2_3 (Format 2, Mode 3)	FrameRate_0	[0]	1.875fps
		FrameRate_1	[1]	3.75fps
		FrameRate_2	[2]	7.5fps
		FrameRate_3	[3]	15fps
		FrameRate_4	[4]	30fps
		FrameRate_5	[5]	60fps
		FrameRate_6	[6]	Reserved
		FrameRate_7	[7]	Reserved

			[8-31]	Reserved
250h	V_RATE_INQ_2_4 (Format 2, Mode 4)	FrameRate_0	[0]	1.875fps
		FrameRate_1	[1]	3.75fps
		FrameRate_2	[2]	7.5fps
		FrameRate_3	[3]	15fps
		FrameRate_4	[4]	30fps
		FrameRate_5	[5]	Reserved
		FrameRate_6	[6]	Reserved
		FrameRate_7	[7]	Reserved
			[8-31]	Reserved
254h	V_RATE_INQ_2_5 (Format 2, Mode 5)	FrameRate_0	[0]	1.875fps
		FrameRate_1	[1]	3.75fps
		FrameRate_2	[2]	7.5fps
		FrameRate_3	[3]	15fps
		FrameRate_4	[4]	30fps
		FrameRate_5	[5]	60fps
		FrameRate_6	[6]	120fps
		FrameRate_7	[7]	Reserved
			[8-31]	Reserved
258h	V_RATE_INQ_2_6 (Format 2, Mode 6)	FrameRate_0	[0]	1.875fps
		FrameRate_1	[1]	3.75fps
		FrameRate_2	[2]	7.5fps
		FrameRate_3	[3]	15fps
		FrameRate_4	[4]	30fps
		FrameRate_5	[5]	60fps
		FrameRate_6	[6]	Reserved
		FrameRate_7	[7]	Reserved
			[8-31]	Reserved
25Ch	V_RATE_INQ_2_7 (Format 2, Mode 7)	FrameRate_0	[0]	1.875fps
		FrameRate_1	[1]	3.75fps
		FrameRate_2	[2]	7.5fps
		FrameRate_3	[3]	15fps
		FrameRate_4	[4]	30fps
		FrameRate_5	[5]	60fps
		FrameRate_6	[6]	Reserved
		FrameRate_7	[7]	Reserved
			[8-31]	Reserved
260h : 2BFh	Reserved			
2E0h	V_CSR_INQ_7_0	Mode_0	[0-31]	CSR quadlet offset for Format_7 Mode_0
2E4h	V_CSR_INQ_7_1	Mode_1	[0-31]	CSR quadlet offset for Format_7 Mode_1
2E8h	V_CSR_INQ_7_2	Mode_2	[0-31]	CSR quadlet offset for Format_7 Mode_2

2ECh	V_CSR_INQ_7_3	Mode_3	[0-31]	CSR quadlet offset for Format_7 Mode_3
2F0h	V_CSR_INQ_7_4	Mode_4	[0-31]	CSR quadlet offset for Format_7 Mode_4
2F4h	V_CSR_INQ_7_5	Mode_5	[0-31]	CSR quadlet offset for Format_7 Mode_5
2F8h	V_CSR_INQ_7_6	Mode_6	[0-31]	CSR quadlet offset for Format_7 Mode_6
2FCh	V_CSR_INQ_7_7	Mode_7	[0-31]	CSR quadlet offset for Format_7 Mode_7

2.6. Inquiry Registers for Basic Functions

The following registers show which DCAM-compliant basic functions are implemented on the camera.

(Bit values = 0: Not Available, 1: Available)

Format:

Offset	Name	Field	Bit	Description
400h	BASIC_FUNC_INQ	Advanced_Feature_Inq	[0]	Inquiry for advanced feature. (Vendor Unique Features)
		Vmode_Error_Status_Inq	[1]	Inquiry for existence of Vmode_Error_Status register
		Feature_Control_Error_Status_Inq	[2]	Inquiry for existence of Feature_Control_Error_Status register
		Opt_Func_CSR_Inq	[3]	Inquiry for optional function CSR.
			[4-7]	Reserved
		1394.b_mode_Capability	[8]	Inquiry for 1394.b mode capability
			[9-15]	Reserved
		Cam_Power_Cntl	[16]	Camera process power ON/OFF capability
			[17-18]	Reserved
		One_Shot_Inq	[19]	One shot transmission capability
		Multi_Shot_Inq	[20]	Multi shot transmission capability
			[21-27]	Reserved

		Memory_Channel	[28-31]	Maximum memory channel number (N) Memory channel no 0 = Factory setting memory 1 = Memory Ch 1 2 = Memory Ch 2 : N= Memory Ch N If 0000, user memory is not available.

2.7. Inquiry Registers for Feature Presence

The following registers show the presence of the DCAM-compliant camera features or optional functions implemented on the camera.

(Bit values = 0: Not Available, 1: Available)

Format:

Offset	Name	Field	Bit	Description
404h	Feature_Hi_Inq	Brightness	[0]	Brightness Control
		Auto_Exposure	[1]	Auto Exposure Control
		Sharpness	[2]	Sharpness Control
		White_Balance	[3]	White Balance Control
		Hue	[4]	Hue Control
		Saturation	[5]	Saturation Control
		Gamma	[6]	Gamma Control
		Shutter	[7]	Shutter Speed Control
		Gain	[8]	Gain Control
		Iris	[9]	IRIS Control
		Focus	[10]	Focus Control
		Temperature	[11]	Temperature Control
		Trigger	[12]	Trigger Control
		Trigger_Delay	[13	Trigger Delay Control
		White_Shading	[14]	White Shading Compensation Control
		Frame_Rate	[15]	Frame rate prioritize control
			[16-31]	Reserved
408h	Feature_Lo_Inq	Zoom	[0]	Zoom Control
		Pan	[1]	Pan Control
		Tilt	[2]	Tilt Control
		Optical Filter	[3]	Optical Filter Control
			[4-15]	Reserved
		Capture_Size	[16]	Capture image size for Format_6
		Capture_Quality	[17]	Capture image quality for Format_6
			[18-31]	Reserved
40Ch	Opt_Function_Inq	-	[0]	Reserved
		PIO	[1]	Parallel input/output control
		SIO	[2]	Serial Input/output control
		Strobe_Output	[3]	Strobe signal output
		-	[4-31]	Reserved
410h-47Fh	Reserved			

480h	Advanced_Feature_Inq	Advanced_Feature_Quadlet_Offset	[0-31]	Quadlet offset of the advanced feature CSR's (see the *Advanced Registers* section) from the base address of initial register space. (Vendor unique)
484h	PIO_Control_CSR_Inq	PIO_Control_Quadlet_Offset	[0-31]	Quadlet offset of the PIO control CSR's (see the *Parallel Input/Output (PIO)* section) from the base address of initial register space.
488h	SIO_Control_CSR_Inq	SIO_Control_Quadlet_Offset	[0-31]	Quadlet offset of the SIO control CSR's (see the *Serial Port Input/Output (SIO)* section) from the base address of initial register space.
48Ch	Strobe_Output_CSR_Inq	Strobe_Output_Quadlet_Offset	[0-31]	Quadlet offset of the strobe output signal CSR's (see the *Strobe Signal Output* section) from the base address of initial register space.

2.8. Inquiry Registers for Feature Elements

The following registers show the presence of specific features, modes and minimum and maximum values for each of the DCAM-compliant camera features or optional functions implemented by the camera (see the section *Inquiry Registers for Feature Presence*).

(Bit values = 0: Not Available, 1: Available)

Format:

Offset	Name	Field	Bit	Description
500h	BRIGHTNESS_INQ	Presence_Inq	[0]	Presence of this feature
		Abs_Control_Inq	[1]	Absolute value control
			[2]	Reserved
		One_Push_Inq	[3]	One push auto mode (controlled automatically by camera only once)
		ReadOut_Inq	[4]	Ability to read the value of this feature
		On_Off_Inq	[5]	Ability to switch feature ON and OFF
		Auto_Inq	[6]	Auto mode (controlled automatically by camera)
		Manual_Inq	[7]	Manual mode (controlled by user)
		Min_Value	[8-19]	Minimum value for this feature control
		Max_Value	[20-31]	Maximum value for this feature control
504h	AUTO_EXPOSURE_INQ	Same format as the BRIGHTNESS_INQ register		
508h	SHARPNESS_INQ	Same format as the BRIGHTNESS_INQ register		
50Ch	WHITE_BALANCE_INQ	Same format as the BRIGHTNESS_INQ register		
510h	HUE_INQ	Same format as the BRIGHTNESS_INQ register		
514h	SATURATION_INQ	Same format as the BRIGHTNESS_INQ register		
518h	GAMMA_INQ	Same format as the BRIGHTNESS_INQ register		
51Ch	SHUTTER_INQ	Same format as the BRIGHTNESS_INQ register		
520h	GAIN_INQ	Same format as the BRIGHTNESS_INQ register		

524h	IRIS_INQ	Same format as the BRIGHTNESS_INQ register			
528h	FOCUS_INQ	Same format as the BRIGHTNESS_INQ register			
52Ch	TEMPERATURE_INQ	Same format as the BRIGHTNESS_INQ register			
530h	TRIGGER_INQ	Presence_Inq	[0]	Presence of this feature	
		Abs_Control_Inq	[1]	Absolute value control	
			[2-3]	Reserved	
		ReadOut_Inq	[4]	Ability to read the value of this feature	
		On_Off_Inq	[5]	Ability to switch feature ON and OFF	
		Polarity_Inq	[6]	Ability to change trigger input polarity	
		Value_Read_Inq	[7]	Ability to read raw trigger input	
		Trigger_Source0_Inq	[8]	Presence of Trigger Source 0	ID=0
		Trigger_Source1_Inq	[9]	Presence of Trigger Source 1	ID=1
		Trigger_Source2_Inq	[10]	Presence of Trigger Source 2	ID=2
		Trigger_Source3_Inq	[11]	Presence of Trigger Source 3	ID=3
			[12-14]	Reserved	ID=4-6
		Software_Trigger_Inq	[15]	Presence of Software Trigger	ID=7
		Trigger_Mode0_Inq	[16]	Presence of Trigger Mode 0	
		Trigger_Mode1_Inq	[17]	Presence of Trigger Mode 1	
		Trigger_Mode2_Inq	[18]	Presence of Trigger Mode 2	
		Trigger_Mode3_Inq	[19]	Presence of Trigger Mode 3	
		Trigger_Mode4_Inq	[20]	Presence of Trigger Mode 4	
		Trigger_Mode5_Inq	[21]	Presence of Trigger Mode 5	
			[22-29]	Reserved	
		Trigger_Mode14_Inq	[30]	Presence of Trigger Mode 14 (Vendor unique trigger mode 0)	
		Trigger_Mode15_Inq	[31]	Presence of Trigger Mode 15 (Vendor unique trigger mode 1)	
534h	TRIGGER_DLY_INQ	Presence_Inq	[0]	Presence of this feature	
		Abs_Control_Inq	[1]	Absolute value control	
			[2]	Reserved	
		One_Push_Inq	[3]	One push auto mode (controlled automatically by camera only once)	
		ReadOut_Inq	[4]	Ability to read the value of this feature	
		On_Off_Inq	[5]	Ability to switch feature ON and OFF	
			[6-7]	Reserved	
		Min_Value	[8-19]	Minimum value for this feature control	
		Max_Value	[20-31]	Maximum value for this feature control	
538h	WHITE_SHD_INQ	Same format as the BRIGHTNESS_INQ register			
53Ch	FRAME_RATE_INQ	Same format as the BRIGHTNESS_INQ register			
540h : 57Ch	Reserved for other FEATURE_HI_INQ				
580h	ZOOM_INQ	Presence_Inq	[0]	Presence of this feature	
		Abs_Control_Inq	[1]	Absolute value control	
			[2]	Reserved	
		One_Push_Inq	[3]	One push auto mode (controlled automatically by camera only once)	
		ReadOut_Inq	[4]	Ability to read the value of this feature	

		On_Off_Inq	[5]	Ability to switch feature ON and OFF
		Auto_Inq	[6]	Auto mode (controlled automatically by camera)
		Manual_Inq	[7]	Manual mode (controlled by user)
		Min_Value	[8-19]	Minimum value for this feature control
		Max_Value	[20-31]	Maximum value for this feature control
584h	PAN_INQ	Same format as the ZOOM_INQ register		
588h	TILT_INQ	Same format as the ZOOM_INQ register		
58Ch	OPTICAL_FILTER_INQ	Same format as the ZOOM_INQ register		

2.9. Control and Status Registers (CSRs)

The following section details a series of standard control and status registers.

2.9.1. CURRENT_FRAME_RATE: 600h

Allows the user to query and modify the current frame rate of the camera.

Format:

Field	Bit	Description
Cur_V_Frm_Rate	[0-2]	Current frame rate FrameRate_0 .. FrameRate_7
	[3-31]	Reserved.

Camera Notes:

Camera	Model/Sensor	Firmware	Avail.	Notes
Dragonfly	ALL	2.1.2.14	✓	Changes to EXTENDED_SHUTTER register 1028h will affect the published frame rates. For example, if the camera is put into 32Hz mode, frame rate 4 would become 32, 3 would become 16, etc. This is true for all extended shutter modes except for the 50Hz mode.

2.9.2. CURRENT_VIDEO_MODE: 604h

Allows the user to query and modify the current video mode of the camera.

Format:

Field	Bit	Description
Cur_V_Mode	[0-2]	Current video mode Mode_0 .. Mode_7
	[3-31]	Reserved.

2.9.3. CURRENT_VIDEO_FORMAT: 608h

Allows the user to query and modify the current video format of the camera.

Format:

Field	Bit	Description
Cur_V_Format	[0-2]	Current video format Format_0 .. Format_7
	[3-31]	Reserved.

2.9.4. ISO_CHANNEL / ISO_SPEED: 60Ch

Allows the user to query the camera's isochronous transmission channel and speed information.

Format:

Field	Bit	Description
ISO_Channel	[0-3]	Isochronous channel number for video data transmission (Except for Format_6)
	[4-5]	Reserved
ISO_Speed	[6-7]	Isochronous transmit speed code. (Except for Format_6) 0 = 100Mbps 1 = 200Mbps 2 = 400Mbps
	[8-15]	Reserved
Operation_Mode	[16]	1394 operation mode Change control register sets of ISO_Channel and ISO_Speed registers 0 = Legacy (v1.30 compatible) 1 = 1394.b (v1.31 mode) Camera shall start in legacy mode for backward compatibility
	[17]	Reserved
ISO_Channel_B	[18-23]	Isochronous channel number for video data transmission of 1394.b mode (Except for Format_6)
	[24-28]	Reserved
ISO_Speed_B	[29-31]	Isochronous transmit speed code of 1394.b mode (Except for Format_6) 0 = 100Mbps 1 = 200Mbps 2 = 400Mbps 3 = 800Mbps 4 = 1.6Gbps 5 = 3.2Gbpss

2.9.5. CAMERA_POWER: 610h

Allows the user to power-up or power-down components of the camera. The exact components, e.g. image sensor, A/D converter, other board electronics, will vary between camera models.

If isochronous transmit (ISO_EN / ONE_SHOT / MULTI_SHOT) is enabled while the camera is powered down, the camera will automatically write *Cam_Pwr_Ctrl* = 1 to power itself up. However, disabling isochronous transmit does not automatically power-down the camera.

The camera will typically not send the first two images acquired after power-up unless the camera is in asynchronous trigger mode. The auto-exposure algorithm does not run while the camera is powered down. It may therefore take several (*n*) images to get a satisfactory image, where *n* is undefined.

Format:

Field	Bit	Description
Cam_Pwr_Ctrl	[0]	Write: 0: Begin power-down process 1: Begin power-up process Read: 0: Camera is powered down, or in the process of powering up i.e., bit will be zero until camera completely powered up (outside IIDC specification). 1: Camera is powered up
	[1-30]	Reserved
Camera_Power_Status	[31]	Read only Read: the pending value of *Cam_Pwr_Ctrl*

2.9.6. ISO_EN / CONTINUOUS_SHOT: 614h

This register allows the control of isochronous data transmission. Continuous shot must be enabled (Bit 0 = 1) to generate a software trigger using SOFT_ASYNC_TRIGGER register 102Ch. During ISO_EN = 1 or One_Shot = 1 or Multi_Shot =1, the register value which reflects the Isochronous packet format cannot change. Data transfer control priority is ISO_EN > One_Shot > Multi_Shot.

Format:

Field	Bit	Description
ISO_EN / Continuous Shot	[0]	1 = Start ISO transmission of video data. 0 = Stop ISO transmission of video data. Continuous Shot is not enabled.
	[1-31]	Reserved.

2.9.7. MEMORY_SAVE: 618h

This register allows the user to control whether the current status and modes are saved to the memory channel specified in the MEM_SAVE_CH register 0x620.

There is currently no way to save modifications to the default LUT or SIO configuration.

All channels can be reset back to the original factory defaults by writing the value 0xDEAFBEEF to *Memory_Save* (ignores MEM_SAVE_CH). The factory defaults channel can be overwritten by writing the value 0x87654321 to the MEMORY_SAVE register 618h when *Mem_Save_Ch* [620h] is zero.

Refer to the Appendix section *Memory Channel Registers* for a complete list of registers that get stored.

Format:

Field	Bit	Description
Memory_Save	[0]	1 = Current status and modes are saved to MEM_SAVE_CH (Self cleared)
	[1-31]	Reserved.

2.9.8. ONE_SHOT / MULTI_SHOT: 61Ch

This register allows the user to control single and multi-shot functionality of the camera. During ISO_EN = 1 or *One_Shot* = 1 or *Multi_Shot* =1, the register value which reflects the Isochronous packet format cannot change. Data transfer control priority is ISO_EN > One_Shot > Multi_Shot.

Format:

Field	Bit	Description
One_Shot	[0]	1 = only one frame of video data is transmitted. (Self cleared after transmission) Ignored if ISO_EN = 1
Multi_Shot	[1]	1 = N frames of video data is transmitted. (Self cleared after transmission) Ignored if ISO_EN = 1 or One_Shot =1
	[2-15]	Reserved.
Count_Number	[16-31]	Count number for Multi-shot function.

2.9.9. MEM_SAVE_CH: 620h

This register allows the user to specify the memory channel number to be used by the MEMORY_SAVE command.

The camera will initialize itself at power-up, or when explicitly reinitialized, using the contents of the last saved memory channel.

Attempting to save user settings to the (read-only) factory defaults channel will cause the camera to switch back to using the factory defaults during initialization.

Format:

Field	Bit	Description
Mem_Save_Ch	[0-3]	Write channel for Memory_Save command. Shall be >=0001 (0 is for factory default settings) See BASIC_FUNC_INQ register.
	[4-31]	Reserved.

2.9.10. CUR_MEM_CH: 624h

This register allows the user to load the camera settings configuration stored in the specified memory channel, and reports the current memory channel being used.

Format:

Field	Bit	Description
Cur_Mem_Ch	[0-3]	Write: Loads the camera status, modes and values from the specified memory channel. Read: The current memory channel number.
	[4-31]	Reserved.

2.9.11. VMODE_ERROR_STATUS: 628h

This register is used by the camera to report any camera configuration errors. If an error has occurred, no image data will be sent by the camera.

Format:

Field	Bit	Description
Vmode_Error_Status	[0]	Error status of combination of video format, mode, frame rate and ISO_SPEED setting. 0: no error 1: error This flag will be updated every time one of the above settings is changed by writing a new value.
	[1-31]	Reserved.

2.9.12. SOFTWARE_TRIGGER: 62Ch (v1.31)

This register allows the user to generate a software asynchronous trigger.

Format:

Field	Bit	Description
Software_Trigger	[0]	Write: 0: Reset software trigger, 1: Set software trigger (This bit automatically resets to 0 in all trigger modes except Trigger_Mode=3) Read: 0: Ready, 1: Busy

Camera Notes:

Camera	Model/Sensor	Firmware	Avail.	Notes
Dragonfly	ALL	2.1.2.14	-	Not implemented. Use SOFT_ASYNC_TRIGGER register 102Ch.

Other Resources:

Type	Description
Software	*AsyncTriggerEx* sample program (PGR FlyCapture SDK)
Documentation	Technical Application Note TAN2004004

2.9.13. DATA_DEPTH: 630h (v1.31)

This register allows the user to query the effective depth of the current image data. The image data format is least significant bit (LSB) and odd bits are filled with zeros.

Format:

Field	Bit	Description
Data_Depth	[0-7]	If read value of Data_Depth is zero, shall ignore this field. Write: Ignored Read: Effective data depth
-	[8-31]	Reserved

2.10. Control and Status Registers for Features

The user can control each feature of the camera through these registers. The controllable items are *Mode* and *Value*.

Mode:
Each CSR has three bits for mode control, ON_OFF, One_Push and A_M_Mode (Auto/Manual mode). Each feature can have four states corresponding to the combination of mode control bits.

Note: Not all features implement all modes.

One_Push	ON_OFF	A_M_Mode	State
X	0	X	**Off state**. Feature will be fixed value state and uncontrollable.
X	1	1	**Auto control state**. Camera controls feature by itself continuously.
0	1	0	**Manual control state**. User can control feature by writing value to the value field.
1 (Self clear)	1	0	**One-Push action**. Camera controls feature by itself only once and returns to the Manual control state with adjusted value.

(X: don't care)

Value:
If the *Presence_Inq* bit of the register is one, the value field is valid and can be used for controlling the feature. The user can write control values to the value field only in the Manual control state. In the other states, the user can only read the value. The camera always has to show the real setting value at the value field if *Presence_Inq* is one.

2.10.1. BRIGHTNESS: 800h

This register allows the user to control the brightness of the image.

Format:

Field	Bit	Description
Presence_Inq	[0]	Presence of this feature 0: N/A, 1: Available
Abs_Control	[1]	Absolute value control 0: Control with the value in the Value field 1: Control with the value in the Absolute value CSR. If this bit = 1, the value in the Value field is read-only.
	[2-4]	Reserved
One_Push	[5]	One push auto mode (controlled automatically by camera only once) Write: 1: Begin to work (self-cleared after operation) Read: 0: Not in operation, 1: In operation If A_M_Mode = 1, this bit is ignored
ON_OFF	[6]	Write: ON or OFF for this feature Read: read a status 0: OFF, 1: ON If this bit = 0, other fields will be read only
A_M_Mode	[7]	Write: set the mode Read: read a current mode 0: Manual, 1: Automatic
	[8-19]	Reserved
Value	[20-31]	Value. A write to this value in 'Auto' mode will be ignored.

Camera Notes:

Camera	Model/Sensor	Firmware	Avail.	Notes
Dragonfly	ALL	2.1.2.14	✓	▪ The *Value* field specifies the black level using 1/16 pixel units supporting a range of black=0 (0) to black=15.94 (255). ▪ This register corresponds to the A/D converter's clamp level register.

Scorpion	SCOR-13FF	1.1.0.13	✓	▪ The brightness CSR value is directly written into the sensor 's DAC_RAW register 0x9. With DAC_VHIGH=0 Ohm and DAC_VLOW=0 Ohm you can vary the analog dark signal from 3.0V (0) to 1.6V (127). There is no fixed formula for this. ▪ Note that the output range of the output amplifier is between 3V and 1.2V. ▪ The offset is applied before the gain so it will be changing when the gain is increased.
Scorpion	SCOR-13SM	0.0.0.33	✓	▪ The brightness CSR value is directly written into the sensor black level control register (0x19)

2.10.2. AUTO_EXPOSURE: 804h

This register allows the user to control the camera system's automatic exposure algorithm. It has three useful states:

State	Description
Off	Control of the exposure is achieved via setting both the SHUTTER and GAIN registers. This mode is achieved by setting the *ON_OFF* field to be 0. An equivalent mode can be achieved by setting the *A_M_Mode* fields in the SHUTTER and GAIN registers to 0 (Manual).
ON Manual Exposure Control	The camera automatically modifies the SHUTTER and GAIN registers to try and match the average image intensity to the value written to the Value field. This mode is achieved by setting the *A_M_Mode* value of the AUTO_EXPOSURE register to 0 (manual) and either/both of the *A_M_Mode* values for the SHUTTER and GAIN registers to 1 (Auto).
ON Auto Exposure Control	The camera modifies the *Value* field in order to produce an image that is visually pleasing. This mode is achieved by setting the *A_M_MODE* for all three of the AUTO_EXPOSURE, SHUTTER and GAIN registers to 1 (Auto). In this mode, the *Value* field reflects the average image intensity.

Auto exposure can only control the exposure when the SHUTTER and/or GAIN registers have their *A_M_Mode* bits set. If only one of the registers is in "auto" mode then the auto exposure controller attempts to control the image intensity using just that one register. If both of these registers are in "auto" mode the auto exposure controller uses a shutter-before-gain heuristic to try and maximize the signal-to-noise ratio by favoring a longer shutter time over a larger gain value.

In absolute mode, an exposure value (EV) of 1 is twice as bright as an EV of 0. A value of 0 can be considered to be "normal exposure". In theoretical terms, this equates to a shutter of 1 second using an f1.0 aperture lens. Normal exposure is where the average intensity of the image is 18% of 1023 (18% grey).

Format:

Field	Bit	Description
Presence_Inq	[0]	Presence of this feature 0: N/A, 1: Available
Abs_Control	[1]	Absolute value control 0: Control with the value in the Value field 1: Control with the value in the Absolute value CSR. If this bit = 1, the value in the Value field is read-only.
	[2-4]	Reserved
One_Push	[5]	One push auto mode (controlled automatically by camera only once) Write: 1: Begin to work (self-cleared after operation) Read: 0: Not in operation, 1: In operation If A_M_Mode = 1, this bit is ignored
ON_OFF		Write: ON or OFF for this feature Read: read a status 0: OFF, 1: ON If this bit = 0, other fields will be read only
A_M_Mode	[7]	Write: set the mode Read: read a current mode 0: Manual, 1: Automatic
	[8-19]	Reserved
Value	[20-31]	Value. A write to this value in ‘Auto’ mode will be ignored.

2.10.3. SHARPNESS: 808h

This register provides a mechanism to control a sharpening filter applied to the image on the camera before it is transmitted to the PC.

Format:
Same definition as BRIGHTNESS.

2.10.4. WHITE_BALANCE: 80Ch

This register controls the relative gain of pixels in the Bayer tiling used in the CCD of a color camera. Control of the register is achieved via the *R_Value* and *B_Value* fields and the *On_Off* bit. Both value fields specify relative gain, with a value that is half the maximum value being a relative gain of zero. This register has two states:

- OFF - the same gain is applied to all pixels in the Bayer tiling.
- ON - the *R_Value* field is applied to the red pixels of the Bayer tiling and the *B_Value* field is applied to the blue pixels of the Bayer tiling.

The following table illustrates the default gain settings for most cameras.

	Red	Green	Blue
Black and White	32	32	32
Color	50	22	50

Note: The BAYER_TILE_GAIN register (offset 1044h) provides an alternate way of setting these gains and allows the setting of both green pixel gains.

Format:

Field	Bit	Description
Presence_Inq	[0]	Presence of this feature 0: N/A, 1: Available
Abs_Control	[1]	Absolute value control 0: Control with value in the Value field 1: Control with value in the associated Abs Value CSR If this bit is 1, then Value is ignored
	[2-4]	Reserved
One_Push	[5]	One push auto mode (controlled automatically by camera only once) Write: 1: Begin to work (self-cleared after operation) Read: 0: Not in operation, 1: In operation If A_M_Mode = 1, this bit is ignored
ON_OFF	[6]	Write: ON or OFF for this feature Read: read a status 0: OFF, 1: ON If this bit = 0, other fields will be read only
A_M_Mode	[7]	Write: Set the mode. Read: read the current mode. 0: Manual, 1: Auto
U_Value / B_Value	[8-19]	Blue Value. A write to this value in ‘Auto’ mode will be ignored.
V_Value / R_Value	[20-31]	Red Value. A write to this value in ‘Auto’ mode will be ignored.

2.10.5. HUE: 810h

This register provides a mechanism to control the Hue component of the images being produced by the camera, given a standard Hue, Saturation, Value (HSV) color space.

Format:
Same definition as BRIGHTNESS.

2.10.6. SATURATION: 814h

This register provides a mechanism to control the Saturation component of the images being produced by the camera, given a standard Hue, Saturation, Value (HSV) color space.

Format:
Same definition as BRIGHTNESS.

2.10.7. GAMMA: 818h

This register provides a mechanism to control the function used to non-linearly map a higher bit depth image produced by the sensor to the requested number of bits. The following function applies to all PGR cameras that implement gamma:

```
y = 255 * pow ( x/z, 1/g)
```

Where:

```
z = pow(2,n) - 1
y = output
x = input
pow(a,b) = a to the power of b
g = Gamma in Absolute value = Gamma in integer value/1024.0
n = # of bits from the analog-to-digital (A/D) converter
```

Format:
Same definition as BRIGHTNESS.

2.10.8. SHUTTER: 81Ch

This register provides a mechanism to control the integration time. Control of the register is via the *Value* field and the *Abs_Control* and *A_M_Mode* bits (*ON_OFF* is always set). This register has three states:

State	Description:
Manual/Abs	The shutter value is set by the user via the Abs_Shutter register. The *Value* field becomes read only and reflects the converted value of the Abs_Shutter register.
Manual	The user sets the shutter value via the *Value* field - the Abs_Shutter register becomes read only and contains the current shutter time.
Auto	The shutter value is set by the auto exposure controller (if enabled). Both the *Value* field and the Abs_Shutter register become read only.

See the *Gain and Shutter Settings* section (where applicable) of your camera's *Technical Reference Manual* for conversion of values to real-world units.

Note that the shutter times are scaled by the divider of the basic frame rate. For example, dividing the frame rate by two (e.g. 15fps to 7.5fps) causes the maximum shutter time to double (e.g. 33ms to 66ms).

Format:

Field	Bit	Description
Presence_Inq	[0]	Presence of this feature 0: N/A, 1: Available
Abs_Control	[1]	Absolute value control 0: Control with the value in the Value field 1: Control with the value in the Absolute value CSR. If this bit = 1, the value in the Value field is ignored.
	[2-4]	Reserved
One_Push	[5]	One push auto mode (controlled automatically by camera only once) Write: 1: Begin to work (self-cleared after operation) Read: 0: Not in operation, 1: In operation If A_M_Mode = 1, this bit is ignored

ON_OFF	[6]	Write: ON or OFF for this feature Read: read a status 0: OFF, 1: ON If this bit = 0, other fields will be read only
A_M_Mode	[7]	Write: set the mode Read: read a current mode 0: Manual, 1: Automatic
High_Value	[8-19]	Upper 4 bits of the shutter value available only in extended shutter mode (outside of specification).
Value	[20-31]	Value. A write to this value in 'Auto' mode will be ignored.

Other Resources:

Type	Description
KB Article	Article 202 - Using Absolute Value registers
KB Article	Article 16 - Calculating Dragonfly gain and shutter settings

2.10.9. GAIN: 820h

This register controls the gain of the A/D converter. Control of the register is via the *Value* field and the *Abs_Control* and *A_M_Mode* bits (*ON_OFF* is always set). This register has three states:

State	Description
Manual/Abs	The gain value is set by the user via the Abs_Gain register: the *Value* field becomes read only and reflects the converted absolute value.
Manual	The gain value is set by the user via the *Value* field: the Abs_Gain register becomes read only and contains the current gain.
Auto	The gain value is set by the auto exposure controller (if enabled): both the *Value* field and the Abs_Gain register become read only.

See *Gain and Shutter Settings* section (where applicable) of your camera's *Technical Reference Manual* for conversion of values to real-world units.

Format:

Field	Bit	Description
Presence_Inq	[0]	Presence of this feature 0: N/A, 1: Available
Abs_Control	[1]	Absolute value control 0: Control with the value in the Value field 1: Control with the value in the Absolute value CSR. If this bit = 1, the value in the Value field is ignored.
	[2-4]	Reserved
One_Push	[5]	One push auto mode (controlled automatically by camera only once) Write: 1: Begin to work (self-cleared after operation) Read: 0: Not in operation, 1: In operation If A_M_Mode = 1, this bit is ignored
ON_OFF	[6]	Write: ON or OFF for this feature Read: read a status 0: OFF, 1: ON If this bit = 0, other fields will be read only

A_M_Mode	[7]	Write: set the mode Read: read a current mode 0: Manual, 1: Automatic
	[8-19]	Reserved
Value	[20-31]	Value. A write to this value in 'Auto' mode will be ignored.

Camera Notes:

Camera	Model/Sensor	Firmware	Avail.	Notes
Scorpion	SCOR-13SM	0.0.0.33	✓	▪ Auto and One_Push implemented ▪ Values come from the Gain CSR, which map to the Symagery Gain Configuration Register (register 0x04) in the following way 0 => 0x02 9 => 0x15 1 => 0x03 10 => 0x3B 2 => 0x04 11 => 0x35 3 => 0x05 12 => 0x36 4 => 0x06 13 => 0x37 5 => 0x07 14 => 0x3D 6 => 0x0E 15 => 0x3E 7 => 0x14 16 => 0x3F 8 => 0x1B

Other Resources:

Type	Description
KB Article	Article 142 - Method for determining signal-to-noise ratio (SNR)
KB Article	Article 81 - Controlling the white balance for all four pixels
KB Article	Article 16 - Calculating Dragonfly gain and shutter settings

2.10.10. IRIS: 824h

This register provides a mechanism to control the iris on cameras that support lenses with an automatic or motorized aperture.

Format:
Same definition as BRIGHTNESS.

2.10.11. FOCUS: 828h

This register provides a mechanism to control the focus on cameras that support lenses with an automatic or motorized focus.

Format:
Same definition as BRIGHTNESS.

2.10.12. TEMPERATURE: 82Ch

Allows the user to get the temperature of the camera board-level components. For cameras housed in a case, it is the ambient temperature within the case. The *Value* is in kelvins (0°C = 273.15K) and are in one-tenths (0.1) of a kelvin.

Format:

Field	Bit	Description
Presence_Inq	[0]	Presence of this feature 0: N/A, 1: Available
Abs_Control	[1]	Absolute value control 0: Control with the value in the Value field 1: Control with the value in the Absolute value CSR. If this bit = 1, the value in the Value field is read-only.
	[2-4]	Reserved
One_Push	[5]	One push auto mode (controlled automatically by camera only once) Write: 1: Begin to work (self-cleared after operation) Read: 0: Not in operation, 1: In operation If A_M_Mode = 1, this bit is ignored
ON_OFF	[6]	Write: ON or OFF for this feature Read: read a status 0: OFF, 1: ON If this bit = 0, other fields will be read only
A_M_Mode	[7]	Read: read a current mode 0: Manual, 1: Automatic
	[8-19]	Reserved
Value	[20-31]	Value. A write to this value in 'Auto' mode will be ignored.

2.10.13. TRIGGER_MODE: 830h

This register controls the trigger mode. Control of the register is via the *On_Off* bit and the *Trigger_Mode* and *Parameter* fields.

For cameras using the PGR-Specific GPIO Modes (see section 4.1: *PGR-Specific GPIO Modes*), the *Trigger_Polarity* bit is used to invert the polarity of ***all*** trigger signals. Polarities generally default to active low. Writing a 1 to this bit would therefore set all trigger polarities to be active high. For cameras using the DCAM v1.31 trigger functionality (see section 4.2: *GPIO Control Using DCAM v1.31 PIO* / Strobe), the *Trigger_Polarity* bit controls the polarity of the current *Trigger_Source*. *Trigger_Polarity* does not affect the trigger pin polarity of DCAM v1.31-compliant cameras that are using GPIO_MODE_2.

The *Trigger_Source* bit is used to select which GPIO pin will be used for external trigger purposes when using the DCAM v1.31 trigger functionality. For more information, consult section 4.2: *GPIO Control Using DCAM v1.31 PIO* / Strobe.

The *Trigger_Value* bit is used to determine the current raw signal value on the pin.

The *Trigger_Mode* bit is used to set the trigger mode to be used. To determine the trigger modes supported by an individual camera, query the TRIGGER_INQ register 530h (see the *Inquiry*

Registers for Feature Elements section). For individual trigger mode descriptions, see the *Trigger Modes* section).

The *Trigger_Queue* field in the GPIO_XTRA register 1104h can be used to control how an external trigger signal that is sent during integration (between shutter open and close) is handled: queued (stored to immediately trigger the next frame) or dropped. Refer to this register to determine if this is implemented for your camera.

Format:

Field	Bit	Description
Presence_Inq	[0]	Presence of this feature 0: N/A, 1: Available
Abs_Control	[1]	Absolute value control 0: Control with the value in the Value field 1: Control with the value in the Absolute value CSR. If this bit = 1, the value in the Value field is read-only.
	[2-5]	Reserved
ON_OFF	[6]	Write: ON or OFF for this feature Read: read a status 0: OFF, 1: ON If this bit = 0, other fields will be read only
Trigger_Polarity	[7]	Select trigger polarity (except for Software_Trigger) 0: Trigger active low, 1: Trigger active high
Trigger_Source (v1.31)	[8-10]	Select trigger source Sets trigger source ID from *Trigger_Source_Inq* field of TRIGGER_INQ register.
Trigger_Value (v1.31)	[11]	Trigger input raw signal value Read only 0: Low, 1: High
	[8-11]	Reserved
Trigger_Mode	[12-15]	Trigger mode (Trigger_Mode_0..15) Sets the trigger mode. Query the *Trigger_Mode_Inq* fields of the TRIGGER_INQ register for available trigger modes.
	[16-19]	Reserved
Parameter	[20-31]	Parameter for trigger function, if required (optional)

Camera Notes:

Camera	Model/Sensor	Firmware	Avail.	Notes
Dragonfly	ALL	2.1.2.14	✓	Does not implement *Trigger_Source* or *Trigger_Value* – implemented through GPIO registers

Other Resources:

Type	Description
Software	*AsyncTriggerEx* sample program (PGR FlyCapture SDK)
Documentation	Technical Application Note TAN2004004

2.10.14. TRIGGER_DELAY: 834h (v1.31)

This register provides control over the time delay between one of the following, depending on the current mode:

1. Asynchronous trigger mode: controls the delay between the trigger event and the start of integration (shutter open).
2. Continuous shot (free-running) mode: controls the synchronization offset of the camera relative to normal synchronization. This is useful for offsetting image acquisition between automatically synchronized cameras. Refer to the camera's *Technical Reference* manual for more information on automatic synchronization.

Format:

Field	Bit	Description
Presence_Inq	[0]	Presence of this feature 0: N/A, 1: Available
Abs_Control	[1]	Absolute value control 0: Control with the value in the Value field 1: Control with the value in the Absolute value CSR. If this bit = 1, the value in the Value field is read-only.
	[2-5]	Reserved
ON_OFF	[6]	Write: ON or OFF for this feature Read: read a status 0: OFF, 1: ON If this bit = 0, other fields will be read only
	[7-19]	Reserved
Value	[20-31]	Value.

Camera Notes:

Camera	Model/Sensor	Firmware	Avail.	Notes
Dragonfly	ALL	2.1.2.14	-	Not implemented. See register SHUTTER_DELAY: 1108h.
DR2	ALL	0.9.0.42	✓	• Delay is in units of a 24.576MHz clock. • Less than 1024 ticks is linear; greater than 1024 ticks is non-linear. • Recommend using register 950h ABS_VAL_TRIGGER_DELAY.
DX		1.1.1.21		
Flea		1.1.0.13		
Flea2		0.0.0.20		
FFMV		0.0.0.11		
BB2		0.9.1.40		
GRAS		0.9.1.28		
BBX3		0.9.1.10		
Scorpion	SCOR-03SO	1.1.0.13	✓	Except Scorpion SCOR-03KD and SCOR-13SM
	SCOR-14SO			
	SCOR-20SO			
	SCOR-13FF			

2.10.15. FRAME_RATE: 83Ch (v1.31)

This register provides control over the frame rate of the camera. The actual frame interval (time between individual image acquisitions) is fixed by the frame rate value. When this feature is ON, exposure time is limited by the frame rate value dynamically. The available frame rate range depends on the current video format and/or video mode.

Format:
Same definition as BRIGHTNESS.

Camera Notes:

Camera	Model/Sensor	Firmware	Avail.	Notes
Dragonfly	ALL	2.1.2.14	-	Not implemented. See FRAME_TIME register 1240h.
ALL	ALL		✓	Turn FRAME_RATE to OFF to enable Extended Shutter mode (except FFMV), or Global Shutter mode for SCOR-13FF.

Other Resources:

Type	Description
Software	*ExtendedShutterEx* sample program (PGR FlyCapture SDK)
KB Article	Article 115 - Key differences between rolling shutter and frame (global) shutter.

2.10.16. PAN: 884h

This register provides a mechanism to horizontally move the current portion of the CCD that is being imaged.

Format:
Same definition as BRIGHTNESS.

Camera Notes:

Camera	Model/Sensor	Firmware	Avail.	Notes
BB2	ALL	0.9.1.40	✓	Controls current sensor being streamed

2.10.17. TILT: 888h

This register provides a mechanism to vertically move the current portion of the CCD that is being imaged.

Format:
Same definition as BRIGHTNESS.

2.11. Absolute Value CSR Registers

Many Point Grey IEEE-1394 cameras implement "absolute" modes for various camera settings that report real-world values, such as Shutter times in seconds (s) and Gain values in decibels (dB). Using the absolute values contained in the following registers is easier and more efficient than applying complex conversion formulas to the information in the *Value* field of the associated Control and Status Register. A relative value does not always translate to the same absolute value. Two properties that can affect this relationship are pixel clock frequency and horizontal line frequency. These properties are, in turn, affected by such properties as resolution, frame rate, region of intererest (ROI) size and position, and packet size. In addition, these conversion formulas can change between firmware versions. Point Grey therefore recommends using the absolute registers to determine camera values.

2.11.1. Inquiry Registers for Absolute Value CSR Offset Addresses

The following set of registers indicates the locations of the absolute value CSR registers that are implemented by PGR IEEE-1394 cameras. These offsets are relative to the 1394 base offset 0xFFFF F0F0 0000.

Offset	Name	Bit	Description
700h	ABS_CSR_HI_INQ_0	[0..31]	Quadlet offset for the absolute value CSR for Brightness.
704h	ABS_CSR_HI_INQ_1	[0..31]	Quadlet offset for the absolute value CSR for Auto Exposure.
708h	ABS_CSR_HI_INQ_2	[0..31]	Quadlet offset for the absolute value CSR for Sharpness.
70Ch	ABS_CSR_HI_INQ_3	[0..31]	Quadlet offset for the absolute value CSR for White Balance.
710h	ABS_CSR_HI_INQ_4	[0..31]	Quadlet offset for the absolute value CSR for Hue.
714h	ABS_CSR_HI_INQ_5	[0..31]	Quadlet offset for the absolute value CSR for Saturation.
718h	ABS_CSR_HI_INQ_6	[0..31]	Quadlet offset for the absolute value CSR for Gamma.
71Ch	ABS_CSR_HI_INQ_7	[0..31]	Quadlet offset for the absolute value CSR for Shutter.
720h	ABS_CSR_HI_INQ_8	[0..31]	Quadlet offset for the absolute value CSR for Gain.
724h	ABS_CSR_HI_INQ_9	[0..31]	Quadlet offset for the absolute value CSR for Iris.
728h	ABS_CSR_HI_INQ_10	[0..31]	Quadlet offset for the absolute value CSR for Focus.
72Ch	ABS_CSR_HI_INQ_11	[0..31]	Quadlet offset for the absolute value CSR for Temperature.
730h	ABS_CSR_HI_INQ_12	[0..31]	Quadlet offset for the absolute value CSR for Trigger.
734h	ABS_CSR_HI_INQ_13	[0..31]	Quadlet offset for the absolute value CSR for Trigger Delay.
73Ch	ABS_CSR_HI_INQ_15	[0..31]	Quadlet offset for the absolute value CSR for Frame Rate.
740h - 77Fh	Reserved		
7C4h	ABS_CSR_LO_INQ_1	[0..31]	Quadlet offset for the absolute value CSR for Pan.
7C8h	ABS_CSR_LO_INQ_2	[0..31]	Quadlet offset for the absolute value CSR for Tilt.

2.11.2. Current Absolute Value Register Offsets

At the time of this revision, the absolute value offsets that would be derived using the quadlet offset information in the *Inquiry Registers for Absolute Value CSR Offset Addresses* section would be as follows:

The following table of absolute value offsets is current as of the revision date. These offsets are subject to change without notice.

Offset	Name	Field	Bit	Description
900h	ABS_VAL_AUTO_EXPOSURE	Min_Value	[0-31]	Min auto exposure value.
904h		Max_Value	[0-31]	Max auto exposure value.
908h		Value	[0-31]	Current auto exposure value.
910h	ABS_VAL_SHUTTER	Min_Value	[0-31]	Min shutter value seconds
914h		Max_Value	[0-31]	Max shutter value seconds
918h		Value	[0-31]	Current shutter value seconds
920h	ABS_VAL_GAIN	Min_Value	[0-31]	Min gain value dB
924h		Max_Value	[0-31]	Max gain value dB
928h		Value	[0-31]	Current gain value dB
930h	ABS_VAL_BRIGHTNESS	Min_Value	[0-31]	Min brightness value %
934h		Max_Value	[0-31]	Max brightness value %
938h		Value	[0-31]	Current brightness value %
940h	ABS_VAL_GAMMA	Min_Value	[0-31]	Min gamma value
944h		Max_Value	[0-31]	Max gamma value
948h		Value	[0-31]	Current gamma value
950h	ABS_VAL_TRIGGER_DELAY	Min_Value	[0-31]	Min delay value seconds
954h		Max_Value	[0-31]	Max delay value seconds
958h		Value	[0-31]	Current delay value seconds
960h	ABS_VAL_FRAME_RATE	Min_Value	[0-31]	Min frame rate FPS
964h		Max_Value	[0-31]	Max frame rate FPS
968h		Value	[0-31]	Current frame rate FPS
970h	ABS_VAL_HUE	Min_Value	[0-31]	Min hue deg
974h		Max_Value	[0-31]	Max hue deg
978h		Value	[0-31]	Current hue deg
980h	ABS_VAL_SATURATION	Min_Value	[0-31]	Min saturation %
984h		Max_Value	[0-31]	Max saturation %
988h		Value	[0-31]	Current saturation %

2.11.3. Absolute Value Register Format

The IIDC DCAM Specification defines the Absolute Value CSRs. Each set of absolute value CSRs consist of three registers (quadlets): a minimum value, a maximum value (both read only) and the current value. The DCAM specification defines the offsets of the Absolute Value CSRs for each of the camera features, as described above.

Offset	Name	Field	Bit	Description
000h	Absolute Value	Min_Value	[0-31]	Minimum value for this feature. Read only.
004h		Max_Value	[0-31]	Maximum value for this feature. Read only.
008h		Value	[0-31]	Current value of this feature.

0-7	8-15	16-23	24-31
Floating-point value with IEEE/REAL*4 format			

Sign(S)	Exponent(exp)	Mantissa(m)
1bit	8bit	23bit

2.11.4. Units of Value for Absolute Value CSR Registers

The following tables describe the real-world units that are used for the absolute value registers. Each value is either Absolute (value is an absolute value) or Relative (value is an absolute value, but the reference is system dependent).

Feature element name	Function	Unit	Unit Description	Reference point	Value Type
Brightness	Black level offset	%		----	Absolute
Auto Exposure	Auto Exposure	EV	exposure value	0	Relative
White_Balance	White Balance	K	kelvin	----	Absolute
Hue	Hue	deg	degree	0	Relative
Saturation	Saturation	%		100	Relative
Shutter	Integration time	s	seconds	----	Absolute
Gain	Circuit gain	dB	decibel	0	Relative
Iris	Iris	F	F number	----	Absolute
Focus	Focus	m	meter	----	Absolute
Trigger	External Trigger	times		----	Absolute
Trigger_Delay	Trigger Delay	S	seconds	----	Absolute
Frame_Rate	Frame rate	fps	frames per second	----	Absolute

2.11.5. Determining Absolute Value Register Values

The Absolute Value CSR's store 32-bit floating-point values with IEEE/REAL*4 format, as described in the *Absolute Value Register Format* section. To determine the minimum, maximum and current values for a property such as shutter[1]:

1. Read the ABS_CSR_HI_INQ_7 register 71Ch to obtain the quadlet offset for the absolute value CSR for shutter:

```
flycaptureGetCameraRegister( context, 0x71C, &ulValue );
```

2. The 32-bit ulValue is a quadlet offset, so multiply by 4 to get the actual offset:

```
ulValue = ulValue * 4; // ulValue == 0x3C0244, actual offset == 0xF00910
```

This offset represents the offset from the 1394 base address 0xFFFF Fxxx xxxx. Since the *PGR FlyCapture API* automatically takes into account the 1394 base offset 0xFFFF F0F0 0000, the actual offset in this example would be 0x910.

[1] Code snippets use function calls included in the PGR FlyCapture SDK

3. Use the offset obtained to read the min, max and current absolute values and convert the 32-bit hexadecimal values to floating point:

```
// declare a union of a floating point and unsigned long
typedef union _AbsValueConversion
{
       unsigned long ulValue;
       float    fValue;
} AbsValueConversion;

float               fMinShutter, fMaxShutter, fCurShutter;
AbsValueConversion  minShutter, maxShutter, curShutter;

// read the 32-bit hex value into the unsigned long member
flycaptureGetCameraRegister( context, 0x910, &minShutter.ulValue );
flycaptureGetCameraRegister( context, 0x914, &maxShutter.ulValue );
flycaptureGetCameraRegister( context, 0x918, &curShutter.ulValue );
fMinShutter =  minShutter.fValue;
fMaxShutter =  maxShutter.fValue;
fCurShutter =  curShutter.fValue;
```

The FlyCapture *API provides function calls to automatically get and set absolute values, e.g. flycaptureGetCameraAbsProperty(), etc. Refer to the* PGR FlyCapture User Manual *for function definitions.*

2.11.6. Setting Absolute Value Register Values

The user must write a 1 to bit [1] of the associated feature CSR order to change the Value field of this register from being read-only. For example, to enable absolute value control of shutter, bit [1] of SHUTTER register 0x81C must be set to 1.

2.12. Video Mode Control and Status Registers for Format_7

These registers provide Format_7, Mode_x information for cameras that implement Format_7 (Partial Image Size Format). Not all registers are implemented for all PGR cameras.

2.12.1. Inquiry Registers for Format_7 CSR Offset Addresses

The following set of registers indicates the locations of the Format_7 Mode_x CSR registers that are implemented by PGR IEEE-1394 cameras. These offsets are relative to the 1394 base offset 0xFFFF F0F0 0000.

Offset	Name	Field	Bit	Description
2E0h	V_CSR_INQ_7_0	Mode_0	[0-31]	CSR quadlet offset for Format_7 Mode_0
2E4h	V_CSR_INQ_7_1	Mode_1	[0-31]	CSR quadlet offset for Format_7 Mode_1
2E8h	V_CSR_INQ_7_2	Mode_2	[0-31]	CSR quadlet offset for Format_7 Mode_2
2ECh	V_CSR_INQ_7_3	Mode_3	[0-31]	CSR quadlet offset for Format_7 Mode_3
2F0h	V_CSR_INQ_7_4	Mode_4	[0-31]	CSR quadlet offset for Format_7 Mode_4
2F4h	V_CSR_INQ_7_5	Mode_5	[0-31]	CSR quadlet offset for Format_7 Mode_5
2F8h	V_CSR_INQ_7_6	Mode_6	[0-31]	CSR quadlet offset for Format_7 Mode_6
2FCh	V_CSR_INQ_7_7	Mode_7	[0-31]	CSR quadlet offset for Format_7 Mode_7

2.12.2. Current Format_7 Register Offsets

At the time of this revision, the actual offsets that would be derived using the quadlet offset information in the *Inquiry Registers for Format_7 CSR Offset Addresses* section would be as follows:

The following table of Format_7 offsets is current as of the revision date. These offsets are subject to change without notice.

Offset Range	Description
A00h – A7Ch	Format_7 Mode_0 register offsets
A80h – AFCh	Format_7 Mode_1 register offsets
B00h – B7Ch	Format_7 Mode_2 register offsets
B80h – BFCh	Format_7 Mode_3 register offsets
C00h – C7Ch	Format_7 Mode_4 register offsets
C80h – CFCh	Format_7 Mode_5 register offsets

For example, to read the contents of the Format_7 Mode_3 BYTE_PER_PACKET register:

4. Read the V_CSR_INQ_7_3 register 2ECh to obtain the quadlet offset for the Format_7 Mode_3 registers:

```
error = flycaptureGetCameraRegister( context, 0x2EC, &ulValue );
printf( “0x%x” );  // 0x003C02E0
```

5. The 32-bit ulValue is a quadlet offset, so multiply by 4 to get the actual offset:

```
ulValue = ulValue * 4; // ulValue * 4 == 0xF00B80
```

   This offset represents the offset from the 1394 base address 0xFFFF Fxxx xxxx. Since the *PGR FlyCapture API* automatically takes into account the 1394 base offset 0xFFFF F0F0 0000, the actual offset in this example would be 0xB80.

```
ulValue = ulValue & 0x000FFFFF; // ulValue == 0xB80
```

6. Add the BYTE_PER_PACKET register offset (0x044) to the base offset for the Format_7 Mode_3 registers (0xB80) calculated in Step 2:

```
ulValue = ulValue + 0x044; // ulValue == 0xBC4
```

7. Use the final offset calculated in Step 3 to determine the current BYTE_PER_PACKET value for Format_7 Mode_3:

```
error = flycaptureGetCameraRegister( context, ulValue, &ulBPPValue );
```

2.12.3. MAX_IMAGE_SIZE_INQ: 000h

This register is an inquiry register for maximum image size.

Format:

Field	Bit	Description
Hmax	[0-15]	Maximum horizontal pixel number
Vmax	[16-31]	Maximum vertical pixel number

2.12.4. UNIT_SIZE_INQ (004h) and UNIT_POSITION_INQ (04Ch)

This register is an inquiry register for unit size.

Hmax = Hunit * n = Hposunit*n3 (n, n3 are integers)
Vmax = Vunit * m = Vposunit*m3 (m, m3 are integers)

If the read value of Hposunit is 0, Hposunit = Hunit for compatibility with DCAM Rev 1.20.
If the read value of Vposunit is 0, Vposunit = Vunit for compatibility with DCAM Rev 1.20.

Format (UNIT_SIZE_INQ: 004h):

Field	Bit	Description
Hunit	[0-15]	Horizontal unit pixel number
Vunit	[16-31]	Vertical unit pixel number

Format (UNIT_POSITION_INQ: 04Ch):

Field	Bit	Description
Hposunit	[0-15]	Horizontal unit pixel number for position If read value of Hposunit is 0, Hposunit = Hunit for compatibility.
Vposunit	[16-31]	Vertical unit number for position If read value of Vposunit is 0, Vposunit = Vunit for compatibility.

2.12.5. IMAGE_POSITION (008h) and IMAGE_SIZE (00Ch)

These registers determine an area of required data. All the data must be as follows:

Left = Hposunit * n1
Top = Vposunit * m1
Width = Hunit * n2
Height = Vunit * m2 (n1, n2, m1, m2 are integers)
Left + Width <= Hmax
Top + Height <= Vmax

Format (IMAGE_POSITION: 008h):

Field	Bit	Description
Left	[0-15]	Left position of requested image region (pixels)
Top	[16-31]	Top position of requested image region (pixels)

Format (IMAGE_SIZE: 00Ch):

Field	Bit	Description
Width	[0-15]	Width of requested image region (pixels)
Height	[16-31]	Height of requested image region (pixels)

2.12.6. COLOR_CODING_ID (010h) and COLOR_CODING_INQ (014h)

The COLOR_CODING_INQ register describes available the color-coding capability of the system. Each coding scheme has its own ID number. The required color-coding scheme must be set to COLOR_CODING_ID register as the ID number.

Format (COLOR_CODING_ID: 010h):

Field	Bit	Description
Coding_ID	[0-7]	Color coding ID from COLOR_CODING_INQ register
	[8-31]	Reserved (all zero)

Format (COLOR_CODING_INQ: 014h):

Field	Bit	Description	ID
Mono8	[0]	Y only. Y=8bits, non compressed	0
4:1:1 YUV8	[1]	4:1:1, Y=U=V= 8bits, non compressed	1
4:2:2 YUV8	[2]	4:2:2, Y=U=V=8bits, non compressed	2
4:4:4 YUV8	[3]	4:4:4, Y=U=V=8bits, non compressed	3
RGB8	[4]	R=G=B=8bits, non compressed	4
Mono16	[5]	Y only, Y=16bits, non compressed	5
RGB16	[6]	R=G=B=16bits, non compressed	6
Signed Mono16	[7]	Y only, Y=16 bits, non compressed (signed integer)	7
Signed RGB16	[8]	R=G=B=16 bits, non compressed (signed integer)	8
Raw8	[9]	Raw data output of color filter sensor, 8 bits	9
Raw16	[10]	Raw data output of color filter sensor, 16 bits	10
	[11-31]	Reserved (all zero)	11-31

2.12.7. PIXEL_NUMBER_INQ (034h), TOTAL_BYTES_HI_INQ (038h), and TOTAL_BYTES_LO_INQ (03Ch)

The PIXEL_NUMBER_INQ register includes the total number of pixels in the required image area. The TOTAL_BYTE_INQ register includes the total number of bytes in the required image area.

If the *Presence* bit in the VALUE_SETTING register is zero, the values of these registers will be updated by writing the new value to the IMAGE_POSITION, IMAGE_SIZE and COLOR_CODING_ID registers.

If the *Presence* bit in the VALUE_SETTING register is one, the values of these registers will be updated by writing one to the *Setting_1* bit in the VALUE_SETTING register. If the *ErrorFlag_1* bit is zero after the *Setting_1* bit returns to zero, the values of these registers are valid.

Format (PIXEL_NUMBER_INQ: 034h):

Field	Bit	Description
PixelPerFrame	[0-31]	Pixel number per frame

Format (TOTAL_BYTES_HI_INQ: 038h):

Field	Bit	Description
BytesPerFrameHi	[0-31]	Higher quadlet of total bytes of image data per frame

Format (TOTAL_BYTES_LO_INQ: 03Ch):

Field	Bit	Description
BytesPerFrameLo	[0-31]	Lower quadlet of total bytes of image data per frame

2.12.8. PACKET_PARA_INQ (040h) and BYTE_PER_PACKET (044h)

MaxBytePerPacket describes the maximum packet size for one isochronous packet.
UnitBytePerPacket is the unit for isochronous packet size.
RecBytePerPacket describes the recommended packet size for one isochronous packet. If *RecBytePerPacket* is zero, you must ignore this field.

If the *Presence* bit in the VALUE_SETTING register is zero, values of these fields will be updated by writing the new value to the IMAGE_POSITION, IMAGE_SIZE and COLOR_CODING_ID registers with the value of the ISO_Speed register (60Ch [6..7]).

First, the ISO_Speed register must be written. Then the IMAGE_POSITION, IMAGE_SIZE and COLOR_CODING_ID registers should be updated.

If the *Presence* bit in the VALUE_SETTING register is one, the values of these fields will be updated by writing one to the *Setting_1* bit in the VALUE_SETTING register. If the *ErrorFlag_1* bit is zero after the *Setting_1* bit returns to zero, the values of these fields are valid.

The *BytePerPacket* value determines the real packet size and transmission speed for one frame image. The *BytePerPacket* value must keep the following condition.

BytePerPacket = UnitBytePerPacket * n (n is an integer)
BytePerPacket <= MaxBytePerPacket

Format (PACKET_PARA_INQ: 040h):

Field	Bit	Description
UnitBytePerPacket	[0-15]	Minimum bytes per packet
MaxBytePerPacket	[16-31]	Maximum bytes per packet

Format (BYTE_PER_PACKET: 044h):

Field	Bit	Description
BytePerPacket	[0-15]	Packet size
RecBytePerPacket	[16-31]	Recommended bytes per packet. If this value is zero, must ignore this field.

2.12.9. PACKET_PER_FRAME_INQ: 048h

If *BytePerPacket* * n != *BytePerFrame* (n is an integer), you must use padding. The *PacketPerFrame* value is the number of packets per one frame. This register will be updated after *BytePerPacket* is written.

The total number of bytes of transmission data per one frame = *BytePerPacket* * *PacketPerFrame*.

The number of bytes of padding = *BytePerPacket* * *PacketPerFrame* – *BytePerFrame*. The receiver must ignore the above padding data in the last packet of each frame.

Format:

Field	Bit	Description
PacketPerFrame	[0-31]	Number of packets per frame

2.12.10. FRAME_INTERVAL_INQ: 050h

This register describes the frame interval based on the current camera conditions, including exposure time. The reciprocal value of this (1 / FrameInterval) is the frame rate of the camera. If the value of this register is zero, the camera can't report this value and it should be ignored. FrameInterval is in seconds and reported in IEEE1394/REAL*4 floating-point format (see section 2.12.5: *Determining Absolute Value Register Values*).

Format:

Field	Bit	Description
FrameInterval	[0-31]	Current frame interval (seconds) (IEEE/REAL*4 floating-point value) If read value of FrameInterval is zero, ignore this field.

2.12.11. VALUE_SETTING: 07Ch

The purpose of the *Setting_1* bit is for updating the TOTAL_BYTES_HI_INQ, TOTAL_BYTES_LO_INQ, PACKET_PARA_INQ and BYTE_PER_PACKET registers. If one of the values in the IMAGE_POSITION, IMAGE_SIZE, COLOR_CODING_ID and ISO_Speed registers is changed, the *Setting_1* bit must be set to 1. The *ErrorFlag_1* field will be updated when the *Setting_1* bit returns to 0. If the *ErrorFlag_1* field is zero, the values of the TOTAL_BYTES_HI_INQ, TOTAL_BYTES_LO_INQ, PACKET_PARA_INQ and BYTE_PER_PACKET registers are valid.

After the *BytePerPacket* value is written, the *ErrorFlag_2* field will be updated. If the *ErrorFlag_2* field is zero, isochronous transmission can be started without any problem.

Format:

Field	Bit	Description
Presence	[0]	If this bit is one, *Setting_1* , *ErrorFlag_1* and *ErrorFlag_2* fields are valid. This bit is read only.
Setting_1	[1]	If writing "1" to this bit, IMAGE_POSITION, IMAGE_SIZE, COLOR_CODING_ID and ISO_Speed register value will be reflected in PIXEL_NUMBER_INQ, TOTAL_BYTES_HI_INQ, TOTAL_BYTES_LO_INQ, PACKET_PARA_INQ and BYTE_PER_PACKET registers. This bit is self-cleared.
	[2-7]	Reserved
ErrorFlag_1	[8]	Combination of the values of IMAGE_POSITION, IMAGE_SIZE, COLOR_CODING_ID and ISO_Speed register is not acceptable. 0: no error, 1: error This flag will be updated every time when *Setting_1* bit returns to "0" from "1".
ErrorFlag_2	[9]	*BytePerPacket* value is not acceptable. 0: no error, 1: error
	[10-31]	Reserved

2.13. Advanced Registers

The following set of registers are specific to PGR IEEE-1394 cameras, and are outside of the DCAM specification.

2.13.1. ACCESS_CONTROL_REGISTERS: 1000h – 100Ch

According to the DCAM specification, these registers must be configured properly before access to the advanced registers is granted. This requirement is not enforced on the camera but the registers' formats are here for completeness.

Offset	Name	Field	Bit	Description
1000h	ACCESS_CONTROL_HI	Feature_ID_Hi	[0-31]	
1004h	ACCESS_CONTROL_LO	Feature_ID_Lo	[0-15]	
			[16-19]	Reserved
		Time_Out	[20-31]	Milliseconds until time out (max 4.095s)
1008h-100Ch	FEATURE_ID	Company_ID	[0-23]	00B09D
		Adv_Feature_Set	[24-47]	Advanced Feature set unique value (currently 000004)

Feature Availability:

Camera	Model/Sensor	Firmware	Avail.	Notes
ALL	ALL		✓	These registers are supported on all PGR IEEE-1394 DCAM cameras

2.13.2. EXTENDED_SHUTTER: 1028h

Allows the user to access a number of different extended shutter modes. Placing the camera into extended shutter mode removes the restriction that the shutter integration time must be less than the frame rate. The actual frame rate will be the maximum of the nominal frame rate and the shutter time.

DRAGONFLY ONLY: The maximum shutter values for the various modes are as follows:

Frame Rate	Maximum Shutter Value
30Hz	532 * 1/16000sec.
32Hz	500 * 1/16000sec.
Extended shutter	4000 * 1/16000sec.
50Hz	256 * 1/12800sec.
24Hz	666 * 1/16000sec.

Format:

Field	Bit	Description
Presence_Inq	[0]	Presence of this feature 0: N/A 1: Available
	[1-12]	Reserved
Shutter_Mode	[13-15]	0: 30Hz (default) 1: 32Hz 2: extended shutter 3: 50Hz 4: 24Hz
	[16-31]	Reserved.

Feature Availability:

Camera	Model/Sensor	Firmware	Avail.	Notes
ALL	ALL		-	Not implemented (except Dragonfly). Turn FRAME_RATE register OFF (where applicable) to enable extended shutter.

Other Resources:

Type	Description
Software	*ExtendedShutterEx* sample program (PGR FlyCapture SDK)

2.13.3. SOFT_ASYNC_TRIGGER: 102Ch

Provides a software method for generating an asynchronous trigger event. When the camera is in Trigger_Mode_0, writing a zero to bit 31 of this register will generate an asynchronous trigger.

Format:

Field	Bit	Description
Presence_Inq	[0]	Presence of this feature. 0: N/A, 1: Available
	[1-29]	Reserved.
Trigger	[30-31]	Write: 0: generate trigger Read: 0: camera is not ready to be triggered; integration is complete but camera is transferring image data 1: camera is ready to be triggered 2: camera is in the middle of integration

Feature Availability:

Camera	Model/Sensor	Firmware	Avail.	Notes
Dragonfly	ALL	2.1.2.14	✓	Does not implement *Trigger* field status mode 2 (middle of integration)
ALL	ALL		✓	Deprecated. Recommend using SOFTWARE_TRIGGER register 62Ch. Not implemented on Scorpion SCOR-03KD.

Other Resources:

Type	Description

Software	*AsyncTriggerEx* sample program (PGR FlyCapture SDK)
KB Article	Article 169 - Time between software asynchronous trigger and start of integration.

2.13.4. BAYER_TILE_MAPPING: 1040h

This 32 bit read only register specifies the sense of the cameras' Bayer tiling. Various colors are indicated by the ASCII representation of the first letter of their name.

Color	ASCII
Red (R)	52h
Green (G)	47h
Blue (B)	42h
Monochrome (Y)	59h

For example, 0x52474742 is RGGB and 0x59595959 is YYYY.

On color cameras that support on-board color processing, the camera reports YYYY tiling when operating in any non-raw Bayer data format. For more information, consult the Color and Greyscale Conversion section of your camera's Technical Reference Manual.

Format:

Field	Bit	Description
Bayer_Sense_A	[0-7]	ASCII representation of the first letter of the color of pixel (0,0) in the Bayer tile.
Bayer_Sense_B	[8-15]	ASCII representation of the first letter of the color of pixel (0,1) in the Bayer tile.
Bayer_Sense _C	[16-24]	ASCII representation of the first letter of the color of pixel (1,0) in the Bayer tile.
Bayer_Sense _D	[25-31]	ASCII representation of the first letter of the color of pixel (1,1) in the Bayer tile.

Feature Availability:

Camera	Model/Sensor	Firmware	Avail.	Notes
ALL	ALL		✓	Read only (except Dragonfly)

2.13.5. BAYER_TILE_GAIN: 1044h

Allows the user to specify all four Bayer tile pixel gains. The ordering matches that of the BAYER_TILE_MAPPING register (offset 1040h) and the units match those of the WHITE_BALANCE register (offset 80Ch).

Any write to this register will set the *On_Off* bit of the WHITE_BALANCE register.

Format:

Field	Bit	Description

Bayer_Gain_A	[0-7]	Gain for pixel (0,0) in the Bayer tile.
Bayer_Gain_B	[8-15]	Gain for pixel (0,1) in the Bayer tile.
Bayer_Gain_C	[16-24]	Gain for pixel (1,0) in the Bayer tile.
Bayer_Gain_D	[25-31]	Gain for pixel (1,1) in the Bayer tile.

Feature Availability:

Camera	Model/Sensor	Firmware	Avail.	Notes
Dragonfly	ALL	2.1.2.14	✓	Implemented on Dragonfly only.

2.13.6. IMAGE_DATA_FORMAT: 1048h

This register allows the user to specify various image data format parameters.

Mirror_Image_Ctrl allows the user to toggle between normal and mirror (horizontally flipped) image modes.

Bayer_Mono_Ctrl allows the user to control whether non-Format_7 Y8 or Y16 monochrome modes on a color camera will output monochrome (greyscale) or raw Bayer data.

> *Selecting a half-width, half-height image size and monochrome pixel format, such as 800x600 Y8, using non-Format_7 modes provides a monochrome binned image. In some cases, enabling raw Bayer output in mono mode provides a raw Bayer region of interest of 800x600, centered within the larger pixel array. This has an effect on the field of view.*

Y16_Data_Format controls the endianness of Y16 images – either IIDC 1394 DCAM-compliant mode (default) or PGR-specific (Intel-compatible) mode – as described below.

IIDC 1394 DCAM Y16 mode:

Description	Data Format	
Actual bit depth: Dependent on A/D converter Bit alignment: MSB Byte alignment: Big-endian	0-7	8-15
	98765432	10xxxxxx

PGR-specific Y16 mode:

Description	Data Format	
Actual bit depth: Dependent on A/D converter Bit alignment: MSB Byte alignment: Little-endian	0-7	8-15
	10xxxxxx	98765432

Format:

Field	Bit	Description
Presence_Inq	[0]	Presence of this feature. 0: N/A, 1: Available
	[1-22]	Reserved.

Mirror_Image_Ctrl	[23]	Value 0: Disable horizontal (mirror) image flip 1: Enable horizontal (mirror) image flip
Bayer_Mono_Ctrl	[24]	Value 0: Disable raw bayer output in non-Format_7 mono modes 1: Enable raw bayer output in non-Format_7 mono modes
	[25-30]	Reserved.
Y16_Data_Format	[31]	Value 0: PGR-specific mode 1: DCAM-compliant mode (default)

2.13.7. TEST_PATTERN: 104Ch

This register allows the user to enable or disable the test pattern image.

Format:

Field	Bit	Description
Presence_Inq	[0]	Presence of this feature. 0: N/A, 1: Available
	[1-30]	Reserved.
Test_Pattern_2	[30]	Value 0: Disable test pattern 1: Enable test pattern
Test_Pattern_1	[31]	Value 0: Disable test pattern 1: Enable test pattern

2.13.8. AUTO_EXPOSURE_RANGE: 1088h

Specifies the range of allowed exposure values to be used by the automatic exposure controller when in auto mode.

Format:

Field	Bit	Description
Presence_Inq	[0]	Presence of this feature 0: N/A 1: Available
	[1-7]	Reserved
Min_Value	[8-19]	Lower bound
Max_Value	[20-31]	Upper bound

2.13.9. AUTO_SHUTTER_RANGE: 1098h

Allows the user to specify the range of shutter values to be used by the automatic exposure controller - generally some subset of the entire shutter range described by register 51Ch. This is useful in cases where users wish to limit the minimum and/or maximum shutter speed of the camera when it is running in auto exposure mode.

Format:

Field	Bit	Description

Presence_Inq	[0]	Presence of this feature 0: N/A 1: Available
	[1-5]	Reserved
Min_Dark_Noise	[6]	Minimizes dark current noise with extended shutter times. This feature is currently experimental. 0: Disable dark noise minimization 1: Enable dark noise minimization
	[7]	Reserved
Min_Value	[8-19]	Lower bound
Max_Value	[20-31]	Upper bound

Note: The actual range used is further restricted to match the current grab mode (see Shutter register [offset 81Ch] for the list of ranges).

Note: Although 0xFFA0 is the maximum shutter setting in extended shutter mode, 0xFA0 is the maximum shutter setting for the AUTO_SHUTTER_RANGE.

Camera Notes:

Camera	Model/Sensor	Firmware	Avail.	Notes
Scorpion	SCOR-20SO	1.1.0.14	✓	Implements *Min_Dark_Noise* • Only in non-triggered modes • Applicable shutter times are currently undefined

2.13.10. AUTO_GAIN_RANGE: 10A0h

Allows the user to specify the range of gain values to be used by the automatic exposure controller - generally some subset of the entire gain range described by register 520h. This is useful in cases where users wish to limit the minimum and/or maximum gain of the camera when it is running in auto exposure mode.

Format:

Field	Bit	Description
Presence_Inq	[0]	Presence of this feature 0: N/A 1: Available
	[1-5]	Reserved
ON_OFF	[6]	Write: ON or OFF for this feature Read: read a status 0: OFF 1: ON If this bit = 0, other fields will be read only Controls auto white balance gain boost.
	[7]	Reserved
Min_Value	[8-19]	Lower bound
Max_Value	[20-31]	Upper bound

2.13.11. GPIO_CONTROL: 1100h

Provides status information about the camera's general-purpose I/O pins.

0: Voltage low, 1: Voltage high

> *Opto-isolated input pins with pull-up resistors report a value of '1' when unconnected. Consult your camera's technical reference manual for GPIO pinout details.*

Format:

Field	Bit	Description
Presence_Inq	[0]	Presence of this feature 0: N/A 1: Available
Pin_Count	[12-15]	Number of available GPIO pins
	[16-28]	Reserved
Value_3	[28]	Value of IO3
Value_2	[29]	Value of IO2
Value_1	[30]	Value of IO1
Value_0	[31]	Value of IO0

2.13.12. GPIO_XTRA: 1104h

The GPIO_XTRA register has three main functions:

1. *Strobe_Start*: Controls when the strobe starts: relative to the start of integration (default) or relative to the time of an asynchronous trigger.
2. *Trigger_Queue*: Control how an external trigger signal that is sent during integration (between shutter open and close) is handled: queued (stored to immediately trigger the next frame) or dropped.
3. *Strobe_Divider* (***Dragonfly only***): This acts on three different components:
    a. Strobe delay (set in GPIO_XTRA_PIN_x register, *Mode_Specific_1* field)
    b. Strobe duration (set in GPIO_XTRA_PIN_x register, *Mode_Specific_2* field)
    c. Shutter delay (set in SHUTTER_DELAY register, *Shutter_Delay* field)

    This allows the strobe signal delay/duration and shutter delay to be extended.

> *The Strobe_Divider is only for use by the* Dragonfly *only. Other cameras have access to the full strobe delay/duration range using the* GPIO_XTRA_PIN_x *registers only.*
>
> *The strobe can be extended beyond the 65,535 ticks of the 49.152MHz clock allowable in the GPIO_XTRA_PIN / SHUTTER_DELAY registers, according to the following formula:*
>
> New_duration_or_delay = 16-bit_field_value * (Strobe_Divider + 1)
>
> *For example, to extend the strobe from 1.33ms (*Mode_Specific_2 = *FFFFh) to 21.20ms, enter F in the* Strobe_ Divider *field.*

Format:

Field	Bit	Description
Strobe_Start	[0]	Current Mode 0: Strobe start is relative to start of integration 1: Strobe start is relative to external trigger
Trigger_Queue	[1]	Current Mode 0: Trigger sent during integration is queued 1: Trigger sent during integration is dropped
	[2-23]	Reserved
Strobe_Divider	[24-31]	

Feature Availability:

Camera	Model/Sensor	Firmware	Avail.	Notes
CMLN	ALL	0.9.2.5	✓	
Dragonfly	ALL	2.1.2.14	✓	
DR2	ALL	0.9.0.42	✓	▪ *Strobe_Start* defaults to time of trigger when in asynchronous trigger mode ▪ *Strobe_Divider* deprecated. Use GPIO_XTRA_PIN_x only.
DX		1.1.1.21		
Flea		1.1.0.13		
Flea2		0.0.0.20		
FFMV		0.0.0.11		
BB2		0.9.1.40		
GRAS		0.9.1.28		
BBX3		0.9.1.10		
Scorpion	SCOR-03SO	1.1.0.13		
	SCOR-14SO			
	SCOR-20SO			
	SCOR-13FF			
Scorpion	SCOR-03KD	0.0.1.48	-	Not implemented

2.13.13. SHUTTER_DELAY: 1108h

This register provides control over the time delay between an external trigger and the start of integration (shutter open).

Format:

Field	Bit	Description
	[0-15]	Reserved
Shutter_Delay	[16-31]	Delay before the start of integration.

Feature Availability:

Camera	Model/Sensor	Firmware	Avail.	Notes
Dragonfly	ALL	2.1.2.14	✓	Implemented on Dragonfly only. Delay is in ticks of a 49.152MHz clock. To extend the duration of this delay, use the *Strobe_Multiplier* defined in the GPIO_XTRA register. For other cameras, use TRIGGER_DELAY register.

2.13.14. GPIO_STRPAT_CTRL: 110Ch

This register provides control over a shared 4-bit counter with programmable period. When the *Current_Count* equals N a GPIO pin will only output a strobe pulse if bit[N] of the GPIO_STRPAT_MASK_PIN_x register's *Enable_Pin* field is set to '1'.

Please refer to *Technical Application Note: TAN2005003* for a full description of the strobe pattern functionality.

Field	Bit	Description
Presence_Inq	[0]	Presence of this feature 0: N/A 1: Available
	[1-18]	Reserved
Count_Period	[19-23]	Controls the period of the strobe pattern Valid values: 1..16
	[24-27]	Reserved
Current_Count	[28-31]	Read-only The value of the bit index defined in GPIO_x_STRPAT_MASK that will be used during the next image's strobe. *Current_Count* increments at the same time as the strobe start signal occurs.

2.13.15. GPIO_CTRL_PIN_0: 1110h

This register provides control over the first GPIO pin (Pin 0).

Format:

Field	Bit	Description
Presence_Inq	[0]	Presence of this feature 0: N/A 1: Available
	[1-11]	Reserved
Pin_Mode	[12-15]	Current GPIO_Mode 0: Input 1: Output 2: Asynchronous trigger 3: Strobe 4: Pulse width modulation (PWM) 8: Output (DCAM Specification v1.31-compliant cameras only)
Data	[16-31]	Data field GPIO_MODE_0 – bit 31 contains value GPIO_MODE_1 – bit 31 contains value GPIO_MODE_2 – 0: trigger on falling edge, 1: on rising edge GPIO_MODE_3 – 0: High active output, 1: Low active output GPIO_MODE_4 – see the "*PGR Specific GPIO Modes*" section.

2.13.16. GPIO_XTRA_PIN_0: 1114h

This register contains mode specific data for the first GPIO pin (Pin 0).

Format:

Field	Bit	Description
Mode_Specific_1	[0-15]	GPIO_MODE_3: Delay before the start of the pulse GPIO_MODE_4: Low period of PWM pulse (if Pwm_Pol = 0)
Mode_Specific_2	[16-31]	GPIO_MODE_3: Duration of the pulse GPIO_MODE_4: High period of PWM pulse (if Pwm_Pol = 0)

Camera Notes:

Camera	Model/Sensor	Firmware	Avail.	Notes
Dragonfly	ALL	2.1.2.14	✓	Units are ticks of a 49.152MHz clock
ALL	ALL		✓	Units are ticks of a 1.024MHz clock

2.13.17. GPIO_STRPAT_MASK_PIN_0: 1118h

This register defines the actual strobe pattern to be implemented by GPIO0 in conjunction with the *Count_Period* defined in GPIO_STRPAT_CTRL register 110Ch.

For example, if *Count_Period* is set to '3', bits 16-18 of the *Enable_Mask* can be used to define a strobe pattern. An example strobe pattern might be bit 16=0, bit 17=0, and bit 18=1, which will cause a strobe to occur every three frames (when the *Current_Count* is equal to 2).

Format:

Field	Bit	Description
Presence_Inq	[0]	Presence of this feature 0: N/A 1: Available
	[1-15]	Reserved
Enable_Mask	[16-31]	Bit field representing the strobe pattern used in conjunction with *Count_Period* in GPIO_STRPAT_CTRL 0: Do not output a strobe 1: Output a strobe

2.13.18. GPIO_CTRL_PIN_1: 1120h

This register provides control over the second GPIO pin (Pin 1).

Format:

Field	Bit	Description
Presence_Inq	[0]	Presence of this feature 0: N/A 1: Available
	[1-11]	Reserved

Pin_Mode	[12-15]	Current GPIO_Mode 0: Input 1: Output 2: Asynchronous trigger 3: Strobe 4: Pulse width modulation (PWM) 8: Output (DCAM Specification v1.31-compliant cameras only)
Data	[16-31]	Data field GPIO_MODE_0 – bit 31 contains value GPIO_MODE_1 – bit 31 contains value GPIO_MODE_2 – 0: trigger on falling edge, 1: on rising edge GPIO_MODE_3 – 0: High active output, 1: Low active output GPIO_MODE_4 – see the "*PGR Specific GPIO Modes*" section.

2.13.19. GPIO_XTRA_PIN_1: 1124h

This register contains mode specific data for the second GPIO pin (Pin 1).

Format:

Field	Bit	Description
Mode_Specific_1	[0-15]	GPIO_MODE_3: Delay before the start of the pulse GPIO_MODE_4: Low period of PWM pulse (if Pwm_Pol = 0)
Mode_Specific_2	[16-31]	GPIO_MODE_3: Duration of the pulse GPIO_MODE_4: High period of PWM pulse (if Pwm_Pol = 0)

Camera Notes:

Camera	Model/Sensor	Firmware	Avail.	Notes
Dragonfly	ALL	2.1.2.14	✓	Units are ticks of a 49.152MHz clock
ALL	ALL		✓	Units are ticks of a 1.024MHz clock

2.13.20. GPIO_STRPAT_MASK_PIN_1: 1128h

This register defines the actual strobe pattern to be implemented by GPIO1 in conjunction with the *Count_Period* defined in GPIO_STRPAT_CTRL register 110Ch.

For example, if *Count_Period* is set to '3', bits 16-18 of the *Enable_Mask* can be used to define a strobe pattern. An example strobe pattern might be bit 16=0, bit 17=0, and bit 18=1, which will cause a strobe to occur every three frames (when the *Current_Count* is equal to 2).

Format:

Field	Bit	Description
Presence_Inq	[0]	Presence of this feature 0: N/A 1: Available
	[1-15]	Reserved

Enable_Mask	[16-31]	Bit field representing the strobe pattern used in conjunction with *Count_Period* in GPIO_STRPAT_CTRL 0: Do not output a strobe 1: Output a strobe

2.13.21. GPIO_CTRL_PIN_2: 1130h

This register provides control over the third GPIO pin.

Format:

Field	Bit	Description
Presence_Inq	[0]	Presence of this feature 0: N/A 1: Available
	[1-11]	Reserved
Pin_Mode	[12-15]	Current GPIO_Mode 0: Input 1: Output 2: Asynchronous trigger 3: Strobe 4: Pulse width modulation (PWM) 8: Output (DCAM Specification v1.31-compliant cameras only)
Data	[16-31]	Data field GPIO_MODE_0 – bit 31 contains value GPIO_MODE_1 – bit 31 contains value GPIO_MODE_2 – 0: trigger on falling edge, 1: on rising edge GPIO_MODE_3 – 0: High active output, 1: Low active output GPIO_MODE_4 – see the "*PGR Specific GPIO Modes*" section.

2.13.22. GPIO_XTRA_PIN_2: 1134h

This register contains mode specific data for the third GPIO pin.

Format:

Field	Bit	Description
Mode_Specific_1	[0-15]	GPIO_MODE_3: Delay before the start of the pulse GPIO_MODE_4: Low period of PWM pulse (if Pwm_Pol = 0)
Mode_Specific_2	[16-31]	GPIO_MODE_3: Duration of the pulse GPIO_MODE_4: High period of PWM pulse (if Pwm_Pol = 0)

Camera Notes:

Camera	Model/Sensor	Firmware	Avail.	Notes
Dragonfly	ALL	2.1.2.14	✓	Units are ticks of a 49.152MHz clock
ALL	ALL		✓	Units are ticks of a 1.024MHz clock

2.13.23. GPIO_STRPAT_MASK_PIN_2: 1138h

This register defines the actual strobe pattern to be implemented by GPIO2 in conjunction with the *Count_Period* defined in GPIO_STRPAT_CTRL register 110Ch.

For example, if *Count_Period* is set to '3', bits 16-18 of the *Enable_Mask* can be used to define a strobe pattern. An example strobe pattern might be bit 16=0, bit 17=0, and bit 18=1, which will cause a strobe to occur every three frames (when the *Current_Count* is equal to 2).

Format:

Field	Bit	Description
Presence_Inq	[0]	Presence of this feature 0: N/A 1: Available
	[1-15]	Reserved
Enable_Mask	[16-31]	Bit field representing the strobe pattern used in conjunction with *Count_Period* in GPIO_STRPAT_CTRL 0: Do not output a strobe 1: Output a strobe

2.13.24. GPIO_CTRL_PIN_3: 1140h

This register provides control over the fourth GPIO pin.

Format:

Field	Bit	Description
Presence_Inq	[0]	Presence of this feature 0: N/A 1: Available
	[1-11]	Reserved
Pin_Mode	[12-15]	Current GPIO_Mode 0: Input 1: Output 2: Asynchronous trigger 3: Strobe 4: Pulse width modulation (PWM) 8: Output (DCAM Specification v1.31-compliant cameras only)
Data	[16-31]	Data field GPIO_MODE_0 – bit 31 contains value GPIO_MODE_1 – bit 31 contains value GPIO_MODE_2 – 0: trigger on falling edge, 1: on rising edge GPIO_MODE_3 – 0: High active output, 1: Low active output GPIO_MODE_4 – see the "*PGR Specific GPIO Modes*" section.

Camera Notes:

Camera	Model/Sensor	Firmware	Avail.	Notes

Dragonfly	ALL	2.1.2.14	✓	Must be physically implemented to work. See *Technical Reference Manual*. Default: GPIO_MODE_0

2.13.25. GPIO_XTRA_PIN_3: 1144h

This register contains mode specific data for the fourth GPIO pin.

Format:

Field	Bit	Description
Mode_Specific_1	[0-15]	GPIO_MODE_3: Delay before the start of the pulse GPIO_MODE_4: Low period of PWM pulse (if Pwm_Pol = 0)
Mode_Specific_2	[16-31]	GPIO_MODE_3: Duration of the pulse GPIO_MODE_4: High period of PWM pulse (if Pwm_Pol = 0)

Camera Notes:

Camera	Model/Sensor	Firmware	Avail.	Notes
Dragonfly	ALL	2.1.2.14	✓	Units are ticks of a 49.152MHz clock
ALL	ALL		✓	Units are ticks of a 1.024MHz clock

2.13.26. GPIO_STRPAT_MASK_PIN_3: 1148h

This register defines the actual strobe pattern to be implemented by GPIO3 in conjunction with the *Count_Period* defined in GPIO_STRPAT_CTRL register 110Ch.

For example, if *Count_Period* is set to ‘3’, bits 16-18 of the *Enable_Mask* can be used to define a strobe pattern. An example strobe pattern might be bit 16=0, bit 17=0, and bit 18=1, which will cause a strobe to occur every three frames (when the *Current_Count* is equal to 2).

Format:

Field	Bit	Description
Presence_Inq	[0]	Presence of this feature 0: N/A 1: Available
	[1-15]	Reserved
Enable_Mask	[16-31]	Bit field representing the strobe pattern used in conjunction with *Count_Period* in GPIO_STRPAT_CTRL 0: Do not output a strobe 1: Output a strobe

2.13.27. PIO_OUTPUT: 11F0h

This section describes the control and inquiry registers for the PIO_Output functionality specified in the *IIDC 1394-based Digital Camera (DCAM) Specification Version v1.31*. See the section *GPIO Control Using DCAM v1.31 PIO* / Strobe for further information.

Format:

Field	Bit	Description

IO0_Status	[0]	State (voltage level) of the IO0 pin 0: Low, 1: High
IO1_Status	[1]	State (voltage level) of the IO1 pin 0: Low, 1: High
IO2_Status	[2]	State (voltage level) of the IO2 pin 0: Low, 1: High
IO3_Status	[3]	State (voltage level) of the IO3 pin 0: Low, 1: High
	[4-31]	Reserved

Feature Availability:

Camera	Model/Sensor	Firmware	Avail.	Notes
CMLN	ALL	0.9.2.5	✓	Except Scorpion SCOR-03KD and SCOR-13SM.
DR2	ALL	0.9.0.42	✓	
DX		1.1.1.21		
Flea		1.1.0.13		
Flea2		0.0.0.20		
FFMV		0.0.0.11		
BB2		0.9.1.40		
GRAS		0.9.1.28		
BBX3		0.9.1.10		
Scorpion		1.1.0.13		

2.13.28. PIO_INPUT: 11F4h

This section describes the control and inquiry registers for the PIO_Input functionality specified in the *IIDC 1394-based Digital Camera (DCAM) Specification Version v1.31*. See the section *GPIO Control Using DCAM v1.31 PIO* / Strobe for further information.

Format:

Field	Bit	Description
IO0_Status	[0]	State (voltage level) of the IO0 pin 0: Low, 1: High
IO1_Status	[1]	State (voltage level) of the IO1 pin 0: Low, 1: High
IO2_Status	[2]	State (voltage level) of the IO2 pin 0: Low, 1: High
IO3_Status	[3]	State (voltage level) of the IO3 pin 0: Low, 1: High
	[4-31]	Reserved

Feature Availability:

Camera	Model/Sensor	Firmware	Avail.	Notes
CMLN	ALL	0.9.2.5	✓	Except Scorpion SCOR-03KD and SCOR-13SM.
DR2		0.9.0.42		
DX		1.1.1.21		
Flea		1.1.0.13		
Flea2		0.0.0.20		
FFMV		0.0.0.11		
BB2		0.9.1.40		

GRAS		0.9.1.28		
BBX3		0.9.1.10		
Scorpion		1.1.0.13		

2.13.29. PIO_DIRECTION: 11F8h

If the *IOx_Mode* bit is asserted (write a '1'), this means the GPIO pin is currently configured as an output and the *Pin_Mode* of the GPIO pin (see the GPIO_CTRL_PIN_x register) is GPIO_Mode_8. Otherwise, the *Pin_Mode* will be GPIO_Mode_0 (Input). The PIO_DIRECTION register is writeable only when the current GPIO_Mode is GPIO_Mode_0 or GPIO_Mode_8.

See the section *GPIO Control Using DCAM v1.31 PIO* / Strobe.

Format:

Field	Bit	Description
IO0_Mode	[0]	Current mode of GPIO Pin 0 0: Other, 1: Output
IO1_Mode	[1]	Current mode of GPIO Pin 1 0: Other, 1: Output
IO2_Mode	[2]	Current mode of GPIO Pin 2 0: Other, 1: Output
IO3_Mode	[3]	Current mode of GPIO Pin 3 0: Other, 1: Output
	[4-31]	Reserved

Feature Availability:

Camera	Model/Sensor	Firmware	Avail.	Notes
CMLN	ALL	0.9.2.5	✓	Except Scorpion SCOR-03KD and SCOR-13SM.
DR2		0.9.0.42		
DX		1.1.1.21		
Flea		1.1.0.13		
Flea2		0.0.0.20		
FFMV		0.0.0.11		
BB2		0.9.1.40		
GRAS		0.9.1.28		
BBX3		0.9.1.10		
Scorpion		1.1.0.13		

2.13.30. FRAME_TIME: 1240h

The FRAME_TIME register is implemented for the PGR *Dragonfly* only.

This register provides control over frame rate relative to the CURRENT_FRAME_RATE value.

For example, when CURRENT_FRAME_RATE = 4 (i.e. 30Hz on a lo-res Dragonfly) the camera sends 240 iso packets per image. To achieve 30Hz operation the camera waits for about 26-27 iso periods before sending the next image.

The FRAME_TIME register allows the desired frame rate to be specified, which could be considerably less than the nominal rate specified by CURRENT_FRAME_RATE. For example, with a CURRENT_FRAME_RATE of 30fps, 25fps is now possible.

The formula to determine the *Value* is:

FRAME_TIME = 800 * (Current_Frame_Rate / Desired_Frame_Rate)

Example:
To achieve 25fps while the current frame rate is 30fps:

FRAME_TIME = 800 * (30fps / 25fps)
= 960 = 3C0h

Enter 3C0h in the *Value* field (last 16 bits) of 1240h to achieve 25fps.

Format:

Field	Bit	Description
Presence_Inq	[0]	Presence of this feature 0: N/A 1: Available
	[1-5]	Reserved
ON_OFF	[6]	Always ON. To turn this feature OFF, write a 0 to this bit and bits 20-31 (Value_Field).
	[7–19]	Reserved
Value	[20-31]	Value

Camera Notes:

Camera	Model/Sensor	Firmware	Avail.	Notes
Dragonfly	ALL	2.1.2.14	✓	Implemented on Dragonfly only. For other cameras, use FRAME_RATE register.

2.13.31. DATA_FLASH_CTRL: 1240h

This register controls access to the camera's on-board flash memory that is available for non-volatile user data storage. Each bit in the data flash is initially set to 1.

Format:

Field	Bit	Description
Presence_Inq	[0]	Presence of this feature 0: N/A 1: Available
	[1-5]	Reserved
Clean_Page	[6]	Write: 1: Write page to data flash 0: No-op Read: 1: Page is clean 0: Page is dirty
	[7]	Reserved
Page_Size	[8-19]	8 == 256 byte page
Num_Pages	[20-31]	11 == 2048 pages

2.13.32. FRAME_SYNC_OFFSET: 1244h

The FRAME_SYNC_OFFSET register is implemented for the PGR *Dragonfly* only.

Multiple cameras of the same type on the same IEEE-1394 bus are automatically synchronized to each other at the hardware level. This register allows the user to offset the synchronization of one camera relative to another camera by a defined amount of time. For example, it would be possible for camera “B” to always grab images 1ms after camera “A” grabs images; the two cameras are therefore synchronized, but the grabbing of “B” is delayed by 1ms.

This register has the same format as the FRAME_TIME register and uses the same units. The offset must be some number between 0 and 1/- where - is the current frame rate. If the FRAME_TIME *Value* does not divide evenly into 128 seconds and the offset register is not written for all applicable cameras within the same 128s ISO period, setting a FRAME_SYNC_OFFSET *Value* will not work properly.

Format:

Field	Bit	Description
Presence_Inq	[0]	Presence of this feature 0: N/A 1: Available
	[1-5]	Reserved
ON_OFF	[6]	Always ON. To turn this feature OFF, write a 0 to this bit and bits 20-31 (Value_Field).
	[7–19]	Reserved
Value	[20-31]	Value

The formula to determine the FRAME_SYNC_OFFSET *Value* is:

$$\text{FRAME\_SYNC\_OFFSET} = \frac{\text{Desired\_Offset\_Time}}{(1 / \text{Current\_Frame\_Rate}) / \text{FRAME\_TIME\_}\mathit{Value}}$$

Example:
To determine the *Value* required to offset the synchronization of a camera running at 30Hz by 1ms, read the FRAME_TIME register 1240h *Value* field. Assuming the *Value* is 320h:

$$\text{FRAME\_SYNC\_OFFSET} = \frac{0.001\text{s}}{(1 / 30\text{fps}) / 320\text{h}}$$

$$= 0.001\text{s} / 0.0000416\text{s/unit}$$
$$= 24 = 18\text{h}$$

Enter 18h in the *Value* field of 1244h to offset that camera’s synchronization by 1ms.

Camera Notes:

Camera	Model/Sensor	Firmware	Avail.	Notes
Dragonfly	ALL	2.1.2.14	✓	Implemented on Dragonfly only. For other cameras, use TRIGGER_DELAY register.

2.13.33. DATA_FLASH_DATA: 1244h

This register provides the quadlet offset to the start of the actual data contained in the flash memory, if supported (query DATA_FLASH_CTRL register 1240h).

Any access outside of a modified page will automatically cause the page to be rewritten to flash, i.e. the user can write as much information as necessary, then perform a single write to the DATA_FLASH_CTRL register 1240h.

Format:

Field	Bit	Description
DF_Data	[0-31]	Quadlet offset to the start of data

2.13.34. TIME_FROM_INITIALIZE: 12E0h

This register reports the time, in seconds, since the camera (FPGA) was initialized. This initialization occurs during a hard power-up. This is different from powering up the camera via the CAMERA_POWER register, which will not reset this time.

Format:

Field	Bit	Description
Time_From_Init	[0-31]	Time in seconds since the camera was initialized.

Feature Availability:

Camera	Model/Sensor	Firmware	Avail.	Notes
GRAS	ALL	0.9.1.28	✓	

2.13.35. TIME_FROM_BUS_RESET: 12E4h

This register reports the time, in seconds, since the last IEEE-1394 bus reset occurred. This will be equal to the value reported by TIME_FROM_INITIALIZE if no reset has occurred since the last time the camera was initialized.

Format:

Field	Bit	Description
Time_From_Reset	[0-31]	Time in seconds since the camera detected a bus reset.

Feature Availability:

Camera	Model/Sensor	Firmware	Avail.	Notes
GRAS	ALL	0.9.1.28	✓	

2.13.36. IMAGE_RETRANSMIT: 12E8h

This register provides an interface to the camera's frame buffer functionality. The user can cause images to accumulate in the frame buffer by enabling the `HoldImg` bit of register 12E8h. This effectively disables the transmission of images over the 1394 interface in favor of accumulating them in the frame buffer. The user is then required to use the remaining elements of the interface to cause the transmission of the images.

The buffer system is circular in nature, storing only the most recent image data allowed by the buffer size. The number of images that this amounts to depends on the currently configured image size.

Format:

Field	Bit	Description
Presence_Inq	[0]	Presence of this feature 0: N/A 1: Available
Reserved	[1-5]	Reserved
HoldImg	[6]	Store images to frame buffer rather than transmitting 0: Off 1: On
Reserved	[7-15]	Reserved
BufferSize	[16-23]	Maximum number of images in the current configuration.
NumOfImages	[24-31]	Read: Number of images currently in buffer. Write: When HoldImg is enabled, transmits a single image and deletes the specified number of images from the buffer.

Feature Availability:

Camera	Model/Sensor	Firmware	Notes
Grasshopper	ALL	0.9.0.18	
Flea2	FL2G-13S2, FL2G-50S5	0.9.1.8	

2.13.37. FRAME_INFO: 12F8h

This register allows the user to control the types of frame-specific information that is embedded into the first several pixels of the image. The first byte of embedded image data starts at pixel 0,0 (column 0, row 0) and continues in the first row of the image data i.e. (1,0), (2,0), etc. Users using color cameras that do Bayer color processing on the PC must extract the value from the non-color processed image in order for the data to be valid.

Embedded image values are those in effect at the end of shutter integration.

Each piece of information takes up 1 quadlet (4 bytes) of the image. When the camera is operating in Y8 (8bits/pixel) mode, this is therefore 4 pixels worth of data. The types of information that can be embedded (e.g. image timestamp, camera shutter and gain settings, etc.) vary between models.

Insertion of each quadlet is controlled by a bit in this register. Because it is a bit field, quadlets appear in reverse order from the bits that control them. So, setting bit 31 to '1' turns on the Timestamp, bit 30 controls Gain, etc. For black and white cameras, white balance is still included, but no valid data is provided.

For example, a write of 800003FFh to this register on a PGR *Flea* would turn on all possible options. Therefore, the first 10 quadlets (40 bytes) of image data would contain camera information, in the following format:

```
FlyCaptureImage image;
image.pDatal[0]        = first byte of Timestamp data
image.pData[4]         = first byte of Gain data
image.pData[24]        = first byte of Frame Counter data
```

If you just turned on Shutter (0x12F8 = 0x80000004), then the first 4 bytes of the image would contain Shutter information for that image. Similarly, if you just turned on Brightness, the first 4 bytes would contain Brightness information.

Format:

Field	Bit	Description	Frame-Specific Information
Presence_Inq	[0]	Presence of this feature 0: N/A 1: Available	
	[1-21]	Reserved	
Insert_Info	22	Display image-specific information 0: Off 1: On	Region of Interest (ROI) position (See "Interpreting ROI Information" below)
	23		GPIO Pin State
	24		Strobe Pattern Counter
	25		Frame Counter
	26		White Balance CSR
	27		Exposure CSR
	28		Brightness CSR
	29		Shutter Value
	30		Gain CSR
	31		Timestamp (See "Interpreting Timestamp information" below)

Feature Availability:

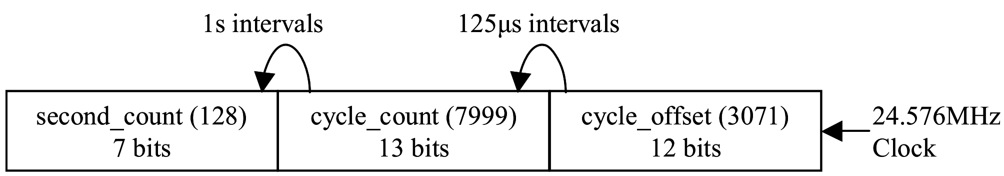
Camera	Model/Sensor	Firmware	Notes
Dragonfly	ALL	2.1.2.14	Timestamp only
Firefly MV	FFMV-03M2 & FMVU-03MT	0.9.2.12	Timestamp, GPIO Pin State and Strobe Pattern Counter
	FMVU-13S2	0.9.2.12	Timestamp, GPIO Pin State and Exposure CSR
DR2	ALL	0.9.0.42	Timestamp (bottom 4 bits are a 4-bit version of the Frame Counter) Gain CSR[2] Shutter Value Brightness CSR
DX		1.1.1.21	
Flea		1.1.0.13	
BB2		0.9.1.40	
GRAS		0.9.1.28	

[2] The full 32-bit value of the control and status register is embedded
[3] For monochrome cameras, the info embedded will be all zero's (black)

BBX3		0.9.1.10	Exposure CSR White Balance CSR[3] Frame Counter Strobe Pattern Counter GPIO Pin State
CMLN	ALL	0.9.2.5	All of the above, plus Region of Interest (ROI) position
Flea2		0.9.2.9	
Flea2G	ALL	0.9.0.6	All of the above, plus Region of Interest (ROI) position
Scorpion	ALL		See the *Scorpion Technical Reference Manual* for model-specific information.

Interpreting Timestamp information

The Timestamp format matches the CYCLE_TIME 0xFF100200 register format as follows (some cameras replace the bottom 4 bits of the cycle_offset with a 4-bit version of the Frame Counter):



Interpreting ROI information

The first two bytes of the quadlet are the distance from the left frame border that the region of interest (ROI) is shifted. The next two bytes are the distance from the top frame border that the ROI is shifted.

2.13.38. XMIT_FAILURE: 12FCh

This register contains a count of the number of failed frame transmissions that have occurred since the last reset. An error occurs if the camera cannot arbitrate for the bus to transmit image data and the image data FIFO overflows.

Format:

Field	Bit	Description
Frame_Count	[0-31]	Read: Count of failed frame transmissions. Write: Reset.

Feature Availability:

Camera	Model/Sensor	Firmware	Avail.	Notes
ALL	ALL		✓	

2.13.39. HDR: 1800h – 1884h

This register allows the user to access and control a multiple exposure quick cycle mode, which is useful for high dynamic range (HDR) imaging. The user can configure four (4) different sets of gain and shutter settings. When the feature is turned on, the camera will automatically begin cycling through each set, applying one gain and shutter value pair per frame. The camera will cycle through all available sets, regardless of their value.

Note that if bit [31] of the FRAME_INFO register 12F8h is set to 1, the camera will embed the current shutter / gain value in the image when bit [6] of HDR_CTRL is set to 1. The image timestamp will be embedded in the first quadlet of image data, the shutter value in the second quadlet, and gain in the third, all in big-endian format.

Format:

Offset	Name	Field	Bit	Description
1800h	HDR_CTRL	Presence_Inq	[0]	Presence of this feature 0: Not available, 1: Available
		-	[1-5]	Reserved
		ON_OFF	[6]	Write: ON or OFF for this feature Read: read a status 0: OFF, 1: ON If this bit = 0, other fields will be read only
		-	[7-31]	Reserved
1820h	HDR_SHUTTER_0	Presence_Inq	[0]	Presence of this feature 0: Not available, 1: Available
		-	[1-19]	Reserved
		Value	[20-31]	Query SHUTTER_INQ register 51Ch for range of possible shutter values
1824h	HDR_GAIN_0	Presence_Inq	[0]	Presence of this feature 0: Not available, 1: Available
		-	[1-19]	Reserved
		Value	[20-31]	Query GAIN_INQ register 520h for range of possible gain values
1840h	HDR_SHUTTER_1	Same format as HDR_SHUTTER_0		
1844h	HDR_GAIN_1	Same format as HDR_GAIN_0		
1860h	HDR_SHUTTER_2	Same format as HDR_SHUTTER_0		
1864h	HDR_GAIN_2	Same format as HDR_GAIN_0		
1880h	HDR_SHUTTER_3	Same format as HDR_SHUTTER_0		
1884h	HDR_GAIN_3	Same format as HDR_GAIN_0		

2.13.40. LED_CTRL: 1A14h

This register allows the user to turn off the camera's status LED. The LED will be re-enabled the next time the camera is power cycled.

Format:

Field	Bit	Description
Presence_Inq	[0]	Presence of this feature 0: N/A 1: Available
	[1-22]	Reserved
LED_Ctrl	[23-31]	Enable or disable the status LED 0x00: Off, 0x74: On

2.13.41. LUT: 1A40h – 1A44h

This register allows the user to access and control a lookup table (LUT), with entries stored on-board the camera. Changes to GAMMA are translated to writes of the LUT CSR registers. The LUT will also be modifed under the following circumstances:

- Camera reinitialization via the INITIALIZE register 000h
- Changing the CURRENT_VIDEO_MODE or CURRENT_VIDEO_FORMAT registers 604h or 608h
- Changing the GAMMA register 818h or ABS_VAL_GAMMA register
- Changing the WHITE_BALANCE register 80Ch (SCOR-13FF only)
- Writing the AUTO_EXPOSURE_RANGE register 108Ch (Flea only)

Format:

Offset	Name	Field	Bit	Description
1A40h	LUT_LO_CTRL	Presence_Inq	[0]	Presence of this feature 0: Not available, 1: Available
		-	[1-2]	Reserved
		Num_Channels	[3-5]	Number of channels
		ON_OFF	[6]	Write: ON or OFF for this feature Read: read a status 0: OFF, 1: ON If this bit = 0, other fields will be read only
		-	[7]	Reserved
		Bit_Depth	[8-15]	Bit depth of the lookup table
		Entries	[16-31]	Number of entries in the table
1A44h	LUT_HI_INQ		[0-31]	Quadlet offset of the lookup table

Camera Notes:

Camera	Model/Sensor	Firmware	Avail.	Notes
DR2	ALL	0.9.0.42	✓	• Three channels, 9-bit depth stored in 64 bits, 16 bits for each channel plus an additional 16 bits of packing. Same number of channels apply when in Mono mode. • LUT can be toggled ON or OFF.
FL2		0.0.0.20		
BB2		0.9.1.40		
GRAS		0.9.1.28		
BBX3		0.9.1.10		
DX	ALL	1.1.1.21	✓	• One channel, 8-bit depth • Capable of doing block transfers. • Not supported in Mono16 (Y16) modes. • LUT is always ON.
Flea		1.1.0.13		
Scorpion	SCOR-03SO	1.1.0.13		
	SCOR-14SO			
	SCOR-20SO			
	SCOR-13FF			

2.13.42. VOLTAGE: 1A50h – 1A54h

This register allows the user to access and monitor the various voltage registers supported by the camera.

Format:

Offset	Name	Field	Bit	Description
1A50h	VOLTAGE_LO_INQ	Presence_Inq	[0]	Presence of this feature 0: Not available, 1: Available
		-	[1-7]	Reserved
			[8-19]	Number of voltage registers supported
		-	[20-31]	Reserved
1A54h	VOLTAGE_HI_INQ		[0-31]	Quadlet offset of the voltage CSR's, which report the current voltage in Volts using the 32-bit floating-point IEEE/REAL*4 format.

2.13.43. PIXEL_DEFECT_CTRL: 1A60h

This register provides the user with an interface into enabling or disabling the mechanism used to correct defective (hot, dead, burned or bright) pixels.

Format:

Field	Bit	Description
Presence_Inq	[0]	Presence of this feature 0: N/A 1: Available
	[1-5]	Reserved
ON_OFF	[6]	Enable or disable pixel correction 0: Off 1: On
Reserved	[7]	Reserved
Max_Pixels	[8-19]	Maximum number of pixels that can be corrected
Cur_Pixels	[20-31]	Current number of pixels that are being corrected

2.13.44. AE_ROI: 1A70 – 1A74h

This register allows the user to specify a region of interest within the full image to be used for both auto exposure and white balance. The ROI position and size are relative to the transmitted image. If the request ROI is of zero width or height, the entire image will be used.

Format:

Offset	Name	Field	Bit	Description
1A70h	AE_ROI_CTRL	Presence_Inq	[0]	Presence of this feature 0: Not available, 1: Available
		-	[1-5]	Reserved
		ON_OFF	[6]	Write: ON or OFF for this feature Read: read a status 0: OFF, 1: ON If this bit = 0, other fields will be read only
		-	[7-31]	Reserved

1A74h	AE_ROI_OFFSET		[0-31]	Quadlet offset of the base address for the ROI CSR's
Base+0h (1C40h)	AE_ROI_UNIT_POSITION_INQ	Hposunit	[0-15]	Horizontal units for position
		Vposunit	[16-31]	Vertical units for position
Base+4h (1C44h)	AE_ROI_UNIT_SIZE_INQ	Hunit	[0-15]	Horizontal units for size
		Vunit	[16-31]	Vertical units for size
Base+8h (1C48h)	AE_ROI_POSITION	Left	[0-15]	Left position of ROI
		Top	[16-31]	Top position of ROI
Base+Ch (1C4Ch)	AE_ROI_SIZE	Width	[0-15]	Width of ROI
		Height	[16-31]	Height of ROI

2.13.45. FORMAT_7_RESIZE_INQ: 1AC8h

This register reports all internal camera processes being used to generate images in the current Format 7 mode. For example, users can read this register to determine if pixel binning and/or subsampling is being used to achieve a non-standard custom image size.

This register is read-only.

Format:

Field	Bit	Description
Presence_Inq	[0]	Presence of this feature 0: N/A 1: Available
	[1-7]	Reserved
Num_Cols	[8-11]	Number of columns being binned / subsampled, minus one e.g. if combining four columns together, this register will report a value of three.
Num_Rows	[12-15]	Number of rows binned / subsampled, minus one e.g. if combining four columns together, this register will report a value of three.
	[16-23]	Reserved
V_Pre_Color	[24]	Vertical subsampling / downsampling performed before color processing 0: Off, 1: On
H_Pre_Color	[25]	Horizontal subsampling / downsampling performed before color processing 0: Off, 1: On
V_Post_Color	[26]	Vertical subsampling / downsampling performed after color processing 0: Off, 1: On
H_Post_Color	[27]	Horizontal subsampling / downsampling performed after color processing 0: Off, 1: On

V_Bin	[28]	Standard vertical binning (addition of adjacent lines within horizontal shift register) 0: Off, 1: On
H_Bin	[29]	Standard horizontal binning (addition of adjacent lines within horizontal shift register) 0: Off, 1: On
V_Bayer_Bin	[30]	Vertical bayer binning (addition of adjacent even / odd lines within the interline transfer buffer) 0: Off, 1: On
H_Bayer_Bin	[31]	Horizontal bayer binning (addition of adjacent even / odd columns within the horizontal shift register) 0: Off, 1: On

2.13.46. PIXEL_CLOCK_FREQ: 1AF0h

This register specifies the current pixel clock frequency (in Hz) in IEEE-754 32-bit floating point format. The camera pixel clock defines an upper limit to the rate at which pixels can be read off the image sensor.

Format:

Field	Bit	Description
Pixel_Clock_Freq	[0-31]	Pixel clock frequency in Hz (read-only).

Feature Availability:

Camera	Model/Sensor	Firmware	Avail.	Notes
Dragonfly	ALL	2.1.2.14	-	Uses a fixed pixel clock frequency: • 1024x768: ~16.6MHz • 640x480: ~12.3MHz
ALL	ALL		✓	

2.13.47. HORIZONTAL_LINE_FREQ: 1AF4h

This register specifies the current horizontal line frequency in Hz in IEEE-754 32-bit floating point format.

Format:

Field	Bit	Description
Horizontal_Line_Freq	[0-31]	Horizontal line frequency in Hz (read-only).

Feature Availability:

Camera	Model/Sensor	Firmware	Avail.	Notes
ALL	ALL		✓	Except Scorpion SCOR-03KD and SCOR-13SM

2.13.48. CAMERA_LOG: 1D00 – 1DFFh

This register provides access to the camera's 256 byte internal message log, which is often useful for debugging camera problems. Characters are hexadecimal representations of ASCII characters. Contact technical support for interpretation of message logs.

Format:

Offset	Description
1D00..1D44	Each byte is the hexadecimal representation of an ASCII characters. Characters should be read starting at 1D00.

Feature Availability:

Camera	Model/Sensor	Firmware	Avail.	Notes
DR2	ALL	0.9.0.42	✓	
Flea2		0.0.0.20		
FFMV		0.0.0.11		
BB2		0.9.1.40		
GRAS		0.9.1.28		
BBX3		0.9.1.10		

2.13.49. SERIAL_NUMBER: 1F20h

This register specifies the unique serial number of the camera.

Format:

Field	Bit	Description
Serial_Number	[0-31]	Unique serial number of camera (read-only)

Feature Availability:

Camera	Model/Sensor	Firmware	Avail.	Notes
ALL	ALL		✓	

2.13.50. MAIN_BOARD_INFO: 1F24h

This register specifies the type of camera (according to the main printed circuit board).

Format:

Field	Bit	Description
Major_Board_Design	[0-11]	0x2: Digiclops 0x3: Dragonfly 0x4: Sync Unit 0x6: Ladybug Head 0x7: Ladybug Base Unit 0x8: Bumblebee 0xA: Scorpion Back Board 0x10: Flea 0x12: Dragonfly Express 0x18: Dragonfly2 0x19: Flea2 0x1A: Firefly MV 0x1C: Bumblebee2 0x1F: Grasshopper 0x21: Flea2G-13S2 0x24: Flea2G-50S5 0x26: Chameleon
Minor_Board_Rev	[12-15]	Internal use
Reserved	[16-31]	Reserved

Feature Availability:

Camera	Model/Sensor	Firmware	Avail.	Notes
ALL	ALL		✓	

2.13.51. SENSOR_BOARD_INFO: 1F28h

This register specifies the type of imaging sensor used by the camera (due to the wide variety of sensors available).

The interpretation of this register varies depending on the camera type, as defined in the MAIN_BOARD_INFO register 0x1F24 i.e. read MAIN_BOARD_INFO to determine how to use the Sensor_Type_x fields.

Format:

Field	Bit	Description
Sensor_Type_1	[0-11]	Scorpion: 0x001: Symagery VCA1281 CMOS 0x002: Kodak LM9618 CMOS 0x003: FillFactory IBIS5 CMOS 0x005: Sony ICX274 CCD 0x008: Sony ICX414 CCD 0x009: Sony ICX267 CCD Flea2: 0x001: Sony ICX424 / ICX204 CCD 0x002: Sony ICX267 / ICX274 CCD Grasshopper: 0x005: Sony ICX274 CCD 0x008: Sony ICX414 CCD 0x009: Sony ICX267 CCD 0x010: Sony ICX285 CCD 0x011: Sony ICX625 CCD
Minor_Board_Rev	[12-15]	Internal use
Reserved	[16-27]	Reserved
Sensor_Type_2	[28-31]	Scorpion: 0xA: 640x480 color (Sony ICX424AQ CCD) 0xB: 640x480 monochrome (Sony ICX424AL CCD) 0xC: 1024x768 color (Sony ICX204AQ CCD) 0xD: 1024x768 monochrome (Sony ICX204AL CCD) 0xE: Bayer (Scorpion) 0xF: Monochrome (Scorpion) Flea2: 0xA: Sony ICX424AQ color CCD 0xB: Sony ICX424AL mono CCD 0xC: Sony ICX204AQ color CCD 0xD: Sony ICX204AL mono CCD 0xE: Sony ICX267AK color CCD 0xF: Sony ICX267AL mono CCD 0x8: Sony ICX274AK color CCD 0x9: Sony ICX274AL mono CCD Grasshopper: 0xE: Bayer (color) 0xF: Monochrome

Feature Availability:

Camera	Model/Sensor	Firmware	Avail.	Notes
ALL	ALL		✓	

2.13.52. BUILD_TIMESTAMP: 1F40h

This register specifies the date that the current version of the firmware was built in Unix time format.

Format:

Field	Bit	Description
Build_Date	[0-31]	Date firmware was built (read-only)

Feature Availability:

Camera	Model/Sensor	Firmware	Avail.	Notes
ALL	ALL		✓	

2.13.53. FIRMWARE_VERSION: 1F60h

This register contains the version information for the currently loaded camera firmware. For more information on PGR versioning standards, see *Software and Version Numbering*.

Field	Bit	Description
Major	[0-7]	Major revision number
Minor	[8-15]	Minor revision number
Type	[16-19]	Type of release 0: Alpha 1: Beta 2: Release Candidate 3: Release
Revision	[20-31]	Revision number

Feature Availability:

Camera	Model/Sensor	Firmware	Avail.	Notes
ALL	ALL		✓	

2.13.54. FIRMWARE_BUILD_DATE: 1F64h

Specifies the date that the current version of the firmware was built in Unix time format.

Format:

Field	Bit	Description
Build_Date	[0-31]	Date firmware was built (read-only)

Feature Availability:

Camera	Model/Sensor	Firmware	Avail.	Notes
ALL	ALL		✓	

2.13.55. FIRMWARE_DESCRIPTION: 1F68-1F7Ch

Null padded, big-endian string describing the currently loaded version of firmware.

Feature Availability:

Camera	Model/Sensor	Firmware	Avail.	Notes
ALL	ALL		✓	

3 Isochronous Packet Format

Unlike simple register reads and writes, which are handled by asynchronous communication, the camera transmits image data using a guaranteed bandwidth mechanism known as isochronous data transmission. This section details the format and bandwidth requirements of the isochronous data broadcast by the camera. The amount of isochronous bandwidth allocated to a camera must be negotiated with the isochronous resource manager node (generally the 1394 host adapter in the PC). Every video format, mode and frame rate has a different video data format.

All Point Grey Research IEEE-1394 cameras follow these DCAM isochronous packet format specifications. To determine the formats / frame rates implemented by your camera, consult your camera's Technical Reference manual.

3.1. Isochronous Packet Format for Format_0, Format_1 and Format_2

The following table shows the format of the first quadlet (a quadlet being four bytes) in the data field of an isochronous data block.

<table>
<tr><th>0-7</th><th>8-15</th><th colspan="2">16-23</th><th colspan="2">24-31</th></tr>
<tr><td colspan="2">data_length</td><td>tag</td><td>channel</td><td>tCode</td><td>sy</td></tr>
<tr><td colspan="6">header_CRC</td></tr>
<tr><td colspan="6">Video data payload</td></tr>
<tr><td colspan="6">data_CRC</td></tr>
</table>

Table 1: Isochronous Data Packet Format for Format_0, Format_1 and Format_2.

data_length – the number of bytes in the data field.
tag – (tag field) shall be set to 0
channel – isochronous channel number, as programmed in the iso_channel field of the cam_sta_ctrl register
tCode – (transaction code) shall be set to the isochronous data block packet tCode.
sy – (synchronization value) shall be set to 0001h on the first isochronous data block of a frame, and shall be set to zero on all other isochronous data blocks.
Video data payload – shall contain the digital video information.

3.1.1. Isochronous Bandwidth Requirements

The amount of isochronous bandwidth required to transmit images from the camera is dependent on the format and frame rate. The following table describes the bandwidth requirements for each available format and frame rate. Each entry in the table indicates the required bandwidth in number of lines, pixels and quadlets per isochronous period. Bandwidth requirements for Format 7 are negotiated with the camera at runtime.

Format_0

Mode	Video Format	240fps	120fps	60fps	30fps	15fps	7.5fps	3.75fps	1.875fps
0	160x120 YUV(4:4:4) 24bit/pixel	4H 640p 480q	2H 320p 240q	1H 160p 120q	1/2H 80p 60q	1/4H 40p 30q	1/8H 20p 15q		
1	320x240 YUV(4:2:2) 16bit/pixel	8)8H 2560p 1280q	4)4H 1280p 640q	2H 640p 320q	1H 320p 160q	1/2H 160p 80q	1/4H 80p 40q	1/8H 40p 20q	1/16H 20p 10q
2	640x480 YUV(4:1:1) 12bit/pixel	16)16H 10240p 3840q	8)8H 5120p 1920q	4)4H 2560p 960q	2)2H 1280p 480q	1H 640p 240q	1/2H 320p 120q	1/4H 160p 60q	1/8H 80p 30q
3	640x480 YUV(4:2:2) 16bit/pixel	32)16H 10240p 5120q	16)8H 5120p 2560q	8)4H 2560p 1280q	4)2H 1280p 640q	2)1H 640p 320q	1/2H 320p 160q	1/4H 160p 80q	1/8H 80p 40q
4	640x480 RGB 24bit/pixel	32)16H 10240p 7680q	16)8H 5120p 3840q	8)4H 2560p 1920q	4)2H 1280p 960q	2)1H 640p 480q	1/2H 320p 240q	1/4H 160p 120q	1/8H 80p 60q
5	640x480 Y (Mono) 8bit/pixel	16)16H 10240p 2560q	8)8H 5120p 1280q	4)4H 2560p 640q	2)2H 1280p 320	1H 640p 160q	1/2H 320p 80q	1/4H 160p 40q	1/8H 80p 20q
6	640x480 Y (Mono) 16bit/pixel	32)16H 10240p 5120q	16)8H 5120p 2560q	8)4H 2560p 1280q	4)2H 1280p 640q	2)1H 640p 320q	1/2H 320p 160q	1/4H 160p 80q	1/8H 80p 40q
7	Reserved								

Format_1

Mode	Video Format	240fps	120fps	60fps	30fps	15fps	7.5fps	3.75fps	1.875fps
0	800*600 YUV(4:2:2) 16bit/pixel	32)20H 16000p 8000q	16)10H 8000p 4000q	8)5H 4000p 2000q	4)5/2H 2000p 1000q	2)5/4H 1000p 500q	5/8H 500p 250q	5/16H 250p 125q	
1	800x600 RGB 24bit/pixel		32)10H 8000p 600q	16)5H 4000p 3000q	8)5/2H 2000p 1500q	4)5/4H 1000p 750q	2)5/8H 500p 375q		
2	800x600 Y (Mono) 8bit/pixel	16)20H 16000p 4000q	8)10H 8000p 2000q	4)5H 4000p 1000q	2)5/2H 2000p 500q	5/4H 1000p 250q	5/8H 500p 125q		
3	1024x768 YUV(4:2:2) 16bit/pixel		32)12H 12288p 6144q	16)6H 6144p 3072q	8)3H 3072p 1536q	4)3/2H 1536p 768q	2)3/4H 768p 384q	3/8H 384p 192q	3/16H 192p 96q
4	1024x768 RGB 24bit/pixel			32)6H 6144p 4608q	16)3H 3072p 2304q	8)3/2H 1536p 1152q	4)3/4H 768p 576q	2)3/8H 384p 288q	3/16 192p 144q
5	1024x768 Y (Mono) 8bit/pixel	32)24H 24576p 6144q	16)12H 12288p 3072q	8)6H 6144p 1536q	4)3H 3072p 768q	2)3/2H 1536p 384q	3/4H 768p 192q	3/8H 384p 96q	3/16H 192p 48q
6	800x600 Y (Mono16) 16bit/pixel	32)20H 16000p 8000q	16)10H 8000p 4000q	8)5H) 4000p 2000q	4)5/2H 2000p 1000q	2)5/4H 1000p 500q	5/8H 500p 250q	5/16H 250p 125q	
7	1024x768 Y (Mono16) 16bit/pixel		32)12H 12288p 6144q	16)6H 6144p 3072q	8)3H 3072p 1536q	4)3/2H 1536p 768q	2)3/4H 768p 384q	3/8H 384p 192q	3/16H 192p 96q

Format_2

Mode	Video Format	120fps	60fps	30fps	15fps	7.5fps	3.75fps	1.875fps
0	1280x960 YUV(4:2:2) 16bit/pixel		32)8H 10240p 5120q	16)4H 5120p 2560q	8)2H 2560p 1280q	4)1H 1280p 640q	2)1/2H 640p 320q	1/4H 320p 160q

1	1280x960 RGB 24bit/pixel		32)8H 10240p 7680q	16)4H 5120p 3840q	8)2H 2560p 1920q	4)1H 1280p 960q	2)1/2H 640p 480q	1/4H 320p 240q
2	1280x960 Y (Mono) 8bit/pixel	32)16H 20480p 5120q	16)8H 10240p 2560q	8)4H 5120p 1280q	4)2H 2560p 640q	2)1H 1280p 320q	1/2H 640p 160q	1/4H 320p 80q
3	1600x1200 YUV(4:2:2) 16bit/pixel		32)10H 16000p 8000q	16)5H 8000p 4000q	8)5/2H 4000p 2000q	4)5/4H 2000p 1000q	2)5/8H 1000p 500q	5/16H 500p 250q
4	1600x1200 RGB 24bit/pixel			32)5H 8000p 6000q	16)5/2H 4000p 3000q	8)5/4H 2000p 1500q	4)5/8H 1000p 750q	2)5/16H 500p 375q
5	1600x1200 Y (Mono) 8bit/pixel	32)20H 32000p 8000q	16)10H 16000p 4000q	8)5H 8000p 2000q	4)5/2H 4000p 1000q	2)5/4H 2000p 500q	5/8H 1000p 250q	5/16H 500p 125q
6	1280x960 Y (Mono16) 16bit/pixel		32)8H 10240p 5120q	16)4H 5120p 2560q	8)2H 2560p 1280q	4)1H 1280p 640q	2)1/2H 640p 320q	1/4H 320p 160q
7	1600x1200 Y (Mono16) 16bit/pixel		32)10H 16000p 8000q	16)5H 8000p 4000qH	8)5/2H 4000p 2000q	4)5/4H 2000p 1000q	2)5/8H 1000p 500q	5/16H 500p 250q

[--H – Lines/Packet]
[--p – Pixels/Packet]
[--q – Quadlets/Packet]

2) : required S200 data rate
4) : required S400 data rate
8) : required S800 data rate
16) : required S1600 data rate
32) : required S3200 data rate

3.2. Isochronous Packet Format for Format_7

The following table shows the format of the first quadlet (a quadlet being four bytes) in the data field of an isochronous data block.

<table>
<tr><th>0-7</th><th>8-15</th><th colspan="2">16-23</th><th colspan="2">24-31</th></tr>
<tr><td colspan="2">data_length</td><td>tag</td><td>channel</td><td>tCode</td><td>sy</td></tr>
<tr><td colspan="6">header_CRC</td></tr>
<tr><td colspan="6">Video data payload</td></tr>
<tr><td colspan="6">data_CRC</td></tr>
</table>

Table 2: Isochronous Data Packet Format for Format_7.

data_length – the number of bytes in the data field.
tag – (tag field) shall be set to 0
channel – isochronous channel number, as programmed in the iso_channel field of the cam_sta_ctrl register
tCode – (transaction code) shall be set to the isochronous data block packet tCode.
sy – (synchronization value) shall be set to 0001h on the first isochronous data block of a frame, and shall be set to zero on all other isochronous data blocks.
Video data payload – shall contain the digital video information.

4 General Purpose Input / Output

This section describes the general purpose input/output (GPIO) functionality implemented on PGR IEEE-1394 cameras equipped with GPIO pins (see individual camera *Technical Reference Manual* for GPIO pin information).

Historically, PGR IEEE-1394 cameras that have implemented GPIO functionality (e.g. Dragonfly) have done so using the advanced GPIO_CTRL_PIN_x and GPIO_XTRA_PIN_x registers (1100h to 1144h) in conjunction with the GPIO Modes outlined below. However, with the addition of similar GPIO functionality to the *IIDC 1394-based Digital Camera (DCAM) Specification Version v1.31*, many PGR camera models are currently changing to also support the newly-defined trigger, parallel input/output (PIO), serial input/output (SIO) and strobe functionality outlined in version 1.31 of the DCAM. Therefore, while all PGR cameras support the PGR-specific GPIO modes, some cameras will also support the DCAM v1.31-specific input/output modes.

To determine whether your camera model supports the new DCAM v1.31 trigger functionality: 1) check the "Feature Availability" table for the relevant feature; or 2) query the camera's Opt_Function_Inq register 40Ch.

4.1. PGR-Specific GPIO Modes

The following modes are PGR-specific GPIO modes used exclusively with the GPIO_CTRL_PIN_x registers. All PGR IEEE-1394 digital cameras that are equipped with GPIO connectors currently support these GPIO registers and modes, with the exception of GPIO_Mode_8, which applies specifically to cameras that implement the DCAM v1.31-compliant input/output modes.

4.1.1. GPIO_Mode_0: Input

When a GPIO pin is put into *GPIO_Mode_0* and external wiring is attached to the pin, the associated GPIO_CTRL_PIN_x register's *Data* field will reflect the voltage level of the wiring. For example, a voltage of 0V would be reflected as a '0' in Bit 31, and a voltage of +3.3V would be reflected as a '1'.

4.1.2. GPIO_Mode_1: Output

A GPIO pin in *GPIO_Mode_1* will output a defined voltage signal, either high or low. If Bit 31 of the GPIO_CTRL_PIN_x register's *Data* field is '0', the pin will output 0V. If Bit 31 is set to '1', the pin will output +3.3V. Toggling this bit will therefore cause a rising or falling edge transition, which can be used to manually trigger external circuitry. Please note *GPIO_Mode_3* is the mode to use for automatic (continuous) triggering.

Do not connect power to a pin configured as an output (effectively connecting two outputs to each other). Doing so can cause damage to camera electronics.

4.1.3. GPIO_Mode_2: Asynchronous (External) Trigger

When a GPIO pin is put into *GPIO_Mode_2*, and an external TRIGGER_MODE enabled (which disables isochronous data transmission), the camera can be asynchronously triggered to grab an image by sending a voltage transition to the pin. Writing a '0' to Bit 31 of the GPIO_CTRL_PIN_x register will cause the camera to be triggered when it detects a falling edge; a '1' is used for a rising edge.

4.1.4. GPIO_Mode_3: Strobe

A GPIO pin in *GPIO_Mode_3* will output a voltage pulse of fixed delay and duration, according to the 32-bit value of the associated GPIO_XTRA_PIN_x register. The *Strobe_Start* and *Strobe_Multiplier* fields in the GPIO_XTRA register can be used to change the strobe behaviour.

When a GPIO pin is in this mode, a value written to the *Count_Period* field of the GPIO_STRPAT_CTRL register 0x110C, and a value written to the *Enable_Mask* field of the GPIO_STRPAT_MASK_PIN_x register, the pin will output a variable strobe pattern. Refer to Technical Application Note TAN2005003 for full details regarding the strobe pattern functionality.

4.1.5. GPIO_Mode_4: Pulse Width Modulation (PWM)

A GPIO pin in *GPIO_Mode_4* will output a specified number of pulses with programmable high and low duration.

The start of these pulses is defined by the user by writing the GPIO_CTRL_PIN_x register that is controlling the PWM. The pulse is independent of integration or external trigger. There is only one real PWM signal source (i.e. two or more pins cannot simultaneously output different PWM's), but the pulse can appear on any of the GPIO pins.

The units of time may vary between cameras, but is generally standardized to be in ticks of a 1.024MHz clock. New functionality has been added to recent firmware versions (available at http://www.ptgrey.com/support/downloads) that allow the user to designate a separate GPIO pin as an "enable pin"; the PWM pulses will continue only as long as the enable pin is held in a certain state (high or low).

The pin configured to output a PWM signal (PWM pin) remains in the same state at the time the 'enable pin' is disabled. For example, if the PWM is in a high signal state when the 'enable pin' is disabled, the PWM pin remains in a high state. To re-set the pin signal, you must re-

configure the PWM pin from GPIO_Mode_4 to GPIO_Mode_1.

To configure the camera to generate an infinite number of PWM pulses, set the *Pwm_Count* to 0xFF (255). To stop the infinite PWM pulse mode, set the *Pwm_Count* to 0x00 (0), or take the GPIO pin out of PWM mode by setting *Pin_Mode* to 0x00 (0).

Format of GPIO_CTRL_PIN_x Register in GPIO_Mode_4

Field	Bit	Description
Presence_Inq	[0]	Value should be ‘1’
	[1-11]	Reserved
Pin_Mode	[12-15]	Value should be ‘4’
Pwm_Count	[16-23]	Number of PWM pulses Read: The current count i.e. counts down the remaining pulses. After reaching zero, the count does not automatically reset to the previously-written value. Write: Writing the number of pulses starts the PWM. Write 0xFF for infinite pulses. *If this field is set to 0xFF (infinite pulses), it must be manually set to 0x00 before writing a different value.*
	[24]	Reserved
En_Pin	[25-27]	The GPIO pin to be used as a PWM enable; i.e. the PWM continues as long as the En_Pin is held in a certain state (high or low).
	[28]	Reserved
Disable_Pol	[29]	Polarity of the PWM enable pin (En_Pin) that will disable the PWM. For example, if this bit is zero, the PWM will be disabled when the PWM enable pin goes low.
En_En	[30]	0: Disable enable pin (En_Pin) functionality 1: Enable En_Pin functionality
Pwm_Pol	[31]	Polarity of the PWM signal 0: Low, 1: High

4.1.6. GPIO_Mode_8: Output (DCAM Specification v1.31)

A GPIO pin in *GPIO_MODE_8* is currently configured as an output using the DCAM v1.31 functionality. See the section, *GPIO Control Using DCAM v1.31 PIO* / Strobe.

4.2. GPIO Control Using DCAM v1.31 PIO / Strobe

Version 1.31 of the *IIDC 1394-based Digital Camera (DCAM) Specification* includes a new set of “Optional Function CSR” registers, which define a mechanism for controlling parallel input/output, strobe and serial port operations. These Optional Functions CSRs are implemented in some PGR

IEEE-1394 cameras. For cameras that implement this functionality, PGR recommends using these new registers instead of the GPIO registers 1100h to 1144h.

> *Refer to Technical Application Note (TAN2004004):* Synchronizing to an external device using DCAM 1.31 Trigger Mode_0*, for more information on how to use this new functionality. Technical Application Note's can be downloaded from* http://www.ptgrey.com/support/downloads/.

5 Parallel Input / Output (PIO)

5.1. PIO Control and Inquiry Registers

A GPIO pin can be in one of two states: output/strobe or input/trigger. The behaviour of each GPIO pin is controlled using the PIO registers.

5.1.1. Inquiry Register for PIO CSR Offset Addresses

The following register indicates the locations of the PIO CSR registers that are implemented by PGR IEEE-1394 cameras. These offsets are relative to the 1394 base offset 0xFFFF F0F0 0000.

Offset	Name	Field	Bit	Description
484h	PIO_CONTROL_CSR_INQ	PIO_Control_Quadlet_Offset	[0-31]	Quadlet offset of the PIO control CSRs from the base address of initial register space

5.1.2. Current PIO Register Offsets

At the time of this revision, the PIO offsets that would be derived using the quadlet offset information in the *Inquiry Registers for PIO CSR Offset Addresses* section would be as follows:

> *The following table of PIO offsets is current as of the revision date. These offsets are subject to change without notice. Refer to the section* Calculating Actual Offsets using Inquiry Register Quadlet Offsets *for information on calculating the actual offsets of the following registers.*

Offset	Name	Field	Bit	Description

11F0h	PIO_OUTPUT	Output_Port	[0-31]	General purpose PIO output
11F4h	PIO_INPUT	Input_Port	[0-31]	General purpose PIO input
11F8h	PIO_DIRECTION	Input_Output_Ctrl	[0-31]	Current state of the PIO

PIO_DIRECTION is used for configuring pins to be either inputs or outputs, and is used in conjunction with the PIO_OUTPUT and PIO_INPUT registers. If the *IOx_Mode* bit is asserted (write a '1'), this means the GPIO pin is currently configured as an output and the *Pin_Mode* of the GPIO pin (see the GPIO_CTRL_PIN_x register) is GPIO_Mode_8. Otherwise, the *Pin_Mode* will be GPIO_Mode_0 (Input). The PIO_DIRECTION register is writeable only when the current GPIO_Mode is GPIO_Mode_0 or GPIO_Mode_8.

PIO_OUTPUT is used for configuring the output values for individual pins. PIO_INPUT is used for configuring the input values for individual pins.

5.1.3. Configuring PIO for External Trigger

To configure a GPIO pin to be a trigger, set the bit for the relevant pin in the PIO_DIRECTION: 11F8h register to '0', then set the bit for the relevant pin in the TRIGGER_MODE register *Trigger_Source* field.

Only one GPIO pin can be configured as a trigger source using this method. To have multiple pins acting as a trigger sources, use the GPIO_MODE_2 method via the GPIO_CTRL_PIN_x registers.

5.1.4. Configuring PIO for Strobe Output

To configure a GPIO pin to output a strobe pulse, set the bit for the relevant pin in the PIO_DIRECTION: 11F8h register to '1', then set the duration and delay using the related STROBE_x_CNT register.

6 Strobe Signal Output

This section describes the control and inquiry registers for the Strobe Signal functionality specified in the *IIDC 1394-based Digital Camera (DCAM) Specification Version v1.31*.

6.1. Inquiry Register for Strobe Output CSR Offset Addresses

The following register indicates the locations of the Strobe Output CSR registers that are implemented by PGR IEEE-1394 cameras. These offsets are relative to the 1394 base offset 0xFFFF F0F0 0000.

Offset	Name	Field	Bit	Description
48Ch	STROBE_OUTPUT_CSR_INQ	Strobe_Output_Quadlet_Offset	[0-31]	Quadlet offset of the Strobe output signal CSRs from the base address of initial register space

6.2. Current Strobe Output Register Offsets

At the time of this revision, the strobe output offsets that would be derived using the quadlet offset information in the *Inquiry Registers for Strobe Output CSR Offset Addresses* section would be as follows:

The following table of strobe output offsets is current as of the revision date. These offsets are subject to change without notice. Refer to the section Calculating Actual Offsets using Inquiry Register Quadlet Offsets *for information on calculating the actual offsets of the following registers.*

(Bit values = 0: Not Available, 1: Available)

Format:

Offset	Name	Field	Bit	Description
1300h	STROBE_CTRL_INQ	Strobe_0_Inq	[0]	Presence of strobe 0 signal
		Strobe_1_Inq	[1]	Presence of strobe 1 signal
		Strobe_2_Inq	[2]	Presence of strobe 2 signal
		Strobe_3_Inq	[3]	Presence of strobe 3 signal
		-	[4-31]	Reserved
1304h : 13FCh	Reserved			

1400h	STROBE_0_INQ	Presence_Inq	[0]	Presence of this feature 0: N/A 1: Available
			[1-3]	Reserved
		ReadOut_Inq	[4]	Ability to read the value of this feature
		On_Off_Inq	[5]	Ability to switch feature ON and OFF
		Polarity_Inq	[6]	Ability to change signal polarity
			[7]	Reserved
		Min_Value	[8-19]	Minimum value for this feature control
		Max_Value	[20-31]	Maximum value for this feature control
1404h	STROBE_1_INQ	Same definition as Strobe_0_Inq		
1408h	STROBE_2_INQ	Same definition as Strobe_0_Inq		
140Ch	STROBE_3_INQ	Same definition as Strobe_0_Inq		
1410h : 14Ch	Reserved			
1500h	STROBE_0_CNT	Presence_Inq	[0]	Presence of this feature 0: N/A 1: Available
			[1-5]	Reserved
		On_Off	[6]	Write: ON or OFF this function Read: read a status 0: OFF, 1: ON If this bit = 0, other fields will be read only.
		Signal_Polarity	[7]	Select signal polarity If Polarity_Inq is “1”: - Write to change strobe output polarity - Read to get strobe output polarity If Polarity_Inq is “0”: - Read only 0: Low active output 1: High active output
		Delay_Value	[8-19]	Delay after start of exposure until the strobe signal asserts
		Duration_Value	[20-31]	Duration of the strobe signal A value of 0 means de-assert at the end of exposure, if required.
1504h	STROBE_1_CNT	Same definition as Strobe_0_Cnt		
1508h	STROBE_2_CNT	Same definition as Strobe_0_Cnt		
150Ch	STROBE_3_CNT	Same definition as Strobe_0_Cnt		
1510h-15FFh	Reserved			

7 Serial Port Input / Output (SIO)

Some PGR IEEE-1394 cameras are equipped with RS232 serial port functionality via the camera's GPIO connector. For specific hardware configuration information regarding the serial port connector consult your camera's *Technical Reference* manual or *Getting Started* manual. For information on how to configure your camera's registers and GPIO connector to act as an RS232 serial port connector, consult *Technical Application Note TAN2004001: Configuring and testing the RS-232 serial port*, available at http://www.ptgrey.com/support/downloads/.

7.1. SIO Buffers

- Both the transmit and receive buffers are implemented as circular buffers that may exceed the 255 byte maximum specified by the *Buffer_Size_Inq* [24..31] field of the Serial_Mode_Reg register 2000h.
- The transmit buffer size is 512B.
- The receive buffer size is 2KB.
- Block reads and writes are both supported. Neither their length nor their address have to be quadlet aligned or divisible by 4.

7.2. Serial Input Transaction (Receiving Data)

This section provides a general overview of the steps for a serial input transaction, where the camera is receiving data from a transmitting serial port.

1. Read the valid data size of current receive buffer *RBUF_ST* or *RDRD* flag.
2. Write the input data length to *RBUF_CNT*.
3. Read received characters from *SIO_Data_Register*.
4. To input more characters, repeat step 1.

7.3. Serial Output Transaction (Transmitting Data)

This section provides a general overview of the steps for a serial output transaction, where the camera is transmitting data to a receiving serial port.

1. Read the available data space of the current transmit buffer *TBUF_ST* or *TDRD* flag.
2. Write characters to the *SIO_Data_Register*.
3. Write the valid output data length to *TBUF_CNT* to start transmit.
4. To output more characters, repeat step 1.

7.4. SIO Control and Inquiry Registers

This section describes the control and inquiry registers for the serial input/output (SIO) control functionality defined in the *IIDC 1394-based Digital Camera (DCAM) Specification Version v1.31*.

7.4.1. Inquiry Register for SIO CSR Offset Addresses

The following register indicates the locations of the Strobe Output CSR registers that are implemented by PGR IEEE-1394 cameras. These offsets are relative to the 1394 base offset 0xFFFF F0F0 0000.

Offset	Name	Field	Bit	Description
488h	SIO_CONTROL_CSR_INQ	SIO_Control_Quadlet_Offset	[0-31]	Quadlet offset of the SIO control CSRs from the base address of initial register space

7.4.2. Current SIO Register Offsets

At the time of this revision, the SIO offsets that would be derived using the quadlet offset information in the *Inquiry Registers for SIO CSR Offset Addresses* section would be as follows:

The following table of SIO offsets is current as of the revision date. These offsets are subject to change without notice. Refer to the section Calculating Actual Offsets using Inquiry Register Quadlet Offsets *for information on calculating the actual offsets of the following registers.*

(Bit values = 0: Not Available, 1: Available)

Format:

Offset	Name	Field	Bit	Description
2000h	SERIAL_MODE_REG	Baud_Rate	[0-7]	*Baud rate setting* Write: Set baud rate Read: Get current baud rate 0: 300bps 1: 600bps 2: 1200bps 3: 2400bps 4: 4800bps 5: 9600bps 6: 19200bps 7: 38400bps 8: 57600bps 9: 115200bps 10: 230400bps Other values reserved

		Char_Length	[8-15]	*Character length setting* Write: Set data length (must not be 0) Read: Get data length 7: 7bits 8: 8bits Other values reserved
		Parity	[16-17]	*Parity setting* Write: Set parity Read: Get current parity 0: None 1: Odd 2: Even
		Stop_Bit	[18-19]	*Stop bits* Write: Set stop bit Read: Get current stop bit 0: 1 1: 1.5 2: 2
		-	[20-23]	Reserved
		Buffer_Size_Inq	[24-31]	*Buffer Size (Read-Only)* This field indicates the maximum size of the receive/transmit data buffer. See also section 7.1: *SIO Buffers*. If this value=1, *Buffer_Status_Control* and *SIO_Data_Register* characters 1-3 should be ignored.
2004h	SERIAL_CONTROL_REG	RE	[0]	*Receive enable* Indicates if the camera's ability to receive data has been enabled. Enabling this register causes the receive capability to be immediately started. Disabling this register causes the data in the buffer to be flushed. Read: Current status Write: 0: Disable, 1: Enable
		TE	[1]	*Transmit enable* Indicates if the camera's ability to transmit data has been enabled. Enabling this register causes the transmit capability to be immediately started. Disabling this register causes data transmission to stop immediately, and any pending data is discarded. Read: Current status Write: 0: Disable, 1: Enable
		-	[2-7]	Reserved

	SERIAL_STATUS_REG	TDRD	[8]	*Transmit data buffer ready (read only)* Indicates if the transmit buffer is ready to receive data from the user. It will be in the *Ready* state as long as *TBUF_ST* != 0 and TE is enabled. Read only 0: Not ready, 1: Ready
		-	[9]	Reserved
		RDRD	[10]	*Receive data buffer ready (read only)* Indicates if the receive buffer is ready to be read by the user. It will be in the *Ready* state as long as *RBUF_ST* != 0 and RE is enabled. Read only 0: Not ready, 1: Ready
		-	[11]	Reserved
		ORER	[12]	*Receive buffer over run error* Read: Current status Write: 0: Clear flag, 1: Ignored
		FER	[13]	*Receive data framing error* Read: Current status Write: 0: Clear flag, 1: Ignored
		PER	[14]	*Receive data parity error* Read: Current status Write: 0: Clear flag, 1: Ignored
		-	[15-31]	Reserved
2008h	RECEIVE_BUFFER_STATUS_CONTROL	RBUF_ST	[0-8]	*SIO receive buffer status* Indicates the number of bytes that have arrived at the camera but have yet to be queued to be read. Read: Valid data size of current receive buffer Write: Ignored
		RBUF_CNT	[8-15]	*SIO receive buffer control* Indicates the number of bytes that are ready to be read. Read: Remaining data size for read Write: Set input data size
		-	[16-31]	Reserved
200Ch	TRANSMIT_BUFFER_STATUS_CONTROL	TBUF_ST	[0-8]	*SIO output buffer status* Indicates the minimum number of free bytes available to be filled in the transmit buffer. It will count down as bytes are written to any of the *SIO_Data_Registers* starting at 2100h. It will count up as bytes are actually transmitted after a write to *TBUF_CNT*. Although its maximum value is 255, the actual amount of available buffer space may be larger. Read: Available data space of transmit buffer Write: Ignored

		TBUF_CNT	[8-15]	*SIO output buffer control* Indicates the number of bytes that have been stored since it was last written to. Writing any value to *TBUF_CNT* will cause it to go to 0. Writing a number less than its value will cause that many bytes to be transmitted and the rest thrown away. Writing a number greater than its value will cause that many bytes to be written - its value being valid and the remainder being padding. Read: Written data size to buffer Write: Set output data size for transmit.
		-	[16-31]	Reserved
2010h : 20FFh	Reserved			
2100h	SIO_DATA_REGISTER	Char_0	[0-7]	*Character_0* Read: Read character from receive buffer. Padding data if data is not available. Write: Write character to transmit buffer. Padding data if data is invalid.
		Char_1	[8-16]	*Character_1* Read: Read character from receive buffer+1. Padding data if data is not available. Write: Write character to transmit buffer+1. Padding data if data is invalid.
		Char_2	[17-23]	*Character_2* Read: Read character from receive buffer+2. Padding data if data is not available. Write: Write character to transmit buffer+2. Padding data if data is invalid.
		Char_3	[24-31]	*Character_3* Read: Read character from receive buffer+3. Padding data if data is not available. Write: Write character to transmit buffer+3. Padding data if data is invalid.
2104h : 21FFh	SIO_DATA_REGISTER_ALIAS		[0-31]	Alias SIO_Data_Register area for block transfer.

Feature Availability:

Camera	Model/Sensor	Firmware	Avail.	Notes
DR2	ALL	0.9.0.42	✓	Except Scorpion SCOR-03KD and SCOR-13SM. Supports block transfers.
DX		1.1.1.21		
Flea		1.1.0.13		

Flea2		0.0.0.20		Consult Technical Application Note TAN2004001 for further configuration information.
FFMV		0.0.0.11		
BB2		0.9.1.40		
Scorpion		1.1.0.13		

8 Trigger Modes

This section describes the internal and external trigger modes available. Not all cameras support all trigger modes. For information on the trigger modes supported by individual cameras, consult their respective *Getting Started Manual* or *Technical Reference*, or read the camera's TRIGGER_INQ register 0x530 (refer to the *Point Grey Digital Camera Register Reference*).

These modes and their interaction with the GPIO pins can be configured and controlled via the TRIGGER_MODE register at 830h and the GPIO registers at 1100h-1144h.

8.1.1. Trigger_Mode_0 (“Standard External Trigger Mode”)

Trigger_Mode_0 is best described as the standard external trigger mode. When the camera is put into Trigger_Mode_0, the camera starts integration of the incoming light from external trigger input falling/rising edge. The SHUTTER register describes integration time. No parameter is required. The camera can be triggered in this mode using the GPIO pins as external trigger or the SOFTWARE_TRIGGER (62Ch) or SOFT_ASYNC_TRIGGER (102Ch) registers.

It is not possible to trigger the camera the full frame rate using Mode_0; however, this is possible using Trigger_Mode_14.

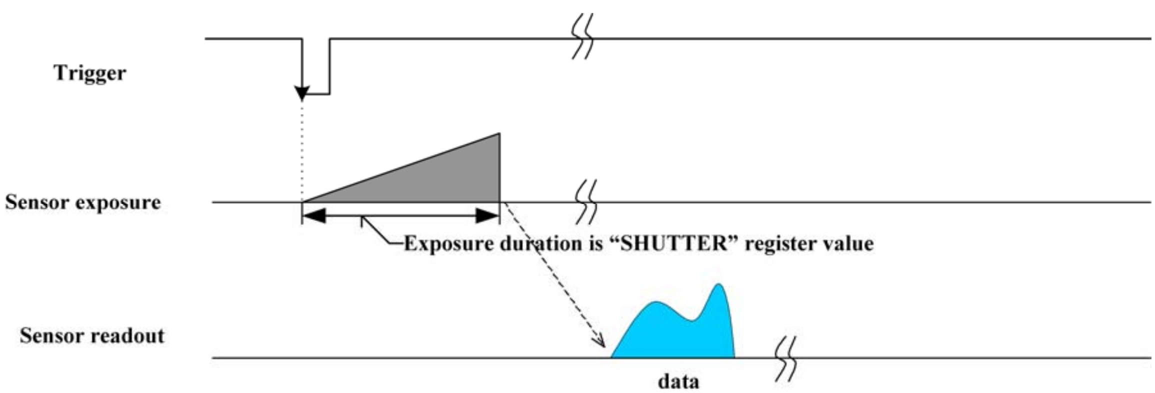


Figure 1: Trigger_Mode_0 (“Standard External Trigger Mode”)

8.1.2. Trigger_Mode_1 (“Bulb Shutter Mode”)

Also known as Bulb Shutter mode, Trigger_Mode_1 is an IIDC 1394 DCAM-compliant trigger mode, in which the camera starts integration of the incoming light from external trigger input falling edge. Integration time is equal to low state time of the external trigger input.

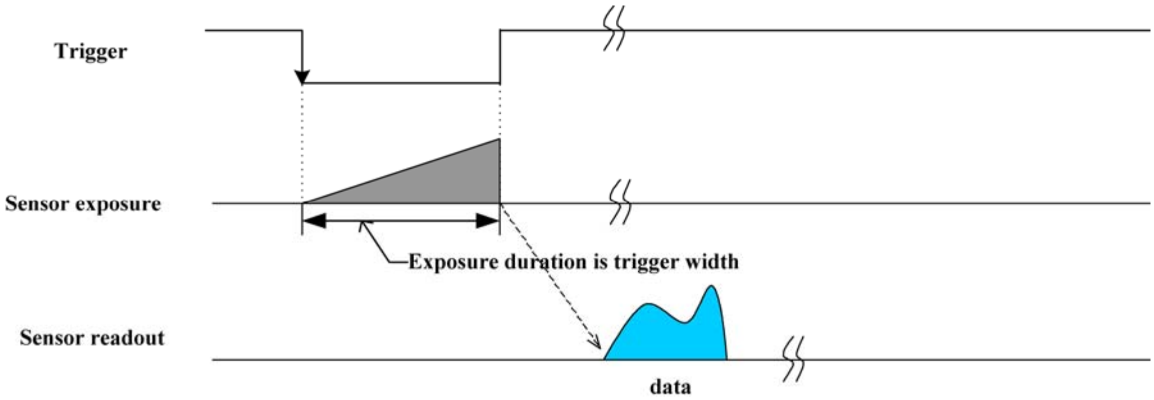


Figure 2: Trigger_Mode_1 ("Bulb Shutter Mode")

8.1.3. Trigger_Mode_3 ("Skip Frames Mode")

Trigger_Mode_3 allows the user to put the camera into a mode where the camera only transmits one out of N specified images. This is an internal trigger mode that requires no external interaction. Where N is the parameter set in bits [20-31] of the TRIGGER_MODE register (offset 830h), the camera will issue a trigger internally at a cycle time that is N times greater than the current frame rate. Again, the SHUTTER register describes integration time. Note that this is different from the IIDC specification that states the cycle time will be N times greater than the fastest frame rate.

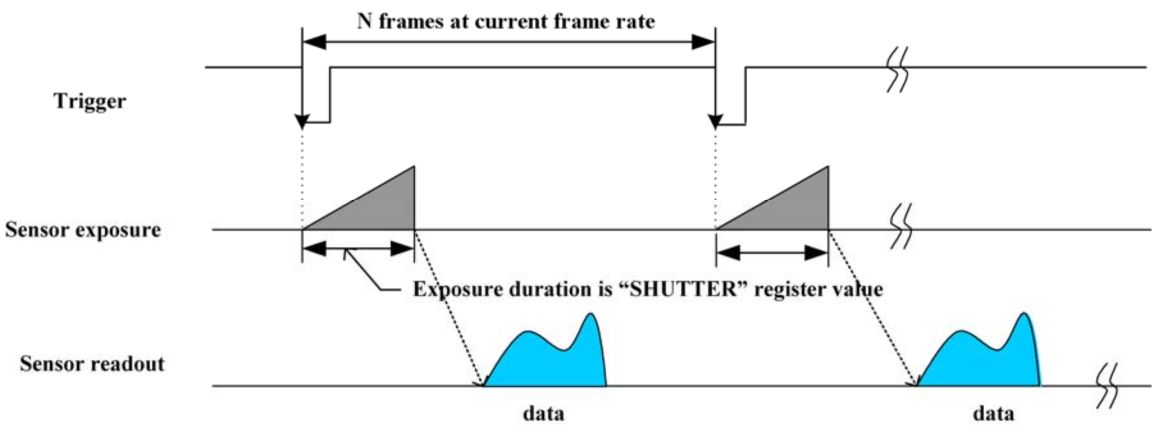


Figure 3: Trigger_Mode_3 ("Skip Frames Mode")

8.1.4. Trigger_Mode_4 ("Multiple Exposure Preset Mode")

Trigger_Mode_4 allows the user to set the number of triggered images to be exposed before the image readout starts. In the case of Trigger_Mode_4, the shutter time is controlled by the SHUTTER CSR value; the minimum resolution of the duration is therefore limited by the shutter resolution.

In the figure below, the camera starts integration of incoming light from the first external trigger input falling edge and exposes incoming light at shutter time. Repeat this sequence for N (parameter) external trigger inputs edge then finish integration. Parameter is required and shall be one or more (N >= 1).

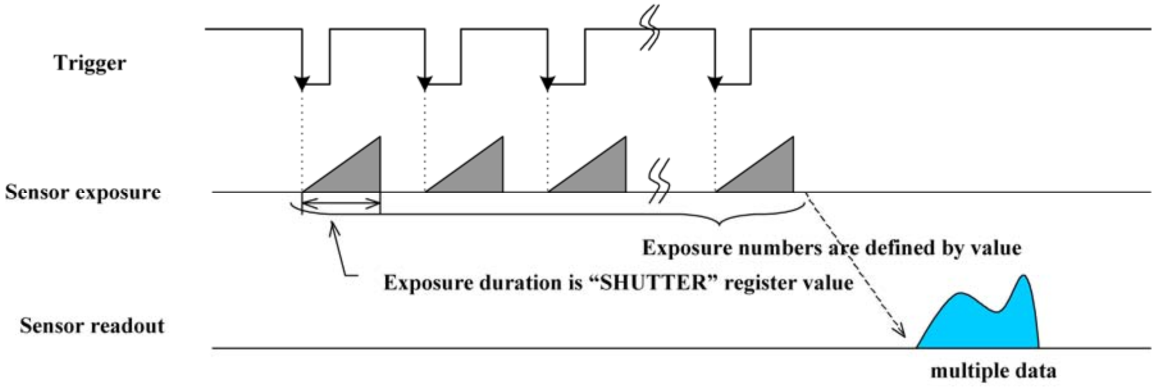


Figure 4: Trigger_Mode_4 ("Multiple Exposure Preset Mode")

8.1.5. Trigger_Mode_5 ("Multiple Exposure Pulse Width Mode")

Trigger_Mode_5 allows the user to set the number of triggered images to be exposed before the image readout starts. In the case of Trigger_Mode_5, the shutter time is controlled by the trigger pulse duration; the minimum resolution of the duration is generally 1 tick of the pixel clock (see the PIXEL_CLOCK_FREQ register 0x1AF0). The resolution also depends on the quality of the input trigger signal and the current TRIGGER_DELAY.

In the figure below, the camera starts integration of incoming light from the first external trigger input falling edge and exposes incoming light until the trigger is inactive. Repeat this sequence for N (parameter) external trigger inputs then finish integration. Parameter is required and shall be one or more (N >= 1).

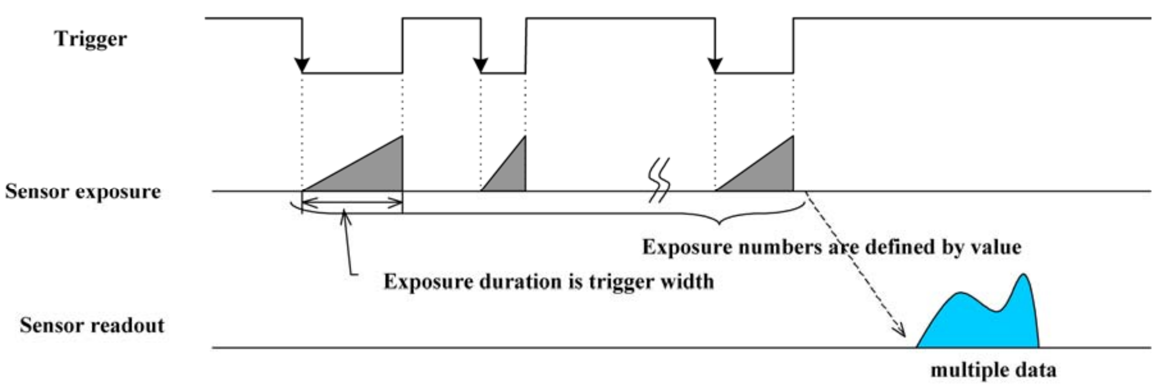


Figure 5: Trigger_Mode_5 ("Multiple Exposure Pulse Width Mode")

8.1.6. Trigger_Mode_14 ("Overlapped Exposure / Readout Mode")

Trigger_Mode_14 is a vendor-unique trigger mode that is very similar to Trigger_Mode_0, but allows for triggering at faster frame rates. This mode works well for users who want to drive exposure start with an external event. However, users who need a precise exposure start should use Trigger_Mode_0.

In the figure below, the trigger may be overlapped with the readout of the image, similar to continuous shot (free-running) mode. If the trigger arrives before the end of shutter integration, it is dropped. If the trigger arrives after sensor readout is complete, it will start as quickly as the imaging area can be cleared. If the trigger arrives while the image is still being read out of the sensor, the start of exposure will be delayed until the next opportunity to clear the imaging area without injecting noise into the output image. The end of exposure cannot occur before the end of the previous image readout. Therefore, exposure start may be delayed to ensure this, which means priority is given to maintaining the proper exposure time instead of to the trigger start.

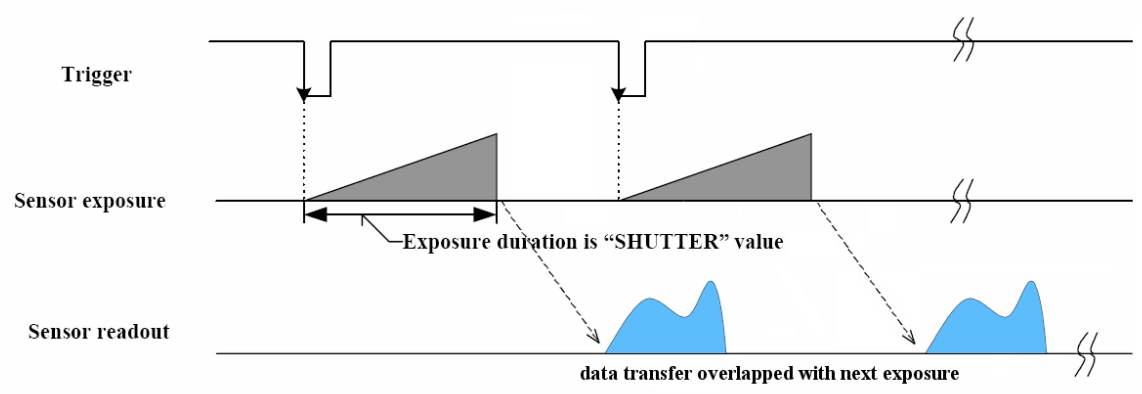


Figure 6: Trigger_Mode_14 (“Overlapped Exposure / Readout Mode”)

8.1.7. Trigger_Mode_15 (“Multi-Shot Trigger Mode”)

Trigger_Mode_15 is a vendor-unique trigger mode that allows the user to fire a single hardware or software trigger and have the camera acquire and stream a predetermined number of images at the current frame rate.

The number of images to be acquired is determined by the Parameter field of the TRIGGER_MODE register 0x830, which allows up to 255 images to be acquired from a single trigger. Writing a value of 0 to the parameter field will result in an infinite number of images to be acquired, essentially allowing users to trigger the camera into a free-running mode. Once the trigger is fired, the camera will acquire N images with an exposure time equal to the value defined by the SHUTTER register, and stream the images to the host system at the current frame rate. Once this is complete, the camera can be triggered again to repeat the sequence.

Any write to the TRIGGER_MODE register 0x830 will cause the current sequence to stop.

Note: during the capture of N images, the camera is still in an asynchronous trigger mode (essentially Trigger Mode 14), rather than continuous (free-running) mode. The result of this is that the FRAME_RATE register 0x83C will be turned OFF, and the camera put into extended shutter mode (see Knowledge Base Article 166). Users should therefore ensure that the maximum shutter time is limited to 1/frame_rate to get the N images captured at the current frame rate.

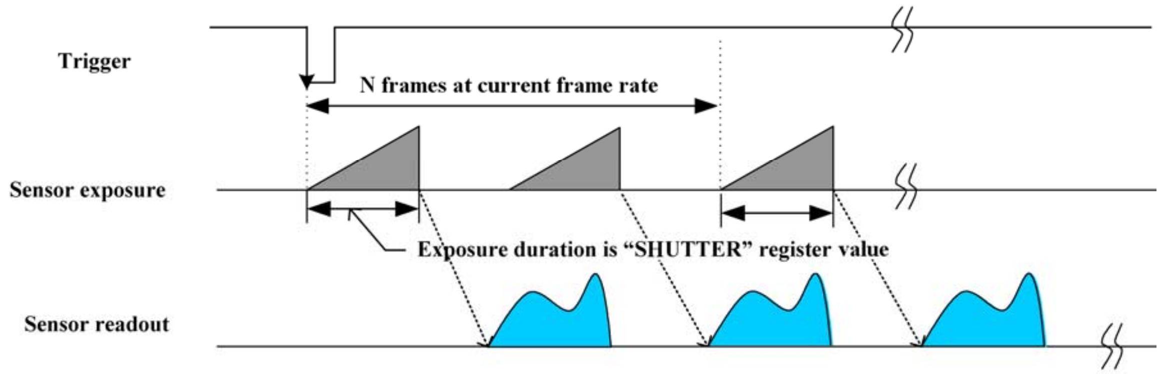


Figure 7: Trigger_Mode_15 ("Multi-Shot Trigger Mode")

9 Technical Support Resources

Point Grey Research Inc. endeavors to provide the highest level of technical support possible to our customers. Most support resources can be accessed through the Product Support section of our website: www.ptgrey.com/support.

Creating a Customer Login Account

The first step in accessing our technical support resources is to obtain a Customer Login Account. This requires a valid name, e-mail address, and camera serial number. To apply for a Customer Login Account go to www.ptgrey.com/support/downloads/.

Knowledge Base

Our on-line knowledge base at www.ptgrey.com/support/kb/ contains answers to some of the most common support questions. It is constantly updated, expanded, and refined to ensure that our customers have access to the latest information.

Product Downloads

Customers with a Customer Login Account can access the latest software and firmware for their cameras from our downloads site at www.ptgrey.com/support/downloads. We encourage our customers to keep their software and firmware up-to-date by downloading and installing the latest versions.

Contacting Technical Support

Before contacting Technical Support, have you:

1. *Read the product documentation and user manual?*
2. *Searched the Knowledge Base?*
3. *Downloaded and installed the latest version of software and/or firmware?*

If you have done all the above and still can't find an answer to your question, contact our Technical Support team at www.ptgrey.com/support/contact/.

10 Contacting Point Grey Research Inc.

For any questions, concerns or comments please contact us via the following methods:

Email:	For all general questions about Point Grey Research please contact us at info@ptgrey.com. For technical support (existing customers only) contact us at http://www.ptgrey.com/support/contact/.	
Knowledge Base:	Find answers to commonly asked questions in our knowledge base at http://www.ptgrey.com/support/kb/.	
Downloads:	Users can download the latest manuals and software from http://www.ptgrey.com/support/downloads/	
Main Office:	**Mailing Address:** Point Grey Research, Inc. 12051 Riverside Way Richmond, BC, Canada V6W 1K7	**Tel:** +1 (604) 242-9937 **Toll-free** (North America only)**:** +1 (866) 765-0827 **Fax:** +1 (604) 242-9938 sales@ptgrey.com
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USA	**Tel:** +1 (866) 765-0827 na-sales@ptgrey.com	
Europe Israel	**Mailing Address:** Point Grey Research GmbH Schwieberdinger Strasse 60 71636 Ludwigsburg Germany	**Tel:** +49 7141 488817-0 **Fax:** +49 7141 488817-99 eu-sales@ptgrey.com
Japan	ViewPLUS Inc. (http://www.viewplus.co.jp/)	
Korea	Cylod Co. Ltd. (http://www.cylod.com)	
China	LUSTER LightVision Tech. Co., Ltd (www.lusterlighttech.com)	
Singapore Malaysia Thailand	Voltrium Systems Pte Ltd. (www.voltrium.com.sg)	
Taiwan	Apo Star Co., Ltd. (www.apostar.com.tw)	

Appendix A: Version Numbering Scheme

10.1.1. Overview

All PGR software and firmware follow a standardized version-naming scheme that allows users to quickly and easily determine the latest software versions. All software and firmware version numbers consist of 4 numbers separated by periods e.g. firmware version 2.0.0.20. This follows the general pattern of:

```
MajorRevision.MinorRevision.TypeOfRelease.BuildNumber
```

where Type of Release is always '0' for an Alpha version, '1' for Beta, '2' for Release Candidate, and '3' for Release. All future firmware and software versions posted on our download site will follow this scheme. To determine the latest version of a particular family of software, look first at Major Revision, then Minor Revision and finally Build Number. The Build Number does not increase indefinitely, but instead resets after each increase of either the Minor or Major Revision Number.

Example:
Version 2.0.1.24 is a later version than 2.0.0.23, and is also Beta class software. However, version 2.1.0.1 is a later version than 2.0.1.24, as this product has undergone a minor revision. Version 1.4.0.18 is a later version than 1.3.3.5, even though it is Alpha class software.

10.1.2. Alpha

Software that meets the PGR Alpha standard is not required to satisfy a large percentage of the full software release process. This classification has been instituted for quick bug fixes and new functionality. As such, a user of an Alpha release has very few guarantees outside from the software version number being correct. As a general rule, Alpha releases will not be made public. Upon request, they can and will be emailed to knowledgeable users.

10.1.3. Beta

The requirements for a piece of software to meet the Beta standard are substantially stricter than those of the Alpha standard. A release that meets the Beta requirements will be functionally complete. It will have been tested internally and by Alpha users, source code documentation will be complete and memory leaks and other similar problems will be solved. These releases will be made public. They will be posted to the web pages in a category separate from Release Candidates and Releases. Again, software that meets the Beta standard is designed for knowledgeable users.

10.1.4. Release Candidate

The only difference between software that meets the Release Candidate standard and software that meets the Release standard will be the amount of testing and the delivery mechanism. Release Candidates will be fully supported and posted to the web pages but not burned to CDs - they will be designed for use by new users.

10.1.5. Release

Software will only meet the Release standard when it is burned to CD and shipped with new camera systems. Similar to Release Candidate users, users of Release software can expect fully functional libraries, examples and installation scripts.

Appendix B: Glossary

Term	Definition
1394a	An Institute of Electrical and Electronics Engineers (IEEE) interface standard capable of transferring data at a rate of 400Mbit per second.
1394b	An IEEE interface standard capable of transferring data at a rate of 400Mbit per second.
Absolute Values	Real-world values, such as milliseconds (ms), decibels (dB) or percent (%). Using the absolute values is easier and more efficient than applying complex conversion formulas to integer values.
Analog-to-Digital Converter	Often abbreviated as ADC or A/D converted, it is a device that converts a voltage to a digital number.
API	Application Programming Interface. Essentially a library of software functions.
Asynchronous Transmission	The transfer of image data from the camera to the PC that is regulated by an external signal, such as a trigger. Asynchronous transfers do not guarantee when data will be transferred. However, they do guarantee that data will arrive as sent. Asynchronous transfers may be used when data integrity is a higher priority than speed. An example might be an image data transfer to a printer, where speed is less critical than getting the image pixels correct. Asynchronous transfers are initiated from a single node, designated the 'requestor', to or from the address space of another node, designated the 'responder'. Asynchronous requests are packet-based. The requestor node generates a request packet that the 1394 bus sends to the responder node. The responder node is responsible for handling the request packet and creating a response packet that is sent back to the requestor node to complete a single transfer. There are three types of 1394 asynchronous transfers: Read, Write and Lock.
BPP	Bytes per packet. An image is broken into multiple packets of data, which are then streamed isochronously to the host system. Each packet is made up of multiple bytes of data.
Brightness (%)	This is essentially the level of black in an image. A high brightness will result in a low amount of black in the image. In the absence of noise, the minimum pixel value in an image acquired with a brightness setting of 1% should be 1% of the A/D converter's minimum value.
Config ROM	Configuration read-only memory. A section of memory dedicated to describing low-level device characteristics such as Model and Vendor ID, IEEE-1394 version compliance, base address quadlet offsets, etc.
Color Processing	Also known as 'interpolation,' an algorithm for converting raw Bayer-tiled image data into full color images. Depending on camera model, this process takes place either on-camera or on the PC. For more information, refer to Knowledge Base Article 33.
DCAM	Abbreviation for the *IIDC 1394-based Digital Camera (DCAM) Specification*, which is the standard used for building FireWire-based cameras.
Dynamic Range	The difference between the maximum and minimum amounts of light that a sensor can measure. This is bounded on the upper end by the maximum charge that any pixel can contain (sensor full well depth) and at the lower end by the small charge that every sensor spontaneously generates (read noise).
Exposure (EV)	This is the average intensity of the image. It will use other available (non-manually adjustable) controls to adjust the image.
Firmware	Programming that is inserted into programmable read-only memory, thus becoming a permanent part of a computing device. Firmware is created and tested like software and can be loaded onto the camera.
Format_7	Encompasses partial or custom image video formats and modes, such as region of interest of pixel binned modes. Format_7 modes and frame rates are defined by the camera manufacturer, as opposed to the DCAM specification.
FPS	Frames Per Second.
Frame Rate	Often defined in terms of number of frames per second (FPS) or frequency (Hz). This is the speed at which the camera is streaming images to the host system. It basically defines the interval between consecutive image transfers.
Gain (dB)	The amount of amplification that is applied to a pixel by the A/D converter. An increase in gain can result in a brighter image and an increase in noise.
Gamma	Gamma defines the function between incoming light level and output picture level. Gamma can also be useful in emphasizing details in the darkest and/or brightest regions

	of the image.
GPIO	General Purpose Input/Output.
Grabbing Images	A commonly-used phrase to refer to the process of enabling isochronous transfers on a camera, which allows image data to be streamed from the camera to the host system.
Hz	Hertz. A unit of frequency; one Hertz has a periodic interval of one second. Often used interchangeably with FPS as a measure of frame rate.
Isochronous Transmission	The transfer of image data from the camera to the PC in a continual stream that is regulated by an internal clock. Isochronous transfers on the 1394 bus guarantee timely delivery of data. Specifically, isochronous transfers are scheduled by the bus so that they occur once every 125µs. Each 125µs timeslot on the bus is called a frame. Isochronous transfers, unlike asynchronous transfers, do not guarantee the integrity of data through a transfer. No response packet is sent for an isochronous transfer. Isochronous transfers are useful for situations that require a constant data rate but not necessarily data integrity. Examples include video or audio data transfers. Isochronous transfers on the 1394 bus do not target a specific node. Isochronous transfers are broadcast transfers which use channel numbers to determine destination.
Lookup Table	A matrix of gamma functions for each color value of the current pixel encoding format.
Node	An addressable device attached to a bus. Although multiple nodes may be present within the same physical enclosure (module), each has its own bus interface and address space and may be reset independently of the others.
Node ID	A 16-bit number that uniquely differentiates a node from all other nodes within a group of interconnected buses. Although the structure of the node ID is bus-dependent, it usually consists of a bus ID portion and a local ID portion. The most significant bits of the node ID are the same for all nodes on the same bus; this is the bus ID. The least-significant bits of the node ID are unique for each node on the same bus; this is called the local ID. The local ID may be assigned as a consequence of bus initialization.
One Push	For use when a control is in manual adjust mode, One Push sets a parameter to an auto-adjusted value, then returns the control to manual adjust mode.
PHY	Physical layer. Each 1394 PHY provides the interface to the 1394 bus and performs key functions in the communications process, such as bus configuration, speed signaling and detecting transfer speed, 1394 bus control arbitration, and others.
Pan	A mechanism to horizontally move the current portion of the sensor that is being imaged. In stereo and spherical cameras, Pan controls which individual sensors transmit images.
Pixel Clock	The rate at which the sensor outputs voltage signals in each pixel from the optical input.
Pixel Format	The encoding scheme by which color or greyscale images are produced from raw image data.
Quadlet	A 4 byte (32-bit) value.
Quadlet Offset	The number of quadlets separating a base address and the desired CSR address. For example, if the base address is 0xFFFFF0F00000 and the value of the quadlet offset is 0x100, then the actual address offset is 0x400 and the actual adress 0xFFFFF0F00400.
Register	A term used to describe quadlet-aligned addresses that may be read or written by bus transactions.
Saturation	This is how far a color is from a gray image of the same intensity. For example, red is highly saturated, whereas a pale pink is not.
SDK	Software Development Kit
Sharpness	This works by filtering the image to reduce blurred edges.
Shutter	A mechanism to control the length of time the sensor is exposed to light from the image field for each frame. In milliseconds (ms), it is the amount of time that the shutter stays open, also known as the *exposure* or *integration* time. The shutter time defines the start and end point of when light falls on the imaging sensor. At the end of the exposure period, all charges are simultaneously transferred to light-shielded areas of the sensor. The charges are then shifted out of the light shielded areas of the sensor and read out.
Signal-to-Noise Ratio (dB)	The difference between the ideal signal that you expect and the real-world signal that you actually see is usually called noise. The relationship between signal and noise is called the signal-to-nose ratio (SNR). SNR is calculated using the general methodology outlined in Knowledge Base Article 142.
SXGA	1280x1024 pixel resolution
Tilt	A mechanism to vertically move the current portion of the sensor that is being imaged.
Trigger	A signal to which the acquisition of images by the camera is synchronized. Triggers can be from an outside electrical source (external) or software-generated (internal).
UXGA	1600x1200 pixel resolution
VGA	640x480 pixel resolution
White Balance	A method to enable white areas of an image to appear correctly by modifying the gain of red and blue channels relative to the green channel. White balance can be used to accommodate differing lighting conditions.

XVGA	1024x768 pixel resolution

Appendix C: Memory Channel Registers

Register Name	Offset
CURRENT_FRAME_RATE	600h
CURRENT_VIDEO_MODE	604h
CURRENT_VIDEO_FORMAT	608h
CAMERA_POWER	610h
CUR_SAVE_CH	620h
BRIGHTNESS	800h
AUTO_EXPOSURE	804h
SHARPNESS	808h
WHITE_BALANCE	80Ch
HUE	810h
SATURATION	814h
GAMMA	818h
SHUTTER	81Ch
GAIN	820h
IRIS	824h
FOCUS	828h
TRIGGER_MODE	830h
TRIGGER_DELAY	834h
FRAME_RATE	83Ch
PAN	884h
TILT	888h
ABS_VAL_AUTO_EXPOSURE	908h
ABS_VAL_SHUTTER	918h
ABS_VAL_GAIN	928h
ABS_VAL_BRIGHTNESS	938h
ABS_VAL_GAMMA	948h
ABS_VAL_TRIGGER_DELAY	958h
ABS_VAL_FRAME_RATE	968h
IMAGE_DATA_FORMAT	1048h
AUTO_EXPOSURE_RANGE	1088h
AUTO_SHUTTER_RANGE	1098h
AUTO_GAIN_RANGE	10A0h
GPIO_XTRA	1104h
SHUTTER_DELAY	1108h
GPIO_STRPAT_CTRL	110Ch
GPIO_CTRL_PIN_x	1110h, 1120h, 1130h, 1140h
GPIO_XTRA_PIN_x	1114h, 1124h, 1134h, 1144h
GPIO_STRPAT_MASK_PIN_x	1118h, 1128h, 1138h, 1148h
FRAME_INFO	12F8h
FORMAT_7_IMAGE_POSITION	008h
FORMAT_7_IMAGE_SIZE	00Ch
FORMAT_7_COLOR_CODING_ID	010h
FORMAT_7_BYTE_PER_PACKET	044h

Appendix D: Revision History

Revision	Date	Notes
2.1	August 2, 2007	• Added Revision History to appendix • Renamed manual to Point Grey Digital Camera Register Reference • Section 2.13 Advanced Registers additions: TIME_FROM_INITIALIZE 12E0h, TIME_FROM_BUS_RESET 12E4, HDR 1800h – 1484h, LED_CTRL 1A14h, PIXEL_DEFECT_CTRL 1A60h, FORMAT_7_RESIZE_INQ 1AC8 • Section 8 Trigger Modes additions: Trigger_Mode_15 • Removed *Feature Availability* tables where register implements *Presence_Inq* field, or where a separate feature inquiry register is present (e.g. BRIGHTNESS_INQUIRY) • Added *Camera Notes* tables to highlight non-standard implementation of specific features
2.2	November 15, 2007	• Updated section 2.13.36 FRAME_INFO for the FFMV (Timestamp only)

2.3	October 10, 2008	• Added section 2.13.36. IMAGE_RETRANSMIT 12E8h
		• Updated section 2.13.37 FRAME_INFO 12F8h.
		    • For the Firefly MV, this register contains information only about timestamp and GPIO pin state.
		    • Flea2 can embed Region of Interest (ROI) information using this register.
		• Section 2.13.39 HDR: Updated the names of offsets 1880h and 1884h.
		• Updated Section 10 with new company address and phone numbers.

2.4	January 9, 2009	• Added FL2G and CMLN cameras to section 1.1 Scope and Applicable Cameras. • Updated section 2.13.50 MAIN_BOARD_INFO: 1F24h with values for the FL2G and Chameleon cameras. • Added the CMLN camera to the Feature Availability tables of several registers. • Updated section 2.13.37 FRAME_INFO 12F8h. Changed ‘Shutter CSR’ to ‘Shutter Value.’ CSR value is not embedded; shutter value is measured directly from the shutter duration. Added address of CYCLE_TIME register and added index reference.
2.5	March 2, 2009	• Updated FL2G model information in Section 2.13.50: MAIN_BOARD_INFO: 1F24h. • Updated Appendix B: Glossary.

2.6	June 1, 2009	• Section 4.1.5 GPIO_Mode_4: Added that if bits 16-23 of **GPIO_CTRL_PIN_x Register in GPIO_Mode_4** are set to 0xFF (infinite), they must be manually set to 0x00 before writing a new value. • Section 4.1.5 GPIO_Mode_4:Clarified that the pin configured to output a PWM signal (PWM pin) remains in the same state at the time the 'enable pin' is disabled. • Clarified in Section 2.13.37 (FRAME_INFO 12F8h) that embedded image values are those in effect at the end of shutter integration. • Section 2.13.11 GPIO_CONTROL 1100h: Added that opto-isolated input pins with pull-up resistors report a value of '1' when unconnected. • Section 2.13.6 IMAGE_DATA_FORMAT 1048h: Under *Bayer_Mono_Ctrl* parameter, added that in some cases, enabling raw Bayer output in half-width, half-height image size provides a raw Bayer region of interest of 800x600, centered within the larger pixel array, which has an effect on the field of view.
2.7	August 28, 2009	• Section 4.1.5: Clarified bits 24 and 28 are Reserved in GPIO_CTRL_PIN_x register when camera operates in GPIO_Mode_4. • Section 2.13.37: FRAME_INFO: 12F8h: Clarified Firefly MV embedded image information, by model. • Section 1.3.2 Format: Clarified that bit 0 is always the most significant bit of the register value. • Section 8.1.6 Trigger_Mode_14 ("Overlapped Exposure / Readout Mode"): Added that the trigger must be armed; otherwise it is dropped. • Section 2.11 Absolute Value CSR Registers: Added clarification about why a relative value does not always translate to the same absolute value.
2.8	November 24, 2010	• Section 2.9.12 SOFTWARE_TRIGGER: 62Ch (v1.31): Clarified that bit 0 automatically resets to 0 in all trigger modes except Trigger_Mode = 3. • Section 2.13.37 FRAME_INFO: 12F8h: Added FL2G support for embedded information of ROI position.

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